Date: Apr. 11, 2013

RENESAS TECHNICAL UPDATE

1753, Shimonumabe, Nakahara-ku, Kawasaki-shi, Kanagawa 211-8668 Japan
Renesas Electronics Corporation

Product Category	MPU/MCU		Document No.	TN-R8C-A031A/E	Rev.	1.00
Title	Note on Serial Interface (UART2)		Information Category	Technical Notification		
Applicable Products	See below	Lot No. __	Reference Document			

The information in this Technical Update applies to the products below.

1. Applicable products

R8C/32A Group, R8C/32C Group, R8C/32D Group, R8C/32M Group

R8C/33A Group, R8C/33C Group, R8C/33D Group, R8C/33M Group

R8C/34C Group, R8C/34M Group

R8C/35A Group, R8C/35C Group, R8C/35D Group, R8C/35M Group

R8C/36A Group, R8C/36C Group, R8C/36M Group

R8C/38A Group, R8C/38C Group, R8C/38M Group

R8C/3GA Group, R8C/3GC Group, R8C/3GD Group, R8C/3GM Group

R8C/3JA Group, R8C/3JC Group, R8C/3JM Group

R8C/33T Group, R8C/3JT Group, R8C/3NT Group

R8C/34K Group, R8C/34U Group, R8C/3MK Group, R8C/3MU Group

R8C/32G Group, R8C/32H Group, R8C/33G Group, R8C/33H Group

R8C/34P Group, R8C/34R Group

R8C/34E Group, R8C/34F Group, R8C/34G Group, R8C/34H Group

R8C/36E Group, R8C/36F Group, R8C/36G Group, R8C/36H Group

R8C/38E Group, R8C/38F Group, R8C/38G Group, R8C/38H Group

R8C/34W Group, R8C/34X Group, R8C/34Y Group, R8C/34Z Group

R8C/36W Group, R8C/36X Group, R8C/36Y Group, R8C/36Z Group

R8C/38W Group, R8C/38X Group, R8C/38Y Group, R8C/38Z Group

R8C/L35A Group, R8C/L35B Group, R8C/L35C Group, R8C/L35M Group

R8C/L36A Group, R8C/L36B Group, R8C/L36 Group, R8C/L36M Group

R8C/L38A Group, R8C/L38B Group, R8C/L38C Group, R8C/L38M Group

R8C/L3AA Group, R8C/L3AB Group, R8C/L3AC Group, R8C/L3AM Group

R8C/LA6A Group, R8C/LA8A Group

2. Notes when transmission/reception of the serial interface (UART2) starts

(1) Condition

When using the clock synchronous serial I/O mode (internal clock selected) or clock asynchronous serial I/O (UART) mode and setting 00h to the U2BRG register.

(2) Notes

Immediately after the U2BRG register is set to 00h, the start of data transmission/reception may be delayed 256 cycles of the U2BRG register count source.

The following occur due to the delay in the data transmission/reception being started:

- When transmitting/receiving in clock synchronous serial I/O mode (internal clock selected) and transmitting clock asynchronous serial I/O (UART) mode

  The timing when the TI bit in the U2C1 register becomes 1 (no data in the U2TB register) and the TXEPT bit in the U2C0 register becomes 0 (data in the transmit register (mid-transmission) is delayed.
- When receiving in clock asynchronous serial I/O (UART) mode

  The start bit detection timing is delayed, the transfer clock is not generated even though the falling edge of the start bit is detected, and the receive operation does not start.

(3) Operation

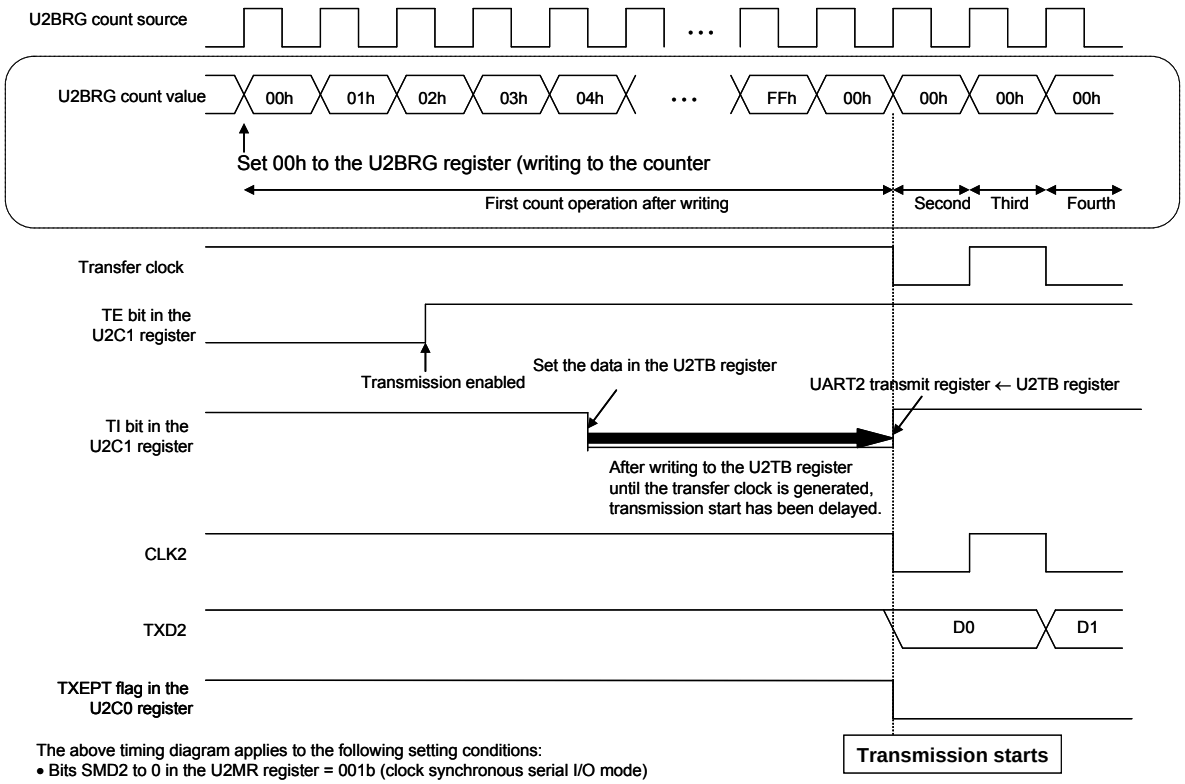
When setting 00h to the U2BRG register, the first count operation is performed up to FFh. During this period, data transmission/reception does not start because the transfer clock is not generated.

However, only the first count operation immediately after writing to the U2BRG register is performed and count operation with the setting value is performed after second count operation.

When setting 00h to the U2BRG register, set the U2BRG register before 256 cycles or more of transmission/reception start.

The timing diagram of when an internal clock is selected and transmitted is shown below.

Operation example when setting 00h to the U2BRG register



The above timing diagram applies to the following setting conditions:
- Bits SMD2 to 0 in the U2MR register = 001b (clock synchronous serial I/O mode)
- CKDIR bit in the U2MR register = 0 (internal clock selected)
- CKPOL bit in the U2C0 register = 0 (Transmit data output at the falling edge of the transfer clock and receive data input at the rising edge of the transfer clock.)
- UFORM bit in the U2C0 register = 0 (LSB first)

3. Notes when switching the serial logic data of the serial interface (UART2)

(1) Condition

When using clock asynchronous serial I/O (UART) mode and the U2LCH bit in the U2C1 register to switch the serial data logic.

(2) Note

When setting 1 (inverted) to the U2LCH bit, the only values of D0 to D7 are inverted and the parity bit is not inverted.

The serial data logic figure described in the User's Manual: Hardware has been revised.

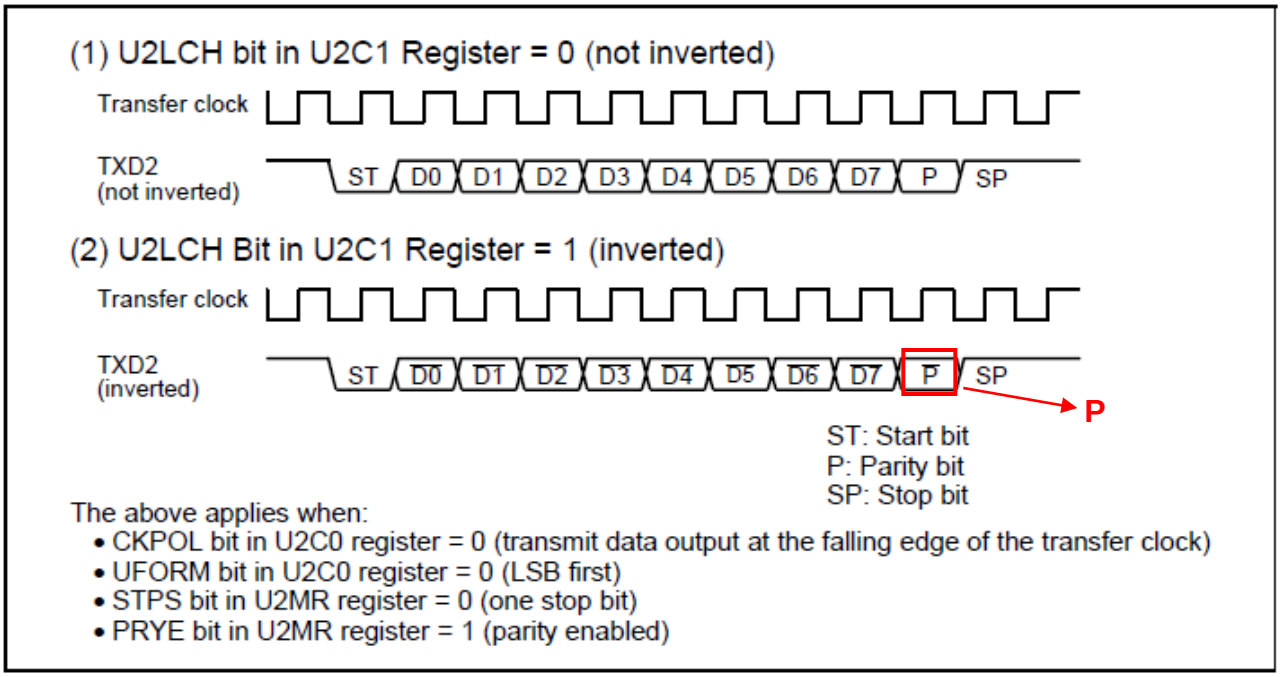


Figure Serial Data Logic Switching