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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-SY*-A031B/E	Rev.	2.00
Title	Functional Limitation of the Ethernet Peripheral Interface		Information Category	Technical Notification		
Applicable Product	Renesas Synergy™ S5D5 MCU Group	Lot No. All lots	Reference Document	S5D5 MCU Group User's Manual Rev.1.10		

The Ethernet DMA Controller (EDMAC) in the S5D5 MCU Group exhibits improper padding of the received Ethernet Packets resulting in behavior that is not compliant with the specification of section 30.2.17 of the S5D5 MCU Group User's Manual Rev.1.10.

Renesas is planning to revise the S5D5 mask set so that this limitation will be no longer be present. Table 1 below summarizes the old part numbers and their updated counterparts. The new devices will be available by July, 2019.

Renesas provided a software workaround in the Synergy Software Package (SSP) that addresses the EDMAC limitation at the expense of introducing a small CPU overhead. This Silicon fix will eliminate the need of a software patch and will remove the CPU overhead. The SSP workaround code was designed to only run if specific mask revision is detected. Since the Silicon fix is coming with a different mask revision, no software modification will be required for the applications to take advantage of the enhanced EDMAC operation.

Table 1. Orderable part numbers

Product part number	Orderable part number with EDMAC limitation (current)	Orderable part number without EDMAC limitation (new)	Note
R7FS5D57C2A01CLK	R7FS5D57C2A01CLK#AC0	R7FS5D57C2A01CLK#AC1	Renesas will switch to mass production of devices with the new part numbers by July 2019
R7FS5D57C3A01CFB	R7FS5D57C3A01CFB#AA0	R7FS5D57C3A01CFB#AA1	
R7FS5D57C3A01CFP	R7FS5D57C3A01CFP#AA0	R7FS5D57C3A01CFP#AA1	
R7FS5D57A2A01CLK	R7FS5D57A2A01CLK#AC0	R7FS5D57A2A01CLK#AC1	
R7FS5D57A3A01CFB	R7FS5D57A3A01CFB#AA0	R7FS5D57A3A01CFB#AA1	
R7FS5D57A3A01CFP	R7FS5D57A3A01CFP#AA0	R7FS5D57A3A01CFP#AA1	

Below is the detailed description of the EDMAC issue announced previously with document TN-SY*-A031A/E Rev.1.00.

The Ethernet DMA Controller (EDMAC) of MCUs in the S5D5 Group exhibit improper padding of received Ethernet packets resulting in behavior that is not compliant with the specification of section 30.2.17 of the S5D5 MCU Group User's Manual. There is a software solution available to correct this behavior.

The EDMAC Padding Size control field, PADS[1:0], within the Receive Data Padding Insert Register (RPADIR) control how many bytes are to be inserted automatically in the data field of each received Ethernet packet. The count of bytes to be inserted can be specified in the PADS[1:0] field as 0, 1, 2, or 3 inserted bytes.

If the value of the PADS[1:0] field is set to any value other than 0, incorrect behavior occurs. In this scenario, the received packet is not processed completely by the EDMAC, such that the last 1 or 2 bytes are not transferred as expected. As a result, the upper layer software reports a checksum error and rejects the packet. The EDMAC operates properly when the padding is set to 0 bytes (disabled). The problem appears only when Ethernet packets are received with a size equal to 4*N + 1 and 4*N + 2, where N is a natural number. For this reason, some applications may not report errors if their host sends Ethernet packets

formatted such that their length is outside the stated limitation.

The releases of the Synergy Software Package (SSP) starting with version 1.3.0, and up to and including version 1.4.0, version 1.5.0, set the value of the PADS[1:0] field to 2 (2 inserted bytes), which enables the incorrect padding behavior in hardware.

Renesas provides a software-based workaround by using a version of the SSP Ethernet driver (sf_el_nx) that sets the PADS[1:0] field to a value of 0 (no hardware data padding), and executes the data padding function in software.

Please contact your Renesas Sales person to change the orderable parts number.

Technical Support:

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