

# RENESAS TECHNICAL UPDATE

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Product Category	MPU & MCU	Document No.	TN-16C-A240A/E	Rev.	1.00
Title	Deletion of Specifications and Errata for R32C/118A Group User's Manual: Hardware		Information Category	Technical Notification	
Applicable Product	R32C/118A Group	Lot No.	Reference Document	R32C/118A Group User's Manual: Hardware Rev. 1.10 (R01UH0215EJ0110)	

This document describes deletion of specifications and errata for the R32C/118A Group User's Manual: Hardware, Rev. 1.10.

## 1. Deletion of Specifications

Development of products on the planning phase in Table 1.5 is discontinued. Accordingly, specifications for the N version are deleted from the Operating Temperature in Tables 1.2, 1.4, and 29.2, and the Temperature Code in Figure 1.1.

## 2. Errata

The corrections are indicated in red in the list below.

- Page 1 of 639, expression "I<sup>2</sup>C" in line 9 of 1.1 is modified as follows:  
"I<sup>2</sup>C-bus interface"
- Page 185 of 639, description in lines 9 and 10 of chapter 12 is modified as follows:  
"One divides the on-chip oscillator clock by 1, 2, 4 or 8; the other divides the peripheral bus clock by 16 or 128."
- Page 212 of 639, descriptions in Figure 14.5 is modified as follows:  
"The figure below applies under the following conditions:  
memory-to-memory transfer; incrementing source address; non-incrementing destination address; single transfer mode; transfer complete interrupt generated after 2 transfers (transfer counter = 2); no chain transfer"
- Page 219 of 639, description of the third bullet point of 16.1 is corrected as follows:  
"One-shot timer mode: The timer outputs a pulse after a trigger input until the counter reaches 0000h"
- Page 224 of 639, typos "b2 b3", "b4 b5", and "b6 b7" in Figure 16.9 are corrected as follows:  
"b3 b2", "b5 b4", and "b7 b6"
- Page 231 of 639, typo "INT" in Note 1 of Figures 16.13 and 16.14 is corrected as follows:  
"INT2"

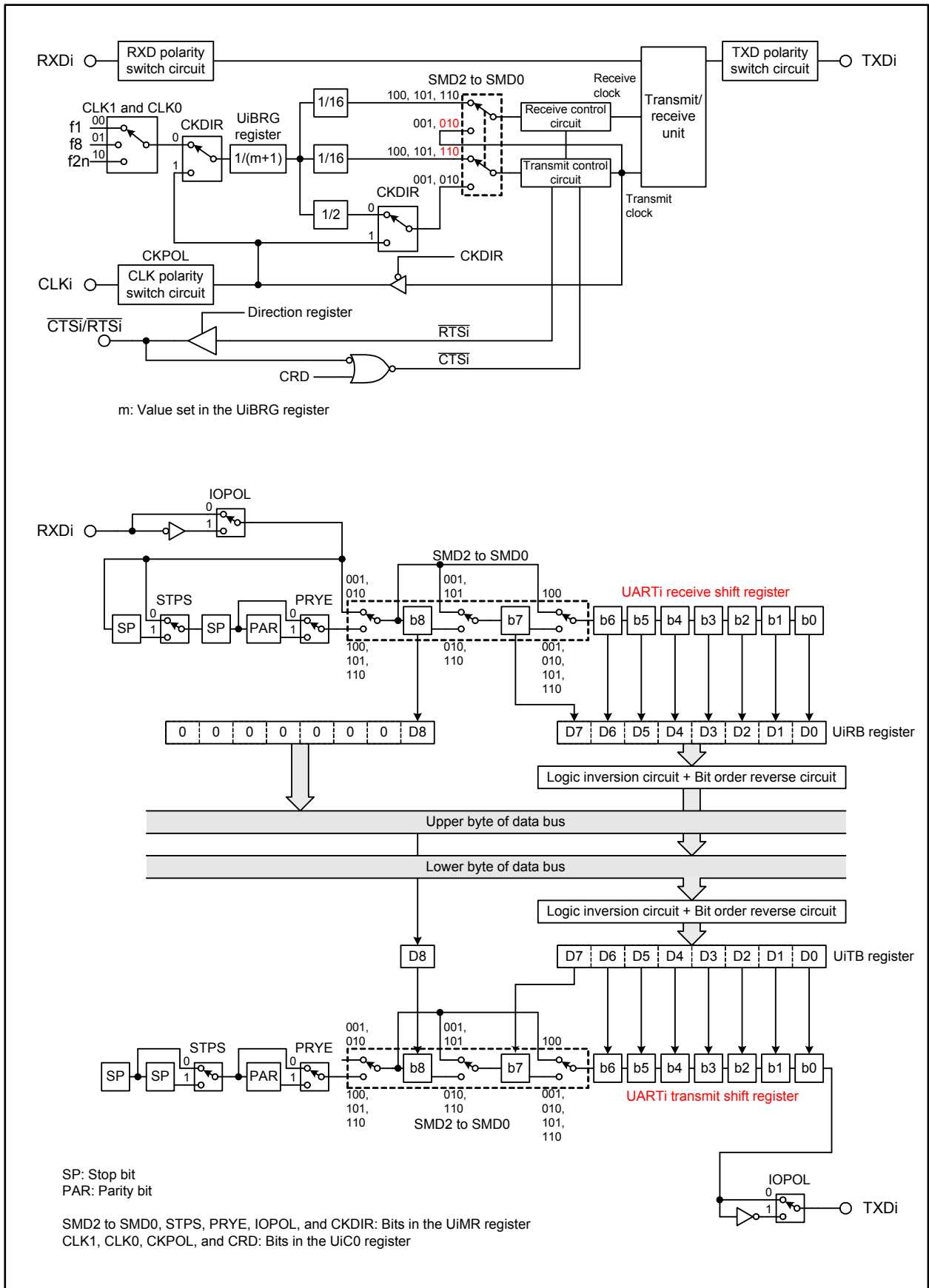
- Page 235 of 639, bit symbol “TAiS” in the Function column for the MR2 bit in Figure 16.16 is corrected as follows:

“TAiOS”

- Pages 268 to 319 of 639, terms in chapter 18 are corrected as follows:

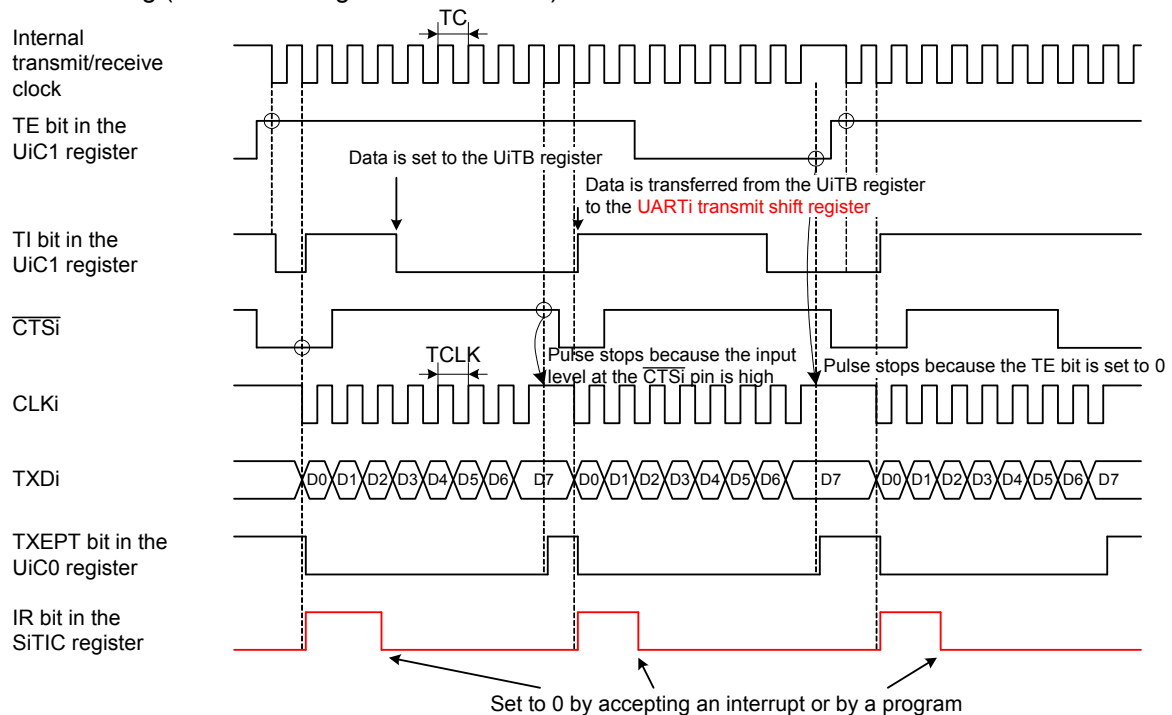
Before Correction	After Correction	Figure/Table/Section Number
receive register	receive shift register	Figures 18.1, 18.2, 18.22, 18.28 Tables 18.2, 18.5, 18.11, 18.14 Section 18.3.8
transmit register	transmit shift register	Figures 18.1, 18.2, 18.21, 18.22, 18.26, 18.27 Tables 18.2 (2 corrections), 18.3, 18.4, 18.5 (2 corrections), 18.6, 18.7, 18.10, 18.14 (2 corrections), 18.15 Section 18.3.8 (3 corrections)
SS function	slave select function	Figure 18.13 (3 corrections) Table 18.14 Sections 18.4.1, 18.4.1.1, 18.4.1.2
BRG	UiBRG	Table 18.8 (3 corrections)
restart condition	repeated START condition	Figure 18.14 Table 18.10 Sections 18.3.2 (2 corrections), 18.5.3

•Page 269 of 639, positions of “010” for bits SMD2 to SMD0 in Figure 18.1 are corrected as follows:



- Page 279 of 639, expression “baud rate generator count source” in the function of bits DL0 to DL2 in Figure 18.13 is corrected as follows:  
 “count source for the UiBRG register”
- Pages 286, 287, 294, 295, 304, 314 of 639, descriptions in Function of the UiBRG register in Tables 18.3, 18.4, 18.6, 18.7, 18.10, and 18.15 are modified as follows:  
 “Set the divide ratio according to the bit rate”
- Pages 287, 295 of 639, description for (b7 to b4) to registers UiC1 and U78CON in Tables 18.4 and 18.7 is added as follows:  
 “(b7 to b4) Set the bits to 0000b”
- Page 288 of 639, waveform of the IR bit in Figure 18.21 is corrected as follows:

Transmit timing (when selecting an internal clock)



This figure applies under the following conditions:

- The CKDIR bit in the UiMR register is 0 (internal clock).
- The CRD bit in the UiC0 register is 0 (CTS function enabled).
- The CKPOL bit in the UiC0 register is 0 (output transmit data on the falling edge of the transmit/receive clock).
- The UiIRS bit in registers UiC1, U78CON, and U910CON is 0 (an interrupt request is generated when the transmit buffer is empty).

$$TC = TCLK = 2(m + 1)/fx$$

fx: UiBRG count source frequency (f1, f8, or f2n)

m: Value setting in the UiBRG register

•Page 290 of 639, descriptions in 18.1.1 are modified as follows:

“When a transmit/receive error occurs in synchronous serial interface mode, follow the procedures below to perform a reset:

- (1) Set the TE bit to 0 (transmission disabled) and the RE bit to 0 (reception disabled) in the UiC1 register (i = 0 to 10).
- (2) Set bits SMD2 to SMD0 in the UiMR register to 000b (serial interface disabled).
- (3) Set again bits SMD2 to SMD0 to either of 001b, 101b, or 110b.
- (4) Set the TE bit to 1 (transmission enabled) and the RE bit to 1 (reception enabled) in the UiC1 register.”

•Page 292 of 639, the following description is added to line 3 of 18.1.6:

“after the last bit is transmitted”

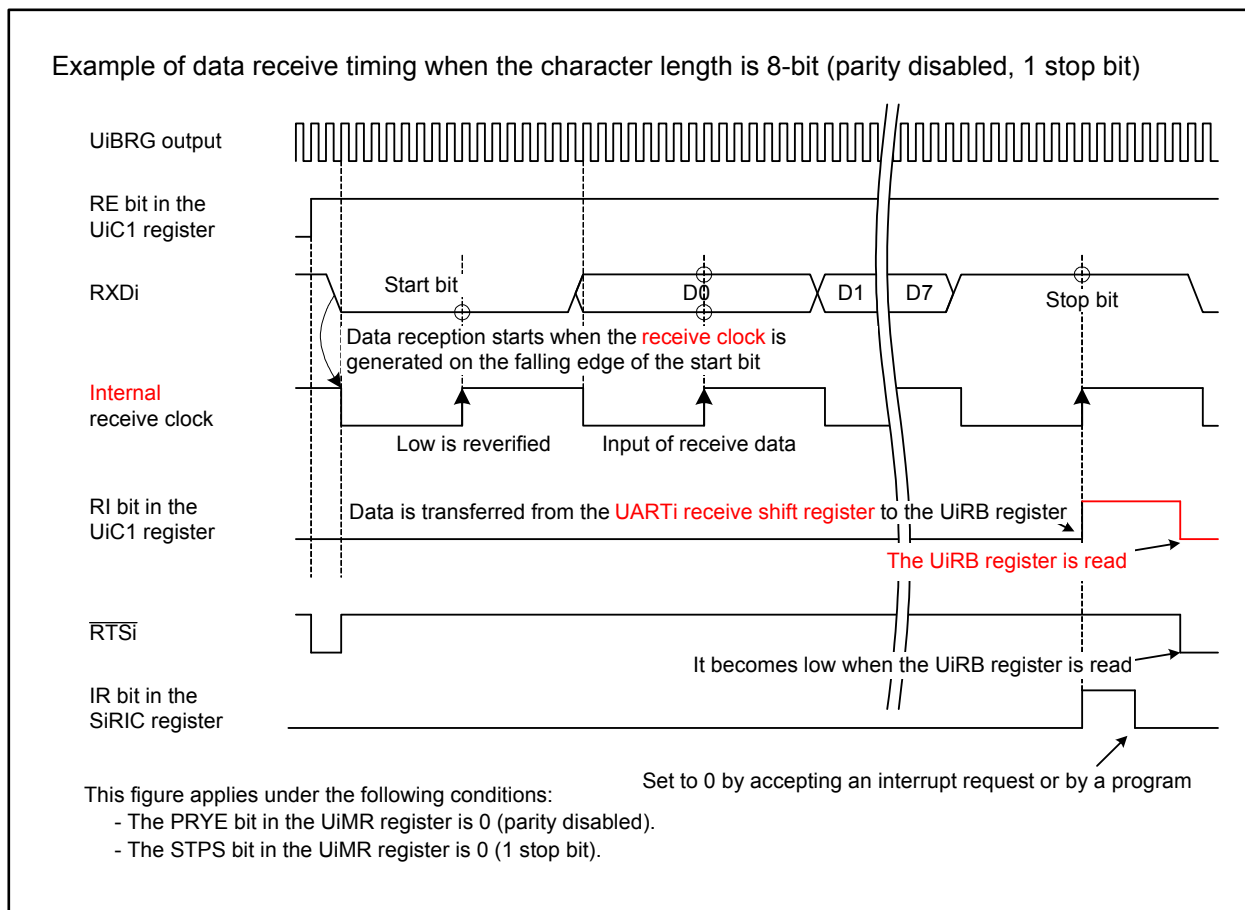
•Page 295 of 639, description for (b7) to the UiMR register in Table 18.7 is added as follows:

“(b7) Set the bit to 0”

•Pages 296, 297 of 639, description “Internal transmit/receive clock” in Figures 18.26 and 18.27 is corrected as follows:

“Internal transmit clock”

•Page 298 of 639, Figure 18.28 is corrected as follows:



•Page 299 of 639, descriptions in 18.2.2 are modified as follows:

“When a transmit/receive error occurs in UART mode, follow the procedure below to perform a reset:

- (1) Set the TE bit to 0 (transmission disabled) and the RE bit to 0 (reception disabled) in the UiC1 register (i = 0 to 10).
- (2) Set bits SMD2 to SMD0 in the UiMR register to 000b (serial interface disabled).
- (3) Set again bits SMD2 to SMD0 to either of 001b, 101b, or 110b.
- (4) Set the TE bit to 1 (transmission enabled) and the RE bit to 1 (reception enabled) in the UiC1 register.

•Page 302 of 639, descriptions for the Interrupt request generating timing in Table 18.9 are modified as follows:

Interrupt request generating timing	<ul style="list-style-type: none"> <li>• START condition is detected</li> <li>• STOP condition is detected</li> <li>• ACK (acknowledge) is detected, or reception is completed</li> <li>• NACK (not-acknowledge) is detected, or transmission is completed</li> </ul>
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•Page 304 of 639, description for (b6 to b4) to the UiMR register in Table 18.10 is added as follows:

“(b6 to b4) Set the bits to 000b”

•Page 319 of 639, description for suspending and resuming communication is added to 18.5.4 as follows:

**“18.5.4 Reset Procedure or Suspend/Resume Procedure**

Operations which result in communication errors such as rewriting function select registers during transmission/reception should not be performed. Follow the procedure below to reset the internal circuit once the communication error occurs in the following cases: when the operation above is performed by a receiver or transmitter or when a bit slip is caused by noise.

Also follow the procedure below when suspending and resuming communication in an emergency.”

•Page 432 of 639, description for Mode transition for bus-off recovery in Table 26.1 is modified as follows:

Mode transition for bus-off recovery	<p>Mode after recovering from the bus-off state can be selected:</p> <ul style="list-style-type: none"> <li>• ISO 11898-1 compliant</li> <li>• Automatic transition to CAN halt mode immediately after becoming bus-off.</li> <li>• Automatic transition to CAN halt mode when recovering from the bus-off state.</li> <li>• Transition to CAN halt mode by a program</li> <li>• Transition to the error-active state by a program</li> </ul>
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•Page 433 of 639, description for Mode transition for Error state monitoring in Table 26.2 is modified as follows:

Error state monitoring	<ul style="list-style-type: none"> <li>• CAN bus errors (stuff error, form error, ACK error, CRC error, bit error, and ACK delimiter error) can be monitored</li> <li>• Transition to error states can be detected (error-warning, error-passive, bus-off, and bus-off recovery)</li> <li>• The error counters can be read</li> </ul>
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•Page 436 of 639, description for the BOM bit in Figure 26.2 is modified as follows:

“00: Normal mode

(ISO 11898-1 compliant)

01: Automatically enters CAN halt mode immediately after becoming bus-off

10: Automatically enters CAN halt mode when recovering from the bus-off state

11: Enters CAN halt mode (during bus-off period) by a program request”

- Page 440 of 639, the following description is added to 26.1.2:  
 “The CiCLKR register is used to select the clock source of the CAN communication clock for the protocol controller. Operation in the CAN module is always synchronized with the peripheral bus clock.”
- Page 443 of 639, description in 26.1.4 is modified as follows:  
 “Each channel has eight mask registers. Refer to 26.5 “Acceptance Filtering and Masking Function” for details on the mask registers.”
- Page 447 of 639, description is added to 26.1.7 as follows:  
 “Each channel has 32 mailboxes. Each mailbox is 16 bytes and can be set for transmission or for reception individually by the CiMCTLj register.  
 Table 26.4 lists the CANi mailbox memory mapping, and Table 26.5 lists the CAN data frame structure. The reset value of the CANi mailbox is undefined.”
- Page 472 of 639, descriptions for bits BOEIF and BORIF are modified in Figure 26.25 as follows:

Bit Symbol	Bit Name	Function	RW
BOEIF	Bus-off Detect Flag	0:CAN module is not bus-off 1:CAN module became bus-off	RW
BORIF	Bus-off Recovery Detect Flag	0:CAN module does not recover from the bus-off state 1:CAN module recovered from the bus-off state normally	RW

- Page 474 of 639, description in 26.1.20.8 is corrected as follows (refer to TN-16C-A230A/E):  
 “The BLIF bit becomes 1 if 32 consecutive dominant bits are detected on the CAN bus while the CAN module is in CAN operation mode.  
 After the BLIF bit becomes 1, bus lock can be detected again after either of the following conditions is satisfied:
  - After this bit is set to 0 from 1, recessive bits are detected (bus lock is resolved).
  - After this bit is set to 0 from 1, the CAN module enters CAN reset mode and then enters CAN operation mode again (internal reset).”
- Page 483 of 639, Note 1 in Figure 26.34 is corrected and Note 3 is added as follows (refer to TN-16C-A230A/E):  
 “Notes:
  1. The transition timing from the bus-off state to CAN halt mode depends on the setting of the BOM bit.
    - When the BOM bit is 01b, the CAN module enters CAN Halt mode immediately after becoming bus-off.
    - When the BOM bit is 10b, the CAN module enters CAN Halt mode when recovering from the bus-off state.
    - When the BOM bit is 11b, the CAN module enters CAN Halt mode when setting the CANM bit to 10b (CAN halt mode).
  2. Write only to the SLPM bit to exit/set CAN sleep mode.
  3. The CAN module does not enter CAN Halt mode while the CAN bus is locked in dominant state. Enter CAN reset mode instead.”

- Page 485 of 639, Note 2 is added to the CAN halt mode row in the Transmitter column of Table 26.9. Note 2, Note 3, and Note 4 is corrected as follows (refer to TN-16C-A230A/E):

Notes:

1. If several messages are requested to be transmitted, mode transition occurs after the completion of the first message transmission. When CAN reset mode is being requested during suspend transmission, mode transition occurs when the bus is idle, the next transmission ends, or the CAN module becomes a receiver.
2. If the CAN bus is locked in dominant state, the program can detect this state by monitoring the BLIF bit in the CiEIFR register. **The CAN module does not enter CAN Halt mode while the CAN bus is locked in dominant state. Enter CAN reset mode instead.**
3. If a CAN bus error occurs during reception after CAN halt mode is requested, the CAN module enters CAN halt mode. **However, the CAN module does not enter CAN Halt mode when the CAN bus is locked in dominant state.**
4. If a CAN bus error or arbitration lost occurs during transmission after CAN reset mode or CAN halt mode is requested, the CAN module enters the requested operating mode. **However, the CAN module does not enter CAN Halt mode when the CAN bus is locked in dominant state.**

- Page 499 of 639, bit symbol "SENDTDATA" in (4) of 26.6.2 is corrected as follows:  
"SENTDATA"

- Page 501 of 639, descriptions in lines 5 and 6 of 27. I/O Pins are modified as follows:  
"The pull-up resistors are enabled for every group of four pins. However, **when a pin functions as an output pin, a pull-up resistor is disabled regardless of the register settings.**"

- Page 501 of 639, description in the last paragraph of 27. I/O Pins is corrected as follows:  
"The input-only port P8\_5 shares a pin with NMI and has **neither function select register nor the corresponding direction bit.** Port P14\_1 also functions as an input-only port. The function select register and bit 1 in the PD14 register are reserved. Port P9 is protected from unexpected write accesses by the PRC2 bit in the PRCR register (refer to 10. "Protection")."

- Pages 535, 536 of 639, description in Note 2 of Tables 27.2 and 27.3 are modified as follows:  
"When configuring **as an output port to release the pin open, it remains as an input port until it is set as an output port after a reset is released. Therefore, while it remains as an input port,** the power supply current may increase due to the undefined voltage level of the pin. In addition, the direction register value may change due to noise or program runaway caused by the noise. To avoid these situations, reconfigure the direction register regularly by software, which may achieve higher program reliability."

- Pages 535, 536 of 639, description "addresses: 03E2h, 03E3h, 03E6h and 03E7h" in Note 4 of Tables 27.2 and 27.3 is modified as follows:  
"registers PD16 and PD17, PD18, and PD19"

- Page 595, 598, 608, 611, 628 of 639, expression "restart condition" in Tables 29.34, 29.39, 29.40, 29.60, 29.65, 29.66, and line 1 of 30.9.3 is modified as follows:  
"repeated START condition"

- Page 629 of 639, description for suspending and resuming communication is added to 30.9.4 as follows:

**"30.9.4 Reset Procedure or Suspend/Resume Procedure**

Operations which result in communication errors such as rewriting function select registers during transmission/reception should not be performed. Follow the procedure below to reset the internal circuit once the communication error occurs in the following cases: when the operation above is performed by a receiver or transmitter or when a bit slip is caused by noise.

**Also follow the procedure below when suspending and resuming communication in an emergency."**