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Old Company Name in Catalogs and Other Documents

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RENESAS TECHNICAL UPDATE

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Product Category	MPU&MCU	Document No.	TN-H8*-272A/EA	Rev.	1.0
Title	Corrections of the timer Z settings in complementary PWM mode in the H8/300H Tiny Series hardware manuals		Information Category	Correction or Supplement of Documents	
Applicable Product	H8/3687 Group H8/36037 Group H8/36049 Group	Lot No. All	Reference Document	H8/3687 Group hardware manual: REJ09B0027-0400Z Rev.4.00 H8/36057 Group, H8/36037 Group hardware manual: REJ09B0026-0200Z Rev.2.00 H8/36049 Group hardware manual: REJ09B0060-0100Z Rev.1.00	

We wish to notify you of the following corrections of the timer Z settings to output waveforms with a duty cycle of 0% and 100% during complementary PWM mode in the H8/3687 Group hardware manual, H8/36057 Group, H8/36037 Group hardware manual, and H8/36049 Group hardware manual, as detailed below.

In the following corrections, underlined figure numbers and sections are for the H8/3687 Group hardware manual. The figure numbers and sections differ depending on the Group. The corresponding figure numbers and sections are shown in each correction.

[Correction 1] Description of item 7 in figure 13.29, Example of Complementary PWM Mode Setting Procedure, amended

Group	H8/3687	H8/36037	H8/36049
Page	211	195	234
Amended Figure	Figure 13.29	Figure 12.29	Figure 14.29

[Error]

T ≤ X (X: Initial value of GRB_0, GRA_1, and GRB_1)

[Correction]

For GR settings, see 3. Setting GR Value in Complementary PWM Mode.

[Correction 2] Note in figure 13.29, Example of Complementary PWM Mode Setting Procedure, amended

Group	H8/3687	H8/36037	H8/36049
Page	211	195	234
Amended Figure	Figure 13.29	Figure 12.29	Figure 14.29

[Error]

Note: To re-enter complementary PWM mode after it has been cancelled during operation, repeat the setting procedures from [1].

[Correction]

Note: To re-enter complementary PWM mode, first, enter a mode other than the complementary PWM mode. After that, repeat the setting procedures from [1].
For settings of waveform outputs with a duty cycle of 0% and 100%, see the settings shown in 2. Examples of Complementary PWM Mode Operation and 3. Setting GR Value in Complementary PWM Mode.

[Correction 3] Description shown below figure 13.31 is amended

Group	H8/3687	H8/36037	H8/36049
Page	213	197	236
Amended Description	Shown below figure 13.31	Shown below figure 12.31	Shown below figure 14.31
Corresponding Figures and Sections	Figure 13.32	Figure 12.32	Figure 14.32
	Figure 13.32 (1)	Figure 12.32 (1)	Figure 14.32 (1)
	Figure 13.32 (2)	Figure 12.32 (2)	Figure 14.32 (2)

[Error]

Figure 13.32 shows examples of PWM waveform output with 0% duty and 100% duty in complementary PWM mode (for one phase). In this example, by setting the GRB_0 to a value equal to or more than GRA_0, and H'0000 for the value of GRB_0, the waveform with a duty of 0% and 100% can be output. When buffer operation is also used, manipulation of the above operation and modification of the duty can be done easily during operation. For details on buffer operation, refer to section 13.4.8, Buffer Operation.

[Correction]

Figures 13.32 (1) and 13.32 (2) show examples of a PWM waveform output with a duty cycle of 0% and 100% for one phase in complementary PWM mode.

- TPSC2 = TPSC1 = TPSC0 = 0
  Set GRB_0 to H'0000 or a value equal to or more than GRA_0. The waveform with a duty cycle of 0% and 100% can be output. When buffer operation is used together, the duty cycles can easily be changed, including the above settings, during operation. For details on buffer operation, refer to section 13.4.8, Buffer Operation.
- Other than TPSC2 = TPSC1 = TPSC0 = 0
  Set GRB_0 to satisfy the following expression: GRA_0 + 1 < GRB_0 < H'FFFF. The waveform with a duty cycle of 0% and 100% can be output. For details on 0%- and 100%-duty cycle waveform output, see 3. C., Outputting a waveform with a duty cycle of 0% and 100% (see No. 7 in this document).

[Correction 4] Title of figure 13.32, Example of Complementary PWM Mode Operation (1) (TPSC2 = TPSC1 = TPSC0 = 0), amended

Group	H8/3687	H8/36037	H8/36049
Page	214	198	237
Amended Figure Title	Figure 13.32	Figure 12.32	Figure 14.32
	Figure 13.32 (1)	Figure 12.32 (1)	Figure 14.32 (1)

[Error]

Figure 13.32, Example of Complementary PWM Mode Operation (1)

[Correction]

Figure 13.32 (1), Example of Complementary PWM Mode Operation (1) (TPSC2 = TPSC1 = TPSC0 = 0)

[Correction 5] Figure 13.32 (2), Example of Complementary PWM Mode Operation (1) (TPSC2 = TPSC1 = TPSC0 = 0), added

Group	H8/3687	H8/36037	H8/36049
Page	214	198	237
Added Figure	Figure 13.32 (2)	Figure 12.32 (2)	Figure 14.32 (2)

[Error]

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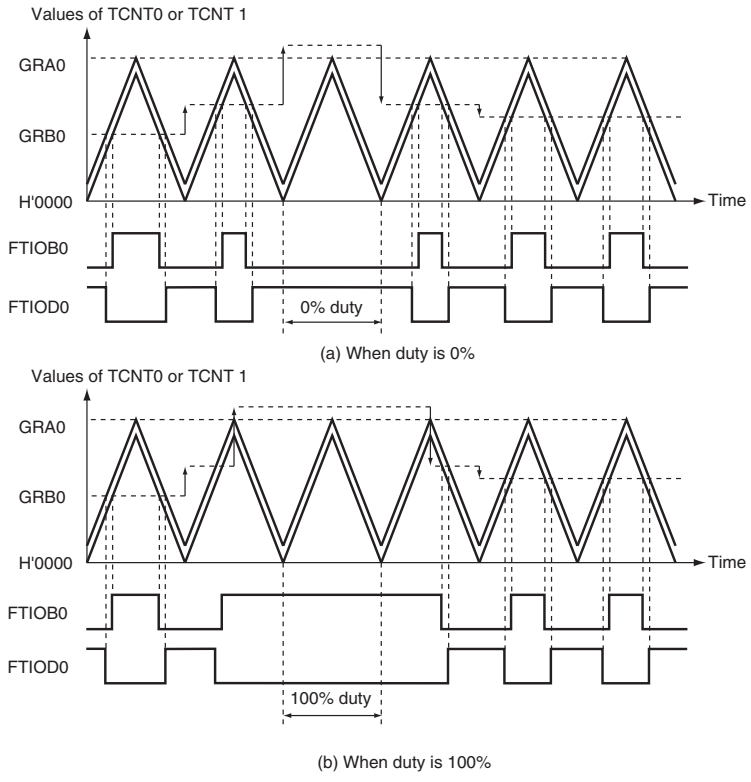
[Correction]

Figure 13.32 (2),Examples of Complementary PWM Mode Operation (3) (Other than TPSC2 = TPSC1 = TPSC0), added.



[Correction 6] Description shown below figure 13.34, Timing of Undershooting, amended

Group	H8/3687	H8/36037	H8/36049
Page	215	199	238
Amended Description	Shown below figure 13.34	Shown below figure 12.34	Shown below figure 14.34

[Error]

When the counter is incremented or decremented, the IMFA flag of channel 0 is set to 1, and when the register is underflowed, the UDF flag of channel 0 is set to 1. After buffer operation has been designated for BR, BR is transferred to GR when the counter is incremented by compare match A0 or when TCNT_1 is underflowed.

[Correction]

When the counter is incremented or decremented, the IMFA flag of channel 0 is set to 1, and when the register is underflowed, the UDF flag of channel 0 is set to 1. After buffer operation has been designated for BR, BR is transferred to GR when compare match A0 occurs if the counter is incremented or when TCNT_1 is underflowed. If the ϕ or ϕ/2 clock is selected by bits TPSC2 to TPSC0, the OVF flag is not set to 1 at the timing that the counter value changes from H'FFFF to H'0000. If the ϕ/4 or ϕ/8 clock is selected by bits TPSC2 to TPSC0, the OVF flag is set to 1.

[Correction 7] GR settings in 3. Setting GR Value in Complementary PWM Mode amended

Group	H8/3687	H8/36037	H8/36049
Page	216	200	239
Corresponding Section	13.4.8	12.4.8	14.4.8

[Error]

3. Setting GR Value in Complementary PWM Mode: To set GR or modify GR during operation in complementary PWM mode, refer to the following notes.
   A. Initial value
      a. H'0000 to T – 1 (T: Initial value of TCNT0) must not be set for the initial value.
      b. GRA_0 – (T – 1) or more must not be set for the initial value.
      c. When using buffer operation, the same values must be set in the buffer registers and corresponding general registers.
   B. Modifying the setting value
      Use buffer operation. When GR is written to directly, a correct waveform may not be output. Do not change settings of GRA_0 during operation.

[Correction]

3. Setting GR Value in Complementary PWM Mode: To set the general register (GR) or modify GR during operation in complementary PWM mode, refer to the following notes.
   A. Initial value
      a. When other than TPSC2 = TPSC1 = TPSC0 = 0, the CRA_0 value must be equal to H'FFFC or less. When TPSC2 = TPSC1 = TPSC0 = 0, the CRA_0 value can be set to H'FFFF or less.
      b. H'0000 to T – 1 (T: Initial value of TCNT_0) must not be set for the initial value.
      c. GRA_0 – (T – 1) or more must not be set for the initial value.
      d. When using buffer operation, the same values must be set in the buffer registers and corresponding general registers.
   B. Modifying the setting value
      a. Writing to GR directly must be performed while the TCNT_1 and TCNT_0 values should satisfy the following expression: H'0000 ≤ TCNT_1 < previous GR value, and previous GR value < TCNT_0 ≤ GRA_0. Otherwise, a waveform is not output correctly. For details on outputting a waveform with a duty cycle of 0% and 100%, see C., Outputting a waveform with a duty cycle of 0% and 100%.
      b. Do not write the following values to GR directly. When writing the values, a waveform is not output correctly.
      H'0000 ≤ GR ≤ T – 1 and GRA_0 – (T – 1) ≤ GR < GRA_0 when TPSC2 = TPSC1 = TPSC0 = 0

H'0000 < GR ≤ T – 1 and GRA_0 – (T – 1) ≤ GR < GRA_0 + 1 when TPSC2 = TPSC1 = TPSC0 = 0

c. Do not change settings of GRA_0 during operation.

C. Outputting a waveform with a duty cycle of 0% and 100%

a. Buffer operation is not used and TPSC2 = TPSC1 = TPSC0 = 0

Write H'0000 or a value equal to or more than the GRA_0 value to GR directly at the timing shown below.

- To output a 0%-duty cycle waveform, write a value equal to or more than the GRA_0 value while H'0000 ≤ TCNT_1 < previous GR value
- To output a 100%-duty cycle waveform, write H'0000 while previous GR value< TCNT_0 ≤ GRA_0

To change duty cycles while a waveform with a duty cycle of 0% or 100% is being output, make sure the following procedure.

- To change duty cycles while a 0%-duty cycle waveform is being output, write to GR while H'0000 ≤ TCNT_1 < previous GR value
- To change duty cycles while a 100%-duty cycle waveform is being output, write to GR while previous GR value< TCNT_0 ≤ GRA_0

Note that changing from a 0%-duty cycle waveform to a 100%-duty cycle waveform and vice versa is not possible.

b. Buffer operation is used and TPSC2 = TPSC1 = TPSC0 = 0

Write H'0000 or a value equal to or more than the GRA_0 value to the buffer register.

- To output a 0%-duty cycle waveform, write a value equal to or more than the GRA_0 value to the buffer register
- To output a 100%-duty cycle waveform, write H'0000 to the buffer register

For details on buffer operation, see section 13.4.8, Buffer Operation.

c. Buffer operation is not used and other than TPSC2 = TPSC1 = TPSC0 = 0

Write a value which satisfies GRA_0 + 1 < GR < H'FFFF to GR directly at the timing shown below.

- To output a 0%-duty cycle waveform, write the value while H'0000 ≤ TCNT_1 < previous GR value
- To output a 100%-duty cycle waveform, write the value while previous GR value< TCNT_0 ≤ GRA_0

To change duty cycles while a waveform with a duty cycle of 0% and 100% is being output, the following procedure must be followed.

- To change duty cycles while a 0%-duty cycle waveform is being output, write to GR while H'0000 ≤ TCNT_1 < previous GR value
- To change duty cycles while a 100%-duty cycle waveform is being output, write to GR while previous GR value< TCNT_0 ≤ GRA_0

Note that changing from a 0%-duty cycle waveform to a 100%-duty cycle waveform and vice versa is not possible.

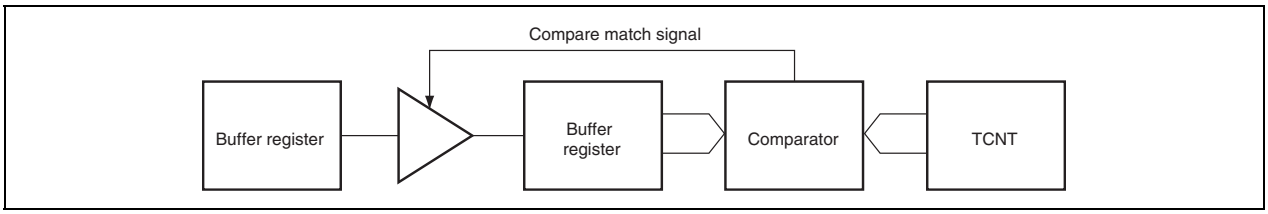
d. Buffer operation is used and other than TPSC2 = TPSC1 = TPSC0 = 0

Write a value which satisfies GRA_0 + 1 < GR < H'FFFF to the buffer register. A waveform with a duty cycle of 0% can be output. However, a waveform with a duty cycle of 100% cannot be output using the buffer operation. Also, the buffer operation cannot be used to change duty cycles while a waveform with a duty cycle of 100% is being output. For details on buffer operation, see section 13.4.8, Buffer Operation.

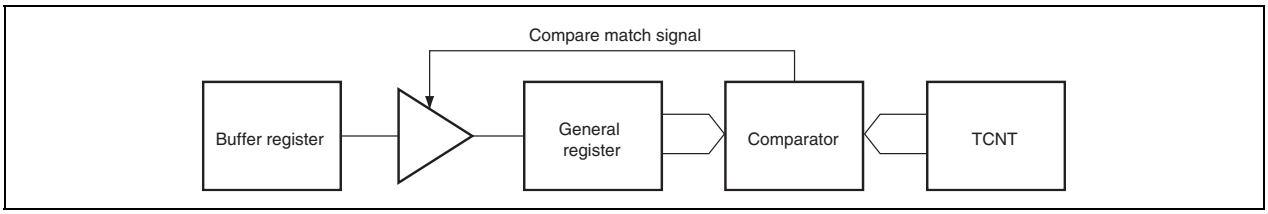
[Correction 8] Error amended in figure 13.35, Compare Match Buffer Operation

Group	H8/3687	H8/36037	H8/36049
Page	216	200	239
Amended Figure	Figure 13.35	Figure 12.35	Figure 14.35

[Error]



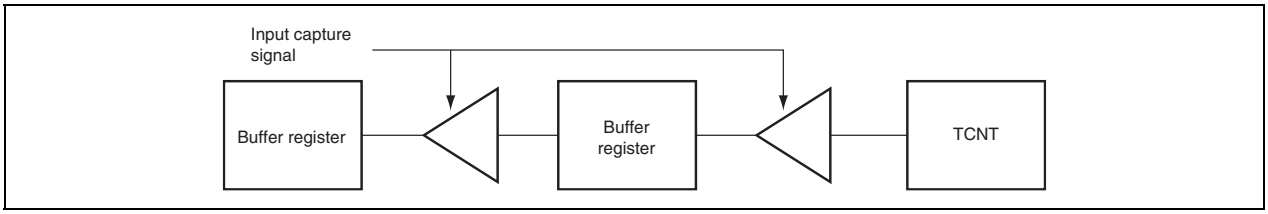
[Correction]



[Correction 9] Error amended in figure 13.36, Input Capture Buffer Operation

Group	H8/3687	H8/36037	H8/36049
Page	217	201	240
Amended Figure	Figure 13.36	Figure 12.36	Figure 14.36

[Error]



[Correction]