To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

Send any inquiries to http://www.renesas.com/inquiry.

Date: Dec.06.2006

RENESAS TECHNICAL UPDATE

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Renesas Technology Corp.

Product Category	MPU&MCU		Document No.	TN-H8*-A352B/E	Rev.	2.00
Title	Corrections of Serial Communication Interface 3 (SCI3)		Information Category	Technical notification		
Applicable Product	See below	Lot No. All lots	Reference Document	See below		

We would like to inform you of the corrections of the usage notes on the serial communication interface 3 (SCI3), in the H8/300H Tiny Series of the Renesas 16-bit single-chip MCU/MPU.

1. Serial Communication Interface 3 (SCI3)

- **Mark State and Break Sending**

[Before change]

When TE is 0, the TxD pin is used as an I/O port whose direction (input or output) and level are determined by PCR and PDR. This can be used to set the TxD pin to mark state (high level) or send a break during serial data transmission. To maintain the communication line at mark state until TE is set to 1, set both PCR and PDR to 1. As TE is cleared to 0 at this point, the TxD pin becomes an I/O port, and 1 is output from the TxD pin. To send a break during serial transmission, first set PCR to 1 and PDR to 0, and then clear TE to 0. When TE is cleared to 0, the transmitter is initialized regardless of the current transmission state, the TxD pin becomes an I/O port, and 0 is output from the TxD pin.

[After change]

When the TXD or TXD2 bit*[1] in PMR1 or the TXD_3 bit*[2] in SMCR is 0, the TxD pin is used as an I/O port whose direction (input or output) and level are determined by PCR and PDR. This can be used to set the TxD pin to mark state (high level) or send a break during serial data transmission. To maintain the communication line at mark state until TE is set to 1, set PCR and PDR to 1 respectively, and also clear the TXD bit to 0. At this time, the TxD pin becomes an I/O port, and 1 is output from the TxD pin. To send a break during serial data transmission, first set PCR to 1 and clear PDR to 0, and then clear the TXD bit to 0. Regardless of the current transmission state, the TxD pin becomes an I/O port and 0 is output from the TxD pin.

Notes: *1. For two-channel SCI3
*2. For three-channel SCI3

2. Applicable Product and Reference Document

Applicable Product Group	Reference Document Title	Rev. No.	Document No.
H8/3664	H8/3664 Group Hardware Manual	Rev.6.0	REJ09B0142-0600
H8/3672	H8/3672 Group Hardware Manual	Rev.4.0	REJ09B0143-0400
H8/3687	H8/3687 Group Hardware Manual	Rev.5.0	REJ09B0027-0500
H8/3694	H8/3694 Group Hardware Manual	Rev.5.0	REJ09B0028-0500
H8/36024, H8/36014	H8/36024 Group, H8/36014 Group Hardware Manual	Rev.4.0	REJ09B0025-0400
H8/36057, H8/36037	H8/36057 Group, H8/36037 Group Hardware Manual	Rev.4.0	REJ09B0026-0400
H8/36087	H8/36087 Group Hardware Manual	Rev.2.0	REJ09B0160-0200
H8/36049	H8/36049 Group Hardware Manual	Rev.3.0	REJ09B0060-0300
H8/36064	H8/36064 Group Hardware Manual	Rev.2.0	REJ09B0068-0200