

RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-RL*-A0125A/E	Rev.	1.00
Title	Correction for Incorrect Description Notice RL78/G15 Descriptions in the User's Manual: Hardware Rev. 1.00 Changed		Information Category	Technical Notification		
Applicable Product	RL78/G15 Group	Lot No.	Reference Document	RL78/G15 User's Manual: Hardware Rev. 1.00 R01UH0959EJ0100 (Sep. 2022)		
		All lots				

This document describes misstatements found in the RL78/G15 User's Manual: Hardware Rev. 1.00 (R01UH0959EJ0100).

Corrections

Applicable Item	Applicable Page	Contents
(1) Vector table area	Page 60	Incorrect descriptions revised
4.5.1 Basic concept when using alternate function	Page 117	Incorrect descriptions revised
4.5.3 Register setting examples for used port and alternate functions	Page 118 to Page 125	Incorrect descriptions revised
14.3 Registers Controlling Interrupt Functions	Page 606	Incorrect descriptions revised
CHAPTER 23 ELECTRICAL SPECIFICATIONS (T _A = -40 to +85°C) (Target)	Page 708	Incorrect descriptions revised
23.2.2 On-chip oscillator characteristics	Page 710	Incorrect descriptions revised
23.8 Flash Memory Programming Characteristics	Page 728	Incorrect descriptions revised
23.10 Timing of Entry to Flash Memory Programming Mode	Page 729	Incorrect descriptions revised
CHAPTER 24 ELECTRICAL SPECIFICATIONS (T _A = -40 to +105°C, T _A = -40 to +125°C) (Target)	Page 730	Incorrect descriptions revised
24.2.2 On-chip oscillator characteristics	Page 732	Incorrect descriptions revised
24.8 Flash Memory Programming Characteristics	Page 750	Incorrect descriptions revised
24.10 Timing of Entry to Flash Memory Programming Mode	Page 751	Incorrect descriptions revised
25.1 8-pin products	Page 752	Incorrect descriptions revised

Document Improvement

The above corrections will be made for the next revision of the User's Manual: Hardware.

No.	Corrections and Applicable Items			Pages in this document for corrections
	Document No.	English	R01UH0959EJ0100	
1	(1) Vector table area		Page 60	Page 3
2	4.5.1 Basic concept when using alternate function		Page 117	Page 4
3	4.5.3 Register setting examples for used port and alternate functions		Page 118 to Page 125	Page 4 to Page 11
4	14.3 Registers Controlling Interrupt Functions		Page 606	Page 12
5	CHAPTER 23 ELECTRICAL SPECIFICATIONS (T _A = -40 to +85°C) (Target)		Page 708	Page 13
6	23.2.2 On-chip oscillator characteristics		Page 710	Page 13
7	23.8 Flash Memory Programming Characteristics		Page 728	Page 14
8	23.10 Timing of Entry to Flash Memory Programming Mode		Page 729	Page 14
9	CHAPTER 24 ELECTRICAL SPECIFICATIONS (T _A = -40 to +105°C, T _A = -40 to +125°C) (Target)		Page 730	Page 14
10	24.2.2 On-chip oscillator characteristics		Page 732	Page 15
11	24.8 Flash Memory Programming Characteristics		Page 750	Page 16
12	24.10 Timing of Entry to Flash Memory Programming Mode		Page 751	Page 16
13	25.1 8-pin products		Page 752	Page 17

Incorrect: **Bold with underline:** Correct: Gray hatched

Revision HistoryNo,

RL78/G15 Correction for incorrect description notice

Document Number	Issue Date	Description
TN-RL*-A0125A/E	Mar. 3, 2023	First edition issued Corrections No.1 to No.13 revised (this document)

1. **(1) Vector table area (Page 60)**

Incorrect:

Table 3-3. Vector Table

Vector Table Address	Interrupt Source	20-pin	16-pin	10-pin	8-pin
00000H	RESET, SPOR, WDT, TRAP, IAW	✓	✓	✓	✓
00004H	INTWDTI	✓	✓	✓	✓
00006H	INTP0	✓	✓	✓	✓
00008H	INTP1	✓	✓	✓	✓
0000AH	INTP2	✓	✓	✓	✓
0000CH	INTP3	✓	✓	✓	✓
0000EH	INTP4	✓	✓	✓	✓
00010H	INTP5	✓	✓	✓	✓
00012H	INTST0, INTCSI00, INTIIC00	✓	✓	✓	✓
00014H	INTSR0, INTCSI01, INTIIC01	✓	✓	✓	✓
00016H	INTSRE0	✓	✓	✓	✓
00018H	INTTM01H	✓	✓	✓	✓
0001AH	INTTM00	✓	✓	✓	✓
0001CH	INTTM01	✓	✓	✓	✓
0001EH	INTAD	✓	✓	✓	✓
00020H	INTP6	✓	✓	✓	—
00022H	INTP7	✓	✓	✓	—
00024H	INTTM03H	✓	✓	≡	≡
00026H	INTICA0	✓	✓	≡	≡
00028H	INTTM02	✓	✓	≡	≡
0002AH	INTTM03	✓	✓	≡	≡
0002CH	INTIT	✓	✓	✓	✓
0002EH	INTTM04	✓	✓	≡	≡
00030H	INTTM05	✓	≡	≡	≡
00032H	INTTM06	✓	✓	≡	≡
00034H	INTTM07	✓	≡	≡	≡
00036H	INTCMP0	✓	✓	✓	✓
00038H	INTCMP1	✓	—	—	—
0007EH	BRK	✓	✓	✓	✓

Correct:

Table 3-3. Vector Table

Vector Table Address	Interrupt Source	20-pin	16-pin	10-pin	8-pin
00000H	RESET, SPOR, WDT, TRAP, IAW	✓	✓	✓	✓
00004H	INTWDTI	✓	✓	✓	✓
00006H	INTP0	✓	✓	✓	✓
00008H	INTP1	✓	✓	✓	✓
0000AH	INTP2	✓	✓	✓	✓
0000CH	INTP3	✓	✓	✓	✓
0000EH	INTP4	✓	✓	✓	✓
00010H	INTP5	✓	✓	✓	✓
00012H	INTST0, INTCSI00, INTIIC00	✓	✓	✓	✓
00014H	INTSR0, INTCSI01, INTIIC01	✓	✓	✓	✓
00016H	INTSRE0	✓	✓	✓	✓
00018H	INTTM01H	✓	✓	✓	✓
0001AH	INTTM00	✓	✓	✓	✓
0001CH	INTTM01	✓	✓	✓	✓
0001EH	INTAD	✓	✓	✓	✓
00020H	INTP6	✓	✓	✓	—
00022H	INTP7	✓	✓	✓	—
00024H	INTTM03H	✓	✓	☒	☒
00026H	INTICA0	✓	✓	☒	☒
00028H	INTTM02	✓	✓	☒	☒
0002AH	INTTM03	✓	✓	☒	☒
0002CH	INTIT	✓	✓	✓	✓
0002EH	INTTM04	✓	✓	☒	☒
00030H	INTTM05	✓	☒	☒	☒
00032H	INTTM06	✓	✓	☒	☒
00034H	INTTM07	✓	☒	☒	☒
00036H	INTCMP0	✓	✓	✓	✓
00038H	INTCMP1	✓	—	—	—
0007EH	BRK	✓	✓	✓	✓

2. 4.5.1 Basic concept when using alternate function (page 117)

Incorrect:

Table 4-6. Concept of Basic Settings

Output Function of Used Pin	Output Settings of Unused Alternate Function		
	Output Function for Port	Output Function for SAU	Output Function for other than SAU
Output function for port	—	Output: High (1)	Output: Low (0)
Output function for SAU	High (1)	—	Output: Low (0)
Output function for other than SAU	Low (0)	Output: High (1)	Output:Low (0) ^{Note 1}

3. 4.5.3 Register setting examples for used port and alternate functions (page 118 – page 125)

Incorrect:

Table 4-7. Setting Examples of Registers and Output Latches When Using Pin Function (1/10)

Pin Name	Used Function		PIORr	POMp	PMCq	PMn	Pm	Alternate Function Output		20-pin	16-pin	10-pin	8-pin
	Function Name	I/O						SAU Output Function	Other than SAU				
P00	P00	Input	—	x	—	1	x	x	x	✓	✓	✓	—
	(SCLA0)	I/O	PIOR14 = 1	1	—	0	0	1x00/SQ00=1 (SCK01/SCL01)=1	x	✓	✓	—	—

Correct:

Table 4-6. Concept of Basic Settings

Output Function of Used Pin	Output Settings of Unused Alternate Function		
	Output Function for Port	Output Function for SAU	Output Function for other than SAU
Output function for port	—	Output: High (1)	Output: Low (0)
Output function for SAU	High (1)	—	Output: Low (0)
Output function for other than SAU	Low (0)	don't care	Output:Low (0) ^{Note 1}

Correct:

Table 4-7. Setting Examples of Registers and Output Latches When Using Pin Function (1/10)

Pin Name	Used Function		PIORr	POMp	PMCq	PMn	Pm	Alternate Function Output		20-pin	16-pin	10-pin	8-pin
	Function Name	I/O						SAU Output Function	Other than SAU				
P00	P00	Input	—	x	—	1	x	x	x	✓	✓	✓	—
	(SCLA0)	I/O	PIOR14 = 1	1	—	0	0	*	x	✓	✓	—	—

Incorrect:

Table 4-7. Setting Examples of Registers and Output Latches When Using Pin Function (2/10)

Pin Name	Used Function		PIORr	POMp	PMCq	PMn	Pm	Alternate Function Output		20-pin	16-pin	10-pin	8-pin
	Function Name	I/O						SAU Output Function	Other than SAU				
P01	P01	Input	—	x	0	1	x	x	x	✓	✓	✓	✓

(TO02)	Output	PIOR05 = 0 PIOR04 = 1	0	0	0	0	0	SDA00 = 1 (SDAA0) = 0 (SDA01) = 1	(SDAA0) = 0	✓	✓	—	—
(SI01)	Input	PIOR13 = 0 ^{Note 2} PIOR12 = 1	x	0	1	x	x	x	x	✓	✓	—	—
(SDA01)	I/O	PIOR13 = 0 ^{Note 2} PIOR12 = 1	1	0	0	1	1	SDA00 = 1 (TO02) = 0 (SDAA0) = 0	(TO02) = 0 (SDAA0) = 0	✓	✓	—	—
(SDAA0)	I/O	PIOR14 = 1	1	0	0	0	0	SDA00 = 1 (SDAA0) = 1	(TO02) = 0	✓	✓	—	—
TI02	Input	—	x	0	1	x	x	x	x	—	—	✓	✓
TO02	Output	—	0	0	0	0	0	SDA00 = 1 SDAA0 = 0	SDAA0 = 0	—	—	✓	✓
SDAA0	I/O	—	1	0	0	0	0	SDA00 = 1 (TO02) = 0	(TO02) = 0	—	—	✓	✓

Correct:

Table 4-7. Setting Examples of Registers and Output Latches When Using Pin Function (2/10)

Pin Name	Used Function		PIORr	POMp	PMCq	PMn	Pm	Alternate Function Output		20-pin	16-pin	10-pin	8-pin
	Function Name	I/O						SAU Output Function	Other than SAU				
P01	P01	Input	—	x	0	1	x	x	x	✓	✓	✓	✓

(TO02)	Output	PIOR05 = 0 PIOR04 = 1	0	0	0	0	0	⊗	(SDAA0) = 0	✓	✓	—	—
(SI01)	Input	PIOR13 = 0 ^{Note 2} PIOR12 = 1	x	0	1	x	x	x	x	✓	✓	—	—
(SDA01)	I/O	PIOR13 = 0 ^{Note 2} PIOR12 = 1	1	0	0	1	1	SDA00 = 1 (TO02) = 0 (SDAA0) = 0	(TO02) = 0 (SDAA0) = 0	✓	✓	—	—
(SDAA0)	I/O	PIOR14 = 1	1	0	0	0	0	x	(TO02) = 0	✓	✓	—	—
TI02	Input	—	x	0	1	x	x	x	x	—	—	✓	✓
TO02	Output	—	0	0	0	0	0	⊗	SDAA0 = 0	—	—	✓	✓
SDAA0	I/O	—	1	0	0	0	0	⊗	(TO02) = 0	—	—	✓	✓

Incorrect:

Correct:

Table 4-7. Setting Examples of Registers and Output Latches When Using Pin Function (3/10)

Table 4-7. Setting Examples of Registers and Output Latches When Using Pin Function (3/10)

Pin Name	Used Function		PIORr	POMp	PMCq	PMn	Pm	Alternate Function Output		20-pin	16-pin	10-pin	8-pin
	Function Name	I/O						SAU Output Function	Other than SAU				
P02	P02	Input	—	—	0	1	x	x	x	✓	✓	✓	—

Pin Name	Used Function		PIORr	POMp	PMCq	PMn	Pm	Alternate Function Output		20-pin	16-pin	10-pin	8-pin
	Function Name	I/O						SAU Output Function	Other than SAU				
P02	P02	Input	—	—	0	1	x	x	x	✓	✓	✓	—

PCLBUZ0	Output	PIOR31 = 0 ^{Note 1} PIOR30 = 0	—	0	0	0	0	SCK00/SCL00 = 1 (SO01) = 1 ^{Note 1}	VCOU0 = 0 (TO01) = 0	✓	✓	✓	—
VCOU0	Output	PIOR32 = 0	—	0	0	0	0	SCK00/SCL00 = 1 (SO01) = 1 ^{Note 1}	PCLBUZ0 = 0 (TO01) = 0	✓	✓	✓	—
INTP7	Input	PIOR35 = 0 ^{Note 2} PIOR34 = 0 ^{Note 1}	—	0	1	1	x	x	x	✓	✓	✓	—
(TI01)	Input	PIOR03 = 1 PIOR02 = 0	—	0	1	1	x	x	x	✓	✓	✓	—
(TO01)	Output	PIOR03 = 1 PIOR02 = 0	—	0	0	0	0	SCK00/SCL00 = 1 (SO01) = 1 ^{Note 1}	PCLBUZ0 = 0 VCOU0 = 0 (TO01) = 0	✓	✓	✓	—
(SO01)	Output	PIOR13 = 0 ^{Note 2} PIOR12 = 1	—	0	0	1	1	SCK00/SCL00 = 1	PCLBUZ0 = 0 VCOU0 = 0 (TO01) = 0	✓	✓	—	—
P03	P03	Input	—	x	0	1	x	x	x	✓	✓	✓	✓
		Output	—	0	0	0	0/1	SO00/TxD0 = 1 ^{Note 4} (SO00/TxD0) = 1 ^{Note 1}	TO00 = 0 SCLA0 = 0 ^{Note 3}	✓	✓	✓	✓
		N-ch open drain output	—	1	0	0	0/1	(SO00/TxD0) = 1 ^{Note 1}	SCLA0 = 0 ^{Note 3}	✓	✓	✓	✓
	ANI2	Analog input	—	x	1	1	x	x	x	✓	✓	✓	✓
TO00	Output	PIOR01 = 0 ^{Note 2} PIOR00 = 0 ^{Note 2}	0	0	0	0	0	SO00/TxD0 = 1 ^{Note 4} (SO00/TxD0) = 1 ^{Note 1}	SCLA0 = 0 ^{Note 3}	✓	✓	✓	✓
INTP4	Input	PIOR23 = 0 ^{Note 1}	x	0	1	1	x	x	x	✓	✓	✓	✓

PCLBUZ0	Output	PIOR31 = 0 ^{Note 1} PIOR30 = 0	—	0	0	0	0	x	VCOU0 = 0 (TO01) = 0	✓	✓	✓	—
VCOU0	Output	PIOR32 = 0	—	0	0	0	0	x	PCLBUZ0 = 0 (TO01) = 0	✓	✓	✓	—
INTP7	Input	PIOR35 = 0 ^{Note 2} PIOR34 = 0 ^{Note 1}	—	0	1	1	x	x	x	✓	✓	✓	—
(TI01)	Input	PIOR03 = 1 PIOR02 = 0	—	0	1	1	x	x	x	✓	✓	✓	—
(TO01)	Output	PIOR03 = 1 PIOR02 = 0	—	0	0	0	0	x	PCLBUZ0 = 0 VCOU0 = 0 (TO01) = 0	✓	✓	✓	—
(SO01)	Output	PIOR13 = 0 ^{Note 2} PIOR12 = 1	—	0	0	1	1	SCK00/SCL00 = 1	PCLBUZ0 = 0 VCOU0 = 0 (TO01) = 0	✓	✓	—	—
P03	P03	Input	—	x	0	1	x	x	x	✓	✓	✓	✓
		Output	—	0	0	0	0/1	SO00/TxD0 = 1 ^{Note 4} (SO00/TxD0) = 1 ^{Note 1}	TO00 = 0 SCLA0 = 0 ^{Note 3}	✓	✓	✓	✓
		N-ch open drain output	—	1	0	0	0/1	(SO00/TxD0) = 1 ^{Note 1}	SCLA0 = 0 ^{Note 3}	✓	✓	✓	✓
	ANI2	Analog input	—	x	1	1	x	x	x	✓	✓	✓	✓
TO00	Output	PIOR01 = 0 ^{Note 2} PIOR00 = 0 ^{Note 2}	0	0	0	0	0	x	SCLA0 = 0 ^{Note 3}	✓	✓	✓	✓
INTP4	Input	PIOR23 = 0 ^{Note 1}	x	0	1	1	x	x	x	✓	✓	✓	✓

(TxD0)	Output	PIOR11 = 1 PIOR10 = 0	0/1	0	0	1	1	x	TO00 = 0	✓	✓	—	—
SCLA0	I/O	—	1	0	0	0	0	SO00/TxD0 = 1 ^{Note 4}	TO00 = 0	—	—	✓	✓
SO00	Output	—	0	0	0	1	1	x	TO00 = 0 SCLA0 = 0	—	—	—	✓

(TxD0)	Output	PIOR11 = 1 PIOR10 = 0	0/1	0	0	1	1	x	TO00 = 0	✓	✓	—	—
SCLA0	I/O	—	1	0	0	0	0	x	TO00 = 0	—	—	✓	✓
SO00	Output	—	0	0	0	1	1	x	TO00 = 0 SCLA0 = 0	—	—	—	✓

Incorrect:

Table 4-7. Setting Examples of Registers and Output Latches When Using Pin Function (4/10)

Pin Name	Used Function		PIORr	POMp	PMCq	PMn	Pm	Alternate Function Output		20-pin	16-pin	10-pin	8-pin
	Function Name	I/O						SAU Output Function	Other than SAU				
P04	P04	Input	—	x	0	1	x	x	x	✓	✓	✓	✓
		Output	—	0	0	0	0/1	(SO00/TxD0) = 1 ^{Note 1} (SDA00) = 1 ^{Note 1} SCL00/SCL00 = 1 ^{Note 4}	TO01 = 0				
		N-ch open drain output	—	1	0	0	0/1						
ANI3	Analog input	—	x	1	1	x	x	x	✓	✓	✓	✓	
TI01	Input	PIOR03 = 0 ^{Note 5} PIOR02 = 0	x	0	1	x	x	x	✓	✓	✓	✓	
TO01	Output	PIOR03 = 0 ^{Note 5} PIOR02 = 0	0	0	0	0	(SO00/TxD0) = 1 ^{Note 1} (SDA00) = 1 ^{Note 1} SCL00/SCL00 = 1 ^{Note 4}	x	✓	✓	✓	✓	

Correct:

Table 4-7. Setting Examples of Registers and Output Latches When Using Pin Function (4/10)

Pin Name	Used Function		PIORr	POMp	PMCq	PMn	Pm	Alternate Function Output		20-pin	16-pin	10-pin	8-pin
	Function Name	I/O						SAU Output Function	Other than SAU				
P04	P04	Input	—	x	0	1	x	x	x	✓	✓	✓	✓
		Output	—	0	0	0	0/1	(SO00/TxD0) = 1 ^{Note 1} (SDA00) = 1 ^{Note 1} SCL00/SCL00 = 1 ^{Note 4}	TO01 = 0				
		N-ch open drain output	—	1	0	0	0/1						
ANI3	Analog input	—	x	1	1	x	x	x	✓	✓	✓	✓	
TI01	Input	PIOR03 = 0 ^{Note 5} PIOR02 = 0	x	0	1	x	x	x	✓	✓	✓	✓	
TO01	Output	PIOR03 = 0 ^{Note 5} PIOR02 = 0	0	0	0	0	(SO00/TxD0) = 1 ^{Note 1} (SDA00) = 1 ^{Note 1} SCL00/SCL00 = 1 ^{Note 4}	x	✓	✓	✓	✓	

Incorrect:

Table 4-7. Setting Examples of Registers and Output Latches When Using Pin Function (5/10)

Pin Name	Used Function		PIORr	POMp	PMCq	PMn	Pm	Alternate Function Output		20-pin	16-pin	10-pin	8-pin		
	Function Name	I/O						SAU Output Function	Other than SAU						
P05	P05	Input	—	x	0	1	x	x	x	✓	✓	—	—		
		TO02	Output	PIOR05 = 0	0	0	0	0	SA01 = 1	x	✓	✓	—	—	
				PIOR04 = 0					(SCK00/SCL00) = 1						
								(SDA00) = 1							
P06	P06	Input	—	x	0	1	x	x	x	✓	✓	—	—		
		SCLA0	I/O	PIOR14 = 0	1	0	0	0	SDA01 = 1	(PCLBUZ0) = 0	✓	✓	—	—	
									(SCK00/SCL00) = 1						
		(INTP7)	Input	PIOR35 = 0 ^{Note 2}	x	0	1	x	x	✓	✓	—	—		
				PIOR34 = 1											
		(PCLBUZ0)	Output	PIOR31 = 1	0	0	0	0	SDA01 = 1	SCLA0 = 0	✓	✓	—	—	
				PIOR30 = 0					(SCK00/SCL00) = 1						

Correct:

Table 4-7. Setting Examples of Registers and Output Latches When Using Pin Function (5/10)

Pin Name	Used Function		PIORr	POMp	PMCq	PMn	Pm	Alternate Function Output		20-pin	16-pin	10-pin	8-pin		
	Function Name	I/O						SAU Output Function	Other than SAU						
P05	P05	Input	—	x	0	1	x	x	x	✓	✓	—	—		
		TO02	Output	PIOR05 = 0	0	0	0	0	x	x	✓	✓	—	—	
				PIOR04 = 0											
P06	P06	Input	—	x	0	1	x	x	x	✓	✓	—	—		
		SCLA0	I/O	PIOR14 = 0	1	0	0	0	x	(PCLBUZ0) = 0	✓	✓	—	—	
		(INTP7)	Input	PIOR35 = 0 ^{Note 2}	x	0	1	x	x	x	✓	✓	—	—	
				PIOR34 = 1											
		(PCLBUZ0)	Output	PIOR31 = 1	0	0	0	0	x	SCLA0 = 0	✓	✓	—	—	
				PIOR30 = 0											

Incorrect:

Table 4-7. Setting Examples of Registers and Output Latches When Using Pin Function (6/10)

Pin Name	Used Function		PIORr	POMp	PMCq	PMn	Pm	Alternate Function Output		20-pin	16-pin	10-pin	8-pin
	Function Name	I/O						SAU Output Function	Other than SAU				
P07	P07	Input	—	x	0	1	x	x	x	✓	✓	—	—
		Output	—	0	0	0	0/1	SCK01/SCL01 = 1 (TO03) = 0	SDAA0 = 0	✓	✓	—	—
		N-ch open drain output	—	1	0	0	0/1	SDAA0 = 0					
ANI6	Analog input	—	x	1	1	x	x	x	✓	✓	—	—	
(TO03)	Output	PIOR07 = 0 ^{Note 2} PIOR06 = 1	0/1	0	0	0	SCK01/SCL01 = 1	SDAA0 = 0	✓	✓	—	—	
SCK01	SCK01	Input	PIOR13 = 0 ^{Note 2} PIOR12 = 0	x	0	1	x	x	x	✓	✓	—	—
		Output	PIOR13 = 0 ^{Note 2} PIOR12 = 0	0	0	0	1	x	(TO03) = 0 SDAA0 = 0	✓	✓	—	—
SCL01	Output	PIOR13 = 0 ^{Note 2} PIOR12 = 0	0	0	0	1	x	(TO03) = 0 SDAA0 = 0	✓				
SDAA0	I/O	PIOR14 = 0	1	0	0	0	SCK01/SCL01 = 1	(TO03) = 0	✓	✓	—	—	
(INTP5)	Input	PIOR25 = 0 ^{Note 2} PIOR24 = 1	x	0	1	x	x	x	✓	✓	—	—	

Correct:

Table 4-7. Setting Examples of Registers and Output Latches When Using Pin Function (6/10)

Pin Name	Used Function		PIORr	POMp	PMCq	PMn	Pm	Alternate Function Output		20-pin	16-pin	10-pin	8-pin
	Function Name	I/O						SAU Output Function	Other than SAU				
P07	P07	Input	—	x	0	1	x	x	x	✓	✓	—	—
		Output	—	0	0	0	0/1	SCK01/SCL01 = 1 (TO03) = 0	SDAA0 = 0	✓	✓	—	—
		N-ch open drain output	—	1	0	0	0/1	SDAA0 = 0					
ANI6	Analog input	—	x	1	1	x	x	x	✓	✓	—	—	
(TO03)	Output	PIOR07 = 0 ^{Note 2} PIOR06 = 1	0/1	0	0	0	x	SDAA0 = 0	✓	✓	—	—	
SCK01	SCK01	Input	PIOR13 = 0 ^{Note 2} PIOR12 = 0	x	0	1	x	x	x	✓	✓	—	—
		Output	PIOR13 = 0 ^{Note 2} PIOR12 = 0	0	0	0	1	x	(TO03) = 0 SDAA0 = 0	✓	✓	—	—
SCL01	Output	PIOR13 = 0 ^{Note 2} PIOR12 = 0	0	0	0	1	x	(TO03) = 0 SDAA0 = 0	✓				
SDAA0	I/O	PIOR14 = 0	1	0	0	0	x	(TO03) = 0	✓	✓	—	—	
(INTP5)	Input	PIOR25 = 0 ^{Note 2} PIOR24 = 1	x	0	1	x	x	x	✓	✓	—	—	

Incorrect:

Table 4-7. Setting Examples of Registers and Output Latches When Using Pin Function (7/10)

Pin Name	Used Function		PIORr	POMp	PMCq	PMn	Pm	Alternate Function Output		20-pin	16-pin	10-pin	8-pin
	Function Name	I/O						SAU Output Function	Other than SAU				
P20	P20	Input	—	—	0	1	x	x	x	✓	—	—	—
	(TO03)	Output	PIOR07 = 1 PIOR06 = 0	—	0	0	0	(SCK01)(SCL01)=1	x	✓	—	—	—
P22	P22	Input	—	x	0	1	x	x	x	✓	—	—	—
	TO06	Output	—	0	0	0	0	(SDA01)=1	x	✓	—	—	—
	(INTP5)	Input	PIOR25 = 1 PIOR24 = 0	x	0	1	x	x	x	✓	—	—	—
P23	P23	Input	—	—	0	1	x	x	x	✓	—	—	—
	TO04	Output	—	—	0	0	0	(SCL01)=1	x	✓	—	—	—

Correct:

Table 4-7. Setting Examples of Registers and Output Latches When Using Pin Function (7/10)

Pin Name	Used Function		PIORr	POMp	PMCq	PMn	Pm	Alternate Function Output		20-pin	16-pin	10-pin	8-pin
	Function Name	I/O						SAU Output Function	Other than SAU				
P20	P20	Input	—	—	0	1	x	x	x	✓	—	—	—
	(TO03)	Output	PIOR07 = 1 PIOR06 = 0	—	0	0	0	⊗	x	✓	—	—	—
P22	P22	Input	—	x	0	1	x	x	x	✓	—	—	—
	TO06	Output	—	0	0	0	0	⊗	x	✓	—	—	—
	(INTP5)	Input	PIOR25 = 1 PIOR24 = 0	x	0	1	x	x	x	✓	—	—	—
P23	P23	Input	—	—	0	1	x	x	x	✓	—	—	—
	TO04	Output	—	—	0	0	0	⊗	x	✓	—	—	—

Incorrect:

Correct:

Table 4-7. Setting Examples of Registers and Output Latches When Using Pin Function (8/10)

Table 4-7. Setting Examples of Registers and Output Latches When Using Pin Function (8/10)

Pin Name	Used Function		PIORr	POMp	PMCq	PMn	Pm	Alternate Function Output		20-pin	16-pin	10-pin	8-pin
	Function Name	I/O						SAU Output Function	Other than SAU				
P41	P41	Input	—	x	—	1	x	x	x	✓	✓	—	—
		Output	—	0	—	0	0/1	(SDA01/SO01) = 1 ^{Note 2} TO03 = 0	TO03 = 0				
		N-ch open drain output	—	1	—	0	0/1	(SDA01/SO01) = 1 ^{Note 2} TO03 = 0 VCOUT1 = 0 ^{Note 2}	TO03 = 0 VCOUT1 = 0 ^{Note 2}				
	TI03	Input	PIOR07 = 0 ^{Note 2}	x	—	1	x	x	x	✓	✓	—	—
	TO03	Output	PIOR07 = 0 ^{Note 2} PIOR06 = 0	0	—	0	0	(SDA01/SO01) = 1 ^{Note 2} TO03 = 0 VCOUT1 = 0 ^{Note 2}	TO03 = 0 VCOUT1 = 0 ^{Note 2}	✓	✓	—	—
	(INTP4)	Input	PIOR23 = 1	x	—	1	x	x	x	✓	✓	—	—
	(TI02)	Input	PIOR05 = 1 PIOR04 = 0	x	—	1	x	x	x	✓	✓	—	—
	(TO02)	Output	PIOR05 = 1 PIOR04 = 0	0	—	0	0	(SDA01/SO01) = 1 ^{Note 2} TO03 = 0 VCOUT1 = 0 ^{Note 2}	TO03 = 0 VCOUT1 = 0 ^{Note 2}	✓	✓	—	—
	VCOUT1	Output	PIOR33 = 0	0	—	0	0	(SDA01/SO01) = 1 TO03 = 0 TO02 = 0	TO03 = 0 TO02 = 0	✓	—	—	—
	(SDA01)	I/O	PIOR13 = 1 PIOR12 = 0	1	—	0	1	x	TO03 = 0 TO02 = 0 VCOUT1 = 0	TO03 = 0 TO02 = 0 VCOUT1 = 0	✓	—	—
(SO01)	Output	PIOR13 = 1 PIOR12 = 0	0	—	0	1	x	TO03 = 0 TO02 = 0 VCOUT1 = 0	TO03 = 0 TO02 = 0 VCOUT1 = 0	✓	—	—	—

Pin Name	Used Function		PIORr	POMp	PMCq	PMn	Pm	Alternate Function Output		20-pin	16-pin	10-pin	8-pin
	Function Name	I/O						SAU Output Function	Other than SAU				
P41	P41	Input	—	x	—	1	x	x	x	✓	✓	—	—
		Output	—	0	—	0	0/1	(SDA01/SO01) = 1 ^{Note 2} TO03 = 0	TO03 = 0				
		N-ch open drain output	—	1	—	0	0/1	(SDA01/SO01) = 1 ^{Note 2} TO03 = 0 VCOUT1 = 0 ^{Note 2}	TO03 = 0 VCOUT1 = 0 ^{Note 2}				
	TI03	Input	PIOR07 = 0 ^{Note 2}	x	—	1	x	x	x	✓	✓	—	—
	TO03	Output	PIOR07 = 0 ^{Note 2} PIOR06 = 0	0	—	0	0	(SDA01/SO01) = 1 ^{Note 2} TO03 = 0 VCOUT1 = 0 ^{Note 2}	TO03 = 0 VCOUT1 = 0 ^{Note 2}	✓	✓	—	—
	(INTP4)	Input	PIOR23 = 1	x	—	1	x	x	x	✓	✓	—	—
	(TI02)	Input	PIOR05 = 1 PIOR04 = 0	x	—	1	x	x	x	✓	✓	—	—
	(TO02)	Output	PIOR05 = 1 PIOR04 = 0	0	—	0	0	(SDA01/SO01) = 1 ^{Note 2} TO03 = 0 VCOUT1 = 0 ^{Note 2}	TO03 = 0 VCOUT1 = 0 ^{Note 2}	✓	✓	—	—
	VCOUT1	Output	PIOR33 = 0	0	—	0	0	(SDA01/SO01) = 1 TO03 = 0 TO02 = 0	TO03 = 0 TO02 = 0	✓	—	—	—
	(SDA01)	I/O	PIOR13 = 1 PIOR12 = 0	1	—	0	1	x	TO03 = 0 TO02 = 0 VCOUT1 = 0	TO03 = 0 TO02 = 0 VCOUT1 = 0	✓	—	—
(SO01)	Output	PIOR13 = 1 PIOR12 = 0	0	—	0	1	x	TO03 = 0 TO02 = 0 VCOUT1 = 0	TO03 = 0 TO02 = 0 VCOUT1 = 0	✓	—	—	—

4. 14.3 Registers Controlling Interrupt Functions(page 606)

Incorrect:

Table 14-2. Flags Corresponding to Interrupt Request Sources (2/2)

Interrupt Source	Interrupt Request Flag		Interrupt Mask Flag		Priority Specification Flag		20-bit	16-bit	10-bit	8-bit
		Register		Register		Register				
INTTM03H	TMIF03H	IF1L	TMMK03H	MK1L	TMPR003H, TMPR103H	PR01L,	✓	✓	✓	✓
INTIICA0	IICAIF0		IICAMK0		IICAPR00, IICAPR10	PR11L	✓	✓	✗	✗
INTTM02	TMIF02		TMMK02		TMPR002, TMPR102		✓	✓	✓	✓
INTTM03	TMIF03		TMMK03		TMPR003, TMPR103		✓	✓	✓	✓
INTIT	ITIF		ITMK		ITPR0, ITPR1		✓	✓	✓	✓
INTTM04	TMIF04		TMMK04		TMPR004, TMPR104		✓	✓	✓	✓
INTTM05	TMIF05		TMMK05		TMPR005, TMPR105		✓	✓	✓	✓
INTTM06	TMIF06		TMMK06		TMPR006, TMPR106		✓	✓	✓	✓
INTTM07	TMIF07	IF1H	TMMK07	MK1H	TMPR007, TMPR107	PR01H,	✓	✓	✓	✓
INTCMP0	CMPIF0		CMPMK0		CMPPR00, CMPPR10	PR11H	✓	✓	✓	✓
INTCMP1	CMPIF1		CMPMK1		CMPPR01, CMPPR11		✓	—	—	—

Correct:

Table 14-2. Flags Corresponding to Interrupt Request Sources (2/2)

Interrupt Source	Interrupt Request Flag		Interrupt Mask Flag		Priority Specification Flag		20-bit	16-bit	10-bit	8-bit
		Register		Register		Register				
INTTM03H	TMIF03H	IF1L	TMMK03H	MK1L	TMPR003H, TMPR103H	PR01L,	✓	✓	✓	✓
INTIICA0	IICAIF0		IICAMK0		IICAPR00, IICAPR10	PR11L	✓	✓	✗	✗
INTTM02	TMIF02		TMMK02		TMPR002, TMPR102		✓	✓	✓	✓
INTTM03	TMIF03		TMMK03		TMPR003, TMPR103		✓	✓	✓	✓
INTIT	ITIF		ITMK		ITPR0, ITPR1		✓	✓	✓	✓
INTTM04	TMIF04		TMMK04		TMPR004, TMPR104		✓	✓	✓	✓
INTTM05	TMIF05		TMMK05		TMPR005, TMPR105		✓	✓	✓	✓
INTTM06	TMIF06		TMMK06		TMPR006, TMPR106		✓	✓	✓	✓
INTTM07	TMIF07	IF1H	TMMK07	MK1H	TMPR007, TMPR107	PR01H,	✓	✓	✓	✓
INTCMP0	CMPIF0		CMPMK0		CMPPR00, CMPPR10	PR11H	✓	✓	✓	✓
INTCMP1	CMPIF1		CMPMK1		CMPPR01, CMPPR11		✓	—	—	—

5. CHAPTER 23 ELECTRICAL SPECIFICATIONS (T_A = -40 to +85°C) (Target)
(page 708)

Incorrect:

CHAPTER 23 ELECTRICAL SPECIFICATIONS (T_A = -40 to +85°C).~~(Target)~~

(omitted)

~~Caution 3. The electrical characteristics of the 8-pin DFN product are target values because the product is under evaluation. After the evaluation is completed, the electrical characteristics are determined and we update the user's manual.~~

6. 23.2.2 On-chip oscillator characteristics (page 710)

Incorrect:

23.2.2 On-chip oscillator characteristics^{Note 3}

(omitted)

~~Note 3. The electrical characteristics of the 8-pin DFN product are target values because the product is under evaluation. After the evaluation is completed, the electrical characteristics are determined and we update the user's manual.~~

Correct:

CHAPTER 23 ELECTRICAL SPECIFICATIONS (T_A = -40 to +85°C)

(omitted)

(deletion)

Correct:

23.2.2 On-chip oscillator characteristics

(omitted)

(deletion)

7. 23.8 Flash Memory Programming Characteristics (page 728)

Incorrect:

(omitted)
Code flash/data flash self-programming time

Correct:

(omitted)
Code flash/data flash self-programming time
[$T_A = -40$ to $+85^\circ\text{C}$, $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$]

8. 23.10 Timing of Entry to Flash Memory Programming Mode (page 729)

Incorrect:

23.10 Timing of Entry to Flash Memory Programming Mode

Correct:

23.10 Timing of Entry to Flash Memory Programming Mode
[$T_A = -40$ to $+85^\circ\text{C}$, $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$]

9. CHAPTER 24 ELECTRICAL SPECIFICATIONS ($T_A = -40$ to $+105^\circ\text{C}$, $T_A = -40$ to $+125^\circ\text{C}$) (Target) (page 730)

Incorrect:

CHAPTER 24 ELECTRICAL SPECIFICATIONS ($T_A = -40$ to $+105^\circ\text{C}$, $T_A = -40$ to $+125^\circ\text{C}$) (Target)
(omitted)

Correct:

CHAPTER 24 ELECTRICAL SPECIFICATIONS ($T_A = -40$ to $+105^\circ\text{C}$, $T_A = -40$ to $+125^\circ\text{C}$)
(omitted)
(deletion)

~~Caution 3. The electrical characteristics of the 8-pin DFN product are target values because the product is under evaluation. After the evaluation is completed, the electrical characteristics are determined and we update the user's manual.~~

10. 24.2.2 On-chip oscillator characteristics^{Note 3} (page 732)

Incorrect:

24.2.2 On-chip oscillator characteristics^{Note 3}

[T_A = -40 to +105°C: G products, T_A = -40 to +125°C: M products, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V]

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
High-speed on-chip oscillator clock frequency ^{Note 1, Note 2}	f _{HS}		1		16	MHz
High-speed on-chip oscillator clock frequency accuracy		T _A = +85 to +125°C	-2.0		+2.0	%
		T _A = -20 to +85°C	-1.0		+1.0	%
		T _A = -40 to -20°C	-1.5		+1.5	%
Low-speed on-chip oscillator clock frequency	f _{LS}			15		kHz
Low-speed on-chip oscillator clock frequency accuracy			-15		+15	%

(omitted)

~~Note 3. The electrical characteristics of the 8-pin DFN product are target values because the product is under evaluation. After the evaluation is completed, the electrical characteristics are determined and we update the user's manual.~~

Correct:

24.2.2 On-chip oscillator characteristics

[T_A = -40 to +105°C: G products, T_A = -40 to +125°C: M products, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V]

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
High-speed on-chip oscillator clock frequency ^{Note 1, Note 2}	f _{HS}		1		16	MHz
High-speed on-chip oscillator clock frequency accuracy		T _A = +85 to +125°C	-1.5		+1.5	%
		T _A = -20 to +85°C	-1.0		+1.0	%
		T _A = -40 to -20°C	-1.5		+1.5	%
Low-speed on-chip oscillator clock frequency	f _{LS}			15		kHz
Low-speed on-chip oscillator clock frequency accuracy			-15		+15	%

(omitted)

(deletion)

11. 24.8 Flash Memory Programming Characteristics-(page 750)

Incorrect:

[T_A = -40 to +105°C: G products, T_A = -40 to +125°C: M products, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V]

Item	Symbol	Condition		MIN.	TYP.	MAX.	Unit
Number of code flash rewrites <small>Note 1, Note 2</small>	C _{erwr}	Retained for 20 years	T _A = ±125°C	1000			Times
Number of data flash rewrites <small>Note 1, Note 2</small>		Retained for 1 year	T _A = +25°C		1,000,000		Times
		Retained for 5 years	T _A = ±125°C	100,000			Times
		Retained for 20 years	T _A = ±125°C	10,000			Times

(omitted)

Code flash/data flash self-programming time

12. 24.10 Timing of Entry to Flash Memory Programming Mode (page 751)

Incorrect:

Correct:

[T_A = -40 to +105°C: G products, T_A = -40 to +125°C: M products, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V]

Item	Symbol	Condition		MIN.	TYP.	MAX.	Unit
Number of code flash rewrites <small>Note 1, Note 2</small>	C _{erwr}	Retained for 20 years	T _A = +85°C	1000			Times
Number of data flash rewrites <small>Note 1, Note 2</small>		Retained for 1 year	T _A = +25°C		1,000,000		Times
		Retained for 5 years	T _A = +85°C	100,000			Times
		Retained for 20 years	T _A = +85°C	10,000			Times

(omitted)

Code flash/data flash self-programming time

[T_A = -40 to +105°C: G products, T_A = -40 to +125°C: M products, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V]

Correct:

[T_A = -40 to +105°C: G products, T_A = -40 to +125°C: M products, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V]

13. 25.1 8-pin products-(page 752)

Incorrect:

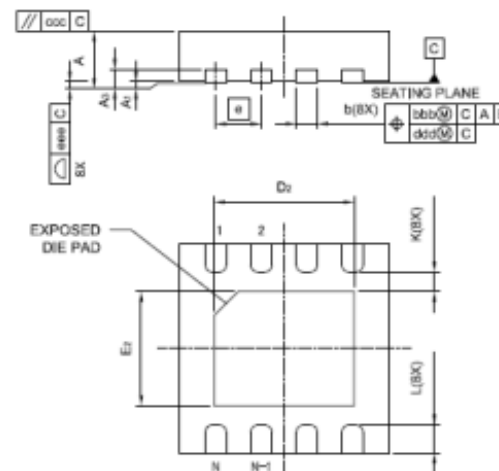
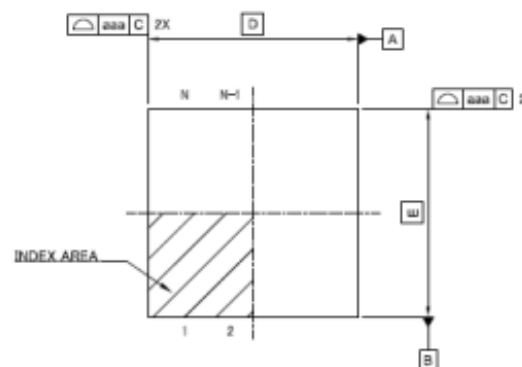
R5F12008MNS, R5F12008GNS, R5F12008ANS
 R5F12007MNS, R5F12007GNS, R5F12007ANS

~~After the package outline drawings are determined, we update the user's manual.~~

Correct:

R5F12008MNS, R5F12008GNS, R5F12008ANS
 R5F12007MNS, R5F12007GNS, R5F12007ANS

JEITA Package code	RENESAS code	MASS(TYP.)(g)
P-HWSON8-3x3-0.65	PWSN0008JG-A	0.02



Reference Symbol	Dimension In Millimeters		
	Min.	Nom.	Max.
A	—	—	0.80
A ₁	0.00	—	0.05
A ₂	0.203 REF.		
b	0.25	0.30	0.35
D	3.00		
E	3.00		
E ₁	0.65		
N	8		
L	0.35	0.40	0.45
K	0.20	—	—
D ₁	1.95	2.00	2.05
E ₂	1.60	1.65	1.70
aaa	—	—	0.15
bbb	—	—	0.10
ccc	—	—	0.10
ddd	—	—	0.05
eee	—	—	0.05