To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: http://www.renesas.com

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Renesas Electronics Corporation

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RENESAS TECHNICAL UPDATE

Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan
Renesas Technology Corp.

Product Category	MPU&MCU		Document No.	TN-H8*-A403A/E	Rev.	1.00
Title	Correction of errors in the H8SX/1650 Group Hardware Manual		Information Category	Technical Notification		
Applicable Product	H8SX/1650 Group	Lot No. All lots	Reference Document	H8SX/1650 Group Hardware Manual (REJ09B0311-0200)		

We would like to inform you of the correction of errors in the above listed hardware manuals. Please refer to the following for details.

<Corrections>

Section 1 Overview

(1) Page 2, table 1.1 Overview of Functions

[Before Change]

Classification	Module/ Function	Description
CPU	CPU	- Description omitted (no changes) - • Supports multiply-and-accumulate instructions (16 × 16 + 32 → 32 bits)

[After Change]

Classification	Module/ Function	Description
CPU	CPU	- Description omitted (no changess) - • Supports multiply-and-accumulate instructions (**16 × 16 + 42 → 42 bits**)

Section 5 Interrupt Controller

Deletion of DTCERF, DTCERG, and DTCERH in DTCER

(1) Page 113 to 114, 5.6.5 DTC Activation by Interrupt

[Before Change]

(1) Selection of Interrupt Sources

Each interrupt source is set for a DTC activation request or a CPU interrupt request by the DTCE bit in DTCERA to DTCERH of the DTC.

- Description omitted (no changes) –

(2) Priority Determination

- Description omitted (no changes) –

(3) Operation Order

- Description omitted (no changes) –

Table 5.6 lists the selection of interrupt sources and interrupt source clear control by means of the setting of the DTCE bit in DTCERA to DTCERH of the DTC, and the DISEL bit in MRB of the DTC.

[After Change]

(1) Selection of Interrupt Sources

Each interrupt source is set for a DTC activation request or a CPU interrupt request by the DTCE bit in DTCERA to **DTCERE** of the DTC.

- Description omitted (no changes) –

(2) Priority Determination

- Description omitted (no changes) –

(3) Operation Order

- Description omitted (no changes) –

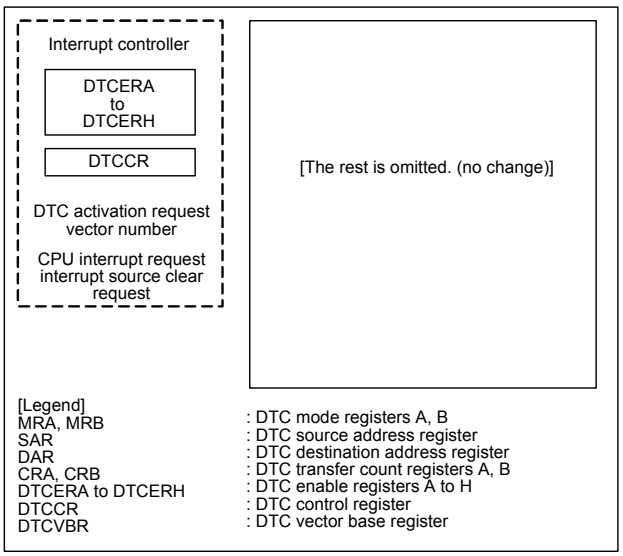
Table 5.6 lists the selection of interrupt sources and interrupt source clear control by means of the setting of the DTCE bit in DTCERA to **DTCERE** of the DTC, and the DISEL bit in MRB of the DTC.

Section 7 Data Transfer Controller

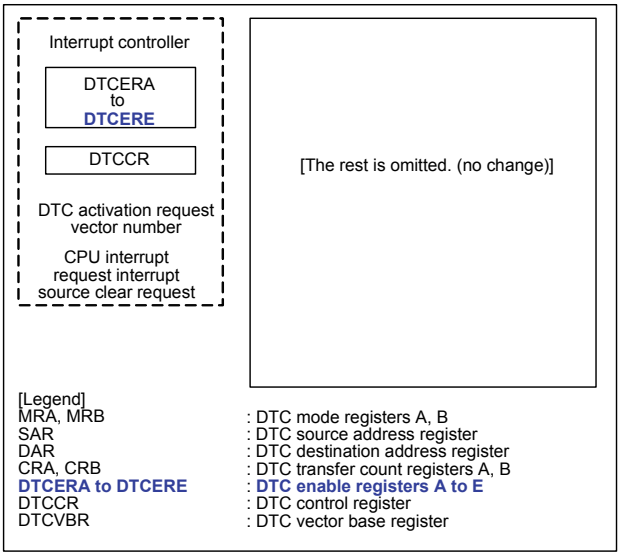
Deletion of DTCERF, DTCERG, and DTCERH in DTCER

(1) Page 218, DTCER description in figure 7.1

[Before Change]



[After Change]



(2) Page 219, section 7.2 Register Descriptions

Deletion of DTCERF, DTCERG, and DTCERH in DTCER

[Before Change]

- DTC enable registers A to H (DTCERA to DTCERH)

[After Change]

- DTC enable registers A to **E** (DTCERA to **DTCERE**)

(3) Page 225, section 7.2.7 DTC Enable Register

Deletion of DTCERF, DTCERG, and DTCERH in the DTCER descriptions

[Before Change]

7.2.7 DTC Enable Register A to H (DTCERA to DTCERH)

DTCER, which is comprised of eight registers, DTCERA to DTCERH, is a register that specifies DTC activation interrupt sources.

[After Change]

7.2.7 DTC Enable Register A to **E** (DTCERA to **DTCERE**)

DTCER, which is comprised of **five** registers, DTCERA to DTCERH, is a register that specifies DTC activation interrupt sources.

Section 8 I/O Ports

(1) Page 289, PA1 description in table 8.5 Available Output Signals and Settings in Each Port

[Before Change]

Port		Output Specification Signal Name	Output Signal Name	Signal Selection Register Settings	Peripheral Module Settings
PA	1	$\overline{\text{BACK}}$_OE	$\overline{\text{BACK}}$		BCR1.BRLE = 1
		(RD/$\overline{\text{WR}}$)_OE	RD/$\overline{\text{WR}}$		PFCR2.REWRE = 1 or SRAMCR.BCSELn = 1

[After Change]

Port		Output Specification Signal Name	Output Signal Name	Signal Selection Register Settings	Peripheral Module Settings
PA	1	$\overline{\text{BACK}}$_OE	$\overline{\text{BACK}}$		BCR1.BRLE = 1
		(RD/$\overline{\text{WR}}$)_OE	RD/$\overline{\text{WR}}$		PFCR2. **RDWRE** = 1 or SRAMCR.BCSELn = 1

Section 11 8-bit Timer

(1) Page 431, section 11.7.2 A/D Converter Activation

[Before Change]

The A/D converter can be activated only by TMR_0 compare match A.

If the ADTE bit in TCSR_0 is set to 1 when the CMFA flag in TCSR_0 is set to 1 by the occurrence of TMR_0 compare match A, a request to start A/D conversion is sent to the A/D converter. If the 8-bit timer conversion start trigger has been selected on the A/D converter side at this time, A/D conversion is started.

[After Change]

The A/D converter can be activated only by **TMR_0 or TMR_2 compare match A**.

If the ADTE bit in TCSR_0 is set to 1 when the CMFA flag in TCSR_0 is set to 1 **by the occurrence of compare match A**, a request to start A/D conversion is sent to the A/D converter. If the 8-bit timer conversion start trigger has been selected on the A/D converter side at this time, A/D conversion is started.

Section 13 Serial Communication Interface

(1) Page 463, the name of bit 4 in Serial Status Register (SSR)

[Before Change]

Serial Status Register (SSR)

- When SMIF in SCMR = 0

Bit	7	6	5	4	3	2	1	0
Bit Name	TDRE	RDRF	ORER	FRE	PER	TEND	MPB	MPBT
Initial Value	1	0	0	0	0	1	0	0
R/W	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R	R	R/W

Note: * Only 0 can be written, to clear the flag.

[After Change]

- When SMIF in SCMR = 0

Bit	7	6	5	4	3	2	1	0
Bit Name	TDRE	RDRF	ORER	**FER**	PER	TEND	MPB	MPBT
Initial Value	1	0	0	0	0	1	0	0
R/W	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R	R	R/W

Note: * Only 0 can be written, to clear the flag.

Section 19 List of Registers

(1) Page 592, section 19.1 Register Addresses

Deletion of DTCERF, DTCERG, and DTCERH in DTCER

[Before Change]

Register Name	Abbreviation	Number of Bits	Address	Module	Data Width	Access Cycles (Read/Write)
– Description omitted (no changes) –						
DTC enable register E	DTCERE	16	H'FFF28	INTC	16	2Iφ/3Iφ
DTC enable register F	**DTCERF**	**16**	**H'FFF2A**	**INTC**	**16**	**2Iφ/3Iφ**
DTC enable register G	**DTCERG**	**16**	**H'FFF2C**	**INTC**	**16**	**2Iφ/3Iφ**
DTC enable register H	**DTCERH**	**16**	**H'FFF2E**	**INTC**	**16**	**2Iφ/3Iφ**
DTC control register	DTCCR	8	H'FFF30	INTC	16	2Iφ/3Iφ
– Description omitted (no changes) –						

[After Change]

Register Name	Abbreviation	Number of Bits	Address	Module	Data Width	Access Cycles (Read/Write)
– Description omitted (no changes) –						
DTC enable register E	DTCERE	16	H'FFF28	INTC	16	2Iφ/3Iφ
DTC control register	DTCCR	8	H'FFF30	INTC	16	2Iφ/3Iφ
– Description omitted (no changes) –						

(2) Page 601 to 602, section 19.2 Register Bits

Deletion of DTCERF, DTCERG, and DTCERH in INTC

[Before Change]

Register Abbreviation	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0	Module
				– Description omitted (no changes) –					TPU_5
DTCERA to DTCERD				– Description omitted (no changes) –					INTC
DTCERE	DTCE15	DTCE14	DTCE13	DTCE12	DTCE11	DTCE10	DTCE9	DTCE8	
	DTCE7	DTCE6	DTCE5	DTCE4	DTCE3	DTCE2	DTCE1	DTCE0	
DTCERF	**DTCE15**	**DTCE14**	**DTCE13**	**DTCE12**	**DTCE11**	**DTCE10**	**DTCE9**	**DTCE8**	
	DTCE7	**DTCE6**	**DTCE5**	**DTCE4**	**DTCE3**	**DTCE2**	**DTCE1**	**DTCE0**	
DTCERG	**DTCE15**	**DTCE14**	**DTCE13**	**DTCE12**	**DTCE11**	**DTCE10**	**DTCE9**	**DTCE8**	
	DTCE7	**DTCE6**	**DTCE5**	**DTCE4**	**DTCE3**	**DTCE2**	**DTCE1**	**DTCE0**	
DTCERH	**DTCE15**	**DTCE14**	**DTCE13**	**DTCE12**	**DTCE11**	**DTCE10**	**DTCE9**	**DTCE8**	
	DTCE7	**DTCE6**	**DTCE5**	**DTCE4**	**DTCE3**	**DTCE2**	**DTCE1**	**DTCE0**	
DTCCR	–	–	–	RRS	RCHNE	–	–	ERR	
INTCR to ISR				– Description omitted (no changes) –					
				– Description omitted (no changes) –					I/O port

[After Change]

Register Abbreviation	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0	Module
				– Description omitted (no changes) –					TPU_5
DTCERA to DTCERD				– Description omitted (no changes) –					INTC
DTCERE	DTCE15	DTCE14	DTCE13	DTCE12	DTCE11	DTCE10	DTCE9	DTCE8	
	DTCE7	DTCE6	DTCE5	DTCE4	DTCE3	DTCE2	DTCE1	DTCE0	
DTCCR	–	–	–	RRS	RCHNE	–	–	ERR	
INTCR to ISR				– Description omitted (no changes) –					
				– Description omitted (no changes) –					I/O port

(3) Page 611, section 19.3 Register States in Each Operating Mode

Deletion of DTCERF, DTCERG, and DTCERH in INTC

[Before Chenage]

Register Abbreviation	Reset	Module Stop State	Sleep Mode	All-Module-Clock-Stop Mode	Software Standby Mode	Hardware Standby Mode	Module
		– Description omitted (no changes) –					TPU_5
DTCERA to DTCERD		– Description omitted (no changes) –					INTC
DTCERE	Initialized	–	–	–	–	Initialized	
DTCERF	**Initialized**	**–**	**–**	**–**	**–**	**Initialized**	
DTCERG	**Initialized**	**–**	**–**	**–**	**–**	**Initialized**	
DTCERH	**Initialized**	**–**	**–**	**–**	**–**	**Initialized**	
DTCCR	Initialized	–	–	–	–	Initialized	
INTCR to ISR		– Description omitted (no changes) –					
		– Description omitted (no changes) –					I/O port

[After Change]

Register Abbreviation	Reset	Module Stop State	Sleep Mode	All-Module-Clock-Stop Mode	Software Standby Mode	Hardware Standby Mode	Module
		– Description omitted (no changes) –					TPU_5
DTCERA to DTCERD		– Description omitted (no changes) –					INTC
DTCERE	Initialized	–	–	–	–	Initialized	
DTCCR	Initialized	–	–	–	–	Initialized	
INTCR to ISR		– Description omitted (no changes) –					
		– Description omitted (no changes) –					I/O port