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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-H8*-A426A/E	Rev.	1.00
Title	Additional Usage Notes on Interrupts		Information Category	Technical Notification		
Applicable Product	H8SX Group	Lot No. All lots	Reference Document	Refer to the "Reference Documents" section below		

Thank you for your consistent patronage of Renesas semiconductor products.

We would like to inform you of additional usage notes in the description about the interrupt controller in the H8SX Group Hardware Manual. Please read these additional notes carefully before using the H8SX Group products.

1. Additional Usage Note on Conflict between Interrupt Generation and Disabling

As described in the Usage Notes of the interrupt controller in the hardware manual, when there is a conflict between interrupt generation and interrupt disabling by clearing the interrupt enable bit or interrupt source flag, the interrupt exception handling for that interrupt may be executed on completion of the interrupt disabling instruction. For this note, we found additional applicable behavior and register setting.

If this conflict occurs in interrupt control mode 2, the interrupt exception handling with priority equal to or lower than the interrupt mask level (I2 to I0 setting in EXR) may be executed on completion of the interrupt disabling instruction.

In addition, note that the interrupt priority register (IPR) may generate this conflict.

Table 1 Registers that May Generate Conflict between Interrupt Generation and Disabling

Interrupt Control Mode	Applicable Register Setting	Hardware Manual
Mode 0	Interrupt enable bit clearing	Described
	Interrupt source flag clearing	Described
Mode 2	Interrupt enable bit clearing	Described
	Interrupt source flag clearing	Described
	Interrupt disabling through IPR setting	Not described

When a conflict between interrupt generation and disabling may occur in your system, avoid it by masking interrupts as shown in figure 1. There is no additional note about interrupt control mode 0, but if a conflict may occur in this mode, it should also be avoided through the procedure shown in figure 1.

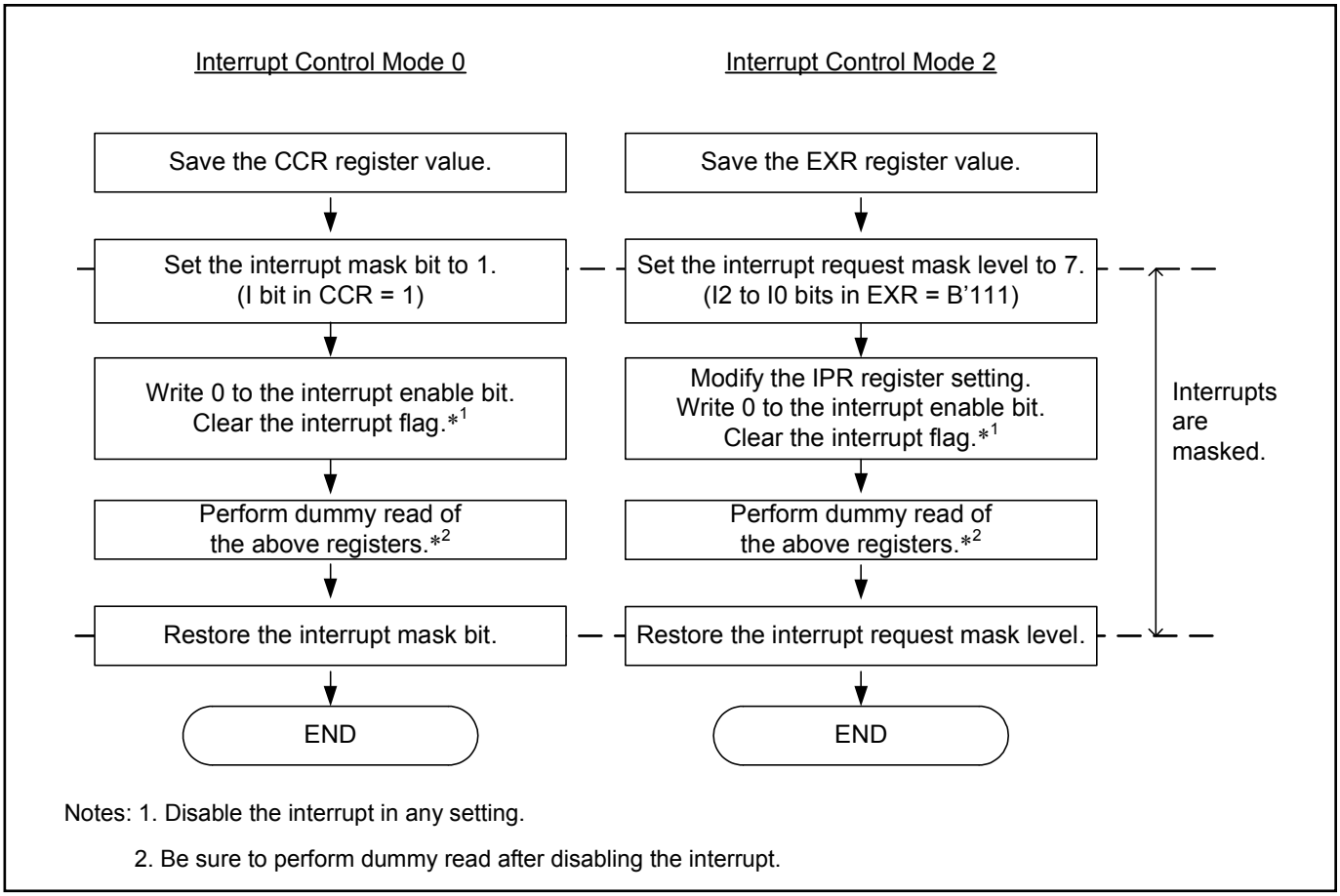

Figure 1 Interrupt Masking Procedure to Avoid Conflict between Interrupt Generation and Disabling

2. Additional Usage Note on Interrupt Source Flag Clearing in Interrupt Processing Routine

As described in the Usage Notes of the interrupt controller in the hardware manual, to clear an interrupt source flag in a peripheral module by the CPU, the flag must be read after being cleared within the interrupt processing routine for synchronization with the peripheral module. For this note, we found another applicable register setting.

Table 2 Registers that Must be Read after being Cleared

Interrupt Control Mode	Module	Register that Must be Read after being Cleared	Hardware Manual
Modes 0 and 2	Peripheral modules	Interrupt source flag	Described
		Interrupt enable bit	Not described
	DMAC and IRQ	None	—

When clearing an interrupt source flag or interrupt enable bit of a peripheral module within the interrupt processing routine, read the corresponding register. If both the source flag and enable bit for a single interrupt are cleared in the interrupt processing routine, read either one (it is not necessary to read both).

When manipulating the enable bit, source flag, or IPR setting for an interrupt that has a higher priority than the CPU interrupt mask level in the interrupt processing routine, be careful about conflict between interrupt generation and disabling described in section 1 above.

3. Hardware Manual Modifications

According to the above additions to the Usage Notes, the descriptions in the hardware manual are modified as follows.

[Modification 1]

7.8.1 Conflict between Interrupt Generation and Disabling

Note: The following example shows the description in the H8SX/1665 Group, H8SX/1665M Group Hardware Manual.

[Before Change]

When an interrupt enable bit is cleared to 0 to mask the interrupt, the masking becomes effective after execution of the instruction.

When an interrupt enable bit is cleared to 0 by an instruction such as BCLR or MOV, if an interrupt is generated during execution of the instruction, the interrupt concerned will still be enabled on completion of the instruction, and so interrupt exception handling for that interrupt will be executed on completion of the instruction. However, if there is an interrupt request with priority over that interrupt, interrupt exception handling will be executed for the interrupt with priority, and another interrupt will be ignored. The same also applies when an interrupt source flag is cleared to 0. Figure 7.7 shows an example in which the TCIEV bit in TIER of the TPU is cleared to 0. The above conflict will not occur if an enable bit or interrupt source flag is cleared to 0 while the interrupt is masked.

[After Change]

When an interrupt enable bit is cleared to 0 to mask the interrupt, the masking becomes effective after execution of the instruction.

When an interrupt enable bit is cleared to 0 by an instruction such as BCLR or MOV, if an interrupt is generated during execution of the instruction, the interrupt concerned will still be enabled on completion of the instruction, and so interrupt exception handling for that interrupt will be executed on completion of the instruction. If this conflict occurs in interrupt control mode 2, the interrupt exception handling with priority equal to or lower than the CPU interrupt mask level specified in the I2 to I0 bits in EXR may be executed on completion of the interrupt disabling instruction. However, if there is an interrupt request with priority over that interrupt, interrupt exception handling will be executed for the interrupt with priority, and another interrupt will be ignored. The same also applies when an interrupt source flag is cleared to 0. In interrupt control mode 2, the same also applies when the interrupt is disabled by modifying the IPR setting. Figure 7.7 shows an example in which the TCIEV bit in TIER of the TPU is cleared to 0. The above conflict will not occur if an enable bit or interrupt source flag is cleared to 0 or IPR is modified while the interrupt is masked.

Figure 7.8 shows the interrupt masking procedure to avoid this conflict.

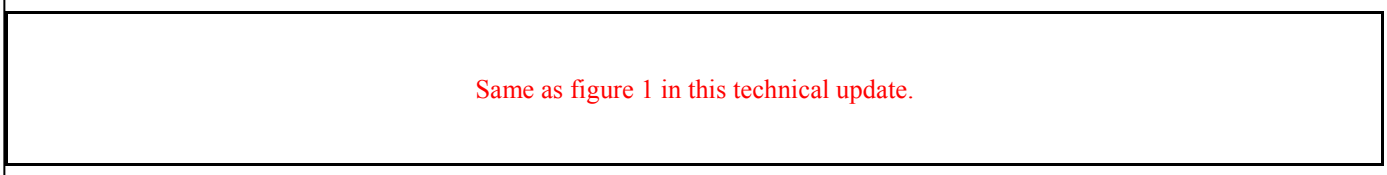

Figure 7.8 Procedure for Avoiding Interrupt Conflict

[Modification 2]

7.8.6 Interrupts of Peripheral Modules

Note: The following example shows the description in the H8SX/1665 Group, H8SX/1665M Group Hardware Manual.

[Before Modification]

To clear an interrupt source flag by the CPU using an interrupt function of a peripheral module, the flag must be read from after clearing within the interrupt processing routine. This makes the request signal synchronized with the peripheral module clock.

[After Modification]

To clear an interrupt source flag or an interrupt enable bit by the CPU using an interrupt function of a peripheral module, the flag or enable register must be read from after clearing within the interrupt processing routine. This makes the request signal synchronized with the peripheral module clock.

Reference Documents:

H8SX/1520R Group Hardware Manual (REJ09B0282-0100)
H8SX/1520 Group Hardware Manual (REJ09B0104-0300)
H8SX/1544 Group Hardware Manual (REJ09B0381-0300)
H8SX/1582 Hardware Manual (REJ09B0199-0200)
H8SX/1622 Group Hardware Manual (REJ09B0414-0200)
H8SX/1635 Group, H8SX/1635L Group Hardware Manual (REJ09B0496-0200)
H8SX/1638 Group, H8SX/1638L Group Hardware Manual (REJ09B0364-0200)
H8SX/1645 Group H8SX/1645L Group Hardware Manual (REJ09B0497-0200)
H8SX/1648, H8SX/1648A, H8SX/1648L,
H8SX/1648G, H8SX/1648H Group Hardware Manual (REJ09B0365-0200)
H8SX/1650 Group Hardware Manual (REJ09B0311-0200)
H8SX/1651 Group Hardware Manual (REJ09B0248-0200)
H8SX/1653 Group Hardware Manual (REJ09B0219-0100)
H8SX/1655 Group H8SX/1655M Group Hardware Manual (REJ09B0499-0200)
H8SX/1657 Group Hardware Manual (REJ09B0341-0200)
H8SX/1658R Group, H8SX/1658M Group Hardware Manual (REJ09B0413-0200)
H8SX/1663 Group Hardware Manual (REJ09B0294-0100)
H8SX/1665 Group, H8SX/1665M Group Hardware Manual (REJ09B0498-0200)
H8SX/1668R Group, H8SX/1668M Group Hardware Manual (REJ09B0412-0200)
H8SX/1720S Group Hardware Manual (REJ09B0563-0100)