Date: May 12, 2016

RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-SY*-A004A/E	Rev.	1.00
Title	Additional precaution about the operation of Flash memory		Information Category	Technical Notification		
Applicable Product	Synergy S7 Series S7G2	Lot No. All lots	Reference Document	S7G2 User's Manual: Microcontrollers, Rev.1.00		

1. Additional precaution about the operation of Flash memory

• Additional step to set up the flash cache and prepare to rewrite the flash memory in the section 54.4,

Step comparison as follows:

[Before]

54.4 Operation

Use the FCACHEE register to set up and enable flash operation.

To set up the flash cache and prepare to rewrite the flash memory:

1. Disable the flash cache by resetting FCACHEE.FCACHEEN.*1
2. Invalidate the flash cache by setting FCACHEIV.FCACHEIV.
3. Check that FCACHEIV.FCACHEIV is 0.
4. Enable the flash cache by setting FCACHEE.FCACHEEN.

Note 1. It is not necessary to disable the flash cache on the first setup after reset

[After]

54.4 Operation

Use the FCACHEE register to set up and enable flash operation.

To set up the flash cache and prepare to rewrite the flash memory:

1. Disable the flash cache by resetting FCACHEE.FCACHEEN.*1
2. Changing the read mode of Flash *2 if necessary.
3. Invalidate the flash cache by setting FCACHEIV.FCACHEIV.
4. Check that FCACHEIV.FCACHEIV is 0.
5. Enable the flash cache by setting FCACHEE.FCACHEEN.

Note 1. It is not necessary to disable the flash cache on the first setup after reset

Note 2. Operation of the SOPCCR and FLWT

2. Additional information about the section 11.5.1 Setting the Operating Power Control Mode

• Detailed procedure for switching operating power control modes in case of using the flash cache.

(1) Switching from a higher to a lower power mode

Example 2: To switch from High-speed mode to Subosc-speed mode:

Operation begins in High-speed mode

1. Disable the flash cache by resetting FCACHEE.FCACHEEN when the flash cache is cacheable in High-speed mode.
2. Change the clock source to the sub-clock oscillator. Turn off HOCO, MOCO, LOCO, main oscillator, and PLL.
3. Confirm that all clock sources except the sub-clock oscillator are stopped.
4. Set the FLWT.FLWT to 000
5. Confirm that the SOPCCR.SOPCMTSF flag is 0 (indicates transition completed).
6. Set the SOPCCR.SOPCM bit to 1 (Subosc-speed mode).
7. Confirm that the SOPCCR.SOPCMTSF flag is 0 (indicates transition completed).

Set the following steps when the flash cache is cacheable in Subosc-speed mode.

8. Invalidate the flash cache by setting FCACHEIV.FCACHEIV.
9. Check that FCACHEIV.FCACHEIV is 0.
10. Enable the flash cache by setting FCACHEE.FCACHEEN.

Operation is now in Subosc-speed mode.

(2) Switching from a lower to a higher power mode

Example 1: To switch from Subosc-speed mode to High-speed mode:

Operation begins in Subosc-speed mode.

1. Disable the flash cache by resetting FCACHEE.FCACHEEN when the flash cache is cacheable in Subosc-speed mode
2. Confirm that the SOPCCR.SOPCMTSF flag is 0 (indicates transition completed).
3. Set the SOPCCR.SOPCM bit to 0 (High-speed mode).
4. Confirm that the SOPCCR.SOPCMTSF flag is 0 (indicates transition completed).
5. Change the appropriate wait cycle for the clock frequency by setting the FLWT.FLWT.
6. Turn on the oscillator wanted in High-speed mode.
7. Set the frequency of each clock lower than the maximum operating frequency for High- or Low-speed mode.

Set the following steps when the flash cache is cacheable in High-speed mode.

8. Invalidate the flash cache by setting FCACHEIV.FCACHEIV.
9. Check that FCACHEIV.FCACHEIV is 0.
10. Enable the flash cache by setting FCACHEE.FCACHEEN.

Operation is now in High-speed mode.