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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-RX*-A072A/E	Rev.	1.00
Title	Addition of a LGA package for RX21A Group		Information Category	Technical Notification		
Applicable Product	RX21A Group	Lot No. All	Reference Document	RX21A Group User's Manual: Hardware Rev.1.00 (R01UH0251EJ0100)		

This document describes the discription of the additional LGA package for 'RX21A Group User's Manual: Hardware Rev.1.00.' Changes are underlined in the list below.

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Add LGA package to the Features.

PLQP0100KB-A 14 X 14 mm, 0.5-mm pitch

PLQP0080KB-A 12 X 12 mm, 0.5-mm pitch

PLQP0064KB-A 10 X 10 mm, 0.5-mm pitch

PTLG0100JA-A 7X7mm, 0.65-mm pitch

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Add LGA package to 'Table 1.1 Outline of Specifications (4 / 4)'.

Table 1.1 Outline of Specifications (4 / 4)

Classification	Module/Function	Description
Package		100-pin LQFP (PLQP0100KB-A) 14 x 14 mm, 0.5-mm pitch 80-pinLQFP (PLQP0080KB-A) 12 x 12mm, 0.5-mm pitch 64-pinLQFP (PLQP0064KB-A) 10 x 10mm, 0.5-mm pitch **100-pinTFLGA (PTLG0100JA-A) 7 x 7mm, 0.65-mm pitch**

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Add LGA package to ‘Table 1.2 Comparison of Functions for Different Packages’.

Table 1.2 Comparison of Functions for Different Packages

Module/Functions	RX21A Group		
	100 Pins	80 Pins	64 Pins
Package	100-pin LQFP **100-pin TFLGA**	80-pin LQFP	64-pin LQFP

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Add Part. No.’s of LGA package and a note to ‘Table 1.3 List of Products’.

Table 1.3 List of Products

Group	Part No.	Package	ROM Capacity	RAM Capacity	E2 DataFlash	Operating Frequency (Max.)	Operating temperature
RX21A	R5F521A8BDFP	PLQP0100KB-A	512 Kbytes	64 Kbytes	64 Kbytes	50MHz	-40 to +85°C
	R5F521A8BDFN	PLQP0080KB-A					
	R5F521A8BDFM	PLQP0064KB-A					
	R5F521A8BDLJ	**PTLG0100JA-A**					
	R5F521A7BDFP	PLQP0100KB-A	384 Kbytes	64 Kbytes	64 Kbytes		
	R5F521A7BDFN	PLQP0080KB-A					
	R5F521A7BDFM	PLQP0064KB-A					
	R5F521A7BDLJ	**PTLG0100JA-A**					
	R5F521A6BDFP	PLQP0100KB-A	256 Kbytes	32 Kbytes	64 Kbytes		
	R5F521A6BDFN	PLQP0080KB-A					
	R5F521A6BDFM	PLQP0064KB-A					
	R5F521A6BDLJ	**PTLG0100JA-A**					
	R5F521A8BGFP	PLQP0100KB-A	512 Kbytes	64 Kbytes	64 Kbytes	50MHz	-40 to +105°C ***1**
	R5F521A8BGFN	PLQP0080KB-A					
	R5F521A8BGFM	PLQP0064KB-A					
	R5F521A7BGFP	PLQP0100KB-A	384 Kbytes				
	R5F521A7BGFN	PLQP0080KB-A					
	R5F521A7BGFM	PLQP0064KB-A					
	R5F521A6BGFP	PLQP0100KB-A	256 Kbytes	32 Kbytes			
	R5F521A6BGFN	PLQP0080KB-A					
	R5F521A6BGFM	PLQP0064KB-A					

Note 1. Contact Renesas Electronics when G version is to be used.

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Add LGA package type to ‘Figure 1.1 How to Read the Product Part No., Memory Capacity, and Package Type’.

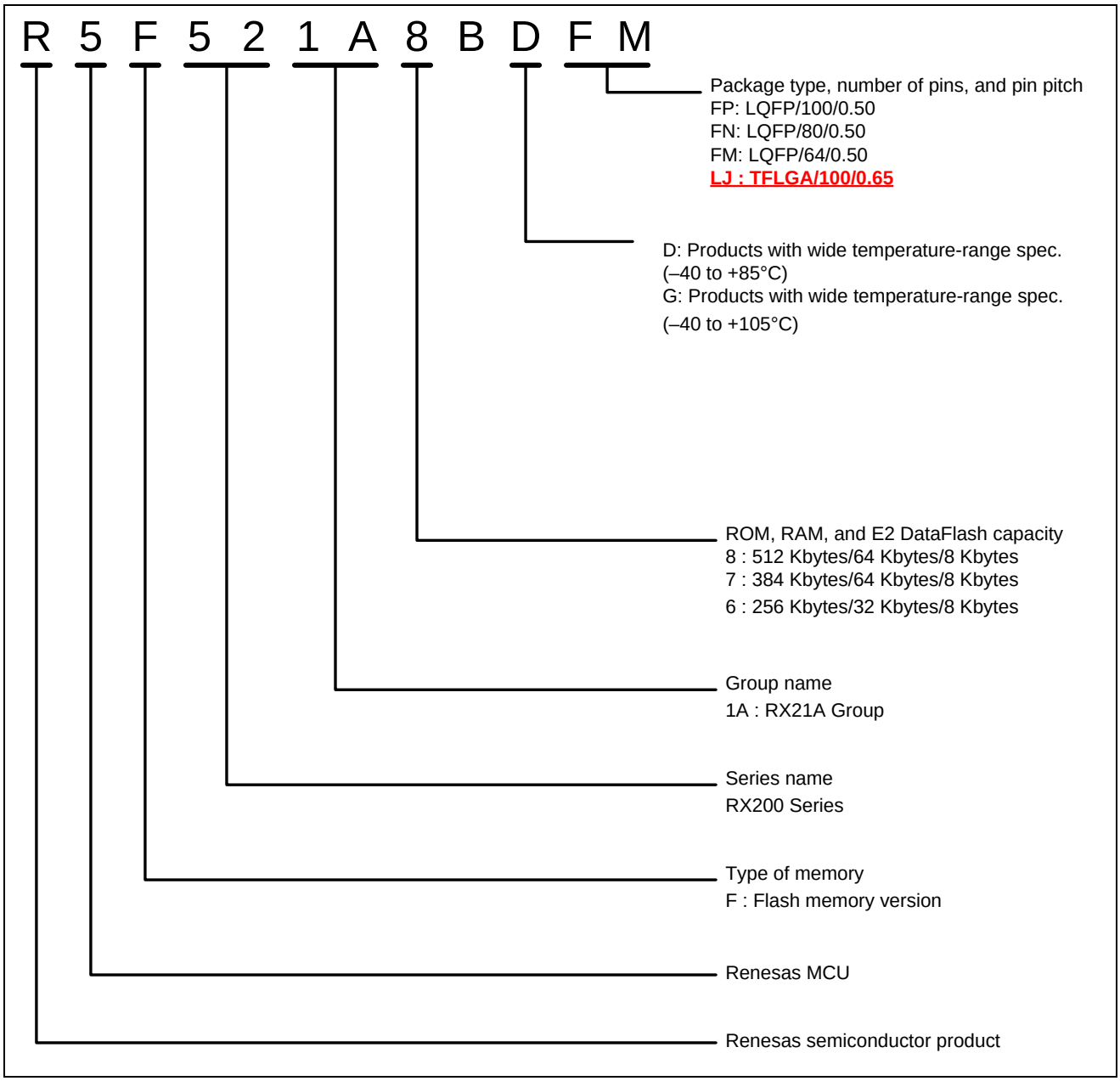

Figure 1.1 How to Read the Product Part No., Memory Capacity, and Package Type

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Add ‘Figure 1.6 Pin Assignments of the 100-Pin TFLGA (Upper Perspective View)’ next to Figure 1.6.

RX21A Group
PTLG0100JA-A
(100-pin TFLGA)
(Upper perspective view)

	10	9	8	7	6	5	4	3	2	1	
K	PC2	PC3	PC5	P51	PH1	PH2	P14	P20	P22	P23	K
J	PC1	PC0	PC4	P50	PH3	PH0	P13	P17	P21	P24	J
H	PB7	PB6	PC6	PC7	P54	P55	P15	P16	P25	P26	H
G	VCC	PB1	PB4	PB5	P52	P53	P27	P30	P31	P33	G
F	VSS	PA7	PB0	PB2	PB3	P12	P32	P35	VCC	P36/ EXTAL	F
E	PA3	PA5	PA4	PA6	PA2	P41	P34	RES#	VSS	P37/ XTAL	E
D	PA0	PA1	PE7	PE6	ANDS5	ANDS6	PJ1	MD	XCOUT	XCIN	D
C	ANDS0N	BGR_BO	ANDS3P	VREFDSL	ANDS4	P42	VREFH0	PJ3	VREFL	VCL	C
B	ANDS0P	ANDS2P	ANDS3N	AVCCA	VREFDSH	ANDSSG	P40	AVCC0	AVSS0	P03	B
A	ANDS1N	ANDS1P	ANDS2N	AVSSA	VCOMDS	P43	VREFL0	P07	VREFH	P05	A
	10	9	8	7	6	5	4	3	2	1	

Note: . This figure indicates the power supply pins and I/O port pins. For the pin configuration, see the table “List of Pins and Pin Functions (100-Pin TFLGA)”.

Note: . For the position of A1 pin in the package, see “Package Dimensions”.

Figure 1.6 Pin Assignments of the 100-Pin TFLGA (Upper Perspective View)

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Add ‘Table 1.8 List of Pins and Pin Functions (100-Pin TFLGA)’.

Pin No.	Power Supply, Clock, System Control	I/O Port	Timers (MTU, TMR, POE)	Communication (SCIc, RSPI, RIIC)	Others
A1		P05			AN5/DA1
A2	VREFH				
A3		P07			AN6/ADTRG0#
A4	VREFL0				
A5		P43			AN3
A6	VCOMDS				
A7	AVSSA				
A8					ANDS2N
A9					ANDS1P
A10					ANDS1N
B1		P03			AN4/DA0
B2	AVSS0				
B3	AVCC0				
B4		P40			AN0
B5	ANDSSG				
B6	VREFDSH				
B7	AVCCA				
B8					ANDS3N
B9					ANDS2P
B10					ANDS0P
C1	VCL				
C2	VREFL				
C3		PJ3	MTIOC3C	CTS6#/RTS6#/SS6#	
C4	VREFH0				
C5		P42			AN2
C6					ANDS4
C7	VREFDSL				
C8					ANDS3P
C9	BGR_BO				
C10					ANDS0N
D1	XCIN				
D2	XCOUT				
D3	MD				FINED
D4		PJ1	MTIOC3A		
D5					ANDS6
D6					ANDS5
D7		PE6		MOSIB	IRQ6
D8		PE7		MISOB	IRQ7-DS
D9		PA1	MTIOC0B/MTCLKC	SCK5/SSLA2	CVREFA
D10		PA0	MTIOC4A	SSLA1	CACREF/CMPA1
E1	XTAL	P37			
E2	VSS				
E3	RES#				
E4		P34	MTIOC0A/TMCI3/POE2#	SCK6	IRQ4
E5		P41			AN1
E6		PA2		RXD5/SMISO5/SSCL5/ IRRXD5/SSLA3	CMPA2
E7		PA6	MTIC5V/MTCLKB/TMCI3/POE2#	CTS5#/RTS5#/SS5#/MOSIA	CVREFB0
E8		PA4	MTIC5U/MTCLKA/TMRI0	TXD5/SMOSI5/SSDA5/ IRTXD5/SSLA0	IRQ5-DS/CVREFB1
E9		PA5		RSPCKA	
E10		PA3	MTIOC0D/MTCLKD	RXD5/SMISO5/SSCL5/ IRRXD5	IRQ6-DS/CMPB1
F1	EXTAL	P36			
F2	VCC				
F3		P35			NMI
F4		P32	MTIOC0C/TMO3	TXD6/SMOSI6/SSDA6	IRQ2-DS/RTCOUT/RTCIC2

Pin No.	Power Supply, Clock, System Control	I/O Port	Timers (MTU, TMR, POE)	Communication (SCIc, RSPI, RIIC)	Others
F5		P12	TMCI1	SCL0	IRQ2
F6		PB3	MTIOC0A/MTIOC4A/TMO0/POE3#	SCK6	
F7		PB2		CTS6#/RTS6#/SS6#	
F8		PB0	MTIC5W	RXD6/SMISO6/SSCL6/ RSPCKA	CMPB0
F9		PA7		MISOA	
F10	VSS				
G1		P33	MTIOC0D/TMRI3/POE3#	RXD6/SMISO6/SSCL6	IRQ3-DS
G2		P31	MTIOC4D/TMCI2	CTS1#/RTS1#/SS1#/SSLB0	IRQ1-DS/RTCIC1
G3		P30	MTIOC4B/TMRI3/POE8#	RXD1/SMISO1/SSCL1/MISOB	IRQ0-DS/RTCIC0
G4		P27	MTIOC2B/TMCI3	SCK1/RSPCKB	
G5		P53			
G6		P52		SSLB3	
G7		PB5	MTIOC2A/MTIOC1B/TMRI1/POE1#	SCK9	
G8		PB4		CTS9#/RTS9#/SS9#	
G9		PB1	MTIOC0C/MTIOC4C/TMCI0	TXD6/SMOSI6/SSDA6	IRQ4-DS
G10	VCC				
H1		P26	MTIOC2A/TMO1	TXD1/SMOSI1/SSDA1/MOSIB	
H2		P25	MTIOC4C/MTCLKB		ADTRG0#
H3		P16	MTIOC3C/MTIOC3D/TMO2	TXD1/SMOSI1/SSDA1/MOSIA/SCL0-DS	IRQ6/RTCOUT/ADTRG0#
H4		P15	MTIOC0B/MTCLKB/TMCI2	RXD1/SMISO1/SSCL1	IRQ5
H5		P55	MTIOC4D/TMO3		
H6		P54	MTIOC4B/TMCI1		
H7		PC7	MTIOC3A/TMO2/MTCLKB	TXD8/SMOSI8/SSDA8/MISOA	CACREF
H8		PC6	MTIOC3C/MTCLKA/TMCI2	RXD8/SMISO8/SSCL8/MOSIA	
H9		PB6	MTIOC3D	RXD9/SMISO9/SSCL9	
H10		PB7	MTIOC3B	TXD9/SMOSI9/SSDA9	
J1		P24	MTIOC4A/MTCLKA/TMRI1		
J2		P21	MTIOC1B/TMCI0	SCL1	
J3		P17	MTIOC3A/MTIOC3B/TMO1/POE8#	SCK1/MISOA/SDA0-DS	IRQ7
J4		P13	MTIOC0B/TMO3	SDA0	IRQ3
J5		PH0			CACREF
J6		PH3	TMCI0		
J7		P50		SSLB1	
J8		PC4	MTIOC3D/MTCLKC/TMCI1/POE0#	SCK5/CTS8#/RTS8#/SS8#/SSLA0	
J9		PC0	MTIOC3C	CTS5#/RTS5#/SS5#/SSLA1	
J10		PC1	MTIOC3A	SCK5/SSLA2	
K1		P23	MTIOC3D/MTCLKD		
K2		P22	MTIOC3B/MTCLKC/TMO0		
K3		P20	MTIOC1A/TMRI0	SDA1	
K4		P14	MTIOC3A/MTCLKA/TMRI2	CTS1#/RTS1#/SS1#	IRQ4
K5		PH2	TMRI0		IRQ1
K6		PH1	TMO0		IRQ0
K7		P51		SSLB2	
K8		PC5	MTIOC3B/MTCLKD/TMRI2	SCK8/RSPCKA	
K9		PC3	MTIOC4D	TXD5/SMOSI5/SSDA5/IRTXD5	
K10		PC2	MTIOC4B	RXD5/SMISO5/SSCL5/SSLA3/IRRXD5	

Note: • Pin names to which –DS is appended are for pins that can be used to trigger release from deep software standby mode.

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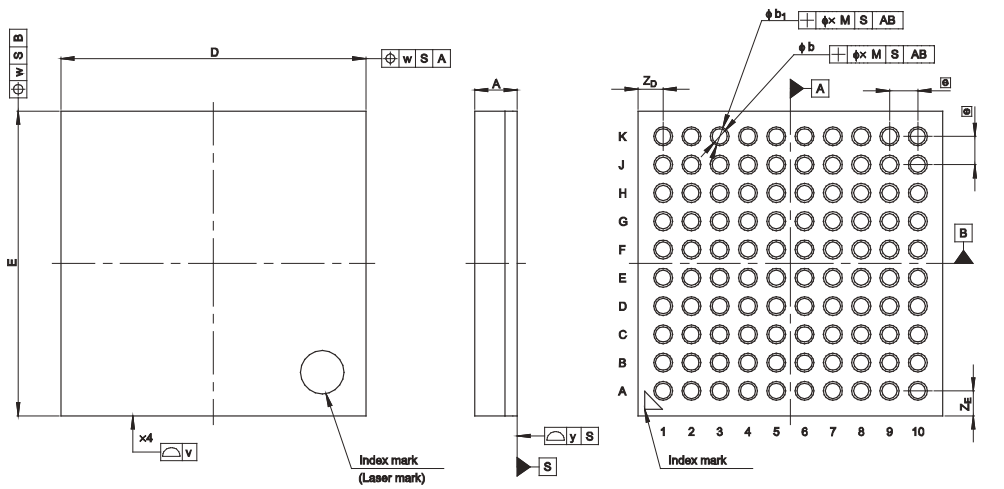
Add ’ Figure D 100-Pin TFLGA (PTLG0100JA-A)’ to Appendix 2.

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-TFLGA100-7x7-0.65	PTLG0100JA-A	100F0G	0.1g



Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	—	7.0	—
E	—	7.0	—
v	—	—	0.15
w	—	—	0.20
A	—	—	1.05
e	—	0.65	—
b	0.31	0.35	0.39
b_1	0.385	0.435	0.485
x	—	—	0.08
y	—	—	0.10
Z_D	—	0.575	—
Z_E	—	0.575	—

Figure D 100-Pin TFLGA (PTLG0100JA-A)