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# 1 Purpose of Document

This document summarizes the changes between the previous SAP5 silicon revision C and the current silicon revision D. These include requested UART design changes. The purpose of the redesign was to correct reported timing errors by the UART in the following modes: Master, Monitor, and Repeater. A problem with slave communication in special network constellations was also fixed.

# 2 Indication of the *End_Bit* Transmission Error

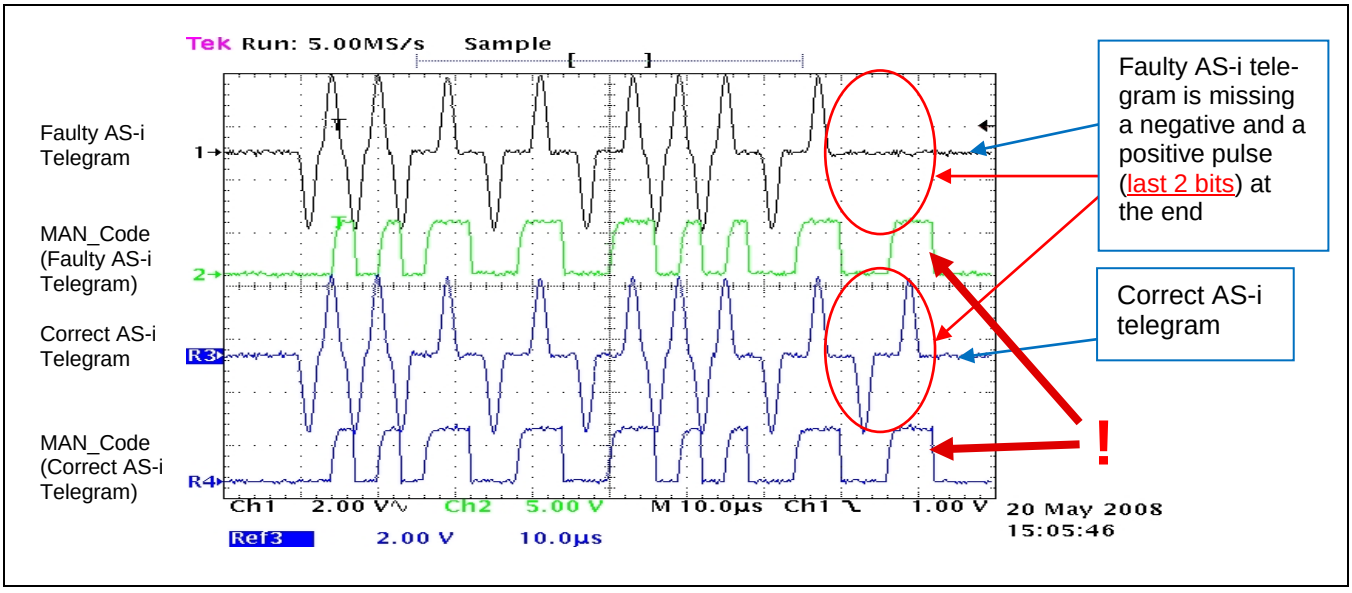
## 2.1. Problem Description

If the SAP5 revision C operates in Master Mode or in Repeater Mode, the error signaling for an *End_Bit_Error* does not work correctly. In some special cases, the generated MAN-Code of a signal with an *End_Bit _Error* looks similar to the MAN-Code of a signal without any errors as demonstrated in Figure 2.1.

This malfunction of the SAP5 revision C results in an MAN coded output signal that does not allow distinction between correct AS-I pulse sequences and pulse sequences that are shortened (missing one negative and one positive pulse). It occurs only under the following conditions:

- The parity of the signal is even.
- The last bit of the corrupt telegram is equal to binary 1.
- The *Stop_Bit* and the *Parity_Bit* or the *Start_Bit* and the *Control_Bit* are missing.
- If the *Start_Bit* and the *Control_Bit* are missing, the first pulse must have a negative polarity.

***Figure 2.1 Comparison of Valid MAN-Code Signal to Faulty MAN-Code Signal***



### 2.2. Design Corrections in the UART

The following changes in the UART block were implemented in SAP5 silicon revision D:

1. A new principle for ASI-telegram pause detection was implemented. The previous method caused erroneous pause detection in some cases; e.g., a telegram starting with a wrong Start bit (SB=1) and second bit = 0.
2. A new *Endbit_error* detection principle was implemented to comply with the *AS-I Complete Specification V3.0*. The new principle ensures than an *Endbit_error* is detected only if the polarity of the pulse at time (36µs/78µs ± tolerance) is negative.
3. The internal computation of *No_info_error*, *Timing_error,* and *Length_error* was reviewed and corrected to comply with the *AS-I Complete Specification V3.0*.

## 3 Master Pause Detection in Slave Mode

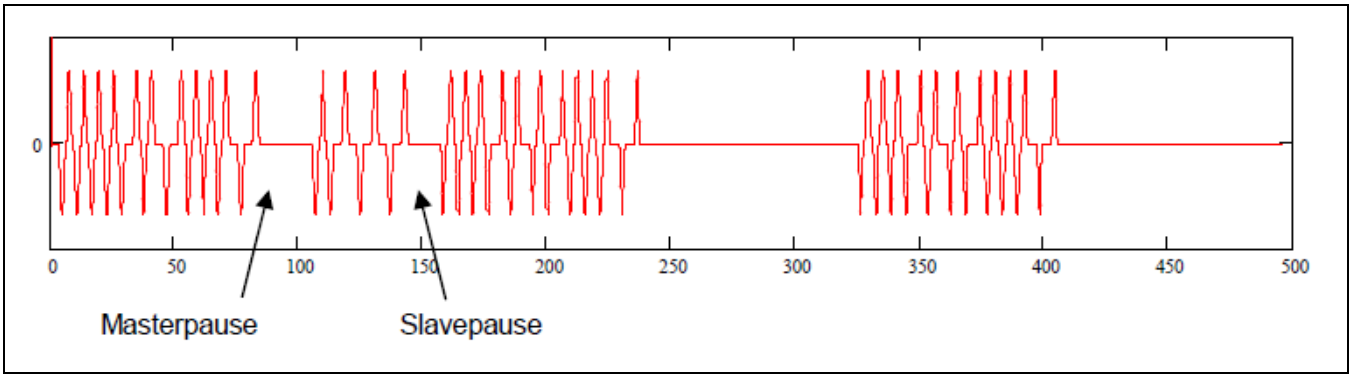
### 3.1. Problem Description

If the previous SAP5 revision C is operated in Slave Mode, the UART Master Pause detection does not always function correctly when the UART must listen to slave responses from a different slave. Depending on the actual AS-I line pulse timing, a slave response from a different slave is sometimes not recognized correctly, which results in a UART communication error. This prevents the Slave from understanding the next Master telegram correctly. If the Master telegram addresses the Slave itself, the error leads to a missing slave response and the Slave replies on a second repetition of the Master Call to its own address in asynchronous mode.

This behavior was mostly observed in mixed networks that used modules with the ASI4U, SAP5, and SAP4.1.

Figure 3.1 shows a telegram test case to reproduce the error. The AS-I signals shown in Figure 3.1 were generated by a signal generator that allowed sweeping the Master Pause and Slave Pause duration over the allowed specification limit. The first Master Call contains a different slave address than the tested slave. The second and third master calls address the tested slave. The tested slave replied with the erroneous behavior for certain Master pause and Slave pause scenarios only. The majority of the test cases were passed without error.

***Figure 3.1 Test for SAP5 Revision C Error in Master Pause Detection***



### 3.2. Design Correction

A new principle of AS-i telegram pause detection was implemented in SAP5 silicon revision D that is more precise and able to cover all valid timing scenarios for Master and Slave pauses. The new principle is now independent of the internal timing constraints of the UART state machine.

## 4 Analog Block

The Power Fail Detection Threshold in Master Mode has been changed:

Power Fail Detection Threshold = 19V - 2V

The typical switch point is at 17.6V.

## 5 Related Documents

| Document |
|---|
| *SAP5S/SAP51 Feature Sheet* |
| *SAP5S/SAP51 Data Sheet* |
| *SAP5S/SAP51 Errata Sheet* |
| *Compare SAP5 UART Revision C to Revision D ** |

Visit the SAP5/SAP51 product page www.IDT.com/SAP5 or contact your nearest sales office for the latest version of these documents.

* Note: Documents marked with an asterisk (*) are available only on request.

# 6 Document Revision History

| Revision | Date | Description |
|---|---|---|
| 1.10 | August 3, 2012 | Previous release. |
| 1.20 | January 22, 2015 | Full content revision including addition of illustrations.<br>Update for template.<br>Minor edits for clarity.<br>Addition of “Related Documents” section. |
| 1.21 | January 29, 2015 | Minor edit |
| | April 14, 2016 | Changed to IDT branding. |

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