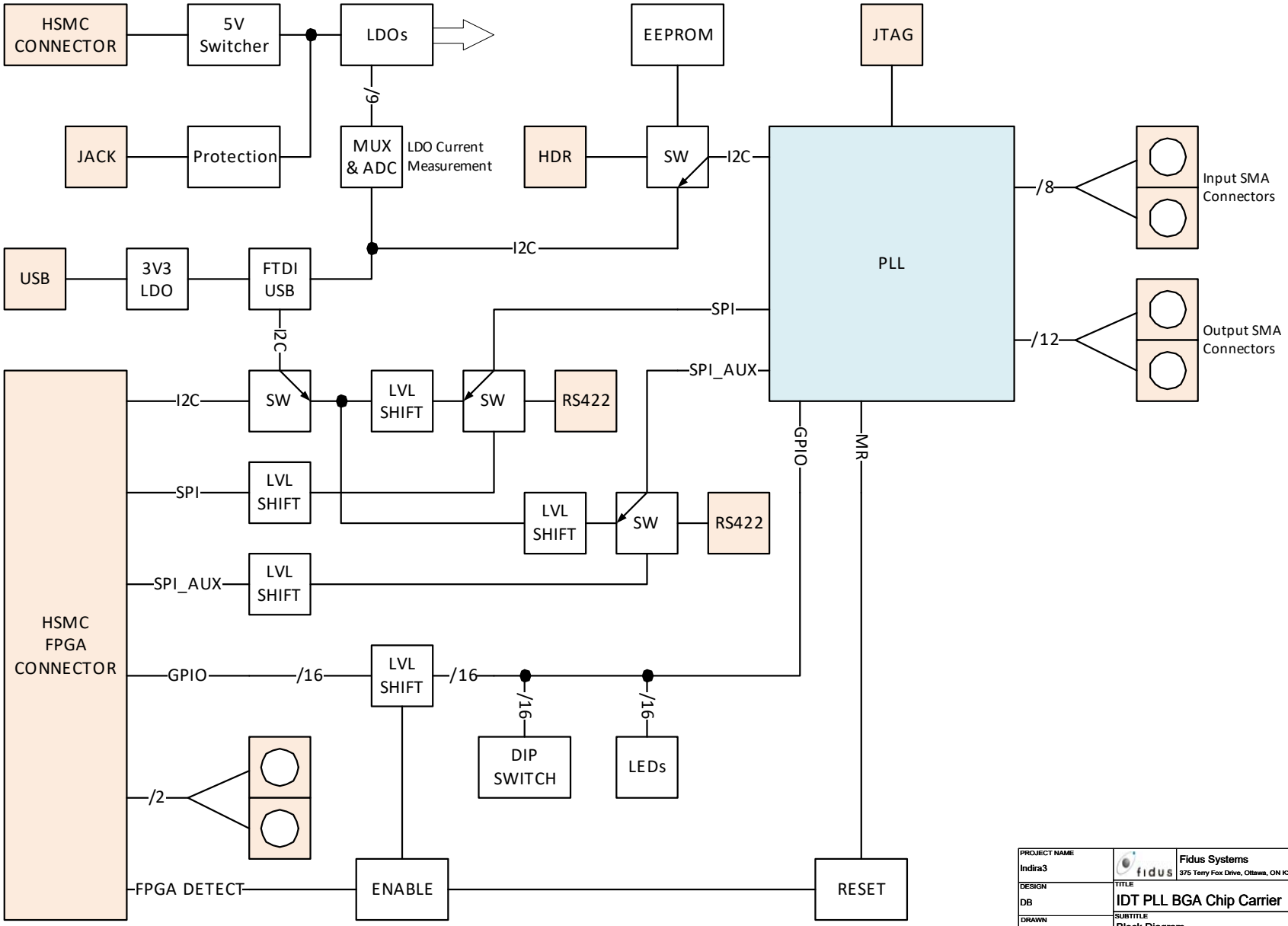
IDT PLL BGA CHIP CARRIER

TABLE OF CONTENTS

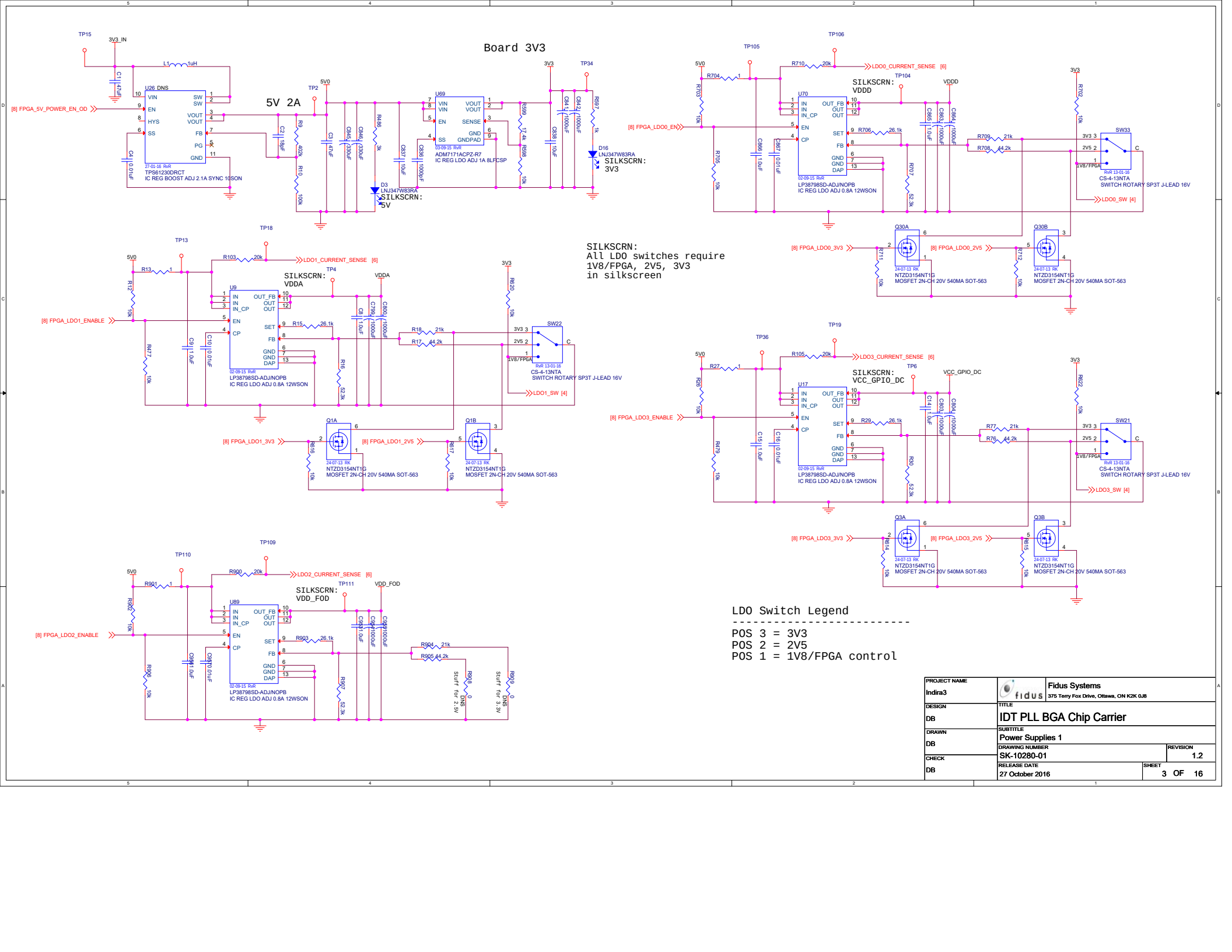
REVISION HISTORY

REVISION	DATE	CHANGE DETAILS
0.1	14 September 2016	First Release
0.2	16 September 2016	Updates to 5V0 input, EEPROM connections, and SPI selection pages.
0.3	19 September 2016	Added individual filters on VDDO lines. Removed J27 & J28. Added SMA on output of Y4.
0.4	19 September 2016	Added 0 Ohm resistors in series with inductors for U58 power supply filtering.
0.5	19 September 2016	Removed U79, U89, and FTDI_PLL_CS signal.
0.6	21 September 2016	C761 connected to GND.
0.7	22 September 2016	Added J83 and J84 for external I2C access.
0.8	11 October 2016	Removed J84. Updated block diagram.
0.9	11 October 2016	Updated title blocks. Update to block diagram. Corrected names of VDDO nets.
0.10	17 October 2016	Power supply changes. Changes to input and output clock terminations.
0.11	17 October 2016	Changed R910 to stuffed, 2.67k. Connected C795 to 3V3_IN.
1.0	27 October 2016	Release for build This version built November, 2016
1.1	7 March 2017	Changed SPI level shifters to TI TXB0104 parts Changed EEPROM to Microchip 24LC64 part
1.2	10 April 2017	BoM changes as per emails from Leon, 4 April 2017, and 10 April 2017.

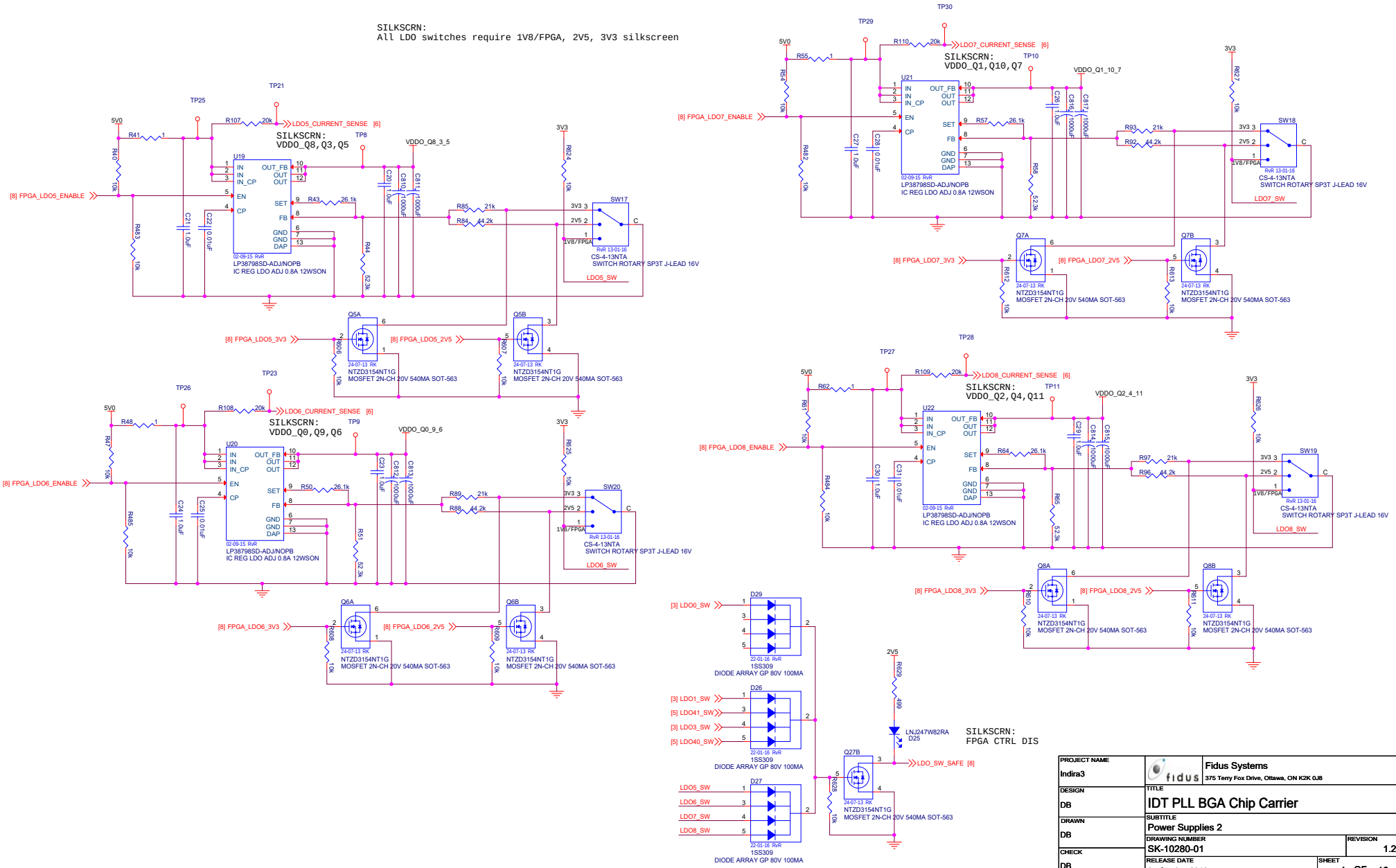
PROJECT NAME: Indira3	Fidus Systems 375 Terry Fox Drive, Ottawa, ON K2K 0J8	
DESIGN: DB	TITLE: IDT PLL BGA Chip Carrier	
DRAWN: DB	SUBTITLE: Table of Contents and Revision History	
CHECK: DB	DRAWING NUMBER: SK-10280-01	REVISION: 1.2
	RELEASE DATE: 27 October 2016	SHEET: 1 OF 16



PROJECT NAME	Indira3
DESIGN	DB
DRAWN	DB
CHECK	DB
	Fidus Systems 375 Terry Fox Drive, Ottawa, ON K2K 0J8
TITLE	IDT PLL BGA Chip Carrier
SUBTITLE	Block Diagram
DRAWING NUMBER	SK-10280-01
REVISION	1.2
RELEASE DATE	27 October 2016
SHEET	2 OF 16

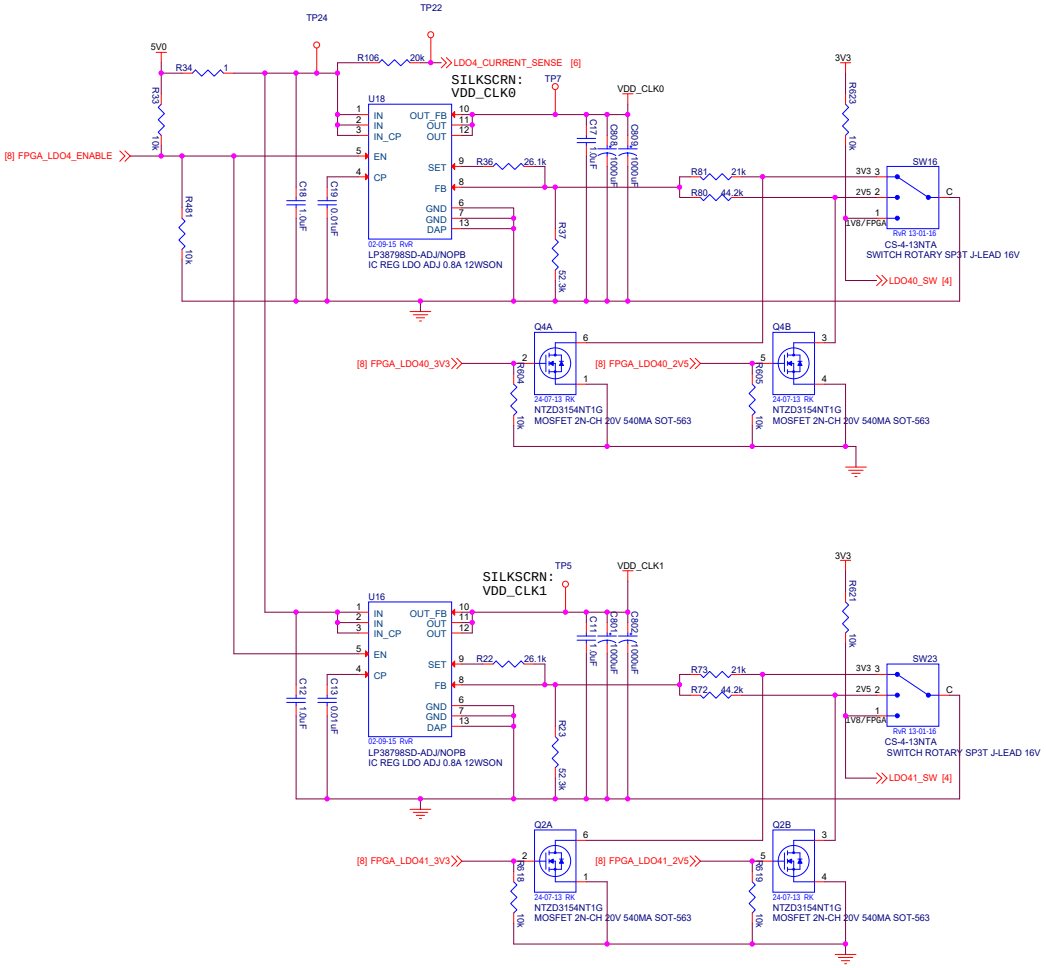

Board 3V3
5V 2A
SILKSCRN:
All LDO switches require
1V8/FPGA, 2V5, 3V3
in silkscreen
LDO Switch Legend
POS 3 = 3V3
POS 2 = 2V5
POS 1 = 1V8/FPGA control
SILKSCRN: 3V3
SILKSCRN: 5V
SILKSCRN: VDDA
SILKSCRN: VDDD
SILKSCRN: VCC_GPIO_DC
SILKSCRN: VDD_FOD
TPS61230DRCT
IC REG BOOST ADJ 2.1A SYNC 10SON
ADM7171ACPZ-R7
IC REG LDO ADJ 1A 8LFCSP
LP38798SD-ADJ/NOPB
IC REG LDO ADJ 0.8A 12WSON
NTZD3154NT1G
MOSFET 2N-CH 20V 540MA SOT-563
CS-4-13NTA
SWITCH ROTARY SP3T J-LEAD 16V
LNJ347W83RA
Stuff for 2.5V
Stuff for 3.3V
Fidus Systems
375 Terry Fox Drive, Ottawa, ON K2K 0J8
PROJECT NAME
Indira3
DESIGN
DB
DRAWN
DB
CHECK
DB
TITLE
IDT PLL BGA Chip Carrier
SUBTITLE
Power Supplies 1
DRAWING NUMBER
SK-10280-01
REVISION
1.2
RELEASE DATE
27 October 2016
SHEET
3 OF 16

SILKSCRN:
All LDO switches require 1V8/FPGA, 2V5, 3V3 silkscreen

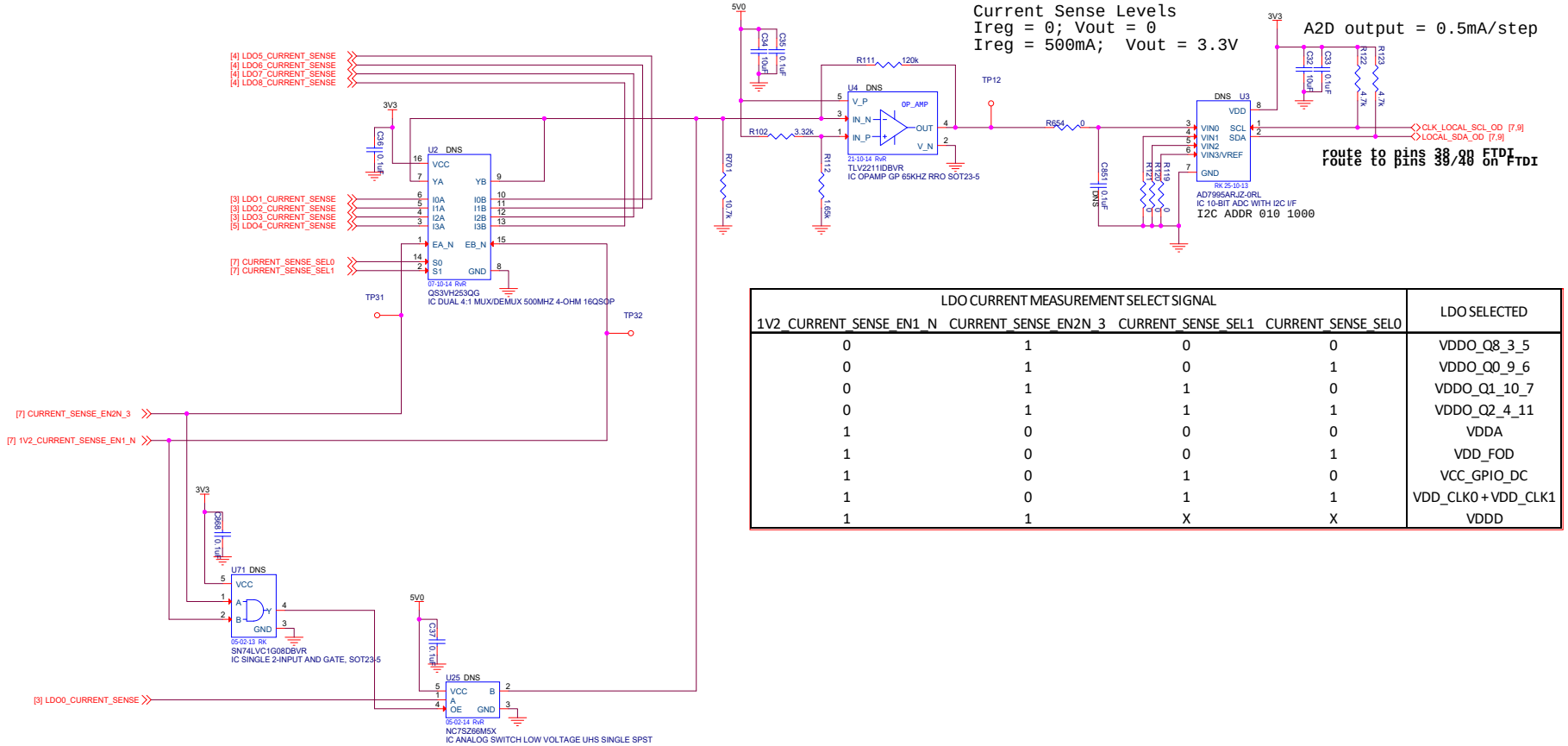


PROJECT NAME	Indira3
DESIGN	DB
DRAWN	DB
CHECK	DB
	Fidus Systems 375 Terry Fox Drive, Ottawa, ON K2K 0J8
TITLE	IDT PLL BGA Chip Carrier
SUBTITLE	Power Supplies 2
DRAWING NUMBER	SK-10280-01
REVISION	1.2
RELEASE DATE	27 October 2016
SHEET	4 OF 16

SILKSCRN:
All LDO switches require 1V8/FPGA, 2V5, 3V3 silkscreen

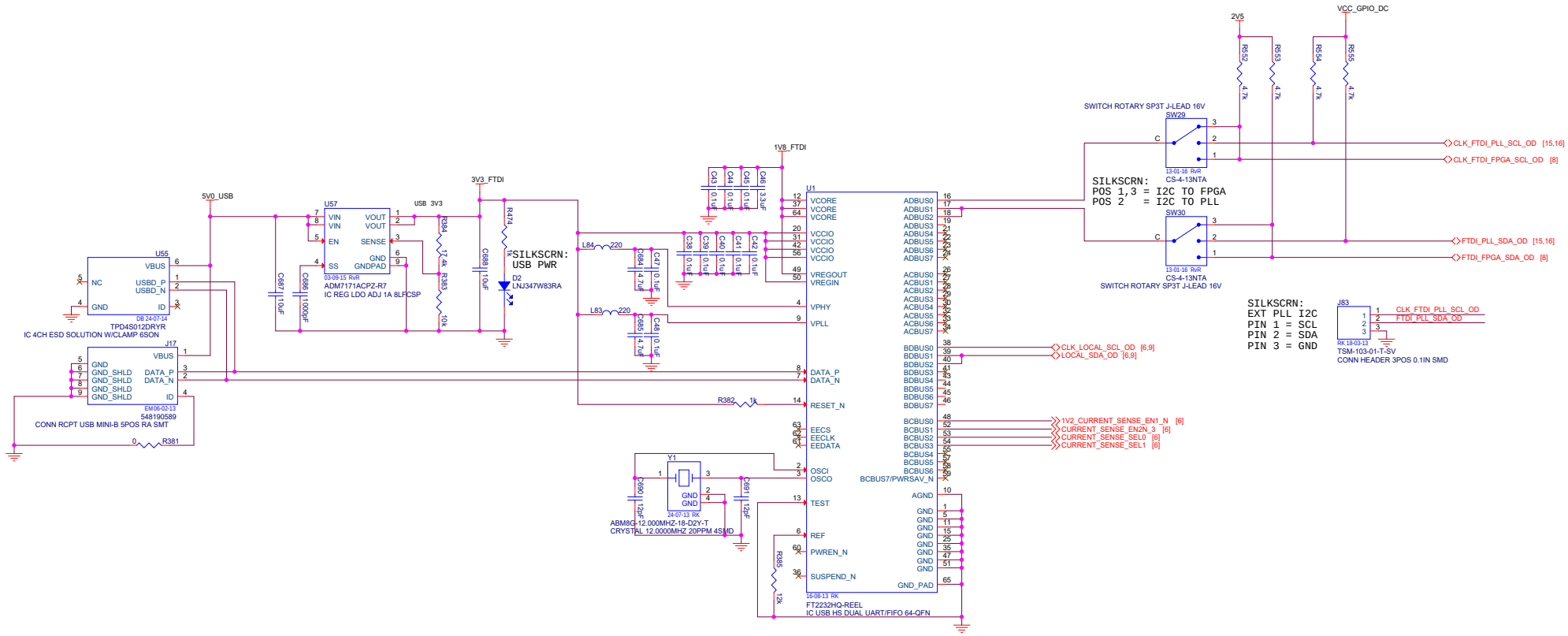


PROJECT NAME	Indira3
DESIGN	RK
DRAWN	RK
CHECK	DB
	Fidus Systems 375 Terry Fox Drive, Ottawa, ON K2K 0J8
TITLE	IDT PLL BGA Chip Carrier
SUBTITLE	Power Supplies 3
DRAWING NUMBER	SK-10280-01
REVISION	1.2
RELEASE DATE	27 October 2016
SHEET	5 OF 16

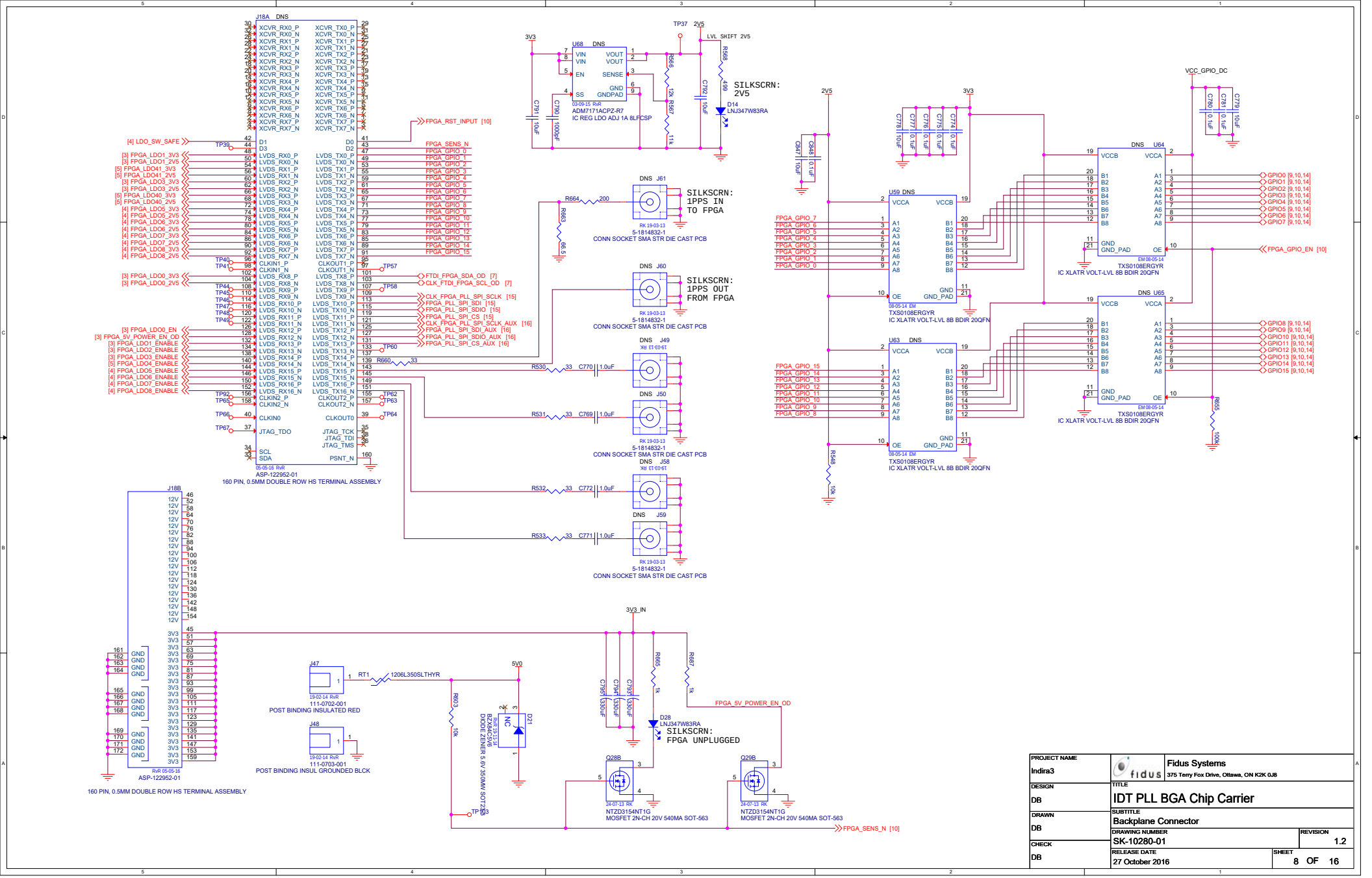


LDO CURRENT MEASUREMENT SELECT SIGNAL				LDO SELECTED
1V2_CURRENT_SENSE_EN1_N	CURRENT_SENSE_EN2N_3	CURRENT_SENSE_SEL1	CURRENT_SENSE_SEL0	
0	1	0	0	VDDO_Q8_3_5
0	1	0	1	VDDO_Q0_9_6
0	1	1	0	VDDO_Q1_10_7
0	1	1	1	VDDO_Q2_4_11
1	0	0	0	VDDA
1	0	0	1	VDD_FOD
1	0	1	0	VCC_GPIO_DC
1	0	1	1	VDD_CLK0 + VDD_CLK1
1	1	X	X	VDDD

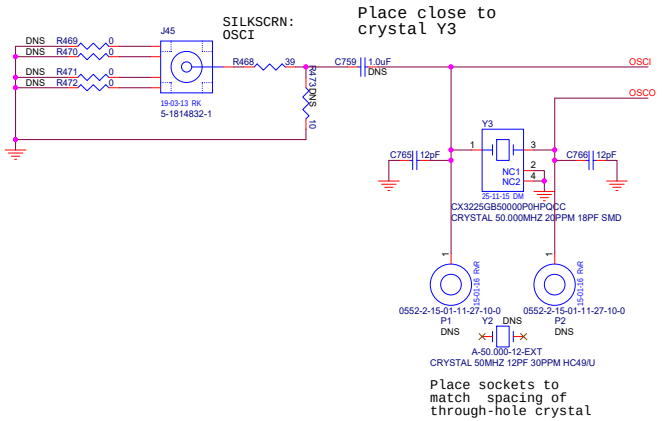
PROJECT NAME	Indira3
DESIGN	DB
DRAWN	DB
CHECK	DB
	Fidus Systems, 375 Terry Fox Drive, Ottawa, ON K2K 0J8
TITLE	IDT PLL BGA Chip Carrier
SUBTITLE	Current Measurement
DRAWING NUMBER	SK-10280-01
REVISION	1.2
RELEASE DATE	27 October 2016
SHEET	6 OF 16

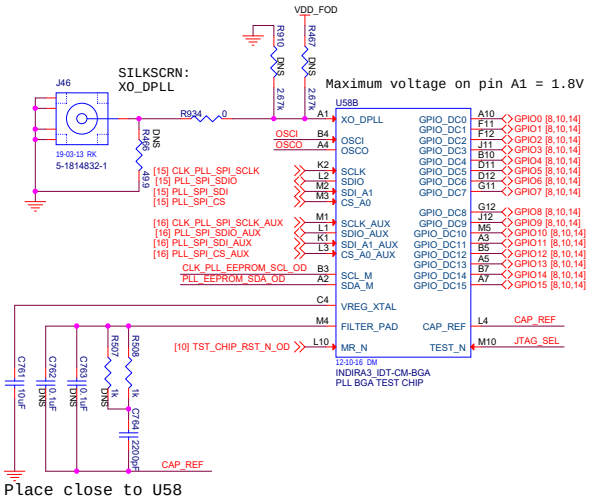


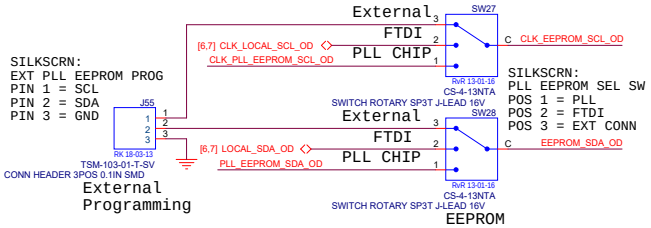
PROJECT NAME	Indira3
DESIGN	DB
DRAWN	DB
CHECK	DB
	Fidus Systems 375 Terry Fox Drive, Ottawa, ON K2K 0J8
TITLE	IDT PLL BGA Chip Carrier
SUBTITLE	FTDI USB Interface
DRAWING NUMBER	SK-10280-01
REVISION	1.2
RELEASE DATE	27 October 2016
SHEET	7 OF 16

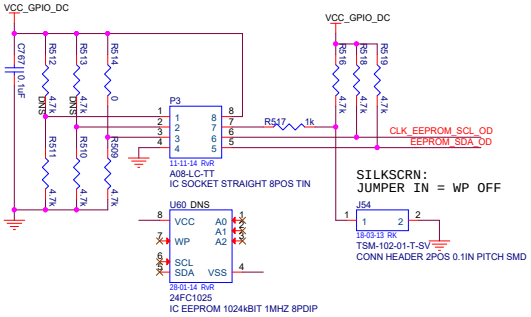

J18A DNS
ASP-122952-01
160 PIN, 0.5MM DOUBLE ROW HS TERMINAL ASSEMBLY
J18B
ASP-122952-01
160 PIN, 0.5MM DOUBLE ROW HS TERMINAL ASSEMBLY
U68 DNS
ADM7171ACPZ-R7
IC REG LDO ADJ 1A 8LFCSP
SILKSCRN:
2V5
D14
LNJ347W83RA
LVL SHIFT 2V5
TP37 2V5
J61 DNS
SILKSCRN:
1PPS IN
TO FPGA
J60 DNS
SILKSCRN:
1PPS OUT
FROM FPGA
5-1814832-1
CONN SOCKET SMA STR DIE CAST PCB
J49 DNS
J50 DNS
J58 DNS
J59 DNS
U59 DNS
U63 DNS
U64 DNS
U65 DNS
TXS0108ERGYR
IC XLATR VOLT-LVL 8B BDIR 20QFN
VCC_GPIO_DC
FPGA_GPIO_EN [10]
FPGA_RST_INPUT [10]
FPGA_SENS_N [10]
FPGA_5V_POWER_EN_OD
3V3_IN
5V0
J47
J48
111-0702-001
POST BINDING INSULATED RED
111-0703-001
POST BINDING INSUL GROUNDED BLCK
1206L350SLTHYR
D28
LNJ347W83RA
SILKSCRN:
FPGA UNPLUGGED
Q28B
Q29B
NTZD3154NT1G
MOSFET 2N-CH 20V 540MA SOT-563
PROJECT NAME
Indira3
DESIGN
DB
DRAWN
DB
CHECK
DB
Fidus Systems
375 Terry Fox Drive, Ottawa, ON K2K 0J8
TITLE
IDT PLL BGA Chip Carrier
SUBTITLE
Backplane Connector
DRAWING NUMBER
SK-10280-01
REVISION
1.2
RELEASE DATE
27 October 2016
SHEET
8 OF 16

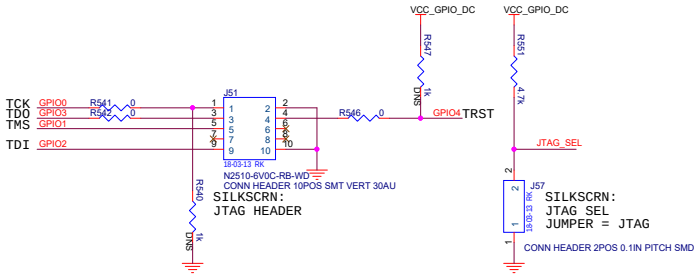
DNS



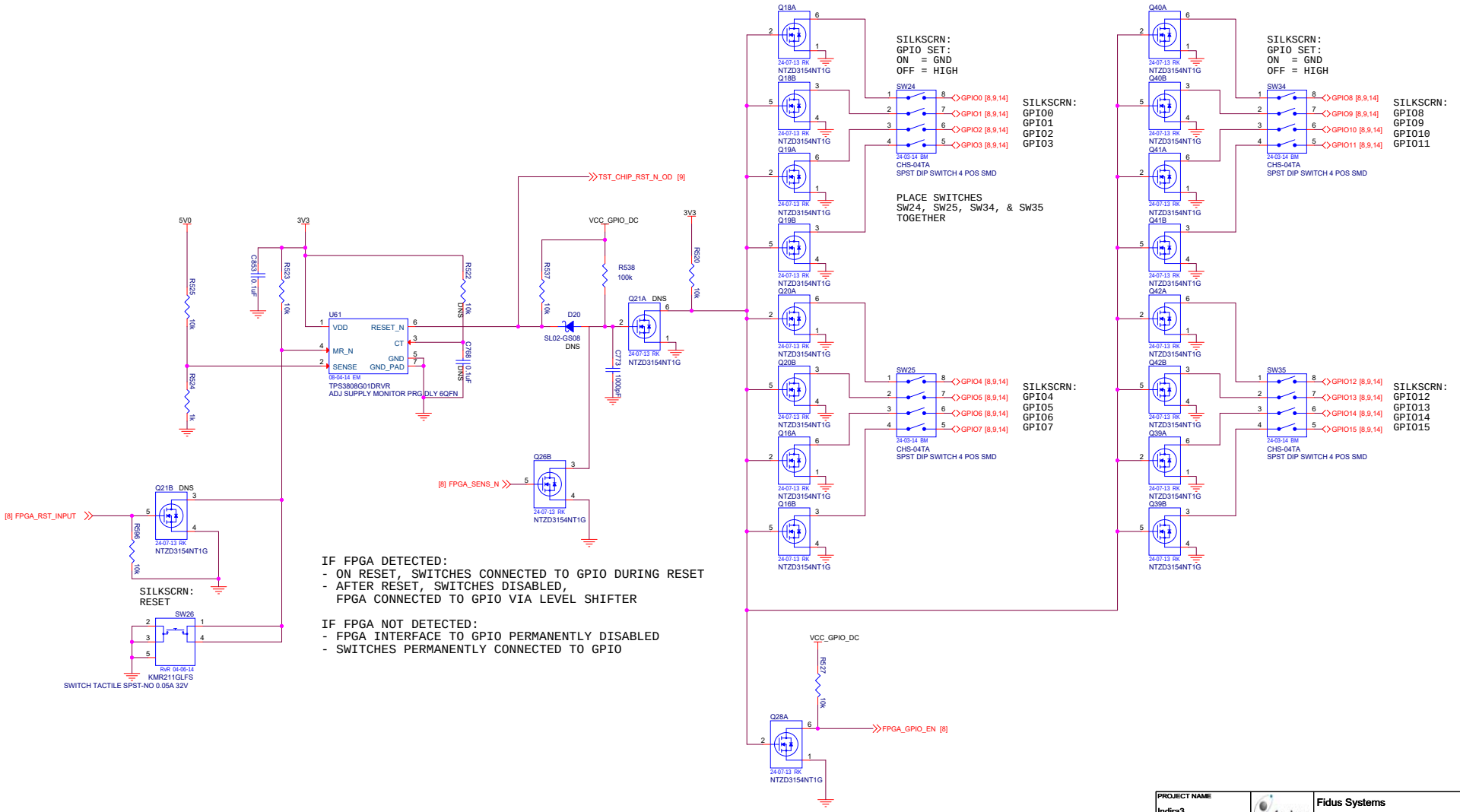






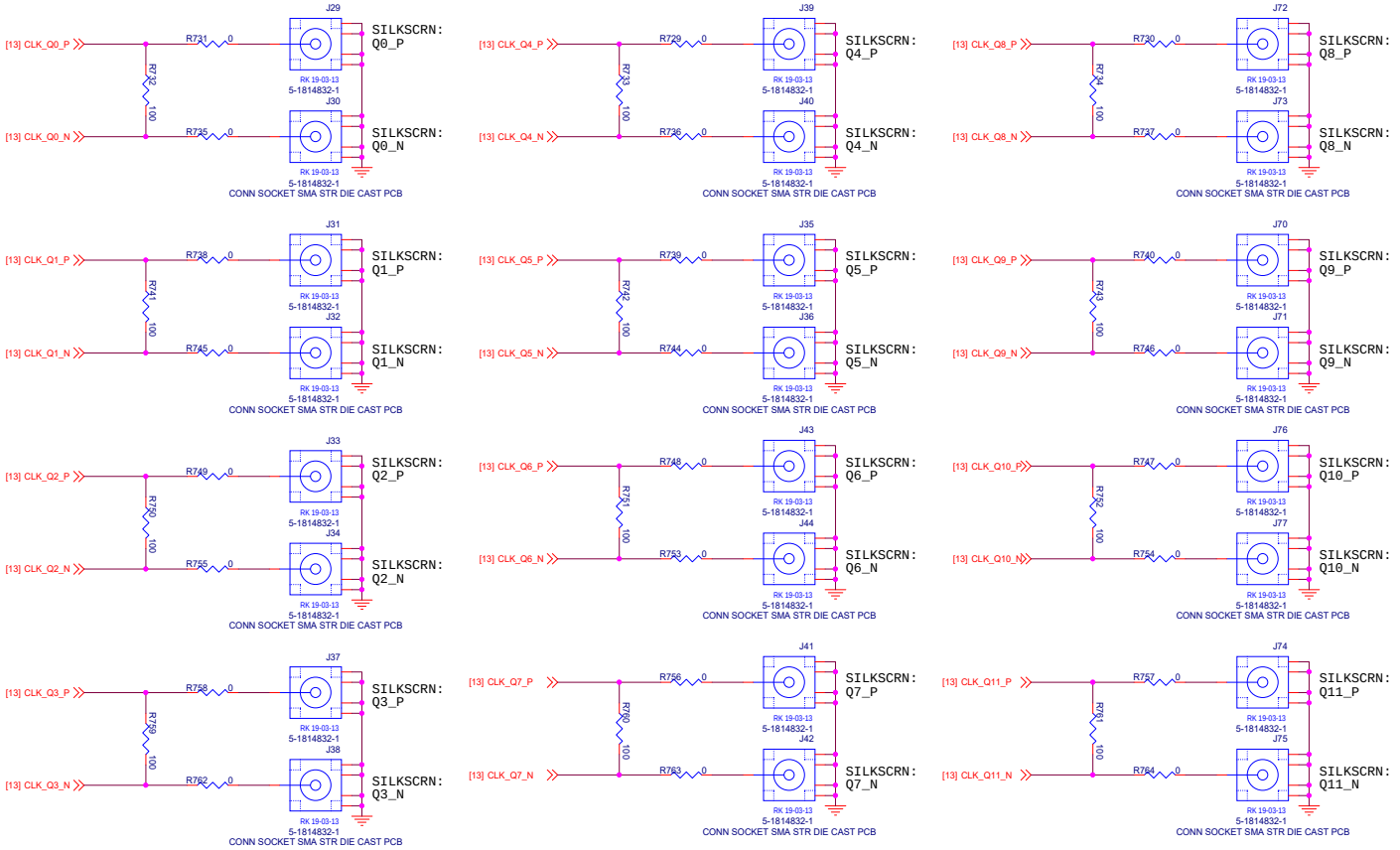


PROJECT NAME	Indira3
DESIGN	DB
DRAWN	DB
CHECK	DB
Fidus Systems	375 Terry Fox Drive, Ottawa, ON K2K 0J8
TITLE	IDT PLL BGA Chip Carrier
SUBTITLE	PLL Core
DRAWING NUMBER	SK-10280-01
REVISION	1.2
RELEASE DATE	27 October 2016
SHEET	9 OF 16

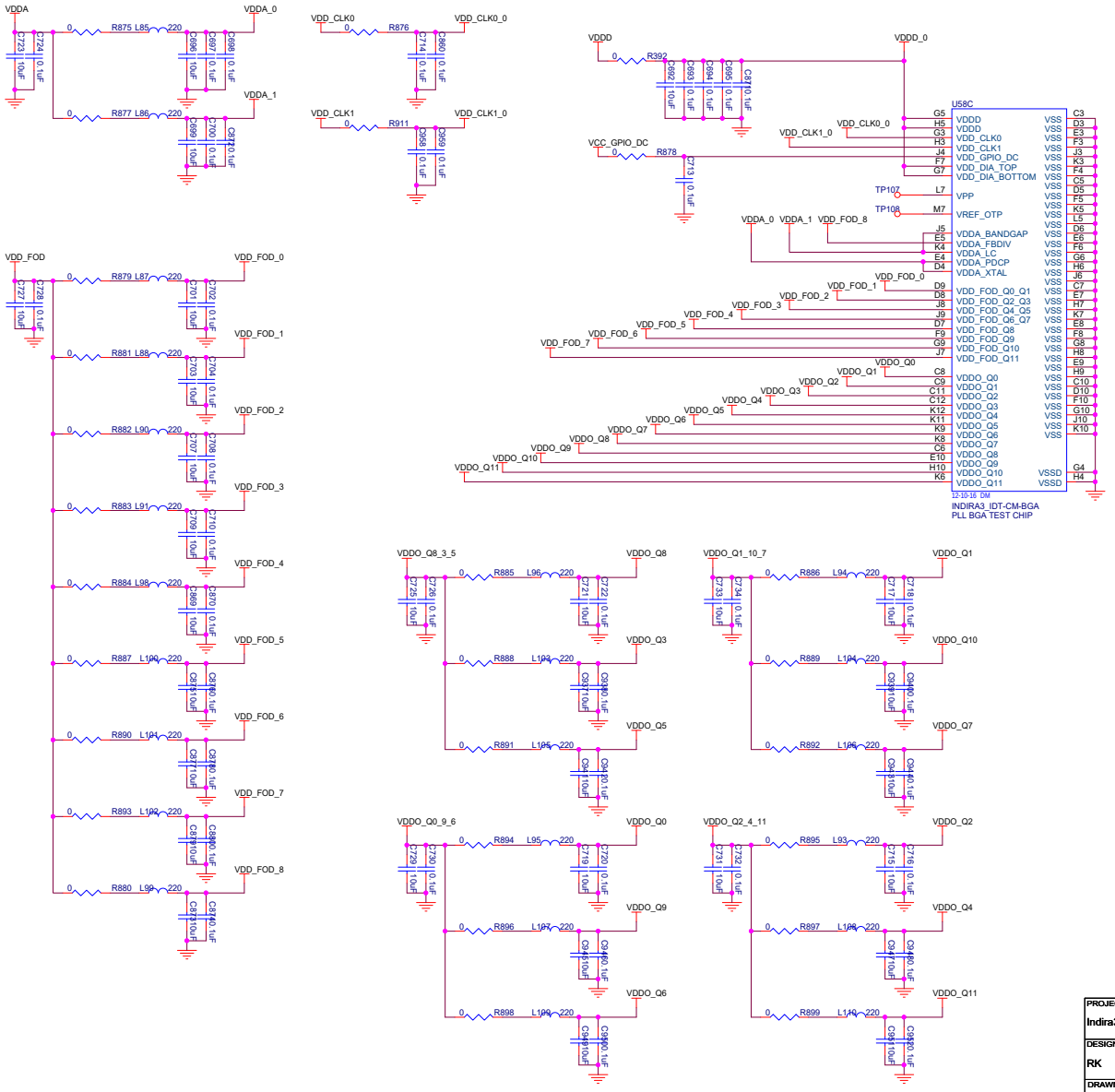


PROJECT NAME	Indira3
DESIGN	DB
DRAWN	DB
CHECK	DB
	Fidus Systems 375 Terry Fox Drive, Ottawa, ON K2K 0J8
TITLE	IDT PLL BGA Chip Carrier
SUBTITLE	GPIO DIP SW
DRAWING NUMBER	SK-10280-01
REVISION	1.2
RELEASE DATE	27 October 2016
SHEET	10 OF 16

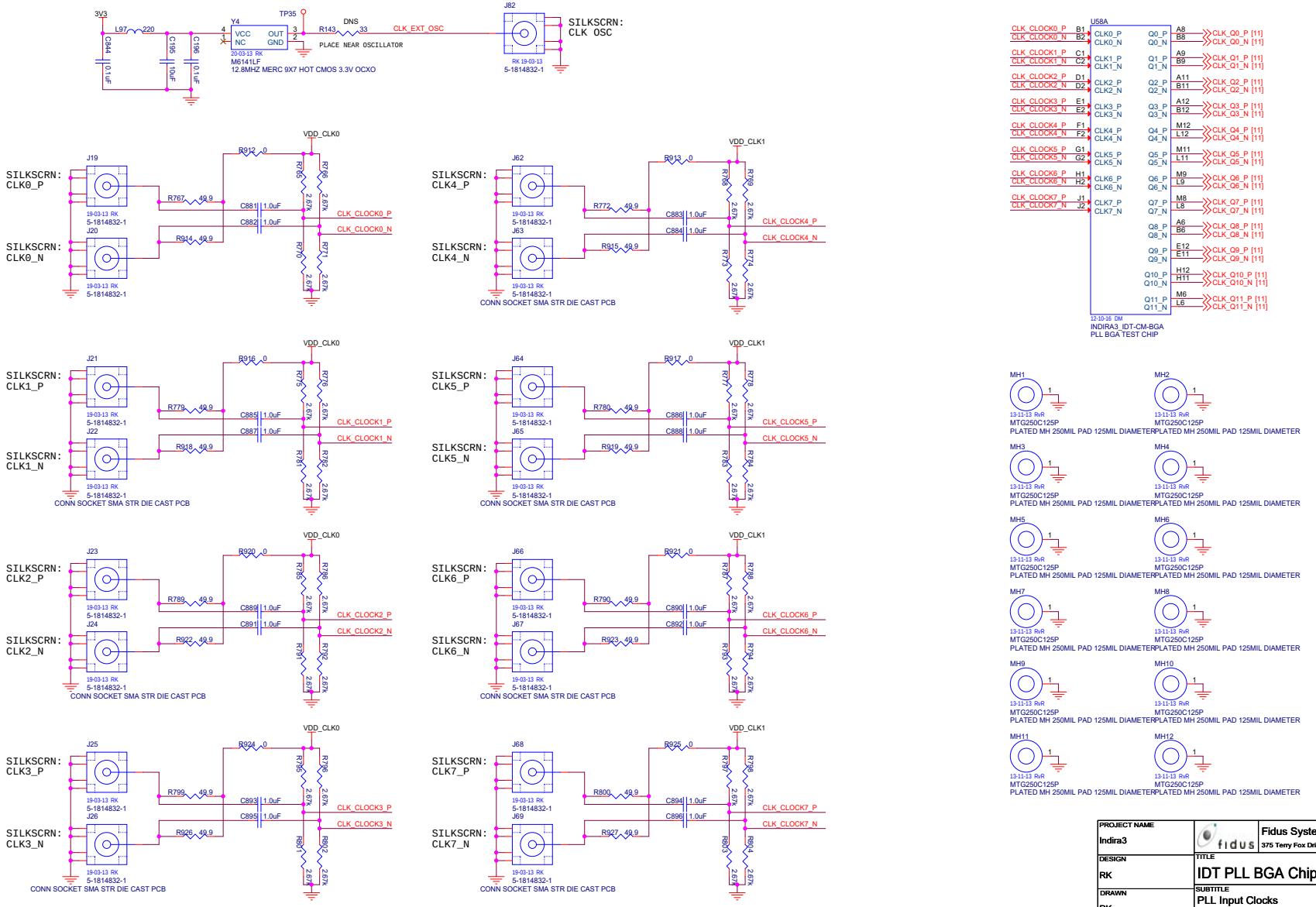
PLACE PARALLEL
TERMINATIONS
CLOSE TO U58



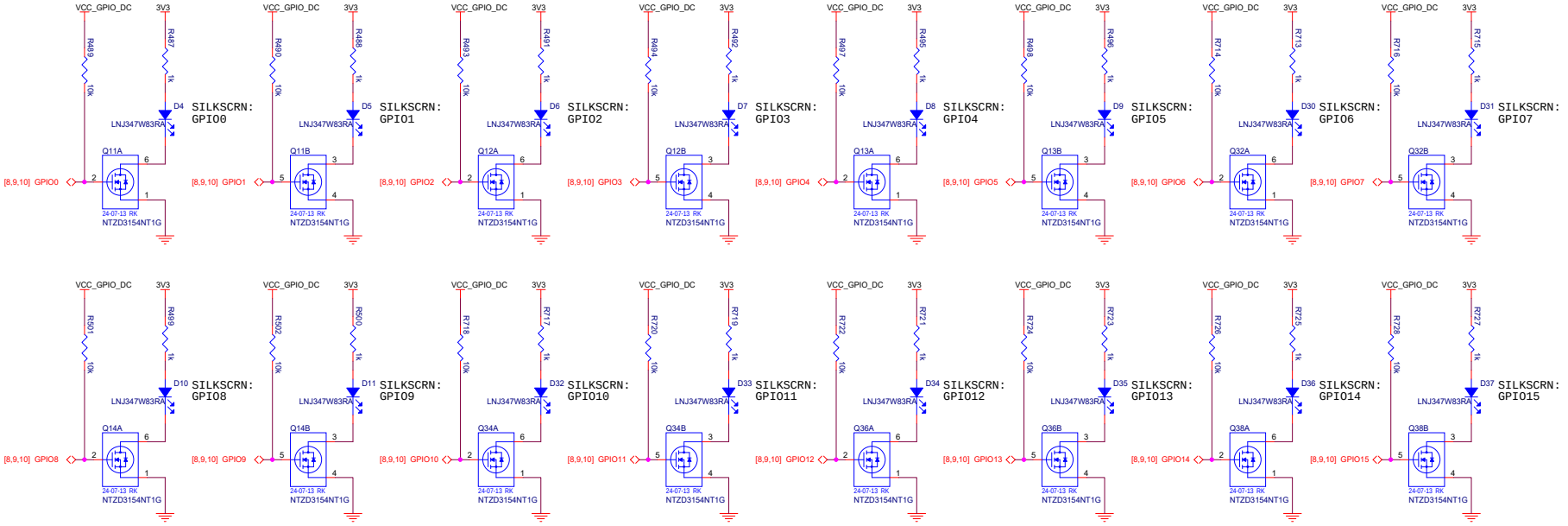
PROJECT NAME	Indira3
DESIGN	DB
DRAWN	DB
CHECK	DB
	Fidus Systems 375 Terry Fox Drive, Ottawa, ON K2K 0J8
TITLE	IDT PLL BGA Chip Carrier
SUBTITLE	PLL Output Clocks
DRAWING NUMBER	SK-10280-01
REVISION	1.2
RELEASE DATE	27 October 2016
SHEET	11 OF 16



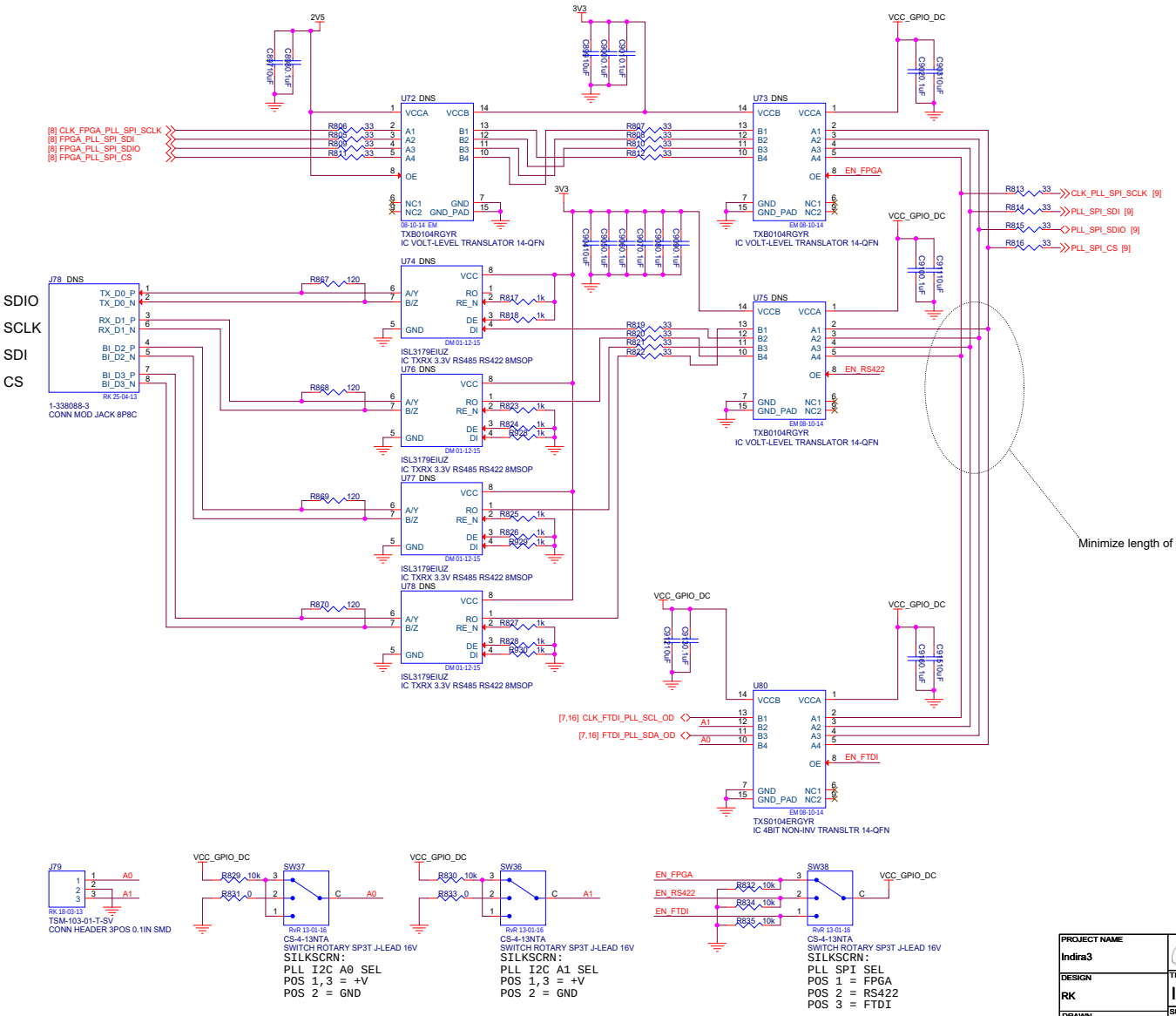
PROJECT NAME	Indira3
DESIGN	RK
DRAWN	RK
CHECK	DB
	Fidus Systems 375 Terry Fox Drive, Ottawa, ON K2K 0J8
TITLE	IDT PLL BGA Chip Carrier
SUBTITLE	PLL Power
DRAWING NUMBER	SK-10280-01
REVISION	1.2
RELEASE DATE	27 October 2016
SHEET	12 OF 16



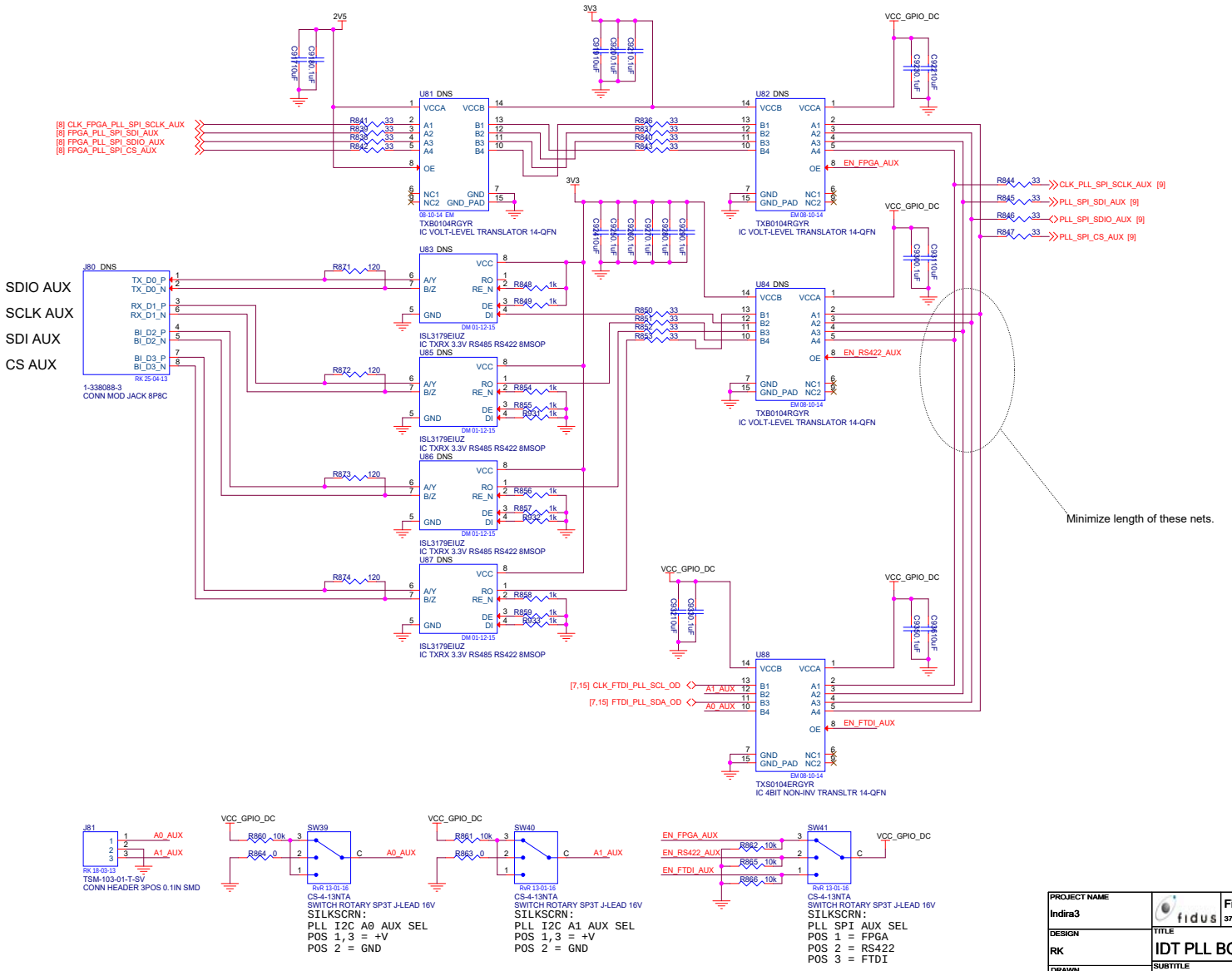
PROJECT NAME	Indira3
DESIGN	RK
DRAWN	RK
CHECK	DB
	Fidus Systems 375 Terry Fox Drive, Ottawa, ON K2K 0J8
TITLE	IDT PLL BGA Chip Carrier
SUBTITLE	PLL Input Clocks
DRAWING NUMBER	SK-10280-01
REVISION	1.2
RELEASE DATE	27 October 2016
SHEET	13 OF 16



PROJECT NAME	Indira3
DESIGN	RK
DRAWN	RK
CHECK	DB
	Fidus Systems 375 Terry Fox Drive, Ottawa, ON K2K 0J8
TITLE	IDT PLL BGA Chip Carrier
SUBTITLE	GPIO LEDs
DRAWING NUMBER	SK-10280-01
REVISION	1.2
RELEASE DATE	27 October 2016
SHEET	14 OF 16



PROJECT NAME	Indira3
DESIGN	RK
DRAWN	RK
CHECK	DB
	Fidus Systems 375 Terry Fox Drive, Ottawa, ON K2K 0J8
TITLE	IDT PLL BGA Chip Carrier
SUBTITLE	PLL SPI Select
DRAWING NUMBER	SK-10280-01
REVISION	1.2
RELEASE DATE	27 October 2016
SHEET	15 OF 16



PROJECT NAME	Indira3
DESIGN	RK
DRAWN	RK
CHECK	DB
	Fidus Systems 375 Terry Fox Drive, Ottawa, ON K2K 0J8
TITLE	IDT PLL BGA Chip Carrier
SUBTITLE	PLL AUX SPI Select
DRAWING NUMBER	SK-10280-01
REVISION	1.2
RELEASE DATE	27 October 2016
SHEET	16 OF 16