

Smart Configurator for RL78 Plug-in in e² studio 2023-04

Smart Configurator for RL78 V1.6.0

Release Note

Introduction

Thank you for using the Smart Configurator for RL78.

This document describes the restrictions and points for caution. Read this document before using the product.

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1. Introduction

Smart Configurator is a utility for combining software to meet your needs. It supports the following three functions related to the embedding of Renesas drivers in your systems: importing middleware, generating driver code, and setting pins.

Smart Configurator for RL78 V1.6.0 is equivalent to Smart Configurator for RL78 Plug-in in e² studio 2023-04.

1.1 System requirements

The operating environment is as follows.

1.1.1 Windows PC

- System: x64/x86 based processor
 - Windows® 11
 - Windows® 10 (64-bit version)
 - Windows® 8.1 (64-bit version)
- Memory capacity: We recommend 4 GB or more.
- Capacity of hard disk: At least 300 MB of free space.
- Display: Graphics resolution should be at least 1024 x 768, and the mode should display at least 65,536 colors.
- Processor: 1 GHz or higher (must support hyper-threading, multi-core CPUs)

1.1.2 Linux PC

Smart Configurator for RL78 plug-in in e² studio 2023-01 or later is supported on Linux OS.

- System: x64 based processor, 2 GHz or faster (with multicore CPUs)
 - Ubuntu 22.04 LTS Desktop (64-bit version)
 - Ubuntu 20.04 LTS Desktop (64-bit version)
- Memory capacity: We recommend 2 GB or more.
- Capacity of hard disk: At least 2 GB of free space.

1.1.3 Development Environments

- Renesas Electronics Compiler for RL78 [CC-RL] V1.12 or later
- LLVM for Renesas RL78 10.0.0.202209 or later
- IAR Embedded Workbench for Renesas RL78 V5.10.1 or later
- SMS Assembler ^{Note1} V1.00.00 or later
- FAA Assembler ^{Note2} V1.04.02 or later

Note:

1. If you want to add SMS Assembler to e² studio, install it from the integrated installer of e² studio 21-04 or later. ([e² studio](#))

As with other compilers, select and install from the [Additional Software] - [Renesas Toolchains & Utilities] tab of the e² studio setup wizard.

2. If you want to add FAA Assembler to e² studio, install it from the integrated installer of e² studio 23-04 or later. ([e² studio](#))

As with other compilers, select and install from the [Additional Software] - [Renesas Toolchains & Utilities] tab of the e² studio setup wizard.

2. Support List

2.1 Support Devices List

Below is a list of devices supported by the Smart Configurator for RL78 V1.6.0.

Table 2-1 Support Devices (1/2)

Group (HW Manual number)	PIN	Device name
RL78/G23 Group (R01UH0896EJ0120)	30pin	R7F100GAFxSP, R7F100GAGxSP, R7F100GAHxSP, R7F100GAJxSP
	32pin	R7F100GBFxBP, R7F100GBGxBP, R7F100GBHxBP, R7F100GBJxBP, R7F100GBFxFP, R7F100GBGxFP, R7F100GBHxFP, R7F100GBJxFP
	36pin	R7F100GCFxLA, R7F100GCGxLA, R7F100GCHxLA, R7F100GCJxLA
	40pin	R7F100GEFxBP, R7F100GEGxBP, R7F100GEHxBP, R7F100GEJxBP
	44pin	R7F100GFFxFP, R7F100GFGxFP, R7F100GFHxFP, R7F100GFJxFP, R7F100GFKxFP, R7F100GFLxFP, R7F100GFNxFP
	48pin	R7F100GGFxFB, R7F100GGGxFB, R7F100GGHxFB, R7F100GGJxFB, R7F100GGKxFB, R7F100GGLxFB, R7F100GGNxFB, R7F100GGFxBP, R7F100GGGxBP, R7F100GGHxBP, R7F100GGJxBP, R7F100GGKxBP, R7F100GGLxBP, R7F100GGNxBP
	52pin	R7F100GJFxFA, R7F100GJGxFA, R7F100GJHxFA, R7F100GJJxFA, R7F100GJKxFA, R7F100GJLxFA, R7F100GJNxFA
	64pin	R7F100GLFxFA, R7F100GLGxFA, R7F100GLHxFA, R7F100GLJxFA, R7F100GLKxFA, R7F100GLLxFA, R7F100GLNxFA, R7F100GLFxFB, R7F100GLGxFB, R7F100GLHxFB, R7F100GLJxFB, R7F100GLKxFB, R7F100GLLxFB, R7F100GLNxFB, R7F100GLFxFA, R7F100GLGxFA, R7F100GLHxFA, R7F100GLJxFA, R7F100GLKxFA, R7F100GLLxFA, R7F100GLNxFA
	80pin	R7F100GMGxFA, R7F100GMHxFA, R7F100GMJxFA, R7F100GMKxFA, R7F100GMLxFA, R7F100GMNxFA, R7F100GMGxFB, R7F100GMHxFB, R7F100GMJxFB, R7F100GMKxFB, R7F100GMLxFB, R7F100GMNxFB
	100pin	R7F100GPGxFB, R7F100GPHxFB, R7F100GPJxFB, R7F100GPKxFB, R7F100GPLxFB, R7F100GPNxFB, R7F100GPGxFA, R7F100GPHxFA, R7F100GPJxFA, R7F100GPKxFA, R7F100GPLxFA, R7F100GPNxFA
	128pin	R7F100GSJxFB, R7F100GSKxFB, R7F100GSLxFB, R7F100GSNxFB
RL78/F24 Group (R01UH0944EJ0100)	32pin	R7F124FBJ3xNP, R7F124FBJ4xNP, R7F124FBJ5xNP
	48pin	R7F124FGJ3xFB, R7F124FGJ4xFB, R7F124FGJ5xFB
	64pin	R7F124FLJ3xFB, R7F124FLJ4xFB, R7F124FLJ5xFB
	80pin	R7F124FMJ3xFB, R7F124FMJ4xFB, R7F124FMJ5xFB
	100pin	R7F124FPJ3xFB, R7F124FPJ4xFB, R7F124FPJ5xFB
RL78/G15 Group (R01UH0959EJ0100)	8pin	R5F12008xNS, R5F12007xNS
	10pin	R5F12018xSP, R5F12017xSP
	16pin	R5F12048xNA, R5F12047xNA, R5F12048xSP, R5F12047xSP
	20pin	R5F12068xSP, R5F12067xSP
RL78/F23 Group (R01UH0944EJ0100)	32pin	R7F123FBG3xNP, R7F123FBG4xNP, R7F123FBG5xNP
	48pin	R7F123FGG3xFB, R7F123FGG4xFB, R7F123FGG5xFB
	64pin	R7F123FLG3xFB, R7F123FLG4xFB, R7F123FLG5xFB
	80pin	R7F123FMG3xFB, R7F123FMG4xFB, R7F123FMG5xFB
RL78/G22 Group (R01UH0978EJ0100)	16pin	R7F102G4ExNP, R7F102G4CxNP
	20pin	R7F102G6ExSP, R7F102G6CxSP
	24pin	R7F102G7ExNP, R7F102G7CxNP
	25pin	R7F102G8ExLA, R7F102G8CxLA
	30pin	R7F102GAExSP, R7F102GACxSP
	32pin	R7F102GBExNP, R7F102GBCxNP, R7F102GBExFP, R7F102GBCxFP
	36pin	R7F102GCExLA, R7F102GCCxLA
	40pin	R7F102GEExNP, R7F102GECxNP
	44pin	R7F102GFExFP, R7F102GFCxFP
	48pin	R7F102GGExFB, R7F102GGExNP, R7F102GGCxFB, R7F102GGCxCNP

Table 2-2 Support Devices (2/2)

Group (HW Manual number)	PIN	Device name
RL78/G24 Group (R01UH0961EJ0080)	20pin	R7F101G6GxSP, R7F101G6ExSP
	24pin	R7F101G7GxNP, R7F101G7ExNP
	25pin	R7F101G8GxLA, R7F101G8ExLA
	30pin	R7F101GAGxSP, R7F101GAExSP
	32pin	R7F101GBGxNP, R7F101GBExNP, R7F101GBGxFP, R7F101GBExFP
	40pin	R7F101GEGxNP, R7F101GEEExNP
	44pin	R7F101GFGxFP, R7F101GFExFP
	48pin	R7F101GGGxFB, R7F101GGEExFB, R7F101GGGxNP, R7F101GGEExNP
	52pin	R7F101GJGxFA, R7F101GJExFA
	64pin	R7F101GLGxFA, R7F101GLGxFB, R7F101GLEExFA, R7F101GLEExFB
RL78/G16 Group (R01UH0980EJ0090)	10pin	R5F1211AxSP, R5F1211CxSP
	16pin	R5F1214AxNA, R5F1214AxSP, R5F1214CxNA, R5F1214CxSP
	20pin	R5F1216AxSP, R5F1216CxSP
	24pin	R5F1217AxNA, R5F1217CxNA
	32pin	R5F121BAxFP, R5F121BAxNA, R5F121BCxFP, R5F121BCxNA

2.2 Support Components List

Below is a list of Components supported by the Smart Configurator for RL78 V1.6.0.

Table 2-3 Support Components (1/2)

✓ : Support, - : Non-support

No	Components	Mode	RL78/G23	RL78/F24	RL78/G15	RL78/F23	RL78/G22	RL78/G16	RL78/G24	Remarks
1	12 Bit A/D Single Scan	-	-	✓	-	✓	-	-	-	
2	12 Bit A/D Continuous Scan	-	-	✓	-	✓	-	-	-	
3	12 Bit A/D Group Scan	-	-	✓	-	✓	-	-	-	
4	A/D Converter	Normal mode	✓	-	✓	-	✓	✓	✓	Only RL78/G24 A/D converter has mode selection GUI. For other devices, the default mode is "Normal mode" and no GUI is provided for mode selection.
5	Clock Output/Buzzer Output Controller	-	✓	✓	✓	✓	✓	✓	✓	
6	Comparator	-	✓	✓	✓	-	-	✓	✓	
7	D/A Converter	-	✓	✓	-	-	-	-	✓	
8	Data Transfer Controller	-	✓	✓	-	✓	✓	-	✓	
9	Delay Counter	-	✓	✓	✓	✓	✓	✓	✓	
10	Divider Function	-	✓	✓	✓	✓	✓	✓	✓	
11	Event Link Controller	-	-	✓	-	-	✓	-	✓	
12	External Event Counter	-	✓	✓	✓	✓	✓	✓	✓	
13	IIC Communication (Master mode)	-	✓	✓	✓	✓	✓	✓	✓	
14	IIC Communication (Slave mode)	-	✓	✓	✓	✓	✓	✓	✓	
15	Input Capture Function	-	-	✓	-	✓	-	-	✓	
16	Input Pulse Interval/Period Measurement	-	✓	✓	✓	✓	✓	✓	✓	
17	Input Signal High-/Low-Level Width Measurement	-	✓	✓	✓	✓	✓	✓	✓	
18	Interrupt Controller	-	✓	✓	✓	✓	✓	✓	✓	
19	Interval Timer	8 bit count mode	✓	✓	✓	✓	✓	✓	✓	
		12 bit count mode	-	-	✓	-	-	✓	-	
		16 bit count mode	✓	✓	✓	✓	✓	✓	✓	
		16 bit capture mode	✓	-	-	-	✓	-	✓	
		32 bit count mode	✓	-	-	-	✓	-	✓	
20	Key Interrupt	-	✓	✓	-	✓	✓	-	✓	
21	One-Shot Pulse Output	One-Shot Pulse Output	✓	✓	✓	✓	✓	✓	✓	
		Two-Channel Input with One-Shot Pulse Output	-	-	✓	-	-	✓	-	
22	Output Compare Function	-	-	✓	-	✓	-	-	✓	
23	Ports	-	✓	✓	✓	✓	✓	✓	✓	

Table 2-4 Support Components (2/2)

✓ : Support, -: Non-support

No	Components	Mode	RL78/G23	RL78/F24	RL78/G15	RL78/F23	RL78/G22	RL78/G16	RL78/G24	Remarks
24	PWM Option Unit A	-	-	✓	-	✓	-	-	✓	
25	PWM Output	PWM mode	✓	✓	✓	✓	✓	✓	✓	
		PWM3 mode	-	✓	-	✓	-	-	✓	
		Extended PWM mode	-	✓	-	✓	-	-	✓	
		PWM2 mode	-	-	-	-	-	-	✓	
26	Real-Time Clock	-	✓	✓	-	✓	✓	✓	✓	
27	Remote Control Signal Receiver	-	✓	-	-	-	-	-	-	
28	SNOOZE Mode Sequencer	-	✓	-	-	-	✓	-	-	
29	SPI (CSI) Communication	Transmission	✓	✓	✓	✓	✓	✓	✓	
		Reception	✓	✓	✓	✓	✓	✓	✓	
		Transmission/reception	✓	✓	✓	✓	✓	✓	✓	
30	Square Wave Output	-	✓	✓	✓	✓	✓	✓	✓	
31	Three-phase PWM Output	Reset Synchronous PWM Mode	-	✓	-	✓	-	✓	✓	
		Complementary PWM Mode	-	✓	-	✓	-	✓	✓	
		Extended Complementary PWM Mode	-	✓	-	✓	-	✓	✓	
32	UART Communication	Transmission	✓	✓	✓	✓	✓	✓	✓	
		Reception	✓	✓	✓	✓	✓	✓	✓	
		Transmission/reception	✓	✓	✓	✓	✓	✓	✓	
33	Voltage Detector	-	✓	✓	-	✓	✓	-	✓	
34	Watchdog Timer	-	✓	✓	✓	✓	✓	✓	✓	
35	Logic & Event Link Controller	-	✓	-	-	-	-	-	-	Need download in Smart Configurator RL78
36	Phase Counting Mode	-	-	-	-	-	-	-	✓	
37	Programmable Gain Amplifier	-	-	-	-	-	-	-	✓	
38	Flexible Application Accelerator	-	-	-	-	-	-	-	✓	

2.3 New support

2.3.1 Support RL78/G16 and RL78/G24 devices

See **Table 2-1 Support Devices (1/2)** Support Devices List for details on supported packages.

2.3.2 BSP (Board Support Package) revision update

BSP rev1.60 is supported and will be added as default BSP when creating Smart Configurator project.

2.3.3 Flexible Application Accelerator (FAA) configurator support

New software component type FAA configurator was supported for Flexible Application Accelerator from Smart Configurator for RL78 V1.6.0.

Through FAA configurator, user can check and download FAA functionalities data from web, e.g., Motor control (FOC), Calculation etc. After downloading FAA functionalities data, user can select the FAA functionalities and do configuration with GUI. During the configuration, user can check H/W resource confliction between CPU and FAA. After finishing configuration and click 'Code Generate' button, user can generate FAA assembler code with CPU files, the FAA used data & code size information also will be reported in Console view with code generation.

FAA configurator support the Builder/Debugger option^{Note} reflection at selecting Renesas CC-RL or LLVM project case. Standalone Smart Configurator supports IAR EW for integrating with DSP assembler.

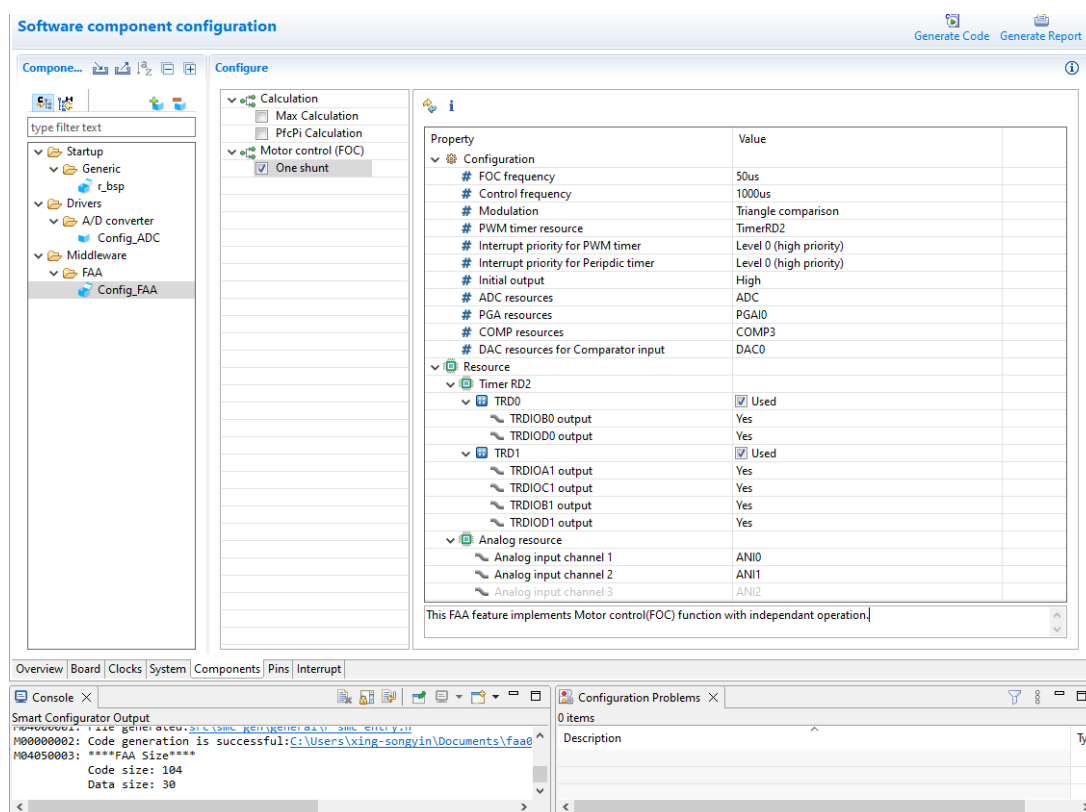


Figure 2-1 FAA Configurator

Note:

To run FAA configuration generated code with CCRL project under e² studio 2023-04, user need manually add "FAACODE=FAACODER" and "FAADATA=FAADATAR" to the linker option of '-rom' as below through project context menu: C/C++ Build → Settings → Linker → Output → ROM to RAM mapped section (-rom).

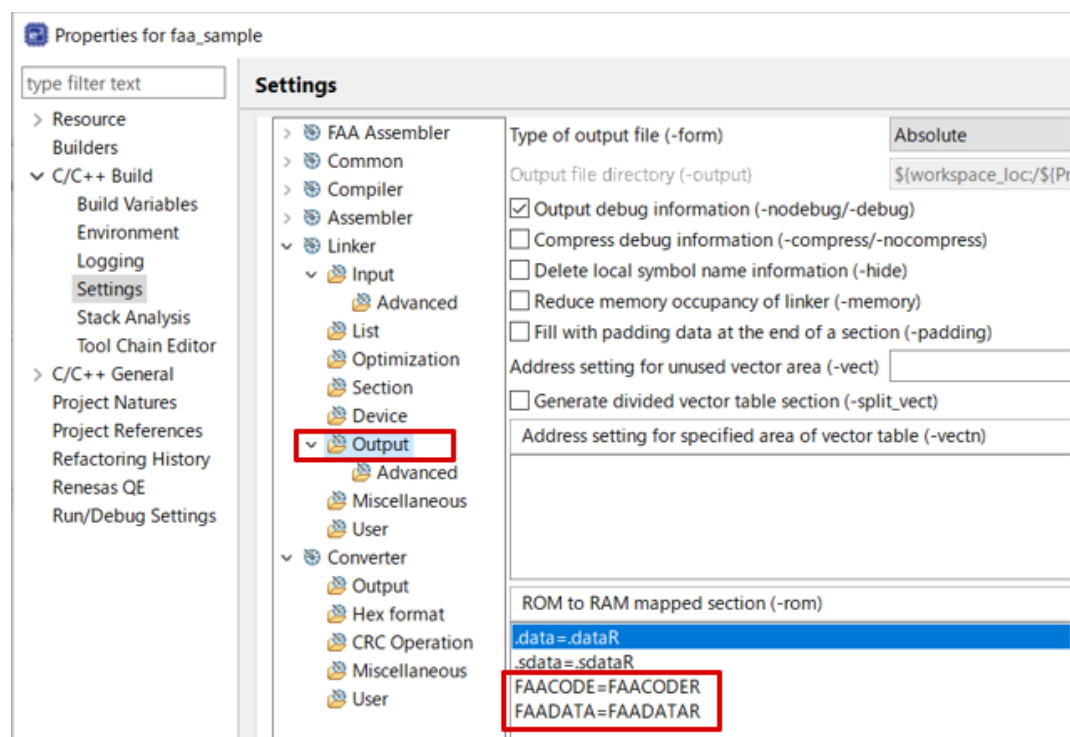


Figure 2-2 Linker option of -rom

2.3.4 The BDF file and debugger information can be imported in e² studio project

When creating a project in e² studio, select a target board, then the debug configuration changes according to this BDF file automatically. After creating this project, the [Board] page in Smart Configurator selects the board which is same as this BDF file and the [System] page in Smart configurator selects the on-chip debug operation setting which is same as this BDF file too.

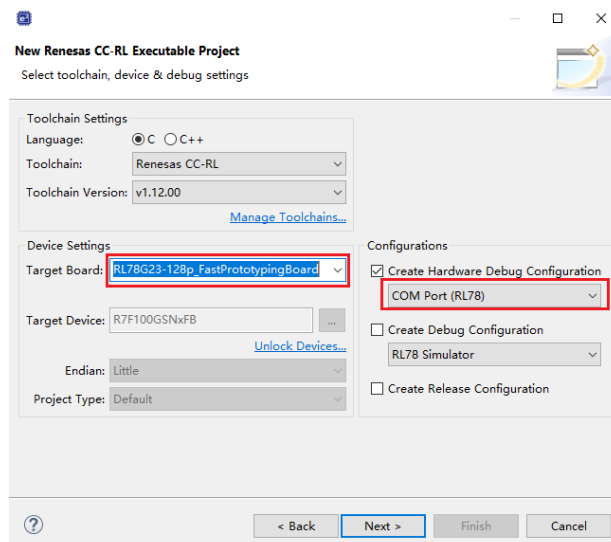


Figure 2-3 When creating a project in e² studio, select a target board

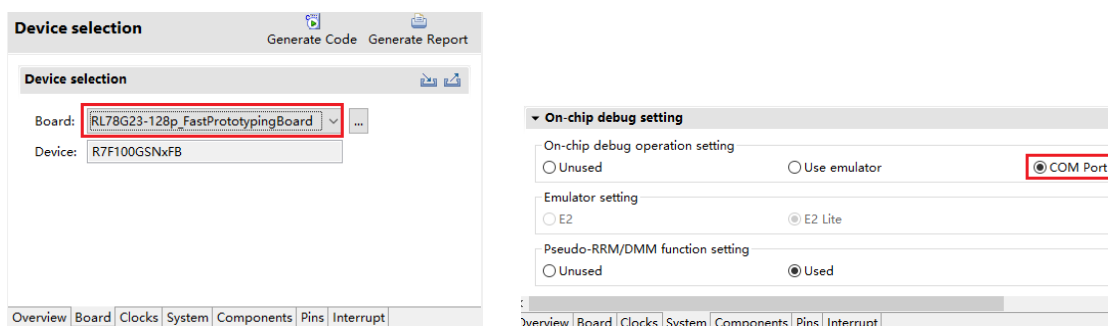


Figure 2-4 [Board] page and [System] page after creating the project

Note: When creating a new project and changing the debug configuration, the [System] page can select the on-chip debug operation setting according to the debug configuration.

3. Changes

This chapter describes changes to the Smart Configurator for RL78 V1.6.0.

3.1 Correction of issues/limitations

Table 3-1 List of Correction of issues/limitations

✓ : Applicable, -: Not Applicable

No	Description	RL78/G23	RL78/F24	RL78/G15	RL78/F23	RL78/G22	RL78/G16	RL78/G24	Remarks
1	Fixed the issue of XT1 oscillator can be selected when the low-speed on-chip oscillator is running	-	✓	-	✓	-	-	-	
2	Fixed the issue of the redundant contents in "Show view" dialog in Standalone Smart Configurator	✓	✓	✓	✓	✓	✓	✓	

3.1.1 Fixed the issue of XT1 oscillator can be selected when the low-speed on-chip oscillator is running

When the low-speed on-chip oscillator is selected as source clock of fSL, XT1 oscillator can be selected. If user select XT1 oscillator at this time, it wouldn't output a message. This issue has been fixed from Smart Configurator for RL78 V1.6.0.

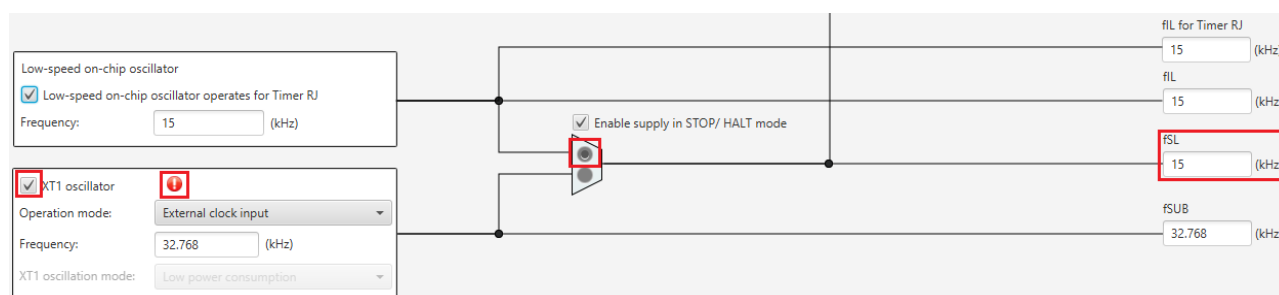


Figure 3-1 XT1 oscillator can't be used when the low-speed on-chip oscillator is running

3.1.2 Fixed the issue of the redundant contents in "Show view" dialog in Standalone Smart Configurator

When configuring the "Show View" dialog in Standalone Smart Configurator, there are some redundant contents shown inside the menu.

This issue has been fixed from Smart Configurator for RL78 V1.6.0.

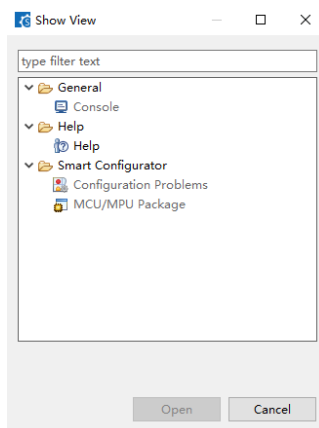


Figure 3-2 The "Show view" dialog in Standalone Smart Configurator

3.2 Specification changes

Table 3-2 List of Specification changes

✓: Applicable, -: Not Applicable

No	Description	RL78/G23	RL78/F24	RL78/G15	RL78/F23	RL78/G22	RL78/G16	RL78/G24	Remarks
1	Improvement for removing multiple components at the same time	✓	✓	✓	✓	✓	✓	✓	
2	Improvement for moving the ADCLK setting from [Clocks] setting to 12 Bit A/D Single Scan, 12 Bit A/D Continuous Scan and 12 Bit A/D Group Scan	-	✓	-	✓	-	-	-	
3	Improvement for supporting user code protection feature for standalone Smart Configurator	✓	✓	✓	✓	✓	✓	✓	
4	Improvement for supporting the low-speed on-chip oscillator for Timer RJ individually	-	✓	-	✓	-	-	-	

3.2.1 Improvement for removing multiple components at the same time

From Smart Configurator for RL78 V1.6.0, the user can select some components together by using Ctrl+<select multiple components> and click the "Remove" button to remove the selected components at the same time.

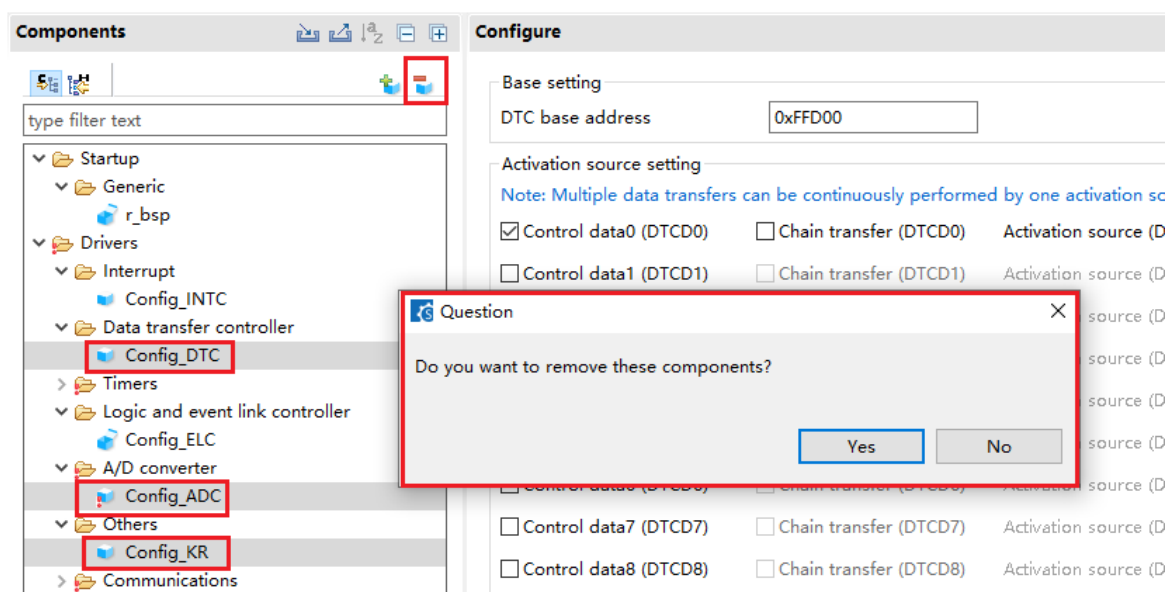


Figure 3-3 Removing multiple components at the same time

3.2.2 Improvement for moving the ADCLK setting from [Clocks] setting to 12 Bit A/D Single Scan, 12 Bit A/D Continuous Scan and 12 Bit A/D Group Scan

When ADCEN is set to 0 in user code, ADCKS register is reset, which causes the actual ADCLK value is inconsistent with [Clocks] setting. From Smart Configurator for RL78 V1.6.0, the ADCLK setting is moved from [Clocks] setting to 12 Bit A/D Single Scan, 12 Bit A/D Continuous Scan and 12 Bit A/D Group Scan, so that ADCKS register can be re-initialized by calling “R_<Config_S12AD0>_Create()” function in *Config_S12AD0.c*.

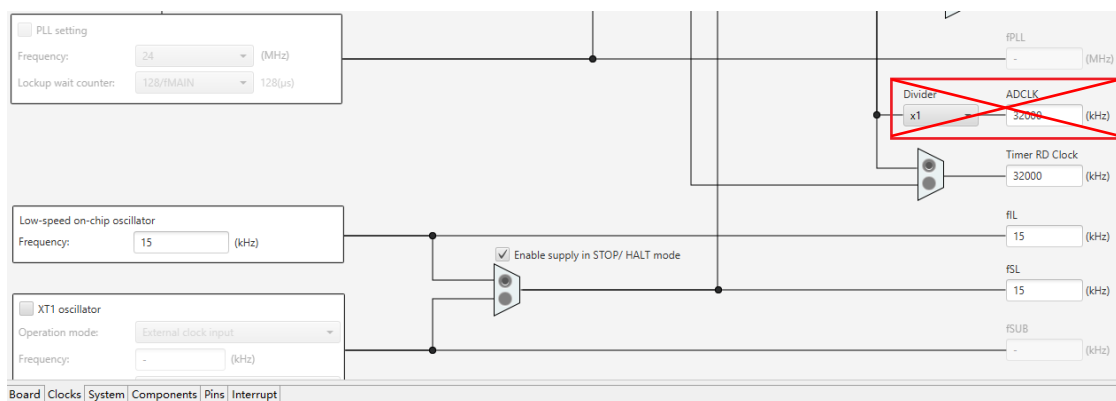


Figure 3-4 Delete the ADCLK setting in [Clocks] setting

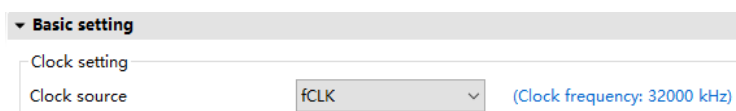


Figure 3-5 Add the ADCLK setting in 12-bit A/D converter component

3.2.3 Improvement for supporting user code protection feature for standalone Smart Configurator

From Smart Configurator for RL78 V1.6.0, Standalone Smart Configurator can support user code protection function.

3.2.4 Improvement for supporting the low-speed on-chip oscillator for Timer RJ individually

Add “Low-speed on-chip oscillator for Timer RJ” on [Clocks] setting. Only when it is checked, low-speed on-chip oscillator can output to Timer RJ.

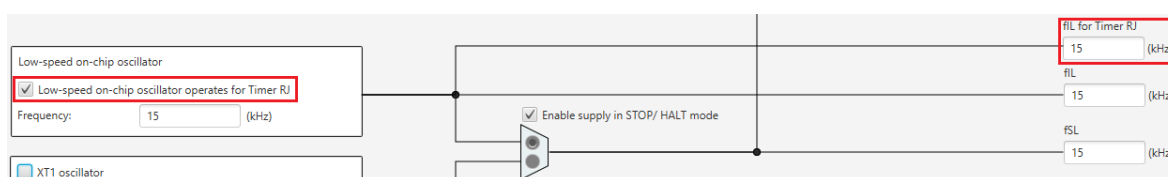


Figure 3-6 Add “Low-speed on-chip oscillator for Timer RJ” on [Clocks] setting

4. List of RENESAS TOOL NEWS AND TECHNICAL UPDATE

Below is a list of notifications delivered by RENESAS TOOL NEWS and TECHNICAL UPDATE.

Issue date	Document No.	Description	Applicable MCUs	Fixed version
Oct. 01, 2021	R20TS0757	1. Notes on creating LLVM for Renesas RL78 C/C++ Executable Project 2. Notes on using Port Input buffer function https://www.renesas.com/document/tnn/notes-e-studio-smart-configurator-plug-smart-configurator-rl78	RL78/G23	V1.2.0
Mar. 16, 2022	R20TS0822	1. Notes when build or clean e ² studio Smart Configurator project https://www.renesas.com/document/tnn/notes-e-studio-smart-configurator-plug-smart-configurator-rl78-0	RL78/G23	V1.3.0
Dec. 01, 2022	R20TS0895	1. Notes when changing version of Board Support Program (BSP) or RL78 Software Integration System (SIS) modules https://www.renesas.com/us/en/document/tnn/notes-e-studio-smart-configurator-rl78-plug-smart-configurator-rl78	RL78/G23 RL78/F24 RL78/G15	V1.5.0

5. Points for Limitation

This section describes points for limitation regarding the Smart Configurator for RL78 V1.6.0.

5.1 List of Limitation

Table 5-1 List of Limitation

✓: Applicable, -: Not Applicable

No	Description	RL78/G23	RL78/F24	RL78/G15	RL78/F23	RL78/G22	RL78/G16	RL78/G24	Remarks
1	Note on extra help document issue	✓	✓	✓	✓	✓	✓	✓	
2	Note on ELCL D flip flop component GUI warning display incorrectly	✓	-	-	-	-	-	-	
3	Note on the unsupported setting items for some ELCL components	✓	-	-	-	-	-	-	
4	Note on CC-RL V1.12 build warning about security option byte	-	✓	-	✓	-	-	-	

5.2 Details of Limitation

5.2.1 Note on extra help document issue

For Smart Configurator, there is an extra help "Smart Browser" under "[Help] > [Help Contents]". Please ignore it.

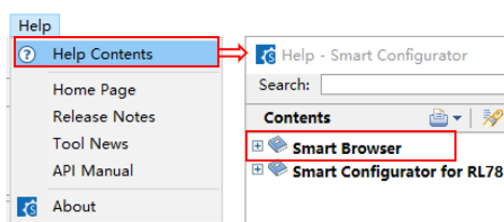


Figure 5-1 Extra help issue

5.2.2 Note on ELCL D flip flop component GUI warning display incorrectly

When selecting the event signal in ELCL D flip flop component, even if the selected signal consists with the hardware specification, there still displays the warning on the GUI.

[Avoidance measure]

Make reference to the hardware manual and set the selectable event signal though warning appeared in GUI, the warning is no impact for the code generation.

The following is example of using flip-flop 0 and flip-flop 1 in ELCL logic cell block L1.

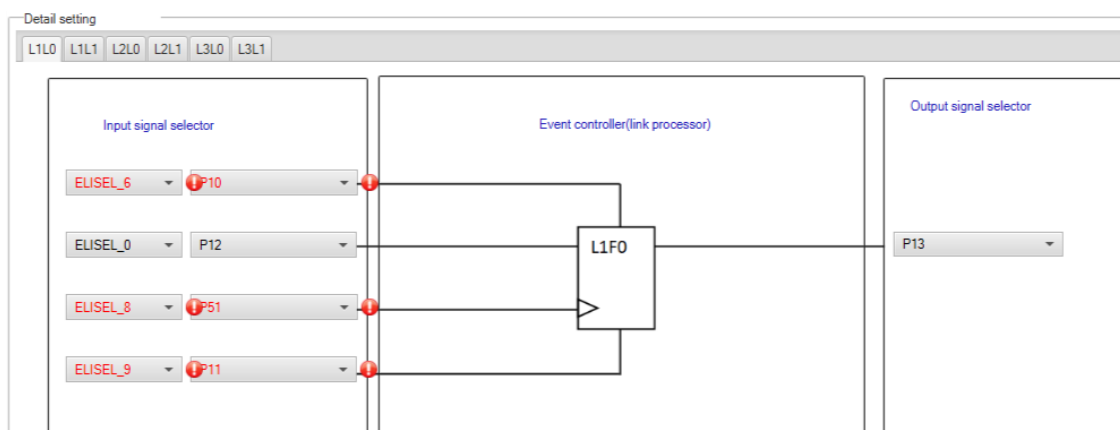


Figure 5-2 The flip-flop 0 in ELCL logic cell block L1 usage example

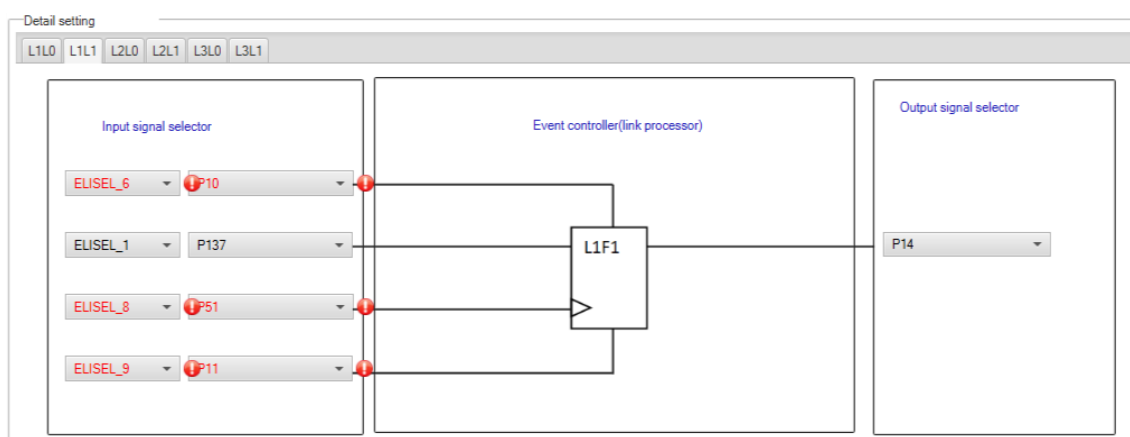


Figure 5-3 The flip-flop 1 in ELCL logic cell block L1 usage example

5.2.3 Note on the unsupported setting items for some ELCL components

In the following ELCL modules, it is not possible to set "no selection (fixed to 0)" as the input signal of the logic cell block and "negative logic output (inverted)" as the output level of the event signal.

- ELCL AND
- ELCL D flip flop
- ELCL EXOR
- ELCL selector
- ELCL Through

[Avoidance measure] None

5.2.4 Note on CC-RL V1.12 build warning about security option byte

In CS+, when the CC-RL compiler version is V1.12, there is a build warning W0561520 about security option byte.

```

Output
>src\smc_gen\r_bsp\mcu\all\cstart.asm
>src\smc_gen\r_bsp\mcu\all\r_bsp_common_ccrl.asm
>DefaultBuild\F24.abs DefaultBuild\F24.mot
W0561520: "security option byte" in ".option_byte" created by device file
Renesas Optimizing Linker Completed
----- Build ended(Error:0, Warning:1) (F24, DefaultBuild) -----
----- Ended(Success:1 Projects, Failed:0 Projects) (2023年3月29日 11:15:05) -----

```

Figure 5-4 CC-RL V1.12 build warning

[Avoidance measure]

Please set CC-RL (Build tool) > Link Options > Device > Set security option byte to "Yes(-SECURITY_OPT_BYTE)", and set "Security option byte value" to "FE", which is default value of security option byte.

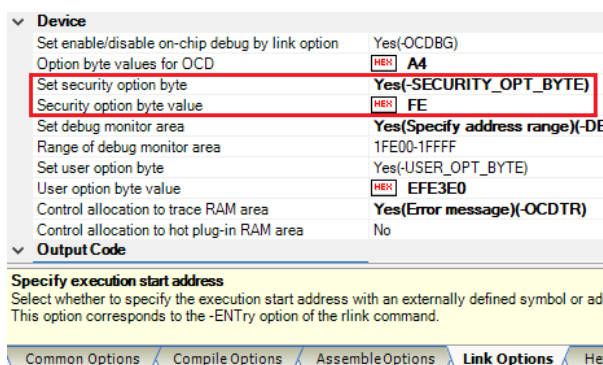


Figure 5-5 Set CS+ property about security option byte

6. Points for Caution

This section describes points for caution regarding the Smart Configurator for RL78 V1.6.0.

6.1 List of Caution

Table 6-1 List of Caution

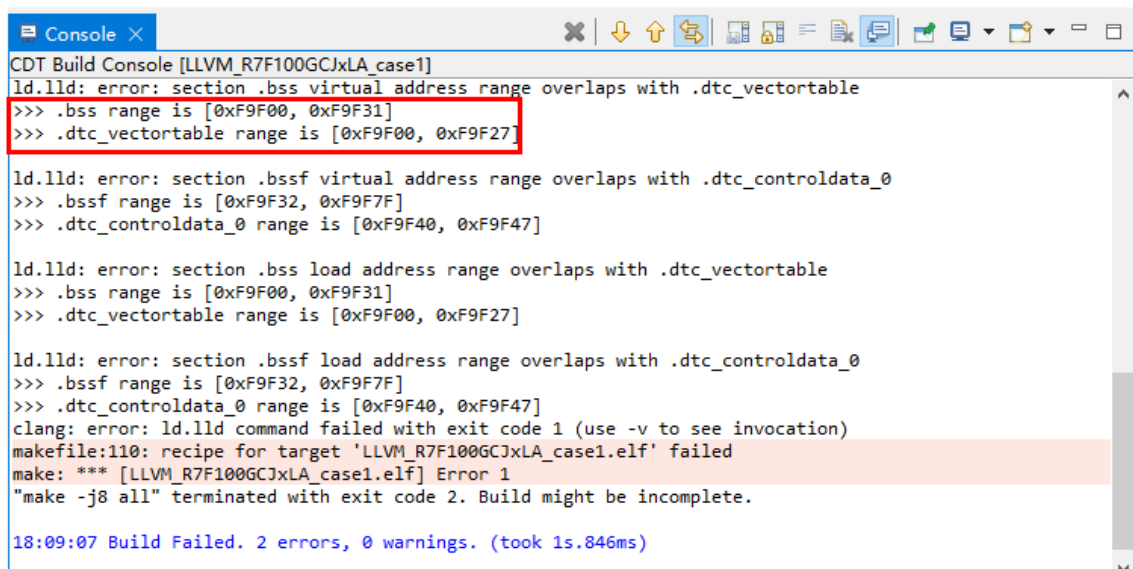
✓ : Applicable, -: Not Applicable

No	Description	RL78/G23	RL78/F24	RL78/G15	RL78/F23	RL78/G22	RL78/G16	RL78/G24	Remarks
1	Note on the build error message such as "section .bss virtual address range overlaps with .dtc_vectortable"	✓	✓	-	✓	✓	-	✓	
2	Note on the installation of the Smart Configurator	✓	✓	✓	✓	✓	✓	✓	
3	Note on using TRDIOA0 for Input capture and TRDIOB0 for Output compare at same time	-	✓	-	-	-	-	✓	
4	Note on pulse width calculation of Timer RD input capture function	-	✓	-	-	-	-	✓	
5	Note on using Touch middleware and UART communication components	✓	-	-	-	-	-	-	
6	Note on the include path update issue when renaming the component's configuration name	✓	✓	✓	✓	✓	✓	✓	
7	Note on TAU Input Signal High/Low level Measurement components.	✓	✓	✓	✓	✓	✓	✓	
8	Note on C++ project of CC-RL V1.12	✓	✓	✓	✓	✓	✓	✓	
9	Note on browsing "Release Notes" and "Tool News" URL from the help menu	✓	✓	✓	-	-	-	-	
10	Note on using user code protection feature	✓	✓	✓	✓	✓	✓	✓	
11	Note on IAR build error when using SMS function	✓	-	-	-	-	-	-	
12	Note on A/D conversion time setting after performing [Change device] or [Change resource]	✓	✓	✓	✓	✓	✓	✓	

6.2 Details of Caution

6.2.1 Note on the build error message such as “section .bss virtual address range overlaps with .dtc_vectortable”

When user use many components and DTC component together, the generated code build might fail due to some section address overlaps.



```
CDT Build Console [LLVM_R7F100GCJxLA_case1]
ld.lld: error: section .bss virtual address range overlaps with .dtc_vectortable
>>> .bss range is [0xF9F00, 0xF9F31]
>>> .dtc_vectortable range is [0xF9F00, 0xF9F27]

ld.lld: error: section .bssf virtual address range overlaps with .dtc_controldata_0
>>> .bssf range is [0xF9F32, 0xF9F7F]
>>> .dtc_controldata_0 range is [0xF9F40, 0xF9F47]

ld.lld: error: section .bss load address range overlaps with .dtc_vectortable
>>> .bss range is [0xF9F00, 0xF9F31]
>>> .dtc_vectortable range is [0xF9F00, 0xF9F27]

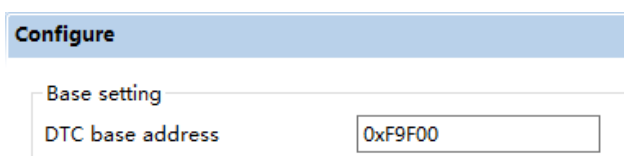
ld.lld: error: section .bssf load address range overlaps with .dtc_controldata_0
>>> .bssf range is [0xF9F32, 0xF9F7F]
>>> .dtc_controldata_0 range is [0xF9F40, 0xF9F47]
clang: error: ld.lld command failed with exit code 1 (use -v to see invocation)
makefile:110: recipe for target 'LLVM_R7F100GCJxLA_case1.elf' failed
make: *** [LLVM_R7F100GCJxLA_case1.elf] Error 1
"make -j8 all" terminated with exit code 2. Build might be incomplete.

18:09:07 Build Failed. 2 errors, 0 warnings. (took 1s.846ms)
```

Figure 6-1 Build error message

[Workaround]

The Smart Configurator cannot set “.bss” and “.bssf” section address. So user should consider to modify “.bss” and “.bssf” section address manually in “linker_script.ld” file or change the DTC base address to avoid such section overlap error.



Configure	
Base setting	
DTC base address	0xF9F00

Figure 6-2 DTC base address setting

6.2.2 Note on the installation of the Smart Configurator

Do not set more than 64 characters for the installation directory.

You might see an error message "The specified path is too long" and will not be able to install Smart Configurator.

6.2.3 Note on using TRDIOA0 for Input capture and TRDIOB0 for Output compare at same time

If user sets up TRDIOA0 for Input capture and TRDIOB0 for Output compare at the same time. Smart Configurator will output a Peripheral conflict error.

User can ignore this Smart Configurator error message and use these two functions at the same time.

6.2.4 Note on pulse width calculation of Timer RD input capture function

The pulse width calculation code is with the assumption that the counter is not cleared between two interrupts occurrence, except the input pulse width which is selected as counter clear trigger on GUI.

For example, when "Clear by TRDGRA0 input capture" is selected, only TRDIOA0 pulse width calculation handle counter clear, other input pulse width calculation doesn't handle counter clear.



Figure 6-3 Counter clear setting in Input capture function

6.2.5 Note on using Touch middleware and UART communication components

When use Touch middleware, please do not change the name of UART components. Otherwise, due the file name mismatch will bring build error.

For example, in touch middleware select UART0 as UART channel, for UART0 component please use Config_UART0.

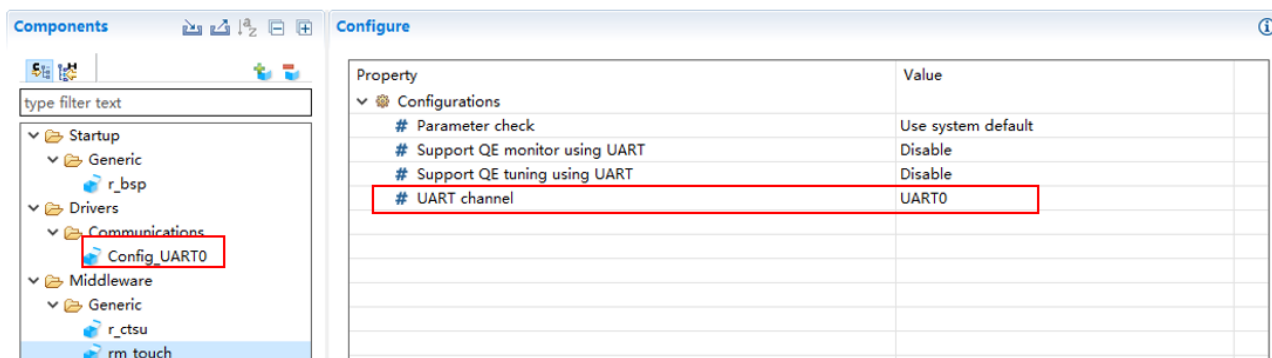


Figure 6-4 Touch middleware and UART communication components

6.2.6 Note on the include path update issue when renaming the component's configuration name

When renaming the added component's configuration in e² studio Smart Configurator project that has self-defined include path setting for any folder or file, include path setting for that folder or file will keep the old name setting after code generation. This will cause build error when compiling the newly generated codes so please manually update the include path.

The folder or file which has self-defined include path setting can be recognized by checking the overlay icon (📁) on that folder or file. Below is an example on how to handle the include path update after renaming Compare Match Timer component configuration.

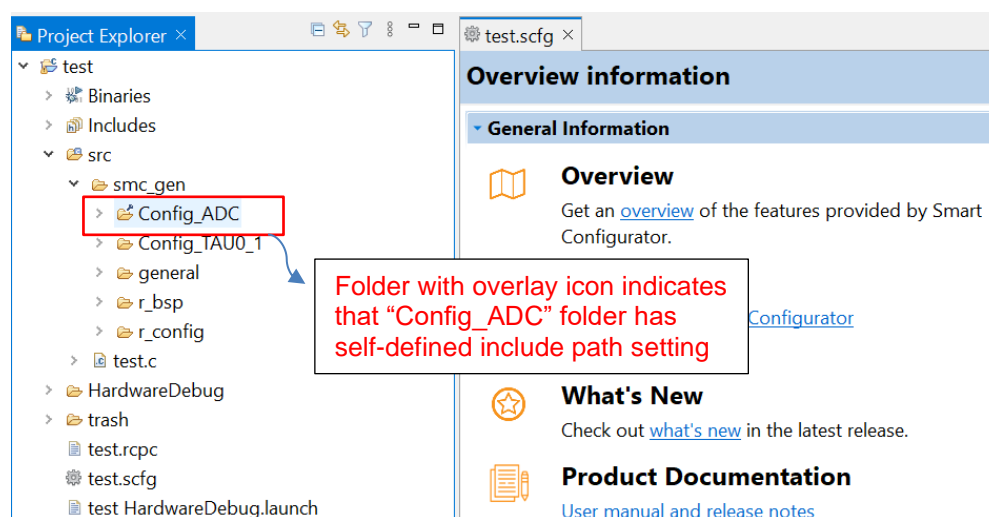


Figure 6-5 Interval Timer component configuration before renaming

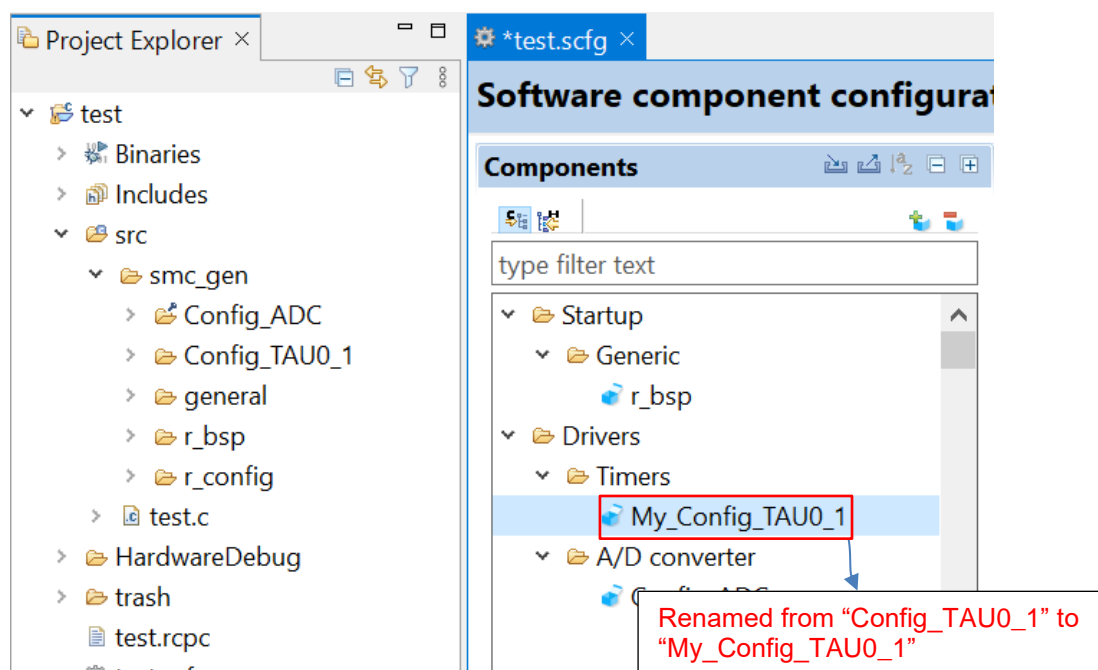


Figure 6-6 The Interval Timer component configuration after renaming

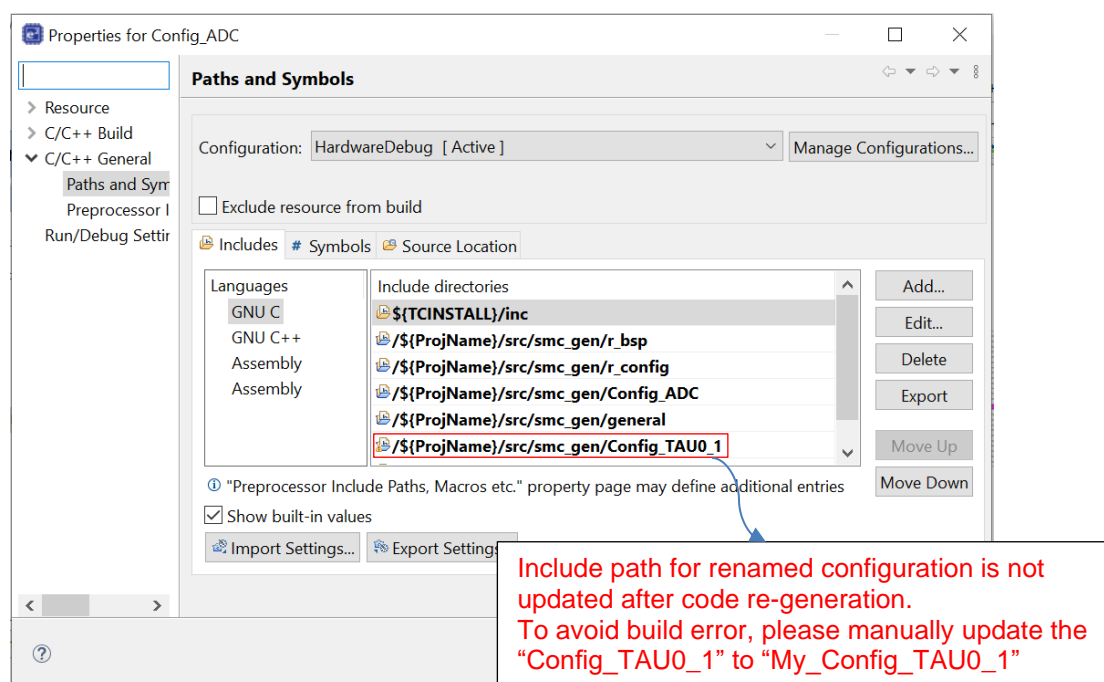


Figure 6-7 Include path setting for the "Config_ADC" configuration

6.2.7 Note on TAU Input Signal High/Low level Measurement component

When using TAU Input Signal High/Low level Measurement component, after used noise filter function for TImn input pulse, please make sure the High/Low level width min value needs to be greater than two times the minimum value prompted on the UI.

For example, the High/Low level width min value is 0.032us (min value), when use noise filter function, the width min value should be 0.064us.



Figure 6-8 High/Low level width min value

6.2.8 Note on CC-RL V1.12 C++ project

In CC-RL V1.12 C++ project, there are some dummy issues such as “EI()” in editor. However this is editor specification and does not affect the program operation. Please ignore it.

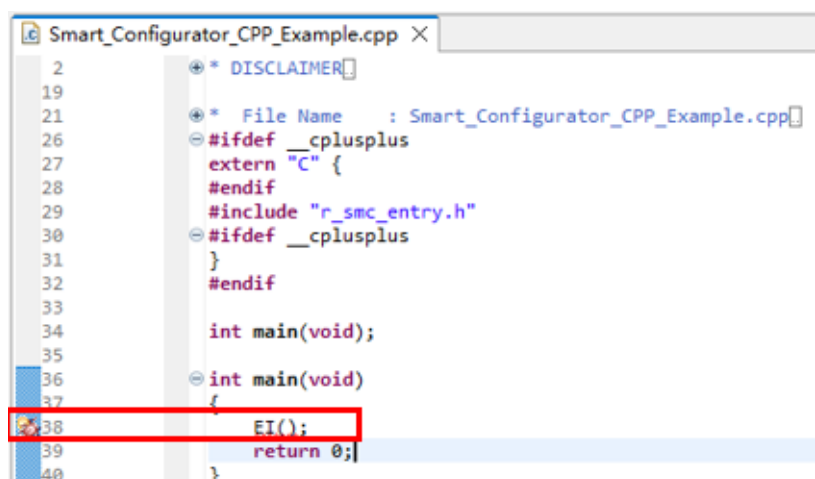


Figure 6-9 CODAN issue in CC-RL V1.12 C++ project

6.2.9 Note on browsing “Release Notes” and “Tool News” URL from the help menu

For Smart Configurator for RL78 V1.4.0 or before version, “Release Notes” and “Tools News” in the help menu cannot access the correct URL. This issue has been fixed from this version.

Please access the URL below directly for Smart Configurator for RL78 V1.4.0 or before version.

Release Notes: <https://www.renesas.com/rl78-smart-configurator-release-note>

Tool News: <https://www.renesas.com/rl78-smart-configurator-tn-notes>

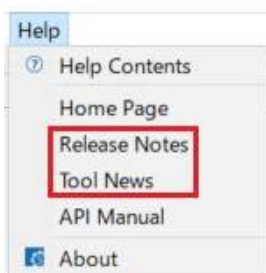


Figure 6-10 Release Notes and Tool News in Smart Configurators

6.2.10 Note on using user code protection feature

From Smart Configurator for RL78 V1.5.0 onwards, user code protection feature will be supported for all Code Generation components. Please use the following specific tags to add user code when using the user code protection feature. If the specific tags do not match exactly, inserted user code will not be protected after the code generation.

```
/* Start user code */
```

User code can be added between the specific tags

```
/* End user code */
```

The user code protection feature will only be supported on the files that are generated by the Code Generation component. Hence, the user code protection feature is not available for non-Code Generation components.

6.2.11 Note on IAR build error when using SMS component

When using SMS component, if the following build error is met in IAR Embedded workbench, please check the build order setting in project [Options...] -> [Custom Build] page.

- 1) When using IAR Embedded workbench V5.10, select "Run before compiling/assembling" (refer to Figure 6-12)
- 2) When using IAR Embedded workbench V4.21, make "Run this tool before all other tools" checked (refer to Figure 6-13)

The above setting can eliminate this build error.



Figure 6-11 IAR build error

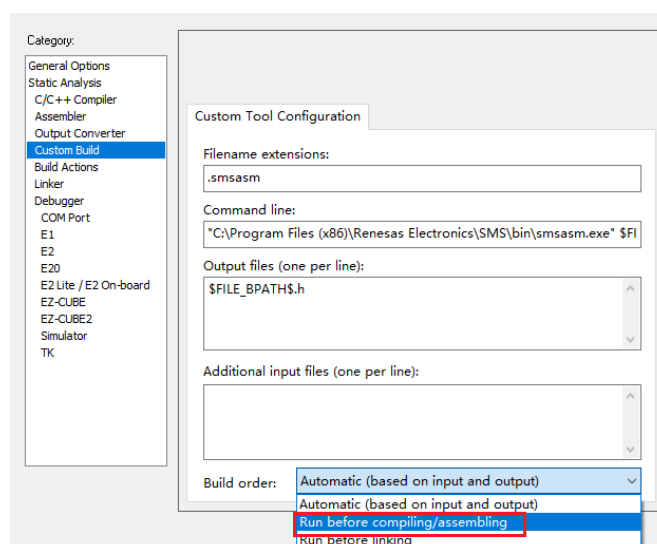


Figure 6-12 "Build order" setting of IAR Embedded workbench V5.10

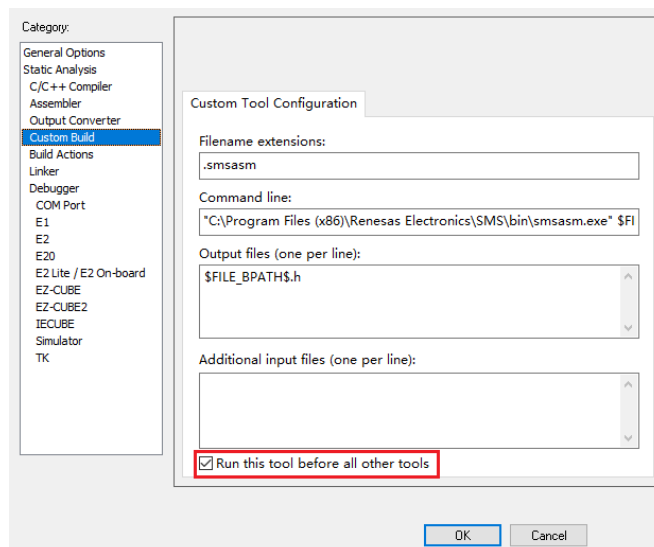


Figure 6-13 Custom build setting of IAR Embedded workbench V4.21

6.2.12 Note on A/D conversion time setting after performing [Change device]

After performing [Change device] (for example, change from RL78/G23 to RL78/G24), the A/D conversion time setting can't be kept. Users should take note to reconfirm the conversion time setting as he wants.

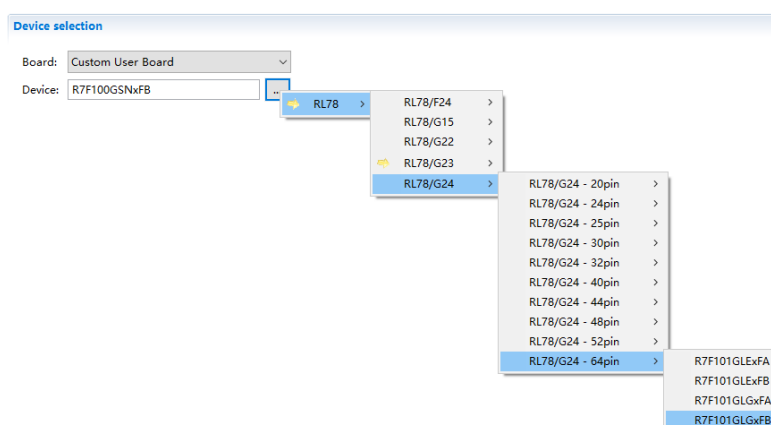


Figure 6-14 [Change device] operation

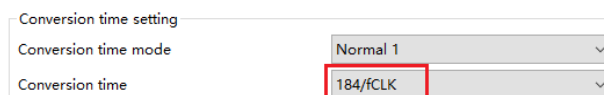


Figure 6-15 A/D conversion time setting

Revision History

Rev.	Section	Description
1.00	-	First edition issued

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.

2. Processing at power-on

The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.

3. Input of signal during power-off state

Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.

4. Handling of unused pins

Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.

5. Clock signals

After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.

6. Voltage application waveform at input pin

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).

7. Prohibition of access to reserved addresses

Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.

8. Differences between products

Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan

www.renesas.com

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