ISL73141SEHMF7

Total Dose Test Report

Introduction

This report documents the results of Low Dose Rate (LDR) total dose testing and subsequent high temperature biased annealing of the ISL73141SEHMF7 5V, 14-Bit, 1Msps Successive Approximation Register (SAR) Analog-to-Digital Converter. The tests were conducted to provide an assessment of the total dose hardness of the part and to provide an estimate of bias or anneal sensitivity. Parts were irradiated biased and unbiased at LDR (0.01rad(Si)/s) to 100krad(Si), followed by a 168-hour high temperature anneal at 100°C under bias. The ISL73141SEHMF7 is rated to 75krad(Si) at LDR.

Product Description

The ISL73141SEHMF7 is a radiation hardened high precision 14-bit, 1Msps SAR Analog-to-Digital Converter (ADC) that features Signal-to-Noise Ratio (SNR) of 82.1dBFS and dissipates only 60mW when operating from a 5V supply.

The ISL73141SEHMF7 features 1Msps throughput at 5V with no data latency and features excellent linearity and dynamic accuracy. It also provides a high-speed SPI-compatible serial interface that supports logic ranging from 2.2V to 3.6V using a separate digital I/O supply pin.

The ISL73141SEHMF7 provides a separate power-down pin that reduces power dissipation to <50µW. The analog input signal range is determined by an external reference.

The ISL73141SEHMF7 operates across the military temperature range from -55°C to +125°C and is available in a 14 Ld hermetically sealed Ceramic Dual Flat-Pack (CDFP) package.

The block diagram for the ISL73141SEHMF7 is shown in Figure 1.

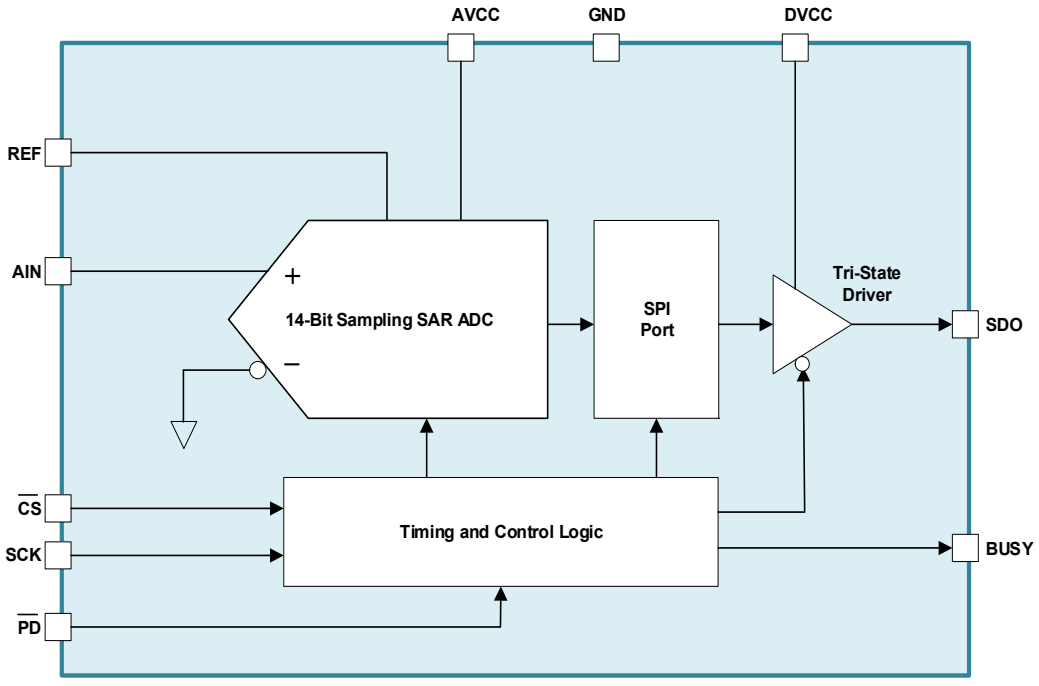


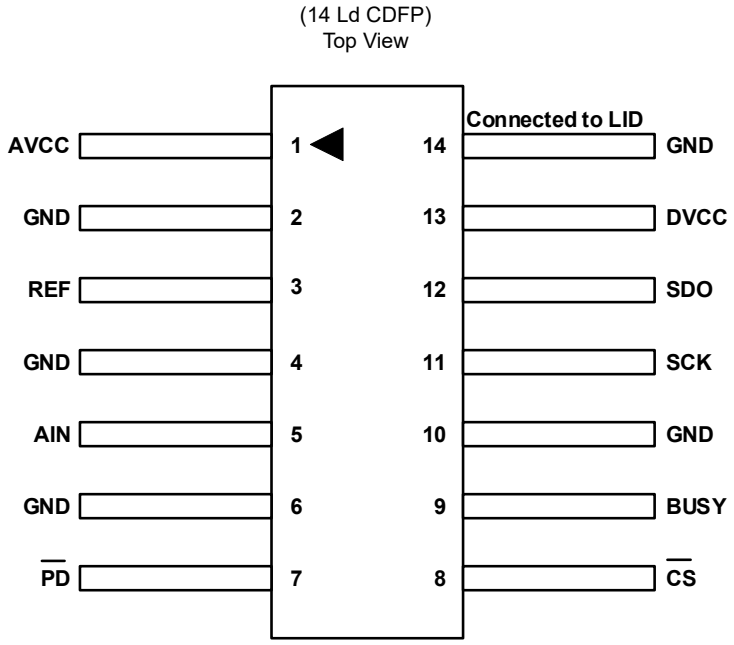
Figure 1. ISL73141SEHMF7 Block Diagram

Related Literature

For a full list of related documents, visit our website:

- ISL73141SEH device page
- MIL-STD-883 Test Method 1019

The pin configuration for the ISL73141SEHMF7 is shown in Figure 2 with the pin descriptions shown in Table 1.



Note: The ESD triangular mark is indicative of Pin #1. It is a part of the device marking and is placed on the lid in the quadrant where Pin #1 is located.

Figure 2. ISL73141SEHMF7 Package and Pin Configurations

Table 1. ISL73141SEHMF7 Pin Descriptions

Pin Number	Pin Name	Description
1	AVCC	Analog supply. The supply range is 4.5V to 5.5V. Bypass this pin to GND with a 10µF ceramic capacitor.
2, 4, 6, 10, 14	GND	Analog and digital supply ground. Connect these pins directly to the PCB GND plane. Pin 14 (GND pin) is electrically connected to the package seal ring and lid.
3	REF	Reference input. The input range of REF is 3.9V to 4.2V. The voltage at the REF pin (V_{REF}) defines the input range of the analog input as 0V to V_{REF}. Bypass REF to GND with a low ESR 10µF ceramic capacitor.
5	AIN	Analog input. AIN supports an input voltage range of 0V to V_{REF}.
8	$\overline{CS}$	Convert Start Low input. A falling edge on this input starts a new conversion. The conversion is timed using an internal oscillator. The device automatically powers down following the conversion process. The logic state of the $\overline{CS}$ pin controls the state of the SDO pin. A logic high on the $\overline{CS}$ pin disables the SDO pin driver and the SDO pin impedance is Hi-Z. A logic low on the $\overline{CS}$ pin enables the SDO driver (unless $\overline{PD}$ is low) and allows data to be read out following a conversion.
7	$\overline{PD}$	Power-down low input. When this pin is brought low the ADC enters power-down mode. If this occurs during a conversion, the conversion is halted and the SDO pin is placed in Hi-Z. Logic levels are determined by DV_{CC}.
9	BUSY	Busy output. A logic high indicates a conversion is in progress. The BUSY indicator returns low following the completion of a conversion. Logic levels are determined by DV_{CC}.
11	SCK	Serial data clock input. When $\overline{CS}$ is low and the BUSY indicator is low, the conversion result is shifted out on SDO on the rising edges of SCK, Most Significant Bit (MSB) first to Least Significant Bit (LSB) last. Logic levels are determined by DV_{CC}. SCK should be held low when it is not being asserted.
12	SDO	Serial data output. The current conversion result is serially shifted out on this pin on the rising edges of SCK, MSB first to LSB last. The data stream is composed of 14 bits of conversion data followed by trailing zeros. Logic Levels are determined by DV_{CC}.
13	DVCC	Digital I/O supply. Voltage range on this pin is 2.2V to 3.6V. DV_{CC} is nominally set to the same supply voltage as the host interface (2.5V or 3.3V). Bypass DVCC to GND with 0.1µF capacitor.
LID	N/A	Package Lid is internally connected to GND through Pin 14.

1. Test Description

1.1 Irradiation Facilities

The irradiation was performed at 0.01rad(Si)/s using the Intersil Palm Bay Hopewell Designs N40 panoramic commercial irradiator. This irradiator uses PbAl spectrum hardening filters to shield the test board and devices under test against low energy secondary gamma radiation. Biased irradiation and annealing were performed on all samples following irradiation, at 100°C for 168 hours in a small temperature chamber.

1.2 Test Fixturing

Figure 3 shows the configuration used for biased irradiation.

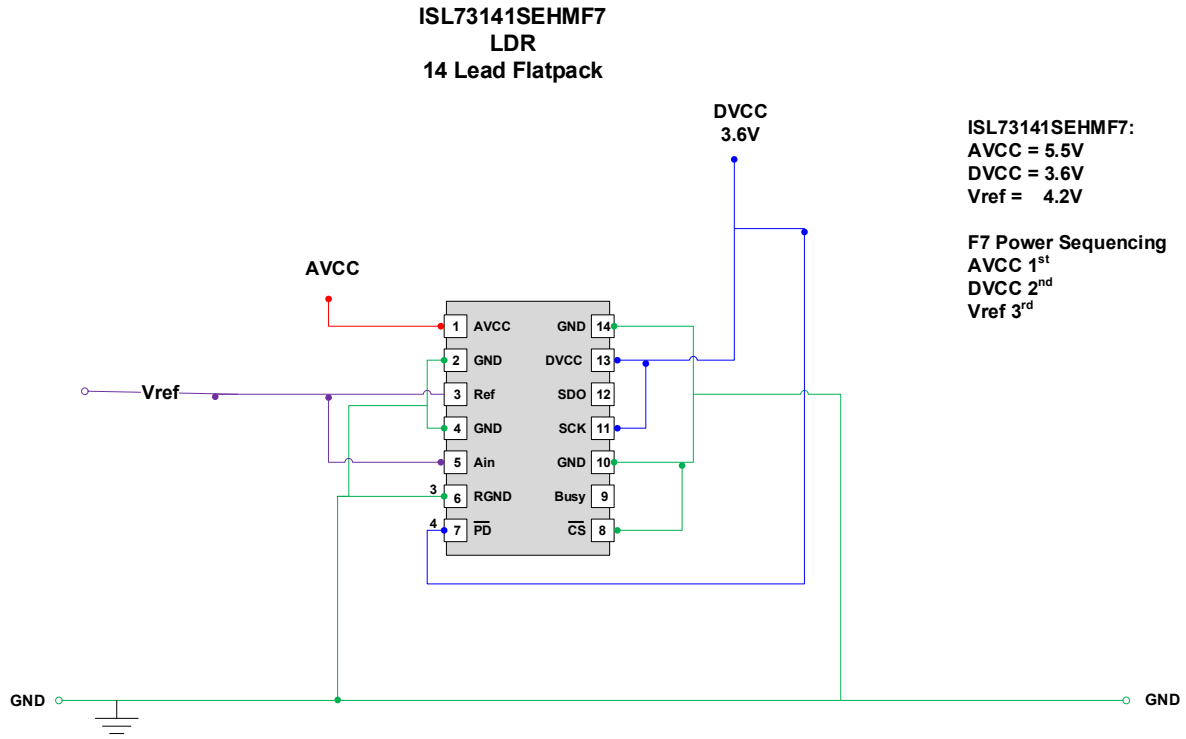


Figure 3. ISL73141SEHMF7 TID Bias Schematic

1.3 Characterization Equipment and Procedures

All electrical testing was performed at room temperature outside the irradiator, using production Automated Test Equipment (ATE) with data logging at each downpoint.

1.4 Experimental Matrix

Irradiation was performed in accordance with the guidelines of MIL-STD-883 Test Method 1019. The experimental matrix consisted of 15 samples irradiated under bias and 12 samples irradiated with all pins grounded. At anneal all 24 samples were biased. Because of the board limitations only 9 samples from the grounded bias group could be put on anneal.

The ISL73141SEHMF7 samples were drawn from wafer lots V6C498, V6C565, and V6C566. All samples were packaged in the standard 14 Ld SDFP package.

1.5 Downpoints

Downpoints for the tests were 0, 10, 30, 50, 75, and 100krad(Si), followed by a 168-hour high temperature anneal at 100°C under bias, as described in Experimental Matrix.

2. Test Results

2.1 Attributes Data

Total dose testing of the ISL73141SEHMF7 is complete. All tested parameters passed the datasheet limits. Table 2 summarizes the results.

Table 2. ISL73141SEHMF7 Total Dose Test Attributes Data

Dose Rate (rad(Si)/s)	Condition	Sample Size	Downpoint	Pass (Note 1)	Fail
0.01	Biased (Figure 3)	15	Pre-irradiation	15	
			10krad(Si)	15	0
			30krad(Si)	15	0
			50krad(Si)	15	0
			75krad(Si)	15	0
			100krad(Si)	15	0
			Anneal	15	0
0.01	GND	12	Pre-irradiation	12	
			10krad(Si)	12	0
			30krad(Si)	12	0
			50krad(Si)	12	0
			75krad(Si)	12	0
			100krad(Si)	12	0
			Anneal	9	0

Note:
1. A pass indicates a sample that passes all post-irradiation datasheet limits.

2.2 Key Parameter Variables Data

The plots in Figure 4 through Figure 32 illustrate the TID response of selected parameters as shown in Table 3 in the Appendix. The plots show the average tested values of the key parameters as a function of total dose for both conditions, biased and grounded, and post anneal (PA). The plots also include error bars at each downpoint, representing the minimum and maximum measured values of the samples, although in some plots the error bars are not visible because of their values compared to the scale of the graph.

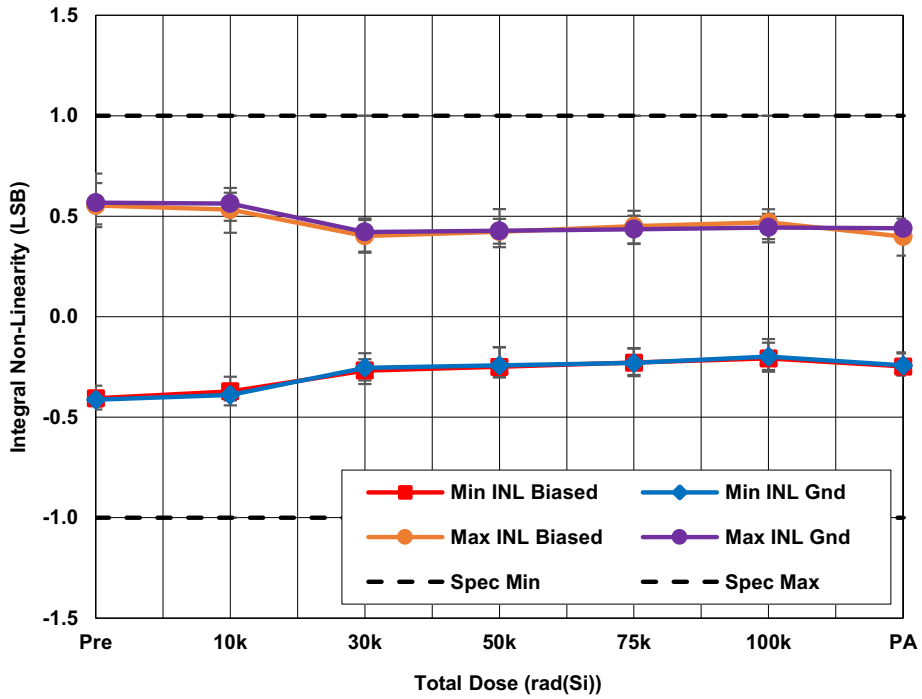


Figure 4. ISL73141SEHMF7 average minimum and maximum integral non-linearity (INL) with AV_{CC} = 5V, DV_{CC} = 2.5V, REF = 4.096V, f_{SAMP} = 1Msps, and A_{IN} = full-scale sine wave as a function of LDR irradiation and anneal. The error bars represent the minimum and maximum measured values. The datasheet limits are -1 LSB minimum and 1 LSB maximum.

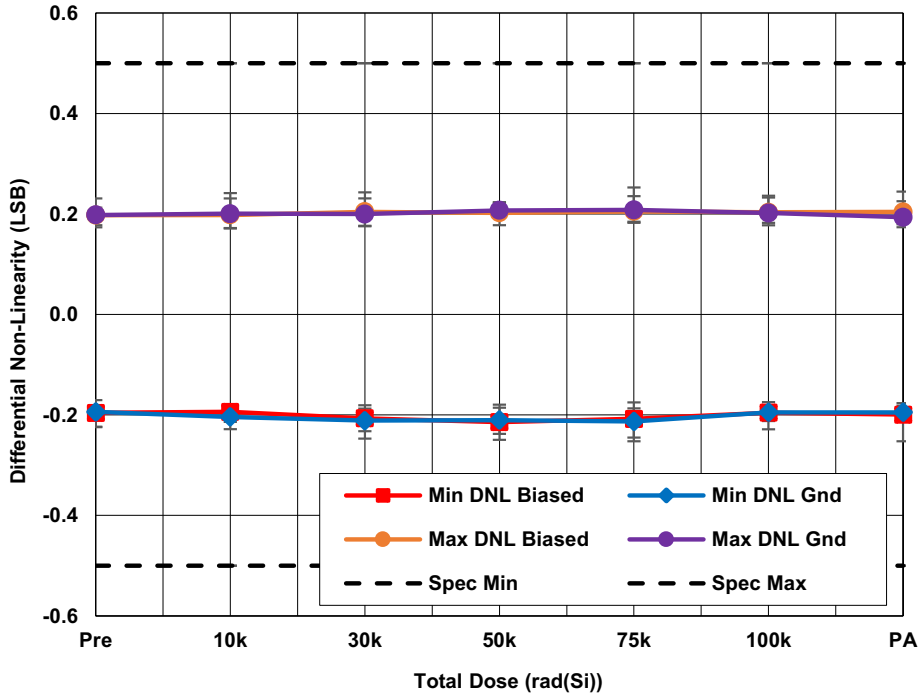


Figure 5. ISL73141SEHMF7 average minimum and maximum differential non-linearity (DNL) with AV_{CC} = 5V, DV_{CC} = 2.5V, REF = 4.096V, f_{SAMP} = 1Msps, and A_{IN} = full-scale sine wave as a function of LDR irradiation and anneal. The error bars represent the minimum and maximum measured values. The datasheet limits are -0.5 LSB minimum and 0.5 LSB maximum.

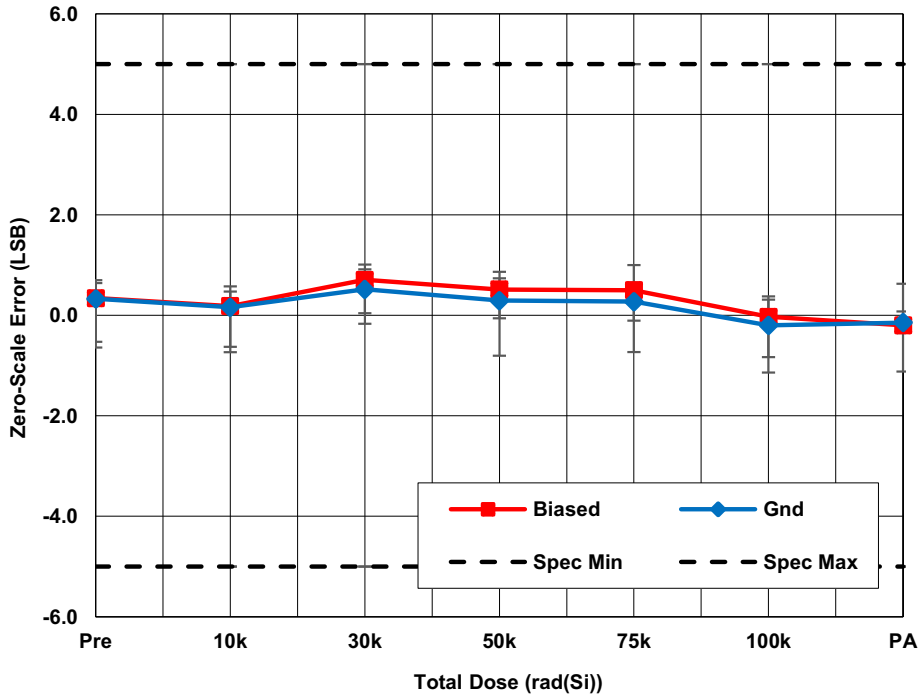


Figure 6. ISL73141SEHMF7 average zero-scale error (VOFF) with AV_{CC} = 5V, DV_{CC} = 2.5V, REF = 4.096V, f_{SAMP} = 1Msps, and A_{IN} = GND as a function of LDR irradiation and anneal. The error bars represent the minimum and maximum measured values. The datasheet limits are -5 LSB minimum and 5 LSB maximum.

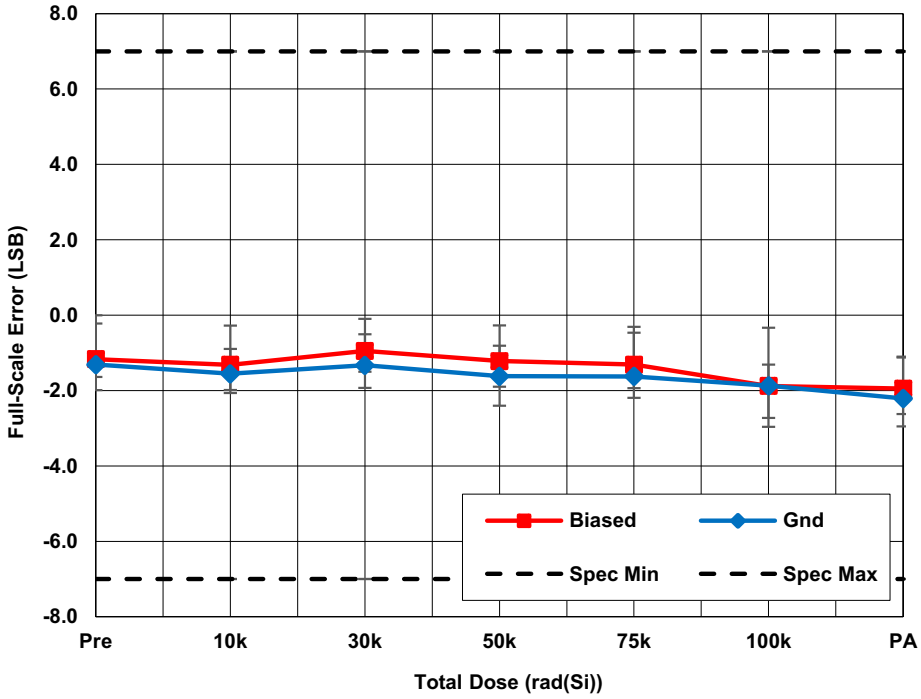


Figure 7. ISL73141SEHMF7 average full-scale error (FSE) with AV_{CC} = 5.0V, DV_{CC} = 2.5V, REF = 4.096V, f_{SAMP} = 1Msps, and A_{IN} = VREF as a function of LDR irradiation and anneal. The error bars represent the minimum and maximum measured values. The datasheet limits are -7 LSB minimum and 7 LSB maximum.

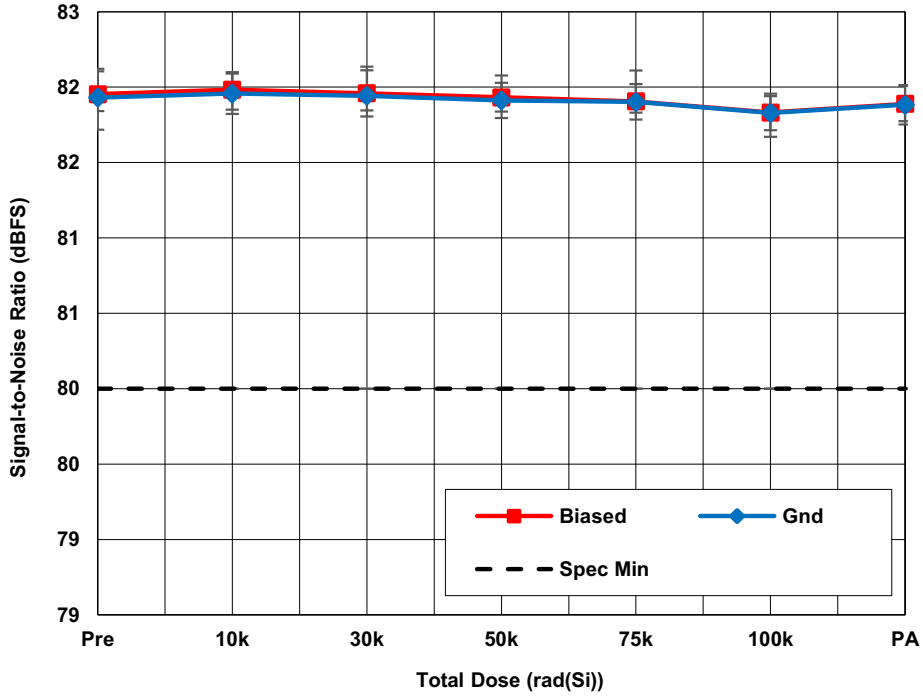


Figure 8. ilSL73141SEHMF7 average signal-to-noise ratio (SNR) with AV_{CC} = 5.0V, DV_{CC} = 2.5V, REF = 4.096V, f_{SAMP} = 105ksps and A_{IN} = -1dBFS as a function of LDR irradiation and anneal. The error bars represent the minimum and maximum measured values. The datasheet limit is 80dB minimum.

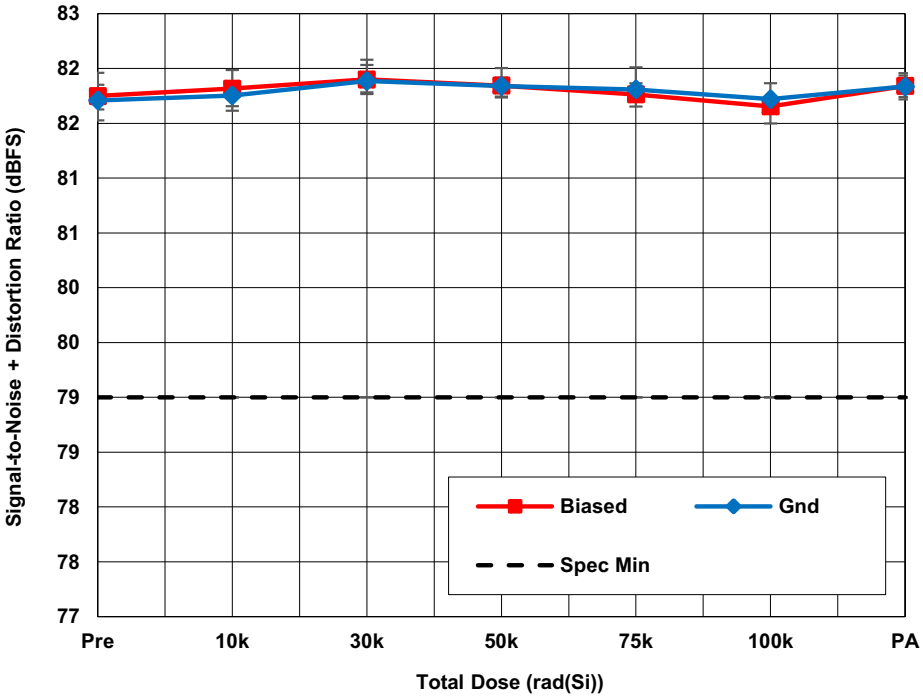


Figure 9. ISL73141SEHMF7 average signal-to-noise + distortion ratio (SINAD) with AV_{CC} = 5.0V, DV_{CC} = 2.5V, REF = 4.096V, f_{SAMP} = 105ksps, and A_{IN} = -1dBFS as a function of LDR irradiation and anneal. The error bars represent the minimum and maximum measured values. The datasheet limit is 79dB minimum.

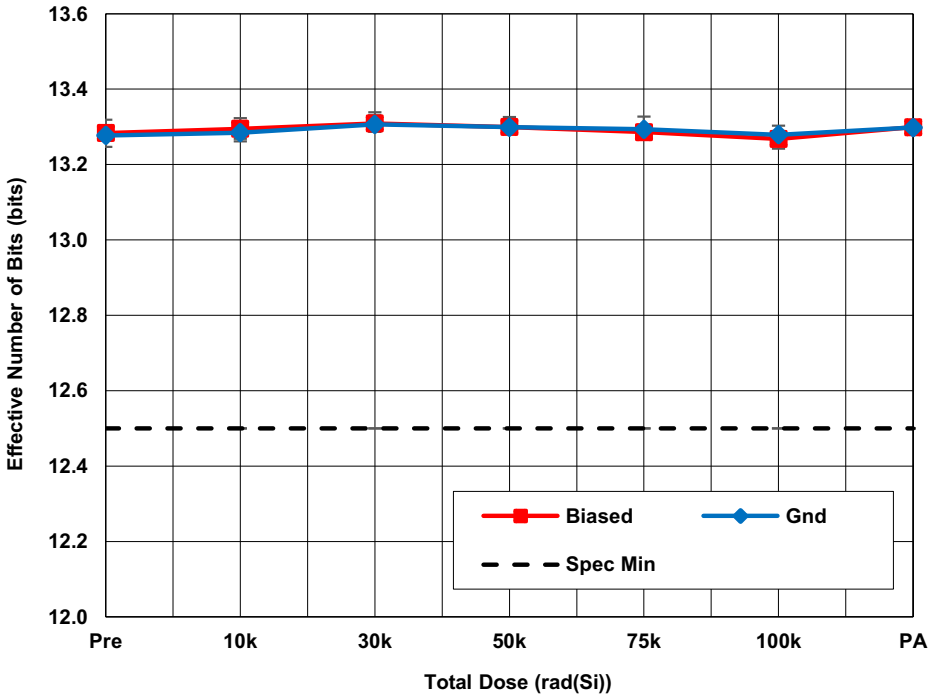


Figure 10. ISL73141SEHMF7 average effective number of bits (ENOB) with AV_{CC} = 5.0V, DV_{CC} = 2.5V, REF = 4.096V, f_{SAMP} = 105ksps, and A_{IN} = -1dBFS as a function of LDR irradiation and anneal. The error bars represent the minimum and maximum measured values. The datasheet limit is 12.5 bits minimum.

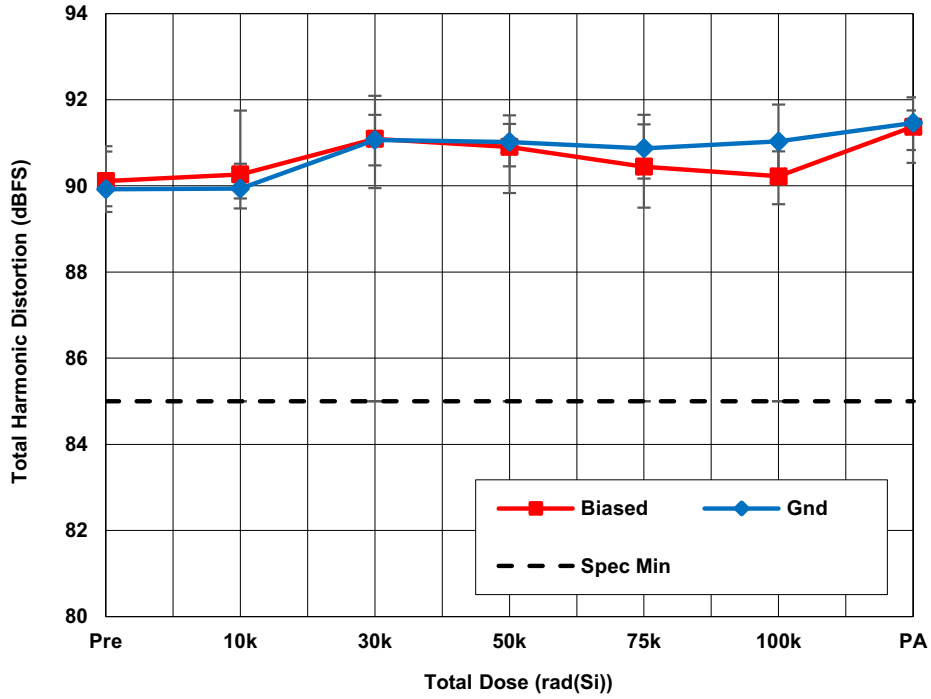


Figure 11. .ISL73141SEHMF7 average total harmonic distortion (THD) with AV_{CC} = 5.0V, DV_{CC} = 2.5V, REF = 4.096V, f_{SAMP} = 105ksps (first five harmonics), and A_{IN} = -1dBFS as a function of LDR irradiation and anneal. The error bars represent the minimum and maximum measured values. The datasheet limit is 85dB minimum.

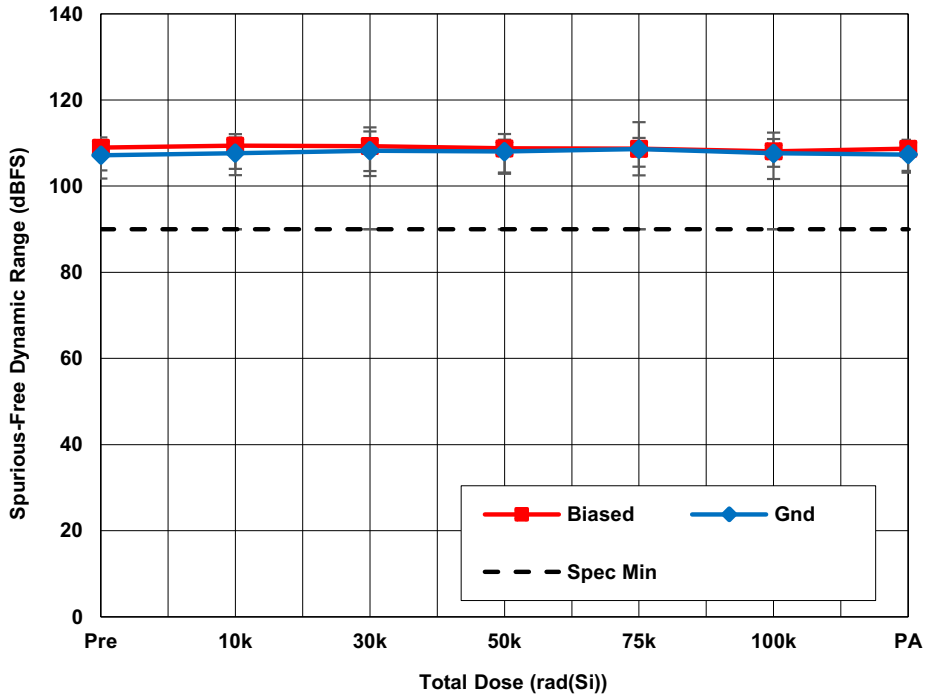


Figure 12. ISL73141SEHMF7 average spurious-free dynamic range (SFDR) with AV_{CC} = 5V, DV_{CC} = 2.5V, REF = 4.096V, f_{SAMP} = 105ksps (first five harmonics), and A_{IN} = -1dBFS as a function of LDR irradiation and anneal. The error bars represent the minimum and maximum measured values. The datasheet limit is 90 dB minimum.

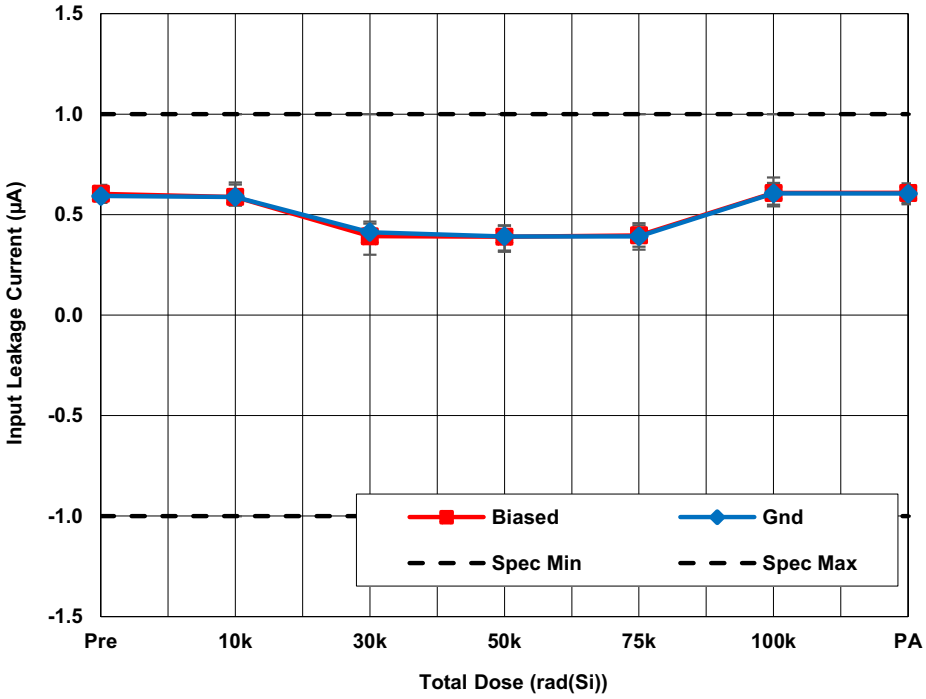


Figure 13. ISL73141SEHMF7 average input leakage current (IA_{IN}) with AV_{CC} = 5V, DV_{CC} = 2.5V, REF = 4.096V as a function of LDR irradiation and anneal. The error bars represent the minimum and maximum measured values. The datasheets limits are -1µA minimum and 1µA maximum.

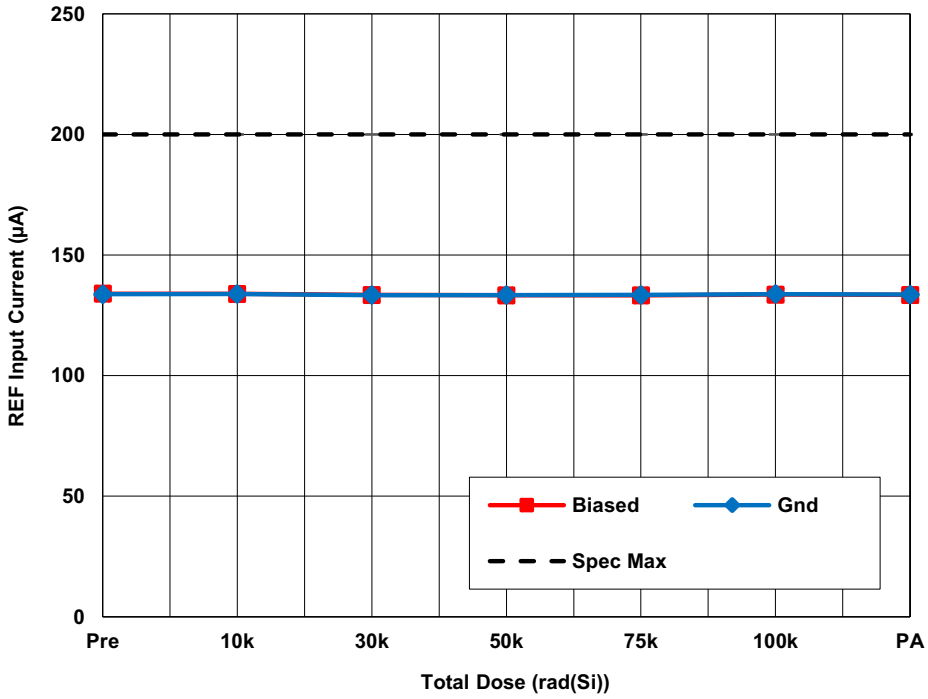


Figure 14. .ISL73141SEHMF7 average REF input current (I_{REF}) with AV_{CC} = 5V, DV_{CC} = 2.5V, REF = 4.096V as a function of LDR irradiation and anneal. The error bars represent the minimum and maximum measured values. The datasheet limit is 200µA maximum.

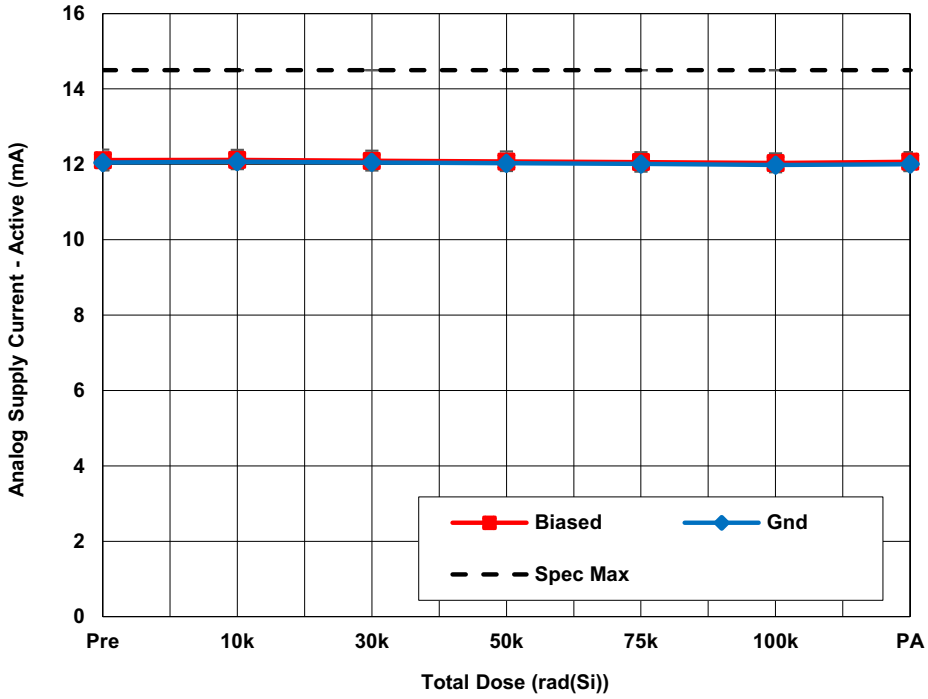


Figure 15. ISL73141SEHMF7 average analog supply current - active (I_{AVCC}) with AV_{CC} = 5V, DV_{CC} = 2.5V, REF = 4.096V, f_{SAMP} = 1Msps, and A_{IN} = -1dBFS as a function of LDR irradiation and anneal. The error bars represent the minimum and maximum measured values. The datasheet limit is 14.5mA maximum.

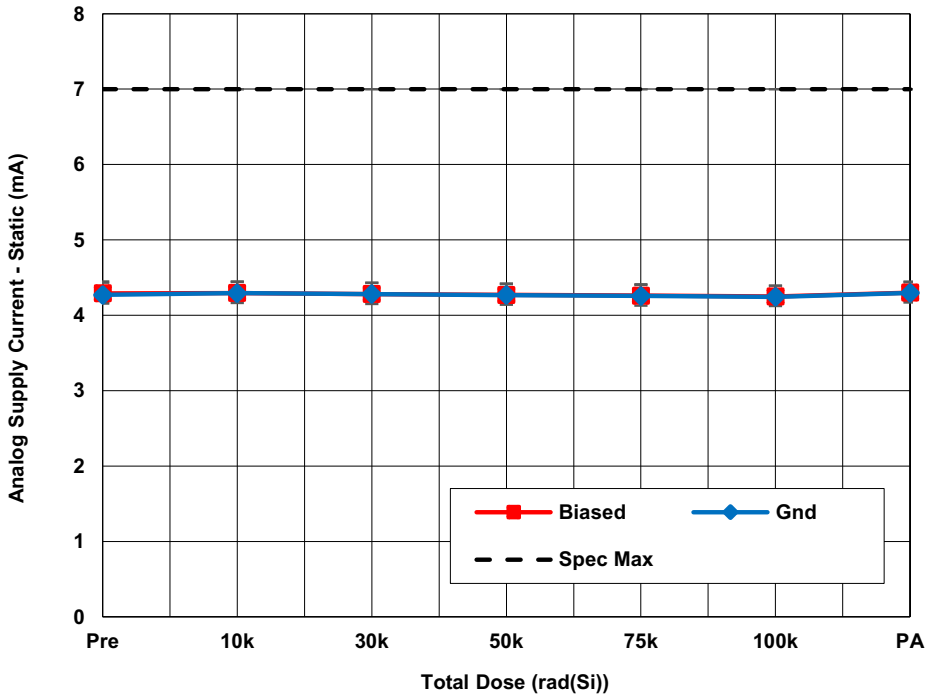


Figure 16. ISL73141SEHMF7 average analog supply current - static (I_{STATIC}) with AV_{CC} = 5V, DV_{CC} = 2.5V, REF = 4.096V, and $\overline{CS}$ = DVCC as a function of LDR irradiation and anneal. The error bars represent the minimum and maximum measured values. The datasheet limit is 7mA maximum.

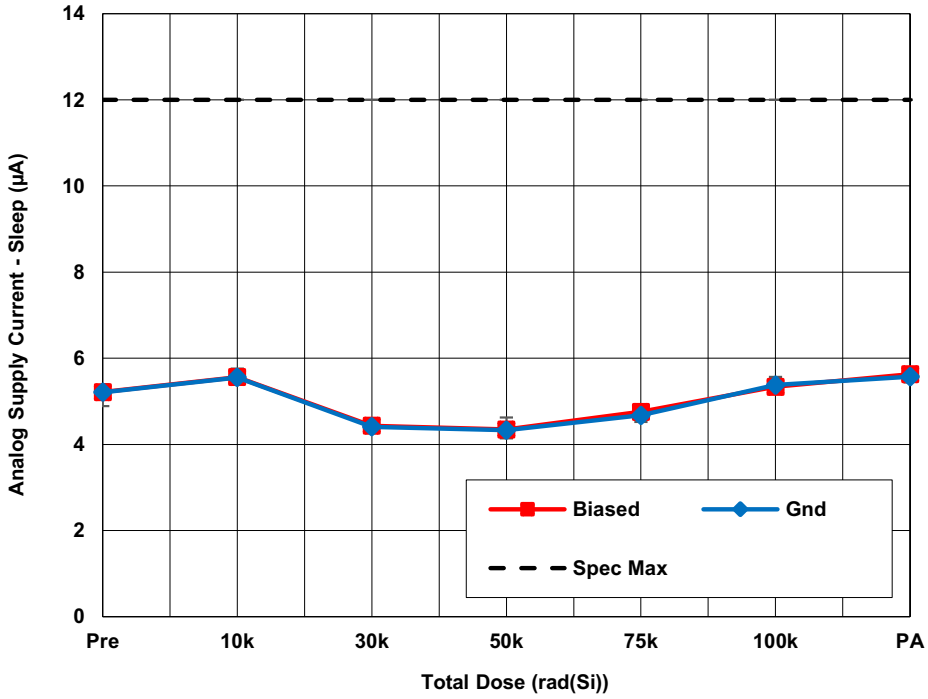


Figure 17. ISL73141SEHMF7 average analog supply current - sleep (I_{SLAVCC}) with AV_{CC} = 5V, DV_{CC} = 2.5V, REF = 4.096V, and $\overline{PD}$ = GND as a function of LDR irradiation and anneal. The error bars represent the minimum and maximum measured values. The datasheet limit is 12µA maximum.

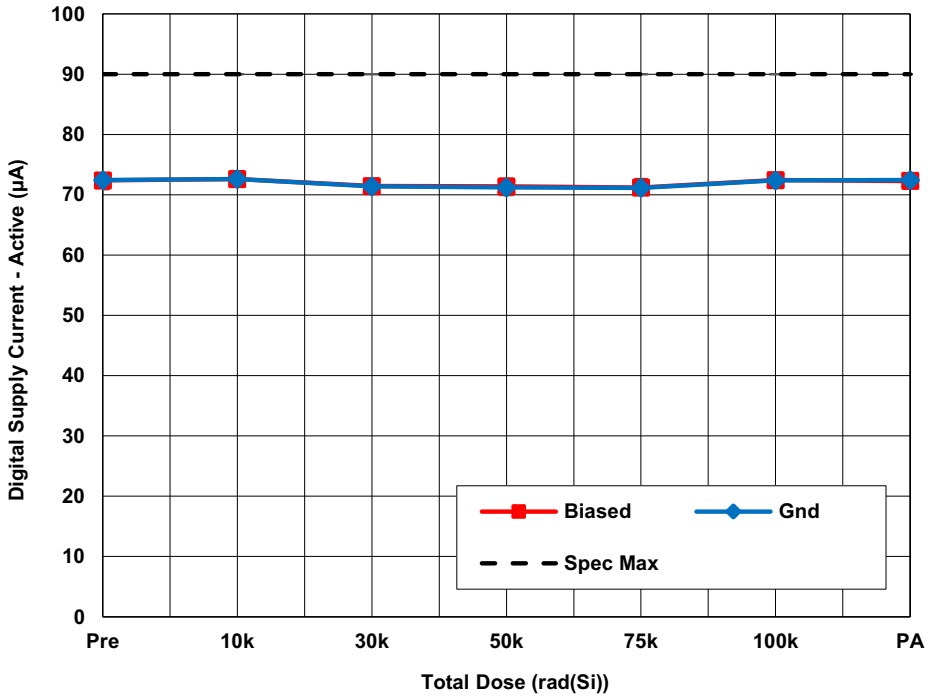


Figure 18. ISL73141SEHMF7 average digital supply current - active (I_{DVCC}) with AV_{CC} = 5V, DV_{CC} = 2.5V, REF = 4.096V, f_{SCK} = 50MHz, and C_L = 10pF as a function of LDR irradiation and anneal. The error bars represent the minimum and maximum measured values. The datasheet limit is 90µA maximum.

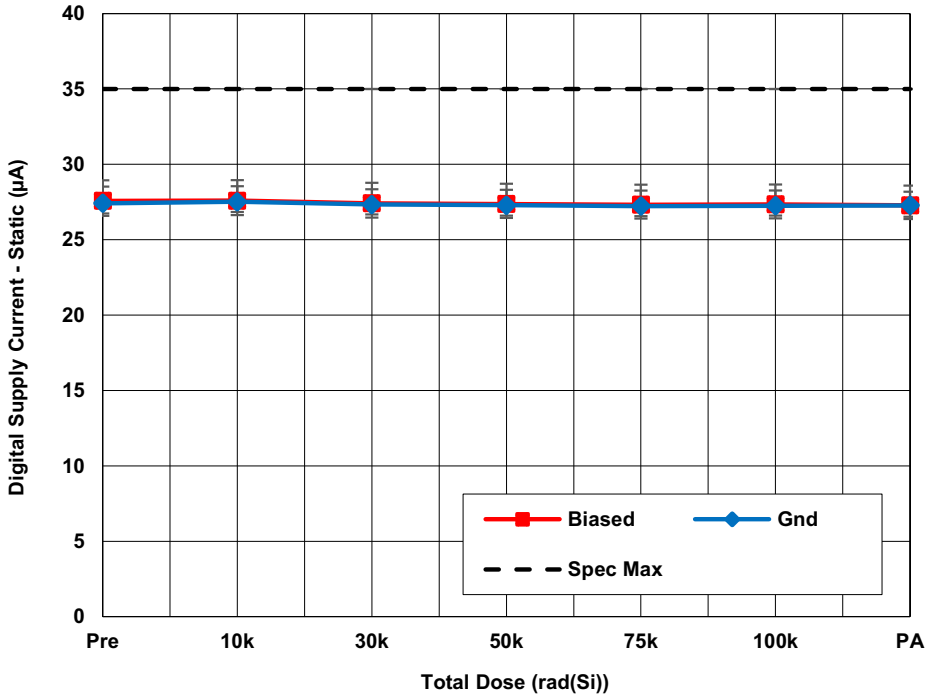


Figure 19. ISL73141SEHMF7 average digital supply current - static (I_{STDVCC}) with AV_{CC} = 5V, DV_{CC} = 2.5V, REF = 4.096V, and $\overline{CS}$ = DV_{CC} as a function of LDR irradiation and anneal. The error bars represent the minimum and maximum measured values. The datasheet limit is 35µA maximum.

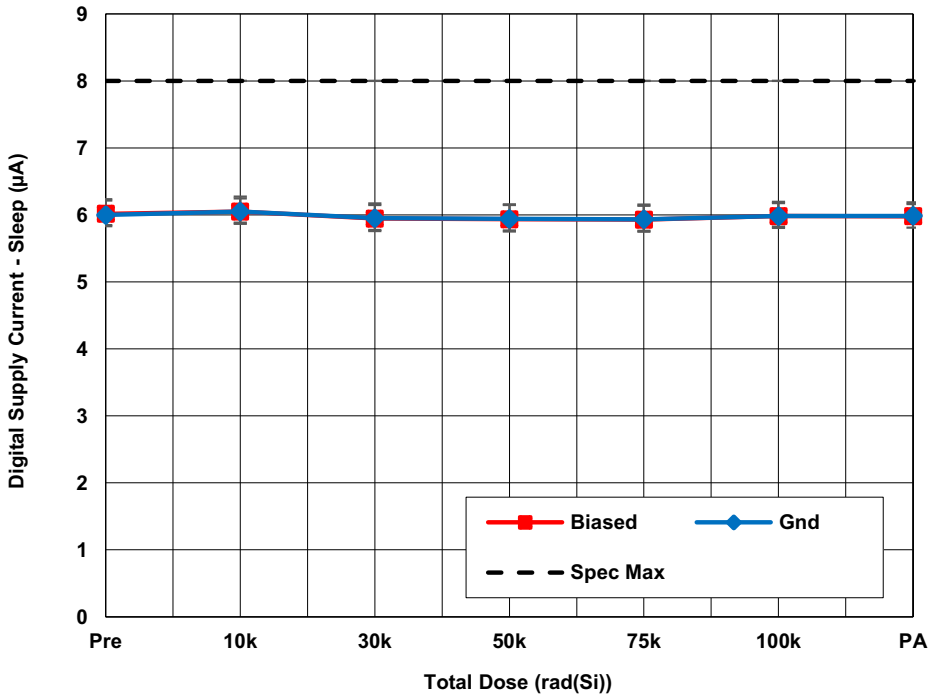


Figure 20. ISL73141SEHMF7 average digital supply current - sleep (I_{SLDVCC}) with AV_{CC} = 5V, DV_{CC} = 2.5V, REF = 4.096V, $\overline{PD}$ = GND as a function of LDR irradiation and anneal. The error bars represent the minimum and maximum measured values. The datasheet limit is 8µA maximum.

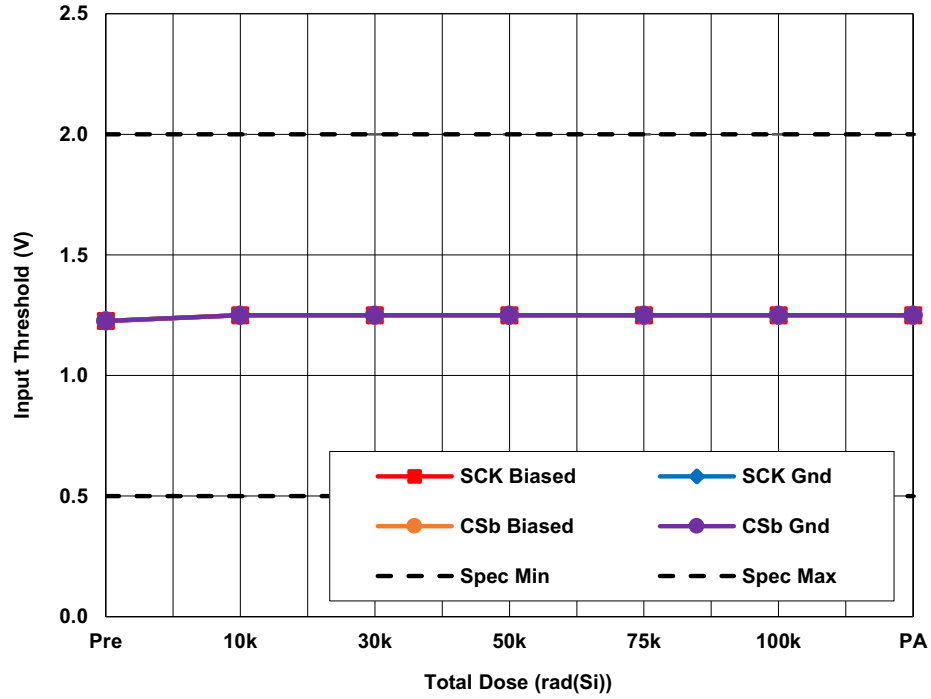


Figure 21. ISL73141SEHMF7 average high-level input (V_{IH}) and low level input (V_{IL}) with AV_{CC} = 5V, DV_{CC} = 2.5V, REF = 4.096V as a function of LDR irradiation and anneal. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limit for V_{IH} is 2.0V minimum and the datasheet limit for V_{IL} is 0.5V maximum.

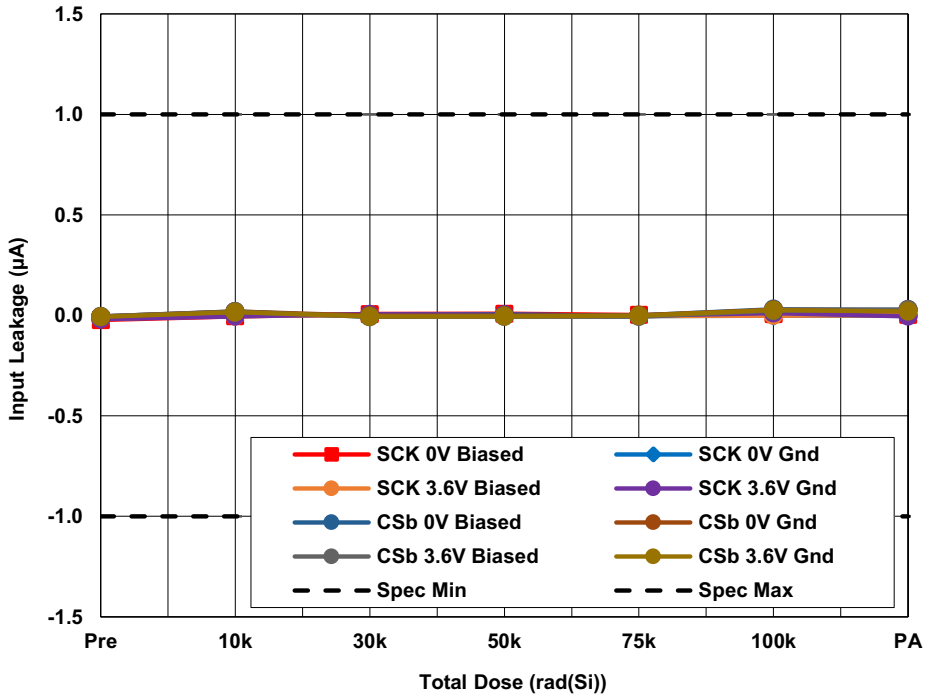


Figure 22. ISL73141SEHMF7 average input leakage current (I_{IN}) on SCK and $\overline{CS}$ with AV_{CC} = 5V, DV_{CC} = 2.5V, REF = 4.096V and V_{IN} = 0V and 5V as a function of LDR irradiation and anneal. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limits are -1µA minimum and 1µA maximum.

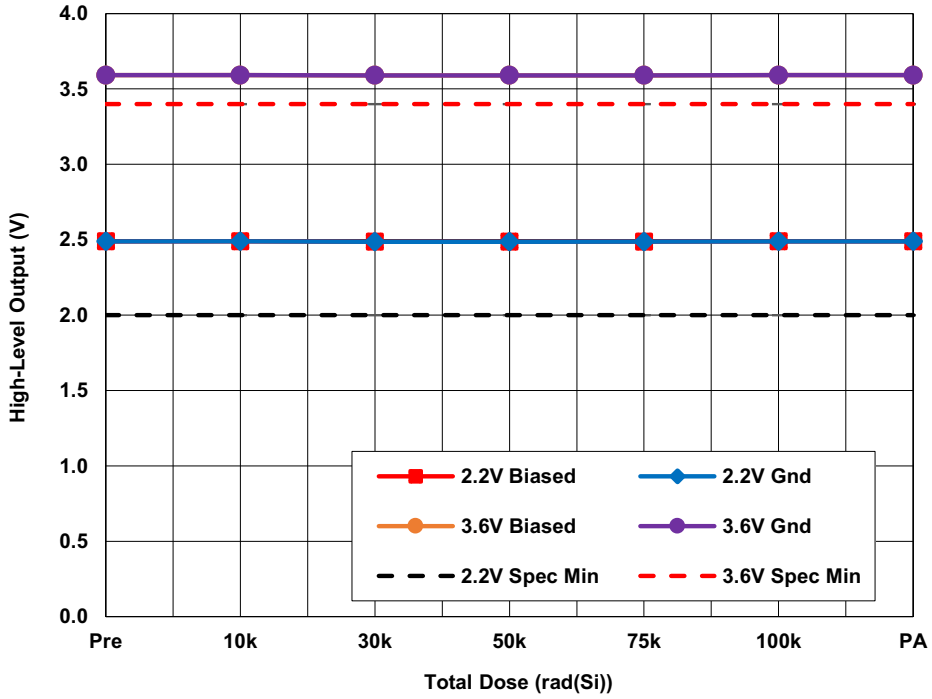


Figure 23. ISL73141SEHMF7 average high-level output (V_{OH}) with AV_{CC} = 5V, DV_{CC} = 2.2V and 3.6V, REF = 4.096V and I_O = -500µA as a function of LDR irradiation and anneal. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limits are 2.0V minimum for DV_{CC} = 2.2V and 3.4V minimum for DV_{CC} = 3.6V.

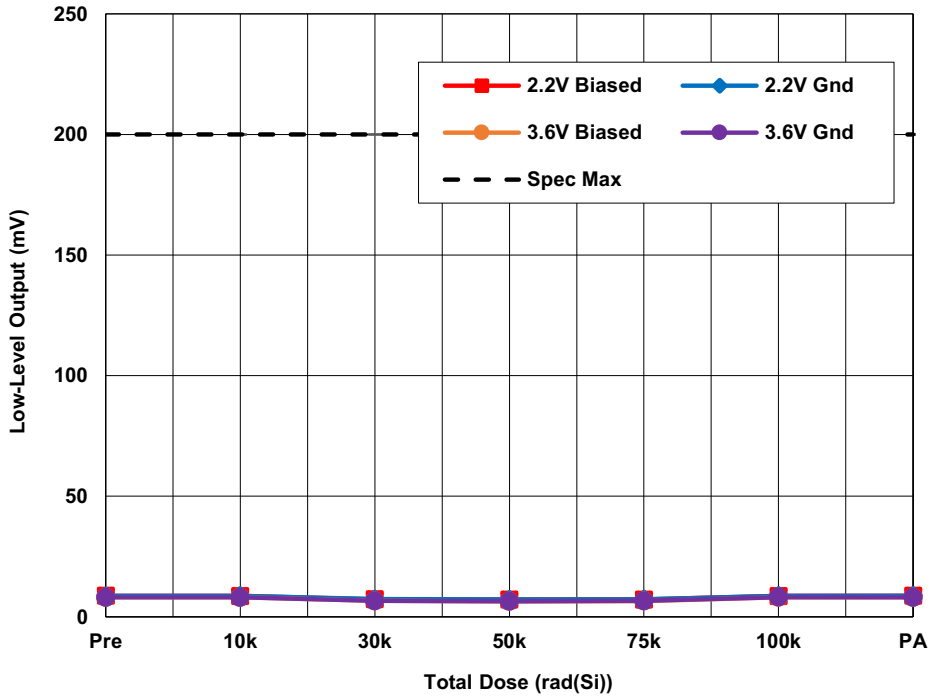


Figure 24. ISL73141SEHMF7 average low-level output (V_{OL}) with AV_{CC} = 5V, DV_{CC} = 2.5V and 3.6V, REF = 4.096V, and I_O = 500µA as a function of LDR irradiation and anneal. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limit is 200mV maximum.

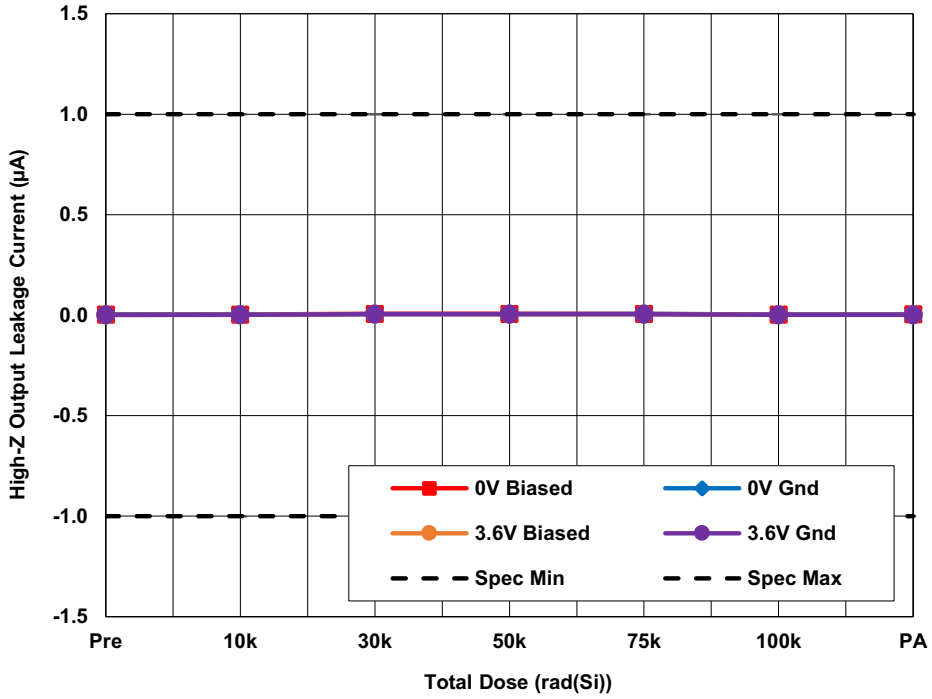


Figure 25. ISL73141SEHMF7 average output leakage current (I_{OZ}) with AV_{CC} = 5V, DV_{CC} = 3.6V, REF = 4.096V, as a function of LDR irradiation and anneal. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limits are -1µA minimum and 1µA maximum.

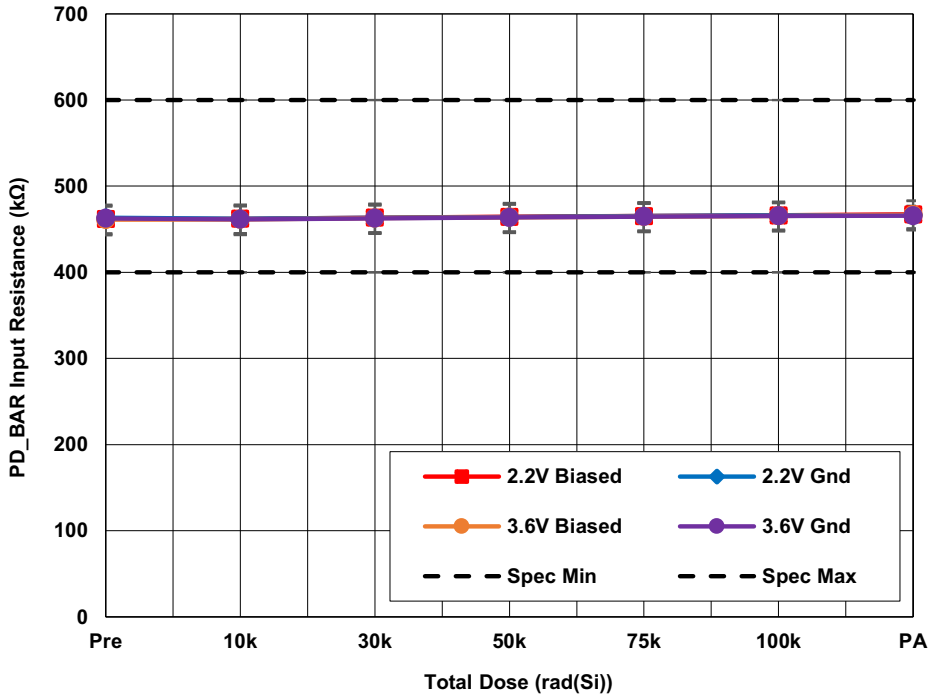


Figure 26. ISL73141SEHMF7 average $\overline{PD}$ input resistance (R_{INPDL}) with AV_{CC} = 5V, DV_{CC} = 2.2V and 3.6V and REF = 4.096V as a function of LDR irradiation and anneal. The error bars represent the minimum and maximum measured values. The datasheet limits are 400kΩ minimum and 600kΩ maximum.

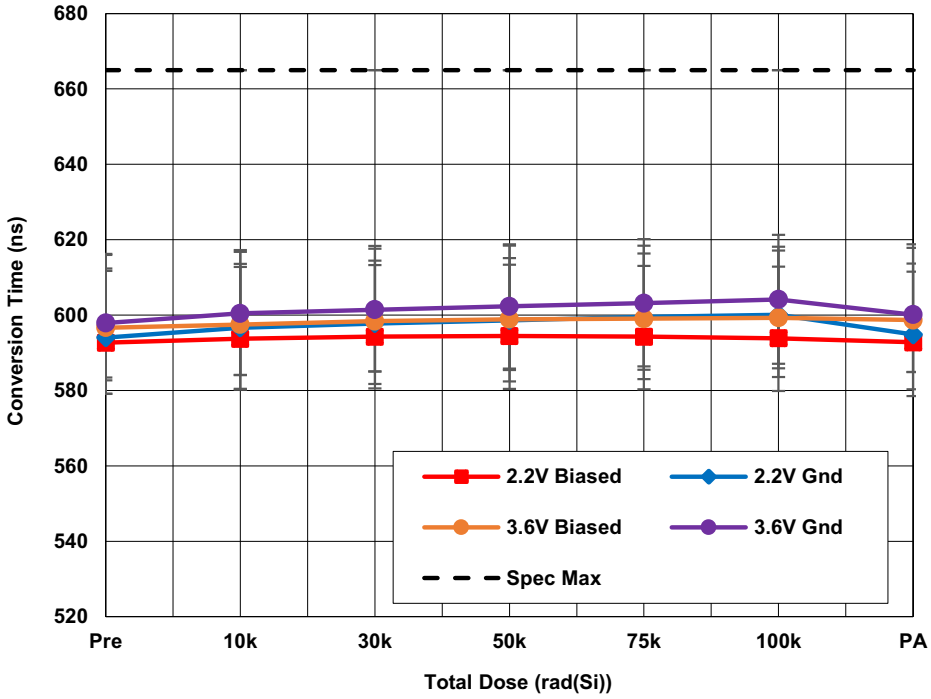


Figure 27. ISL73141SEHMF7 average conversion time (t_{CONV}) with AV_{CC} = 4.5V, DV_{CC} = 2.2V and AV_{CC} = 5.5V, DV_{CC} = 3.6V, REF = 4.096V, f_{SAMP} = 1Msps, and A_{IN} = -1dbFS as a function of LDR irradiation and anneal. The error bars represent the minimum and maximum measured values. The datasheet limit is 665ns maximum.

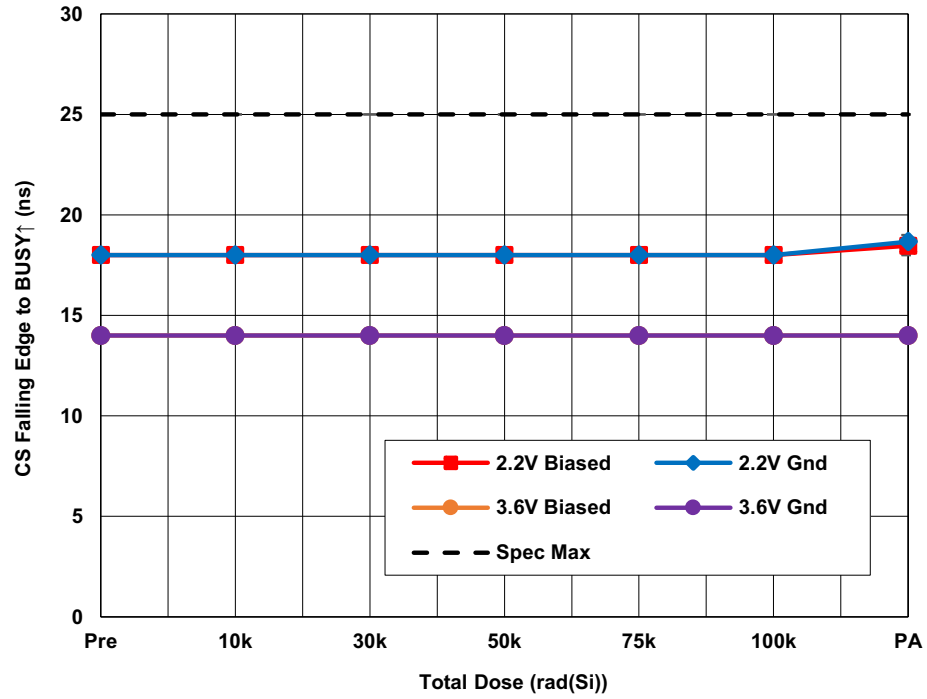


Figure 28. ISL73141SEHMF7 average $\overline{CS}$ falling edge to BUSY rising edge (t_{BUSYLH}) with AV_{CC} = 4.5V, DV_{CC} = 2.2V and AV_{CC} = 5.5V, DV_{CC} = 3.6V, REF = 4.096V, f_{SAMP} = 1Msps, A_{IN} = -1dbFS and C_L = 10pF as a function of LDR irradiation and anneal. The error bars represent the minimum and maximum measured values. The datasheet limit is 25ns maximum.

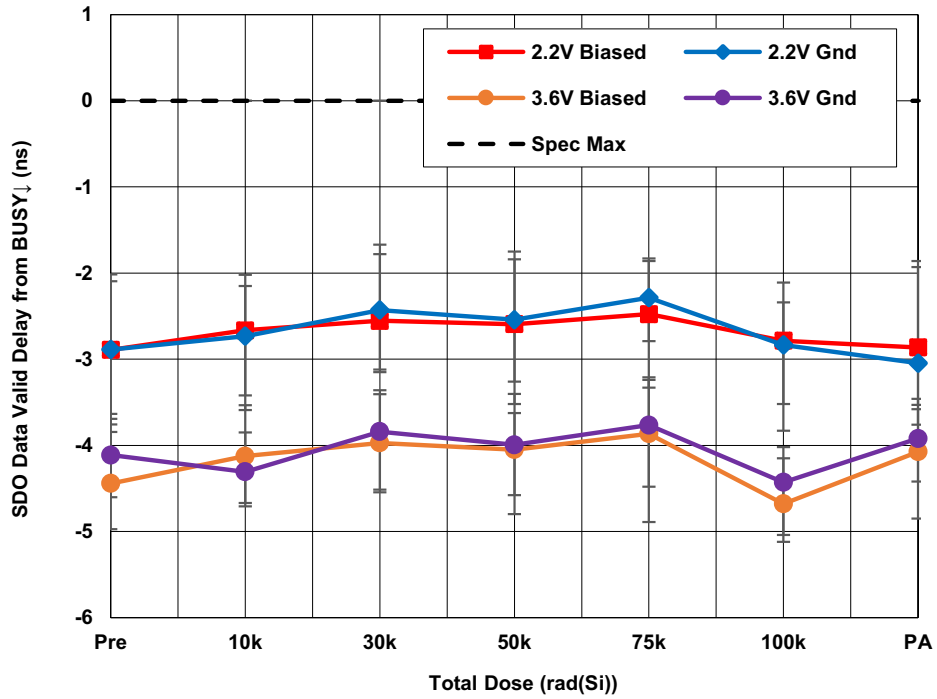


Figure 29. ISL73141SEHMF7 average SDO data valid delay from BUSY falling edge ($t_{DBUSYLSDOV}$) with AV_{CC} = 4.5V, DV_{CC} = 2.2V and AV_{CC} = 5.5V, DV_{CC} = 3.6V, REF = 4.096V, f_{SAMP} = 1Msps, A_{IN} = -1dbFS and C_L = 10pF as a function of LDR irradiation and anneal. The error bars represent the minimum and maximum measured values. The datasheet limit is 0ns maximum.

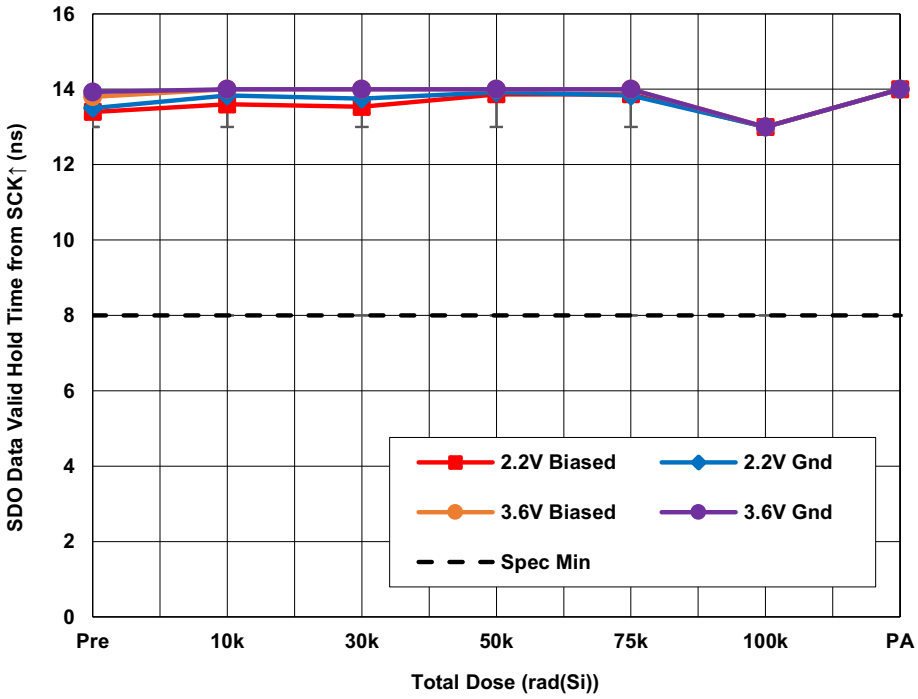


Figure 30. ISL73141SEHMF7 average SDO data valid hold time from SCK rising edge (t_{HSDOV}) with AV_{CC} = 4.5V, DV_{CC} = 2.2V and AV_{CC} = 5.5V, DV_{CC} = 3.6V, REF = 4.096V, f_{SAMP} = 1Msps, A_{IN} = -1dbFS, and C_L = 10pF as a function of LDR irradiation and anneal. The error bars represent the minimum and maximum measured values. The datasheet limit is 8ns minimum.

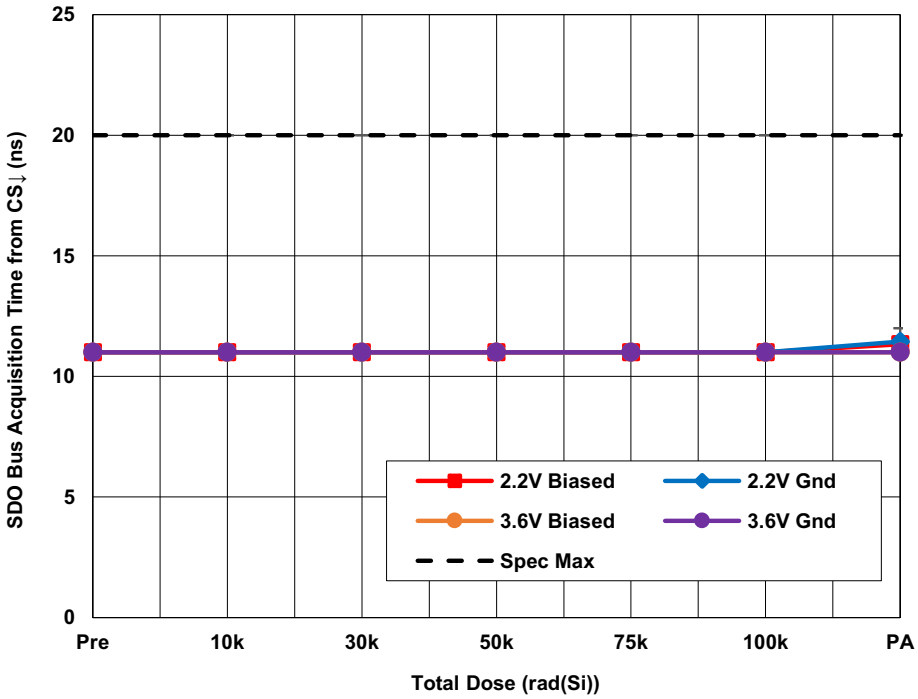


Figure 31. ISL73141SEHMF7 average SDO bus acquisition time from $\overline{CS}$ falling edge ($t_{DCSLSDOL}$) with AV_{CC} = 4.5V, DV_{CC} = 2.2V and AV_{CC} = 5.5V, DV_{CC} = 3.6V, REF = 4.096V, f_{SAMP} = 1Msps, A_{IN} = -1dbFS and C_L = 10pF as a function of LDR irradiation and anneal. The error bars represent the minimum and maximum measured values. The datasheet limit is 20ns maximum.

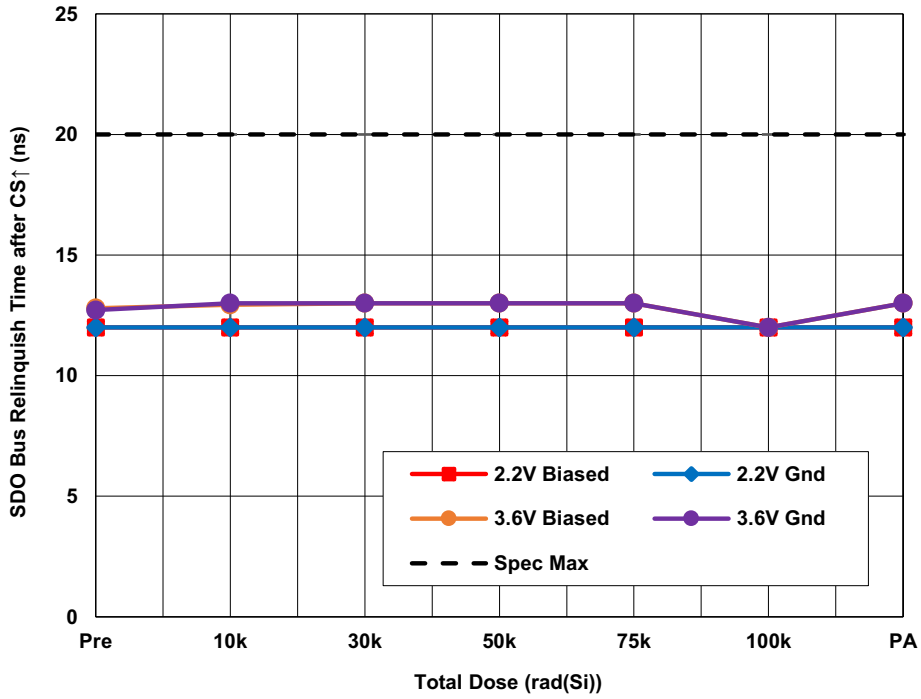


Figure 32. ISL73141SEHMF7 average SDO bus relinquish time after $\overline{CS}$ rising edge ($t_{DCSHSDOZ}$) with AV_{CC} = 4.5V, DV_{CC} = 2.2V and AV_{CC} = 5.5V, DV_{CC} = 3.6V, REF = 4.096V, f_{SAMP} = 1Msps, A_{IN} = -1dbFS, and C_L = 10pF as a function of LDR irradiation and anneal. The error bars represent the minimum and maximum measured values. The datasheet limit is 20ns maximum.

3. Discussion and Conclusion

We report the results of a LDR total dose test of the ISL73141SEHMF7 5V 14-bit SAR ADC. The irradiation of biased and grounded samples to 100krad(Si) was followed by a 168-hour anneal at 100°C under bias. All datasheet parameters passed at all downpoints. No evidence of bias dependence was observed.

4. Appendices

4.1 Reported Parameters

Table 3 lists the key parameters that are considered indicative of part performance. These parameters are plotted in Figure 4 through Figure 32. All limits are taken from the ISL73141SEH datasheet.

Table 3. ISL73141SEHMF7 Key Total Dose Parameters (T_A = 25°C)

Figure	Parameter	Symbol	Conditions	Low Limit	High Limit	Unit
4	Integral Non-Linearity	INL	Measured with full-scale input signal	-1.0	1.0	LSB
5	Differential Non-Linearity	DNL	Measured with full-scale input signal	-0.5	0.5	LSB
6	Zero Scale Error	VOFF	Measured with input grounded	-5	5	LSB
7	Full Scale Error	FSE	Measured with input connected to VREF	-7	7	LSB
8	Signal-to-Noise Ratio	SNR	F_{IN} = 105kHz	80		dB
9	Signal-to-Noise + Distortion Ratio	SINAD	F_{IN} = 105kHz	79		dB
10	Effective Number of Bits	ENOB	F_{IN} = 105kHz	12.5		bits
11	Total Harmonic Distortion	THD	F_{IN} = 105kHz, first five harmonics	85		dB
12	Spurious-Free Dynamic Range	SFDR	F_{IN} = 105kHz, first five harmonics	90		dB
13	Input Leakage Current	I_{AIN}		-1	1	µA
14	REF Input Current	I_{REF}			200	µA
15	Analog Supply Current - Active	I_{AVCC}	Active, f_{SAMP} – 1Msps		14.5	mA
16	Analog Supply Current - Static	I_{STATIC}	$\overline{CS}$ held high		7	mA
17	Analog Supply Current - Sleep	I_{SLAVCC}	$\overline{PD}$ held low		12	µA
18	Digital Supply Current - Active	I_{DVCC}	f_{SCK} = 50MHz, 10pF load		90	µA
19	Digital Supply Current - Static	I_{STDVCC}	$\overline{CS}$ held high		35	µA
20	Digital Supply Current - Sleep	I_{SLDVCC}	$\overline{PD}$ held low		8	µA
21	High Input Level	V_{IH}		0.8*DV_{CC}		V
	Low Input Level	V_{IL}			0.5	V
22	Input Current ($\overline{CS}$, SCK)	I_{IN}	V_{IN} = 0V to DV_{CC}	-1	1	µA
23	High-Level Output	V_{OH}	DV_{CC} – Output, I_O = -500µA	DV_{CC} – 0.2V		V
24	Low-Level Output	V_{OL}	I_O = 500µA		200	mV
25	Hi-Z Output Leakage Current	I_{OZ}	V_{OUT} = 0V to DV_{CC}	-1	1	µA
26	$\overline{PD}$ Input Resistance	R_{INPDL}	Internal pull-up resistance to DV_{CC}	400	600	kΩ
27	Conversion Time	t_{CONV}	BUSY Output High Time		665	ns
28	$\overline{CS}$ Falling Edge to BUSY↑	t_{BUSYLH}	C_L = 10pF		25	ns
29	SDO Data Valid Delay from BUSY↓	$t_{DBUSYLSDOV}$	C_L = 10pF		0	ns
30	SDO Data Valid Hold Time from SCK↑	t_{HSDOV}	C_L = 10pF	8		ns
31	SDO Bus Acquisition Time from $\overline{CS}$↓	$t_{DCSLSDOL}$	C_L = 10pF		20	ns
32	SDO Bus Relinquish Time after $\overline{CS}$↑	$t_{DCSHSDOZ}$	C_L = 10pF		20	ns

5. Revision History

Rev.	Date	Description
1.00	Jan.5.21	Initial release

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