Integrated Device Technology, Inc.
6024 Silver Creek Valley Road, San Jose, CA 95138

PRODUCT/PROCESS CHANGE NOTICE (PCN)

PCN #: **L0808-01** DATE: **9/18/2008**
Product Affected: **IDT74FCT621TSOG**
IDT74FCT621ATSOG

Date Effective: **12/18/2008**

MEANS OF DISTINGUISHING CHANGED DEVICES:
- ☐ Product Mark
- ☐ Back Mark
- ■ Date Code Top mark will show "Z" die rev
- ☐ Other

Contact: Nicole Chang
Title: Quality Engineer
Phone #: (408) 284-4539
Fax #: (408) 284-1450
E-mail: Nicole.Chang@idt.com

Attachment: ■ Yes ☐ No

Samples: Available upon request

DESCRIPTION AND PURPOSE OF CHANGE:
- ☐ Die Technology
- ☐ Wafer Fabrication Process
- ☐ Assembly Process
- ☐ Equipment
- ☐ Material
- ☐ Testing
- ■ Manufacturing Site
- ☐ Data Sheet
- ☐ Other

This PCN is to document wafer fab production from Salinas, California (Fab 2) to Hillsboro, Oregon (Fab 4).

RELIABILITY/QUALIFICATION SUMMARY:

Refer to the attached qualification summary.

CUSTOMER ACKNOWLEDGMENT OF RECEIPT:

IDT records indicate that you require written notification of this change. Please use the acknowledgement below or E-Mail to grant approval or request additional information. If IDT does not receive acknowledgement within 30 days of this notice it will be assumed that this change is acceptable.
IDT reserves the right to ship either version manufactured after the process change effective date until the inventory on the earlier version has been depleted.

Customer: _____ ☐ ***Approval for shipments prior to effective date.***

Name/Date: _____ E-Mail Address: _____

Title: _____ Phone # /Fax #: _____

CUSTOMER COMMENTS: _____

IDT ACKNOWLEDGMENT OF RECEIPT:

RECD. BY: _____ DATE: _____

Integrated Device Technology, Inc.
6024 Silver Creek Valley Road, San Jose, CA 95138

PRODUCT/PROCESS CHANGE NOTICE (PCN)

ATTACHMENT I - PCN #: L0808-01

PCN Type: Fab site change

Data Sheet Change: None

Detail of Change: Transfer existing qualified products from Salinas, California IDT wafer fab facility (Fab 2) to Hillsboro, Oregon IDT wafer fab facility (Fab 4).

Description	Old Fab	New Fab
Die Revision	K	Z
Wafer Fab	Fab 2	Fab 4
Fab Technology	CeMOS 7	CeMOS 8.5
# Poly Layers	1	1
# Metal Layers	2	2
Minimum Gate Length (µm)	0.60	0.37
Die Dimensions (k sq. mils)	2.687	2.943

Sample Availability: Now. Contact sales to request samples.

Integrated Device Technology, Inc.
6024 Silver Creek Valley Road, San Jose, CA 95138

PRODUCT/PROCESS CHANGE NOTICE (PCN)

ATTACHMENT I - PCN #: L0808-01

Qualification Plan #: QLG-03-07R1

Test Vehicle: 74FCT3244Z

Qualification Test Plan and Result:

Test Description	Test Method (Latest specs in effect)	Test Results SS / Rej
High Temperature Operating Life (Dynamic) (+125°C @ 1000 hours or equivalent)	JESD22-A108	116/0
ESD: Human Body Model @ 2000 Volts	MIL-STD 883 Method 3015	3/0
ESD: Charged Device Model @ 1000 Volts	JEDEC 22-101	3/0
Latch-up (+ - I and V stress, + - 100mA Trigger)	JESD78	10/0