Product Change Notice

(PCN tracking number: CST-R2-AD141 Rev.1.0)

July 31, 2018

To:	Valued Renesas Customer
Renesas Product Summary:	Standard SRAM products.
Change Description:	**Generation change of 32Mb and 64Mb Low Power SRAM products, with die shrink from 0.15um to 0.11um process**
Reason for Change:	・To serve the objective of stable supply by improved manufacturing efficiency ・To provide value-added products by significantly reduced power consumption
Identification:	Identifiable by the part name marked on package surface.
Anticipated Impact	Together with the die shrink, successor products incorporate following changes: ・Assembly site (Affected parts: 32Mb/64Mb 52pin-µTSOP, 64Mb 48pin-TSOP(I)) ・Assembly material, inner structure of package (Affected parts: Same as above) ・Moisture sensitivity level (Affected parts: Same as above) ・Package dimensions (Affected part: 64Mb 48ball-FBGA) ・Packing specifications (Affected parts: 32Mb/64Mb 52pin-µTSOP, 64Mb 48ball-FBGA)
Schedule:	32Mb 48pin-TSOP(I), 64Mb 48ball-FBGA: January 2019 Other products except above: March 2019
Supplemental Information:	Refer to pp. 3 ~ pp.8 in this notification and the attachment (Appendix for CST-R2-AD141)
Contact:	Renesas Electronics Corporation Broad-based Solution Business Unit, Industrial Analog & Power Business Division, Analog Products Department, Standard Memory Products Section
Attachments:	Appendix for CST-R2-AD141

In case of any questions, please contact your Renesas sales representative.

Note:

1. Acknowledgement must be received by Renesas within 30 days or Renesas will consider the change as approved.
2. If timely acknowledgement is provided by Customer, then Customer shall have 90 days from the date of acknowledgement of this PCN in which to make any objections to the PCN. If Customer fails to make objections to this PCN within 90 days of the acknowledgement of the PCN then Renesas will consider the PCN changes as approved.
3. If customer cannot accept the PCN then customer must provide Renesas with a last time buy demand and purchase order.

Customer Response (PCN tracking number: CST-R2-AD141)

Please response in the case you could not accept this PCN.
(to be returned by email or mail)

Company: _____

Name & Position: _____

Email: _____

Phone: _____

Date: _____

_____
Signature of customer

The reason why you could not accept this PCN (please comment below);

1. Background of Change

Renesas announces a generation change of 32Mb and 64Mb Low Power SRAM products with die shrink from 0.15um to 0.11um process. The reasons of this change are as follows:

・To serve the objective of stable supply by improved manufacturing efficiency.

・To provide value-added products by significantly reduced power consumption.

Together with the die shrink, successor products incorporate following changes:

・Assembly site (Affected parts: 32Mb/64Mb 52pin-µTSOP, 64Mb 48pin-TSOP(I))

・Assembly material and inner structure of package (Affected parts: Same as above)

・Moisture sensitivity level (Affected parts: Same as above)

・Package dimensions (Affected part: 64Mb 48ball-FBGA)

・Packing specifications (Affected parts: 32Mb/64Mb 52pin-µTSOP, 64Mb 48ball-FBGA)

We greatly appreciate your understanding and cooperation in this matter.

2. Details of Change

2.1 Wafer process

Regarding 32Mb and 64Mb Low Power SRAM products, wafer process will be transferred from 0.15um to 0.11um technology node within existing Saijo factory, Renesas Semiconductor Manufacturing Co., Ltd. This will result in a die shrink. The electrical characteristics such as power consumption will be improved significantly by this change. Refer to the attachment (CST-R2-AD141 appendix) for detail electrical characteristics comparison. Successor products also utilize Renesas patented Advanced Low Power SRAM technology, in which a memory cell features TFT type loads and dedicated capacitors in order to achieve extremely low soft-error rate, as well as the existing products.

2.2 Assembly site, assembly material, inner structure of package and moisture sensitivity level

Regarding the products currently assembled in Renesas Semiconductor (Beijing) Co., Ltd., the assembly site will be transferred to Greatek Electronics Inc. to serve the objective of stable supply.
Along with this site change, assembly material and assembly material, inner structure of package will be changed (ex. Base metal material of lead frame will be changed from 42Alloy to Copper). Accompanied with the copper lead frame, the moisture sensitivity level is changed from MSL2 to MSL3. Refer to p.5 in this notification and the attachment (CST-R2-AD141 appendix) for detail information.

2.3 Package dimensions

Regarding 48ball-FBGA products, package dimensions will be changed to offer smaller package size, while keeping fit of pin configuration. Refer to p.6 in this notification.

2.4 Packing specifications

Regarding 52pin-µTSOP products, the specification of emboss tape will be changed for ease of procurement. Regarding 48ball-FBGA products, both tray and tape & reel specifications will be changed along with package dimensions change. Refer to the attachment (CST-R2-AD141 appendix) for detail information.

Details of change are described according to each assembly site in the following.

(a) Assembly Site：Amkor Technology Malaysia Sdn. Bhd.
Affected part：R1LV3216RSA-5SI（32Mb：48pin-TSOP(I)）

Comparison Table

Item		EOL product	Successor product
Orderable Part Name		R1LV3216RSA-5SI#B1/#S1	RMLV3216AGSA-5S2#AA0/#KA0
Wafer Process	Site Name	Renesas Semiconductor Manufacturing Co., Ltd. Saijo Factory	No Change
	Site Location	Japan	No Change
	Technology Node	0.15µm	0.11µm

Before and after this change,

・Assembly site and material are no change.
・Package form, fit and pin assignment are equivalent.
・DC/AC electrical characteristics are upward compatible.
・Reliability and quality level are equivalent.

(b) Assembly Site：Renesas Semiconductor (Beijing) Co., Ltd.
Affected parts：R1LV3216RSD-5SI（32Mb：52pin-μTSOP）
R1WV6416RSD-5SI（64Mb：52pin-μTSOP）
R1WV6416RSA-5SI（64Mb：48pin-TSOP(I)）

Comparison Table

Item			EOL products	Successor products
Orderable Part Name			R1LV3216RSD-5SI#B0/#S0	RMLV3216AGSD-5S2#AA0/#HA0
			R1WV6416RSD-5SI#B0/#S0	RMWV6416AGSD-5S2#AA0/#HA0
			R1WV6416RSA-5SI#B0/#S0	RMWV6416AGSA-5S2#AA0/#KA0
Wafer Process	Site Name		Renesas Semiconductor Manufacturing Co., Ltd. Saijo Factory	No Change
	Site Location		Japan	No Change
	Technology Node		0.15μm	0.11μm
Assembly	Site Name		Renesas Semiconductor (Beijing) Co., Ltd.	Greatek Electronics Inc.
	Site Location		China	Taiwan
	Mate-rial	Base Metal of Lead Frame	42Alloy	Cu
		Lead Plating	Sn-Cu	Sn
		inner structure of package	Current Specification	New Specification
			Refer to CST-R2-AD141 appendix.	
Moisture Sensitivity Level			MSL2	MSL3
Packing	Tape & Reel	52pin-μTSOP	Current Specification	New Specification
			Refer to CST-R2-AD141 appendix.	
		48pin-TSOP(I)	Current Specification	No Change

Before and after this change,

・Package form, fit and pin assignment are equivalent.
・Base metal of lead frame will be changed from 42 Alloy to Copper, in order to further improve mounting reliability. This will result in change of moisture sensitivity level from MSL2 to MSL3. Along with this site change, inner structure of package will be changed.
・Lead plating will be changed from Sn-Cu to Sn.
・DC/AC electrical characteristics are upward compatible.
・Reliability and quality level are equivalent.
・For 52pin-μTSOP products, the specification of emboss tape will be changed for ease of procurement.
・Refer to the attachment (CST-R2-AD141 appendix) for detail information.

(c) Assembly Site：J-Devices Corporation Kumamoto District
Affected part：R1WV6416RBG-5SI（64Mb：48ball-FBGA）

Comparison Table

Item		EOL product	Successor product
Orderable Part Name		R1WV6416RBG-5SI#B0/#S0	RMWV6416AGBG-5S2#AC0/#KC0
Wafer Process	Site Name	Renesas Semiconductor Manufacturing Co., Ltd. Saijo Factory	No Change
	Site Location	Japan	No Change
	Technology Node	0.15μm	0.11μm
Assembly	Site Name	J-Devices Corporation Kumamoto District	No Change
	Site Location	Japan	No Change
	Package Dimensions	8.5 x 11.0 mm	7.5 x 8.5 mm
Packing	Tray	Current Specification	New Specification
		Refer to CST-R2-AD141 appendix.	
	Tape & Reel	Current Specification	New Specification
		Refer to CST-R2-AD141 appendix.	

Before and after this change,

・Package dimensions will be changed to offer smaller package size, while keeping fit of package.
By this change, the package dimensions of successor product will be same as 0.11um Advanced Low Power SRAM product families.
・DC/AC electrical characteristics are upward compatible.
・Reliability and quality level are equivalent.
・Along with package dimensions change, both tray and tape & reel specifications will be changed.
・Refer to the attachment (CST-R2-AD141 appendix) for detail information.

3. Release Support and Milestones

Commercial Sample	32Mb 48pin-TSOP(I)（RMLV3216AGSA-5S2）， 64Mb 48ball-FBGA（RMWV6416AGBG-5S2）： October, 2018 32Mb 52pin-µTSOP（RMLV3216AGSD-5S2）， 64Mb 52pin-µTSOP（RMWV6416AGSD-5S2）， 64Mb 48pin-TSOP(I)（RMWV6416AGSA-5S2）： December, 2018
Reliability Report	Same as above

4. Identification

It can be identifiable by the part name marked on package surface.

5. Schedule

EOL schedule for current 32Mb/64Mb low power SRAM product families are as follows:

Dec. 2018：EOL announcement
Jun. 2019：Input Last Time Buy amount
Dec. 2019：Last order due date
Dec. 2020：Last shipment

The shipment of successor products will be started as follows:

32Mb 48pin-TSOP(I), 64Mb 48ball-FBGA：January, 2019
32Mb 52pin-µTSOP, 64Mb 52pin-µTSOP, 64Mb 48pin-TSOP(I)：March, 2019

6. Supplemental Information

Please refer to the attachment CST-R2-AD141 appendix.

7. Product list

Density	Package Type	Orderable Part Name	
		EOL product	Successor product
32Mb	48pin-TSOP(I)	R1LV3216RSA-5SI#B1	RMLV3216AGSA-5S2#AA0
		R1LV3216RSA-5SI#S1	RMLV3216AGSA-5S2#KA0
	52pin-µTSOP	R1LV3216RSD-5SI#B0	RMLV3216AGSD-5S2#AA0
		R1LV3216RSD-5SI#S0	RMLV3216AGSD-5S2#HA0
64Mb	48pin-TSOP(I)	R1WV6416RSA-5SI#B0	RMWV6416AGSA-5S2#AA0
		R1WV6416RSA-5SI#S0	RMWV6416AGSA-5S2#KA0
	52pin-µTSOP	R1WV6416RSD-5SI#B0	RMWV6416AGSD-5S2#AA0
		R1WV6416RSD-5SI#S0	RMWV6416AGSD-5S2#HA0
	48ball-FBGA	R1WV6416RBG-5SI#B0	RMWV6416AGBG-5S2#AC0
		R1WV6416RBG-5SI#S0	RMWV6416AGBG-5S2#KC0

To: Valued RENESAS customer,

Renesas Electronics Corporation
Broad-based Solution Business Unit,
Industrial Analog & Power Business Division,
Analog Products Department, Standard Memory Products Section

Rev. 1.00 : July 31, 2018
Rev. 1.01 : April 22, 2019
Rev. 1.02 : June 25, 2019

Appendix for CST-R2-AD141

This appendix states the detailed information of PCN: CST-R2-AD141;
Generation change of 32Mb and 64Mb Low Power SRAM products, with die shrink from 0.15um to 0.11um process.

Contents

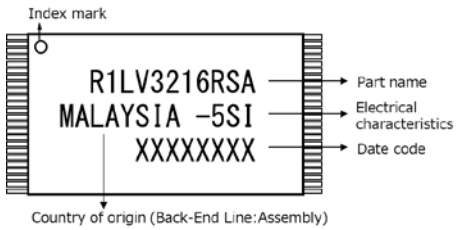
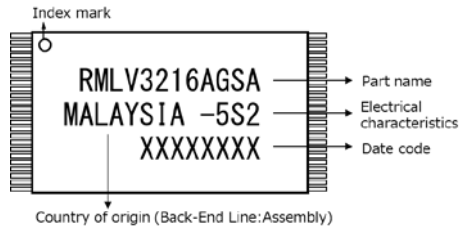
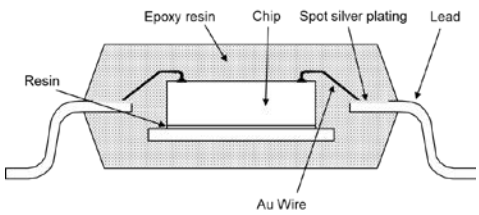
(Note)
From the next page, regarding the assembly site names,
“Amkor Technology Malaysia Sdn. Bhd.” is hereinafter called “Amkor Technology Malaysia” and
“Renesas Semiconductor (Beijing) Co., Ltd.” is hereinafter called “Renesas Semiconductor Beijing”.

1. Product List

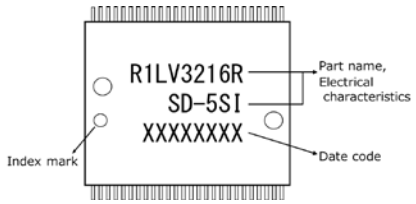
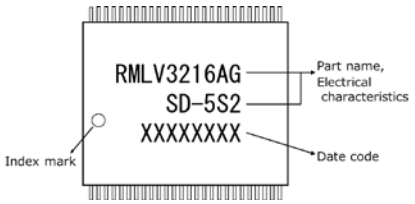
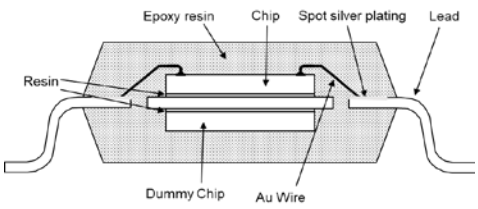
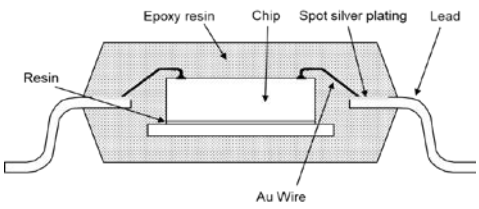
Density	Package Type	Orderable Part Name		Packing Type	Page No. of Comparison Table
		EOL product	**Successor product**		
32Mb	48pin-TSOP(I)	R1LV3216RSA-5SI#B1	RMLV3216AGSA-5S2#AA0	Tray	p.3, pp.8-9
		R1LV3216RSA-5SI#S1	RMLV3216AGSA-5S2#KA0	Tape & Reel	
	52pin-µTSOP	R1LV3216RSD-5SI#B0	RMLV3216AGSD-5S2#AA0	Tray	p.4, pp.8-9
		R1LV3216RSD-5SI#S0	RMLV3216AGSD-5S2#HA0	Tape & Reel	
64Mb	48pin-TSOP(I)	R1WV6416RSA-5SI#B0	RMWV6416AGSA-5S2#AA0	Tray	p.5, pp.10-11
		R1WV6416RSA-5SI#S0	RMWV6416AGSA-5S2#KA0	Tape & Reel	
	52pin-µTSOP	R1WV6416RSD-5SI#B0	RMWV6416AGSD-5S2#AA0	Tray	p.6, pp.10-11
		R1WV6416RSD-5SI#S0	RMWV6416AGSD-5S2#HA0	Tape & Reel	
	48ball-FBGA	R1WV6416RBG-5SI#B0	RMWV6416AGBG-5S2#AC0	Tray	p.7, pp.10-11
		R1WV6416RBG-5SI#S0	RMWV6416AGBG-5S2#KC0	Tape & Reel	

2. Comparison table

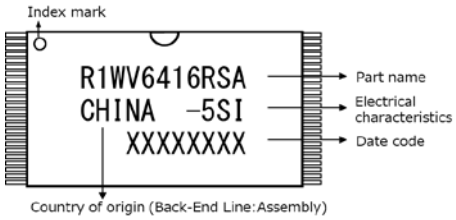
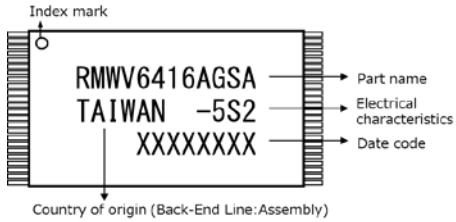
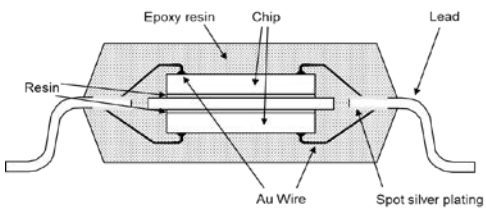
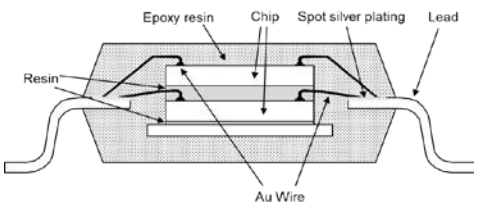
(1) 32Mb 48pin-TSOP(I) Part name： R1LV3216RSA-5SI

Item		EOL product	Successor product
Orderable part name		R1LV3216RSA-5SI#B1 (Tray packing)	RMLV3216AGSA-5S2#AA0 (Tray packing)
		R1LV3216RSA-5SI#S1 (Tape & Reel packing)	RMLV3216AGSA-5S2#KA0 (Tape & Reel packing)
Wafer process line		Renesas Semiconductor Manufacturing Co.,Ltd. Saijo Factry (Japan)	←
Memory cell		TFT Load type Capacitor cell	←
Design rule		0.15um	0.11um
Assembly line		Amkor Technology Malaysia (Malaysia)	←
Country of origin display		MALAYSIA	←
JEITA Package Code		P-TSOP(1)48-12x18.4-0.50	←
Package marking specification			
Assembly Material	Lead frame material	Cu	←
	Lead plating	Sn (pure tin)	←
	Die bonding	Epoxy paste	←
	Wire bonding	Au	←
	Mold	Epoxy resin (Halogen-free)	←
	Inner structure of package		←
Die thickness		Current thickness	←
Final test line		Powertech Technology Inc. (Taiwan)	←
Tray packing	Tray	JEDEC Tray without Renesas Logo (TSOP I package size: 12mm x 18.4mm)	←
	Storage number	96pcs/tray	←
	Laying direction of ICs on a tray	Direction from the top left position to the down side (when the position of chamfer in tray's corner is bottom left.)	←
	Number of trays (Max.)	10 trays + 1 tray (cover)	←
	Inner box size (LxWxH)	351mm x 175mm x 104mm	←
Tape & Reel packing	Embossed tape	Current specification	←
	Storage number	1,000pcs/reel	←
	Inner box size (LxWxH)	362mm x 340mm x 60mm	←
Moisture-proof performance		MSL 3	←
Shipping label		Current specification	No change in format (Changes in orderable part name)

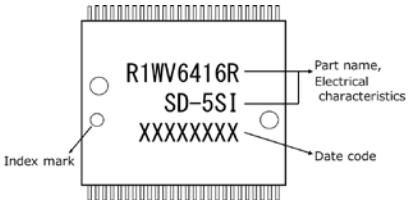
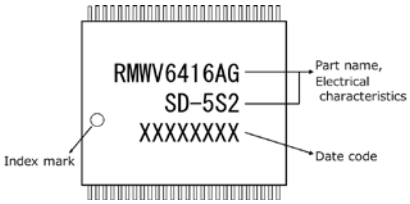
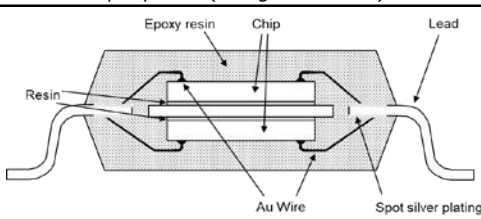
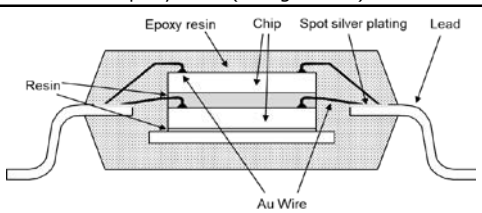
(2) 32Mb 52pin-µTSOP Part name： R1LV3216RSD-5SI

Item		EOL product	Successor product
Orderable part name		R1LV3216RSD-5SI#B0 (Tray packing)	RMLV3216AGSD-5S2#AA0 (Tray packing)
		R1LV3216RSD-5SI#S0 (Tape & Reel packing)	RMLV3216AGSD-5S2#HA0 (Tape & Reel packing)
Wafer process line		Renesas Semiconductor Manufacturing Co.,Ltd. Saijo Factry (Japan)	←
Memory cell		TFT Load type Capacitor cell	←
Design rule		0.15um	0.11um
Assembly line		Renesas Semiconductor Beijing (China)	Greatek Electronics Inc. (Taiwan)
JEITA Package Code		P-TSOP(2)52-8.89x10.79-0.40	←
Package marking specification			
Assembly Material	Lead frame material	42Alloy	Cu
	Lead plating	Sn-Cu	Sn (pure tin)
	Die bonding	Epoxy film	Epoxy paste
	Wire bonding	Au	Au
	Mold	Epoxy resin (Halogen-included)	Epoxy resin (Halogen-free)
	Inner structure of package		
Die thickness		Current thickness	Changed
Final test line		Powertech Technology Inc. (Taiwan)	←
Tray packing	Tray	JEDEC Tray with Renesas Logo (Tray type name : L196-24)	←
	Storage number	230pcs/tray	←
	Laying direction of ICs on a tray	Direction from the top left position to the down side (when the position of chamfer in tray's corner is bottom left.)	←
	Number of trays (Max.)	10 trays + 1 tray (cover)	←
	Inner box size (LxWxH)	351mm x 175mm x 104mm	←
Tape & Reel packing	Embossed tape	Current specification	**Unchanged**
	Storage number	1,000pcs/reel	←
	Inner box size (LxWxH)	289mm x 264mm x 60mm	←
Moisture-proof performance		MSL 2	MSL 3
Shipping label		Current specification	No change in format (Changes in orderable part name, country of origin and MSL display)

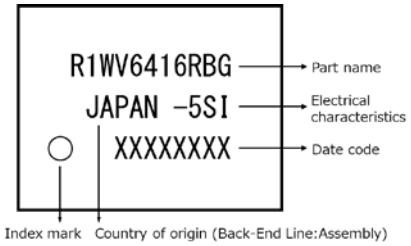
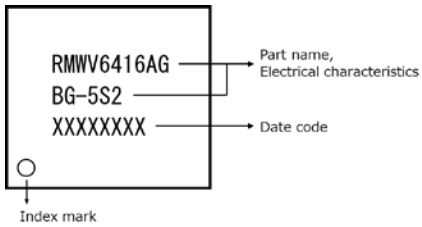
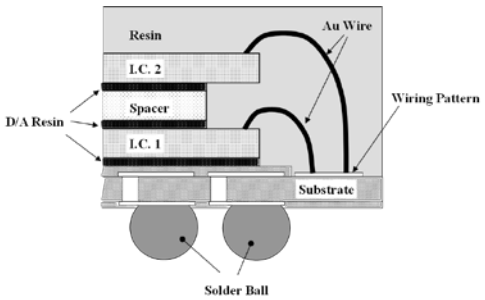
(3) 64Mb 48pin-TSOP(I) Part name： R1WV6416RSA-5SI

Item		EOL product	Successor product
Orderable part name		R1WV6416RSA-5SI#B0 (Tray packing)	RMWV6416AGSA-5S2#AA0 (Tray packing)
		R1WV6416RSA-5SI#S0 (Tape & Reel packing)	RMWV6416AGSA-5S2#KA0 (Tape & Reel packing)
Wafer process line		Renesas Semiconductor Manufacturing Co.,Ltd. Saijo Factry (Japan)	←
Memory cell		TFT Load type Capacitor cell	←
Design rule		0.15um	0.11um
Assembly line		Renesas Semiconductor Beijing (China)	Greatek Electronics Inc. (Taiwan)
Country of origin display		CHINA	TAIWAN
JEITA Package Code		P-TSOP(1)48-12x18.4-0.50	←
Package marking specification			
Assembly Material	Lead frame material	42Alloy	Cu
	Lead plating	Sn-Cu	Sn (pure tin)
	Die bonding	Epoxy film	Epoxy film
	Wire bonding	Au	Au
	Mold	Epoxy resin (Halogen-included)	Epoxy resin (Halogen-free)
	Inner structure of package		
Die thickness		Current thickness	**Changed**
Final test line		Powertech Technology Inc. (Taiwan)	←
Tray packing	Tray	JEDEC Tray without Renesas Logo (TSOP I package size: 12mm x 18.4mm)	←
	Storage number	96pcs/tray	←
	Laying direction of ICs on a tray	Direction from the top left position to the down side (when the position of chamfer in tray's corner is bottom left.)	←
	Number of trays (Max.)	10 trays + 1 tray (cover)	←
	Inner box size (LxWxH)	351mm x 175mm x 104mm	←
Tape & Reel packing	Embossed tape	Current specification	←
	Storage number	1,000pcs/reel	←
	Inner box size (LxWxH)	362mm x 340mm x 60mm	←
Moisture-proof performance		MSL 2	MSL 3
Shipping label		Current specification	No change in format (Changes in orderable part name, country of origin and MSL display)

(4) 64Mb 52pin-μTSOP Part name： R1WV6416RSD-5SI

Item		EOL product	Successor product
Orderable part name		R1WV6416RSD-5SI#B0 (Tray packing)	RMWV6416AGSD-5S2#AA0 (Tray packing)
		R1WV6416RSD-5SI#S0 (Tape & Reel packing)	RMWV6416AGSD-5S2#HA0 (Tape & Reel packing)
Wafer process line		Renesas Semiconductor Manufacturing Co.,Ltd. Saijo Factry (Japan)	←
Memory cell		TFT Load type Capacitor cell	←
Design rule		0.15um	0.11um
Assembly line		Renesas Semiconductor Beijing (China)	Greatek Electronics Inc. (Taiwan)
JEITA Package Code		P-TSOP(2)52-8.89x10.79-0.40	←
Package marking specification			
Assembly Material	Lead frame material	42Alloy	Cu
	Lead plating	Sn-Cu	Sn (pure tin)
	Die bonding	Epoxy film	Epoxy film
	Wire bonding	Au	Au
	Mold	Epoxy resin (Halogen-included)	Epoxy resin (Halogen-free)
	Inner structure of package		
Die thickness		Current thickness	**Changed**
Final test line		Powertech Technology Inc. (Taiwan)	←
Tray packing	Tray	JEDEC Tray with Renesas Logo (Tray type name : L196-24)	←
	Storage number	230pcs/tray	←
	Laying direction of ICs on a tray	Direction from the top left position to the down side (when the position of chamfer in tray's corner is bottom left.)	←
	Number of trays (Max.)	10 trays + 1 tray (cover)	←
	Inner box size (LxWxH)	351mm x 175mm x 104mm	←
Tape & Reel packing	Embossed tape	Current specification	**Unchanged**
	Storage number	1,000pcs/reel	←
	Inner box size (LxWxH)	289mm x 264mm x 60mm	←
Moisture-proof performance		MSL 2	MSL 3
Shipping label		Current specification	No change in format (Changes in orderable part name, country of origin and MSL display)

(5) 64Mb 48ball-FBGA Part name： R1WV6416RBG-5SI

Item		EOL product	Successor product
Orderable part name		R1WV6416RBG-5SI#B0 (Tray packing)	RMWV6416AGBG-5S2#AC0 (Tray packing)
		R1WV6416RBG-5SI#S0 (Tape & Reel packing)	RMWV6416AGBG-5S2#KC0 (Tape & Reel packing)
Wafer process line		Renesas Semiconductor Manufacturing Co.,Ltd. Saijo Factry (Japan)	←
Memory cell		TFT Load type Capacitor cell	←
Design rule		0.15um	0.11um
Assembly line		J-Devices Kumamoto District (Japan)	←
Country of origin display		JAPAN	No display
JEITA Package Code		P-TFBGA48-8.5x11-0.75	P-TFBGA48-7.5x8.5-0.75
Package Dimensions		8.5 x 11.0mm	7.5 x 8.5mm
Ball Pitch		0.75mm	←
Package marking specification			
Assembly Material	Substrate material	Glass epoxy	←
	Solder ball	Sn-Ag-Cu	←
	Die bonding	Epoxy film	←
	Wire bonding	Au	←
	Mold	Epoxy resin (Halogen-included)	Epoxy resin (Halogen-free)
	Inner structure of package		←
Die thickness		Current thickness	←
Final test line		Powertech Technology Inc. (Taiwan)	←
Tray packing	Tray	JEDEC Tray with Renesas Logo (Tray type name : L196-121)	JEDEC Tray with Renesas Logo (Tray type name : L196-45) (Same as other 7.5x8.5mm 48ball FBGA Type)
	Storage number	242pcs/tray	253pcs/tray
	Laying direction of ICs on a tray	Direction from the top left position to the down side (when the position of chamfer in tray's corner is bottom left.)	←
	Number of trays (Max.)	10 trays + 1 tray (cover)	←
	Inner box size (LxWxH)	351mm x 175mm x 104mm	←
Tape & Reel packing	Embossed tape	Current specification	New specification (Same as other 7.5x8.5mm 48ball FBGA Type)
	Storage number	1,000pcs/reel	←
	Inner box size (LxWxH)	289mm x 264mm x 60mm	←
Moisture-proof performance		MSL 3	←
Shipping label		Current specification	No change in format (Changes in orderable part name)

- Note: Regarding the details of change in the tray, please see p.12.

  Regarding the details of change in embossed tape, please see p.13.

3. Electrical characteristics (DC/AC)

(1)–a. Electrical characteristics (DC) : 32Mb

Products

Item	EOL product	Successor product
Orderable part name	R1LV3216RSA-5SI#B1	RMLV3216AGSA-5S2#AA0
	R1LV3216RSA-5SI#S1	RMLV3216AGSA-5S2#KA0
	R1LV3216RSD-5SI#B0	RMLV3216AGSD-5S2#AA0
	R1LV3216RSD-5SI#S0	RMLV3216AGSD-5S2#HA0

DC conditions

Item	Symbol	EOL product	Symbol	Successor product
Supply voltage	Vcc	2.7V～3.6V	Vcc	←
Operating temperature range	Ta	-40℃～85℃	Ta	←
Input high voltage	VIH	2.4V(min.) / Vcc+0.2V(max.)	VIH	2.2V(min.) / Vcc+0.3V(max.)
Input low voltage	VIL	-0.2V(min.) / 0.4V(max.)	VIL	-0.3V(min.) / 0.6V(max.)

DC characteristics

Item	Symbol	EOL product		Symbol	Successor product	
Operating Current	Icc1(TTL, Min.Cycle)	55mA(max.) / 40mA(typ.)		Icc1(TTL, Min.Cycle)	35mA(max.) / 27mA(typ.)	
	Icc2(MOS, Cycle=1us)	8mA(max.) / 3mA(typ.)		Icc2(MOS, Cycle=1us)	4mA(max.) / 2mA(typ.)	
Standby current	ISB(TTL)	0.3mA(max.) / 0.1mA(typ.)		ISB(TTL)	←	
	ISB1(MOS)	～25℃	12uA(max.) / 4uA(typ.)	ISB1(MOS)	～25℃	4uA(max.) / 0.6uA(typ.)
		～40℃	24uA(max.) / 7uA(typ.)		～40℃	6uA(max.) / 1uA(typ.)
		～70℃	50uA(max.)		～70℃	17uA(max.) / 4uA(typ.)
		～85℃	80uA(max.)		～85℃	24uA(max.) / 8uA(typ.)
Output high voltage	VOH	IOH=-1mA	–	VOH	IOH=-1mA	2.4V(min.)
		IOH=-0.5mA	2.4V(min.)		IOH=-0.5mA	–
Output low voltage	VOL	IOL=2mA	0.4V(max.)	VOL	IOL=2mA	←

Capacitance

Item	Symbol	EOL product	Symbol	Successor product
Input capacitance	C in	10pF(max.)	C in	←
Input/Output capacitance	C I/O	10pF(max.)	C I/O	←

Data retention characteristics

Item	Symbol	EOL product		Symbol	Successor product	
Vcc for data retention	VDR	2.0V(min.)		VDR	1.5V(min.)	
Data retention current	IccDR	～25℃	12uA(max.) / 4uA(typ.)	IccDR	～25℃	4uA(max.) / 0.6uA(typ.)
		～40℃	24uA(max.) / 7uA(typ.)		～40℃	6uA(max.) / 1uA(typ.)
		～70℃	50uA(max.)		～70℃	17uA(max.) / 4uA(typ.)
		～85℃	80uA(max.)		～85℃	24uA(max.) / 8uA(typ.)
Chip deselect time to data retention	tCDR	0ns(min.)		tCDR	←	
Operation recovery time	tR	5ms(min.)		tR	←	

(1)–b. Electrical characteristics (AC) : 32Mb

Products

Item	**EOL product**	**Successor product**
Orderable part name	R1LV3216RSA-5SI#B1	RMLV3216AGSA-5S2#AA0
	R1LV3216RSA-5SI#S1	RMLV3216AGSA-5S2#KA0
	R1LV3216RSD-5SI#B0	RMLV3216AGSD-5S2#AA0
	R1LV3216RSD-5SI#S0	RMLV3216AGSD-5S2#HA0

AC characteristics
Read Cycle

Item	Symbol	**EOL product**	Symbol	**Successor product**
Read cycle time	tRC	55ns(min.)	tRC	←
Address access time	tAA	55ns(max.)	tAA	←
Chip select access time	tACS1 / tACS2	55ns(max.)	tACS1 / tACS2	45ns(max.)
Output enable to output valid	tOE	25ns(max.)	tOE	22ns(max.)
Output hold from address change	tOH	10ns(min.)	tOH	←
LB#,UB# access time	tBA	55ns(max.)	tBA	45ns(max.)
Chip select to output in low-Z	tCLZ1 / tCLZ2	10ns(min.)	tCLZ1 / tCLZ2	←
LB#,UB# enable to low-Z	tBLZ	5ns(min.)	tBLZ	←
Output enable to output in low-Z	tOLZ	5ns(min.)	tOLZ	←
Chip deselect to output in high-Z	tCHZ1 / tCHZ2	0ns(min.) / 20ns(max.)	tCHZ1 / tCHZ2	0ns(min.) / 18ns(max.)
LB#,UB# disable to high-Z	tBHZ	0ns(min.) / 20ns(max.)	tBHZ	0ns(min.) / 18ns(max.)
Output disable to output in high-Z	tOHZ	0ns(min.) / 20ns(max.)	tOHZ	0ns(min.) / 18ns(max.)

Write Cycle

Item	Symbol	**EOL product**	Symbol	**Successor product**
Write cycle time	tWC	55ns(min.)	tWC	←
Address valid to end of write	tAW	50ns(min.)	tAW	35ns(min.)
Chip select to end of write	tCW	50ns(min.)	tCW	35ns(min.)
Write pulse width	tWP	40ns(min.)	tWP	35ns(min.)
LB#,UB# valid to end of write	tBW	50ns(min.)	tBW	35ns(min.)
Address setup time	tAS	0ns(min.)	tAS	←
Write recovery time	tWR	0ns(min.)	tWR	←
Data to write time overlap	tDW	25ns(min.)	tDW	←
Data hold from write time	tDH	0ns(min.)	tDH	←
Output enable from end of write	tOW	5ns(min.)	tOW	←
Output disable to output in high-Z	tOHZ	0ns(min.) / 20ns(max.)	tOHZ	0ns(min.) / 18ns(max.)
Write to output in high-Z	tWHZ	0ns(min.) / 20ns(max.)	tWHZ	0ns(min.) / 18ns(max.)

(2)–a. Electrical characteristics (DC) : 64Mb

Products

Item	EOL product	Successor product
Orderable part name	R1WV6416RSA-5SI#B0	RMWV6416AGSA-5S2#AA0
	R1WV6416RSA-5SI#S0	RMWV6416AGSA-5S2#KA0
	R1WV6416RSD-5SI#B0	RMWV6416AGSD-5S2#AA0
	R1WV6416RSD-5SI#S0	RMWV6416AGSD-5S2#HA0
	R1WV6416RBG-5SI#B0	RMWV6416AGBG-5S2#AC0
	R1WV6416RBG-5SI#S0	RMWV6416AGBG-5S2#KC0

DC conditions

Item	Symbol	EOL product	Symbol	Successor product
Supply voltage	Vcc	2.7V～3.6V	Vcc	←
Operating temperature range	Ta	-40℃～85℃	Ta	←
Input high voltage	VIH	2.4V(min.) / Vcc+0.2V(max.)	VIH	2.2V(min.) / Vcc+0.3V(max.)
Input low voltage	VIL	-0.2V(min.) / 0.4V(max.)	VIL	-0.3V(min.) / 0.6V(max.)

DC characteristics

Item	Symbol	EOL product		Symbol	Successor product	
Operating Current	Icc1(TTL, Min.Cycle)	60mA(max.) / 45mA(typ.)		Icc1(TTL, Min.Cycle)	38mA(max.) / 29mA(typ.)	
	Icc2(MOS, Cycle=1us)	10mA(max.) / 5mA(typ.)		Icc2(MOS, Cycle=1us)	5mA(max.) / 2.5mA(typ.)	
Standby current	ISB(TTL)	0.3mA(max.) / 0.1mA(typ.)		ISB(TTL)	←	
	ISB1(MOS)	～25℃	24uA(max.) / 8uA(typ.)	ISB1(MOS)	～25℃	8uA(max.) / 1.2uA(typ.)
		～40℃	48uA(max.) / 14uA(typ.)		～40℃	12uA(max.) / 2uA(typ.)
		～70℃	100uA(max.)		～70℃	34uA(max.)
		～85℃	160uA(max.)		～85℃	46uA(max.)
Output high voltage	VOH	IOH=-1mA	–	VOH	IOH=-1mA	2.4V(min.)
		IOH=-0.5mA	2.4V(min.)		IOH=-0.5mA	–
Output low voltage	VOL	IOL=2mA	0.4V(max.)	VOL	IOL=2mA	←

Capacitance

Item	Symbol	EOL product	Symbol	Successor product
Input capacitance	C in	20pF(max.)	C in	←
Input/Output capacitance	C I/O	20pF(max.)	C I/O	←

Data retention characteristics

Item	Symbol	EOL product		Symbol	Successor product	
Vcc for data retention	VDR	2.0V(min.)		VDR	1.5V(min.)	
Data retention current	IccDR	～25℃	24uA(max.) / 8uA(typ.)	IccDR	～25℃	8uA(max.) / 1.2uA(typ.)
		～40℃	48uA(max.) / 14uA(typ.)		～40℃	12uA(max.) / 2uA(typ.)
		～70℃	100uA(max.)		～70℃	34uA(max.)
		～85℃	160uA(max.)		～85℃	46uA(max.)
Chip deselect time to data retention	tCDR	0ns(min.)		tCDR	←	
Operation recovery time	tR	5ms(min.)		tR	←	

(2)–b. Electrical characteristics (AC) : 64Mb

Products

Item	**EOL product**	**Successor product**
Orderable part name	R1WV6416RSA-5SI#B0	RMWV6416AGSA-5S2#AA0
	R1WV6416RSA-5SI#S0	RMWV6416AGSA-5S2#KA0
	R1WV6416RSD-5SI#B0	RMWV6416AGSD-5S2#AA0
	R1WV6416RSD-5SI#S0	RMWV6416AGSD-5S2#HA0
	R1WV6416RBG-5SI#B0	RMWV6416AGBG-5S2#AC0
	R1WV6416RBG-5SI#S0	RMWV6416AGBG-5S2#KC0

AC characteristics
Read Cycle

Item	Symbol	**EOL product**	Symbol	**Successor product**
Read cycle time	tRC	55ns(min.)	tRC	←
Address access time	tAA	55ns(max.)	tAA	←
Chip select access time	tACS1 / tACS2	55ns(max.)	tACS1 / tACS2	←
Output enable to output valid	tOE	25ns(max.)	tOE	←
Output hold from address change	tOH	10ns(min.)	tOH	←
LB#,UB# access time	tBA	55ns(max.)	tBA	←
Chip select to output in low-Z	tCLZ1 / tCLZ2	10ns(min.)	tCLZ1 / tCLZ2	←
LB#,UB# enable to low-Z	tBLZ	5ns(min.)	tBLZ	←
Output enable to output in low-Z	tOLZ	5ns(min.)	tOLZ	←
Chip deselect to output in high-Z	tCHZ1 / tCHZ2	0ns(min.) / 20ns(max.)	tCHZ1 / tCHZ2	←
LB#,UB# disable to high-Z	tBHZ	0ns(min.) / 20ns(max.)	tBHZ	←
Output disable to output in high-Z	tOHZ	0ns(min.) / 20ns(max.)	tOHZ	←

Write Cycle

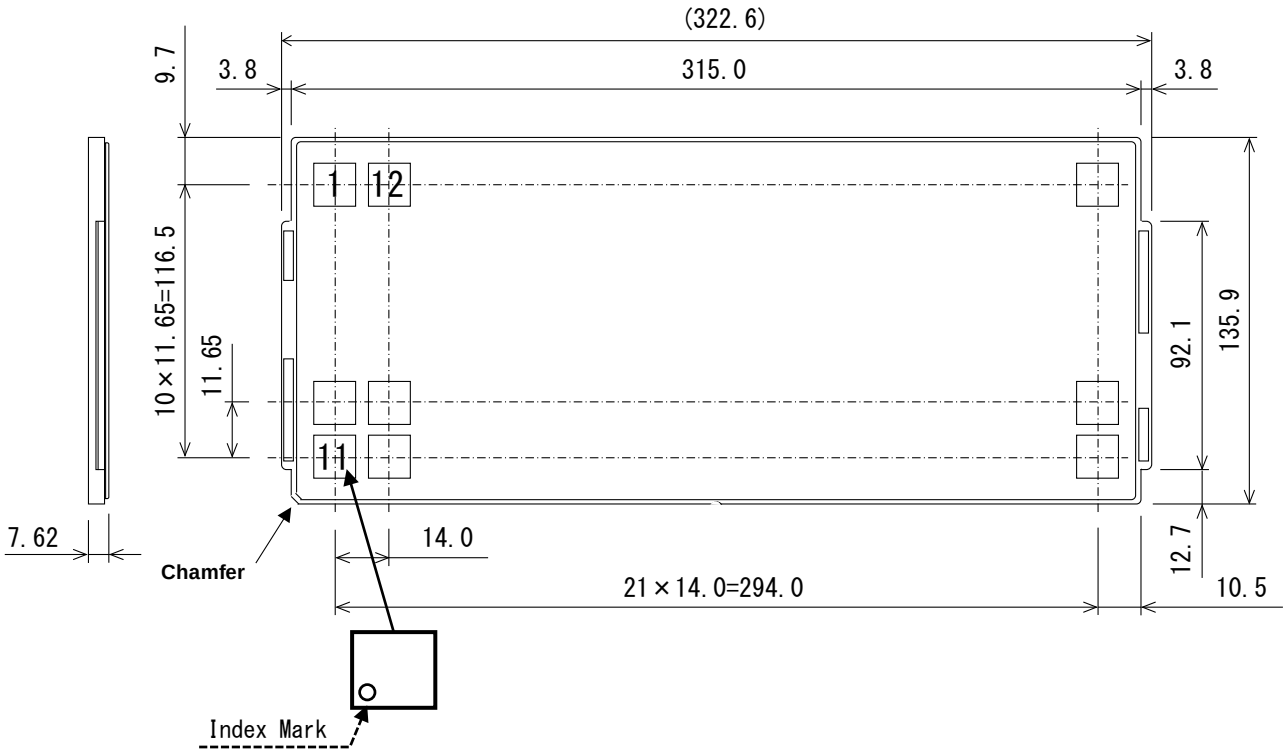
Item	Symbol	**EOL product**	Symbol	**Successor product**
Write cycle time	tWC	55ns(min.)	tWC	←
Address valid to end of write	tAW	50ns(min.)	tAW	45ns(min.)
Chip select to end of write	tCW	50ns(min.)	tCW	45ns(min.)
Write pulse width	tWP	40ns(min.)	tWP	←
LB#,UB# valid to end of write	tBW	50ns(min.)	tBW	45ns(min.)
Address setup time	tAS	0ns(min.)	tAS	←
Write recovery time	tWR	0ns(min.)	tWR	←
Data to write time overlap	tDW	25ns(min.)	tDW	←
Data hold from write time	tDH	0ns(min.)	tDH	←
Output enable from end of write	tOW	5ns(min.)	tOW	←
Output disable to output in high-Z	tOHZ	0ns(min.) / 20ns(max.)	tOHZ	←
Write to output in high-Z	tWHZ	0ns(min.) / 20ns(max.)	tWHZ	←

4. Packing specification

(1) Change the specification of the 48ball-FBGA Tray

- Because of changing package outline size, the tray pocket size is to be changed (see below).
- No change in Laying direction of ICs on a tray.

Pre Change (Tray type name : L196-121, Storage number : 242pcs/tray)



Post Change (Tray type name : L196-45, Storage number : 253pcs/tray)

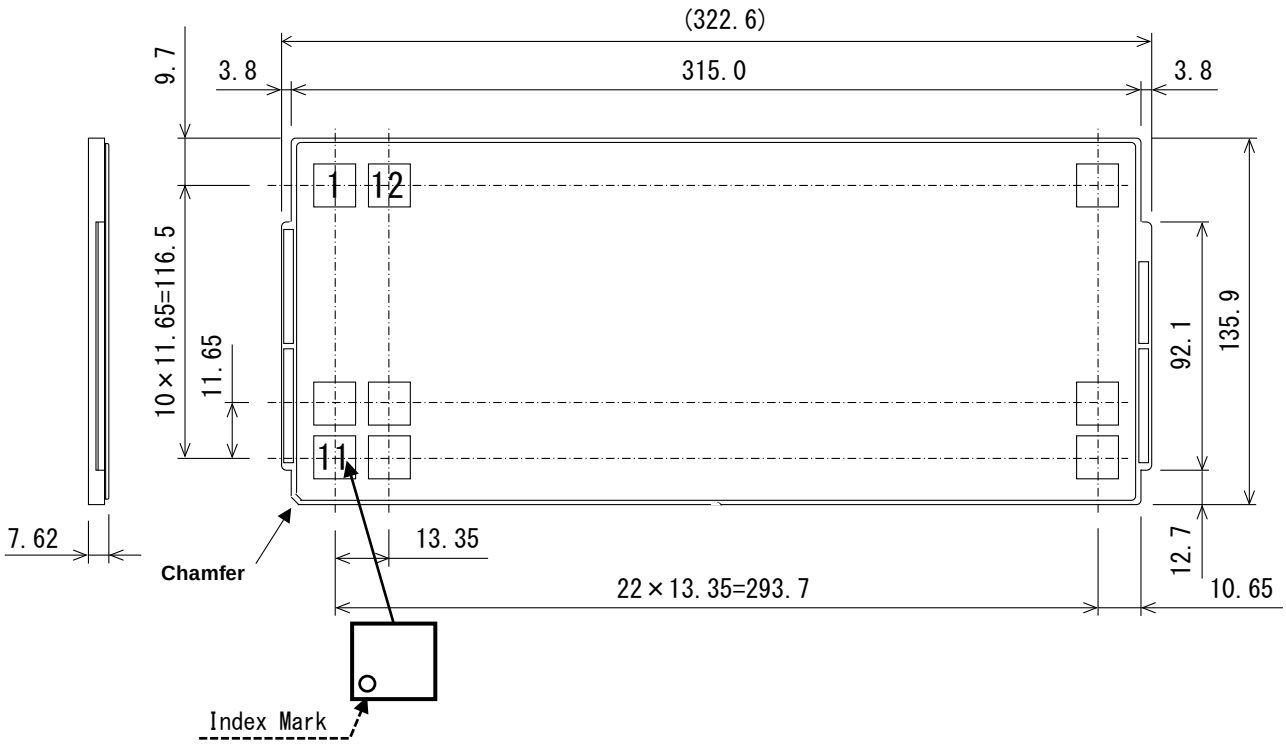
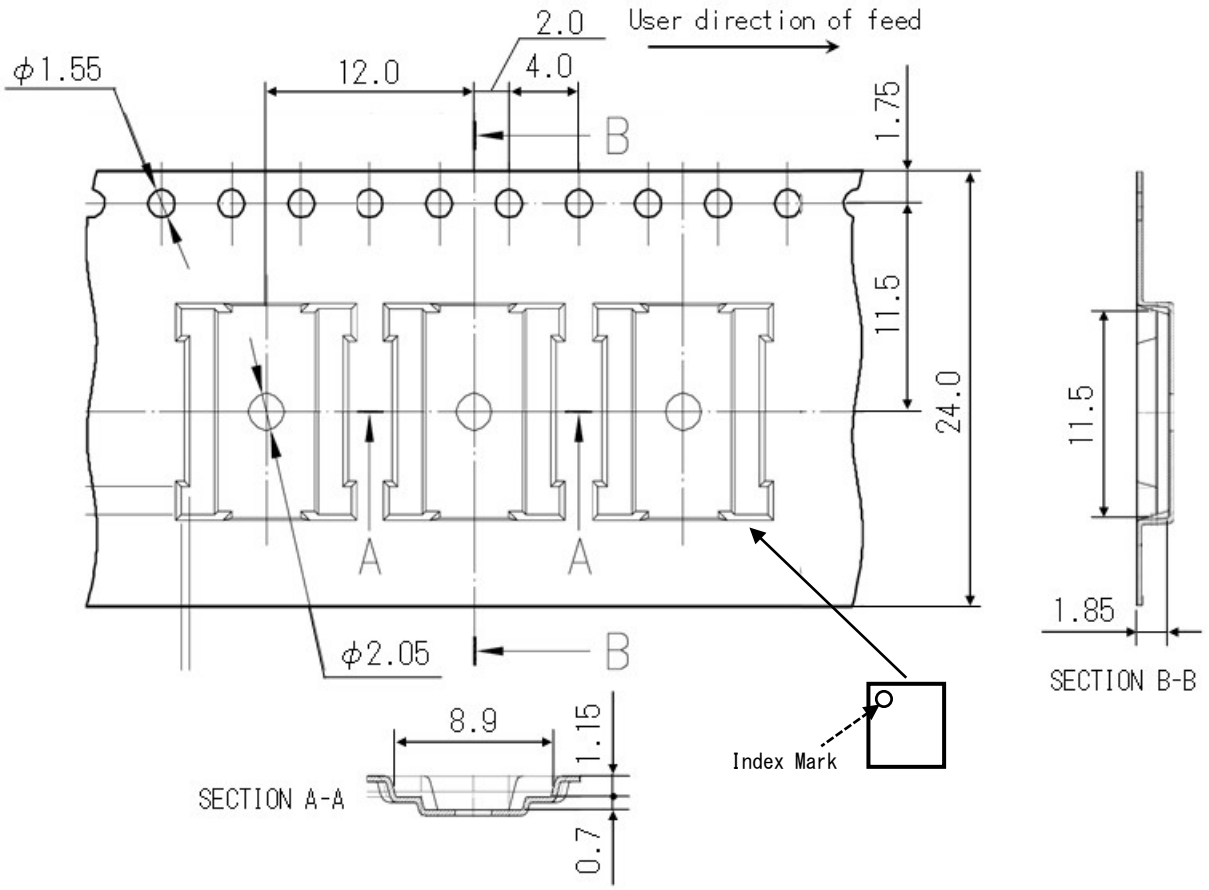


Figure: Dimension of 48ball-FBGA tray and the method to pack ICs (Unit: mm)

(2) Change the specification of the 48ball-FBGA Tape & Reel

- Because of changing package outline size, the package pocket form, size, seat position and embossed tape width are to be changed (see below).
- No change in pocket pitch and reel diameter.

Pre Change (Embossed tape type name : TE2412-48FHK)



Post Change (Embossed tape type name : MTE1612H-48F7Q)

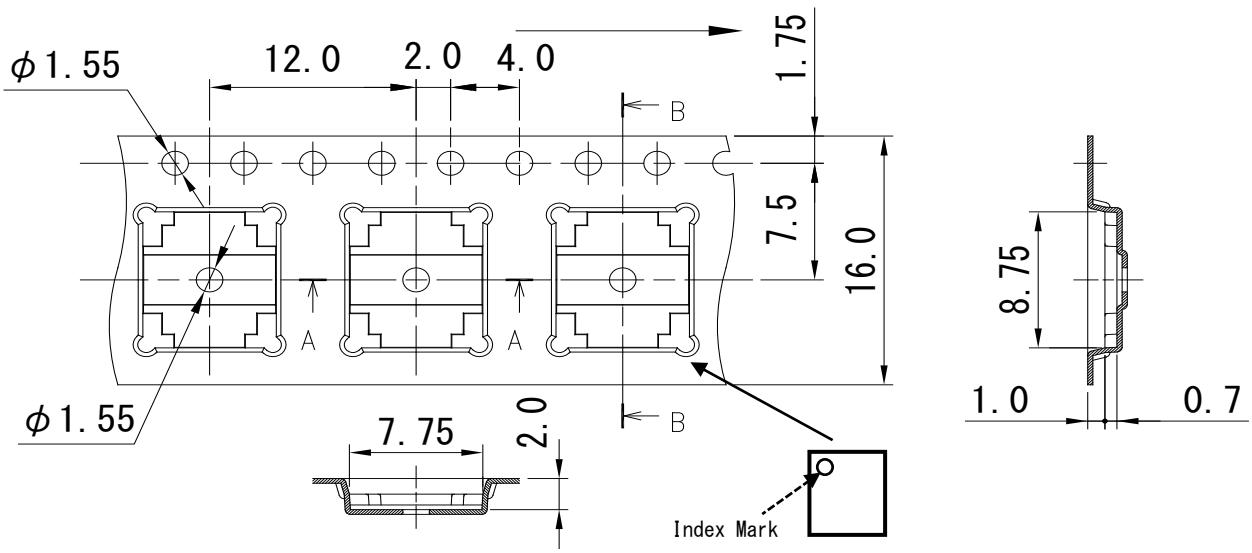


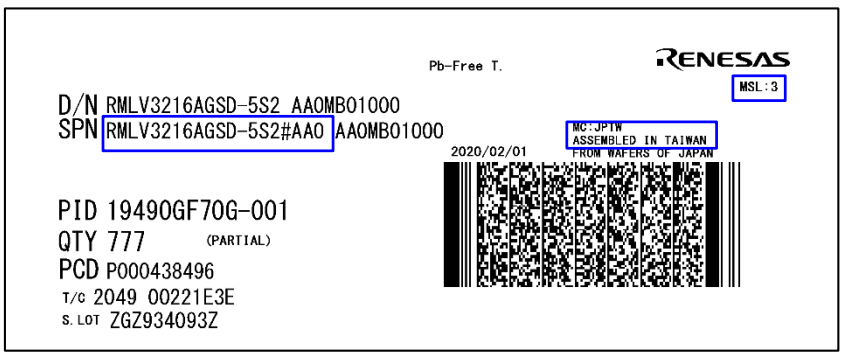
Figure. 48ball-FBGA Embossed Carrier tape Dimensions (Unit: mm)

5. Shipping label

- Label format itself is not changed.
- Written specification: “Orderable part name” is changed.
  Regarding R1LV3216RSD-5SI, R1WV6416RSD-5SI, R1WV6416RSA-5SI,
  “the country of origin” and MSL are changed.
  See below for example.

Pre Change

Post Change



Revision history	Appendix for CST-R2-AD141

Rev.	Date	Outline of changed content
1.00	2018/8/1	Initial issue
1.01	2019/4/22	p.4, p.6： ・Revised the embossed carrier tape from “New specification” to “Unchanged” ・Deleted the footnote: “Note: Regarding the details of change in the embossed tape, please see p.12.” Deleted the whole contents of the page 12 in Rev.1.00. (Change the specification of the 52pin-μTSOP Tape & Reel)
1.02	2019/6/25	p.5, p.6： ・Revised the Die thickness from “Unchanged” to “Changed”

