

Timing Fabric for Next Generation Communications Equipment

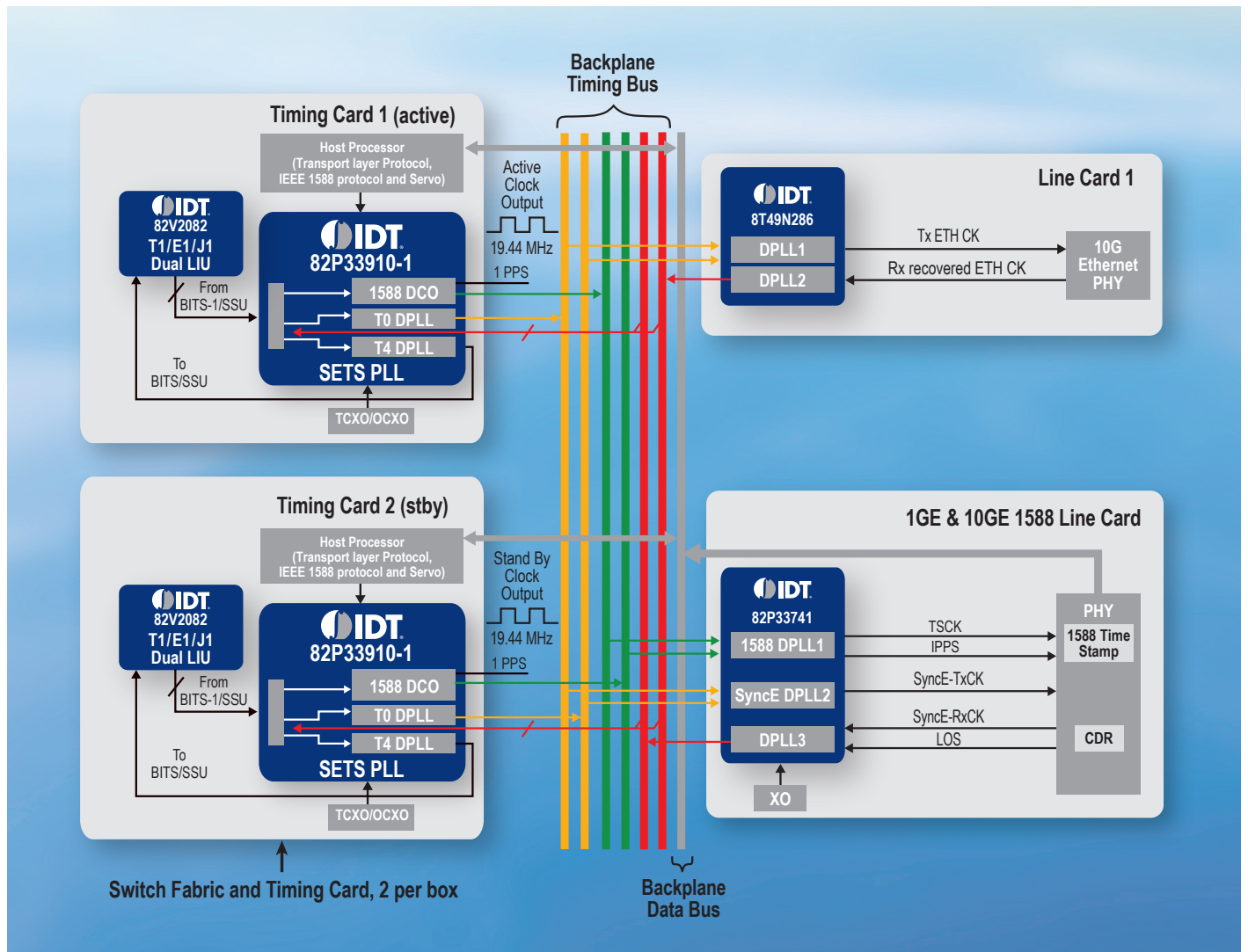
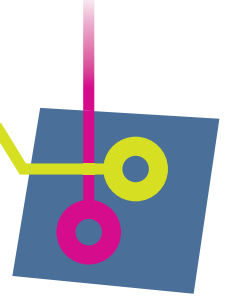


Figure 1 - Timing Fabric Architecture - Timing Cards and Line Cards

IDT TIMING CARD SOLUTIONS

IDT SMU PLL Features

- Up to 14 total inputs and 15 outputs
- IEEE 1588 Support (external DCO* control)
- Three independent DPLL + APPLL paths
 - T0 path for node frequency synchronization
 - 1588 path for node time synchronization
 - T4 path for equipment synchronization
- Frequency range: 1 Hz to 650 MHz
- Ethernet and SONET/SDH clocks
- Phase noise <1ps RMS (12 kHz to 20 MHz)

ARCHITECTURE OVERVIEW

Communication equipment requires synchronization to transport multiple services (voice, data and video) over Carrier networks. The timing fabric, as illustrated in *Figures 1* and *2*, enables equipment such as routers, multi-service switching platforms, PONs (Passive Optical Network) and DSLAMs (Digital Subscriber Line Access Multiplexer), to meet the stringent synchronization requirements of communication networks.

The architecture in *Figure 1* segments the timing fabric into two major elements: timing cards and line cards. On the timing cards, the Synchronization Management Unit (SMU) PLLs are primarily responsible for compliance with synchronization standards. The T1/E1 LIUs receive external BITS/SSU references for the T0 DPLLs which generate standards compliant synchronous clocks and distribute them to the backplane for the line cards. The external 1 PPS receive external PRTC references for the 1588 DPLLs which generate standards-compliant, time-synchronous clocks and distribute them to the backplane for the line cards.



Timing Fabric for Next Generation Communications Equipment

IDT T1/E1 LIU Features

- Dual and single channel LIU devices available
- Supports hitless protection switching for 1+1 protection without external relays
- Receiver sensitivity exceeds -36db @ 772kHz and -43dB @ 1024kHz
- Programmable T1/E1/J1 switchability allows one bill of material for any line type
- Loss of Signal (LOS) and Alarm Indication Signal (AIS) detection

IDT LINE CARD SOLUTIONS

Line Card PLL Features

- Dual PLL chip: one can be used for the transmit path and the other for the receive path
- Programmable DPLL bandwidth
- Supports automatic hitless reference switching
- Provides a 1PPS sync input signal and a 1PPS sync output signal
- Generates output clocks for synchronous Ethernet, SONET, SDH, GPS, 3G and GSM components

Jitter Attenuator Features

- FemtoClock® product is a frequency multiplier and jitter attenuator component that generates low jitter Ethernet clocks and can easily meet 10 gigabit Ethernet requirements.
- Optimized for Ethernet jitter attenuation
- Attenuates the phase jitter of the input clock by using a low-cost pullable fundamental mode VCXO crystal

Recovered clocks from the Line Card PHYs are used as references by the T4 DPLLs which rate convert them for the T1/E1 LIU transmitters that provide line references to the external BITS/SSU.

On the line cards, DPLLs select a backplane reference from one of the timing cards; the reference is then rate converted and jitter attenuated to meet the needs of the specific PHYs used on these cards. Depending on the number of PHY reference clocks required on each line card a discrete fanout buffer may be needed. Recovered clocks from line card PHYs are rate converted to a backplane frequency (8kHz, 19.44MHz, or 25MHz) and sent to the backplane for the T0/T4 DPLLs on the timing cards.

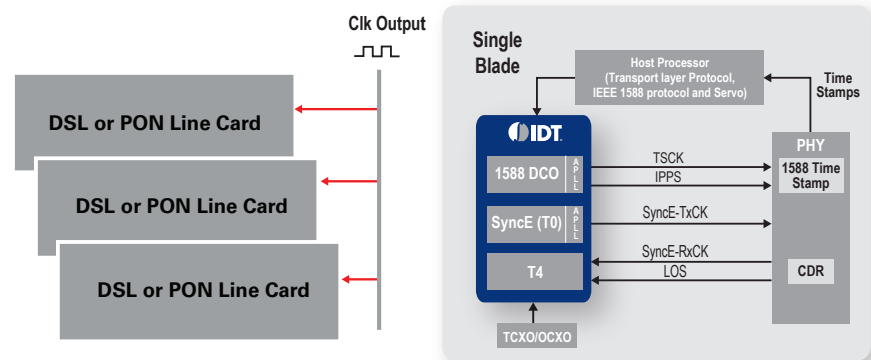


Figure 2 - Timing Fabric Architecture (Up-link Transmission Card)

The architecture in Figure 2 has the timing fabric in one up-link transmission card. Both the traditional timing card and line card functionality are combined into one card. The recovered clock from the PHY is sent to the SMU PLL for filtering, frequency translation and generation of backplane clocks. The clock generated by the SMU PLL is filtered with an integrated jitter attenuator and used as a transmitting clock for the PHY + Framer. The host processor processes the IEEE 1588 packets and controls the 1588 DCO to generate standards-compliant, time-synchronous clocks and 1 PPS.

As the only supplier with all of the different timing components to provide complete solutions, IDT is uniquely positioned to meet the needs of communication equipment suppliers and offer compelling solutions for all timing fabric architectures.

- Standards Compliant SMU PLLs [T-BC, T-TSC, EEC, PEC-S-F*, SEC, ST3/SMC (ITU-T G.8273.2, G.8262, G.8263, G.813 and Telcordia GR-253-CORE, GR-1244-CORE)]
- Standards Compliant PTP stack and profiles (IEEE 1588-2008, ITU-T G.8265.1, G.8275.1)
- T1/E1 Dual LIUs
- Line card PLLs
- Jitter attenuators and frequency translators
- Differential fanout buffers with low additive RMS phase jitter
- Backplane interface / translators (as needed)

* With supporting 1588 filtering algorithm software



Timing Fabric for Next Generation Communications Equipment

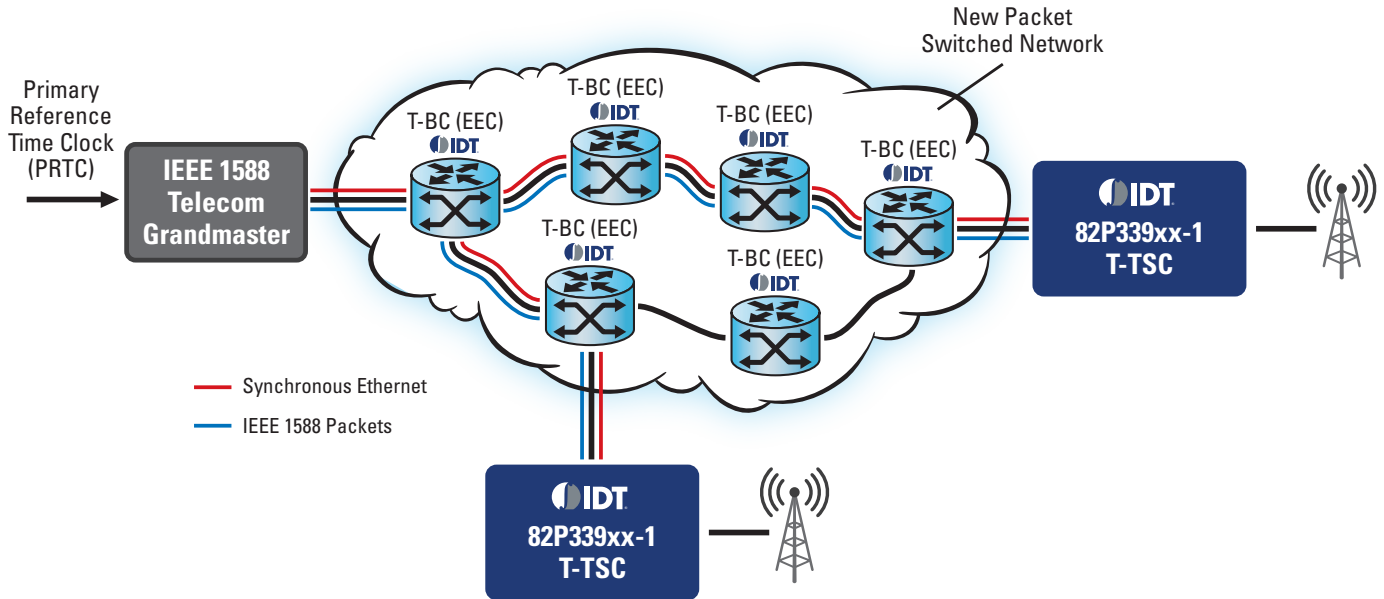


Figure 3 - Distributed PRTC Synchronization Network

IDT SOFTWARE SOLUTIONS

PTP Stack Features

- Industry proven compliant stack
 - Ordinary clock
 - Boundary clock
 - Transparent clock
 - One-step/two-step clock
 - One-way/two-way mode
 - Best master clock algorithms
 - Multicast
 - Unicast with negotiation
 - Annex D,E,F transports (IPv4, IPv6, 802.3)
- Platform & OS independent ANSI-C code
- Hardware abstraction layer separates protocol stack from target system

1588 Profiles

- IEEE 1588 Default Profiles (Annex J)
- ITU-T Telecom Profiles (G.8265.1, G.8275.1)

Packet Clock Features

- Local clock state machine, managing clock acquisition, lock & holdover modes of operation
- Independent reference trackers to support monitoring of multiple master clocks
- Support for hitless & phase limiting reference switching, using revertive or non-revertive priority selection
- Advance PDV filtering techniques for both frequency & phase/time clock recovery over 1588 unaware networks

IEEE 1588 PRECISION TIME PROTOCOL & PROFILES

With the transition from time-division multiplexing (TDM) to packet switched networks, the need to transport time/synchronization over a packet network became a necessity. IEEE 1588 (IEEE Std 1588™-2008 [1]), also known as Precision Time Protocol (PTP), is becoming the main protocol to transport precision time/phase/frequency over packet networks.

The 82P339xx-1 products are composed of IEEE 1588-compliant software and IDT Synchronization Management Unit (SMU) chips that deliver a complete telecom network synchronization solution for IEEE 1588 and synchronous Ethernet. The hardware/software solution includes an IEEE 1588 protocol stack, clock recovery servos for frequency and phase/time, and clock synthesis hardware with physical layer frequency support.

The 82P339xx-1 SMUs automatically filter IEEE 1588 phase/time information and combine it with physical layer frequency information in accordance with ITU-T G.8273.2 to generate accurate, stable and low-jitter clocks. The phase/time and frequency filters are implemented in hardware to ensure deterministic filter bandwidths, eliminating the need for additional software processing.

In addition to the compliant stack, the hardware/software solution also includes all of the configuration options required for the ITU-T Telecom Profiles. For additional information on the ITU-T Telecom Profiles, please refer to IDT's whitepaper: www.idt.com/document/whp/itu-t-profiles-ieee-1588.



Timing Fabric for Next Generation Communications Equipment

Timing Card/Up-link Transmission Card Components										
Part Number	Product Type	Clock Support	Channels (#)	Inputs (#)	Diff. Inputs	Input Freq Range Type	Output Freq Range Type	Phase Jitter Typ RMS (ps)	Outputs (#)	Diff. Outputs
82P33810	Synchronization Management Unit (SMU) for IEEE 1588 and Synchronous Ethernet	G.813 (SEC), G.8262 (EEC), G.8273.2 (T-BC/T-TSC), GR-253-CORE (ST3/SMC), GR-1244-CORE (ST3/ST4/ST4E)	3	14	6	1 Hz to 650 MHz, Composite Clock (G.703 64kbps)	1 Hz to 650 MHz, Composite Clock (G.703 64kbps)	0.56	13	4
82P33814	Synchronization Management Unit (SMU) for IEEE 1588 and Synchronous Ethernet	G.813 (SEC), G.8262 (EEC), G.8273.2 (T-BC/T-TSC), GR-253-CORE (ST3/SMC), GR-1244-CORE (ST3/ST4/ST4E)	3	6	4	1 Hz to 650 MHz	1 Hz to 650 MHz	0.56	12	4
82P33831	Synchronization Management Unit (SMU) for IEEE 1588 and 10G/40G Synchronous Ethernet	G.813 (SEC), G.8262 (EEC), G.8273.2 (T-BC/T-TSC), GR-253-CORE (ST3/SMC), GR-1244-CORE (ST3/ST4/ST4E)	3	14	6	1 Hz to 650 MHz, Composite Clock (G.703 64kbps)	1 Hz to 650 MHz, Composite Clock (G.703 64kbps)	0.23	14	6
82P33910-1	Synchronization System For IEEE 1588	G.813 (SEC), G.8262 (EEC), G.8273.2 (T-BC/T-TSC), GR-253-CORE (ST3/SMC), GR-1244-CORE (ST3/ST4/ST4E)	3	14	6	1 Hz to 650 MHz, Composite Clock (G.703 64kbps)	1 Hz to 650 MHz, Composite Clock (G.703 64kbps)	0.56	13	4
82P33914-1	Synchronization System For IEEE 1588	G.813 (SEC), G.8262 (EEC), G.8273.2 (T-BC/T-TSC), GR-253-CORE (ST3/SMC), GR-1244-CORE (ST3/ST4/ST4E)	3	6	4	1 Hz to 650 MHz	1 Hz to 650 MHz	0.56	12	4
82P33931-1	Synchronization System For IEEE 1588 and 10G/40G Synchronous Ethernet	G.813 (SEC), G.8262 (EEC), G.8273.2 (T-BC/T-TSC), GR-253-CORE (ST3/SMC), GR-1244-CORE (ST3/ST4/ST4E)	3	14	6	1 Hz to 650 MHz, Composite Clock (G.703 64kbps)	1 Hz to 650 MHz, Composite Clock (G.703 64kbps)	0.23	14	6

Line Card Components									
Part Number	Product Type	Channels (#)	Inputs (#)	Diff. Inputs	Input Freq Range Type	Output Freq Range Type	Phase Jitter Typ RMS (ps)	Outputs (#)	Diff. Outputs
82P33724	Port Synchronizer for IEEE 1588 and Synchronous Ethernet	3	6	4	8 kHz to 650 MHz, Sync Pulse	1 Hz to 650 MHz	0.56	12	4
82P33741	Port Synchronizer for IEEE 1588 and 10G/40G Synchronous Ethernet	3	12	6	8 kHz to 650 MHz, Sync Pulse	1 Hz to 650 MHz	0.23	12	6

To request samples, download documentation, or learn more, visit: idt.com/go/sync