QSpan II™ Schematic Review Checklist

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1. Schematic Review Checklist for QSpan II

This document discusses the following schematic review topics for the QSpan II:

Revision History

8091862_CL001_02, November 2009

This version of the document was rebranded as IDT. It does not include any technical changes.

8091862_CL001_01, October 2001

This is the first release of the document.

1.1 Overview

The *QSpan II Schematic Review Checklist* describes common design issues that resulted from IDT's debugging of a variety of QSpan II applications. This document is intended for designers that are in the process of completing their QSpan II board schematics. For this reason, it is beneficial to review the contents of the checklist *before* routing your QSpan II-based board.

For more information about QSpan II's hardware and software, see the following:

- *QSpan II User Manual*
- *QSpan II Debug Checklist*

1.2 QSpan II Versions

The following two sections explain the hardware differences between the prototype and production versions of the QSpan II.

1.2.1 QSpan II Prototype Device

The QSpan II/Z/Z1 (CA91L862A-xxCEZx) defines pin R3 as VIO. This pin is redefined in the QSpan II production device (CA91L862A-xxCE) as VH. This change may impact some board designs.

The QSpan IIZ/Z1 defines VIO as an input pin. The VIO pin determines the PCI signaling characteristics. This implementation restricts the power-up sequencing of the QSpan II. If 5V is applied to the VIO pin, then the 3.3V power ramp must occur before the 5V power in order to ensure the current specification for the VIO pin is not exceeded. The current may be limited to VIO through an external series resistor. IDT suggests a 470 ohm pull-up resistor on VIO.

1.2.2 QSpan II Production Device

The QSpan II production device defines VH (Highest I/O voltage) as a power pin. This implementation removes the restriction on power sequencing. VH must be connected to the highest voltage level that the QSpan II I/Os will observe on either the QBus or the PCI bus. The QSpan II also contains Universal PCI buffers, meaning, the signaling characteristics of the device operate in both a 5V and a 3.3V signaling environment. For more information, see the *QSpan II Differences Summary* document, which is downloadable from our website.

1.3 Host versus Adaptor Issues

The following two sections explain how the QSpan II handles resets and interrupts in host and adapter card applications.

1.3.1 Resets

IDT recommends three reset scenarios that depend on the type of host processor connected to your QSpan II-based application.

MPC860 Interface

1. PCI host bridge application: QSpan II's PCI RST# --> MPC860's RESETH_.

   QSpan II's RESETO_ --> PCI RST# inputs of other PCI devices.

   This reset example allows the MPC860 to reset all PCI agents under software control. The MPC860 can write to QSpan II's MISC_CTL register, which causes the QSpan II to assert the RESETO_ signal. QSpan II's reset input RESETI_ is normally unused and should be pulled high through a resistor.

2. PCI adapter card application: QSpan II's RESETO_ --> MPC860's RESETH_, QSpan II's PCI RST# --> PCI RST#.

   This reset example allows the QSpan II to reset the MPC860 when the PCI RST# input is asserted, or when the software bit is asserted in the MISC_CTL register. QSpan II's reset input RESETI_ is normally unused and should be pulled high through a resistor. HS_HEALTHY_ should be left open since it has an internal pull-down resistor.

3. CompactPCI card that supports Hot Swap: QSpan II's HS_HEALTHY_ --> Hot Swap Controller's HEALTHY_.

   The remainder of the reset signals are connected using the same method as the PCI adapter card application.

MC68360 Interface

All three reset scenarios for the MC68360 Interface are the same as described in the MPC860 Interface.

M68040 Interface

1. PCI host bridge application: QSpan II's PCI RST# --> M68040 RESETI_. QSpan II's RESETO_ --> PCI RST# inputs of other PCI devices.

   This reset example also allows the M68040 to reset all of the PCI agents under software control. The M68040 can write to the software reset bit in the MISC_CTL register, which will cause the QSpan II to assert RESETO_. QSpan II's reset input RESETI_ is normally unused and should be pulled high through a resistor.

2. PCI adapter card application: QSpan II's RESETO_ --> M68040 RSTI_, QSpan II's RST# --> PCI RST#.

   This enables the QSpan II to reset the M68040 processor when PCI RST# is asserted, or when the software reset bit is asserted in the MISC_CTL register. QSpan II's reset input RESETI_ is normally unused and should be pulled high through a resistor.

3. CompactPCI card that supports Hot Swap: QSpan II's HS_HEALTHY_ --> Hot Swap Controller's HEALTHY_.

   The remainder of the signals should be connected the same as the PCI adapter card application.

1.3.2 Interrupts

MPC860 Interface

Host bridging applications: The QSpan II can accept INT# as an input and assert QINT_ as an output. QSpan II's interrupt output QINT_ should be connected to one of the seven possible interrupt inputs (IRQ[7:1]) on the MPC860.

Adapter card applications: The QSpan II can accept interrupts from the QBus on the QINT_ pin, and can pass them through the QSpan II to its PCI INT# output.

MC68360 Interface

Host bridging applications: The QSpan II can accept INT# as an input and assert QINT_ as an output. QSpan II's interrupt output QINT_ should be connected to one of seven possible interrupt pins (IRQ[7:1]) on the MC68360. When the MC68360 is acknowledging a QSpan II interrupt, it must be programmed to generate the cycle termination. The QSpan II is an autovector interrupter: it cannot assert AVEC_ during the interrupt acknowledge cycle.

Adapter card applications: The QSpan II can accept interrupts from the QBus on the QINT_ pin, and can pass them through the QSpan II to its PCI INT# output.

M68040 Interface

Host bridging applications: The QSpan II can accept INT# as an input and assert QINT_ as an output. QSpan II's interrupt output QINT_ should be connected to the interrupt prioritizing logic that is connected to the IPL[2:0] lines on the M68040 processor. When the M68040 is acknowledging a QSpan II interrupt there must be external logic to terminate the cycle. External logic is required because the QSpan II is an autovector interrupter: it cannot assert AVEC_ or TA_ during the interrupt acknowledge cycle.

Adapter card applications: The QSpan II can accept interrupts for the QBus on the QINT_ pin and pass them through the QSpan II to its PCI INT# output.

1.4 Clocking Strategies

The PCLK can operate anywhere from DC to 33 MHz. The maximum QCLK frequency depends on the host processor. For MPC860 applications, the maximum QCLK frequency is 50 MHz. For MC68360 applications, the maximum frequency is 33 MHz. The QSpan II is compatible with all M68040 variants in large buffer mode up to 40 MHz. The QSpan II is compatible with all M68040 variants in small buffer mode up to 33 MHz. The QCLK input is not required to be operating to complete QSpan II accesses from the PCI bus.

1.4.1 MPC860 Interface

QSpan II's QCLK input must be derived form the MPC860 CLKOUT signal. All of the AC timing waveforms shown in the *QSpan II User Manual* for the MPC860/QSpan II Interface are based on this clock output. IDT recommends to buffer the CLKOUT signal with a low skew PLL-based clock buffer because of the low drive strength of the CLKOUT signal. IDT also recommends a clock skew of 1 ns or less between the MPC860 and the QSpan II. If there is a change in clock frequency during operation, the example code in Appendix C of the *QSpan II Manual* must be implemented.

1.4.2 MC68360 Interface

The QSpan II must be clocked by the CLK01 output from the MC68360 processor. All of the AC timing waveforms shown in the *QSpan II Manual* for the QSpan II/MC68360 Interface are based on CLK01. Please note that when connecting the CLK01 output to the QSpan II QCLK input directly this connection can cause jitter. If you are using a clock buffer, the clock skew of this clock must be zero clock skew (skew < 1 ns).

1.4.3 M68040 Interface

QSpan II's QCLK input and M68040's BCLK input should be clocked from the same clock source. The AC timing waveforms shown in the *QSpan II Manual* for the M68040/QSpan II Interface are based on this assumption.

1.5 Processor Types — Transaction Channels

The QSpan II implements two main transaction channels:

- QBus Slave Channel
- PCI Target Channel

When using the QBus Slave Channel the path of the transaction is from the QBus to the PCI bus. When using the PCI bus Target Channel the path of the transaction is from the PCI bus to the QBus.

The following two sections explain some of the key processor differences that occur when completing transactions through these channels.

1.5.1 The QBus Slave Channel

1. The *QSpan II User Manual* adopts the convention that the most significant bit is always the largest number. MPC860 designers must ensure that they connect their pins accordingly. For example, pin A[31] on the QSpan II connects to pin A[31] on the MC68360 and M68040 bus, but connects to pin A[0] on the MPC860 bus. This applies to all MPC860 buses (D[31:0], AT[3:0], TSIZ[1:0]) not only the address bus.
2. During write transactions only MPC860 and M68040 Masters are capable of initiating burst transactions. The MPC860 and M68040 perform bursts of 16 bytes. Bursts accepted from the QBus are translated to the PCI bus as one or more burst transactions.
3. The QSpan II supports prefetched reads in the QBus Slave Channel for MPC860 and MC68360 cycles; M68040 cycles are not supported.

1.5.2 The PCI Target Channel

1. The QSpan II can support burst reads and burst writes on the QBus in MPC860 mode only. The QSpan II can only burst as a master on the QBus in MPC860 mode. This also holds true for DMA transfers. QSpan II generates DMA transfers on the QBus as an MC68360 master, as an MPC860 master, or as an M68040 master. As stated before the QBus master only generates burst cycles as an MPC860 master.
2. Transaction codes on the QBus. QSpan II's TC[3:0] are intended to be connected as follows, but can be used for other special decoding purposes. Any unused TC pins should be connected to pull-up resistors. QSpan II's TC[3:0] lines can be connected to the FC[3:0] lines of the MC68360 bus, the AT[0:3] lines of the MPC860 bus, and a subset of the TT[1:0] and TM[2:0] lines of the M68040 bus.
3. QBus arbitration and sampling. The QBus MC68360 Master Module’s default arbitration mode is asynchronous: it double-samples the BG_ and BB_/BGACK_ inputs using the falling and rising edge of QCLK. The MPC860 Master Module’s default arbitration mode is synchronous. The M68040 Master Module’s default operation is synchronous.

1.6 Processor Types — Master and Slave Modes of Operation

This section describes QSpan II's four QBus Master and Slave modes (see Table 1). The mode of operation is determined by the BDIP_ and the SIZ[1] signals at reset. The QBus can be in MC68360, MPC860, or M68040 Master mode.

The Master and Slave modes of the QSpan II are controlled by BDIP_ and SIZ[1] signals as follows:

Table 1: Reset Options for QBus Master and Slave Modes

Reset Sampling		Master Mode	Slave Mode
BDIP_	SIZ[1]		
0	0	MC68360	MC68360 and M68040
0	1	MC68360	MC68360 and MPC860
1	0	M68040	MC68360 and M68040
1	1	MPC860	MC68360 and MPC860

1.7 Power Supply

The QSpan II is available in two packages:

- 17 mm x 17 mm, 1.0 mm ball pitch, 256 PBGA
- 27 mm x 27 mm, 1.27 mm ball pitch, 256 PBGA

Both packages require a 3.3V power supply and provide 3.3V or 5V I/O signaling characteristics on the PCI bus. Both devices are also 5V tolerant. The recommended operating conditions can be found in Appendix F of the *QSpan II User Manual*.

1.8 Unused Pins

Unused inputs should be tied high or low; they should not be left floating. Unused input pins should be tied through pull-ups or pull-downs to VDD or VSS. Unused output pins can be left unconnected.

1.9 JTAG

The QSpan II includes dedicated user-accessible test logic that is fully compatible with the IEEE 1149.1 Standard Test Access Port and Boundary Scan Architecture. The following pins are provided: TCK, TDI, TDO, TMS, and TRST#.

There is an internal pull-up resistor on TMS that keeps QSpan II's JTAG controller in a reset state without requiring TRST# to be low.

1.10 Recommended Signal Terminations

This section describes the recommended termination of the signals in a typical QSpan II application.

These terminations only list the required pull-ups and pull-downs, which vary per application. For more information, see the previous sections and the "Typical Application" appendix of the *QSpan II User Manual*.

1.10.1 PCI Signals

AD [31:0]

PCI Address/Data Bus: Address and data are multiplexed over these pins to create a 32-bit address/data bus.

Signal type: Tristate bidirectional
Recommended termination: None

Checkpoint: Pass___ Fail___ Caution___ Help me___

Notes:

CBE# [3:0]

Bus Command and Byte Enable Lines: Command information during the address phase and byte line enables during the data phase of a transaction.

Signal type: Tristate bidirectional
Recommended termination: Pull-up

Checkpoint: Pass___ Fail___ Caution___ Help me___

Notes:

DEVSEL#

PCI Device Select: Driven by the QSpan II when it is accessed as PCI slave; sampled by the QSpan II when it is PCI master.

Signal type: Tristate bidirectional
Recommended termination: Pull-up

Checkpoint: Pass___ Fail___ Caution___ Help me___

Notes:

EXT_GNT#[6:1]

External Grant: Used by QSpan II to indicate to an external device that it has been granted access to the PCI bus.

Signal type: Output
Recommended termination: pull-up

Checkpoint: Pass___ Fail___ Caution___ Help me___

Notes:

EXT_REQ#[6:1]

External Request: Used by an external device to indicate to the QSpan II PCI bus arbiter that it wants to master the PCI bus.

Signal type: Bidirectional
Recommended termination: Pull-up

Checkpoint: Pass___ Fail___ Caution___ Help me___

Notes:

FRAME#

PCI Cycle Frame for PCI Bus: Driven by the QSpan II when it is PCI master; it is monitored by the QSpan II when it is PCI target. This signal indicates the beginning and duration of a transaction.

Signal type: Tristate bidirectional
Recommended termination: Pull-up

Checkpoint: Pass___ Fail___ Caution___ Help me___

Notes:

GNT#

PCI Grant: As an input, when the QSpan II uses an external arbiter, it indicates to the QSpan II that it has been granted ownership of the PCI bus. GNT# can be parked at QSpan II to improve its PCI master performance (for more information, see the “PCI Bus Arbiter” chapter of the *QSpan II User Manual*.

As an output, when the QSpan II is the PCI bus arbiter, it indicates to an external device that it has been granted access to the PCI bus.

Signal type: Bidirectional
Recommended termination: Pull-up

Checkpoint: Pass___ Fail___ Caution___ Help me___

Notes:

IDSEL

PCI Initialization Device Select: Used as a chip select during Configuration read and write transactions.

Signal type: Input
Recommended termination: Pull low.

Checkpoint: Pass___ Fail___ Caution___ Help me___

Notes:

INT#

PCI Interrupt: As an output, it indicates that the QSpan II is generating an internal interrupt. As an input, this signal causes QINT# to be asserted on the QBus (if enabled). The signal can be used as an input for an application where the MPC860 is the system host.

Signal type: Bidirectional open-drain
Recommended termination: Pull-up

Checkpoint: Pass___ Fail___ Caution___ Help me___

Notes:

IRDY#

PCI Initiator Ready: Used by the QSpan II to indicate that it is ready to complete the current data phase of the transaction. As a PCI target, the QSpan II monitors this signal during reads to determine when the PCI master is ready to accept data.

Signal type: Tristate bidirectional
Recommended termination: Pull-up

Checkpoint: Pass___ Fail___ Caution___ Help me___

Notes:

PAR

Parity: The parity is even across AD[31:0] and C/BE#[3:0]. The number of ones across these lines and PAR equal an even number.

Signal type: Tristate bidirectional
Recommended termination: None

Checkpoint: Pass___ Fail___ Caution___ Help me___

Notes:

PCLK

PCI Clock: Clock input for the PCI Interface: PCLK normally operates from 25 MHz and 33 MHz.

Signal type: Input
Recommended termination: None

Checkpoint: Pass___ Fail___ Caution___ Help me___

Notes:

PERR#

PCI Parity Error: Reports parity errors during all PCI transactions except a special cycle. The QSpan II asserts PERR# within two clocks of receiving a parity error on incoming data, and holds PERR# for at least one clock for each data phase that experiences errors.

Signal type: Tristate bidirectional
Recommended termination: Pull-up

Checkpoint: Pass___ Fail___ Caution___ Help me___

Notes:

REQ#

PCI Bus Request: Used by the QSpan II to indicate that it requires the use of the PCI bus; this is an output when the QSpan II uses an external arbiter. REQ# is also used by an external device to indicate to the QSpan II PCI bus arbiter that it wants use of the PCI bus; this signal is an input when the QSpan II PCI bus arbiter is used.

Signal type: Tristate bidirectional
Recommended termination: This pin must be weakly pulled high.

Checkpoint: Pass___ Fail___ Caution___ Help me___

Notes:

RST#

PCI Reset: Asynchronous reset that is used to bring PCI-specific registers, state machines, and signals, to a consistent state.

Signal type: Tristate bidirectional
Recommended termination: Pull-up

Checkpoint: Pass___ Fail___ Caution___ Help me___

Notes:

SERR#

PCI System Error: Reports address parity error during all transactions. QSpan II asserts SERR# within two clocks of receiving a parity error on incoming address, and holds SERR# for at least one clock for each data phase that experiences errors.

Signal type: Open drain
Recommended termination: Pull-up

Checkpoint: Pass___ Fail___ Caution___ Help me___

Notes:

STOP#

PCI Stop: Used by the QSpan II as PCI target when it wants to signal the PCI master to stop the current transaction. As PCI master, the QSpan II terminates the transaction if it receives STOP# from the PCI target.

Signal type: Tristate bidirectional
Recommended termination: Pull-up

Checkpoint: Pass___ Fail___ Caution___ Help me___

Notes:

TRDY#

PCI Target Ready: Used by the QSpan II as the PCI target to indicate it is ready to complete the current data phase. During a read with QSpan II as the PCI master, the target asserts TRDY# to indicate to the QSpan II that valid data is present on the data bus.

Signal type: Tristate bidirectional
Recommended termination: Pull-up

Checkpoint: Pass___ Fail___ Caution___ Help me___

Notes:

1.10.2 QBus Signals

A[31:0]

Address Bus: Address for the current bus cycle.

Signal type: Tristate bidirectional
Recommended termination: None

Checkpoint: Pass___ Fail___ Caution___ Help me___

Notes:

AS_

Address Strobe: Indicates the beginning, and duration, of a transaction on the QBus.

Signal type: Rescinding Tristate bidirectional
Recommended termination: Pull-up

Checkpoint: Pass___ Fail___ Caution___ Help me___

Notes:

AT[0:3]
See TC[3:0]

BB_/BGACK_
Bus Busy: Indicates the ownership of the QBus.

Signal type: Rescinding tristate bidirectional
Recommended termination: Pull-up

Checkpoint: Pass___ Fail___ Caution___ Help me___

Notes:

BDIP_
Burst Data In Progress: QBus master uses BDIP_ in burst writes to indicate the second last data beat. The QBus slave monitors BDIP_ as a signal to indicate the second last data beat in the burst.

Signal type: Bidirectional
Recommended termination: see modes section

Checkpoint: Pass___ Fail___ Caution___ Help me___

Notes:

BERR_/TEA_
Transfer Error Acknowledge: Indicates that a bus error occurred during the current transaction.

Signal type: Rescinding tristate bidirectional
Recommended termination: Pull-up

Checkpoint: Pass___ Fail___ Caution___ Help me___

Notes:

BG_

Bus Grant: Indicates that the QSpan II can be the next QBus master.

Signal type: Input
Recommended termination: Pull-up

Checkpoint: Pass___ Fail___ Caution___ Help me___

Notes:

BM_EN/FIFO_RDY_

Bus Master Enable/FIFO Ready: If this input is asserted (set as 1) during PCI reset, the Bus Master Enable bit in the PCI_CS register is also set. The allows the QSpan II to be the PCI bus master after reset.

Signal type: Bidirectional
Recommended termination: None; this signal has an internal pull-down

Checkpoint: Pass___ Fail___ Caution___ Help me___

Notes:

BR_

Bus Request: Used by the QSpan II to request ownership of the QBus.

Signal type: Output
Recommended termination: Pull-up

Checkpoint: Pass___ Fail___ Caution___ Help me___

Notes:

BURST_/TIP

Burst: Indicates the current transaction is a burst cycle.

Signal type: Tristate bidirectional
Recommended termination: Pull-up

Checkpoint: Pass___ Fail___ Caution___ Help me___

Notes:

CSPCI_

PCI Chip Select: Indicates the current transaction on the QBus is an access to the PCI Bus.

Signal type: Input
Recommended termination: Pull-up

Checkpoint: Pass___ Fail___ Caution___ Help me___

Notes:

CSREG_

Register Chip Select: Indicates the current transaction on the QBus is an access to QSpan II’s registers.

Signal type: Input
Recommended termination: Pull-up

Checkpoint: Pass___ Fail___ Caution___ Help me___

Notes:

DP[3:0]

Data Parity: Provides the parity information for the data on D[31:0]. It is valid on the same clock as the data.

Signal type: Bidirectional
Recommended termination: None

Checkpoint: Pass___ Fail___ Caution___ Help me___

Notes:

D[31:0]

Data Bus: Provides the general-purpose data path between the QSpan II, the local processor, and other devices.

Signal type: Tristate bidirectional
Recommended termination: None

Checkpoint: Pass___ Fail___ Caution___ Help me___

Notes:

DACK_/SDACK_

IDMA Acknowledge: Indicates to the QSpan II that the current transaction is an IDMA transaction.

Signal type: Input
Recommended termination: Pull-up

Checkpoint: Pass___ Fail___ Caution___ Help me___

Notes:

DONE_

IDMA Done: This signal is not used with MPC860 transfers.

Signal type: Input
Recommended termination: Pull-up

Checkpoint: Pass___ Fail___ Caution___ Help me___

Notes:

DREQ_

IDMA Request: Request to the MPC860 IDMA to either transfer data to the QSpan II IFIFO (PCI write) or to remove data from the IFIFO (PCI read). It is asserted from the rising edge of QCLK in MPC860 mode.

Signal type: Output
Recommended termination: Pull-up

Checkpoint: Pass___ Fail___ Caution___ Help me___

Notes:

DSACK0_

Data and Size Acknowledge: Acknowledge the completion of a data transfer on the QBus.

Signal type: Rescinding tristate bidirectional
Recommended termination: Pull-up

Checkpoint: Pass___ Fail___ Caution___ Help me___

Notes:

DSACK1_/TA_

Transaction Acknowledge: Driven by the addressed slave to acknowledge the completion of a data transfer on the QBus.

Signal type: Rescinding tristate bidirectional
Recommended termination: Pull-up

Checkpoint: Pass___ Fail___ Caution___ Help me___

Notes:

DS_

Data Strobe: Used to indicate valid data on the data bus during write transactions, and to request data during read transaction.

Signal type: Rescinding tristate output
Recommended termination: Pull-up

Checkpoint: Pass___ Fail___ Caution___ Help me___

Notes:

HALT_/TRETRY_

Transfer Retry: Used for generating retries.

Signal type: Rescinding tristate bidirectional
Recommended termination: Pull-up

Checkpoint: Pass___ Fail___ Caution___ Help me___

Notes:

IMSEL

Image Select: Selects which QBus Slave Image to use when CSPCI_ is asserted.

Signal type: Input
Recommended termination: None

Checkpoint: Pass___ Fail___ Caution___ Help me___

Notes:

QCLK

QBus Clock: All devices intended to connect to the QSpan II QBus Interface must synchronize to this clock.

Signal type: Input
Recommended termination: None

Checkpoint: Pass___ Fail___ Caution___ Help me___

Notes:

QINT_

QBus Interrupt: As an output, this open-drain signal is asserted by the QSpan II when an interrupt event occurs. As an input, this signal can be mapped to the PCI INT# output.

Signal type: Open-drain bidirectional
Recommended termination: Pull-up

Checkpoint: Pass___ Fail___ Caution___ Help me___

Notes:

RESETI_

QBus Reset Input: Resets the QSpan II from the QSpan II QBus Interface. Note that RESETI_ does not reset PCI configuration and status registers.

Signal type: Input
Recommended termination: Pull-up

Checkpoint: Pass___ Fail___ Caution___ Help me___

Notes:

RESETO_

QBus Reset Output: Asserted when QSpan II's PCI RST# input is asserted, or the internal software reset bit is set.

Signal type: Open-drain output
Recommended termination: Pull-up

Checkpoint: Pass___ Fail___ Caution___ Help me___

Notes:

R/W_

Read Write: Indicates the direction of the data transfer on the Data bus. High indicates a read transaction; low indicates a write.

Signal type: Tristate bidirectional
Recommended termination: None

Checkpoint: Pass___ Fail___ Caution___ Help me___

Notes:

SIZ[1:0]

Size: Indicates the number of bytes to be transferred during a bus cycle. The value of the Size bits, along with the lower two address bits and the port width, defines the byte lanes that are active.

Signal type: Tristate bidirectional
Recommended termination: None; also see modes section for SIZ[1]

Checkpoint: Pass___ Fail___ Caution___ Help me___

Notes:

TA_

See DSACK1_/TA_

TC[3:0]

Transaction Code Bus: Provides additional information about a bus cycle when the QSpan II is a QBus master.

Signal type: Tristate bidirectional
Recommended termination: None

Checkpoint: Pass___ Fail___ Caution___ Help me___

Notes:

TEA_

See BERR_/TEA_

TRETRY_

See HALT_/TRETRY_

TS_

Transfer Start: TS_ is a three-state bidirectional signal that indicates the beginning of an MPC860 bus transaction on the QBus.

Signal type: Rescinding tristate bidirectional
Recommended termination: Pull-up

Checkpoint: Pass___ Fail___ Caution___ Help me___

Notes:

1.10.3 Hot Swap Signals

ENUM#

Hot Swap Event Interrupt: Notifies the PCI host that either a board has been inserted or is about to be extracted.

Signal type: Open-drain output
Recommended termination: None

Checkpoint: Pass___ Fail___ Caution___ Help me___

Notes:

HS_HEALTHY_

Hot Swap Healthy: QSpan II internally OR's this input with PCI reset (RST#) to determine when back-end power is stable.

Signal type: Input
Recommended termination: None; this signal has an internal pull-down

Checkpoint: Pass___ Fail___ Caution___ Help me___

Notes:

HS_LED

Hot Swap LED control: This signal is driven by the QSpan II to control the status of the LED. The signal is driven low to turn on the LED during the hardware and software connection stages. The signal is tri-stated during normal operation to turn off the LED.

Signal type: Output

Recommended termination: None
Checkpoint: Pass___ Fail___ Caution___ Help me___

Notes:

HS_SWITCH

Hot Swap Switch: QSpan II uses this input to monitor the state of the Hot Swap board ejector latch. A low value on this signal indicates that the ejector latch is open.

Signal type: Input
Recommended termination: None; this signal has an internal pull-down

Checkpoint: Pass___ Fail___ Caution___ Help me___

Notes:

1.10.4 Miscellaneous Signals

ENID

ENID: EEPROM Loading Reset Option. If ENID is sampled high after a PCI reset, then the QSpan II downloads register information from the EEPROM. If an EEPROM is not used in you application, IDT recommends this pin be pulled low on the board through a pull-down resistor.

Signal type: Input
Recommended termination: See description; this signal has an internal pull-down

Checkpoint: Pass___ Fail___ Caution___ Help me___

Notes:

PCI_ARB_EN

PCI Arbiter Enable: If PCI_ARB_EN is sampled high at the negation of Reset, QSpan II's PCI bus arbiter is enabled and functions as the PCI bus arbiter. If the internal arbiter is used, the PCI_ARB_EN pin should be pulled high through a pull-up resistor on the board.

Signal type: Input
Recommended termination: See description; has an internal pull-down

Checkpoint: Pass___ Fail___ Caution___ Help me___

Notes:

PCI_DIS

PCI Configuration Disable: This is a power-up option that makes the QSpan II hold off on ENUM# assertion and retry PCI configuration cycles to allow the Host processor to perform local configuration. The QSpan II accepts PCI configuration cycles after the PCI_DIS bit is cleared in the MISC_CTL2 register.

Signal type: Input
Recommended termination: Pull-up

Checkpoint: Pass___ Fail___ Caution___ Help me___

Notes:

PME#

Power Management Event Interrupt: This signal is asserted to request a change in its current power management state and/or to indicate that a power management event has occurred.

Signal type: Open-drain output
Recommended termination: None

Checkpoint: Pass___ Fail___ Caution___ Help me___

Notes:

SCL

Serial Clock: EEPROM Serial clock. The frequency of the SCL is the PCLK frequency divided by 2 to the tenth power.

Signal type: Output
Recommended termination: None

Checkpoint: Pass___ Fail___ Caution___ Help me___

Notes:

SDA

Serial Data: EEPROM Serial data line. If SDA is sampled high after a PCI reset, then the QSpan II downloads register information from the EEPROM. If your design is not using an EEPROM this pin should be pulled low on the board.

Signal type: bidirectional
Recommended termination: None; see description.

Checkpoint: Pass___ Fail___ Caution___ Help me___

Notes:

TEST1

This is a manufacturing test input that should be left open. This pin has an internal pull-up resistor.

Signal type: Input
Recommended termination: None; see description.

Checkpoint: Pass___ Fail___ Caution___ Help me___

Notes:

TEST2

This is a manufacturing test input that should be left open. This pin has an internal pull-down resistor.

Signal type: Input
Recommended termination: None; see description.

Checkpoint: Pass___ Fail___ Caution___ Help me___

Notes:

TEST3

This is a manufacturing test input that should be left open. This pin has an internal pull-down resistor.

Signal type: Input
Recommended termination: None; see description.

Checkpoint: Pass___ Fail___ Caution___ Help me___

Notes:

TMODE[1:0]

Test Mode: Selects the QSpan II test mode. These pins have internal pull-down resistors.

Signal type: Input
Recommended termination: See Table 2.

Checkpoint: Pass___ Fail___ Caution___ Help me___

Notes:

Table 2: Test Mode Operation

TMODE[1:0]	Operation Mode
00	Normal Mode
01	Reserved
10	Reserved
11	NAND Tree/Tristate Outputs

VH

Highest I/O Voltage: VH is a power pin that must be connected to the highest voltage level that the QSpan II I/Os will observe on either the QBus or the PCI bus.

Signal type: Power
Recommended termination: See the description.

Checkpoint: Pass___ Fail___ Caution___ Help me___

Notes: