User's Manual

RZ/G2L, RZ/V2L SMARC Module Board

User's Manual: Hardware

Renesas Microprocessor
RZ Family / RZ/G, RZ/V Series

Renesas Electronics
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— Arm® Cortex®-A55
— Arm® Cortex®-M33
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General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products
   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

Table of Contents

1. Overview

1.1 Purpose

First, only the RZ/G2L SMARC Module Board is explained here.

The difference between the RZ/G2L SMARC Module Board (hereafter referred to as “RZ/G2L SMARC Module”) and the RZ/V2L SMARC Module Board (hereafter referred to as “RZ/V2L SMARC Module”) is that the RZ/V2L SMARC Module uses the Renesas Electronics RZ/V2L microprocessor, which is pin-compatible with the RZ/G2L. In other words, they are functionally the same.

The RZ/G2L SMARC Module is a platform designed according to the SMARC 2.1 Specification to evaluate the Renesas RZ/G2L microprocessor.
Basically, the RZ/G2L SMARC Module is connected to the Renesas RZ SMARC Series Carrier Board (hereafter referred to as “RZ SMARC Carrier”) and used as the RZ/G2L SMARC Evaluation Board Kit (hereafter referred to as “RZ/G2L EVKIT”).

This guide includes system setup and configuration. It also provides detailed information on the overall design and use of this board from a hardware system perspective.

1.2 Configuration

Figure 1.1 shows an example of system configuration using the RZ/G2L SMARC Module.

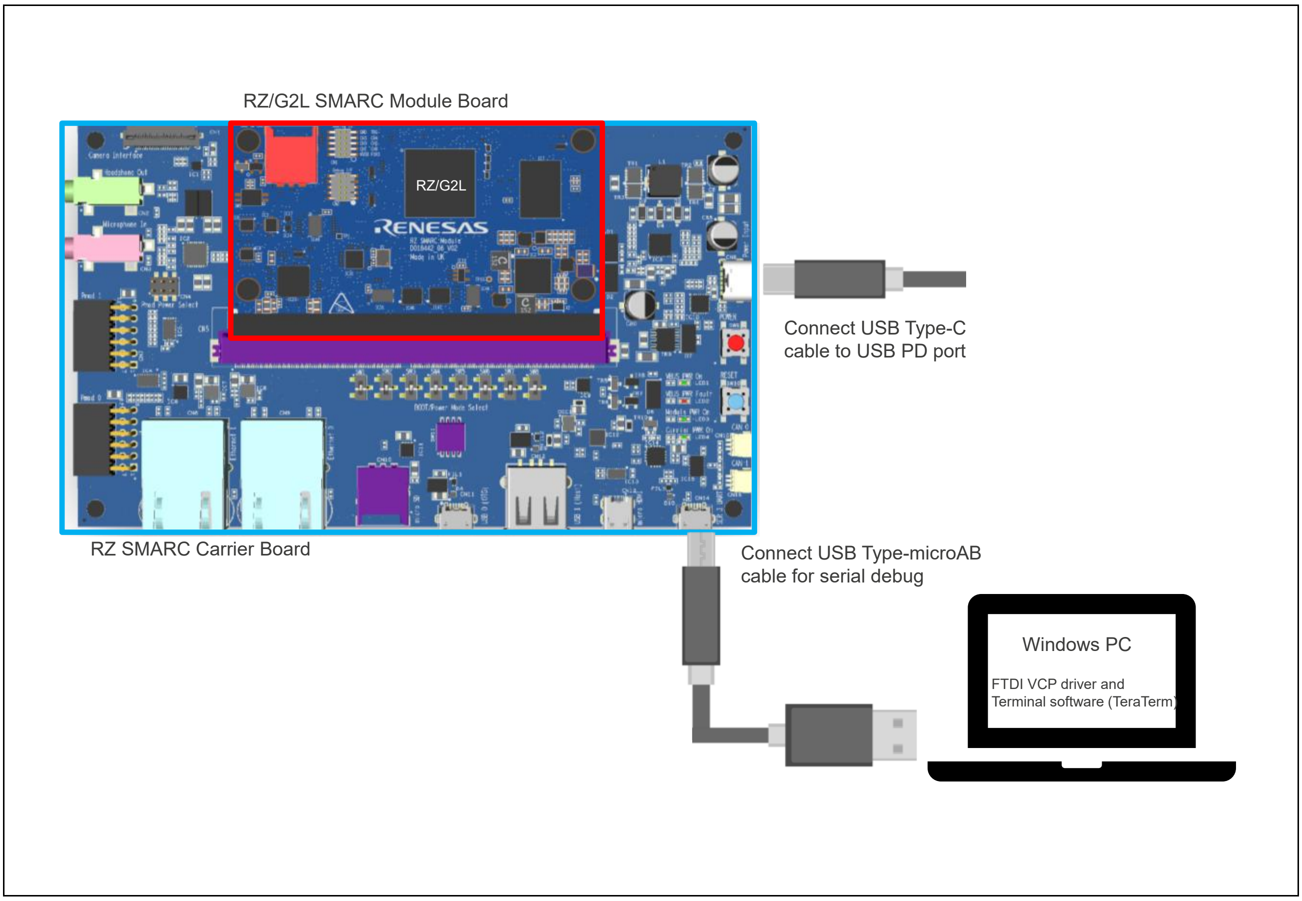


Figure 1.1 Example of System Configuration

1.3 Features

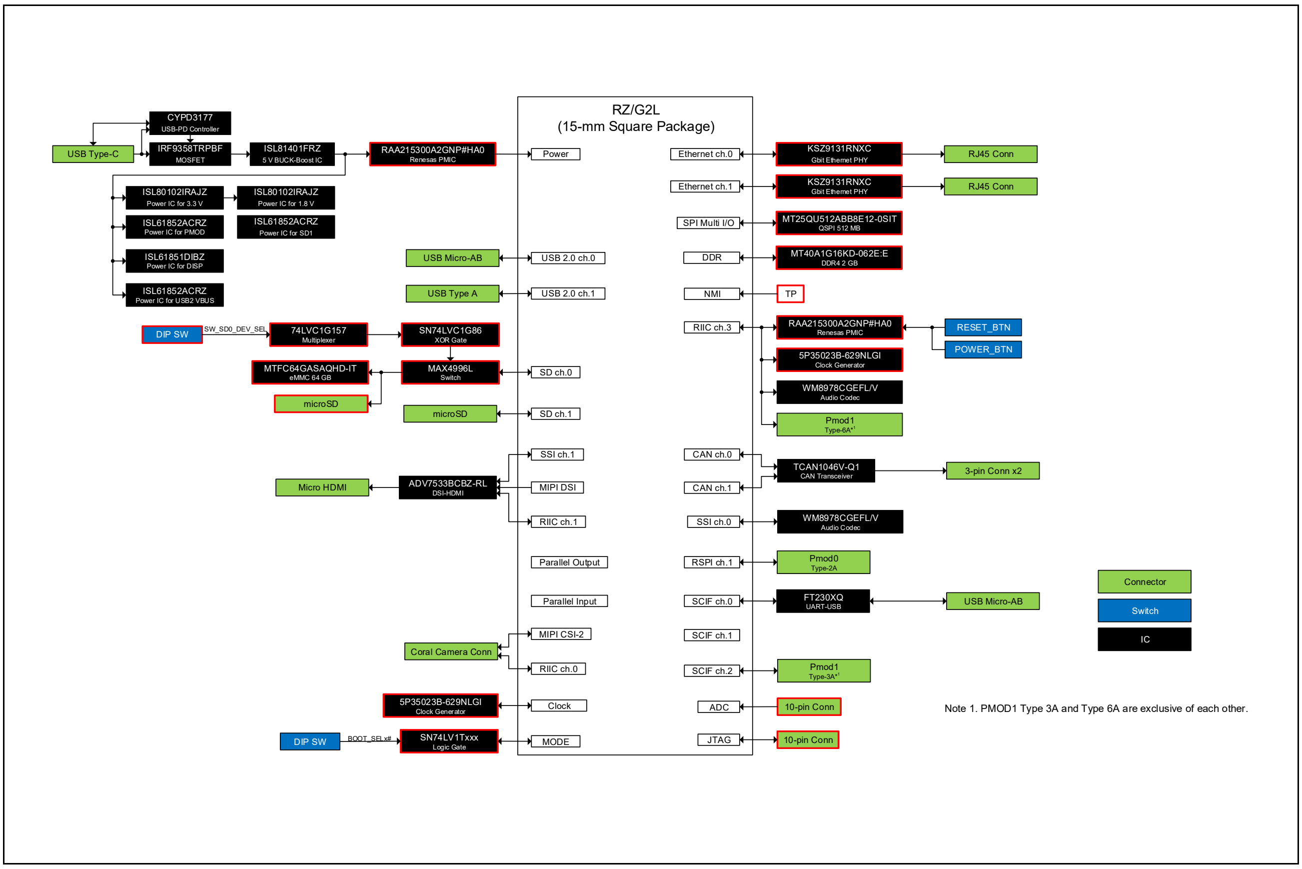
Table 1.1 lists the features of the RZ/G2L SMARC Module.

Table 1.1 Features

Item	Details
MPU	RZ/G2L: R9A07G044L23GBG or R9A07G044L27GBG Package: 456-pin LFBGA, 15 mm × 15 mm, 0.5-mm pitch
NOR Flash	Micron MT25QU512ABB8E12-0SIT 512-Mbit
DDR4	Micron MT40A1G16KD-062E:E 2-GB 1Gx16, supporting the data rate up to 1600 MT/s
Ethernet Interface	Ethernet PHY: KSZ9131RNXC × 2
ADC Interface	Connector: 10-pin with 1.27-mm pitch
Clock	Clock generator: 5P35023B-629NLGI RZ/G2L main: 24 MHz RZ/G2L external clock 1 for audio: 11.2896 MHz RZ/G2L external clock 2 for audio: 12.2880 MHz Ethernet PHY: 25 MHz Audio codec: 11.2896 MHz
Power Supply	PMIC: RAA215300A2GNP#HA0
Debug Interface	Connector: 10-pin with 1.27-mm pitch
eMMC	Micron MTFC64GASAQHD-IT 64-GB, supporting HS200 transfer modes
SD Interface	Connector: microSD card slot Support for default, high-speed, and UHS-I transfer modes, including SDR50 and SDR104
Switch	For mode setting and SD ch. 0 selection: 2-bit DIP switch
Boot Mode	Support for eSD, 1.8-V eMMC, 1.8-V SPI, and SCIF download mode
Circuit board specifications	Dimensions: 82 mm (W) × 50 mm (L) × 1.2 mm (H) Mount: Double-sided mounting (6 layers)

1.4 Blcok Diagram

Figure 1.2 shows a block diagram of the RZ/G2L EVKIT.



Note 1. PMOD1 Type 3A and Type 6A are exclusive of each other.

Figure 1.2 Block Diagram

1.5 Component Layout

Figure 1.3 and **Figure 1.4** show the component layouts on the top and bottom sides of the RZ/G2L SMARC Module.

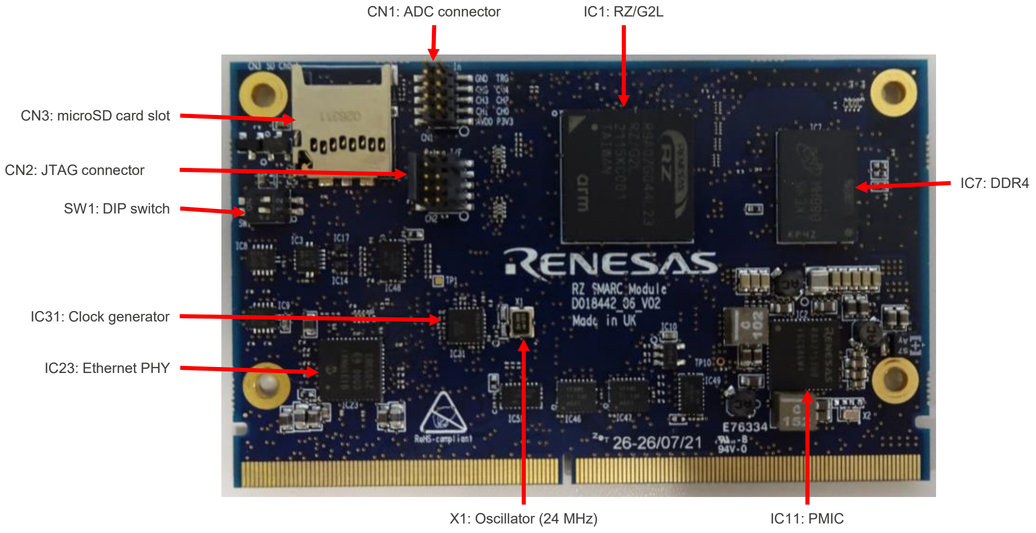


Figure 1.3 Component Layout (Top View)

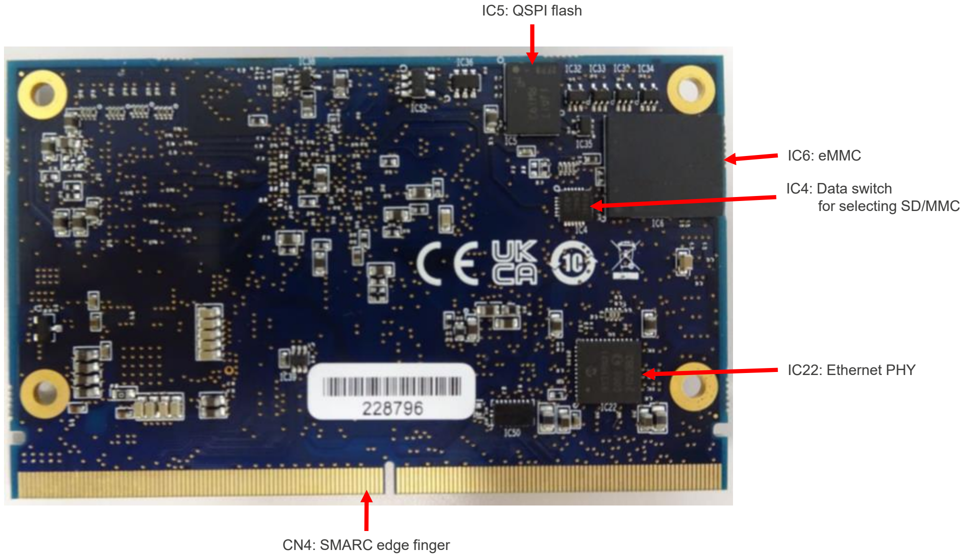


Figure 1.4 Component Layout (Bottom View)

1.6 Absolute Maximum Ratings

Table 1.2 lists the absolute maximum ratings of the RZ/G2L EVKIT.

Table 1.2 Absolute Maximum Ratings

Symbol	Item	Rated Value	Note
VDD_IN	Power voltage	5.25 V	Reference: Vss
—	Maximum power consumption	3 A	Includes continuous RZ SMARC Carrier current consumption
Topr	Operating ambient temperature*[1]	0°C to 50°C	Do not expose to condensation or corrosive gases
Tstg	Storage temperature*[1]	-10°C to 60°C	Do not expose to condensation or corrosive gases

Note 1. Ambient temperature is the air temperature at a position as close to the board as possible.

1.7 Operating Condition

Table 1.3 lists the operating conditions of the RZ/G2L EVKIT.

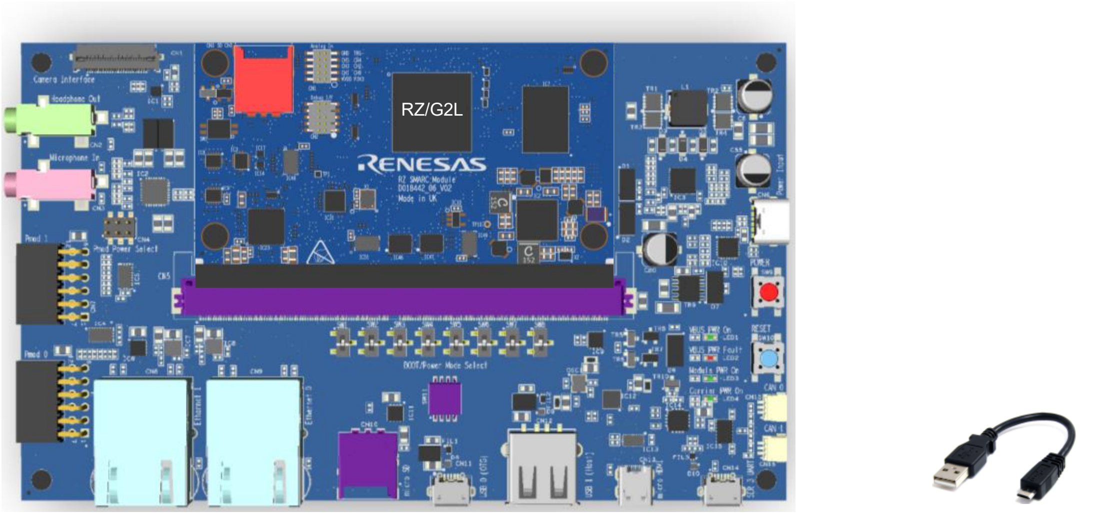
Table 1.3 Operating Conditions

Symbol	Item	Rated Value	Note
VDD_IN	Power voltage	3.0 V to 5.25 V	Reference: SMARC v2.1 specification
Topr	Operating ambient temperature*[1]	0°C to 40°C	Do not expose to condensation or corrosive gases

Note 1. Ambient temperature is the air temperature at a position as close to the board as possible.

2. Box Contents

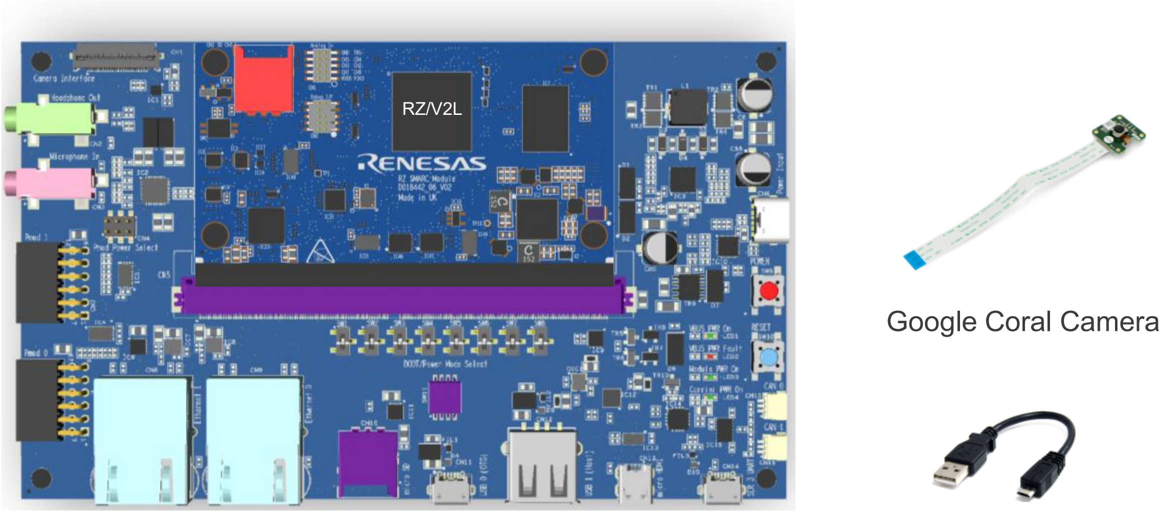
Figure 2.1 and **Figure 2.2** show the components included in each box.



RZ/G2L EVKIT

USB Type-A to micro B cable

Figure 2.1 RZ/G2L EVKIT



Google Coral Camera

RZ/V2L EVKIT

USB Type-A to micro B cable

Figure 2.2 RZ/V2L EVKIT

3. Ordering Infomation

- RZ/G2L EVKIT orderable part numbers:
  RTK9744L23S01000BE
  RTK9744L27S01000BE

There are two types of RZ/G2L EVKIT, as listed above.

RTK9744L23S01000BE is equipped with R9A07G044L23GBG (for which the security is not supported) as the microprocessor. However, this kit is planned to be discontinued (EOL). No additional production is planned, and it is only available while supplies last.

RTK9744L27S01000BE is equipped with R9A07G044L27GBG (for which the security is supported). RTK9744L27S01000BE can be evaluated the same as RTK9744L23S01000BE if you do not activate the security function.

- RZ/V2L EVKIT orderable part numbers:
  RTK9754L23S01000BE
  RTK9754L27S01000BE

There are two types of RZ/V2L EVKIT, as listed above.

RTK9754L23S01000BE is equipped with R9A07G054L23GBG (for which the security is not supported) as the microprocessor.

RTK9754L27S01000BE is equipped with R9A07G054L27GBG (for which the security is supported). This kit is compatible with the security type. RTK9754L27S01000BE can be evaluated the same as RTK9754L23S01000BE if you do not activate the security function.

4. Functional Specifications

4.1 MPU

4.1.1 Processor

The RZ/G2L includes a dual ARM® Cortex®-A55 core with speeds up to 1.2 GHz, and a single Arm® Cortex®-M33 core with speeds up to 200 MHz.

The Arm® Mali™-G31 as 3D graphics and display output and H.264 as video codec are supported for HMI applications. In addition, many interfaces such as camera input, dual 1-Gbit/s Ethernet controllers, and USB 2.0 are supported.

The RZ/G2L is useful for the following applications:

- Entry-class HMI, embedded devices with video capabilities, etc.

For details on the processor, refer to the “RZ/G2L Group, RZ/G2LC Group User’s Manual: Hardware”.

The RZ/V2L includes a dual ARM® Cortex®-A55 core with speeds up to 1.2 GHz, a single Arm® Cortex®-M33 core with speeds up to 200 MHz, and a “DRP-AI” AI accelerator for vision processing, which is Renesas’ original technology.

The RZ/V2L is useful for the following applications:

- Industrial vision system, AI-enabled consumer devices, surveillance cameras, etc.

For details on the processor, refer to the “RZ/V2L Group User’s Manual: Hardware”.

4.1.2 List of Pin Functions

Table 4.1 lists the pin functions of the RZ/G2L for use with the RZ/G2L SMARC Module.

Table 4.1 List of Pin Function Selections (1/17)

Pin Location	Pin Name	Pin Function	Description	SMARC Pin No.	SMARC Pin Name
G12	VDD18	VDD18	1.8 V	—	—
B11	ABG_NCP_OUT	ABG_NCP_OUT	Connected to GND via the 1-μF bypass capacitor*[1]	—	—
E22	ADC_AVDD18	ADC_AVDD18	1.8 V	—	—
A28	ADC_CH0	ADC_CH0	Pin header CN1 for ADC input	—	—
B27	ADC_CH1	ADC_CH1	Pin header CN1 for ADC input	—	—
B28	ADC_CH2	ADC_CH2	Pin header CN1 for ADC input	—	—
A27	ADC_CH3	ADC_CH3	Pin header CN1 for ADC input	—	—
C26	ADC_CH4	ADC_CH4	Pin header CN1 for ADC input	—	—
B26	ADC_CH5	ADC_CH5	Pin header CN1 for ADC input	—	—
A26	ADC_CH6	ADC_CH6	Connected to GND*[1]	—	—
B25	ADC_CH7	ADC_CH7	Connected to GND*[1]	—	—
E12	AUDIO_CLK1	AUDIO_CLK1	Input 11.2896 MHz from 5P35023 for generating the CD sampling rate (44.1 kHz)	—	—
B8	AUDIO_CLK2	AUDIO_CLK2	Input 12.2880 MHz from 5P35023 for generating the DVD sampling rate (48.0 kHz)	—	—
AB23	BSCANP	BSCANP	Initial setting: 0 (pull-down) It should be controllable by a resistor.	—	—
AB24	VSS	VSS	GND	—	—
AG12	CSI_CLKN	CSI_CLKN	24-pin FFC connector on the RZ SMARC Carrier	P4	CSI1_CLK-
AG13	CSI_CLKP	CSI_CLKP	24-pin FFC connector on the RZ SMARC Carrier	P3	CSI1_CLK+
AH13	CSI_DATA0_N	CSI_DATA0_N	24-pin FFC connector on the RZ SMARC Carrier	P8	CSI1_RX0-
AJ13	CSI_DATA0_P	CSI_DATA0_P	24-pin FFC connector on the RZ SMARC Carrier	P7	CSI1_RX0+
AH12	CSI_DATA1_N	CSI_DATA1_N	24-pin FFC connector on the RZ SMARC Carrier	P11	CSI1_RX1-
AJ12	CSI_DATA1_P	CSI_DATA1_P	24-pin FFC connector on the RZ SMARC Carrier	P10	CSI1_RX1+
AH14	CSI_DATA2_N	CSI_DATA2_N	24-pin FFC connector on the RZ SMARC Carrier	P14	CSI1_RX2-
AJ14	CSI_DATA2_P	CSI_DATA2_P	24-pin FFC connector on the RZ SMARC Carrier	P13	CSI1_RX2+
AH11	CSI_DATA3_N	CSI_DATA3_N	24-pin FFC connector on the RZ SMARC Carrier	P17	CSI1_RX3-
AJ11	CSI_DATA3_P	CSI_DATA3_P	24-pin FFC connector on the RZ SMARC Carrier	P16	CSI1_RX3+
AD12	CSI_VDD18	CSI_VDD18	1.8 V	—	—
AD13	CSI_VDD18	CSI_VDD18	1.8 V	—	—
G29	DDR_ADDR0	DDR_ADDR0	DDR4 SDRAM (MT40A1G16KD-062E:E)	—	—
M27	DDR_ADDR1	DDR_ADDR1	DDR4 SDRAM (MT40A1G16KD-062E:E)	—	—
R29	DDR_ADDR10	DDR_ADDR10	DDR4 SDRAM (MT40A1G16KD-062E:E)	—	—
K28	DDR_ADDR11	DDR_ADDR11	DDR4 SDRAM (MT40A1G16KD-062E:E)	—	—
P29	DDR_ADDR12	DDR_ADDR12	DDR4 SDRAM (MT40A1G16KD-062E:E)	—	—
E29	DDR_ADDR13	DDR_ADDR13	DDR4 SDRAM (MT40A1G16KD-062E:E)	—	—
H29	DDR_ADDR14	DDR_ADDR14	DDR4 SDRAM (MT40A1G16KD-062E:E)	—	—

Table 4.1 List of Pin Function Selections (2/17)

Pin Location	Pin Name	Pin Function	Description	SMARC Pin No.	SMARC Pin Name
G27	DDR_ADDR15	DDR_ADDR15	DDR4 SDRAM (MT40A1G16KD-062E:E)	—	—
F28	DDR_ADDR2	DDR_ADDR2	DDR4 SDRAM (MT40A1G16KD-062E:E)	—	—
F29	DDR_ADDR3	DDR_ADDR3	DDR4 SDRAM (MT40A1G16KD-062E:E)	—	—
L29	DDR_ADDR4	DDR_ADDR4	DDR4 SDRAM (MT40A1G16KD-062E:E)	—	—
D29	DDR_ADDR5	DDR_ADDR5	DDR4 SDRAM (MT40A1G16KD-062E:E)	—	—
L28	DDR_ADDR6	DDR_ADDR6	DDR4 SDRAM (MT40A1G16KD-062E:E)	—	—
C28	DDR_ADDR7	DDR_ADDR7	DDR4 SDRAM (MT40A1G16KD-062E:E)	—	—
H28	DDR_ADDR8	DDR_ADDR8	DDR4 SDRAM (MT40A1G16KD-062E:E)	—	—
E28	DDR_ADDR9	DDR_ADDR9	DDR4 SDRAM (MT40A1G16KD-062E:E)	—	—
H27	DDR_BA0	DDR_BA0	DDR4 SDRAM (MT40A1G16KD-062E:E)	—	—
M28	DDR_BA1	DDR_BA1	DDR4 SDRAM (MT40A1G16KD-062E:E)	—	—
G28	DDR_BA2	DDR_BA2	DDR4 SDRAM (MT40A1G16KD-062E:E)	—	—
C29	DDR_CALIBRATION	DDR_CALIBRATION	DDR4 SDRAM (MT40A1G16KD-062E:E)	—	—
K29	DDR_CAS#	DDR_CAS#	DDR4 SDRAM (MT40A1G16KD-062E:E)	—	—
N28	DDR_CKE	DDR_CKE	DDR4 SDRAM (MT40A1G16KD-062E:E)	—	—
T28	DDR_CLK_N	DDR_CLK_N	DDR4 SDRAM (MT40A1G16KD-062E:E)	—	—
T29	DDR_CLK_P	DDR_CLK_P	DDR4 SDRAM (MT40A1G16KD-062E:E)	—	—
P28	DDR_CS0#	DDR_CS0#	DDR4 SDRAM (MT40A1G16KD-062E:E)	—	—
M29	DDR_CS1#	DDR_CS1#	DDR4 SDRAM (MT40A1G16KD-062E:E)	—	—
W29	DDR_DM0	DDR_DM0	DDR4 SDRAM (MT40A1G16KD-062E:E)	—	—
AC29	DDR_DM1	DDR_DM1	DDR4 SDRAM (MT40A1G16KD-062E:E)	—	—
V28	DDR_DQ0	DDR_DQ0	DDR4 SDRAM (MT40A1G16KD-062E:E)	—	—
AB29	DDR_DQ1	DDR_DQ1	DDR4 SDRAM (MT40A1G16KD-062E:E)	—	—
AC28	DDR_DQ10	DDR_DQ10	DDR4 SDRAM (MT40A1G16KD-062E:E)	—	—
AE29	DDR_DQ11	DDR_DQ11	DDR4 SDRAM (MT40A1G16KD-062E:E)	—	—
AH29	DDR_DQ12	DDR_DQ12	DDR4 SDRAM (MT40A1G16KD-062E:E)	—	—
AE28	DDR_DQ13	DDR_DQ13	DDR4 SDRAM (MT40A1G16KD-062E:E)	—	—
AF29	DDR_DQ14	DDR_DQ14	DDR4 SDRAM (MT40A1G16KD-062E:E)	—	—
AG29	DDR_DQ15	DDR_DQ15	DDR4 SDRAM (MT40A1G16KD-062E:E)	—	—
U28	DDR_DQ2	DDR_DQ2	DDR4 SDRAM (MT40A1G16KD-062E:E)	—	—
AB28	DDR_DQ3	DDR_DQ3	DDR4 SDRAM (MT40A1G16KD-062E:E)	—	—
V27	DDR_DQ4	DDR_DQ4	DDR4 SDRAM (MT40A1G16KD-062E:E)	—	—
W28	DDR_DQ5	DDR_DQ5	DDR4 SDRAM (MT40A1G16KD-062E:E)	—	—
U27	DDR_DQ6	DDR_DQ6	DDR4 SDRAM (MT40A1G16KD-062E:E)	—	—
V29	DDR_DQ7	DDR_DQ7	DDR4 SDRAM (MT40A1G16KD-062E:E)	—	—
AF28	DDR_DQ8	DDR_DQ8	DDR4 SDRAM (MT40A1G16KD-062E:E)	—	—
AD29	DDR_DQ9	DDR_DQ9	DDR4 SDRAM (MT40A1G16KD-062E:E)	—	—
Y28	DDR_DQS0_N	DDR_DQS0_N	DDR4 SDRAM (MT40A1G16KD-062E:E)	—	—

Table 4.1 List of Pin Function Selections (3/17)

Pin Location	Pin Name	Pin Function	Description	SMARC Pin No.	SMARC Pin Name
AA29	DDR_DQS0_P	DDR_DQS0_P	DDR4 SDRAM (MT40A1G16KD-062E:E)	—	—
AC27	DDR_DQS1_N	DDR_DQS1_N	DDR4 SDRAM (MT40A1G16KD-062E:E)	—	—
AC26	DDR_DQS1_P	DDR_DQS1_P	DDR4 SDRAM (MT40A1G16KD-062E:E)	—	—
N29	DDR_ODT0	DDR_ODT0	DDR4 SDRAM (MT40A1G16KD-062E:E)	—	—
N27	DDR_ODT1	DDR_ODT1	DDR4 SDRAM (MT40A1G16KD-062E:E)	—	—
J29	DDR_RAS#	DDR_RAS#	DDR4 SDRAM (MT40A1G16KD-062E:E)	—	—
B29	DDR_RESET#	DDR_RESET#	DDR4 SDRAM (MT40A1G16KD-062E:E)	—	—
H25	DDR_VDDQ	DDR_VDDQ	1.2 V	—	—
M25	DDR_VDDQ	DDR_VDDQ	1.2 V	—	—
N25	DDR_VDDQ	DDR_VDDQ	1.2 V	—	—
U25	DDR_VDDQ	DDR_VDDQ	1.2 V	—	—
V25	DDR_VDDQ	DDR_VDDQ	1.2 V	—	—
AA25	DDR_VDDQ	DDR_VDDQ	1.2 V	—	—
AB25	DDR_VDDQ	DDR_VDDQ	1.2 V	—	—
J28	DDR_WE#	DDR_WE#	DDR4 SDRAM (MT40A1G16KD-062E:E)	—	—
AE18	DEBUGEN	DEBUGEN	DIP_SW (SW1)	—	—
AG18	DSI_CLKN	DSI_CLKN	MIPI-DSI-to-HDMI transmitter on the RZ SMARC Carrier	S135	DSI0_CLK-
AG17	DSI_CLKP	DSI_CLKP	MIPI-DSI-to-HDMI transmitter on the RZ SMARC Carrier	S134	DSI0_CLK+
AJ16	DSI_DATA0_N	DSI_DATA0_N	MIPI-DSI-to-HDMI transmitter on the RZ SMARC Carrier	S126	DSI0_D0-
AH16	DSI_DATA0_P	DSI_DATA0_P	MIPI-DSI-to-HDMI transmitter on the RZ SMARC Carrier	S125	DSI0_D0+
AJ17	DSI_DATA1_N	DSI_DATA1_N	MIPI-DSI-to-HDMI transmitter on the RZ SMARC Carrier	S129	DSI0_D1-
AH17	DSI_DATA1_P	DSI_DATA1_P	MIPI-DSI-to-HDMI transmitter on the RZ SMARC Carrier	S128	DSI0_D1+
AJ15	DSI_DATA2_N	DSI_DATA2_N	MIPI-DSI-to-HDMI transmitter on the RZ SMARC Carrier	S132	DSI0_D2-
AH15	DSI_DATA2_P	DSI_DATA2_P	MIPI-DSI-to-HDMI transmitter on the RZ SMARC Carrier	S131	DSI0_D2+
AJ18	DSI_DATA3_N	DSI_DATA3_N	MIPI-DSI-to-HDMI transmitter on the RZ SMARC Carrier	S138	DSI0_D3-
AH18	DSI_DATA3_P	DSI_DATA3_P	MIPI-DSI-to-HDMI transmitter on the RZ SMARC Carrier	S137	DSI0_D3+
AC17	DSI_VDD18	DSI_VDD18	1.8 V	—	—
AC18	DSI_VDD18	DSI_VDD18	1.8 V	—	—
N6	PVDD182533_0	PVDD182533_0	1.8 V	—	—
U7	PVDD182533_1	PVDD182533_1	1.8 V	—	—
AG2	EXCLK	EXCLK	Input 24 MHz from 5P35023 for generating system clock	—	—
V7	VDD18	VDD18	1.8 V	—	—
E8	MD_BOOT0	MD_BOOT0	Input BOOT_SEL0#, BOOT_SEL1#, BOOT_SEL2# logic states	P123, P124, P125	BOOT_SEL 0#,1#,2#
E7	MD_BOOT1	MD_BOOT1	Input BOOT_SEL0#, BOOT_SEL1#, BOOT_SEL2# logic states	P123, P124, P125	BOOT_SEL 0#,1#,2#
G7	MD_BOOT2	MD_BOOT2	Input BOOT_SEL0#, BOOT_SEL1#, BOOT_SEL2# logic states	P123, P124, P125	BOOT_SEL 0#,1#,2#

Table 4.1 List of Pin Function Selections (4/17)

Pin Location	Pin Name	Pin Function	Description	SMARC Pin No.	SMARC Pin Name
D23	MD_CLKS	MD_CLKS	Initial setting: 1 (pull-up) It should be controllable by a resistor.	—	—
E23	MD_OSCDRV0	MD_OSCDRV0	Initial setting: 0 (pull-down) It should be controllable by a resistor.	—	—
D27	MD_OSCDRV1	MD_OSCDRV1	Initial setting: 0 (pull-down) It should be controllable by a resistor.	—	—
AJ2	NMI	NMI	Connected to the test pin (TP1)	—	—
G17	OTP_VDD18	OTP_VDD18	1.8 V	—	—
A11	P0_0/IRQ0/SCI0_RXD/GTIOC0A/MTIOC0A/SCIF3_TXD	P0_0	For selecting the device connected to the SD/MMC ch. 0 interface Input SD0_DEV_SEL signal to identify the device connected to the SD ch. 0 interface by software	—	—
B12	P0_1/IRQ1/SCI0_TXD/GTIOC0B/MTIOC0B/SCIF3_RXD	IRQ1	Unused	—	—
C13	P1_0/IRQ2/SCI0_SCK/GTIOC1A/MTIOC0C/SCIF3_SCK	IRQ2	Ethernet 0 PHY (KSZ9131RNXC)	—	—
A12	P1_1/IRQ3/SCI0_CTS_N_RTS_N/GTIOC1B/MTIOC0D	IRQ3	Ethernet 1 PHY (KSZ9131RNXC)	—	—
AJ22	P10_0/DISP_DATA6/CAN_CLK/MTIOC6A/GTETRGA	P10_0	Unused	—	—
AH22	P10_1/DISP_DATA7/CAN0_TX/MTIOC6B/GTETRGB	CAN0_TX	CAN transceiver ch. 0*[2] on the RZ SMARC Carrier*[2]	P143	CAN0_TX
AG22	P11_0/DISP_DATA8/CAN0_RX/MTIOC6C/GTETRGC	CAN0_RX	CAN transceiver ch. 0*[2] on the RZ SMARC Carrier*[2]	P144	CAN0_RX
AF22	P11_1/DISP_DATA9/CAN0_TX_DATARATE_EN/MTIOC6D/GTETRGD	P11_1	Unused	—	—
AE22	P12_0/DISP_DATA10/CAN0_RX_DATARATE_EN/POE0_N/GTIOC7A	P12_0	Unused	—	—
AE23	P12_1/DISP_DATA11/CAN1_TX/POE4_N/GTIOC7B	CAN1_TX	CAN transceiver ch. 1*[2] on the RZ SMARC Carrier*[2]	P145	CAN1_TX
AF23	P13_0/DISP_DATA12/CAN1_RX/POE8_N/IRQ0	CAN1_RX	CAN transceiver ch. 1*[2] on the RZ SMARC Carrier*[2]	P146	CAN1_RX

Table 4.1 List of Pin Function Selections (5/17)

Pin Location	Pin Name	Pin Function	Description	SMARC Pin No.	SMARC Pin Name
AG23	P13_1/DISP_DATA13/CAN1_TX_DATARATE_EN/POE10_N/IRQ1	P13_1	Unused	—	—
AG26	P13_2/DISP_DATA14/CAN1_RX_DATARATE_EN/IRQ7/IRQ2	P13_2	Unused	—	—
AF27	P14_0/DISP_DATA15/SSI1_BCK/SD1_CD/MTCLKA	P14_0	Unused	—	—
AJ23	P14_1/DISP_DATA16/SSI1_RCK/SD1_WP/MTCLKB	P14_1	Unused	—	—
AH23	P15_0/DISP_DATA17/SSI1_TXD/GTIOC4A/MTCLKC	P15_0	Unused	—	—
AJ24	P15_1/DISP_DATA18/SSI1_RXD/GTIOC4B/MTCLKD	P15_1	Unused	—	—
AH24	P16_0/DISP_DATA19/SCIF2_TXD/GTIOC5A/IRQ3	P16_0	RAA215300	—	—
AJ25	P16_1/DISP_DATA20/SCIF2_RXD/GTIOC5B/IRQ4	P16_1	RAA215300	—	—
AH25	P17_0/DISP_DATA21/SCIF2_SCK/GTIOC6A/IRQ5	P17_0	Unused	—	—
AJ26	P17_1/DISP_DATA22/SCIF2_CTS/GTIOC6B/IRQ6	P17_1	Unused	—	—
AH26	P17_2/DISP_DATA23/SCIF2_RTS/IRQ7	P17_2	Unused	—	—
C2	P18_0/SD0_CD/GTIOC0A/RIIC3_SDA/MTIOC2A	RIIC3_SDA	RAA215300 and 5P35023 PMOD1 Type-6A and audio codec on the RZ SMARC Carrier	S49	I2C_GP_DAT
D3	P18_1/SD0_WP/GTIOC0B/RIIC3_SCL/MTIOC2B	RIIC3_SCL	RAA215300 and 5P35023 PMOD1 Type-6A and audio codec on the RZ SMARC Carrier	S48	I2C_GP_CK
B1	P19_0/SD1_CD/GTIOC3A/MTIOC1A/RIIC2_SDA	SD1_CD	microSD ch. 1 card slot on the RZ SMARC Carrier	P35	SDIO_CD#
B2	P19_1/SD1_WP/GTIOC3B/MTIOC1B/RIIC2_SCL	P19_1	Unused	P33	SDIO_WP
B13	P2_0/IRQ4/ADC_TRG/GTIOC2A/MTIOC1A/SCIF4_TXD	P2_0	24-pin FFC connector on the RZ SMARC Carrier	P109	GPIO1/CAM1_PWR#
A13	P2_1/IRQ5/GTIOC2B/MTIOC1B/SCIF4_RXD	IRQ5	MIPI-DSI-to-HDMI transmitter on the RZ SMARC Carrier	P110	GPIO2/CAM0_RST#

Table 4.1 List of Pin Function Selections (6/17)

Pin Location	Pin Name	Pin Function	Description	SMARC Pin No.	SMARC Pin Name
N1	P20_0/ET0_TXC_TX_CLK/RSPI0_CK/CAN_CLK	ET0_TXC_TX_CLK	Ethernet 0 PHY (KSZ9131RNXC)	—	—
N2	P20_1/ET0_TX_CTL_TX_EN/RSPI0_MOSI/CAN0_TX	ET0_TX_CTL_TX_EN	Ethernet 0 PHY (KSZ9131RNXC)	—	—
M1	P20_2/ET0_TXD0/RSPI0_MISO/CAN0_RX	ET0_TXD0	Ethernet 0 PHY (KSZ9131RNXC)	—	—
M2	P21_0/ET0_TXD1/RSPI0_SSL/CAN0_TX_DATARATE_EN	ET0_TXD1	Ethernet 0 PHY (KSZ9131RNXC)	—	—
L1	P21_1/ET0_TXD2/CAN0_RX_DATARATE_EN	ET0_TXD2	Ethernet 0 PHY (KSZ9131RNXC)	—	—
L2	P22_0/ET0_TXD3/SSI0_BCK/CAN1_TX/MTCLKA	ET0_TXD3	Ethernet 0 PHY (KSZ9131RNXC)	—	—
M3	P22_1/ET0_TX_ERR/SSI0_RCK/CAN1_RX/MTCLKB	ET0_TX_ERR	Unused	—	—
N4	P23_0/ET0_TX_COL/SSI0_TXD/CAN1_TX_DATARATE_EN/MTCLKC	ET0_TX_COL	Unused	—	—
M4	P23_1/ET0_TX_CRS/SSI0_RXD/CAN1_RX_DATARATE_EN/MTCLKD	ET0_TX_CRS	Unused	—	—
P2	P24_0/ET0_RXC_RX_CLK/SSI1_BCK/POE0_N	ET0_RXC_RX_CLK	Ethernet 0 PHY (KSZ9131RNXC)	—	—
P1	P24_1/ET0_RX_CTL_RX_DV/SSI1_RCK/POE4_N	ET0_RX_CTL_RX_DV	Ethernet 0 PHY (KSZ9131RNXC)	—	—
R2	P25_0/ET0_RXD0/SSI1_TXD/POE8_N	ET0_RXD0	Ethernet 0 PHY (KSZ9131RNXC)	—	—
R1	P25_1/ET0_RXD1/SSI1_RXD/POE10_N	ET0_RXD1	Ethernet 0 PHY (KSZ9131RNXC)	—	—
T2	P26_0/ET0_RXD2/RSPI1_CK/MTIOC8A	ET0_RXD2	Ethernet 0 PHY (KSZ9131RNXC)	—	—
T1	P26_1/ET0_RXD3/RSPI1_MOSI/MTIOC8B	ET0_RXD3	Ethernet 0 PHY (KSZ9131RNXC)	—	—
N3	P27_0/ET0_RX_ERR/RSPI1_MISO/MTIOC8C	ET0_RX_ERR	Unused	—	—
U2	P27_1/ET0_MDC/RSPI1_SSL/MTIOC8D	ET0_MDC	Ethernet 0 PHY (KSZ9131RNXC)	—	—
U1	P28_0/ET0_MDIO	ET0_MDIO	Ethernet 0 PHY (KSZ9131RNXC)	—	—
R3	P28_1/ET0_LINKSTA	ET0_LINKSTA	Ethernet 0 PHY (KSZ9131RNXC)	—	—

Table 4.1 List of Pin Function Selections (7/17)

Pin Location	Pin Name	Pin Function	Description	SMARC Pin No.	SMARC Pin Name
AB2	P29_0/ET1_TXC_TX_CLK/CAM_PCLK/USB1_VBUSEN/SSI2_BCK	ET1_TXC_TX_CLK	Ethernet 0 PHY (KSZ9131RNXC)	—	—
Y1	P29_1/ET1_TX_CTL_TX_EN/CAM_HREF/USB1_OVRCUR/SSI2_RCK	ET1_TX_CTL_TX_EN	Ethernet 0 PHY (KSZ9131RNXC)	—	—
A14	P3_0/IRQ6/RIIC2_SDA/GTIOC3A/MTIOC2A/SCIF4_SCK	P3_0/IRQ6	Unused	P108	GPIO0/CAM0_PWR#
B14	P3_1/IRQ7/RIIC2_SCL/GTIOC3B/MTIOC2B/CAM_FIELD	P3_1/IRQ7	PMOD1 Type-3A on the RZ SMARC Carrier	P118	GPIO10
AB1	P30_0/ET1_TXD0/CAM_VSYNC/SSI2_DATA	ET1_TXD0	Ethernet 1 PHY (KSZ9131RNXC)	—	—
AA2	P30_1/ET1_TXD1/CAM_DATA15	ET1_TXD1	Ethernet 1 PHY (KSZ9131RNXC)	—	—
AA1	P31_0/ET1_TXD2/CAM_DATA0/SCI1_RXD/SSI3_BCK	ET1_TXD2	Ethernet 1 PHY (KSZ9131RNXC)	—	—
Y2	P31_1/ET1_TXD3/CAM_DATA1/SCI1_TXD/SSI3_RCK	ET1_TXD3	Ethernet 1 PHY (KSZ9131RNXC)	—	—
U3	P32_0/ET1_TX_ERR/CAM_DATA2/SCI1_SCK/MTIOC3A/SSI3_TXD	ET1_TX_ERR	Unused	—	—
V4	P32_1/ET1_TX_COL/CAM_DATA3/SCI1_CTS_N_RTS_N/MTIOC3B/SSI3_RXD	ET1_TX_COL	Unused	—	—
U4	P33_0/ET1_TX_CRS/CAM_DATA4/GTIOC2A/SCIF2_TXD/GTIOC0A	ET1_TX_CRS	Unused	—	—
AC1	P33_1/ET1_RXC_RX_CLK/CAM_DATA5/GTIOC2B/SCIF2_RXD/GTIOC0B	ET1_RXC_RX_CLK	Ethernet 1 PHY (KSZ9131RNXC)	—	—
AC2	P34_0/ET1_RX_CTL_RX_DV/CAM_DATA6/GTIOC3A/MTIOC0A/GTIOC1A	ET1_RX_CTL_RX_DV	Ethernet 1 PHY (KSZ9131RNXC)	—	—
AC3	P34_1/ET1_RXD0/CAM_DATA7/GTIOC3B/MTIOC0B/GTIOC1B	ET1_RXD0	Ethernet 1 PHY (KSZ9131RNXC)	—	—
AC4	P35_0/ET1_RXD1/CAM_DATA8/SSI0_BCK/MTIOC0C/GTIOC2A	ET1_RXD1	Ethernet 1 PHY (KSZ9131RNXC)	—	—

Table 4.1 List of Pin Function Selections (8/17)

Pin Location	Pin Name	Pin Function	Description	SMARC Pin No.	SMARC Pin Name
AB4	P35_1/ET1_RXD2/CAM_DATA9/SSI0_RCK/MTIOC0D/GTIOC2B	ET1_RXD2	Ethernet 1 PHY (KSZ9131RNXC)	—	—
AB3	P36_0/ET1_RXD3/CAM_DATA10/SSI0_TXD/MTIOC3C/GTETRGA	ET1_RXD3	Ethernet 1 PHY (KSZ9131RNXC)	—	—
V3	P36_1/ET1_RX_ERR/CAM_DATA11/SSI0_RXD/MTIOC3D/GTETRGB	ET1_RX_ERR	Unused	—	—
W2	P37_0/ET1_MDC/CAM_DATA12/SCIF2_SCK/GTETRGC	ET1_MDC	Ethernet 1 PHY (KSZ9131RNXC)	—	—
W1	P37_1/ET1_MDIO/CAM_DATA13/SCIF2_CTS/GTETRGD	ET1_MDIO	Ethernet 1 PHY (KSZ9131RNXC)	—	—
V2	P37_2/ET1_LINKSTA/CAM_DATA14/SCIF2_RTS	ET1_LINKSTA	Ethernet 1 PHY (KSZ9131RNXC)	—	—
A15	P38_0/SCIF0_TXD/GTETRGA/CAN_CLK/MTIOC4A/USB1_VBUSEN	SCIF0_TXD	Debug UART on the RZ SMARC Carrier	P140	SER3_TX
B15	P38_1/SCIF0_RXD/GTETRGB/CAN0_TX/MTIOC4B/USB1_OVRCUR	SCIF0_RXD	Debug UART on the RZ SMARC Carrier	P141	SER3_RX
A16	P39_0/SCIF0_SCK/GTETRGC/CAN0_RX/MTIOC4C	P39_0	For selecting the voltage of the microSD ch. 0 card	—	—
C15	P39_1/SCIF0_CTS/GTETRGD/CAN0_TX_DATARATE_EN/MTIOC4D	P39_1	RAA215300 For selecting the voltage of the microSD ch. 1 card on the RZ SMARC Carrier	—	—
B16	P39_2/SCIF0_RTS/CAN0_RX_DATARATE_EN	P39_2	microSD ch. 1 card slot on the RZ SMARC Carrier For switching the power of the card slot on or off	P37	SDIO_PWR_EN
AJ5	P4_0/USB0_VBUSEN/SCIF2_TXD/MTIOC7A/ADC_TRG	USB0_VBUSEN	USB2.0 OTG on the RZ SMARC Carrier Include the gate USB0_VBUSEN state	P62	USB0_EN_OC#
AH6	P4_1/SCIF2_RXD/MTIOC7B	P4_1	microSD ch. 0 card slot For switching the power of the card slot on or off	P108	—
C17	P40_0/SCIF1_TXD/GTIOC6A/CAN1_TX/MTIC5U/SCI0_RXD	SCIF1_TXD	Unused	P134	SER1_TX
B17	P40_1/SCIF1_RXD/GTIOC6B/CAN1_RX/MTIC5V/SCI0_TXD	SCIF1_RXD	Unused	P135	SER1_RX
A17	P40_2/SCIF1_SCK/CAN1_TX_DATARATE_EN/MTIC5W/SCI0_SCK	P40_2	24-pin FFC connector on the RZ SMARC Carrier	P111	GPIO3/CAM1_RST#

Table 4.1 List of Pin Function Selections (9/17)

Pin Location	Pin Name	Pin Function	Description	SMARC Pin No.	SMARC Pin Name
E17	P41_0/SCIF1_CTS/GTIOC7A/CAN1_RX_DATARATE_EN/GTIOC3A/SCI0_CTS_N_RTS_N	P41_0	PMOD0 Type-2A on the RZ SMARC Carrier	P114	GPIO6/TACHIN
A18	P41_1/SCIF1_RTS/GTIOC7B/GTIOC3B	P41_1	For selecting the device connected to the SD/MMC ch0 interface	P113	—
AG4	P42_0/USB1_VBUSEN/RSPI2_CK/CAN_CLK/SCIF2_TXD/MTIOC7A	USB1_VBUSEN	USB2.0 Host on the RZ SMARC Carrier Include the gate USB1_VBUSEN state	P67	USB1_EN_OC#
AE7	P42_1/USB1_OVRCUR/RSPI2_MOSI/CAN0_TX/SCIF2_RXD/MTIOC7B	USB1_OVRCUR	USB2.0 Host on the RZ SMARC Carrier Include the gate USB1_OVRCUR state	P67	USB1_EN_OC#
AJ3	P42_2/ADC_TRG/RSPI2_MISO/CAN0_RX/SCIF2_SCK/MTIOC7C	P42_2	CAN transceiver ch. 0*[2] or PMOD1 Type-6A on the RZ SMARC Carrier	P116	GPIO8
AH3	P42_3/RIIC2_SDA/RSPI2_SSL/CAN0_TX_DATARATE_EN/SCIF2_CTS/MTIOC7D	P42_3	CAN transceiver ch. 1*[2] or PMOD1 Type-6A on the RZ SMARC Carrier	P117	GPIO9
AC5	P42_4/RIIC2_SCL/CAM_FIELD/CAN0_RX_DATARATE_EN/SCIF2_RTS	P42_4	PMOD1 Type-6A on the RZ SMARC Carrier	S142	GPIO12
B18	P43_0/RSPI0_CK/GTIOC4A/GTIOC6A/IRQ4/MTIOC8A	P43_0/IRQ4	PMOD0 Type-2A on the RZ SMARC Carrier	P112	GPIO4/HDA_RST#
D17	P43_1/RSPI0_MOSI/GTIOC4B/GTIOC6B/IRQ5/MTIOC8B	P43_1	PMOD0 Type-2A on the RZ SMARC Carrier	P115	GPIO7
E18	P43_2/RSPI0_MISO/GTIOC5A/IRQ6/MTIOC8C	P43_2	PMOD0 Type-2A on the RZ SMARC Carrier	P113	GPIO5/PWM_OUT#
C18	P43_3/RSPI0_SSL/GTIOC5B/IRQ7/MTIOC8D	P43_3	Unused	—	—
A19	P44_0/RSPI1_CK/SSI1_BCK/CAN1_TX/MTIOC3A/GTIOC6A	RSPI1_CK	PMOD0 Type-2A on the RZ SMARC Carrier	P56	SPI1_Clock
F17	P44_1/RSPI1_MOSI/SSI1_RCK/CAN1_RX/MTIOC3B/GTIOC6B	RSPI1_MOSI	PMOD0 Type-2A on the RZ SMARC Carrier	P57	SPI1_DIN
D18	P44_2/RSPI1_MISO/SSI1_TXD/CAN1_TX_DATARATE_EN/MTIOC3C/GTIOC7A	RSPI1_MISO	PMOD0 Type-2A on the RZ SMARC Carrier	P58	SPI1_DO
B19	P44_3/RSPI1_SSL/SSI1_RXD/CAN1_RX_DATARATE_EN/MTIOC3D/GTIOC7B	RSPI1_SSL	PMOD0 Type-2A on the RZ SMARC Carrier	P54	SPI1_CS0#
A8	P45_0/SSI0_BCK/POE0_N/SCI1_RXD	SSI0_BCK	Audio codec on the RZ SMARC Carrier	S42	I2S0_CK

Table 4.1 List of Pin Function Selections (10/17)

Pin Location	Pin Name	Pin Function	Description	SMARC Pin No.	SMARC Pin Name
D12	P45_1/SSI0_RCK/POE4_N/SCI1_TXD	SSI0_RCK	Audio codec on the RZ SMARC Carrier	S39	I2S0_LRCK
A9	P45_2/SSI0_TXD/POE8_N/SCI1_SCK	SSI0_TXD	Audio codec on the RZ SMARC Carrier	S40	I2S0_SDOUT
B9	P45_3/SSI0_RXD/POE10_N/SCI1_CTS_N_RTS_N	SSI0_RXD	Audio codec on the RZ SMARC Carrier	S41	I2S0_SDIN
B10	P46_0/SSI1_BCK/GTETRGA/CAN1_TX/RIIC2_SDA	SSI1_BCK	MIPI-DSI-to-HDMI transmitter on the RZ SMARC Carrier	S53	I2S2_CK
A10	P46_1/SSI1_RCK/GTETRGB/CAN1_RX/RIIC2_SCL	SSI1_RCK	MIPI-DSI-to-HDMI transmitter on the RZ SMARC Carrier	S50	I2S2_LRCK
C12	P46_2/SSI1_TXD/GTETRGC/CAN1_TX_DATARATE_EN/RIIC3_SDA	SSI1_TXD	MIPI-DSI-to-HDMI transmitter on the RZ SMARC Carrier	S51	I2S2_SDOUT
D13	P46_3/SSI1_RXD/GTETRGD/CAN1_RX_DATARATE_EN/RIIC3_SCL	SSI1_RXD	Unused	S52	I2S2_SDIN
B20	P47_0/SCI0_RXD/SD0_CD/IRQ0/SSI1_BCK/RSPI0_CK	SD0_CD	microSD ch. 0 card slot	—	—
A20	P47_1/SCI0_TXD/SD0_WP/IRQ1/SSI1_RCK/RSPI0_MOSI	P47_1	Unused	—	—
A21	P47_2/SCI0_SCK/SD1_CD/IRQ2/SSI1_TXD/RSPI0_MISO	P47_2	PMOD1 Type-6A on the RZ SMARC Carrier	S123	GPIO13
B21	P47_3/SCI0_CTS_N_RTS_N/SD1_WP/IRQ3/SSI1_RXD/RSPI0_SSL	P47_3	Unused	P118	—
B22	P48_0/SCIF2_TXD/RSPI1_CK/RIIC2_SDA/MTCLKA	SCIF2_TXD	PMOD1 Type-3A on the RZ SMARC Carrier	P129	SER0_TX
A23	P48_1/SCIF2_RXD/RSPI1_MOSI/RIIC2_SCL/MTCLKB	SCIF2_RXD	PMOD1 Type-3A on the RZ SMARC Carrier	P130	SER0_RX
A22	P48_2/SCIF2_SCK/RSPI1_MISO/RIIC3_SDA/MTCLKC	P48_2	Unused	—	—
C22	P48_3/SCIF2_CTS/RSPI1_SSL/RIIC3_SCL/MTCLKD	SCIF2_CTS	PMOD1 Type-3A on the RZ SMARC Carrier	P132	SER0_CTS#
B23	P48_4/SCIF2_RTS/ADC_TRG	SCIF2_RTS	PMOD1 Type-3A on the RZ SMARC Carrier	P131	SER0_RTS#
AJ4	P5_0/USB0_OVRCUR/SCIF2_SCK/MTIOC7C/SSI2_BCK	USB0_OVRCUR	USB2.0 OTG on the RZ SMARC Carrier include the gate USB0_OVRCUR state	P62	USB0_EN_OC#

Table 4.1 List of Pin Function Selections (11/17)

Pin Location	Pin Name	Pin Function	Description	SMARC Pin No.	SMARC Pin Name
AH4	P5_1/USB0_OTG_ID/SCIF2_CTS/MTIOC7D/SSI2_RCK	USB0_OTG_ID	USB2.0 OTG on the RZ SMARC Carrier USB_OTG_ID state	P64	USB0_OTG_ID
AH5	P5_2/USB0_OTG_EXICEN/SCIF2_RTS/SSI2_DATA	P5_2	PMOD1 Type-3A on the RZ SMARC Carrier	P119	GPIO11
AJ27	P6_0/DISP_CLK/SSI0_BCK/USB0_VBUSEN/MTIOC1A	P6_0	Unused	—	—
AH27	P6_1/DISP_HSYNC/SSI0_RCK/MTIOC1B	P6_1	Unused	—	—
AJ28	P7_0/DISP_VSYNC/SSI0_TXD/USB0_OVRCUR/MTIC5U	P7_0	Unused	—	—
AH28	P7_1/DISP_DE/SSI0_RXD/USB0_OTG_ID/MTIC5V	P7_1	Unused	—	—
AJ19	P7_2/DISP_DATA0/USB0_OTG_EXICEN/MTIC5W	P7_2	Unused	—	—
AH19	P8_0/DISP_DATA1/USB1_VBUSEN/RSPI2_CK/RIIC3_SCL	P8_0	Unused	—	—
AJ20	P8_1/DISP_DATA2/USB1_OVRCUR/RSPI2_MOSI/RIIC3_SDA	P8_1	Unused	—	—
AH20	P8_2/DISP_DATA3/RSPI2_MISO	P8_2	Unused	—	—
AJ21	P9_0/DISP_DATA4/ADC_TRG/RSPI2_SSL/MTIOC2A	ADC_TRG	Pin header CN1 for ADC input	—	—
AH21	P9_1/DISP_DATA5/MTIOC2B	P9_1	Unused	—	—
N7	PLL1_AVDD18	PLL1_AVDD18	1.8 V	—	—
W9	PLL23_AVDD18	PLL23_AVDD18	1.8 V	—	—
V5	PLL23_DVDD11	PLL23_DVDD11	1.1 V	—	—
U23	PLL4_AVDD18	PLL4_AVDD18	1.8 V	—	—
AA15	PLL5_DVDD11	PLL5_DVDD11	1.1 V	—	—
G13	PLL6_AVDD18	PLL6_AVDD18	1.8 V	—	—
AF3	PRST#	PRST#	Input system reset signal from RAA215300	—	—
AC7	PVDD	PVDD	3.3 V	—	—
AC12	PVDD	PVDD	3.3 V	—	—
AC22	PVDD	PVDD	3.3 V	—	—
AC23	PVDD	PVDD	3.3 V	—	—
H7	PVDD	PVDD	3.3 V	—	—
E13	PVDD	PVDD	3.3 V	—	—
G18	PVDD	PVDD	3.3 V	—	—
G23	PVDD	PVDD	3.3 V	—	—

Table 4.1 List of Pin Function Selections (12/17)

Pin Location	Pin Name	Pin Function	Description	SMARC Pin No.	SMARC Pin Name
B6	QSPI_INT#	QSPI_INT#	Connected to a pull-up resistor by the SPI_PVDD power supply*[1]	—	—
A5	QSPI_RESET#	QSPI_RESET#	QSPI flash memory (MT25QU512ABB8E12-0SIT)	—	—
B5	QSPI_WP#	QSPI_WP#	Unused	—	—
A3	QSPI0_IO0	QSPI0_IO0	QSPI flash memory (MT25QU512ABB8E12-0SIT)	—	—
B3	QSPI0_IO1	QSPI0_IO1	QSPI flash memory (MT25QU512ABB8E12-0SIT)	—	—
A4	QSPI0_IO2	QSPI0_IO2	QSPI flash memory (MT25QU512ABB8E12-0SIT)	—	—
B4	QSPI0_IO3	QSPI0_IO3	QSPI flash memory (MT25QU512ABB8E12-0SIT)	—	—
C4	QSPI0_SPCLK	QSPI0_SPCLK	QSPI flash memory (MT25QU512ABB8E12-0SIT)	—	—
A2	QSPI0_SSL	QSPI0_SSL	QSPI flash memory (MT25QU512ABB8E12-0SIT)	—	—
C7	QSPI1_IO0	QSPI1_IO0	Unused	—	—
D7	QSPI1_IO1	QSPI1_IO1	Unused	—	—
A6	QSPI1_IO2	QSPI1_IO2	Unused	—	—
D8	QSPI1_IO3	QSPI1_IO3	Unused	—	—
B7	QSPI1_SPCLK	QSPI1_SPCLK	Unused	—	—
C8	QSPI1_SSL	QSPI1_SSL	Unused	—	—
B24	RIIC0_SCL	RIIC0_SCL	24-pin FFC connector on the RZ SMARC Carrier	S1	I2C_CAM1_CK
A25	RIIC0_SDA	RIIC0_SDA	24-pin FFC connector on the RZ SMARC Carrier	S2	I2C_CAM1_DAT
C23	RIIC1_SCL	RIIC1_SCL	MIPI-DSI-to-HDMI transmitter on the RZ SMARC Carrier	S139	I2C_LCD_CK
A24	RIIC1_SDA	RIIC1_SDA	MIPI-DSI-to-HDMI transmitter on the RZ SMARC Carrier	S140	I2C_LCD_DAT
F1	SD0_CLK	SD0_CLK	eMMC memory (MTFC64GASAQHD-IT) or microSD ch. 0 card slot	—	—
F2	SD0_CMD	SD0_CMD	eMMC memory (MTFC64GASAQHD-IT)	—	—
G2	SD0_DATA0	SD0_DATA0	eMMC memory (MTFC64GASAQHD-IT)	—	—
H4	SD0_DATA1	SD0_DATA1	eMMC memory (MTFC64GASAQHD-IT)	—	—
G3	SD0_DATA2	SD0_DATA2	eMMC memory (MTFC64GASAQHD-IT) or microSD ch. 0 card slot	—	—
G4	SD0_DATA3	SD0_DATA3	eMMC memory (MTFC64GASAQHD-IT) or microSD ch. 0 card slot	—	—
E1	SD0_DATA4	SD0_DATA4	eMMC memory (MTFC64GASAQHD-IT)	—	—
D1	SD0_DATA5	SD0_DATA5	eMMC memory (MTFC64GASAQHD-IT)	—	—
E2	SD0_DATA6	SD0_DATA6	eMMC memory (MTFC64GASAQHD-IT)	—	—
D2	SD0_DATA7	SD0_DATA7	eMMC memory (MTFC64GASAQHD-IT)	—	—

Table 4.1 List of Pin Function Selections (13/17)

Pin Location	Pin Name	Pin Function	Description	SMARC Pin No.	SMARC Pin Name
H5	SD0_PVDD	SD0_PVDD	1.8 V/3.3 V	—	—
C1	SD0_RST#	SD0_RST#	eMMC memory (MTFC64GASAQHD-IT)	—	—
H3	SD1_CLK	SD1_CLK	microSD ch. 1 card slot on the RZ SMARC Carrier	P36	SDIO_CK
J2	SD1_CMD	SD1_CMD	microSD ch. 1 card slot on the RZ SMARC Carrier	P34	SDIO_CMD
H1	SD1_DATA0	SD1_DATA0	microSD ch. 1 card slot on the RZ SMARC Carrier	P39	SDIO_D0
H2	SD1_DATA1	SD1_DATA1	microSD ch. 1 card slot on the RZ SMARC Carrier	P40	SDIO_D1
K2	SD1_DATA2	SD1_DATA2	microSD ch. 1 card slot on the RZ SMARC Carrier	P41	SDIO_D2
J1	SD1_DATA3	SD1_DATA3	microSD ch. 1 card slot on the RZ SMARC Carrier	P42	SDIO_D3
M6	SD1_PVDD	SD1_PVDD	1.8 V/3.3 V	—	—
F8	SPI_PVDD	SPI_PVDD	1.8 V	—	—
AE1	TCK/SWDCLK	TCK/SWDCLK	Connected to the JTAG connector (CN2)	—	—
AF1	TDI	TDI	Connected to the JTAG connector (CN2)	—	—
AE2	TDO	TDO	Connected to the JTAG connector (CN2)	—	—
AD18	VSS	VSS	GND	—	—
AD2	TMS/SWDIO	TMS/SWDIO	Connected to the JTAG connector (CN2)	—	—
AF2	TRST#	TRST#	Connected to the JTAG connector (CN2)	—	—
AB7	VDD18	VDD18	1.8 V	—	—
AG8	USB_AVDD18	USB_AVDD18	1.8 V	—	—
AG7	USB_RREF	USB_RREF	Connected to GND via the 1.8-Ω resistor	—	—
AF7	USB_VDD18	USB_VDD18	1.8 V	—	—
AF8	USB_VDD18	USB_VDD18	1.8 V	—	—
AD8	USB_VDD33	USB_VDD33	3.3 V	—	—
AE8	USB_VDD33	USB_VDD33	3.3 V	—	—
AJ6	VSS	VSS	GND	—	—
AH7	VSS	VSS	GND	—	—
AC8	VSS	VSS	GND	—	—
AJ9	VSS	VSS	GND	—	—
AJ8	USB0_DM	USB0_DM	USB2.0 OTG on the RZ SMARC Carrier	P61	USB0-
AH9	USB0_DP	USB0_DP	USB2.0 OTG on the RZ SMARC Carrier	P60	USB0+
AH10	USB0_VBUSIN	USB0_VBUSIN	USB2.0 OTG on the RZ SMARC Carrier	P63	USB0_VBUS_DET
AJ7	USB1_DM	USB1_DM	USB2.0 Host on the RZ SMARC Carrier	P66	USB1-
AH8	USB1_DP	USB1_DP	USB2.0 Host on the RZ SMARC Carrier	P65	USB1+
J9	VDD	VDD	1.1 V	—	—
L9	VDD	VDD	1.1 V	—	—
N9	VDD	VDD	1.1 V	—	—
R9	VDD	VDD	1.1 V	—	—
U9	VDD	VDD	1.1 V	—	—
AA9	VDD	VDD	1.1 V	—	—

Table 4.1 List of Pin Function Selections (14/17)

Pin Location	Pin Name	Pin Function	Description	SMARC Pin No.	SMARC Pin Name
K10	VDD	VDD	1.1 V	—	—
M10	VDD	VDD	1.1 V	—	—
P10	VDD	VDD	1.1 V	—	—
T10	VDD	VDD	1.1 V	—	—
V10	VDD	VDD	1.1 V	—	—
Y10	VDD	VDD	1.1 V	—	—
J11	VDD	VDD	1.1 V	—	—
AA11	VDD	VDD	1.1 V	—	—
K12	VDD	VDD	1.1 V	—	—
Y12	VDD	VDD	1.1 V	—	—
J13	VDD	VDD	1.1 V	—	—
AA13	VDD	VDD	1.1 V	—	—
K14	VDD	VDD	1.1 V	—	—
Y14	VDD	VDD	1.1 V	—	—
J15	VDD	VDD	1.1 V	—	—
K16	VDD	VDD	1.1 V	—	—
Y16	VDD	VDD	1.1 V	—	—
J17	VDD	VDD	1.1 V	—	—
AA17	VDD	VDD	1.1 V	—	—
K18	VDD	VDD	1.1 V	—	—
Y18	VDD	VDD	1.1 V	—	—
J19	VDD	VDD	1.1 V	—	—
AA19	VDD	VDD	1.1 V	—	—
K20	VDD	VDD	1.1 V	—	—
M20	VDD	VDD	1.1 V	—	—
P20	VDD	VDD	1.1 V	—	—
T20	VDD	VDD	1.1 V	—	—
V20	VDD	VDD	1.1 V	—	—
Y20	VDD	VDD	1.1 V	—	—
J21	VDD	VDD	1.1 V	—	—
L21	VDD	VDD	1.1 V	—	—
N21	VDD	VDD	1.1 V	—	—
R21	VDD	VDD	1.1 V	—	—
U21	VDD	VDD	1.1 V	—	—
W21	VDD	VDD	1.1 V	—	—
AA21	VDD	VDD	1.1 V	—	—
A1	VSS	VSS	GND	—	—
G1	VSS	VSS	GND	—	—
K1	VSS	VSS	GND	—	—
V1	VSS	VSS	GND	—	—

Table 4.1 List of Pin Function Selections (15/17)

Pin Location	Pin Name	Pin Function	Description	SMARC Pin No.	SMARC Pin Name
AD1	VSS	VSS	GND	—	—
AJ1	VSS	VSS	GND	—	—
AH2	VSS	VSS	GND	—	—
G5	VSS	VSS	GND	—	—
M5	VSS	VSS	GND	—	—
N5	VSS	VSS	GND	—	—
U5	VSS	VSS	GND	—	—
AB5	VSS	VSS	GND	—	—
H6	VSS	VSS	GND	—	—
U6	VSS	VSS	GND	—	—
V6	VSS	VSS	GND	—	—
AB6	VSS	VSS	GND	—	—
A7	VSS	VSS	GND	—	—
M7	VSS	VSS	GND	—	—
G8	VSS	VSS	GND	—	—
AJ10	VSS	VSS	GND	—	—
L11	VSS	VSS	GND	—	—
N11	VSS	VSS	GND	—	—
R11	VSS	VSS	GND	—	—
U11	VSS	VSS	GND	—	—
W11	VSS	VSS	GND	—	—
F12	VSS	VSS	GND	—	—
M12	VSS	VSS	GND	—	—
P12	VSS	VSS	GND	—	—
T12	VSS	VSS	GND	—	—
V12	VSS	VSS	GND	—	—
AE12	VSS	VSS	GND	—	—
AF12	VSS	VSS	GND	—	—
F13	VSS	VSS	GND	—	—
L13	VSS	VSS	GND	—	—
N13	VSS	VSS	GND	—	—
R13	VSS	VSS	GND	—	—
U13	VSS	VSS	GND	—	—
W13	VSS	VSS	GND	—	—
AE13	VSS	VSS	GND	—	—
AF13	VSS	VSS	GND	—	—

Table 4.1 List of Pin Function Selections (16/17)

Pin Location	Pin Name	Pin Function	Description	SMARC Pin No.	SMARC Pin Name
M14	VSS	VSS	GND	—	—
P14	VSS	VSS	GND	—	—
T14	VSS	VSS	GND	—	—
V14	VSS	VSS	GND	—	—
L15	VSS	VSS	GND	—	—
N15	VSS	VSS	GND	—	—
R15	VSS	VSS	GND	—	—
U15	VSS	VSS	GND	—	—
W15	VSS	VSS	GND	—	—
AG15	VSS	VSS	GND	—	—
M16	VSS	VSS	GND	—	—
P16	VSS	VSS	GND	—	—
T16	VSS	VSS	GND	—	—
V16	VSS	VSS	GND	—	—
L17	VSS	VSS	GND	—	—
N17	VSS	VSS	GND	—	—
R17	VSS	VSS	GND	—	—
U17	VSS	VSS	GND	—	—
W17	VSS	VSS	GND	—	—
AD17	VSS	VSS	GND	—	—
AE17	VSS	VSS	GND	—	—
AF17	VSS	VSS	GND	—	—
F18	VSS	VSS	GND	—	—
M18	VSS	VSS	GND	—	—
P18	VSS	VSS	GND	—	—
T18	VSS	VSS	GND	—	—
V18	VSS	VSS	GND	—	—
AF18	VSS	VSS	GND	—	—
L19	VSS	VSS	GND	—	—
N19	VSS	VSS	GND	—	—
R19	VSS	VSS	GND	—	—
U19	VSS	VSS	GND	—	—
W19	VSS	VSS	GND	—	—
F22	VSS	VSS	GND	—	—
G22	VSS	VSS	GND	—	—
AD22	VSS	VSS	GND	—	—
V23	VSS	VSS	GND	—	—
H24	VSS	VSS	GND	—	—
U24	VSS	VSS	GND	—	—
V24	VSS	VSS	GND	—	—

Table 4.1 List of Pin Function Selections (17/17)

Pin Location	Pin Name	Pin Function	Description	SMARC Pin No.	SMARC Pin Name
G25	VSS	VSS	GND	—	—
AC25	VSS	VSS	GND	—	—
G26	VSS	VSS	GND	—	—
H26	VSS	VSS	GND	—	—
M26	VSS	VSS	GND	—	—
N26	VSS	VSS	GND	—	—
U26	VSS	VSS	GND	—	—
V26	VSS	VSS	GND	—	—
AB27	VSS	VSS	GND	—	—
D28	VSS	VSS	GND	—	—
R28	VSS	VSS	GND	—	—
AA28	VSS	VSS	GND	—	—
AD28	VSS	VSS	GND	—	—
AG28	VSS	VSS	GND	—	—
A29	VSS	VSS	GND	—	—
U29	VSS	VSS	GND	—	—
Y29	VSS	VSS	GND	—	—
AJ29	VSS	VSS	GND	—	—
D22	WDTOVF_ PERROUT#	WDTOVF_ PERROUT#	Input hardware reset signal from RAA215300	—	—
AH1	XIN	XIN	GND	—	—
AG1	XOUT	XOUT	Open	—	—

NOTES

1. This pin is treated as open-circuit in the schematic, but this is incorrect.
2. The CAN connector is implemented on the RZ SMARC Carrier, but it is not available as a CAN-FD interface because a CAN transceiver is not fitted on this board.
   The following carrier boards are equipped with a CAN transceiver and the CAN-FD interface is already available.
   S.LOT# in the outer box label: 000251812 or later
   S.LOT# label on the carrier board: 251812 or later

4.2 Memory

QSPI flash memory and DDR4 SDRAM are mounted on the RZ/G2L SMARC Module as external memory.

Please refer to the following for details.

4.2.1 QSPI Flash Memory

Figure 4.1 shows a block diagram of the serial flash memory interface.

The QSPI flash memory is controlled by the SPI multi-I/O bus controller (SPIBSC) of the RZ/G2L. This flash memory defaults to standard SPI mode and supports both single data rate (SDR) and double data rate (DDR) transfers at clock frequencies of 66 MHz and 50 MHz.

NOTE

For the pull-up resistor of the clock line "RZ_QSPI0_SPCLK", place it wherever you want.

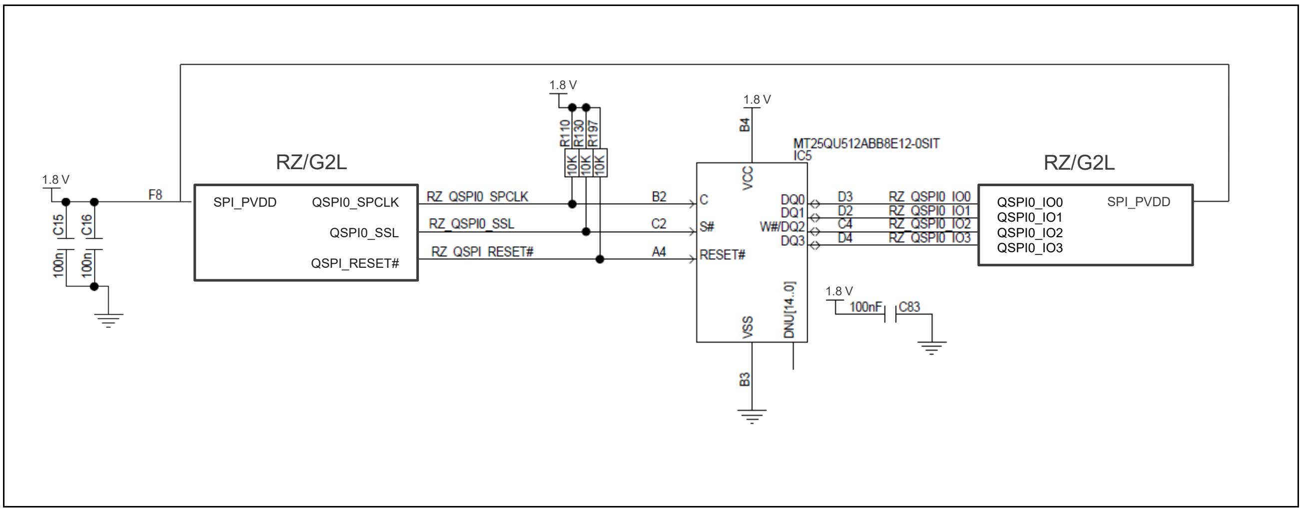


Figure 4.1 Block Diagram of Serial Flash Memory I/F

4.2.2 DDR4 SDRAM

Figure 4.2 shows a block diagram of the DDR4 SDRAM interface.

The DDR4 SDRAM is controlled by the memory controller (MEMC) of the RZ/G2L. It supports a data bus width of 16 bits, a data transfer rate of 1600 Mbps, and inline ECC.

This interface complies with JEDEC STANDARD JESD79-4C.

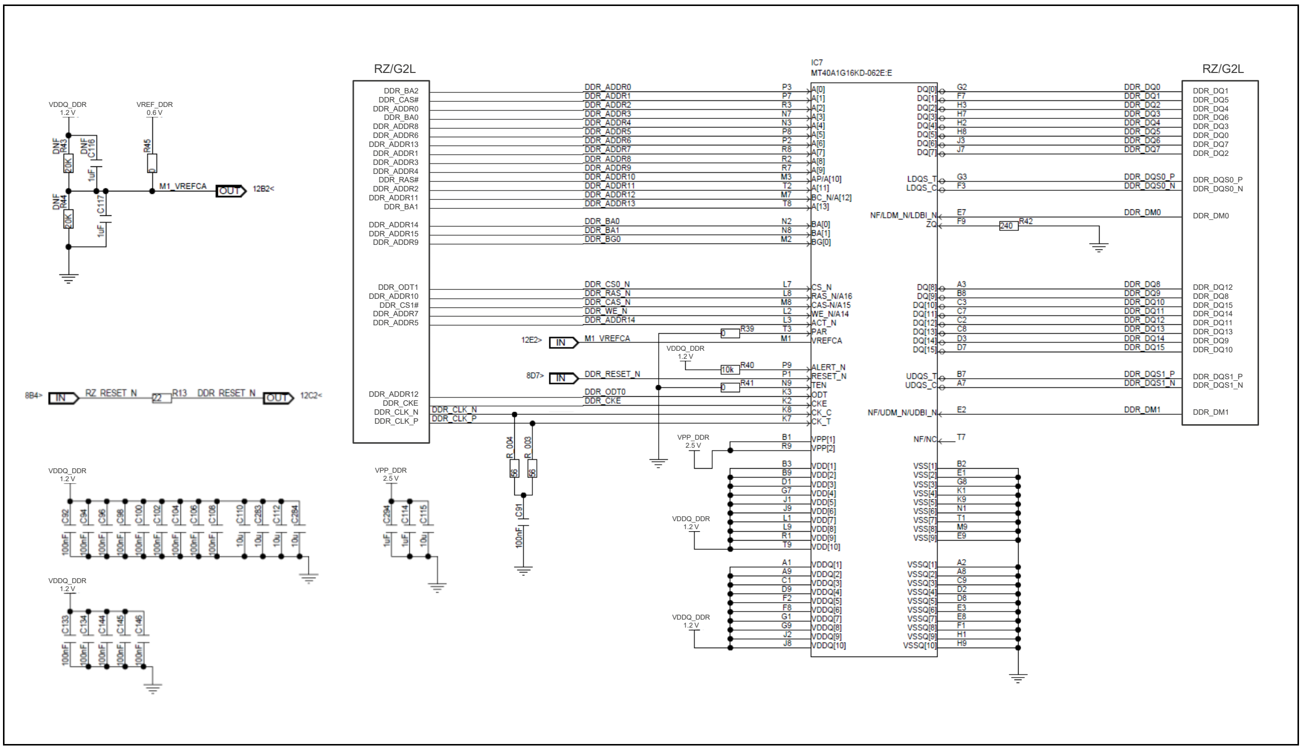


Figure 4.2 Block Diagram of DDR4 SDRAM I/F

4.3 Gigabit Ethernet Interface

Figure 4.3 and **Figure 4.4** show block diagrams of the Gigabit Ethernet 0 and Ethernet 1 interfaces.

The Gigabit Ethernet interface is controlled by the Ethernet controller (E-MAC) of the RZ/G2L. The Ethernet clock is sourced from a clock generator connected to the Ethernet PHY.

This interface complies with IEEE802.3 PHY RGMII.

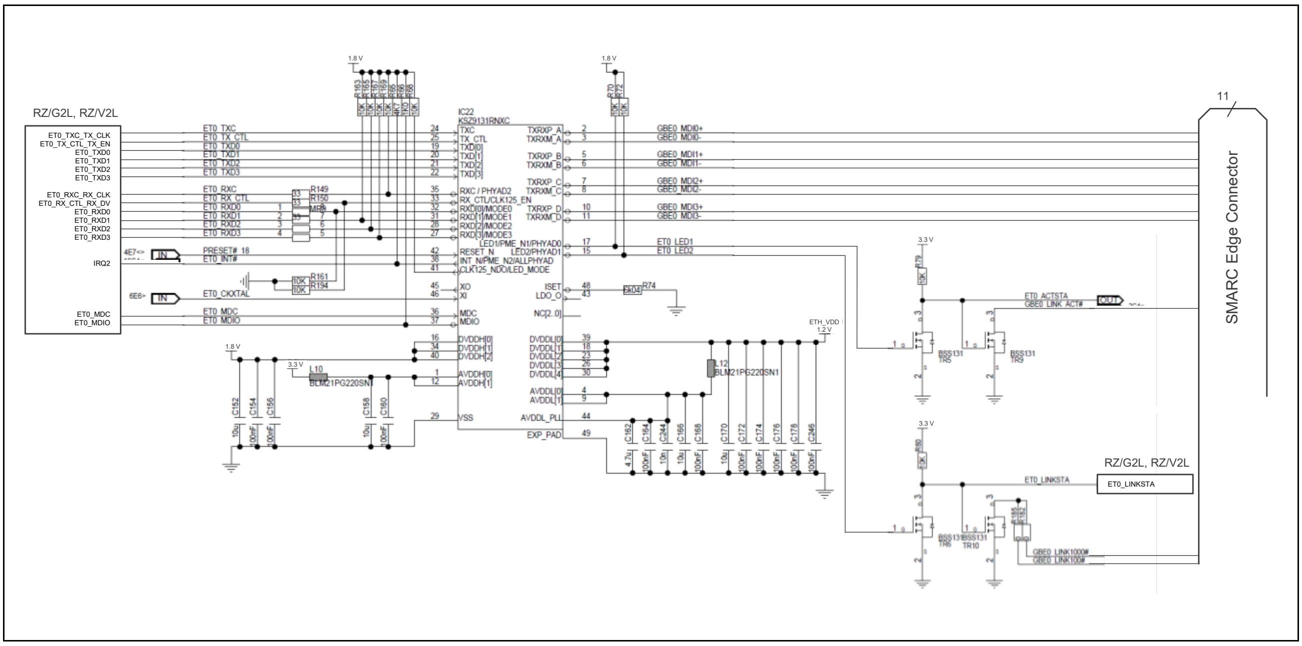


Figure 4.3 Block Diagram of Gigabit Ethernet 0 I/F

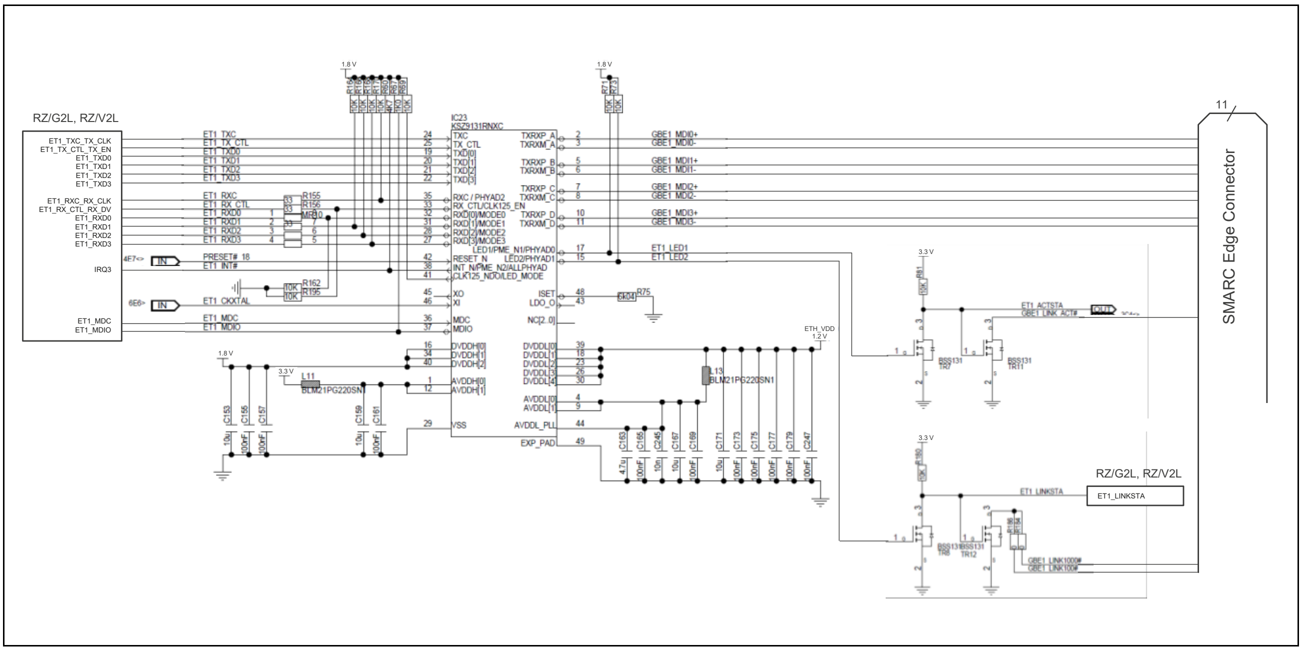


Figure 4.4 Block Diagram of Gigabit Ethernet 1 I/F

4.4 ADC Interface

Figure 4.5 shows a block diagram of the ADC interface.

The 10-pin connector is implemented on this board and the 6-channel input can be used as an analog signal.

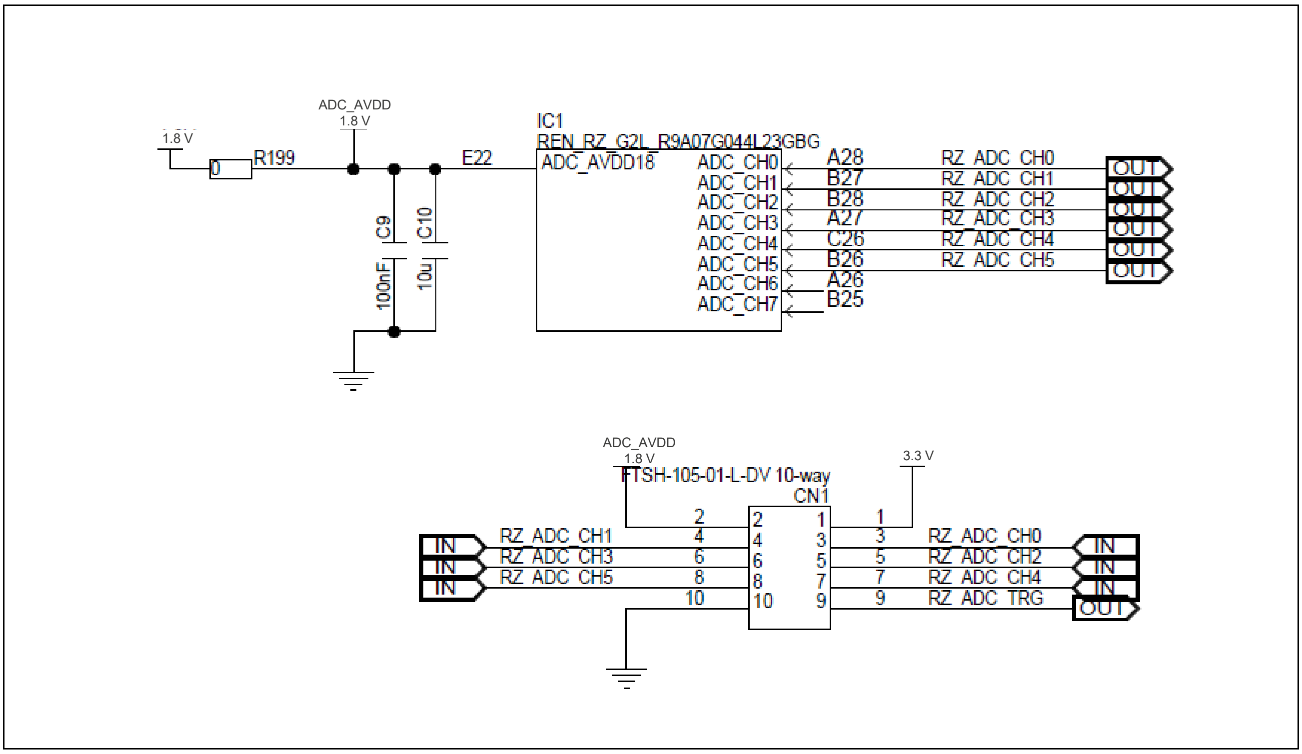


Figure 4.5 Block Diagram of ADC I/F

Table 4.2 Signal Connections of ADC Connector (CN1)

Pin	Signal Name	MPU
1	3.3 V	—
2	RZ_ADC_AVDD18	—
3	RZ_ADC_CH0	ADC_CH0
4	RZ_ADC_CH1	ADC_CH1
5	RZ_ADC_CH2	ADC_CH2
6	RZ_ADC_CH3	ADC_CH3
7	RZ_ADC_CH4	ADC_CH4
8	RZ_ADC_CH5	ADC_CH5
9	RZ_ADC_TRG	P9_0
10	VSS	—

4.5 Clock Configuration

Figure 4.6 shows a block diagram of the clock configuration.

The clock generator (part number 5P35023B-629NLGI) provides the clock required for the RZ/G2L and peripheral interfaces.

The 5P35023B is a Renesas VersaClock® 3S programmable clock generator that supports 6 unique frequency outputs. The 5P35023B-629NLGI uses a 24-MHz crystal as the reference input and provides one 24-MHz reference clock output for the RZ/G2L, two 11.2896-MHz LVCMOS clock outputs for the RZ/G2L and Audio codec, two 25-MHz LVCMOS clock output for two Ethernet PHYs, and one 12.2880-MHz LVCMOS clock output for the RZ/G2L.

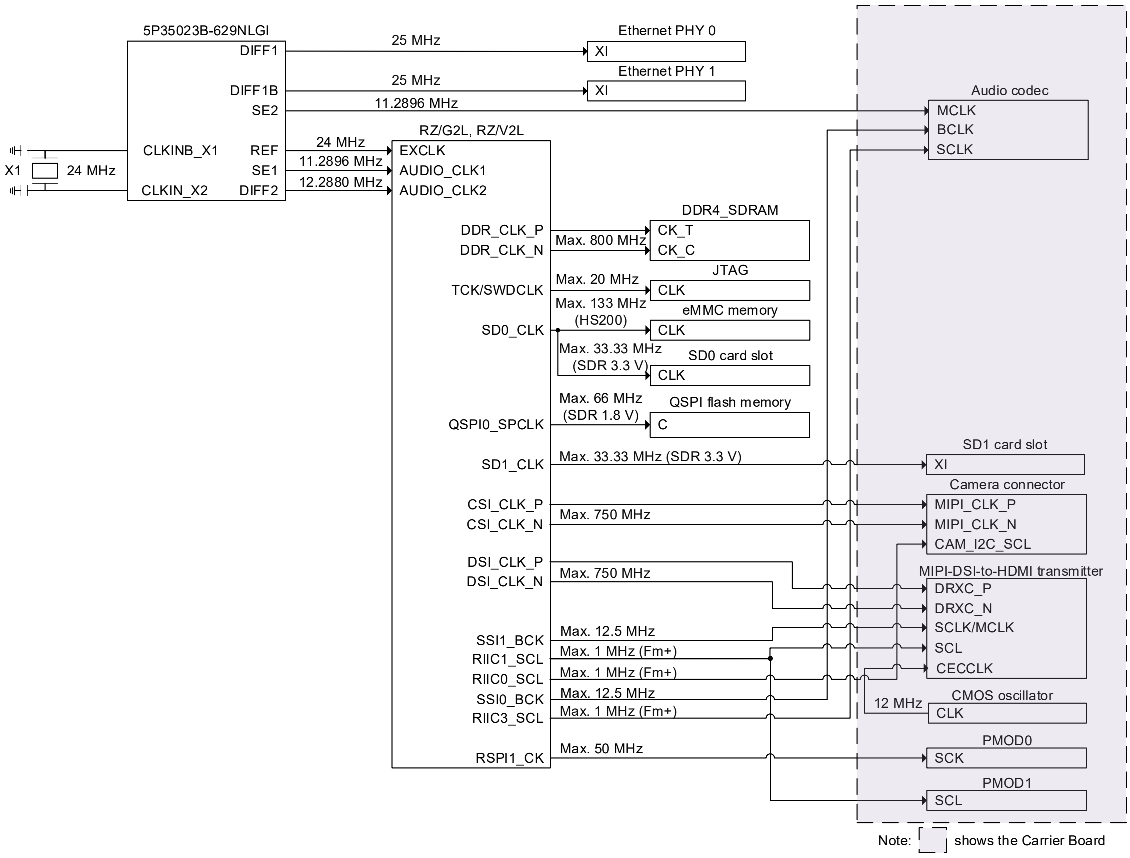


Figure 4.6 Block Diagram of Clock Configuration

4.6 Reset Control

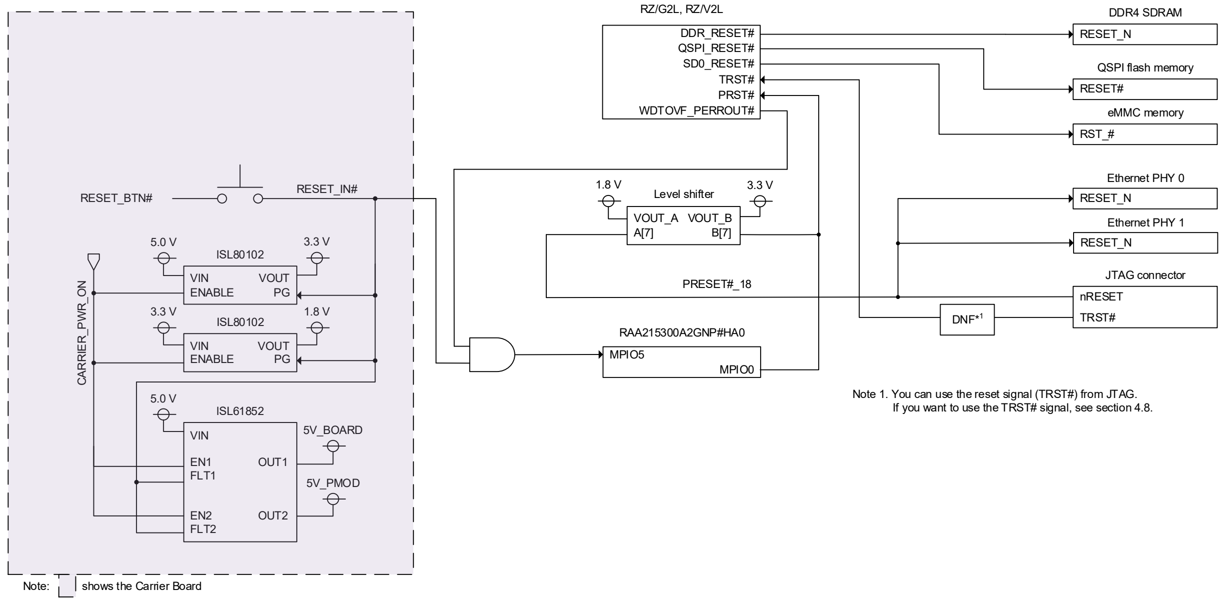
Figure 4.7 shows a block diagram of reset control for the RZ/G2L EVKIT.

Reset control for the RZ/G2L and Ethernet PHYs is handled by reset signals generated by the PMIC.

The DDR4 SDRAM, QSPI flash memory, and eMMC memory are reset by the RZ/G2L through software control.

The external emulator can reset the RZ/G2L via the debug interface.

There are two types of system reset: a power-on reset and a reset by the button switch.



Note: shows the Carrier Board

Note 1. You can use the reset signal (TRST#) from JTAG.
If you want to use the TRST# signal, see section 4.8.

Figure 4.7 Block Diagram of Reset Control

4.7 Power Supply

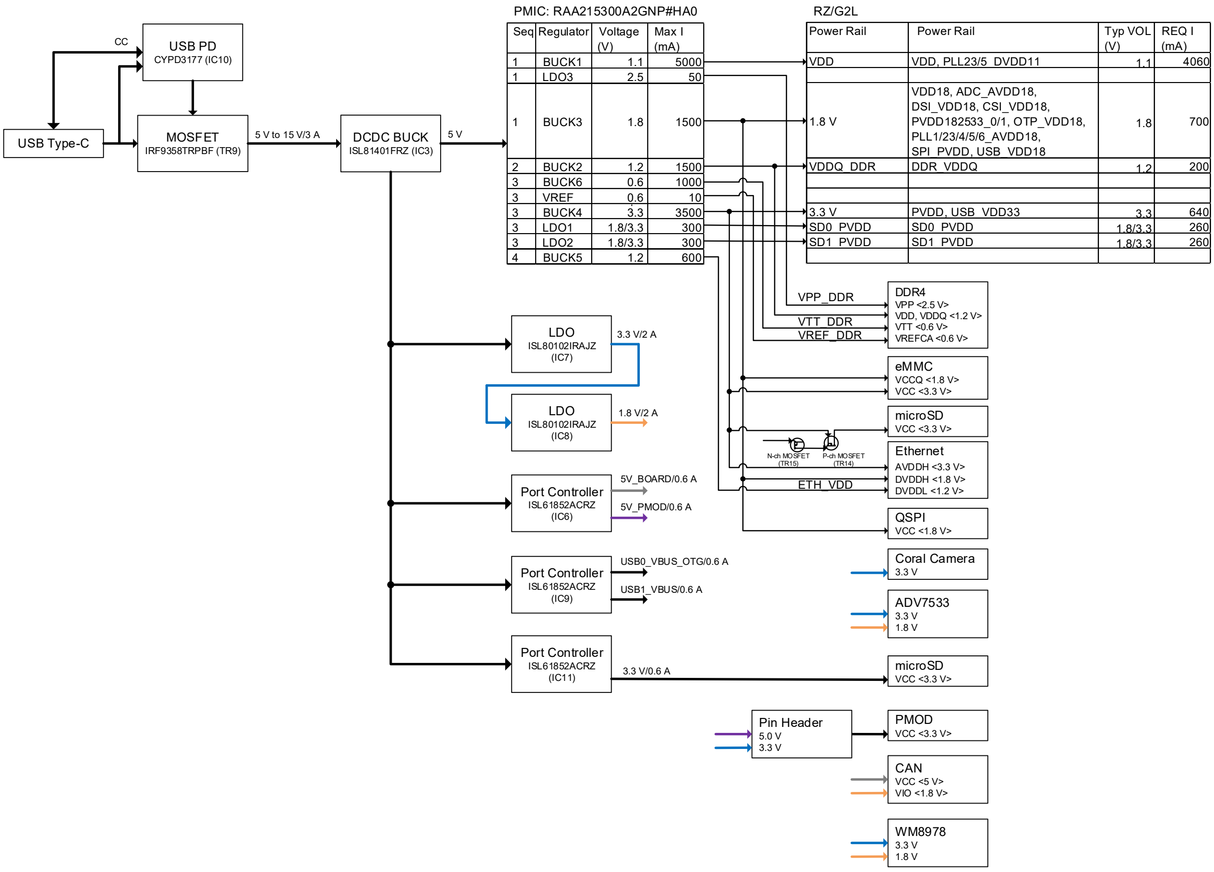
4.7.1 Power Supply Configuration

Figure 4.8 shows a block diagram of the power configuration for the RZ/G2L EVKIT.

This board has one USB Type-C receptacle for power input with USB Power Delivery. The input voltage of VBUS can be selected between 5 V and 9 V.

The default setting for controlling the input voltage level is 5 V (max. 3 A input) with SW11-4 turned on. When the switch is turned off, the input voltage is 9 V (max. 3 A input). SW11-4 is only turned off when the RZ/G2L EVKIT is connected to an external device that requires a lot of power and is expected to run out of power.

The 5-V power supply is supplied to the PMIC mounted on the RZ/G2L SMARC Module, and the PMIC generates the power supply voltage for each interface.



PMIC: RAA215300A2GNP#HA0

Seq	Regulator	Voltage (V)	Max I (mA)
1	BUCK1	1.1	5000
1	LDO3	2.5	50
1	BUCK3	1.8	1500
2	BUCK2	1.2	1500
3	BUCK6	0.6	1000
3	VREF	0.6	10
3	BUCK4	3.3	3500
3	LDO1	1.8/3.3	300
3	LDO2	1.8/3.3	300
4	BUCK5	1.2	600

RZ/G2L

Power Rail	Power Rail	Typ VOL (V)	REQ I (mA)
VDD	VDD, PLL23/5_DVDD11	1.1	4060
1.8 V	VDD18, ADC_AVDD18, DSI_VDD18, CSI_VDD18, PVDD182533_0/1, OTP_VDD18, PLL1/23/4/5/6_AVDD18, SPI_PVDD, USB_VDD18	1.8	700
VDDQ_DDR	DDR_VDDQ	1.2	200
3.3 V	PVDD, USB_VDD33	3.3	640
SD0_PVDD	SD0_PVDD	1.8/3.3	260
SD1_PVDD	SD1_PVDD	1.8/3.3	260

Figure 4.8 RZ/G2L EVKIT Power Supply

4.7.2 PMIC

Figure 4.9 shows the RZ/G2L pin assignment for the PMIC.

The RAA215300A2GNP#HA0 is used as the PMIC on the RZ/G2L EVKIT to supply and manage power for the RZ/G2L.

It integrates 6 synchronous buck regulators and 3 LDO regulators to support power distribution and power sequencing control required by the RZ/G2L.

The LDO1 and LDO2 output voltage values are fixed by P39_0 and P39_1.

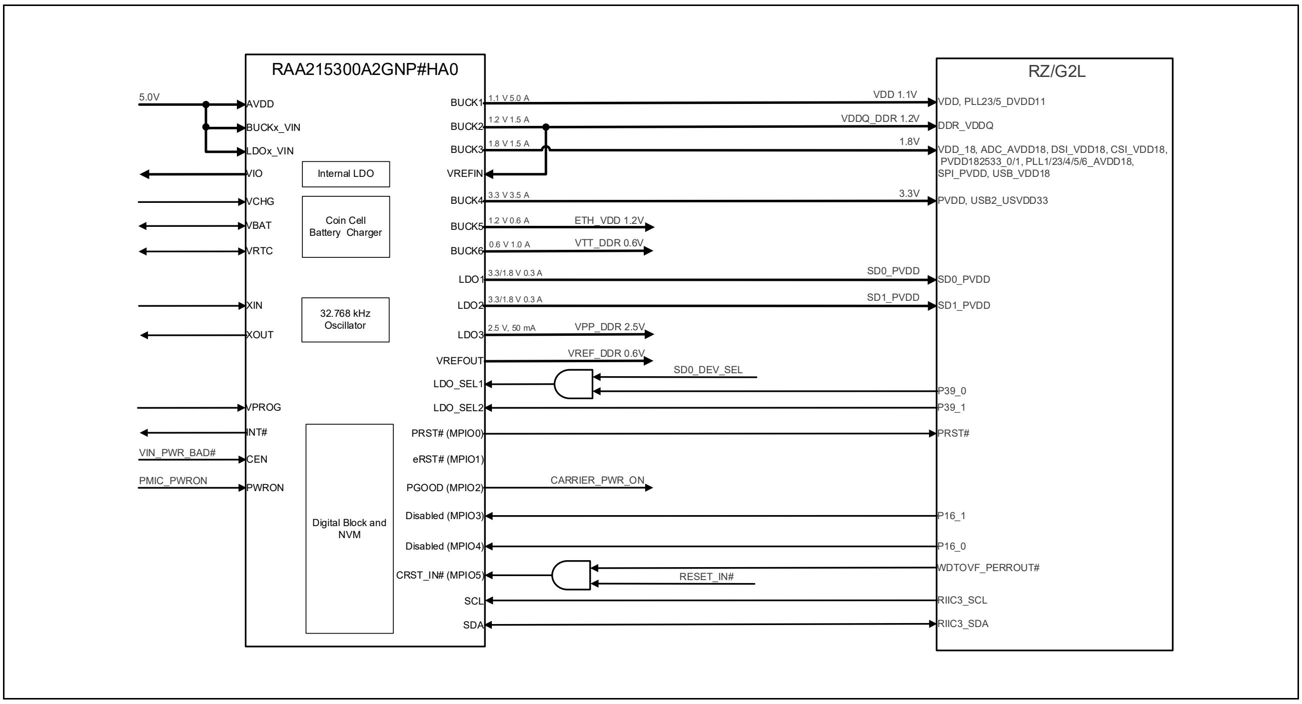


Figure 4.9 Block Diagram around PMIC

4.8 Debug Interface

Figure 4.10 shows a block diagram of the debug interface.

This interface provides supports for debugging and development of the RZ/G2L.

It allows an external debugger to be connected for debugging operations such as CPU core debugging and register access.

In default operation, pin 9 of the debug interface is used for ground detection. Although with resistor (R20) fitting options, it is possible to use the same pin to independently drive the JTAG_TRST# signal.

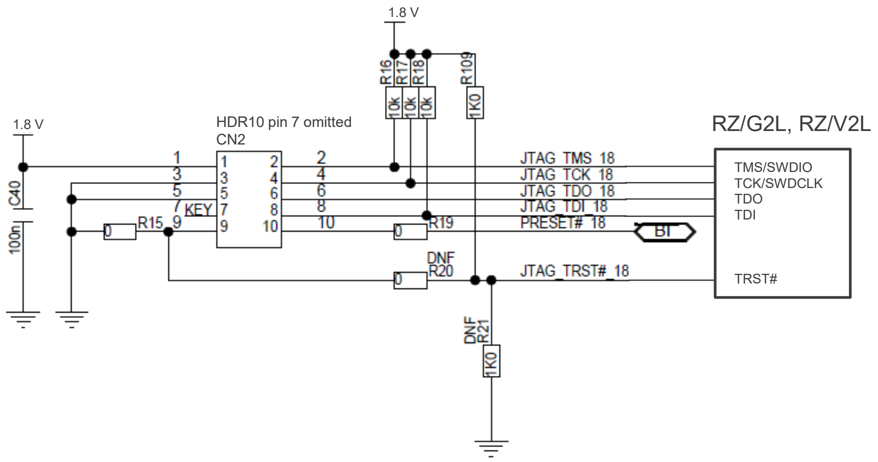


Figure 4.10 Block Diagram of Debug I/F

Table 4.3 Signal Connections of JTAG Connector (CN2)

Pin	Signal Name	MPU
1	1.8 V	—
2	JTAG_TMST_18	TMS/SWDIO
3	VSS	—
4	JTAG_TCK_18	TCK/SWDCLK
5	VSS	—
6	JTAG_TDO_18	TDO
7	—	—
8	JTAG_TDI_18	TDI
9	JTAG_TRST#_18	TRST#
10	PRESET#_18	PRST#

4.9 SD/MMC Host Interface

4.9.1 eMMC Memory

Figure 4.11 shows a block diagram of the MMC interface.

The eMMC memory is connected to channel 0 of the SD/MMC interface of the RZ/G2L. This memory is used in conjunction with a microSD card.

The eMMC memory can be used when

- SW_SD0_DEV_SEL is enabled (SW1-2: Selection SD/MMC is OFF).

This interface complies with the JEDEC standard version 4.51 and supports HS200 mode.

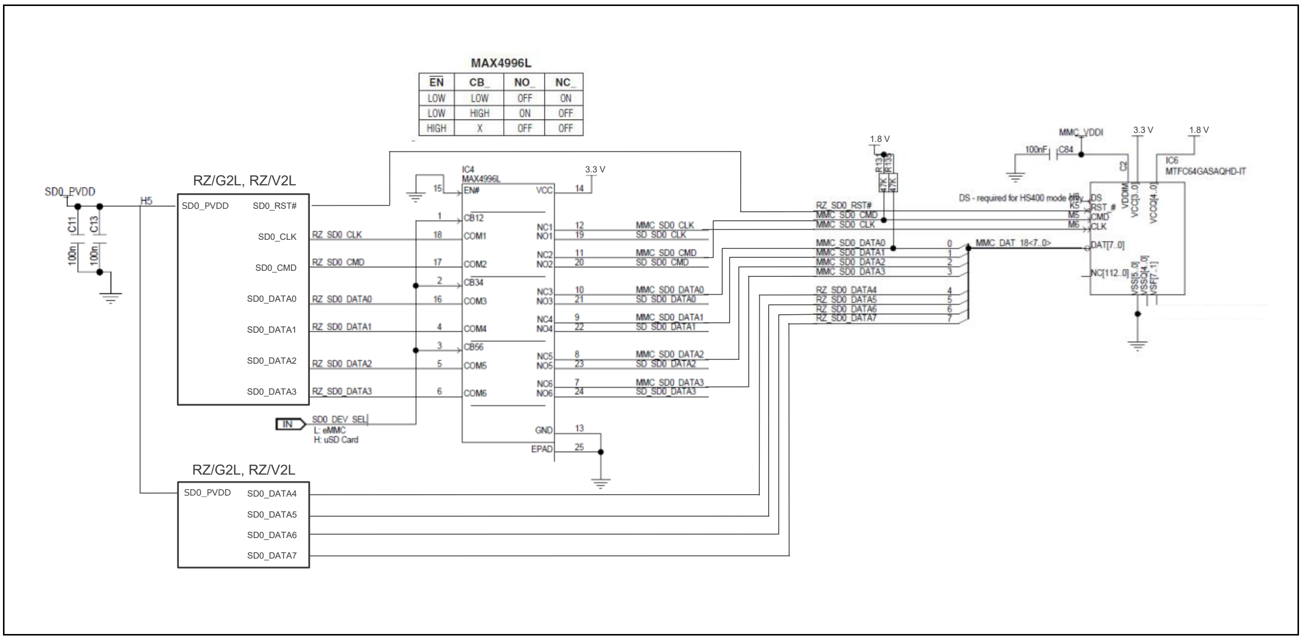


Figure 4.11 Block Diagram of eMMC I/F

4.9.2 microSD Card

Figure 4.12 shows a block diagram of the SDHI interface.

The microSD card is connected to channel 0 of the SD/MMC interface of the RZ/G2L. This memory card is used in conjunction with eMMC memory.

The microSD card can be used when

- microSD is the selected boot mode*[1] (SW11-1: ON, SW11-2: ON, SW11-3: OFF), and
- SW_SD0_DEV_SEL is disabled (SW1-2: Selection SD/MMC is ON) and eMMC memory is not the selected boot mode (SW11-1: ON, SW11-2: OFF, SW11-3: OFF).

This interface complies with the memory card standard version 3.0 and supports UHS-I modes of 50 MB/s (SDR50) and 104 MB/s (SDR104).

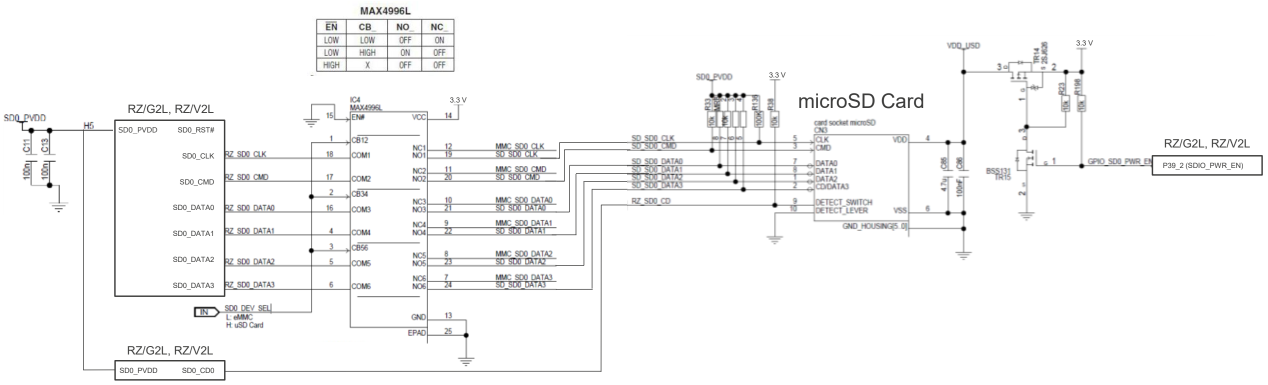


Figure 4.12 Block Diagram of SDHI I/F

Table 4.4 Signal Connections of SD Card Slot (CN4)

Pin	Signal Name	MPU
1	SD_SD0_DATA2	SD0_DATA2
2	SD_SD0_DATA3	SD0_DATA3
3	SD_SD0_CMD	SD0_CMD
4	3.3 V	P4_1 (Power supply control)
5	SD_SD0_CLK	SD0_CLK
6	VSS	—
7	SD_SD0_DATA0	SD0_DATA0
8	SD_SD0_DATA1	SD0_DATA1
9	RZ_SD0_CD	P18_0
10	—	—
—	SD0_PWR_SEL	P39_0 (IO voltage selection of SD0)

Note 1. Due to the circuit specifications, a reboot by pressing the reset button (SW10) is not supported during an eSD boot. In such cases, please use the power switch (SW9) to turn power to the board off and then back on again.

The following is an example of a circuit for executing a reboot during an eSD boot.

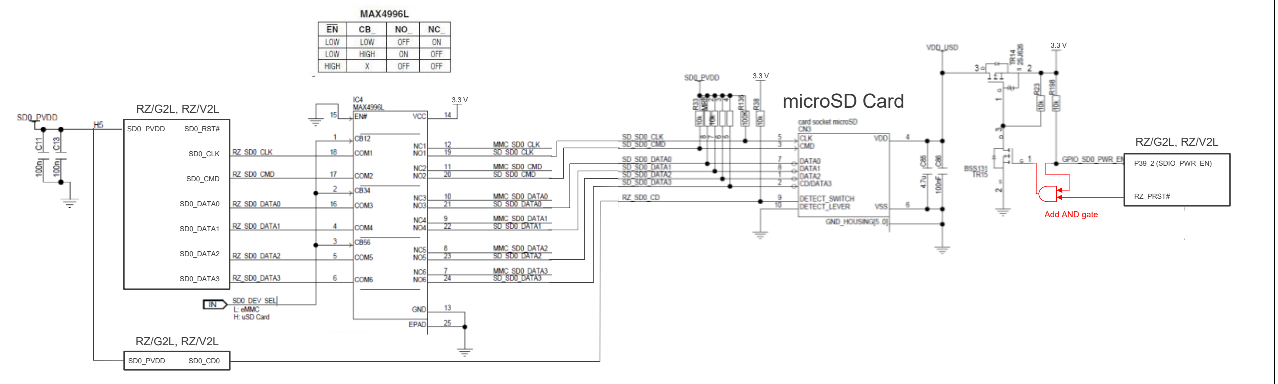


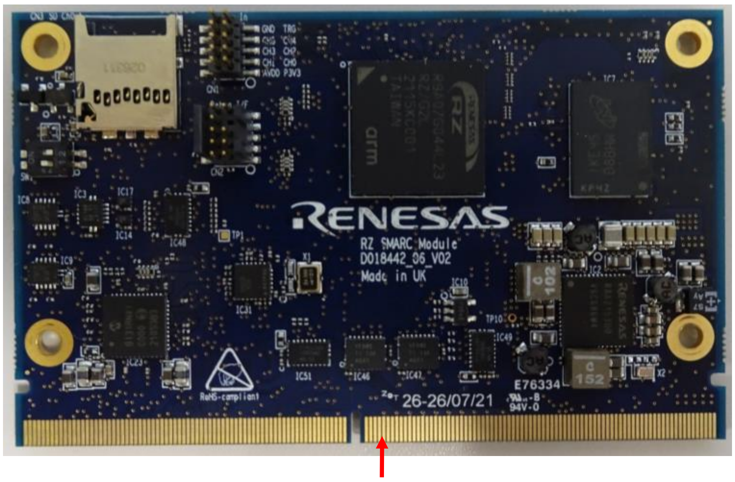
Figure 4.13 Proposed Block Diagram of SDHI I/F

4.10 SMARC Edge Finger

Figure 4.14 illustrates the layout of the edge finger for mating with the SMARC edge connector on the RZ SMARC Carrier.

The SMARC edge connector is a 314-pin, 0.5 mm-pitch, right angle part designed for use with 1.2-mm thick mating PCBs with the edge finger pattern. The SMARC edge connector has a Primary side (Pxx) and a Secondary side (Sxx). The SMARC signal names and edge connector pin numbers are listed in **section 4.1.2, List of Pin Functions** along with the RZ/G2L port pins (if applicable) and signal names.

For the pin assignment of the SMARC edge connector, please refer to “4 MODULE PIN-OUT MAP” of the document “SMARC module 2.1 Specification”.



CN4: SMARC edge finger

Figure 4.14 Layout of Carrier Board Connecting Pins

4.11 Operation Components

4.11.1 Configuration at Shipment

Figure 4.15 shows the switch settings at the time of shipment.

Figure 4.15 Switch Settings at Shipment

4.11.2 Configuration by Switches and Mode Terminals

This board is equipped with DIP switches SW1 for selecting the functions. The functions set by the switches are explained below. The default settings are highlighted.

Figure 4.16 shows a block diagram of the System Setting interface.

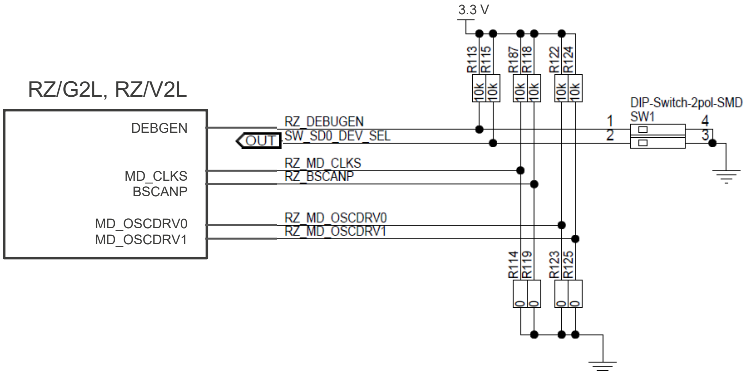


Figure 4.16 Block Diagram of System Setting I/F

Table 4.5 and **Table 4.6** list the functions of SW1 and the mode terminals, respectively.

Table 4.5 Functions of System Setting Switches (SW1)

No.	Setting	Function
SW1-1 DEBUGEN	OFF DEBUGEN = “H”	Debugging with debuggers for ARM
	ON DEBUGEN = “L”	Normal operation
SW1-2 Selection SD/MMC	OFF Selection = “H”	Select the eMMC memory
	ON Selection = “L”	Select the SD card

Table 4.6 Functions of System Settings (Mode Terminals)

No.	Setting	Function
MD_CLKS	0 MD_CLKS = “L”	SSCG is disabled
	1 MD_CLKS = “H”	SSCG is enabled
BSCANP	0 BSCANP = “L”	Normal operation
	1 BSCANP = “H”	Boundary scan test mode
MD_OSCDRV0	0 MD_OSCDRV0 = “L”	Adjust the drive capacity of the OSC buffer
	1 MD_OSCDRV0 = “H”	Adjust the drive capacity of the OSC buffer (Not supported)
MD_OSCDRV1	0 MD_OSCDRV1 = “L”	Adjust the drive capacity of the OSC buffer
	1 MD_OSCDRV1 = “H”	Adjust the drive capacity of the OSC buffer (Not supported)

5. Appendix

5.1 Part Number and Features of Each Board

This section describes the part number and features of each board.

Figure 5.1 shows a picture of the RZ/G2L SMARC Module Board.

Figure 5.1 Top View of the RZ/G2L SMARC Module Board

Please refer to **section 1.3, Features** onwards for the actual functions of the board.

Board Name	Part Number	MPU
RZ/G2L SMARC Module Board	RTK9744L23C01000BE RTK9744L27C01000BE	RZ/G2L (R9A07G044L23GBG or R9A07G044L27GBG)

Figure 5.2 shows a picture of the RZ SMARC Series Carrier Board.

Figure 5.2 Top View of the RZ SMARC Series Carrier Board

Board Name	Part Number
RZ SMARC Series Carrier Board	RTK97X4XXXB00000BE

Figure 5.3 shows a picture of the RZ/G2L SMARC Evaluation Board Kit.

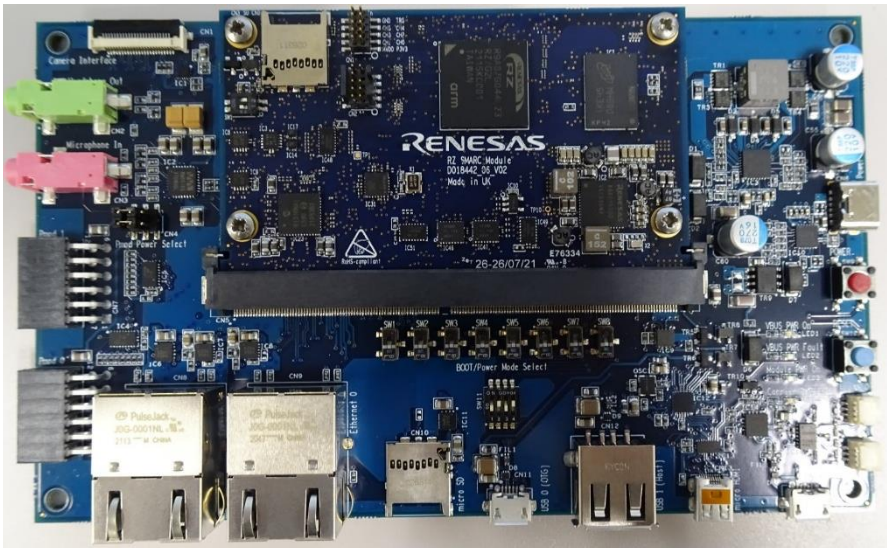


Figure 5.3 Top View of the RZ/G2L SMARC Evaluation Board Kit

The evaluation board kits are similarly designed to use a common board layout and to be pin-compatible.

Board Name	Part Number	MPU
RZ/G2L SMARC Evaluation Board Kit	RTK9744L23S01000BE RTK9744L27S01000BE	RZ/G2L (R9A07G044L23GBG or R9A07G044L27GBG)

5.2 How to Identify Each SMARC Module Board

Table 5.1 lists the difference between the RZ/G2L and RZ/V2L SMARC Module Boards. Figure 4 shows pictures of the RZ/G2L SMARC Module Board.

Table 5.1 Comparison of SMARC Module Boards

Part Number	RZ/G2L SMARC Module Board	RZ/V2L SMARC Module Board
IC1	RZ/G2L (R9A07G044L23GBG or R9A07G044L27GBG)	RZ/V2L (R9A07G054L23GBG or RTK07G054L27GBG)

Figure 5.4 Top and Bottom Views of the RZ/G2L SMARC Module

5.3 How to Replace the SMARC Module Board

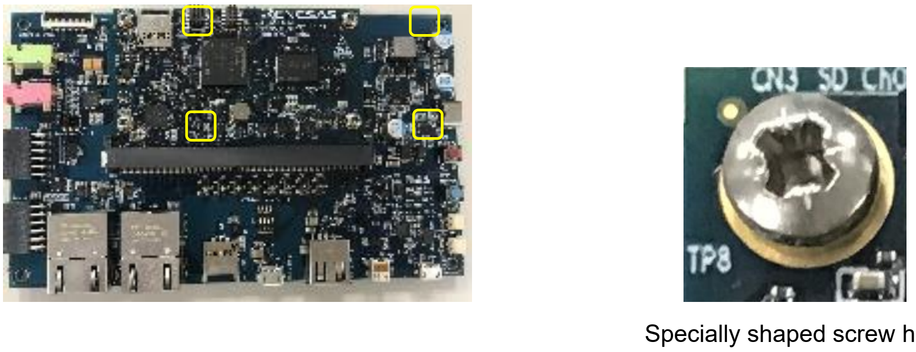
Take care with the following when replacing the board.

1. Remove the four screws.

NOTE

The screw head has a special shape, so be careful not to crush the screw head.

We recommend preparing a torx screwdriver with “T6” head size.



Specially shaped screw head

Figure 5.5 How to Remove the Screws

2. After removing the screws, the SMARC Module Board will stand up at an angle. Slide it out.

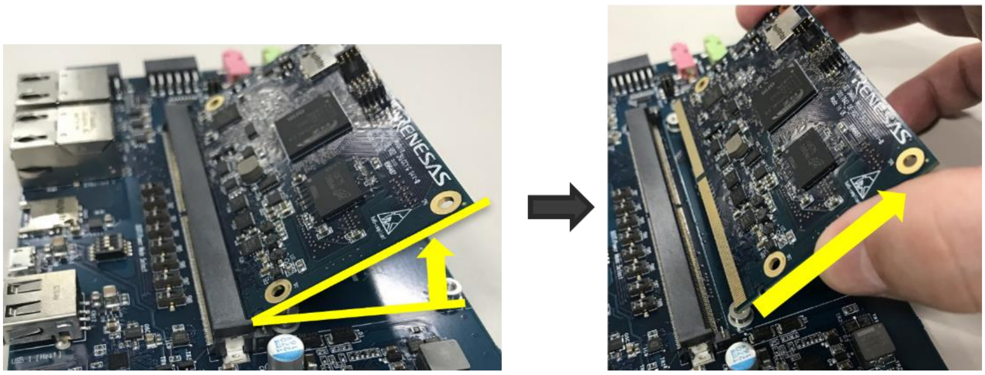


Figure 5.6 How to Remove the SMARC Module Board

3. Insert the replacement SMARC Module Board diagonally, then roll the board until it is parallel to the RZ SMARC Carrier and fix it in place with screws.

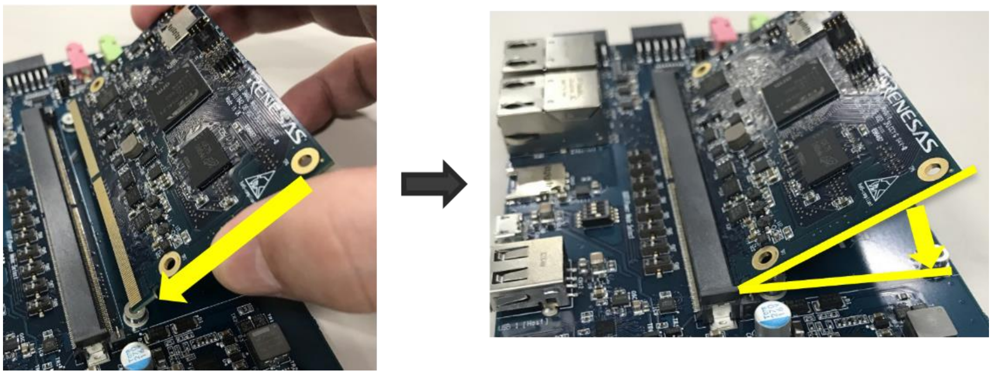


Figure 5.7 How to Install the SMARC Module Board

6. Certifications

The RZ/G2L and RZ/V2L SMARC Module Boards comprising the RZ/G2L and RZ/V2L EVKITs meet the following certification/standards. For important disclaimers and safety precautions, please refer to the page following the cover page of this user's manual.

6.1 EMC/EMI Standards

- FCC Notice (Class A)

  This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

  [NOTE] — This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

  - Reorient or relocate the receiving antenna.
  - Increase the separation between the equipment and receiver.
  - Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
  - Consult the dealer or an experienced radio/television technician for help.

- Innovation, Science and Economic Development Canada ICES-003 Compliance:
  CAN ICES-3 (A)/NMB-3(A)

- CE Class A (EMC)

  This product is herewith confirmed to comply with the requirements set out in the Council Directives on the Approximation of the laws of the Member States relating to Electromagnetic Compatibility Directive 2014/30/EU.

  [Warning] — This is a Class A product. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures to correct this interference.

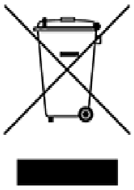
- UKCA Class A (EMC)

  This product is in conformity with the following relevant UK Statutory Instrument(s) (and its amendments): 2016 No. 1091 Electromagnetic Compatibility Regulations 2016.

  [Warning] — This is a Class A product. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures to correct this interference.

6.2 Material Selection, Waste, Recycling and Disposal Standards

- EU RoHS
- WEEE Directive (2012/19/EU) & The Waste Electrical and Electronic Equipment Regulations 2013



For customers in the UK & European Union the WEEE (Waste Electrical and Electronic Equipment) regulations put responsibilities on producers for the collection and recycling or disposal of electrical and electronic waste. Return of WEEE under these regulations is applicable in the UK and European Union.

This equipment (including all accessories) is not intended for household use. After use the equipment cannot be disposed of as household waste, and the WEEE must be treated, recycled and disposed of in an environmentally sound manner.

Renesas Electronics Europe GmbH can take back end of life equipment. Register for this service at: https://www.renesas.com/en/support/regional-customer-support/weee

6.3 Safety Standards

- UL 94V-0

REVISION HISTORY	RZ/G2L, RZ/V2L SMARC Module Board User's Manual: Hardware

Rev.	Date	Description	
		Page	Summary
1.00	Sep. 27, 2021	—	First edition issued
1.01	Oct. 07, 2021	1	For front cover, it is changed the description from "RZ/G2L SMARC Module Board RTK9744L23C01000BE" to "RZ/G2L, RZ/V2L SMARC Module Board". It is changed the description from "RZ Family / RZ/G Series" to "RZ Family / RZ/G, RZ/V Series" It is added the description "RTK9754L23C01000BE".
		7	For Title, it is changed the description from "RZ Family / RZ/G Series RZ/G2L SMARC Module Board RTK9744L23C01000BE" to "RZ Family / RZ/G, RZ/V Series RZ/G2L, RZ/V2L SMARC Module Board". For section "Overview", it is added the description "To begin with, only RTK9744L23C01000BE will be explained here. The difference between RTK9744L23C01000BE and RTK9754L23C01000BE is that RTK9754L23C01000BE uses Renesas Electronics microprocessor RZ/V2L "R9A07G054L23GBG", which is pin-compatible with RZ/G2L. In other words, they are functionally the same".
		60	For Revision History, it is changed the description from "RZ Family / RZ/G Series RZ/G2L SMARC Module Board RTK9744L23C01000BE" to "RZ Family / RZ/G, RZ/V Series RZ/G2L, RZ/V2L SMARC Module Board".
		62	For back cover, it is changed the description from "RZ Family / RZ/G Series" to "RZ Family / RZ/G, RZ/V Series".
1.02	Apr. 26, 2022	8, 11 to 14, 52 to 57	For each figure, the figure style has been improved.
		10	For section title, it is changed the description from "Outside View" to "Physical View". Figure 1.2 is modified.
		15	For Table 1.2 and Table 1.3, the Recommend Optional Parts is removed.
		40, 42, 49 to 51	For each interface, the description is added.
		41	For DDR4 SDRAM, the description is added. For Figure 2.2, the pin swap is modified.
		60 to 64	Section 4 Appendix is added.
1.10	Dec. 09, 2022	23, 39	Restrictions on use are added. When used in combination with the RZ SMARC Series Carrier Board (P/N: RTR97X4XXXB00000BE), CAN0 and CAN1 interface cannot be used because a CAN transceiver is not fitted on the RTK97X4XXXB00000BE.
1.20	Apr. 03, 2024	18 to 34	For section 2.2.2 "List of Pin Functions", the pin names, pin functions, and descriptions in the table are modified.
		34	Restrictions on use are modified. The CAN connector is implemented on the RZ SMARC Series Carrier Board (P/N: RTK97X4XXXB00000BE), but the CAN-FD interface cannot be used because a CAN transceiver is not fitted. The following carrier boards are equipped with a CAN transceiver and the CAN-FD interface is available already. S.LOT# in the outer box label: 000251812 or later S.LOT# label on the carrier board: 251812 or later
		37	For section 2.4 "Gigabit Ethernet Interface", the figures are modified.
		40	For section 2.7 "Reset Control", the figure is modified.
		41	For section 2.8 "Power Supply Configuration", the figure is modified.
		43	For section 2.9 "PMIC", the figure is modified
		44	For section 2.10 "Debug Interface", the figure is modified.
		45	For section 2.11.1 "eMMC Memory", the figure is modified.
1.30	Nov. 25, 2025	60, 61	Section 5 "Certifications", added

Rev.	Date	Description	
		Page	Summary
2.00	May 27, 2026	All	Restructured the sections of the document and reorganized some sentences, figures, and tables to make them easier to read. Basically, the content of the document remains unchanged.
		13	Section 2 “Box Contents”, added
		14	Section 3 “Ordering Information”, added
		44	For section 4.9.2 “microSD Card”, the specification restriction and countermeasure for eSD boot were added.

RZ/G2L, RZ/V2L SMARC Module Board User's Manual: Hardware

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RZ/G2L, RZ/V2L SMARC Module Board

Renesas Electronics Corporation