RENESAS

RX660 Group

Renesas Starter Kit for RX660
User's Manual

RENESAS 32-Bit MCU
RX Family / RX600 Series

Renesas Electronics
www.renesas.com

Rev.1.00 Jan 2022

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(Rev.5.0-1 October 2020)

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General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.

2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.

3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.

4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.

5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.

6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).

7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.

8. Differences between products

   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

Disclaimer

By using this Renesas Starter Kit (RSK), the user accepts the following terms:

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Precautions

The following precautions should be observed when operating any RSK product:

This Renesas Starter Kit is only intended for use in a laboratory environment under ambient temperature and humidity conditions. A safe separation distance should be used between this and any sensitive equipment. Its use outside the laboratory, classroom, study area or similar such area invalidates conformity with the protection requirements of the Electromagnetic Compatibility Directive and could lead to prosecution.

The product generates, uses, and can radiate radio frequency energy and may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment causes harmful interference to radio or television reception, which can be determined by turning the equipment off or on, you are encouraged to try to correct the interference by one or more of the following measures;

- ensure attached cables do not lie across the equipment
- reorient the receiving antenna
- increase the distance between the equipment and the receiver
- connect the equipment into an outlet on a circuit different from that which the receiver is connected
- power down the equipment when not in use
- consult the dealer or an experienced radio/TV technician for help NOTE: It is recommended that wherever possible shielded interface cables are used.

The product is potentially susceptible to certain EMC phenomena. To mitigate against them it is recommended that the following measures be undertaken;

- The user is advised that mobile phones should not be used within 10m of the product when in use.
- The user is advised to take ESD precautions when handling the equipment.

The Renesas Starter Kit does not represent an ideal reference design for an end product and does not fulfil the regulatory standards for an end product.

How to Use This Manual

1.   Purpose and Target Readers

This manual is designed to provide the user with an understanding of the CPU Board hardware functionality, and electrical characteristics. It is intended for users designing sample code on the CPU Board platform, using the many different incorporated peripheral devices.

The manual comprises of an overview of the capabilities of the RSK product, but does not intend to be a guide to embedded programming or hardware design.

> Particular attention should be paid to the precautionary notes when using the manual. These notes occur within the body of the text, at the end of each section, and in the Usage Notes section.

> The revision history summarizes the locations of revisions and additions. It does not list all revisions. Refer to the text of the manual for details.

The following documents apply to the RSKRX660. Make sure to refer to the latest versions of these documents. The newest versions of the documents listed may be obtained from the Renesas Electronics Web site.

Document Type	Description	Document Title	Document No.
User's Manual	Describes the technical details of the RSK hardware.	Renesas Starter Kit for RX660 User's Manual	R20UT5017EG
Tutorial Manual	Provides a guide to setting up RSK environment, running sample code and debugging programs.	Renesas Starter Kit for RX660 Tutorial Manual	CS+: R20UT5018EG e^2 studio: R20UT5021EG
Quick Start Guide	Provides simple instructions to setup the RSK and run the first sample.	Renesas Starter Kit for RX660 Quick Start Guide	CS+: R20UT5019EG e^2 studio: R20UT5022EG
Smart Configurator Tutorial	Provides a guide to code generation and importing into the e^2 studio/CS+ IDE.	Renesas Starter Kit for RX660 Smart Configurator Tutorial Manual	CS+: R20UT5020EG e^2 studio: R20UT5023EG
Schematics	Full detail circuit schematics of the CPU Board.	Renesas Starter Kit for RX660 Schematics	R20UT5016EG
Hardware Manual	Provides technical details of the RX660 microcontroller.	RX660 Group Hardware Manual	R01UH0937EJ

2. List of Abbreviations and Acronyms

Abbreviation	Full Form
ADC	Analog-to-Digital Converter
BC	Battery Charging
bps	bits per second
CAN	Controller Area Network
CPU	Central Processing Unit
DAC	Digital-to-Analog Converter
DIP	Dual In-line Package
DMA	Direct Memory Access
DMAC	Direct Memory Access Controller
DNF	Do Not Fit
E1 / E2 Lite	Renesas On-chip Debugging Emulator
EEPROM	Electronically Erasable Programmable Read Only Memory
EMC	Electromagnetic Compatibility
ESD	Electrostatic Discharge
GLCDC	Graphic LCD Controller
I2C (IIC)	Philips™ Inter-Integrated Circuit Connection Bus
IRQ	Interrupt Request
LCD	Liquid Crystal Display
LED	Light Emitting Diode
LIN	Local Interconnect Network
MCU	Micro-controller Unit
MTU	Multi-Function Timer Pulse Unit
n/a (NA)	Not Applicable
n/c (NC)	Not Connected
NMI	Non-maskable Interrupt
OTG	On The Go™
PC	Personal Computer
PDC	Parallel Data Capture Unit
PLL	Phase Locked Loop
Pmod™	This is a Digilent Pmod™ Compatible connector. Pmod™ is registered to Digilent Inc. Digilent-Pmod_Interface_Specification
POE	Port Output Enable
PWM	Pulse Width Modulation
RAM	Random Access Memory
ROM	Read Only Memory
RSK	Renesas Starter Kit
RTC	Real Time Clock
SCI	Serial Communications Interface
SPI	Serial Peripheral Interface
SSI	Serial Sound Interface
TFT	Thin Film Transistor
UART	Universal Asynchronous Receiver/Transmitter
USB	Universal Serial Bus
WDT	Watchdog Timer

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Table of Contents

1.Overview

1.1 Purpose

This CPU Board is an evaluation tool for Renesas microcontrollers. This manual describes the technical details of the CPU Board hardware.

1.2 Features

This RSK provides an evaluation of the following features:
- Renesas microcontroller programming
- User code debugging
- User circuitry such as switches, LEDs and a potentiometer
- Sample applications
- Sample peripheral device initialisation code

The RSK board contains all the circuitry required for microcontroller operation.

1.3 Board specification

Board specification was shown in **Table 1-1** below.

Table 1-1: Board Specification

Item	Specification
Microcontroller	Part No : R5F56609HDFB
	Package : 144-pin PLQP0144KA-B
	On-Chip Memory : ROM 1MB, RAM 128KB
On-Board Memory	I²C EEPROM: 2Kbit
Input Clock	RX660 Main : 24MHz
	RX660 Sub : 32.768kHz
	RL78/G1C Main: 12MHz
Power Supply *1	DC Power Jack : 5 V Input
	Power Supply IC : 5V Input, 3.3V Output
Debug Interface *4	E2 Lite 14-pin box header
Push Switch	Reset Switch x 1
	User Switch x 3
Potentiometer(for ADC)	Single-turn, 10kΩ
LED	Power indicator: green x 1
	User : green x 1, orange x 1, red x 2
CAN	Connector : 2.54mm pitch, 3-pin x 1
	CAN Driver x 1
LIN *2	Connector: 2.54mm pitch, 3-pin x 1 *2
	LIN Driver x 1
Remote Control	IR Receiver Module x 1 *3
USB to Serial Converter Interface	Connector : USB-MiniB
	Driver : RL78/G1C Microcontroller (Part No R5F10JBCANA)
Pmod™	PMOD1 : Angle type, 12-pin Connector
	PMOD2 : Straight type, 12-pin Connector
Application Board Interface *2	2.54 mm pitch, 26-pin x 2 (JA1, JA2), 50-pin x 1 (JA3), 24-pin x 2 (JA5, JA6)

*1: Board can also supply 5V into RX660 microcontroller without Power Supply IC.

*2: The connector is not included in the product.

*3: IR Receiver Module is not included in the product.

*4: When using JTAG communication unwanted interference from the emulator may affect the operation of the user system. Please refer to the 'Precautions' section in this manual for more information.

2. Power Supply

2.1 Requirements

This board has an optional centre positive supply connector using a 2.0mm barrel power jack (PWR). The main power supply connected to PWR should supply a minimum of 10W to ensure full functionality. When the board is connected to another system then that system should supply power to the board.

This CPU board supports one external voltage input. Details of the external power supply connection are shown in **Table 2-1 and Table 2-2** below. The default power configuration is shown in **bold, blue text.**

Table 2-1: PWR connector Requirements

Connector	Supply voltage
PWR	Input 5VDC

There are RSK products which supports the 12V voltage input. Since this board is supporting the 5V voltage input, be careful not to connect the power supply of a high-voltage output accidentally.
Moreover, the main power supply connected to PWR should supply a minimum of 10W to ensure full functionality.

Table 2-2: Main Power Supply Requirements

J7 Setting	J6 Setting	Supply Source	Board_VCC UC_VCC
1-2 Shorted	**Open**	**E2-Lite** (3V3) / JA1-3V3	**3.3V** [*1]
1-2 Shorted	1-2 Shorted	PWR / Unregulated_VCC / JA1-5V	3.3V [*2]
2-3 Shorted	1-2 Shorted	PWR / Unregulated_VCC / JA1-5V	5V [*3]

[*1]: 5V Pmod™ interface and CAN, LIN can't be used.

[*2]: 5V Pmod™ interface can't be used.

[*3]: Pmod™ LCD and 3V3 interface can't be used.

2.2 Power-Up Behaviour

When the RSK is purchased, the RSK board has the 'Release' build of the example tutorial software pre-programmed into the Renesas microcontroller. Please consult the 'Renesas Starter Kit Smart Configurator Tutorial Manual' for further information of this example.

3. Board Layout

3.1 Component Layout

Figure 3-**1** below shows the top component layout of the board.
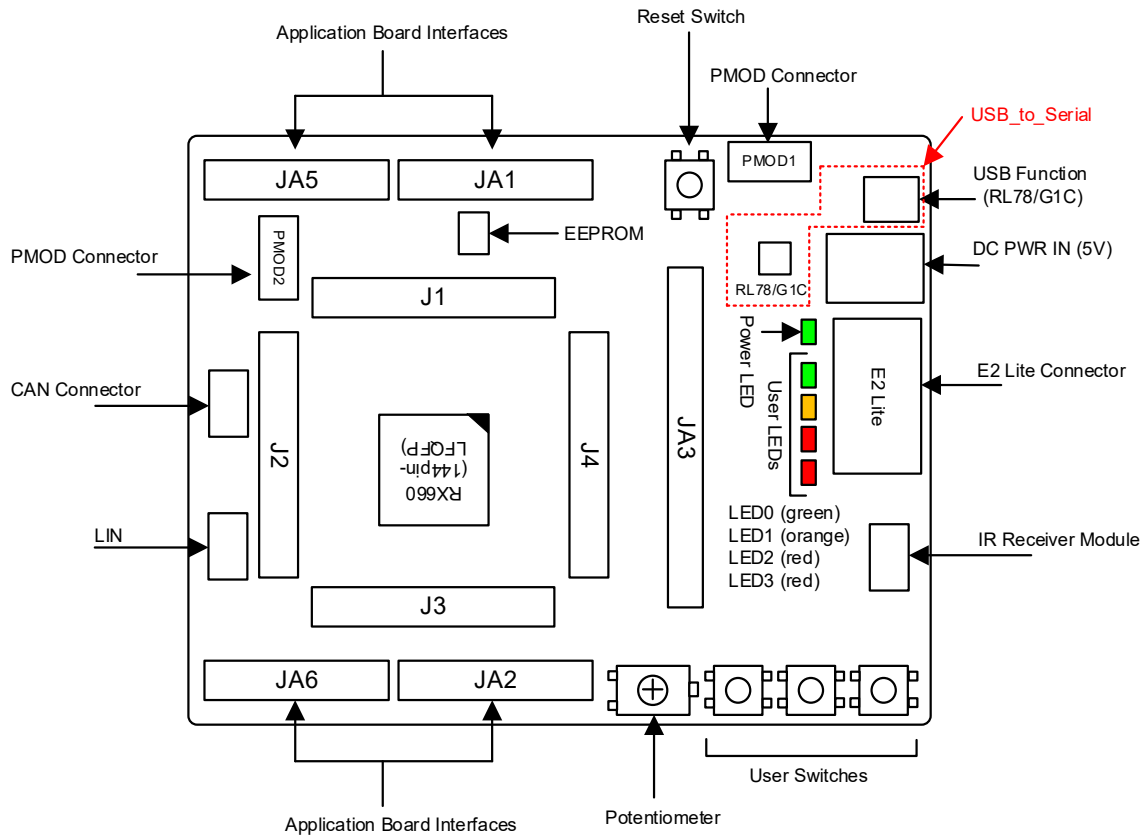
Figure 3-**1: Board Layout**

3.2   Board Dimensions

Figure 3-2 below gives the board dimensions and connector positions. All the through-hole connectors are on a common 2.54mm pitch grid for easy interfacing.
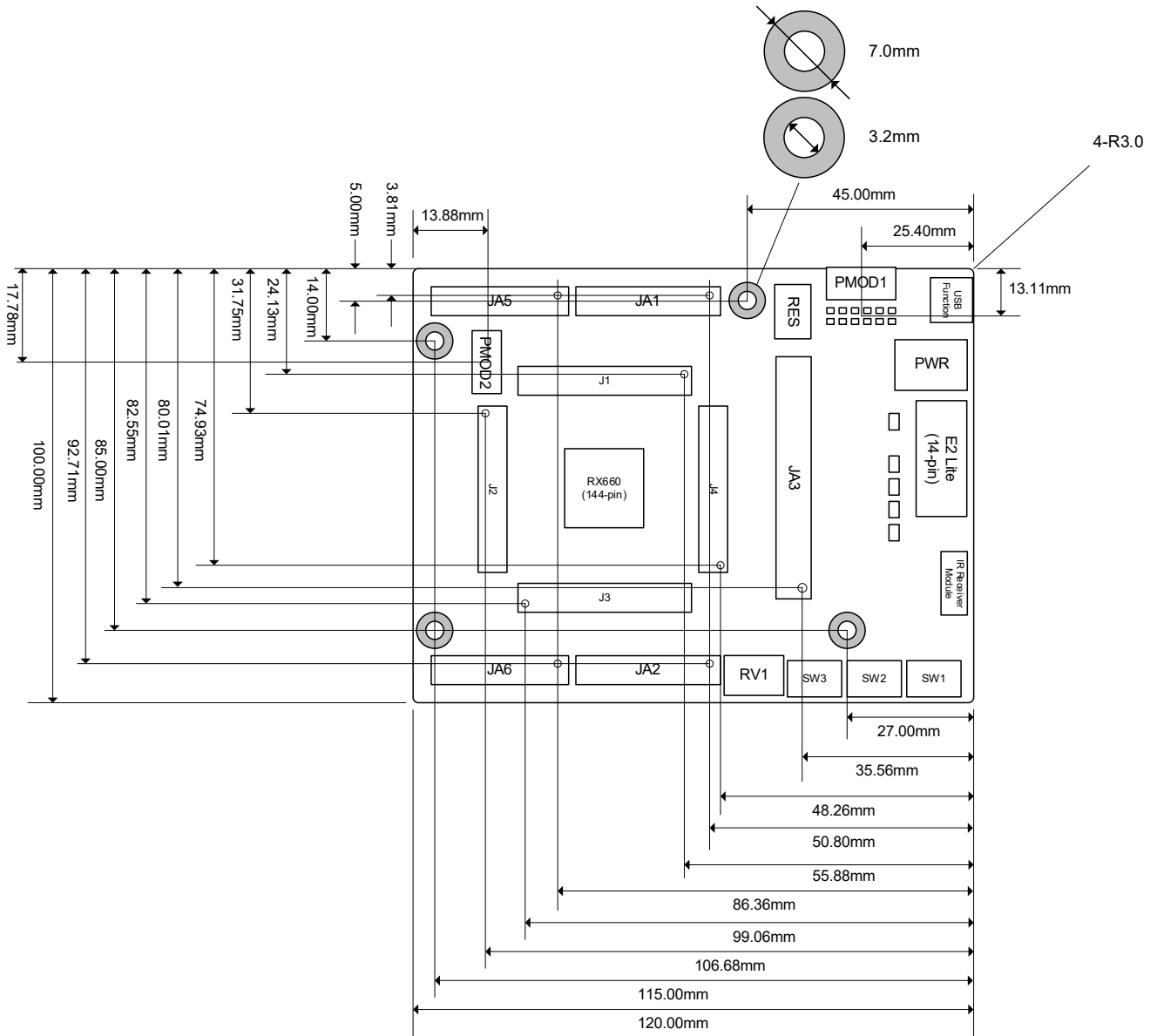
Figure 3-2: Board Dimensions

3.3 Component Placement

Figure 3-3 below shows placement of individual components on the top-side PCB – bottom-side component placement can be seen in **Figure 3-4.** Component types and values are shown on the board schematics.
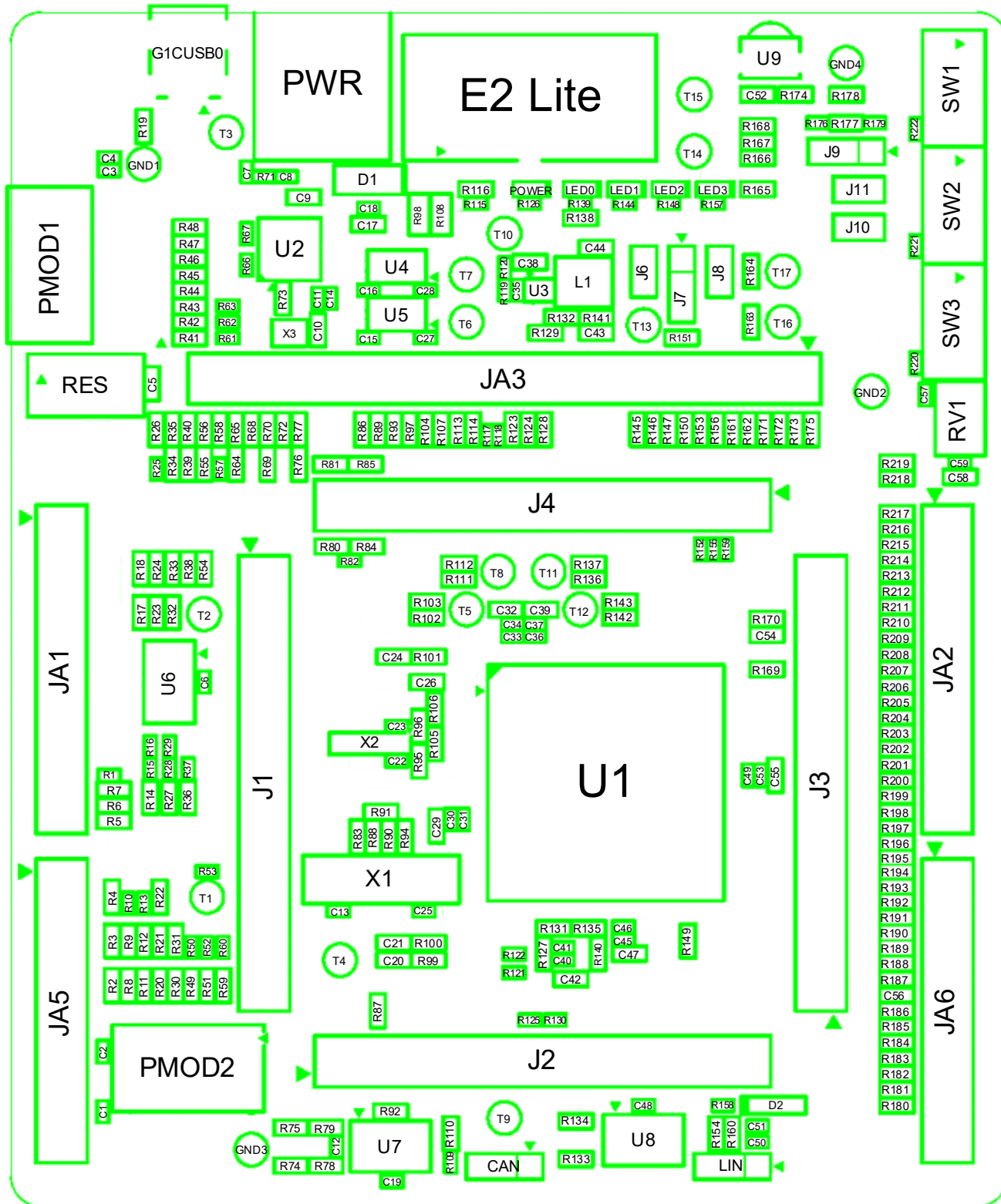
Figure 3-3: Top-Side Component Placement
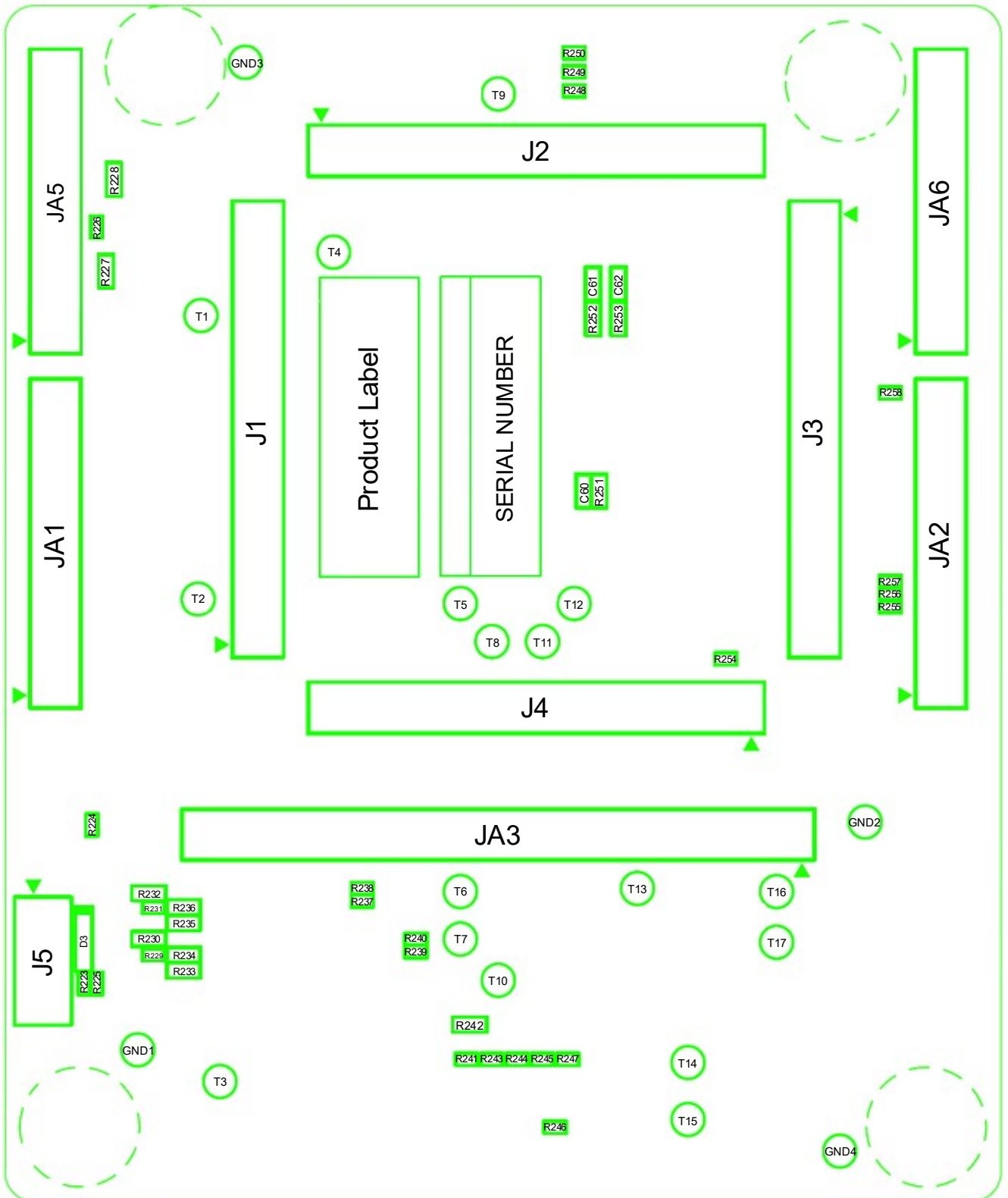
Figure 3-4: Bottom-Side Component Placement

4.   Connectivity

4.1   Internal Board Connections

The diagram below shows the CPU board components and their connectivity to the MCU.
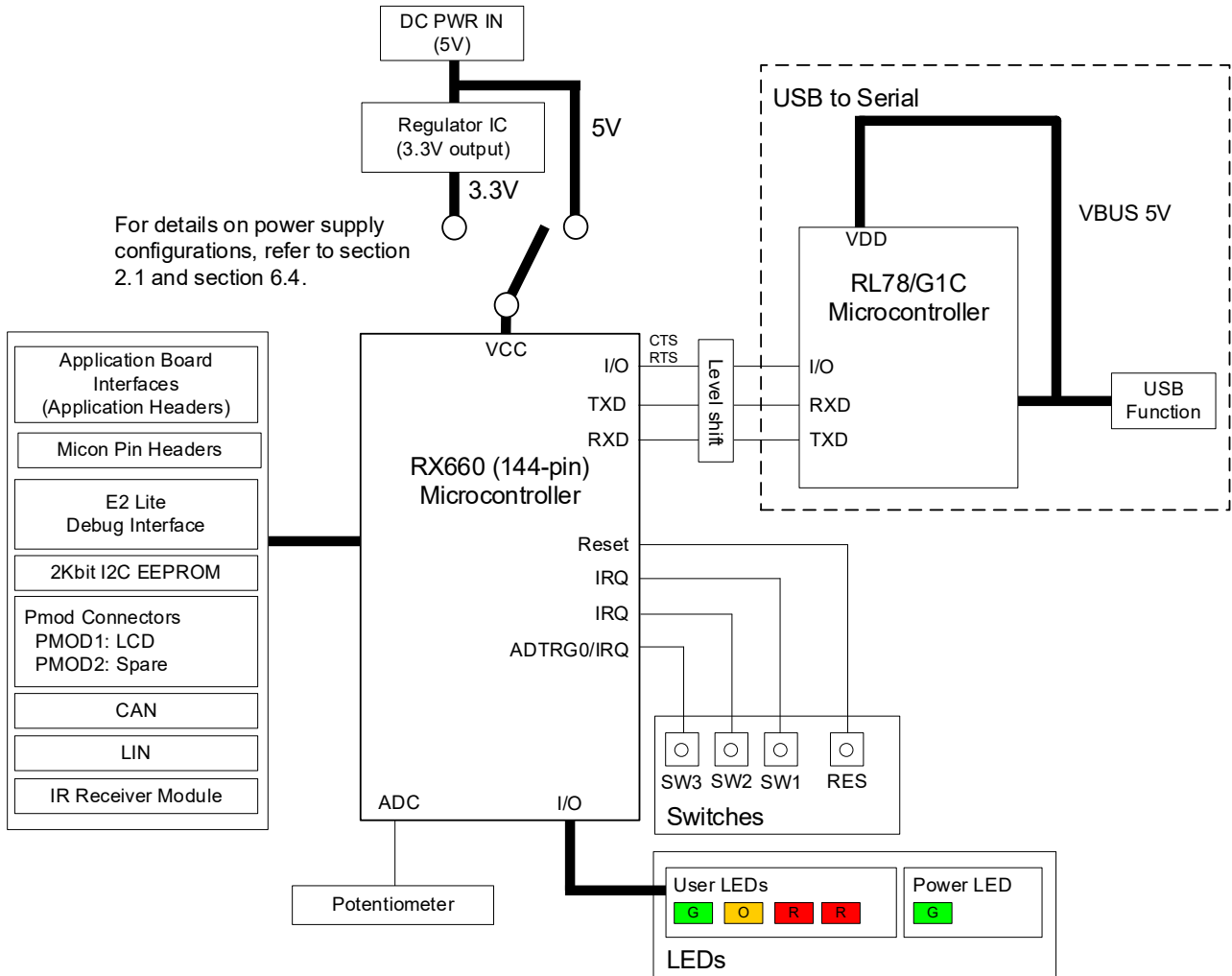
Figure 4-1: Internal Board Block Diagram

4.2 Debugger Connections

Figure 4-2 below shows the connections between the CPU board, E2 Lite debugger and the host PC.

Figure 4-2: Debugger Connection Diagram

5. User Circuitry

5.1 Reset Circuit

A reset control circuit is fitted to the CPU board to generate the required reset signal, and is triggered from the RES switch. Refer to the RX660 Group User's Manual: Hardware for details regarding the reset signal timing requirements, and the CPU board schematics for information regarding the reset circuitry in use on the board.

5.2 Clock Circuit
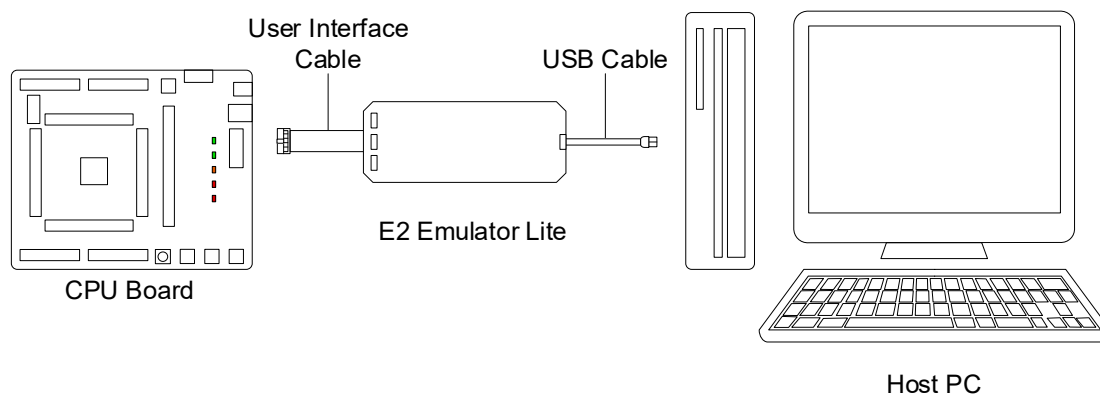
A clock circuit is fitted to the CPU board to generate the required clock signal to drive the MCU, and associated peripherals. Refer to the RX660 Group Hardware Manual and the RL78/G1C hardware manual for details regarding the clock signal requirements, and the CPU board schematics for information regarding the clock circuitry in use on the CPU board. Details of the oscillators fitted to the board are listed in **Table 5-1** below.

Table 5-1: Crystal

Crystal	Function	Default Placement	Frequency	Device Package
X1	Main MCU crystal for RX660	Fitted	24MHz	Encapsulated, SMT
X2	Real time Clock for RX660	Fitted	32.768kHz	Encapsulated, SMT
X3	Main MCU crystal for RL78/G1C	Fitted	12MHz	Encapsulated, SMT

5.3 Switches

There are four switches located on the CPU board. The function of each switch and its connection is shown in **Table 5-2**. For further information regarding switch connectivity, refer to the CPU board schematics.

Table 5-2: Push Switch Connections

Switch	Function	MCU	
		Signal (Port)	Pin
RES	When pressed, the microcontroller is reset.	RES#	19
SW1	Connects to an IRQ9 input for user controls.	P91	129
SW2	Connects to an IRQ10 input for user controls.	P92	128
SW3	Connects to an IRQ15 input for user controls. Connects to an ADTRG0 input for ADC controls.	P07	144

5.4 LEDs

There are five LEDs on the RSK board. The function of each LED, its colour, and its connections are shown in **Table 5-3**.

Table 5-3: LED Connections

LED	Colour	Function	MCU	
			Port	Pin
POWER	Green	Indicates the status of the Board_VCC power rail.	NC	NC
LED0	Green	User operated LED.	P17	38
LED1	Orange	User operated LED.	PF5	9
LED2	Red	User operated LED.	P04	5
LED3	Red	User operated LED.	P06	3

5.5 Potentiometer

A single-turn potentiometer is connected as a potential divider to analog input AN000 (Port P40, pin 141). The potentiometer can be used to create a voltage between Board_VCC and AVSS0.
Refer to the maker site for specification of the potentiometer (VISHAY with part number TS53 series).

> The potentiometer offers an easy method of supplying a variable analog input to the microcontroller. It does not necessarily reflect the accuracy of the controller's ADC. Refer to the RX660 Group User's Manual: Hardware for further details.

5.6 Pmod™

The RSK board is equipped with connectors for Digilent Pmod™ interface. Please connect the provided LCD module to the PMOD1 connector.

> Care should be taken when installing the LCD module to ensure pins are not bent or damaged. The LCD module is vulnerable to electrostatic discharge (ESD); therefore appropriate ESD protection should be used.

Figure 5-1 below shows Digilent Pmod™ Compatible Header Pin Numbering. Connection information for the Digilent Pmod™ Compatible header is provided in **Table 5-4** and **Table 5-5** below.

Please note that the connector numbering adheres to the Digilent Pmod™ standard and is different from all other connectors on the RSK designs. Details can be found in the Digilent Pmod™ Interface Specification.
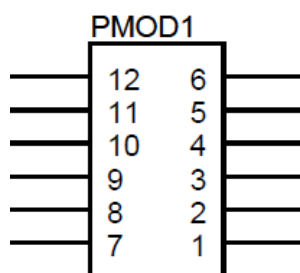
Figure 5-1: Digilent Pmod™ Compatible Header Pin Numbering

Table 5-4: Pmod™1 Header Connections

Pin	Pmod™ Interface			MCU	
	Type 2A (SPI)	Type 3A (UART)	Type 6A (I2C)	Port	Pin No.
1	CS	CTS/GPIO	INT	PJ3/CTS6#/IRQ11	13
2	MOSI	TXD	RESET	P00/TXD6/SMOSI6	8
3	MISO	RXD	SCL	P01/RXD6/SMISO6	7
				PB0/SSCL4*2	87
4	SCK	RTS/GPIO	SDA	P02/SCK6	6
				PB1/SSDA4*2	84
5	GND	GND	GND	-	-
6	3V3/5V*1	3V3/5V*1	3V3/5V*1	-	-
7	GPIO/INT	GPIO/INT	GPIO	P56/IRQ6	50
8	GPIO/RESET	GPIO/RESET	GPIO	PL0	76
9	GPIO/CS2	GPIO	GPIO	P71	86
10	GPIO/CS3	GPIO	GPIO	P72	85
11	GND	GND	GND	-	-
12	3V3/5V*1	3V3/5V*1	3V3/5V*1	-	-

*1: This board allows you to choose between 3V3 and 5V, and the default RSK configuration is 3V3.
*2: This connection is a not available in the default RSK configuration - refer to section 6 for the required modifications.

Table 5-5: Pmod™2 Header Connections

Pin	Pmod™ Interface			MCU	
	Type 2A (SPI)	Type 3A (UART)	Type 6A (I2C)	Port	Pin No.
1	CS	CTS/GPIO	INT	P20/IRQ8	37
2	MOSI	TXD	RESET	P23/TXD3/SMOSI3	34
3	MISO	RXD	SCL	P25/RXD3/SMISO3	32
				PA3/SSCL5*2	94
4	SCK	RTS/GPIO	SDA	P24/SCK3	33
				PA4/SSDA5*2	92
5	GND	GND	GND	-	-
6	3V3/5V*1	3V3/5V*1	3V3/5V*1	-	-
7	GPIO/INT	GPIO/INT	GPIO	P82/IRQ2	63
8	GPIO/RESET	GPIO/RESET	GPIO	P90	131
9	GPIO/CS2	GPIO	GPIO	PB7/TXD9*3	78
10	GPIO/CS3	GPIO	GPIO	PB6/RXD9*3	79
11	GND	GND	GND	-	-
12	3V3/5V*1	3V3/5V*1	3V3/5V*1	-	-

*1: This board allows you to choose between 3V3 and 5V, and the default RSK configuration is 3V3.
*2: This connection is a not available in the default RSK configuration - refer to section 6 for the required modifications.
*3: TXD9 and RXD9 are special assignments for connecting with Renesas Silex WiFi Pmod.

5.7 USB Serial Port

A USB serial port is implemented in a Renesas low power microcontroller (RL78/G1C) and is connected to the RX660 Serial Communications Interface (SCI) module. Multiple options are provided to allow the selection of the connected SCI1 port. Connections between the USB to Serial converter and the microcontroller are listed in **Table 5-6** below.

Table 5-6: Serial Port Connections

Signal Name	Function	MCU	
		Port	Pin
SERIAL-TXD	SCI1 Transmit Signal. [1]	P26	31
	SCI10 Transmit Signal.	P87	39
	External RS232 Transmit Signal. [1]	-	-
SERIAL-RXD	SCI1 Receive Signal. [1]	P30	29
	SCI10 Receive Signal.	P86	41
	External RS232 Receive Signal. [1]	-	-
SERIAL-CTS [2]	Clear To Send.	P15	42
SERIAL-RTS [2]	Request To Send.	P16	40

[1]: This connection is a not available in the default RSK configuration - refer to section 6 for the required modifications.

[2]: Flow control is a signal provided for expansion and is not currently supported. There is no schedule of function expansion at present.

When the CPU board is first connected to a PC running Windows™ with the USB/Serial connection, the PC will look for a driver. This driver is installed during the installation process, so the PC should be able to find it. The PC will report that it is installing a driver and then report that a driver has been installed successfully, as shown in **Figure 5-2**. The exact messages may vary depending upon operating system.
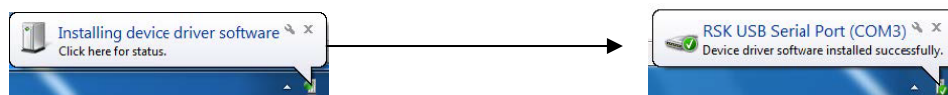
Figure 5-2: USB-Serial Windows™ Installation message

If you do not have the driver, please download the driver installer from the following URL.

https://www.renesas.com/document/rsk-usb-serial-driver?language=en

5.8 Controller Area Network (CAN)

A CAN-FD transceiver IC(Maximum data rate 5Mbps) is fitted to the RSK board, and connected to the CAN MCU peripheral. For further details regarding the CAN protocol and supported modes of operation, please refer to the RX660 Group User's Manual: Hardware. The connections for the CAN microcontroller signals are listed in **Table 5-7** below.

Table 5-7: CAN Connections

CAN Signal	Function	MCU	
		Port	Pin
CAN-TX	CAN Data Transmission.	P32	27
JA5-CAN1TX [1]			
CAN-RX	CAN Data Reception.	P33	26
JA5-CAN1RX [1]			

[1]: This connection is a not available in the default RSK configuration - refer to section 6 for the required modifications.

5.9   Local Interconnect Network (LIN)

A LIN transceiver IC is fitted to the RSK and connected to the Extended serial mode MCU peripheral. For further details regarding the supported modes of operation, please refer to the RX660 Group User's Manual: Hardware. Connections between the LIN connector and microcontroller are listed in **Table 5-8** below.

Table 5-8: LIN Connections

LIN signal	Function	MCU	
		Port	Pin
LIN-TX	LIN Transmit Signal	PE1	110
LIN-RX	LIN Receive Signal	PE2	109
LIN-NSLP	LIN Transceiver Device Sleep Control	PF7	130

5.10   I²C Bus (Inter-IC Bus)

The RX660 features I²C (Inter-IC Bus) interface (RIICa). RIIC0 is connected to a 2Kbit EEPROM. The connections for the I²C Bus Interface signals are listed in **Table 5-9** below.

Table 5-9: I²C Bus Connections

I²C Bus signal	Function	MCU	
		Port	Pin
E2P-SDA	Data	P13	44
E2P-SCL	Clock	P12	45

5.11   Remote Control Signal Receiver

The RSK Board is equipped with a pattern of IR Receiver Module for remote control receive function. IR Receiver Module is not included in the product. Refer to the maker site for specification of the IR Receiver Module (VISHAY with part number TSOP32438). The connections for the remote control receive signals are listed in **Table 5-10** below.

Table 5-10: Remote Control Signal Receiver Connections

SDHI signal	Function	MCU	
		Port	Pin
REMC-PMC0	External pulse signal input	PC5	62

6.   Configuration

6.1   Modifying the RSK

This section lists the option links that are used to modify the way CPU board operates in order to access different configurations. Configurations are made by modifying link resistors or headers with movable jumpers.

A link resistor is a 0Ω surface mount resistor, which is used to short or isolate parts of a circuit. Option links are listed in the following sections, detailing their function when fitted or removed. **Bold, blue text** indicates the default configuration that the CPU board is supplied with. Refer to the component placement diagram (section 3) to locate the option links, jumpers.

> When removing soldered components, always ensure that the CPU board is not exposed to a soldering iron for intervals greater than 5 seconds. This is to avoid damage to nearby components mounted on the board.

> When modifying a link resistor, always check the related option links to ensure there is no possible signal contention or short circuits. Because many of the MCU's pins are multiplexed, some of the peripherals must be used exclusively. Refer to the RX660 Group User's Manual: Hardware and CPU board schematics for further information.

> In the table in this section, "pin" expression is omitted, so please read as follows.
> Example: U5.3 -> U5.3pin

6.2   MCU Operating Modes

Table 6-1 below details the function of the jumpers associated with configuring the MCU Operating Modes.
Table 6-1: MCU Operating Modes Configuration Jumper Settings

J10 [1]	J11 [1]	Explanation
Open	**Open (don't care)**	**Single Chip Mode**
1-2 shorted	Open	SCI Boot Mode
1-2 shorted	1-2 shorted	User Boot Mode

[1]: Jumper J10 and J11 are not mounted on the board at the time of product shipment.

6.3   E2 Lite Debugger Configuration

Table 6-2 below details the function of the option links associated with E2 Lite Debugger Configuration.

Table 6-2: E2 Lite Debugger Configuration Option Links

Signal name	MCU		MCU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
UB	60	PC7	**UB**	-	-	**E2Lite.10**	-	-
						J11.2	-	-
TRSTn	25	P34	**TRSTn**	-	-	**E2Lite.3**	-	-
P31	28	P31	**TMS**	**R167**	**R210**	**E2Lite.9**	-	-
			JA2-CTSaRTSa	R210	R167	JA2.12	-	-
P30	29	P30	**TDI_RXD**	**R168**	**R214, R215**	**E2Lite.11**	-	-
			JA2-RXDa	R214	R168, **R215**	JA2.8	-	-
			SERIAL-RXD	R215	R168, **R214**	U5.3	-	R193, **R192**
P27	30	P27	**TCK**	**R242**	**R212**	**E2Lite.1**	**R116**	-
			JA2-SCKa	R212	R242	JA2.10	-	-
P26	31	P26	**TDO_TXD**	**R166**	**R216, R217**	**E2Lite.5**	-	-
			JA2-TXDa	R216	R166, **R217**	JA2.6	-	-
			SERIAL-TXD	R217	R166, **R216**	U4.3	-	R190, **R191**
RES#	19	-	**RESn**	-	-	**E2Lite.13**	-	-
						RES(Switch)	-	-
						JA2.1	-	-
EMLE	10	-	**EMLE**	-	-	**E2Lite.4**	-	-
						J9.2	-	-
MD_FINED	16	-	**MD_FINED**	-	-	**E2Lite.7**	-	-
						J10.2	-	-

6.4   Power Supply Configuration

Table 6-3 below details the function of the option links associated with Power Supply Configuration.

Table 6-3: Power Supply Configuration Option Links

Reference	Explanation	Fit	DNF
Unregulated_VCC	**Connect 5V power rail to Unregulated_VCC.**	**R108**	-
JA1-5V	**Connect 5V power rail to JA1-5V.**	**R98**	-
Board_5V	**Connect 5V power rail to Board_5V.**	-	-
JA1-3V3	**Disconnect JA1-3V3 from Power Supply IC output. (Power supply source: E2 Lite (3.3V), JA1-3V3)**	**R151**	**J6.Open**
	Connect JA1-3V3 to Power Supply IC output. (Power supply source: Unregulated_VCC, JA1-5V)	**R151,** J6.Short	-
Board_3V3	**Disconnect Board_3V3 from Power Supply IC output. (Power supply source: E2 Lite (3.3V), JA1-3V3)**	**-**	**J6.Open**
	Connect Board_3V3 to Power Supply IC output. (Power supply source: Unregulated_VCC, JA1-5V)	J6.Short	-
UC_VCC	**Connect UC_VCC to Board_VCC power rail.**	J8.Short or **R164**	-
	Enable current probe for measurement MCU current consumption.	-	**J8.Open,** R164

Table 6-4 below details the function of the jumpers associated with the Power Supply Configuration.

Table 6-4: Power Supply Configuration Jumper Settings

Reference	Jumper Position	Explanation
J8(DNF) [1]	**Shorted**	**Connect UC_VCC to Board_VCC power rail.**
	All open	Enable current probe for measurement MCU current consumption.
J7	**Shorted Pin 1-2**	**Connect Board_3V3 to Board_VCC.**
	Shorted Pin 2-3	Connect Board_5V to Board_VCC.
	All open	DO NOT SET.
J6	Shorted	Connect Power Supply IC output to Board_3V3.
	All open	**Disconnect Power Supply IC output from Board_3V3.**

[1]: Jumper J8 is not fitted on the default CPU board. Same as Jumper Position "shorted" setting by resistor R164.

6.5   Clock Configuration

Table 6-5 below details the function of the option links associated with Clock Configuration.

Table 6-5: Clock Configuration Option Links

Reference	Explanation	Fit	DNF
XTAL, EXTAL	**Connect 24MHz crystal (X1) to RX660.**	**R90, R88**	**R83, R94**
	Connect JA2-EXTAL to RX660.	R83, R94	R90, R88
XCIN, XCOUT	**Connect 32.768kHz crystal (X2) to RX660.**	**R95, R96**	**R106**
	Disconnect X2 from RX660.	R106	R95, R96

6.6   Analog Power, ADC and DAC Configuration

Table 6-6 below details the function of the option links associated with Analog Power, ADC and DAC Configuration.

Table 6-6: Analog Power, ADC and DAC Configuration Option Links

Signal name	MCU		MCU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
P07	144	P07	SW3	R84	R80, R7	SW3	-	-
			JA1-ADTRG	R80	R84, R7	JA1.8	-	-
			JA1-IRQd	R7	R84, R80	JA1.23	-	-
JA5-ADC7	133	P47	JA5-ADC7	-	-	JA5.4	-	-
JA5-ADC6	134	P46	JA5-ADC6	-	-	JA5.3	-	-
JA5-ADC5	135	P45	JA5-ADC5	-	-	JA5.2	-	-
JA5-ADC4	136	P44	JA5-ADC4	-	-	JA5.1	-	-
JA1-ADC3	137	P43	JA1-ADC3	-	-	JA1.12	-	-
JA1-ADC2	138	P42	JA1-ADC2	-	-	JA1.11	-	-
JA1-ADC1	139	P41	JA1-ADC1	-	-	JA1.10	-	-
P40	141	P40	RV1-ADC	R85	R81	RV1	-	-
			JA1-ADC0	R81	R85	JA1.9	-	-
VREFH0	142	PJ6	UC_VCC	R136	R137	-	-	-
			JA1-VREFH	R137	R136	JA1.7	-	-
VREFL0	140	PJ7	GROUND	R142	R143	-	-	-
			JA1-AVSS_VREFL	R143	R142	JA1.6	-	-
AVCC0	143	-	UC_VCC	R111	R112, R218	-	-	-
			JA1-AVCC	R112	R111, R218	JA1.5	-	-
			Board_VCC	R219, R218	R111, R112	-	-	-
AVSS0	1	-	GROUND	R102	R103	-	-	-
			JA1-AVSS_VREFL	R103	R102	JA1.6	-	-
JA1-DAC0	4	P03	JA1-DAC0	-	-	JA1.13	-	-
JA1-DAC1	2	P05	JA1-DAC1	-	-	JA1.14	-	-

6.7 BUS Configuration

This board is designed to be shared with other microcontrollers. Therefore, RX660 does not support SDRAM controller, but SDRAM signals are assigned to Application Header JA3 and Microcontroller Pin Headers.
The affected signals are: JA3-DQMH, JA3-DQML, JA3-SDCLK, JA3-CKE, JA3-WEn, JA3-RAS, JA3-CAS

Table 6-7 and **Table 6-8** below details the function of the option links associated with BUS Configuration.

Table 6-7: BUS Configuration Option Links (1)

Signal name	MCU		MCU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
P55	51	P55	**JA2-M1WN**	**R204**	**R64**	**JA2.18**	-	-
			JA3-WAIT	R64	R204	JA3.45	R65	R58
P54	52	P54	**JA2-M1WP**	**R203**	**R69**	**JA2.17**	-	-
			JA3-ALE	R69	R203	JA3.46	**R70**	**R68**
P53	53	P53	**JA3-BCLK**	**R76**	-	**JA3.44**	**R77**	**R72**
JA3-RDn	54	P52	**JA3-RDn**	-	-	**JA3.25**	-	-
JA3-WRHn	55	P51	**JA3-WRHn**	-	-	**JA3.47**	**R26**	**R35**
P50	56	P50	**JA3-WRLn**	**R55**	**R128**	**JA3.48**	**R56**	**R40**
			JA3-WRn	R128	R55	JA3.26	**R124**	**R123**
JA3-A20	66	PC4	**JA3-A20**	-	-	**JA3.41**	-	-
JA3-A19	67	PC3	**JA3-A19**	-	-	**JA3.40**	-	-
PC2	70	PC2	**JA6-TXDB011**	**R182**	**R86**	**JA6.17**	-	-
			JA3-A18	R86	R182	JA3.39	-	-
PC1	73	PC1	**JA6-TXDA011**	**R181**	**R89**	**JA6.19**	-	-
			JA3-A17	R89	R181	JA3.38	-	-
PC0	75	PC0	**JA2-M1UD**	**R209**	**R93**	**JA2.11**	-	-
			JA3-A16	R93	R209	JA3.37	-	-
JA3-CSc	77	P73	**JA3-CSc**		-	**JA3.45**	**R58**	**R65**
P70	104	P70	JA3-SDCLK	**R170**	-	JA3.44	R72	R77
PB7	78	PB7	**PMOD2-IO6_CS1_WIFITXD**	**R12**	**R207, R145**	**PMOD2.9**	-	-
			JA2-M1UP	R207	R12, **R145**	JA2.13	-	-
			JA3-A15	R145	R12, **R207**	JA3.16	-	-
PB6	79	PB6	**PMOD2-IO7_CS2_WIFIRXD**	**R227**	**R208, R146**	**PMOD2.10**	-	-
			JA2-M1UN	R208	R227, **R146**	JA2.14	-	-
			JA3-A14	R146	R227, **R208**	JA3.15	-	-
PB5	80	PB5	**JA3-A13**	**R147**	**R195**	**JA3.14**	-	-
			JA2-M1ENC	R195	R147	JA2.23	R196	R198
PB4	81	PB4	**JA6-DE011**	**R180**	**R150**	**JA6.21**	-	-
			JA3-A12	R150	R180	JA3.13	-	-
PB3	82	PB3	**JA2-IRQa_M1HSIN0**	**R213**	**R153**	**JA2.7**	-	-
			JA3-A11	R153	R213	JA3.12	-	-
JA3-A10	83	PB2	**JA3-A10**	-	-	**JA3.11**	-	-
PB1	84	PB1	**JA2-IRQc_M1HSIN2**	**R197**	**R156, R230**	**JA2.23**	**R198**	**R196**
			JA3-A9	R156	R197, **R230**	JA3.10	-	-
			PMOD1-SDA	R230	R197, **R156**	PMOD1.4	R234	R233
PB0	87	PB0	**JA6-M1WIN**	**R184**	**R161, R232**	**JA6.16**	-	-
			JA3-A8	R161	R184, **R232**	JA3.9	-	-
			PMOD1-SCL	R232	R184, **R161**	PMOD1.3	R236	R235

Table 6-8: BUS Configuration Option Links (2)

Signal name	MCU		MCU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
JA3-A7	88	PA7	JA3-A7	-	-	JA3.8	-	-
PA6	89	PA6	JA6-M1VIN	R183	R162	JA6.15	-	-
			JA3-A6	R162	R183	JA3.7	-	-
JA3-A5	90	PA5	JA3-A5	-	-	JA3.6	-	-
PA4	92	PA4	JA6-M1UIN	R186	R171, R4	JA6.14	-	-
			JA3-A4	R171	R186, R4	JA3.5	-	-
			PMOD2-SDA	R4	R186, R171	PMOD2.4	R3	R9
PA3	94	PA3	JA3-A3	R172	R22	JA3.4	-	-
			PMOD2-SCL	R22	R172	PMOD2.3	R21	R31
JA3-A2	95	PA2	JA3-A2	-	-	JA3.3	-	-
PA1	96	PA1	JA2-IRQb_M1HSIN1	R211	R173	JA2.9	-	-
			JA3-A1	R173	R211	JA3.2	-	-
PA0	97	PA0	JA2-M1VP	R205	R175	JA2.15	-	-
			JA3-A0	R175	R205	JA3.1	-	-
P67	98	P67	JA2-TIMIN0	R199	R34	JA2.21	-	-
			JA3-DQMH	R34	R199	JA3.47	R35	R26
P66	99	P66	JA2-TIMIN1	R200	R39	JA2.22	-	-
			JA3-DQML	R39	R200	JA3.48	R40	R56
JA3-CKE	100	P65	JA3-CKE	-	-	JA3.46	R68	R70
JA3-WEn	112	P64	JA3-WEn	-	-	JA3.26	R123	R124
P63	113	P63	JA3-CAS	-	-	JA3.49	-	-
P62	114	P62	JA3-RAS	-	-	JA3.50	-	-
P60	117	P60	JA5-IRQe	R228	R114	JA5.9	-	-
			JA3-CSa	R114	R228	JA3.27	-	-
PE7	101	PE7	JA2-TIMOUT0	R201	R97	JA2.19	-	-
			JA3-D15	R97	R201	JA3.36	-	-
PE6	102	PE6	JA2-TIMOUT1	R202	R104	JA2.20	-	-
			JA3-D14	R104	R202	JA3.35	-	-
JA3-D13	106	PE5	JA3-D13	-	-	JA3.34	-	-
JA3-D12	107	PE4	JA3-D12	-	-	JA3.33	-	-
JA3-D11	108	PE3	JA3-D11	-	-	JA3.32	-	-
PE2	109	PE2	LIN-RX	R134	R107	U8.1	-	-
			JA3-D10	R107	R134	JA3.31	-	-
PE1	110	PE1	LIN-TX	R133	R113	U8.4	-	-
			JA3-D9	R113	R133	JA3.30	-	-
JA3-D8	111	PE0	JA3-D8	-	-	JA3.29	-	-
JA3-CSb	115	P61	JA3-CSb	-	-	JA3.28	-	-
JA3-D7	119	PD7	JA3-D7	-	-	JA3.24	-	-
JA3-D6	120	PD6	JA3-D6	-	-	JA3.23	-	-
JA3-D5	121	PD5	JA3-D5	-	-	JA3.22	-	-
JA3-D4	122	PD4	JA3-D4	-	-	JA3.21	-	-
JA3-D3	123	PD3	JA3-D3	-	-	JA3.20	-	-
JA3-D2	124	PD2	JA3-D2	-	-	JA3.19	-	-
JA3-D1	125	PD1	JA3-D1	-	-	JA3.18	-	-
JA3-D0	126	PD0	JA3-D0	-	-	JA3.17	-	-

6.8   CAN Configuration

Table 6-9 below details the function of the option links associated with CAN Configuration.

Table 6-9: CAN Configuration Option Links

Signal name	MCU		MCU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
P33	26	P33	CAN-RX	R78	R74	U7.4	-	-
			JA5-CAN1RX	R74	R78	JA5.6	-	-
P32	27	P32	CAN-TX	R79	R75	U7.1	-	-
			JA5-CAN1TX	R75	R79	JA5.5	-	-

6.9   General IO & LED Configuration

Table 6-10 below details the function of the option links associated with General IO & LED Configuration.

Table 6-10: General IO & LED Configuration Option Links

Signal name	MCU		MCU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
LED3	3	P06	LED3	-	-	LED3.K	R165	-
LED2	5	P04	LED2	-	-	LED2.K	R165	-
LED1	9	PF5	LED1	-	-	LED1.K	R165	-
P17	38	P17	LED0	R138	-	LED0.K	R165	-
			JA6-M1TOGGLE	R185	-	JA6.13	-	-
JA1-IO3	35	P22	JA1-IO3	-	-	JA1.18	-	-
JA1-IO2	36	P21	JA1-IO2	-	-	JA1.17	-	-
JA1-IO1	11	PJ5	JA1-IO1	-	-	JA1.16	-	-
JA1-IO0	12	PJ4	JA1-IO0	-	-	JA1.15	-	-
JA1-IO7	103	PK5	JA1-IO7	-	-	JA1.22	-	-
JA1-IO6	105	PK4	JA1-IO6	-	-	JA1.21	-	-
JA1-IO5	116	PK3	JA1-IO5	-	-	JA1.20	-	-
JA1-IO4	118	PK2	JA1-IO4	-	-	JA1.19	-	-

6.10 I2C & EEPROM Configuration

Table 6-11 and **Table 6-12** below detail the function of the option links associated with I2C & EEPROM Configuration.

Table 6-11: I2C & EEPROM Configuration Option Links (1)

Signal name	MCU		MCU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
P12	45	P12	**E2P-SCL**	**R27**	-	**U6.6**	-	-
			JA1-SCL	**R5**	-	**JA1.26**	-	-
P13	44	P13	**E2P-SDA**	**R14**	-	**U6.5**	-	-
			JA1-SDA	**R6**	-	**JA1.25**	-	-

Table 6-12: I2C & EEPROM Configuration Option Links (2)

Reference	Explanation	Fit	DNF
EEPROM Power	**Supply Board_3V3 and connect pull-up resistor to Board_3V3.**	**R54**	**R38**
	Supply Board_5V and connect pull-up resistor to Board_5V.	R38	R54
WP	**Disable EEPROM Write protect**	**-**	**R36**
	Enable EEPROM Write protect	R36	-
A0, A1, A2	**Device address (0xA6).**	**R33, R24, R17**	**R32, R23, R18**
	Device address (0xA4).	R32, **R24, R17**	R33, **R23, R18**

6.11 IRQ & Switch Configuration

Table 6-13 below details the function of the option links associated with IRQ & Switch Configuration.

Table 6-13: IRQ & Switch Configuration Option Links

Signal name	MCU		MCU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
P07	144	P07	**SW3**	**R84**	**R80, R7**	**SW3**	-	-
			JA1-ADTRG	R80	R84, **R7**	JA1.8	-	-
			JA1-IRQd	R7	R84, **R80**	JA1.23	-	-
P35	24	P35	**JA2-NMIn**	-	-	**JA2.3**	-	-
SW2	128	P92	**SW2**	-	-	**SW2**	-	-
SW1	129	P91	**SW1**	-	-	**SW1**	-	-
PA1	96	PA1	**JA2-IRQb_M1HSIN1**	**R211**	**R173**	**v**	-	-
			JA3-A1	R173	R211	JA3.2	-	-
PB3	82	PB3	**JA2-IRQa_M1HSIN0**	**R213**	**R153**	**JA2.7**	-	-
			JA3-A11	R153	R213	JA3.12	-	-
PB1	84	PB1	**JA2-IRQc_M1HSIN2**	**R197**	**R156, R230**	**JA2.23**	**R198**	**R196**
			JA3-A9	R156	R197, **R230**	JA3.10	-	-
			PMOD1-SDA	R230	R197, **R156**	PMOD1.4	R234	R233
RES#	19	-	**RESn**	-	-	**E2Lite.13**	-	-
						RES(Switch)	-	-
						JA2.1	-	-
JA5-IRQf	47	PH2	**JA5-IRQf**	-	-	**JA5.10**	-	-
P60	117	P60	**JA5-IRQe**	**R228**	**R114**	**JA5.9**	-	-
			JA3-CSa	R114	R228	JA3.27	-	-

6.12 MTU & POE & Timer Configuration

Table 6-14 below details the function of the option links associated with MTU & POE & Timer Configuration.

Table 6-14: MTU & POE & Timer Configuration Option Links

Signal name	MCU		MCU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
P17	38	P17	LED0	R138	-	LED0.K	R165	-
			JA6-M1TOGGLE	R185	-	JA6.13	-	-
P15	42	P15	JA2-M1TRDCLK	R194	R87	JA2.26	-	-
			SERIAL-CTS	R87	R194	U5.2	-	-
JA2-M1TRCCLK	43	P14	JA2-M1TRCCLK	-	-	JA2.25	-	-
P55	51	P55	JA2-M1WN	R204	R64	JA2.18	-	-
			JA3-WAIT	R64	R204	JA3.45	R65	R58
P54	52	P54	JA2-M1WP	R203	R69	JA2.17	-	-
			JA3-ALE	R69	R203	JA3.46	R70	R68
P83	58	P83	JA2-M1VN	R206	R187	JA2.16	-	-
			JA6-SCKb	R187	R206	JA6.10	-	-
JA2-M1POE	127	P93	JA2-M1POE	-	-	JA2.24	-	-
PA6	89	PA6	JA6-M1VIN	R183	R162	JA6.15	-	-
			JA3-A6	R162	R183	JA3.7	-	-
PA4	92	PA4	JA6-M1UIN	R186	R171, R4	JA6.14	-	-
			JA3-A4	R171	R186, R4	JA3.5	-	-
			PMOD2-SDA	R4	R186, R171	PMOD2.4	R3	R9
PA1	96	PA1	JA2-IRQb_M1HSIN1	R211	R173	JA2.9	-	-
			JA3-A1	R173	R211	JA3.2	-	-
PA0	97	PA0	JA2-M1VP	R205	R175	JA2.15	-	-
			JA3-A0	R175	R205	JA3.1	-	-
PB7	78	PB7	PMOD2-IO6_CS1_WIFITXD	R12	R207, R145	PMOD2.9	-	-
			JA2-M1UP	R207	R12, R145	JA2.13	-	-
			JA3-A15	R145	R12, R207	JA3.16	-	-
PB6	79	PB6	PMOD2-IO7_CS2_WIFIRXD	R227	R208, R146	PMOD2.10	-	-
			JA2-M1UN	R208	R227, R146	JA2.14	-	-
			JA3-A14	R146	R227, R208	JA3.15	-	-
PB5	80	PB5	JA3-A13	R147	R195	JA3.14	-	-
			JA2-M1ENC	R195	R147	JA2.23	R196	R198
PB3	82	PB3	JA2-IRQa_M1HSIN0	R213	R153	JA2.7	-	-
			JA3-A11	R153	R213	JA3.12	-	-
PB1	84	PB1	JA2-IRQc_M1HSIN2	R197	R156, R230	JA2.23	R198	R196
			JA3-A9	R156	R197, R230	JA3.10	-	-
			PMOD1-SDA	R230	R197, R156	PMOD1.4	R234	R233
PB0	87	PB0	JA6-M1WIN	R184	R161, R232	JA6.16	-	-
			JA3-A8	R161	R184, R232	JA3.9	-	-
			PMOD1-SCL	R232	R184, R161	PMOD1.3	R236	R235
PC0	75	PC0	JA2-M1UD	R209	R93	JA2.11	-	-
			JA3-A16	R93	R209	JA3.37	-	-
PE7	101	PE7	JA2-TIMOUT0	R201	R97	JA2.19	-	-
			JA3-D15	R97	R201	JA3.36	-	-
PE6	102	PE6	JA2-TIMOUT1	R202	R104	JA2.20	-	-
			JA3-D14	R104	R202	JA3.35	-	-
P67	98	P67	JA2-TIMIN0	R199	R34	JA2.21	-	-
			JA3-DQMH	R34	R199	JA3.47	R35	R26
P66	99	P66	JA2-TIMIN1	R200	R39	JA2.22	-	-
			JA3-DQML	R39	R200	JA3.48	R40	R56

6.13 PMOD1 Configuration

Table 6-15 below details the function of the option links associated with PMOD1 Configuration.

Table 6-15: PMOD1 Configuration Option Links

Signal name	MCU Pin	MCU Port	MCU Peripheral Selection Signal	Fit	DNF	Destination Selection Interface /Function	Fit	DNF
PMOD1-IO3_SCK_RTS	6	P02	PMOD1-IO3_SCK_RTS	-	-	PMOD1.4	R233	R234
PMOD1-IO2_MISO_RXD	7	P01	PMOD1-IO2_MISO_RXD	-	-	PMOD1.3	R235	R236
PMOD1-IO1_MOSI_TXD_RESET0	8	P00	PMOD1-IO1_MOSI_TXD_RESET0	-	-	PMOD1.2	-	-
PMOD1-IO4_INT1	50	P56	PMOD1-IO4_INT1	-	-	PMOD1.7	-	-
PMOD1-IO5_RESET1	72	P74	PMOD1-IO5_RESET1	-	-	PMOD1.8	-	-
PMOD1-IO7_CS2	85	P72	PMOD1-IO7_CS2	-	-	PMOD1.10	-	-
PMOD1-IO6_CS1	86	P71	PMOD1-IO6_CS1	-	-	PMOD1.9	-	-
PMOD1-IO0_CS0_CTS_INT0	13	PJ3	PMOD1-IO0_CS0_CTS_INT0	-	-	PMOD1.1	-	-
PB1	84	PB1	JA2-IRQc_M1HSIN2	R197	R156, R230	JA2.23	R198	R196
			JA3-A9	R156	R197, R230	JA3.10	-	-
			PMOD1-SDA	R230	R197, R156	PMOD1.4	R234	R233
PB0	87	PB0	JA6-M1WIN	R184	R161, R232	JA6.16	-	-
			JA3-A8	R161	R184, R232	JA3.9	-	-
			PMOD1-SCL	R232	R184, R161	PMOD1.3	R236	R235

6.14 PMOD2 Configuration

Table 6-16 below details the function of the option links associated with PMOD2 Configuration.

Table 6-16: PMOD2 Configuration Option Links

Signal name	MCU Pin	MCU Port	MCU Peripheral Selection Signal	Fit	DNF	Destination Selection Interface /Function	Fit	DNF
PMOD2-IO1_MOSI_TXD_RESET0	34	P23	PMOD2-IO1_MOSI_TXD_RESET0	-	-	PMOD2.2	-	-
PMOD2-IO2_MISO_RXD	32	P25	PMOD2-IO2_MISO_RXD	-	-	PMOD2.3	R31	R21
PB6	79	PB6	PMOD2-IO7_CS2_WIFIRXD	R227	R208, R146	PMOD2.10	-	-
			JA2-M1UN	R208	R227, R146	JA2.14	-	-
			JA3-A14	R146	R227, R208	JA3.15	-	-
PB7	78	PB7	PMOD2-IO6_CS1_WIFITXD	R12	R207, R145	PMOD2.9	-	-
			JA2-M1UP	R207	R12, R145	JA2.13	-	-
			JA3-A15	R145	R12, R207	JA3.16	-	-
PMOD2-IO3_SCK_RTS	33	P24	PMOD2-IO3_SCK_RTS	-	-	PMOD2.4	R9	R3
PMOD2-IO4_INT1_WIFIWKUP	63	P82	PMOD2-IO4_INT1_WIFIWKUP	-	-	PMOD2.7	-	-
PMOD2-IO5_RESET1_WIFIMDRES	131	P90	PMOD2-IO5_RESET1_WIFIMDRES	-	-	PMOD2.8	-	-
PMOD2-IO0_CS0_CTS_INT0	37	P20	PMOD2-IO0_CS0_CTS_INT0	-	-	PMOD2.1	-	-
PA4	92	PA4	JA6-M1UIN	R186	R171, R4	JA6.14	-	-
			JA3-A4	R171	R186, R4	JA3.5	-	-
			PMOD2-SDA	R4	R186, R171	PMOD2.4	R3	R9
PA3	94	PA3	JA3-A3	R172	R22	JA3.4	-	-
			PMOD2-SCL	R22	R172	PMOD2.3	R21	R31

6.15 Serial & USB to Serial Configuration

Table 6-17 below details the function of the option links associated with Serial & USB to Serial Configuration.

Table 6-17: Serial & USB to Serial Configuration Option Links

Signal name	MCU		MCU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
P30	29	P30	**TDI_RXD**	**R168**	**R214, R215**	**E2Lite.11**	-	-
			JA2-RXDa	R214	R168, **R215**	JA2.8	-	-
			SERIAL-RXD	R215	R168, **R214**	U5.3	-	R193, **R192**
P26	31	P26	**TDO_TXD**	**R166**	**R216, R217**	**E2Lite.5**	-	-
			JA2-TXDa	R216	R166, **R217**	JA2.6	-	-
			SERIAL-TXD	R217	R166, **R216**	U4.3	-	R190, **R191**
P87	39	P87	**SERIAL-TXD**	**R190**	**R189**	**U4.3**	-	**R217, R191**
			JA6-TXDb	R189	R190	JA6.8	-	-
SERIAL-RTS	40	P16	**SERIAL-RTS**	-	-	**U4.2**	-	-
P86	41	P86	**SERIAL-RXD**	**R193**	**R188**	**U5.3**	-	**R215, R192**
			JA6-RXDb	R188	R193	JA6.7	-	-
P15	42	P15	**JA2-M1TRDCLK**	**R194**	**R87**	**JA2.26**	-	-
			SERIAL-CTS	R87	R194	U5.2	-	-
JA6-TXDc	68	P77	**JA6-TXDc**	-	-	**JA6.9**	-	-
JA6-RXDc	69	P76	**JA6-RXDc**	-	-	**JA6.12**	-	-
JA6-SCKc	71	P75	**JA6-SCKc**	-	-	**JA6.11**	-	-
PC2	70	PC2	**JA6-TXDB011**	**R182**	**R86**	**JA6.17**	-	-
			JA3-A18	R86	R182	JA3.39	-	-
PC1	73	PC1	**JA6-TXDA011**	**R181**	**R89**	**JA6.19**	-	-
			JA3-A17	R89	R181	JA3.38	-	-
PB4	81	PB4	**JA6-DE011**	**R180**	**R150**	**JA6.21**	-	-
			JA3-A12	R150	R180	JA3.13	-	-
JA6-CTS011	72	P74	**JA6-CTS011**	-	-	**JA6.22**	-	-
-	-	-	JA6-RS232RX	R192	**-**	U5.3	-	R193, **R215**
-	-	-	JA6-RS232TX	R191	**-**	U4.3	-	R190, **R217**

6.16 LIN Configuration

Table 6-18 and **Table 6-19** below details the function of the option links associated with LIN Configuration.

Table 6-18: LIN Configuration Option Links (1)

Signal name	MCU		MCU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
LIN-NSLP	130	PF7	**LIN-NSLP**	-	-	**U8.2**	-	-
PE1	110	PE1	**LIN-TX**	**R133**	**R113**	**U8.4**	-	-
			JA3-D9	R113	R133	JA3.30	-	-
PE2	109	PE2	**LIN-RX**	**R134**	**R107**	**U8.1**	-	-
			JA3-D10	R107	R134	JA3.31	-	-

Table 6-19: LIN Configuration Option Links (2)

Reference	Explanation	Fit	DNF
LIN Operating Mode	**Master mode**	**R154, R160**	-
	Slave mode	-	R154, R160

6.17 Remote Control Signal Receiver Configuration

Table 6-20 below details the function of the option links associated with Remote Control Signal Receiver Configuration.

Table 6-20: Remote Control Signal Receiver Option Links

Signal name	MCU		MCU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
REMC-PMC0	62	PC5	REMC-PMC0	R178	-	U9.1	U9	-

7. Headers

This board is designed to be shared with other microcontrollers. Therefore, RX660 does not support SDRAM controller, but SDRAM signals are assigned to Application Header JA3 and Microcontroller Pin Headers.
The affected signals are: JA3-DQMH, JA3-DQML, JA3-SDCLK, JA3-CKE, JA3-WEn, JA3-RAS, JA3-CAS

7.1   Application Headers

This RSK board is fitted with application headers, which can be used to connect compatible Renesas application devices or as easy access to MCU pins.

Table 7-1 below lists the connections of the application header, JA1.

Table 7-1: Application Header JA1 Connections

Application Header JA1					
Pin	**Header Name** / **Circuit Net Name**	**MCU Pin**	**Pin**	**Header Name** / **Circuit Net Name**	**MCU Pin**
1	5V / JA1-5V	-	2	0V / GROUND	-
3	3V3 / JA1-3V3	-	4	0V / GROUND	-
5	AVCC / JA1-AVCC	143	6	AVSS / JA1-AVSS_VREFL	1, 140
7	AVREF / JA1-VREFH	142	8	ADTRG / JA1-ADTRG	144
9	ADC0 / JA1-ADC0	141	10	ADC1 / JA1-ADC1	139
11	ADC2 / JA1-ADC2	138	12	ADC3 / JA1-ADC3	137
13	DAC0 / JA1-DAC0	4	14	DAC1 / JA1-DAC1	2
15	IO_0 / JA1-IO0	12	16	IO_1 / JA1-IO1	11
17	IO_2 / JA1-IO2	36	18	IO_3 / JA1-IO3	35
19	IO_4 / JA1-IO4	118	20	IO_5 / JA1-IO5	116
21	IO_6 / JA1-IO6	105	22	IO_7 / JA1-IO7	103
23	IRQd / IRQAEC / M2_HSIN0 / JA1-IRQd	144 / NC / 144	24	IIC_EX / NC	NC
25	IIC_SDA / JA1-SDA	44	26	IIC_SCL / JA1-SCL	45

Table 7-2 below lists the connections of the application header, JA2.

Table 7-2: Application Header JA2 Connections

Application Header JA2					
Pin	**Header Name**	**MCU Pin**	**Pin**	**Header Name**	**MCU Pin**
	Circuit Net Name			**Circuit Net Name**	
1	RESET	19	2	EXTAL	22
	RESn			JA2-EXTAL	
3	NMI	24	4	Vss1	-
	JA2-NMIn			GROUND	
5	WDT_OVF	NC	6	SCIaTX	31
	NC			JA2-TXDa	
7	IRQa / WKUP / M1_HSIN0	82 / NC / 82	8	SCIaRX	29
	JA2-IRQa_M1HSIN0			JA2-RXDa	
9	IRQb / M1_HSIN1	96 / 96	10	SCIaCK	30
	JA2-IRQb_M1HSIN1			JA2-SCKa	
11	M1_UD	75	12	CTSaRTSa	28
	JA2-M1UD			JA2-CTSaRTSa	
13	M1_UP	78	14	M1_UN	79
	JA2-M1UP			JA2-M1UN	
15	M1_VP	97	16	M1_VN	58
	JA2-M1VP			JA2-M1VN	
17	M1_WP	52	18	M1_WN	51
	JA2-M1WP			JA2-M1WN	
19	TimerOut0	101	20	TimerOut1	102
	JA2-TIMOUT0			JA2-TIMOUT1	
21	TimerIn0	98	22	TimerIn1	99
	JA2-TIMIN0			JA2-TIMIN1	
23	IRQc / M1_EncZ / M1_HSIN2	84 / 80 / 84	24	M1_POE	127
	JA2-23PIN			JA2-M1POE	
25	M1_TRCCLK	43	26	M1_TRDCLK	42
	JA2-M1TRCCLK			JA2-M1TRDCLK	

Table 7-3 below lists the connections of the application header, JA3.

Table 7-3: Application Header JA3 Connections

	Application Header JA3 (Bus)					
Pin	**Header Name**	**MCU Pin**	**Pin**	**Header Name**	**MCU Pin**
	Circuit Net Name			**Circuit Net Name**	
1	A0	97	2	A1	96
	JA3-A0			JA3-A1	
3	A2	95	4	A3	94
	JA3-A2			JA3-A3	
5	A4	92	6	A5	90
	JA3-A4			JA3-A5	
7	A6	89	8	A7	88
	JA3-A6			JA3-A7	
9	A8	87	10	A9	84
	JA3-A8			JA3-A9	
11	A10	83	12	A11	82
	JA3-A10			JA3-A11	
13	A12	81	14	A13	80
	JA3-A10			JA3-A13	
15	A14	79	16	A15	78
	JA3-A14			JA3-A15	
17	D0	126	18	D1	125
	JA3-D0			JA3-D1	
19	D2	124	20	D3	123
	JA3-D2			JA3-D3	
21	D4	122	22	D5	121
	JA3-D4			JA3-D5	
23	D6	120	24	D7	119
	JA3-D6			JA3-D7	
25	RDn	54	26	WR / SDWE	56 / 112
	JA3-RDn			JA3-26PIN	
27	CSa	117	28	CSb	115
	JA3-CSa			JA3-CSb	
29	D8	111	30	D9	110
	JA3-D8			JA3-D9	
31	D10	109	32	D11	108
	JA3-D10			JA3-D11	
33	D12	107	34	D13	106
	JA3-D12			JA3-D13	
35	D14	102	36	D15	101
	JA3-D14			JA3-D15	
37	A16	75	38	A17	73
	JA3-A16			JA3-A17	
39	A18	70	40	A19	67
	JA3-A18			JA3-A19	
41	A20	66	42	A21	NC
	JA3-A20			NC	
43	A22	NC	44	BCLK / SDCLK	53 / 104
	NC			JA3-44PIN	
45	CSc / Wait	77 / 55	46	ALE / SDCKE	52 / 100
	JA3-45PIN			JA3-46PIN	
47	HWRn / DQMH	55 / 98	48	LWRn / DQML	56 / 99
	JA3-47PIN			JA3-48PIN	
49	CAS	113	50	RAS	114
	JA3-CAS			JA3-RAS	

Table 7-4 below lists the connections of the application header, JA5.

Table 7-4: Application Header JA5 Connections

	Application Header JA5					
Pin	**Header Name**	**MCU Pin**	**Pin**	**Header Name**	**MCU Pin**
	Circuit Net Name			**Circuit Net Name**	
1	ADC4	136	2	ADC5	135
	JA5-ADC4			JA5-ADC5	
3	ADC6	134	4	ADC7	133
	JA5-ADC6			JA5-ADC7	
5	CAN1TX	27	6	CAN1RX	26
	JA5-CAN1TX			JA5-CAN1RX	
7	CAN2TX	NC	8	CAN2RX	NC
	NC			NC	
9	IRQe / M2_EncZ / M2HSIN1	117 / NC / NC	10	IRQf / M2_HSIN2	47 / NC
	JA5-IRQe			JA5-IRQf	
11	M2_UD	NC	12	M2_Uin	NC
	NC			NC	
13	M2_Vin	NC	14	M2_Win	NC
	NC			NC	
15	M2_Toggle	NC	16	M2_POE	NC
	NC			NC	
17	M2_TRCCLK	NC	18	M2_TRDCLK	NC
	NC			NC	
19	M2_UP	NC	20	M2_UN	NC
	NC			NC	
21	M2_VP	NC	22	M2_VN	NC
	NC			NC	
23	M2_WP	NC	24	M2_WN	NC
	NC			NC	

Table 7-5 below lists the connections of the application header, JA6.

Table 7-5: Application Header JA6 Connections

Pin	Header Name / Circuit Net Name	MCU Pin	Pin	Header Name / Circuit Net Name	MCU Pin
	Application Header JA6				
1	DREQ / NC	NC	2	DACK / NC	NC
3	TEND / NC	NC	4	STBYn / NC	NC
5	RS232TX / JA6-RS232TX	NC	6	RS232RX / JA6-RS232RX	NC
7	SCIbRX / JA6-RXDb	41	8	SCIbTX / JA6-TXDb	39
9	SCIcTX / JA6-TXDc	68	10	SCIbCK / JA6-SCKb	58
11	SCIcCK / JA6-SCKc	71	12	SCIcRX / JA6-RXDc	69
13	M1_Toggle / JA6-M1TOGGLE	38	14	M1_Uin / JA6-M1UIN	92
15	M1_Vin / JA6-M1VIN	89	16	M1_Win / JA6-M1WIN	87
17	Features for RX660 only / JA6-TXDB011	70	18	Reserved / NC	NC
19	Features for RX660 only / JA6-TXDA011	73	20	Reserved / NC	NC
21	Features for RX660 only / JA6-DE011	81	22	EX_RX660_CTS011 / JA6-CTS011	72
23	Unregulated_VCC / Unregulated_VCC	-	24	Vss / GROUND	-

7.2   Microcontroller Pin Headers

This RSK is fitted with MCU pin headers, which are used to access all the MCU's pins.
Table 7-6 below lists the connections of the microcontroller pin header, J1.

Table 7-6: Microcontroller Pin Header, J1

Microcontroller Pin Header J1					
Pin	Circuit Net Name	MCU Pin	Pin	Circuit Net Name	MCU Pin
1	AVSS0	1	2	JA1-DAC1	2
3	LED3	3	4	JA1-DAC0	4
5	LED2	5	6	PMOD1-IO3_SCK_RTS	6
7	PMOD1-IO2_MISO_RXD	7	8	PMOD1-IO1_MOSI_TXD_RESET0	8
9	LED1	9	10	EMLE	10
11	JA1-IO1	11	12	JA1-IO0	12
13	PMOD1-IO0_CS0_CTS_INT0	13	14	NC	NC
15	PJ1	15	16	MD_FINED	16
17	NC	NC	18	NC	NC
19	RESn	19	20	J1-20	20
21	GROUND	-	22	JA2-EXTAL	22
23	UC_VCC	-	24	JA2-NMIn	24
25	TRSTn	25	26	P33	26
27	P32	27	28	P31	28
29	P30	29	30	P27	30
31	P26	31	32	PMOD2-IO2_MISO_RXD	32
33	PMOD2-IO3_SCK_RTS	33	34	PMOD2-IO1_MOSI_TXD_RESET0	34
35	JA1-IO3	35	36	JA1-IO2	36

Table 7-7 below lists the connections of the microcontroller pin header, J2.

Table 7-7: Microcontroller Pin Header, J2

Microcontroller Pin Header J2					
Pin	Circuit Net Name	MCU Pin	Pin	Circuit Net Name	MCU Pin
1	PMOD2-IO0_CS0_CTS_INT0	37	2	P17	38
3	P87	39	4	SERIAL-RTS	40
5	P86	41	6	P15	42
7	JA2-M1TRCCLK	43	8	P13	44
9	P12	45	10	J2-10	46
11	JA5-IRQf	47	12	PH1	48.
13	J2-13	49	14	PMOD1-IO4_INT1	50
15	P55	51	16	P54	52
17	P53	53	18	JA3-RDn	54
19	JA3-WRHn	55	20	P50	56
21	GROUND	-	22	P83	58
23	UC_VCC	-	24	UB	60
25	PC6	61	26	REMC-PMC0	62
27	PMOD2-IO4_INT1_WIFIWKUP	63	28	P81	64
29	P80	65	30	JA3-A20	66
31	JA3-A19	67	32	JA6-TXDc	68
33	JA6-RXDc	69	34	PC2	70
35	JA6-SCKc	71	36	JA6-CTS011	72

Table 7-8 below lists the connections of the microcontroller pin header, J3.

Table 7-8: Microcontroller Pin Header, J3

	Microcontroller Pin Header J3				
Pin	**Circuit Net Name**	**MCU Pin**	**Pin**	**Circuit Net Name**	**MCU Pin**
1	PC1	73	2	PL1	74
3	PC0	75	4	PMOD1-IO5_RESET1	76
5	JA3-CSc	77	6	PB7	78
7	PB6	79	8	PB5	80
9	PB4	81	10	PB3	82
11	JA3-A10	83	12	PB1	84
13	PMOD1-IO7_CS2	85	14	PMOD1-IO6_CS1	86
15	PB0	87	16	JA3-A7	88
17	PA6	89	18	JA3-A5	90
19	UC_VCC	-	20	PA4	92
21	GROUND	-	22	PA3	94
23	JA3-A2	95.	24	PA1	96
25	PA0	97	26	P67	98
27	P66	99	28	JA3-CKE	100
29	PE7	101	30	PE6	102
31	JA1-IO7	103	32	P70	104
33	JA1-IO6	105	34	JA3-D13	106
35	JA3-D12	107	36	JA3-D11	108

Table 7-9 below lists the connections of the microcontroller pin header, J4.

Table 7-9: Microcontroller Pin Header, J4

	Microcontroller Pin Header J4				
Pin	**Circuit Net Name**	**MCU Pin**	**Pin**	**Circuit Net Name**	**MCU Pin**
1	PE2	109	2	PE1	110
3	JA3-D8	111	4	JA3-WEn	112
5	JA3-CAS	113	6	JA3-RAS	114
7	JA3-CSb	115	8	JA1-IO5	116
9	P60	117	10	JA1-IO4	118
11	JA3-D7	119	12	JA3-D6	120
13	JA3-D5	121	14	JA3-D4	122
15	JA3-D3	123	16	JA3-D2	124
17	JA3-D1	125	18	JA3-D0	126
19	JA2-M1POE	127	20	SW2	128
21	SW1	129	22	LIN-NSLP	130
23	PMOD2-IO5_RESET1_WIFIMDRES	131	24	PF6	132
25	JA5-ADC7	133	26	JA5-ADC6	134
27	JA5-ADC5	135	28	JA5-ADC4	136
29	JA1-ADC3	137	30	JA1-ADC2	138
31	JA1-ADC1	139	32	VREFL0	140
33	P40	141	34	VREFH0	142
35	AVCC0	143	36	P07	144

8. Code Development

8.1   Overview

For all code debugging using Renesas software tools, the RSK board must be connected to a PC via an E2 Lite debugger. An E2 Lite debugger is supplied with this RSK product.

For further information regarding the debugging capabilities of the E2 Lite debuggers, refer to E2 emulator Lite User's Manual (R20UT3240EJ), E1/E20/E2 Emulator, E2 Emulator Lite Additional Document for User's Manual (R20UT0399EJ).

8.2   Compiler Restrictions

The compiler supplied with this RSK is fully functional for a period of 60 days from first use. After the first 60 days of use have expired, the compiler will default to a maximum of 128k code and data. To use the compiler with programs greater than this size you need to purchase the full tools from your distributor.

The protection software for the compiler will detect changes to the system clock. Changes to the system clock back in time may cause the trial period to expire prematurely.

8.3   Mode Support

The MCU supports Single Chip and Boot Modes (SCI, User and FINE), which are configured on the RSK board. Details of the modifications required can be found in section 6.2. All other MCU operating modes are configured within the MCU's registers, which are listed in the RX660 Group User's Manual: Hardware.

Only ever change the MCU operating mode whilst the RSK is in reset, or turned off; otherwise the MCU may become damaged as a result.

8.4   Debugging Support

The E2 Emulator Lite (as supplied with this RSK) supports break points, event points (including mid-execution insertion) and basic trace functionality. It is limited to a maximum of 8 on-chip event points, 256 software breaks and 256 branch/cycle trace. For further details, refer E2 Emulator Lite User's Manual (R20UT3240EJ).

8.5   Address Space

For the MCU address space details, refer to the 'Address Space' section of RX660 Group User's Manual: Hardware.

9. Additional Information

Technical Support

For information about the RX660 Group microcontrollers refer to the 'RX660 Group Manual: Hardware'.

For information about the RX assembly language, refer to the 'RX Family User's Manual: Software'.

Technical Contact Details

America: techsupport.america@renesas.com
Europe: https://www.renesas.com/eu/en/support/contact.html
Global & Japan: https://www.renesas.com/support/contact.html

General information on this product can be found on the Renesas website at:
https://www.renesas.com/rskrx660

General information on Renesas microcontrollers can be found on the Renesas website at:
https://www.renesas.com/

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REVISION HISTORY	RX660 Group Renesas Starter Kit for RX660 User's Manual

Rev.	Date	Description	
		Page	**Summary**
1.00	Jan 17, 2022	-	First Edition issued

RX660 Group