CPX3 PLC Module

Using the CPX3 PLC module

R01AN27EG0102
Rev.1.02
Oct 19, 2020

Introduction

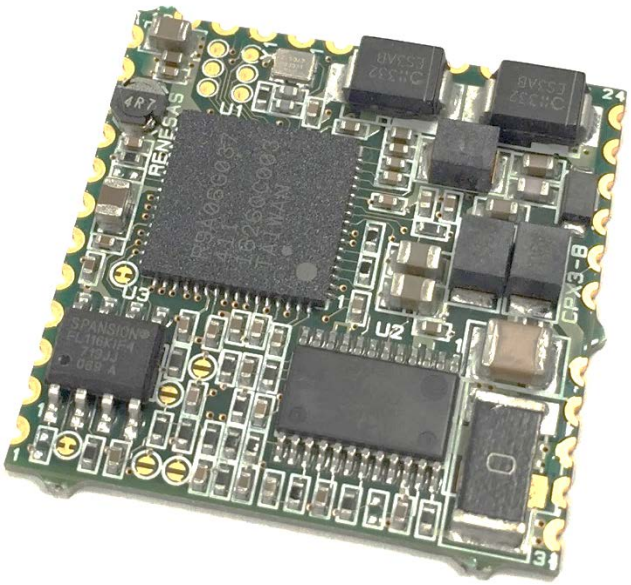
The CPX3 PLC modem module is a pre-assembled, small form-factor, narrow-band PLC modem based around the Renesas R9A06G037 LSI.

The module integrates the PLC processing MCU and DSP core, Renesas' R9A06G037 PLC device, with the line transceiver (power amplifier and line receiver), and all passive components required to complete the modem, with the exception of the high-voltage line coupler and zero-crossing detector isolator circuit.

The PLC modem is optimized for operation with a variety of PLC protocols such as G3-PLC (CENELEC A, CENELEC B, ARIB and FCC), PRIME (1.4 and 1.3.6) and Meters and More.

Target Device

CPX3 PLC modem module, integrating Renesas R9A06G037, and NJRC NJM45001



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1.1 Pin Functions

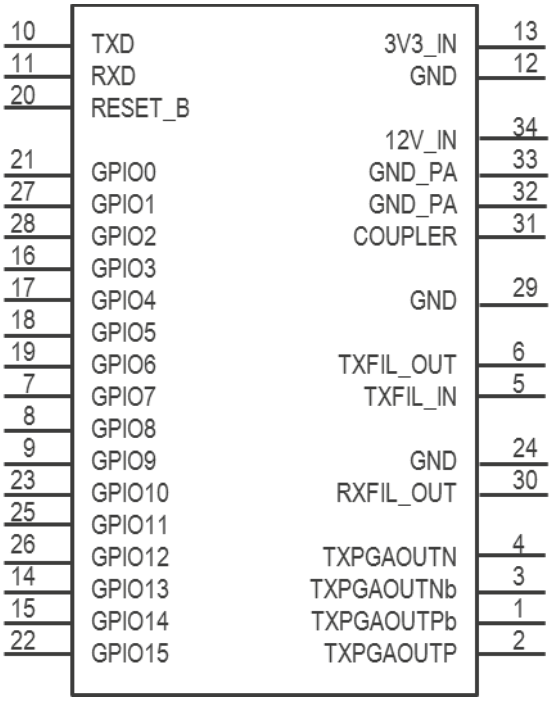


Table 1-1 CPX3 module pin functions

Module Pin Number	Module Pin Name	Type	Module Pin Function
12, 24, 29	GND	P	Power supply input 0V: Connect to common 0V
32, 33	GND_PA	P	Power supply input 0V: Connect to common 0V Note 1: *Power Amplifier electrical ground connections, ensure low impedance connection to ground plane for maximum signal integrity.* Note 2: *Power amplifier thermal heat-spreading connections, ensure low thermal resistivity to ground plane.*
13	3V3_IN	P	Power supply input, 3V3: Connect to regulated digital 3V3 power supply. Decouple to GND (pin 12) close to the module package.
34	12V_IN	P	Power supply input, 12V: Connect to regulated PA 12V to 15V power supply. Decouple to GND_PA close to the module package.
31	COUPLER	I/O	PLC signal input/output: Connect to the PLC line coupler circuit. See section 0 for application circuit.
11	RXD	In	UART receive input: Connect to host MCU
10	TXD	Out	UART transmit output: Connect to host MCU
20	RESET_B	In	CPX3 reset input: Connect to host MCU. Reset condition when set LOW. Pull-up resistor to 3V3_IN recommended.
21	GPIO0	-	Reserved, no electrical connection: No connection required
27	GPIO1	-	Reserved, no electrical connection: No connection required
28	GPIO2	-	Reserved function (CPX3 pin48): Do not connect
16	GPIO3	-	Reserved function (CPX3 pin45): Do not connect

Module Pin Number	Module Pin Name	Type	Module Pin Function
17	GPIO4	-	Reserved function (CPX3 pin46): Do not connect
18	GPIO5	-	Reserved function (CPX3 pin47): Do not connect
19	GPIO6	In	Zero crossing detector input (CPX3 pin43): Connect to opto-isolator for zero-crossing detection. See section 2.3 for application circuit.
7	GPIO7	In	TX_Break (CPX3 pin49): Transmission stop control input – transmission disabled when set LOW. Pull-up resistor to 3V3_IN recommended.
8	GPIO8	-	Undefined function (CPX3 pin50): No connection required
9	GPIO9	-	Undefined function (CPX3 pin51): No connection required
23	GPIO10	Out	PHY_RX flag (CPX3 pin52): PHY RX indication when set LOW.
25	GPIO11	Out	PHY_TX flag (CPX3 pin53): PHY TX indication when set LOW.
26	GPIO12	Out	TJALM1 (CPX Pin55): Limit of junction temperature alarm from PA, shutdown condition enabled when set LOW. No connection required
14	GPIO13	Out	TJALM2 (CPX Pin56): High junction temperature alarm from PA, request for lower duty cycle when set LOW. No connection required
15	GPIO14	Out	TXENB (CPX Pin57): PHY TX condition when set LOW. No connection required
22	GPIO15	Out	RXSATT (CPX Pin58): Step attenuator gain set to -18dB when set HIGH, 0dB when set LOW. No connection required
5	TXFIL_IN	-	Reserved, no electrical connection: No connection required
6	TXFIL_OUT	-	Reserved, no electrical connection: No connection required
30	RXFIL_OUT	I/O	Optional external RX filter connection: No connection required
4	TXPGAOUTN	Out	Optional external TX filter connection: No connection required
3	TXPGAOUTNb	In	Optional external TX filter connection: No connection required
2	TXPGAOUTP	Out	Optional external TX filter connection: No connection required
1	TXPGAOUTPb	In	Optional external TX filter connection: No connection required

1.2 Electrical Specifications

Table 1-2 Recommended Operating Conditions

Parameter	Symbol	Condition	Min	Typ	Max	Units
Supply voltage (3V3_IN)	V_{DD}		3.0	3.3	3.6	V
Supply voltage (12V_IN)	V_{DD12}		12	15	18	V
PA Thermal shutdown		GPIO12 (TJALM1) output set to LOW	-	160	-	ºC
PA Thermal shutdown recovery threshold		GPIO12 (TJALM1) output returned to HIGH	-	140	-	ºC
PA Thermal alarm		GPIO13 (TJALM2) output set to LOW	-	135	-	ºC
PA Thermal alarm recovery threshold		GPIO13 (TJALM2) output returned to HIGH	-	125	-	ºC
Operating ambient temperature	T_a		-40	-	+85	ºC

Table 1-3 DC Characteristics (VDD = 3.3V, Ta = -40 to 85ºC)

Parameter	Symbol	Condition	Min	Typ	Max	Units
Low level input voltage	V_{IL}	GPIO and UART pins (except GPIO13 and GPIO14) V_{DD} = 3.3V	-0.3	-	0.8	V
High level input voltage	V_{IH}	GPIO and UART pins (except GPIO13 and GPIO14) V_{DD} = 3.3V	2.0	-	VDD+0.3	V
Low level output voltage	V_{OL}	GPIO and UART pins (except GPIO13 and GPIO14) I_{OL} = 0mA	-	-	0.1	V
High level output voltage	V_{OH}	GPIO and UART pins (except GPIO13 and GPIO14) I_{OH} = 0mA	VDD-0.1	-	-	V
Low level output voltage	V_{OL}	GPIO13 and GPIO14 V_{DD} = 3.3V, load ≥ 10kΩ to V_{DD}	-	-	1	V
High level output voltage	V_{OH}	GPIO13 and GPIO14 V_{DD} = 3.3V, load ≥ 10kΩ to GND	2.3	-	-	V

Note: All figures quoted are for guidance only and are not guaranteed. Please refer to the Renesas R9A06G037 (CPX3) and NJRC NJM45001 device hardware user manuals for specific values.

Table 1-4 Power consumption (VDD = 3.3V, VDD12 = 15V, Ta = 25ºC)

Parameter	Symbol	Condition	Min	Typ	Max	Units
Power consumption (3V3_IN)	P_{3V3_IN}			155		mW
Power consumption (12_IN)	P_{12_IN}	Average power, transmit mode, during active transmission into; Line impedance = 50Ω LISN Line impedance = 2Ω LISN		 1.1 5.1		 W W

2. Application information

2.1 Module Connections

The electrical connections to the module are described in Table 1-1 above. Pins marked as ***Do not connect*** or ***No connection required*** should be left unconnected in the application circuit (pin floating).

All digital input/output pins have a 3.3V LVCMOS interface.

2.1.1 Power domain split

The module implements a single common ground plane shared between the 3.3V digital power domain (pins **3V3_IN, GND**) and the 12-15V power amplifier domain (**pins 12V_IN, GND_PA**). The application board should mirror the single common ground plane architecture, however care should be taken in the application board design to ensure that current flows within the two domains are routed so as to maintain good signal integrity.

The 3.3V and 12-15V power supplies ground references (**GND** and **GND_PA**) should be linked with a low impedance path outside of the module so as to prevent any ground currents flowing through the module, that may impact upon performance. The ground plane may be split to control current flows within the application board if necessary, but the **GND** to **GND_PA** link should be located under the module to form a star-point. If the ground plane is split, the star-point should not be located at the PSU or another point.

2.1.2 Decoupling

The 3.3V power supply should be decoupled with a 100nF ceramic capacitor between pins **3V3_IN** (pin 13) and **GND** (pin 12) as close to the module as possible.

The 12-15V power supply should be decoupled with a 100µF low ESR capacitor, such as ceramic or tantalum, between pins **12V_IN** (pin 34) and **GND_PA** (pins 32 and 33) as close to the module as possible.

The 12-15V power supply sources currents that can peak at 3A, so care should be taken to ensure very low impedance connections between the ground and power planes and the module pads. Double vias are recommended for all connections to the **12V_IN** and **GND_PA** pads and associated decoupling capacitors.

2.1.3 Thermal management

The power amplifier can dissipate considerable thermal energy during high duty-cycle transmission periods, especially with low line impedance conditions. The PA package is thermally bonded to the ground plane within the module, and the layout of the module is further enhanced to provide a direct thermal conduction path to the application board through the two **GND_PA** pins (pins 32 and 33).

To ensure optimal thermal performance, the **GND_PA** pins should be directly connected to a heat spreading layer within the application board.

2.1.4 PCB layout under the module

The module is fabricated on a four-layer FR4 substrate. The inner two layers form power and ground planes, and the outer layers are used for interconnection tracking.

The application board directly under the module should be designed with minimal tracking so as to prevent unwanted coupling between signals flowing within the module and those flowing on the application board. A plane area ***must not*** be placed on or close to the top surface of the application board directly below the module, otherwise parasitic currents will be induced into the plane area which will create unwanted current loops that may adversely impact on the sensitivity of the module.

2.1.5 Compliance and conformity

The CPX3 module is designed to communicate using the low-voltage electrical cables. There are many different worldwide standards and regulations for products such as CE, FCC and ARIB to ensure that products comply and conform to a region's safety, health, and environmental protection requirements. It is the user's responsibility to ensure that complete design incorporating the CPX3 module and its ancillary components meet these requirements.

One particular conformance test is the European standard EN50065, this standard applies to electrical equipment using signals in the frequency range 3 kHz to 148,5 kHz to transmit information on low voltage electrical systems, either on the public electricity distribution network or within installations in consumers' premises. Through its several parts, it specifies general requirements, frequency bands and electromagnetic disturbances, immunity requirements, low voltage decoupling filters and equipment impedance.

The CPX3 module has been designed such a way that all the regulations should be possible to achieve, in some cases with fine tuning software settings, for example conducted disturbances.

Subset EN50065-7 refers to equipment impedance and is one of the CE marking standards for Power Line Communication (PLC). In this case, Renesas recommends adding the following components and circuitry between the **COUPLER** (pin 31) and the **LINE COUPLER** [described in section 2.2] as indicated below. Please also refer to the Renesas application note "Circuit example of input impedance improvement" for further details. As every design is unique in behavior and characteristics, the application note and proposed circuitry below is intended as a guide only and provides information to support designers when designing equipment which requires conforming to EN50065-7.

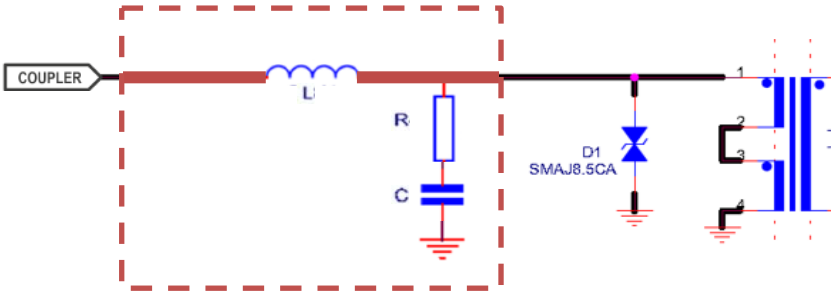


Figure 2-1 Circuit example of input impedance improvement

Table 2-1 Recommended component selections for Figure 2-1

Component	Value
R	120 Ohm
C	1uF
L	6.8 uH

Note the components above are matched with the C1 value of 1uF as used in the **LINE COUPLER** [described in section 2.2]

2.2 Line Coupler

The module does not contain the final stage of the line coupler circuit. This must be implemented on the application board. Figure 2-22 below shows an example single-phase line interface circuit (D1, T1, C1, R1). An example fused surge protection circuit (F1, VA1, F2, VA2) is also included, but is application specific.

The connections to the module are through pins **COUPLER** and **GND_PA**.

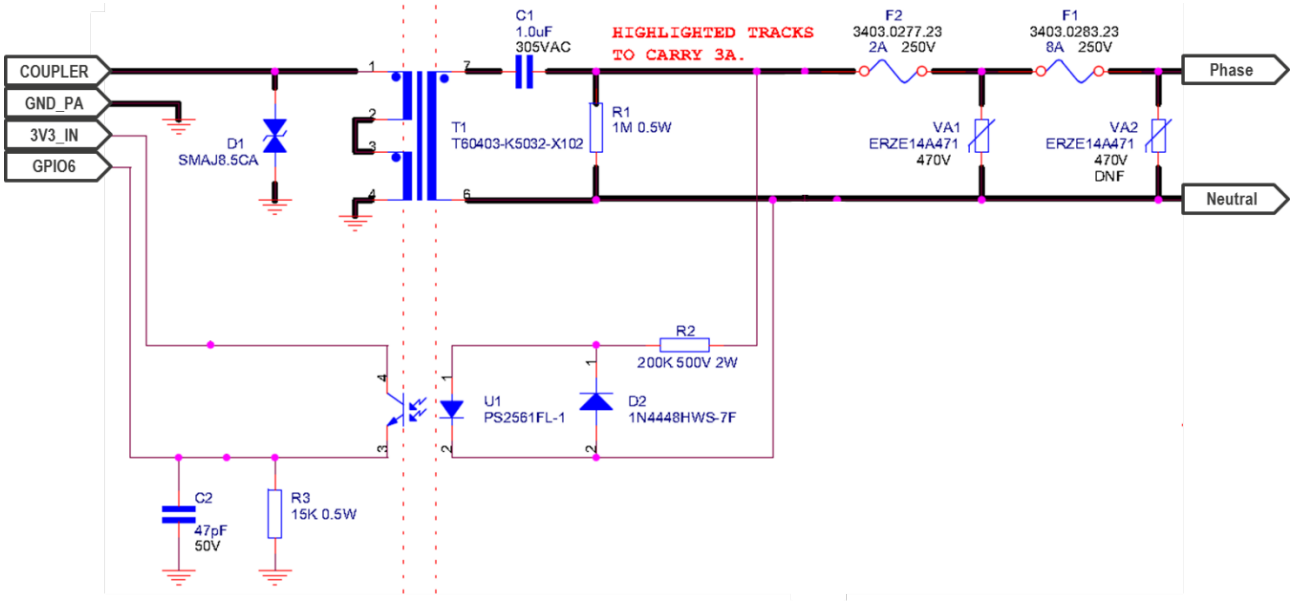


Figure 2-2 Line interface circuit and zero-crossing detector

2.3 Zero-crossing Detector

The module does not contain the zero-crossing detector circuit. This must be implemented on the application board. Figure 2-3 above shows an example single-phase opto-coupled ZCD circuit (C2, R3, U1, D2, R2).

The connections to the module are through pins **3V3_IN** and **GPIO6**.

2.4 Power Supply

Two power supply rails are required to operate the module, 3.3V for the digital and analogue signal chain, and 12V to 15V for the Power Amplifier.

2.4.1 3.3V supply rail

The 3.3V supply (**3V3_IN**) is split between the analogue function blocks in CPX3 and the PA, the digital IO in CPX3 and the PA, and is used to generate the 1.1V digital supply within CPX3 (an internal buck regulator within CPX3).

It is recommended to generate **3V3_IN** with a linear regulator for maximum performance. This supply may be derived from the 12-15V PA supply if necessary.

2.4.2 12V to 15V PA supply rail

The PA supply rail should be between 12V and 15V (15V recommended for low impedance lines). This regulator should be capable of providing peak currents of up to 1.5A for a typical application.

High value bulk decoupling capacitors with low-ESR should be included in the output stage of the regulator to enable the PA to source the required high currents demanded during the transmission peaks seen with the transitory nature of the PLC signal. Low-ESR tantalum capacitors are recommended here.

The bulk-decoupling capacitor value required should be carefully evaluated during prototyping to ensure that the **12V_IN** supply rail does not dip during peak signal transmission with the lowest line impedance supported, due to full depletion of the charge in the bulk-decoupling capacitors. Typical values required are >470µF.

Dips in the 12V_IN supply rail will result in clipping of the output signal, which will manifest itself as an increase in the noise floor of the output spectrum which may generate violations of the spectral emissions, as required for type approval by global standards bodies such as CENELEC, FCC etc.

Particular attention should be paid to noise filtering and line impedance stabilization at the input of the system power supply. Noise coupled into the AC line by the system PSU can degrade the sensitivity of the PLC modem dramatically. It is recommended to introduce a filter between the AC line connection point, where the PLC signal is coupled onto the line, and the input to the PSU subsystem. The specific characteristics of the PSU subsystem used in the application will determine the characteristic of the filter required.

2.5 Tx and Rx Filter

The module has an integrated Rx filter, configured for use with all global frequency bands, including CENELEC A, FCC and ARIB. The module also has an integrated Tx filter, again configured for use with all global frequency bands.

The *GLOBAL* filter configuration is show in the table in the module schematic, an extract of which is shown in Figure 2-33 below. The alternative CENELEC A and FCC/ARIB specific filter configurations are also shown, however these will require modifications to be made to the module configuration.

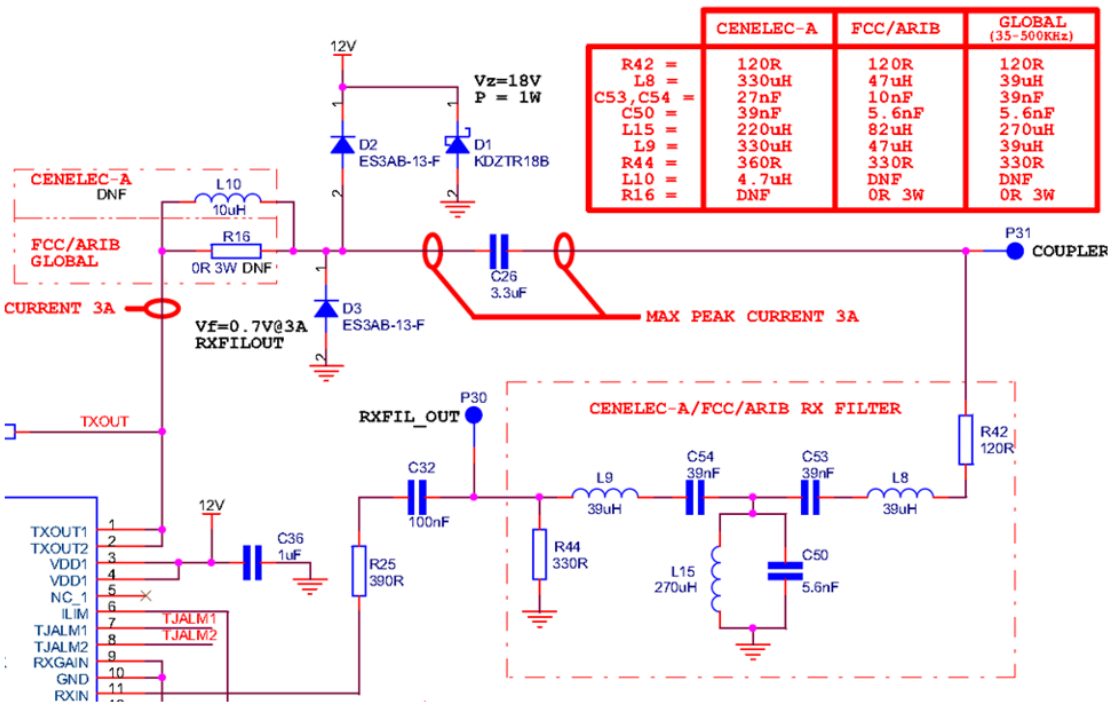


Figure 2-3 Default *GLOBAL* Tx and Rx Filter configuration

3. Mechanical

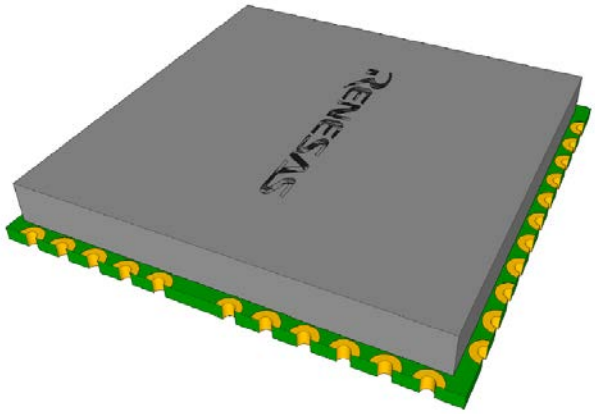
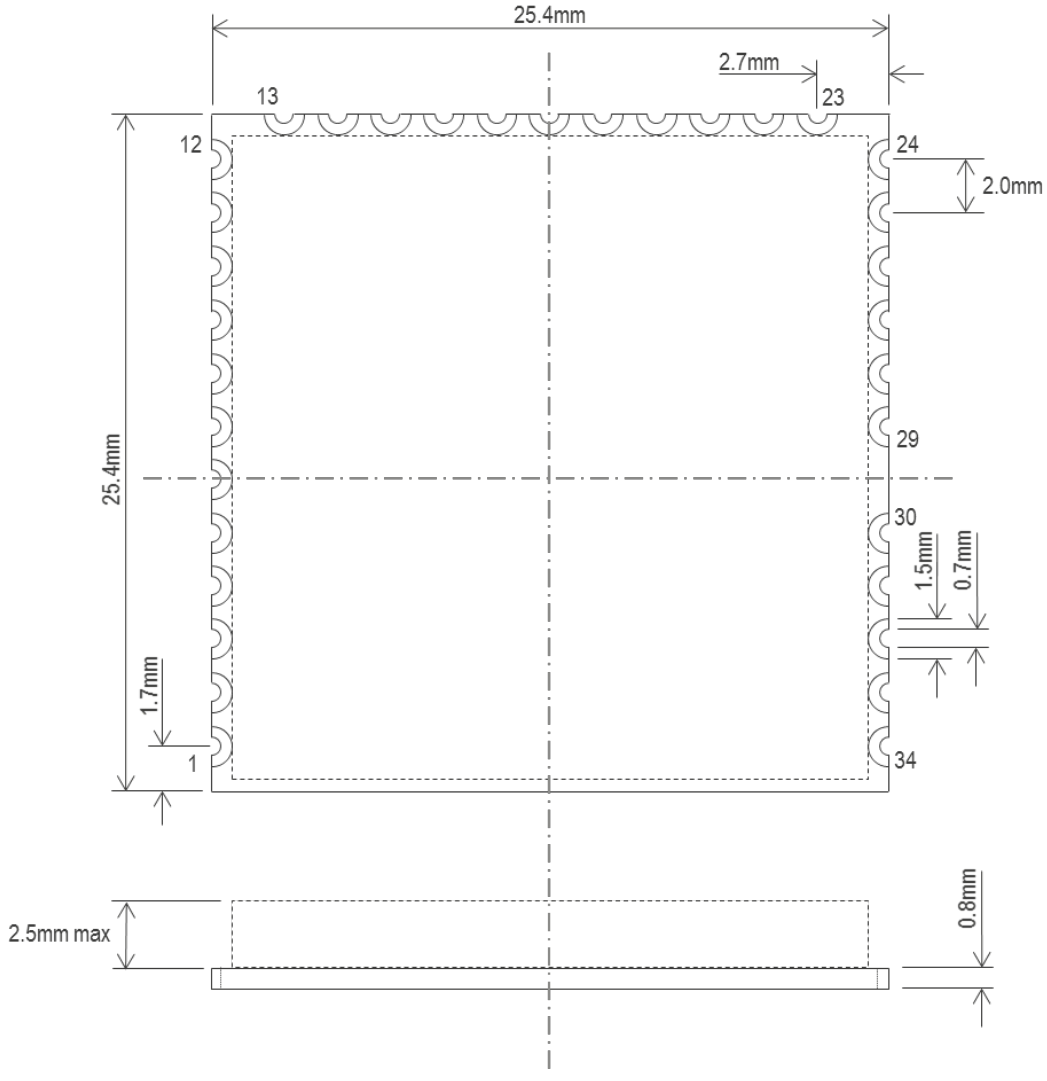
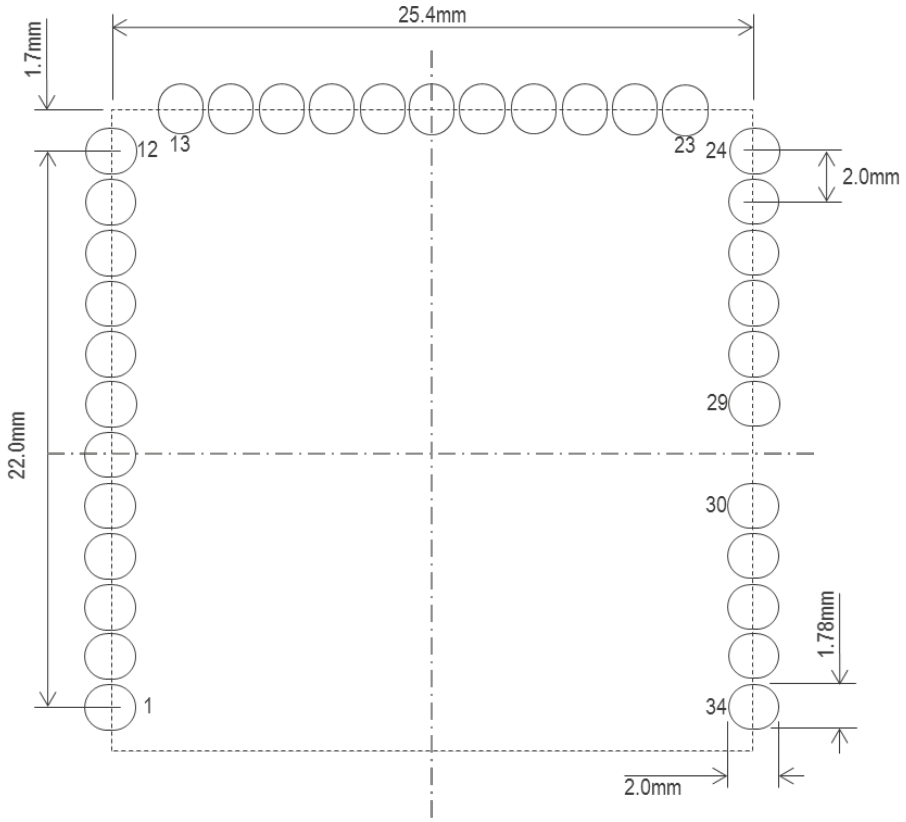


Figure 3-1 CPX3 PLC module

3.1 Package Outline

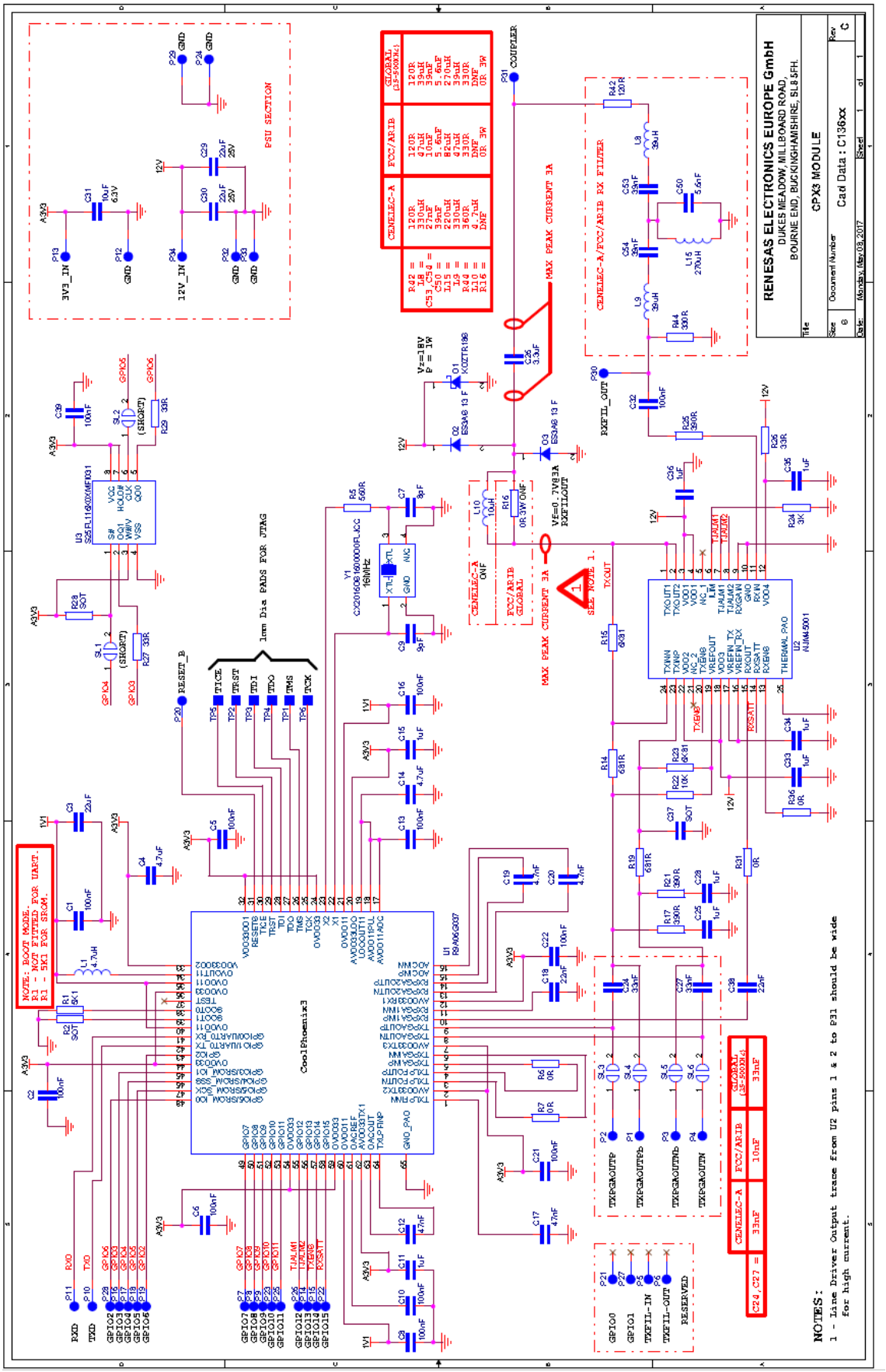


3.2 Recommended Footprint



4. Appendix

4.1 Module schematic



Website and Support

Renesas Electronics Website
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Revision History

		Description	
Rev.	**Date**	**Section**	**Summary**
1	Oct 11, 2018	All	First release
1.01	Sept 3, 2020	All	Internal review
1.02	Oct 19, 2020	All	Added section 2.1.5 Compliance and conformity

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins

   Handle unused pins in accordance with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.

   — The characteristics of Microprocessing unit or Microcontroller unit products in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.