ISL8024DEMO2Z
A Power Module for Xilinx RFSoC Applications
Demonstration Board

Industrial Analog and Power
1. Overview
The ISL8024DEMO2Z is a low-noise power module to power the high-speed data converters on Xilinx RFSoCs. It is used as a power module that plugs into an application board.

1.1 Key Features
• Three input voltage sources: 5.0V, 3.3V, and 1.8V
• Five output voltages: ADC_AVCC, ADC_AVCCAUX, DAC_AVCC, DAC_AVTT, and DAC_AVCCAUX
• PMBus interface that can digitally control the voltage set-point and margining of the DAC_AVTT rail
• All rails have differential point-of-load voltage sensing
• Additional low-pass filter to reduce output voltage ripple related to the switching regulator while maintaining high efficiency

1.2 Specifications

<table>
<thead>
<tr>
<th>Rail</th>
<th>Typical Voltage (V)</th>
<th>Voltage Set-Point Accuracy (%)</th>
<th>Adjustment Range (V)</th>
<th>Maximum Current (A)</th>
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<tr>
<td>ADC_AVCC</td>
<td>0.925</td>
<td>±1</td>
<td>0.70 to 1.16</td>
<td>2.0</td>
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<tr>
<td>ADC_AVCCAUX</td>
<td>1.8</td>
<td>±1</td>
<td>1.35 to 2.25</td>
<td>2.0</td>
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<tr>
<td>DAC_AVCC</td>
<td>0.925</td>
<td>±1</td>
<td>0.70 to 1.16</td>
<td>3.5</td>
</tr>
<tr>
<td>DAC_AVCCAUX</td>
<td>1.8</td>
<td>±1</td>
<td>1.35 to 2.25</td>
<td>2.0</td>
</tr>
<tr>
<td>DAC_AVTT</td>
<td>2.5 and 3.0</td>
<td>±1</td>
<td>1.88 to 3.75</td>
<td>2.0</td>
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1.3 Ordering Information

<table>
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<th>Part Number</th>
<th>Description</th>
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<tr>
<td>ISL8024DEMO2Z</td>
<td>ISL8024 demonstration board</td>
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</tbody>
</table>

1.4 Related Literature
For a full list of related documents, visit our website:
• [ISL8024](#), [ISL28191](#) device pages
2. Functional Description

Overall system power blocks are shown in Figure 1. The 1.8V and 2.5V output voltage is derived from 5V, and the 0.925V rails are derived from 3.3V. Each rail is followed by an additional LC filter to reduce output voltage ripple.

![Figure 1. Simplified Block Diagram of the ISL8024DEMO2Z Power Module Board](image)

Based on the specification, the ISL8024 is used as the DC/DC converter solution and as the main component. The ISL8024 has ±0.8% VFB tolerance across the temperature range of -40°C to +85°C. It has a programmable switching frequency up to 2MHz to reduce the size of the LC filters. To further reduce the output voltage ripple, a 2nd stage LC filter is used after the LC filter for the buck regulators. To reduce the conductor trace voltage drop related to the board connectors and to achieve the best load point voltage regulation, a remote sense scheme is used with the ISL28191 as a differential amplifier. Reduce the EMI to the upstream converters, a dedicated LC filter is also used as the input filter for each rail. An example power block and its related schematics is shown in Figure 2, demonstrating the device components.

![Figure 2. Single Rail Power Block](image)
Low-pass filter design requires a balance between phase loss and $V_{OUT}$ ripple attenuation. The LC filter used in Figure 2 has about 40dB noise attenuation at 2MHz and a phase drop of 20° at 100kHz as shown in Figure 3. The compensation design of the ISL8024 regulator has been tuned to accommodate this phase loss.

2. Functional Description

![Figure 3. 2nd Stage LC Filter Characteristics](image)

2.1 Quick Start Guide

The ISL8024DEMO2Z board can be powered on or off with external connectors, or plugged into Xilinx application boards.
3. PCB Layout Guidelines

3.1 ISL8024DEMO2Z Demonstration Board

Figure 4. ISL8024DEMO2Z Demonstration Board (Bottom)

Figure 5. ISL8024DEMO2Z Demonstration Board (Top)
3.2 ISL8024DEMO2Z Circuit Schematic

Figure 6. ISL8024DEMO2Z Schematics, Page 1
Figure 7. ISL8024DEMO2Z Schematics, Page 2
Figure 8. ISL8024DEMO2Z Schematics, Page 3
Figure 9. ISL8024DEMO2Z Schematics, Page 4
### 3.3 Bill of Materials

<table>
<thead>
<tr>
<th>Qty</th>
<th>Reference Designator</th>
<th>Description</th>
<th>PCB Footprint</th>
<th>Part Number</th>
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<td>SMC0805, X5R, 10V</td>
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### 3.4 Board Layout

![Figure 10. Top Layer](image.png)

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<td>R22, R117</td>
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<td>110k</td>
<td>SMR0402, 1%</td>
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<tr>
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<td>R113</td>
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Figure 11. Bottom Layer
4. Typical Performance Curves

Efficiency was tested on these boards.

Figure 12. ADC_AVCC Rail, Peak Efficiency = 84%

Figure 13. DAC_AVCC Rail, Peak Efficiency = 85%

Figure 14. ADC_ACCAUX Rail, Peak Efficiency = 90%

Figure 15. DAC_AVCCAUX Rail, Peak Efficiency = 90%

Figure 16. DAC_AVTT Rail, Peak Efficiency = 92%
5. Summary

The ISL8024DEMO2Z demonstration board integrates five output voltage rails into a high-density plug-in power module. It offers a very low output voltage ripple with dual LC filters. It has very tight load-point voltage regulation with remote voltage sense to compensate for board copper loss and interconnection voltage drop. Digital programmability is also available as an option. LC filters at each input rail alleviate the EMI interactions between different rails.
### 6. Revision History

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<td>The Typical Performance Curves heading was modified: “output voltage ripple” was deleted. Typical Performance Curves 13, 15, 17, 19, and 21 were deleted, and the remaining figures were renumbered.</td>
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<td>Initial release</td>
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