

# Renesas Flexible Software Package (FSP) v2.0.0

User's Manual

RA Family

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# Chapter 1 Introduction

## 1.1 Overview

This manual describes how to use the Renesas Flexible Software Package (FSP) for writing applications for the RA microcontroller series.

## 1.2 Using this Manual

This manual provides a wide variety of information, so it can be helpful to know where to start. Here is a short description of each main section and how they can be used.

[Starting Development](#) - Provides a step by step guide on how to use e2 studio and FSP to develop a project for RA MCUs. This is a good place to start to get up to speed quickly and efficiently.

[FSP Architecture](#) - Provides useful background material on key FSP concepts such as Modules, Stacks, and API standards. Reference this section to extend or refresh your knowledge of FSP concepts.

### API Reference

- Provides detailed information on each module and interface including features, API functions, configuration settings, usage notes, function prototypes and code examples. Board Support Package (BSP) related API functions are also included.

#### Note

*Much of the information in the API Reference section is available from within the e2 studio tool via the [Developer Assistance](#) feature. The information here can be referenced for additional details on API features.*

## 1.3 Documentation Standard

Each module user guide outlines the following:

- Features: A bullet list of high level features provided by the module.
- Configuration: A description of module specific configurations available in the RA Configuration editor.
- Usage Notes: Module specific documentation and limitations.
- Examples: Example code provided to help the user get started.
- API Reference: Usage notes for each API in the module, including the function prototype and hyperlinks to the interface documentation for parameter definitions.

Interface documentation includes typed enumerations and structures—including a structure of function pointers that defines the API—that are shared by all modules that implement the interface.

## 1.4 Introduction to FSP

### 1.4.1 Purpose

The Renesas Flexible Software Package (FSP) is an optimized software package designed to provide easy to use, scalable, high quality software for embedded system design. The primary goal is to provide lightweight, efficient drivers that meet common use cases in embedded systems.

### **1.4.2 Quality**

FSP code quality is enforced by peer reviews, automated requirements-based testing, and automated static analysis.

### **1.4.3 Ease of Use**

FSP provides uniform and intuitive APIs that are well documented. Each module is supported with detailed user documentation including example code.

### **1.4.4 Scalability**

FSP modules can be used on any MCU in the RA family, provided the MCU has any peripherals required by the module.

### **1.4.5 Build Time Configurations**

FSP modules also have build time configurations that can be used to optimize the size of the module for the feature set required by the application.

### **1.4.6 e2 studio IDE**

FSP provides a host of efficiency enhancing tools for developing projects targeting the Renesas RA series of MCU devices. The e2 studio IDE provides a familiar development cockpit from which the key steps of project creation, module selection and configuration, code development, code generation, and debugging are all managed.

# Chapter 2 Starting Development

## 2.1 Starting Development Introduction

The wealth of resources available to learn about and use e2 studio and FSP can be overwhelming on first inspection, so this section provides a Starting Development Guide with a list of the most important initial steps. Following these highly recommended first 11 steps will bring you up to speed on the development environment in record time. Even experienced developers can benefit from the use of this guide, to learn the terminology that might be unfamiliar or different from previous environments.

1. Read the section [What is e2 studio?](#), up to but not including [e2 studio Prerequisites](#). This will provide a description of the various windows and views to use e2 studio to create a project, add modules and threads, configure module properties, add code, and debug a project. It also describes how to use key coding 'accelerators' like Developer Assist (to drag and drop parameter populated API function calls right into your code), a context aware Autocomplete (to easily find and select from suggested enumerations, functions, types, and many other coding elements), and many other similar productivity enhancers.
2. Read the [FSP Architecture](#), [FSP Modules](#) and [FSP Stacks](#) sections. These provide the basic background on how FSP modules and stacks are used to construct your application. Understanding their definitions and the theory behind how they combine will make it easier to develop with FSP.
3. Read a few [Modules](#) sections to see how to use API function calls, structures, enumerations, types and callbacks. These module guides provide the information you will use to implement your project code.
4. After you have a Kit and you have downloaded and installed e2 studio and FSP, you can build and debug a simple project to test your installation, tool flow, and the kit. (If you do not have a Kit or have not yet installed the development software, use the links included in the [e2 studio Prerequisites](#) for more information.) The simple [Tutorial: Your First RA MCU Project - Blinky](#) will Blink an LED on and off. Follow the instructions for importing and running this project in section [Create a New Project for Blinky](#). It will use some of the key steps for managing projects within e2 studio and is a good way to learn the basics.
5. Once you have successfully run Blinky you have a good starting point for using FSP for more complex projects. The Using HAL Drivers Tutorial, available at [Tutorial: Using HAL Drivers - Programming the WDT](#), shows how to create a project from scratch, using FSP API functions. Do this next.
6. Several Hands-on Quick FSP Labs are available that cover key development topics with short 15-minute Do it Yourself (DIY) activities targeting the EK-RA6M3. Topics covered include code development accelerators like Developer Assistance, Autocomplete, Edit Hover, Help, Visual Expressions and using Example Projects. The complete list of available Quick FSP Labs can be found here: <https://en-support.renesas.com/knowledgeBase/19308277>. Doing a couple of these labs provides further details on using FSP, and is also good practice. Running these labs is highly recommended.
7. The balance of the [FSP Architecture](#) sections (that is, those not called out in step 2 above) contain additional reference material that may be helpful in the future. Scan them so you know what they contain, in case you need them.
8. The balance of the e2 studio User Guide, starting with the [What is a Project?](#) section up to, but not including, [Writing the Application](#) section, provides a detailed description of each of

the key steps, windows, and entries used to create, manage, configure, build and debug a project. Much of this may be familiar after running through the tutorials and Quick Labs. However, it is important to have a good grasp of what each of the configuration tabs are used for as that is where the bulk of the project preparation work takes place prior to writing code. Skim over this section as it may help with any questions in the future.

9. Read the [Writing the Application](#) section to get a short introduction to the steps used when creating application code with FSP. It covers both RTOS-independent and RTOS-dependent applications. It also includes a short description for several of the code accelerators you should be familiar with by now. Using additional Quick FSP Labs is a good way to become familiar with the application development process and links to them are included in the appropriate places in this section. You can find the complete list of available Quick FSP Labs here: <https://en-support.renesas.com/knowledgeBase/19308277>.
10. Scan the [Debugging the Project](#) section to see the steps required to download and start a debug session.
11. Explore the additional material available on the following web pages and bookmark the resources that look most valuable to you:
  - a. RA Landing Page: <https://www.renesas.com/ra>
  - b. FSP Landing Page: <https://www.renesas.com/fsp>
  - c. Example Projects on GitHub: <https://github.com/renesas/ra-fsp-examples>
  - d. Quick FSP Labs Listing: <https://en-support.renesas.com/knowledgeBase/19308277>
  - e. RA and FSP Knowledge Base (with articles of interest on RA and FSP): <https://en-support.renesas.com/knowledgeBase/category/31087>
  - f. RA and FSP Renesas Rulz site (Community posted and answered questions): <https://renesasrulz.com/ra/>
  - g. FSP Releases: <https://github.com/renesas/fsp/releases>
  - h. FSP Documentation: <https://renesas.github.io/fsp>
  - i. Online Technical Support: <https://www.renesas.com/us/en/support/contact.html>

## 2.2 e2 studio User Guide

### 2.2.1 What is e2 studio?

Renesas e2 studio is a development tool encompassing code development, build, and debug. e2 studio is based on the open-source Eclipse IDE and the associated C/C++ Development Tooling (CDT).

When developing for RA MCUs, e2 studio hosts the Renesas Flexible Software Package (FSP). FSP provides a wide range of time saving tools to simplify the selection, configuration, and management of modules and threads, to easily implement complex applications. The time saving tools available in e2 studio and FSP include the following:

- A Graphical User Interface (GUI) (see [Adding Threads and Drivers](#)) with numerous wizards for configuring and auto-generating code
- A context sensitive Autocomplete (see [Tutorial: Using HAL Drivers - Programming the WDT](#)) feature that provides intelligent options for completing a programming element
- A [Developer Assistance](#) tool for selection of and drag and drop placement of API functions directly in application code
- An [Edit Hover](#) feature to show detailed descriptions of code elements while editing
- A [Welcome Window](#) with links to example projects, application notes and a variety of other self-help support resources
- An [Information Icon](#) from each module is provided in the graphic configuration viewer that links to specific design resources, including code 'cheat sheets' that provide useful starting points for common application implementations.



Figure 1: e2 studio Splash Screen

e2 studio organizes project work based on Perspectives, Views, Windows, Panes, and Pages (sometimes called Tabs). A window is a section of the e2 studio GUI that presents information on a key topic. Windows often use tabs to select sub-topics. For example, an editor window might have a tab available for each open file, so it is easy to switch back and forth between them. A window Pane is a section of a window. Within a window, multiple Panes can be opened and viewed simultaneously, as opposed to a tabbed window, where only individual content is displayed. A memory-display Window, for example, might have multiple Panes that allow the data to be displayed in different formats, simultaneously. A Perspective is a collection of Views and Windows typical for a specific stage of development. The default perspectives are a C/C++ Perspective, an FSP Configuration Perspective and a Debug Perspective. These provide specific Views, Windows, Tabs, and Panes tailored for the common tasks needed during the specific development stage.

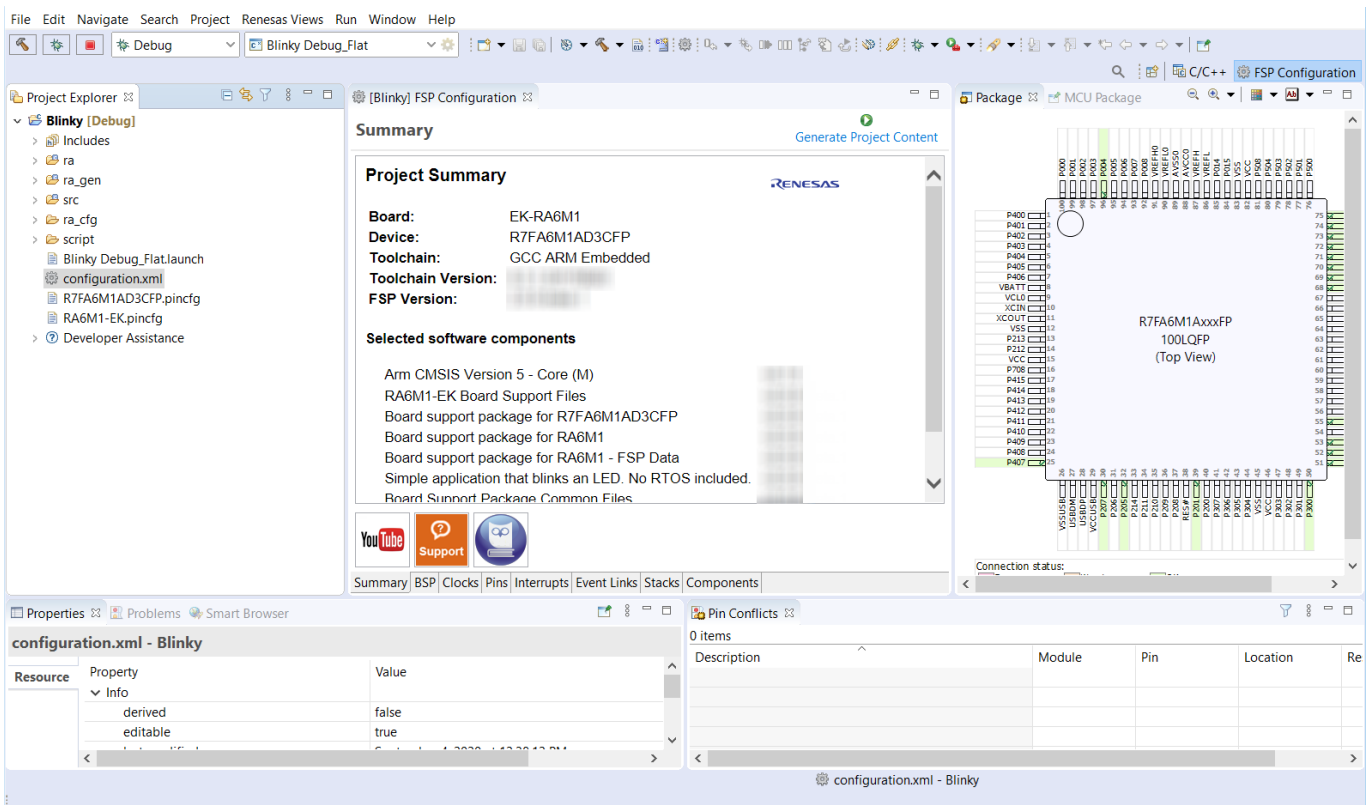


Figure 2: Default Perspective



In addition to managing project development, selecting modules, configuring them and simplifying code development, e2 studio also hosts the engine for automatically generating code based on module selections and configurations. The engine continually checks for dependencies and automatically adds any needed lower level modules to the module stack. It also identifies any lower level modules that require configuration (for example, an interrupt that needs to have a priority assigned). It also provides a guide for selecting between multiple choices or options to make it easy to complete a fully functional module stack.

The Generate Project Content function takes the selected and configured modules and automatically generates the complete and correct configuration code. The code is added to the folders visible in the **Project Explorer** window in e2 studio. The configuration.xml file in the project folder holds all the generated configuration settings. This file can be opened in the GUI-based RA Configuration editor to make further edits and changes. Once a project has been generated, you can go back and reconfigure any of the modules and settings if required using this editor.

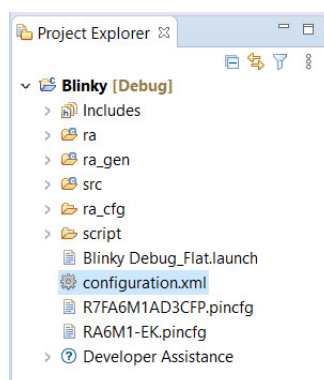


Figure 3: Project Explorer Window showing generated folders and configuration.xml file

## 2.2.2 e2 studio Prerequisites

### 2.2.2.1 Obtaining an RA MCU Kit

To develop applications with FSP, start with one of the Renesas RA MCU Evaluation Kits. The Renesas RA MCU Evaluation Kits are designed to seamlessly integrate with the e2 studio.

Ordering information, Quick Start Guides, User Manuals, and other related documents for all RA MCU Evaluation Kits are available at <https://www.renesas.com/ra>.

### 2.2.2.2 PC Requirements

The following are the minimum PC requirements to use e2 studio:

- Windows 10 with Intel i5 or i7, or AMD A10-7850K or FX
- Memory: 8-GB DDR3 or DDR4 DRAM (16-GB DDR4/2400-MHz RAM is preferred)
- Minimum 250-GB hard disk

### 2.2.2.3 Installing e2 studio, platform installer and the FSP package

Detailed installation instructions for the e2 studio and the FSP are available on the Renesas website <https://www.renesas.com/fsp>. Review the release notes for e2 studio to ensure that the e2 studio version supports the selected FSP version. The starting version of the installer includes all features of the RA MCUs.

### 2.2.2.4 Choosing a Toolchain

e2 studio can work with several toolchains and toolchain versions such as the GNU Arm compiler and Arm AC6. A version of the GNU Arm compiler is included in the e2 studio installer and has been verified to run with the FSP version.

### 2.2.2.5 Licensing

FSP licensing includes full source code, limited to Renesas hardware only.

## 2.2.3 What is a Project?

In e2 studio, all FSP applications are organized in RA MCU projects. Setting up an RA MCU project involves:

1. Creating a Project
2. Configuring a Project

These steps are described in detail in the next two sections. When you have existing projects already, after you launch e2 studio and select a workspace, all projects previously saved in the selected workspace are loaded and displayed in the **Project Explorer** window. Each project has an associated configuration file named `configuration.xml`, which is located in the project's root directory.

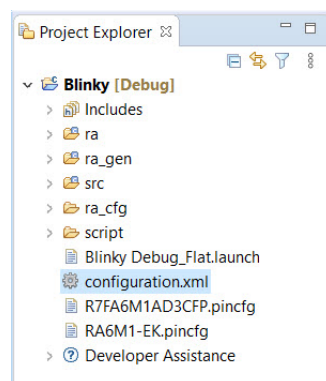


Figure 4: e2 studio Project Configuration file

Double-click on the `configuration.xml` file to open the RA MCU Project Editor. To edit the project configuration, make sure that the **FSP Configuration** perspective is selected in the upper right hand corner of the e2 studio window. Once selected, you can use the editor to view or modify the configuration settings associated with this project.

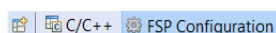


Figure 5: e2 studio FSP Configuration Perspective

#### Note

*Whenever the RA project configuration (that is, the `configuration.xml` file) is saved, a verbose RA Project Report file (`ra_cfg.txt`) with all the project settings is generated. The format allows differences to be easily viewed using a text comparison tool. The generated file is located in the project root directory.*

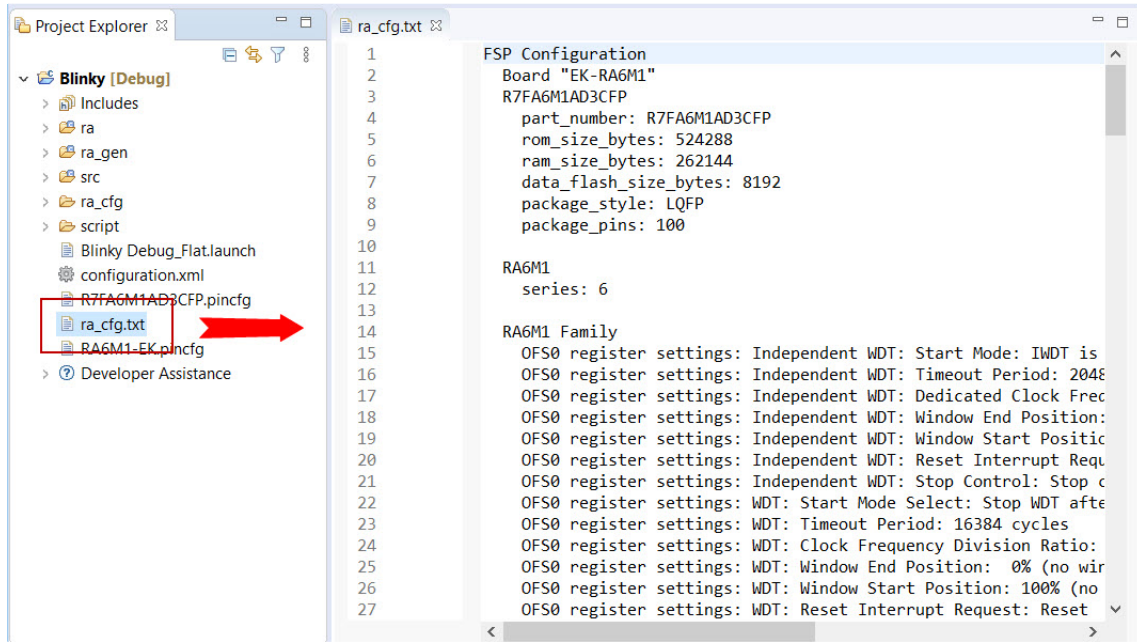


Figure 6: RA Project Report

The RA Project Editor has a number of tabs. The configuration steps and options for individual tabs are discussed in the following sections.

*Note*

*The tabs available in the RA Project Editor depend on the e2 studio version and the layout may vary slightly, however the functionality should be easy to follow..*

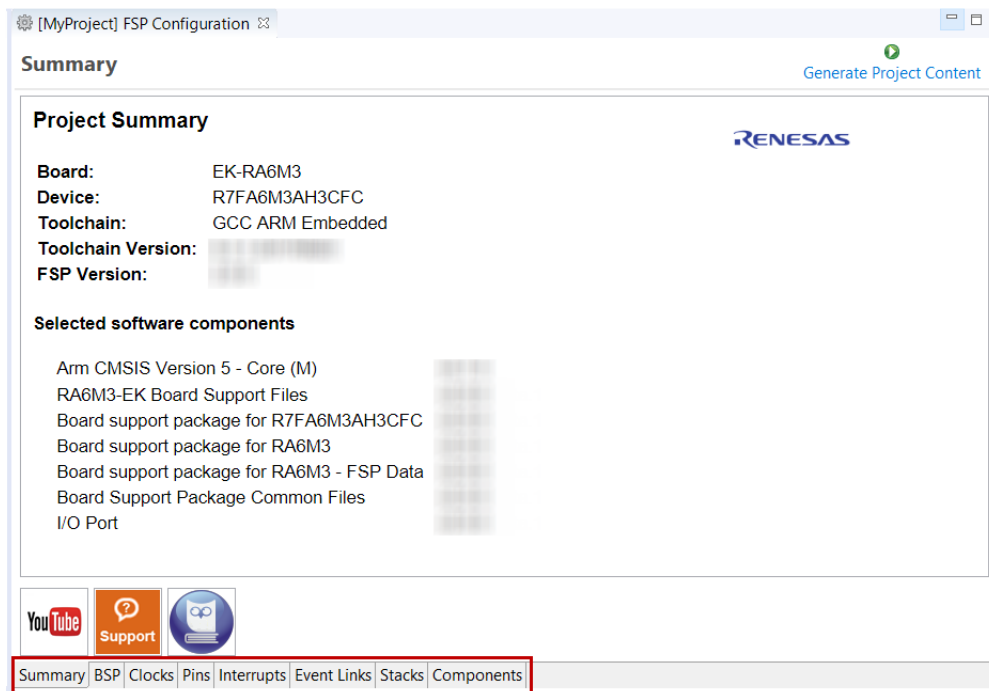


Figure 7: RA Project Editor tabs

- Click on the YouTube icon to visit the Renesas FSP playlist on YouTube
- Click on the Support icon to visit RA support pages at Renesas.com
- Click on the user manual (owl) icon to open the RA software package User's Manual

## 2.2.4 Creating a Project

During project creation, you specify the type of project, give it a project name and location, and configure the project settings for version, target board, whether an RTOS is included, the toolchain version, and the beginning template. This section includes easy-to-follow step-by-step instructions for all of the project creation tasks. Once you have created the project, you can move to configuring the project hardware (clocks, pins, interrupts) and the parameters of all the modules that are part of your application.

### 2.2.4.1 Creating a New Project

For RA MCU applications, generate a new project using the following steps:

1. Click on **File > New > RA C/C++ Project**.

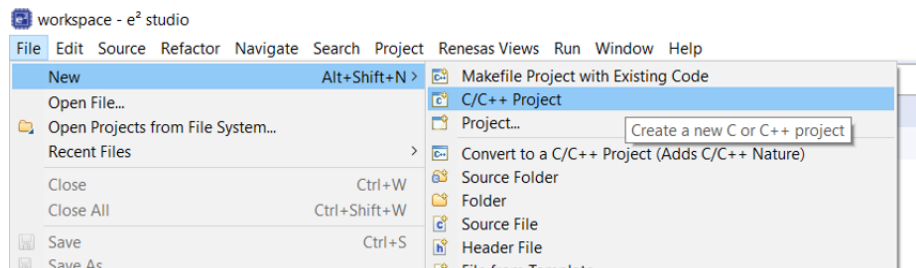


Figure 8: New RA MCU Project

Then click on the type of template for the type of project you are creating.

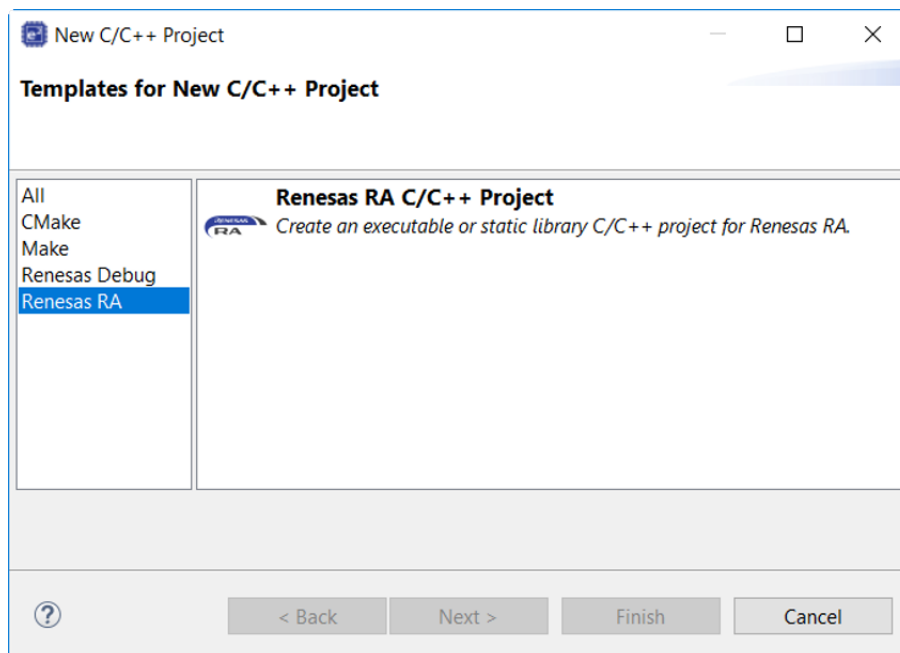


Figure 9: New Project Templates

## 2. Select a project name and location.

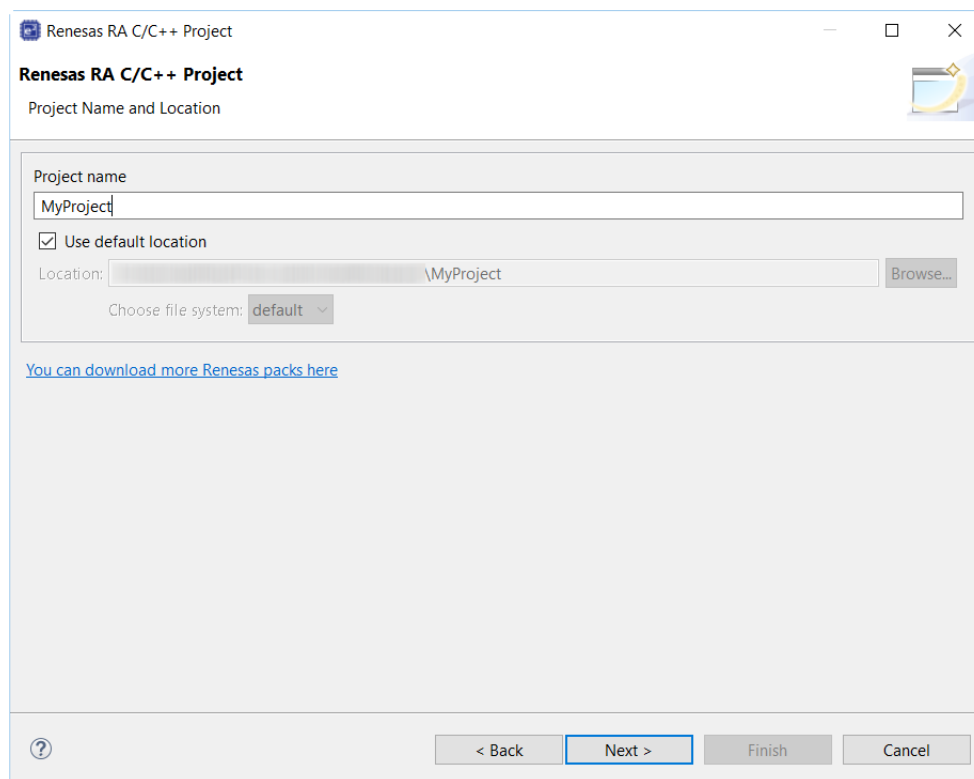


Figure 10: RA MCU Project Generator (Screen 1)

## 3. Click **Next**.

### 2.2.4.2 Selecting a Board and Toolchain

In the **Project Configuration** window select the hardware and software environment:

1. Select the **FSP version**.
2. Select the **Board** for your application. You can select an existing RA MCU Evaluation Kit or select **Custom User Board** for any of the RA MCU devices with your own BSP definition.
3. Select the **Device**. The **Device** is automatically populated based on the **Board** selection. Only change the **Device** when using the **Custom User Board (Any Device)** board selection.
4. To add threads, select **RTOS**, or **No RTOS** if an RTOS is not being used.
5. The **Toolchain** selection defaults to **GCC Arm Embedded**.
6. Select the **Toolchain version**. This should default to the installed toolchain version.
7. Select the **Debugger**. The J-Link Arm Debugger is preselected.

## 8. Click **Next**.

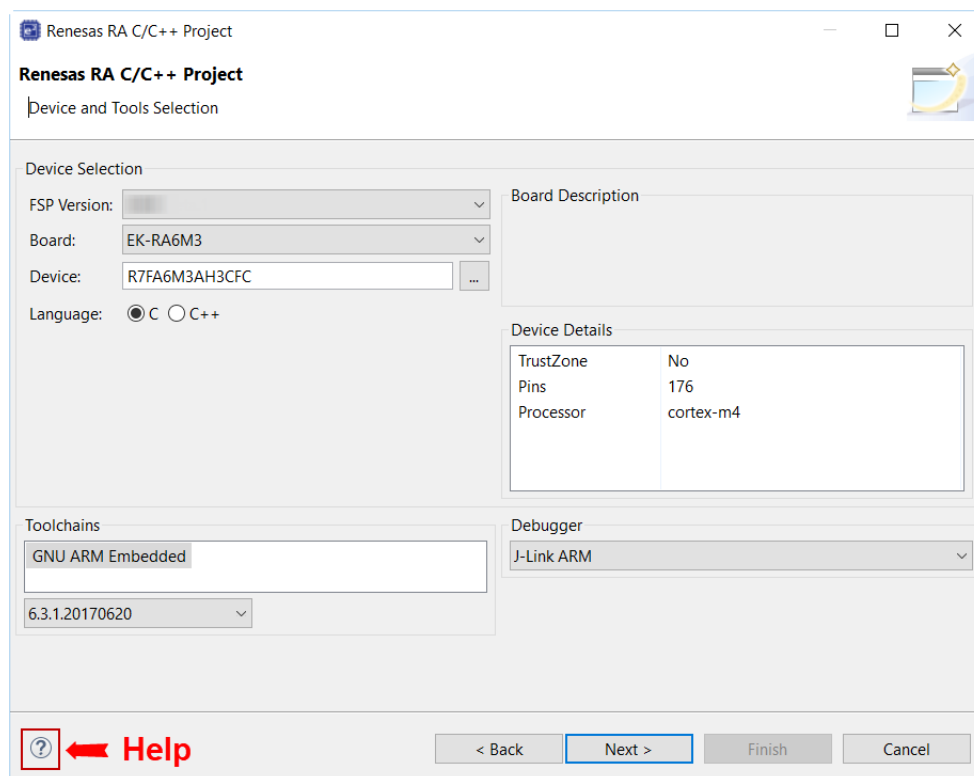


Figure 11: RA MCU Project Generator (Screen 2)

*Note*

*Click on the **Help** icon (?) for user guides, RA contents, and other documents.*

### 2.2.4.3 Selecting a Project Template

In the next window, select the build artifact and RTOS.

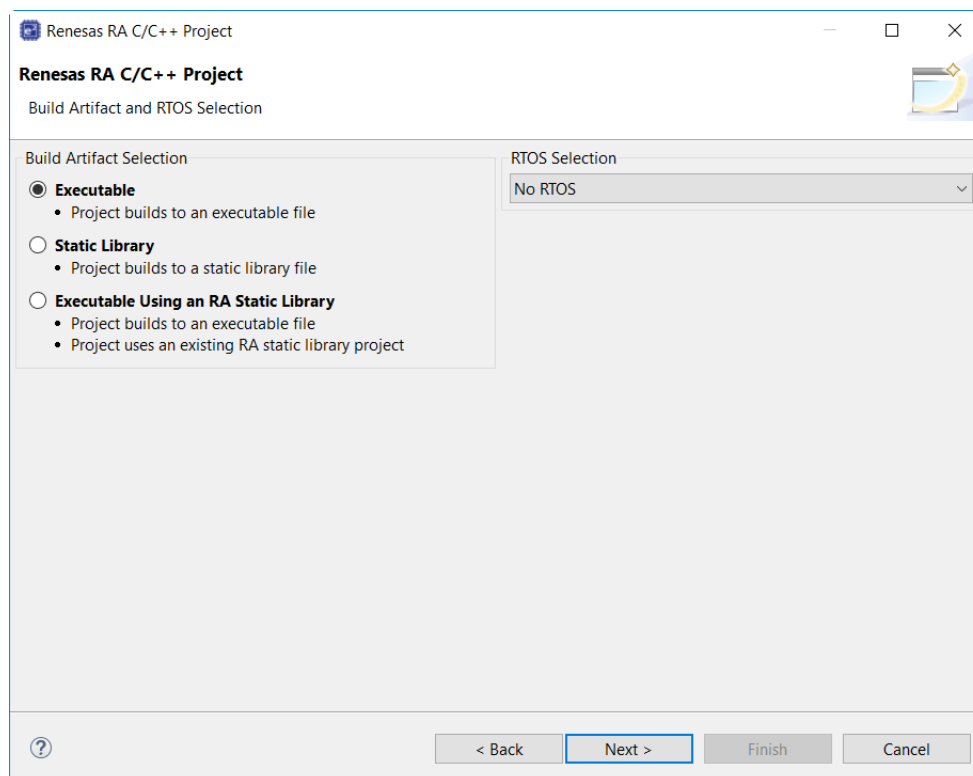


Figure 12: RA MCU Project Generator (Screen 3)

In the next window, select a project template from the list of available templates. By default, this screen shows the templates that are included in your current RA MCU pack. Once you have selected the appropriate template, click **Finish**.

*Note*

*If you want to develop your own application, select the basic template for your board, **Bare Metal - Minimal**.*

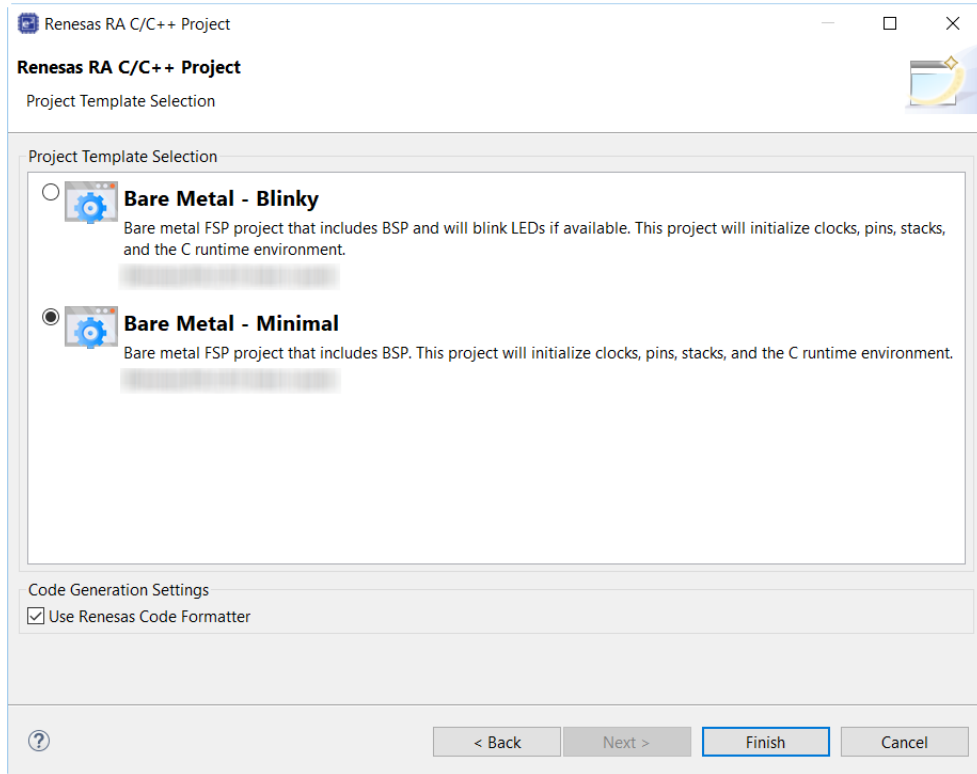


Figure 13: RA MCU Project Generator (Screen 4)

When the project is created, e2 studio displays a summary of the current project configuration in the RA MCU Project Editor.

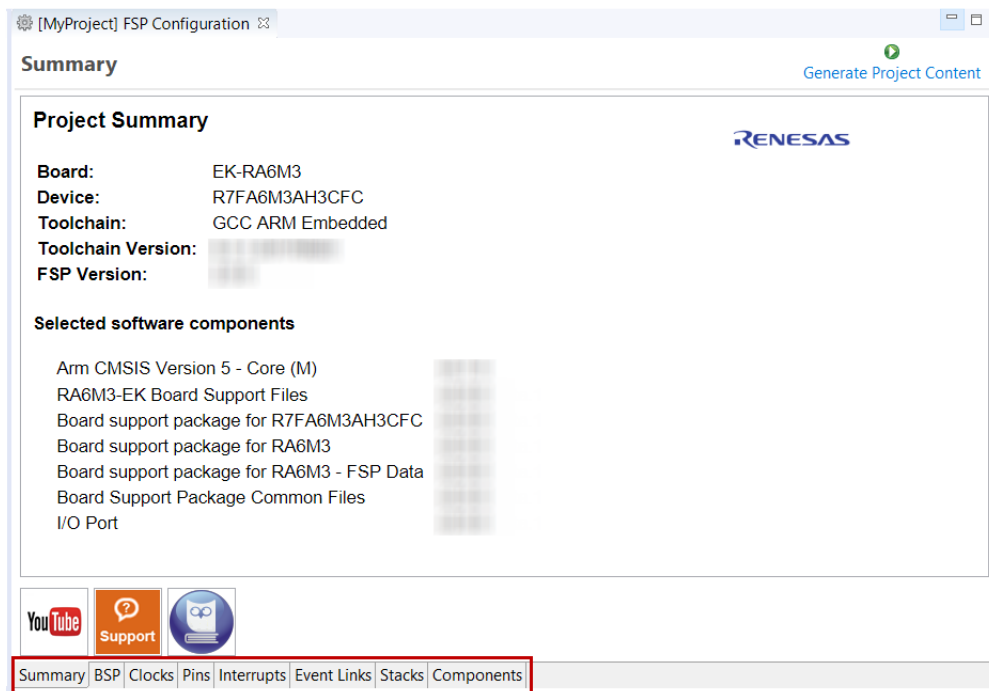


Figure 14: RA MCU Project Editor and available editor tabs



On the bottom of the RA MCU Project Editor view, you can find the tabs for configuring multiple aspects of your project:

- With the **Summary** tab, you can see all the key characteristics of the project: board, device, toolchain, and more.
- With the **BSP** tab, you can change board specific parameters from the initial project selection.
- With the **Clocks** tab, you can configure the MCU clock settings for your project.
- With the **Pins** tab, you can configure the electrical characteristics and functions of each port pin.
- With the **Interrupts** tab, you can add new user events/interrupts.
- With the **Event Links** tab, you can configure events used by the Event Link Controller.
- With the **Stacks** tab, you can add and configure FSP modules. For each module selected in this tab, the **Properties** window provides access to the configuration parameters, interrupt priorities, and pin selections.
- The **Components** tab provides an overview of the selected modules. Although you can also add drivers for specific FSP releases and application sample code here, this tab is normally only used for reference.

The functions and use of each of these tabs is explained in detail in the next section.

## 2.2.5 Configuring a Project

Each of the configurable elements in an FSP project can be edited using the appropriate tab in the RA Configuration editor window. Importantly, the initial configuration of the MCU after reset and before any user code is executed is set by the configuration settings in the **BSP**, **Clocks** and **Pins** tabs. When you select a project template during project creation, e2 studio configures default values that are appropriate for the associated board. You can change those default values as needed. The following sections detail the process of configuring each of the project elements for each of the associated tabs.

### 2.2.5.1 Summary Tab

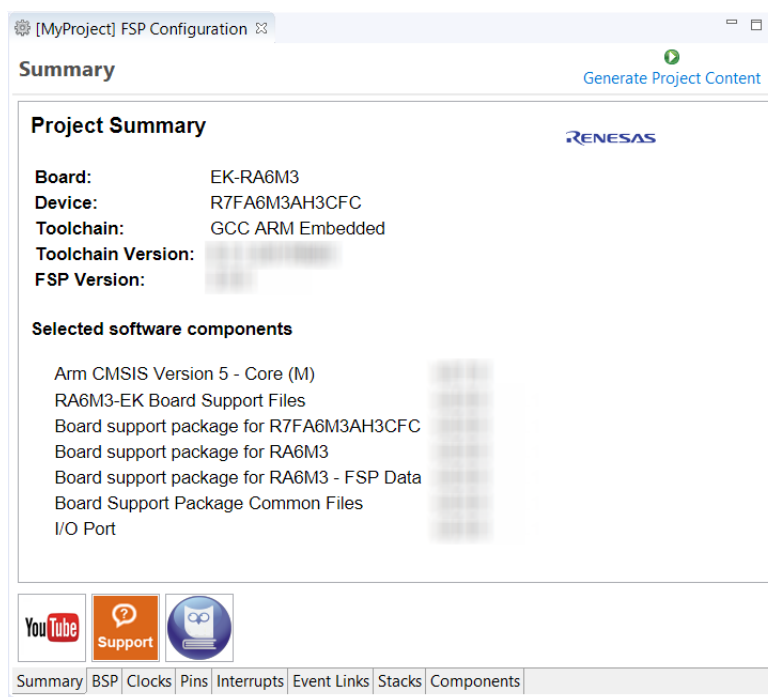


Figure 15: Configuration Summary tab

The **Summary** tab, seen in the above figure, identifies all the key elements and components of a project. It shows the target board, the device, toolchain and FSP version. Additionally, it provides a list of all the selected software components and modules used by the project. This is a more convenient summary view when compared to the **Components** tab.

The summary tab also includes handy icons with links to the Renesas YouTube channel, the Renesas support page and to the RA FSP User Manual that was downloaded during the installation process.

### 2.2.5.2 Configuring the BSP

The **BSP** tab shows the currently selected board (if any) and device. The Properties view is located in the lower left of the Project Configurations view as shown below.

*Note*

*If the Properties view is not visible, click **Window > Show View > Properties** in the top menu bar.*

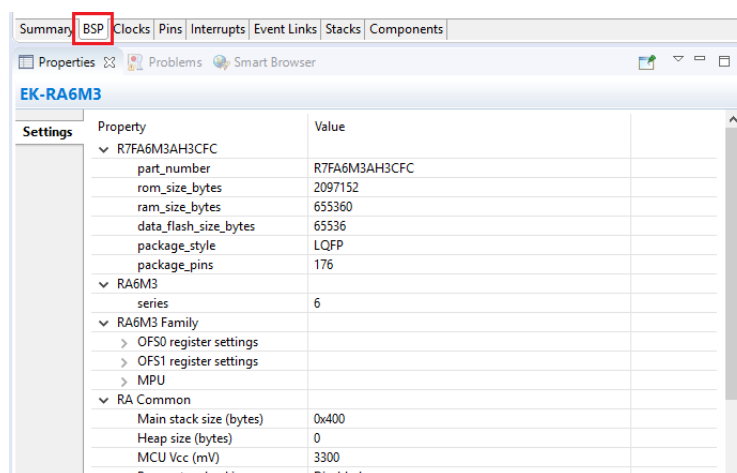


Figure 16: Configuration BSP tab

The **Properties** view shows the configurable options available for the BSP. These can be changed as required. The BSP is the FSP layer above the MCU hardware. e2 studio checks the entry fields to flag invalid entries. For example, only valid numeric values can be entered for the stack size.

When you click the **Generate Project Content** button, the BSP configuration contents are written to `ra_cfg/fsp_cfg/bsp/bsp_cfg.h`

This file is created if it does not already exist.

Warning

Do not edit this file as it is overwritten whenever the **Generate Project Content** button is clicked.

### 2.2.5.3 Configuring Clocks

The **Clocks** tab presents a graphical view of the MCU's clock tree, allowing the various clock dividers and sources to be modified. If a clock setting is invalid, the offending clock value is highlighted in red. It is still possible to generate code with this setting, but correct operation cannot be guaranteed. In the figure below, the USB clock UCLK has been changed so the resulting clock frequency is 60 MHz

instead of the required 48 MHz. This parameter is colored red.

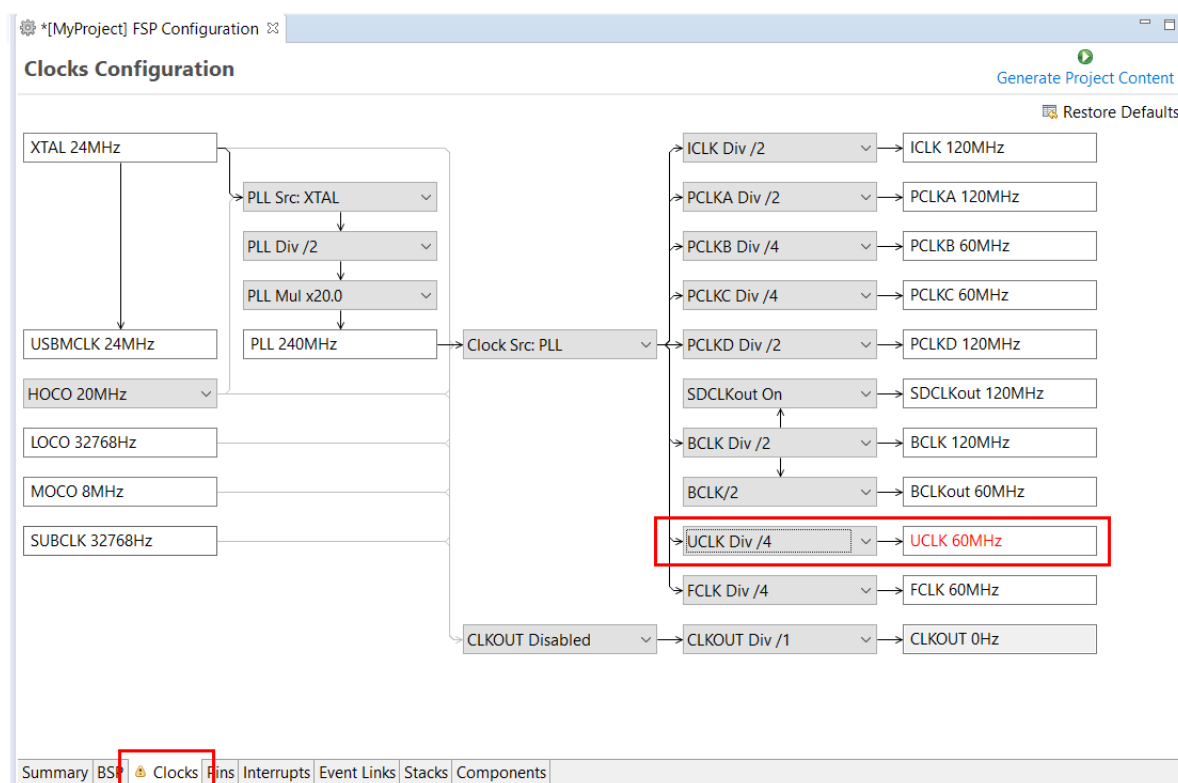


Figure 17: Configuration Clocks tab

When you click the **Generate Project Content** button, the clock configuration contents are written to: `ra_gen/bsp_clock_cfg.h`

This file will be created if it does not already exist.

#### Warning

Do not edit this file as it is overwritten whenever the **Generate Project Content** button is clicked.

### 2.2.5.4 Configuring Pins

The **Pins** tab provides flexible configuration of the MCU's pins. As many pins are able to provide multiple functions, they can be configured on a peripheral basis. For example, selecting a serial channel via the SCI peripheral offers multiple options for the location of the receive and transmit pins for that module and channel. Once a pin is configured, it is shown as green in the **Package** view.

#### Note

If the **Package** view window is not open in e2 studio, select **Window > Show View > Pin Configurator > Package** from the top menu bar to open it.

The **Pins** tab simplifies the configuration of large packages with highly multiplexed pins by highlighting errors and presenting the options for each pin or for each peripheral. If you selected a project template for a specific board such as the EK-RA6M3, some peripherals connected on the board are preselected.

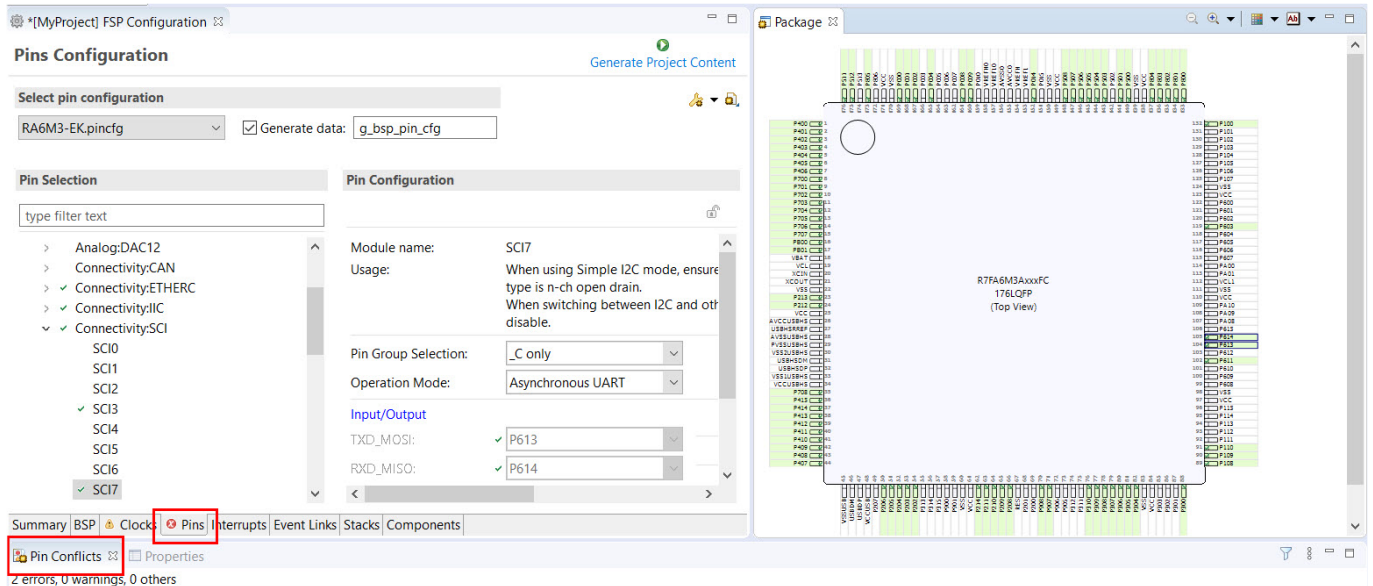


Figure 18: Pins Configuration

The pin configurator includes a built-in conflict checker, so if the same pin is allocated to another peripheral or I/O function the pin will be shown as red in the package view and also with white cross in a red square in the **Pin Selection** pane and **Pin Configuration** pane in the main **Pins** tab. The **Pin Conflicts** view provides a list of conflicts, so conflicts can be quickly identified and fixed.

#### Note

*There is a limitation in the pin configuration where it does not support setting ASEL and PSEL bit fields for the same pin. Example: When configure the DAC pin in A2A1 device, only the ASEL bit is set and the generated pin data does not match the expected pin data.*

In the example shown below, port P611 is already used by the CAC, and the attempt to connect this port to the Serial Communications Interface (SCI) results in a dangling connection error. To fix this error, select another port from the pin drop-down list or disable the CAC in the **Pin Selection** pane on the left side of the tab.

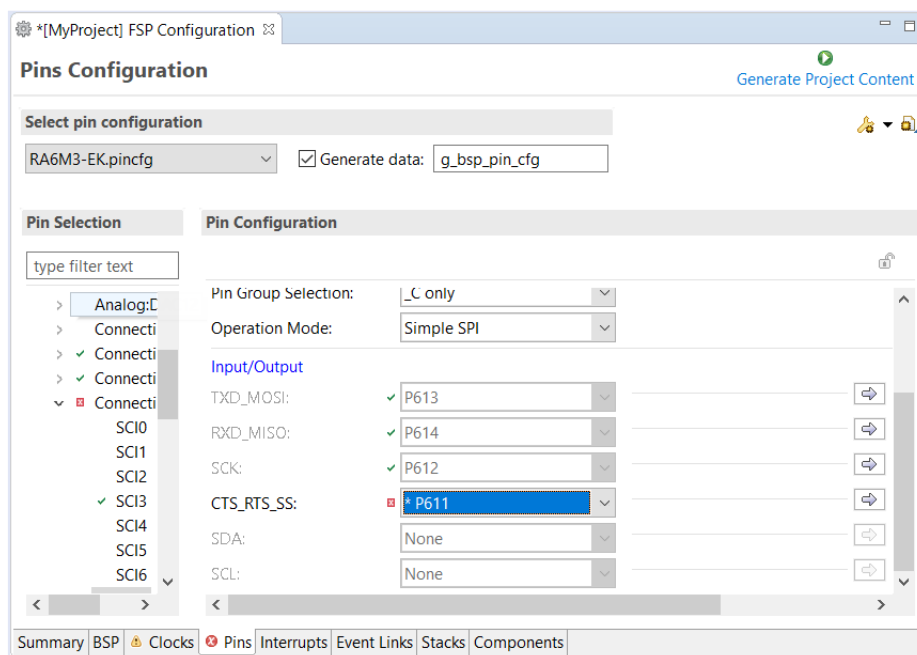


Figure 19: e2 studio Pin configurator

The pin configurator also shows a package view and the selected electrical or functional characteristics of each pin.

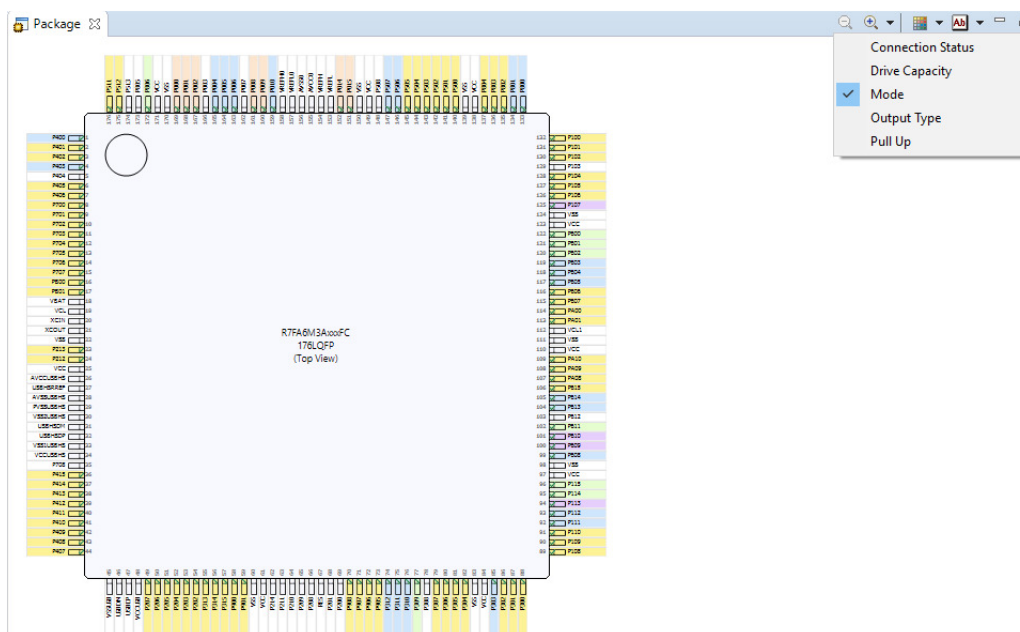


Figure 20: e2 studio Pin configurator package view

When you click the **Generate Project Content** button, the pin configuration contents are written to: `ra_gen\bsp_pin_cfg.h`

This file will be created if it does not already exist.

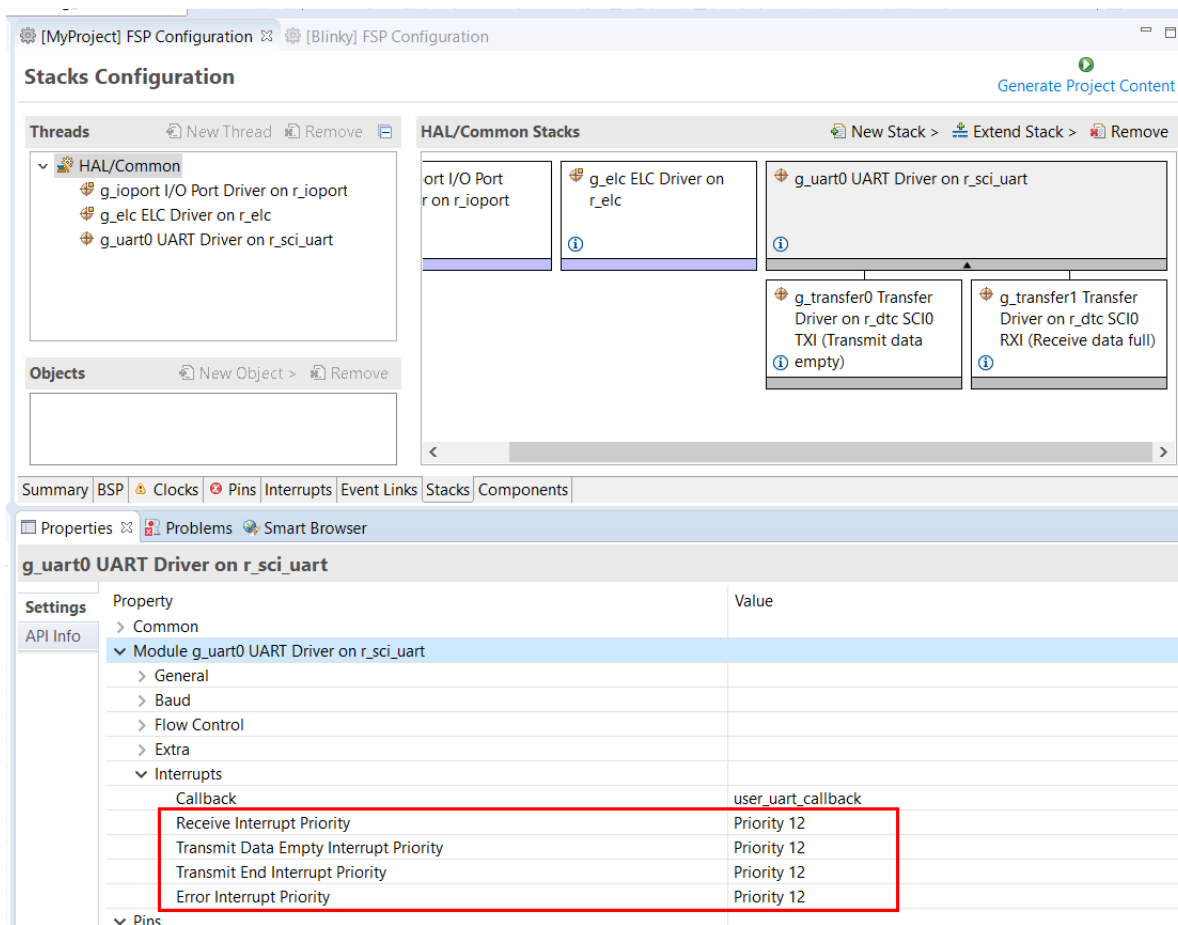
## Warning

Do not edit this file as it is overwritten whenever the **Generate Project Content** button is clicked.

To make it easy to share pinning information for your project, e2 studio exports your pin configuration settings to a csv format and copies the csv file to `ra_gen/<MCU package>.csv`.

### 2.2.5.5 Configuring Interrupts from the Stacks Tab

You can use the **Properties** view in the **Stacks** tab to enable interrupts by setting the interrupt priority. Select the driver in the **Stacks** pane to view and edit its properties.



The screenshot shows the 'Stacks Configuration' window in e2 studio. The 'HAL/Common Stacks' tab is active, displaying a list of drivers. The 'g\_uart0 UART Driver on r\_sci\_uart' driver is selected. Below the Stacks pane, the 'Properties' view for this driver is shown. The 'Interrupts' section is expanded, and the following table is visible:

Property	Value
Callback	user_uart_callback
Receive Interrupt Priority	Priority 12
Transmit Data Empty Interrupt Priority	Priority 12
Transmit End Interrupt Priority	Priority 12
Error Interrupt Priority	Priority 12

Figure 21: Configuring Interrupts in the Stacks tab

### Creating Interrupts from the Interrupts Tab

On the **Interrupts** tab, the user can bypass a peripheral interrupt set by the FSP by setting a user-defined ISR. This can be done by adding a new event via the **New User Event** button.

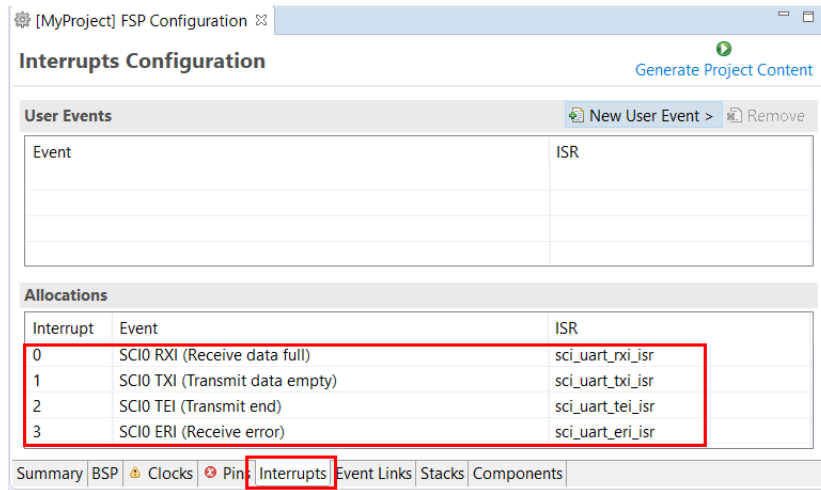


Figure 22: Configuring interrupt in Interrupt Tab

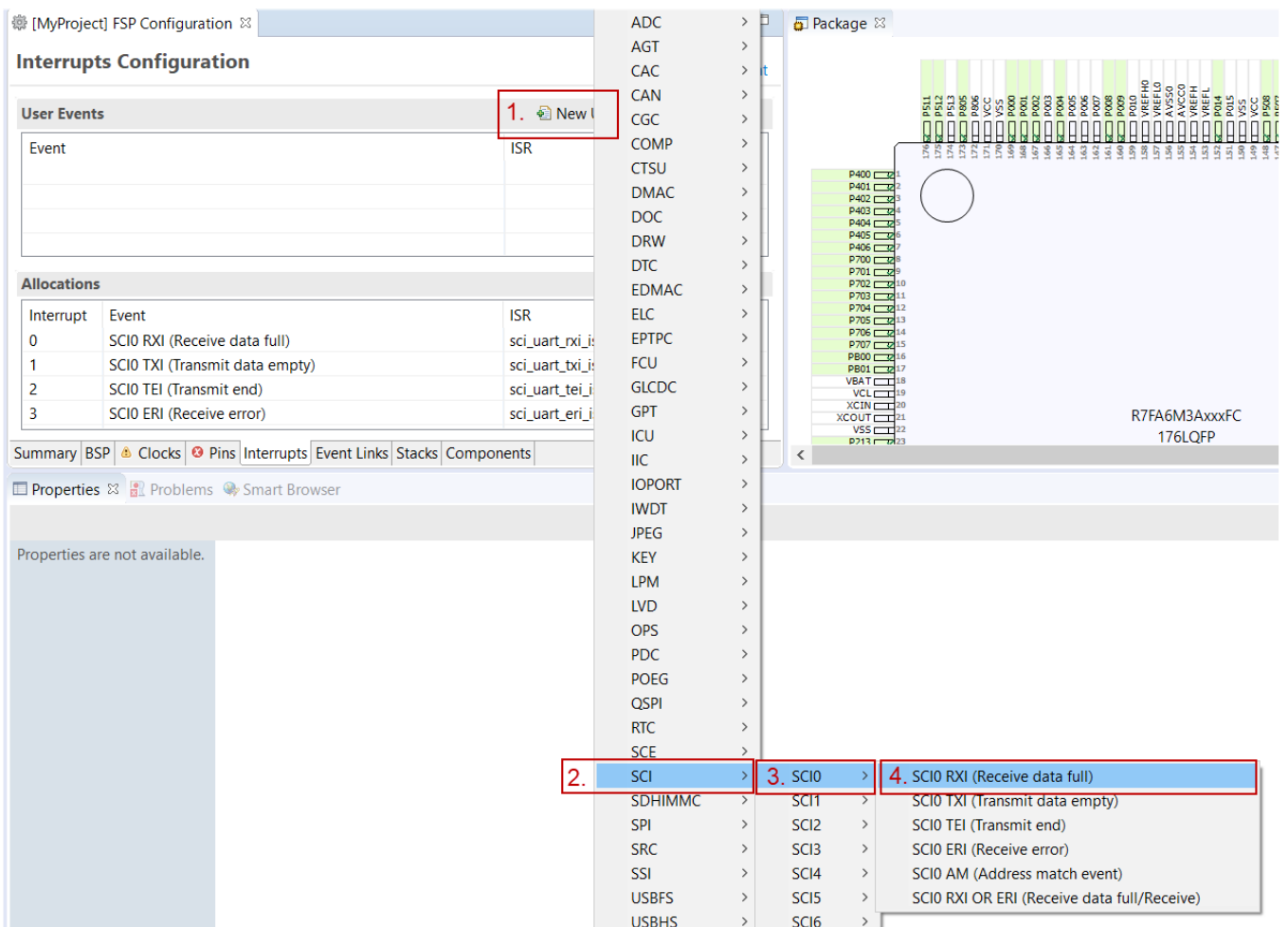


Figure 23: Adding user-defined event

Enter the name of ISR for the new user event.

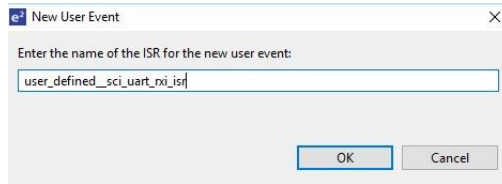


Figure 24: User-defined event ISR

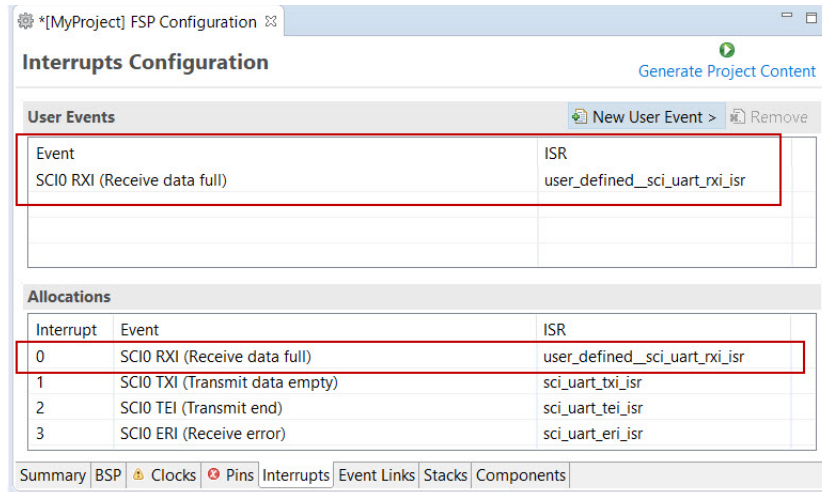


Figure 25: Using a user-defined event

### 2.2.5.6 Viewing Event Links

The Event Links tab can be used to view the Event Link Controller events. The events are sorted by peripheral to make it easy to find and verify them.

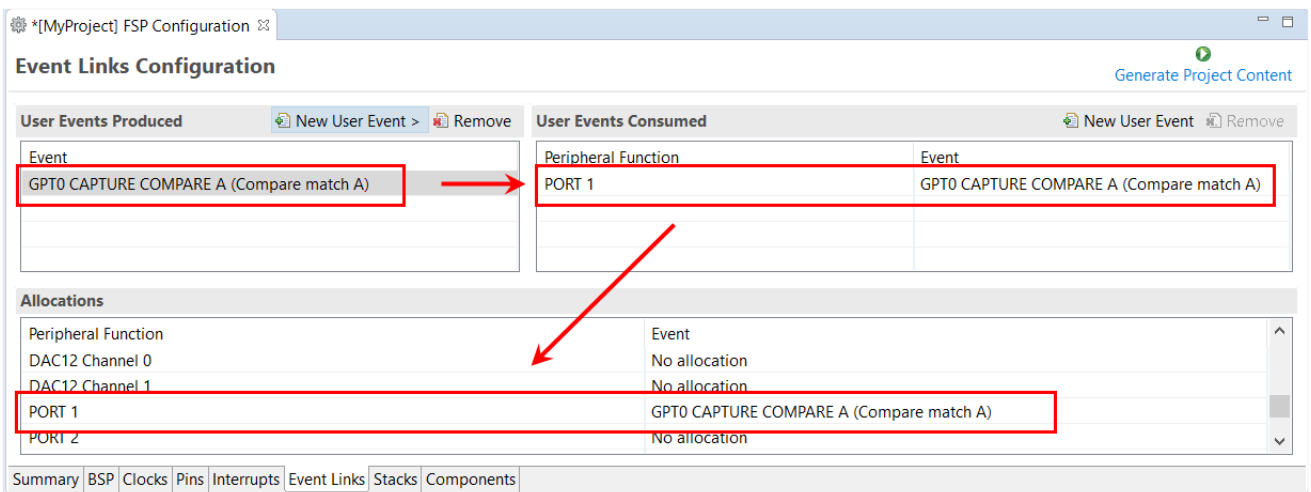


Figure 26: Viewing Event Links

Like the Interrupts tab, user-defined event sources and destinations (producers and consumers) can be defined by clicking the relevant **New User Event** button. Once a consumer is linked to a producer the link will appear in the **Allocations** section at the bottom.



*Note*

*When selecting an ELC event to receive for a module (or when manually defining an event link), only the events that are made available by the modules configured in the project will be shown.*

## 2.2.6 Adding Threads and Drivers

Every FreeRTOS-based RA Project includes at least one RTOS Thread and a stack of FSP modules running in that thread. The **Stacks** tab is a graphical user interface which helps you to add the right modules to a thread and configure the properties of both the threads and the modules associated with each thread. Once you have configured the thread, e2 studio automatically generates the code reflecting your configuration choices.

For any driver, or, more generally, any module that you add to a thread, e2 studio automatically resolves all dependencies with other modules and creates the appropriate stack. This stack is displayed in the Stacks pane, which e2 studio populates with the selected modules and module options for the selected thread.

The default view of the **Stacks** tab includes a Common Thread called **HAL/Common**. This thread includes the driver for I/O control (IOPORT). The default stack is shown in the **HAL/Common Stacks** pane. The default modules added to the HAL/Common driver are special in that the FSP only requires a single instance of each, which e2 studio then includes in every user-defined thread by default.

In applications that do not use an RTOS or run outside of the RTOS, the HAL/Common thread becomes the default location where you can add additional drivers to your application.

For a detailed description on how to add and configure modules and stacks, see the following sections:

- [Adding and Configuring HAL Drivers](#)
- [Adding Drivers to a Thread and Configuring the Drivers](#)

Once you have added a module either to HAL/Common or to a new thread, you can access the driver's configuration options in the **Properties** view. If you added thread objects, you can access the objects configuration options in the **Properties** view in the same way.

You can find details about how to configure threads here: [Configuring Threads](#)

*Note*

*Driver and module selections and configuration options are defined in the FSP pack and can therefore change when the FSP version changes.*

### 2.2.6.1 Adding and Configuring HAL Drivers

For applications that run outside or without the RTOS, you can add additional HAL drivers to your application using the HAL/Common thread. To add drivers, follow these steps:

1. Click on the HAL/Common icon in the **Stacks** pane. The Modules pane changes to **HAL/Common Stacks**.

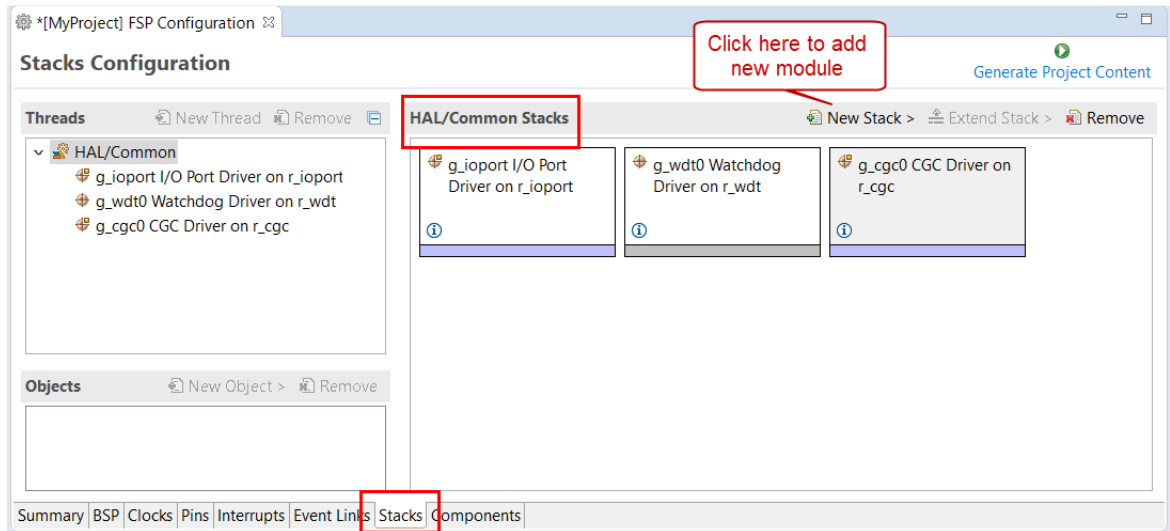


Figure 27: e2 studio Project configurator - Adding drivers

2. Click **New Stack** to see a drop-down list of HAL level drivers available in the FSP.
3. Select a driver from the menu **New Stack > Driver**.

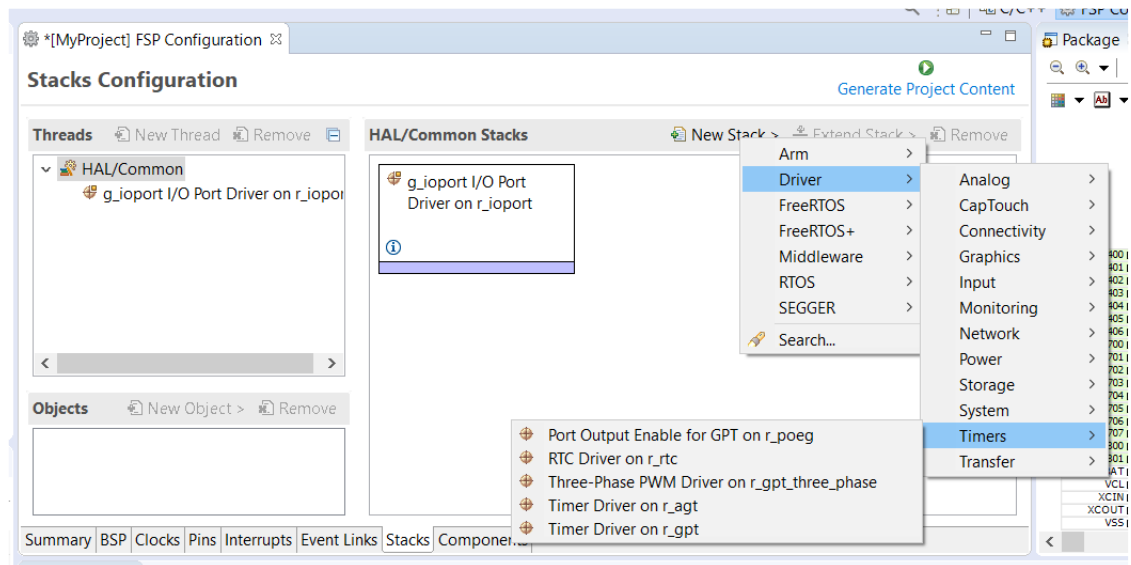


Figure 28: Select a driver

4. Select the driver module in the **HAL/Common Modules** pane and configure the driver properties in the **Properties** view.

e2 studio adds the following files when you click the **Generate Project Content** button:

- The selected driver module and its files to the ra/fsp directory
- The main() function and configuration structures and header files for your application as shown in the table below.

File	Contents	Overwritten by Generate Project Content?
------	----------	------------------------------------------

ra_gen/main.c	Contains main() calling generated and user code. When called, the BSP already has Initialized the MCU.	Yes
ra_gen/hal_data.c	Configuration structures for HAL Driver only modules.	Yes
ra_gen/hal_data.h	Header file for HAL driver only modules.	Yes
src/hal_entry.c	User entry point for HAL Driver only code. Add your code here.	No

The configuration header files for all included modules are created or overwritten in this folder:  
ra\_cfg/fsp\_cfg

### 2.2.6.2 Adding Drivers to a Thread and Configuring the Drivers

For an application that uses the RTOS, you can add one or more threads, and for each thread at least one module that runs in the thread. You can select modules from the Driver dropdown menu. To add modules to a thread, follow these steps:

1. In the **Threads** pane, click **New Thread** to add a Thread.

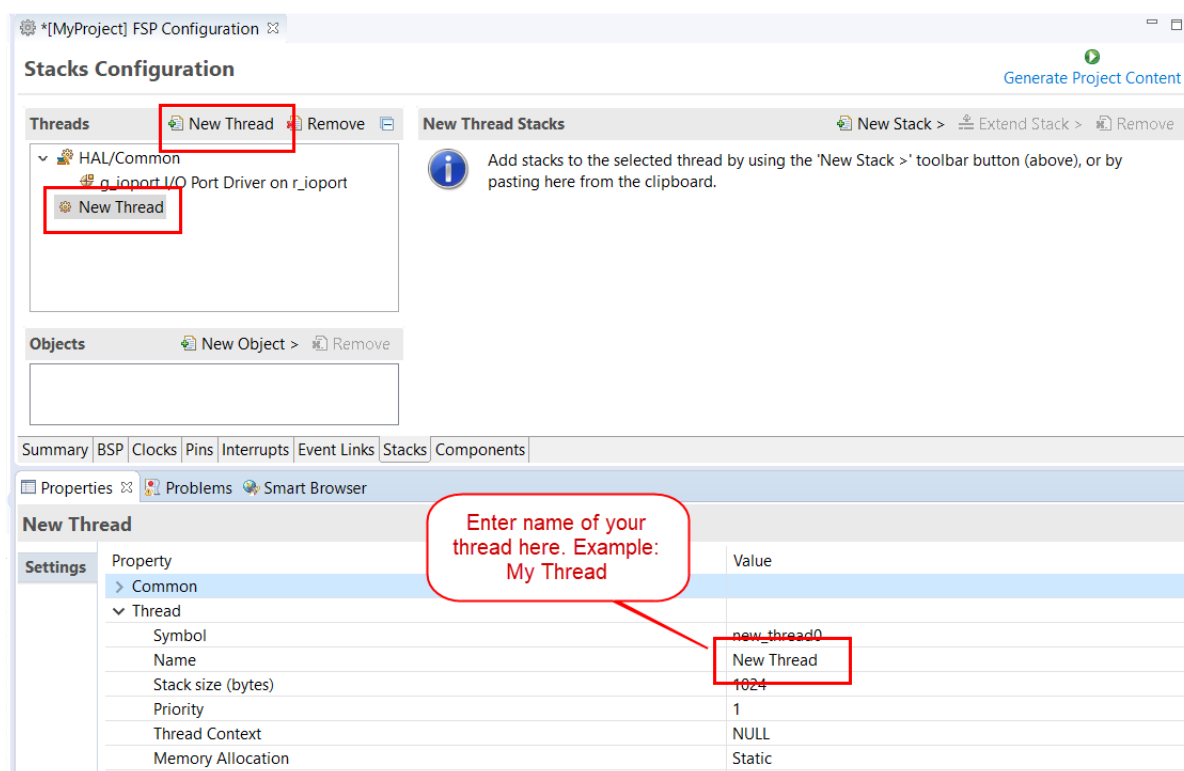


Figure 29: Adding a new RTOS Thread on the Stacks tab

2. In the **Properties** view, click on the **Name** and **Symbol** entries and enter a distinctive name and symbol for the new thread.

Note

*e2 studio updates the name of the thread stacks pane to **My Thread Stacks**.*

3. In the **My Thread Stacks** pane, click on **New Stack** to see a list of modules and drivers. HAL-level drivers can be added here.

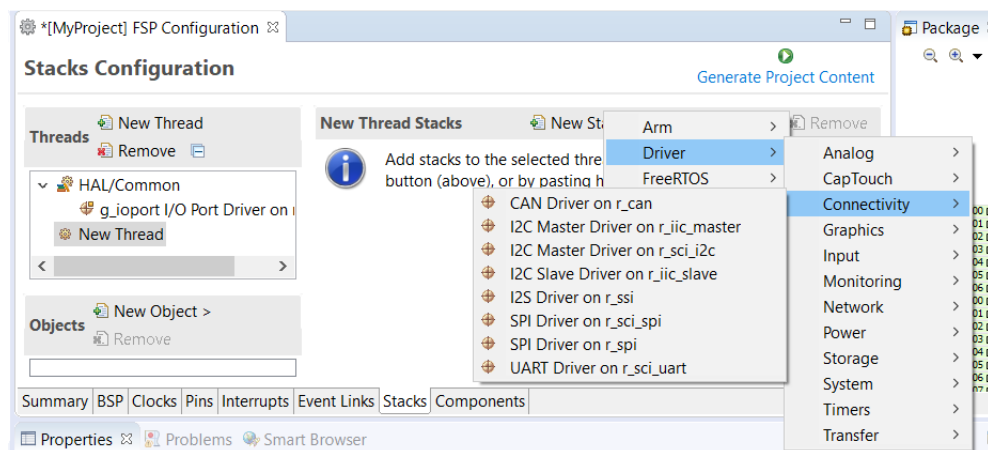


Figure 30: Adding Modules and Drivers to a thread

4. Select a module or driver from the list.
5. Click on the added driver and configure the driver as required by the application by updating the configuration parameters in the **Properties** view. To see the selected module or driver and be able to edit its properties, make sure the Thread containing the driver is highlighted in the **Threads** pane.

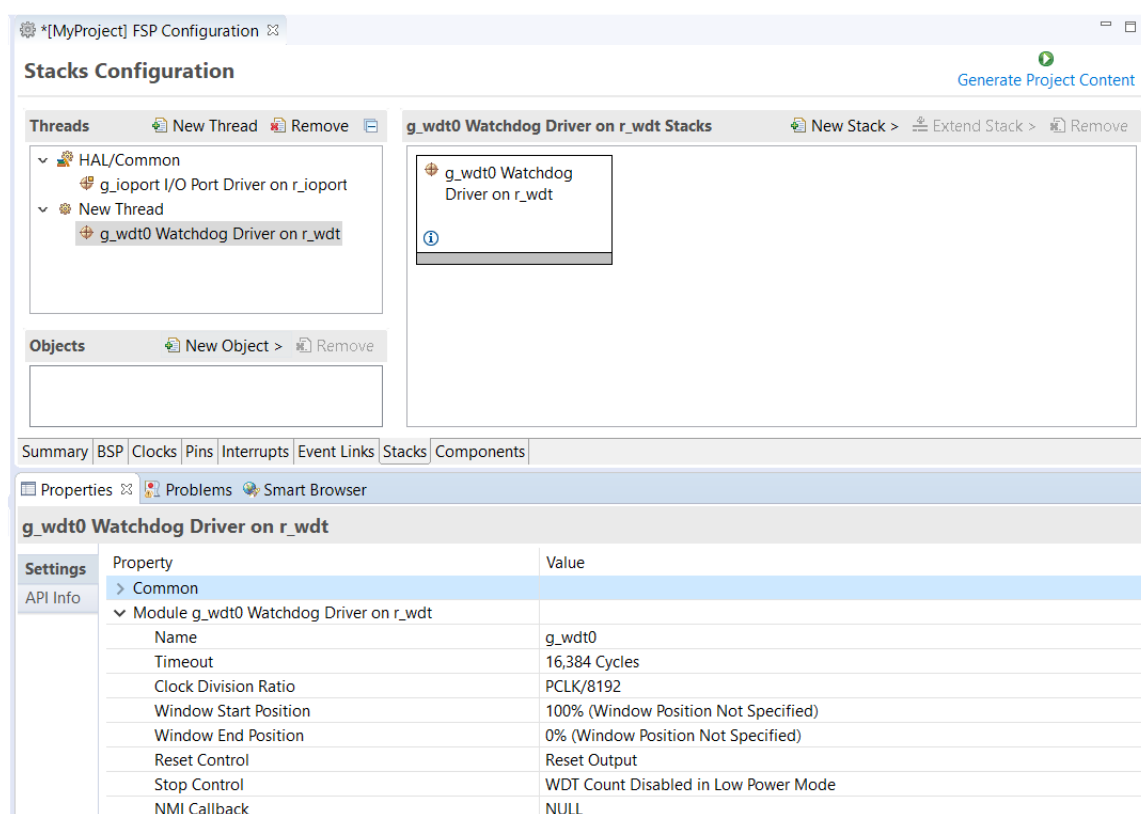


Figure 31: Configuring Module or Driver properties

6. If needed, add another thread by clicking **New Thread** in the **Threads** pane.

When you press the **Generate Project Content** button for the example above, e2 studio creates the files as shown in the following table:

File	Contents	Overwritten by Generate Project Content?
ra_gen/main.c	Contains main() calling generated and user code. When called the BSP will have initialized the MCU.	Yes
ra_gen/my_thread.c	Generated thread "my_thread" and configuration structures for modules added to this thread.	Yes
ra_gen/my_thread.h	Header file for thread "my_thread"	Yes
ra_gen/hal_data.c	Configuration structures for HAL Driver only modules.	Yes
ra_gen/hal_data.h	Header file for HAL Driver only modules.	Yes
src/hal_entry.c	User entry point for HAL Driver only code. Add your code here.	No

src/my_thread_entry.c	User entry point for thread "my_thread". Add your code here.	No
-----------------------	--------------------------------------------------------------	----

The configuration header files for all included modules and drivers are created or overwritten in the following folders: ra\_cfg/fsp\_cfg/<header files>

### 2.2.6.3 Configuring Threads

If the application uses the FreeRTOS, the **Stacks** tab can be used to simplify the creation of FreeRTOS threads, semaphores, mutexes, and event flags.

The components of each thread can be configured from the **Properties** view as shown below.

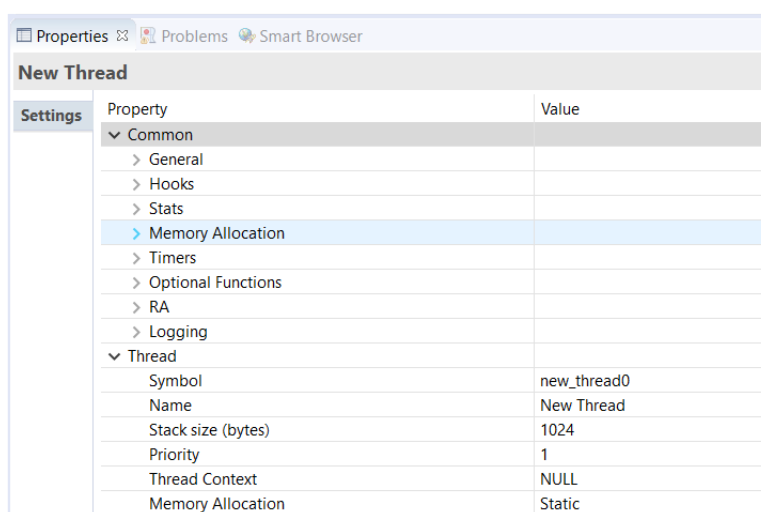


Figure 32: New Thread Properties

The **Properties** view contains settings common for all Threads (**Common**) and settings for this particular thread (**Thread**).

For this thread instance, the thread's name and properties (such as priority level or stack size) can be easily configured. e2 studio checks that the entries in the property field are valid. For example, it will verify that the field **Priority**, which requires an integer value, only contains numeric values between 0 and 9.

To add FreeRTOS resources to a Thread, select a thread and click on **New Object** in the Thread Objects pane. The pane takes on the name of the selected thread, in this case **My Thread Objects**.

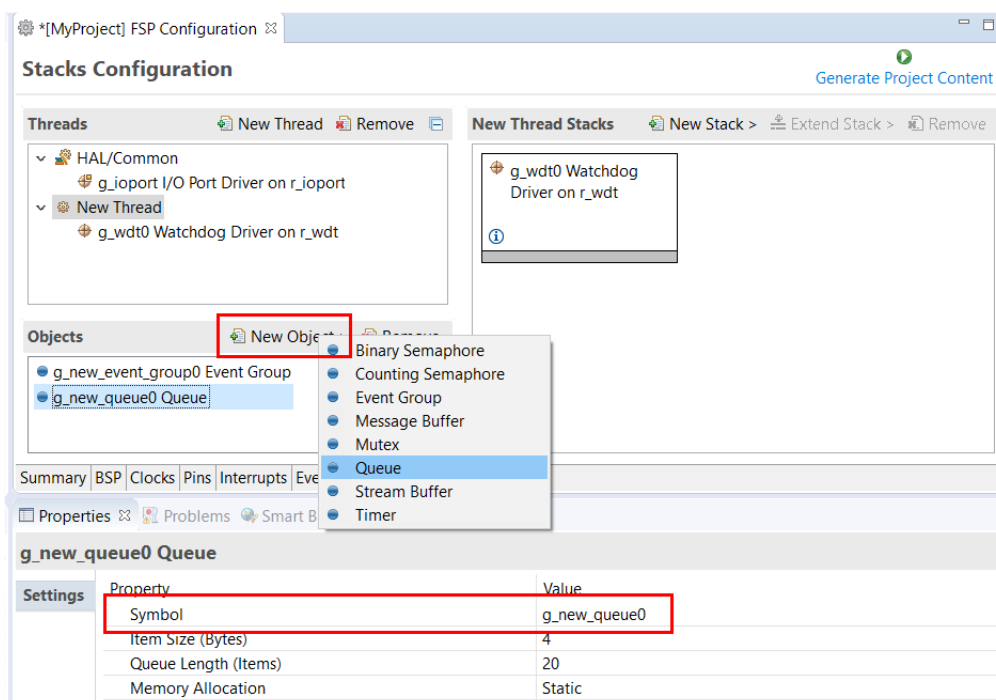


Figure 33: Configuring Thread Object Properties

Make sure to give each thread object a unique name and symbol by updating the **Name** and **Symbol** entries in the **Properties** view.

## 2.2.7 Reviewing and Adding Components

The **Components** tab enables the individual modules required by the application to be included or excluded. Modules common to all RA MCU projects are preselected (for example: **BSP > BSP > Board-specific BSP** and **HAL Drivers > all > r\_cgc**). All modules that are necessary for the modules selected in the **Stacks** tab are included automatically. You can include or exclude additional modules by ticking the box next to the required component.

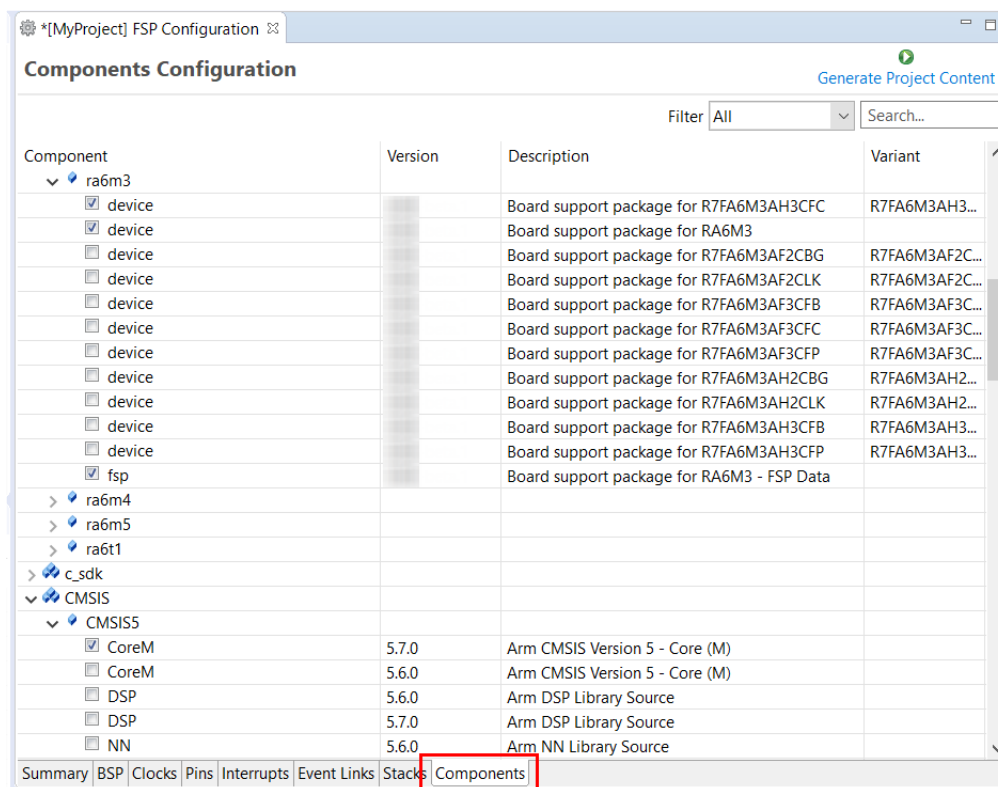


Figure 34: Components Tab

Clicking the **Generate Project Content** button copies the .c and .h files for each selected component into the following folders:

- ra/fsp/inc/api
- ra/fsp/inc/instances
- ra/fsp/src/bsp
- ra/fsp/src/<Driver\_Name>

e2 studio also creates configuration files in the ra\_cfg/fsp\_cfg folder with configuration options set in the **Stacks** tab.

## 2.2.8 Writing the Application

Once you have added Modules and drivers and set their configuration parameters in the **Stacks** tab, you can add the application code that calls the Modules and drivers.

*Note*

*To check your configuration, build the project once without errors before adding any of your own application code.*

### 2.2.8.1 Coding Features

e2 studio provides several efficiency improving features that help write code. Review these features prior to digging into the code development step-by-step sections that follow.

#### Autocomplete

Autocomplete is a context aware coding accelerator that suggests possible completions for partially



typed-in code elements. If you can 'guess' the first part of a macro, for example, the Autocomplete function can suggest options for completing the rest of the macro.

In the following example, a macro related to a BSP\_IO setting needs to be found. After typing BSP\_IO\_ in a source code file, pressing Ctrl + Space opens the Autocomplete list. This list shows a selection of context aware options for completing the macro. Scroll through the window to find the desired macro (in this case BSP\_IO\_LEVEL\_HIGH) and click on it to add it to your code.

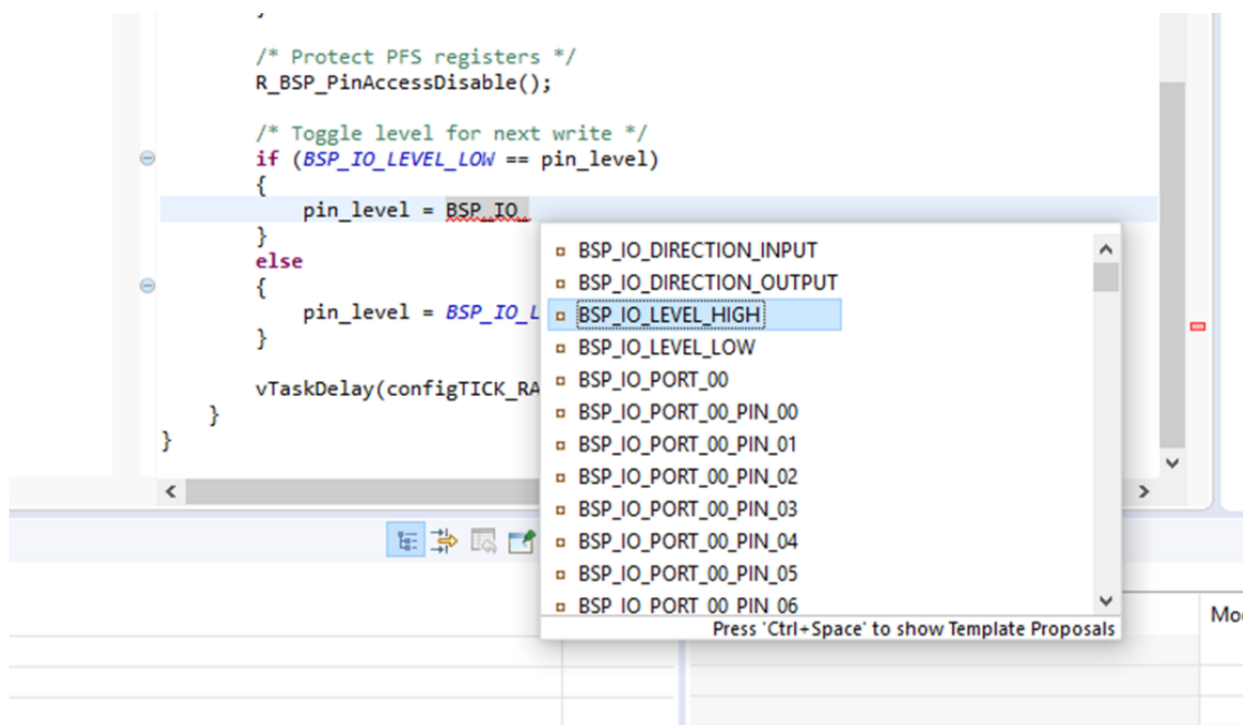


Figure 35: Autocomplete example

Other code elements can use autocomplete too. Some of the more common uses for Autocomplete include Enumerations, Types, and API functions - but try it in any situation you think the tool may have enough context to determine what you might be looking for.

For a hands-on experience using Autocomplete use the Quick FSP Labs for [Creating Blinky from Scratch](#) and [Creating an RTC Blinky from Scratch](#). These 15-minute Do it Yourself labs take you through the step-by-step process of using Autocomplete, Developer Assistance, Edit hover, and the Help system.

### Edit Hover

e2 studio supports hovers in the textual editor. This function can be enabled or disabled via **Window > Preferences > C/C++ > Editor > Hovers**.

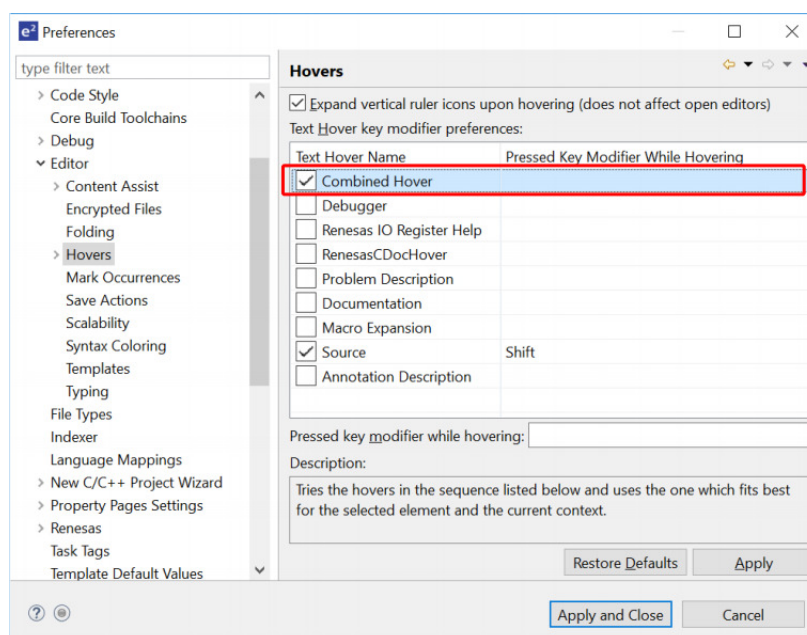


Figure 36: Hover preference

To enable hover, check **Combined Hover** box. To disable it, uncheck this box. By default, it is enabled. The Hover function allows a user to view detailed information about any identifiers in the source code by hovering the mouse over an identifier and checking the pop-up.

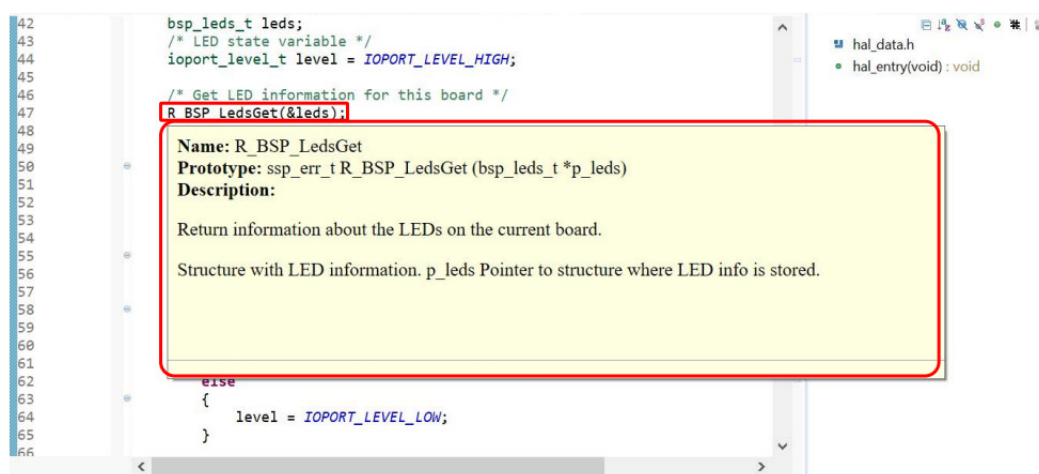


Figure 37: Hover Example

For a hands-on experience using Edit Hover use the Quick FSP Labs for [Creating Blinky from Scratch](#) and [Creating an RTC Blinky from Scratch](#). These 15-minute Do it Yourself labs take you through the step-by-step process of using Autocomplete, Developer Assistance, Edit hover, and the Help system.

## Welcome Window

The e2 studio Welcome window displays useful information and common links to assist in development. Check out these resources to see what is available. They are updated with each release, so check back to see what has been added after a new release.

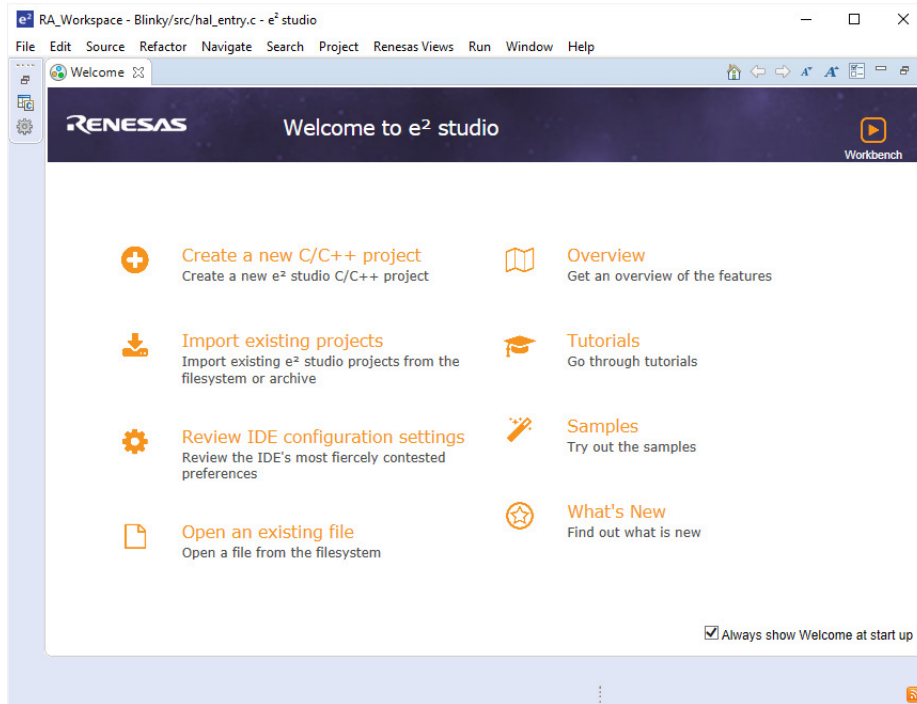


Figure 38: Welcome window

## Cheat Sheets

Cheat sheets are macro driven illustrations of some common tasks. They show, step-by-step, what commands and menus are used. These will be populated with more examples on each release. Cheat Sheets are available from the **Help** menu.

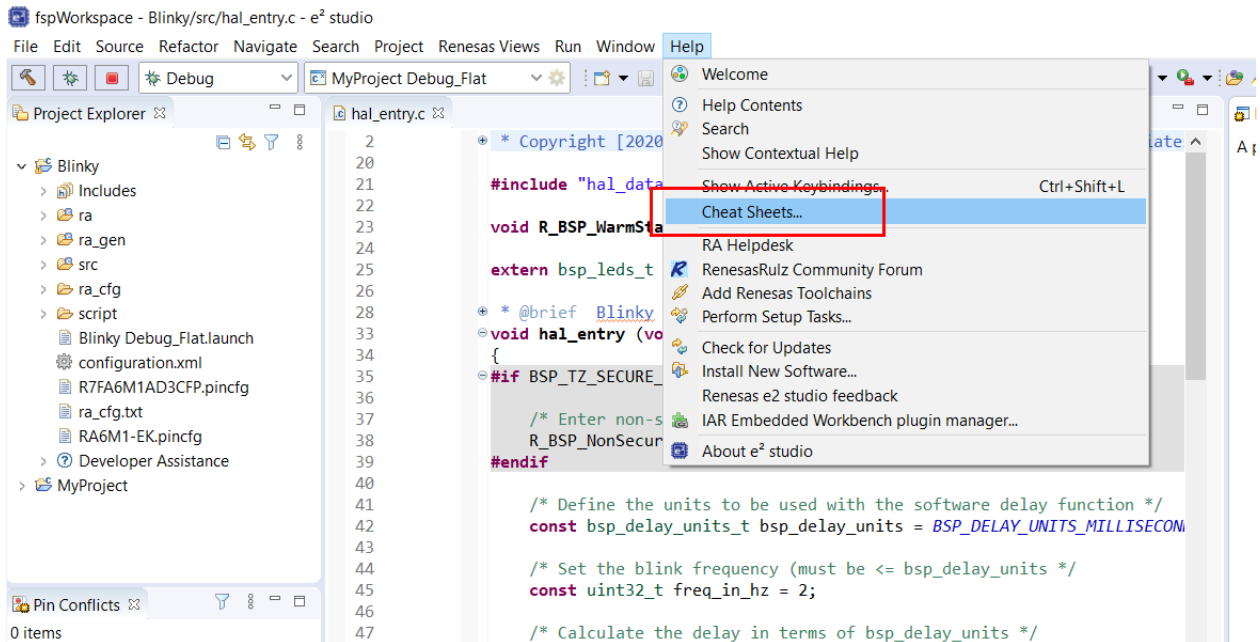


Figure 39: Cheat Sheets

## Developer Assistance

FSP Developer Assistance provides developers with module and Application Programming Interface (API) reference documentation in e2 studio. After configuring the threads and software stacks for an FSP project with the RA Configuration editor, Developer Assistance quickly helps you get started writing C/C++ application code for the project using the configured stack modules.

### 1. Expand the project explorer to view Developer Assistance

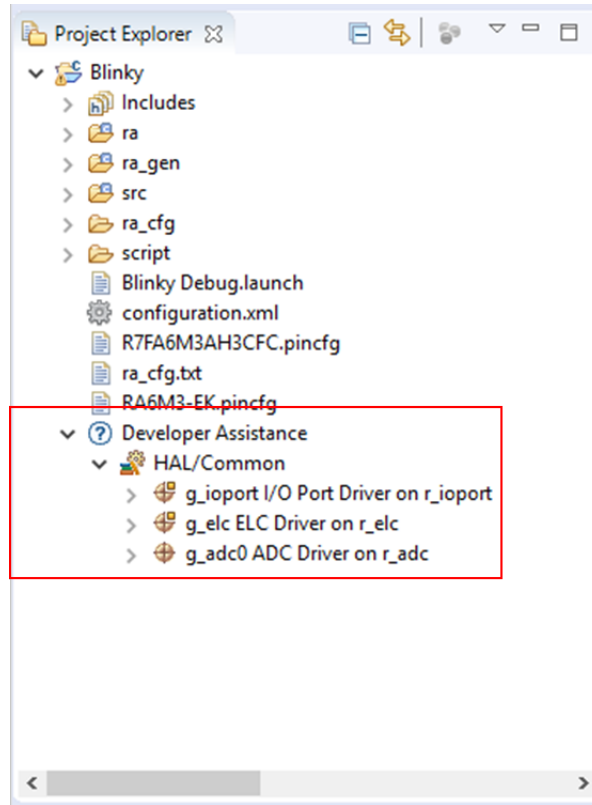


Figure 40: Developer Assistance

### 2. Expand a stack module to show its APIs

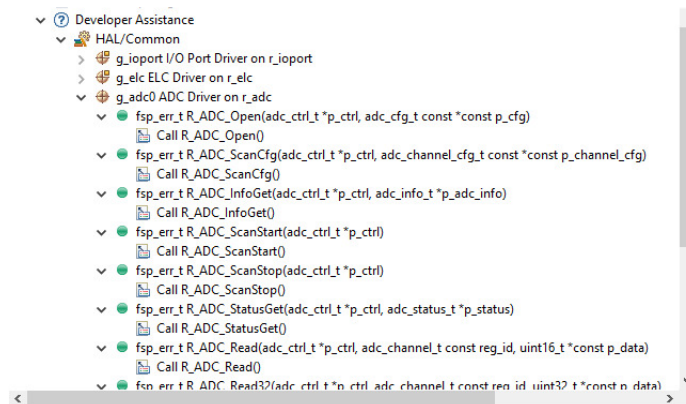


Figure 41: Developer Assistance APIs

### 3. Dragging and dropping an API from Developer Assistance to a source file helps to write source

code quickly.

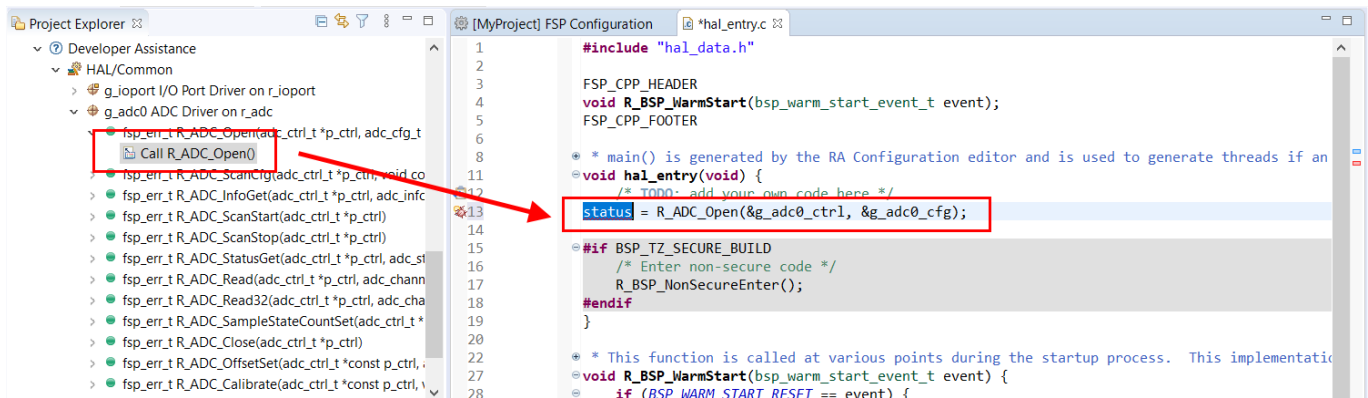


Figure 42: Dragging and Dropping an API in Developer Assistance

For a hands-on experience using Developer Assistance use the Quick FSP Labs for [An Introduction to Developer Assistance](#), [Creating Blinky from Scratch](#) and [Creating an RTC Blinky from Scratch](#). These 15-minute Do it Yourself labs take you through the step-by-step process of using Autocomplete, Developer Assistance, Edit hover, and the Help system.

### Information Icon

Information icons are available on each module in the thread stack. Clicking on these icons opens a module folder on GitHub that contains additional information on the module. An example information icon is shown below:

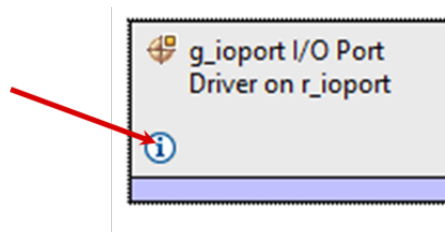


Figure 43: Information icon

### IDE Help

A good source of additional information for many FSP topics is the Help system. To get to the Help system, click on **Help** and then select **Help Contents** as seen below.

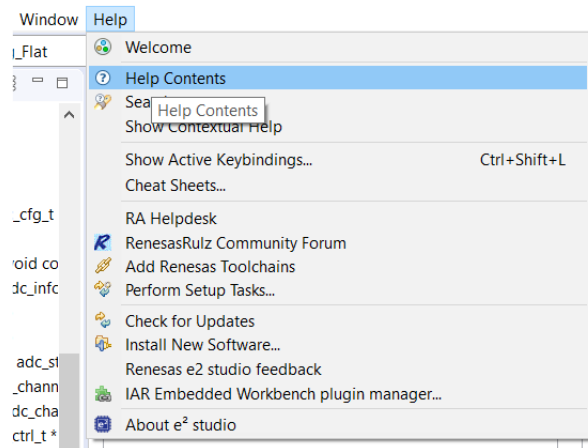


Figure 44: Opening the Help System

Once the Help system is open, select the **RA Contents** entry in the left side Guide-bar. Expand it to see the main RA Topics.

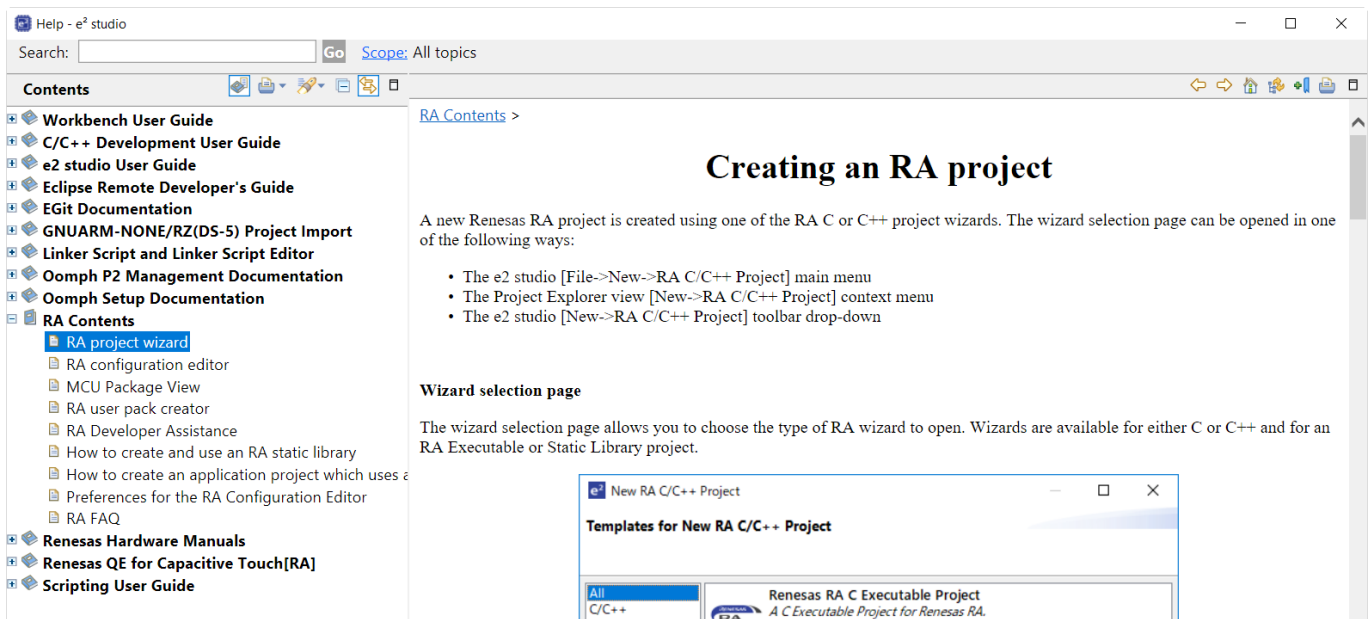


Figure 45: RA Content Help

You can also search for help topics by using the Search bar. Below is an example searching for Visual Expressions, a helpful feature in the e2 studio debugger.

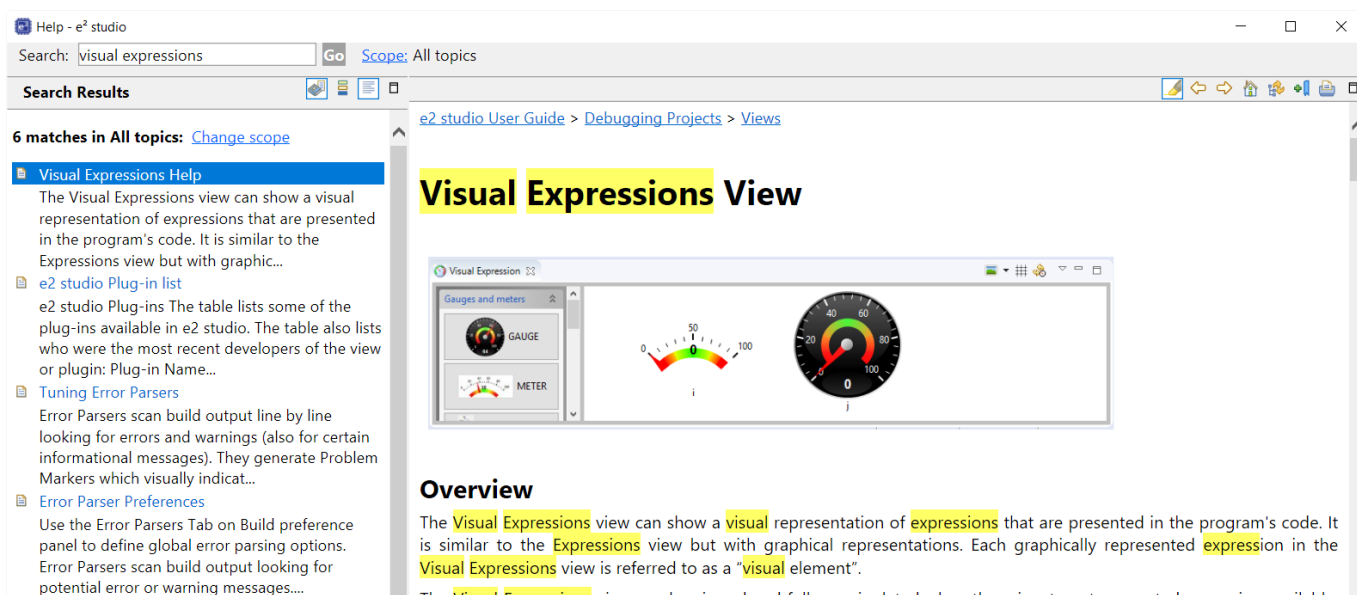


Figure 46: e2 studio Help from the Search Bar

For a hands-on experience using the Help system use the Quick FSP Labs for [An Introduction to Developer Assistance](#), [Creating Blinky from Scratch](#) and [Creating an RTC Blinky from Scratch](#). These 15-minute Do it Yourself labs take you through the step-by-step process of using Autocomplete, Developer Assistance, Edit hover, and the Help system.

### 2.2.8.2 HAL Modules in FSP: A Practical Description

The [FSP Architecture](#) section describes FSP stacks, modules and interfaces in significant detail, providing an understanding of the theory behind them. The following sections provides a quick and practical introduction on how to use API functions when writing code and where in the API reference sections you can find useful API related information.

#### Introduction to HAL Modules

In FSP, HAL module drivers provide convenient API functions that access RA processor peripheral features. Module properties are defined in the RA GUI configurator, eliminating the tedious and error prone process of setting peripheral control registers. When configuration is complete, the generator automatically creates the code needed to implement the associated API functions. API functions are the main way a developer interacts with the target processor and peripherals.

#### HAL Driver API Function Call Formats

HAL driver API functions all have a similar format. They all start with "R\_" to indicate they are HAL related functions. Next comes the module name followed by the function and any parameters. This format is illustrated below:

```
R_<module>_<function>( <parameters> );
```

Here are some examples:



```

status = R_GPT_Open(&g_timer0_ctrl, &g_timer0_cfg);
status = R_GPT_Start(&g_timer0_ctrl);
status = R_GPT_PeriodSet(&g_timer0_ctrl, period);
status = R_ADC_Open(&g_adc0_ctrl, &g_adc0_cfg);
status = R_ADC_InfoGet(&g_adc0_ctrl, &adc_info);

```

## HAL Driver API Call Reference Information

Each HAL module has a useful API Reference section that includes key details on each function. The function prototype is presented first, showing the return type (usually `fsp_status_t` for HAL functions) and the function parameters. A short description and any warnings or notes follow the function definition. In some cases, a code snippet is included to illustrate use of the function. Finally, all possible return values are provided to assist in debugging and error management.

### ◆ R\_GPT\_PeriodSet()

```

fsp_err_t R_GPT_PeriodSet ( timer_ctrl_t *const p_ctrl,
                          uint32_t const   period_counts
                          )

```

Sets period value provided. If the timer is running, the period will be updated after the next counter overflow. If the timer is stopped, this function resets the counter and updates the period. Implements `timer_api_t::periodSet`.

**Warning**  
If periodic output is used, the duty cycle buffer registers are updated after the period buffer register. If this function is called while the timer is running and a GPT overflow occurs during processing, the duty cycle will not be the desired 50% duty cycle until the counter overflow after processing completes.

Example:

```

/* Get the source clock frequency (in Hz). There are 3 ways to do this in FSP:
 * - If the PCLKD frequency has not changed since reset, the source clock
 *   frequency is
 *   BSP_STARTUP_PCLKD_HZ >> timer_cfg_t::source_div
 * - Use the R_GPT_InfoGet function (it accounts for the divider).
 * - Calculate the current PCLKD frequency using R_FSP_SystemClockHzGet
 *   (FSP_PRIV_CLOCK_PCLKD) and right shift
 *   by timer_cfg_t::source_div.
 * This example uses the 3rd option (R_FSP_SystemClockHzGet).
 */
uint32_t pclkd_freq_hz = R_FSP_SystemClockHzGet(FSP_PRIV_CLOCK_PCLKD) >>
    g_timer0_cfg.source_div;

/* Calculate the desired period based on the current clock. Note that this
 * calculation could overflow if the
 * desired period is larger than UINT32_MAX / pclkd_freq_hz. A cast to uint64_t is
 * used to prevent this. */
uint32_t period_counts =
    (uint32_t) (((uint64_t) pclkd_freq_hz * GPT_EXAMPLE_DESIRED_PERIOD_MSEC) /
    GPT_EXAMPLE_MSEC_PER_SEC);

/* Set the calculated period. */
err = R_GPT_PeriodSet(&g_timer0_ctrl, period_counts);
handle_error(err);

```

**Return values**

<code>FSP_SUCCESS</code>	Period value written successfully.
<code>FSP_ERR_ASSERTION</code>	<code>p_ctrl</code> was NULL.
<code>FSP_ERR_NOT_OPEN</code>	The instance is not opened.

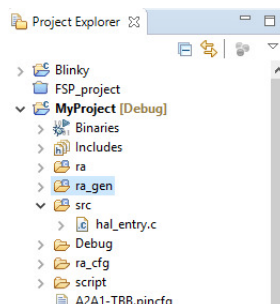
Figure 47: Module Api Reference Section Example

### 2.2.8.3 RTOS-Independent Applications

To write application code:



1. Add all drivers and modules in the **Stacks** tab and resolve all dependencies flagged by e2 studio such as missing interrupts or drivers.
2. Configure the drivers in the **Properties** view.
3. In the Project Configuration view, click the **Generate Project Content** button.
4. In the **Project Explorer** view, double-click on the src/hal\_entry.c file to edit the source file.

*Note*

All configuration structures necessary for the driver to be called in the application are initialized in `ra_gen/hal_data.c`.

**Warning**

Do not modify the files in the directory `ra_gen`. These files are overwritten every time you push the **Generate Project Content** button.

5. Add your application code here:

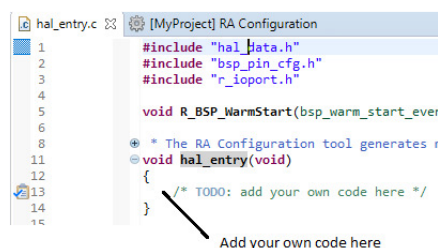


Figure 48: Adding user code to hal\_entry.c

6. Build the project without errors by clicking on **Project > Build Project**.

The following tutorial shows how execute the steps above and add application code: [Tutorial: Using HAL Drivers - Programming the WDT](#).

The WDT example is a HAL level application which does not use an RTOS. The user guides for each module also include basic application code that you can add to `hal_entry.c`.

### 2.2.8.4 RTOS Applications

To write RTOS-aware application code using FreeRTOS, follow these steps:

1. Add a thread using the **Stacks** tab.
2. Provide a unique name for the thread in the **Properties** view for this thread.

3. Configure all drivers and resources for this thread and resolve all dependencies flagged by e2 studio such as missing interrupts or drivers.
  4. Configure the thread objects.
  5. Provide unique names for each thread object in the **Properties** view for each object.
  6. Add more threads if needed and repeat steps 1 to 5.
  7. In the **RA Project Editor**, click the **Generate Project Content** button.
8. In the **Project Explorer** view, double-click on the src/my\_thread\_1\_entry.c file to edit the source file.

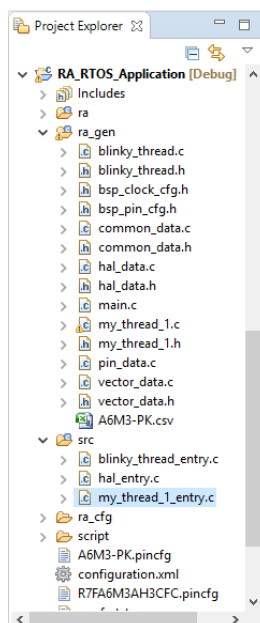


Figure 49: Generated files for an RTOS application

*Note*

All configuration structures necessary for the driver to be called in the application are initialized in ra\_gen/my\_thread\_1.c and my\_thread\_2.c

**Warning**

Do not modify the files in the directory ra\_gen. These files are overwritten every time you push the **Generate Project Content** button.

9. Add your application code here:

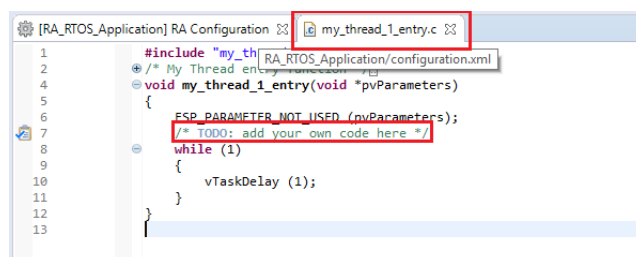


Figure 50: Adding user code to my\_thread\_1.entry

10. Repeat steps 1 to 9 for the next thread.

11. Build your project without errors by clicking on **Project > Build Project**.

## 2.2.8.5 Additional Resources for Application Development

### Example Projects

A wide variety of Example Projects for FSP and RA MCUs is available on the GitHub site here: <https://github.com/renesas/ra-fsp-examples>. Example projects are organized by target kit so it is easy to find all the examples for your kit of choice.

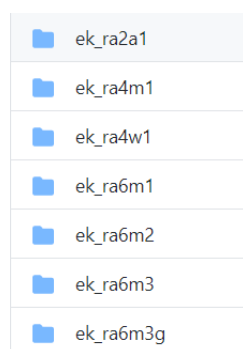


Figure 51: FSP Example Projects Organized by Kit

Projects are available as both downloadable zip files and as project source files. Typically, there is a project for each module. New example projects are being added periodically, so check back if a particular module isn't yet available.

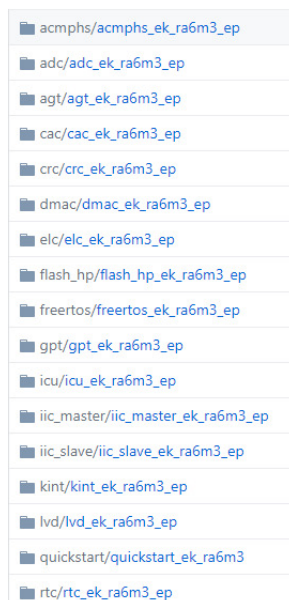


Figure 52: A Selection of Example Projects Available on GitHub

### Quick Labs

A variety of Hands-on Do It Yourself labs are available on the Renesas RA and FSP Knowledge Base. Quick FSP Labs target the EK-RA6M3 kit and typically require only 15 minutes to complete. Each lab covers a couple related development tools and techniques like Edit Hover, Autocomplete, Developer

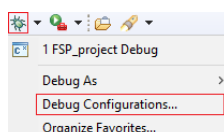
Assistance, console I/O over RTT, and Visual Expressions, that can speed up the development process. A list of all available Quick Labs can be found here: <https://en-support.renesas.com/knowledgeBase/19450948>

## 2.2.9 Debugging the Project

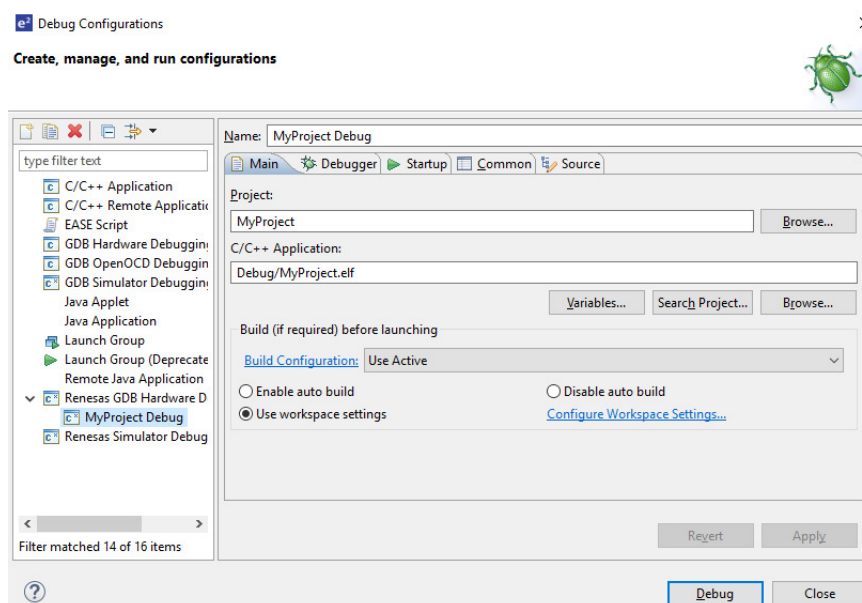
Once your project builds without errors, you can use the Debugger to download your application to the board and execute it.

To debug an application follow these steps:

1. On the drop-down list next to the debug icon, select **Debug Configurations**.



2. In the **Debug Configurations** view, click on your project listed as **MyProject Debug**.



3. Connect the board to your PC via either a standalone Segger J-Link debugger, a Segger J-Link On-Board (included on all RA EKs), or an E2 or E2 Lite and click **Debug**.

*Note*

*For details on using J-Link and connecting the board to the PC, see the Quick Start Guide included in the RA MCU Kit.*

## 2.2.10 Modifying Toolchain Settings

There are instances where it may be necessary to make changes to the toolchain being used (for example, to change optimization level of the compiler or add a library to the linker). Such modifications can be made from within e2 studio through the menu **Project > Properties > Settings** when the project is selected. The following screenshot shows the settings dialog for the GNU Arm toolchain. This dialog will look slightly different depending upon the toolchain being used.

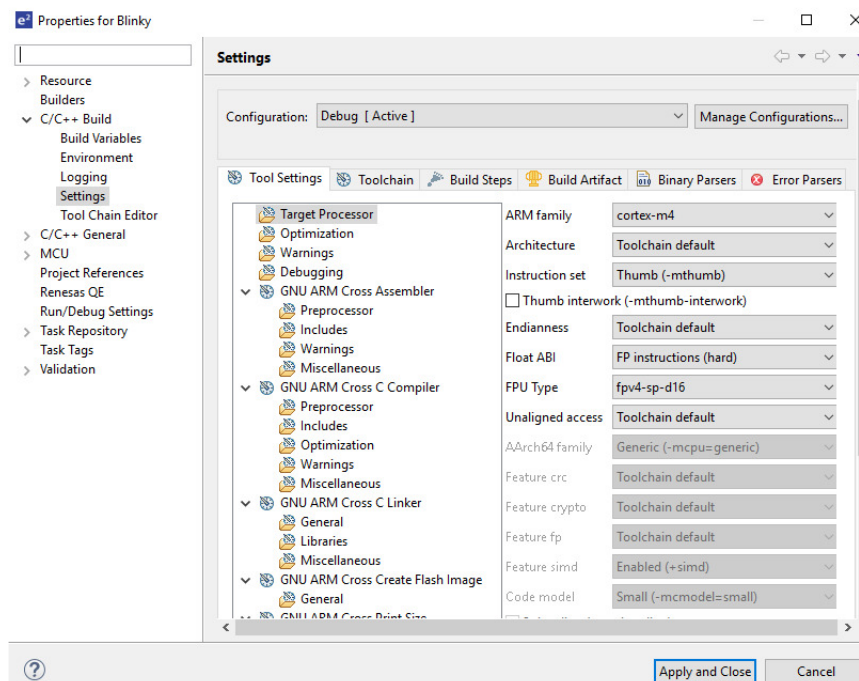


Figure 53: e2 studio Project toolchain settings

The scope for the settings is project scope which means that the settings are valid only for the project being modified.

The settings for the linker which control the location of the various memory sections are contained in a script file specific for the device being used. This script file is included in the project when it is created and is found in the script folder (for example, /script/a6m3.ld).

### 2.2.11 Creating RA project with ARM Compiler 6 in e2 studio

e2 studio does not include the ARM Compiler 6 (AC6) toolchain by default. Follow the steps below to integrate AC6 into e2 studio and create an AC6 RA project.

#### Note

*It is assumed that the user is already familiar with RA project creation in e2 studio. e2 studio does not include ARM Compiler 6 (AC6) toolchain by default.*

Steps 1 through 8 describe the process for integrating ARM Compiler 6 into e2 studio.

1. Download, install, and configure license for the AC6 toolchain (<https://developer.arm.com/tools-and-software/embedded/arm-compiler/downloads/version-6>).
2. Launch e2 studio.
3. Go to **Window > Preferences > Toolchains**.

4. Click **Add**.

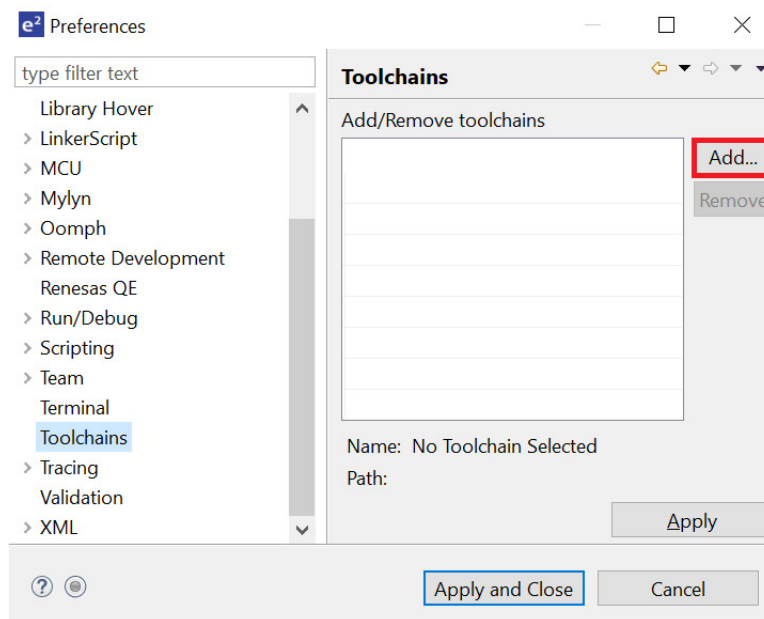


Figure 54: Add Toolchain

5. Browse to the path where AC6 toolchain is installed and select the \bin folder. Click **Next**.

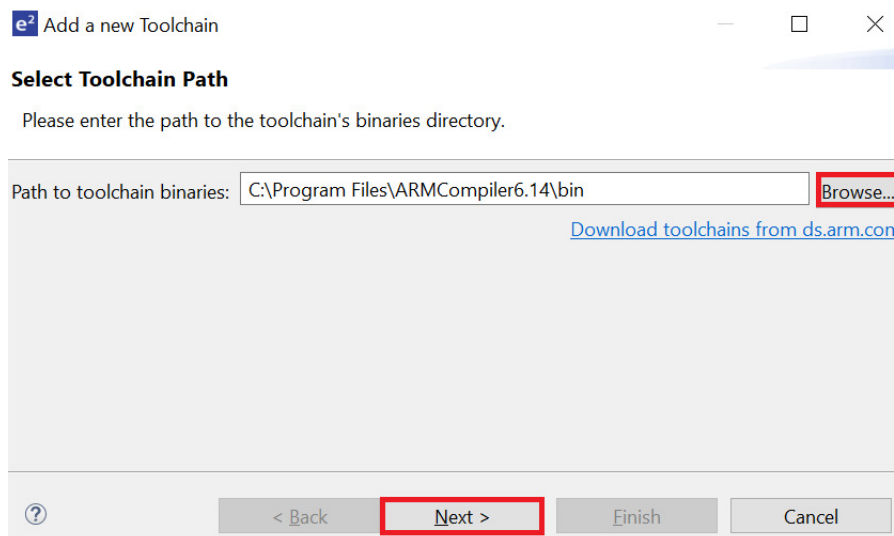


Figure 55: Browse to AC6 Compiler

6. Toolchain information is displayed. Click **Finish**.

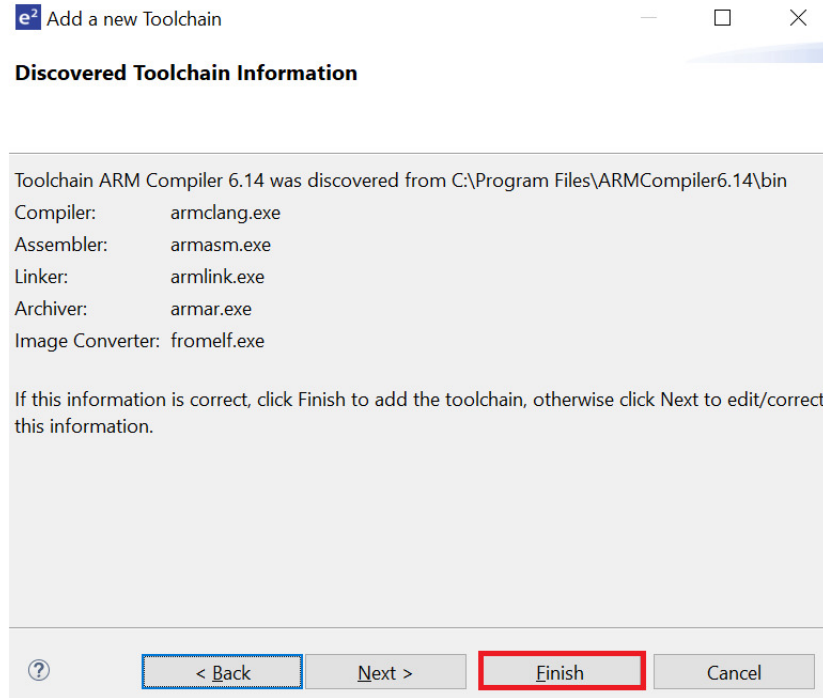


Figure 56: Toolchain Information

7. Click **Apply and Close**.

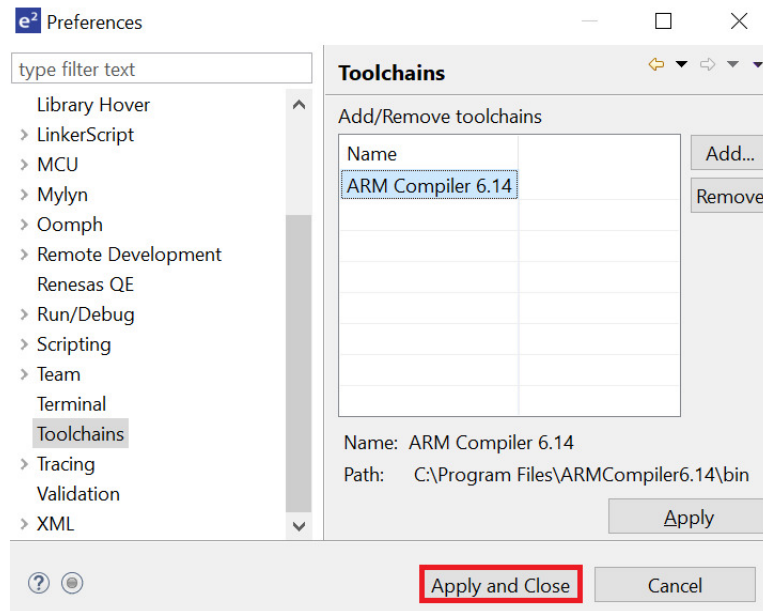


Figure 57: Apply and Close

8. Click **Restart Eclipse** when prompted.

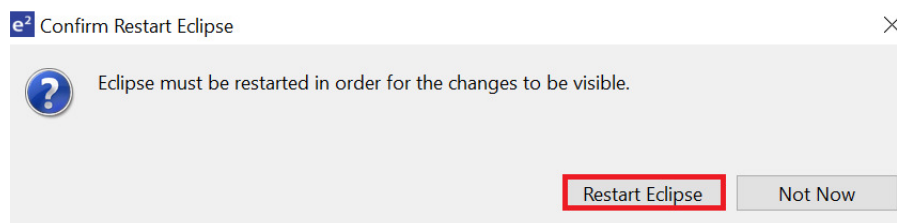


Figure 58: Restart Eclipse

9. When creating a new RA C/C++ project, select **ARM Compiler 6** included in the Toolchains section.

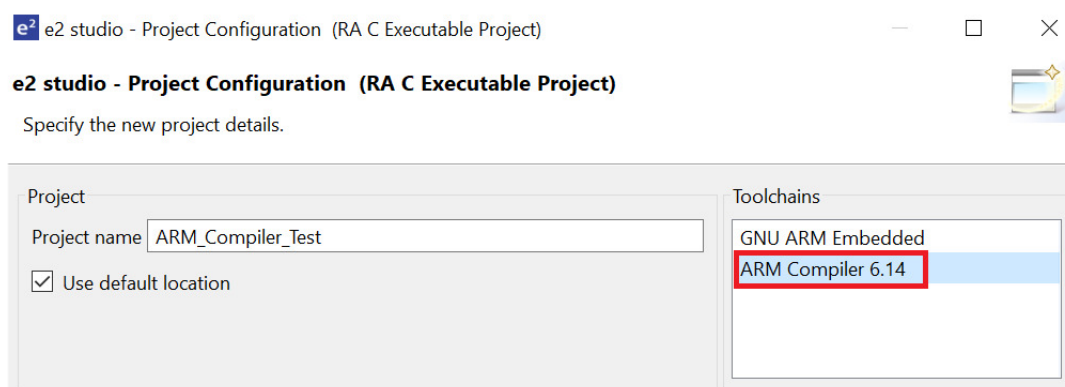


Figure 59: Select Arm Compiler

## 2.2.12 Importing an Existing Project into e2 studio

1. Start by opening e2 studio.
2. Open an existing Workspace to import the project and skip to step d. If the workspace doesn't exist, proceed with the following steps:
  - a. At the end of e2 studio startup, you will see the Workspace Launcher Dialog box as shown in the following figure.

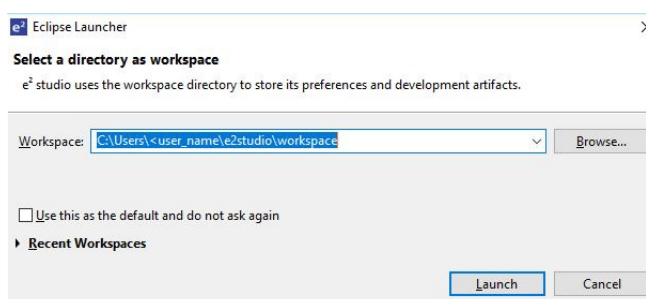


Figure 60: Workspace Launcher dialog



- b. Enter a new workspace name in the Workspace Launcher Dialog as shown in the following figure. e2 studio creates a new workspace with this name.

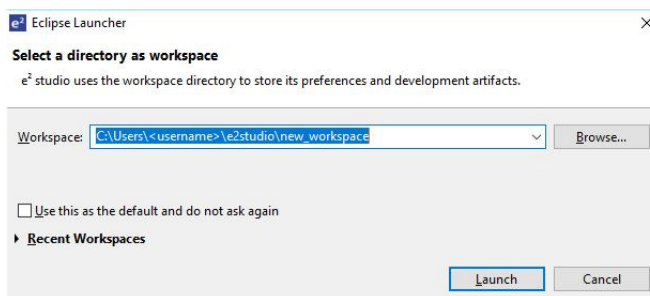


Figure 61: Workspace Launcher dialog - Select Workspace

- c. Click **Launch**.
- d. When the workspace is opened, you may see the Welcome Window. Click on the **Workbench** arrow button to proceed past the Welcome Screen as seen in the following figure.

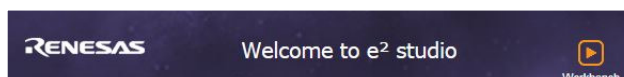


Figure 62: Workbench arrow button

3. You are now in the workspace that you want to import the project into. Click the **File** menu in the menu bar, as shown in the following figure.

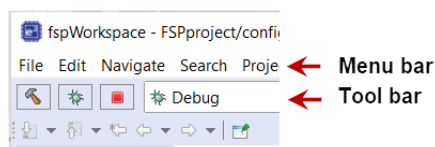


Figure 63: Menu and tool bar

4. Click **Import** on the **File** menu or in the menu bar, as shown in the following figure.

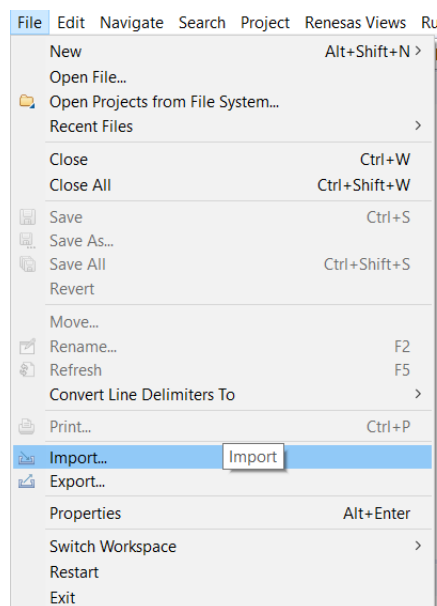


Figure 64: File drop-down menu

5. In the **Import** dialog box, as shown in the following figure, choose the **General** option, then **Existing Projects into Workspace**, to import the project into the current workspace.

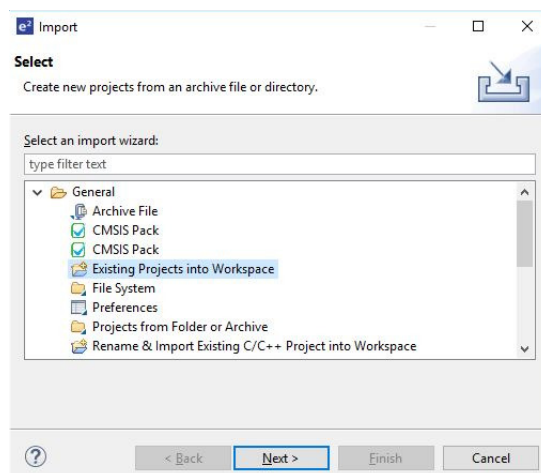


Figure 65: Project Import dialog with "Existing Projects into Workspace" option selected

6. Click **Next**.
7. To import the project, use either **Select archive file** or **Select root directory**.
  - a. Click **Select archive file** as shown in the following figure.

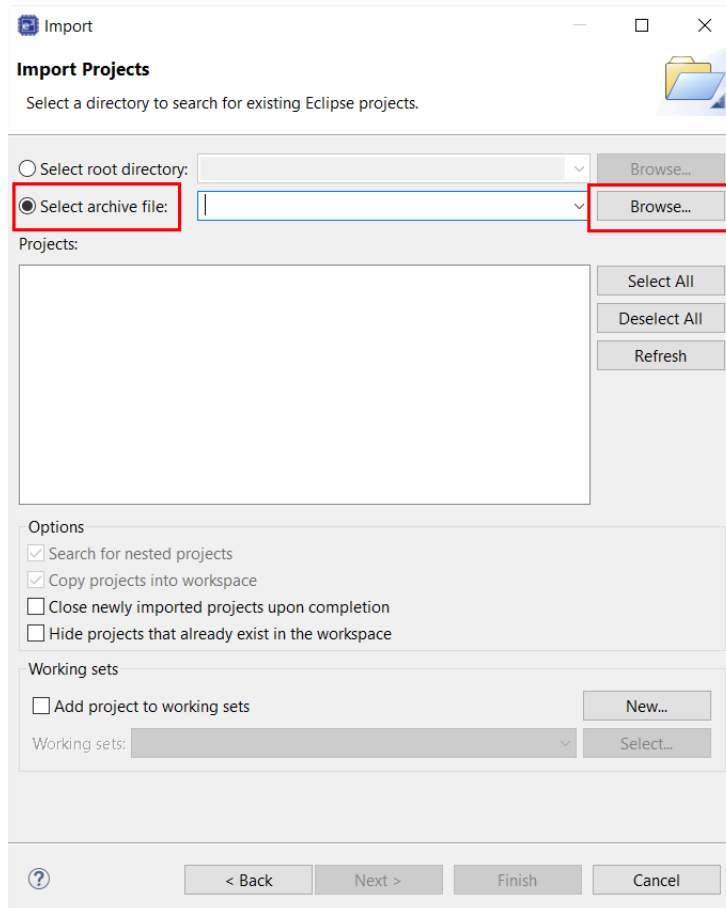


Figure 66: Import Existing Project dialog 1 - Select archive file

- b. Click **Select root directory** as shown in the following figure.

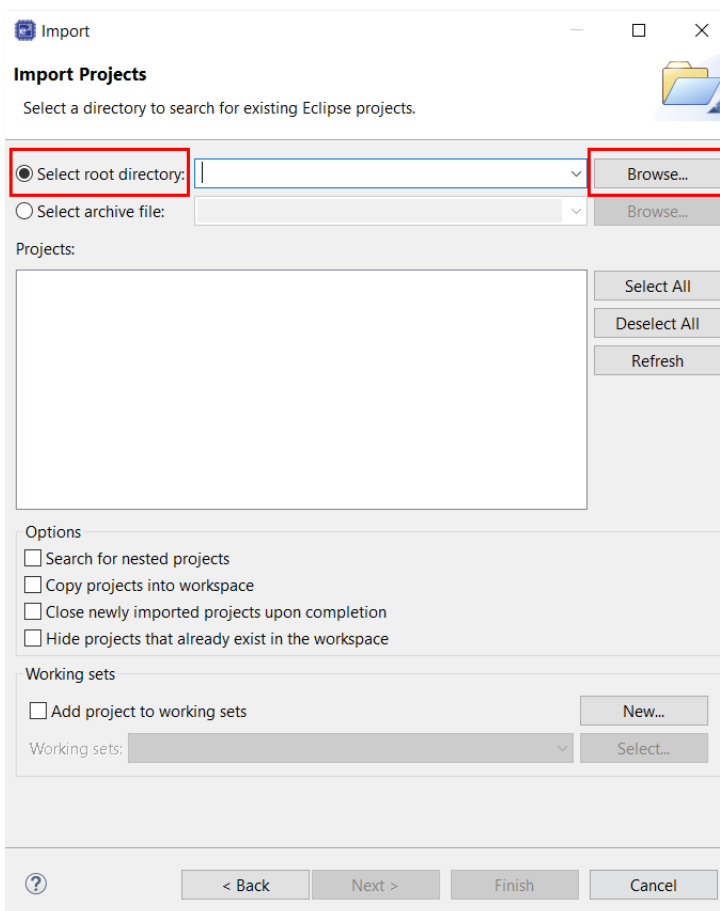


Figure 67: Import Existing Project dialog 1 - Select root directory

8. Click **Browse**.
9. For **Select archive file**, browse to the folder where the zip file for the project you want to import is located. For **Select root directory**, browse to the project folder that you want to import.
10. Select the file for import. In our example, it is CAN\_HAL\_MG\_AP.zip or CAN\_HAL\_MG\_AP.
11. Click **Open**.
12. Select the project to import from the list of **Projects**, as shown in the following figure.

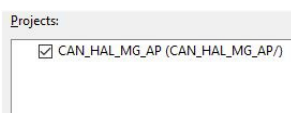


Figure 68: Import Existing Project dialog 2

13. Click **Finish** to import the project.

## 2.3 Tutorial: Your First RA MCU Project - Blinky

### 2.3.1 Tutorial Blinky

The goal of this tutorial is to quickly get acquainted with the Flexible Platform by moving through the

steps of creating a simple application using e2 studio and running that application on an RA MCU board.

## 2.3.2 What Does Blinky Do?

The application used in this tutorial is Blinky, traditionally the first program run in a new embedded development environment.

Blinky is the "Hello World" of microcontrollers. If the LED blinks you know that:

- The toolchain is setup correctly and builds a working executable image for your chip.
- The debugger has installed with working drivers and is properly connected to the board.
- The board is powered up and its jumper and switch settings are probably correct.
- The microcontroller is alive, the clocks are running, and the memory is initialized.

The Blinky example application used in this tutorial is designed to run the same way on all boards offered by Renesas that hold the RA microcontroller. The code in Blinky is completely board independent. It does the work by calling into the BSP (board support package) for the particular board it is running on. This works because:

- Every board has at least one LED connected to a GPIO pin.
- That one LED is always labelled LED1 on the silk screen.
- Every BSP supports an API that returns a list of LEDs on a board, and their port and pin assignments.

## 2.3.3 Prerequisites

To follow this tutorial, you need:

- Windows based PC
- e2 studio
- Flexible Software Package
- An RA MCU board kit

## 2.3.4 Create a New Project for Blinky

The creation and configuration of an RA MCU project is the first step in the creation of an application. The base RA MCU pack includes a pre-written Blinky example application that is simple and works on all Renesas RA MCU boards.

Follow these steps to create an RA MCU project:

1. In e2 studio, click **File > New > C/C++ Project** and select **Renesas RA** and **Renesas RA C/C++ Project**.
2. Assign a name to this new project. Blinky is a good name to use for this tutorial.
3. Click **Next**. The **Project Configuration** window shows your selection.

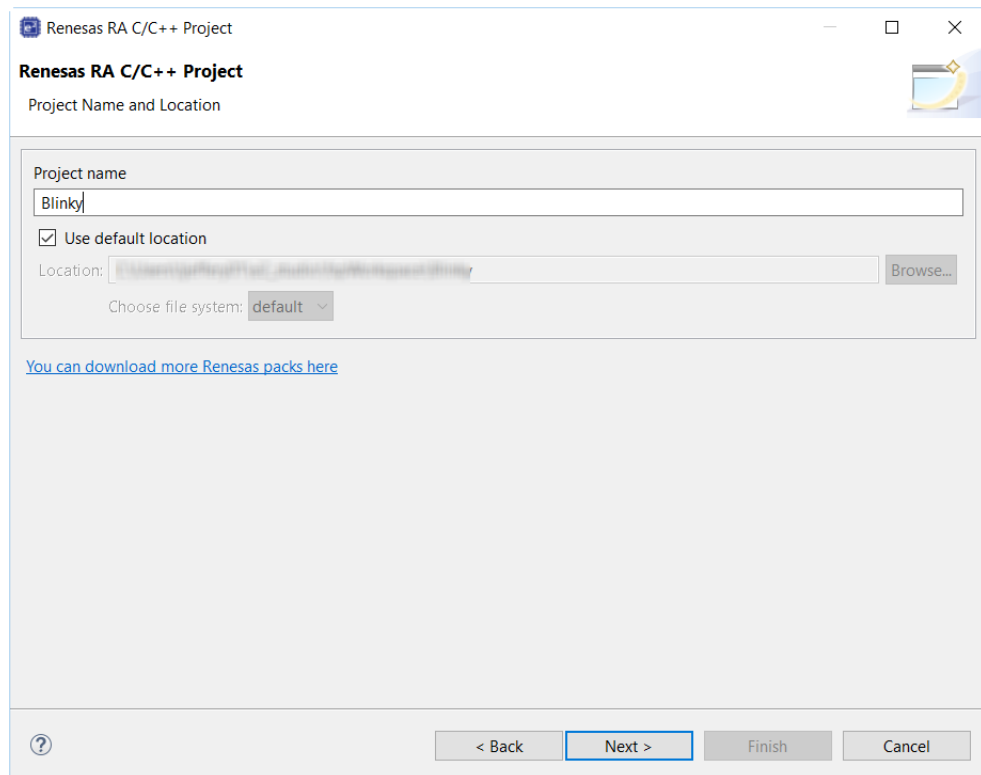


Figure 69: e2 studio Project Configuration window (part 1)

4. Select the board support package by selecting the name of your board from the **Device Selection** drop-down list and click **Next**.

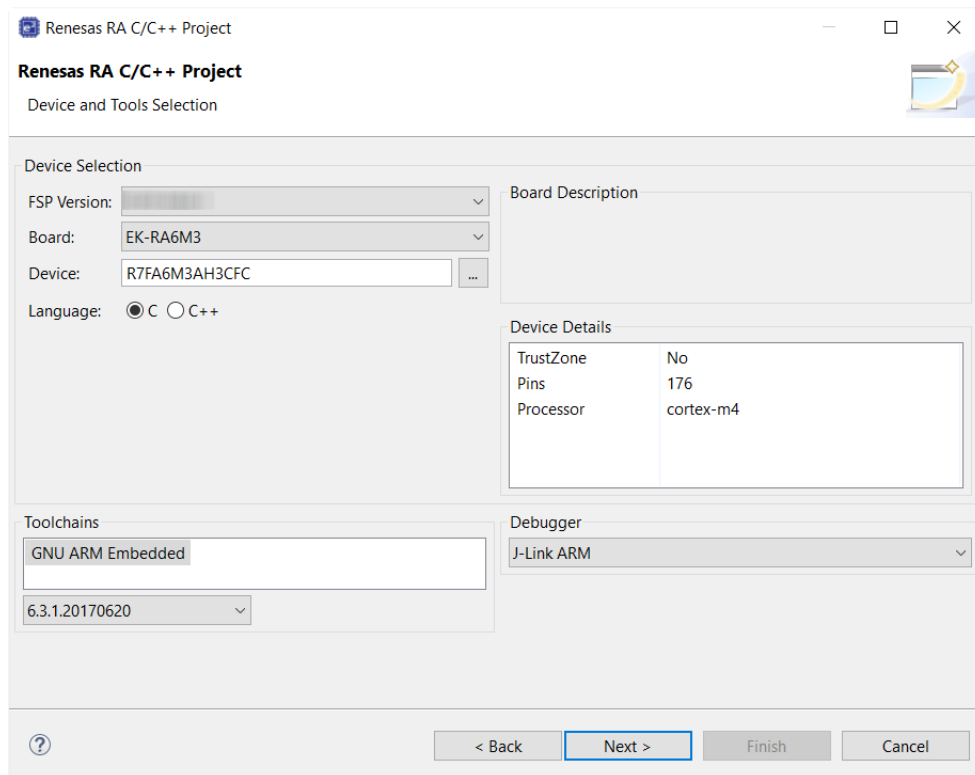


Figure 70: e2 studio Project Configuration window (part 2)

5. Select the build artifact and RTOS.

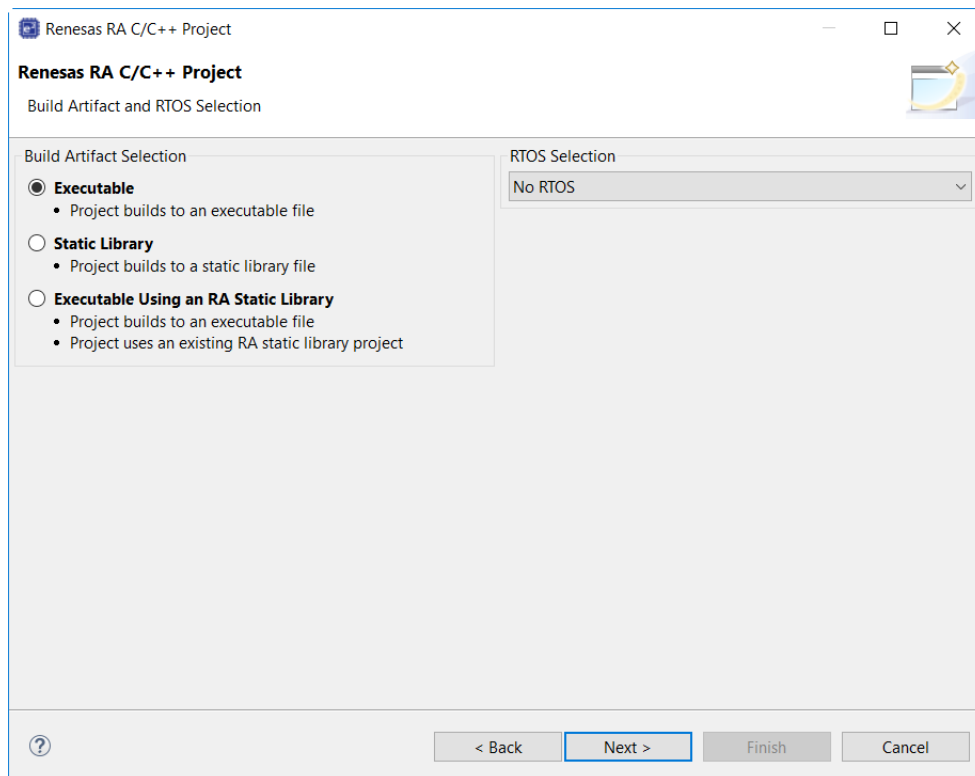


Figure 71: e2 studio Project Configuration window (part 3)

1. Select the Blinky template for your board and click **Finish**.

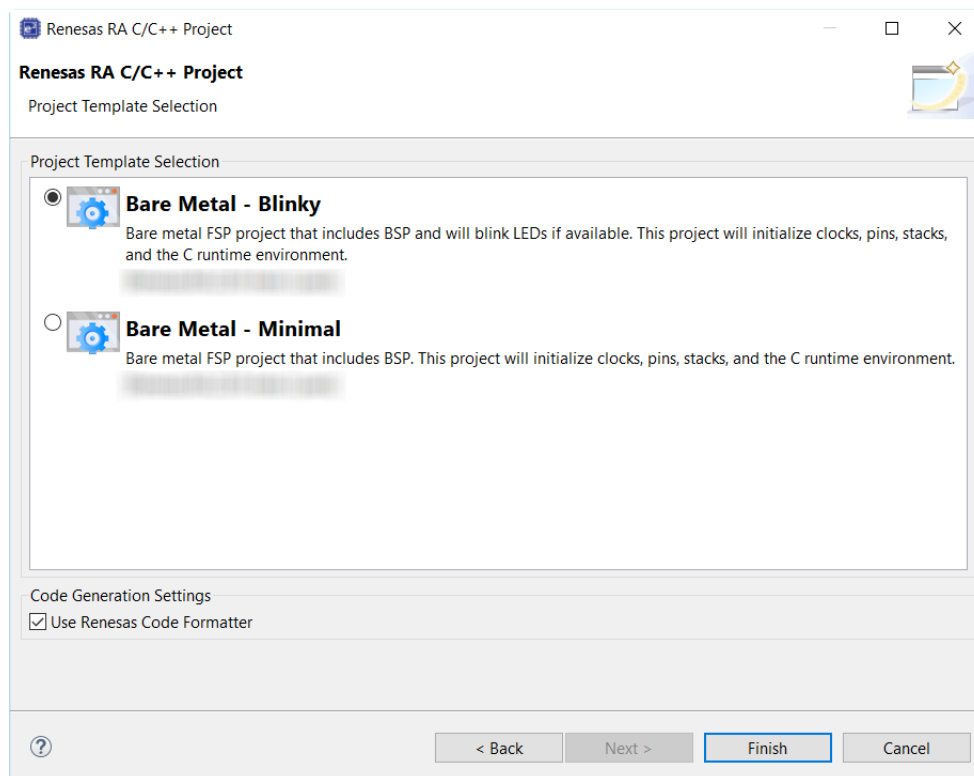


Figure 72: e2 studio Project Configuration window (part 4)

Once the project has been created, the name of the project will show up in the **Project Explorer** window of e2 studio. Now click the **Generate Project Content** button in the top right corner of the **Project Configuration** window to generate your board specific files.

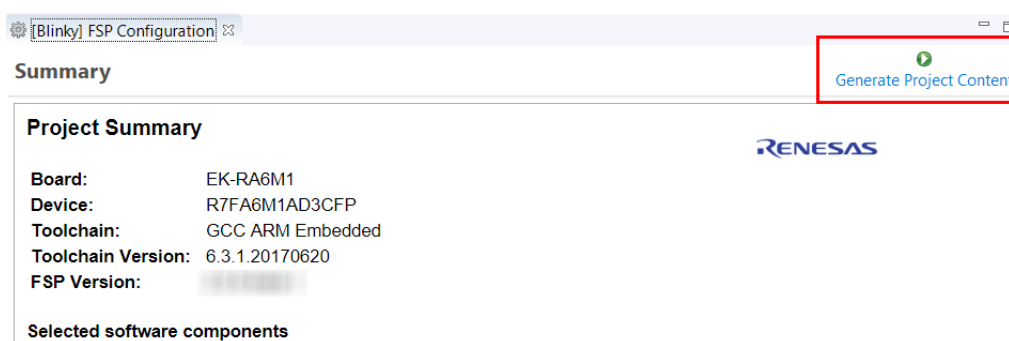


Figure 73: e2 studio Project Configuration tab

Your new project is now created, configured, and ready to build.

### 2.3.4.1 Details about the Blinky Configuration



The **Generate Project Content** button creates configuration header files, copies source files from templates, and generally configures the project based on the state of the **Project Configuration** screen.

For example, if you check a box next to a module in the **Components** tab and click the **Generate Project Content** button, all the files necessary for the inclusion of that module into the project will be copied or created. If that same check box is then unchecked those files will be deleted.

#### 2.3.4.2 Configuring the Blinky Clocks

By selecting the Blinky template, the clocks are configured by e2 studio for the Blinky application. The clock configuration tab (see [Configuring Clocks](#)) shows the Blinky clock configuration. The Blinky clock configuration is stored in the BSP clock configuration file (see [BSP Clock Configuration](#)).

#### 2.3.4.3 Configuring the Blinky Pins

By selecting the Blinky template, the GPIO pins used to toggle the LED1 are configured by e2 studio for the Blinky application. The pin configuration tab shows the pin configuration for the Blinky application (see [Configuring Pins](#)). The Blinky pin configuration is stored in the BSP configuration file (see [BSP Pin Configuration](#)).

#### 2.3.4.4 Configuring the Parameters for Blinky Components

The Blinky project automatically selects the following HAL components in the Components tab:

- r\_ioport

To see the configuration parameters for any of the components, check the **Properties** tab in the HAL window for the respective driver (see [Adding and Configuring HAL Drivers](#)).

#### 2.3.4.5 Where is main()?

The main function is located in < project >/ra\_gen/main.c. It is one of the files that are generated during the project creation stage and only contains a call to hal\_entry(). For more information on generated files, see [Adding and Configuring HAL Drivers](#).

#### 2.3.4.6 Blinky Example Code

The blinky application is stored in the hal\_entry.c file. This file is generated by e2 studio when you select the Blinky Project template and is located in the project's src/ folder.

The application performs the following steps:

1. Get the LED information for the selected board by bsp\_leds\_t structure.
2. Define the output level HIGH for the GPIO pins controlling the LEDs for the selected board.
3. Get the selected system clock speed and scale down the clock, so the LED toggling can be observed.
4. Toggle the LED by writing to the GPIO pin with R\_BSP\_PinWrite((bsp\_io\_port\_pin\_t) pin, pin\_level);

### 2.3.5 Build the Blinky Project

Highlight the new project in the **Project Explorer** window by clicking on it and build it.

There are three ways to build a project:

1. Click on **Project** in the menu bar and select **Build Project**.
2. Click on the hammer icon.
3. Right-click on the project and select **Build Project**.

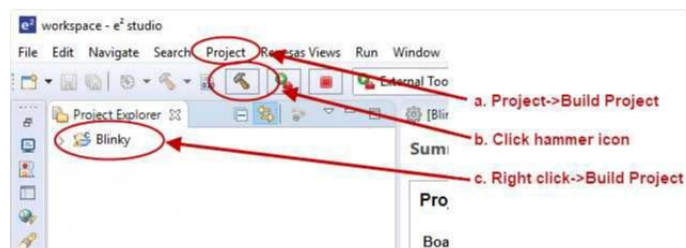


Figure 74: e2 studio Project Explorer window

Once the build is complete a message is displayed in the build **Console** window that displays the final image file name and section sizes in that image.

```

CDT Build Console [Blinky]
'Finished building: ../ra/board/ra6m3_ek/board_leds.c'
'Finished building: ../ra/board/ra6m3_ek/board_init.c'
'
'
'Finished building: ../ra/board/ra6m3_ek/board_qspi.c'
'Building target: Blinky.elf'
'Invoking: GNU ARM Cross C Linker'
arm-none-eabi-gcc @"Blinky.elf.in"
'Finished building target: Blinky.elf'
'
'Invoking: GNU ARM Cross Create Flash Image'
arm-none-eabi-objcopy -O srec "Blinky.elf" "Blinky.srec"
'Invoking: GNU ARM Cross Print Size'
arm-none-eabi-size --format=berkeley "Blinky.elf"
  text  data  bss   dec   hex filename
 4240   8   1152  5400  1518 Blinky.elf
'Finished building: Blinky.srec'
'Finished building: Blinky.siz'
'
'
11:50:45 Build Finished. 0 errors, 0 warnings. (took 19s.208ms)

```

Figure 75: e2 studio Project Build console

## 2.3.6 Debug the Blinky Project

### 2.3.6.1 Debug prerequisites

To debug the project on a board, you need

- The board to be connected to e2 studio
- The debugger to be configured to talk to the board
- The application to be programmed to the microcontroller

Applications run from the internal flash of your microcontroller. To run or debug the application, the application must first be programmed to the microcontroller's flash. There are two ways to do this:

- JTAG debugger
- Built-in boot-loader via UART or USB

Some boards have an on-board JTAG debugger and others require an external JTAG debugger connected to a header on the board.

Refer to your board's user manual to learn how to connect the JTAG debugger to e2 studio.

### 2.3.6.2 Debug steps

To debug the Blinky application, follow these steps:

1. Configure the debugger for your project by clicking **Run > Debugger Configurations ...**

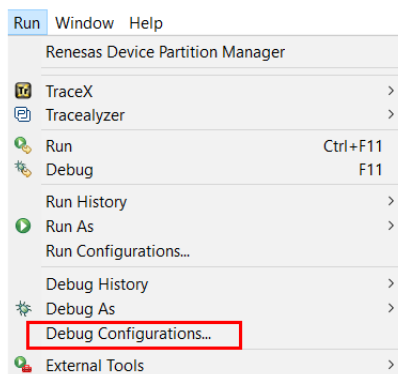


Figure 76: e2 studio Debug icon

or by selecting the drop-down menu next to the bug icon and selecting **Debugger Configurations ...**

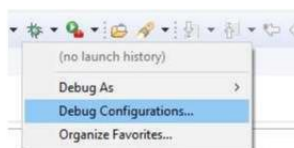


Figure 77: e2 studio Debugger Configurations selection option

2. Select your debugger configuration in the window. If it is not visible then it must be created by clicking the **New** icon in the top left corner of the window. Once selected, the **Debug Configuration** window displays the Debug configuration for your Blinky project.

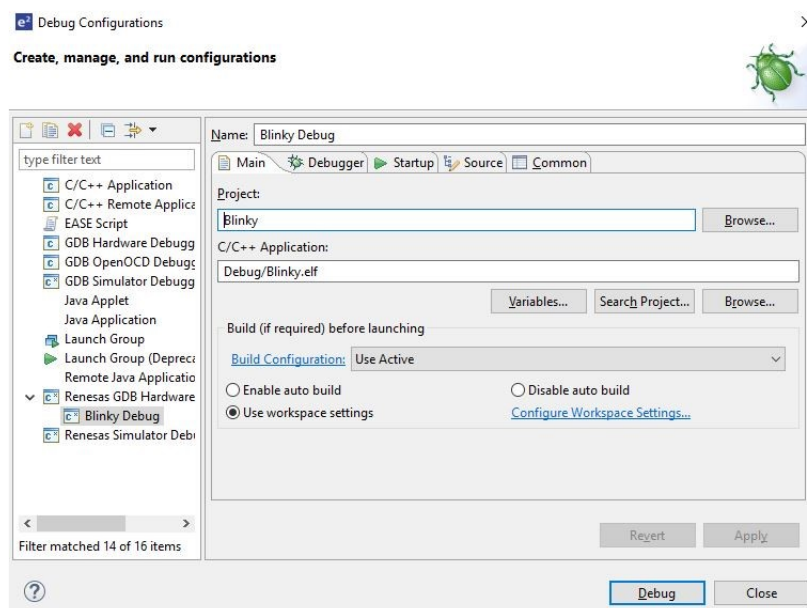
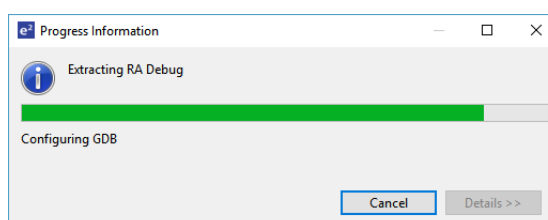


Figure 78: e2 studio Debugger Configurations window with Blinky project

3. Click **Debug** to begin debugging the application.

4. Extracting RA Debug.



### 2.3.6.3 Details about the Debug Process

In debug mode, e2 studio executes the following tasks:

1. Downloading the application image to the microcontroller and programming the image to the internal flash memory.
2. Setting a breakpoint at main().
3. Setting the stack pointer register to the stack.
4. Loading the program counter register with the address of the reset vector.
5. Displaying the startup code where the program counter points to.

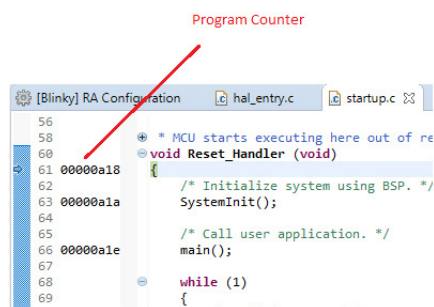


Figure 79: e2 studio Debugger memory window

## 2.3.7 Run the Blinky Project

While in Debug mode, click **Run > Resume** or click on the **Play** icon twice.



Figure 80: e2 studio Debugger Play icon

The LEDs on the board marked LED1, LED2, and LED3 should now be blinking.

## 2.4 Tutorial: Using HAL Drivers - Programming the WDT

### 2.4.1 Application WDT

This tutorial illustrates the creation of a simple application that uses the Watchdog Timer module to monitor program operation. The tutorial shows each step in the development process and in particular identifies the auto-generated files and project structure created when using FSP and its GUI based configurator. The level of detail provided here is more than is normally needed during development but can be helpful in explaining how FSP works behind the scenes to simplify your work.

This application makes use of the following FSP modules:

- [MCU Board Support Package](#)
- [Watchdog Timer \(r\\_wdt\)](#)
- [I/O Ports \(r\\_ioport\)](#)

### 2.4.2 Creating a WDT Application Using the RA MCU FSP and e2 studio

#### 2.4.2.1 Using the FSP and e2 studio

The Flexible Software Package (FSP) from Renesas provides a complete driver library for developing RA MCU applications. The FSP provides Hardware Abstraction Layer (HAL) drivers, Board Support Package (BSP) drivers for the developer to use to create applications. The FSP is integrated into Renesas e2 studio based on eclipse providing build (editor, compiler and linker) and debug phases with an extended GNU Debug (GDB) interface.

#### 2.4.2.2 The WDT Application

The flowchart for the WDT application is shown below.

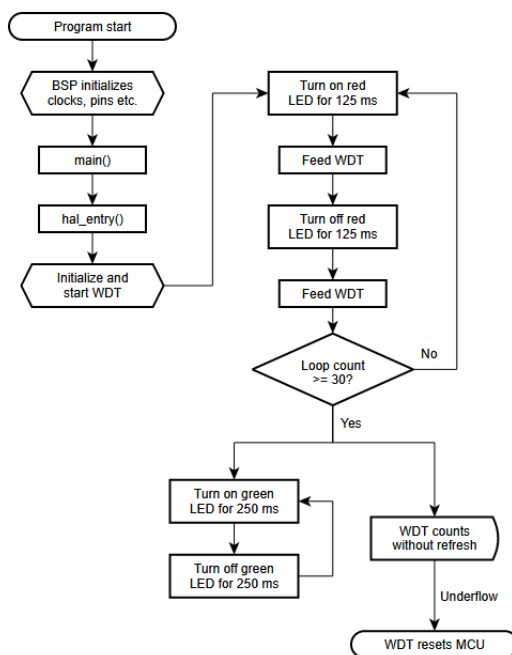


Figure 81: WDT Application flow diagram

### 2.4.2.3 WDT Application flow

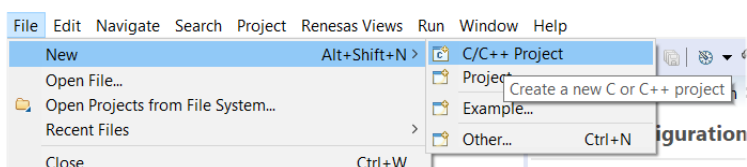
The main sections of the WDT application are:

1. The BSP initializes the clocks, pins and other elements of the MCU readying the application to run.
2. main() calls hal\_entry(). The function hal\_entry() is created by the FSP with a placeholder for user code. The code for the WDT is added to this function.
3. Initialize the WDT, but do not start it.
4. Start the WDT by refreshing it.
5. In the first loop the red LED flashes 30 times and refreshes the watchdog each time the LED state is changed.
6. In the second loop, the green LED flashes, but the program DOES NOT refresh the watchdog. After the watchdog timeout period the device will reset which can be observed by the red LED flashing again as the sequence repeats.

### 2.4.3 Creating the Project with e2 studio

Start e2 studio and choose a workspace folder in the Workspace Launcher. Configure a new RA MCU project as follows.

1. Select **File > New > RA C/C++ Project**. Then select the template for the project.



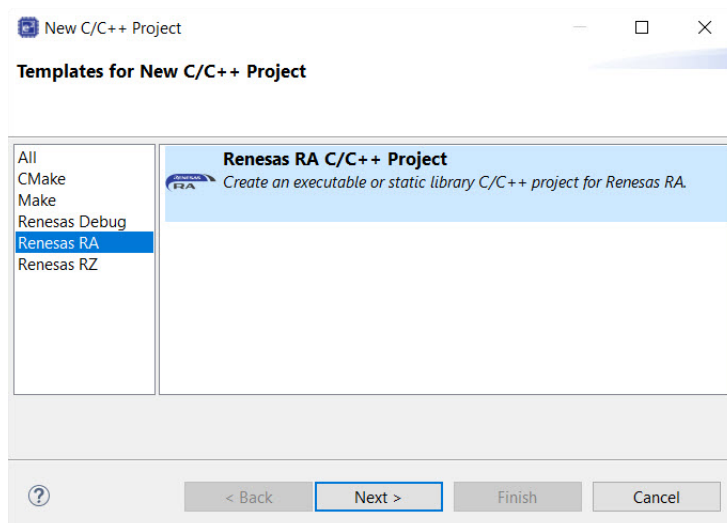


Figure 82: Creating a new project

2. In the e2 studio Project **Configuration (RA Project)** window enter a project name, for example, WDT\_Application. In addition, select the toolchain. If you want to choose new locations for the project unselect **Use default location**. Click **Next**.

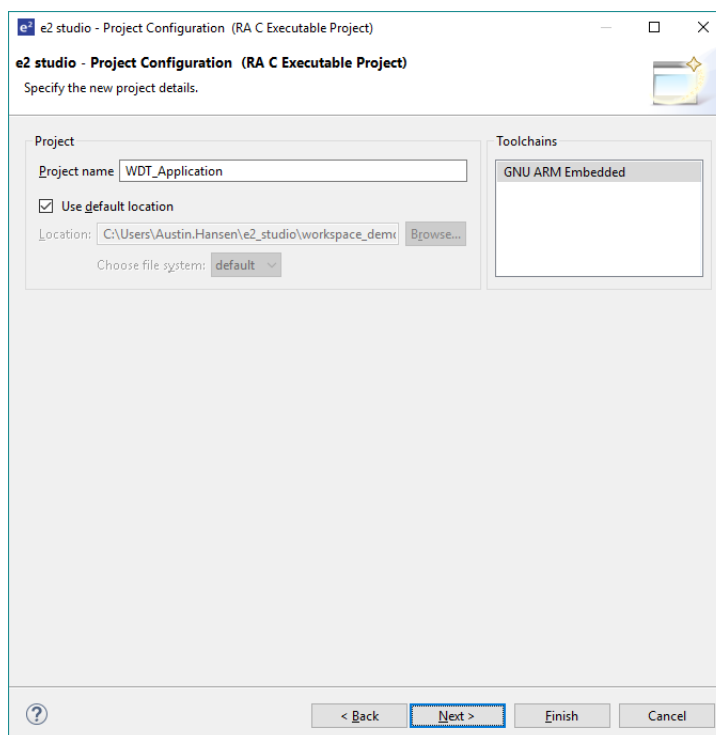


Figure 83: Project configuration (part 1)

3. This application runs on the EK-RA6M3 board. So, for the **Board** select **EK-RA6M3**.

This will automatically populate the **Device** drop-down with the correct device used on this board. Select the **Toolchain** version. Select **J-Link ARM** as the **Debugger**. Click **Next** to configure the project.

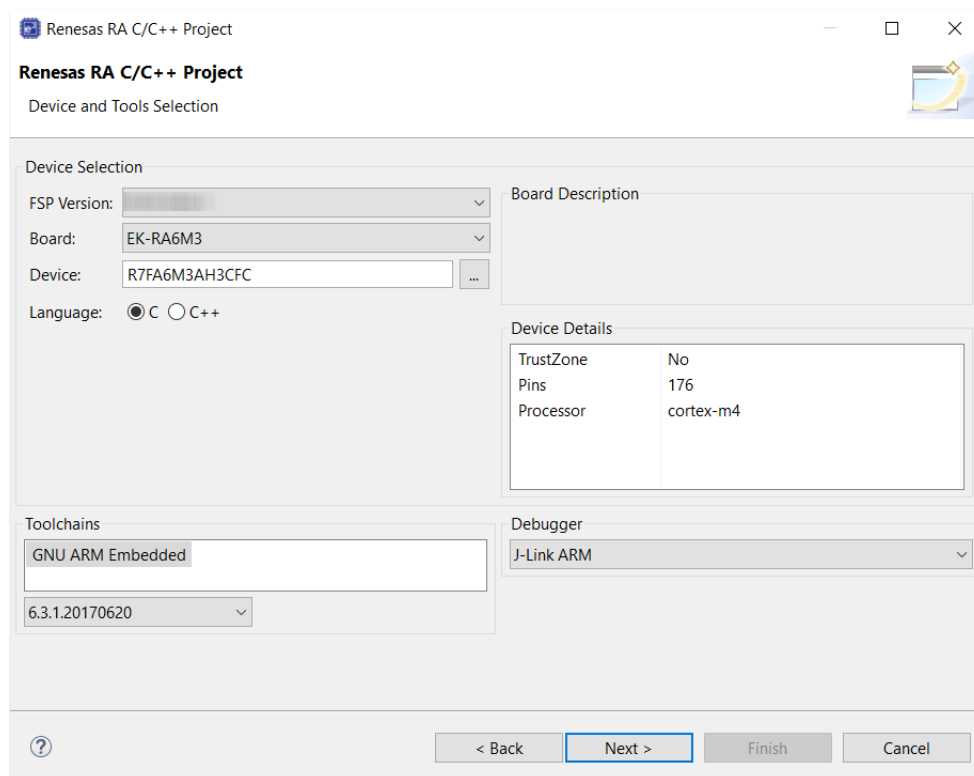


Figure 84: Project configuration (part 2)

The project template is now selected. As no RTOS is required select **Bare Metal - Blinky**.



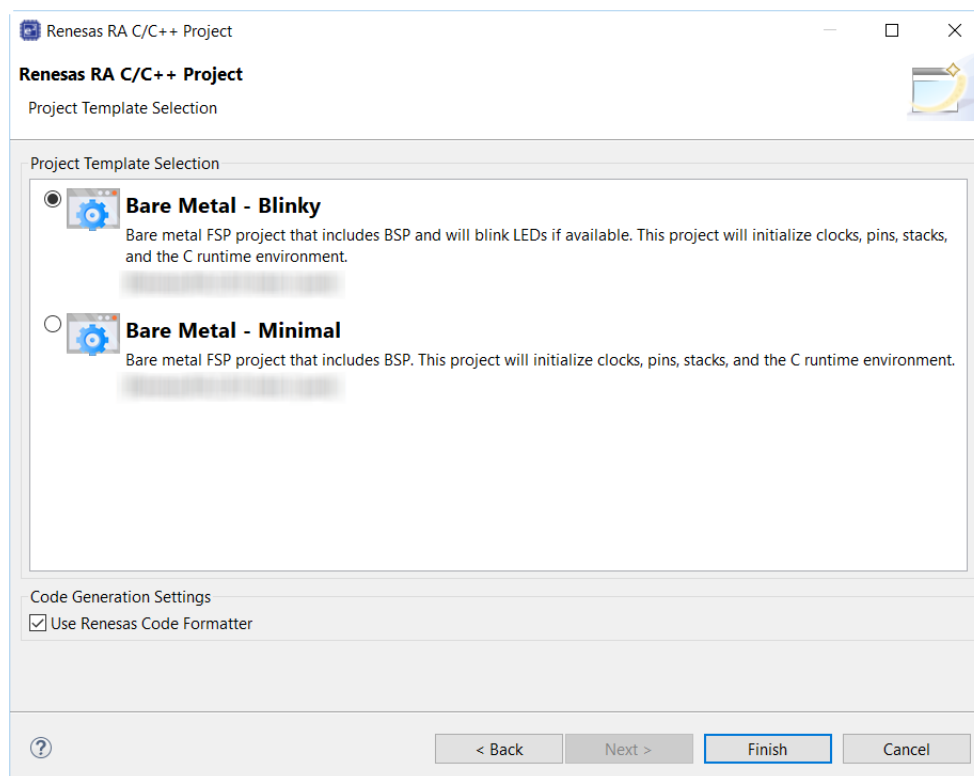


Figure 85: Project configuration (part 3)

#### 4. Click **Finish**.

e2 studio creates the project and opens the **Project Explorer** and **Project Configuration Settings** views with the **Summary** page showing a summary of the project configuration.

### 2.4.4 Configuring the Project with e2 studio

e2 studio simplifies and accelerates the project configuration process by providing a GUI interface for selecting the options to configure the project.

e2 studio offers a selection of perspectives presenting different windows to the user depending on the operation in progress. The default perspectives are **C/C++**, **FSP Configuration** and **Debug**. The perspective can be changed by selecting a new one from the buttons at the top right.

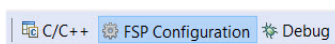


Figure 86: Selecting a perspective

The **C/C++** perspective provides a layout selected for code editing. The **FSP Configuration** perspective provides elements for configuring a RA MCU project, and the **Debug** perspective provides a view suited for debugging.

1. In order to configure the project settings ensure the **FSP Configuration** perspective is selected.

2. Ensure the **Project Configuration [WDT Application]** is open. It is already open if the Summary information is visible. To open the Project Configuration now or at any time make sure the **RA Configuration** perspective is selected and double-click on the configuration.xml file in the Project Explorer pane on the right side of e2 studio.

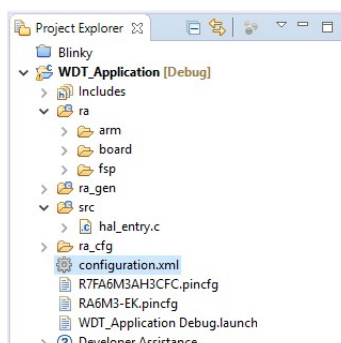


Figure 87: RA MCU Project Configuration Settings

At the base of the Project Configuration view there are several tabs for configuring the project. A project may require changes to some or all of these tabs. The tabs are shown below.

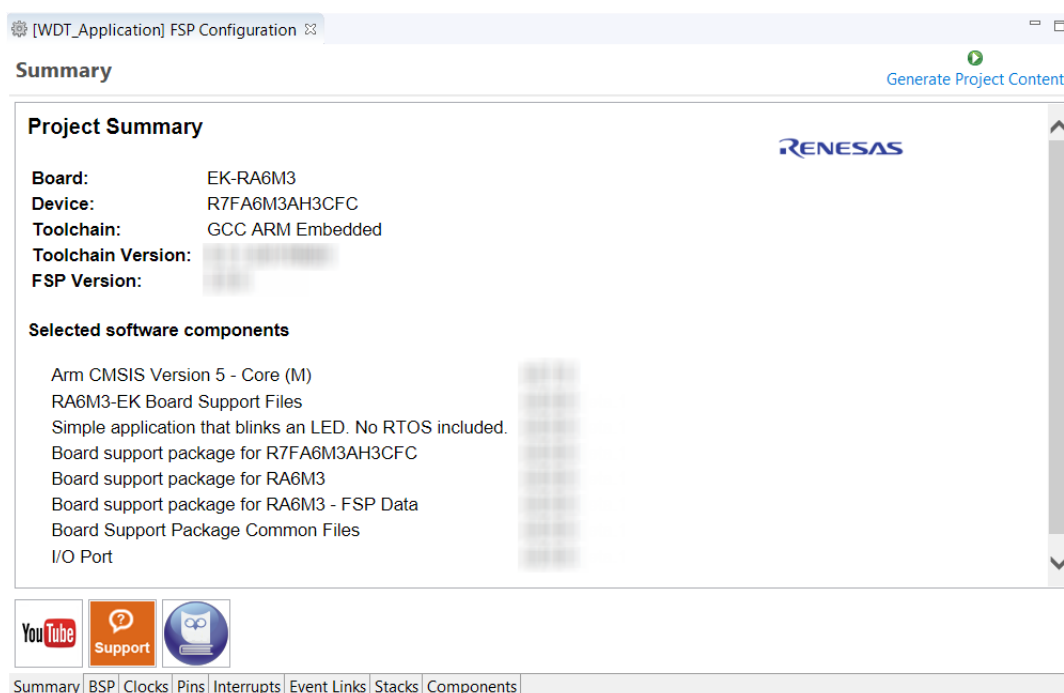


Figure 88: Project Configuration Tabs

#### 2.4.4.1 BSP Tab

The **BSP** tab allows the Board Support Package (BSP) options to be modified from their defaults. For this particular WDT project no changes are required. However, if you want to use the WDT in auto-start mode, you can configure the settings of the OFS0 (Option Function Select Register 0) register in the **BSP** tab. See the RA Hardware User's Manual for details on the WDT autostart mode.

#### 2.4.4.2 Clocks Tab

The **Clocks** tab presents a graphical view of the clock tree of the device. The drop-down boxes in the GUI enables configuration of the various clocks. The WDT uses PCLKB. The default output frequency for this clock is 60 MHz. Ensure this clock is outputting this value.

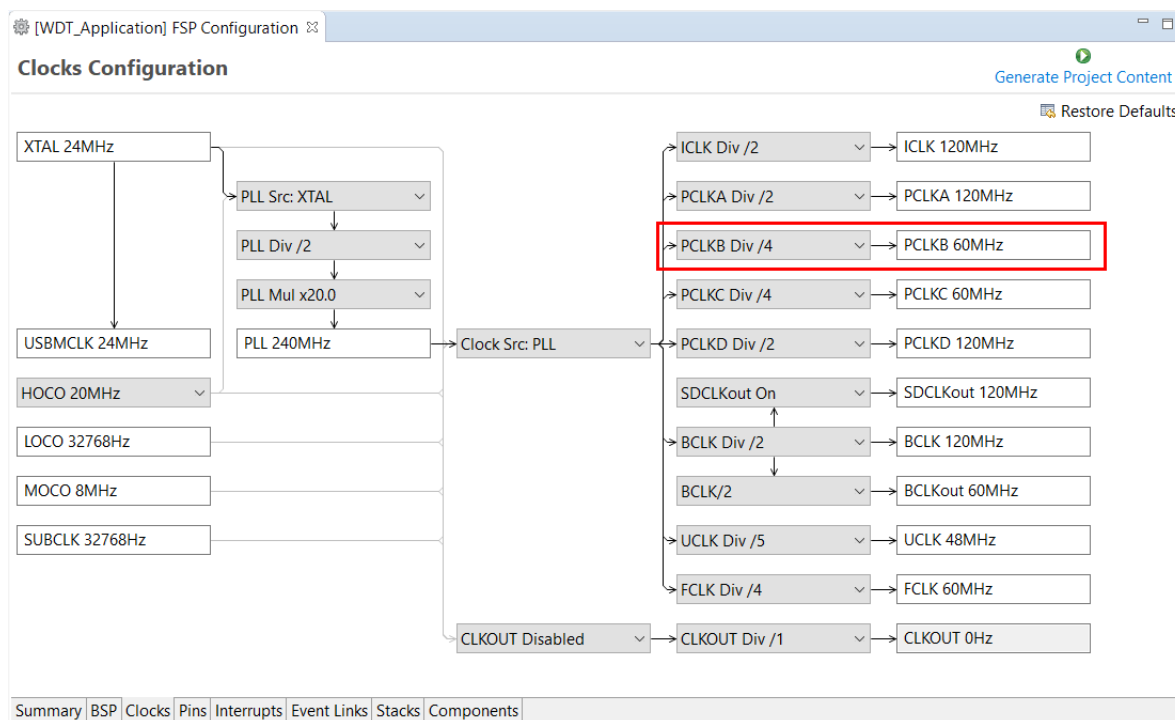


Figure 89: Clock configuration

### 2.4.4.3 Interrupts Tab

The **Interrupts** tab is used to add new user events or interrupts. No new interrupts or events are needed by the application, so no edits in this tab are required.

### 2.4.4.4 Event Links Tab

The **Event Links** tab is used to configure events used by the Event Link Controller (ELC). This project doesn't use the ELC, so no edits in this tab are required.

### 2.4.4.5 Pins Tab

The **Pins** tab provides a graphical tool for configuring the functionality of the pins of the device. For the WDT project no pin configuration is required. Although the project uses two LEDs connected to pins on the device, these pins are pre-configured as output GPIO pins by the BSP.

### 2.4.4.6 Stacks Tab

You can add any driver to the project using the **Stacks** tab. The HAL driver IO port pins are added automatically by e2 studio when the project is configured. The WDT application uses no RTOS Resources, so you only need to add the HAL WDT driver.

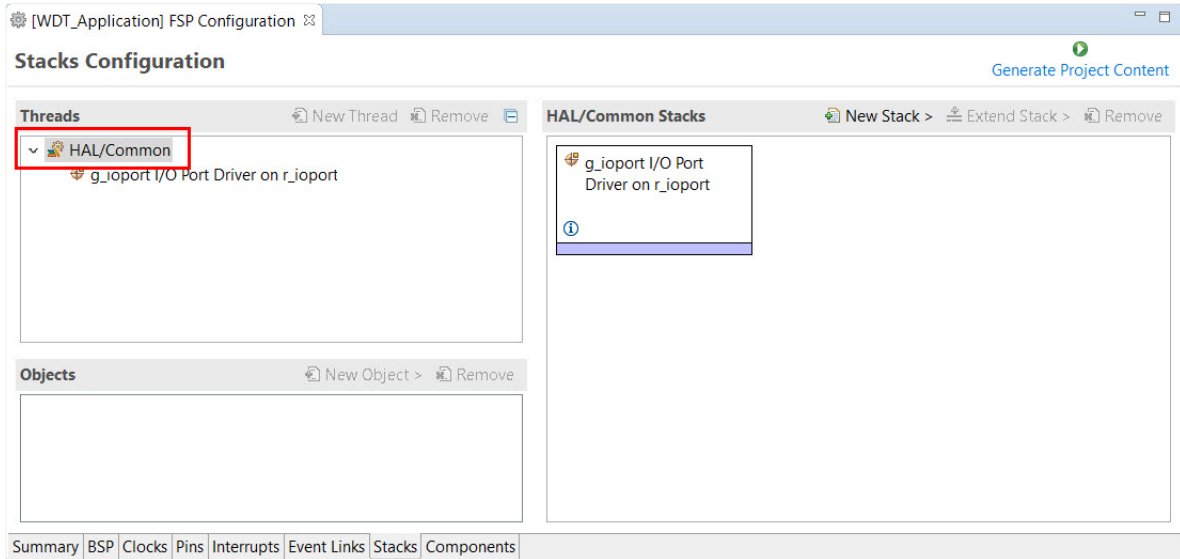


Figure 90: Stacks tab

1. Click on the **HAL/Common Panel** in the Threads Window as indicated in the figure above.

The Stacks Panel becomes a **HAL/Common Stacks** panel and is populated with the modules preselected by e2 studio.

2. Click on **New Stack** to find a pop-up window with the available HAL level drivers.
3. Select **WATCHDOG Driver on r\_wdt**.

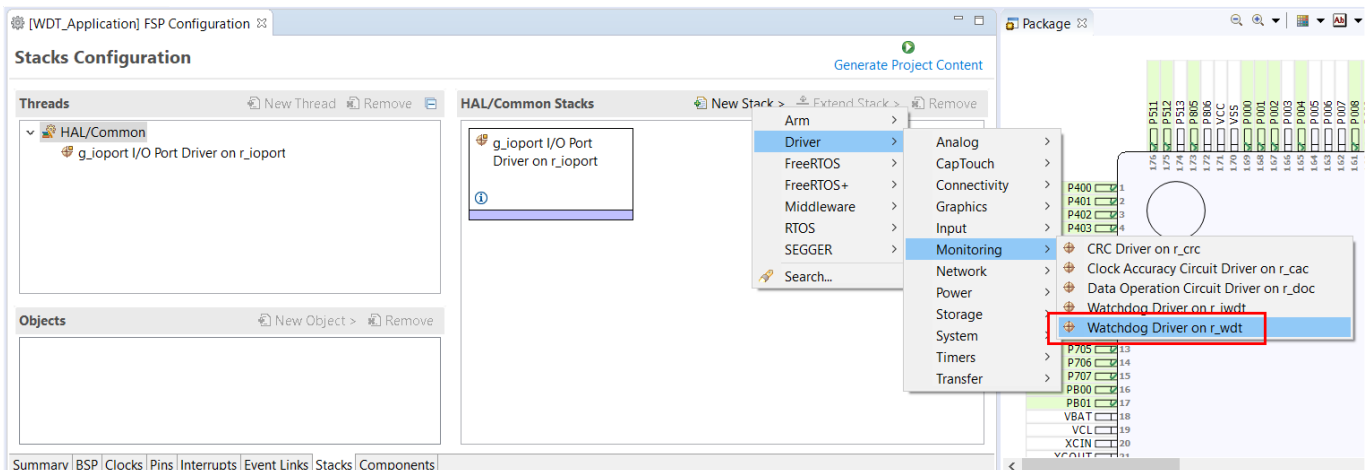
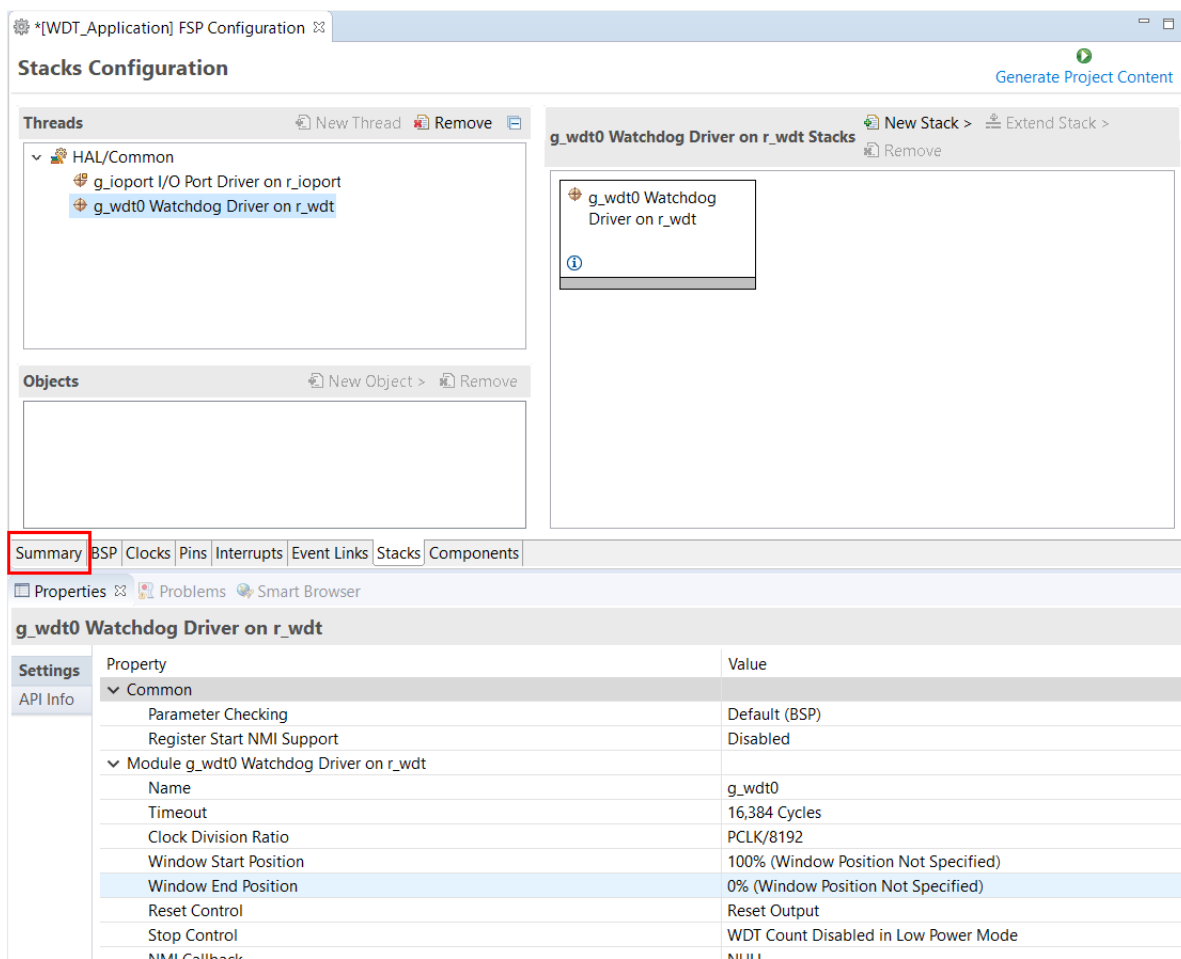


Figure 91: Module Selection

The selected HAL WDT driver is added to the **HAL/Common Stacks** Panel and the **Property** Window shows all configuration options for the selected module. The **Property** tab for the WDT should be visible at the bottom left of the screen. If it is not visible, check that the **FSP Configuration** perspective is selected.

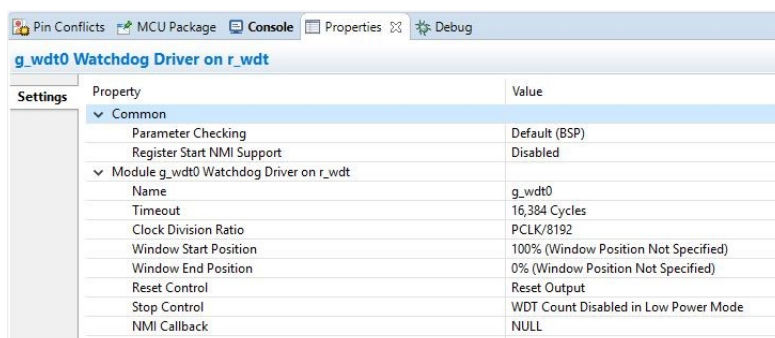


The screenshot shows the 'Stacks Configuration' window in the IDE. The 'Summary' tab is selected, displaying the configuration for the 'g\_wdt0 Watchdog Driver on r\_wdt' module. The configuration is presented as a table with columns for 'Property' and 'Value'.

Property	Value
Common	
Parameter Checking	Default (BSP)
Register Start NMI Support	Disabled
Module g_wdt0 Watchdog Driver on r_wdt	
Name	g_wdt0
Timeout	16,384 Cycles
Clock Division Ratio	PCLK/8192
Window Start Position	100% (Window Position Not Specified)
Window End Position	0% (Window Position Not Specified)
Reset Control	Reset Output
Stop Control	WDT Count Disabled in Low Power Mode
NMI Callback	NULL

Figure 92: Module Properties

All parameters can be left with their default values.



The screenshot shows the 'Properties' window in the IDE, displaying the configuration for the 'g\_wdt0 Watchdog Driver on r\_wdt' module. The configuration is presented as a table with columns for 'Property' and 'Value'.

Property	Value
Common	
Parameter Checking	Default (BSP)
Register Start NMI Support	Disabled
Module g_wdt0 Watchdog Driver on r_wdt	
Name	g_wdt0
Timeout	16,384 Cycles
Clock Division Ratio	PCLK/8192
Window Start Position	100% (Window Position Not Specified)
Window End Position	0% (Window Position Not Specified)
Reset Control	Reset Output
Stop Control	WDT Count Disabled in Low Power Mode
NMI Callback	NULL

Figure 93: g\_wdt WATCHDOG Driver on WDT properties

With PCLKB running at 60 MHz the WDT will reset the device 2.23 seconds after the last refresh.

$$\text{WDT clock} = 60 \text{ MHz} / 8192 = 7.32 \text{ kHz}$$

$$\text{Cycle time} = 1 / 7.324 \text{ kHz} = 136.53 \text{ us}$$

Timeout =  $136.53 \text{ us} \times 16384 = 2.23 \text{ seconds}$

Save the **Project Configuration** file and click the **Generate Project Content** button in the top right corner of the **Project Configuration** pane.

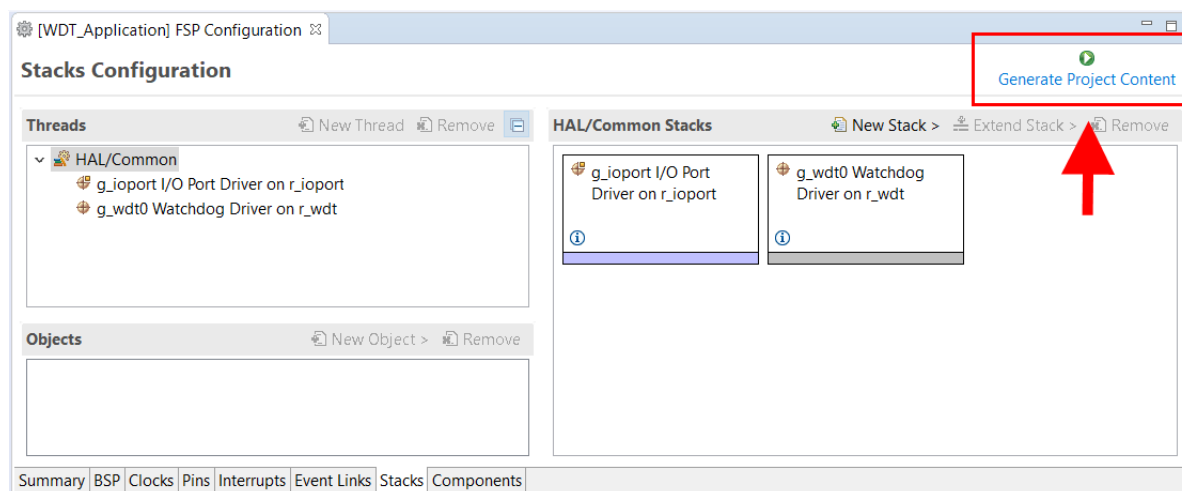


Figure 94: Generate Project Content button

e2 studio generates the project files.

#### 2.4.4.7 Components Tab

The components tab is included for reference to see which modules are included in the project. Modules are selected automatically in the Components view after they are added in the Stacks Tab.

For the WDT project ensure that the following modules are selected:

1. HAL\_Drivers -> r\_ioport
2. HAL\_Drivers -> r\_wdt

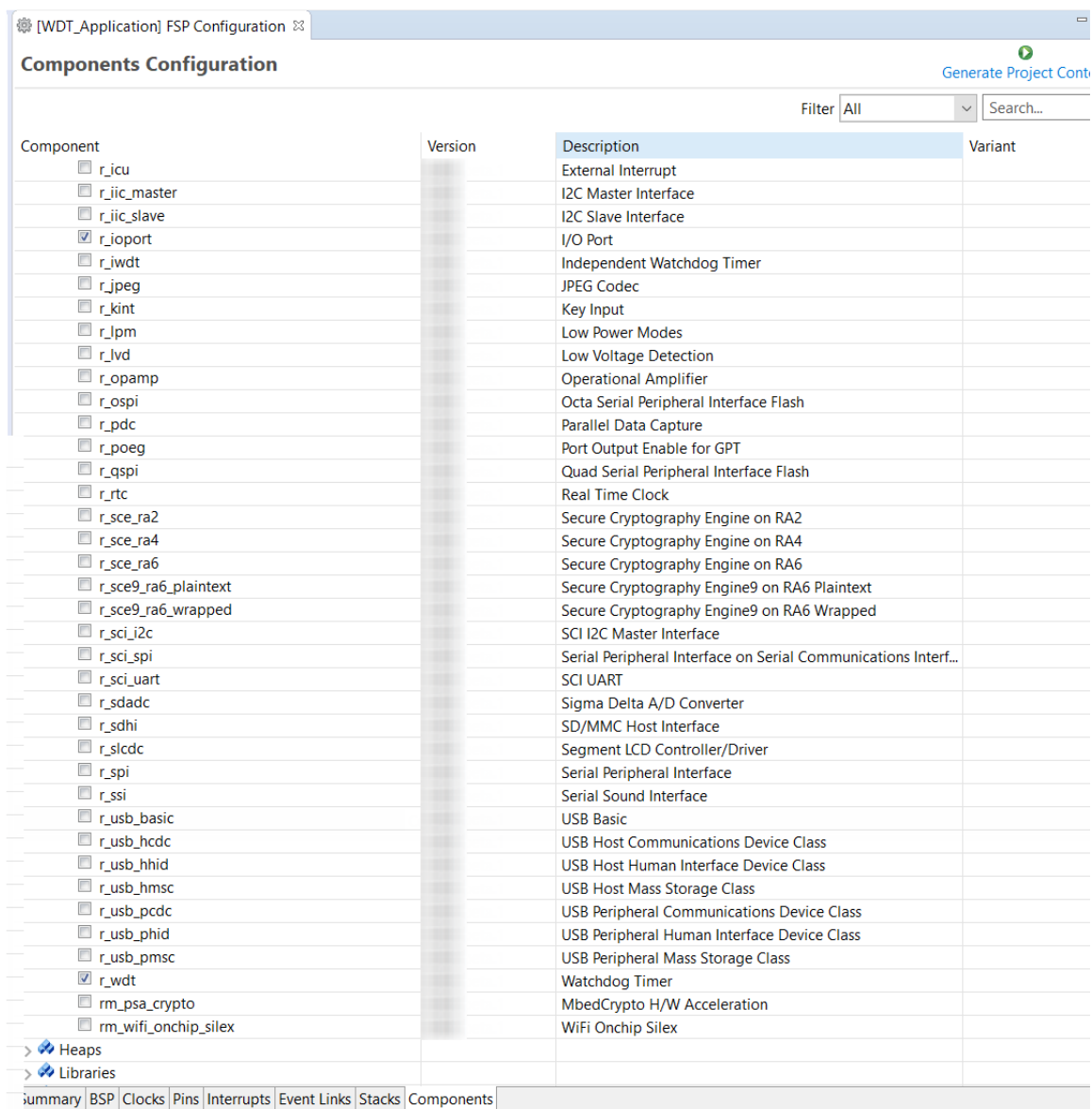


Figure 95: Component Selection

*Note*

The list of modules displayed in the Components tab depends on the installed FSP version.

## 2.4.5 WDT Generated Project Files

Clicking the Generate Project Content button performs the following tasks.

- r\_wdt folder and WDT driver contents created at:

ra/fsp/src

- r\_wdt\_api.h created in:

ra/fsp/inc/api

- r\_wdt.h created in:

ra/fsp/inc/instances

The above files are the standard files for the WDT HAL module. They contain no specific project contents. They are the driver files for the WDT. Further information on the contents of these files can be found in the documentation for the WDT HAL module.

Configuration information for the WDT HAL module in the WDT project is found in:

ra\_cfg/fsp\_cfg/r\_wdt\_cfg.h

The above file's contents are based upon the **Common** settings in the **g\_wdt WATCHDOG Driver on WDT Properties** pane.

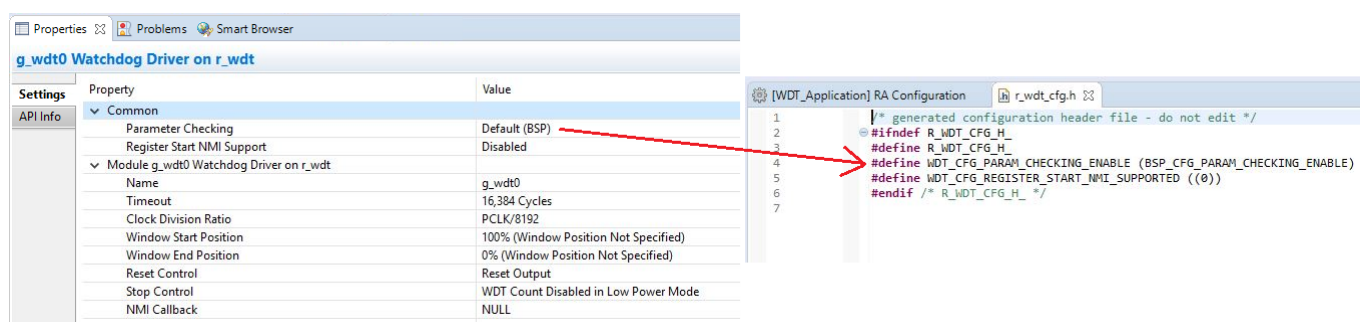


Figure 96: r\_wdt\_cfg.h contents

## Warning

Do not edit any of these files as they are recreated every time the Generate Project Content button is clicked and so any changes will be overwritten.

The r\_ioport folder is not created at ra/fsp/src as this module is required by the BSP and so already exists. It is included in the WDT project in order to include the correct header file in ra\_gen/hal\_data.c—see later in this document for further details. For the same reason the other IOPORT header files— ra/fsp/inc/api/r\_ioport\_api.h and ra/fsp/inc/instances/r\_ioport.h—are not created as they already exist.

In addition to generating the HAL driver files for the WDT and IOPORT files e2 studio also generates files containing configuration data for the WDT and a file where user code can safely be added. These files are shown below.



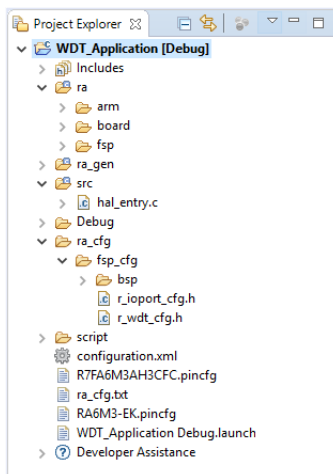


Figure 97: WDT project files

### 2.4.5.1 WDT hal\_data.h

The contents of hal\_data.h are shown below.

```
/* generated HAL header file - do not edit */  
#ifndef HAL_DATA_H_  
#define HAL_DATA_H_  
#include <stdint.h>  
#include "bsp_api.h"  
#include "common_data.h"  
#include "r_wdt.h"  
#include "r_wdt_api.h"  
#ifdef __cplusplus  
extern "C"  
{  
#endif  
extern const wdt_instance_t g_wdt0;  
#ifndef NULL  
void NULL(wdt_callback_args_t * p_args);  
#endif  
extern wdt_instance_ctrl_t g_wdt0_ctrl;  
extern const wdt_cfg_t g_wdt0_cfg;  
void hal_entry(void);  
void g_hal_init(void);
```

```
#ifndef __cplusplus
} /* extern "C" */
#endif
#endif /* HAL_DATA_H_ */
```

hal\_data.h contains the header files required by the generated project. In addition this file includes external references to the **g\_wdt0** instance structure which contains pointers to the configuration, control, api structures used for WDT HAL driver.

#### Warning

This file is regenerated each time Generate Project Content is clicked and must not be edited.

#### 2.4.5.2 WDT hal\_data.c

The contents of hal\_data.c are shown below.

```
/* generated HAL source file - do not edit */
#include "hal_data.h"
wdt_instance_ctrl_t g_wdt0_ctrl;
const wdt_cfg_t g_wdt0_cfg =
{
    .timeout          = WDT_TIMEOUT_16384,
    .clock_division  = WDT_CLOCK_DIVISION_8192,
    .window_start    = WDT_WINDOW_START_100,
    .window_end      = WDT_WINDOW_END_0,
    .reset_control   = WDT_RESET_CONTROL_RESET,
    .stop_control    = WDT_STOP_CONTROL_ENABLE,
    .p_callback      = NULL,
};
/* Instance structure to use this module. */
const wdt_instance_t g_wdt0 =
{.p_ctrl = &g_wdt0_ctrl, .p_cfg = &g_wdt0_cfg, .p_api = &g_wdt_on_wdt};
void g_hal_init (void)
{
    g_common_init();
}
```

hal\_data.c contains g\_wdt0\_ctrl which is the control structure for this instance of the WDT HAL driver. This structure should not be initialized as this is done by the driver when it is opened.

The contents of g\_wdt0\_cfg are populated in this file using the **Watchdog Driver on g\_wdt0** pane in the Project Configuration **Stacks** tab. If the contents of this structure do not reflect the settings made in the IDE, ensure the **Project Configuration** settings are saved before clicking the **Generate Project Content** button.

#### Warning

This file is regenerated each time Generate Project Content is clicked and so should not be edited.

### 2.4.5.3 WDT main.c

Contains main() called by the BSP start-up code. main() calls hal\_entry() which contains user developed code (see next file). Here are the contents of main.c.

```
/* generated main source file - do not edit*/
#include "hal_data.h"

int main (void)
{
    hal_entry();
    return 0;
}
```

#### Warning

This file is regenerated each time Generate Project Content is clicked and so should not be edited.

### 2.4.5.4 WDT hal\_entry.c

This file contains the function hal\_entry() called from main(). User developed code should be placed in this file and function.

For the WDT project edit the contents of this file to contain the code below. This code implements the flowchart in overview section of this document.

```
#include "hal_data.h"
#include "bsp_pin_cfg.h"
#include "r_ioport.h"
#define RED_LED_NO_OF_FLASHES 30
#define RED_LED_PIN BSP_IO_PORT_01_PIN_00
#define GREEN_LED_PIN BSP_IO_PORT_04_PIN_00
#define RED_LED_DELAY_MS 125
```

```
#define GREEN_LED_DELAY_MS 250
volatile uint32_t delay_counter;
volatile uint16_t loop_counter;
void R_BSP_WarmStart(bsp_warm_start_event_t event);
/*****
*****/
void hal_entry (void)
{
    /* Allow the WDT to run when the debugger is connected */
    R_DEBUG->DBGSTOPCR_b.DBGSTOP_WDT = 0;

    /* Open the WDT */
    R_WDT_Open(&g_wdt0_ctrl, &g_wdt0_cfg);

    /* Start the WDT by refreshing it */
    R_WDT_Refresh(&g_wdt0_ctrl);

    /* Flash the red LED and feed the WDT for a few seconds */
    for (loop_counter = 0; loop_counter < RED_LED_NO_OF_FLASHES; loop_counter++)
    {
        /* Turn red LED on */
        R_IOPORT_PinWrite(&g_ioport_ctrl, RED_LED_PIN, BSP_IO_LEVEL_LOW);

        /* Delay */
        R_BSP_SoftwareDelay(RED_LED_DELAY_MS, BSP_DELAY_UNITS_MILLISECONDS);

        /* Refresh WDT */
        R_WDT_Refresh(&g_wdt0_ctrl);

        R_IOPORT_PinWrite(&g_ioport_ctrl, RED_LED_PIN, BSP_IO_LEVEL_HIGH);

        /* Delay */
        R_BSP_SoftwareDelay(RED_LED_DELAY_MS, BSP_DELAY_UNITS_MILLISECONDS);

        /* Refresh WDT */
        R_WDT_Refresh(&g_wdt0_ctrl);
    }

    /* Flash green LED but STOP feeding the WDT. WDT should reset the
    * device */
    while (1)
    {
        /* Turn green LED on */
```

```

R_IOPORT_PinWrite(&g_ioport_ctrl, GREEN_LED_PIN, BSP_IO_LEVEL_LOW);
/* Delay */
R_BSP_SoftwareDelay(GREEN_LED_DELAY_MS, BSP_DELAY_UNITS_MILLISECONDS);
/* Turn green off */
R_IOPORT_PinWrite(&g_ioport_ctrl, GREEN_LED_PIN, BSP_IO_LEVEL_HIGH);
/* Delay */
R_BSP_SoftwareDelay(GREEN_LED_DELAY_MS, BSP_DELAY_UNITS_MILLISECONDS);
}
}
/*****
*****/
void R_BSP_WarmStart (bsp_warm_start_event_t event)
{
    if (BSP_WARM_START_RESET == event)
    {
#if BSP_FEATURE_FLASH_LP_VERSION != 0
        /* Enable reading from data flash. */
        R_FACI_LP->DFLCTL = 1U;

        /* Would normally have to wait for tDSTOP(6us) for data flash recovery. Placing the
enable here, before clock and
        * C runtime initialization, should negate the need for a delay since the
initialization will typically take more than 6us. */
#endif
    }

    if (BSP_WARM_START_POST_C == event)
    {
        /* C runtime environment and system clocks are setup. */
        /* Configure pins. */
        R_IOPORT_Open(&g_ioport_ctrl, &g_bsp_pin_cfg);
    }
}

```

The WDT HAL driver API functions are defined in `r_wdt.h`. The WDT HAL driver is opened through the `open` API call using the instance structure defined in `r_wdt_api.h`:

```
/* Open the WDT */  
R_WDT_Open(&g_wdt0_ctrl, &g_wdt0_cfg);
```

The first passed parameter is the pointer to the control structure `g_wdt0_ctrl` instantiated in `hal_data.c`. The second parameter is the pointer to the configuration data `g_wdto_cfg` instantiated in the same `hal_data.c` file.

The WDT is started and refreshed through the API call:

```
/* Start the WDT by refreshing it */  
R_WDT_Refresh(&g_wdt0_ctrl);
```

Again the first (and only in this case) parameter passed to this API is the pointer to the control structure of this instance of the driver.

## 2.4.6 Building and Testing the Project

Build the project in e2 studio by clicking **Build > Build Project** or by clicking the build icon. The project should build without errors.

To debug the project

1. Connect the USB cable between the target board debug port and host PC.
2. In the **Project Explorer** pane on the left side of e2 studio, right-click on the WDT project **WDT\_Application** and select **Debug As > Debug Configurations**.
3. Under **Renesas GDB Hardware Debugging** select **WDT\_Application Debug** as shown below.

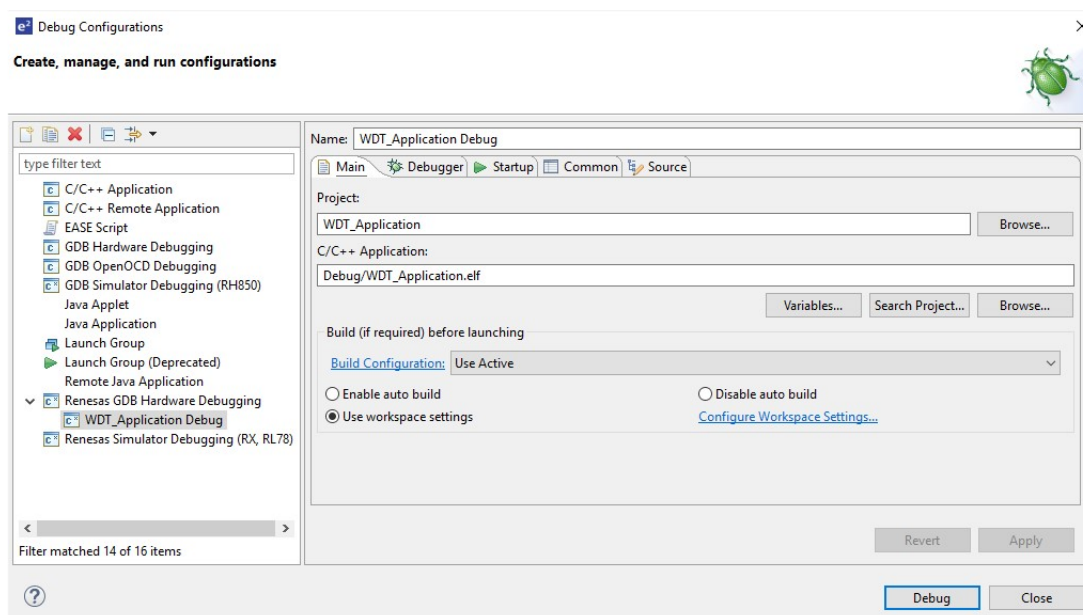
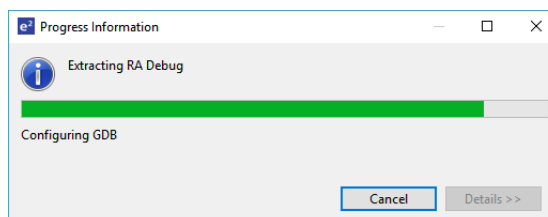


Figure 98: Debug configuration

- Click the **Debug** button. Click Yes to the debug perspective if asked.



- The code should run the `Reset_Handler()` function.
- Resume execution via **Run > Resume**. Execution will stop in `main()` at the call to `hal_entry()`.
- Resume execution again.

The red LED should start flashing. After 30 flashes the green LED will start flashing and the red LED will stop flashing.

While the green LED is flashing the WDT will underflow and reset the device resulting in the red LED to flash again as the sequence repeats.

- Stop the debugger in e2 studio via **Run > Terminate**.
- Click the reset button on the target board. The LEDs begin flashing.

## 2.5 Primer: TrustZone Project Development

This section will introduce the user to the tools supporting TrustZone configuration for the RA Family of microcontrollers. It is intended to be read by development engineers implementing RA TrustZone projects for the first time. It will introduce basic concepts followed by workflow and tooling functions

designed to simplify and accelerate their first TrustZone development. A background knowledge of e<sup>2</sup> studio and RA device hardware is expected.

## Target Device

RA Cortex<sup>®</sup>-M33 or Cortex<sup>®</sup>-M23 devices with TrustZone security extension.

### 2.5.1 Renesas Implementation of Arm TrustZone Technology

For brevity, TrustZone will be abbreviated to TZ in this document.

The following section is supplied for reference only. For full details of TZ implementation, please refer to Arm documentation (<https://developer.arm.com/ip-products/security-ip/trustzone>) and the RA6M4 device manual.

Arm TZ technology divides the MCU and therefore the application into Secure and Non-Secure partitions. Secure applications can access both Secure and Non-Secure memory and resources. Non-Secure code can access Non-Secure memory and resources as well as Secure resources through a set of so-called veneers located in the Non-Secure Callable (NSC) region. This ensures a single access point for Secure code when called from the Non-Secure partition. The MCU starts up in the Secure partition by default. The security state of the CPU can be either Secure or Non-Secure.

The MCU code flash, data flash, and SRAM are divided into Secure (S) and Non-Secure (NS) regions. Code flash and SRAM include a further region known as Non-Secure Callable (NSC). These memory security attributes are set into the non-volatile memory via SCI or USB boot mode commands when the device lifecycle is Secure Software Debug (SSD) state. The memory security attributes are loaded into the Implementation Defined Attribution Unit (IDAU) peripheral and the memory controller before application execution and cannot be updated by application code.

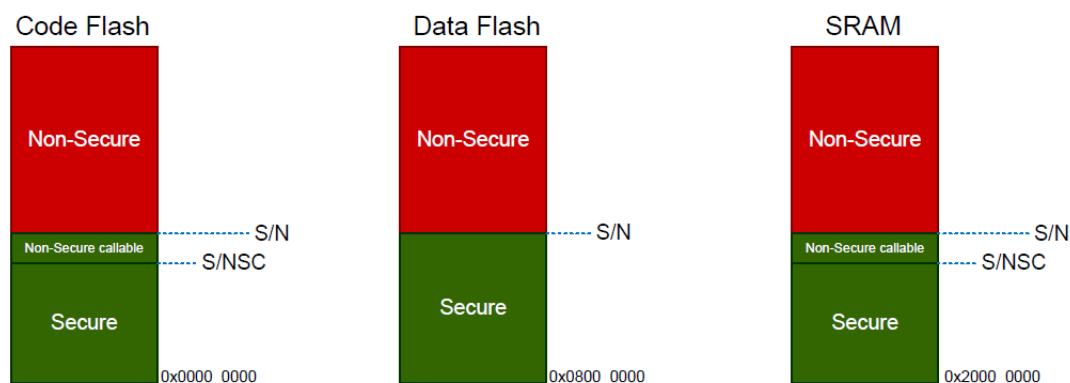


Figure 99: Secure and Non-Secure Regions

Note: All external memory accesses are considered to be Non-Secure.

Code Flash and SRAM can be divided into Secure, Non-Secure, and Non-Secure Callable. All secure memory accesses from the Non-Secure region MUST go through the Non-Secure Callable gateway and target a specific Secure Gateway (SG) assembler instruction. This forces access to Secure APIs at a fixed location and prevents calls to sub-functions and so on. Failing to target an SG instruction will generate a TZ exception.



TZ enabled compilers will manage generation of the NSC veneer automatically using CMSE extensions.

### 2.5.1.1 Calling from Non-Secure to Secure

A new instruction SG (Secure Gateway) has been added to the Armv8-M architecture. This MUST be the destination instruction for any branch within the Non-Secure Callable region. If an attempt is made to branch to any other instruction from the Non-Secure partition, a TZ exception will be thrown.

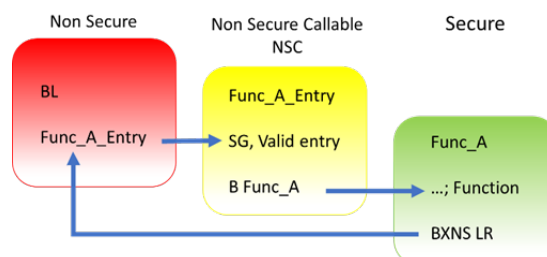


Figure 100: Calling from Non-Secure to Secure Functions

### 2.5.1.2 Calling from Secure to Non-Secure

Secure code uses B(L)XNS instructions to make direct calls to Non-Secure functions. While this is certainly possible, it can create a security vulnerability in the application. It is also challenging for the Secure application to determine the address of the non-secure function during build phase. From the RA Tools and FSP point view, calling directly from Secure to Non-Secure via FSP API is not supported.

Preference is for the Secure code to initialise as necessary from reset, then pass control to the Non-Secure partition. It will manage any data transfers and so forth via FSP call-backs as security checks. For, example secure data can be copied to Non-Secure RAM.

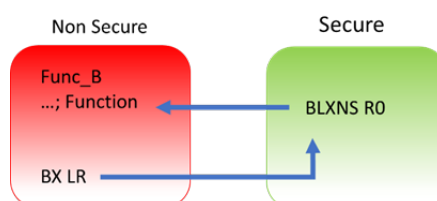


Figure 101: Calling from Secure to Non-Secure Functions

## 2.5.2 Workflow

TrustZone MCU development normally consists of two projects within a workspace, Secure and Non-Secure. General project workflows are described in the following sections. The Renesas project generator also supports development with "Flat project" model with no TrustZone awareness.

### 2.5.2.1 Secure Project

1. Start a new Secure project in e<sup>2</sup> studio.
2. Select and configure pins and drivers/stacks that need to be initialized and used in Secure mode. This should be kept to a minimum to reduce the security attack surface.

3. Expose top of stacks as Non-Secure Callable (NSC) **if** they need to be accessed from Non-Secure partition. Again, this should be kept to a minimum.
4. Generate project content and write Secure code such as key handling and opening drives as needed.
5. Modify/remove any unnecessary "Guard" functions as needed to control access via NSC.
6. Build project.
7. A Non-Secure project will be needed before debugging. If necessary, prepare a "dummy" Non-Secure project or replace `R_BSP_NonSecureEnter();` with `while(1);` in `hal_entry.c`.

### 2.5.2.2 Non-Secure Project

1. Start a new Non-Secure project.
2. If you have access to the Secure project, choose this option. However, if you only have access to a device with pre-programmed Secure code (commonly referred to as provisioned device) choose "Secure Bundle".
3. Select and configure pins and drivers/stacks that need to be initialized and used in Non-Secure mode.
4. Note that you can add NSC drivers and stacks as needed.
5. Generate project content and write Non-Secure code as needed
6. Access NSC drivers and Stacks via Guard functions.
7. Build and debug project.

### 2.5.2.3 Flat Project

A flat project does not technically use TrustZone as the developer has made a decision to place the entire application in Secure partition from restart.

Notes:

- Any code placed in external memory (such as OSPI or QSPI) will be Non-Secure.
- The Ethernet EDMAC is designed to be a Non-Secure bus master so associated Ethernet RAM buffers will be placed in Non-Secure RAM. The tooling will automatically manage this.

The workflow is as follows:

1. Start a new Flat project.
2. Select and configure pins and drivers/stacks as needed.
3. Generate project content and write code as needed.
4. Build and debug project.

## 2.5.3 RA Project Generator (PG)

The RA project generators have been created to help users through setting up new TZ enabled projects. User will be prompted for project settings such as Project Type (Secure, Non-Secure, or Flat), compiler, RTOS and debugger. Care is needed when setting up a TZ project to ensure that the connection between Secure and Non-Secure partitions are managed correctly.

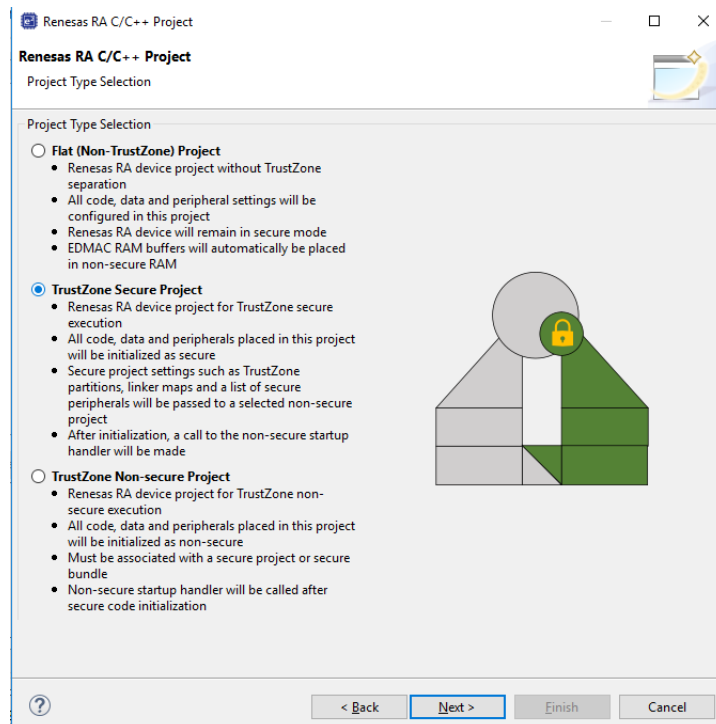


Figure 102: Secure Project (following Arm notation as green)

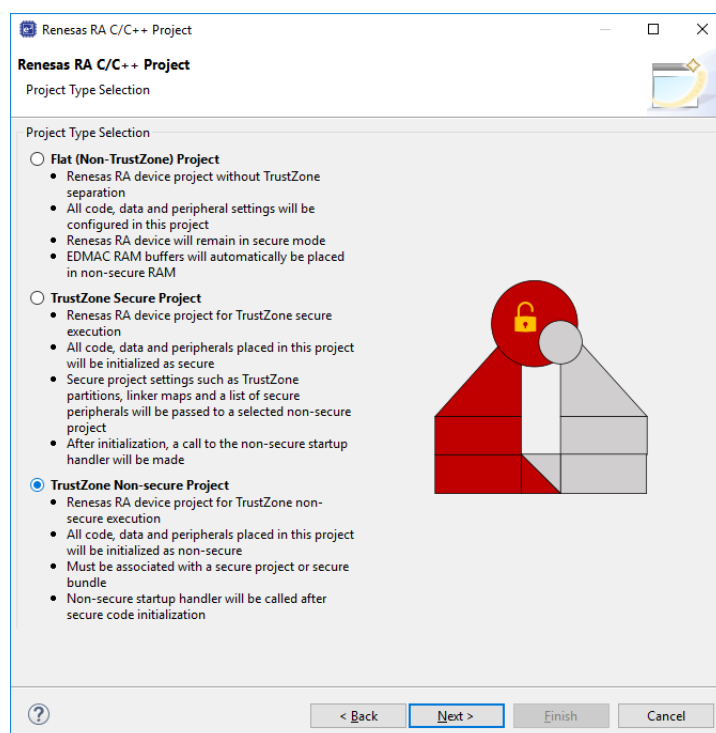


Figure 103: Non-Secure Project (following Arm notation as red)

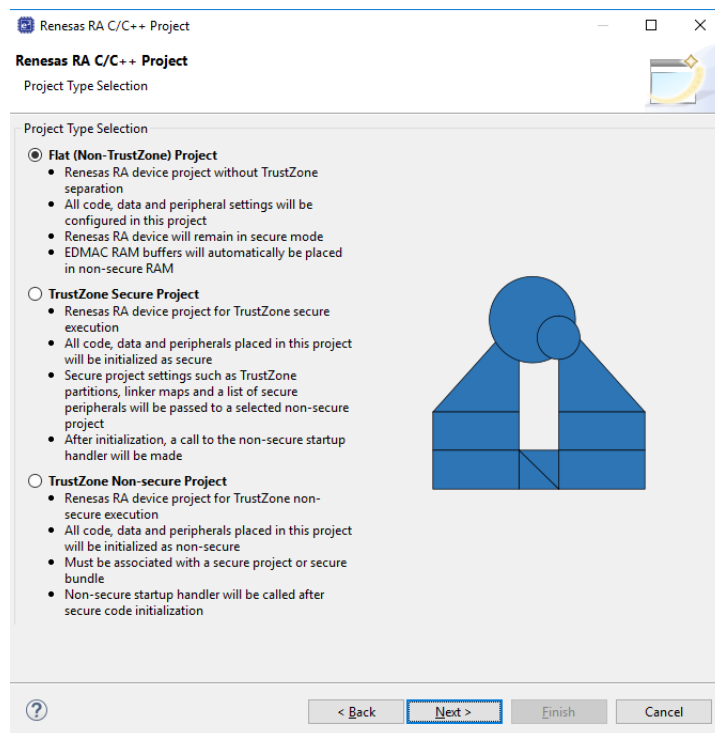


Figure 104: Flat Project

### 2.5.3.1 Secure Project Set Up

All code, data, and peripherals in this project will be configured as Secure using the device Peripheral Security Attribution (PSA) registers. Although it is very application specific, we recommend keeping the Secure project code as small as possible to reduce the attack surface. For example, secure key handling may be the only application code in the secure project.

Necessary values to set up the TZ memory partition (IDAU registers) will be automatically calculated after the project is built to ensure they match the code and data size, keeping the attack surface as small as possible.

Typically, ANSI C start up code (clearing of RAM, variable initialisation, etc) , clock, and secure peripheral initialisation will occur in this project.

At the end of the Secure code, a call will be made to `R_BSP_NonSecureEnter()`; to pass control to the Non-Secure partition.

Non-Secure Callable (NSC) "Guard" functions are added to the project and expose selected modules to Non-Secure projects. User can add application-specific access checks as needed in these functions.

Output of this project type will be an elf file that must be either pre-programmed (provisioned) into a device or referenced by a Non-Secure project (via Secure bundle \*.SBD) to build a final image.

This project type will NOT typically be debugged in isolation and will normally require a Non-Secure project such as a call to a `R_BSP_NonSecureEnter()` to be made. This can be replaced with `while(1);` if needed.

### 2.5.3.2 RTOS Support in TZ Project

Although the RTOS kernel and user tasks will reside in the Non-Secure partition, the Secure partition needs to allocate stack space and so on. It is essential when starting a new RTOS project that the TrustZone Secure RTOS-Minimal template is selected. This will add the Arm TrustZone Context RA Port as below.

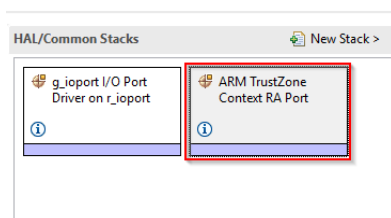
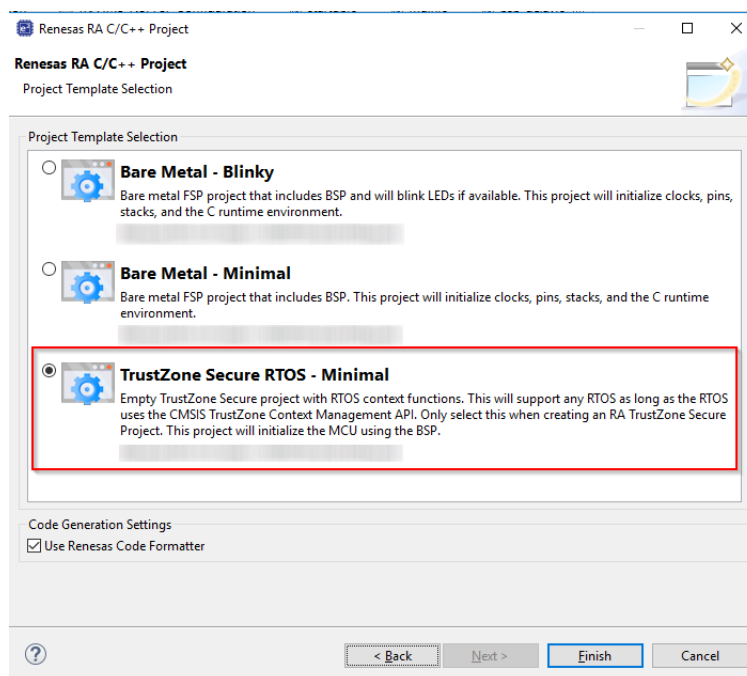


Figure 105: Secure RTOS-Minimal Template

### 2.5.3.3 Peripheral Security Attribution

Each peripheral can be configured to be Secure or Non-Secure. Peripherals are divided into two types.

Type-1 peripherals have one security attribute. Access to all registers is controlled by one security attribute. The Type-1 peripheral security attribute is set in the PSARx (x = B to E) register by the secure application.

Type-2 peripherals have the security attribute for each register or for each bit. Access to each register or bit field is controlled according to these security attributes. The Type-2 peripheral security attribute is set in the Security Attribution register in each module by the Secure application. For more information about the Security Attribution register, see sections in the Appropriate MCU's User's Manual for each peripheral.

Table 1. Secure and Non-Secure Peripherals

Type	Peripheral
Type 1	SCI, SPI, USBFS, CAN, IIC, SCE9, DOC, SDHI, SSIE, CTSU, CRC, CAC, TSN, ADC12, DAC12, POEG, AGT, GPT, RTC, IWDT, WDT
Type 2	System control (Resets, LVD, Clock Generation Circuit, Low Power Modes, Battery Backup Function), FLASH CACHE, SRAM controller, CPU CACHE, DMAC, DTC, ICU, MPU, BUS, Security setting, ELC, I/O ports
Always Non-Secure	CS Area Controller, QSPI, OSPI, ETHERC, EDMAC

FSP will initialise the arbitration registers during Secure project BSP start up. User code may also be written to set or clear further arbitration. However care must be taken not to undermine FSP.

#### 2.5.3.4 Non-Secure

All code, data, and peripherals in this project will be configured as Non-Secure. This project type must be associated with a Secure project to enable access to secure code, peripherals, linker scripts and others.

#### 2.5.3.5 Flat Project Type

All code, data, and peripherals are configured in a Secure single partition except for the EDMAC RAM buffers that will remain in the Non-Secure partition. Effectively, TZ is disabled.

#### 2.5.3.6 Secure Connection to Non-Secure Project

When starting a new Non-Secure Project, the user will be prompted for either a Secure Project or Secure Bundle. In each case, details of the linker settings, Non-Secure Callable functions, and Secure peripherals will be read to enable the Non-Secure project setup.

Should the Secure project or bundle be rebuilt, the Non-Secure editor will detect this and prompt user to regenerate the Non-Secure project configuration.

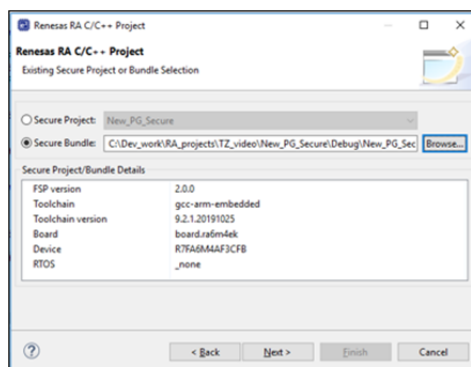


Figure 106: Secure Project or Bundle Selection

### Secure Project (Combined)

A Secure project must reside in the same Workspace as the Non-Secure project and will typically be used when a design engineer has access to both the Secure and Non-Secure project sources. This is sometimes known as "Combined model".

A Secure .elf file will be referenced and included in the debug configuration for download to the target device. The development engineer will have visibility of Secure and Non-Secure project source code and configuration.

### **Secure Bundle (Split)**

A Secure Bundle will ONLY include linker memory ranges, symbol references, and details of locked Secure peripheral configuration settings but no access to Secure source code (API header files will be included as necessary).

The Secure bundle file (\*.SBD) must be supplied to the Non-Secure developer by the Secure project developer.

The development engineer will typically not have access to the Secure project or .elf file which MUST be pre-programmed or provisioned into the target MCU.

The DLM state of target device should then be switched to NSECSD (see section 6.2) before the device is provided to the non-secure developer.

This is often referred to as "Split model" where a basic security set up is developed by a Secure team and then passed to the Non-Secure team in the same facility or at a third party. The Non-Secure team has no access to the Secure source code and cannot directly access Secure peripherals, data, or APIs.

### **2.5.3.7 Debug Configurations**

After each project type has been selected, a suitable debug configuration will be generated.

#### **Non-Secure with Secure Project (Combined)**

Both Secure and Non-Secure .elf files will be downloaded.

A debug configuration called <project name>\_SSD will be generated.

#### **Non-Secure with Secure Bundle (Split)**

Only a Non-Secure elf will be downloaded. This configuration must be used with a pre-provisioned device (Secure project pre-programmed into MCU Flash).

A debug configuration called <project name>\_NSECSD will be generated.

#### **Flat Debug**

A single .elf file will be downloaded.

A debug configuration called <project name>\_FLAT will be generated.

### **2.5.4 Secure Projects**

As mentioned, Secure code will be called immediately after device reset and run ANSI C start up, clock, interrupt vector table, and secure peripheral initialization before starting user code. All

selected peripheral configuration settings will be automatically initialised as Secure.

### 2.5.4.1 Secure Clock

Device clock settings are the possible exception in that they will be initialised in the Secure project (to enable faster start up from reset) but can be set as Secure or Non-Secure as user application may need to change settings during execution (for low-power mode and so on). The Secure and Non-Secure FSP BSPs can both change the clock settings.

However, clock settings can be locked as Secure should the developer choose to do so.

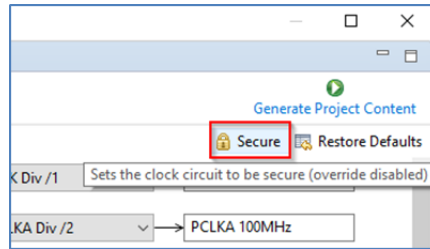


Figure 107: Secure Clock Setting

### 2.5.4.2 Setting Drivers as NSC

Some driver and middleware stacks in the Secure project may need to be accessed by the Non-Secure partition. To enable generation of NSC veneers, set "Non-Secure Callable" from the right-click context menu for the selected modules in the Configurator.

Note: It is only possible to "expose" top of stacks as NSC.

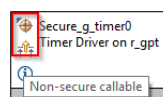
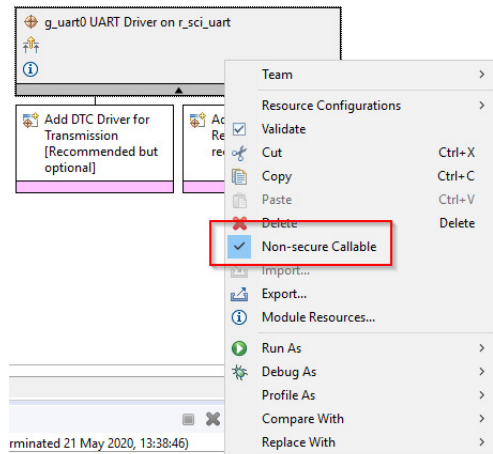


Figure 108: Generate NSC Veneers

The top of the stack will be marked with a new icon and tool tip to signify NSC access.



### 2.5.4.3 Guard Functions

Access to NSC drivers from a Non-Secure project is possible through the Guard APIs. FSP will automatically generate Guard functions for all the top of stack/driver APIs added to the project as Non-Secure Callable.

User can choose to add further levels of access control or delete guard function if they wish to only expose a limited range of APIs to a Non-Secure developer.

```
BSP_CMSE_NONSECURE_ENTRY fsp_err_t g_uart0_open_guard(  
    uart_ctrl_t *const p_api_ctrl, uart_cfg_t const *const p_cfg) {  
    /* TODO: add your own security checks here */  
    FSP_PARAMETER_NOT_USED(p_api_ctrl);  
    FSP_PARAMETER_NOT_USED(p_cfg);  
    return R_SCI_UART_Open(&g_uart0_ctrl, &g_uart0_cfg);  
}
```

For example, an SCI channel may be opened and configured for a desired baud rate by the Secure developer, but only enable the Write API to the Non-Secure developer. In which case, all but `g_uart0_write_guard()` could be deleted. CTRL structures are not required as they will be added on the Secure side.

For example, the call from the Non-Secure partition would be as follows:

```
err = g_uart0_open_guard(0,0);
```

## 2.5.5 Non-Secure projects

Configuration of the project can continue as for other RA devices, but certain resources will be locked if they have been previously set up as Secure.

The Non-Secure project will be called from the Secure project via `R_BSP_NonSecureEnter()`;

### 2.5.5.1 Clock Set Up

You may recall that clocks can be set as Secure or Non-Secure. If they are set as Secure, settings will only be available to view, and user will not be able to change them. The Override button will be greyed. This is useful to preserve CGC sync with secure project by not overriding unless necessary. If it is NOT set as Secure, user can choose to override the initial Secure settings

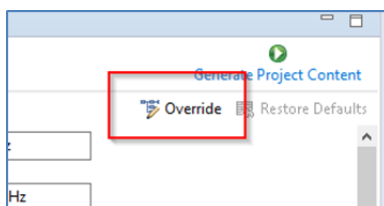


Figure 109: Clock Setting as Non-Secure

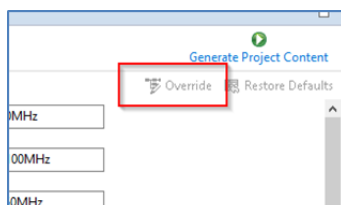


Figure 110: Clock Setting as Secure

### 2.5.5.2 Selecting NSC Drivers

Drivers declared as NSC in a Secure project can be selected and added to Non-Secure project and will be decorated as before.

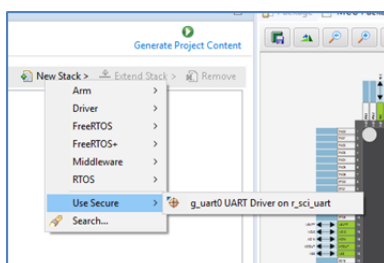
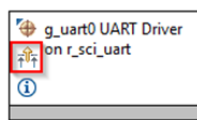


Figure 111: Selecting NSC Drivers

### 2.5.5.3 Locked Resources

When a NSC Secure driver is added to a Non-Secure project, the configuration settings are locked and are available for information only. A padlock is added for indication.

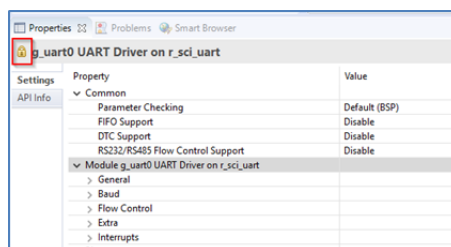


Figure 112: Locked Resources

#### 2.5.5.4 Locked Channels

In a peripheral with multiple channels, for example, DMA, if a Non-Secure developer tries to select a channel that has already been defined as Secure, the following error message type will be displayed.

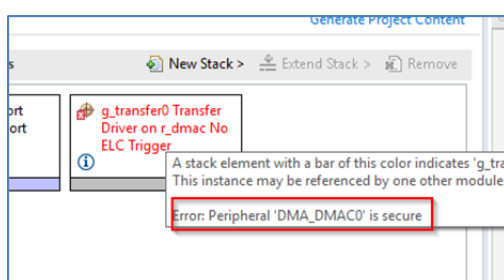


Figure 113: Error Message when Selecting a Secure Channel

### 2.5.6 IDAU registers

Renesas RA TZ-enabled devices include a set of registers known as Implementation Defined Attribution Unit (IDAU) that are used to set up partitions between Secure, Non-Secure Callable, and Non-Secure regions. The IDAU registers can only be programmed during MCU **boot mode** and NOT through the debug interfaces. Because of this, special debugger firmware has been developed to manage bringing the device up in SCI boot mode to set up the IDAU registers (automatically drives MD pin) and then switch back to debug mode as needed.

**Note:** Please be aware of the extra signal connection (MD pin) needed on the debug interface connector. The Renesas Evaluation Kit (EK) for your selected device is a good reference.

Pin No.	SWD	JTAG	Serial Programming using SCI
1	VCC	VCC	VCC
2	P108/SWDIO	P108/TMS	NC
4	P300/SWCLK Wired OR with MD	P300/TCK Wired OR with MD	P201/MD
6	P109/SWO/TXD9	P109/TDO/TXD9	P109/TXD9
8	P110/RXD9	P110/TDI/RXD9	P110/RXD9
9	GNDdetect	GNDdetect	GNDdetect
10	nRESET	nRESET	nRESET
12	P214/TRACECLK	P214/TRACECLK	NC
14	P211/TRACEDATA[0]	P211/TRACEDATA[0]	NC
16	P210/TRACEDATA[1]	P210/TRACEDATA[1]	NC
18	P209/TRACEDATA[2]	P209/TRACEDATA[2]	NC
20	P208/TRACEDATA[3]	P208/TRACEDATA[3]	NC
3, 5, 15,17, 19	GND	GND	GND
7	NC	NC	NC
11, 13	NC	NC	NC

The e<sup>2</sup> studio build phase automatically extracts the IDAU partition register settings from the Secure.elf file and programs them into the device during debug connection, which can be observed in the console.

This is an important phase of TZ development as the Secure partitions should be set as small as possible to ensure that the security attack surface is as small as possible.

However, should the developer wish to make these partitions larger to accommodate, for example during field firmware updates, const or data arrays should be placed in the Secure project as needed.

```

Console Problems Debugger Console Smart Browser
New_PC_Non_Secure_Debug_SSD [Renesas GDB Hardware Debugging]

Starting server with the following options:
  Raw options          : C:\Users\b3800280\

Connecting to E2, ARM target
  GDBServer endian    : little
  Target power        : on
Starting target connection

Current status of the RA TrustZone device
  DLM state           : SSD
  Debug level         : 2
  IDAU memory regions :
  - Code Flash Secure size (kB) : 8
  - Code Flash NSC size (kB)   : 24
  - Data Flash Secure size (kB) : 0
  - SRAM Secure size (kB)      : 2
  - SRAM NSC size (kB)        : 6

```

Figure 114: RA TrustZone Device Current Status

It is also possible to manually set up the partition registers through the Renesas Device Partition Manager.

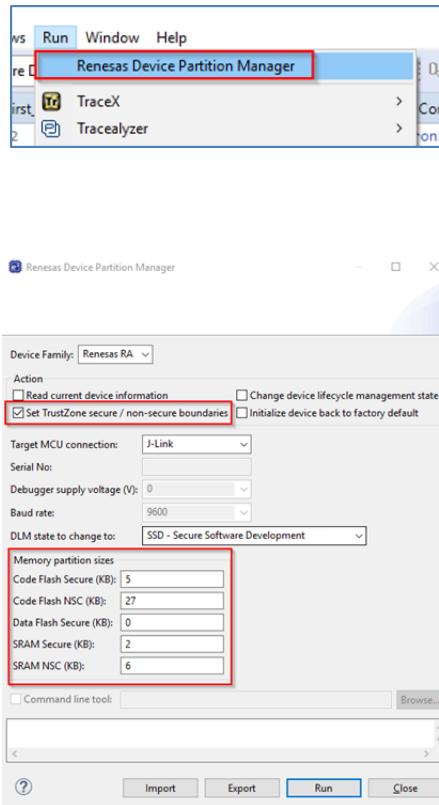


Figure 115: Renesas Device Partition Manager

### 2.5.6.1 SCI Boot Mode

Example of MD mode pin connection to debugger connector (from EK schematic).

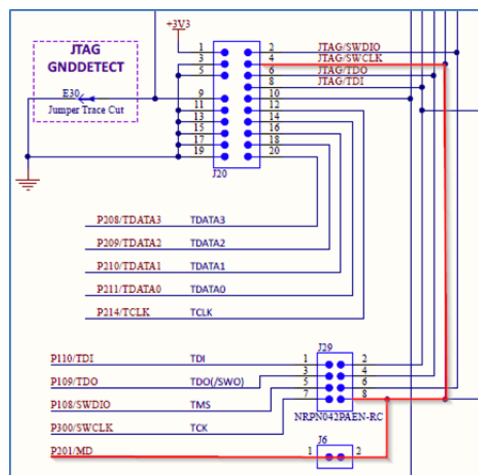


Figure 116: Example of MD Mode Pin Connection to Debugger Connector (from EK schematic)

### 2.5.6.2 DLM States

Device lifecycle defines the current phase of the device and controls the capabilities of the debug interface, the serial programming interface and Renesas test mode. The following illustration shows the lifecycle definitions and capability in each lifecycle.

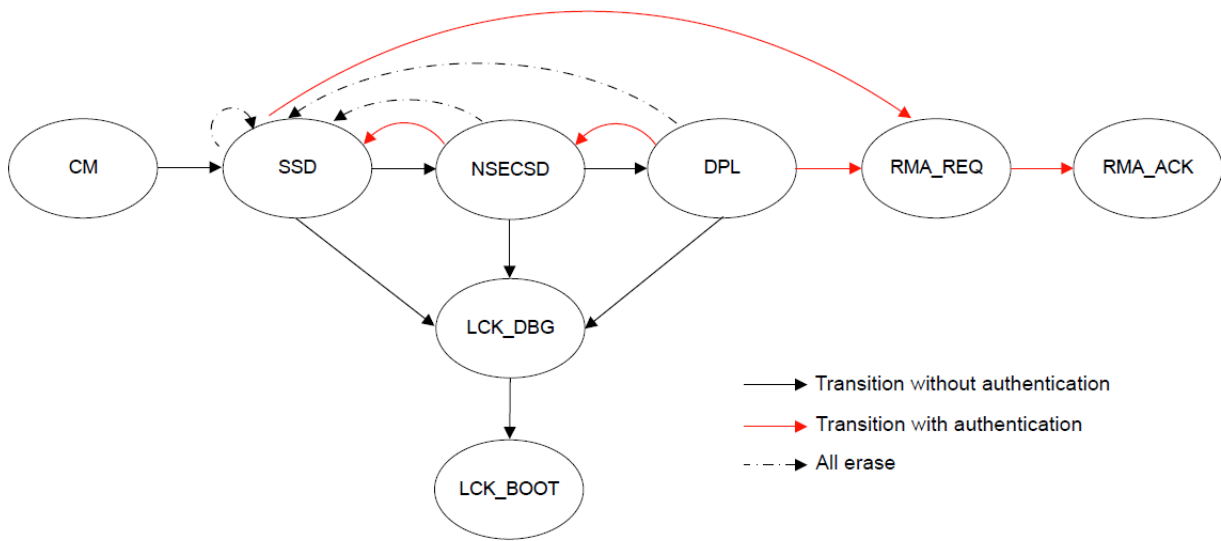


Figure 117: Lifecycle Stages

Note: All authentication key exchange and transitioning to LCK\_DBG, LCK\_BOOT, RMA\_REQ is only managed by Renesas Flash Programmer (RFP) and NOT within e<sup>2</sup> studio.

Lifecycle	Definition	Debug level	Serial programming	Test mode
CM	“Chip Manufacturing” The state when the customer received the device.	DBG2	Available, cannot access code/data flash	Not available
SSD	“Secure Software Development” The secure part of application is being developed.	DBG2	Available can program/erase/read all code/data flash area	Not available
NSECSD	“Non-SECure Software Development” The non-secure part of application is being developed.	DBG1	Available can program/erase/read all code/data flash area	Not available
DPL	“DePloyed” The device is in-field.	DBG0	Available cannot access code/data flash area	Not available
LCK_DBG	“LoCKed DeBuG” The debug interface is permanently disabled.	DBG0	Available cannot access code/data flash area	Not available
LCK_BOOT	“LoCKed BOOT interface” The debug interface and the serial programming interface are permanently disabled.	DBG0	Not available	Not available
RMA_REQ	“Return Material Authorization REQuest” Request for RMA. The customer must send the device to Renesas in this state.	DBG0	Available cannot access code/data flash area	Not available
RMA_ACK	“Return Material Authorization ACKnowledged” Failure analysis in Renesas	DBG2	Available cannot access code/data flash area	Available

Figure 118: Lifecycle Stages and Debug Levels

There are three debug access levels. The debug access level changes according to the lifecycle state.

- DBG2: The debugger connection is allowed, and no restriction to access memories and peripherals

- DBG1: The debugger connection is allowed, and restricted to access only Non-Secure memory regions and peripherals
- DBG0: The debugger connection is not allowed

Transitions for one state to another can be performed using the Renesas Flash Programmer (RFP, see section below) or using the Renesas Device Partition Manager (limited number of states possible). It is possible to secure transitions between states using authentication keys. For more information on DLM states and transitions (device specific), please refer to device user manual.

## 2.5.7 Debug

By default, the device will be in SSD mode and so allow access to Secure and Non-Secure partitions. In this mode both Secure and Non-Secure .elf files will be downloaded.

The current debugger status is displayed in the lower left corner and includes the DLM state (SSD or NSECSD) and current partition (Secure, Non-Secure, or Non-Secure Callable) when the debugger is stopped, for example.

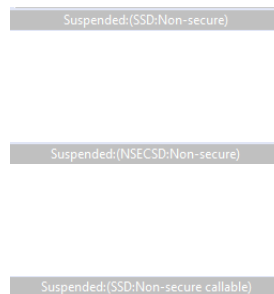


Figure 119: Current Debugger Status

### 2.5.7.1 Non-Secure Debug

Once the device is transitioned to NSECSD mode, only Non-Secure Flash, RAM and Peripherals can be accessed. In this mode, a Secure .elf must be pre-programmed (provisioned) into the device, and only a Non-Secure .elf file will be downloaded.

When in NSECSD mode access to Secure elements will be blocked and data displayed as ????????.

In NSECSD mode, it is not possible to set breakpoints on Secure code or data.

It is not possible to step into Secure code; the debugger will perform a step-over of any Secure function calls. Should the user press the Suspend button during execution, the debugger will stop at the next Non-Secure code access.

Assuming Secure memory region finishes at 32K (0x8000) in NSECSD debug mode (colour coding added for indication only), memory will be displayed as shown in the following figure.

Address	0 - 3	4 - 7	8 - B	C - F
0000000007FD0	????????	????????	????????	????????
0000000007FE0	????????	????????	????????	????????
0000000007FF0	????????	????????	????????	????????
0000000008000	20002496	000089B9	000088A5	000089B5
0000000008010	000089B5	000089B5	000089B5	00000000
0000000008020	00000000	00000000	00000000	000089B5
0000000008030	000089B5	00000000	000089B5	000089B5

Figure 120: Memory Display in NSECSD Debug Mode

Disassembly will be displayed as shown in the following figure.

```

Disassembly 0x8000
Cannot access memory at address 0x7ffc
00007ffd: Failed to execute MI command:
-data-disassemble -s 32765 -e 32797 -- 3
Error message from debugger back end:
Cannot access memory at address 0x7ffc
00007ffe: Failed to execute MI command:
-data-disassemble -s 32766 -e 32798 -- 3
Error message from debugger back end:
Cannot access memory at address 0x7ffe
00007fff: Failed to execute MI command:
-data-disassemble -s 32767 -e 32799 -- 3
Error message from debugger back end:
Cannot access memory at address 0x7ffe
vector:
00008000: movs r4, #152 ; 0x98
00008002: movs r0, #0
00008004: ldrh r1, [r7, #12]
00008006: movs r0, r0
00008008: ldrh r5, [r4, #4]

```

Figure 121: Disassembly Display in NSECSD Debug Mode

## 2.5.8 Debugger support

Renesas E2, E2 Lite, and SEGGER J-Link are supported in e<sup>2</sup> studio for TZ projects.

### Debugger Support for TZ Projects

Feature	E2 Lite	E2	J-Link	J-Link OB	ULINK	IAR i-Jet
JTAG	Yes	Yes	Yes	No	Yes	Yes
SWD	Yes	Yes	Yes	Yes	Yes	Yes
ETB trace	Yes	Yes	Yes	Yes	Yes	Yes
ETM trace	No	Yes	Yes	No	Yes	Yes
TZ partition programming	Yes	Yes	Yes	Yes	No	No
Non secure debug	Yes	Yes	Yes	Yes	Yes	Yes
e <sup>2</sup> studio	Yes	Yes	Yes	Yes	No	TBC
IAR EW Arm	Under consideration	Under consideration	Yes	Yes	No	Yes
Keil MDK	Under consideration	Under consideration	Yes	Yes	Yes	No

## 2.5.9 Third-Party IDEs

Third-party IDEs such as IAR Systems EWARM and Keil MDK (uVision) are supported by the RA Smart Configurator (RA SC).

In general, RA SC offers the same configurator functionality as e<sup>2</sup> studio documented above. Project



generators are available to initialise workspaces in the target IDEs as well as setting up debug configurations and so forth. However, there are some limitations that need to be noted especially with regards to IDAU TZ partition register programming. See the specific RA SC documentation for usage details.

### 2.5.10 Renesas Flash Programmer (RFP)

Updated versions of Renesas Flash Programmer (RFP) are available to support setting of partitions, DLM state and Authentication keys.

RFP can be downloaded free of charge on the Renesas web site.

A new mode has been added to Program Flash Options as shown in the following graphics.

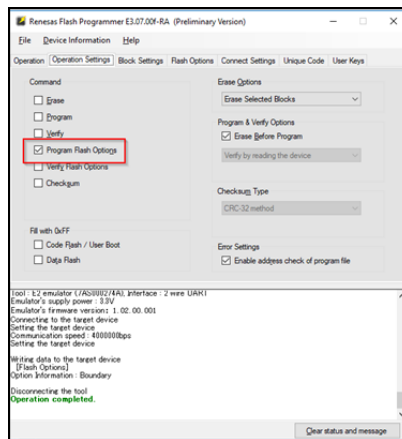


Figure 122: RFP Program Flash Options

Options to set partition boundaries are shown in the following figure.

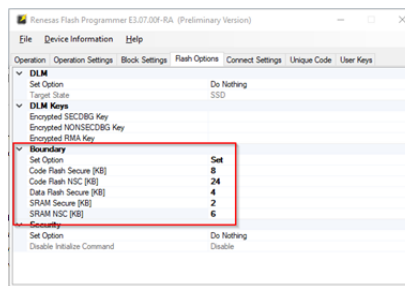


Figure 123: RFP Partition Boundaries

Options to set DLM state, Authentication Option keys, and Security settings are shown in the following figure.

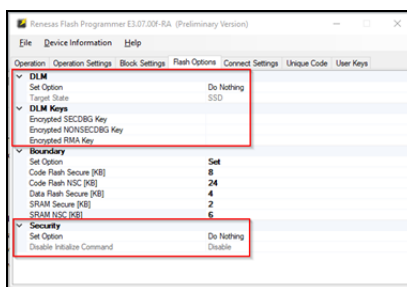


Figure 124: RFP DLM State, Authentication Keys, and Security Settings

Great care is needed here as some DLM states can **\*\*permanently\*\*** turn off debug and boot mode on the devices. Equally programming a security access authentication key can lead to permanently locked devices if the key is lost.

## 2.5.11 Glossary

### IDAU

Implementation Defined Attribute Unit. Used to program TZ partitions in SCI book mode.

### NSECSD

Non-Secure Software Development mode

### SSD

Secure Software Development mode

### NSC

Non-Secure Callable. Special Secure memory region used for Veneer to allow access to Secure APIs from Non-Secure code.

### Provisioned

Device with Secure code pre-programmed and DLM state set to **NSECSD**

### Flat project

All code, data and peripherals are configured as secure with the exception of the EDMAC RAM buffer which are placed in Non-Secure RAM due to the configuration of the internal bus masters.

### Veneer

Code that resides in Non-Secure Callable region

### Combined model

Development engineer has access to both Secure and Non-Secure project and source code

### Split model

Development Engineer has access to only the Non-Secure partition. No visibility of Secure source code. Secure code will be provisioned into device.

### 2.5.11.1 Configurator Icon Glossary

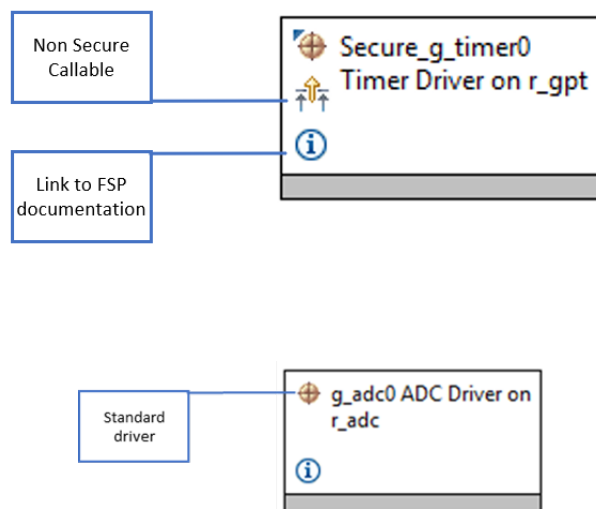


Figure 125: Configurator Icons

## 2.6 RA SC User Guide for MDK and IAR

### 2.6.1 What is RA SC?

The Renesas RA Smart Configurator (RA SC) is a desktop application designed to configure device hardware such as clock set up and pin assignment as well as initialization of FSP software components for a Renesas RA microcontroller project when using a 3rd-party IDE and toolchain.

The RA Smart Configurator can currently be used with

1. Keil MDK and the Arm compiler toolchain.
2. IAR EWARM with IAR toolchain for Arm

Projects can be configured and the project content generated in the same way as in e2 studio. Please refer to [Configuring a Project](#) section for more details.

### 2.6.2 Using RA Smart Configurator with Keil MDK

#### 2.6.2.1 Prerequisites

- Keil MDK and Arm compiler are installed and licensed. Please refer to the Release notes for the version to be installed.
- Import the RA device pack. Download the RA device pack archive file (ex: MDK\_Device\_Packs\_x.x.x.zip) from the [FSP GitHub release page](#). Extract the archive file to locate the RA device pack. To import the RA device pack, launch the PackInstaller.exe from <keil\_mdk\_install\_dir>\UV4. Select the menu item **File > Import...** and browse to the extracted .pack file.
- Verify that the latest updates for RA devices are included in Keil MDK. To verify, select the menu "Packs" in Pack Installer and verify that the menu item **Check for Updates on Launch** is selected. If not, select **Check for Updates on Launch** and relaunch Pack

Installer.

- For flashing and debugging, the latest Segger J-Link DLL is installed into Keil MDK.
- Install RA SC and FSP using the Platform Installer from the GitHub release page.

### 2.6.2.2 Create new RA project

The following steps are required to create an RA project using Keil MDK, RA SC and FSP:

1. To create an RA project in Keil MDK, an example template needs to be copied from the Pack Installer. The Pack Installer can be launched by running PackInstaller.exe from <keil\_mdk\_install\_dir>\UV4.
2. Select the device family or a device in the left pane of pack installer to filter the example templates in Examples tab in the right pane. The search bar in left pane helps to easily find a device. It is important to select the correct device and package type as this will be used by RA SC to configure pins.

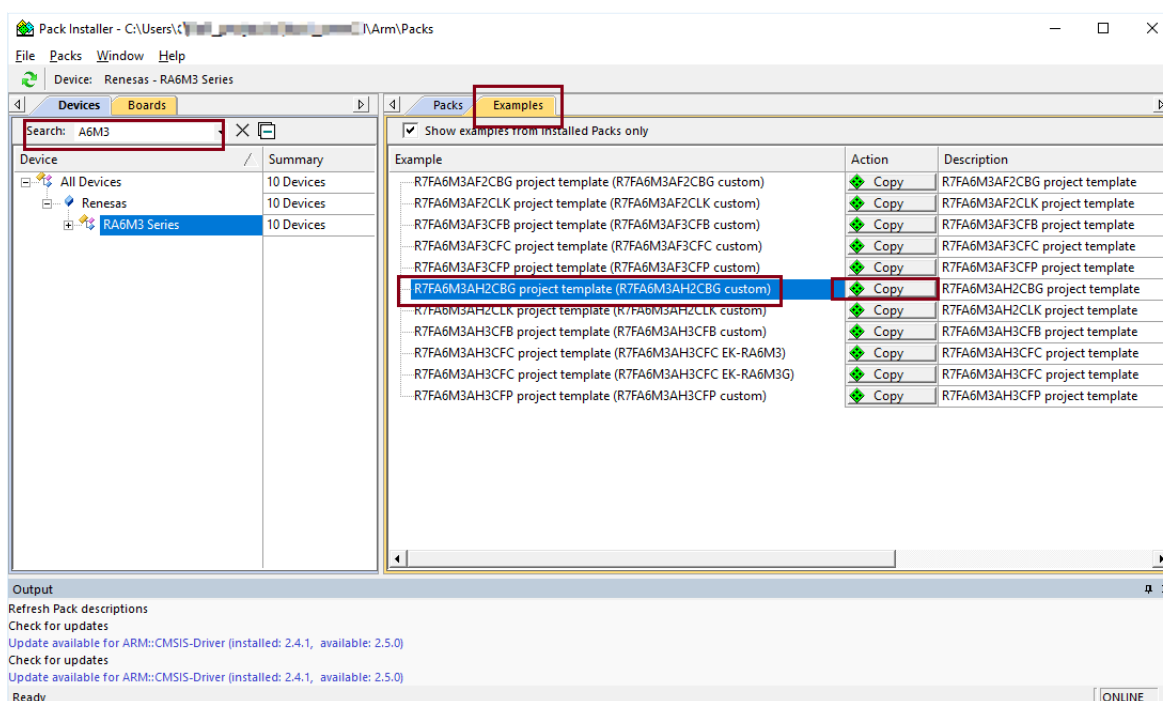


Figure 126: PackInstaller device example template

3. Click the **Copy** button for the example template to launch a dialog box and select where to copy the example project. The default project name will be the target device name.

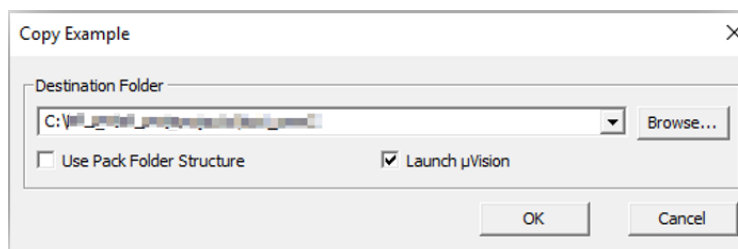


Figure 127: Copy Example dialog

Click **OK** to launch Keil uVision with the new project.

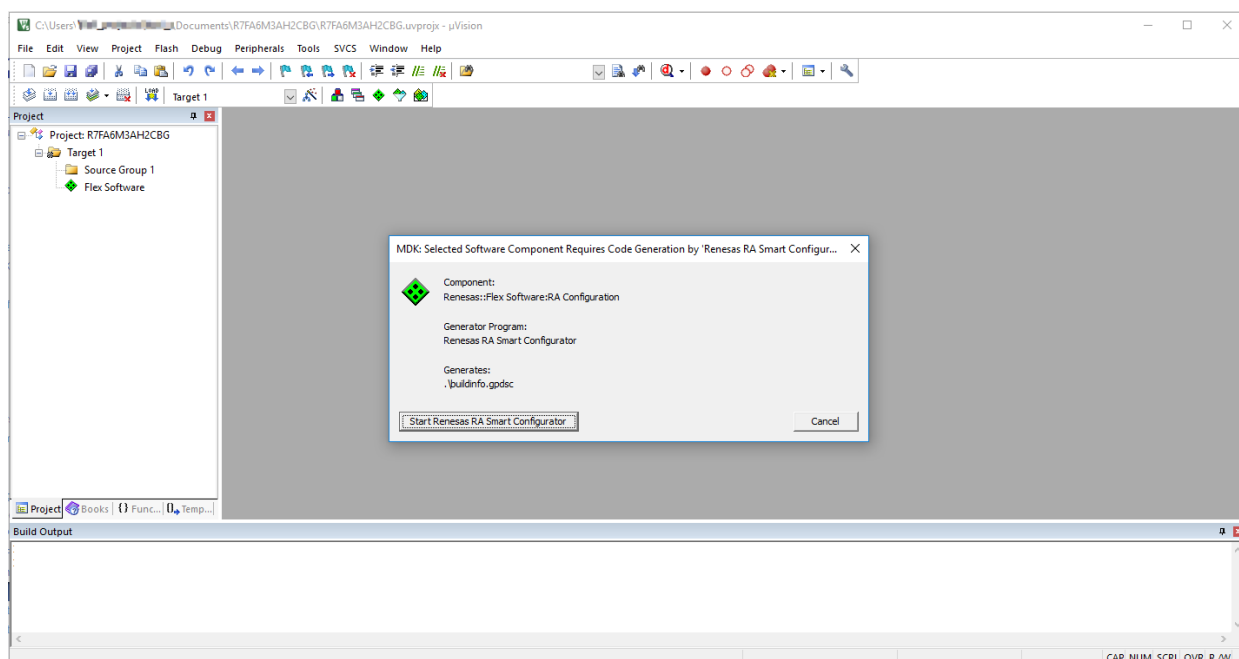


Figure 128: uVision

If the project name needs to be changed then deselect **Launch uVision** in the **Copy Example dialog** and click **\_OK**. Follow project rename instructions here: <http://www.keil.com/support/docs/3579.htm> Once renamed, open the project using menu item **Project > Open Project...** in uVision and continue with steps in [Modify existing RA project](#).

4. uVision offers to start the RA Smart Configurator (RA SC). Click **Start Renesas RA Smart Configurator** to launch it.

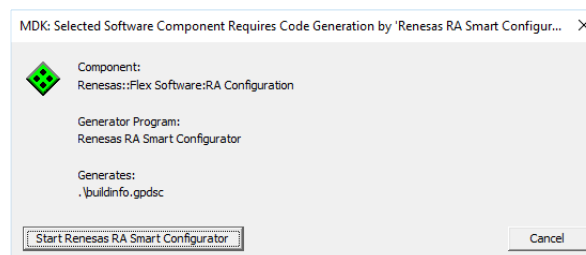
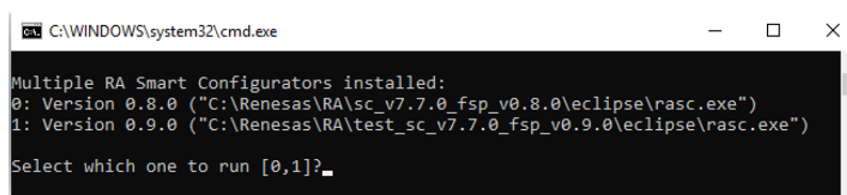


Figure 129: Launch RA SC confirmation dialog

5. If multiple versions of RA SC are installed, select the appropriate version of RA SC to run.



```
C:\WINDOWS\system32\cmd.exe

Multiple RA Smart Configurators installed:
0: Version 0.8.0 ("C:\Renesas\RA\sc_v7.7.0_fsp_v0.8.0\eclipse\rasc.exe")
1: Version 0.9.0 ("C:\Renesas\RA\test_sc_v7.7.0_fsp_v0.9.0\eclipse\rasc.exe")

Select which one to run [0,1]?_
```

Figure 130: RA SC version selection

6. RA SC will be launched with project generator wizard.
7. The configuration window opens once the project wizard is closed. Refer to [Configuring a Project](#) for more details on how to configure the project.
8. After clicking **Generate Project Content** in the RA Smart Configurator, return to uVision. uVision offers a dialog to import the changes and updates to the project made in RA SC. Select **Yes** to import the updated project and the project is ready to build.

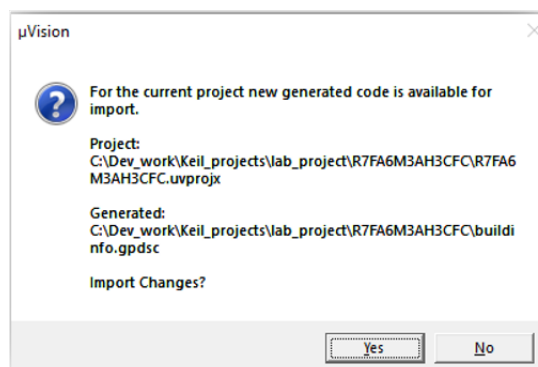


Figure 131: Import project data

RA SC will place the necessary FSP source code and header files into the project workspace. The folder structure is defined as below.

- Source Group 1 User source code should be added to the project in this folder
- Renesas RA Smart Configurator: Common Sources These source files are generated by RA Smart Configurator and can be edited as necessary
- Flex Software These are the source files from FSP and can be modified if needed. However, it is recommended NOT to edit these files as this may impact dependencies or functionality.

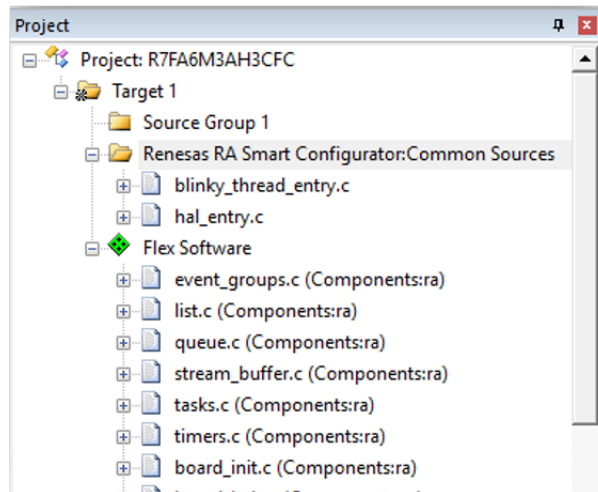


Figure 132: uVision project workspace with imported project data

### 2.6.2.3 Modify existing RA project

Once an initial project has been generated and configured, it is also possible to make changes using RA SC as follows:

1. If the desired project is not already open in uVision, the project can be opened using menu item **Project > Open project...** or selecting from the list of previous projects.
2. Select menu item **Project > Manage > Run-time Environment...** or tool bar button **Manage Run-Time Environment**.
3. Expand the **Flex Software** tree item in the dialog shown and click the green run button next to **FSP Configuration**. This launches RA SC and the FSP project configuration can be modified and updated.

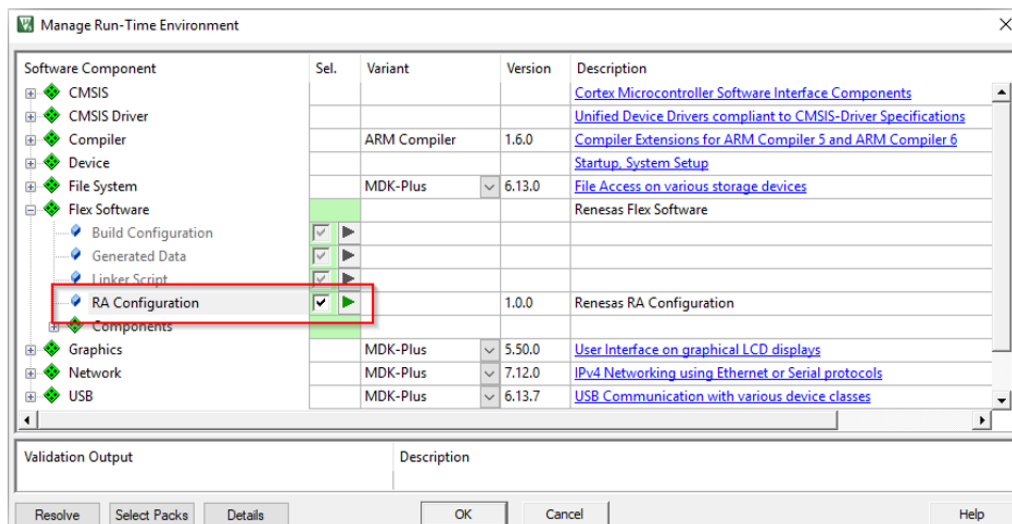


Figure 133: Manage run-time environment

### 2.6.2.4 Build and Debug RA project

The project can be built by selecting the menu item **Project > Build Target** or tool bar item **Rebuild** or the keyboard shortcut F7.

Assembler, Compiler, Linker and Debugger settings can be changed in **Options for Target** dialog, which can be launched using the menu item **Project > Options for Target**, the tool bar item **Options for Target** or the keyboard shortcut Alt+F7.

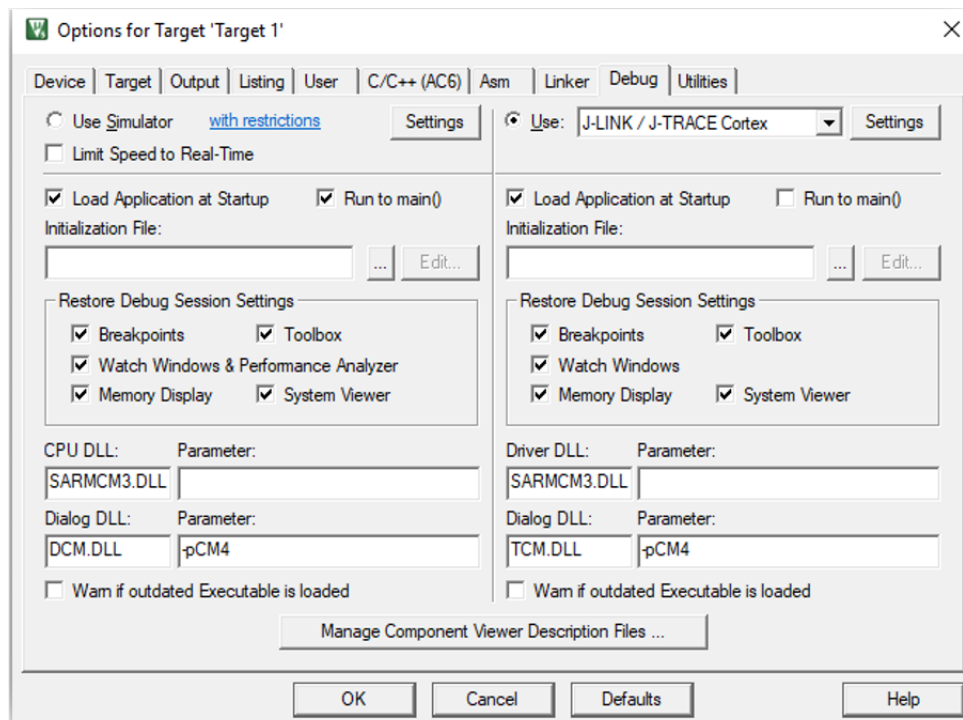


Figure 134: Options for Target

RA SC will set up the uVision project to debug the selected device using J-Link or J-Link OB debugger by default.

A Debug session can be started or stopped by selecting the menu item **Debug > Start/Stop Debug Session** or keyboard shortcut CTRL+F5. When debugging for the first time, J-Link firmware update may be needed if requested by the tool.

Refer to the documentation from Keil to get more information on the debug features in uVision. Note that not all features supported by uVision debugger are implemented in the J-Link interface. Consult SEGGER J-Link documentation for more information.

### 2.6.2.5 Notes and Restrictions

1. When creating a new RA project, do not create a new project directly inside uVision. Follow the steps as mentioned in [Create new RA project](#)
2. RA FSP contains a full set of drivers and middleware and may not be compatible with other CMSIS packs from Keil, Arm or third parties.
3. Flash programming is currently only supported through the debugger connection.

### 2.6.3 Using RA Smart Configurator with IAR EWARM

IAR Systems Embedded Workbench for Arm (EWARM) includes support for Renesas RA devices.



These can be set up as bare metal designs within EWARM. However, most RA developers will want to integrate RA FSP drivers and middleware into their designs. RA SC will facilitate this.

RA SC generates a "Project Connection" file that can be loaded directly into EWARM to update project files.

### 2.6.3.1 Prerequisites

- IAR EWARM installed and licensed. Please refer to the Release notes for the version to be installed.
- RA SC and FSP Installed

### 2.6.3.2 Create new RA project

The following steps are required to create an RA project using IAR EWARM, RA SC and FSP:

1. To Use RA SC with EWARM, RA SC needs to be configured as a tool in EWARM by selecting the menu item **Tools > Configure Tools...**. Select **New** to create a new tool in the dialog shown and add the following information:
  - Menu Text: RA Smart Configurator
  - Command: Select Browse... and navigate to rasc.exe in the installed RA SC
  - Argument: --compiler IAR configuration.xml
  - Initial Directory: \$PROJ\_DIR\$
  - Tool Available: Always

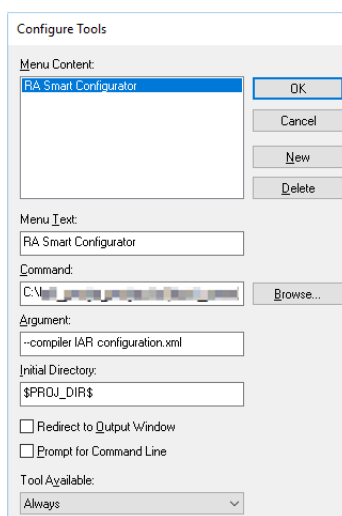


Figure 135: Tool\_setup

2. A new EWARM project can be created using the menu item **Project > Create New Project...** and selecting the **Empty Project** and toolchain as Arm. Save the project to an empty folder.
3. RA SC can now be launched from EWARM using the menu item **Tools > RA Smart Configurator**.

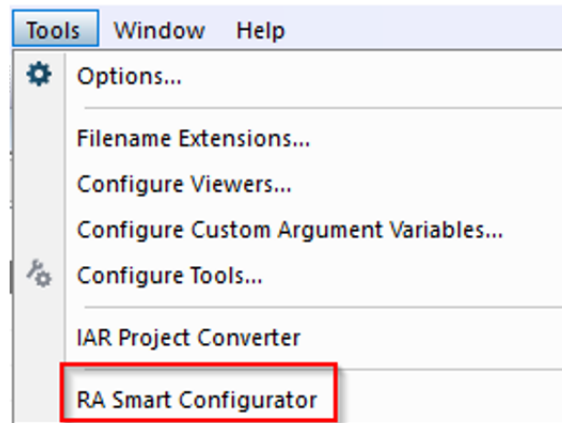


Figure 136: RA SC Menu Item

RA SC will be launched with project generator wizard. The configuration window opens once the project wizard is closed. Refer to [Configuring a Project](#) for more details on how to configure the project. After configuring the project, click **Generate Project Content**. Changes to the RA configuration will be reflected in the EWARM project.

4. A Project connection needs to be set up in EWARM to build the project. Select **Project > Add Project Connection** in EWARM and select **IAR Project Connection**. Navigate to the project folder and select buildinfo.ipcf and click open. The project can now build in EWARM.

# Chapter 3 FSP Architecture

## 3.1 FSP Architecture Overview

This guide describes the Renesas Flexible Software Package (FSP) architecture and how to use the FSP Application Programming Interface (API).

### 3.1.1 C99 Use

The FSP uses the ISO/IEC 9899:1999 (C99) C programming language standard. Specific features introduced in C99 that are used include standard integer types (`stdint.h`), booleans (`stdbool.h`), designated initializers, and the ability to intermingle declarations and code.

### 3.1.2 Doxygen

Doxygen is the default documentation tool used by FSP. You can find Doxygen comments throughout the FSP source.

### 3.1.3 Weak Symbols

Weak symbols are used occasionally in the FSP. They are used to ensure that a project builds even when the user has not defined an optional function.

### 3.1.4 Memory Allocation

Dynamic memory allocation through use of the `malloc()` and `free()` functions are not used in FSP modules; all memory required by FSP modules is allocated in the application and passed to the module in a pointer. Exceptions are considered only for ports of 3rd party code that require dynamic memory.

### 3.1.5 FSP Terms

Term	Description	Reference
BSP	Short for Board Support Package. In the FSP the BSP provides just enough foundation to allow other FSP modules to work together without issue.	<a href="#">MCU Board Support Package</a>

Module	Modules can be peripheral drivers, purely software, or anything in between. Each module consists of a folder with source code, documentation, and anything else that the customer needs to use the code effectively. Modules are independent units, but they may depend on other modules. Applications can be built by combining multiple modules to provide the user with the features they need.	<a href="#">FSP Modules</a>
Driver	A driver is a specific kind of module that directly modifies registers on the MCU.	-
Interface	An interface contains API definitions that can be shared by modules with similar features. Interfaces are definitions only and do not add to code size.	<a href="#">FSP Interfaces</a>
Stacks	The FSP architecture is designed such that modules work together to form a stack. A stack consists of a top level module and all its dependencies.	<a href="#">FSP Stacks</a>
Module Instance	Single and independent instantiation of a module. An application may require two GPT timers. Each of these timers is a module instance of the r_gpt module.	-
Application	Code that is owned and maintained by the user. Application code may be based on sample application code provided by Renesas, but it is the responsibility of the user to maintain as necessary.	-

Callback Function	This term refers to a function that is called when an event occurs. As an example, suppose the user would like to be notified every second based on the RTC. As part of the RTC configuration, a callback function can be supplied that will be jumped to during each RTC interrupt. When a single callback services multiple events, the arguments contain the triggering event. Callback functions for interrupts should be kept short and handled carefully because when they are called the MCU is still inside of an interrupt, delaying any pending interrupts.	-
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## 3.2 FSP Modules

Modules are the core building block of FSP. Modules can do many different things, but all modules share the basic concept of providing functionality upwards and requiring functionality from below.

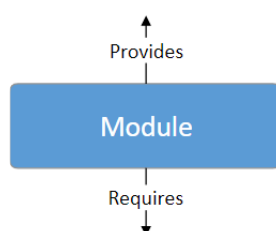


Figure 137: Modules

The amount of functionality provided by a module is determined based on functional use cases. Common functionality required by multiple modules is often placed into a self-contained submodule so it can be reused. Code size, speed and complexity are also considered when defining a module.

The simplest FSP application consists of one module with the Board Support Package (BSP) and the user application on top.

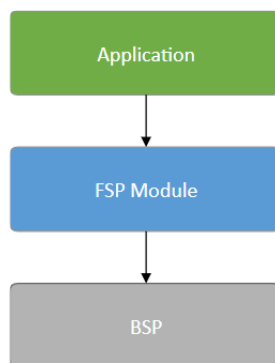


Figure 138: Module with application

The Board Support Package (BSP) is the foundation for FSP modules, providing functionality to determine the MCU used as well as configuring clocks, interrupts and pins. For the sake of clarity, the BSP will be omitted from further diagrams.

### 3.3 FSP Stacks

When modules are layered atop one another, an FSP stack is formed. The stacking process is performed by matching what one module provides with what another module requires. For example, the SPI module ([Serial Peripheral Interface \(r\\_spi\)](#)) requires a module that provides the transfer interface ([Transfer Interface](#)) to send or receive data without a CPU interrupt. The transfer interface requirement can be fulfilled by the DTC driver module ([Data Transfer Controller \(r\\_dtc\)](#)).

Through this methodology the same code can be shared by several modules simultaneously. The example below illustrates how the same DTC module can be used with SPI ([Serial Peripheral Interface \(r\\_spi\)](#)), UART ([Serial Communications Interface \(SCI\) UART \(r\\_sci\\_uart\)](#)) and SDHI ([SD/MMC Host Interface \(r\\_sdhi\)](#)).

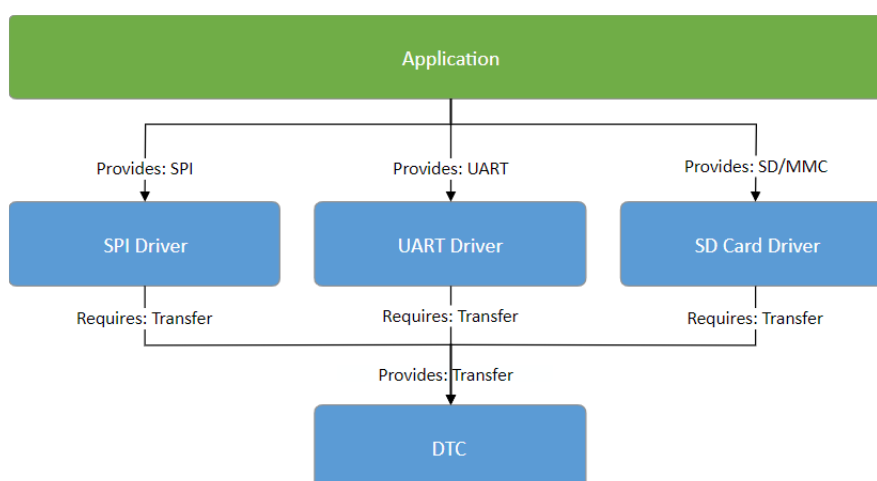


Figure 139: Stacks -- Shared DTC Module

The ability to stack modules ensures the flexibility of the architecture as a whole. If multiple modules include the same functionality issues arise when application features must work across different user designs. To ensure that modules are reusable, any dependent modules must be capable of being swapped out for other modules that provide the same features. The FSP

architecture provides this flexibility to swap modules in and out through the use of FSP interfaces.

## 3.4 FSP Interfaces

At the architecture level, interfaces are the way that modules provide common features. This commonality allows modules that adhere to the same interface to be used interchangeably. Interfaces can be thought of as a contract between two modules - the modules agree to work together using the information that was established in the contract.

On RA hardware there is occasionally an overlap of features between different peripherals. For example, I2C communications can be achieved through use of the IIC peripheral or the SCI peripheral. However, there is a difference in the level of features provided by both peripherals; in I2C mode the SCI peripheral will only support a subset of the capabilities of the fully-featured IIC.

Interfaces aim to provide support for the common features that most users would expect. This means that some of the advanced features of a peripheral (such as IIC) might not be available in the interface. In most cases these features are still available through interface extensions.

In FSP design, interfaces are defined in header files. All interface header files are located in the folder `ra/fsp/inc/api` and end with `*_api.h`. Interface extensions are defined in header files in the folder `ra/fsp/inc/instances`. The following sections detail what makes up an interface.

### 3.4.1 FSP Interface Enumerations

Whenever possible, interfaces use typed enumerations for function parameters and structure members.

```
typedef enum e_i2c_master_addr_mode
{
    I2C_MASTER_ADDR_MODE_7BIT = 1,    ///< Use 7-bit addressing mode
    I2C_MASTER_ADDR_MODE_10BIT = 2,   ///< Use 10-bit addressing mode
} i2c_master_addr_mode_t;
```

Enumerations remove uncertainty when deciding what values are available for a parameter. FSP enumeration options follow a strict naming convention where the name of the type is prefixed on the available options. Combining the naming convention with the autocomplete feature available in e2 studio (Ctrl + Space) provides the benefits of rapid coding while maintaining high readability.

### 3.4.2 FSP Interface Callback Functions

Callback functions allow modules to asynchronously alert the user application when an event has occurred, such as when a byte has been received over a UART channel or an IRQ pin is toggled. FSP driver modules define and handle the interrupt service routines for RA MCU peripherals to ensure any required hardware procedures are implemented. The interrupt service routines in FSP modules then call the user-defined callbacks to allow the application to respond.

Callback functions must be defined in the user application. They always return void and take a structure for their one parameter. The structure is defined in the interface for the module and is named `<interface>_callback_args_t`. The contents of the structure may vary depending on the

interface, but two members are common: event and p\_context.

The event member is an enumeration defined in the interface used by the application to determine why the callback was called. Using the UART example, the callback could be triggered for many different reasons, including when a byte is received, all bytes have been transmitted, or a framing error has occurred. The event member allows the application to determine which of these three events has occurred and handle it appropriately.

The p\_context member is used for providing user-specified data to the callback function. In many cases a callback function is shared between multiple channels or module instances; when the callback occurs, the code handling the callback needs context information so that it can determine which module instance the callback is for. For example, if the callback wanted to make an FSP API call in the callback, then at a minimum the callback will need a reference to the relevant control structure. To make this easy, the user can provide a pointer to the control structure as the p\_context. When the callback occurs, the control structure is passed in the p\_context element of the callback structure.

Callback functions are called from within an interrupt service routine. For this reason callback functions should be kept as short as possible so they do not affect the real time performance of the user's system. An example skeleton function for the flash interface callback is shown below.

```
void flash_callback (flash_callback_args_t * p_args)
{
    /* See what event caused this callback. */
    switch (p_args->event)
    {
        case FLASH_EVENT_ERASE_COMPLETE:
            {
                /* Handle event. */
                break;
            }
        case FLASH_EVENT_WRITE_COMPLETE:
            {
                /* Handle event. */
                break;
            }
        case FLASH_EVENT_BLANK:
            {
                /* Handle event. */
                break;
            }
        case FLASH_EVENT_NOT_BLANK:
```



```
    {  
    /* Handle event. */  
    break;  
    }  
    case FLASH_EVENT_ERR_DF_ACCESS:  
    {  
    /* Handle error. */  
    break;  
    }  
    case FLASH_EVENT_ERR_CF_ACCESS:  
    {  
    /* Handle error. */  
    break;  
    }  
    case FLASH_EVENT_ERR_CMD_LOCKED:  
    {  
    /* Handle error. */  
    break;  
    }  
    case FLASH_EVENT_ERR_FAILURE:  
    {  
    /* Handle error. */  
    break;  
    }  
    case FLASH_EVENT_ERR_ONE_BIT:  
    {  
    /* Handle error. */  
    break;  
    }  
    }  
}
```

When a module is not directly used in the user application (that is, it is not the top layer of the stack), its callback function will be handled by the module above. For example, if a module requires

a UART interface module the upper layer module will control and use the UART's callback function. In this case the user would not need to create a callback function for the UART module in their application code.

### 3.4.3 FSP Interface Data Structures

At a minimum, all FSP interfaces include three data structures: a configuration structure, an API structure, and an instance structure.

#### 3.4.3.1 FSP Interface Configuration Structure

The configuration structure is used for the initial configuration of a module during the <MODULE>\_Open() call. The structure consists of members such as channel number, bitrate, and operating mode.

The configuration structure is used purely as an input into the module. It may be stored and referenced by the module, so the configuration structure and anything it references must persist as long as the module is open.

The configuration structure is allocated for each module instance in files generated by the RA Configuration editor.

When FSP stacks are used, it is also important to understand that configuration structures only have members that apply to the current interface. If multiple layers in the same stack define the same configuration parameters then it becomes difficult to know where to modify the option. For example, the baud rate for a UART is only defined in the UART module instance. Any modules that use the UART interface rely on the baud rate being provided in the UART module instance and do not offer it in their own configuration structures.

#### 3.4.3.2 FSP Interface API Structure

All interfaces include an API structure which contains function pointers for all the supported interface functions. An example structure for the [Digital to Analog Converter \(r\\_dac\)](#) is shown below.

```
typedef struct st_dac_api
{
    /** Initial configuration.
     * @par Implemented as
     * - @ref R_DAC_Open()
     * - @ref R_DAC8_Open()
     *
     * @param[in] p_ctrl Pointer to control block. Must be declared by user. Elements
set here.
     * @param[in] p_cfg Pointer to configuration structure. All elements of this
structure must be set by user.
     */
    fsp_err_t (* open)(dac_ctrl_t * const p_ctrl, dac_cfg_t const * const p_cfg);
}
```

```
/** Close the D/A Converter.
 * @par Implemented as
 * - @ref R_DAC_Close()
 * - @ref R_DAC8_Close()
 *
 * @param[in] p_ctrl Control block set in @ref dac_api_t::open call for this
timer.
 */
fsp_err_t (* close)(dac_ctrl_t * const p_ctrl);
/** Write sample value to the D/A Converter.
 * @par Implemented as
 * - @ref R_DAC_Write()
 * - @ref R_DAC8_Write()
 *
 * @param[in] p_ctrl Control block set in @ref dac_api_t::open call for this
timer.
 * @param[in] value Sample value to be written to the D/A Converter.
 */
fsp_err_t (* write)(dac_ctrl_t * const p_ctrl, uint16_t value);
/** Start the D/A Converter if it has not been started yet.
 * @par Implemented as
 * - @ref R_DAC_Start()
 * - @ref R_DAC8_Start()
 *
 * @param[in] p_ctrl Control block set in @ref dac_api_t::open call for this
timer.
 */
fsp_err_t (* start)(dac_ctrl_t * const p_ctrl);
/** Stop the D/A Converter if the converter is running.
 * @par Implemented as
 * - @ref R_DAC_Stop()
 * - @ref R_DAC8_Stop()
 *
 * @param[in] p_ctrl Control block set in @ref dac_api_t::open call for this
```

```
timer.  
    */  
    fsp_err_t (* stop)(dac_ctrl_t * const p_ctrl);  
    /** Get version and store it in provided pointer p_version.  
    * @par Implemented as  
    * - @ref R_DAC_VersionGet()  
    * - @ref R_DAC8_VersionGet()  
    *  
    * @param[out] p_version Code and API version used.  
    */  
    fsp_err_t (* versionGet)(fsp_version_t * p_version);  
} dac_api_t;
```

The API structure is what allows for modules to easily be swapped in and out for other modules that are instances of the same interface. Let's look at an example application using the DAC interface above.

RA MCUs have an internal DAC peripheral. If the DAC API structure in the DAC interface is not used the application can make calls directly into the module. In the example below the application is making calls to the [R\\_DAC\\_Write\(\)](#) function which is provided in the `r_dac` module.

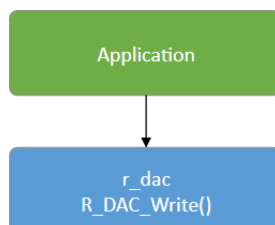


Figure 140: DAC Write example

Now let's assume that the user needs more DAC channels than are available on the MCU and decides to add an external DAC module named `dac_external` using I2C for communications. The application must now distinguish between the two modules, adding complexity and further dependencies to the application.

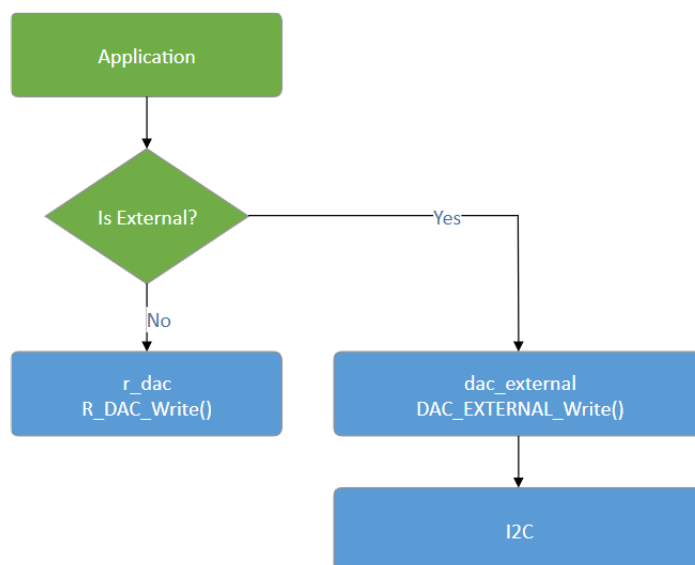


Figure 141: DAC Write with two write modules

The use of interfaces and the API structure allows for the use of an abstracted DAC. This means that no extra logic is needed if the user's `dac_external` module implements the FSP DAC interface, so the application no longer depends upon hard-coded module function names. Instead the application now depends on the DAC interface API which can be implemented by any number of modules.

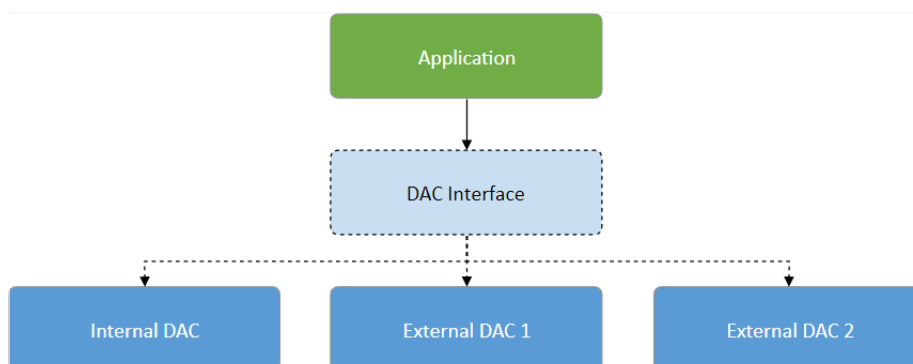


Figure 142: DAC Interface

### 3.4.3.3 FSP Interface Instance Structure

Every FSP interface also has an instance structure. The instance structure encapsulates everything required to use the module:

- A pointer to the instance API structure ([FSP Instance API](#))
- A pointer to the configuration structure
- A pointer to the control structure

The instance structure is not required at the application layer. It is used to connect modules to their dependencies (other than the BSP).

Instance structures have a standardized name of `<interface>_instance_t`. An example from the [Transfer Interface](#) is shown below.

```
typedef struct st_transfer_instance
{
    transfer_ctrl_t      * p_ctrl; ///< Pointer to the control structure for this
instance
    transfer_cfg_t const * p_cfg;   ///< Pointer to the configuration structure
for this instance
    transfer_api_t const * p_api;   ///< Pointer to the API structure for this
instance
} transfer_instance_t;
```

Note that when an instance structure variable is declared, the API is the only thing that is instance specific, not *module instance* specific. This is because all module instances of the same module share the same underlying module source code. If SPI is being used on SCI channels 0 and 2 then both module instances use the same API while the configuration and control structures are typically different.

## 3.5 FSP Instances

While interfaces dictate the features that are provided, instances actually implement those features. Each instance is tied to a specific interface. Instances use the enumerations, data structures, and API prototypes from the interface. This allows an application that uses an interface to swap out the instance when needed.

On RA MCUs some peripherals are used to implement multiple interfaces. In the example below the IIC and SPI peripherals map to only one interface each while the SCI peripheral implements three interfaces.

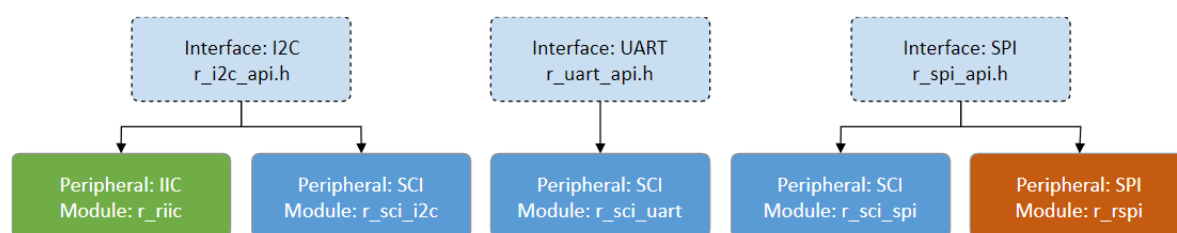


Figure 143: Instances

In FSP design, instances consist of the interface extension and API defined in the instance header file located in the folder `ra/fsp/inc/instances` and the module source `ra/fsp/src/<module>`.

### 3.5.1 FSP Instance Control Structure

The control structure is used as a unique identifier for the module instance and contains memory required by the module. Elements in the control structure are owned by the module and *must not be modified* by the application. The user allocates storage for a control structure, often as a global variable, then sends a pointer to it into the `<MODULE>_Open()` call for a module. At this point, the

module initializes the structure as needed. The user must then send in a pointer to the control structure for all subsequent module calls.

## 3.5.2 FSP Interface Extensions

In some cases, instances require more information than is provided in the interface. This situation can occur in the following cases:

- An instance offers extra features that are not common to most instances of the interface. An example of this is the start source selection of the GPT ([General PWM Timer \(r\\_gpt\)](#)). The GPT can be configured to start based on hardware events such as a falling edge on a trigger pin. This feature is not common to all timers, so it is included in the GPT instance.
- An interface must be very generic out of necessity. As an interface becomes more generic, the number of possible instances increases. An example of an interface that must be generic is a block media interface that abstracts functions required by a file system. Possible instances include SD card, SPI Flash, SDRAM, USB, and many more.

The `p_extend` member provides this extension function.

Use of interface extensions is not always necessary. Some instances do not offer an extension since all functionality is provided in the interface. In these cases the `p_extend` member can be set to `NULL`. The documentation for each instance indicates whether an interface extension is available and whether it is mandatory or optional.

### 3.5.2.1 FSP Extended Configuration Structure

When extended configuration is required it can be supplied through the `p_extend` parameter of the interface configuration structure.

The extended configuration structure is part of the instance, but it is also still considered to be part of the configuration structure. All usage notes about the configuration structure described in [FSP Interface Configuration Structure](#) apply to the extended configuration structure as well.

The extended configuration structure and all typed structures and enumerations required to define it make up the interface extension.

## 3.5.3 FSP Instance API

Each instance includes a constant global variable tying the interface API functions to the functions provided by the module. The name of this structure is standardized as `g_<interface>_on_<instance>`. Examples include `g_spi_on_spi`, `g_transfer_on_dtc`, and `g_adc_on_adc`. This structure is available to be used through an extern in the instance header file (`r_spi.h`, `r_dtc.h`, and `r_adc.h` respectively).

## 3.6 FSP API Standards

### 3.6.1 FSP Function Names

FSP functions start with the uppercase module name (`<MODULE>`). All modules have `<MODULE>_Open()` and `<MODULE>_Close()` functions. The `<MODULE>_Open()` function must be called before any of the other functions. The only exception is the `<MODULE>_VersionGet()` function which is not dependent upon any user provided information.

Other functions that will commonly be found are `<MODULE>_Read()`, `<MODULE>_Write()`,

<MODULE>\_InfoGet(), and <MODULE>\_StatusGet(). The <MODULE>\_StatusGet() function provides a status that could change asynchronously, while <MODULE>\_InfoGet() provides information that cannot change after open or can only be updated by API calls. Example function names include:

- R\_SPI\_Read(), R\_SPI\_Write(), R\_SPI\_WriteRead()
- R\_SDHI\_StatusGet()
- R\_RTC\_CalendarAlarmSet(), R\_RTC\_CalendarAlarmGet()
- R\_FLASH\_HP\_AccessWindowSet(), R\_FLASH\_HP\_AccessWindowClear()

### 3.6.2 Use of const in API parameters

The const qualifier is used with API parameters whenever possible. An example case is shown below.

```
fsp_err_t R_FLASH_HP_Open(flash_ctrl_t * const p_api_ctrl, flash_cfg_t const * const
p_cfg);
```

In this example, `flash_cfg_t` is a structure of configuration parameters for the `r_flash_hp` module. The parameter `p_cfg` is a pointer to this structure. The first const qualifier on `p_cfg` ensures the `flash_cfg_t` structure cannot be modified by `R_FLASH_HP_Open()`. This allows the structure to be allocated as a const variable and stored in ROM instead of RAM.

The const qualifier after the pointer star for both `p_ctrl` and `p_cfg` ensures the FSP function does not modify the input pointer addresses. While not fool-proof by any means this does provide some extra checking inside the FSP code to ensure that arguments that should not be altered are treated as such.

### 3.6.3 FSP Version Information

All instances supply a <MODULE>\_VersionGet() function which fills in a structure of type `fsp_version_t`. This structure is made up of two version numbers: one for the interface (the API) and one for the underlying instance that is currently being used.

```
typedef union st_fsp_version
{
    /** Version id */
    uint32_t version_id;
    /** Code version parameters */
    struct
    {
        uint8_t code_version_minor;    ///< Code minor version
        uint8_t code_version_major;    ///< Code major version
        uint8_t api_version_minor;     ///< API minor version
        uint8_t api_version_major;     ///< API major version
    };
};
```



```
} fsp_version_t;
```

The API version ideally never changes, and only rarely if it does. A change to the API may require users to go back and modify their code. The code version (the version of the current instance) may be updated more frequently due to bug fixes, enhancements, and additional features. Changes to the code version typically do not require changes to user code.

## 3.7 FSP Build Time Configurations

All modules have a build-time configuration header file. Most configuration options are supplied at run time, though options that are rarely used or apply to all instances of a module may be moved to build time. The advantage of using a build-time configuration option is to potentially reduce code size reduction by removing an unused feature.

All modules have a build time option to enable or disable parameter checking for the module. FSP modules check function arguments for validity when possible, though this feature is disabled by default to reduce code size. Enabling it can help catch parameter errors during development and debugging. By default, each module's parameter checking configuration inherits the BSP parameter checking setting (set on the BSP tab of the RA Configuration editor). Leaving each module's parameter checking configuration set to Default (BSP) allows parameter checking to be enabled or disabled globally in all FSP code through the parameter checking setting on the BSP tab.

If an error condition can reasonably be avoided it is only checked in a section of code that can be disabled by disabling parameter checking. Most FSP APIs can only return FSP\_SUCCESS if parameter checking is disabled. An example of an error that cannot be reasonably avoided is the "bus busy" error that occurs when another master is using an I2C bus. This type of error can be returned even if parameter checking is disabled.

## 3.8 FSP File Structure

The high-level file structure of an FSP project is shown below.

```
ra_gen
ra
+---fsp
    +---inc
    |   +---api
    |   \---instances
    \---src
        +---bsp
        \---r_module
ra_cfg
+---fsp_cfg
    +---bsp
```

```
+---driver
```

Directly underneath the base ra folder the folders are split into the source and include folders. Include folders are kept separate from the source for easy browsing and easy setup of include paths.

The ra\_gen folder contains code generated by the RA Configuration editor. This includes global variables for the control structure and configuration structure for each module.

The ra\_cfg folder is where configuration header files are stored for each module. See [FSP Build Time Configurations](#) for information on what is provided in these header files.

## 3.9 FSP TrustZone Support

TrustZone support for FSP is primarily handled in the RA Configuration Tool.

### 3.9.1 FSP TrustZone Projects

During development of a TrustZone project, users create an RA TrustZone Secure Project first, followed by an RA TrustZone Non-secure Project that is linked to the RA TrustZone Secure Project. Allocation of secure memory is handled automatically within the tooling. The non-secure project starts at the required alignment boundary beyond the memory taken by the secure project.

### 3.9.2 Non-Secure Callable Guard Functions

The tooling generates guard functions for any module marked as Non-secure Callable. These guard functions are owned by the application once generated, so they can be modified as necessary by the secure application developer.

The default non-secure callable guard functions limit the configuration and control structure to the structures generated in the secure project. They also check any input pointers to ensure the caller does not overwrite secure memory.

### 3.9.3 Callbacks in Non-Secure from Non-Secure Callable Modules

If the non-secure project needs a callback function from a non-secure callable module, the callback can be registered after the module is opened using the `callback_set()` guard function.

## 3.10 FSP Architecture in Practice

### 3.10.1 FSP Connecting Layers

FSP modules are meant to be both reusable and stackable. It is important to remember that modules are not dependent upon other modules, but upon other interfaces. The user is then free to fulfill the interface using the instance that best fits their needs.

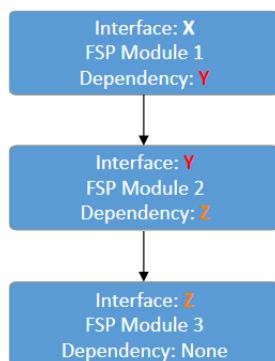


Figure 144: Connecting layers

In the image above interface Y is a dependency of interface X and has its own dependency on interface Z. Interface X only has a dependency on interface Y. Interface X has no knowledge of interface Z. This is a requirement for ensuring that layers can easily be swapped out.

### 3.10.2 Using FSP Modules in an Application

The typical use of an FSP module involves generating required module data then using the API in the application.

#### 3.10.2.1 Create a Module Instance in the RA Configuration Editor

The RA Configuration editor (available both in the Renesas e2 studio IDE as well as through the standalone RA Smart Configurator) provides a graphical user interface for setting the parameters of the interface and instance configuration structures. It also automatically includes those structures (once they are configured in the GUI) in application-specific header files that can be included in application code.

The RA Configuration editor allocates storage for the control structures, all required configuration structures, and the instance structure in generated files in the `ra_gen` folder. Use the **Properties** window to set the values for the members of the configuration structures as needed. Refer to the Configuration section of the module usage notes for documentation about the configuration options.

If the interface has a callback function option then the application must declare and define the function. The return value is always of type `void` and the parameter to the function is a typed structure of name `<interface>_callback_args_t`. Once the function has been defined, assign its name to the `p_callback` member of the configuration structure. Callback function names can be assigned through the **Properties** window for the selected module.

#### 3.10.2.2 Use the Instance API in the Application

Call the module's `<MODULE>_Open()` function. Pass pointers to the generated control structure and configuration structure. The names of these structures are based on the 'Name' field provided in the configuration editor. The control structure is `<Name>_ctrl` and the configuration structure is `<Name>_cfg`. An example `<MODULE>_Open()` call for an `r_rtc` module instance named `g_clock` is:

```
R_RTC_Open(&g_clock_ctrl, &g_clock_cfg);
```

*Note*

*Each layer in the FSP Stack is responsible for calling the API functions of its dependencies. This means that users are only responsible for calling the API functions at the layer at which they are interfacing. Using the example above of a SPI module with a DTC dependency, the application uses only SPI APIs. The application starts by calling `R_SPI_Open()`. Internally, the SPI module opens the DTC. It locates `R_DTC_Open()` by accessing the dependent transfer interface function pointers from the pointers DTC instances (`spi_cfg_t::p_transfer_tx` and `spi_cfg_t::p_transfer_rx`) to open the DTC.*

Refer to the module usage notes for example code to help get started with any particular module.

# Chapter 4 API Reference

This section includes the FSP API Reference for the Module and Interface level functions.

- ▶ [BSP](#) Common code shared by FSP drivers
- ▶ [Modules](#) Modules are the smallest unit of software available in the FSP. Each module implements one interface
- ▶ [Interfaces](#) The FSP interfaces provide APIs for common functionality. They can be implemented by one or more modules. Modules can use other modules as dependencies using this interface layer

## 4.1 BSP

### Detailed Description

Common code shared by FSP drivers.

#### Modules

##### [Common Error Codes](#)

##### [MCU Board Support Package](#)

The BSP is responsible for getting the MCU from reset to the user's application. Before reaching the user's application, the BSP sets up the stacks, heap, clocks, interrupts, C runtime environment, and stack monitor.

##### [BSP I/O access](#)

This module provides basic read/write access to port pins.

#### Data Structures

union [fsp\\_pack\\_version\\_t](#)

struct [fsp\\_pack\\_version\\_t.\\_\\_unnamed\\_\\_](#)

#### Macros

```
#define FSP_VERSION_MAJOR
```

```
#define FSP_VERSION_MINOR
```

```
#define FSP_VERSION_PATCH
```

```
#define FSP_VERSION_BUILD
```

```
#define FSP_VERSION_STRING
```

```
#define FSP_VERSION_BUILD_STRING
```

## Data Structure Documentation

### ◆ fsp\_pack\_version\_t

union fsp_pack_version_t		
FSP Pack version structure		
Data Fields		
uint32_t	version_id	Version id
struct fsp_pack_version_t	__unnamed__	Code version parameters, little endian order.

### ◆ fsp\_pack\_version\_t.\_\_unnamed\_\_

struct fsp_pack_version_t.__unnamed__		
Code version parameters, little endian order.		
Data Fields		
uint8_t	build	Build version of FSP Pack.
uint8_t	patch	Patch version of FSP Pack.
uint8_t	minor	Minor version of FSP Pack.
uint8_t	major	Major version of FSP Pack.

## Macro Definition Documentation

### ◆ FSP\_VERSION\_MAJOR

#define FSP_VERSION_MAJOR
FSP pack major version.

### ◆ FSP\_VERSION\_MINOR

```
#define FSP_VERSION_MINOR
```

FSP pack minor version.

### ◆ FSP\_VERSION\_PATCH

```
#define FSP_VERSION_PATCH
```

FSP pack patch version.

### ◆ FSP\_VERSION\_BUILD

```
#define FSP_VERSION_BUILD
```

FSP pack version build number (currently unused).

### ◆ FSP\_VERSION\_STRING

```
#define FSP_VERSION_STRING
```

Public FSP version name.

### ◆ FSP\_VERSION\_BUILD\_STRING

```
#define FSP_VERSION_BUILD_STRING
```

Unique FSP version ID.

## 4.1.1 Common Error Codes

### BSP

#### Detailed Description

All FSP modules share these common error codes.

#### Data Structures

```
union fsp_version_t
```

```
struct fsp_version_t.__unnamed__
```

## Macros

```
#define FSP_PARAMETER_NOT_USED(p)
```

```
#define FSP_CPP_HEADER
```

```
#define FSP_HEADER
```

```
#define FSP_SECURE_ARGUMENT
```

## Enumerations

```
enum fsp_err_t
```

## Data Structure Documentation

### ◆ fsp\_version\_t

union fsp_version_t		
Common version structure		
Data Fields		
uint32_t	version_id	Version id
struct fsp_version_t	__unnamed__	Code version parameters

### ◆ fsp\_version\_t.\_\_unnamed\_\_

struct fsp_version_t.__unnamed__		
Code version parameters		
Data Fields		
uint8_t	code_version_minor	Code minor version.
uint8_t	code_version_major	Code major version.
uint8_t	api_version_minor	API minor version.
uint8_t	api_version_major	API major version.

## Macro Definition Documentation

### ◆ FSP\_PARAMETER\_NOT\_USED

```
#define FSP_PARAMETER_NOT_USED ( p)
```

This macro is used to suppress compiler messages about a parameter not being used in a function. The nice thing about using this implementation is that it does not take any extra RAM or ROM.



◆ **FSP\_CPP\_HEADER**

```
#define FSP_CPP_HEADER
```

Determine if a C++ compiler is being used. If so, ensure that standard C is used to process the API information.

◆ **FSP\_HEADER**

```
#define FSP_HEADER
```

FSP Header and Footer definitions

◆ **FSP\_SECURE\_ARGUMENT**

```
#define FSP_SECURE_ARGUMENT
```

Macro to be used when argument to function is ignored since function call is NSC and the parameter is statically defined on the Secure side.

**Enumeration Type Documentation**◆ **fsp\_err\_t**

```
enum fsp_err_t
```

Common error codes

Enumerator

FSP_ERR_ASSERTION	A critical assertion has failed.
FSP_ERR_INVALID_POINTER	Pointer points to invalid memory location.
FSP_ERR_INVALID_ARGUMENT	Invalid input parameter.
FSP_ERR_INVALID_CHANNEL	Selected channel does not exist.
FSP_ERR_INVALID_MODE	Unsupported or incorrect mode.
FSP_ERR_UNSUPPORTED	Selected mode not supported by this API.
FSP_ERR_NOT_OPEN	Requested channel is not configured or API not open.
FSP_ERR_IN_USE	Channel/peripheral is running/busy.
FSP_ERR_OUT_OF_MEMORY	Allocate more memory in the driver's cfg.h.

FSP_ERR_HW_LOCKED	Hardware is locked.
FSP_ERR_IRQ_BSP_DISABLED	IRQ not enabled in BSP.
FSP_ERR_OVERFLOW	Hardware overflow.
FSP_ERR_UNDERFLOW	Hardware underflow.
FSP_ERR_ALREADY_OPEN	Requested channel is already open in a different configuration.
FSP_ERR_APPROXIMATION	Could not set value to exact result.
FSP_ERR_CLAMPED	Value had to be limited for some reason.
FSP_ERR_INVALID_RATE	Selected rate could not be met.
FSP_ERR_ABORTED	An operation was aborted.
FSP_ERR_NOT_ENABLED	Requested operation is not enabled.
FSP_ERR_TIMEOUT	Timeout error.
FSP_ERR_INVALID_BLOCKS	Invalid number of blocks supplied.
FSP_ERR_INVALID_ADDRESS	Invalid address supplied.
FSP_ERR_INVALID_SIZE	Invalid size/length supplied for operation.
FSP_ERR_WRITE_FAILED	Write operation failed.
FSP_ERR_ERASE_FAILED	Erase operation failed.
FSP_ERR_INVALID_CALL	Invalid function call is made.
FSP_ERR_INVALID_HW_CONDITION	Detected hardware is in invalid condition.
FSP_ERR_INVALID_FACTORY_FLASH	Factory flash is not available on this MCU.
FSP_ERR_INVALID_STATE	API or command not valid in the current state.
FSP_ERR_NOT_ERASED	Erase verification failed.
FSP_ERR_SECTOR_RELEASE_FAILED	Sector release failed.
FSP_ERR_NOT_INITIALIZED	Required initialization not complete.
FSP_ERR_NOT_FOUND	The requested item could not be found.

FSP_ERR_NO_CALLBACK_MEMORY	Non-secure callback memory not provided for non-secure callback.
FSP_ERR_INTERNAL	Internal error.
FSP_ERR_WAIT_ABORTED	Wait aborted.
FSP_ERR_FRAMING	Framing error occurs.
FSP_ERR_BREAK_DETECT	Break signal detects.
FSP_ERR_PARITY	Parity error occurs.
FSP_ERR_RXBUF_OVERFLOW	Receive queue overflow.
FSP_ERR_QUEUE_UNAVAILABLE	Can't open s/w queue.
FSP_ERR_INSUFFICIENT_SPACE	Not enough space in transmission circular buffer.
FSP_ERR_INSUFFICIENT_DATA	Not enough data in receive circular buffer.
FSP_ERR_TRANSFER_ABORTED	The data transfer was aborted.
FSP_ERR_MODE_FAULT	Mode fault error.
FSP_ERR_READ_OVERFLOW	Read overflow.
FSP_ERR_SPI_PARITY	Parity error.
FSP_ERR_OVERRUN	Overrun error.
FSP_ERR_CLOCK_INACTIVE	Inactive clock specified as system clock.
FSP_ERR_CLOCK_ACTIVE	Active clock source cannot be modified without stopping first.
FSP_ERR_NOT_STABILIZED	Clock has not stabilized after its been turned on/off.
FSP_ERR_PLL_SRC_INACTIVE	PLL initialization attempted when PLL source is turned off.
FSP_ERR_OSC_STOP_DET_ENABLED	Illegal attempt to stop LOCO when Oscillation stop is enabled.
FSP_ERR_OSC_STOP_DETECTED	The Oscillation stop detection status flag is set.

FSP_ERR_OSC_STOP_CLOCK_ACTIVE	Attempt to clear Oscillation Stop Detect Status with PLL/MAIN_OSC active.
FSP_ERR_CLKOUT_EXCEEDED	Output on target output clock pin exceeds maximum supported limit.
FSP_ERR_USB_MODULE_ENABLED	USB clock configure request with USB Module enabled.
FSP_ERR_HARDWARE_TIMEOUT	A register read or write timed out.
FSP_ERR_LOW_VOLTAGE_MODE	Invalid clock setting attempted in low voltage mode.
FSP_ERR_PE_FAILURE	Unable to enter Programming mode.
FSP_ERR_CMD_LOCKED	Peripheral in command locked state.
FSP_ERR_FCLK	FCLK must be $\geq 4$ MHz.
FSP_ERR_INVALID_LINKED_ADDRESS	Function or data are linked at an invalid region of memory.
FSP_ERR_BLANK_CHECK_FAILED	Blank check operation failed.
FSP_ERR_INVALID_CAC_REF_CLOCK	Measured clock rate < reference clock rate.
FSP_ERR_CLOCK_GENERATION	Clock cannot be specified as system clock.
FSP_ERR_INVALID_TIMING_SETTING	Invalid timing parameter.
FSP_ERR_INVALID_LAYER_SETTING	Invalid layer parameter.
FSP_ERR_INVALID_ALIGNMENT	Invalid memory alignment found.
FSP_ERR_INVALID_GAMMA_SETTING	Invalid gamma correction parameter.
FSP_ERR_INVALID_LAYER_FORMAT	Invalid color format in layer.
FSP_ERR_INVALID_UPDATE_TIMING	Invalid timing for register update.
FSP_ERR_INVALID_CLUT_ACCESS	Invalid access to CLUT entry.
FSP_ERR_INVALID_FADE_SETTING	Invalid fade-in/fade-out setting.
FSP_ERR_INVALID_BRIGHTNESS_SETTING	Invalid gamma correction parameter.
FSP_ERR_JPEG_ERR	JPEG error.

FSP_ERR_JPEG_SOI_NOT_DETECTED	SOI not detected until EOI detected.
FSP_ERR_JPEG_SOF1_TO_SOFF_DETECTED	SOF1 to SOFF detected.
FSP_ERR_JPEG_UNSUPPORTED_PIXEL_FORMAT	Unprovided pixel format detected.
FSP_ERR_JPEG_SOF_ACCURACY_ERROR	SOF accuracy error: other than 8 detected.
FSP_ERR_JPEG_DQT_ACCURACY_ERROR	DQT accuracy error: other than 0 detected.
FSP_ERR_JPEG_COMPONENT_ERROR1	Component error 1: the number of SOF0 header components detected is other than 1, 3, or 4.
FSP_ERR_JPEG_COMPONENT_ERROR2	Component error 2: the number of components differs between SOF0 header and SOS.
FSP_ERR_JPEG_SOF0_DQT_DHT_NOT_DETECTED	SOF0, DQT, and DHT not detected when SOS detected.
FSP_ERR_JPEG_SOS_NOT_DETECTED	SOS not detected: SOS not detected until EOI detected.
FSP_ERR_JPEG_EOI_NOT_DETECTED	EOI not detected (default)
FSP_ERR_JPEG_RESTART_INTERVAL_DATA_NUMBER_ERROR	Restart interval data number error detected.
FSP_ERR_JPEG_IMAGE_SIZE_ERROR	Image size error detected.
FSP_ERR_JPEG_LAST_MCU_DATA_NUMBER_ERROR	Last MCU data number error detected.
FSP_ERR_JPEG_BLOCK_DATA_NUMBER_ERROR	Block data number error detected.
FSP_ERR_JPEG_BUFFERSIZE_NOT_ENOUGH	User provided buffer size not enough.
FSP_ERR_JPEG_UNSUPPORTED_IMAGE_SIZE	JPEG Image size is not aligned with MCU.
FSP_ERR_CALIBRATE_FAILED	Calibration failed.
FSP_ERR_IP_HARDWARE_NOT_PRESENT	Requested IP does not exist on this device.
FSP_ERR_IP_UNIT_NOT_PRESENT	Requested unit does not exist on this device.
FSP_ERR_IP_CHANNEL_NOT_PRESENT	Requested channel does not exist on this device.
FSP_ERR_NO_MORE_BUFFER	No more buffer found in the memory block pool.

FSP_ERR_ILLEGAL_BUFFER_ADDRESS	Buffer address is out of block memory pool.
FSP_ERR_INVALID_WORKBUFFER_SIZE	Work buffer size is invalid.
FSP_ERR_INVALID_MSG_BUFFER_SIZE	Message buffer size is invalid.
FSP_ERR_TOO_MANY_BUFFERS	Number of buffer is too many.
FSP_ERR_NO_SUBSCRIBER_FOUND	No message subscriber found.
FSP_ERR_MESSAGE_QUEUE_EMPTY	No message found in the message queue.
FSP_ERR_MESSAGE_QUEUE_FULL	No room for new message in the message queue.
FSP_ERR_ILLEGAL_SUBSCRIBER_LISTS	Message subscriber lists is illegal.
FSP_ERR_BUFFER_RELEASED	Buffer has been released.
FSP_ERR_D2D_ERROR_INIT	D/AVE 2D has an error in the initialization.
FSP_ERR_D2D_ERROR_DEINIT	D/AVE 2D has an error in the initialization.
FSP_ERR_D2D_ERROR_RENDERING	D/AVE 2D has an error in the rendering.
FSP_ERR_D2D_ERROR_SIZE	D/AVE 2D has an error in the rendering.
FSP_ERR_ETHER_ERROR_NO_DATA	No Data in Receive buffer.
FSP_ERR_ETHER_ERROR_LINK	ETHERC/EDMAC has an error in the Auto-negotiation.
FSP_ERR_ETHER_ERROR_MAGIC_PACKET_MODE	As a Magic Packet is being detected, and transmission/reception is not enabled.
FSP_ERR_ETHER_ERROR_TRANSMIT_BUFFER_FULL	Transmit buffer is not empty.
FSP_ERR_ETHER_ERROR_FILTERING	Detect multicast frame when multicast frame filtering enable.
FSP_ERR_ETHER_ERROR_PHY_COMMUNICATION	ETHERC/EDMAC has an error in the phy communication.
FSP_ERR_ETHER_PHY_ERROR_LINK	PHY is not link up.
FSP_ERR_ETHER_PHY_NOT_READY	PHY has an error in the Auto-negotiation.
FSP_ERR_QUEUE_FULL	Queue is full, cannot queue another data.

FSP_ERR_QUEUE_EMPTY	Queue is empty, no data to dequeue.
FSP_ERR_CTSU_SCANNING	Scanning.
FSP_ERR_CTSU_NOT_GET_DATA	Not processed previous scan data.
FSP_ERR_CTSU_INCOMPLETE_TUNING	Incomplete initial offset tuning.
FSP_ERR_CARD_INIT_FAILED	SD card or eMMC device failed to initialize.
FSP_ERR_CARD_NOT_INSERTED	SD card not installed.
FSP_ERR_DEVICE_BUSY	Device is holding DAT0 low or another operation is ongoing.
FSP_ERR_CARD_NOT_INITIALIZED	SD card was removed.
FSP_ERR_CARD_WRITE_PROTECTED	Media is write protected.
FSP_ERR_TRANSFER_BUSY	Transfer in progress.
FSP_ERR_RESPONSE	Card did not respond or responded with an error.
FSP_ERR_MEDIA_FORMAT_FAILED	Media format failed.
FSP_ERR_MEDIA_OPEN_FAILED	Media open failed.
FSP_ERR_CAN_DATA_UNAVAILABLE	No data available.
FSP_ERR_CAN_MODE_SWITCH_FAILED	Switching operation modes failed.
FSP_ERR_CAN_INIT_FAILED	Hardware initialization failed.
FSP_ERR_CAN_TRANSMIT_NOT_READY	Transmit in progress.
FSP_ERR_CAN_RECEIVE_MAILBOX	Mailbox is setup as a receive mailbox.
FSP_ERR_CAN_TRANSMIT_MAILBOX	Mailbox is setup as a transmit mailbox.
FSP_ERR_CAN_MESSAGE_LOST	Receive message has been overwritten or overrun.
FSP_ERR_WIFI_CONFIG_FAILED	WiFi module Configuration failed.
FSP_ERR_WIFI_INIT_FAILED	WiFi module initialization failed.
FSP_ERR_WIFI_TRANSMIT_FAILED	Transmission failed.

FSP_ERR_WIFI_INVALID_MODE	API called when provisioned in client mode.
FSP_ERR_WIFI_FAILED	WiFi Failed.
FSP_ERR_CELLULAR_CONFIG_FAILED	Cellular module Configuration failed.
FSP_ERR_CELLULAR_INIT_FAILED	Cellular module initialization failed.
FSP_ERR_CELLULAR_TRANSMIT_FAILED	Transmission failed.
FSP_ERR_CELLULAR_FW_UPTODATE	Firmware is uptodate.
FSP_ERR_CELLULAR_FW_UPGRADE_FAILED	Firmware upgrade failed.
FSP_ERR_CELLULAR_FAILED	Cellular Failed.
FSP_ERR_CELLULAR_INVALID_STATE	API Called in invalid state.
FSP_ERR_CELLULAR_REGISTRATION_FAILED	Cellular Network registration failed.
FSP_ERR_BLE_FAILED	BLE operation failed.
FSP_ERR_BLE_INIT_FAILED	BLE device initialization failed.
FSP_ERR_BLE_CONFIG_FAILED	BLE device configuration failed.
FSP_ERR_BLE_PRF_ALREADY_ENABLED	BLE device Profile already enabled.
FSP_ERR_BLE_PRF_NOT_ENABLED	BLE device not enabled.
FSP_ERR_BLE_ABS_INVALID_OPERATION	Invalid operation is executed.
FSP_ERR_BLE_ABS_NOT_FOUND	Valid data or free space is not found.
FSP_ERR_CRYPTO_CONTINUE	Continue executing function.
FSP_ERR_CRYPTO_SCE_RESOURCE_CONFLICT	Hardware resource busy.
FSP_ERR_CRYPTO_SCE_FAIL	Internal I/O buffer is not empty.
FSP_ERR_CRYPTO_SCE_HRK_INVALID_INDEX	Invalid index.
FSP_ERR_CRYPTO_SCE_RETRY	Retry.
FSP_ERR_CRYPTO_SCE_VERIFY_FAIL	Verify is failed.
FSP_ERR_CRYPTO_SCE_ALREADY_OPEN	HW SCE module is already opened.



FSP_ERR_CRYPTO_NOT_OPEN	Hardware module is not initialized.
FSP_ERR_CRYPTO_UNKNOWN	Some unknown error occurred.
FSP_ERR_CRYPTO_NULL_POINTER	Null pointer input as a parameter.
FSP_ERR_CRYPTO_NOT_IMPLEMENTED	Algorithm/size not implemented.
FSP_ERR_CRYPTO_RNG_INVALID_PARAM	An invalid parameter is specified.
FSP_ERR_CRYPTO_RNG_FATAL_ERROR	A fatal error occurred.
FSP_ERR_CRYPTO_INVALID_SIZE	Size specified is invalid.
FSP_ERR_CRYPTO_INVALID_STATE	Function used in an valid state.
FSP_ERR_CRYPTO_ALREADY_OPEN	control block is already opened
FSP_ERR_CRYPTO_INSTALL_KEY_FAILED	Specified input key is invalid.
FSP_ERR_CRYPTO_AUTHENTICATION_FAILED	Authentication failed.
FSP_ERR_CRYPTO_SCE_KEY_SET_FAIL	Failure to Init Cipher.
FSP_ERR_CRYPTO_COMMON_NOT_OPENED	Crypto Framework Common is not opened.
FSP_ERR_CRYPTO_HAL_ERROR	Cryoto HAL module returned an error.
FSP_ERR_CRYPTO_KEY_BUF_NOT_ENOUGH	Key buffer size is not enough to generate a key.
FSP_ERR_CRYPTO_BUF_OVERFLOW	Attempt to write data larger than what the buffer can hold.
FSP_ERR_CRYPTO_INVALID_OPERATION_MODE	Invalid operation mode.
FSP_ERR_MESSAGE_TOO_LONG	Message for RSA encryption is too long.
FSP_ERR_RSA_DECRYPTION_ERROR	RSA Decryption error.

## 4.1.2 MCU Board Support Package

### BSP

#### Functions

<code>fsp_err_t</code>	<code>R_FSP_VersionGet (fsp_pack_version_t *const p_version)</code>
<code>void</code>	<code>Reset_Handler (void)</code>
<code>void</code>	<code>Default_Handler (void)</code>
<code>void</code>	<code>SystemInit (void)</code>
<code>void</code>	<code>R_BSP_WarmStart (bsp_warm_start_event_t event)</code>
<code>fsp_err_t</code>	<code>R_BSP_VersionGet (fsp_version_t *p_version)</code>
<code>__STATIC_INLINE IRQn_Type</code>	<code>R_FSP_CurrentIrqGet (void)</code>
<code>__STATIC_INLINE uint32_t</code>	<code>R_FSP_SystemClockHzGet (fsp_priv_clock_t clock)</code>
<code>__STATIC_INLINE bsp_unique_id_t const *</code>	<code>R_BSP_UniqueIdGet ()</code>
<code>__STATIC_INLINE void</code>	<code>R_BSP_FlashCacheDisable ()</code>
<code>__STATIC_INLINE void</code>	<code>R_BSP_FlashCacheEnable ()</code>
<code>void</code>	<code>R_BSP_SoftwareDelay (uint32_t delay, bsp_delay_units_t units)</code>
<code>fsp_err_t</code>	<code>R_BSP_GroupIrqWrite (bsp_grp_irq_t irq, void(*p_callback)(bsp_grp_irq_t irq))</code>
<code>void</code>	<code>NMI_Handler (void)</code>
<code>void</code>	<code>R_BSP_RegisterProtectEnable (bsp_reg_protect_t regs_to_protect)</code>
<code>void</code>	<code>R_BSP_RegisterProtectDisable (bsp_reg_protect_t regs_to_unprotect)</code>

## Detailed Description

The BSP is responsible for getting the MCU from reset to the user's application. Before reaching the user's application, the BSP sets up the stacks, heap, clocks, interrupts, C runtime environment, and stack monitor.

- [BSP Features](#)
- [BSP Clock Configuration](#)
- [System Interrupts](#)
- [Group Interrupts](#)
- [External and Peripheral Interrupts](#)
- [Error Logging](#)
- [BSP Weak Symbols](#)
- [Warm Start Callbacks](#)

- [C Runtime Initialization](#)
- [Register Protection](#)
- [ID Codes](#)
- [Software Delay](#)
- [Board Specific Features](#)
- [Configuration](#)

## Overview

### BSP Features

#### BSP Clock Configuration

All system clocks are set up during BSP initialization based on the settings in `bsp_clock_cfg.h`. These settings are derived from clock configuration information provided from the RA Configuration editor **Clocks** tab.

- Clock configuration is performed prior to initializing the C runtime environment to speed up the startup process, as it is possible to start up on a relatively slow (that is, 32 kHz) clock.
- The BSP implements the required delays to allow the selected clock to stabilize.
- The BSP will configure the CMSIS `SystemCoreClock` variable after clock initialization with the current system clock frequency.

#### System Interrupts

As RA MCUs are based on the Cortex-M ARM architecture, the NVIC Nested Vectored Interrupt Controller (NVIC) handles exceptions and interrupt configuration, prioritization and interrupt masking. In the ARM architecture, the NVIC handles exceptions. Some exceptions are known as System Exceptions. System exceptions are statically located at the "top" of the vector table and occupy vector numbers 1 to 15. Vector zero is reserved for the MSP Main Stack Pointer (MSP). The remaining 15 system exceptions are shown below:

- Reset
- NMI
- Cortex-M4 Hard Fault Handler
- Cortex-M4 MPU Fault Handler
- Cortex-M4 Bus Fault Handler
- Cortex-M4 Usage Fault Handler
- Reserved
- Reserved
- Reserved
- Reserved
- Cortex-M4 SVCALL Handler
- Cortex-M4 Debug Monitor Handler
- Reserved
- Cortex-M4 PendSV Handler
- Cortex-M4 SysTick Handler

NMI and Hard Fault exceptions are enabled out of reset and have fixed priorities. Other exceptions have configurable priorities and some can be disabled.

#### Group Interrupts

Group interrupt is the term used to describe the 12 sources that can trigger the Non-Maskable Interrupt (NMI). When an NMI occurs the NMI Handler examines the NMISR (status register) to

determine the source of the interrupt. NMI interrupts take precedence over all interrupts, are usable only as CPU interrupts, and cannot activate the RA peripherals Data Transfer Controller (DTC) or Direct Memory Access Controller (DMAC).

Possible group interrupt sources include:

- IWDT Underflow/Refresh Error
- WDT Underflow/Refresh Error
- Voltage-Monitoring 1 Interrupt
- Voltage-Monitoring 2 Interrupt
- VBATT monitor Interrupt
- Oscillation Stop is detected
- NMI pin
- RAM Parity Error
- RAM ECC Error
- MPU Bus Slave Error
- MPU Bus Master Error
- MPU Stack Error
- TrustZone Filter Error A user may enable notification for one or more group interrupts by registering a callback using the BSP API function [R\\_BSP\\_GroupIrqWrite\(\)](#). When an NMI interrupt occurs, the NMI handler checks to see if there is a callback registered for the cause of the interrupt and if so calls the registered callback function.

## External and Peripheral Interrupts

User configurable interrupts begin with slot 16. These may be external, or peripheral generated interrupts.

Although the number of available slots for the NVIC interrupt vector table may seem small, the BSP defines up to 512 events that are capable of generating an interrupt. By using Event Mapping, the BSP maps user-enabled events to NVIC interrupts. For an RA6M3 MCU, only 96 of these events may be active at any one time, but the user has flexibility by choosing which events generate the active event.

By allowing the user to select only the events they are interested in as interrupt sources, we are able to provide an interrupt service routine that is fast and event specific.

For example, on other microcontrollers a standard NVIC interrupt vector table might contain a single vector entry for the SCIO (Serial Communications Interface) peripheral. The interrupt service routine for this would have to check a status register for the 'real' source of the interrupt. In the RA implementation there is a vector entry for each of the SCIO events that we are interested in.

## BSP Weak Symbols

You might wonder how the BSP is able to place ISR addresses in the NVIC table without the user having explicitly defined one. All that is required by the BSP is that the interrupt event be given a priority.

This is accomplished through the use of the 'weak' attribute. The weak attribute causes the declaration to be emitted as a weak symbol rather than a global. A weak symbol is one that can be overridden by an accompanying strong reference with the same name. When the BSP declares a function as weak, user code can define the same function and it will be used in place of the BSP function. By defining all possible interrupt sources as weak, the vector table can be built at compile time and any user declarations (strong references) will be used at runtime.

Weak symbols are supported for ELF targets and also for a.out targets when using the GNU assembler and linker.

Note that in CMSIS system.c, there is also a weak definition (and a function body) for the Warm Start callback function `R_BSP_WarmStart()`. Because this function is defined in the same file as the weak declaration, it will be called as the 'default' implementation. The function may be overridden by the user by copying the body into their user application and modifying it as necessary. The linker identifies this as the 'strong' reference and uses it.

## Warm Start Callbacks

As the BSP is in the process of bringing up the board out of reset, there are three points where the user can request a callback. These are defined as the 'Pre Clock Init', 'Post Clock Init' and 'Post C' warm start callbacks.

As described above, this function is already weakly defined as `R_BSP_WarmStart()`, so it is a simple matter of redefining the function or copying the existing body from CMSIS system.c into the application code to get a callback. `R_BSP_WarmStart()` takes an event parameter of type `bsp_warm_start_event_t` which describes the type of warm start callback being made.

This function is not enabled/disabled and is always called for both events as part of the BSP startup. Therefore it needs a function body, which will not be called if the user is overriding it. The function body is located in system.c. To use this function just copy this function into your own code and modify it to meet your needs.

## C Runtime Initialization

This BSP configuration allows the user to skip the FSP C runtime initialization code by setting the "C Runtime Initialization" to "Disabled" on the BSP tab of the RA Configuration editor. Disabling this option is useful in cases where a non-standard linker script is being used or other modifications to the runtime initialization are desired. If this macro is disabled, the user must use the 'Post Clock Init' event from the warm start (described above) to run their own runtime initialization code.

## Heap Allocation

The relatively low amount of on-chip SRAM available and lack of memory protection in an MCU means that heap use must be very carefully controlled to avoid memory leaks, overruns and attempted overallocation. Further, many RTOSes provide their own dynamic memory allocation system. For these reasons the default heap size is set at 0 bytes, effectively disabling dynamic memory. If it is required for an application setting a positive value to the "Heap size (bytes)" option in the RA Common configurations on the **BSP** tab will allocate a heap.

### Note

*When using printf/sprintf (and other variants) to output floating point numbers a heap is required. A minimum size of 0x1000 (4096) bytes is recommended when starting development in this case.*

## Error Logging

When error logging is enabled, the error logging function can be redefined on the command line by defining `FSP_ERROR_LOG(err)` to the desired function call. The default function implementation is `FSP_ERROR_LOG(err)=fsp_error_log(err, FILE, LINE)`. This implementation uses the predefined macros **FILE** and **LINE** to help identify the location where the error occurred. Removing the line from the function call can reduce code size when error logging is enabled. Some compilers may support other predefined macros like **FUNCTION**, which could be helpful for customizing the error logger.

## Register Protection

The BSP register protection functions utilize reference counters to ensure that an application which has specified a certain register and subsequently calls another function doesn't have its register protection settings inadvertently modified.

Each time `R_BSP_RegisterProtectDisable()` is called, the respective reference counter is incremented.

Each time `R_BSP_RegisterProtectEnable()` is called, the respective reference counter is decremented.

Both functions will only modify the protection state if their reference counter is zero.

```
/* Enable writing to protected CGC registers */
R_BSP_RegisterProtectDisable(BSP_REG_PROTECT_CGC);
/* Insert code to modify protected CGC registers. */
/* Disable writing to protected CGC registers */
R_BSP_RegisterProtectEnable(BSP_REG_PROTECT_CGC);
```

## ID Codes

The ID code is a 16-byte value that can be used to protect the MCU from being connected to a debugger or from connecting in Serial Boot Mode. There are different settings that can be set for the ID code; please refer to the hardware manual for your device for available options.

## Software Delay

Implements a blocking software delay. A delay can be specified in microseconds, milliseconds or seconds. The delay is implemented based on the system clock rate.

```
/* Delay at least 1 second. Depending on the number of wait states required for the
region of memory
* that the software_delay_loop has been linked in this could take longer. The
default is 4 cycles per loop.
* This can be modified by redefining DELAY_LOOP_CYCLES. BSP_DELAY_UNITS_SECONDS,
BSP_DELAY_UNITS_MILLISECONDS,
* and BSP_DELAY_UNITS_MICROSECONDS can all be used with R_BSP_SoftwareDelay. */
R_BSP_SoftwareDelay(1, BSP_DELAY_UNITS_SECONDS);
```

## Critical Section Macros

Implements a critical section. Some MCUs (MCUs with the BASEPRI register) support allowing high priority interrupts to execute during critical sections. On these MCUs, interrupts with priority less than or equal to `BSP_CFG_IRQ_MASK_LEVEL_FOR_CRITICAL_SECTION` are not serviced in critical sections. Interrupts with higher priority than `BSP_CFG_IRQ_MASK_LEVEL_FOR_CRITICAL_SECTION` still

execute in critical sections.

```
FSP_CRITICAL_SECTION_DEFINE;

/* Store the current interrupt posture. */

FSP_CRITICAL_SECTION_ENTER;

/* Interrupts cannot run in this section unless their priority is less than
BSP_CFG_IRQ_MASK_LEVEL_FOR_CRITICAL_SECTION. */

/* Restore saved interrupt posture. */

FSP_CRITICAL_SECTION_EXIT;
```

## Board Specific Features

The BSP will call the board's initialization function (`bsp_init`) which can initialize board specific features. Possible board features are listed below.

Board Feature	Description
SDRAM Support	The BSP will initialize SDRAM if the board supports it
QSPI Support	The BSP will initialize QSPI if the board supports it and put it into ROM mode. Use the <code>R_QSPI</code> module to write and erase the QSPI chip.

## Configuration

The BSP is heavily data driven with most features and functionality being configured based on the content from configuration files. Configuration files represent the settings specified by the user and are generated when the project is built and/or when the Generate Project Content button is clicked in the RA Configuration editor.

### Build Time Configurations for `fsp_common`

The following build time configurations are defined in `fsp_cfg/bsp/bsp_cfg.h`:

Configuration	Options	Default	Description
Main stack size (bytes)	Value must be an integer multiple of 8 and between 8 and 0xFFFFFFFF	0x400	Set the size of the main program stack.  NOTE: This entry is for the main stack. When using an RTOS, thread stacks can be configured in the properties for each thread.

Heap size (bytes)	Value must be 0 or an integer multiple of 8 between 8 and 0xFFFFFFFF.	0	The main heap is disabled by default. Set the heap size to a positive integer divisible by 8 to enable it.  A minimum of 4K (0x1000) is recommended if standard library functions are to be used.
MCU Vcc (mV)	Value must between 0 and 5500 (5.5V)	3300	Some peripherals require different settings based on the supplied voltage. Entering Vcc here (in mV) allows the relevant driver modules to configure the associated peripherals accordingly.
Parameter checking	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Disabled	When enabled, parameter checking for the BSP is turned on. In addition, any modules whose parameter checking configuration is set to 'Default (BSP)' will perform parameter checking as well.
Assert Failures	<ul style="list-style-type: none"> <li>• Return FSP_ERR_ASSERTION</li> <li>• Call fsp_error_log then Return FSP_ERR_ASSERTION</li> <li>• Use assert() to Halt Execution</li> <li>• Disable checks that would return FSP_ERR_ASSERTION</li> </ul>	Return FSP_ERR_ASSERTION	Define the behavior of the <a href="#">FSP_ASSERT()</a> macro.
Error Log	<ul style="list-style-type: none"> <li>• No Error Log</li> <li>• Errors Logged via fsp_error_log</li> </ul>	No Error Log	Specify error logging behavior.
Soft Reset	<ul style="list-style-type: none"> <li>• Disabled</li> <li>• Enabled</li> </ul>	Disabled	Support for soft reset. If disabled, registers are assumed to be set



			to their default value during startup.
Main Oscillator Populated	<ul style="list-style-type: none"> <li>• Populated</li> <li>• Not Populated</li> </ul>	Populated	Select whether or not there is a main oscillator (XTAL) on the board. This setting can be overridden in board_cfg.h.
PFS Protect	<ul style="list-style-type: none"> <li>• Disabled</li> <li>• Enabled</li> </ul>	Enabled	Keep the PFS registers locked when they are not being modified. If disabled they will be unlocked during startup.
C Runtime Initialization	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Enabled	Select if the C runtime initialization in the BSP is to be used. If disabled, use the BSP_WARM_START_POST_CLOCK event to run user defined equivalent.
Main Oscillator Wait Time	<ul style="list-style-type: none"> <li>• 0.25 us</li> <li>• 128 us</li> <li>• 256 us</li> <li>• 512 us</li> <li>• 1024 us</li> <li>• 2048 us</li> <li>• 4096 us</li> <li>• 8192 us</li> <li>• 16384 us</li> <li>• 32768 us</li> </ul>	32768 us	Number of cycles to wait for the main oscillator clock to stabilize. This setting can be overridden in board_cfg.h
Main Oscillator Clock Source	<ul style="list-style-type: none"> <li>• External Oscillator</li> <li>• Crystal or Resonator</li> </ul>	Crystal or Resonator	Select the main oscillator clock source. This setting can be overridden in board_cfg.h
Subclock Populated	<ul style="list-style-type: none"> <li>• Populated</li> <li>• Not Populated</li> </ul>	Populated	Select whether or not there is a subclock crystal on the board. This setting can be overridden in board_cfg.h.
Subclock Drive (Drive capacitance availability varies by MCU)	<ul style="list-style-type: none"> <li>• Standard/Normal mode</li> <li>• Low/Low power mode 1</li> <li>• Low power mode 2</li> <li>• Low power mode 3</li> </ul>	Standard/Normal mode	Select the subclock oscillator drive capacitance. This setting can be overridden in board_cfg.h

Subclock Stabilization Time (ms)	Value must be between 0 and 10000	1000	Select the subclock oscillator stabilization time. This is only used in the startup code if the subclock is selected as the system clock on the Clocks tab. This setting can be overridden in board_cfg.h
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## Modules

RA2A1

RA4M1

RA4W1

RA6M1

RA6M2

RA6M3

RA6M4

## Macros

#define BSP\_IRQ\_DISABLED

#define FSP\_RETURN(err)

#define FSP\_ERROR\_LOG(err)

#define FSP\_ASSERT(a)

#define FSP\_ERROR\_RETURN(a, err)

#define FSP\_CRITICAL\_SECTION\_ENTER

#define FSP\_CRITICAL\_SECTION\_EXIT

#define FSP\_INVALID\_VECTOR

#define BSP\_CFG\_HANDLE\_UNRECOVERABLE\_ERROR(x)

#define BSP\_STACK\_ALIGNMENT

#define R\_BSP\_MODULE\_START(ip, channel)

```
#define R_BSP_MODULE_STOP(ip, channel)
```

## Enumerations

```
enum fsp_ip_t
```

```
enum fsp_signal_t
```

```
enum bsp_warm_start_event_t
```

```
enum bsp_delay_units_t
```

```
enum bsp_grp_irq_t
```

```
enum bsp_reg_protect_t
```

## Variables

```
uint32_t SystemCoreClock
```

```
const fsp_version_t g_bsp_version
```

Default initialization function. [More...](#)

## Macro Definition Documentation

### ◆ BSP\_IRQ\_DISABLED

```
#define BSP_IRQ_DISABLED
```

Used to signify that an ELC event is not able to be used as an interrupt.

### ◆ FSP\_RETURN

```
#define FSP_RETURN ( err)
```

Macro to log and return error without an assertion.

### ◆ FSP\_ERROR\_LOG

```
#define FSP_ERROR_LOG ( err)
```

This function is called before returning an error code. To stop on a runtime error, define `fsp_error_log` in user code and do required debugging (breakpoints, stack dump, etc) in this function.

**◆ FSP\_ASSERT**

```
#define FSP_ASSERT ( a )
```

Default assertion calls [FSP\\_ERROR\\_RETURN](#) if condition "a" is false. Used to identify incorrect use of API's in FSP functions.

**◆ FSP\_ERROR\_RETURN**

```
#define FSP_ERROR_RETURN ( a, err )
```

All FSP error codes are returned using this macro. Calls [FSP\\_ERROR\\_LOG](#) function if condition "a" is false. Used to identify runtime errors in FSP functions.

**◆ FSP\_CRITICAL\_SECTION\_ENTER**

```
#define FSP_CRITICAL_SECTION_ENTER
```

This macro temporarily saves the current interrupt state and disables interrupts.

**◆ FSP\_CRITICAL\_SECTION\_EXIT**

```
#define FSP_CRITICAL_SECTION_EXIT
```

This macro restores the previously saved interrupt state, reenabling interrupts.

**◆ FSP\_INVALID\_VECTOR**

```
#define FSP_INVALID_VECTOR
```

Used to signify that the requested IRQ vector is not defined in this system.

**◆ BSP\_CFG\_HANDLE\_UNRECOVERABLE\_ERROR**

```
#define BSP_CFG_HANDLE_UNRECOVERABLE_ERROR ( x )
```

In the event of an unrecoverable error the BSP will by default call the `__BKPT()` intrinsic function which will alert the user of the error. The user can override this default behavior by defining their own `BSP_CFG_HANDLE_UNRECOVERABLE_ERROR` macro.

**◆ BSP\_STACK\_ALIGNMENT**

```
#define BSP_STACK_ALIGNMENT
```

Stacks (and heap) must be sized and aligned to an integer multiple of this number.

### ◆ R\_BSP\_MODULE\_START

```
#define R_BSP_MODULE_START ( ip, channel )
```

Cancels the module stop state.

#### Parameters

ip	fsp_ip_t enum value for the module to be stopped
channel	The channel. Use channel 0 for modules without channels.

### ◆ R\_BSP\_MODULE\_STOP

```
#define R_BSP_MODULE_STOP ( ip, channel )
```

Enables the module stop state.

#### Parameters

ip	fsp_ip_t enum value for the module to be stopped
channel	The channel. Use channel 0 for modules without channels.

## Enumeration Type Documentation

## ◆ fsp\_ip\_t

enum fsp_ip_t	
Available modules.	
Enumerator	
FSP_IP_CFLASH	Code Flash.
FSP_IP_DFLASH	Data Flash.
FSP_IP_RAM	RAM.
FSP_IP_LVD	Low Voltage Detection.
FSP_IP_CGC	Clock Generation Circuit.
FSP_IP_LPM	Low Power Modes.
FSP_IP_FCU	Flash Control Unit.
FSP_IP_ICU	Interrupt Control Unit.
FSP_IP_DMAC	DMA Controller.
FSP_IP_DTC	Data Transfer Controller.
FSP_IP_IOPORT	I/O Ports.
FSP_IP_PFS	Pin Function Select.
FSP_IP_ELC	Event Link Controller.
FSP_IP_MPU	Memory Protection Unit.
FSP_IP_MSTP	Module Stop.
FSP_IP_MMF	Memory Mirror Function.
FSP_IP_KEY	Key Interrupt Function.
FSP_IP_CAC	Clock Frequency Accuracy Measurement Circuit.
FSP_IP_DOC	Data Operation Circuit.
FSP_IP_CRC	Cyclic Redundancy Check Calculator.
FSP_IP_SCI	Serial Communications Interface.

FSP_IP_IIC	I2C Bus Interface.
FSP_IP_SPI	Serial Peripheral Interface.
FSP_IP_CTSU	Capacitive Touch Sensing Unit.
FSP_IP_SCE	Secure Cryptographic Engine.
FSP_IP_SLCDC	Segment LCD Controller.
FSP_IP_AES	Advanced Encryption Standard.
FSP_IP_TRNG	True Random Number Generator.
FSP_IP_FCACHE	Flash Cache.
FSP_IP_SRAM	SRAM.
FSP_IP_ADC	A/D Converter.
FSP_IP_DAC	12-Bit D/A Converter
FSP_IP_TSN	Temperature Sensor.
FSP_IP_DAAD	D/A A/D Synchronous Unit.
FSP_IP_ACMPHS	High Speed Analog Comparator.
FSP_IP_ACMPLP	Low Power Analog Comparator.
FSP_IP_OPAMP	Operational Amplifier.
FSP_IP_SDADC	Sigma Delta A/D Converter.
FSP_IP_RTC	Real Time Clock.
FSP_IP_WDT	Watch Dog Timer.
FSP_IP_IWDT	Independent Watch Dog Timer.
FSP_IP_GPT	General PWM Timer.
FSP_IP_POEG	Port Output Enable for GPT.
FSP_IP_OPS	Output Phase Switch.
FSP_IP_AGT	Asynchronous General-Purpose Timer.

FSP_IP_CAN	Controller Area Network.
FSP_IP_IRDA	Infrared Data Association.
FSP_IP_QSPI	Quad Serial Peripheral Interface.
FSP_IP_USBFS	USB Full Speed.
FSP_IP_SDHI	SD/MMC Host Interface.
FSP_IP_SRC	Sampling Rate Converter.
FSP_IP_SSI	Serial Sound Interface.
FSP_IP_DALI	Digital Addressable Lighting Interface.
FSP_IP_ETHER	Ethernet MAC Controller.
FSP_IP_EDMAC	Ethernet DMA Controller.
FSP_IP_EPTPC	Ethernet PTP Controller.
FSP_IP_PDC	Parallel Data Capture Unit.
FSP_IP_GLCDC	Graphics LCD Controller.
FSP_IP_DRW	2D Drawing Engine
FSP_IP_JPEG	JPEG.
FSP_IP_DAC8	8-Bit D/A Converter
FSP_IP_USBHS	USB High Speed.
FSP_IP_OSPI	Octa Serial Peripheral Interface.



◆ **fsp\_signal\_t**

enum fsp_signal_t	
Signals that can be mapped to an interrupt.	
Enumerator	
FSP_SIGNAL_ADC_COMPARE_MATCH	ADC COMPARE MATCH.
FSP_SIGNAL_ADC_COMPARE_MISMATCH	ADC COMPARE MISMATCH.
FSP_SIGNAL_ADC_SCAN_END	ADC SCAN END.
FSP_SIGNAL_ADC_SCAN_END_B	ADC SCAN END B.
FSP_SIGNAL_ADC_WINDOW_A	ADC WINDOW A.
FSP_SIGNAL_ADC_WINDOW_B	ADC WINDOW B.
FSP_SIGNAL_AES_RDREQ	AES RDREQ.
FSP_SIGNAL_AES_WRREQ	AES WRREQ.
FSP_SIGNAL_AGT_COMPARE_A	AGT COMPARE A.
FSP_SIGNAL_AGT_COMPARE_B	AGT COMPARE B.
FSP_SIGNAL_AGT_INT	AGT INT.
FSP_SIGNAL_CAC_FREQUENCY_ERROR	CAC FREQUENCY ERROR.
FSP_SIGNAL_CAC_MEASUREMENT_END	CAC MEASUREMENT END.
FSP_SIGNAL_CAC_OVERFLOW	CAC OVERFLOW.
FSP_SIGNAL_CAN_ERROR	CAN ERROR.
FSP_SIGNAL_CAN_FIFO_RX	CAN FIFO RX.
FSP_SIGNAL_CAN_FIFO_TX	CAN FIFO TX.
FSP_SIGNAL_CAN_MAILBOX_RX	CAN MAILBOX RX.
FSP_SIGNAL_CAN_MAILBOX_TX	CAN MAILBOX TX.
FSP_SIGNAL_CGC_MOSC_STOP	CGC MOSC STOP.
FSP_SIGNAL_LPM_SNOOZE_REQUEST	LPM SNOOZE REQUEST.

FSP_SIGNAL_LVD_LVD1	LVD LVD1.
FSP_SIGNAL_LVD_LVD2	LVD LVD2.
FSP_SIGNAL_VBATT_LVD	VBATT LVD.
FSP_SIGNAL_LVD_VBATT	LVD VBATT.
FSP_SIGNAL_ACMPHS_INT	ACMPHS INT.
FSP_SIGNAL_ACMLP_INT	ACMLP INT.
FSP_SIGNAL_CTSU_END	CTSU END.
FSP_SIGNAL_CTSU_READ	CTSU READ.
FSP_SIGNAL_CTSU_WRITE	CTSU WRITE.
FSP_SIGNAL_DALI_DEI	DALI DEI.
FSP_SIGNAL_DALI_CLI	DALI CLI.
FSP_SIGNAL_DALI_SDI	DALI SDI.
FSP_SIGNAL_DALI_BPI	DALI BPI.
FSP_SIGNAL_DALI_FEI	DALI FEI.
FSP_SIGNAL_DALI_SDI_OR_BPI	DALI SDI OR BPI.
FSP_SIGNAL_DMAC_INT	DMAC INT.
FSP_SIGNAL_DOC_INT	DOC INT.
FSP_SIGNAL_DRW_INT	DRW INT.
FSP_SIGNAL_DTC_COMPLETE	DTC COMPLETE.
FSP_SIGNAL_DTC_END	DTC END.
FSP_SIGNAL_EDMAC_EINT	EDMAC EINT.
FSP_SIGNAL_ELC_SOFTWARE_EVENT_0	ELC SOFTWARE EVENT 0.
FSP_SIGNAL_ELC_SOFTWARE_EVENT_1	ELC SOFTWARE EVENT 1.
FSP_SIGNAL_EPTPC_IPLS	EPTPC IPLS.

FSP_SIGNAL_EPTPC_MINT	EPTPC MINT.
FSP_SIGNAL_EPTPC_PINT	EPTPC PINT.
FSP_SIGNAL_EPTPC_TIMER0_FALL	EPTPC TIMER0 FALL.
FSP_SIGNAL_EPTPC_TIMER0_RISE	EPTPC TIMER0 RISE.
FSP_SIGNAL_EPTPC_TIMER1_FALL	EPTPC TIMER1 FALL.
FSP_SIGNAL_EPTPC_TIMER1_RISE	EPTPC TIMER1 RISE.
FSP_SIGNAL_EPTPC_TIMER2_FALL	EPTPC TIMER2 FALL.
FSP_SIGNAL_EPTPC_TIMER2_RISE	EPTPC TIMER2 RISE.
FSP_SIGNAL_EPTPC_TIMER3_FALL	EPTPC TIMER3 FALL.
FSP_SIGNAL_EPTPC_TIMER3_RISE	EPTPC TIMER3 RISE.
FSP_SIGNAL_EPTPC_TIMER4_FALL	EPTPC TIMER4 FALL.
FSP_SIGNAL_EPTPC_TIMER4_RISE	EPTPC TIMER4 RISE.
FSP_SIGNAL_EPTPC_TIMER5_FALL	EPTPC TIMER5 FALL.
FSP_SIGNAL_EPTPC_TIMER5_RISE	EPTPC TIMER5 RISE.
FSP_SIGNAL_FCU_FIFERR	FCU FIFERR.
FSP_SIGNAL_FCU_FRDYI	FCU FRDYI.
FSP_SIGNAL_GLCDC_LINE_DETECT	GLCDC LINE DETECT.
FSP_SIGNAL_GLCDC_UNDERFLOW_1	GLCDC UNDERFLOW 1.
FSP_SIGNAL_GLCDC_UNDERFLOW_2	GLCDC UNDERFLOW 2.
FSP_SIGNAL_GPT_CAPTURE_COMPARE_A	GPT CAPTURE COMPARE A.
FSP_SIGNAL_GPT_CAPTURE_COMPARE_B	GPT CAPTURE COMPARE B.
FSP_SIGNAL_GPT_COMPARE_C	GPT COMPARE C.
FSP_SIGNAL_GPT_COMPARE_D	GPT COMPARE D.
FSP_SIGNAL_GPT_COMPARE_E	GPT COMPARE E.

FSP_SIGNAL_GPT_COMPARE_F	GPT COMPARE F.
FSP_SIGNAL_GPT_COUNTER_OVERFLOW	GPT COUNTER OVERFLOW.
FSP_SIGNAL_GPT_COUNTER_UNDERFLOW	GPT COUNTER UNDERFLOW.
FSP_SIGNAL_GPT_AD_TRIG_A	GPT AD TRIG A.
FSP_SIGNAL_GPT_AD_TRIG_B	GPT AD TRIG B.
FSP_SIGNAL_OPS_UVW_EDGE	OPS UVW EDGE.
FSP_SIGNAL_ICU_IRQ0	ICU IRQ0.
FSP_SIGNAL_ICU_IRQ1	ICU IRQ1.
FSP_SIGNAL_ICU_IRQ2	ICU IRQ2.
FSP_SIGNAL_ICU_IRQ3	ICU IRQ3.
FSP_SIGNAL_ICU_IRQ4	ICU IRQ4.
FSP_SIGNAL_ICU_IRQ5	ICU IRQ5.
FSP_SIGNAL_ICU_IRQ6	ICU IRQ6.
FSP_SIGNAL_ICU_IRQ7	ICU IRQ7.
FSP_SIGNAL_ICU_IRQ8	ICU IRQ8.
FSP_SIGNAL_ICU_IRQ9	ICU IRQ9.
FSP_SIGNAL_ICU_IRQ10	ICU IRQ10.
FSP_SIGNAL_ICU_IRQ11	ICU IRQ11.
FSP_SIGNAL_ICU_IRQ12	ICU IRQ12.
FSP_SIGNAL_ICU_IRQ13	ICU IRQ13.
FSP_SIGNAL_ICU_IRQ14	ICU IRQ14.
FSP_SIGNAL_ICU_IRQ15	ICU IRQ15.
FSP_SIGNAL_ICU_SNOOZE_CANCEL	ICU SNOOZE CANCEL.
FSP_SIGNAL_IIC_ERI	IIC ERI.

FSP_SIGNAL_IIC_RXI	IIC RXI.
FSP_SIGNAL_IIC_TEI	IIC TEI.
FSP_SIGNAL_IIC_TXI	IIC TXI.
FSP_SIGNAL_IIC_WUI	IIC WUI.
FSP_SIGNAL_IOPORT_EVENT_1	IOPORT EVENT 1.
FSP_SIGNAL_IOPORT_EVENT_2	IOPORT EVENT 2.
FSP_SIGNAL_IOPORT_EVENT_3	IOPORT EVENT 3.
FSP_SIGNAL_IOPORT_EVENT_4	IOPORT EVENT 4.
FSP_SIGNAL_IWDT_UNDERFLOW	IWDT UNDERFLOW.
FSP_SIGNAL_JPEG_JDTI	JPEG JDTI.
FSP_SIGNAL_JPEG_JEDI	JPEG JEDI.
FSP_SIGNAL_KEY_INT	KEY INT.
FSP_SIGNAL_PDC_FRAME_END	PDC FRAME END.
FSP_SIGNAL_PDC_INT	PDC INT.
FSP_SIGNAL_PDC_RECEIVE_DATA_READY	PDC RECEIVE DATA READY.
FSP_SIGNAL_POEG_EVENT	POEG EVENT.
FSP_SIGNAL_QSPI_INT	QSPI INT.
FSP_SIGNAL_RTC_ALARM	RTC ALARM.
FSP_SIGNAL_RTC_PERIOD	RTC PERIOD.
FSP_SIGNAL_RTC_CARRY	RTC CARRY.
FSP_SIGNAL_SCE_INTEGRATE_RDRDY	SCE INTEGRATE RDRDY.
FSP_SIGNAL_SCE_INTEGRATE_WRRDY	SCE INTEGRATE WRRDY.
FSP_SIGNAL_SCE_LONG_PLG	SCE LONG PLG.
FSP_SIGNAL_SCE_PROC_BUSY	SCE PROC BUSY.

FSP_SIGNAL_SCE_RDRDY_0	SCE RDRDY 0.
FSP_SIGNAL_SCE_RDRDY_1	SCE RDRDY 1.
FSP_SIGNAL_SCE_ROMOK	SCE ROMOK.
FSP_SIGNAL_SCE_TEST_BUSY	SCE TEST BUSY.
FSP_SIGNAL_SCE_WRRDY_0	SCE WRRDY 0.
FSP_SIGNAL_SCE_WRRDY_1	SCE WRRDY 1.
FSP_SIGNAL_SCE_WRRDY_4	SCE WRRDY 4.
FSP_SIGNAL_SCI_AM	SCI AM.
FSP_SIGNAL_SCI_ERI	SCI ERI.
FSP_SIGNAL_SCI_RXI	SCI RXI.
FSP_SIGNAL_SCI_RXI_OR_ERI	SCI RXI OR ERI.
FSP_SIGNAL_SCI_TEI	SCI TEI.
FSP_SIGNAL_SCI_TXI	SCI TXI.
FSP_SIGNAL_SDADC_ADI	SDADC ADI.
FSP_SIGNAL_SDADC_SCANEND	SDADC SCANEND.
FSP_SIGNAL_SDADC_CALIEND	SDADC CALIEND.
FSP_SIGNAL_SDHIMMC_ACCS	SDHIMMC ACCS.
FSP_SIGNAL_SDHIMMC_CARD	SDHIMMC CARD.
FSP_SIGNAL_SDHIMMC_DMA_REQ	SDHIMMC DMA REQ.
FSP_SIGNAL_SDHIMMC_SDIO	SDHIMMC SDIO.
FSP_SIGNAL_SPI_ERI	SPI ERI.
FSP_SIGNAL_SPI_IDLE	SPI IDLE.
FSP_SIGNAL_SPI_RXI	SPI RXI.
FSP_SIGNAL_SPI_TEI	SPI TEI.

FSP_SIGNAL_SPI_TXI	SPI TXI.
FSP_SIGNAL_SRC_CONVERSION_END	SRC CONVERSION END.
FSP_SIGNAL_SRC_INPUT_FIFO_EMPTY	SRC INPUT FIFO EMPTY.
FSP_SIGNAL_SRC_OUTPUT_FIFO_FULL	SRC OUTPUT FIFO FULL.
FSP_SIGNAL_SRC_OUTPUT_FIFO_OVERFLOW	SRC OUTPUT FIFO OVERFLOW.
FSP_SIGNAL_SRC_OUTPUT_FIFO_UNDERFLOW	SRC OUTPUT FIFO UNDERFLOW.
FSP_SIGNAL_SSI_INT	SSI INT.
FSP_SIGNAL_SSI_RXI	SSI RXI.
FSP_SIGNAL_SSI_TXI	SSI TXI.
FSP_SIGNAL_SSI_TXI_RXI	SSI TXI RXI.
FSP_SIGNAL_TRNG_RDREQ	TRNG RDREQ.
FSP_SIGNAL_USB_FIFO_0	USB FIFO 0.
FSP_SIGNAL_USB_FIFO_1	USB FIFO 1.
FSP_SIGNAL_USB_INT	USB INT.
FSP_SIGNAL_USB_RESUME	USB RESUME.
FSP_SIGNAL_USB_USB_INT_RESUME	USB USB INT RESUME.
FSP_SIGNAL_WDT_UNDERFLOW	WDT UNDERFLOW.

◆ **bsp\_warm\_start\_event\_t**

enum <code>bsp_warm_start_event_t</code>	
Different warm start entry locations in the BSP.	
Enumerator	
<code>BSP_WARM_START_RESET</code>	Called almost immediately after reset. No C runtime environment, clocks, or IRQs.
<code>BSP_WARM_START_POST_CLOCK</code>	Called after clock initialization. No C runtime environment or IRQs.
<code>BSP_WARM_START_POST_C</code>	Called after clocks and C runtime environment have been set up.

◆ **bsp\_delay\_units\_t**

enum <code>bsp_delay_units_t</code>	
Available delay units for <code>R_BSP_SoftwareDelay()</code> . These are ultimately used to calculate a total # of microseconds	
Enumerator	
<code>BSP_DELAY_UNITS_SECONDS</code>	Requested delay amount is in seconds.
<code>BSP_DELAY_UNITS_MILLISECONDS</code>	Requested delay amount is in milliseconds.
<code>BSP_DELAY_UNITS_MICROSECONDS</code>	Requested delay amount is in microseconds.



◆ **bsp\_grp\_irq\_t**

enum <code>bsp_grp_irq_t</code>	
Which interrupts can have callbacks registered.	
Enumerator	
<code>BSP_GRP_IRQ_IWDT_ERROR</code>	IWDT underflow/refresh error has occurred.
<code>BSP_GRP_IRQ_WDT_ERROR</code>	WDT underflow/refresh error has occurred.
<code>BSP_GRP_IRQ_LVD1</code>	Voltage monitoring 1 interrupt.
<code>BSP_GRP_IRQ_LVD2</code>	Voltage monitoring 2 interrupt.
<code>BSP_GRP_IRQ_VBATT</code>	VBATT monitor interrupt.
<code>BSP_GRP_IRQ_OSC_STOP_DETECT</code>	Oscillation stop is detected.
<code>BSP_GRP_IRQ_NMI_PIN</code>	NMI Pin interrupt.
<code>BSP_GRP_IRQ_RAM_PARITY</code>	RAM Parity Error.
<code>BSP_GRP_IRQ_RAM_ECC</code>	RAM ECC Error.
<code>BSP_GRP_IRQ_MPU_BUS_SLAVE</code>	MPU Bus Slave Error.
<code>BSP_GRP_IRQ_MPU_BUS_MASTER</code>	MPU Bus Master Error.
<code>BSP_GRP_IRQ_MPU_STACK</code>	MPU Stack Error.
<code>BSP_GRP_IRQ_TRUSTZONE</code>	MPU Stack Error.
<code>BSP_GRP_IRQ_CACHE_PARITY</code>	MPU Stack Error.

◆ **bsp\_reg\_protect\_t**

enum <code>bsp_reg_protect_t</code>	
The different types of registers that can be protected.	
Enumerator	
<code>BSP_REG_PROTECT_CGC</code>	Enables writing to the registers related to the clock generation circuit.
<code>BSP_REG_PROTECT_OM_LPC_BATT</code>	Enables writing to the registers related to operating modes, low power consumption, and battery backup function.
<code>BSP_REG_PROTECT_LVD</code>	Enables writing to the registers related to the LVD: LVCMPCR, LVDLVLRLR, LVD1CR0, LVD1CR1, LVD1SR, LVD2CR0, LVD2CR1, LVD2SR.
<code>BSP_REG_PROTECT_SAR</code>	Enables writing to the registers related to the security function.

**Function Documentation**◆ **R\_FSP\_VersionGet()**

<code>fsp_err_t R_FSP_VersionGet ( fsp_pack_version_t *const p_version)</code>		
Get the FSP version based on compile time macros.		
<b>Parameters</b>		
[out]	<code>p_version</code>	Memory address to return version information to.
<b>Return values</b>		
<code>FSP_SUCCESS</code>		Version information stored.
<code>FSP_ERR_ASSERTION</code>		The parameter <code>p_version</code> is NULL.

◆ **Reset\_Handler()**

<code>void Reset_Handler ( void )</code>
MCU starts executing here out of reset. Main stack pointer is set up already.

◆ **Default\_Handler()**

```
void Default_Handler ( void )
```

Default exception handler.

◆ **SystemInit()**

```
void SystemInit ( void )
```

Initialize the MCU and the runtime environment.

◆ **R\_BSP\_WarmStart()**

```
void R_BSP_WarmStart ( bsp_warm_start_event_t event)
```

This function is called at various points during the startup process. This function is declared as a weak symbol higher up in this file because it is meant to be overridden by a user implemented version. One of the main uses for this function is to call functional safety code during the startup process. To use this function just copy this function into your own code and modify it to meet your needs.

**Parameters**

[in]	event	Where the code currently is in the start up process
------	-------	-----------------------------------------------------

◆ **R\_BSP\_VersionGet()**

```
fsp_err_t R_BSP_VersionGet ( fsp_version_t* p_version)
```

Get the BSP version based on compile time macros.

**Parameters**

[out]	p_version	Memory address to return version information to.
-------	-----------	--------------------------------------------------

**Return values**

FSP_SUCCESS	Version information stored.
FSP_ERR_ASSERTION	The parameter p_version is NULL.

**◆ R\_FSP\_CurrentIrqGet()**

```
__STATIC_INLINE IRQn_Type R_FSP_CurrentIrqGet ( void )
```

Return active interrupt vector number value

**Returns**

Active interrupt vector number value

**◆ R\_FSP\_SystemClockHzGet()**

```
__STATIC_INLINE uint32_t R_FSP_SystemClockHzGet ( fsp_priv_clock_t clock)
```

Gets the frequency of a system clock.

**Returns**

Frequency of requested clock in Hertz.

**◆ R\_BSP\_UniqueIdGet()**

```
__STATIC_INLINE bsp_unique_id_t const* R_BSP_UniqueIdGet ( )
```

Get unique ID for this device.

**Returns**

A pointer to the unique identifier structure

**◆ R\_BSP\_FlashCacheDisable()**

```
__STATIC_INLINE void R_BSP_FlashCacheDisable ( )
```

Disables the flash cache.

**◆ R\_BSP\_FlashCacheEnable()**

```
__STATIC_INLINE void R_BSP_FlashCacheEnable ( )
```

Enables the flash cache.

◆ **R\_BSP\_SoftwareDelay()**

```
void R_BSP_SoftwareDelay ( uint32_t delay, bsp_delay_units_t units )
```

Delay for at least the specified duration in units and return.

**Parameters**

[in]	delay	The number of 'units' to delay.
[in]	units	The 'base' (bsp_delay_units_t) for the units specified. Valid values are: BSP_DELAY_UNITS_SECONDS , BSP_DELAY_UNITS_MILLISECONDS, BSP_DELAY_UNITS_MICROSECONDS. For example: At 1 MHz one cycle takes 1 microsecond (.000001 seconds). At 12 MHz one cycle takes 1/12 microsecond or 83 nanoseconds. Therefore one run through bsp_prv_software_delay_loop( ) takes: ~ (83 * BSP_DELAY_LOOP_CYCLES) or 332 ns. A delay of 2 us therefore requires 2000ns/332ns or 6 loops.

The 'theoretical' maximum delay that may be obtained is determined by a full 32 bit loop count and the system clock rate. @120MHz:  $((0xFFFFFFFF \text{ loops} * 4 \text{ cycles /loop}) / 120000000) = 143$  seconds. @32MHz:  $((0xFFFFFFFF \text{ loops} * 4 \text{ cycles /loop}) / 32000000) = 536$  seconds

Note that requests for very large delays will be affected by rounding in the calculations and the actual delay achieved may be slightly longer. @32 MHz, for example, a request for 532 seconds will be closer to 536 seconds.

Note also that if the calculations result in a loop\_cnt of zero, the bsp\_prv\_software\_delay\_loop() function is not called at all. In this case the requested delay is too small (nanoseconds) to be carried out by the loop itself, and the overhead associated with executing the code to just get to this point has certainly satisfied the requested delay.

**Note**

*This function calls bsp\_cpu\_clock\_get() which ultimately calls R\_CGC\_SystemClockFreqGet() and therefore requires that the BSP has already initialized the CGC (which it does as part of the Sysinit). Care should be taken to ensure this remains the case if in the future this function were to be called as part of the BSP initialization.*

◆ **R\_BSP\_GroupIrqWrite()**

```
fsp_err_t R_BSP_GroupIrqWrite ( bsp_grp_irq_t irq, void(*) (bsp_grp_irq_t irq) p_callback )
```

Register a callback function for supported interrupts. If NULL is passed for the callback argument then any previously registered callbacks are unregistered.

**Parameters**

[in]	irq	Interrupt for which to register a callback.
[in]	p_callback	Pointer to function to call when interrupt occurs.

**Return values**

FSP_SUCCESS	Callback registered
FSP_ERR_ASSERTION	Callback pointer is NULL

◆ **NMI\_Handler()**

```
void NMI_Handler ( void )
```

Non-maskable interrupt handler. This exception is defined by the BSP, unlike other system exceptions, because there are many sources that map to the NMI exception.

◆ **R\_BSP\_RegisterProtectEnable()**

```
void R_BSP_RegisterProtectEnable ( bsp_reg_protect_t regs_to_protect)
```

Enable register protection. Registers that are protected cannot be written to. Register protection is enabled by using the Protect Register (PRCR) and the MPC's Write-Protect Register (PWPR).

**Parameters**

[in]	regs_to_protect	Registers which have write protection enabled.
------	-----------------	------------------------------------------------

**◆ R\_BSP\_RegisterProtectDisable()**

```
void R_BSP_RegisterProtectDisable ( bsp_reg_protect_t regs_to_unprotect)
```

Disable register protection. Registers that are protected cannot be written to. Register protection is disabled by using the Protect Register (PRCR) and the MPC's Write-Protect Register (PWPR).

**Parameters**

[in]	regs_to_unprotect	Registers which have write protection disabled.
------	-------------------	-------------------------------------------------

**Variable Documentation****◆ SystemCoreClock**

```
uint32_t SystemCoreClock
```

System Clock Frequency (Core Clock)

**◆ g\_bsp\_version**

```
const fsp_version_t g_bsp_version
```

Default initialization function.

Version data structure used by error logger macro.

**4.1.2.1 RA2A1**

[BSP » MCU Board Support Package](#)

**Detailed Description****Build Time Configurations for ra2a1\_fsp**

The following build time configurations are defined in fsp\_cfg/bsp/bsp\_mcu\_family\_cfg.h:

Configuration	Options	Default	Description
OFS0 register settings > Independent WDT > Start Mode	<ul style="list-style-type: none"> <li>IWDT is Disabled</li> <li>IWDT is automatically activated after a reset (Autostart)</li> </ul>	IWDT is Disabled	

	mode)	
OFS0 register settings > Independent WDT > Timeout Period	<ul style="list-style-type: none"> <li>• 128 cycles</li> <li>• 512 cycles</li> <li>• 1024 cycles</li> <li>• 2048 cycles</li> </ul>	2048 cycles
OFS0 register settings > Independent WDT > Dedicated Clock Frequency Divisor	<ul style="list-style-type: none"> <li>• 1</li> <li>• 16</li> <li>• 32</li> <li>• 64</li> <li>• 128</li> <li>• 256</li> </ul>	128
OFS0 register settings > Independent WDT > Window End Position	<ul style="list-style-type: none"> <li>• 75%</li> <li>• 50%</li> <li>• 25%</li> <li>• 0% (no window end position)</li> </ul>	0% (no window end position)
OFS0 register settings > Independent WDT > Window Start Position	<ul style="list-style-type: none"> <li>• 25%</li> <li>• 50%</li> <li>• 75%</li> <li>• 100% (no window start position)</li> </ul>	100% (no window start position)
OFS0 register settings > Independent WDT > Reset Interrupt Request Select	<ul style="list-style-type: none"> <li>• NMI request or interrupt request is enabled</li> <li>• Reset is enabled</li> </ul>	Reset is enabled
OFS0 register settings > Independent WDT > Stop Control	<ul style="list-style-type: none"> <li>• Counting continues</li> <li>• Stop counting when in Sleep, Snooze mode, or Software Standby</li> </ul>	Stop counting when in Sleep, Snooze mode, or Software Standby
OFS0 register settings > WDT > Start Mode Select	<ul style="list-style-type: none"> <li>• Automatically activate WDT after a reset (auto-start mode)</li> <li>• Stop WDT after a reset (register-start mode)</li> </ul>	Stop WDT after a reset (register-start mode)
OFS0 register settings > WDT > Timeout Period	<ul style="list-style-type: none"> <li>• 1024 cycles</li> <li>• 4096 cycles</li> <li>• 8192 cycles</li> <li>• 16384 cycles</li> </ul>	16384 cycles
OFS0 register settings > WDT > Clock	<ul style="list-style-type: none"> <li>• 4</li> <li>• 64</li> </ul>	128



Frequency Division Ratio	<ul style="list-style-type: none"> <li>• 128</li> <li>• 512</li> <li>• 2048</li> <li>• 8192</li> </ul>		
OFS0 register settings > WDT > Window End Position	<ul style="list-style-type: none"> <li>• 75%</li> <li>• 50%</li> <li>• 25%</li> <li>• 0% (no window end position)</li> </ul>	0% (no window end position)	
OFS0 register settings > WDT > Window Start Position	<ul style="list-style-type: none"> <li>• 25%</li> <li>• 50%</li> <li>• 75%</li> <li>• 100% (no window start position)</li> </ul>	100% (no window start position)	
OFS0 register settings > WDT > Reset Interrupt Request	<ul style="list-style-type: none"> <li>• NMI</li> <li>• Reset</li> </ul>	Reset	
OFS0 register settings > WDT > Stop Control	<ul style="list-style-type: none"> <li>• Counting continues</li> <li>• Stop counting when entering Sleep mode</li> </ul>	Stop counting when entering Sleep mode	
OFS1 register settings > Voltage Detection 0 Circuit Start	<ul style="list-style-type: none"> <li>• Voltage monitor 0 reset is enabled after reset</li> <li>• Voltage monitor 0 reset is disabled after reset</li> </ul>	Voltage monitor 0 reset is disabled after reset	
OFS1 register settings > Voltage Detection 0 Level	<ul style="list-style-type: none"> <li>• 3.84 V</li> <li>• 2.82 V</li> <li>• 2.51 V</li> <li>• 1.90 V</li> <li>• 1.70 V</li> </ul>	1.90 V	
OFS1 register settings > HOCO Oscillation Enable	HOCO oscillation is enabled after reset	HOCO oscillation is enabled after reset	HOCO must be enabled out of reset because the MCU starts up in low voltage mode and the HOCO must be operating in low voltage mode.
MPU > Enable or disable PC Region 0	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Disabled	
MPU > PC0 Start	Value must be an integer between 0 and 0x000FFFFC (ROM) or between 0x1FF00000	0x000FFFFC	

	and 0x200FFFC (RAM)	
MPU > PC0 End	Value must be an integer between 0x00000003 and 0x000FFFF (ROM) or between 0x1FF00003 and 0x200FFFF (RAM)	0x000FFFF
MPU > Enable or disable PC Region 1	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Disabled
MPU > PC1 Start	Value must be an integer between 0 and 0x000FFFC (ROM) or between 0x1FF0000 and 0x200FFFC (RAM)	0x000FFFC
MPU > PC1 End	Value must be an integer between 0x00000003 and 0x000FFFF (ROM) or between 0x1FF00003 and 0x200FFFF (RAM)	0x000FFFF
MPU > Enable or disable Memory Region 0	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Disabled
MPU > Memory Region 0 Start	Value must be an integer between 0 and 0x000FFFC	0x000FFFC
MPU > Memory Region 0 End	Value must be an integer between 0x00000003 and 0x000FFFF	0x000FFFF
MPU > Enable or disable Memory Region 1	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Disabled
MPU > Memory Region 1 Start	Value must be an integer between 0x1FF00000 and 0x200FFFC	0x200FFFC
MPU > Memory Region 1 End	Value must be an integer between 0x1FF00003 and 0x200FFFF	0x200FFFF
MPU > Enable or disable Memory Region 2	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Disabled
MPU > Memory Region 2 Start	Value must be an integer between 0x400C0000 and	0x407FFFC

	0x400DFFFC or between 0x40100000 and 0x407FFFFC		
MPU > Memory Region 2 End	Value must be an integer between 0x400C0003 and 0x400DFFFF or between 0x40100003 and 0x407FFFFF	0x407FFFFF	
MPU > Enable or disable Memory Region 3	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Disabled	
MPU > Memory Region 3 Start	Value must be an integer between 0x400C0000 and 0x400DFFFC or between 0x40100000 and 0x407FFFFC	0x400DFFFC	
MPU > Memory Region 3 End	Value must be an integer between 0x400C0003 and 0x400DFFFF or between 0x40100003 and 0x407FFFFF	0x400DFFFF	
Use Low Voltage Mode	<ul style="list-style-type: none"> <li>• Enable</li> <li>• Disable</li> </ul>	Disable	Use the low voltage mode. This limits the ICLK operating frequency to 4 MHz and requires all clock dividers to be at least 4 when oscillation stop detection is used.
ID Code Mode	<ul style="list-style-type: none"> <li>• Unlocked (Ignore ID)</li> <li>• Locked with All Erase support</li> <li>• Locked</li> </ul>	Unlocked (Ignore ID)	When set to 'Locked with All Erase support', the ID Code must be set in the debugger to read or write data to the MCU, but the All Erase command is still accepted regardless. When set to 'Locked', all erase/download/debug access is disabled unless the ID Code is provided.
ID Code (32 Hex Characters)	Value must be a 32 character long hex string	FFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFF	Set the ID Code for locking debug access. This setting is only used when the ID Code Mode is not set to

Unlocked.

## Enumerations

enum `elc_event_t`

### Enumeration Type Documentation

#### ◆ `elc_event_t`

enum `elc_event_t`

Sources of event signals to be linked to other peripherals or the CPU

*Note*

*This list may change based on based on the device.*

#### 4.1.2.2 RA4M1

[BSP](#) » [MCU Board Support Package](#)

### Detailed Description

#### Build Time Configurations for `ra4m1_fsp`

The following build time configurations are defined in `fsp_cfg/bsp/bsp_mcu_family_cfg.h`:

Configuration	Options	Default	Description
OFS0 register settings > Independent WDT > Start Mode	<ul style="list-style-type: none"> <li>IWDT is Disabled</li> <li>IWDT is automatically activated after a reset (Autostart mode)</li> </ul>	IWDT is Disabled	
OFS0 register settings > Independent WDT > Timeout Period	<ul style="list-style-type: none"> <li>128 cycles</li> <li>512 cycles</li> <li>1024 cycles</li> <li>2048 cycles</li> </ul>	2048 cycles	
OFS0 register settings > Independent WDT > Dedicated Clock Frequency Divisor	<ul style="list-style-type: none"> <li>1</li> <li>16</li> <li>32</li> <li>64</li> <li>128</li> <li>256</li> </ul>	128	
OFS0 register settings > Independent WDT > Window End Position	<ul style="list-style-type: none"> <li>75%</li> <li>50%</li> <li>25%</li> </ul>	0% (no window end position)	

OFS0 register settings > Independent WDT > Window Start Position	<ul style="list-style-type: none"> <li>• 0% (no window end position)</li> <li>• 25%</li> <li>• 50%</li> <li>• 75%</li> <li>• 100% (no window start position)</li> </ul>	100% (no window start position)
OFS0 register settings > Independent WDT > Reset Interrupt Request Select	<ul style="list-style-type: none"> <li>• NMI request or interrupt request is enabled</li> <li>• Reset is enabled</li> </ul>	Reset is enabled
OFS0 register settings > Independent WDT > Stop Control	<ul style="list-style-type: none"> <li>• Counting continues</li> <li>• Stop counting when in Sleep, Snooze mode, or Software Standby</li> </ul>	Stop counting when in Sleep, Snooze mode, or Software Standby
OFS0 register settings > WDT > Start Mode Select	<ul style="list-style-type: none"> <li>• Automatically activate WDT after a reset (auto-start mode)</li> <li>• Stop WDT after a reset (register-start mode)</li> </ul>	Stop WDT after a reset (register-start mode)
OFS0 register settings > WDT > Timeout Period	<ul style="list-style-type: none"> <li>• 1024 cycles</li> <li>• 4096 cycles</li> <li>• 8192 cycles</li> <li>• 16384 cycles</li> </ul>	16384 cycles
OFS0 register settings > WDT > Clock Frequency Division Ratio	<ul style="list-style-type: none"> <li>• 4</li> <li>• 64</li> <li>• 128</li> <li>• 512</li> <li>• 2048</li> <li>• 8192</li> </ul>	128
OFS0 register settings > WDT > Window End Position	<ul style="list-style-type: none"> <li>• 75%</li> <li>• 50%</li> <li>• 25%</li> <li>• 0% (no window end position)</li> </ul>	0% (no window end position)
OFS0 register settings > WDT > Window Start Position	<ul style="list-style-type: none"> <li>• 25%</li> <li>• 50%</li> <li>• 75%</li> <li>• 100% (no window start position)</li> </ul>	100% (no window start position)

OFS0 register settings > WDT > Reset Interrupt Request	<ul style="list-style-type: none"> <li>• NMI</li> <li>• Reset</li> </ul>	Reset	
OFS0 register settings > WDT > Stop Control	<ul style="list-style-type: none"> <li>• Counting continues</li> <li>• Stop counting when entering Sleep mode</li> </ul>	Stop counting when entering Sleep mode	
OFS1 register settings > Voltage Detection 0 Circuit Start	<ul style="list-style-type: none"> <li>• Voltage monitor 0 reset is enabled after reset</li> <li>• Voltage monitor 0 reset is disabled after reset</li> </ul>	Voltage monitor 0 reset is disabled after reset	
OFS1 register settings > Voltage Detection 0 Level	<ul style="list-style-type: none"> <li>• 3.84 V</li> <li>• 2.82 V</li> <li>• 2.51 V</li> <li>• 1.90 V</li> <li>• 1.70 V</li> </ul>	1.90 V	
OFS1 register settings > HOCO Oscillation Enable	HOCO oscillation is enabled after reset	HOCO oscillation is enabled after reset	HOCO must be enabled out of reset because the MCU starts up in low voltage mode and the HOCO must be operating in low voltage mode.
MPU > Enable or disable PC Region 0	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Disabled	
MPU > PC0 Start	Value must be an integer between 0 and 0x00FFFFFFC (ROM) or between 0x1FF00000 and 0x200FFFFFFC (RAM)	0x00FFFFFFC	
MPU > PC0 End	Value must be an integer between 0x00000003 and 0x00FFFFFFF (ROM) or between 0x1FF00003 and 0x200FFFFFFF (RAM)	0x00FFFFFFF	
MPU > Enable or disable PC Region 1	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Disabled	
MPU > PC1 Start	Value must be an integer between 0 and 0x00FFFFFFC (ROM) or between 0x1FF00000 and 0x200FFFFFFC (RAM)	0x00FFFFFFC	
MPU > PC1 End	Value must be an	0x00FFFFFFF	

	integer between 0x00000003 and 0x00FFFFFF (ROM) or between 0x1FF00003 and 0x200FFFFFF (RAM)	
MPU > Enable or disable Memory Region 0	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Disabled
MPU > Memory Region 0 Start	Value must be an integer between 0 and 0x00FFFFFFC	0x00FFFFFFC
MPU > Memory Region 0 End	Value must be an integer between 0x00000003 and 0x00FFFFFFF	0x00FFFFFFF
MPU > Enable or disable Memory Region 1	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Disabled
MPU > Memory Region 1 Start	Value must be an integer between 0x1FF00000 and 0x200FFFFFFC	0x200FFFFFFC
MPU > Memory Region 1 End	Value must be an integer between 0x1FF00003 and 0x200FFFFFFF	0x200FFFFFFF
MPU > Enable or disable Memory Region 2	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Disabled
MPU > Memory Region 2 Start	Value must be an integer between 0x400C0000 and 0x400DFFFC or between 0x40100000 and 0x407FFFFC	0x407FFFFC
MPU > Memory Region 2 End	Value must be an integer between 0x400C0003 and 0x400DFFFF or between 0x40100003 and 0x407FFFFF	0x407FFFFF
MPU > Enable or disable Memory Region 3	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Disabled
MPU > Memory Region 3 Start	Value must be an integer between 0x400C0000 and 0x400DFFFC or	0x400DFFFC

	between 0x40100000 and 0x407FFFFC		
MPU > Memory Region 3 End	Value must be an integer between 0x400C0003 and 0x400DFFFF or between 0x40100003 and 0x407FFFFF	0x400DFFFF	
Use Low Voltage Mode	<ul style="list-style-type: none"> <li>• Enable</li> <li>• Disable</li> </ul>	Disable	Use the low voltage mode. This limits the ICLK operating frequency to 4 MHz and requires all clock dividers to be at least 4.
ID Code Mode	<ul style="list-style-type: none"> <li>• Unlocked (Ignore ID)</li> <li>• Locked with All Erase support</li> <li>• Locked</li> </ul>	Unlocked (Ignore ID)	When set to 'Locked with All Erase support', the ID Code must be set in the debugger to read or write data to the MCU, but the All Erase command is still accepted regardless. When set to 'Locked', all erase/download/debug access is disabled unless the ID Code is provided.
ID Code (32 Hex Characters)	Value must be a 32 character long hex string	FFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFF	Set the ID Code for locking debug access. This setting is only used when the ID Code Mode is not set to Unlocked.

## Enumerations

```
enum elc\_event\_t
```

### Enumeration Type Documentation

#### ◆ [elc\\_event\\_t](#)

```
enum elc\_event\_t
```

Sources of event signals to be linked to other peripherals or the CPU

*Note*

*This list may change based on based on the device.*



### 4.1.2.3 RA4W1

#### BSP » MCU Board Support Package

## Detailed Description

### Build Time Configurations for ra4w1\_fsp

The following build time configurations are defined in fsp\_cfg/bsp/bsp\_mcu\_family\_cfg.h:

Configuration	Options	Default	Description
OFS0 register settings > Independent WDT > Start Mode	<ul style="list-style-type: none"> <li>IWDT is Disabled</li> <li>IWDT is automatically activated after a reset (Autostart mode)</li> </ul>	IWDT is Disabled	
OFS0 register settings > Independent WDT > Timeout Period	<ul style="list-style-type: none"> <li>128 cycles</li> <li>512 cycles</li> <li>1024 cycles</li> <li>2048 cycles</li> </ul>	2048 cycles	
OFS0 register settings > Independent WDT > Dedicated Clock Frequency Divisor	<ul style="list-style-type: none"> <li>1</li> <li>16</li> <li>32</li> <li>64</li> <li>128</li> <li>256</li> </ul>	128	
OFS0 register settings > Independent WDT > Window End Position	<ul style="list-style-type: none"> <li>75%</li> <li>50%</li> <li>25%</li> <li>0% (no window end position)</li> </ul>	0% (no window end position)	
OFS0 register settings > Independent WDT > Window Start Position	<ul style="list-style-type: none"> <li>25%</li> <li>50%</li> <li>75%</li> <li>100% (no window start position)</li> </ul>	100% (no window start position)	
OFS0 register settings > Independent WDT > Reset Interrupt Request Select	<ul style="list-style-type: none"> <li>NMI request or interrupt request is enabled</li> <li>Reset is enabled</li> </ul>	Reset is enabled	
OFS0 register settings > Independent WDT >	<ul style="list-style-type: none"> <li>Counting continues</li> </ul>	Stop counting when in Sleep, Snooze mode, or	

Stop Control	<ul style="list-style-type: none"> <li>• Stop counting when in Sleep, Snooze mode, or Software Standby</li> </ul>	Software Standby
OFS0 register settings > WDT > Start Mode Select	<ul style="list-style-type: none"> <li>• Automatically activate WDT after a reset (auto-start mode)</li> <li>• Stop WDT after a reset (register-start mode)</li> </ul>	Stop WDT after a reset (register-start mode)
OFS0 register settings > WDT > Timeout Period	<ul style="list-style-type: none"> <li>• 1024 cycles</li> <li>• 4096 cycles</li> <li>• 8192 cycles</li> <li>• 16384 cycles</li> </ul>	16384 cycles
OFS0 register settings > WDT > Clock Frequency Division Ratio	<ul style="list-style-type: none"> <li>• 4</li> <li>• 64</li> <li>• 128</li> <li>• 512</li> <li>• 2048</li> <li>• 8192</li> </ul>	128
OFS0 register settings > WDT > Window End Position	<ul style="list-style-type: none"> <li>• 75%</li> <li>• 50%</li> <li>• 25%</li> <li>• 0% (no window end position)</li> </ul>	0% (no window end position)
OFS0 register settings > WDT > Window Start Position	<ul style="list-style-type: none"> <li>• 25%</li> <li>• 50%</li> <li>• 75%</li> <li>• 100% (no window start position)</li> </ul>	100% (no window start position)
OFS0 register settings > WDT > Reset Interrupt Request	<ul style="list-style-type: none"> <li>• NMI</li> <li>• Reset</li> </ul>	Reset
OFS0 register settings > WDT > Stop Control	<ul style="list-style-type: none"> <li>• Counting continues</li> <li>• Stop counting when entering Sleep mode</li> </ul>	Stop counting when entering Sleep mode
OFS1 register settings > Voltage Detection 0 Circuit Start	<ul style="list-style-type: none"> <li>• Voltage monitor 0 reset is enabled after reset</li> <li>• Voltage monitor 0 reset is disabled after reset</li> </ul>	Voltage monitor 0 reset is disabled after reset

OFS1 register settings > Voltage Detection 0 Level	<ul style="list-style-type: none"> <li>• 3.84 V</li> <li>• 2.82 V</li> <li>• 2.51 V</li> <li>• 1.90 V</li> <li>• 1.70 V</li> </ul>	1.90 V
OFS1 register settings > HOCO Oscillation Enable	<ul style="list-style-type: none"> <li>• HOCO oscillation is enabled after reset</li> <li>• HOCO oscillation is disabled after reset</li> </ul>	HOCO oscillation is disabled after reset
MPU > Enable or disable PC Region 0	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Disabled
MPU > PC0 Start	Value must be an integer between 0 and 0x00FFFFFFC (ROM) or between 0x1FF00000 and 0x200FFFFFFC (RAM)	0x00FFFFFFC
MPU > PC0 End	Value must be an integer between 0x00000003 and 0x00FFFFFFF (ROM) or between 0x1FF00003 and 0x200FFFFFFF (RAM)	0x00FFFFFFF
MPU > Enable or disable PC Region 1	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Disabled
MPU > PC1 Start	Value must be an integer between 0 and 0x00FFFFFFC (ROM) or between 0x1FF00000 and 0x200FFFFFFC (RAM)	0x00FFFFFFC
MPU > PC1 End	Value must be an integer between 0x00000003 and 0x00FFFFFFF (ROM) or between 0x1FF00003 and 0x200FFFFFFF (RAM)	0x00FFFFFFF
MPU > Enable or disable Memory Region 0	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Disabled
MPU > Memory Region 0 Start	Value must be an integer between 0 and 0x00FFFFFFC	0x00FFFFFFC
MPU > Memory Region 0 End	Value must be an integer between 0x00000003 and 0x00FFFFFFF	0x00FFFFFFF

MPU > Enable or disable Memory Region 1	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Disabled	
MPU > Memory Region 1 Start	Value must be an integer between 0x1FF00000 and 0x200FFFFC	0x200FFFFC	
MPU > Memory Region 1 End	Value must be an integer between 0x1FF00003 and 0x200FFFFF	0x200FFFFF	
MPU > Enable or disable Memory Region 2	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Disabled	
MPU > Memory Region 2 Start	Value must be an integer between 0x400C0000 and 0x400DFFFC or between 0x40100000 and 0x407FFFFC	0x407FFFFC	
MPU > Memory Region 2 End	Value must be an integer between 0x400C0003 and 0x400DFFFF or between 0x40100003 and 0x407FFFFF	0x407FFFFF	
MPU > Enable or disable Memory Region 3	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Disabled	
MPU > Memory Region 3 Start	Value must be an integer between 0x400C0000 and 0x400DFFFC or between 0x40100000 and 0x407FFFFC	0x400DFFFC	
MPU > Memory Region 3 End	Value must be an integer between 0x400C0003 and 0x400DFFFF or between 0x40100003 and 0x407FFFFF	0x400DFFFF	
Use Low Voltage Mode	<ul style="list-style-type: none"> <li>• Enable</li> <li>• Disable</li> </ul>	Disable	Use the low voltage mode. This limits the ICLK operating frequency to 4 MHz and requires all clock dividers to be at least 4.

ID Code Mode	<ul style="list-style-type: none"> <li>• Unlocked (Ignore ID)</li> <li>• Locked with All Erase support</li> <li>• Locked</li> </ul>	Unlocked (Ignore ID)	When set to 'Locked with All Erase support', the ID Code must be set in the debugger to read or write data to the MCU, but the All Erase command is still accepted regardless. When set to 'Locked', all erase/download/debug access is disabled unless the ID Code is provided.
ID Code (32 Hex Characters)	Value must be a 32 character long hex string	FFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFF	Set the ID Code for locking debug access. This setting is only used when the ID Code Mode is not set to Unlocked.

## Enumerations

enum [elc\\_event\\_t](#)

## Enumeration Type Documentation

### ◆ [elc\\_event\\_t](#)

enum [elc\\_event\\_t](#)

Sources of event signals to be linked to other peripherals or the CPU1

*Note*

*This list may change based on device. This list is for RA4W1.*

### 4.1.2.4 RA6M1

[BSP](#) » [MCU Board Support Package](#)

## Detailed Description

### Build Time Configurations for [ra6m1\\_fsp](#)

The following build time configurations are defined in `fsp_cfg/bsp/bsp_mcu_family_cfg.h`:

Configuration	Options	Default	Description
OFS0 register settings > Independent WDT > Start Mode	<ul style="list-style-type: none"> <li>• IWDT is Disabled</li> <li>• IWDT is</li> </ul>	IWDT is Disabled	

	automatically activated after a reset (Autostart mode)	
OFS0 register settings > Independent WDT > Timeout Period	<ul style="list-style-type: none"> <li>• 128 cycles</li> <li>• 512 cycles</li> <li>• 1024 cycles</li> <li>• 2048 cycles</li> </ul>	2048 cycles
OFS0 register settings > Independent WDT > Dedicated Clock Frequency Divisor	<ul style="list-style-type: none"> <li>• 1</li> <li>• 16</li> <li>• 32</li> <li>• 64</li> <li>• 128</li> <li>• 256</li> </ul>	128
OFS0 register settings > Independent WDT > Window End Position	<ul style="list-style-type: none"> <li>• 75%</li> <li>• 50%</li> <li>• 25%</li> <li>• 0% (no window end position)</li> </ul>	0% (no window end position)
OFS0 register settings > Independent WDT > Window Start Position	<ul style="list-style-type: none"> <li>• 25%</li> <li>• 50%</li> <li>• 75%</li> <li>• 100% (no window start position)</li> </ul>	100% (no window start position)
OFS0 register settings > Independent WDT > Reset Interrupt Request Select	<ul style="list-style-type: none"> <li>• NMI request or interrupt request is enabled</li> <li>• Reset is enabled</li> </ul>	Reset is enabled
OFS0 register settings > Independent WDT > Stop Control	<ul style="list-style-type: none"> <li>• Counting continues (Note: Device will not enter Deep Standby Mode when selected. Device will enter Software Standby Mode)</li> <li>• Stop counting when in Sleep, Snooze mode, or Software Standby</li> </ul>	Stop counting when in Sleep, Snooze mode, or Software Standby
OFS0 register settings > WDT > Start Mode Select	<ul style="list-style-type: none"> <li>• Automatically activate WDT after a reset (auto-start</li> </ul>	Stop WDT after a reset (register-start mode)

	mode)	
	<ul style="list-style-type: none"> <li>• Stop WDT after a reset (register-start mode)</li> </ul>	
OFS0 register settings > WDT > Timeout Period	<ul style="list-style-type: none"> <li>• 1024 cycles</li> <li>• 4096 cycles</li> <li>• 8192 cycles</li> <li>• 16384 cycles</li> </ul>	16384 cycles
OFS0 register settings > WDT > Clock Frequency Division Ratio	<ul style="list-style-type: none"> <li>• 4</li> <li>• 64</li> <li>• 128</li> <li>• 512</li> <li>• 2048</li> <li>• 8192</li> </ul>	128
OFS0 register settings > WDT > Window End Position	<ul style="list-style-type: none"> <li>• 75%</li> <li>• 50%</li> <li>• 25%</li> <li>• 0% (no window end position)</li> </ul>	0% (no window end position)
OFS0 register settings > WDT > Window Start Position	<ul style="list-style-type: none"> <li>• 25%</li> <li>• 50%</li> <li>• 75%</li> <li>• 100% (no window start position)</li> </ul>	100% (no window start position)
OFS0 register settings > WDT > Reset Interrupt Request	<ul style="list-style-type: none"> <li>• NMI</li> <li>• Reset</li> </ul>	Reset
OFS0 register settings > WDT > Stop Control	<ul style="list-style-type: none"> <li>• Counting continues</li> <li>• Stop counting when entering Sleep mode</li> </ul>	Stop counting when entering Sleep mode
OFS1 register settings > Voltage Detection 0 Circuit Start	<ul style="list-style-type: none"> <li>• Voltage monitor 0 reset is enabled after reset</li> <li>• Voltage monitor 0 reset is disabled after reset</li> </ul>	Voltage monitor 0 reset is disabled after reset
OFS1 register settings > Voltage Detection 0 Level	<ul style="list-style-type: none"> <li>• 2.94 V</li> <li>• 2.87 V</li> <li>• 2.80 V</li> </ul>	2.80 V
OFS1 register settings > HOCO Oscillation Enable	<ul style="list-style-type: none"> <li>• HOCO oscillation is enabled after reset</li> <li>• HOCO</li> </ul>	HOCO oscillation is disabled after reset

	oscillation is disabled after reset	
MPU > Enable or disable PC Region 0	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Disabled
MPU > PC0 Start	Value must be an integer between 0 and 0xFFFFFFFF	0xFFFFFFFF
MPU > PC0 End	Value must be an integer between 0x00000003 and 0xFFFFFFFF	0xFFFFFFFF
MPU > Enable or disable PC Region 1	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Disabled
MPU > PC1 Start	Value must be an integer between 0 and 0xFFFFFFFF	0xFFFFFFFF
MPU > PC1 End	Value must be an integer between 0x00000003 and 0xFFFFFFFF	0xFFFFFFFF
MPU > Enable or disable Memory Region 0	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Disabled
MPU > Memory Region 0 Start	Value must be an integer between 0 and 0x00FFFFFF	0x00FFFFFF
MPU > Memory Region 0 End	Value must be an integer between 0x00000003 and 0x00FFFFFF	0x00FFFFFF
MPU > Enable or disable Memory Region 1	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Disabled
MPU > Memory Region 1 Start	Value must be an integer between 0x1FF00000 and 0x200FFFFC	0x200FFFFC
MPU > Memory Region 1 End	Value must be an integer between 0x1FF00003 and 0x200FFFFF	0x200FFFFF
MPU > Enable or disable Memory Region 2	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Disabled
MPU > Memory Region 2 Start	Value must be an integer between 0x40700000 and 0x407FFFFC	0x407FFFFC



2 Start	integer between 0x400C0000 and 0x400DFFFC or between 0x40100000 and 0x407FFFFC		
MPU > Memory Region 2 End	Value must be an integer between 0x400C0003 and 0x400DFFFF or between 0x40100003 and 0x407FFFFF	0x407FFFFF	
MPU > Enable or disable Memory Region 3	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Disabled	
MPU > Memory Region 3 Start	Value must be an integer between 0x400C0000 and 0x400DFFFC or between 0x40100000 and 0x407FFFFC	0x400DFFFC	
MPU > Memory Region 3 End	Value must be an integer between 0x400C0003 and 0x400DFFFF or between 0x40100003 and 0x407FFFFF	0x400DFFFF	
ID Code Mode	<ul style="list-style-type: none"> <li>• Unlocked (Ignore ID)</li> <li>• Locked with All Erase support</li> <li>• Locked</li> </ul>	Unlocked (Ignore ID)	When set to 'Locked with All Erase support', the ID Code must be set in the debugger to read or write data to the MCU, but the All Erase command is still accepted regardless. When set to 'Locked', all erase/download/debug access is disabled unless the ID Code is provided.
ID Code (32 Hex Characters)	Value must be a 32 character long hex string	FFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFF	Set the ID Code for locking debug access. This setting is only used when the ID Code Mode is not set to Unlocked.

## Enumerations

```
enum elc_event_t
```

## Enumeration Type Documentation

### ◆ elc\_event\_t

enum `elc_event_t`

Sources of event signals to be linked to other peripherals or the CPU

*Note*

*This list may change based on based on the device.*

#### 4.1.2.5 RA6M2

[BSP](#) » [MCU Board Support Package](#)

### Detailed Description

#### Build Time Configurations for `ra6m2_fsp`

The following build time configurations are defined in `fsp_cfg/bsp/bsp_mcu_family_cfg.h`:

Configuration	Options	Default	Description
OFS0 register settings > Independent WDT > Start Mode	<ul style="list-style-type: none"> <li>IWDT is Disabled</li> <li>IWDT is automatically activated after a reset (Autostart mode)</li> </ul>	IWDT is Disabled	
OFS0 register settings > Independent WDT > Timeout Period	<ul style="list-style-type: none"> <li>128 cycles</li> <li>512 cycles</li> <li>1024 cycles</li> <li>2048 cycles</li> </ul>	2048 cycles	
OFS0 register settings > Independent WDT > Dedicated Clock Frequency Divisor	<ul style="list-style-type: none"> <li>1</li> <li>16</li> <li>32</li> <li>64</li> <li>128</li> <li>256</li> </ul>	128	
OFS0 register settings > Independent WDT > Window End Position	<ul style="list-style-type: none"> <li>75%</li> <li>50%</li> <li>25%</li> <li>0% (no window end position)</li> </ul>	0% (no window end position)	
OFS0 register settings > Independent WDT > Window Start Position	<ul style="list-style-type: none"> <li>25%</li> <li>50%</li> <li>75%</li> </ul>	100% (no window start position)	

OFS0 register settings > Independent WDT > Reset Interrupt Request Select	<ul style="list-style-type: none"> <li>• 100% (no window start position)</li> <li>• NMI request or interrupt request is enabled</li> <li>• Reset is enabled</li> </ul>	Reset is enabled
OFS0 register settings > Independent WDT > Stop Control	<ul style="list-style-type: none"> <li>• Counting continues (Note: Device will not enter Deep Standby Mode when selected. Device will enter Software Standby Mode)</li> <li>• Stop counting when in Sleep, Snooze mode, or Software Standby</li> </ul>	Stop counting when in Sleep, Snooze mode, or Software Standby
OFS0 register settings > WDT > Start Mode Select	<ul style="list-style-type: none"> <li>• Automatically activate WDT after a reset (auto-start mode)</li> <li>• Stop WDT after a reset (register-start mode)</li> </ul>	Stop WDT after a reset (register-start mode)
OFS0 register settings > WDT > Timeout Period	<ul style="list-style-type: none"> <li>• 1024 cycles</li> <li>• 4096 cycles</li> <li>• 8192 cycles</li> <li>• 16384 cycles</li> </ul>	16384 cycles
OFS0 register settings > WDT > Clock Frequency Division Ratio	<ul style="list-style-type: none"> <li>• 4</li> <li>• 64</li> <li>• 128</li> <li>• 512</li> <li>• 2048</li> <li>• 8192</li> </ul>	128
OFS0 register settings > WDT > Window End Position	<ul style="list-style-type: none"> <li>• 75%</li> <li>• 50%</li> <li>• 25%</li> <li>• 0% (no window end position)</li> </ul>	0% (no window end position)
OFS0 register settings > WDT > Window Start Position	<ul style="list-style-type: none"> <li>• 25%</li> <li>• 50%</li> <li>• 75%</li> <li>• 100% (no</li> </ul>	100% (no window start position)

	window start position)	
OFS0 register settings > WDT > Reset Interrupt Request	<ul style="list-style-type: none"> <li>• NMI</li> <li>• Reset</li> </ul>	Reset
OFS0 register settings > WDT > Stop Control	<ul style="list-style-type: none"> <li>• Counting continues</li> <li>• Stop counting when entering Sleep mode</li> </ul>	Stop counting when entering Sleep mode
OFS1 register settings > Voltage Detection 0 Circuit Start	<ul style="list-style-type: none"> <li>• Voltage monitor 0 reset is enabled after reset</li> <li>• Voltage monitor 0 reset is disabled after reset</li> </ul>	Voltage monitor 0 reset is disabled after reset
OFS1 register settings > Voltage Detection 0 Level	<ul style="list-style-type: none"> <li>• 2.94 V</li> <li>• 2.87 V</li> <li>• 2.80 V</li> </ul>	2.80 V
OFS1 register settings > HOCO Oscillation Enable	<ul style="list-style-type: none"> <li>• HOCO oscillation is enabled after reset</li> <li>• HOCO oscillation is disabled after reset</li> </ul>	HOCO oscillation is disabled after reset
MPU > Enable or disable PC Region 0	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Disabled
MPU > PC0 Start	Value must be an integer between 0 and 0xFFFFFFFF	0xFFFFFFFF
MPU > PC0 End	Value must be an integer between 0x00000003 and 0xFFFFFFFF	0xFFFFFFFF
MPU > Enable or disable PC Region 1	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Disabled
MPU > PC1 Start	Value must be an integer between 0 and 0xFFFFFFFF	0xFFFFFFFF
MPU > PC1 End	Value must be an integer between 0x00000003 and 0xFFFFFFFF	0xFFFFFFFF

MPU > Enable or disable Memory Region 0	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Disabled
MPU > Memory Region 0 Start	Value must be an integer between 0 and 0x00FFFFFFC	0x00FFFFFFC
MPU > Memory Region 0 End	Value must be an integer between 0x00000003 and 0x00FFFFFFF	0x00FFFFFFF
MPU > Enable or disable Memory Region 1	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Disabled
MPU > Memory Region 1 Start	Value must be an integer between 0x1FF00000 and 0x200FFFFFFC	0x200FFFFFFC
MPU > Memory Region 1 End	Value must be an integer between 0x1FF00003 and 0x200FFFFFFF	0x200FFFFFFF
MPU > Enable or disable Memory Region 2	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Disabled
MPU > Memory Region 2 Start	Value must be an integer between 0x400C0000 and 0x400DFFFC or between 0x40100000 and 0x407FFFFFFC	0x407FFFFFFC
MPU > Memory Region 2 End	Value must be an integer between 0x400C0003 and 0x400DFFFF or between 0x40100003 and 0x407FFFFFFF	0x407FFFFFFF
MPU > Enable or disable Memory Region 3	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Disabled
MPU > Memory Region 3 Start	Value must be an integer between 0x400C0000 and 0x400DFFFC or between 0x40100000 and 0x407FFFFFFC	0x400DFFFC
MPU > Memory Region 3 End	Value must be an integer between 0x400C0003 and	0x400DFFFF

	0x400DFFFF or between 0x40100003 and 0x407FFFFFFF		
ID Code Mode	<ul style="list-style-type: none"> <li>• Unlocked (Ignore ID)</li> <li>• Locked with All Erase support</li> <li>• Locked</li> </ul>	Unlocked (Ignore ID)	When set to 'Locked with All Erase support', the ID Code must be set in the debugger to read or write data to the MCU, but the All Erase command is still accepted regardless. When set to 'Locked', all erase/download/debug access is disabled unless the ID Code is provided.
ID Code (32 Hex Characters)	Value must be a 32 character long hex string	FFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFF	Set the ID Code for locking debug access. This setting is only used when the ID Code Mode is not set to Unlocked.

## Enumerations

enum [elc\\_event\\_t](#)

## Enumeration Type Documentation

### ◆ [elc\\_event\\_t](#)

enum [elc\\_event\\_t](#)

Sources of event signals to be linked to other peripherals or the CPU

*Note*

*This list may change based on based on the device.*

### 4.1.2.6 RA6M3

[BSP » MCU Board Support Package](#)

## Detailed Description

### Build Time Configurations for ra6m3\_fsp

The following build time configurations are defined in `fsp_cfg/bsp/bsp_mcu_family_cfg.h`:

Configuration	Options	Default	Description
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OFS0 register settings > Independent WDT > Start Mode	<ul style="list-style-type: none"> <li>• IWDT is Disabled</li> <li>• IWDT is automatically activated after a reset (Autostart mode)</li> </ul>	IWDT is Disabled
OFS0 register settings > Independent WDT > Timeout Period	<ul style="list-style-type: none"> <li>• 128 cycles</li> <li>• 512 cycles</li> <li>• 1024 cycles</li> <li>• 2048 cycles</li> </ul>	2048 cycles
OFS0 register settings > Independent WDT > Dedicated Clock Frequency Divisor	<ul style="list-style-type: none"> <li>• 1</li> <li>• 16</li> <li>• 32</li> <li>• 64</li> <li>• 128</li> <li>• 256</li> </ul>	128
OFS0 register settings > Independent WDT > Window End Position	<ul style="list-style-type: none"> <li>• 75%</li> <li>• 50%</li> <li>• 25%</li> <li>• 0% (no window end position)</li> </ul>	0% (no window end position)
OFS0 register settings > Independent WDT > Window Start Position	<ul style="list-style-type: none"> <li>• 25%</li> <li>• 50%</li> <li>• 75%</li> <li>• 100% (no window start position)</li> </ul>	100% (no window start position)
OFS0 register settings > Independent WDT > Reset Interrupt Request Select	<ul style="list-style-type: none"> <li>• NMI request or interrupt request is enabled</li> <li>• Reset is enabled</li> </ul>	Reset is enabled
OFS0 register settings > Independent WDT > Stop Control	<ul style="list-style-type: none"> <li>• Counting continues (Note: Device will not enter Deep Standby Mode when selected. Device will enter Software Standby Mode)</li> <li>• Stop counting when in Sleep, Snooze mode, or Software Standby</li> </ul>	Stop counting when in Sleep, Snooze mode, or Software Standby
OFS0 register settings	<ul style="list-style-type: none"> <li>• Automatically</li> </ul>	Stop WDT after a reset

> WDT > Start Mode Select	activate WDT after a reset (auto-start mode) <ul style="list-style-type: none"> <li>Stop WDT after a reset (register-start mode)</li> </ul>	(register-start mode)
OFS0 register settings > WDT > Timeout Period	<ul style="list-style-type: none"> <li>1024 cycles</li> <li>4096 cycles</li> <li>8192 cycles</li> <li>16384 cycles</li> </ul>	16384 cycles
OFS0 register settings > WDT > Clock Frequency Division Ratio	<ul style="list-style-type: none"> <li>4</li> <li>64</li> <li>128</li> <li>512</li> <li>2048</li> <li>8192</li> </ul>	128
OFS0 register settings > WDT > Window End Position	<ul style="list-style-type: none"> <li>75%</li> <li>50%</li> <li>25%</li> <li>0% (no window end position)</li> </ul>	0% (no window end position)
OFS0 register settings > WDT > Window Start Position	<ul style="list-style-type: none"> <li>25%</li> <li>50%</li> <li>75%</li> <li>100% (no window start position)</li> </ul>	100% (no window start position)
OFS0 register settings > WDT > Reset Interrupt Request	<ul style="list-style-type: none"> <li>NMI</li> <li>Reset</li> </ul>	Reset
OFS0 register settings > WDT > Stop Control	<ul style="list-style-type: none"> <li>Counting continues</li> <li>Stop counting when entering Sleep mode</li> </ul>	Stop counting when entering Sleep mode
OFS1 register settings > Voltage Detection 0 Circuit Start	<ul style="list-style-type: none"> <li>Voltage monitor 0 reset is enabled after reset</li> <li>Voltage monitor 0 reset is disabled after reset</li> </ul>	Voltage monitor 0 reset is disabled after reset
OFS1 register settings > Voltage Detection 0 Level	<ul style="list-style-type: none"> <li>2.94 V</li> <li>2.87 V</li> <li>2.80 V</li> </ul>	2.80 V
OFS1 register settings > HOCO Oscillation	<ul style="list-style-type: none"> <li>HOCO oscillation is</li> </ul>	HOCO oscillation is disabled after reset



Enable	enabled after reset <ul style="list-style-type: none"> <li>HOCO oscillation is disabled after reset</li> </ul>	
MPU > Enable or disable PC Region 0	<ul style="list-style-type: none"> <li>Enabled</li> <li>Disabled</li> </ul>	Disabled
MPU > PC0 Start	Value must be an integer between 0 and 0xFFFFFFFFC	0xFFFFFFFFC
MPU > PC0 End	Value must be an integer between 0x00000003 and 0xFFFFFFFF	0xFFFFFFFF
MPU > Enable or disable PC Region 1	<ul style="list-style-type: none"> <li>Enabled</li> <li>Disabled</li> </ul>	Disabled
MPU > PC1 Start	Value must be an integer between 0 and 0xFFFFFFFFC	0xFFFFFFFFC
MPU > PC1 End	Value must be an integer between 0x00000003 and 0xFFFFFFFF	0xFFFFFFFF
MPU > Enable or disable Memory Region 0	<ul style="list-style-type: none"> <li>Enabled</li> <li>Disabled</li> </ul>	Disabled
MPU > Memory Region 0 Start	Value must be an integer between 0 and 0x00FFFFFFC	0x00FFFFFFC
MPU > Memory Region 0 End	Value must be an integer between 0x00000003 and 0x00FFFFFF	0x00FFFFFF
MPU > Enable or disable Memory Region 1	<ul style="list-style-type: none"> <li>Enabled</li> <li>Disabled</li> </ul>	Disabled
MPU > Memory Region 1 Start	Value must be an integer between 0x1FF00000 and 0x200FFFFFFC	0x200FFFFFFC
MPU > Memory Region 1 End	Value must be an integer between 0x1FF00003 and 0x200FFFFFF	0x200FFFFFF
MPU > Enable or disable Memory Region	<ul style="list-style-type: none"> <li>Enabled</li> <li>Disabled</li> </ul>	Disabled

2			
MPU > Memory Region 2 Start	Value must be an integer between 0x400C0000 and 0x400DFFFC or between 0x40100000 and 0x407FFFFC	0x407FFFFC	
MPU > Memory Region 2 End	Value must be an integer between 0x400C0003 and 0x400DFFFF or between 0x40100003 and 0x407FFFFF	0x407FFFFF	
MPU > Enable or disable Memory Region 3	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Disabled	
MPU > Memory Region 3 Start	Value must be an integer between 0x400C0000 and 0x400DFFFC or between 0x40100000 and 0x407FFFFC	0x400DFFFC	
MPU > Memory Region 3 End	Value must be an integer between 0x400C0003 and 0x400DFFFF or between 0x40100003 and 0x407FFFFF	0x400DFFFF	
ID Code Mode	<ul style="list-style-type: none"> <li>• Unlocked (Ignore ID)</li> <li>• Locked with All Erase support</li> <li>• Locked</li> </ul>	Unlocked (Ignore ID)	When set to 'Locked with All Erase support', the ID Code must be set in the debugger to read or write data to the MCU, but the All Erase command is still accepted regardless. When set to 'Locked', all erase/download/debug access is disabled unless the ID Code is provided.
ID Code (32 Hex Characters)	Value must be a 32 character long hex string	FFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFF	Set the ID Code for locking debug access. This setting is only used when the ID Code Mode is not set to Unlocked.

## Enumerations

enum `elc_event_t`

## Enumeration Type Documentation

### ◆ `elc_event_t`

enum `elc_event_t`

Sources of event signals to be linked to other peripherals or the CPU

*Note*

*This list may change based on based on the device.*

#### 4.1.2.7 RA6M4

BSP » [MCU Board Support Package](#)

### Build Time Configurations for `ra6m4_fsp`

The following build time configurations are defined in `fsp_cfg/bsp/bsp_mcu_family_cfg.h`:

Configuration	Options	Default	Description
Security > Exceptions > Exception Response	<ul style="list-style-type: none"> <li>Non-Maskable Interrupt</li> <li>Reset</li> </ul>	Non-Maskable Interrupt	<p>Configure the result of a TrustZone Filter exception. This exception is generated when a the TrustZone Filter detects access to a protected region.</p> <p>This setting is only valid when building projects with TrustZone.</p>
Security > Exceptions > BusFault, HardFault, and NMI Target	<ul style="list-style-type: none"> <li>Non-Secure State</li> <li>Secure State</li> </ul>	Secure State	<p>Value for SCB-&gt;AIRCR register bit BFHFNMIN. Defines whether BusFault and NMI exceptions are Non-secure, and whether exceptions target the Non-secure HardFault exception.</p> <p>This setting is only valid when building projects with TrustZone.</p>

Security > Exceptions > Prioritize Secure Exceptions	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Disabled	<p>Value for SCB-&gt;AIRCR register bit PRIS. When enabled, all Non-secure interrupt priorities are automatically demoted by right shifting their priority by one then setting the most significant bit. As there is effectively one less bit care must be taken to ensure the prioritization of non-secure interrupts is correct.</p> <p>This setting is only valid when building projects with TrustZone.</p>
Security > SRAM Accessibility > SRAM Protection	<ul style="list-style-type: none"> <li>• Both Secure and Non-Secure State</li> <li>• Secure State</li> </ul>	Both Secure and Non-Secure State	<p>Defines whether SRAMPRCR is write accessible for the Non-secure application.</p> <p>This setting is only valid when building projects with TrustZone.</p>
Security > SRAM Accessibility > SRAM ECC	<ul style="list-style-type: none"> <li>• Both Secure and Non-Secure State</li> <li>• Secure State</li> </ul>	Both Secure and Non-Secure State	<p>Defines whether SRAM ECC registers are write accessible for the Non-secure application.</p> <p>This setting is only valid when building projects with TrustZone.</p>
Security > SRAM Accessibility > Standby RAM	<ul style="list-style-type: none"> <li>• Regions 7-0 are all Secure.</li> <li>• Region 7 is Non-secure. Regions 6-0 are Secure.</li> <li>• Regions 7-6 are Non-secure. Regions 5-0 are Secure.</li> <li>• Regions 7-5 are Non-secure. Regions 4-0 are Secure.</li> <li>• Regions 7-4 are Non-secure.</li> </ul>	config.bsp.fsp.tz.stbramsar.both	<p>Defines whether Standby RAM registers are accessible for the Non-secure application.</p> <p>This setting is only valid when building projects with TrustZone.</p>

	<ul style="list-style-type: none"> <li>Regions 3-0 are Secure.</li> <li>Regions 7-3 are Non-secure.</li> <li>Regions 2-0 are Secure.</li> <li>Regions 7-2 are Non-secure.</li> <li>Regions 1-0 are Secure.</li> <li>Regions 7-1 are Non-secure.</li> <li>Region 0 is Secure.</li> <li>Regions 7-0 are all Non-secure.</li> </ul>		
Security > BUS Accessibility > Bus Security Attribution Register A	<ul style="list-style-type: none"> <li>Both Secure and Non-Secure State</li> <li>Secure State</li> </ul>	Both Secure and Non-Secure State	<p>Defines whether the Slave Bus Control Registers (BUSSCNT&lt;slave&gt;) are write accessible for the Non-secure application.</p> <p>This setting is only valid when building projects with TrustZone.</p>
Security > BUS Accessibility > Bus Security Attribution Register B	<ul style="list-style-type: none"> <li>Both Secure and Non-Secure State</li> <li>Secure State</li> </ul>	Both Secure and Non-Secure State	<p>Defines whether the Bus and DMAC/DTC Error Clear Registers are write accessible for the Non-secure application.</p> <p>This setting is only valid when building projects with TrustZone.</p>
Security > System Reset Request Accessibility	<ul style="list-style-type: none"> <li>Both Secure and Non-Secure State</li> <li>Secure State</li> </ul>	Secure State	<p>Value for SCB-&gt;AIRCR register bit SYSRESETREQS. Defines whether the SYSRESETREQ bit is functional for Non-secure use.</p> <p>This setting is only valid when building projects with TrustZone.</p>
Security > System Reset Status	<ul style="list-style-type: none"> <li>Both Secure and Non-Secure State</li> </ul>	Both Secure and Non-Secure State	<p>Defines whether the reset status registers</p>

Accessibility	<ul style="list-style-type: none"> <li>State</li> <li>Secure State</li> </ul>		(RSTSRn) can be cleared from the Non-secure application.
			This setting is only valid when building projects with TrustZone.
Security > Battery Backup Accessibility	<ul style="list-style-type: none"> <li>Both Secure and Non-Secure State</li> <li>Secure State</li> </ul>	Both Secure and Non-Secure State	<p>Defines whether the battery backup registers are accessible for the Non-secure application. If Secure State is selected, all battery backup registers are read only except for VBTBKRn registers which are both read and write protected.</p> <p>This setting is only valid when building projects with TrustZone.</p>
OFS0 register settings > Independent WDT > Start Mode	<ul style="list-style-type: none"> <li>IWDT is Disabled</li> <li>IWDT is automatically activated after a reset (Autostart mode)</li> </ul>	IWDT is Disabled	
OFS0 register settings > Independent WDT > Timeout Period	<ul style="list-style-type: none"> <li>128 cycles</li> <li>512 cycles</li> <li>1024 cycles</li> <li>2048 cycles</li> </ul>	2048 cycles	
OFS0 register settings > Independent WDT > Dedicated Clock Frequency Divisor	<ul style="list-style-type: none"> <li>1</li> <li>16</li> <li>32</li> <li>64</li> <li>128</li> <li>256</li> </ul>	128	
OFS0 register settings > Independent WDT > Window End Position	<ul style="list-style-type: none"> <li>75%</li> <li>50%</li> <li>25%</li> <li>0% (no window end position)</li> </ul>	0% (no window end position)	
OFS0 register settings > Independent WDT > Window Start Position	<ul style="list-style-type: none"> <li>25%</li> <li>50%</li> <li>75%</li> </ul>	100% (no window start position)	

OFS0 register settings > Independent WDT > Reset Interrupt Request Select	<ul style="list-style-type: none"> <li>• 100% (no window start position)</li> <li>• NMI request or interrupt request is enabled</li> <li>• Reset is enabled</li> </ul>	Reset is enabled
OFS0 register settings > Independent WDT > Stop Control	<ul style="list-style-type: none"> <li>• Counting continues (Note: Device will not enter Deep Standby Mode when selected. Device will enter Software Standby Mode)</li> <li>• Stop counting when in Sleep, Snooze mode, or Software Standby</li> </ul>	Stop counting when in Sleep, Snooze mode, or Software Standby
OFS0 register settings > WDT > Start Mode Select	<ul style="list-style-type: none"> <li>• Automatically activate WDT after a reset (auto-start mode)</li> <li>• Stop WDT after a reset (register-start mode)</li> </ul>	Stop WDT after a reset (register-start mode)
OFS0 register settings > WDT > Timeout Period	<ul style="list-style-type: none"> <li>• 1024 cycles</li> <li>• 4096 cycles</li> <li>• 8192 cycles</li> <li>• 16384 cycles</li> </ul>	16384 cycles
OFS0 register settings > WDT > Clock Frequency Division Ratio	<ul style="list-style-type: none"> <li>• 4</li> <li>• 64</li> <li>• 128</li> <li>• 512</li> <li>• 2048</li> <li>• 8192</li> </ul>	128
OFS0 register settings > WDT > Window End Position	<ul style="list-style-type: none"> <li>• 75%</li> <li>• 50%</li> <li>• 25%</li> <li>• 0% (no window end position)</li> </ul>	0% (no window end position)
OFS0 register settings > WDT > Window Start Position	<ul style="list-style-type: none"> <li>• 25%</li> <li>• 50%</li> <li>• 75%</li> <li>• 100% (no</li> </ul>	100% (no window start position)

	window start position)		
OFS0 register settings > WDT > Reset Interrupt Request	<ul style="list-style-type: none"> <li>• NMI</li> <li>• Reset</li> </ul>	Reset	
OFS0 register settings > WDT > Stop Control	<ul style="list-style-type: none"> <li>• Counting continues</li> <li>• Stop counting when entering Sleep mode</li> </ul>	Stop counting when entering Sleep mode	
OFS1 register settings > Voltage Detection 0 Circuit Start	<ul style="list-style-type: none"> <li>• Voltage monitor 0 reset is enabled after reset</li> <li>• Voltage monitor 0 reset is disabled after reset</li> </ul>	Voltage monitor 0 reset is disabled after reset	
OFS1 register settings > Voltage Detection 0 Level	<ul style="list-style-type: none"> <li>• 2.94 V</li> <li>• 2.87 V</li> <li>• 2.80 V</li> </ul>	2.80 V	
OFS1 register settings > HOCO Oscillation Enable	<ul style="list-style-type: none"> <li>• HOCO oscillation is enabled after reset</li> <li>• HOCO oscillation is disabled after reset</li> </ul>	HOCO oscillation is disabled after reset	
Block Protection Settings (BPS) > BPS0	Refer to the RA Configuration tool for available options.	0U	Configure Block Protection Register 0
Block Protection Settings (BPS) > BPS1	<ul style="list-style-type: none"> <li>• Flash Block 32</li> <li>• Flash Block 33</li> <li>• Flash Block 34</li> <li>• Flash Block 35</li> <li>• Flash Block 36</li> <li>• Flash Block 37</li> </ul>	0U	Configure Block Protection Register 1
Block Protection Settings (BPS) > BPS2	Refer to the RA Configuration tool for available options.	0U	Configure Block Protection Register 2
Permanent Block Protection Settings (PBPS) > PBPS0	Refer to the RA Configuration tool for available options.	0U	Configure Permanent Block Protection Register 0
Permanent Block Protection Settings (PBPS) > PBPS1	<ul style="list-style-type: none"> <li>• Flash Block 32</li> <li>• Flash Block 33</li> <li>• Flash Block 34</li> <li>• Flash Block 35</li> <li>• Flash Block 36</li> </ul>	0U	Configure Permanent Block Protection Register 1



- Flash Block 37

Permanent Block Protection Settings (PBPS) > PBPS2

Refer to the RA Configuration tool for available options.

0U

Configure Permanent Block Protection Register 2

Dual Bank Mode

- Enabled
- Disabled

Disabled

Enabling dual bank mode splits the flash into two banks that can be swapped by programming the BANKSEL non-volatile register. When enabled, one bank will start at address 0x0 and the other will start at 0x200000. Each bank contains exactly half the capacity of the entire code flash. When Dual Bank mode is enabled, Startup Program Protection and Block Swap functions cannot be used.

### 4.1.3 BSP I/O access

#### BSP

#### Functions

`__STATIC_INLINE uint32_t R_BSP_PinRead (bsp_io_port_pin_t pin)`

`__STATIC_INLINE void R_BSP_PinWrite (bsp_io_port_pin_t pin, bsp_io_level_t level)`

`__STATIC_INLINE void R_BSP_PinAccessEnable (void)`

`__STATIC_INLINE void R_BSP_PinAccessDisable (void)`

#### Detailed Description

This module provides basic read/write access to port pins.

#### Enumerations

enum `bsp_io_level_t`

enum `bsp_io_direction_t`

enum `bsp_io_port_t`

```
enum bsp_io_port_pin_t
```

## Enumeration Type Documentation

### ◆ bsp\_io\_level\_t

enum bsp_io_level_t	
Levels that can be set and read for individual pins	
Enumerator	
BSP_IO_LEVEL_LOW	Low.
BSP_IO_LEVEL_HIGH	High.

### ◆ bsp\_io\_direction\_t

enum bsp_io_direction_t	
Direction of individual pins	
Enumerator	
BSP_IO_DIRECTION_INPUT	Input.
BSP_IO_DIRECTION_OUTPUT	Output.

◆ **bsp\_io\_port\_t**

enum <code>bsp_io_port_t</code>	
Superset list of all possible IO ports.	
Enumerator	
BSP_IO_PORT_00	IO port 0.
BSP_IO_PORT_01	IO port 1.
BSP_IO_PORT_02	IO port 2.
BSP_IO_PORT_03	IO port 3.
BSP_IO_PORT_04	IO port 4.
BSP_IO_PORT_05	IO port 5.
BSP_IO_PORT_06	IO port 6.
BSP_IO_PORT_07	IO port 7.
BSP_IO_PORT_08	IO port 8.
BSP_IO_PORT_09	IO port 9.
BSP_IO_PORT_10	IO port 10.
BSP_IO_PORT_11	IO port 11.

◆ **bsp\_io\_port\_pin\_t**

enum <code>bsp_io_port_pin_t</code>	
Superset list of all possible IO port pins.	
Enumerator	
BSP_IO_PORT_00_PIN_00	IO port 0 pin 0.
BSP_IO_PORT_00_PIN_01	IO port 0 pin 1.
BSP_IO_PORT_00_PIN_02	IO port 0 pin 2.
BSP_IO_PORT_00_PIN_03	IO port 0 pin 3.
BSP_IO_PORT_00_PIN_04	IO port 0 pin 4.

BSP_IO_PORT_00_PIN_05	IO port 0 pin 5.
BSP_IO_PORT_00_PIN_06	IO port 0 pin 6.
BSP_IO_PORT_00_PIN_07	IO port 0 pin 7.
BSP_IO_PORT_00_PIN_08	IO port 0 pin 8.
BSP_IO_PORT_00_PIN_09	IO port 0 pin 9.
BSP_IO_PORT_00_PIN_10	IO port 0 pin 10.
BSP_IO_PORT_00_PIN_11	IO port 0 pin 11.
BSP_IO_PORT_00_PIN_12	IO port 0 pin 12.
BSP_IO_PORT_00_PIN_13	IO port 0 pin 13.
BSP_IO_PORT_00_PIN_14	IO port 0 pin 14.
BSP_IO_PORT_00_PIN_15	IO port 0 pin 15.
BSP_IO_PORT_01_PIN_00	IO port 1 pin 0.
BSP_IO_PORT_01_PIN_01	IO port 1 pin 1.
BSP_IO_PORT_01_PIN_02	IO port 1 pin 2.
BSP_IO_PORT_01_PIN_03	IO port 1 pin 3.
BSP_IO_PORT_01_PIN_04	IO port 1 pin 4.
BSP_IO_PORT_01_PIN_05	IO port 1 pin 5.
BSP_IO_PORT_01_PIN_06	IO port 1 pin 6.
BSP_IO_PORT_01_PIN_07	IO port 1 pin 7.
BSP_IO_PORT_01_PIN_08	IO port 1 pin 8.
BSP_IO_PORT_01_PIN_09	IO port 1 pin 9.
BSP_IO_PORT_01_PIN_10	IO port 1 pin 10.
BSP_IO_PORT_01_PIN_11	IO port 1 pin 11.
BSP_IO_PORT_01_PIN_12	IO port 1 pin 12.

BSP_IO_PORT_01_PIN_13	IO port 1 pin 13.
BSP_IO_PORT_01_PIN_14	IO port 1 pin 14.
BSP_IO_PORT_01_PIN_15	IO port 1 pin 15.
BSP_IO_PORT_02_PIN_00	IO port 2 pin 0.
BSP_IO_PORT_02_PIN_01	IO port 2 pin 1.
BSP_IO_PORT_02_PIN_02	IO port 2 pin 2.
BSP_IO_PORT_02_PIN_03	IO port 2 pin 3.
BSP_IO_PORT_02_PIN_04	IO port 2 pin 4.
BSP_IO_PORT_02_PIN_05	IO port 2 pin 5.
BSP_IO_PORT_02_PIN_06	IO port 2 pin 6.
BSP_IO_PORT_02_PIN_07	IO port 2 pin 7.
BSP_IO_PORT_02_PIN_08	IO port 2 pin 8.
BSP_IO_PORT_02_PIN_09	IO port 2 pin 9.
BSP_IO_PORT_02_PIN_10	IO port 2 pin 10.
BSP_IO_PORT_02_PIN_11	IO port 2 pin 11.
BSP_IO_PORT_02_PIN_12	IO port 2 pin 12.
BSP_IO_PORT_02_PIN_13	IO port 2 pin 13.
BSP_IO_PORT_02_PIN_14	IO port 2 pin 14.
BSP_IO_PORT_02_PIN_15	IO port 2 pin 15.
BSP_IO_PORT_03_PIN_00	IO port 3 pin 0.
BSP_IO_PORT_03_PIN_01	IO port 3 pin 1.
BSP_IO_PORT_03_PIN_02	IO port 3 pin 2.
BSP_IO_PORT_03_PIN_03	IO port 3 pin 3.
BSP_IO_PORT_03_PIN_04	IO port 3 pin 4.

BSP_IO_PORT_03_PIN_05	IO port 3 pin 5.
BSP_IO_PORT_03_PIN_06	IO port 3 pin 6.
BSP_IO_PORT_03_PIN_07	IO port 3 pin 7.
BSP_IO_PORT_03_PIN_08	IO port 3 pin 8.
BSP_IO_PORT_03_PIN_09	IO port 3 pin 9.
BSP_IO_PORT_03_PIN_10	IO port 3 pin 10.
BSP_IO_PORT_03_PIN_11	IO port 3 pin 11.
BSP_IO_PORT_03_PIN_12	IO port 3 pin 12.
BSP_IO_PORT_03_PIN_13	IO port 3 pin 13.
BSP_IO_PORT_03_PIN_14	IO port 3 pin 14.
BSP_IO_PORT_03_PIN_15	IO port 3 pin 15.
BSP_IO_PORT_04_PIN_00	IO port 4 pin 0.
BSP_IO_PORT_04_PIN_01	IO port 4 pin 1.
BSP_IO_PORT_04_PIN_02	IO port 4 pin 2.
BSP_IO_PORT_04_PIN_03	IO port 4 pin 3.
BSP_IO_PORT_04_PIN_04	IO port 4 pin 4.
BSP_IO_PORT_04_PIN_05	IO port 4 pin 5.
BSP_IO_PORT_04_PIN_06	IO port 4 pin 6.
BSP_IO_PORT_04_PIN_07	IO port 4 pin 7.
BSP_IO_PORT_04_PIN_08	IO port 4 pin 8.
BSP_IO_PORT_04_PIN_09	IO port 4 pin 9.
BSP_IO_PORT_04_PIN_10	IO port 4 pin 10.
BSP_IO_PORT_04_PIN_11	IO port 4 pin 11.
BSP_IO_PORT_04_PIN_12	IO port 4 pin 12.

BSP_IO_PORT_04_PIN_13	IO port 4 pin 13.
BSP_IO_PORT_04_PIN_14	IO port 4 pin 14.
BSP_IO_PORT_04_PIN_15	IO port 4 pin 15.
BSP_IO_PORT_05_PIN_00	IO port 5 pin 0.
BSP_IO_PORT_05_PIN_01	IO port 5 pin 1.
BSP_IO_PORT_05_PIN_02	IO port 5 pin 2.
BSP_IO_PORT_05_PIN_03	IO port 5 pin 3.
BSP_IO_PORT_05_PIN_04	IO port 5 pin 4.
BSP_IO_PORT_05_PIN_05	IO port 5 pin 5.
BSP_IO_PORT_05_PIN_06	IO port 5 pin 6.
BSP_IO_PORT_05_PIN_07	IO port 5 pin 7.
BSP_IO_PORT_05_PIN_08	IO port 5 pin 8.
BSP_IO_PORT_05_PIN_09	IO port 5 pin 9.
BSP_IO_PORT_05_PIN_10	IO port 5 pin 10.
BSP_IO_PORT_05_PIN_11	IO port 5 pin 11.
BSP_IO_PORT_05_PIN_12	IO port 5 pin 12.
BSP_IO_PORT_05_PIN_13	IO port 5 pin 13.
BSP_IO_PORT_05_PIN_14	IO port 5 pin 14.
BSP_IO_PORT_05_PIN_15	IO port 5 pin 15.
BSP_IO_PORT_06_PIN_00	IO port 6 pin 0.
BSP_IO_PORT_06_PIN_01	IO port 6 pin 1.
BSP_IO_PORT_06_PIN_02	IO port 6 pin 2.
BSP_IO_PORT_06_PIN_03	IO port 6 pin 3.
BSP_IO_PORT_06_PIN_04	IO port 6 pin 4.

BSP_IO_PORT_06_PIN_05	IO port 6 pin 5.
BSP_IO_PORT_06_PIN_06	IO port 6 pin 6.
BSP_IO_PORT_06_PIN_07	IO port 6 pin 7.
BSP_IO_PORT_06_PIN_08	IO port 6 pin 8.
BSP_IO_PORT_06_PIN_09	IO port 6 pin 9.
BSP_IO_PORT_06_PIN_10	IO port 6 pin 10.
BSP_IO_PORT_06_PIN_11	IO port 6 pin 11.
BSP_IO_PORT_06_PIN_12	IO port 6 pin 12.
BSP_IO_PORT_06_PIN_13	IO port 6 pin 13.
BSP_IO_PORT_06_PIN_14	IO port 6 pin 14.
BSP_IO_PORT_06_PIN_15	IO port 6 pin 15.
BSP_IO_PORT_07_PIN_00	IO port 7 pin 0.
BSP_IO_PORT_07_PIN_01	IO port 7 pin 1.
BSP_IO_PORT_07_PIN_02	IO port 7 pin 2.
BSP_IO_PORT_07_PIN_03	IO port 7 pin 3.
BSP_IO_PORT_07_PIN_04	IO port 7 pin 4.
BSP_IO_PORT_07_PIN_05	IO port 7 pin 5.
BSP_IO_PORT_07_PIN_06	IO port 7 pin 6.
BSP_IO_PORT_07_PIN_07	IO port 7 pin 7.
BSP_IO_PORT_07_PIN_08	IO port 7 pin 8.
BSP_IO_PORT_07_PIN_09	IO port 7 pin 9.
BSP_IO_PORT_07_PIN_10	IO port 7 pin 10.
BSP_IO_PORT_07_PIN_11	IO port 7 pin 11.
BSP_IO_PORT_07_PIN_12	IO port 7 pin 12.



BSP_IO_PORT_07_PIN_13	IO port 7 pin 13.
BSP_IO_PORT_07_PIN_14	IO port 7 pin 14.
BSP_IO_PORT_07_PIN_15	IO port 7 pin 15.
BSP_IO_PORT_08_PIN_00	IO port 8 pin 0.
BSP_IO_PORT_08_PIN_01	IO port 8 pin 1.
BSP_IO_PORT_08_PIN_02	IO port 8 pin 2.
BSP_IO_PORT_08_PIN_03	IO port 8 pin 3.
BSP_IO_PORT_08_PIN_04	IO port 8 pin 4.
BSP_IO_PORT_08_PIN_05	IO port 8 pin 5.
BSP_IO_PORT_08_PIN_06	IO port 8 pin 6.
BSP_IO_PORT_08_PIN_07	IO port 8 pin 7.
BSP_IO_PORT_08_PIN_08	IO port 8 pin 8.
BSP_IO_PORT_08_PIN_09	IO port 8 pin 9.
BSP_IO_PORT_08_PIN_10	IO port 8 pin 10.
BSP_IO_PORT_08_PIN_11	IO port 8 pin 11.
BSP_IO_PORT_08_PIN_12	IO port 8 pin 12.
BSP_IO_PORT_08_PIN_13	IO port 8 pin 13.
BSP_IO_PORT_08_PIN_14	IO port 8 pin 14.
BSP_IO_PORT_08_PIN_15	IO port 8 pin 15.
BSP_IO_PORT_09_PIN_00	IO port 9 pin 0.
BSP_IO_PORT_09_PIN_01	IO port 9 pin 1.
BSP_IO_PORT_09_PIN_02	IO port 9 pin 2.
BSP_IO_PORT_09_PIN_03	IO port 9 pin 3.
BSP_IO_PORT_09_PIN_04	IO port 9 pin 4.

BSP_IO_PORT_09_PIN_05	IO port 9 pin 5.
BSP_IO_PORT_09_PIN_06	IO port 9 pin 6.
BSP_IO_PORT_09_PIN_07	IO port 9 pin 7.
BSP_IO_PORT_09_PIN_08	IO port 9 pin 8.
BSP_IO_PORT_09_PIN_09	IO port 9 pin 9.
BSP_IO_PORT_09_PIN_10	IO port 9 pin 10.
BSP_IO_PORT_09_PIN_11	IO port 9 pin 11.
BSP_IO_PORT_09_PIN_12	IO port 9 pin 12.
BSP_IO_PORT_09_PIN_13	IO port 9 pin 13.
BSP_IO_PORT_09_PIN_14	IO port 9 pin 14.
BSP_IO_PORT_09_PIN_15	IO port 9 pin 15.
BSP_IO_PORT_10_PIN_00	IO port 10 pin 0.
BSP_IO_PORT_10_PIN_01	IO port 10 pin 1.
BSP_IO_PORT_10_PIN_02	IO port 10 pin 2.
BSP_IO_PORT_10_PIN_03	IO port 10 pin 3.
BSP_IO_PORT_10_PIN_04	IO port 10 pin 4.
BSP_IO_PORT_10_PIN_05	IO port 10 pin 5.
BSP_IO_PORT_10_PIN_06	IO port 10 pin 6.
BSP_IO_PORT_10_PIN_07	IO port 10 pin 7.
BSP_IO_PORT_10_PIN_08	IO port 10 pin 8.
BSP_IO_PORT_10_PIN_09	IO port 10 pin 9.
BSP_IO_PORT_10_PIN_10	IO port 10 pin 10.
BSP_IO_PORT_10_PIN_11	IO port 10 pin 11.
BSP_IO_PORT_10_PIN_12	IO port 10 pin 12.

BSP_IO_PORT_10_PIN_13	IO port 10 pin 13.
BSP_IO_PORT_10_PIN_14	IO port 10 pin 14.
BSP_IO_PORT_10_PIN_15	IO port 10 pin 15.
BSP_IO_PORT_11_PIN_00	IO port 11 pin 0.
BSP_IO_PORT_11_PIN_01	IO port 11 pin 1.
BSP_IO_PORT_11_PIN_02	IO port 11 pin 2.
BSP_IO_PORT_11_PIN_03	IO port 11 pin 3.
BSP_IO_PORT_11_PIN_04	IO port 11 pin 4.
BSP_IO_PORT_11_PIN_05	IO port 11 pin 5.
BSP_IO_PORT_11_PIN_06	IO port 11 pin 6.
BSP_IO_PORT_11_PIN_07	IO port 11 pin 7.
BSP_IO_PORT_11_PIN_08	IO port 11 pin 8.
BSP_IO_PORT_11_PIN_09	IO port 11 pin 9.
BSP_IO_PORT_11_PIN_10	IO port 11 pin 10.
BSP_IO_PORT_11_PIN_11	IO port 11 pin 11.
BSP_IO_PORT_11_PIN_12	IO port 11 pin 12.
BSP_IO_PORT_11_PIN_13	IO port 11 pin 13.
BSP_IO_PORT_11_PIN_14	IO port 11 pin 14.
BSP_IO_PORT_11_PIN_15	IO port 11 pin 15.

## Function Documentation

---

◆ **R\_BSP\_PinRead()**

<code>__STATIC_INLINE uint32_t R_BSP_PinRead ( bsp_io_port_pin_t pin )</code>		
Read the current input level of the pin.		
<b>Parameters</b>		
[in]	pin	The pin
<b>Return values</b>		
Current	input level	

◆ **R\_BSP\_PinWrite()**

<code>__STATIC_INLINE void R_BSP_PinWrite ( bsp_io_port_pin_t pin, bsp_io_level_t level )</code>		
Set a pin to output and set the output level to the level provided		
<b>Parameters</b>		
[in]	pin	The pin
[in]	level	The level

◆ **R\_BSP\_PinAccessEnable()**

<code>__STATIC_INLINE void R_BSP_PinAccessEnable ( void )</code>		
Enable access to the PFS registers. Uses a reference counter to protect against interrupts that could occur via multiple threads or an ISR re-entering this code.		

◆ **R\_BSP\_PinAccessDisable()**

<code>__STATIC_INLINE void R_BSP_PinAccessDisable ( void )</code>		
Disable access to the PFS registers. Uses a reference counter to protect against interrupts that could occur via multiple threads or an ISR re-entering this code.		

## 4.2 Modules

### Detailed Description

Modules are the smallest unit of software available in the FSP. Each module implements one interface.

For more information on FSP Modules and Interfaces review [FSP Modules](#), [FSP Stacks](#) and [FSP Interfaces](#) in the FSP Architecture section of this manual.

## Organization of Module Sections

Each module within FSP has a detailed Users' Guide listed below. Each guide typically includes the following content:

- **Functions:** A list of all the API functions associated with the module
- **Detailed Description:** A short description of the module and the peripherals used
- **Overview:** An operational summary and a list of high level features provided by the module
- **Configuration:** A description of module specific settings available in the configuration tool including clock and pin configurations
- **Usage Notes:** Module specific documentation and limitations
- **Examples:** Illustrative code snippets that help the user better understand API use and operation
- **Data Structure and Enumeration:** Definitions for data structures, enumerations and similar elements used by the module API
- **Function Documentation:** Details on each API function, including the function prototype, a function summary, a simple use example, list of return values and links to documentation for any needed parameter definitions

## Modules

### [High-Speed Analog Comparator \(r\\_acmphs\)](#)

Driver for the ACMPHS peripheral on RA MCUs. This module implements the [Comparator Interface](#).

### [Low-Power Analog Comparator \(r\\_acmplp\)](#)

Driver for the ACMPLP peripheral on RA MCUs. This module implements the [Comparator Interface](#).

### [Analog to Digital Converter \(r\\_adc\)](#)

Driver for the ADC12, ADC14, and ADC16 peripherals on RA MCUs. This module implements the [ADC Interface](#).

### [Asynchronous General Purpose Timer \(r\\_agt\)](#)

Driver for the AGT peripheral on RA MCUs. This module implements the [Timer Interface](#).

### [Bluetooth Low Energy Library \(r\\_ble\)](#)

Driver for the Radio peripheral on RA MCUs. This module implements the [BLE Interface](#).

### [Clock Frequency Accuracy Measurement Circuit \(r\\_cac\)](#)

Driver for the CAC peripheral on RA MCUs. This module implements the [CAC Interface](#).

#### Controller Area Network (r\_can)

Driver for the CAN peripheral on RA MCUs. This module implements the [CAN Interface](#).

#### Clock Generation Circuit (r\_cgc)

Driver for the CGC peripheral on RA MCUs. This module implements the [CGC Interface](#).

#### Cyclic Redundancy Check (CRC) Calculator (r\_crc)

Driver for the CRC peripheral on RA MCUs. This module implements the [CRC Interface](#).

#### Capacitive Touch Sensing Unit (r\_ctsu)

This HAL driver supports the Capacitive Touch Sensing Unit (CTSUS). It implements the [CTSUS Interface](#).

#### Digital to Analog Converter (r\_dac)

Driver for the DAC12 peripheral on RA MCUs. This module implements the [DAC Interface](#).

#### Digital to Analog Converter (r\_dac8)

Driver for the DAC8 peripheral on RA MCUs. This module implements the [DAC Interface](#).

#### Direct Memory Access Controller (r\_dmac)

Driver for the DMAC peripheral on RA MCUs. This module implements the [Transfer Interface](#).

#### Data Operation Circuit (r\_doc)

Driver for the DOC peripheral on RA MCUs. This module implements the [DOC Interface](#).

#### D/AVE 2D Port Interface (r\_drw)

Driver for the DRW peripheral on RA MCUs. This module is a port of D/AVE 2D.

### Data Transfer Controller (r\_dtc)

Driver for the DTC peripheral on RA MCUs. This module implements the [Transfer Interface](#).

### Event Link Controller (r\_elc)

Driver for the ELC peripheral on RA MCUs. This module implements the [ELC Interface](#).

### Ethernet (r\_ether)

Driver for the Ethernet peripheral on RA MCUs. This module implements the [Ethernet Interface](#).

### Ethernet PHY (r\_ether\_phy)

The Ethernet PHY module (r\_ether\_phy) provides an API for standard Ethernet PHY communications applications that use the ETHERC peripheral. It implements the [Ethernet PHY Interface](#).

### High-Performance Flash Driver (r\_flash\_hp)

Driver for the flash memory on RA high-performance MCUs. This module implements the [Flash Interface](#).

### Low-Power Flash Driver (r\_flash\_lp)

Driver for the flash memory on RA low-power MCUs. This module implements the [Flash Interface](#).

### Graphics LCD Controller (r\_glcdc)

Driver for the GLCDC peripheral on RA MCUs. This module implements the [Display Interface](#).

### General PWM Timer (r\_gpt)

Driver for the GPT32 and GPT16 peripherals on RA MCUs. This module implements the [Timer Interface](#).

### General PWM Timer Three-Phase Motor Control Driver (r\_gpt\_three\_phase)

Driver for 3-phase motor control using the GPT peripheral on RA MCUs. This module implements the [Three-Phase Interface](#).

### Interrupt Controller Unit (r\_icu)

Driver for the ICU peripheral on RA MCUs. This module implements the [External IRQ Interface](#).

### I2C Master on IIC (r\_iic\_master)

Driver for the IIC peripheral on RA MCUs. This module implements the [I2C Master Interface](#).

### I2C Slave on IIC (r\_iic\_slave)

Driver for the IIC peripheral on RA MCUs. This module implements the [I2C Slave Interface](#).

### I/O Ports (r\_ioport)

Driver for the I/O Ports peripheral on RA MCUs. This module implements the [I/O Port Interface](#).

### Independent Watchdog Timer (r\_iwdt)

Driver for the IWDT peripheral on RA MCUs. This module implements the [WDT Interface](#).

### JPEG Codec (r\_jpeg)

Driver for the JPEG peripheral on RA MCUs. This module implements the [JPEG Codec Interface](#).

### Key Interrupt (r\_kint)

Driver for the KINT peripheral on RA MCUs. This module implements the [Key Matrix Interface](#).

### Low Power Modes (r\_lpm)

Driver for the LPM peripheral on RA MCUs. This module implements the [Low Power Modes Interface](#).

### Low Voltage Detection (r\_lvd)

Driver for the LVD peripheral on RA MCUs. This module implements the [Low Voltage Detection Interface](#).

### Operational Amplifier (r\_opamp)



Driver for the OPAMP peripheral on RA MCUs. This module implements the [OPAMP Interface](#).

#### [Octa Serial Peripheral Interface Flash \(r\\_ospi\)](#)

Driver for the OSPI peripheral on RA MCUs. This module implements the [SPI Flash Interface](#).

#### [Parallel Data Capture \(r\\_pdc\)](#)

Driver for the PDC peripheral on RA MCUs. This module implements the [PDC Interface](#).

#### [Port Output Enable for GPT \(r\\_poeg\)](#)

Driver for the POEG peripheral on RA MCUs. This module implements the [POEG Interface](#).

#### [Quad Serial Peripheral Interface Flash \(r\\_qspi\)](#)

Driver for the QSPI peripheral on RA MCUs. This module implements the [SPI Flash Interface](#).

#### [Realtime Clock \(r\\_rtc\)](#)

Driver for the RTC peripheral on RA MCUs. This module implements the [RTC Interface](#).

#### [Serial Communications Interface \(SCI\) I2C \(r\\_sci\\_i2c\)](#)

Driver for the SCI peripheral on RA MCUs. This module implements the [I2C Master Interface](#).

#### [Serial Communications Interface \(SCI\) SPI \(r\\_sci\\_spi\)](#)

Driver for the SCI peripheral on RA MCUs. This module implements the [SPI Interface](#).

#### [Serial Communications Interface \(SCI\) UART \(r\\_sci\\_uart\)](#)

Driver for the SCI peripheral on RA MCUs. This module implements the [UART Interface](#).

#### [Sigma Delta Analog to Digital Converter \(r\\_sdadc\)](#)

Driver for the SDADC24 peripheral on RA MCUs. This module

implements the [ADC Interface](#).

#### [SD/MMC Host Interface \(r\\_sdhi\)](#)

Driver for the SD/MMC Host Interface (SDHI) peripheral on RA MCUs. This module implements the [SD/MMC Interface](#).

#### [Segment LCD Controller \(r\\_slcdc\)](#)

Driver for the SLCDC peripheral on RA MCUs. This module implements the [SLCDC Interface](#).

#### [Serial Peripheral Interface \(r\\_spi\)](#)

Driver for the SPI peripheral on RA MCUs. This module implements the [SPI Interface](#).

#### [Serial Sound Interface \(r\\_ssi\)](#)

Driver for the SSIE peripheral on RA MCUs. This module implements the [I2S Interface](#).

#### [USB \(r\\_usb\\_basic\)](#)

Driver for the USB peripheral on RA MCUs. This module implements the [USB Interface](#).

#### [USB Host Communications Device Class Driver \(r\\_usb\\_hcdc\)](#)

This module provides a USB Host Communications Device Class (HDCD) driver. It implements the [USB HDCD Interface](#).

#### [USB Host Human Interface Device Class Driver \(r\\_usb\\_hhid\)](#)

This module provides a USB Host Human Interface Device Class Driver (HHID). It implements the [USB HHID Interface](#).

#### [USB Host Mass Storage Class Driver \(r\\_usb\\_hmsc\)](#)

This module provides a USB Host Mass Storage Class (HMSC) driver. It implements the [USB HMSC Interface](#).

#### [USB Peripheral Communications Device Class \(r\\_usb\\_pcdc\)](#)

This module provides a USB Peripheral Communications Device Class Driver (PCDC). It implements the [USB PCDC Interface](#).

### USB Peripheral Human Interface Device Class (r\_usb\_phid)

This module is USB Peripheral Human Interface Device Class Driver (PHID). It implements the [USB PHID Interface](#).

### USB Peripheral Mass Storage Class (r\_usb\_pmesc)

This module provides a USB Peripheral Mass Storage Class (PMSC) driver. It implements the [USB PMSC Interface](#).

### Watchdog Timer (r\_wdt)

Driver for the WDT peripheral on RA MCUs. This module implements the [WDT Interface](#).

### AWS PKCS11 PAL (rm\_aws\_pkcs11\_pal)

PKCS#11 PAL layer implementation for use by FreeRTOS TLS.

### AWS PKCS11 PAL LITTLEFS (rm\_aws\_pkcs11\_pal\_littlefs)

PKCS#11 PAL LittleFS layer implementation for use by FreeRTOS TLS.

### Bluetooth Low Energy Abstraction (rm\_ble\_abs)

Middleware for the Bluetooth peripheral on RA MCUs. This module implements the [BLE ABS Interface](#).

### SD/MMC Block Media Implementation (rm\_block\_media\_sdmmc)

Middleware to implement the block media interface on SD cards. This module implements the [Block Media Interface](#).

### USB HMSC Block Media Implementation (rm\_block\_media\_usb)

Middleware to implement the block media interface on USB mass storage devices. This module implements the [Block Media Interface](#).

### SEGGER emWin Port (rm\_emwin\_port)

SEGGER emWin port for RA MCUs.

### FreeRTOS+FAT Port (rm\_freertos\_plus\_fat)

Middleware for the FAT File System control on RA MCUs.

[FreeRTOS Plus TCP \(rm\\_freertos\\_plus\\_tcp\)](#)

Middleware for using TCP on RA MCUs.

[FreeRTOS Port \(rm\\_freertos\\_port\)](#)

FreeRTOS port for RA MCUs.

[RTOS Context Management \(rm\\_tz\\_context\)](#)

RTOS Context Management for RA MCUs.

[LittleFS Flash Port \(rm\\_littlefs\\_flash\)](#)

Middleware for the LittleFS File System control on RA MCUs.

[Motor Current \(rm\\_motor\\_current\)](#)

Calculation process for the motor control on RA MCUs. This module implements the [Interface](#).

[Motor Driver \(rm\\_motor\\_driver\)](#)

Calculation process for the motor control on RA MCUs. This module implements the [MOTOR\\_DRIVER Interface](#).

[Motor Angle and Speed Estimation \(rm\\_motor\\_estimate\)](#)

Calculation process for the motor control on RA MCUs. This module implements the [MOTOR\\_ANGLE Interface](#).

[Motor Speed \(rm\\_motor\\_speed\)](#)

Calculation process for the motor control on RA MCUs. This module implements the [MOTOR\\_SPEED Interface](#).

[Crypto Middleware \(rm\\_psa\\_crypto\)](#)

Hardware acceleration for the mbedCrypto implementation of the ARM PSA Crypto API.

[Capacitive Touch Middleware \(rm\\_touch\)](#)

This module supports the Capacitive Touch Sensing Unit (CTSUS). It implements the [Touch Middleware Interface](#).

### Virtual EEPROM (rm\_vee\_flash)

Virtual EEPROM on RA MCUs. This module implements the [Virtual EEPROM Interface](#).

### AWS Device Provisioning

AWS Device Provisioning example software.

### AWS MQTT

This module provides the AWS MQTT integration documentation.

### Wifi Middleware (rm\_wifi\_onchip\_silex)

Wifi and Socket implementation using the Silex SX-ULPGN WiFi module on RA MCUs.

### AWS Secure Sockets

This module provides the AWS Secure Sockets implementation.

## 4.2.1 High-Speed Analog Comparator (r\_acmphs)

### Modules

#### Functions

fsp\_err\_t R\_ACMPHS\_Open (comparator\_ctrl\_t \*p\_ctrl, comparator\_cfg\_t const \*const p\_cfg)

fsp\_err\_t R\_ACMPHS\_OutputEnable (comparator\_ctrl\_t \*const p\_ctrl)

fsp\_err\_t R\_ACMPHS\_InfoGet (comparator\_ctrl\_t \*const p\_ctrl, comparator\_info\_t \*const p\_info)

fsp\_err\_t R\_ACMPHS\_StatusGet (comparator\_ctrl\_t \*const p\_ctrl, comparator\_status\_t \*const p\_status)

fsp\_err\_t R\_ACMPHS\_Close (comparator\_ctrl\_t \*const p\_ctrl)

fsp\_err\_t R\_ACMPHS\_VersionGet (fsp\_version\_t \*const p\_version)

#### Detailed Description

Driver for the ACPHPS peripheral on RA MCUs. This module implements the [Comparator Interface](#).

## Overview

### Features

The ACPHPS HAL module supports the following features:

- Callback on rising edge, falling edge or both
- Configurable debounce filter
- Option for comparator output on VCOOUT pin
- ELC event output

## Configuration

### Build Time Configurations for r\_acmphs

The following build time configurations are defined in fsp\_cfg/r\_acmphs\_cfg.h:

Configuration	Options	Default	Description
Parameter Checking	<ul style="list-style-type: none"> <li>• Default (BSP)</li> <li>• Enabled</li> <li>• Disabled</li> </ul>	Default (BSP)	If selected code for parameter checking is included in the build.

### Configurations for Driver > Analog > Comparator Driver on r\_acmphs

This module can be added to the Stacks tab via New Stack > Driver > Analog > Comparator Driver on r\_acmphs.

Configuration	Options	Default	Description
Name	Name must be a valid C symbol	g_comparator0	Module name.
Channel	Value must be a non-negative integer	0	Select the hardware channel.
Trigger Edge Selector	<ul style="list-style-type: none"> <li>• Rising</li> <li>• Falling</li> <li>• Both Edge</li> </ul>	Both Edge	The trigger specifies when a comparator callback event should occur. Unused if the interrupt priority is disabled or the callback is NULL.
Noise Filter	<ul style="list-style-type: none"> <li>• No Filter</li> <li>• 8</li> <li>• 16</li> <li>• 32</li> </ul>	No Filter	Select the PCLK divisor for the hardware digital debounce filter. Larger divisors provide a longer debounce and take longer for the output to update.

Maximum status retries (CMPMON)	Must be a valid non-negative integer between 2 and 32-bit maximum value	1024	Maximum number of status retries.
Output Polarity	<ul style="list-style-type: none"> <li>• Not Inverted</li> <li>• Inverted</li> </ul>	Not Inverted	When enabled comparator output is inverted. This affects the output read from <a href="#">R_ACMPHS_StatusGet()</a> , the pin output level, and the edge trigger.
Pin Output(VCOUT)	<ul style="list-style-type: none"> <li>• Disabled</li> <li>• Enabled</li> </ul>	Disabled	Turn this on to include the output from this comparator on VCOUT. The comparator output on VCOUT is OR'd with output from all other ACMPHS and ACMPLP comparators.
Callback	Name must be a valid C symbol	NULL	Define this function in the application. It is called when the Trigger event occurs.
Comparator Interrupt Priority	MCU Specific Options		Select the interrupt priority for the comparator interrupt.
Analog Input Voltage Source (IVCMP)	MCU Specific Options		Select the Analog input voltage source. Channel mentioned in the options represents channel in ACMPHS
Reference Voltage Input Source (IVREF)	MCU Specific Options		Select the Analog reference voltage source. Channel mentioned in the options represents channel in ACMPHS

## Clock Configuration

The ACMPHS peripheral is clocked from PCLKB. You can set the PCLKB frequency using the **Clocks** tab of the RA Configuration editor or by using the CGC Interface at run-time.

## Pin Configuration

Comparator output can be enabled or disabled on each channel individually. The VCOUT pin is a logical OR of all comparator outputs.

The IVCMPn pins are used as comparator inputs. The IVREFn pins are used as comparator reference values.

## Usage Notes

### Noise Filter

When the noise filter is enabled, the ACMPHP0/ACMPHP1 signal is sampled three times based on the sampling clock selected. The filter clock frequency is determined by PCLKB and the `comparator_filter_t` setting.

### Output Polarity

If output polarity is configured as "Inverted" then the VCOUT signal will be inverted and the `R_ACMPHS_StatusGet()` will return an inverted status.

### Limitations

- Once the analog comparator is configured, the program must wait for the stabilization time to elapse before using the comparator.
- When the noise filter is not enabled the hardware requires software debouncing of the output (two consecutive equal values). This is automatically managed in `R_ACMPHS_StatusGet` but may result in delay or an API error in rare edge cases.
- Constraints apply on the simultaneous use of ACMPHS analog input and ADC analog input. Refer to the "Usage Notes" section in your MCU's User's Manual for the ADC unit(s) for more details.
- To allow ACMPHS0 to cancel Software Standby mode or enter Snooze, set the CSTEN bit to 1 and the CDFS bits to 00 in the CMPCTL0 register.

## Examples

### Basic Example

The following is a basic example of minimal use of the ACMPHS. The comparator is configured to trigger a callback when the input rises above the internal reference voltage (VREF). A GPIO output acts as the comparator input and is externally connected to the IVCMP input of the ACMPHS.

```
/* Connect this control pin to the VCMP input of the comparator. This can be any GPIO
pin
 * that is not input only. */
#define ACMPHS_EXAMPLE_CONTROL_PIN (BSP_IO_PORT_05_PIN_03)
#define ADC_PGA_BYPASS_VALUE (0x9999)
volatile uint32_t g_comparator_events = 0U;
/* This callback is called when a comparator event occurs. */
void acmphs_example_callback (comparator_callback_args_t * p_args)
{
    FSP_PARAMETER_NOT_USED(p_args);
    g_comparator_events++;
}
```



```
void acmphs_example ()
{
    fsp_err_t err = FSP_SUCCESS;

    /* Disable pin register write protection, if enabled */
    R_BSP_PinAccessEnable();

    /* Start with the VCMP pin low. This example assumes the comparator is configured to
trigger
    * when VCMP rises above VREF. */
    (void) R_BSP_PinWrite(ACMPHS_EXAMPLE_CONTROL_PIN, BSP_IO_LEVEL_LOW);

    /* Initialize the ACMPHS module */
    err = R_ACMPHS_Open(&g_comparator_ctrl, &g_comparator_cfg);

    /* Handle any errors. This function should be defined by the user. */
    handle_error(err);

    /* Bypass PGA on ADC unit 0.
    * (See Table 50.2 "Input source configuration of the ACMPHS" in the RA6M3 User's
Manual (R01UH0886EJ0100)) */
    R_BSP_MODULE_START(FSP_IP_ADC, 0);

    R_ADC0->ADPGACR = ADC_PGA_BYPASS_VALUE;

    R_ADC0->ADPGADCR0 = 0;

    /* Wait for the minimum stabilization wait time before enabling output. */
    comparator_info_t info;
    R_ACMPHS_InfoGet(&g_comparator_ctrl, &info);
    R_BSP_SoftwareDelay(info.min_stabilization_wait_us, BSP_DELAY_UNITS_MICROSECONDS);

    /* Enable the comparator output */
    (void) R_ACMPHS_OutputEnable(&g_comparator_ctrl);

    /* Set the VCMP pin high. */
    (void) R_BSP_PinWrite(ACMPHS_EXAMPLE_CONTROL_PIN, BSP_IO_LEVEL_HIGH);

    while (0 == g_comparator_events)
    {
        /* Wait for interrupt. */
    }

    comparator_status_t status;

    /* Check status of comparator, Status will be COMPARATOR_STATE_OUTPUT_HIGH */
    (void) R_ACMPHS_StatusGet(&g_comparator_ctrl, &status);
}
```

}

## Function Documentation

### ◆ R\_ACMPHS\_Open()

```
fsp_err_t R_ACMPHS_Open ( comparator_ctrl_t *const p_ctrl, comparator_cfg_t const *const p_cfg )
```

Configures the comparator and starts operation. Callbacks and pin output are not active until `outputEnable()` is called. `comparator_api_t::outputEnable()` should be called after the output has stabilized. Implements `comparator_api_t::open()`.

Comparator inputs must be configured in the application code prior to calling this function.

#### Return values

FSP_SUCCESS	Open successful.
FSP_ERR_ASSERTION	An input pointer is NULL
FSP_ERR_INVALID_ARGUMENT	An argument is invalid. Window mode (COMPARATOR_MODE_WINDOW) and filter of 1 (COMPARATOR_FILTER_1) are not supported in this implementation.
FSP_ERR_ALREADY_OPEN	The control block is already open or the hardware lock is taken.

### ◆ R\_ACMPHS\_OutputEnable()

```
fsp_err_t R_ACMPHS_OutputEnable ( comparator_ctrl_t *const p_ctrl)
```

Enables the comparator output, which can be polled using `comparator_api_t::statusGet()`. Also enables pin output and interrupts as configured during `comparator_api_t::open()`. Implements `comparator_api_t::outputEnable()`.

#### Return values

FSP_SUCCESS	Comparator output is enabled.
FSP_ERR_ASSERTION	An input pointer was NULL.
FSP_ERR_NOT_OPEN	Instance control block is not open.

◆ **R\_ACMPHS\_InfoGet()**

```
fsp_err_t R_ACMPHS_InfoGet ( comparator_ctrl_t *const p_ctrl, comparator_info_t *const p_info )
```

Provides the minimum stabilization wait time in microseconds. Implements `comparator_api_t::infoGet()`.

**Return values**

FSP_SUCCESS	Information stored in p_info.
FSP_ERR_ASSERTION	An input pointer was NULL.
FSP_ERR_NOT_OPEN	Instance control block is not open.

◆ **R\_ACMPHS\_StatusGet()**

```
fsp_err_t R_ACMPHS_StatusGet ( comparator_ctrl_t *const p_ctrl, comparator_status_t *const p_status )
```

Provides the operating status of the comparator. Implements `comparator_api_t::statusGet()`.

**Return values**

FSP_SUCCESS	Operating status of the comparator is provided in p_status.
FSP_ERR_ASSERTION	An input pointer was NULL.
FSP_ERR_NOT_OPEN	Instance control block is not open.
FSP_ERR_TIMEOUT	The debounce filter is off and 2 consecutive matching values were not read within 1024 attempts.

◆ **R\_ACMPHS\_Close()**

```
fsp_err_t R_ACMPHS_Close ( comparator_ctrl_t * p_ctrl)
```

Stops the comparator. Implements `comparator_api_t::close()`.

**Return values**

FSP_SUCCESS	Instance control block closed successfully.
FSP_ERR_ASSERTION	An input pointer was NULL.
FSP_ERR_NOT_OPEN	Instance control block is not open.

**◆ R\_ACMPHS\_VersionGet()**

```
fsp_err_t R_ACMPHS_VersionGet ( fsp_version_t *const p_version)
```

Gets the API and code version. Implements [comparator\\_api\\_t::versionGet\(\)](#).

**Return values**

FSP_SUCCESS	Version information available in p_version.
FSP_ERR_ASSERTION	The parameter p_version is NULL.

**4.2.2 Low-Power Analog Comparator (r\_acmplp)**

## Modules

**Functions**

```
fsp_err_t R_ACMPPLP_Open (comparator_ctrl_t *const p_ctrl, comparator_cfg_t
const *const p_cfg)
```

```
fsp_err_t R_ACMPPLP_OutputEnable (comparator_ctrl_t *const p_ctrl)
```

```
fsp_err_t R_ACMPPLP_InfoGet (comparator_ctrl_t *const p_ctrl,
comparator_info_t *const p_info)
```

```
fsp_err_t R_ACMPPLP_StatusGet (comparator_ctrl_t *const p_ctrl,
comparator_status_t *const p_status)
```

```
fsp_err_t R_ACMPPLP_Close (comparator_ctrl_t *const p_ctrl)
```

```
fsp_err_t R_ACMPPLP_VersionGet (fsp_version_t *const p_version)
```

**Detailed Description**

Driver for the ACMPLP peripheral on RA MCUs. This module implements the [Comparator Interface](#).

**Overview****Features**

The ACMPLP HAL module supports the following features:

- Normal mode or window mode
- Callback on rising edge, falling edge or both
- Configurable debounce filter
- Option for comparator output on VCOOUT pin

- ELC event output

## Configuration

### Build Time Configurations for r\_acmplp

The following build time configurations are defined in fsp\_cfg/r\_acmplp\_cfg.h:

Configuration	Options	Default	Description
Parameter Checking	<ul style="list-style-type: none"> <li>• Default (BSP)</li> <li>• Enabled</li> <li>• Disabled</li> </ul>	Default (BSP)	If selected code for parameter checking is included in the build.
Reference Voltage Selection for ACMPLP1 (Standard mode only)	<ul style="list-style-type: none"> <li>• IVREF0</li> <li>• IVREF1</li> </ul>	IVREF1	ACMPLP1 may optionally be configured to use IVREF0 as a reference input instead of IVREF1. Note that if IVREF0 is selected, ACMPLP0 and ACMPLP1 must use the same setting for IVREF.

### Configurations for Driver > Analog > Comparator Driver on r\_acmplp

This module can be added to the Stacks tab via New Stack > Driver > Analog > Comparator Driver on r\_acmplp.

Configuration	Options	Default	Description
Name	Name must be a valid C symbol	g_comparator0	Module name.
Channel	Value must be a non-negative integer	0	Select the hardware channel.
Mode	<ul style="list-style-type: none"> <li>• Standard</li> <li>• Window</li> </ul>	Standard	In standard mode, comparator output is high if VCMP > VREF. In window mode, comparator output is high if VCMP is outside the range of VREF0 to VREF1.
Trigger	<ul style="list-style-type: none"> <li>• Rising</li> <li>• Falling</li> <li>• Both Edge</li> </ul>	Both Edge	The trigger specifies when a comparator callback event should occur. Unused if the interrupt priority is disabled or the callback is NULL.

Filter	<ul style="list-style-type: none"> <li>No sampling (bypass)</li> <li>Sampling at PCLKB</li> <li>Sampling at PCLKB/8</li> <li>Sampling at PCLKB/32</li> </ul>	No sampling (bypass)	Select the PCLK divisor for the hardware digital debounce filter. Larger divisors provide a longer debounce and take longer for the output to update.
Output Polarity	<ul style="list-style-type: none"> <li>Not Inverted</li> <li>Inverted</li> </ul>	Not Inverted	When enabled comparator output is inverted. This affects the output read from <a href="#">R_ACMLP_StatusGet()</a> , the pin output level, and the edge trigger.
Pin Output (VCOUT)	<ul style="list-style-type: none"> <li>Disabled</li> <li>Enabled</li> </ul>	Disabled	Turn this on to include the output from this comparator on VCOUT. The comparator output on VCOUT is OR'd with output from all other ACMPLP and ACMPLP comparators.
Vref (Standard mode only)	<ul style="list-style-type: none"> <li>Enabled</li> <li>Disabled</li> </ul>	Disabled	If reference voltage selection is enabled then internal reference voltage is used as comparator input
Callback	Name must be a valid C symbol	NULL	Define this function in the application. It is called when the Trigger event occurs.
Comparator Interrupt Priority	MCU Specific Options		Select the interrupt priority for the comparator interrupt.
Analog Input Voltage Source (IVCMP)	MCU Specific Options		Select the comparator input source. Only options for the configured channel are valid.
Reference Voltage Input Source (IVREF)	MCU Specific Options		Select the comparator reference voltage source.  If channel 1 is selected and the 'Reference Voltage Selection (ACMPLP1)' config option is set to IVREF0, select one of the Channel 0 options.

In all other cases, only options for the configured channel are valid.

## Clock Configuration

The ACMPLP peripheral is clocked from PCLKB. You can set the PCLKB frequency using the **Clocks** tab of the RA Configuration editor or by using the CGC Interface at run-time.

## Pin Configuration

Comparator output can be enabled or disabled on each channel individually. The VCOUT pin is a logical OR of all comparator outputs.

The CMPINn pins are used as comparator inputs. The CMPREFn pins are used as comparator reference values.

## Usage Notes

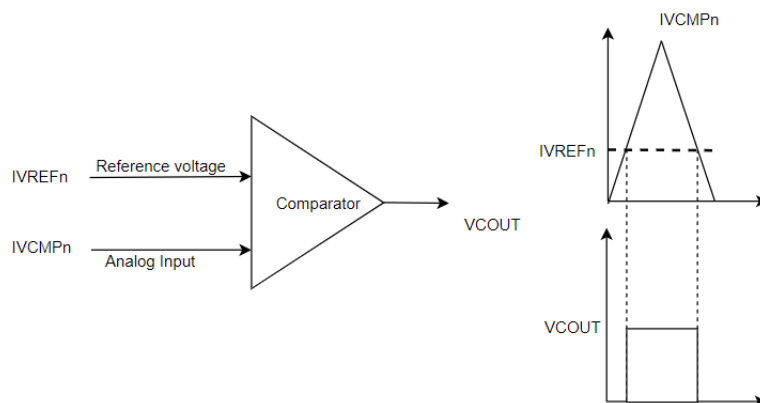


Figure 145: ACMPLP Standard Mode Operation

## Noise Filter

When the noise filter is enabled, the ACMPLP0/ACMPLP1 signal is sampled three times based on the sampling clock selected. The filter clock frequency is determined by PCLKB and the `comparator_filter_t` setting.

## Output Polarity

If output polarity is configured as "Inverted" then the VCOUT signal will be inverted and the `R_ACMPLP_StatusGet()` will return an inverted status.

## Window Mode

In window mode, the comparator indicates if the analog input voltage falls within the window (low and high reference voltage) or is outside the window.

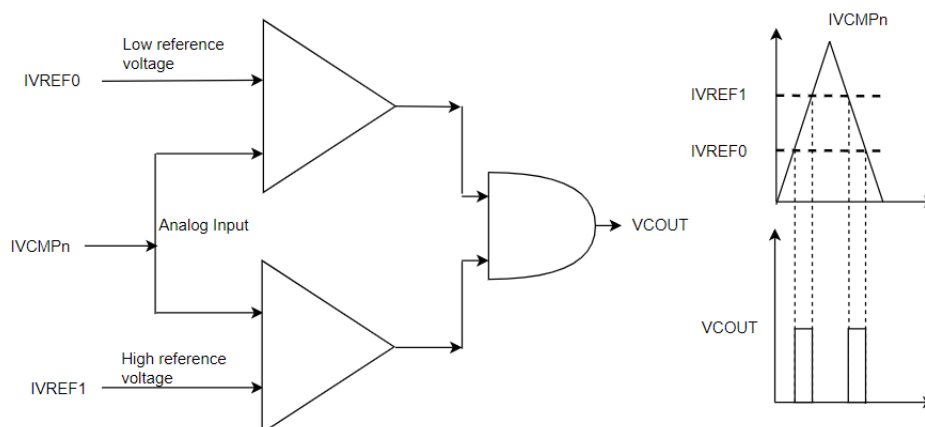


Figure 146: ACMLP Window Mode Operation

## Limitations

- Once the analog comparator is configured, the program must wait for the stabilization time to elapse before using the comparator.
- Low speed is not supported by the ACMLP driver.

## Examples

### Basic Example

The following is a basic example of minimal use of the ACMLP. The comparator is configured to trigger a callback when the input rises above the internal reference voltage (VREF). A GPIO output acts as the comparator input and is externally connected to the CMPIN input of the ACMLP.

```

/* Connect this control pin to the VCMP input of the comparator. This can be any GPIO
pin
 * that is not input only. */
#define ACMLP_EXAMPLE_CONTROL_PIN (BSP_IO_PORT_04_PIN_08)
volatile uint32_t g_comparator_events = 0U;
/* This callback is called when a comparator event occurs. */
void acmplp_example_callback (comparator_callback_args_t * p_args)
{
    FSP_PARAMETER_NOT_USED(p_args);
    g_comparator_events++;
}
void acmplp_example ()
{
    fsp_err_t err = FSP_SUCCESS;

    /* Disable pin register write protection, if enabled */

```



```
R_BSP_PinAccessEnable();

/* Start with the VCMP pin low. This example assumes the comparator is configured to
trigger
 * when VCMP rises above VREF. */
(void) R_BSP_PinWrite(ACMPLP_EXAMPLE_CONTROL_PIN, BSP_IO_LEVEL_LOW);
/* Initialize the ACMPLP module */
err = R_ACMPLP_Open(&g_comparator_ctrl, &g_comparator_cfg);
/* Handle any errors. This function should be defined by the user. */
handle_error(err);
/* Wait for the minimum stabilization wait time before enabling output. */
comparator_info_t info;
R_ACMPLP_InfoGet(&g_comparator_ctrl, &info);
R_BSP_SoftwareDelay(info.min_stabilization_wait_us, BSP_DELAY_UNITS_MICROSECONDS);
/* Enable the comparator output */
(void) R_ACMPLP_OutputEnable(&g_comparator_ctrl);
/* Set VCMP low. */
(void) R_BSP_PinWrite(ACMPLP_EXAMPLE_CONTROL_PIN, BSP_IO_LEVEL_HIGH);
while (0 == g_comparator_events)
{
/* Wait for interrupt. */
}
comparator_status_t status;
/* Check status of comparator, Status will be COMPARATOR_STATE_OUTPUT_HIGH */
(void) R_ACMPLP_StatusGet(&g_comparator_ctrl, &status);
}
```

## Enumerations

enum [acmplp\\_input\\_t](#)

enum [acmplp\\_reference\\_t](#)

## Enumeration Type Documentation

◆ **acmplp\_input\_t**

enum acmplp_input_t	
Enumerator	
ACMPLP_INPUT_AMPO	Not available on all MCUs.
ACMPLP_INPUT_CMPIN_1	Not available on all MCUs.

◆ **acmplp\_reference\_t**

enum acmplp_reference_t	
Enumerator	
ACMPLP_REFERENCE_CMPREF_1	Not available on all MCUs.

**Function Documentation**◆ **R\_ACMPLP\_Open()**

`fsp_err_t R_ACMPLP_Open ( comparator_ctrl_t *const p_ctrl, comparator_cfg_t const *const p_cfg )`

Configures the comparator and starts operation. Callbacks and pin output are not active until `outputEnable()` is called. `comparator_api_t::outputEnable()` should be called after the output has stabilized. Implements `comparator_api_t::open()`.

Comparator inputs must be configured in the application code prior to calling this function.

**Return values**

FSP_SUCCESS	Open successful.
FSP_ERR_ASSERTION	An input pointer is NULL
FSP_ERR_INVALID_ARGUMENT	An argument is invalid. Window mode (COMPARATOR_MODE_WINDOW) and filter of 1 (COMPARATOR_FILTER_1) are not supported in this implementation. <code>p_cfg-&gt;p_callback</code> is not NULL, but ISR is not enabled. ISR must be enabled to use callback function.
FSP_ERR_ALREADY_OPEN	The control block is already open or the hardware lock is taken.
FSP_ERR_IN_USE	The channel is already in use.

◆ **R\_ACMLP\_OutputEnable()**

```
fsp_err_t R_ACMLP_OutputEnable ( comparator_ctrl_t *const p_ctrl)
```

Enables the comparator output, which can be polled using `comparator_api_t::statusGet()`. Also enables pin output and interrupts as configured during `comparator_api_t::open()`. Implements `comparator_api_t::outputEnable()`.

**Return values**

FSP_SUCCESS	Comparator output is enabled.
FSP_ERR_ASSERTION	An input pointer was NULL.
FSP_ERR_NOT_OPEN	Instance control block is not open.

◆ **R\_ACMLP\_InfoGet()**

```
fsp_err_t R_ACMLP_InfoGet ( comparator_ctrl_t *const p_ctrl, comparator_info_t *const p_info )
```

Provides the minimum stabilization wait time in microseconds. Implements `comparator_api_t::infoGet()`.

**Return values**

FSP_SUCCESS	Information stored in p_info.
FSP_ERR_ASSERTION	An input pointer was NULL.
FSP_ERR_NOT_OPEN	Instance control block is not open.

◆ **R\_ACMLP\_StatusGet()**

```
fsp_err_t R_ACMLP_StatusGet ( comparator_ctrl_t *const p_ctrl, comparator_status_t *const p_status )
```

Provides the operating status of the comparator. Implements `comparator_api_t::statusGet()`.

**Return values**

FSP_SUCCESS	Operating status of the comparator is provided in p_status.
FSP_ERR_ASSERTION	An input pointer was NULL.
FSP_ERR_NOT_OPEN	Instance control block is not open.

◆ **R\_ACMLP\_Close()**

```
fsp_err_t R_ACMLP_Close ( comparator_ctrl_t * p_ctrl)
```

Stops the comparator. Implements `comparator_api_t::close()`.

**Return values**

FSP_SUCCESS	Instance control block closed successfully.
FSP_ERR_ASSERTION	An input pointer was NULL.
FSP_ERR_NOT_OPEN	Instance control block is not open.

◆ **R\_ACMLP\_VersionGet()**

```
fsp_err_t R_ACMLP_VersionGet ( fsp_version_t *const p_version)
```

Gets the API and code version. Implements `comparator_api_t::versionGet()`.

**Return values**

FSP_SUCCESS	Version information available in p_version.
FSP_ERR_ASSERTION	The parameter p_version is NULL.

**4.2.3 Analog to Digital Converter (r\_adc)**

## Modules

**Functions**

```
fsp_err_t R_ADC_Open (adc_ctrl_t *p_ctrl, adc_cfg_t const *const p_cfg)
```

```
fsp_err_t R_ADC_ScanCfg (adc_ctrl_t *p_ctrl, void const *const p_extend)
```

```
fsp_err_t R_ADC_InfoGet (adc_ctrl_t *p_ctrl, adc_info_t *p_adc_info)
```

```
fsp_err_t R_ADC_ScanStart (adc_ctrl_t *p_ctrl)
```

```
fsp_err_t R_ADC_ScanStop (adc_ctrl_t *p_ctrl)
```

```
fsp_err_t R_ADC_StatusGet (adc_ctrl_t *p_ctrl, adc_status_t *p_status)
```

```
fsp_err_t R_ADC_Read (adc_ctrl_t *p_ctrl, adc_channel_t const reg_id, uint16_t *const p_data)
```

```
fsp_err_t R_ADC_Read32 (adc_ctrl_t *p_ctrl, adc_channel_t const reg_id,
```

```
uint32_t *const p_data)
```

```
fsp_err_t R_ADC_SampleStateCountSet (adc_ctrl_t *p_ctrl, adc_sample_state_t
*p_sample)
```

```
fsp_err_t R_ADC_Close (adc_ctrl_t *p_ctrl)
```

```
fsp_err_t R_ADC_OffsetSet (adc_ctrl_t *const p_ctrl, adc_channel_t const
reg_id, int32_t offset)
```

```
fsp_err_t R_ADC_Calibrate (adc_ctrl_t *const p_ctrl, void *const p_extend)
```

```
fsp_err_t R_ADC_VersionGet (fsp_version_t *const p_version)
```

```
fsp_err_t R_ADC_CallbackSet (adc_ctrl_t *const p_api_ctrl,
void(*p_callback)(adc_callback_args_t *), void const *const
p_context, adc_callback_args_t *const p_callback_memory)
```

## Detailed Description

Driver for the ADC12, ADC14, and ADC16 peripherals on RA MCUs. This module implements the [ADC Interface](#).

## Overview

### Features

The ADC module supports the following features:

- 12, 14, or 16 bit maximum resolution depending on the MCU
- Configure scans to include:
  - Multiple analog channels
  - Temperature sensor channel
  - Voltage sensor channel
- Configurable scan start trigger:
  - Software scan triggers
  - Hardware scan triggers (timer expiration, for example)
  - External scan triggers from the ADTRGn port pins
- Configurable scan mode:
  - Single scan mode, where each trigger starts a single scan
  - Continuous scan mode, where all channels are scanned continuously
  - Group scan mode, where channels are grouped into group A and group B. The groups can be assigned different start triggers, and group A can be given priority over group B. When group A has priority over group B, a group A trigger suspends an ongoing group B scan.
- Supports adding and averaging converted samples
- Optional callback when scan completes
- Supports reading converted data
- Sample and hold support
- Double-trigger support

## Configuration

### Build Time Configurations for r\_adc

The following build time configurations are defined in fsp\_cfg/r\_adc\_cfg.h:

Configuration	Options	Default	Description
Parameter Checking	<ul style="list-style-type: none"> <li>Default (BSP)</li> <li>Enabled</li> <li>Disabled</li> </ul>	Default (BSP)	If selected code for parameter checking is included in the build.

### Configurations for Driver > Analog > ADC Driver on r\_adc

This module can be added to the Stacks tab via New Stack > Driver > Analog > ADC Driver on r\_adc. Non-secure callable guard functions can be generated for this module by right clicking the module in the RA Configuration tool and checking the "Non-secure Callable" box.

Configuration	Options	Default	Description
General > Name	Name must be a valid C symbol	g_adc0	Module name
General > Unit	Unit must be a non-negative integer	0	Specifies the ADC Unit to be used.
General > Resolution	MCU Specific Options		Specifies the conversion resolution for this unit.
General > Alignment	MCU Specific Options		Specifies the conversion result alignment.
General > Clear after read	<ul style="list-style-type: none"> <li>Off</li> <li>On</li> </ul>	On	Specifies if the result register will be automatically cleared after the conversion result is read.
General > Mode	<ul style="list-style-type: none"> <li>Single Scan</li> <li>Continuous Scan</li> <li>Group Scan</li> </ul>	Single Scan	Specifies the mode that this ADC unit is used in.
General > Double-trigger	<ul style="list-style-type: none"> <li>Disabled</li> <li>Enabled</li> <li>Enabled (extended mode)</li> </ul>	Disabled	When enabled, the scan-end interrupt for Group A is only thrown on every second scan. Extended double-trigger mode (single-scan only) triggers on both ELC events, allowing (for example) a scan on two different

timer compare match values.

In group mode Group B is unaffected.

Specifies if this channel is included in the Sample and Hold Mask.

Specifies the updated sample-and-hold count for the channel dedicated sample-and-hold circuit

In Normal mode of operation, this bitmask field specifies the channels that are enabled in that ADC unit. In group mode, this field specifies which channels belong to group A.

In group mode, this field specifies which channels belong to group B.

Specifies if addition or averaging needs to be done for any of the channels in this unit.

Specify VREFH/VREFADC output voltage control.

Select channels to include in the Addition/Averaging Mask

Input > Sample and Hold > Sample and Hold Channels (Available only on selected MCUs)

- Channel 0
- Channel 1
- Channel 2

Input > Sample and Hold > Sample Hold States (Applies only to channels 0, 1, 2)

Must be a valid non-negative integer with configurable value 4 to 255

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Input > Channel Scan Mask (channel availability varies by MCU)

Refer to the RA Configuration tool for available options.

Input > Group B Scan Mask (channel availability varies by MCU)

Refer to the RA Configuration tool for available options.

Input > Add/Average Count

- Disabled
- Add two samples
- Add three samples
- Add four samples
- Add sixteen samples
- Average two samples
- Average four samples

Disabled

Input > Reference Voltage control

MCU Specific Options

Input > Addition/Averaging Mask (channel availability varies by MCU and unit)

Refer to the RA Configuration tool for available options.

Interrupts > Normal/Group A Trigger	MCU Specific Options		Specifies the trigger type to be used for this unit.
Interrupts > Group B Trigger	MCU Specific Options		Specifies the trigger for Group B scanning in group scanning mode. This event is also used to trigger Group A in extended double-trigger mode.
Interrupts > Group Priority (Valid only in Group Scan Mode)	<ul style="list-style-type: none"> <li>Group A cannot interrupt Group B</li> <li>Group A can interrupt Group B; Group B scan restarts at next trigger</li> <li>Group A can interrupt Group B; Group B scan restarts immediately</li> <li>Group A can interrupt Group B; Group B scan restarts immediately and scans continuously</li> </ul>	Group A cannot interrupt Group B	Determines whether an ongoing group B scan can be interrupted by a group A trigger, whether it should abort on a group A trigger, or if it should pause to allow group A scan and restart immediately after group A scan is complete.
Interrupts > Callback	Name must be a valid C symbol	NULL	A user callback function. If this callback function is provided, it is called from the interrupt service routine (ISR) each time the ADC scan completes.
Interrupts > Scan End Interrupt Priority	MCU Specific Options		Select scan end interrupt priority.
Interrupts > Scan End Group B Interrupt Priority	MCU Specific Options		Select group B scan end interrupt priority.

## Clock Configuration

The ADC clock is PCLKC if the MCU has PCLKC, or PCLKD otherwise.

The clock for this module is derived from the following peripheral clock for each MCU group:

--	--



MCU Group	Peripheral Clock
RA2A1	PCLKD
RA4M1	PCLKC
RA4W1	PCLKC
RA6M1	PCLKC
RA6M2	PCLKC
RA6M3	PCLKC
RA6M4	PCLKC

The ADC clock must be at least 1 MHz when the ADC is used. Many MCUs also have PCLK ratio restrictions when the ADC is used. For details on PCLK ratio restrictions, reference the footnotes in the second table of the Clock Generation Circuit chapter of the MCU User's Manual (for example, Table 9.2 "Specifications of the clock generation circuit for the internal clocks" in the RA6M3 manual R01UH0886EJ0100).

### Pin Configuration

The ANxxx pins are analog input channels that can be used with the ADC.

ADTRG0 and ADTRG1 can be used to start scans with an external trigger for unit 0 and 1 respectively. When external triggers are used, ADC scans begin on the falling edge of the ADTRG pin.

## Usage Notes

### Sample Hold

Enabling the sample and hold functionality reduces the maximum scan frequency because the sample and hold time is added to each scan. Refer to the hardware manual for details on the sample and hold time.

### ADC Operational Modes

The driver supports three operation modes: single-scan, continuous-scan, and group-scan modes. In each mode, analog channels are converted in ascending order of channel number, followed by scans of the temperature sensor and voltage sensor if they are included in the mask of channels to scan.

#### Single-scan Mode

In single scan mode, one or more specified channels are scanned once per trigger.

#### Continuous-scan Mode

In continuous scan mode, a single trigger is required to start the scan. Scans continue until [R\\_ADC\\_ScanStop\(\)](#) is called.

#### Group-scan Mode

Group-scan mode allows the application to allocate channels to one of two groups (A and B). Conversion begins when the specified ELC start trigger for that group is received.

With the priority configuration parameter, you can optionally give group A priority over group B. If group A has priority over group B, a group B scan is interrupted when a group A scan trigger occurs. The following options exist for group B when group A has priority:

- To restart the interrupted group B scan after the group A scan completes.
- To wait for another group B trigger and forget the interrupted scan.
- To continuously scan group B and suspend scanning group B only when a group A trigger is received.

*Note*

*If this option is selected, group B scanning begins immediately after `R_ADC_ScanCfg()`. Group A scan triggers must be enabled by `R_ADC_ScanStart()` and can be disabled by `R_ADC_ScanStop()`. Group B scans can only be disabled by reconfiguring the group A priority to a different mode.*

## Double-triggering

When double-triggering is enabled a single channel is selected to be scanned twice before an interrupt is thrown. The first scan result when using double-triggering is always saved to the selected channel's data register. The second result is saved to the data duplexing register (`ADC_CHANNEL_DUPLEX`).

Double-triggering uses Group A; only one channel can be selected when enabled. No other scanning is possible on Group A while double-trigger mode is selected. In addition, any special ADC channels (such as temperature sensors or voltage references) are not valid double-trigger channels.

When extended double-triggering is enabled both ADC input events are routed to Group A. The interrupt is still thrown after every two scans regardless of the triggering event(s). While the first and second scan are saved to the selected ADC data register and the ADC duplexing register as before, scans associated with event A and B are additionally copied into duplexing register A and B, respectively (`ADC_CHANNEL_DUPLEX_A` and `ADC_CHANNEL_DUPLEX_B`).

## When Interrupts Are Not Enabled

If interrupts are not enabled, the `R_ADC_StatusGet` API can be used to poll the ADC to determine when the scan has completed. The read API function is used to access the converted ADC result. This applies to both normal scans and calibration scans for MCUs that support calibration.

## Sample-State Count Setting

The application program can modify the setting of the sample-state count for analog channels by calling the `R_ADC_SampleStateCountSet()` API function. The application program only needs to modify the sample-state count settings from their default values to increase the sampling time. This can be either because the impedance of the input signal is too high to secure sufficient sampling time under the default setting or if the ADCLK is too slow. To modify the sample-state count for a given channel, set the channel number and the number of states when calling the `R_ADC_SampleStateCountSet()` API function. Valid sample state counts are 7-255.

*Note*

*Although the hardware supports a minimum number of sample states of 5, some MCUs require 7 states, so the minimum is set to 7. At the lowest supported ADC conversion clock rate (1 MHz), these extra states will lead to, at worst case, a 2 microsecond increase in conversion time. At 60 MHz the extra states will add 33.4 ns to the conversion time.*

If the sample state count needs to be changed for multiple channels, the application program must call the `R_ADC_SampleStateCountSet()` API function repeatedly, with appropriately modified

arguments for each channel.

If the ADCLK frequency changes, the sample states may need to be updated.

### Sample States for Temperature Sensor and Internal Voltage Reference

Sample states for the temperature sensor and the internal reference voltage are calculated during `R_ADC_ScanCfg()` based on the ADCLK frequency at the time. The sample states for the temperature sensor and internal voltage reference cannot be updated with `R_ADC_SampleStateCountSet()`. If the ADCLK frequency changes, call `R_ADC_ScanCfg()` before using the temperature sensor or internal reference voltage again to ensure the sampling time for the temperature sensor and internal voltage reference is optimal.

### Selecting Reference Voltage

The ADC16 can select VREFH0 or VREFADC as the high-potential reference voltage on selected MCU's. When using VREFADC stabilization time of 1500us is required after call for `R_ADC_Open()`.

### Using the Temperature Sensor with the ADC

The ADC HAL module supports reading the data from the on-chip temperature sensor. The value returned from the sensor can be converted into degrees Celsius or Fahrenheit in the application program using the following formula,  $T = (Vs - V1)/slope + T1$ , where:

- T: Measured temperature (degrees C)
- Vs: Voltage output by the temperature sensor at the time of temperature measurement (Volts)
- T1: Temperature experimentally measured at one point (degrees C)
- V1: Voltage output by the temperature sensor at the time of measurement of T1 (Volts)
- T2: Temperature at the experimental measurement of another point (degrees C)
- V2: Voltage output by the temperature sensor at the time of measurement of T2 (Volts)
- Slope: Temperature gradient of the temperature sensor (V/degrees C);  $slope = (V2 - V1)/(T2 - T1)$

#### Note

*The slope value can be obtained from the hardware manual for each device in the Electrical Characteristics Chapter - TSN Characteristics Table, Temperature slope entry.*

### Usage Notes for ADC16

#### Calibration

Calibration is required to use the ADC16 peripheral. When using this driver on an MCU that has ADC16, call `R_ADC_Calibrate()` after open, and prior to any other function.

#### Range of ADC16 Results

The range of the ADC16 is from 0 (lowest) to 0x7FFF (highest) when used in single-ended mode. This driver only supports single ended mode.

## Examples

### Basic Example

This is a basic example of minimal use of the ADC in an application.

```
/* A channel configuration is generated by the RA Configuration editor based on the
options selected. If additional
 * configurations are desired additional adc_channel_cfg_t elements can be defined
and passed to R_ADC_ScanCfg. */
const adc_channel_cfg_t g_adc0_channel_cfg =
{
    .scan_mask          = ADC_MASK_CHANNEL_0 | ADC_MASK_CHANNEL_1,
    .scan_mask_group_b = 0,
    .priority_group_a  = (adc_group_a_t) 0,
    .add_mask          = 0,
    .sample_hold_mask  = 0,
    .sample_hold_states = 0,
};

void adc_basic_example (void)
{
    fsp_err_t err = FSP_SUCCESS;
    /* Initializes the module. */
    err = R_ADC_Open(&g_adc0_ctrl, &g_adc0_cfg);
    /* Handle any errors. This function should be defined by the user. */
    handle_error(err);
    /* Enable channels. */
    err = R_ADC_ScanCfg(&g_adc0_ctrl, &g_adc0_channel_cfg);
    handle_error(err);
    /* In software trigger mode, start a scan by calling R_ADC_ScanStart(). In other
modes, enable external
 * triggers by calling R_ADC_ScanStart(). */
    (void) R_ADC_ScanStart(&g_adc0_ctrl);
    /* Wait for conversion to complete. */
    adc_status_t status;
    status.state = ADC_STATE_SCAN_IN_PROGRESS;
    while (ADC_STATE_SCAN_IN_PROGRESS == status.state)
    {
        (void) R_ADC_StatusGet(&g_adc0_ctrl, &status);
    }
}
```

```
/* Read converted data. */
uint16_t channell_conversion_result;
err = R_ADC_Read(&g_adc0_ctrl, ADC_CHANNEL_1, &channell_conversion_result);
handle_error(err);
}
```

## Temperature Sensor Example

This example shows how to calculate the MCU temperature using the ADC and the temperature sensor.

```
#define ADC_EXAMPLE_CALIBRATION_DATA_RA6M1 (0x7D5)
#define ADC_EXAMPLE_VCC_MICROVOLT (3300000)
#define ADC_EXAMPLE_TEMPERATURE_RESOLUTION (12U)
#define ADC_EXAMPLE_REFERENCE_CALIBRATION_TEMPERATURE (127)
void adc_temperature_example (void)
{
    /* The following example calculates the temperature on an RA6M1 device using the
    data provided in the section
    * 44.3.1 "Preparation for Using the Temperature Sensor" of the RA6M1 manual
    R01UH0884EJ0100. */
    fsp_err_t err = FSP_SUCCESS;
    /* Initializes the module. */
    err = R_ADC_Open(&g_adc0_ctrl, &g_adc0_cfg);
    /* Handle any errors. This function should be defined by the user. */
    handle_error(err);
    /* Enable temperature sensor. */
    err = R_ADC_ScanCfg(&g_adc0_ctrl, &g_adc0_channel_cfg);
    handle_error(err);
    /* In software trigger mode, start a scan by calling R_ADC_ScanStart(). In other
    modes, enable external
    * triggers by calling R_ADC_ScanStart(). */
    (void) R_ADC_ScanStart(&g_adc0_ctrl);
    /* Wait for conversion to complete. */
    adc_status_t status;
```

```
status.state = ADC_STATE_SCAN_IN_PROGRESS;
while (ADC_STATE_SCAN_IN_PROGRESS == status.state)
{
    (void) R_ADC_StatusGet(&g_adc0_ctrl, &status);
}
/* Read converted data. */
uint16_t temperature_conversion_result;
err = R_ADC_Read(&g_adc0_ctrl, ADC_CHANNEL_TEMPERATURE,
&temperature_conversion_result);
    handle_error(err);
/* If the MCU does not provide calibration data, use the value in the hardware
manual or determine it
* experimentally. */
/* Get Calibration data from the MCU if available. */
int32_t    reference_calibration_data;
adc_info_t adc_info;
    (void) R_ADC_InfoGet(&g_adc0_ctrl, &adc_info);
    reference_calibration_data = (int32_t) adc_info.calibration_data;
/* NOTE: The slope of the temperature sensor varies from sensor to sensor. Renesas
recommends calculating
* the slope of the temperature sensor experimentally.
*
* This example uses the typical slope provided in Table 52.38 "TSN characteristics"
in the RA6M1 manual
* R01UM0011EU0050. */
int32_t slope_uv_per_c = BSP_FEATURE_ADC_TSN_SLOPE;
/* Formula for calculating temperature copied from section 44.3.1 "Preparation for
Using the Temperature Sensor"
* of the RA6M1 manual R01UH0884EJ0100:
*
* In this MCU, the TSCDR register stores the temperature value (CAL127) of the
temperature sensor measured
* under the condition Ta = Tj = 127 C and AVCC0 = 3.3 V. By using this value as the
sample measurement result
```

```

* at the first point, preparation before using the temperature sensor can be
omitted.
*
* If V1 is calculated from CAL127,
* V1 = 3.3 * CAL127 / 4096 [V]
*
* Using this, the measured temperature can be calculated according to the following
formula.
*
* T = (Vs - V1) / Slope + 127 [C]
* T: Measured temperature (C)
* Vs: Voltage output by the temperature sensor when the temperature is measured (V)
* V1: Voltage output by the temperature sensor when Ta = Tj = 127 C and AVCC0 = 3.3
V (V)
* Slope: Temperature slope given in Table 52.38 / 1000 (V/C)
*/
int32_t v1_uv = (ADC_EXAMPLE_VCC_MICROVOLT >> ADC_EXAMPLE_TEMPERATURE_RESOLUTION)
*
reference_calibration_data;
int32_t vs_uv = (ADC_EXAMPLE_VCC_MICROVOLT >> ADC_EXAMPLE_TEMPERATURE_RESOLUTION)
*
temperature_conversion_result;
int32_t temperature_c = (vs_uv - v1_uv) / slope_uv_per_c +
ADC_EXAMPLE_REFERENCE_CALIBRATION_TEMPERATURE;
/* Expect room temperature, break if temperature is outside the range of 20 C to 25
C. */
if ((temperature_c < 20) || (temperature_c > 25))
{
__BKPT(0);
}
}

```

## Double-Trigger Example

This example demonstrates reading data from a double-trigger scan. A flag is used to wait for a

callback event. Two scans must occur before the callback is called. These results are read via [R\\_ADC\\_Read](#) using the selected channel enum value as well as [ADC\\_CHANNEL\\_DUPLEX](#).

```
volatile bool scan_complete_flag = false;

void adc_callback (adc_callback_args_t * p_args)
{
    FSP_PARAMETER_NOT_USED(p_args);
    scan_complete_flag = true;
}

void adc_double_trigger_example (void)
{
    fsp_err_t err = FSP_SUCCESS;

    /* Initialize the module. */
    err = R_ADC_Open(&g_adc0_ctrl, &g_adc0_cfg);

    /* Handle any errors. This function should be defined by the user. */
    handle_error(err);

    /* Enable double-trigger channel. */
    err = R_ADC_ScanCfg(&g_adc0_ctrl, &g_adc0_channel_cfg);
    handle_error(err);

    /* Enable scan triggering from ELC events. */
    (void) R_ADC_ScanStart(&g_adc0_ctrl);

    /* Wait for conversion to complete. Two scans must be triggered before a callback
occurs. */
    scan_complete_flag = false;
    while (!scan_complete_flag)
    {
        /* Wait for callback to set flag. */
    }

    /* Read converted data from both scans. */
    uint16_t channell_conversion_result_0;
    uint16_t channell_conversion_result_1;
    err = R_ADC_Read(&g_adc0_ctrl, ADC_CHANNEL_1, &channell_conversion_result_0);
    handle_error(err);

    err = R_ADC_Read(&g_adc0_ctrl, ADC_CHANNEL_DUPLEX,
&channell_conversion_result_1);
```



```

handle_error(err);
}

```

## Data Structures

struct [adc\\_sample\\_state\\_t](#)

struct [adc\\_extended\\_cfg\\_t](#)

struct [adc\\_channel\\_cfg\\_t](#)

struct [adc\\_instance\\_ctrl\\_t](#)

## Enumerations

enum [adc\\_mask\\_t](#)

enum [adc\\_add\\_t](#)

enum [adc\\_clear\\_t](#)

enum [adc\\_vref\\_control\\_t](#)

enum [adc\\_sample\\_state\\_reg\\_t](#)

enum [adc\\_group\\_a\\_t](#)

enum [adc\\_double\\_trigger\\_t](#)

## Data Structure Documentation

### ◆ [adc\\_sample\\_state\\_t](#)

struct <a href="#">adc_sample_state_t</a>		
ADC sample state configuration		
Data Fields		
<a href="#">adc_sample_state_reg_t</a>	reg_id	Sample state register ID.
uint8_t	num_states	Number of sampling states for conversion. Ch16-20/21 use the same value.

### ◆ [adc\\_extended\\_cfg\\_t](#)

struct <a href="#">adc_extended_cfg_t</a>		
Extended configuration structure for ADC.		
Data Fields		
<a href="#">adc_add_t</a>	add_average_count	Add or average samples.

<a href="#">adc_clear_t</a>	clearing	Clear after read.
<a href="#">adc_trigger_t</a>	trigger_group_b	Group B trigger source; valid only for group mode.
<a href="#">adc_double_trigger_t</a>	double_trigger_mode	Double-trigger mode setting.
<a href="#">adc_vref_control_t</a>	adc_vref_control	VREFADC output voltage control.

#### ◆ [adc\\_channel\\_cfg\\_t](#)

struct <a href="#">adc_channel_cfg_t</a>		
ADC channel(s) configuration		
Data Fields		
uint32_t	scan_mask	Channels/bits: bit 0 is ch0; bit 15 is ch15.
uint32_t	scan_mask_group_b	Valid for group modes.
uint32_t	add_mask	Valid if add enabled in Open().
<a href="#">adc_group_a_t</a>	priority_group_a	Valid for group modes.
uint8_t	sample_hold_mask	Channels/bits 0-2.
uint8_t	sample_hold_states	Number of states to be used for sample and hold. Affects channels 0-2.

#### ◆ [adc\\_instance\\_ctrl\\_t](#)

struct <a href="#">adc_instance_ctrl_t</a>		
ADC instance control block. DO NOT INITIALIZE. Initialized in <a href="#">adc_api_t::open()</a> .		

## Enumeration Type Documentation

◆ **adc\_mask\_t**

enum <code>adc_mask_t</code>	
For ADC Scan configuration <code>adc_channel_cfg_t::scan_mask</code> , <code>adc_channel_cfg_t::scan_mask_group_b</code> , <code>adc_channel_cfg_t::add_mask</code> and <code>adc_channel_cfg_t::sample_hold_mask</code> . Use bitwise OR to combine these masks for desired channels and sensors.	
Enumerator	
<code>ADC_MASK_OFF</code>	No channels selected.
<code>ADC_MASK_CHANNEL_0</code>	Channel 0 mask.
<code>ADC_MASK_CHANNEL_1</code>	Channel 1 mask.
<code>ADC_MASK_CHANNEL_2</code>	Channel 2 mask.
<code>ADC_MASK_CHANNEL_3</code>	Channel 3 mask.
<code>ADC_MASK_CHANNEL_4</code>	Channel 4 mask.
<code>ADC_MASK_CHANNEL_5</code>	Channel 5 mask.
<code>ADC_MASK_CHANNEL_6</code>	Channel 6 mask.
<code>ADC_MASK_CHANNEL_7</code>	Channel 7 mask.
<code>ADC_MASK_CHANNEL_8</code>	Channel 8 mask.
<code>ADC_MASK_CHANNEL_9</code>	Channel 9 mask.
<code>ADC_MASK_CHANNEL_10</code>	Channel 10 mask.
<code>ADC_MASK_CHANNEL_11</code>	Channel 11 mask.
<code>ADC_MASK_CHANNEL_12</code>	Channel 12 mask.
<code>ADC_MASK_CHANNEL_13</code>	Channel 13 mask.
<code>ADC_MASK_CHANNEL_14</code>	Channel 14 mask.
<code>ADC_MASK_CHANNEL_15</code>	Channel 15 mask.
<code>ADC_MASK_CHANNEL_16</code>	Channel 16 mask.
<code>ADC_MASK_CHANNEL_17</code>	Channel 17 mask.
<code>ADC_MASK_CHANNEL_18</code>	Channel 18 mask.

ADC_MASK_CHANNEL_19	Channel 19 mask.
ADC_MASK_CHANNEL_20	Channel 20 mask.
ADC_MASK_CHANNEL_21	Channel 21 mask.
ADC_MASK_CHANNEL_22	Channel 22 mask.
ADC_MASK_CHANNEL_23	Channel 23 mask.
ADC_MASK_CHANNEL_24	Channel 24 mask.
ADC_MASK_CHANNEL_25	Channel 25 mask.
ADC_MASK_CHANNEL_26	Channel 26 mask.
ADC_MASK_CHANNEL_27	Channel 27 mask.
ADC_MASK_TEMPERATURE	Temperature sensor channel mask.
ADC_MASK_VOLT	Voltage reference channel mask.
ADC_MASK_SENSORS	All sensor channel mask.

◆ **adc\_add\_t**

enum <code>adc_add_t</code>	
ADC data sample addition and averaging options	
Enumerator	
<code>ADC_ADD_OFF</code>	Addition turned off for channels/sensors.
<code>ADC_ADD_TWO</code>	Add two samples.
<code>ADC_ADD_THREE</code>	Add three samples.
<code>ADC_ADD_FOUR</code>	Add four samples.
<code>ADC_ADD_SIXTEEN</code>	Add sixteen samples.
<code>ADC_ADD_AVERAGE_TWO</code>	Average two samples.
<code>ADC_ADD_AVERAGE_FOUR</code>	Average four samples.
<code>ADC_ADD_AVERAGE_EIGHT</code>	Average eight samples.
<code>ADC_ADD_AVERAGE_SIXTEEN</code>	Add sixteen samples.

◆ **adc\_clear\_t**

enum <code>adc_clear_t</code>	
ADC clear after read definitions	
Enumerator	
<code>ADC_CLEAR_AFTER_READ_OFF</code>	Clear after read off.
<code>ADC_CLEAR_AFTER_READ_ON</code>	Clear after read on.

◆ **adc\_vref\_control\_t**

enum <a href="#">adc_vref_control_t</a>	
ADC VREFAMPCNT config options Reference Table 32.12 "VREFADC output voltage control list" in the RA2A1 manual R01UH0888EJ0100.	
Enumerator	
ADC_VREF_CONTROL_VREFH	VREFAMPCNT reset value. VREFADC Output voltage is Hi-Z.
ADC_VREF_CONTROL_1_5V_OUTPUT	BGR turn ON. VREFADC Output voltage is 1.5 V.
ADC_VREF_CONTROL_2_0V_OUTPUT	BGR turn ON. VREFADC Output voltage is 2.0 V.
ADC_VREF_CONTROL_2_5V_OUTPUT	BGR turn ON. VREFADC Output voltage is 2.5 V.

◆ **adc\_sample\_state\_reg\_t**

enum <code>adc_sample_state_reg_t</code>	
ADC sample state registers	
Enumerator	
<code>ADC_SAMPLE_STATE_CHANNEL_0</code>	Sample state register channel 0.
<code>ADC_SAMPLE_STATE_CHANNEL_1</code>	Sample state register channel 1.
<code>ADC_SAMPLE_STATE_CHANNEL_2</code>	Sample state register channel 2.
<code>ADC_SAMPLE_STATE_CHANNEL_3</code>	Sample state register channel 3.
<code>ADC_SAMPLE_STATE_CHANNEL_4</code>	Sample state register channel 4.
<code>ADC_SAMPLE_STATE_CHANNEL_5</code>	Sample state register channel 5.
<code>ADC_SAMPLE_STATE_CHANNEL_6</code>	Sample state register channel 6.
<code>ADC_SAMPLE_STATE_CHANNEL_7</code>	Sample state register channel 7.
<code>ADC_SAMPLE_STATE_CHANNEL_8</code>	Sample state register channel 8.
<code>ADC_SAMPLE_STATE_CHANNEL_9</code>	Sample state register channel 9.
<code>ADC_SAMPLE_STATE_CHANNEL_10</code>	Sample state register channel 10.
<code>ADC_SAMPLE_STATE_CHANNEL_11</code>	Sample state register channel 11.
<code>ADC_SAMPLE_STATE_CHANNEL_12</code>	Sample state register channel 12.
<code>ADC_SAMPLE_STATE_CHANNEL_13</code>	Sample state register channel 13.
<code>ADC_SAMPLE_STATE_CHANNEL_14</code>	Sample state register channel 14.
<code>ADC_SAMPLE_STATE_CHANNEL_15</code>	Sample state register channel 15.
<code>ADC_SAMPLE_STATE_CHANNEL_16_TO_31</code>	Sample state register channel 16 to 31.

◆ **adc\_group\_a\_t**

enum <a href="#">adc_group_a_t</a>	
ADC action for group A interrupts group B scan. This enumeration is used to specify the priority between Group A and B in group mode.	
Enumerator	
ADC_GROUP_A_PRIORITY_OFF	Group A ignored and does not interrupt ongoing group B scan.
ADC_GROUP_A_GROUP_B_WAIT_FOR_TRIGGER	Group A interrupts Group B(single scan) which restarts at next Group B trigger.
ADC_GROUP_A_GROUP_B_RESTART_SCAN	Group A interrupts Group B(single scan) which restarts immediately after Group A scan is complete.
ADC_GROUP_A_GROUP_B_CONTINUOUS_SCAN	Group A interrupts Group B(continuous scan) which continues scanning without a new Group B trigger.

◆ **adc\_double\_trigger\_t**

enum <a href="#">adc_double_trigger_t</a>	
ADC double-trigger mode definitions	
Enumerator	
ADC_DOUBLE_TRIGGER_DISABLED	Double-triggering disabled.
ADC_DOUBLE_TRIGGER_ENABLED	Double-triggering enabled.
ADC_DOUBLE_TRIGGER_ENABLED_EXTENDED	Double-triggering enabled on both ADC ELC events.

**Function Documentation**



◆ **R\_ADC\_Open()**

```
fsp_err_t R_ADC_Open ( adc_ctrl_t* p_ctrl, adc_cfg_t const *const p_cfg )
```

Sets the operational mode, trigger sources, interrupt priority, and configurations for the peripheral as a whole. If interrupt is enabled, the function registers a callback function pointer for notifying the user whenever a scan has completed.

**Return values**

FSP_SUCCESS	Module is ready for use.
FSP_ERR_ASSERTION	An input argument is invalid.
FSP_ERR_ALREADY_OPEN	The instance control structure has already been opened.
FSP_ERR_IRQ_BSP_DISABLED	A callback is provided, but the interrupt is not enabled.
FSP_ERR_IP_CHANNEL_NOT_PRESENT	The requested unit does not exist on this MCU.
FSP_ERR_INVALID_HW_CONDITION	The ADC clock must be at least 1 MHz

◆ **R\_ADC\_ScanCfg()**

```
fsp_err_t R_ADC_ScanCfg ( adc_ctrl_t* p_ctrl, void const *const p_extend )
```

Configures the ADC scan parameters. Channel specific settings are set in this function. Pass a pointer to `adc_channel_cfg_t` to `p_extend`.

**Note**

*This starts group B scans if `adc_channel_cfg_t::priority_group_a` is set to `ADC_GROUP_A_GROUP_B_CONTINUOUS_SCAN`.*

**Return values**

FSP_SUCCESS	Channel specific settings applied.
FSP_ERR_ASSERTION	An input argument is invalid.
FSP_ERR_NOT_OPEN	Unit is not open.

◆ **R\_ADC\_InfoGet()**

```
fsp_err_t R_ADC_InfoGet ( adc_ctrl_t* p_ctrl, adc_info_t* p_adc_info )
```

Returns the address of the lowest number configured channel and the total number of bytes to be read in order to read the results of the configured channels and return the ELC Event name. If no channels are configured, then a length of 0 is returned.

Also provides the temperature sensor slope and the calibration data for the sensor if available on this MCU. Otherwise, invalid calibration data of 0xFFFFFFFF will be returned.

**Note**

*In group mode, information is returned for group A only. Calculating information for group B is not currently supported.*

**Return values**

FSP_SUCCESS	Information stored in p_adc_info.
FSP_ERR_ASSERTION	An input argument is invalid.
FSP_ERR_NOT_OPEN	Unit is not open.

◆ **R\_ADC\_ScanStart()**

```
fsp_err_t R_ADC_ScanStart ( adc_ctrl_t* p_ctrl)
```

Starts a software scan or enables the hardware trigger for a scan depending on how the triggers were configured in the R\_ADC\_Open call. If the unit was configured for ELC or external hardware triggering, then this function allows the trigger signal to get to the ADC unit. The function is not able to control the generation of the trigger itself. If the unit was configured for software triggering, then this function starts the software triggered scan.

**Precondition**

Call R\_ADC\_ScanCfg after R\_ADC\_Open before starting a scan.

On MCUs that support calibration, call R\_ADC\_Calibrate and wait for calibration to complete before starting a scan.

**Return values**

FSP_SUCCESS	Scan started (software trigger) or hardware triggers enabled.
FSP_ERR_ASSERTION	An input argument is invalid.
FSP_ERR_NOT_OPEN	Unit is not open.
FSP_ERR_IN_USE	Another scan is still in progress (software trigger).

◆ **R\_ADC\_ScanStop()**

```
fsp_err_t R_ADC_ScanStop ( adc_ctrl_t* p_ctrl)
```

Stops the software scan or disables the unit from being triggered by the hardware trigger (ELC or external) based on what type of trigger the unit was configured for in the R\_ADC\_Open function. Stopping a hardware triggered scan via this function does not abort an ongoing scan, but prevents the next scan from occurring. Stopping a software triggered scan aborts an ongoing scan.

**Return values**

FSP_SUCCESS	Scan stopped (software trigger) or hardware triggers disabled.
FSP_ERR_ASSERTION	An input argument is invalid.
FSP_ERR_NOT_OPEN	Unit is not open.

◆ **R\_ADC\_StatusGet()**

```
fsp_err_t R_ADC_StatusGet ( adc_ctrl_t* p_ctrl, adc_status_t* p_status )
```

Provides the status of any scan process that was started, including scans started by ELC or external triggers and calibration scans on MCUs that support calibration.

**Return values**

FSP_SUCCESS	Module status stored in the provided pointer p_status
FSP_ERR_ASSERTION	An input argument is invalid.
FSP_ERR_NOT_OPEN	Unit is not open.

◆ **R\_ADC\_Read()**

```
fsp_err_t R_ADC_Read ( adc_ctrl_t* p_ctrl, adc_channel_t const reg_id, uint16_t*const p_data )
```

Reads conversion results from a single channel or sensor.

**Return values**

FSP_SUCCESS	Data read into provided p_data.
FSP_ERR_ASSERTION	An input argument is invalid.
FSP_ERR_NOT_OPEN	Unit is not open.

◆ **R\_ADC\_Read32()**

```
fsp_err_t R_ADC_Read32 ( adc_ctrl_t * p_ctrl, adc_channel_t const reg_id, uint32_t *const p_data )
```

Reads conversion results from a single channel or sensor register into a 32-bit result.

**Return values**

FSP_SUCCESS	Data read into provided p_data.
FSP_ERR_ASSERTION	An input argument is invalid.
FSP_ERR_NOT_OPEN	Unit is not open.

◆ **R\_ADC\_SampleStateCountSet()**

```
fsp_err_t R_ADC_SampleStateCountSet ( adc_ctrl_t * p_ctrl, adc_sample_state_t * p_sample )
```

Sets the sample state count for individual channels. This only needs to be set for special use cases. Normally, use the default values out of reset.

*Note*

*The sample states for the temperature and voltage sensor are set in R\_ADC\_ScanCfg.*

**Return values**

FSP_SUCCESS	Sample state count updated.
FSP_ERR_ASSERTION	An input argument is invalid.
FSP_ERR_NOT_OPEN	Unit is not open.

◆ **R\_ADC\_Close()**

```
fsp_err_t R_ADC_Close ( adc_ctrl_t * p_ctrl)
```

This function ends any scan in progress, disables interrupts, and removes power to the A/D peripheral.

**Return values**

FSP_SUCCESS	Module closed.
FSP_ERR_ASSERTION	An input argument is invalid.
FSP_ERR_NOT_OPEN	Unit is not open.

◆ **R\_ADC\_OffsetSet()**

```
fsp_err_t R_ADC_OffsetSet ( adc_ctrl_t *const p_ctrl, adc_channel_t const reg_id, int32_t offset )
```

`adc_api_t::offsetSet` is not supported on the ADC.

**Return values**

FSP_ERR_UNSUPPORTED	Function not supported in this implementation.
---------------------	------------------------------------------------

◆ **R\_ADC\_Calibrate()**

```
fsp_err_t R_ADC_Calibrate ( adc_ctrl_t *const p_ctrl, void *const p_extend )
```

Initiates calibration of the ADC on MCUs that require calibration. This function must be called before starting a scan on MCUs that require calibration.

Calibration is complete when the callback is called with `ADC_EVENT_CALIBRATION_COMPLETE` or when `R_ADC_StatusGet` returns `ADC_STATUS_IDLE`. Reference Figure 32.35 "Software flow and operation example of calibration operation." in the RA2A1 manual R01UH0888EJ0100.

ADC calibration time: 12 PCLKB + 774,930 ADCLK. (Reference Table 32.16 "Required calibration time (shown as the number of ADCLK and PCLKB cycles)" in the RA2A1 manual R01UH0888EJ0100. The lowest supported ADCLK is 1MHz.

Calibration will take a minimum of 24 milliseconds at 32 MHz PCLKB and ADCLK. This wait could take up to 780 milliseconds for a 1 MHz PCLKD (ADCLK).

**Parameters**

[in]	p_ctrl	Pointer to the instance control structure
[in]	p_extend	Unused argument. Pass NULL.

**Return values**

FSP_SUCCESS	Calibration successfully initiated.
FSP_ERR_INVALID_HW_CONDITION	A scan is in progress or hardware triggers are enabled.
FSP_ERR_UNSUPPORTED	Calibration not supported on this MCU.
FSP_ERR_ASSERTION	An input argument is invalid.
FSP_ERR_NOT_OPEN	Unit is not open.

◆ **R\_ADC\_VersionGet()**

```
fsp_err_t R_ADC_VersionGet ( fsp_version_t *const p_version)
```

Retrieve the API version number.

**Return values**

FSP_SUCCESS	Version stored in the provided p_version.
FSP_ERR_ASSERTION	An input argument is invalid.

◆ **R\_ADC\_CallbackSet()**

```
fsp_err_t R_ADC_CallbackSet ( adc_ctrl_t *const p_api_ctrl, void(*) (adc_callback_args_t *)
p_callback, void const *const p_context, adc_callback_args_t *const p_callback_memory )
```

Updates the user callback and has option of providing memory for callback structure. Implements `adc_api_t::callbackSet`

**Return values**

FSP_SUCCESS	Callback updated successfully.
FSP_ERR_ASSERTION	A required pointer is NULL.
FSP_ERR_NOT_OPEN	The control block has not been opened.

**4.2.4 Asynchronous General Purpose Timer (r\_agt)**

## Modules

**Functions**

```
fsp_err_t R_AGT_Close (timer_ctrl_t *const p_ctrl)
```

```
fsp_err_t R_AGT_PeriodSet (timer_ctrl_t *const p_ctrl, uint32_t const
period_counts)
```

```
fsp_err_t R_AGT_DutyCycleSet (timer_ctrl_t *const p_ctrl, uint32_t const
duty_cycle_counts, uint32_t const pin)
```

```
fsp_err_t R_AGT_Reset (timer_ctrl_t *const p_ctrl)
```

```
fsp_err_t R_AGT_Start (timer_ctrl_t *const p_ctrl)
```

fsp_err_t	R_AGT_Enable (timer_ctrl_t *const p_ctrl)
fsp_err_t	R_AGT_Disable (timer_ctrl_t *const p_ctrl)
fsp_err_t	R_AGT_InfoGet (timer_ctrl_t *const p_ctrl, timer_info_t *const p_info)
fsp_err_t	R_AGT_StatusGet (timer_ctrl_t *const p_ctrl, timer_status_t *const p_status)
fsp_err_t	R_AGT_Stop (timer_ctrl_t *const p_ctrl)
fsp_err_t	R_AGT_Open (timer_ctrl_t *const p_ctrl, timer_cfg_t const *const p_cfg)
fsp_err_t	R_AGT_CallbackSet (timer_ctrl_t *const p_api_ctrl, void(*p_callback)(timer_callback_args_t *), void const *const p_context, timer_callback_args_t *const p_callback_memory)
fsp_err_t	R_AGT_VersionGet (fsp_version_t *const p_version)

## Detailed Description

Driver for the AGT peripheral on RA MCUs. This module implements the [Timer Interface](#).

## Overview

### Features

The AGT module has the following features:

- Supports periodic mode, one-shot mode, and PWM mode.
- Signal can be output to a pin.
- Configurable period (counts per timer cycle).
- Configurable duty cycle in PWM mode.
- Configurable clock source, including PCLKB, LOCO, SUBCLK, and external sources input to AGTIO.
- Supports runtime reconfiguration of period.
- Supports runtime reconfiguration of duty cycle in PWM mode.
- Supports counting based on an external clock input to AGTIO.
- Supports debounce filter on AGTIO pins.
- Supports measuring pulse width or pulse period.
- APIs are provided to start, stop, and reset the counter.
- APIs are provided to get the current period, source clock frequency, and count direction.
- APIs are provided to get the current timer status and counter value.

### Selecting a Timer

RA MCUs have two timer peripherals: the General PWM Timer (GPT) and the Asynchronous General Purpose Timer (AGT). When selecting between them, consider these factors:

	GPT	AGT
--	-----	-----

Low Power Modes	The GPT can operate in sleep mode.	The AGT can operate in all low power modes (when count source is LOCO or subclock).
Available Channels	The number of GPT channels is device specific. All currently supported MCUs have at least 7 GPT channels.	All MCUs have 2 AGT channels.
Timer Resolution	All MCUs have at least one 32-bit GPT timer.	The AGT timers are 16-bit timers.
Clock Source	The GPT runs off PCLKD with a configurable divider up to 1024. It can also be configured to count ELC events or external pulses.	The AGT runs off PCLKB, LOCO, or subclock with a configurable divider up to 8 for PCLKB or up to 128 for LOCO or subclock.

## Configuration

### Build Time Configurations for r\_agt

The following build time configurations are defined in fsp\_cfg/r\_agt\_cfg.h:

Configuration	Options	Default	Description
Parameter Checking	<ul style="list-style-type: none"> <li>Default (BSP)</li> <li>Enabled</li> <li>Disabled</li> </ul>	Default (BSP)	If selected code for parameter checking is included in the build.
Pin Output Support	<ul style="list-style-type: none"> <li>Disabled</li> <li>Enabled</li> </ul>	Disabled	If selected code for outputting a waveform to a pin is included in the build.
Pin Input Support	<ul style="list-style-type: none"> <li>Disabled</li> <li>Enabled</li> </ul>	Disabled	Enable input support to use pulse width measurement mode, pulse period measurement mode, or input from P402, P402, or AGTIO.

### Configurations for Driver > Timers > Timer Driver on r\_agt

This module can be added to the Stacks tab via New Stack > Driver > Timers > Timer Driver on r\_agt. Non-secure callable guard functions can be generated for this module by right clicking the module in the RA Configuration tool and checking the "Non-secure Callable" box.

Configuration	Options	Default	Description
General > Name	Name must be a valid C symbol	g_timer0	Module name.
General > Channel	Channel number does	0	Physical hardware



	not exist		channel.
General > Mode	<ul style="list-style-type: none"> <li>• Periodic</li> <li>• One-Shot</li> <li>• PWM</li> </ul>	Periodic	Mode selection. Note: One-shot mode is implemented in software. ISR's must be enabled for one shot even if callback is unused.
General > Period	Value must be non-negative	0x10000	<p>Specify the timer period based on the selected unit.</p> <p>When the unit is set to 'Raw Counts', setting the period to 0x10000 results in the maximum period at the lowest divisor (fastest timer tick). Set the period to 0x10000 for a free running timer, pulse width measurement or pulse period measurement. Setting the period higher will automatically select a higher divider; the period can be set up to 0x80000 when counting from PCLKB or 0x800000 when counting from LOCO/subclock, which will use a divider of 8 or 128 respectively with the maximum period.</p>
General > Period Unit	<ul style="list-style-type: none"> <li>• Raw Counts</li> <li>• Nanoseconds</li> <li>• Microseconds</li> <li>• Milliseconds</li> <li>• Seconds</li> <li>• Hertz</li> <li>• Kilohertz</li> </ul>	Raw Counts	Unit of the period specified above
General > Count Source	<ul style="list-style-type: none"> <li>• PCLKB</li> <li>• LOCO</li> <li>• SUBCLOCK</li> <li>• AGT0 Underflow</li> <li>• P402 Input</li> <li>• P403 Input</li> <li>• AGTIO Input</li> </ul>	PCLKB	AGT counter clock source. NOTE: The divisor is calculated automatically based on the selected period. See agt_count_source_t documentation for details.

Output > Duty Cycle Percent (only applicable in PWM mode)	Value must be between 0 and 100	50	Specify the timer duty cycle percent. Only used in PWM mode.
Output > AGTOA Output	<ul style="list-style-type: none"> <li>• Disabled</li> <li>• Start Level Low</li> <li>• Start Level High</li> </ul>	Disabled	Configure AGTOA output.
Output > AGTOB Output	<ul style="list-style-type: none"> <li>• Disabled</li> <li>• Start Level Low</li> <li>• Start Level High</li> </ul>	Disabled	Configure AGTOB output.
Output > AGTO Output	<ul style="list-style-type: none"> <li>• Disabled</li> <li>• Start Level Low</li> <li>• Start Level High</li> </ul>	Disabled	Configure AGTO output.
Input > Measurement Mode	<ul style="list-style-type: none"> <li>• Measure Disabled</li> <li>• Measure Low Level Pulse Width</li> <li>• Measure High Level Pulse Width</li> <li>• Measure Pulse Period</li> </ul>	Measure Disabled	Select if the AGT should be used to measure pulse width or pulse period. In high level pulse width measurement mode, the AGT counts when AGTIO is high and starts counting immediately in the middle of a pulse if AGTIO is high when <a href="#">R_AGT_Start()</a> is called. In low level pulse width measurement mode, the AGT counts when AGTIO is low and could start counting in the middle of a pulse if AGTIO is low when <a href="#">R_AGT_Start()</a> is called.
Input > Input Filter	<ul style="list-style-type: none"> <li>• No Filter</li> <li>• Filter sampled at PCLKB</li> <li>• Filter sampled at PCLKB / 8</li> <li>• Filter sampled at PCLKB / 32</li> </ul>	No Filter	Input filter, applies AGTIO in pulse period measurement, pulse width measurement, or event counter mode. The filter requires the signal to be at the same level for 3 successive reads at the specified filter frequency.
Input > Enable Pin	<ul style="list-style-type: none"> <li>• Enable Pin Not Used</li> <li>• Enable Pin Active Low</li> <li>• Enable Pin Active High</li> </ul>	Enable Pin Not Used	Select active edge for the AGTEE pin if used. Only applies if the count source is P402, P403 or AGTIO.

Input > Trigger Edge	<ul style="list-style-type: none"> <li>• Trigger Edge Rising</li> <li>• Trigger Edge Falling</li> <li>• Trigger Edge Both</li> </ul>	Trigger Edge Rising	Select the trigger edge. Applies if measurement mode is pulse period, or if the count source is P402, P403, or AGTIO. Do not select Trigger Edge Both with pulse period measurement.
Interrupts > Callback	Name must be a valid C symbol	NULL	A user callback function. If this callback function is provided, it is called from the interrupt service routine (ISR) each time the timer period elapses.
Interrupts > Underflow Interrupt Priority	MCU Specific Options		Timer interrupt priority.

## Clock Configuration

The AGT clock is based on the PCLKB, LOCO, or Subclock frequency. You can set the clock frequency using the **Clocks** tab of the RA Configuration editor or by using the CGC Interface at run-time.

## Pin Configuration

This module can use the AGTOA and AGTOB pins as output pins for periodic, one-shot, or PWM signals.

For input capture, the input signal must be applied to the AGTIO pin.

For event counting, the AGTEEn enable pin is optional.

## Timer Period

The RA Configuration editor will automatically calculate the period count value and source clock divider based on the selected period time, units, and clock speed.

When the selected unit is "Raw counts", the maximum allowed period setting varies depending on the selected clock source:

Clock source	Maximum period (counts)
LOCO/Subclock	0x800000
PCLKB	0x80000
All other sources	0x10000

### Note

*Though the AGT is a 16-bit timer, because the period interrupt occurs when the counter underflows, setting the period register to 0 results in an effective period of 1 count. For this reason all user-provided raw count values reflect the actual number of period counts (not the raw register values).*

## Usage Notes

### Starting and Stopping the AGT

After starting or stopping the timer, AGT registers cannot be accessed until the AGT state is updated after 3 AGTCLK cycles. If another AGT function is called before the 3 AGTCLK period elapses, the function spins waiting for the AGT state to update. The required wait time after starting or stopping the timer can be determined using the frequency of AGTCLK, which is derived from [timer\\_cfg\\_t::source\\_div](#) and [agt\\_extended\\_cfg\\_t::count\\_source](#).

The application is responsible for ensuring required clocks are started and stable before accessing MCU peripheral registers.

#### Warning

The subclock can take seconds to stabilize. The RA startup code does not wait for subclock stabilization unless the subclock is the main clock source. When running AGT or RTC off the subclock, the application must ensure the subclock is stable before starting operation.

### Low Power Modes

The AGT1 (channel 1 only) can be used to enter snooze mode or to wake the MCU from snooze, software standby, or deep software standby modes when a counter underflow occurs. The compare match A and B events can also be used to wake from software standby or snooze modes.

### One-Shot Mode

The AGT timer does not support one-shot mode natively. One-shot mode is achieved by stopping the timer in the interrupt service routine before the callback is called. If the interrupt is not serviced before the timer period expires again, the timer generates more than one event. The callback is only called once in this case, but multiple events may be generated if the timer is linked to the [Data Transfer Controller \(r\\_dtc\)](#).

### One-Shot Mode Output

The output waveform in one-shot mode is one AGT clock cycle less than the configured period. The configured period must be at least 2 counts to generate an output pulse.

Examples of one-shot signals that can be generated by this module are shown below:

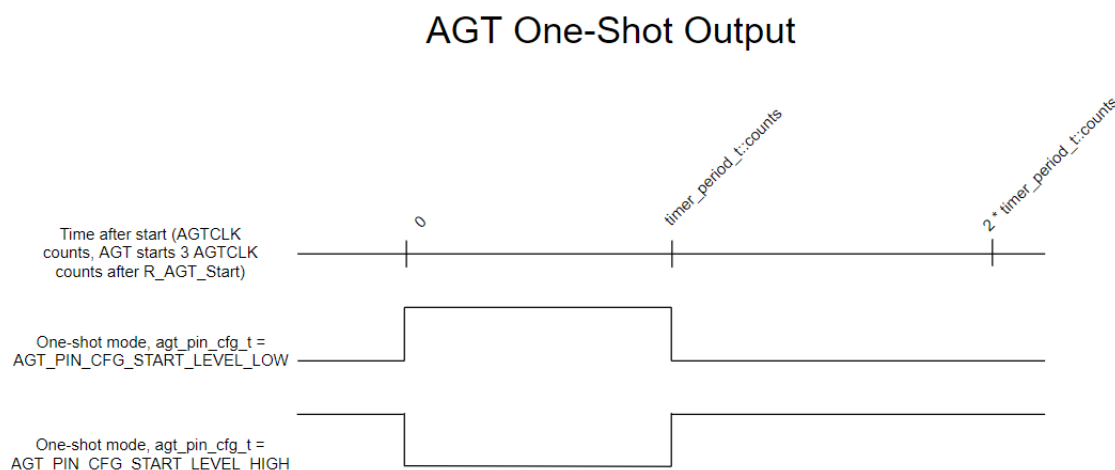


Figure 147: AGT One-Shot Output

## Periodic Output

The AGTOA or AGTOB pin toggles twice each time the timer expires in periodic mode. This is achieved by defining a PWM wave at a 50 percent duty cycle so that the period of the resulting square (from rising edge to rising edge) matches the period of the AGT timer. Since the periodic output is actually a PWM output, the time at the stop level is one cycle shorter than the time opposite the stop level for odd period values.

Examples of periodic signals that can be generated by this module are shown below:

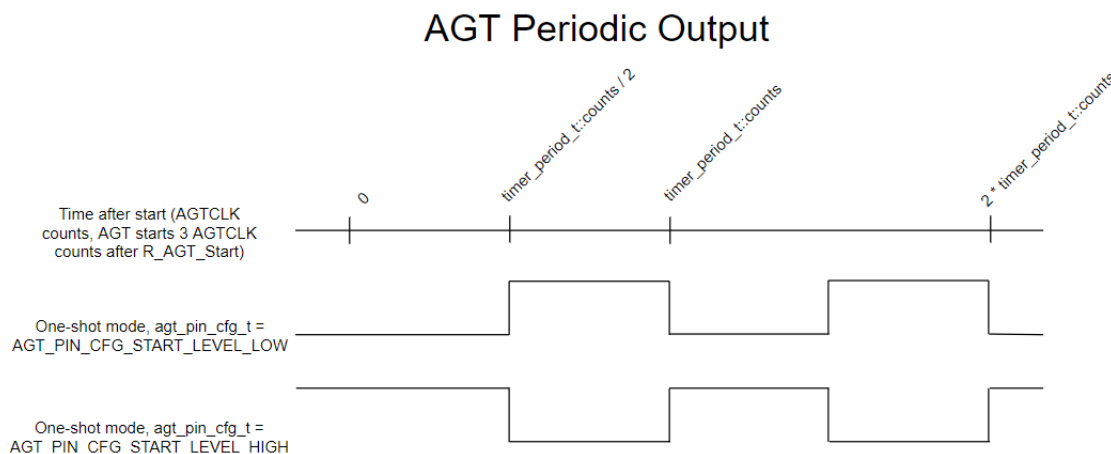


Figure 148: AGT Periodic Output

## PWM Output

This module does not support in phase PWM output. The PWM output signal is low at the beginning of the cycle and high at the end of the cycle.

Examples of PWM signals that can be generated by this module are shown below:

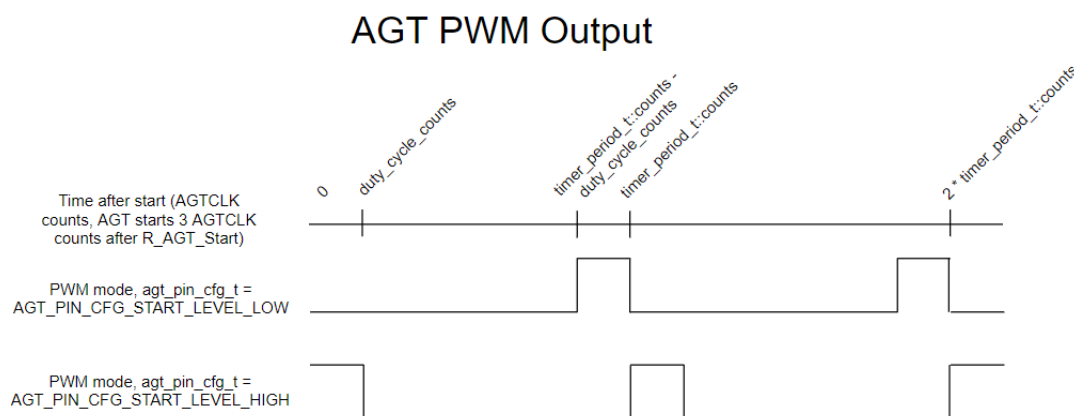


Figure 149: AGT PWM Output

## Triggering ELC Events with AGT

The AGT timer can trigger the start of other peripherals. The [Event Link Controller \(r\\_elc\)](#) guide

provides a list of all available peripherals.

## Examples

### AGT Basic Example

This is a basic example of minimal use of the AGT in an application.

```
void agt_basic_example (void)
{
    fsp_err_t err = FSP_SUCCESS;
    /* Initializes the module. */
    err = R_AGT_Open(&g_timer0_ctrl, &g_timer0_cfg);
    /* Handle any errors. This function should be defined by the user. */
    handle_error(err);
    /* Start the timer. */
    (void) R_AGT_Start(&g_timer0_ctrl);
}
```

### AGT Callback Example

This is an example of a timer callback.

```
/* Example callback called when timer expires. */
void timer_callback (timer_callback_args_t * p_args)
{
    if (TIMER_EVENT_CYCLE_END == p_args->event)
    {
        /* Add application code to be called periodically here. */
    }
}
```

### AGT Free Running Counter Example

To use the AGT as a free running counter, select periodic mode and set the the Period to 0xFFFF.

```
void agt_counter_example (void)
```

```
{
    fsp_err_t err = FSP_SUCCESS;
    /* Initializes the module. */
    err = R_AGT_Open(&g_timer0_ctrl, &g_timer0_cfg);
    /* Handle any errors. This function should be defined by the user. */
    handle_error(err);
    /* Start the timer. */
    (void) R_AGT_Start(&g_timer0_ctrl);
    /* (Optional) Stop the timer. */
    (void) R_AGT_Stop(&g_timer0_ctrl);
    /* Read the current counter value. Counter value is in status.counter. */
    timer_status_t status;
    (void) R_AGT_StatusGet(&g_timer0_ctrl, &status);
}
```

### AGT Input Capture Example

This is an example of using the AGT to capture pulse width or pulse period measurements.

```
/* Example callback called when a capture occurs. */
uint64_t g_captured_time = 0U;
uint32_t g_capture_overflows = 0U;
void timer_capture_callback (timer_callback_args_t * p_args)
{
    if (TIMER_EVENT_CAPTURE_A == p_args->event)
    {
        /* (Optional) Get the current period if not known. */
        timer_info_t info;
        (void) R_AGT_InfoGet(&g_timer0_ctrl, &info);
        uint32_t period = info.period_counts;
        /* Process capture from AGTIO. */
        g_captured_time = ((uint64_t) period * g_capture_overflows) +
p_args->capture;
        g_capture_overflows = 0U;
    }
}
```

```
if (TIMER_EVENT_CYCLE_END == p_args->event)
{
    /* An overflow occurred during capture. This must be accounted for at the
application layer. */
    g_capture_overflows++;
}
}
void agt_capture_example (void)
{
    fsp_err_t err = FSP_SUCCESS;
    /* Initializes the module. */
    err = R_AGT_Open(&g_timer0_ctrl, &g_timer0_cfg);
    /* Handle any errors. This function should be defined by the user. */
    handle_error(err);
    /* Enable captures. Captured values arrive in the interrupt. */
    (void) R_AGT_Enable(&g_timer0_ctrl);
    /* (Optional) Disable captures. */
    (void) R_AGT_Disable(&g_timer0_ctrl);
}
```

## AGT Period Update Example

This an example of updating the period.

```
#define AGT_EXAMPLE_MSEC_PER_SEC (1000)
#define AGT_EXAMPLE_DESIRED_PERIOD_MSEC (20)
/* This example shows how to calculate a new period value at runtime. */
void agt_period_calculation_example (void)
{
    fsp_err_t err = FSP_SUCCESS;
    /* Initializes the module. */
    err = R_AGT_Open(&g_timer0_ctrl, &g_timer0_cfg);
    /* Handle any errors. This function should be defined by the user. */
    handle_error(err);
    /* Start the timer. */
```



```

(void) R_AGT_Start(&g_timer0_ctrl);

/* Get the source clock frequency (in Hz). There are several ways to do this in FSP:
 * - If LOCO or subclock is chosen in agt_extended_cfg_t::clock_source
 * - The source clock frequency is BSP_LOCO_HZ >> timer_cfg_t::source_div
 * - If PCLKB is chosen in agt_extended_cfg_t::clock_source and the PCLKB frequency
has not changed since reset,
 * - The source clock frequency is BSP_STARTUP_PCLKB_HZ >> timer_cfg_t::source_div
 * - Use the R_AGT_InfoGet function (it accounts for the clock source and divider).
 * - Calculate the current PCLKB frequency using
R_FSP_SystemClockHzGet(FSP_PRIV_CLOCK_PCLKB) and right shift
 * by timer_cfg_t::source_div.
 *
 * This example uses the last option (R_FSP_SystemClockHzGet).
 */
uint32_t timer_freq_hz = R_FSP_SystemClockHzGet(FSP_PRIV_CLOCK_PCLKB) >>
g_timer0_cfg.source_div;

/* Calculate the desired period based on the current clock. Note that this
calculation could overflow if the
 * desired period is larger than UINT32_MAX / pclk_freq_hz. A cast to uint64_t is
used to prevent this. */
uint32_t period_counts =
    (uint32_t) (((uint64_t) timer_freq_hz * AGT_EXAMPLE_DESIRED_PERIOD_MSEC) /
AGT_EXAMPLE_MSEC_PER_SEC);

/* Set the calculated period. This will return an error if parameter checking is
enabled and the calculated
 * period is larger than UINT16_MAX. */
err = R_AGT_PeriodSet(&g_timer0_ctrl, period_counts);
handle_error(err);
}

```

## AGT Duty Cycle Update Example

This an example of updating the duty cycle.

```
#define AGT_EXAMPLE_DESIRED_DUTY_CYCLE_PERCENT (25)
```

```
#define AGT_EXAMPLE_MAX_PERCENT (100)

/* This example shows how to calculate a new duty cycle value at runtime. */
void agt_duty_cycle_calculation_example (void)
{
    fsp_err_t err = FSP_SUCCESS;

    /* Initializes the module. */
    err = R_AGT_Open(&g_timer0_ctrl, &g_timer0_cfg);

    /* Handle any errors. This function should be defined by the user. */
    handle_error(err);

    /* Start the timer. */
    (void) R_AGT_Start(&g_timer0_ctrl);

    /* Get the current period setting. */
    timer_info_t info;
    (void) R_AGT_InfoGet(&g_timer0_ctrl, &info);
    uint32_t current_period_counts = info.period_counts;

    /* Calculate the desired duty cycle based on the current period. */
    uint32_t duty_cycle_counts = (current_period_counts *
AGT_EXAMPLE_DESIRED_DUTY_CYCLE_PERCENT) /
                                AGT_EXAMPLE_MAX_PERCENT;

    /* Set the calculated duty cycle. */
    err = R_AGT_DutyCycleSet(&g_timer0_ctrl, duty_cycle_counts, AGT_OUTPUT_PIN_AGTOA
);
    handle_error(err);
}
```

### AGT Cascaded Timers Example

This an example of using AGT0 underflow as the count source for AGT1.

```
/* This example shows how use cascaded timers. The count source for AGT channel 1 is
set to AGT0 underflow. */
void agt_cascaded_timers_example (void)
{
    fsp_err_t err = FSP_SUCCESS;

    /* Initialize the timers in any order. */
```

```

err = R_AGT_Open(&g_timer_channel0_ctrl, &g_timer_channel0_cfg);
handle_error(err);

err = R_AGT_Open(&g_timer_channel1_ctrl, &g_timer_channel1_cfg);
handle_error(err);

/* Start AGT channel 1 first. */

(void) R_AGT_Start(&g_timer_channel1_ctrl);
(void) R_AGT_Start(&g_timer_channel0_ctrl);

/* (Optional) Stop AGT channel 0 first. */

(void) R_AGT_Stop(&g_timer_channel0_ctrl);
(void) R_AGT_Stop(&g_timer_channel1_ctrl);

/* Read the current counter value. Counter value is in status.counter. */
timer_status_t status;

(void) R_AGT_StatusGet(&g_timer_channel1_ctrl, &status);
}

```

## Data Structures

struct [agt\\_instance\\_ctrl\\_t](#)

struct [agt\\_extended\\_cfg\\_t](#)

## Enumerations

enum [agt\\_clock\\_t](#)

enum [agt\\_measure\\_t](#)

enum [agt\\_agtio\\_filter\\_t](#)

enum [agt\\_enable\\_pin\\_t](#)

enum [agt\\_trigger\\_edge\\_t](#)

enum [agt\\_output\\_pin\\_t](#)

enum [agt\\_pin\\_cfg\\_t](#)

## Data Structure Documentation

### ◆ [agt\\_instance\\_ctrl\\_t](#)

struct [agt\\_instance\\_ctrl\\_t](#)

Channel control block. DO NOT INITIALIZE. Initialization occurs when [timer\\_api\\_t::open](#) is called.

## ◆ agt\_extended\_cfg\_t

struct agt_extended_cfg_t		
Optional AGT extension data structure.		
Data Fields		
agt_clock_t	count_source	AGT channel clock source. Valid values are: AGT_CLOCK_PCLKB, AGT_CLOCK_LOCO, AGT_CLOCK_FSUB.
union agt_extended_cfg_t	__unnamed__	
agt_pin_cfg_t	agto: 3	Configure AGTO pin.  <i>Note</i> <i>AGTIO polarity is opposite AGTO</i>
agt_measure_t	measurement_mode	Measurement mode.
agt_agtio_filter_t	agtio_filter	Input filter for AGTIO.
agt_enable_pin_t	enable_pin	Enable pin (event counting only)
agt_trigger_edge_t	trigger_edge	Trigger edge to start pulse period measurement or count external event.

## Enumeration Type Documentation

◆ **agt\_clock\_t**

enum agt_clock_t	
Count source	
Enumerator	
AGT_CLOCK_PCLKB	PCLKB count source, division by 1, 2, or 8 allowed.
AGT_CLOCK_LOCO	LOCO count source, division by 1, 2, 4, 8, 16, 32, 64, or 128 allowed.
AGT_CLOCK_AGT0_UNDERFLOW	Underflow event signal from AGT0, division must be 1.
AGT_CLOCK_SUBCLOCK	Subclock count source, division by 1, 2, 4, 8, 16, 32, 64, or 128 allowed.
AGT_CLOCK_P402	Counts events on P402, events are counted in deep software standby mode.
AGT_CLOCK_P403	Counts events on P403, events are counted in deep software standby mode.
AGT_CLOCK_AGTIO	Counts events on AGTIO, events are not counted in software standby modes.

◆ **agt\_measure\_t**

enum agt_measure_t	
Enable pin for event counting mode.	
Enumerator	
AGT_MEASURE_DISABLED	AGT used as a counter.
AGT_MEASURE_PULSE_WIDTH_LOW_LEVEL	AGT used to measure low level pulse width.
AGT_MEASURE_PULSE_WIDTH_HIGH_LEVEL	AGT used to measure high level pulse width.
AGT_MEASURE_PULSE_PERIOD	AGT used to measure pulse period.

◆ **agt\_agtio\_filter\_t**

enum agt_agtio_filter_t	
Input filter, applies AGTIO in pulse period measurement, pulse width measurement, or event counter mode. The filter requires the signal to be at the same level for 3 successive reads at the specified filter frequency.	
Enumerator	
AGT_AGTIO_FILTER_NONE	No filter.
AGT_AGTIO_FILTER_PCLKB	Filter at PCLKB.
AGT_AGTIO_FILTER_PCLKB_DIV_8	Filter at PCLKB / 8.
AGT_AGTIO_FILTER_PCLKB_DIV_32	Filter at PCLKB / 32.

◆ **agt\_enable\_pin\_t**

enum agt_enable_pin_t	
Enable pin for event counting mode.	
Enumerator	
AGT_ENABLE_PIN_NOT_USED	AGTEE is not used.
AGT_ENABLE_PIN_ACTIVE_LOW	Events are only counted when AGTEE is low.
AGT_ENABLE_PIN_ACTIVE_HIGH	Events are only counted when AGTEE is high.

◆ **agt\_trigger\_edge\_t**

enum agt_trigger_edge_t	
Trigger edge for pulse period measurement mode and event counting mode.	
Enumerator	
AGT_TRIGGER_EDGE_RISING	Measurement starts or events are counted on rising edge.
AGT_TRIGGER_EDGE_FALLING	Measurement starts or events are counted on falling edge.
AGT_TRIGGER_EDGE_BOTH	Events are counted on both edges (n/a for pulse period mode)

◆ **agt\_output\_pin\_t**

enum <code>agt_output_pin_t</code>	
Output pins, used to select which duty cycle to update in <code>R_AGT_DutyCycleSet()</code> .	
Enumerator	
<code>AGT_OUTPUT_PIN_AGTOA</code>	GTIOCA.
<code>AGT_OUTPUT_PIN_AGTOB</code>	GTIOCB.

◆ **agt\_pin\_cfg\_t**

enum <code>agt_pin_cfg_t</code>	
Level of AGT pin	
Enumerator	
<code>AGT_PIN_CFG_DISABLED</code>	Not used as output pin.
<code>AGT_PIN_CFG_START_LEVEL_LOW</code>	Pin level low.
<code>AGT_PIN_CFG_START_LEVEL_HIGH</code>	Pin level high.

**Function Documentation**◆ **R\_AGT\_Close()**

<code>fsp_err_t R_AGT_Close ( timer_ctrl_t *const p_ctrl)</code>	
Stops counter, disables interrupts, disables output pins, and clears internal driver data. Implements <code>timer_api_t::close</code> .	
<b>Return values</b>	
<code>FSP_SUCCESS</code>	Timer closed.
<code>FSP_ERR_ASSERTION</code>	<code>p_ctrl</code> is NULL.
<code>FSP_ERR_NOT_OPEN</code>	The instance control structure is not opened.

## ◆ R\_AGT\_PeriodSet()

```
fsp_err_t R_AGT_PeriodSet ( timer_ctrl_t *const p_ctrl, uint32_t const period_counts )
```

Updates period. The new period is updated immediately and the counter is reset to the maximum value. Implements `timer_api_t::periodSet`.

**Warning**

If periodic output is used, the duty cycle buffer registers are updated after the period buffer register. If this function is called while the timer is running and an AGT underflow occurs during processing, the duty cycle will not be the desired 50% duty cycle until the counter underflow after processing completes.

Stop the timer before calling this function if one-shot output is used.

**Example:**

```
/* Get the source clock frequency (in Hz). There are several ways to do this in FSP:
 * - If LOCO or subclock is chosen in agt_extended_cfg_t::clock_source
 * - The source clock frequency is BSP_LOCO_HZ >> timer_cfg_t::source_div
 * - If PCLKB is chosen in agt_extended_cfg_t::clock_source and the PCLKB frequency
has not changed since reset,
 * - The source clock frequency is BSP_STARTUP_PCLKB_HZ >> timer_cfg_t::source_div
 * - Use the R_AGT_InfoGet function (it accounts for the clock source and divider).
 * - Calculate the current PCLKB frequency using
R_FSP_SystemClockHzGet(FSP_PRIV_CLOCK_PCLKB) and right shift
 * by timer_cfg_t::source_div.
 *
 * This example uses the last option (R_FSP_SystemClockHzGet).
 */
uint32_t timer_freq_hz = R_FSP_SystemClockHzGet(FSP_PRIV_CLOCK_PCLKB) >>
g_timer0_cfg.source_div;
/* Calculate the desired period based on the current clock. Note that this
calculation could overflow if the
 * desired period is larger than UINT32_MAX / pclk_freq_hz. A cast to uint64_t is
used to prevent this. */
uint32_t period_counts =
    (uint32_t) (((uint64_t) timer_freq_hz * AGT_EXAMPLE_DESIRED_PERIOD_MSEC) /
AGT_EXAMPLE_MSEC_PER_SEC);
/* Set the calculated period. This will return an error if parameter checking is
enabled and the calculated
```



```
* period is larger than UINT16_MAX. */  
err = R_AGT_PeriodSet(&g_timer0_ctrl, period_counts);  
handle_error(err);
```

**Return values**

FSP_SUCCESS	Period value updated.
FSP_ERR_ASSERTION	A required pointer was NULL, or the period was not in the valid range of 1 to 0xFFFF.
FSP_ERR_NOT_OPEN	The instance control structure is not opened.

## ◆ R\_AGT\_DutyCycleSet()

```
fsp_err_t R_AGT_DutyCycleSet ( timer_ctrl_t *const p_ctrl, uint32_t const duty_cycle_counts,
uint32_t const pin )
```

Updates duty cycle. If the timer is counting, the new duty cycle is reflected after the next counter underflow. Implements [timer\\_api\\_t::dutyCycleSet](#).

Example:

```
/* Get the current period setting. */
timer_info_t info;
(void) R_AGT_InfoGet(&g_timer0_ctrl, &info);
uint32_t current_period_counts = info.period_counts;
/* Calculate the desired duty cycle based on the current period. */
uint32_t duty_cycle_counts = (current_period_counts *
AGT_EXAMPLE_DESIRED_DUTY_CYCLE_PERCENT) /
AGT_EXAMPLE_MAX_PERCENT;
/* Set the calculated duty cycle. */
err = R_AGT_DutyCycleSet(&g_timer0_ctrl, duty_cycle_counts, AGT_OUTPUT_PIN_AGTOA);
handle_error(err);
```

### Return values

FSP_SUCCESS	Duty cycle updated.
FSP_ERR_ASSERTION	A required pointer was NULL, or the pin was not AGT_AGTO_AGTOA or AGT_AGTO_AGTOB.
FSP_ERR_INVALID_ARGUMENT	Duty cycle was not in the valid range of 0 to period (counts) - 1
FSP_ERR_NOT_OPEN	The instance control structure is not opened.
FSP_ERR_UNSUPPORTED	AGT_CFG_OUTPUT_SUPPORT_ENABLE is 0.

◆ **R\_AGT\_Reset()**

```
fsp_err_t R_AGT_Reset ( timer_ctrl_t *const p_ctrl)
```

Resets the counter value to the period minus one. Implements `timer_api_t::reset`.

**Return values**

FSP_SUCCESS	Counter reset.
FSP_ERR_ASSERTION	p_ctrl is NULL
FSP_ERR_NOT_OPEN	The instance control structure is not opened.

◆ **R\_AGT\_Start()**

```
fsp_err_t R_AGT_Start ( timer_ctrl_t *const p_ctrl)
```

Starts timer. Implements `timer_api_t::start`.

Example:

```
/* Start the timer. */
(void) R_AGT_Start(&g_timer0_ctrl);
```

**Return values**

FSP_SUCCESS	Timer started.
FSP_ERR_ASSERTION	p_ctrl is null.
FSP_ERR_NOT_OPEN	The instance control structure is not opened.

◆ **R\_AGT\_Enable()**

```
fsp_err_t R_AGT_Enable ( timer_ctrl_t *const p_ctrl)
```

Enables external event triggers that start, stop, clear, or capture the counter. Implements [timer\\_api\\_t::enable](#).

Example:

```
/* Enable captures. Captured values arrive in the interrupt. */
(void) R_AGT_Enable(&g_timer0_ctrl);
```

**Return values**

FSP_SUCCESS	External events successfully enabled.
FSP_ERR_ASSERTION	p_ctrl was NULL.
FSP_ERR_NOT_OPEN	The instance is not opened.

◆ **R\_AGT\_Disable()**

```
fsp_err_t R_AGT_Disable ( timer_ctrl_t *const p_ctrl)
```

Disables external event triggers that start, stop, clear, or capture the counter. Implements [timer\\_api\\_t::disable](#).

Example:

```
/* (Optional) Disable captures. */
(void) R_AGT_Disable(&g_timer0_ctrl);
```

**Return values**

FSP_SUCCESS	External events successfully disabled.
FSP_ERR_ASSERTION	p_ctrl was NULL.
FSP_ERR_NOT_OPEN	The instance is not opened.

◆ **R\_AGT\_InfoGet()**

```
fsp_err_t R_AGT_InfoGet ( timer_ctrl_t *const p_ctrl, timer_info_t *const p_info )
```

Gets timer information and store it in provided pointer p\_info. Implements `timer_api_t::infoGet`.

Example:

```
/* (Optional) Get the current period if not known. */
timer_info_t info;
(void) R_AGT_InfoGet(&g_timer0_ctrl, &info);
uint32_t period = info.period_counts;
```

**Return values**

FSP_SUCCESS	Period, count direction, and frequency stored in p_info.
FSP_ERR_ASSERTION	A required pointer is NULL.
FSP_ERR_NOT_OPEN	The instance control structure is not opened.

◆ **R\_AGT\_StatusGet()**

```
fsp_err_t R_AGT_StatusGet ( timer_ctrl_t *const p_ctrl, timer_status_t *const p_status )
```

Retrieves the current state and counter value stores them in p\_status. Implements `timer_api_t::statusGet`.

Example:

```
/* Read the current counter value. Counter value is in status.counter. */
timer_status_t status;
(void) R_AGT_StatusGet(&g_timer0_ctrl, &status);
```

**Return values**

FSP_SUCCESS	Current status and counter value provided in p_status.
FSP_ERR_ASSERTION	A required pointer is NULL.
FSP_ERR_NOT_OPEN	The instance control structure is not opened.

**◆ R\_AGT\_Stop()**

```
fsp_err_t R_AGT_Stop ( timer_ctrl_t *const p_ctrl)
```

Stops the timer. Implements `timer_api_t::stop`.

Example:

```
/* (Optional) Stop the timer. */  
(void) R_AGT_Stop(&g_timer0_ctrl);
```

**Return values**

FSP_SUCCESS	Timer stopped.
FSP_ERR_ASSERTION	p_ctrl was NULL.
FSP_ERR_NOT_OPEN	The instance control structure is not opened.

## ◆ R\_AGT\_Open()

```
fsp_err_t R_AGT_Open ( timer_ctrl_t *const p_ctrl, timer_cfg_t const *const p_cfg )
```

Initializes the AGT module instance. Implements `timer_api_t::open`.

The AGT hardware does not support one-shot functionality natively. The one-shot feature is therefore implemented in the AGT HAL layer. For a timer configured as a one-shot timer, the timer is stopped upon the first timer expiration.

The AGT implementation of the general timer can accept an optional `agt_extended_cfg_t` extension parameter. For AGT, the extension specifies the clock to be used as timer source and the output pin configurations. If the extension parameter is not specified (NULL), the default clock PCLKB is used and the output pins are disabled.

Example:

```
/* Initializes the module. */
err = R_AGT_Open(&g_timer0_ctrl, &g_timer0_cfg);
```

### Return values

FSP_SUCCESS	Initialization was successful and timer has started.
FSP_ERR_ASSERTION	A required input pointer is NULL or the period is not in the valid range of 1 to 0xFFFF.
FSP_ERR_ALREADY_OPEN	R_AGT_Open has already been called for this p_ctrl.
FSP_ERR_IRQ_BSP_DISABLED	A required interrupt has not been enabled in the vector table.
FSP_ERR_IP_CHANNEL_NOT_PRESENT	Requested channel number is not available on AGT.

◆ **R\_AGT\_CallbackSet()**

```
fsp_err_t R_AGT_CallbackSet ( timer_ctrl_t *const p_api_ctrl, void (*)(timer_callback_args_t *)
p_callback, void const *const p_context, timer_callback_args_t *const p_callback_memory )
```

Updates the user callback with the option to provide memory for the callback argument structure. Implements `timer_api_t::callbackSet`.

**Return values**

FSP_SUCCESS	Callback updated successfully.
FSP_ERR_ASSERTION	A required pointer is NULL.
FSP_ERR_NOT_OPEN	The control block has not been opened.
FSP_ERR_NO_CALLBACK_MEMORY	<code>p_callback</code> is non-secure and <code>p_callback_memory</code> is either secure or NULL.

◆ **R\_AGT\_VersionGet()**

```
fsp_err_t R_AGT_VersionGet ( fsp_version_t *const p_version)
```

Sets driver version based on compile time macros. Implements `timer_api_t::versionGet`.

**Return values**

FSP_SUCCESS	Version in <code>p_version</code> .
FSP_ERR_ASSERTION	The parameter <code>p_version</code> is NULL.

**4.2.5 Bluetooth Low Energy Library (r\_ble)**

## Modules

**Functions**

ble\_status\_t [R\\_BLE\\_Open](#) (void)  
Open the BLE protocol stack. [More...](#)

ble\_status\_t [R\\_BLE\\_Close](#) (void)  
Close the BLE protocol stack. [More...](#)



`ble_status_t` [R\\_BLE\\_Execute](#) (void)  
Execute the BLE task. [More...](#)

`uint32_t` [R\\_BLE\\_IsTaskFree](#) (void)  
Check the BLE task queue is free or not. [More...](#)

`ble_status_t` [R\\_BLE\\_SetEvent](#) (`ble_event_cb_t` cb)  
Set event. [More...](#)

`uint32_t` [R\\_BLE\\_GetVersion](#) (void)  
Get the BLE FIT module version. [More...](#)

`uint32_t` [R\\_BLE\\_GetLibType](#) (void)  
Get the type of BLE protocol stack library. [More...](#)

## Detailed Description

Driver for the Radio peripheral on RA MCUs. This module implements the [BLE Interface](#).

## Overview

The bluetooth low energy library (r\_ble) provides an API to control the Radio peripheral. This module is configured via the [QE for BLE](#). QE for BLE provides standard services defined by standardization organization and custom services defined by user. [Bluetooth LE Profile API Document User's Manual](#) describes the APIs for standard services.

## Features

- Common
  - Open/Close the BLE protocol stack.
  - Execute the BLE job.
  - Add an event in the BLE protocol stack internal queue.
- [GAP](#)
  - Initialization of the Host stack.
  - Start/Stop Advertising.
  - Start/Stop Scan.
  - Connect/Disconnect a link.
  - Initiate/Respond a pairing request.
- [GATT Common](#)
  - Get MTU size.
- [GATT Server](#)
  - Initialization of GATT Server.
  - Notification/Indication.
- [GATT Client](#)

- Discovery services, characteristics.
- Read/Write characteristic.
- L2CAP
  - Credit-based flow control transaction.
- Vendor Specific
  - DTM.
  - Set/Get transmit power.
  - Set/Get BD\_ADDR.

## Target Devices

The Renesas Bluetooth Low Energy Library supports the following devices.

- RA4W1

# Configuration

## Clock Configuration

### Note

*System clock (ICLK): 8 MHz or more*

*Peripheral module clock A (PCLKA): 8MHz or more*

*The BLE Protocol Stack is optimized for ICLK and PCLKA frequencies of 32 MHz.*

*It is recommended that the clock be set so that the ICLK and PCLKA frequencies are 32MHz in order to get the best performance from the BLE.*

## Pin Configuration

This module does not use I/O pins.

# Usage Notes

Figure shows the software structure of the BLE FSP module.

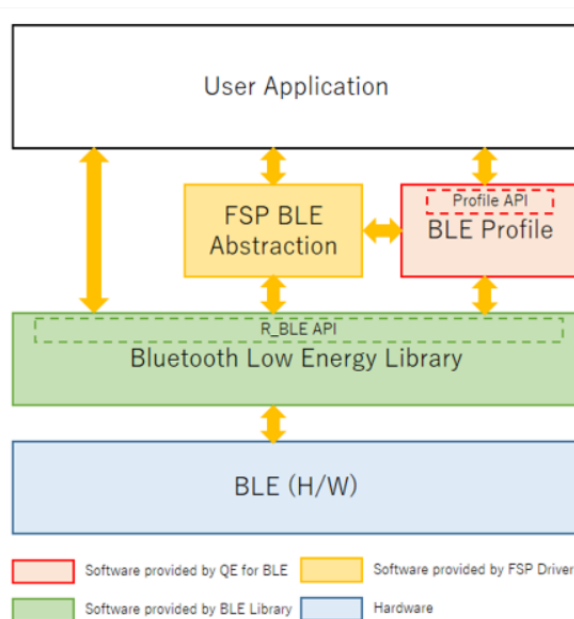


Figure 150: BLE software structure

The BLE FSP module consists of the BLE library.  
 The BLE Application uses the BLE functions via the [R\\_BLE API](#) provided by the BLE Library.  
 The QE for BLE generates the source codes (BLE base skeleton program) as a base for the BLE Application and the BLE Profile codes including the Profile API.

## Limitations

Developers should be aware of the following limitations when using the ble:

### Modules

GAP

GATT\_COMMON

GATT\_SERVER

GATT\_CLIENT

L2CAP

VS

### Typedefs

```
typedef void(* ble_event_cb_t) (void)
```

ble\_event\_cb\_t is the callback function type for [R\\_BLE\\_SetEvent\(\)](#).  
[More...](#)

### Typedef Documentation

#### ◆ ble\_event\_cb\_t

ble\_event\_cb\_t

ble\_event\_cb\_t is the callback function type for [R\\_BLE\\_SetEvent\(\)](#).

#### Parameters

[in]

void

#### Returns

none

### Function Documentation

**◆ R\_BLE\_Open()**

ble\_status\_t R\_BLE\_Open ( void )

Open the BLE protocol stack.

This function should be called once before using the BLE protocol stack.

**Return values**

BLE_SUCCESS(0x0000)	Success
---------------------	---------

**◆ R\_BLE\_Close()**

ble\_status\_t R\_BLE\_Close ( void )

Close the BLE protocol stack.

This function should be called once to close the BLE protocol stack.

**Return values**

BLE_SUCCESS(0x0000)	Success
---------------------	---------

**◆ R\_BLE\_Execute()**

ble\_status\_t R\_BLE\_Execute ( void )

Execute the BLE task.

This handles all the task queued in the BLE protocol stack internal task queue and return. This function should be called repeatedly in the main loop.

**Return values**

BLE_SUCCESS(0x0000)	Success
---------------------	---------

◆ **R\_BLE\_IsTaskFree()**

uint32\_t R\_BLE\_IsTaskFree ( void )

Check the BLE task queue is free or not.

This function returns the BLE task queue free status. When this function returns 0x0, call [R\\_BLE\\_Execute\(\)](#) to execute the BLE task.

**Return values**

0x0	BLE task queue is not free
0x1	BLE task queue is free

◆ **R\_BLE\_SetEvent()**

ble\_status\_t R\_BLE\_SetEvent ( ble\_event\_cb\_t cb)

Set event.

This function add an event in the BLE protocol stack internal queue. The event is handled in [R\\_BLE\\_Execute](#) just like Bluetooth event. This function is intended to be called in hardware interrupt context. Even if calling this function with the same cb before the cb is invoked, only one event is registered. The maximum number of the events can be registered at a time is eight.

**Parameters**

cb	The callback for the event.
----	-----------------------------

**Return values**

BLE_SUCCESS(0x0000)	Success
BLE_ERR_ALREADY_IN_PROGRESS(0x000A)	The event already registered with the callback.
BLE_ERR_CONTEXT_FULL(0x000B)	No free slot for the event.

◆ **R\_BLE\_GetVersion()**

uint32\_t R\_BLE\_GetVersion ( void )

Get the BLE FIT module version.

This function returns the BLE FIT module version.

The major version(BLE\_VERSION\_MAJOR) is contained in the two most significant bytes, and the minor version(BLE\_VERSION\_MINOR) occupies the remaining two bytes.

**Return values**

BLE_VERSION_MAJOR   BLE_VERSION_MINOR	
---------------------------------------	--

### ◆ R\_BLE\_GetLibType()

uint32\_t R\_BLE\_GetLibType ( void )

Get the type of BLE protocol stack library.

This function returns the type of BLE protocol stack library.

#### Return values

BLE_LIB_ALL_FEATS(0x00)	All Features
BLE_LIB_BALANCE(0x01)	Balance
BLE_LIB_COMPACT(0x02)	Compact

### 4.2.5.2 GATT\_COMMON

Modules » [Bluetooth Low Energy Library \(r\\_ble\)](#)

#### Functions

ble\_status\_t R\_BLE\_GATT\_GetMtu (uint16\_t conn\_hdl, uint16\_t \*p\_mtu)

This function gets the current MTU used in GATT communication.

[More...](#)

#### Detailed Description

#### Function Documentation

◆ **R\_BLE\_GATT\_GetMtu()**

```
ble_status_t R_BLE_GATT_GetMtu ( uint16_t conn_hdl, uint16_t* p_mtu )
```

This function gets the current MTU used in GATT communication.

Both GATT server and GATT Client can use this function.

The result of this API call is returned by a return value.

**Parameters**

[in]	conn_hdl	Connection handle identifying the GATT Server or the GATT Client.
[in]	p_mtu	The Current MTU. Before MTU exchange, this parameter is 23 bytes. After MTU exchange, this parameter is the negotiated MTU.

**Return values**

BLE_SUCCESS(0x0000)	Success
BLE_ERR_INVALID_PTR(0x0001)	The mtu parameter is NULL.
BLE_ERR_INVALID_HDL(0x000E)	The GATT Server or the GATT Client specified by conn_hdl was not found.

**4.2.6 Clock Frequency Accuracy Measurement Circuit (r\_cac)**

## Modules

**Functions**

```
fsp_err_t R_CAC_Open (cac_ctrl_t *const p_ctrl, cac_cfg_t const *const p_cfg)
```

```
fsp_err_t R_CAC_StartMeasurement (cac_ctrl_t *const p_ctrl)
```

```
fsp_err_t R_CAC_StopMeasurement (cac_ctrl_t *const p_ctrl)
```

```
fsp_err_t R_CAC_Read (cac_ctrl_t *const p_ctrl, uint16_t *const p_counter)
```

```
fsp_err_t R_CAC_Close (cac_ctrl_t *const p_ctrl)
```

```
fsp_err_t R_CAC_VersionGet (fsp_version_t *const p_version)
```

```
fsp_err_t R_CAC_CallbackSet (cac_ctrl_t *const p_ctrl, void(*p_callback)(cac_callback_args_t *), void const *const
```

```
p_context, cac_callback_args_t *const p_callback_memory)
```

## Detailed Description

Driver for the CAC peripheral on RA MCUs. This module implements the [CAC Interface](#).

## Overview

The interface for the clock frequency accuracy measurement circuit (CAC) peripheral is used to check a system clock frequency with a reference clock signal by counting the number of measurement clock edges that occur between two edges of the reference clock.

## Features

- Supports clock frequency-measurement and monitoring based on a reference signal input
- Reference can be either an externally supplied clock source or an internal clock source
- An interrupt request may optionally be generated by a completed measurement, a detected frequency error, or a counter overflow.
- A digital filter is available for an externally supplied reference clock, and dividers are available for both internally supplied measurement and reference clocks.
- Edge-detection options for the reference clock are configurable as rising, falling, or both.

## Configuration

### Build Time Configurations for r\_cac

The following build time configurations are defined in fsp\_cfg/r\_cac\_cfg.h:

Configuration	Options	Default	Description
Parameter Checking	<ul style="list-style-type: none"> <li>• Default (BSP)</li> <li>• Enabled</li> <li>• Disabled</li> </ul>	Default (BSP)	If selected code for parameter checking is included in the build.

### Configurations for Driver > Monitoring > Clock Accuracy Circuit Driver on r\_cac

This module can be added to the Stacks tab via New Stack > Driver > Monitoring > Clock Accuracy Circuit Driver on r\_cac. Non-secure callable guard functions can be generated for this module by right clicking the module in the RA Configuration tool and checking the "Non-secure Callable" box.

Configuration	Options	Default	Description
Name	Name must be a valid C symbol	g_cac0	Module name.
Reference clock divider	<ul style="list-style-type: none"> <li>• 32</li> <li>• 128</li> <li>• 1024</li> <li>• 8192</li> </ul>	32	Reference clock divider.
Reference clock source	<ul style="list-style-type: none"> <li>• Main Oscillator</li> <li>• Sub-clock</li> </ul>	Main Oscillator	Reference clock source.



	<ul style="list-style-type: none"> <li>• HOCO</li> <li>• MOCO</li> <li>• LOCO</li> <li>• PCLKB</li> <li>• IWDT</li> <li>• External</li> </ul>		
Reference clock digital filter	<ul style="list-style-type: none"> <li>• Disabled</li> <li>• Sampling clock =Measuring freq</li> <li>• Sampling clock =Measuring freq/4</li> <li>• Sampling clock =Measuring freq/16</li> </ul>	Disabled	Reference clock digital filter.
Reference clock edge detect	<ul style="list-style-type: none"> <li>• Rising</li> <li>• Falling</li> <li>• Both</li> </ul>	Rising	Reference clock edge detection.
Measurement clock divider	<ul style="list-style-type: none"> <li>• 1</li> <li>• 4</li> <li>• 8</li> <li>• 32</li> </ul>	1	Measurement clock divider.
Measurement clock source	<ul style="list-style-type: none"> <li>• Main Oscillator</li> <li>• Sub-clock</li> <li>• HOCO</li> <li>• MOCO</li> <li>• LOCO</li> <li>• PCLKB</li> <li>• IWDT</li> </ul>	HOCO	Measurement clock source.
Upper Limit Threshold	Value must be a non-negative integer, between 0 to 65535	0	Top end of allowable range for measurement completion.
Lower Limit Threshold	Value must be a non-negative integer, between 0 to 65535	0	Bottom end of allowable range for measurement completion.
Frequency Error Interrupt Priority	MCU Specific Options		CAC frequency error interrupt priority.
Measurement End Interrupt Priority	MCU Specific Options		CAC measurement end interrupt priority.
Overflow Interrupt Priority	MCU Specific Options		CAC overflow interrupt priority.
Callback	Name must be a valid C symbol	NULL	Function name for callback

## Clock Configuration

The CAC measurement clock source can be configured as the following:

1. MAIN\_OSC
2. SUBCLOCK
3. HOCO
4. MOCO
5. LOCO
6. PCLKB
7. IWDT

The CAC reference clock source can be configured as the following:

1. MAIN\_OSC
2. SUBCLOCK
3. HOCO
4. MOCO
5. LOCO
6. PCLKB
7. IWDT
8. External Clock Source (CACREF)

### Pin Configuration

The CACREF pin can be configured to provide the reference clock for CAC measurements.

## Usage Notes

### Measurement Accuracy

The clock measurement result may be off by up to one pulse depending on the phase difference between the edge detection circuit, digital filter, and CACREF pin signal, if applicable.

### Frequency Error Interrupt

The frequency error interrupt is only triggered at the end of a CAC measurement. This means that there will be a measurement complete interrupt in addition to the frequency error interrupt.

## Examples

### Basic Example

This is a basic example of minimal use of the CAC in an application.

```
volatile uint32_t g_callback_complete;
void cac_basic_example ()
{
    g_callback_complete = 0;
    fsp_err_t err = R_CAC_Open(&g_cac_ctrl, &g_cac_cfg);
    /* Handle any errors. This function should be defined by the user. */
    handle_error(err);
    (void) R_CAC_StartMeasurement(&g_cac_ctrl);
}
```

```
/* Wait for measurement to complete. */
while (0 == g_callback_complete)
{
}

uint16_t value;

/* Read the CAC measurement. */
(void) R_CAC_Read(&g_cac_ctrl, &value);
}

/* Called when measurement is completed. */
static void r_cac_callback (cac_callback_args_t * p_args)
{
    if (CAC_EVENT_MEASUREMENT_COMPLETE == p_args->event)
    {
        g_callback_complete = 1U;
    }
}
```

## Data Structures

struct [cac\\_instance\\_ctrl\\_t](#)

## Data Structure Documentation

### ◆ [cac\\_instance\\_ctrl\\_t](#)

struct [cac\\_instance\\_ctrl\\_t](#)

CAC instance control block. DO NOT INITIALIZE.

## Function Documentation

◆ **R\_CAC\_Open()**

```
fsp_err_t R_CAC_Open ( cac_ctrl_t *const p_ctrl, cac_cfg_t const *const p_cfg )
```

The Open function configures the CAC based on the provided user configuration settings.

**Return values**

FSP_SUCCESS	CAC is available and available for measurement(s).
FSP_ERR_ASSERTION	An argument is invalid.
FSP_ERR_ALREADY_OPEN	The CAC has already been opened.

*Note*

*There is only a single CAC peripheral.*

◆ **R\_CAC\_StartMeasurement()**

```
fsp_err_t R_CAC_StartMeasurement ( cac_ctrl_t *const p_ctrl)
```

Start the CAC measurement process.

**Return values**

FSP_SUCCESS	CAC measurement started.
FSP_ERR_ASSERTION	NULL provided for p_instance_ctrl or p_cfg.
FSP_ERR_NOT_OPEN	<a href="#">R_CAC_Open()</a> has not been successfully called.

◆ **R\_CAC\_StopMeasurement()**

```
fsp_err_t R_CAC_StopMeasurement ( cac_ctrl_t *const p_ctrl)
```

Stop the CAC measurement process.

**Return values**

FSP_SUCCESS	CAC measuring has been stopped.
FSP_ERR_ASSERTION	NULL provided for p_instance_ctrl or p_cfg.
FSP_ERR_NOT_OPEN	<a href="#">R_CAC_Open()</a> has not been successfully called.

◆ **R\_CAC\_Read()**

```
fsp_err_t R_CAC_Read ( cac_ctrl_t *const p_ctrl, uint16_t *const p_counter )
```

Read and return the CAC status and counter registers.

**Return values**

FSP_SUCCESS	CAC read successful.
FSP_ERR_ASSERTION	An argument is NULL.
FSP_ERR_NOT_OPEN	R_CAC_Open() has not been successfully called.

◆ **R\_CAC\_Close()**

```
fsp_err_t R_CAC_Close ( cac_ctrl_t *const p_ctrl)
```

Release any resources that were allocated by the Open() or any subsequent CAC operations.

**Return values**

FSP_SUCCESS	Successful close.
FSP_ERR_ASSERTION	NULL provided for p_instance_ctrl or p_cfg.
FSP_ERR_NOT_OPEN	R_CAC_Open() has not been successfully called.

◆ **R\_CAC\_VersionGet()**

```
fsp_err_t R_CAC_VersionGet ( fsp_version_t *const p_version)
```

Get the API and code version information.

**Return values**

FSP_SUCCESS	Version info returned.
FSP_ERR_ASSERTION	An argument is NULL.

**◆ R\_CAC\_CallbackSet()**

```
fsp_err_t R_CAC_CallbackSet ( cac_ctrl_t *const p_ctrl, void(*) (cac_callback_args_t *) p_callback,
void const *const p_context, cac_callback_args_t *const p_callback_memory )
```

Updates the user callback with the option to provide memory for the callback argument structure. Implements `cac_api_t::callbackSet`.

**Return values**

FSP_SUCCESS	Callback updated successfully.
FSP_ERR_ASSERTION	A required pointer is NULL.
FSP_ERR_NOT_OPEN	The control block has not been opened.
FSP_ERR_NO_CALLBACK_MEMORY	<code>p_callback</code> is non-secure and <code>p_callback_memory</code> is either secure or NULL.

**4.2.7 Controller Area Network (r\_can)**

## Modules

**Functions**

```
fsp_err_t R_CAN_Open (can_ctrl_t *const p_api_ctrl, can_cfg_t const *const
p_cfg)
```

```
fsp_err_t R_CAN_Close (can_ctrl_t *const p_api_ctrl)
```

```
fsp_err_t R_CAN_Write (can_ctrl_t *const p_api_ctrl, uint32_t const mailbox,
can_frame_t *const p_frame)
```

```
fsp_err_t R_CAN_ModeTransition (can_ctrl_t *const p_api_ctrl,
can_operation_mode_t operation_mode, can_test_mode_t test_mode)
```

```
fsp_err_t R_CAN_InfoGet (can_ctrl_t *const p_api_ctrl, can_info_t *const p_info)
```

```
fsp_err_t R_CAN_CallbackSet (can_ctrl_t *const p_api_ctrl,
void(*p_callback)(can_callback_args_t *), void const *const
p_context, can_callback_args_t *const p_callback_memory)
```

```
fsp_err_t R_CAN_VersionGet (fsp_version_t *const version)
```

**Detailed Description**

Driver for the CAN peripheral on RA MCUs. This module implements the [CAN Interface](#).

## Overview

The Controller Area network (CAN) HAL module provides a high-level API for CAN applications and supports the CAN peripherals available on RA microcontroller hardware. A user-callback function must be defined that the driver will invoke when transmit, receive or error interrupts are received. The callback is passed a parameter which indicates the channel, mailbox and event as well as the received data (if available).

### Features

- Supports both standard (11-bit) and extended (29-bit) messaging formats
- Supports speeds upto 1 Mbps
- Support for bit timing configuration as defined in the CAN specification
- Supports up to 32 transmit or receive mailboxes with standard or extended ID frames
- Receive mailboxes can be configured to capture either data or remote CAN Frames
- Receive mailboxes can be configured to receive a range of IDs using mailbox masks
- Mailboxes can be configured with Overwrite or Overrun mode
- Supports a user-callback function when transmit, receive, or error interrupts are received

## Configuration

### Build Time Configurations for r\_can

The following build time configurations are defined in fsp\_cfg/r\_can\_cfg.h:

Configuration	Options	Default	Description
Parameter Checking	<ul style="list-style-type: none"> <li>• Default (BSP)</li> <li>• Enabled</li> <li>• Disabled</li> </ul>	Default (BSP)	If selected code for parameter checking is included in the build.

### Configurations for Driver > Connectivity > CAN Driver on r\_can

This module can be added to the Stacks tab via New Stack > Driver > Connectivity > CAN Driver on r\_can. Non-secure callable guard functions can be generated for this module by right clicking the module in the RA Configuration tool and checking the "Non-secure Callable" box.

Configuration	Options	Default	Description
General > Name	Name must be a valid C symbol	g_can0	Module name.
General > Channel	Channel should be 0 or 1	0	Specify the CAN channel to use.
General > Clock Source	MCU Specific Options		Select the CAN clock source.
General > Overwrite/Overrun Mode	<ul style="list-style-type: none"> <li>• Overwrite Mode</li> <li>• Overrun Mode</li> </ul>	Overwrite Mode	Select whether receive mailbox will be overwritten or overrun if data is not read in time.

General > Standard or Extended ID Mode	<ul style="list-style-type: none"> <li>Standard ID Mode</li> <li>Extended ID Mode</li> </ul>	Standard ID Mode	Select whether the driver will use the CAN standard or extended IDs.
General > Number of Mailboxes	<ul style="list-style-type: none"> <li>4 Mailboxes</li> <li>8 Mailboxes</li> <li>16 Mailboxes</li> <li>32 Mailboxes</li> </ul>	32 Mailboxes	Select 4, 8, 16 or 32 mailboxes.
Baud Rate Settings > Auto-generated Settings > Sample-Point (%)	Must be a valid integer between 0 and 100. Ignore when Override Baud Settings is Enabled.	75	Sample-Point = (TSEG1 + 1) / (TSEG1 + TSEG2 + 1).
Baud Rate Settings > Auto-generated Settings > CAN Baud Rate (Hz)	Must be a valid integer configurable upto maximum 1MHz. Ignore when Override Baud Settings is Enabled.	500000	Specify baud rate in Hz.
Baud Rate Settings > Override Auto-generated Settings > Override Baud Settings	<ul style="list-style-type: none"> <li>Enabled</li> <li>Disabled</li> </ul>	Disabled	Override calculated baudrate parameters and instead use the ones specified below. This option ignores the parameters specified under Sample-Point (%) and CAN Baud Rate (Hz)
Baud Rate Settings > Override Auto-generated Settings > Baud Rate Prescaler	Value must be a non-negative integer between 1 and 1024.	1	Specify division value of baud rate prescaler (baud rate prescaler + 1).
Baud Rate Settings > Override Auto-generated Settings > Time Segment 1	Refer to the RA Configuration tool for available options.	4 Time Quanta	Select the time segment 1 value. (4-16). Check module usage notes for how to calculate this value.
Baud Rate Settings > Override Auto-generated Settings > Time Segment 2	<ul style="list-style-type: none"> <li>2 Time Quanta</li> <li>3 Time Quanta</li> <li>4 Time Quanta</li> <li>5 Time Quanta</li> <li>6 Time Quanta</li> <li>7 Time Quanta</li> <li>8 Time Quanta</li> </ul>	2 Time Quanta	Select the time segment 2 value (2-8). Check module usage notes for how to calculate this value.
Baud Rate Settings > Override Auto-generated Settings > Synchronization Jump Width	<ul style="list-style-type: none"> <li>1 Time Quanta</li> <li>2 Time Quanta</li> <li>3 Time Quanta</li> <li>4 Time Quanta</li> </ul>	1 Time Quanta	Select the Synchronization Jump Width value (1-4). Check module usage notes for how to calculate this value.



Interrupts > Callback	Name must be a valid C symbol	can_callback	A user callback function. If this callback function is provided, it is called from the interrupt service routine (ISR) each time any interrupt occurs.
Interrupts > Interrupt Priority Level	MCU Specific Options		Error/Receive/Transmit interrupt priority.
Input > Mailbox 0-3 Group > Mailbox ID > Mailbox 0 ID	Value must be decimal or HEX integer of 0x1FFFFFFF or less.	0	Select the receive ID for mailbox 0, between 0 and 0x7ff when using standard IDs, between 0 and 0x1FFFFFFF when using extended IDs. Value is not used when the mailbox is set as transmit type.
Input > Mailbox 0-3 Group > Mailbox ID > Mailbox 1 ID	Value must be decimal or HEX integer of 0x1FFFFFFF or less.	1	Select the receive ID for mailbox 1, between 0 and 0x7ff when using standard IDs, between 0 and 0x1FFFFFFF when using extended IDs. Value is not used when the mailbox is set as transmit type.
Input > Mailbox 0-3 Group > Mailbox ID > Mailbox 2 ID	Value must be decimal or HEX integer of 0x1FFFFFFF or less.	2	Select the receive ID for mailbox 2, between 0 and 0x7ff when using standard IDs, between 0 and 0x1FFFFFFF when using extended IDs. Value is not used when the mailbox is set as transmit type.
Input > Mailbox 0-3 Group > Mailbox ID > Mailbox 3 ID	Value must be decimal or HEX integer of 0x1FFFFFFF or less.	3	Select the receive ID for mailbox 3, between 0 and 0x7ff when using standard IDs, between 0 and 0x1FFFFFFF when using extended IDs. Value is not used when the mailbox is set as transmit type.
Input > Mailbox 0-3 Group > Mailbox Type > Mailbox 0 Type	<ul style="list-style-type: none"> <li>Receive Mailbox</li> <li>Transmit Mailbox</li> </ul>	Transmit Mailbox	Select whether the mailbox is used for receive or transmit.
Input > Mailbox 0-3	<ul style="list-style-type: none"> <li>Receive</li> </ul>	Receive Mailbox	Select whether the

Group > Mailbox Type > Mailbox 1 Type	Mailbox • Transmit Mailbox		mailbox is used for receive or transmit.
Input > Mailbox 0-3 Group > Mailbox Type > Mailbox 2 Type	• Receive Mailbox • Transmit Mailbox	Receive Mailbox	Select whether the mailbox is used for receive or transmit.
Input > Mailbox 0-3 Group > Mailbox Type > Mailbox 3 Type	• Receive Mailbox • Transmit Mailbox	Receive Mailbox	Select whether the mailbox is used for receive or transmit.
Input > Mailbox 0-3 Group > Mailbox Frame Type > Mailbox 0 Frame Type	• Data Mailbox • Remote Mailbox	Remote Mailbox	Select whether the mailbox is used to capture data frames or remote frames (ignored for transmit mailboxes).
Input > Mailbox 0-3 Group > Mailbox Frame Type > Mailbox 1 Frame Type	• Data Mailbox • Remote Mailbox	Data Mailbox	Select whether the mailbox is used to capture data frames or remote frames (ignored for transmit mailboxes).
Input > Mailbox 0-3 Group > Mailbox Frame Type > Mailbox 2 Frame Type	• Data Mailbox • Remote Mailbox	Data Mailbox	Select whether the mailbox is used to capture data frames or remote frames (ignored for transmit mailboxes).
Input > Mailbox 0-3 Group > Mailbox Frame Type > Mailbox 3 Frame Type	• Data Mailbox • Remote Mailbox	Data Mailbox	Select whether the mailbox is used to capture data frames or remote frames (ignored for transmit mailboxes).
Input > Mailbox 0-3 Group > Mailbox 0-3 Group Mask	Value must be decimal or HEX integer of 0x1FFFFFFF or less.	0x1FFFFFFF	Select the Mask for mailboxes 0-3.
Input > Mailbox 4-7 Group > Mailbox ID > Mailbox 4 ID	Value must be decimal or HEX integer of 0x1FFFFFFF or less.	4	Select the receive ID for mailbox 4, between 0 and 0x7ff when using standard IDs, between 0 and 0x1FFFFFFF when using extended IDs. Value is not used when the mailbox is set as transmit type.
Input > Mailbox 4-7 Group > Mailbox ID >	Value must be decimal or HEX integer of	5	Select the receive ID for mailbox 5, between

Mailbox 5 ID	0x1FFFFFFF or less.		0 and 0x7ff when using standard IDs, between 0 and 0x1FFFFFFF when using extended IDs. Value is not used when the mailbox is set as transmit type.
Input > Mailbox 4-7 Group > Mailbox ID > Mailbox 6 ID	Value must be decimal or HEX integer of 0x1FFFFFFF or less.	6	Select the receive ID for mailbox 6, between 0 and 0x7ff when using standard IDs, between 0 and 0x1FFFFFFF when using extended IDs. Value is not used when the mailbox is set as transmit type.
Input > Mailbox 4-7 Group > Mailbox ID > Mailbox 7 ID	Value must be decimal or HEX integer of 0x1FFFFFFF or less.	7	Select the receive ID for mailbox 7, between 0 and 0x7ff when using standard IDs, between 0 and 0x1FFFFFFF when using extended IDs. Value is not used when the mailbox is set as transmit type.
Input > Mailbox 4-7 Group > Mailbox Type > Mailbox 4 Type	<ul style="list-style-type: none"> <li>• Receive Mailbox</li> <li>• Transmit Mailbox</li> </ul>	Receive Mailbox	Select whether the mailbox is used for receive or transmit.
Input > Mailbox 4-7 Group > Mailbox Type > Mailbox 5 Type	<ul style="list-style-type: none"> <li>• Receive Mailbox</li> <li>• Transmit Mailbox</li> </ul>	Receive Mailbox	Select whether the mailbox is used for receive or transmit.
Input > Mailbox 4-7 Group > Mailbox Type > Mailbox 6 Type	<ul style="list-style-type: none"> <li>• Receive Mailbox</li> <li>• Transmit Mailbox</li> </ul>	Receive Mailbox	Select whether the mailbox is used for receive or transmit.
Input > Mailbox 4-7 Group > Mailbox Type > Mailbox 7 Type	<ul style="list-style-type: none"> <li>• Receive Mailbox</li> <li>• Transmit Mailbox</li> </ul>	Receive Mailbox	Select whether the mailbox is used for receive or transmit.
Input > Mailbox 4-7 Group > Mailbox Frame Type > Mailbox 4 Frame Type	<ul style="list-style-type: none"> <li>• Data Mailbox</li> <li>• Remote Mailbox</li> </ul>	Data Mailbox	Select whether the mailbox is used to capture data frames or remote frames (ignored for transmit mailboxes).
Input > Mailbox 4-7 Group > Mailbox Frame Type > Mailbox 5	<ul style="list-style-type: none"> <li>• Data Mailbox</li> <li>• Remote Mailbox</li> </ul>	Data Mailbox	Select whether the mailbox is used to capture data frames or

Frame Type			remote frames (ignored for transmit mailboxes).
Input > Mailbox 4-7 Group > Mailbox Frame Type > Mailbox 6 Frame Type	<ul style="list-style-type: none"> <li>• Data Mailbox</li> <li>• Remote Mailbox</li> </ul>	Data Mailbox	Select whether the mailbox is used to capture data frames or remote frames (ignored for transmit mailboxes).
Input > Mailbox 4-7 Group > Mailbox Frame Type > Mailbox 7 Frame Type	<ul style="list-style-type: none"> <li>• Data Mailbox</li> <li>• Remote Mailbox</li> </ul>	Data Mailbox	Select whether the mailbox is used to capture data frames or remote frames (ignored for transmit mailboxes).
Input > Mailbox 4-7 Group > Mailbox 4-7 Group Mask	Value must be decimal or HEX integer of 0x1FFFFFFF or less.	0x1FFFFFFF	>Select the Mask for mailboxes 4-7.
Input > Mailbox 8-11 Group > Mailbox ID > Mailbox 8 ID	Value must be decimal or HEX integer of 0x1FFFFFFF or less.	8	Select the receive ID for mailbox 8, between 0 and 0x7ff when using standard IDs, between 0 and 0x1FFFFFFF when using extended IDs. Value is not used when the mailbox is set as transmit type.
Input > Mailbox 8-11 Group > Mailbox ID > Mailbox 9 ID	Value must be decimal or HEX integer of 0x1FFFFFFF or less.	9	Select the receive ID for mailbox 9, between 0 and 0x7ff when using standard IDs, between 0 and 0x1FFFFFFF when using extended IDs. Value is not used when the mailbox is set as transmit type.
Input > Mailbox 8-11 Group > Mailbox ID > Mailbox 10 ID	Value must be decimal or HEX integer of 0x1FFFFFFF or less.	10	Select the receive ID for mailbox 10, between 0 and 0x7ff when using standard IDs, between 0 and 0x1FFFFFFF when using extended IDs. Value is not used when the mailbox is set as transmit type.
Input > Mailbox 8-11 Group > Mailbox ID > Mailbox 11 ID	Value must be decimal or HEX integer of 0x1FFFFFFF or less.	11	Select the receive ID for mailbox 11, between 0 and 0x7ff when using standard IDs, between 0 and

			0x1FFFFFFF when using extended IDs. Value is not used when the mailbox is set as transmit type.
Input > Mailbox 8-11 Group > Mailbox Type > Mailbox 8 Type	<ul style="list-style-type: none"> <li>• Receive Mailbox</li> <li>• Transmit Mailbox</li> </ul>	Receive Mailbox	Select whether the mailbox is used for receive or transmit.
Input > Mailbox 8-11 Group > Mailbox Type > Mailbox 9 Type	<ul style="list-style-type: none"> <li>• Receive Mailbox</li> <li>• Transmit Mailbox</li> </ul>	Receive Mailbox	Select whether the mailbox is used for receive or transmit.
Input > Mailbox 8-11 Group > Mailbox Type > Mailbox 10 Type	<ul style="list-style-type: none"> <li>• Receive Mailbox</li> <li>• Transmit Mailbox</li> </ul>	Receive Mailbox	Select whether the mailbox is used for receive or transmit.
Input > Mailbox 8-11 Group > Mailbox Type > Mailbox 11 Type	<ul style="list-style-type: none"> <li>• Receive Mailbox</li> <li>• Transmit Mailbox</li> </ul>	Receive Mailbox	Select whether the mailbox is used for receive or transmit.
Input > Mailbox 8-11 Group > Mailbox Frame Type > Mailbox 8 Frame Type	<ul style="list-style-type: none"> <li>• Data Mailbox</li> <li>• Remote Mailbox</li> </ul>	Data Mailbox	Select whether the mailbox is used to capture data frames or remote frames (ignored for transmit mailboxes).
Input > Mailbox 8-11 Group > Mailbox Frame Type > Mailbox 9 Frame Type	<ul style="list-style-type: none"> <li>• Data Mailbox</li> <li>• Remote Mailbox</li> </ul>	Data Mailbox	Select whether the mailbox is used to capture data frames or remote frames (ignored for transmit mailboxes).
Input > Mailbox 8-11 Group > Mailbox Frame Type > Mailbox 10 Frame Type	<ul style="list-style-type: none"> <li>• Data Mailbox</li> <li>• Remote Mailbox</li> </ul>	Data Mailbox	Select whether the mailbox is used to capture data frames or remote frames (ignored for transmit mailboxes).
Input > Mailbox 8-11 Group > Mailbox Frame Type > Mailbox 11 Frame Type	<ul style="list-style-type: none"> <li>• Data Mailbox</li> <li>• Remote Mailbox</li> </ul>	Data Mailbox	Select whether the mailbox is used to capture data frames or remote frames (ignored for transmit mailboxes).
Input > Mailbox 8-11 Group > Mailbox 8-11 Group Mask	Value must be decimal or HEX integer of 0x1FFFFFFF or less.	0x1FFFFFFF	Select the Mask for mailboxes 8-11.
Input > Mailbox 12-15	Value must be decimal	12	Select the receive ID

Group > Mailbox ID > Mailbox 12 ID	or HEX integer of 0x1FFFFFFF or less.		for mailbox 12, between 0 and 0x7ff when using standard IDs, between 0 and 0x1FFFFFFF when using extended IDs. Value is not used when the mailbox is set as transmit type.
Input > Mailbox 12-15 Group > Mailbox ID > Mailbox 13 ID	Value must be decimal or HEX integer of 0x1FFFFFFF or less.	13	Select the receive ID for mailbox 13, between 0 and 0x7ff when using standard IDs, between 0 and 0x1FFFFFFF when using extended IDs. Value is not used when the mailbox is set as transmit type.
Input > Mailbox 12-15 Group > Mailbox ID > Mailbox 14 ID	Value must be decimal or HEX integer of 0x1FFFFFFF or less.	14	Select the receive ID for mailbox 14, between 0 and 0x7ff when using standard IDs, between 0 and 0x1FFFFFFF when using extended IDs. Value is not used when the mailbox is set as transmit type.
Input > Mailbox 12-15 Group > Mailbox ID > Mailbox 15 ID	Value must be decimal or HEX integer of 0x1FFFFFFF or less.	15	Select the receive ID for mailbox 15, between 0 and 0x7ff when using standard IDs, between 0 and 0x1FFFFFFF when using extended IDs. Value is not used when the mailbox is set as transmit type.
Input > Mailbox 12-15 Group > Mailbox Type > Mailbox 12 Type	<ul style="list-style-type: none"> <li>• Receive Mailbox</li> <li>• Transmit Mailbox</li> </ul>	Receive Mailbox	Select whether the mailbox is used for receive or transmit.
Input > Mailbox 12-15 Group > Mailbox Type > Mailbox 13 Type	<ul style="list-style-type: none"> <li>• Receive Mailbox</li> <li>• Transmit Mailbox</li> </ul>	Receive Mailbox	Select whether the mailbox is used for receive or transmit.
Input > Mailbox 12-15 Group > Mailbox Type > Mailbox 14 Type	<ul style="list-style-type: none"> <li>• Receive Mailbox</li> <li>• Transmit Mailbox</li> </ul>	Receive Mailbox	Select whether the mailbox is used for receive or transmit.

Input > Mailbox 12-15 Group > Mailbox Type > Mailbox 15 Type	<ul style="list-style-type: none"> <li>• Receive Mailbox</li> <li>• Transmit Mailbox</li> </ul>	Receive Mailbox	Select whether the mailbox is used for receive or transmit.
Input > Mailbox 12-15 Group > Mailbox Frame Type > Mailbox 12 Frame Type	<ul style="list-style-type: none"> <li>• Data Mailbox</li> <li>• Remote Mailbox</li> </ul>	Data Mailbox	Select whether the mailbox is used to capture data frames or remote frames (ignored for transmit mailboxes).
Input > Mailbox 12-15 Group > Mailbox Frame Type > Mailbox 13 Frame Type	<ul style="list-style-type: none"> <li>• Data Mailbox</li> <li>• Remote Mailbox</li> </ul>	Data Mailbox	Select whether the mailbox is used to capture data frames or remote frames (ignored for transmit mailboxes).
Input > Mailbox 12-15 Group > Mailbox Frame Type > Mailbox 14 Frame Type	<ul style="list-style-type: none"> <li>• Data Mailbox</li> <li>• Remote Mailbox</li> </ul>	Data Mailbox	Select whether the mailbox is used to capture data frames or remote frames (ignored for transmit mailboxes).
Input > Mailbox 12-15 Group > Mailbox Frame Type > Mailbox 15 Frame Type	<ul style="list-style-type: none"> <li>• Data Mailbox</li> <li>• Remote Mailbox</li> </ul>	Data Mailbox	Select whether the mailbox is used to capture data frames or remote frames (ignored for transmit mailboxes).
Input > Mailbox 12-15 Group > Mailbox 12-15 Group Mask	Value must be decimal or HEX integer of 0x1FFFFFFF or less.	0x1FFFFFFF	Select the Mask for mailboxes 12-15.
Input > Mailbox 16-19 Group > Mailbox ID > Mailbox 16 ID	Value must be decimal or HEX integer of 0x1FFFFFFF or less.	16	Select the receive ID for mailbox 16, between 0 and 0x7ff when using standard IDs, between 0 and 0x1FFFFFFF when using extended IDs. Value is not used when the mailbox is set as transmit type.
Input > Mailbox 16-19 Group > Mailbox ID > Mailbox 17 ID	Value must be decimal or HEX integer of 0x1FFFFFFF or less.	17	Select the receive ID for mailbox 17, between 0 and 0x7ff when using standard IDs, between 0 and 0x1FFFFFFF when using extended IDs. Value is not used when the mailbox is set as transmit type.

Input > Mailbox 16-19 Group > Mailbox ID > Mailbox 18 ID	Value must be decimal or HEX integer of 0x1FFFFFFF or less.	18	Select the receive ID for mailbox 18, between 0 and 0x7ff when using standard IDs, between 0 and 0x1FFFFFFF when using extended IDs. Value is not used when the mailbox is set as transmit type.
Input > Mailbox 16-19 Group > Mailbox ID > Mailbox 19 ID	Value must be decimal or HEX integer of 0x1FFFFFFF or less.	19	Select the receive ID for mailbox 19, between 0 and 0x7ff when using standard IDs, between 0 and 0x1FFFFFFF when using extended IDs. Value is not used when the mailbox is set as transmit type.
Input > Mailbox 16-19 Group > Mailbox Type > Mailbox 16 Type	<ul style="list-style-type: none"> <li>• Receive Mailbox</li> <li>• Transmit Mailbox</li> </ul>	Receive Mailbox	Select whether the mailbox is used for receive or transmit.
Input > Mailbox 16-19 Group > Mailbox Type > Mailbox 17 Type	<ul style="list-style-type: none"> <li>• Receive Mailbox</li> <li>• Transmit Mailbox</li> </ul>	Receive Mailbox	Select whether the mailbox is used for receive or transmit.
Input > Mailbox 16-19 Group > Mailbox Type > Mailbox 18 Type	<ul style="list-style-type: none"> <li>• Receive Mailbox</li> <li>• Transmit Mailbox</li> </ul>	Receive Mailbox	Select whether the mailbox is used for receive or transmit.
Input > Mailbox 16-19 Group > Mailbox Type > Mailbox 19 Type	<ul style="list-style-type: none"> <li>• Receive Mailbox</li> <li>• Transmit Mailbox</li> </ul>	Receive Mailbox	Select whether the mailbox is used for receive or transmit.
Input > Mailbox 16-19 Group > Mailbox Frame Type > Mailbox 16 Frame Type	<ul style="list-style-type: none"> <li>• Data Mailbox</li> <li>• Remote Mailbox</li> </ul>	Data Mailbox	Select whether the mailbox is used to capture data frames or remote frames (ignored for transmit mailboxes).
Input > Mailbox 16-19 Group > Mailbox Frame Type > Mailbox 17 Frame Type	<ul style="list-style-type: none"> <li>• Data Mailbox</li> <li>• Remote Mailbox</li> </ul>	Data Mailbox	Select whether the mailbox is used to capture data frames or remote frames (ignored for transmit mailboxes).
Input > Mailbox 16-19 Group > Mailbox Frame Type > Mailbox 18 Frame Type	<ul style="list-style-type: none"> <li>• Data Mailbox</li> <li>• Remote Mailbox</li> </ul>	Data Mailbox	Select whether the mailbox is used to capture data frames or remote frames (ignored for transmit mailboxes).
Input > Mailbox 16-19 Group > Mailbox Frame Type > Mailbox 19 Frame Type	<ul style="list-style-type: none"> <li>• Data Mailbox</li> <li>• Remote Mailbox</li> </ul>	Data Mailbox	Select whether the mailbox is used to capture data frames or remote frames (ignored for transmit mailboxes).



Type > Mailbox 18 Frame Type			capture data frames or remote frames (ignored for transmit mailboxes).
Input > Mailbox 16-19 Group > Mailbox Frame Type > Mailbox 19 Frame Type	<ul style="list-style-type: none"> <li>• Data Mailbox</li> <li>• Remote Mailbox</li> </ul>	Data Mailbox	Select whether the mailbox is used to capture data frames or remote frames (ignored for transmit mailboxes).
Input > Mailbox 16-19 Group > Mailbox 16-19 Group Mask	Value must be decimal or HEX integer of 0x1FFFFFFF or less.	0x1FFFFFFF	Select the Mask for mailboxes 16-19.
Input > Mailbox 20-23 Group > Mailbox ID > Mailbox 20 ID	Value must be decimal or HEX integer of 0x1FFFFFFF or less.	20	Select the receive ID for mailbox 20, between 0 and 0x7ff when using standard IDs, between 0 and 0x1FFFFFFF when using extended IDs. Value is not used when the mailbox is set as transmit type.
Input > Mailbox 20-23 Group > Mailbox ID > Mailbox 21 ID	Value must be decimal or HEX integer of 0x1FFFFFFF or less.	21	Select the receive ID for mailbox 21, between 0 and 0x7ff when using standard IDs, between 0 and 0x1FFFFFFF when using extended IDs. Value is not used when the mailbox is set as transmit type.
Input > Mailbox 20-23 Group > Mailbox ID > Mailbox 22 ID	Value must be decimal or HEX integer of 0x1FFFFFFF or less.	22	Select the receive ID for mailbox 22, between 0 and 0x7ff when using standard IDs, between 0 and 0x1FFFFFFF when using extended IDs. Value is not used when the mailbox is set as transmit type.
Input > Mailbox 20-23 Group > Mailbox ID > Mailbox 23 ID	Value must be decimal or HEX integer of 0x1FFFFFFF or less.	23	Select the receive ID for mailbox 23, between 0 and 0x7ff when using standard IDs, between 0 and 0x1FFFFFFF when using extended IDs. Value is not used when the

mailbox is set as transmit type.

Input > Mailbox 20-23 Group > Mailbox Type > Mailbox 20 Type

- Receive Mailbox
- Transmit Mailbox

Receive Mailbox

Select whether the mailbox is used for receive or transmit.

Input > Mailbox 20-23 Group > Mailbox Type > Mailbox 21 Type

- Receive Mailbox
- Transmit Mailbox

Receive Mailbox

Select whether the mailbox is used for receive or transmit.

Input > Mailbox 20-23 Group > Mailbox Type > Mailbox 22 Type

- Receive Mailbox
- Transmit Mailbox

Receive Mailbox

Select whether the mailbox is used for receive or transmit.

Input > Mailbox 20-23 Group > Mailbox Type > Mailbox 23 Type

- Receive Mailbox
- Transmit Mailbox

Receive Mailbox

Select whether the mailbox is used for receive or transmit.

Input > Mailbox 20-23 Group > Mailbox Frame Type > Mailbox 20 Frame Type

- Data Mailbox
- Remote Mailbox

Data Mailbox

Select whether the mailbox is used to capture data frames or remote frames (ignored for transmit mailboxes).

Input > Mailbox 20-23 Group > Mailbox Frame Type > Mailbox 21 Frame Type

- Data Mailbox
- Remote Mailbox

Data Mailbox

Select whether the mailbox is used to capture data frames or remote frames (ignored for transmit mailboxes).

Input > Mailbox 20-23 Group > Mailbox Frame Type > Mailbox 22 Frame Type

- Data Mailbox
- Remote Mailbox

Data Mailbox

Select whether the mailbox is used to capture data frames or remote frames (ignored for transmit mailboxes).

Input > Mailbox 20-23 Group > Mailbox Frame Type > Mailbox 23 Frame Type

- Data Mailbox
- Remote Mailbox

Data Mailbox

Select whether the mailbox is used to capture data frames or remote frames (ignored for transmit mailboxes).

Input > Mailbox 20-23 Group > Mailbox 20-23 Group Mask

Value must be decimal or HEX integer of 0x1FFFFFFF or less.

0x1FFFFFFF

Select the Mask for mailboxes 20-23

Input > Mailbox 24-27 Group > Mailbox ID > Mailbox 24 ID

Value must be decimal or HEX integer of 0x1FFFFFFF or less.

24

Select the receive ID for mailbox 24, between 0 and 0x7ff when using standard

IDs, between 0 and 0x1FFFFFFF when using extended IDs. Value is not used when the mailbox is set as transmit type.

Select the receive ID for mailbox 25, between 0 and 0x7ff when using standard IDs, between 0 and 0x1FFFFFFF when using extended IDs. Value is not used when the mailbox is set as transmit type.

Select the receive ID for mailbox 26, between 0 and 0x7ff when using standard IDs, between 0 and 0x1FFFFFFF when using extended IDs. Value is not used when the mailbox is set as transmit type.

Select the receive ID for mailbox 27, between 0 and 0x7ff when using standard IDs, between 0 and 0x1FFFFFFF when using extended IDs. Value is not used when the mailbox is set as transmit type.

Select whether the mailbox is used for receive or transmit.

Select whether the mailbox is used for receive or transmit.

Select whether the mailbox is used for receive or transmit.

Select whether the mailbox is used for receive or transmit.

Input > Mailbox 24-27 Group > Mailbox ID > Mailbox 25 ID      Value must be decimal or HEX integer of 0x1FFFFFFF or less.      25

Input > Mailbox 24-27 Group > Mailbox ID > Mailbox 26 ID      Value must be decimal or HEX integer of 0x1FFFFFFF or less.      26

Input > Mailbox 24-27 Group > Mailbox ID > Mailbox 27 ID      Value must be decimal or HEX integer of 0x1FFFFFFF or less.      27

Input > Mailbox 24-27 Group > Mailbox Type > Mailbox 24 Type      

- Receive Mailbox
- Transmit Mailbox

      Receive Mailbox

Input > Mailbox 24-27 Group > Mailbox Type > Mailbox 25 Type      

- Receive Mailbox
- Transmit Mailbox

      Receive Mailbox

Input > Mailbox 24-27 Group > Mailbox Type > Mailbox 26 Type      

- Receive Mailbox
- Transmit Mailbox

      Receive Mailbox

Input > Mailbox 24-27 Group > Mailbox Type > Mailbox 27 Type      

- Receive Mailbox
- Transmit

      Receive Mailbox

## Mailbox

Input > Mailbox 24-27 Group > Mailbox Frame Type > Mailbox 24 Frame Type	<ul style="list-style-type: none"> <li>• Data Mailbox</li> <li>• Remote Mailbox</li> </ul>	Data Mailbox	Select whether the mailbox is used to capture data frames or remote frames (ignored for transmit mailboxes).
Input > Mailbox 24-27 Group > Mailbox Frame Type > Mailbox 25 Frame Type	<ul style="list-style-type: none"> <li>• Data Mailbox</li> <li>• Remote Mailbox</li> </ul>	Data Mailbox	Select whether the mailbox is used to capture data frames or remote frames (ignored for transmit mailboxes).
Input > Mailbox 24-27 Group > Mailbox Frame Type > Mailbox 26 Frame Type	<ul style="list-style-type: none"> <li>• Data Mailbox</li> <li>• Remote Mailbox</li> </ul>	Data Mailbox	Select whether the mailbox is used to capture data frames or remote frames (ignored for transmit mailboxes).
Input > Mailbox 24-27 Group > Mailbox Frame Type > Mailbox 27 Frame Type	<ul style="list-style-type: none"> <li>• Data Mailbox</li> <li>• Remote Mailbox</li> </ul>	Data Mailbox	Select whether the mailbox is used to capture data frames or remote frames (ignored for transmit mailboxes).
Input > Mailbox 24-27 Group > Mailbox 24-27 Group Mask	Value must be decimal or HEX integer of 0x1FFFFFFF or less.	0x1FFFFFFF	Select the Mask for mailboxes 24-27.
Input > Mailbox 28-31 Group > Mailbox ID > Mailbox 28 ID	Value must be decimal or HEX integer of 0x1FFFFFFF or less.	28	Select the receive ID for mailbox 28, between 0 and 0x7ff when using standard IDs, between 0 and 0x1FFFFFFF when using extended IDs. Value is not used when the mailbox is set as transmit type.
Input > Mailbox 28-31 Group > Mailbox ID > Mailbox 29 ID	Value must be decimal or HEX integer of 0x1FFFFFFF or less.	29	Select the receive ID for mailbox 29, between 0 and 0x7ff when using standard IDs, between 0 and 0x1FFFFFFF when using extended IDs. Value is not used when the mailbox is set as transmit type.
Input > Mailbox 28-31 Group > Mailbox ID >	Value must be decimal or HEX integer of	30	Select the receive ID for mailbox 30,

Mailbox 30 ID	0x1FFFFFFF or less.		between 0 and 0x7ff when using standard IDs, between 0 and 0x1FFFFFFF when using extended IDs. Value is not used when the mailbox is set as transmit type.
Input > Mailbox 28-31 Group > Mailbox ID > Mailbox 31 ID	Value must be decimal or HEX integer of 0x1FFFFFFF or less.	31	Select the receive ID for mailbox 31, between 0 and 0x7ff when using standard IDs, between 0 and 0x1FFFFFFF when using extended IDs. Value is not used when the mailbox is set as transmit type.
Input > Mailbox 28-31 Group > Mailbox Type > Mailbox 28 Type	<ul style="list-style-type: none"> <li>• Receive Mailbox</li> <li>• Transmit Mailbox</li> </ul>	Receive Mailbox	Select whether the mailbox is used for receive or transmit.
Input > Mailbox 28-31 Group > Mailbox Type > Mailbox 29 Type	<ul style="list-style-type: none"> <li>• Receive Mailbox</li> <li>• Transmit Mailbox</li> </ul>	Receive Mailbox	Select whether the mailbox is used for receive or transmit.
Input > Mailbox 28-31 Group > Mailbox Type > Mailbox 30 Type	<ul style="list-style-type: none"> <li>• Receive Mailbox</li> <li>• Transmit Mailbox</li> </ul>	Receive Mailbox	Select whether the mailbox is used for receive or transmit.
Input > Mailbox 28-31 Group > Mailbox Type > Mailbox 31 Type	<ul style="list-style-type: none"> <li>• Receive Mailbox</li> <li>• Transmit Mailbox</li> </ul>	Receive Mailbox	Select whether the mailbox is used for receive or transmit.
Input > Mailbox 28-31 Group > Mailbox Frame Type > Mailbox 28 Frame Type	<ul style="list-style-type: none"> <li>• Data Mailbox</li> <li>• Remote Mailbox</li> </ul>	Data Mailbox	Select whether the mailbox is used to capture data frames or remote frames (ignored for transmit mailboxes).
Input > Mailbox 28-31 Group > Mailbox Frame Type > Mailbox 29 Frame Type	<ul style="list-style-type: none"> <li>• Data Mailbox</li> <li>• Remote Mailbox</li> </ul>	Data Mailbox	Select whether the mailbox is used to capture data frames or remote frames (ignored for transmit mailboxes).
Input > Mailbox 28-31 Group > Mailbox Frame Type > Mailbox 30 Frame Type	<ul style="list-style-type: none"> <li>• Data Mailbox</li> <li>• Remote Mailbox</li> </ul>	Data Mailbox	Select whether the mailbox is used to capture data frames or remote frames (ignored for transmit mailboxes).
Input > Mailbox 28-31 Group > Mailbox Frame Type > Mailbox 31 Frame Type	<ul style="list-style-type: none"> <li>• Data Mailbox</li> <li>• Remote Mailbox</li> </ul>	Data Mailbox	Select whether the mailbox is used to capture data frames or remote frames (ignored for transmit mailboxes).

for transmit mailboxes).

Select whether the mailbox is used to capture data frames or remote frames (ignored for transmit mailboxes).

Select the Mask for mailboxes 28-31.

Input > Mailbox 28-31 Group > Mailbox Frame Type > Mailbox 31 Frame Type	• Data Mailbox • Remote Mailbox	Data Mailbox
--------------------------------------------------------------------------	------------------------------------	--------------

Input > Mailbox 28-31 Group > Mailbox 28-31 Group Mask	Value must be decimal or HEX integer of 0x1FFFFFFF or less.	0x1FFFFFFF
--------------------------------------------------------	-------------------------------------------------------------	------------

## Clock Configuration

The CAN peripheral uses the CANMCLK (main-clock oscillator) or PCLKB as its clock source (fCAN, CAN System Clock.) Using the PCLKB with the default of 60 MHz and the default CAN configuration will provide a CAN bit rate of 500 Kbit. To set the PCLKB frequency, use the **Clocks** tab of the RA Configuration editor. To change the clock frequency at run-time, use the CGC Interface. Refer to the CGC module guide for more information on configuring clocks.

- The user application must start the main-clock oscillator (CANMCLK or XTAL) at run-time using the CGC Interface if it has not already started (for example, if it is not used as the MCU clock source.)
- For RA6, RA4 and RA2 MCUs, the following clock restriction must be satisfied for the CAN HAL module when the clock source is the main-clock oscillator (CANMCLK):
  - $f_{PCLKB} \geq f_{CANCLK}$  ( $f_{CANCLK} = XTAL / \text{Baud Rate Prescaler}$ )
- For RA6 and RA4 MCUs, the source of the peripheral module clocks must be PLL for the CAN HAL module when the clock source is PCLKB.
- For RA4 MCUs, the clock frequency ratio of PCLKA and PCLKB must be 2:1 when using the CAN HAL module. Operation is not guaranteed for other settings.
- For RA2 MCUs, the clock frequency ratio of ICLK and PCLKB must be 2:1 when using the CAN HAL module. Operation is not guaranteed for other settings.

## Pin Configuration

The CAN peripheral module uses pins on the MCU to communicate to external devices. I/O pins must be selected and configured as required by the external device. A CAN channel would consist of two pins - CRX and CTX for data transmission/reception.

## Usage Notes

### Bit Rate Calculation

For convenience, the baudrate of the CAN peripheral is automatically set through the RA Configuration editor using a best effort approach. If the auto-generated baud settings cause deviation that is not tolerable by the application, the user can override the auto-generated settings and put in manually calculated values through RA Configuration editor. For more details on how the baudrate is set refer to section 37.4 "Data Transfer Rate Configuration" of the RA6M3 User's Manual (R01UH0886EJ0100).

## Examples

### Basic Example

This is a basic example of minimal use of the CAN in an application.

```
can_frame_t g_can_tx_frame;
can_frame_t g_can_rx_frame;
volatile bool g_rx_flag = false;
volatile bool g_tx_flag = false;
volatile bool g_err_flag = false;
volatile uint32_t g_rx_id;
void can_callback (can_callback_args_t * p_args)
{
    switch (p_args->event)
    {
    case CAN_EVENT_RX_COMPLETE: /* Receive complete event. */
        {
            g_rx_flag = true;
            g_rx_id = p_args->p_frame->id;
            /* Read received frame */
            memcpy(&g_can_rx_frame, p_args->p_frame, sizeof(can_frame_t));
        }
        break;
    case CAN_EVENT_TX_COMPLETE: /* Transmit complete event. */
        {
            g_tx_flag = true;
        }
        break;
    case CAN_EVENT_ERR_BUS_OFF: /* Bus error event. (bus off) */
    case CAN_EVENT_ERR_PASSIVE: /* Bus error event. (error passive) */
    case CAN_EVENT_ERR_WARNING: /* Bus error event. (error warning) */
    case CAN_EVENT_BUS_RECOVERY: /* Bus error event. (bus recovery) */
    case CAN_EVENT_MAILBOX_MESSAGE_LOST: /* Overwrite/overrun error */
        {
            /* Set error flag */
            g_err_flag = true;
        }
        break;
    }
}
```

```
default:
    {
break;
    }
}
}
void basic_example (void)
{
    fsp_err_t err;
    uint32_t i;
    uint32_t timeout_ms = CAN_BUSY_DELAY;
    /* Initialize the CAN module */
    err = R_CAN_Open(&g_can0_ctrl, &g_can0_cfg);
    /* Handle any errors. This function should be defined by the user. */
    handle_error(err);
    g_can_tx_frame.id = CAN_DESTINATION_DEVICE_MAILBOX_NUMBER; /* CAN
Destination Device ID */
    g_can_tx_frame.type = CAN_FRAME_TYPE_DATA;
    g_can_tx_frame.data_length_code = CAN_FRAME_TRANSMIT_DATA_BYTES;
    /* Write some data to the transmit frame */
    for (i = 0; i < sizeof(g_can_tx_frame.data); i++)
    {
        g_can_tx_frame.data[i] = (uint8_t) i;
    }
    /* Send data on the bus */
    g_tx_flag = false;
    g_err_flag = false;
    err = R_CAN_Write(&g_can0_ctrl, CAN_MAILBOX_NUMBER_31, &g_can_tx_frame);
    handle_error(err);
    /* Since there is nothing else to do, block until Callback triggers*/
    while ((true != g_tx_flag) && timeout_ms)
    {
R_BSP_SoftwareDelay(1U, BSP_DELAY_UNITS_MILLISECONDS);
        timeout_ms--;
    }
}
```



```
    }  
    if (true == g_err_flag)  
    {  
        __BKPT(0);  
    }  
}
```

## External Loop-back Test

This example requires a 120 Ohm resistor connected across channel 0 CAN pins. The mailbox numbers are arbitrarily chosen.

```
void can_external_loopback_example (void)  
{  
    fsp_err_t          err;  
    uint32_t          timeout_ms    = CAN_BUSY_DELAY;  
    can_operation_mode_t operation_mode = CAN_OPERATION_MODE_NORMAL;  
    can_test_mode_t   test_mode     = CAN_TEST_MODE_LOOPBACK_EXTERNAL;  
    int               diff = 0;  
    uint32_t i          = 0;  
    err = R_CAN_Open(&g_can0_ctrl, &g_can0_cfg);  
    /* Handle any errors. This function should be defined by the user. */  
    handle_error(err);  
    err = R_CAN_ModeTransition(&g_can0_ctrl, operation_mode, test_mode);  
    handle_error(err);  
    /* Clear the data part of receive frame */  
    memset(g_can_rx_frame.data, 0, CAN_FRAME_TRANSMIT_DATA_BYTES);  
    /* CAN Destination Device ID, in this case it is the same device with another  
mailbox */  
    g_can_tx_frame.id          = CAN_MAILBOX_NUMBER_4;  
    g_can_tx_frame.type        = CAN_FRAME_TYPE_DATA;  
    g_can_tx_frame.data_length_code = CAN_FRAME_TRANSMIT_DATA_BYTES;  
    /* Write some data to the transmit frame */  
    for (i = 0; i < sizeof(g_can_tx_frame.data); i++)  
    {
```

```
        g_can_tx_frame.data[i] = (uint8_t) i;
    }

    /* Send data on the bus */
    g_rx_flag = false;
    g_err_flag = false;
    err = R_CAN_Write(&g_can0_ctrl, CAN_MAILBOX_NUMBER_31, &g_can_tx_frame);
    handle_error(err);

    /* Since there is nothing else to do, block until Callback triggers*/
    while ((true != g_rx_flag) && timeout_ms)
    {
        R_BSP_SoftwareDelay(1U, BSP_DELAY_UNITS_MILLISECONDS);
        timeout_ms--;
    }
    if (true == g_err_flag)
    {
        __BKPT(0);
    }

    /* Verify received data */
    diff = memcmp(&g_can_rx_frame.data[0], &g_can_tx_frame.data[0],
CAN_FRAME_TRANSMIT_DATA_BYTES);
    if (0 != diff)
    {
        __BKPT(0);
    }
}
```

## Function Documentation

---

◆ **R\_CAN\_Open()**

```
fsp_err_t R_CAN_Open ( can_ctrl_t *const p_api_ctrl, can_cfg_t const *const p_cfg )
```

Open and configure the CAN channel for operation.

Example:

```
/* Initialize the CAN module */
err = R_CAN_Open(&g_can0_ctrl, &g_can0_cfg);
```

**Return values**

FSP_SUCCESS	Channel opened successfully
FSP_ERR_ALREADY_OPEN	Driver already open.
FSP_ERR_CAN_INIT_FAILED	Channel failed to initialize.
FSP_ERR_ASSERTION	Null pointer presented.

◆ **R\_CAN\_Close()**

```
fsp_err_t R_CAN_Close ( can_ctrl_t *const p_api_ctrl)
```

Close the CAN channel.

**Return values**

FSP_SUCCESS	Channel closed successfully.
FSP_ERR_NOT_OPEN	Control block not open.
FSP_ERR_ASSERTION	Null pointer presented.

◆ **R\_CAN\_Write()**

```
fsp_err_t R_CAN_Write ( can_ctrl_t *const p_api_ctrl, uint32_t mailbox, can_frame_t *const p_frame )
```

Write data to the CAN channel. Write up to eight bytes to the channel mailbox.

Example:

```
err = R_CAN_Write(&g_can0_ctrl, CAN_MAILBOX_NUMBER_31, &g_can_tx_frame);
handle_error(err);
```

**Return values**

FSP_SUCCESS	Operation succeeded.
FSP_ERR_NOT_OPEN	Control block not open.
FSP_ERR_CAN_TRANSMIT_NOT_READY	Transmit in progress, cannot write data at this time.
FSP_ERR_CAN_RECEIVE_MAILBOX	Mailbox is setup for receive and cannot send.
FSP_ERR_INVALID_ARGUMENT	Data length or frame type invalid.
FSP_ERR_ASSERTION	Null pointer presented

◆ **R\_CAN\_ModeTransition()**

```
fsp_err_t R_CAN_ModeTransition ( can_ctrl_t *const p_api_ctrl, can_operation_mode_t operation_mode, can_test_mode_t test_mode )
```

CAN Mode Transition is used to change CAN driver state.

Example:

```
err = R_CAN_ModeTransition(&g_can0_ctrl, operation_mode, test_mode);
handle_error(err);
```

**Return values**

FSP_SUCCESS	Operation succeeded.
FSP_ERR_NOT_OPEN	Control block not open.
FSP_ERR_ASSERTION	Null pointer presented

◆ **R\_CAN\_InfoGet()**

```
fsp_err_t R_CAN_InfoGet ( can_ctrl_t *const p_api_ctrl, can_info_t *const p_info )
```

Get CAN state and status information for the channel.

**Return values**

FSP_SUCCESS	Operation succeeded.
FSP_ERR_NOT_OPEN	Control block not open.
FSP_ERR_ASSERTION	Null pointer presented

◆ **R\_CAN\_CallbackSet()**

```
fsp_err_t R_CAN_CallbackSet ( can_ctrl_t *const p_api_ctrl, void(*) (can_callback_args_t *)
p_callback, void const *const p_context, can_callback_args_t *const p_callback_memory )
```

Updates the user callback with the option to provide memory for the callback argument structure. Implements `can_api_t::callbackSet`.

**Return values**

FSP_SUCCESS	Callback updated successfully.
FSP_ERR_ASSERTION	A required pointer is NULL.
FSP_ERR_NOT_OPEN	The control block has not been opened.
FSP_ERR_NO_CALLBACK_MEMORY	p_callback is non-secure and p_callback_memory is either secure or NULL.

◆ **R\_CAN\_VersionGet()**

```
fsp_err_t R_CAN_VersionGet ( fsp_version_t *const p_version)
```

Get CAN module code and API versions.

**Return values**

FSP_SUCCESS	Operation succeeded.
FSP_ERR_ASSERTION	Null pointer presented note This function is reentrant.

**4.2.8 Clock Generation Circuit (r\_cgc)**

## Modules

### Functions

fsp_err_t	R_CGC_Open (cgc_ctrl_t *const p_ctrl, cgc_cfg_t const *const p_cfg)
fsp_err_t	R_CGC_ClocksCfg (cgc_ctrl_t *const p_ctrl, cgc_clocks_cfg_t const *const p_clock_cfg)
fsp_err_t	R_CGC_ClockStart (cgc_ctrl_t *const p_ctrl, cgc_clock_t clock_source, cgc_pll_cfg_t const *const p_pll_cfg)
fsp_err_t	R_CGC_ClockStop (cgc_ctrl_t *const p_ctrl, cgc_clock_t clock_source)
fsp_err_t	R_CGC_ClockCheck (cgc_ctrl_t *const p_ctrl, cgc_clock_t clock_source)
fsp_err_t	R_CGC_SystemClockSet (cgc_ctrl_t *const p_ctrl, cgc_clock_t clock_source, cgc_divider_cfg_t const *const p_divider_cfg)
fsp_err_t	R_CGC_SystemClockGet (cgc_ctrl_t *const p_ctrl, cgc_clock_t *const p_clock_source, cgc_divider_cfg_t *const p_divider_cfg)
fsp_err_t	R_CGC_OscStopDetectEnable (cgc_ctrl_t *const p_ctrl)
fsp_err_t	R_CGC_OscStopDetectDisable (cgc_ctrl_t *const p_ctrl)
fsp_err_t	R_CGC_OscStopStatusClear (cgc_ctrl_t *const p_ctrl)
fsp_err_t	R_CGC_CallbackSet (cgc_ctrl_t *const p_api_ctrl, void(*p_callback)(cgc_callback_args_t *), void const *const p_context, cgc_callback_args_t *const p_callback_memory)
fsp_err_t	R_CGC_Close (cgc_ctrl_t *const p_ctrl)
fsp_err_t	R_CGC_VersionGet (fsp_version_t *version)

### Detailed Description

Driver for the CGC peripheral on RA MCUs. This module implements the [CGC Interface](#).

#### Note

*This module is not required for the initial clock configuration. Initial clock settings are configurable on the **Clocks** tab of the RA Configuration editor. The initial clock settings are applied by the BSP during the startup process before main.*

## Overview

### Features

The CGC module supports runtime modifications of clock settings. Key features include the following:

- Supports changing the system clock source to any of the following options (provided they are supported on the MCU):
  - High-speed on-chip oscillator (HOCO)
  - Middle-speed on-chip oscillator (MOCO)
  - Low-speed on-chip oscillator (LOCO)
  - Main oscillator (external resonator or external clock input frequency)
  - Sub-clock oscillator (external resonator)
  - PLL/PLL2 (not available on all MCUs)
- When the system core clock frequency changes, the following things are updated:
  - The CMSIS standard global variable `SystemCoreClock` is updated to reflect the new clock frequency.
  - Wait states for ROM and RAM are adjusted to the minimum supported value for the new clock frequency.
  - The operating power control mode is updated to the minimum supported value for the new clock settings.
- Supports starting or stopping any of the system clock sources
- Supports changing dividers for the internal clocks
- Supports the oscillation stop detection feature

## Internal Clocks

The RA microcontrollers have up to seven internal clocks. Not all internal clocks exist on all MCUs. Each clock domain has its own divider that can be updated in `R_CGC_SystemClockSet()`. The dividers are subject to constraints described in the footnote of the table "Specifications of the Clock Generation Circuit for the internal clocks" in the hardware manual.

The internal clocks include:

- System clock (ICLK): core clock used for CPU, flash, internal SRAM, DTC, and DMAC
- PCLKA/PCLKB/PCLKC/PCLKD: Peripheral clocks, refer to the table "Specifications of the Clock Generation Circuit for the internal clocks" in the hardware manual to see which peripherals are controlled by which clocks.
- FCLK: Clock source for reading data flash and for programming/erasure of both code and data flash.
- BCLK: External bus clock

## Configuration

### Note

*The initial clock settings are configurable on the **Clocks** tab of the RA Configuration editor.*

*There is a configuration to enable the HOCO on reset in the OFS1 settings on the BSP tab.*

*The following clock related settings are configurable in the RA Common section on the BSP tab:*

- *Main Oscillator Wait Time*
- *Main Oscillator Clock Source (external oscillator or crystal/resonator)*
- *Subclock Populated*
- *Subclock Drive*
- *Subclock Stabilization Time (ms)*

*The default stabilization times are determined based on development boards provided by Renesas, but are generally valid for most designs. Depending on the target board hardware configuration and requirements these values may need to be adjusted for reliability or startup speed.*

## Build Time Configurations for r\_cgc

The following build time configurations are defined in fsp\_cfg/r\_cgc\_cfg.h:

Configuration	Options	Default	Description
Parameter Checking	<ul style="list-style-type: none"> <li>• Default (BSP)</li> <li>• Enabled</li> <li>• Disabled</li> </ul>	Default (BSP)	If selected code for parameter checking is included in the build.

### Configurations for Driver > System > CGC Driver on r\_cgc

This module can be added to the Stacks tab via New Stack > Driver > System > CGC Driver on r\_cgc. Non-secure callable guard functions can be generated for this module by right clicking the module in the RA Configuration tool and checking the "Non-secure Callable" box.

Configuration	Options	Default	Description
Name	Name must be a valid C symbol	g_cgc0	Module name.
NMI Callback	Name must be a valid C symbol	NULL	A user callback function must be provided if oscillation stop detection is used. If this callback function is provided, it is called from the NMI handler if the main oscillator stops.

### Clock Configuration

This module is used to configure the system clocks. There are no module specific clock configurations required to use it.

### Pin Configuration

The CGC module controls the output of the CLOCKOUT signal.

If an external oscillator is used the XTAL and EXTAL pins must be configured accordingly. When running from an on chip oscillator there is no requirement for the main clock external oscillator. In this case, the XTAL and EXTAL pins can be set to a different function in the RA Configuration editor.

The functionality of the subclock external oscillator pins XCIN and XCOU is fixed.

## Usage Notes

### NMI Interrupt

The CGC timer uses the NMI for oscillation stop detection of the main oscillator after R\_CGC\_OscStopDetectEnable is called. The NMI is enabled by default. No special configuration is required. When the NMI is triggered, the callback function registered during R\_CGC\_Open() is called.

### Starting or Stopping the Subclock

If the Subclock Populated property is set to Populated on the BSP configuration tab, then the



subclock is started in the BSP startup routine. Otherwise, it is stopped in the BSP startup routine. Starting and stopping the subclock at runtime is not recommended since the stabilization requirements typically negate the negligible power savings.

The application is responsible for ensuring required clocks are started and stable before accessing MCU peripheral registers.

#### Warning

The subclock can take up to several seconds to stabilize. RA startup code does not wait for subclock stabilization unless the subclock is the main clock source. In this case the default wait time is 1000ms (1 second). When running AGT or RTC off the subclock, the application must ensure the subclock is stable before starting operation. Because there is no hardware stabilization status bit for the subclock R\_CGC\_ClockCheck cannot be used to optimize this wait.

Changing the subclock state during [R\\_CGC\\_ClocksCfg\(\)](#) is not supported.

### Low Power Operation

If "Use Low Voltage Mode" is enabled in the BSP MCU specific properties (not available on all MCUs), the MCU is always in low voltage mode and no other power modes are considered. The following conditions must be met for the MCU to run in low voltage mode:

- Requires HOCO to be running, so HOCO cannot be stopped in low voltage mode
- Requires PLL to be stopped, so PLL APIs are not available in low voltage mode
- Requires ICLK  $\leq$  4 MHz
- If oscillation stop detection is used, dividers of 1 or 2 cannot be used for any clock

If "Use Low Voltage Mode" is not enabled, the MCU applies the lowest power mode by searching through the following list in order and applying the first power mode that is supported under the current conditions:

- Subosc-speed mode (lowest power)
  - Requires system clock to be LOCO or subclock
  - Requires MOCO, HOCO, main oscillator, and PLL (if present) to be stopped
  - Requires ICLK and FCLK dividers to be 1
- Low-speed mode
  - Requires PLL to be stopped
  - Requires ICLK  $\leq$  1 MHz
  - If oscillation stop detection is used, dividers of 1, 2, 4, or 8 cannot be used for any clock
- Middle-speed mode (not supported on all MCUs)
  - Requires ICLK  $\leq$  8 MHz
- High-speed mode
  - Default mode if no other operating mode is supported

Refer to the section "Function for Lower Operating Power Consumption" in the "Low Power Modes" chapter of the hardware manual for MCU specific information about operating power control modes.

When low voltage mode is not used, the following functions adjust the operating power control mode to ensure it remains within the hardware specification and to ensure the MCU is running at the optimal operating power control mode:

- [R\\_CGC\\_ClockStart\(\)](#)
- [R\\_CGC\\_ClockStop\(\)](#)

- [R\\_CGC\\_SystemClockSet\(\)](#)
- [R\\_CGC\\_OscStopDetectEnable\(\)](#)
- [R\\_CGC\\_OscStopDetectDisable\(\)](#)

#### Note

FSP APIs, including these APIs, are not thread safe. These APIs and any other user code that modifies the operating power control mode must not be allowed to interrupt each other. Proper care must be taken during application design if these APIs are used in threads or interrupts to ensure this constraint is met.

No action is required by the user of these APIs. This section is provided for informational purposes only.

## Examples

### Basic Example

This is a basic example of minimal use of the CGC in an application.

```
void cgc_basic_example (void)
{
    fsp_err_t err = FSP_SUCCESS;

    /* Initializes the CGC module. */
    err = R_CGC_Open(&g_cgc0_ctrl, &g_cgc0_cfg);

    /* Handle any errors. This function should be defined by the user. */
    handle_error(err);

    /* Change the system clock to LOCO for power saving. */
    /* Start the LOCO. */
    err = R_CGC_ClockStart(&g_cgc0_ctrl, CGC_CLOCK_LOCO, NULL);
    handle_error(err);

    /* Wait for the LOCO stabilization wait time.
     *
     * NOTE: The MOCO, LOCO and subclock do not have stabilization status bits, so any
    stabilization time must be
     * performed via a software wait when starting these oscillators. For all other
    oscillators, R_CGC_ClockCheck can
     * be used to verify stabilization status.
     */
    R_BSP_SoftwareDelay(BSP_FEATURE_CGC_LOCO_STABILIZATION_MAX_US,
    BSP_DELAY_UNITS_MICROSECONDS);

    /* Set divisors. Divisors for clocks that don't exist on the MCU are ignored. */
    cgc_divider_cfg_t dividers =
```

```
{
/* PCLKB is not used in this application, so select the maximum divisor for lowest
power. */
    .pclkb_div = CGC_SYS_CLOCK_DIV_64,
/* PCLKD is not used in this application, so select the maximum divisor for lowest
power. */
    .pclkd_div = CGC_SYS_CLOCK_DIV_64,
/* ICLK is the MCU clock, allow it to run as fast as the LOCO is capable. */
    .iclk_div = CGC_SYS_CLOCK_DIV_1,
/* These clocks do not exist on some devices. If any clocks don't exist, set the
divider to 1. */
    .pclka_div = CGC_SYS_CLOCK_DIV_1,
    .pclkc_div = CGC_SYS_CLOCK_DIV_1,
    .fclk_div = CGC_SYS_CLOCK_DIV_1,
    .bclk_div = CGC_SYS_CLOCK_DIV_1,
};
/* Switch the system clock to LOCO. */
err = R_CGC_SystemClockSet(&g_cgc0_ctrl, CGC_CLOCK_LOCO, &dividers);
handle_error(err);
}
```

## Configuring Multiple Clocks

This example demonstrates switching to a new source clock and stopping the previous source clock in a single function call using [R\\_CGC\\_ClocksCfg\(\)](#).

```
void cgc_clocks_cfg_example (void)
{
    fsp_err_t err = FSP_SUCCESS;
/* Initializes the CGC module. */
    err = R_CGC_Open(&g_cgc0_ctrl, &g_cgc0_cfg);
/* Handle any errors. This function should be defined by the user. */
    handle_error(err);
/* Change the system clock to PLL running from the main oscillator. */
/* Assuming the system clock is MOCO, switch to HOCO. */
```

```
cgc_clocks_cfg_t clocks_cfg;

clocks_cfg.system_clock      = CGC_CLOCK_PLL;
clocks_cfg.pll_state        = CGC_CLOCK_CHANGE_NONE;
clocks_cfg.pll_cfg.source_clock = CGC_CLOCK_MAIN_OSC; // unused
clocks_cfg.pll_cfg.multiplier = CGC_PLL_MUL_10_0;    // unused
clocks_cfg.pll_cfg.divider   = CGC_PLL_DIV_2;       // unused
clocks_cfg.divider_cfg.iclk_div = CGC_SYS_CLOCK_DIV_1;
clocks_cfg.divider_cfg.pclka_div = CGC_SYS_CLOCK_DIV_4;
clocks_cfg.divider_cfg.pclkb_div = CGC_SYS_CLOCK_DIV_4;
clocks_cfg.divider_cfg.pclkc_div = CGC_SYS_CLOCK_DIV_4;
clocks_cfg.divider_cfg.pclkd_div = CGC_SYS_CLOCK_DIV_4;
clocks_cfg.divider_cfg.bclk_div = CGC_SYS_CLOCK_DIV_4;
clocks_cfg.divider_cfg.fclk_div = CGC_SYS_CLOCK_DIV_4;
clocks_cfg.mainosc_state     = CGC_CLOCK_CHANGE_NONE;
clocks_cfg.hoco_state        = CGC_CLOCK_CHANGE_START;
clocks_cfg.moco_state        = CGC_CLOCK_CHANGE_STOP;
clocks_cfg.loco_state        = CGC_CLOCK_CHANGE_NONE;
err = R_CGC_ClocksCfg(&g_cgc0_ctrl, &clocks_cfg);
handle_error(err);

#if BSP_FEATURE_CGC_HAS_PLL
/* Assuming the system clock is HOCO, switch to PLL running from main oscillator and
stop MOCO. */
clocks_cfg.system_clock      = CGC_CLOCK_PLL;
clocks_cfg.pll_state        = CGC_CLOCK_CHANGE_START;
clocks_cfg.pll_cfg.source_clock = CGC_CLOCK_MAIN_OSC;
clocks_cfg.pll_cfg.multiplier = (cgc_pll_mul_t) BSP_CFG_PLL_MUL;
clocks_cfg.pll_cfg.divider   = (cgc_pll_div_t) BSP_CFG_PLL_DIV;
clocks_cfg.divider_cfg.iclk_div = CGC_SYS_CLOCK_DIV_1;
clocks_cfg.divider_cfg.pclka_div = CGC_SYS_CLOCK_DIV_4;
clocks_cfg.divider_cfg.pclkb_div = CGC_SYS_CLOCK_DIV_4;
clocks_cfg.divider_cfg.pclkc_div = CGC_SYS_CLOCK_DIV_4;
clocks_cfg.divider_cfg.pclkd_div = CGC_SYS_CLOCK_DIV_4;
clocks_cfg.divider_cfg.bclk_div = CGC_SYS_CLOCK_DIV_4;
clocks_cfg.divider_cfg.fclk_div = CGC_SYS_CLOCK_DIV_4;
```

```
clocks_cfg.mainosc_state      = CGC_CLOCK_CHANGE_START;
clocks_cfg.hoco_state         = CGC_CLOCK_CHANGE_STOP;
clocks_cfg.moco_state         = CGC_CLOCK_CHANGE_NONE;
clocks_cfg.loco_state         = CGC_CLOCK_CHANGE_NONE;
err = R_CGC_ClocksCfg(&g_cgc0_ctrl, &clocks_cfg);
handle_error(err);
#endif
}
```

## Oscillation Stop Detection

This example demonstrates registering a callback for oscillation stop detection of the main oscillator.

```
/* Example callback called when oscillation stop is detected. */
void oscillation_stop_callback (cgc_callback_args_t * p_args)
{
    FSP_PARAMETER_NOT_USED(p_args);
    fsp_err_t err = FSP_SUCCESS;

    /* (Optional) If the MCU was running on the main oscillator, the MCU is now running
    on MOCO. Switch clocks if
    * desired. This example shows switching to HOCO. */
    err = R_CGC_ClockStart(&g_cgc0_ctrl, CGC_CLOCK_HOCO, NULL);
    handle_error(err);

    do
    {
        /* Wait for HOCO to stabilize. */
        err = R_CGC_ClockCheck(&g_cgc0_ctrl, CGC_CLOCK_HOCO);
    } while (FSP_SUCCESS != err);

    cgc_divider_cfg_t dividers =
    {
        .pclkb_div = CGC_SYS_CLOCK_DIV_4,
        .pclkd_div = CGC_SYS_CLOCK_DIV_4,
        .iclk_div = CGC_SYS_CLOCK_DIV_1,
        .pclka_div = CGC_SYS_CLOCK_DIV_4,
        .pclkc_div = CGC_SYS_CLOCK_DIV_4,
    }
}
```

```
.fclk_div = CGC_SYS_CLOCK_DIV_4,
.bclk_div = CGC_SYS_CLOCK_DIV_4,
};
err = R_CGC_SystemClockSet(&g_cgc0_ctrl, CGC_CLOCK_HOCO, &dividers);
handle_error(err);
#if BSP_FEATURE_CGC_HAS_PLL
/* (Optional) If the MCU was running on the PLL, the PLL is now in free-running
mode. Switch clocks if
* desired. This example shows switching to the PLL running on HOCO. */
err = R_CGC_ClockStart(&g_cgc0_ctrl, CGC_CLOCK_HOCO, NULL);
handle_error(err);
do
{
/* Wait for HOCO to stabilize. */
err = R_CGC_ClockCheck(&g_cgc0_ctrl, CGC_CLOCK_HOCO);
} while (FSP_SUCCESS != err);
cgc_pll_cfg_t pll_cfg =
{
.source_clock = CGC_CLOCK_HOCO,
.multiplier   = (cgc_pll_mul_t) BSP_CFG_PLL_MUL,
.divider      = (cgc_pll_div_t) BSP_CFG_PLL_DIV,
};
err = R_CGC_ClockStart(&g_cgc0_ctrl, CGC_CLOCK_PLL, &pll_cfg);
handle_error(err);
do
{
/* Wait for PLL to stabilize. */
err = R_CGC_ClockCheck(&g_cgc0_ctrl, CGC_CLOCK_PLL);
} while (FSP_SUCCESS != err);
cgc_divider_cfg_t pll_dividers =
{
.pclkb_div = CGC_SYS_CLOCK_DIV_4,
.pclkd_div = CGC_SYS_CLOCK_DIV_4,
.iclk_div  = CGC_SYS_CLOCK_DIV_1,
```

```
.pclka_div = CGC_SYS_CLOCK_DIV_4,
.pclkc_div = CGC_SYS_CLOCK_DIV_4,
.fclk_div = CGC_SYS_CLOCK_DIV_4,
.bclk_div = CGC_SYS_CLOCK_DIV_4,
};
err = R_CGC_SystemClockSet(&g_cgc0_ctrl, CGC_CLOCK_PLL, &pll_dividers);
handle_error(err);
#endif
/* (Optional) Clear the error flag. Only clear this flag after switching the MCU
clock source away from the main
* oscillator and if the main oscillator is stable again. */
err = R_CGC_OscStopStatusClear(&g_cgc0_ctrl);
handle_error(err);
}
void cgc_osc_stop_example (void)
{
fsp_err_t err = FSP_SUCCESS;
/* Open the module. */
err = R_CGC_Open(&g_cgc0_ctrl, &g_cgc0_cfg);
/* Handle any errors. This function should be defined by the user. */
handle_error(err);
/* Enable oscillation stop detection. The main oscillator must be running at this
point. */
err = R_CGC_OscStopDetectEnable(&g_cgc0_ctrl);
handle_error(err);
/* (Optional) Oscillation stop detection must be disabled before entering any low
power mode. */
err = R_CGC_OscStopDetectDisable(&g_cgc0_ctrl);
handle_error(err);
__WFI();
/* (Optional) Reenable oscillation stop detection after waking from low power mode.
*/
err = R_CGC_OscStopDetectEnable(&g_cgc0_ctrl);
handle_error(err);
```

}

## Data Structures

struct [cgc\\_instance\\_ctrl\\_t](#)

## Data Structure Documentation

### ◆ [cgc\\_instance\\_ctrl\\_t](#)

struct [cgc\\_instance\\_ctrl\\_t](#)CGC private control block. DO NOT MODIFY. Initialization occurs when [R\\_CGC\\_Open\(\)](#) is called.

#### Data Fields

void const \* [p\\_context](#)

## Field Documentation

### ◆ [p\\_context](#)

void const\* [cgc\\_instance\\_ctrl\\_t::p\\_context](#)Placeholder for user data. Passed to the user callback in [cgc\\_callback\\_args\\_t](#).

## Function Documentation

### ◆ [R\\_CGC\\_Open\(\)](#)

[fsp\\_err\\_t](#) [R\\_CGC\\_Open](#) ( [cgc\\_ctrl\\_t](#)\*const *p\_ctrl*, [cgc\\_cfg\\_t](#) const \*const *p\_cfg* )Initialize the CGC API. Implements [cgc\\_api\\_t::open](#).

Example:

```
/* Initializes the CGC module. */
err = R_CGC_Open(&g_cgc0_ctrl, &g_cgc0_cfg);
```

#### Return values

FSP_SUCCESS	CGC successfully initialized.
FSP_ERR_ASSERTION	Invalid input argument.
FSP_ERR_ALREADY_OPEN	Module is already open.



## ◆ R\_CGC\_ClocksCfg()

```
fsp_err_t R_CGC_ClocksCfg ( cgc_ctrl_t *const p_ctrl, cgc_clocks_cfg_t const *const p_clock_cfg )
```

Reconfigures all main system clocks. This API can be used for any of the following purposes:

- start or stop clocks
- change the system clock source
- configure the PLL/PLL2 multiplication and division ratios when starting the PLL
- change the system dividers

If the requested system clock source has a stabilization flag, this function blocks waiting for the stabilization flag of the requested system clock source to be set. If the requested system clock source was just started and it has no stabilization flag, this function blocks for the stabilization time required by the requested system clock source according to the Electrical Characteristics section of the hardware manual. If the requested system clock source has no stabilization flag and it is already running, it is assumed to be stable and this function will not block. If the requested system clock is the subclock, the subclock must be stable prior to calling this function.

The internal dividers (`cgc_clocks_cfg_t::divider_cfg`) are subject to constraints described in footnotes of the hardware manual table detailing specifications for the clock generation circuit for the internal clocks for the MCU. For example:

- RA6M3: see footnotes of Table 9.2 "Specifications of the clock generation circuit for the internal clocks" in the RA6M3 manual R01UH0886EJ0100
- RA2A1: see footnotes of Table 9.2 "Clock generation circuit specifications for the internal clocks" in the RA2A1 manual R01UH0888EJ0100

Do not attempt to stop the requested clock source or the source of a PLL if the PLL will be running after this operation completes.

Implements `cgc_api_t::clocksCfg`.

Example:

```
/* Assuming the system clock is MOCO, switch to HOCO. */
cgc_clocks_cfg_t clocks_cfg;

clocks_cfg.system_clock          = CGC_CLOCK_PLL;

clocks_cfg.pll_state             = CGC_CLOCK_CHANGE_NONE;

clocks_cfg.pll_cfg.source_clock = CGC_CLOCK_MAIN_OSC; // unused

clocks_cfg.pll_cfg.multiplier   = CGC_PLL_MUL_10_0;   // unused

clocks_cfg.pll_cfg.divider      = CGC_PLL_DIV_2;      // unused

clocks_cfg.divider_cfg.iclk_div = CGC_SYS_CLOCK_DIV_1;

clocks_cfg.divider_cfg.pclka_div = CGC_SYS_CLOCK_DIV_4;

clocks_cfg.divider_cfg.pclkb_div = CGC_SYS_CLOCK_DIV_4;

clocks_cfg.divider_cfg.pclkc_div = CGC_SYS_CLOCK_DIV_4;

clocks_cfg.divider_cfg.pclkd_div = CGC_SYS_CLOCK_DIV_4;

clocks_cfg.divider_cfg.bclk_div = CGC_SYS_CLOCK_DIV_4;
```

```

clocks_cfg.divider_cfg.fclk_div = CGC_SYS_CLOCK_DIV_4;
clocks_cfg.mainosc_state         = CGC_CLOCK_CHANGE_NONE;
clocks_cfg.hoco_state           = CGC_CLOCK_CHANGE_START;
clocks_cfg.moco_state           = CGC_CLOCK_CHANGE_STOP;
clocks_cfg.loco_state           = CGC_CLOCK_CHANGE_NONE;
err = R_CGC_ClocksCfg(&g_cgc0_ctrl, &clocks_cfg);
handle_error(err);

```

**Return values**

FSP_SUCCESS	Clock configuration applied successfully.
FSP_ERR_ASSERTION	Invalid input argument.
FSP_ERR_UNSUPPORTED	PLL/PLL2 is not available on this MCU.
FSP_ERR_NOT_OPEN	Module is not open.
FSP_ERR_IN_USE	Attempt to stop the current system clock or the PLL source clock.
FSP_ERR_CLOCK_ACTIVE	PLL configuration cannot be changed while PLL is running.
FSP_ERR_OSC_STOP_DET_ENABLED	PLL multiplier must be less than 20 if oscillation stop detect is enabled and the input frequency is less than 12.5 MHz.
FSP_ERR_NOT_STABILIZED	PLL clock source is not stable.
FSP_ERR_PLL_SRC_INACTIVE	PLL clock source is not running.

◆ **R\_CGC\_ClockStart()**

```
fsp_err_t R_CGC_ClockStart ( cgc_ctrl_t *const p_ctrl, cgc_clock_t clock_source, cgc_pll_cfg_t const
*const p_pll_cfg )
```

Start the specified clock if it is not currently active. The PLL configuration cannot be changed while the PLL is running. Implements `cgc_api_t::clockStart`.

The PLL source clock must be operating and stable prior to starting the PLL.

Example:

```
/* Start the LOCO. */
err = R_CGC_ClockStart(&g_cgc0_ctrl, CGC_CLOCK_LOCO, NULL);
handle_error(err);
```

**Return values**

FSP_SUCCESS	Clock initialized successfully.
FSP_ERR_ASSERTION	Invalid input argument.
FSP_ERR_NOT_OPEN	Module is not open.
FSP_ERR_NOT_STABILIZED	The clock source is not stabilized after being turned off or PLL clock source is not stable.
FSP_ERR_PLL_SRC_INACTIVE	PLL clock source is not running.
FSP_ERR_CLOCK_ACTIVE	PLL configuration cannot be changed while PLL is running.
FSP_ERR_OSC_STOP_DET_ENABLED	PLL multiplier must be less than 20 if oscillation stop detect is enabled and the input frequency is less than 12.5 MHz.

◆ **R\_CGC\_ClockStop()**

```
fsp_err_t R_CGC_ClockStop ( cgc_ctrl_t *const p_ctrl, cgc_clock_t clock_source )
```

Stop the specified clock if it is active. Implements `cgc_api_t::clockStop`.

Do not attempt to stop the current system clock source. Do not attempt to stop the source clock of a PLL if the PLL is running.

**Return values**

FSP_SUCCESS	Clock stopped successfully.
FSP_ERR_ASSERTION	Invalid input argument.
FSP_ERR_NOT_OPEN	Module is not open.
FSP_ERR_IN_USE	Attempt to stop the current system clock or the PLL source clock.
FSP_ERR_OSC_STOP_DET_ENABLED	Attempt to stop MOCO when Oscillation stop is enabled.
FSP_ERR_NOT_STABILIZED	Clock not stabilized after starting.

◆ **R\_CGC\_ClockCheck()**

```
fsp_err_t R_CGC_ClockCheck ( cgc_ctrl_t *const p_ctrl, cgc_clock_t clock_source )
```

Check the specified clock for stability. Implements `cgc_api_t::clockCheck`.

**Return values**

FSP_SUCCESS	Clock is running and stable.
FSP_ERR_ASSERTION	Invalid input argument.
FSP_ERR_NOT_OPEN	Module is not open.
FSP_ERR_NOT_STABILIZED	Clock not stabilized.
FSP_ERR_CLOCK_INACTIVE	Clock not turned on.

## ◆ R\_CGC\_SystemClockSet()

```
fsp_err_t R_CGC_SystemClockSet ( cgc_ctrl_t *const p_ctrl, cgc_clock_t clock_source,
cgc_divider_cfg_t const *const p_divider_cfg )
```

Set the specified clock as the system clock and configure the internal dividers for ICLK, PCLKA, PCLKB, PCLKC, PCLKD, BCLK, and FCLK. Implements `cgc_api_t::systemClockSet`.

The requested clock source must be running and stable prior to calling this function. The internal dividers are subject to constraints described in the hardware manual table "Specifications of the Clock Generation Circuit for the internal clocks".

The internal dividers (`p_divider_cfg`) are subject to constraints described in footnotes of the hardware manual table detailing specifications for the clock generation circuit for the internal clocks for the MCU. For example:

- RA6M3: see footnotes of Table 9.2 "Specifications of the clock generation circuit for the internal clocks" in the RA6M3 manual R01UH0886EJ0100
- RA2A1: see footnotes of Table 9.2 "Clock generation circuit specifications for the internal clocks" in the RA2A1 manual R01UH0888EJ0100

This function also updates the RAM and ROM wait states, the operating power control mode, and the SystemCoreClock CMSIS global variable.

Example:

```
/* Set divisors. Divisors for clocks that don't exist on the MCU are ignored. */
cgc_divider_cfg_t dividers =
{
/* PCLKB is not used in this application, so select the maximum divisor for lowest
power. */
.pclkb_div = CGC_SYS_CLOCK_DIV_64,
/* PCLKD is not used in this application, so select the maximum divisor for lowest
power. */
.pclkd_div = CGC_SYS_CLOCK_DIV_64,
/* ICLK is the MCU clock, allow it to run as fast as the LOCO is capable. */
.iclk_div = CGC_SYS_CLOCK_DIV_1,
/* These clocks do not exist on some devices. If any clocks don't exist, set the
divider to 1. */
.pclka_div = CGC_SYS_CLOCK_DIV_1,
.pclkc_div = CGC_SYS_CLOCK_DIV_1,
.fclk_div = CGC_SYS_CLOCK_DIV_1,
.bclk_div = CGC_SYS_CLOCK_DIV_1,
};
/* Switch the system clock to LOCO. */
```

```
err = R_CGC_SystemClockSet(&g_cg0_ctrl, CGC_CLOCK_LOCO, &dividers);
handle_error(err);
```

**Return values**

FSP_SUCCESS	Operation performed successfully.
FSP_ERR_ASSERTION	Invalid input argument.
FSP_ERR_NOT_OPEN	Module is not open.
FSP_ERR_CLOCK_INACTIVE	The specified clock source is inactive.
FSP_ERR_NOT_STABILIZED	The clock source has not stabilized

**◆ R\_CGC\_SystemClockGet()**

```
fsp_err_t R_CGC_SystemClockGet ( cgc_ctrl_t *const p_ctrl, cgc_clock_t *const p_clock_source,
cgc_divider_cfg_t *const p_divider_cfg )
```

Return the current system clock source and configuration. Implements `cgc_api_t::systemClockGet`.

**Return values**

FSP_SUCCESS	Parameters returned successfully.
FSP_ERR_ASSERTION	Invalid input argument.
FSP_ERR_NOT_OPEN	Module is not open.

### ◆ R\_CGC\_OscStopDetectEnable()

```
fsp_err_t R_CGC_OscStopDetectEnable ( cgc_ctrl_t *const p_ctrl)
```

Enable the oscillation stop detection for the main clock. Implements `cgc_api_t::oscStopDetectEnable`.

The MCU will automatically switch the system clock to MOCO when a stop is detected if Main Clock is the system clock. If the system clock is the PLL, then the clock source will not be changed and the PLL free running frequency will be the system clock frequency.

Example:

```
/* Enable oscillation stop detection. The main oscillator must be running at this
point. */
err = R_CGC_OscStopDetectEnable(&g_cgc0_ctrl);
handle_error(err);
```

#### Return values

FSP_SUCCESS	Operation performed successfully.
FSP_ERR_ASSERTION	Invalid input argument.
FSP_ERR_NOT_OPEN	Module is not open.
FSP_ERR_LOW_VOLTAGE_MODE	Settings not allowed in low voltage mode.

◆ **R\_CGC\_OscStopDetectDisable()**

```
fsp_err_t R_CGC_OscStopDetectDisable ( cgc_ctrl_t *const p_ctrl)
```

Disable the oscillation stop detection for the main clock. Implements `cgc_api_t::oscStopDetectDisable`.

Example:

```
/* (Optional) Oscillation stop detection must be disabled before entering any low
power mode. */
err = R_CGC_OscStopDetectDisable(&g_cgc0_ctrl);
handle_error(err);
__WFI();
```

**Return values**

FSP_SUCCESS	Operation performed successfully.
FSP_ERR_ASSERTION	Invalid input argument.
FSP_ERR_NOT_OPEN	Module is not open.
FSP_ERR_OSC_STOP_DETECTED	The Oscillation stop detect status flag is set. Under this condition it is not possible to disable the Oscillation stop detection function.



### ◆ R\_CGC\_OscStopStatusClear()

```
fsp_err_t R_CGC_OscStopStatusClear ( cgc_ctrl_t *const p_ctrl)
```

Clear the Oscillation Stop Detection Status register. This register is not cleared automatically if the stopped clock is restarted. Implements `cgc_api_t::oscStopStatusClear`.

After clearing the status, oscillation stop detection is no longer enabled.

This register cannot be cleared while the main oscillator is the system clock or the PLL source clock.

Example:

```
/* (Optional) Clear the error flag. Only clear this flag after switching the MCU
clock source away from the main
* oscillator and if the main oscillator is stable again. */
err = R_CGC_OscStopStatusClear(&g_cgc0_ctrl);
handle_error(err);
```

#### Return values

FSP_SUCCESS	Operation performed successfully.
FSP_ERR_ASSERTION	Invalid input argument.
FSP_ERR_NOT_OPEN	Module is not open.
FSP_ERR_CLOCK_INACTIVE	Main oscillator must be running to clear the oscillation stop detection flag.
FSP_ERR_OSC_STOP_CLOCK_ACTIVE	The Oscillation Detect Status flag cannot be cleared if the Main Osc or PLL is set as the system clock. Change the system clock before attempting to clear this bit.
FSP_ERR_INVALID_HW_CONDITION	Oscillation stop status was not cleared. Check preconditions and try again.

◆ **R\_CGC\_CallbackSet()**

```
fsp_err_t R_CGC_CallbackSet ( cgc_ctrl_t *const p_api_ctrl, void(*) (cgc_callback_args_t *)
p_callback, void const *const p_context, cgc_callback_args_t *const p_callback_memory )
```

Updates the user callback and has option of providing memory for callback structure. Implements `cgc_api_t::callbackSet`

**Return values**

FSP_SUCCESS	Callback updated successfully.
FSP_ERR_ASSERTION	A required pointer is NULL.
FSP_ERR_NOT_OPEN	The control block has not been opened.

◆ **R\_CGC\_Close()**

```
fsp_err_t R_CGC_Close ( cgc_ctrl_t *const p_ctrl)
```

Closes the CGC module. Implements `cgc_api_t::close`.

**Return values**

FSP_SUCCESS	The module is successfully closed.
FSP_ERR_ASSERTION	Invalid input argument.
FSP_ERR_NOT_OPEN	Module is not open.

◆ **R\_CGC\_VersionGet()**

```
fsp_err_t R_CGC_VersionGet ( fsp_version_t *const p_version)
```

Return the driver version. Implements `cgc_api_t::versionGet`.

**Return values**

FSP_SUCCESS	Module version provided in p_version.
FSP_ERR_ASSERTION	Invalid input argument.

## 4.2.9 Cyclic Redundancy Check (CRC) Calculator (r\_crc)

### Modules

### Functions

```
fsp_err_t R_CRC_Open (crc_ctrl_t *const p_ctrl, crc_cfg_t const *const p_cfg)
```

```
fsp_err_t R_CRC_Close (crc_ctrl_t *const p_ctrl)
```

```
fsp_err_t R_CRC_Calculate (crc_ctrl_t *const p_ctrl, crc_input_t *const
p_crc_input, uint32_t *calculatedValue)
```

```
fsp_err_t R_CRC_CalculatedValueGet (crc_ctrl_t *const p_ctrl, uint32_t
*calculatedValue)
```

```
fsp_err_t R_CRC_SnoopEnable (crc_ctrl_t *const p_ctrl, uint32_t crc_seed)
```

```
fsp_err_t R_CRC_SnoopDisable (crc_ctrl_t *const p_ctrl)
```

```
fsp_err_t R_CRC_VersionGet (fsp_version_t *const p_version)
```

## Detailed Description

Driver for the CRC peripheral on RA MCUs. This module implements the [CRC Interface](#).

## Overview

The CRC module provides a API to calculate 8, 16 and 32-bit CRC values on a block of data in memory or a stream of data over a Serial Communication Interface (SCI) channel using industry-standard polynomials.

### Features

- CRC module supports the following 8 and 16 bit CRC polynomials which operates on 8-bit data in parallel
  - $X^8 + X^2 + X + 1$  (CRC-8)
  - $X^{16} + X^{15} + X^2 + 1$  (CRC-16)
  - $X^{16} + X^{12} + X^5 + 1$  (CRC-CCITT)
- CRC module supports the following 32 bit CRC polynomials which operates on 32-bit data in parallel
  - $X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$  (CRC-32)
  - $X^{32} + X^{28} + X^{27} + X^{26} + X^{25} + X^{23} + X^{22} + X^{20} + X^{19} + X^{18} + X^{14} + X^{13} + X^{11} + X^{10} + X^9 + X^8 + X^6 + 1$  (CRC-32C)
- CRC module can calculate CRC with LSB first or MSB first bit order.

## Configuration

### Build Time Configurations for r\_crc

The following build time configurations are defined in fsp\_cfg/r\_crc\_cfg.h:

Configuration	Options	Default	Description
---------------	---------	---------	-------------

Parameter Checking	<ul style="list-style-type: none"> <li>• Default (BSP)</li> <li>• Enabled</li> <li>• Disabled</li> </ul>	Default (BSP)	If selected code for parameter checking is included in the build.
--------------------	----------------------------------------------------------------------------------------------------------	---------------	-------------------------------------------------------------------

### Configurations for Driver > Monitoring > CRC Driver on r\_crc

This module can be added to the Stacks tab via New Stack > Driver > Monitoring > CRC Driver on r\_crc. Non-secure callable guard functions can be generated for this module by right clicking the module in the RA Configuration tool and checking the "Non-secure Callable" box.

Configuration	Options	Default	Description
Name	Name must be a valid C symbol	g_crc0	Module name.
CRC Polynomial	<ul style="list-style-type: none"> <li>• CRC-8</li> <li>• CRC-16</li> <li>• CRC-CCITT</li> <li>• CRC-32</li> <li>• CRC-32C</li> </ul>	CRC-32C	Select the CRC polynomial.
Bit Order	<ul style="list-style-type: none"> <li>• LSB</li> <li>• MSB</li> </ul>	MSB	Select the CRC bit order.
Snoop Address	Refer to the RA Configuration tool for available options.	NONE	Select the SCI register address CRC snoop

### Clock Configuration

There is no clock configuration for the CRC module.

### Pin Configuration

This module does not use I/O pins.

## Usage Notes

### CRC Snoop

The CRC snoop function monitors reads from and writes to a specified I/O register address and performs CRC calculation on the data read from and written to the register address automatically. Instead of calling R\_CRC\_Calculate on a block of data, R\_CRC\_SnoopEnable is called to start monitoring reads/writes and R\_CRC\_CalculatedValueGet is used to obtain the current CRC.

#### Note

*Snoop mode is available for transmit/receive operations on SCI only.*

### Limitations

When using CRC32 polynomial functions the CRC module produces the same results as popular online CRC32 calculators, but it is important to remember a few important points.

- Online CRC32 calculators allow the input to be any number of bytes. The FSP CRC32 API

function uses 32-bit words. This means the online calculations must be 'padded' to end on a 32-bit boundary.

- Online CRC32 calculators usually invert the output prior to presenting it as a result. It is up to the application program to include this step if needed.
- The seed value of 0xFFFFFFFF needs to be used by both the online calculator and the R\_CRC module API (CRC32 polynomials)
- Make sure the bit orientation of the R\_CRC CRC32 is set for LSB and that you have CRC32 selected and not CRC32C.
- Some online CRC tools XOR the final result with 0xFFFFFFFF.

## Examples

### Basic Example

This is a basic example of minimal use of the CRC module in an application.

```
void crc_example ()
{
    uint32_t length;
    uint32_t uint8_calculated_value;
    length = sizeof(g_data_8bit) / sizeof(g_data_8bit[0]);
    crc_input_t example_input =
    {
        .p_input_buffer = g_data_8bit,
        .num_bytes      = length,
        .crc_seed       = 0,
    };
    /* Open CRC module with 8 bit polynomial */
    R_CRC_Open(&crc_ctrl, &g_crc_test_cfg);
    /* 8-bit CRC calculation */
    R_CRC_Calculate(&crc_ctrl, &example_input, &uint8_calculated_value);
}
```

### Snoop Example

This example demonstrates CRC snoop operation.

```
void crc_snoop_example ()
{
    /* Open CRC module with 8 bit polynomial */
    R_CRC_Open(&crc_ctrl, &g_crc_test_cfg);
```

```

/* Open SCI Driver */
/* Configure Snoop address and enable snoop mode */
R_CRC_SnoopEnable(&crc_ctrl, 0);
/* Perform SCI read/write operation depending on the SCI snoop address configure */
/* Read CRC value */
R_CRC_CalculatedValueGet(&crc_ctrl, &g_crc_buff);
}

```

## Data Structures

```
struct crc\_instance\_ctrl\_t
```

## Data Structure Documentation

### ◆ [crc\\_instance\\_ctrl\\_t](#)

```
struct crc\_instance\_ctrl\_t
```

Driver instance control structure.

## Function Documentation

### ◆ [R\\_CRC\\_Open\(\)](#)

```
fsp\_err\_t R_CRC_Open ( crc\_ctrl\_t *const p_ctrl, crc\_cfg\_t const *const p_cfg )
```

Open the CRC driver module

Implements [crc\\_api\\_t::open](#)

Open the CRC driver module and initialize the driver control block according to the passed-in configuration structure.

#### Return values

FSP_SUCCESS	Configuration was successful.
FSP_ERR_ASSERTION	p_ctrl or p_cfg is NULL.
FSP_ERR_ALREADY_OPEN	Module already open

◆ **R\_CRC\_Close()**

```
fsp_err_t R_CRC_Close ( crc_ctrl_t *const p_ctrl)
```

Close the CRC module driver.

Implements `crc_api_t::close`

**Return values**

FSP_SUCCESS	Configuration was successful.
FSP_ERR_ASSERTION	p_ctrl is NULL.
FSP_ERR_NOT_OPEN	The driver is not opened.

◆ **R\_CRC\_Calculate()**

```
fsp_err_t R_CRC_Calculate ( crc_ctrl_t *const p_ctrl, crc_input_t *const p_crc_input, uint32_t *
calculatedValue )
```

Perform a CRC calculation on a block of 8-bit/32-bit (for 32-bit polynomial) data.

Implements `crc_api_t::calculate`

This function performs a CRC calculation on an array of 8-bit/32-bit (for 32-bit polynomial) values and returns an 8-bit/32-bit (for 32-bit polynomial) calculated value

**Return values**

FSP_SUCCESS	Calculation successful.
FSP_ERR_ASSERTION	Either p_ctrl, inputBuffer, or calculatedValue is NULL.
FSP_ERR_INVALID_ARGUMENT	length value is NULL.
FSP_ERR_NOT_OPEN	The driver is not opened.

◆ **R\_CRC\_CalculatedValueGet()**

```
fsp_err_t R_CRC_CalculatedValueGet ( crc_ctrl_t *const p_ctrl, uint32_t * calculatedValue )
```

Return the current calculated value.

Implements [crc\\_api\\_t::crcResultGet](#)

CRC calculation operates on a running value. This function returns the current calculated value.

**Return values**

FSP_SUCCESS	Return of calculated value successful.
FSP_ERR_ASSERTION	Either p_ctrl or calculatedValue is NULL.
FSP_ERR_NOT_OPEN	The driver is not opened.

◆ **R\_CRC\_SnoopEnable()**

```
fsp_err_t R_CRC_SnoopEnable ( crc_ctrl_t *const p_ctrl, uint32_t crc_seed )
```

Configure the snoop channel and set the CRC seed.

Implements [crc\\_api\\_t::snoopEnable](#)

The CRC calculator can operate on reads and writes over any of the first ten SCI channels. For example, if set to channel 0, transmit, every byte written out SCI channel 0 is also sent to the CRC calculator as if the value was explicitly written directly to the CRC calculator.

**Return values**

FSP_SUCCESS	Snoop configured successfully.
FSP_ERR_ASSERTION	Pointer to control structure is NULL
FSP_ERR_NOT_OPEN	The driver is not opened.

◆ **R\_CRC\_SnoopDisable()**

```
fsp_err_t R_CRC_SnoopDisable ( crc_ctrl_t *const p_ctrl)
```

Disable snooping.

Implements [crc\\_api\\_t::snoopDisable](#)

**Return values**

FSP_SUCCESS	Snoop disabled.
FSP_ERR_ASSERTION	p_ctrl is NULL.
FSP_ERR_NOT_OPEN	The driver is not opened.



◆ **R\_CRC\_VersionGet()**

```
fsp_err_t R_CRC_VersionGet ( fsp_version_t *const p_version)
```

Get the driver version based on compile time macros.

Implements `crc_api_t::versionGet`

**Return values**

FSP_SUCCESS	Successful close.
FSP_ERR_ASSERTION	p_version is NULL.

**4.2.10 Capacitive Touch Sensing Unit (r\_ctsu)**

## Modules

**Functions**

```
fsp_err_t R_CTSU_Open (ctsu_ctrl_t *const p_ctrl, ctstu_cfg_t const *const p_cfg)
```

Opens and configures the CTSU driver module. Implements `ctsu_api_t::open`. [More...](#)

```
fsp_err_t R_CTSU_ScanStart (ctsu_ctrl_t *const p_ctrl)
```

This function should be called each time a periodic timer expires. If initial offset tuning is enabled, The first several calls are used to tuning for the sensors. Before starting the next scan, first get the data with `R_CTSU_DataGet()`. If a different control block scan should be run, check the scan is complete before executing. Implements `ctsu_api_t::scanStart`. [More...](#)

```
fsp_err_t R_CTSU_DataGet (ctsu_ctrl_t *const p_ctrl, uint16_t *p_data)
```

This function gets the sensor values as scanned by the CTSU. If initial offset tuning is enabled, The first several calls are used to tuning for the sensors. Implements `ctsu_api_t::dataGet`. [More...](#)

```
fsp_err_t R_CTSU_CallbackSet (ctsu_ctrl_t *const p_api_ctrl, void(*p_callback)(ctsu_callback_args_t *), void const *const p_context, ctstu_callback_args_t *const p_callback_memory)
```

```
fsp_err_t R_CTSU_Close (ctsu_ctrl_t *const p_ctrl)
```

Disables specified CTSU control block. Implements `ctsu_api_t::close`.

[More...](#)`fsp_err_t R_CTSU_VersionGet (fsp_version_t *const p_version)`

Return CTSU HAL driver version. Implements `ctsu_api_t::versionGet`.  
[More...](#)

## Detailed Description

This HAL driver supports the Capacitive Touch Sensing Unit (CTSU). It implements the [CTSU Interface](#).

## Overview

The capacitive touch sensing unit HAL driver (`r_ctsu`) provides an API to control the CTSU peripheral. This module performs capacitance measurement based on various settings defined by the configuration. This module is configured via the [QE for Capacitive Touch](#).

## Features

- Supports both Self-capacitance multi scan mode and Mutual-capacitance full scan mode
- Scans may be started by software or an external trigger
- Returns measured capacitance data on scan completion
- Optional DTC support

## Configuration

### Note

*This module is configured via the [QE for Capacitive Touch](#). For information on how to use the QE tool, once the tool is installed click [Help](#) -> [Help Contents](#) in e2 studio and search for "QE".*

### Build Time Configurations for r\_ctsu

The following build time configurations are defined in `fsp_cfg/r_ctsu_cfg.h`:

Configuration	Options	Default	Description
Parameter Checking	<ul style="list-style-type: none"> <li>• Default (BSP)</li> <li>• Enabled</li> <li>• Disabled</li> </ul>	Default (BSP)	If selected code for parameter checking is included in the build.
Support for using DTC	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Disabled	Enable DTC support for the CTSU module.
Interrupt priority level	MCU Specific Options		Priority level of all CTSU interrupt (CSTU_WR, CTSU_RD, CTSU_FN)

### Configurations for Driver > CapTouch > CTSU Driver on r\_ctsu

This module can be added to the Stacks tab via New Stack > Driver > CapTouch > CTSU Driver on r\_ctsu. Non-secure callable guard functions can be generated for this module by right clicking the module in the RA Configuration tool and checking the "Non-secure Callable" box.

Configuration	Options	Default	Description
Scan Start Trigger	MCU Specific Options		CTSU Scan Start Trigger Select

## Interrupt Configuration

The first `R_CTSU_Open` function call sets CTSU peripheral interrupts. The user should provide a callback function to be invoked at the end of the CTSU scan sequence. The callback argument will contain information about the scan status.

## Clock Configuration

The CTSU peripheral module uses PCLKB as its clock source. You can set the PCLKB frequency using the **Clocks** tab of the RA Configuration editor or by using the CGC Interface at run-time.

*Note*

*The CTSU Drive pulse will be calculated and set by the tooling depending on the selected transfer rate.*

## Pin Configuration

The TS<sub>n</sub> pins are sensor pins for the CTSU.

The TSCAP pin is used for an internal low-pass filter and must be connected to an external decoupling capacitor.

# Usage Notes

## CTSU

### Self-capacitance multi scan mode

In self-capacitance mode each TS pin is assigned to one touch button. Electrodes of multiple TS pins can be physically aligned to create slider or wheel interfaces.

- Scan Order
  - The hardware scans the specified pins in ascending order.
  - For example, if pins TS05, TS08, TS02, TS03, and TS06 are specified in your application, the hardware will scan them in the order TS02, TS03, TS05, TS06, TS08.
- Element
  - An element refers to the index of a pin within the scan order. Using the previous example, TS05 is element 2.
- Scan Time
  - Scanning is handled directly by the CTSU peripheral and does not utilize any main processor time.
  - It takes approximately 500us to scan a single sensor.
  - If DTC is not used additional overhead is required for the main processor to transfer data to/from registers when each sensor is scanned.

### Mutual-capacitance full scan mode

In mutual-capacitance mode each TS pin acts as either a 'row' or 'column' in an array of sensors. As a result, this mode uses fewer pins when more than five sensors are configured. Mutual-capacitance mode is ideal for applications where many touch sensors are required, like keypads, button matrices and pads.

As an example, consider a standard phone keypad comprised of a matrix of four rows and three columns.

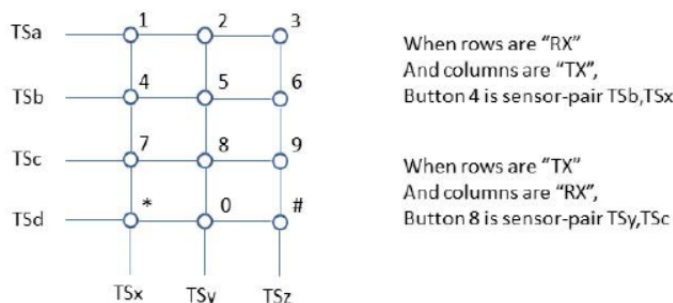


Figure 154: Mutual Button Image

In mutual capacitance mode only 7 pins are necessary to scan 12 buttons. In self mode, 12 pins would be required.

- Scan Order
  - The hardware scans the matrix by iterating over the TX pins first and the RX pins second.
  - For example, if pins TS10, TS11, and TS03 are specified as RX sensors and pins TS02, TS07, and TS04 are specified as TX sensors, the hardware will scan them in the following sensor-pair order:  
TS03-TS02, TS03-TS04, TS03-TS07, TS10-TS02, TS10-TS04, TS10-TS07, TS11-TS02, TS11-TS04, TS11-TS07
- Element
  - An element refers to the index of a sensor-pair within the scan order. Using the previous example, TS10-TS07 is element 5.
- Scan Time
  - Because mutual-capacitance scans two patterns for one element it takes twice as long as self-capacitance (1ms vs 0.5ms per element).

## TrustZone Support

In r\_ctsu and rm\_touch module, Non-Secure Callable Guard Functions are only generated from QE for Capacitive Touch. QE can be used for tuning in secure or flat project, but not in non-secure project. If you want to use in non-secure project, copy the output file from secure or flat project. Refer to QE Help for more information.

## Examples

### Basic Example

This is a basic example of minimal use of the CTSU in an application.

```
volatile bool g_scan_flag = false;
```

```
void ctsu_callback (ctsu_callback_args_t * p_args)
{
    if (CTSU_EVENT_SCAN_COMPLETE == p_args->event)
    {
        g_scan_flag = true;
    }
}

void ctsu_basic_example (void)
{
    fsp_err_t err = FSP_SUCCESS;

    uint16_t data[CTSU_CFG_NUM_SELF_ELEMENTS];
    err = R_CTSU_Open(&g_ctsu_ctrl, &g_ctsu_cfg);
    /* Handle any errors. This function should be defined by the user. */
    handle_error(err);

    while (true)
    {
        err = R_CTSU_ScanStart(&g_ctsu_ctrl);
        handle_error(err);

        while (!g_scan_flag)
        {
            /* Wait for scan end callback */
        }

        g_scan_flag = false;
        err = R_CTSU_DataGet(&g_ctsu_ctrl, data);

        if (FSP_SUCCESS == err)
        {
            /* Application specific data processing. */
        }
    }
}
```

### Multi-configuration Example

This is an optional example of using both Self-capacitance and Mutual-capacitance configurations in the same project.

```
void ctsu_optional_example (void)
{
    fsp_err_t err = FSP_SUCCESS;

    uint16_t data[CTSU_CFG_NUM_SELF_ELEMENTS + (CTSU_CFG_NUM_MUTUAL_ELEMENTS * 2)];
    err = R_CTSU_Open(&g_ctsu_ctrl, &g_ctsu_cfg);
    handle_error(err);

    err = R_CTSU_Open(&g_ctsu_ctrl_mutual, &g_ctsu_cfg_mutual);
    handle_error(err);

    while (true)
    {
        R_CTSU_ScanStart(&g_ctsu_ctrl);
        while (!g_scan_flag)
        {
            /* Wait for scan end callback */
        }
        g_scan_flag = false;
        R_CTSU_ScanStart(&g_ctsu_ctrl_mutual);
        while (!g_scan_flag)
        {
            /* Wait for scan end callback */
        }
        g_scan_flag = false;
        err = R_CTSU_DataGet(&g_ctsu_ctrl, data);
        handle_error(err);
        if (FSP_SUCCESS == err)
        {
            /* Application specific data processing. */
        }
        err = R_CTSU_DataGet(&g_ctsu_ctrl_mutual, data);
        handle_error(err);
        if (FSP_SUCCESS == err)
        {
            /* Application specific data processing. */
        }
    }
}
```

```

}
}

```

## Data Structures

struct [ctsu\\_ctsuwr\\_t](#)

struct [ctsu\\_self\\_buf\\_t](#)

struct [ctsu\\_mutual\\_buf\\_t](#)

struct [ctsu\\_correction\\_info\\_t](#)

struct [ctsu\\_instance\\_ctrl\\_t](#)

## Enumerations

enum [ctsu\\_state\\_t](#)

enum [ctsu\\_tuning\\_t](#)

enum [ctsu\\_correction\\_status\\_t](#)

enum [ctsu\\_range\\_t](#)

## Data Structure Documentation

### ◆ [ctsu\\_ctsuwr\\_t](#)

struct <a href="#">ctsu_ctsuwr_t</a>		
CTSUWR write register value		
Data Fields		
uint16_t	ctsussc	Copy from (ssdiv << 8) by Open API.
uint16_t	ctsus0	Copy from ((snum << 10)   so) by Open API.
uint16_t	ctsus1	Copy from (sdpa << 8) by Open API. ICOG and RICOA is set recommend value.

### ◆ [ctsu\\_self\\_buf\\_t](#)

struct <a href="#">ctsu_self_buf_t</a>		
Scan buffer data formats (Self)		
Data Fields		
uint16_t	sen	Sensor counter data.

uint16_t	ref	Reference counter data (Not used)
----------	-----	-----------------------------------

◆ **ctsu\_mutual\_buf\_t**

struct ctsu_mutual_buf_t		
Scan buffer data formats (Mutual)		
Data Fields		
uint16_t	pri_sen	Primary sensor data.
uint16_t	pri_ref	Primary reference data (Not used)
uint16_t	snd_sen	Secondary sensor data.
uint16_t	snd_ref	Secondary reference data (Not used)

◆ **ctsu\_correction\_info\_t**

struct ctsu_correction_info_t		
Correction information		
Data Fields		
<a href="#">ctsu_correction_status_t</a>	status	Correction status.
<a href="#">ctsu_ctsuwr_t</a>	ctsuwr	Correction scan parameter.
volatile <a href="#">ctsu_self_buf_t</a>	scanbuf	Correction scan buffer.
uint16_t	first_val	1st correction value
uint16_t	second_val	2nd correction value
uint32_t	first_coefficient	1st correction coefficient
uint32_t	second_coefficient	2nd correction coefficient
uint32_t	ctsu_clock	CTSUS clock [MHz].

◆ **ctsu\_instance\_ctrl\_t**

struct ctsu_instance_ctrl_t		
CTSUS private control block. DO NOT MODIFY. Initialization occurs when <a href="#">R_CTSU_Open()</a> is called.		
<b>Data Fields</b>		
uint32_t	<a href="#">open</a>	
		Whether or not driver is open.
<a href="#">ctsu_state_t</a>	<a href="#">state</a>	
		CTSUS run state.



<code>ctsu_tuning_t</code>	<code>tuning</code>
	CTSU Initial offset tuning status.
<code>uint16_t</code>	<code>num_elements</code>
	Number of elements to scan.
<code>uint16_t</code>	<code>wr_index</code>
	Word index into ctsuwr register array.
<code>uint16_t</code>	<code>rd_index</code>
	Word index into scan data buffer.
<code>uint8_t *</code>	<code>p_tuning_count</code>
	Pointer to tuning count of each element. <code>g_ctsu_tuning_count[]</code> is set by Open API.
<code>int32_t *</code>	<code>p_tuning_diff</code>
	Pointer to difference from base value of each element. <code>g_ctsu_tuning_diff[]</code> is set by Open API.
<code>uint16_t</code>	<code>average</code>
	CTSU Moving average counter.
<code>uint16_t</code>	<code>num_moving_average</code>
	Copy from config by Open API.
<code>uint8_t</code>	<code>ctsucr1</code>
	Copy from ( <code>atune1 &lt;&lt; 3</code> , <code>md &lt;&lt; 6</code> ) by Open API. CLK, ATUNE0, CSW, and PON is set by HAL driver.

<code>ctsu_ctsuwr_t *</code>	<code>p_ctsuwr</code>
	CTSUWR write register value. <code>g_ctsu_ctsuwr[]</code> is set by Open API.
<code>ctsu_self_buf_t *</code>	<code>p_self_raw</code>
	Pointer to Self raw data. <code>g_ctsu_self_raw[]</code> is set by Open API.
<code>uint16_t *</code>	<code>p_self_work</code>
	Pointer to Self work buffer. <code>g_ctsu_self_work[]</code> is set by Open API.
<code>uint16_t *</code>	<code>p_self_data</code>
	Pointer to Self moving average data. <code>g_ctsu_self_data[]</code> is set by Open API.
<code>ctsu_mutual_buf_t *</code>	<code>p_mutual_raw</code>
	Pointer to Mutual raw data. <code>g_ctsu_mutual_raw[]</code> is set by Open API.
<code>uint16_t *</code>	<code>p_mutual_pri_work</code>
	Pointer to Mutual primary work buffer. <code>g_ctsu_mutual_pri_work[]</code> is set by Open API.
<code>uint16_t *</code>	<code>p_mutual_snd_work</code>
	Pointer to Mutual secondary work buffer. <code>g_ctsu_mutual_snd_work[]</code> is set by Open API.
<code>uint16_t *</code>	<code>p_mutual_pri_data</code>
	Pointer to Mutual primary moving average data. <code>g_ctsu_mutual_pri_data[]</code> is set by Open API.
<code>uint16_t *</code>	<code>p_mutual_snd_data</code>

	Pointer to Mutual secondary moving average data. g_ctsu_mutual_snd_data[] is set by Open API.
ctsu_correction_info_t *	p_correction_info
	Pointer to correction info.
ctsu_cfg_t const *	p_ctsu_cfg
	Pointer to initial configurations.
IRQn_Type	write_irq
	Copy from config by Open API. CTSU_CTSUWR interrupt vector.
IRQn_Type	read_irq
	Copy from config by Open API. CTSU_CTSURD interrupt vector.
IRQn_Type	end_irq
	Copy from config by Open API. CTSU_CTSUFN interrupt vector.
void(*	p_callback )(ctsu_callback_args_t *)
	Callback provided when a CTSUFN occurs.
ctsu_callback_args_t *	p_callback_memory
	Pointer to non-secure memory that can be used to pass arguments to a callback in non-secure memory.
void const *	p_context
	Placeholder for user data.

## Enumeration Type Documentation

### ◆ ctsu\_state\_t

enum <a href="#">ctsu_state_t</a>	
CTSU run state	
Enumerator	
CTSU_STATE_INIT	Not open.
CTSU_STATE_IDLE	Opened.
CTSU_STATE_SCANNING	Scanning now.
CTSU_STATE_SCANNED	Scan end.

### ◆ ctsu\_tuning\_t

enum <a href="#">ctsu_tuning_t</a>	
CTSU Initial offset tuning status	
Enumerator	
CTSU_TUNING_INCOMPLETE	Initial offset tuning incomplete.
CTSU_TUNING_COMPLETE	Initial offset tuning complete.

### ◆ ctsu\_correction\_status\_t

enum <a href="#">ctsu_correction_status_t</a>	
CTSU Correction status	
Enumerator	
CTSU_CORRECTION_INIT	Correction initial status.
CTSU_CORRECTION_RUN	Correction scan running.
CTSU_CORRECTION_COMPLETE	Correction complete.
CTSU_CORRECTION_ERROR	Correction error.

◆ **ctsu\_range\_t**

enum <code>ctsu_range_t</code>	
CTSU range definition	
Enumerator	
<code>CTSU_RANGE_20UA</code>	20uA mode
<code>CTSU_RANGE_40UA</code>	40uA mode
<code>CTSU_RANGE_80UA</code>	80uA mode
<code>CTSU_RANGE_160UA</code>	160uA mode
<code>CTSU_RANGE_NUM</code>	number of range

**Function Documentation**◆ **R\_CTSU\_Open()**

```
fsp_err_t R_CTSU_Open ( ctsu_ctrl_t*const p_ctrl, ctsu_cfg_t const *const p_cfg )
```

Opens and configures the CTSU driver module. Implements `ctsu_api_t::open`.

Example:

```
err = R_CTSU_Open(&g_ctsu_ctrl, &g_ctsu_cfg);
```

**Return values**

<code>FSP_SUCCESS</code>	CTSU successfully configured.
<code>FSP_ERR_ASSERTION</code>	Null pointer, or one or more configuration options is invalid.
<code>FSP_ERR_ALREADY_OPEN</code>	Module is already open. This module can only be opened once.
<code>FSP_ERR_INVALID_ARGUMENT</code>	Configuration parameter error.

**Note**

*In the first Open, measurement for correction works, and it takes several tens of milliseconds.*

## ◆ R\_CTSU\_ScanStart()

```
fsp_err_t R_CTSU_ScanStart ( ctsu_ctrl_t *const p_ctrl)
```

This function should be called each time a periodic timer expires. If initial offset tuning is enabled, The first several calls are used to tuning for the sensors. Before starting the next scan, first get the data with [R\\_CTSU\\_DataGet\(\)](#). If a different control block scan should be run, check the scan is complete before executing. Implements [ctsu\\_api\\_t::scanStart](#).

Example:

```
while (true)
{
    err = R_CTSU_ScanStart(&g_ctsu_ctrl);
    handle_error(err);
while (!g_scan_flag)
{
    /* Wait for scan end callback */
}
    g_scan_flag = false;
    err = R_CTSU_DataGet(&g_ctsu_ctrl, data);
if (FSP_SUCCESS == err)
{
    /* Application specific data processing. */
}
}
```

### Return values

FSP_SUCCESS	CTSU successfully configured.
FSP_ERR_ASSERTION	Null pointer passed as a parameter.
FSP_ERR_NOT_OPEN	Module is not open.
FSP_ERR_CTSU_SCANNING	Scanning this instance or other.
FSP_ERR_CTSU_NOT_GET_DATA	The previous data has not been retrieved by DataGet.

### ◆ R\_CTSU\_DataGet()

```
fsp_err_t R_CTSU_DataGet ( ctsu_ctrl_t *const p_ctrl, uint16_t * p_data )
```

This function gets the sensor values as scanned by the CTSU. If initial offset tuning is enabled, The first several calls are used to tuning for the sensors. Implements [cts\\_u\\_api\\_t::dataGet](#).

Example:

```
while (true)
{
    err = R_CTSU_ScanStart(&g_ctsu_ctrl);
    handle_error(err);
while (!g_scan_flag)
{
    /* Wait for scan end callback */
}
    g_scan_flag = false;
    err = R_CTSU_DataGet(&g_ctsu_ctrl, data);
if (FSP_SUCCESS == err)
{
    /* Application specific data processing. */
}
}
```

#### Return values

FSP_SUCCESS	CTSU successfully configured.
FSP_ERR_ASSERTION	Null pointer passed as a parameter.
FSP_ERR_NOT_OPEN	Module is not open.
FSP_ERR_CTSU_SCANNING	Scanning this instance.
FSP_ERR_CTSU_INCOMPLETE_TUNING	Incomplete initial offset tuning.

◆ **R\_CTSU\_CallbackSet()**

```
fsp_err_t R_CTSU_CallbackSet ( ctsu_ctrl_t *const p_api_ctrl, void(*) (ctsu_callback_args_t *)
p_callback, void const *const p_context, ctsu_callback_args_t *const p_callback_memory )
```

Updates the user callback and has option of providing memory for callback structure. Implements `ctsu_api_t::callbackSet`

**Return values**

FSP_SUCCESS	Callback updated successfully.
FSP_ERR_ASSERTION	A required pointer is NULL.
FSP_ERR_NOT_OPEN	The control block has not been opened.

◆ **R\_CTSU\_Close()**

```
fsp_err_t R_CTSU_Close ( ctsu_ctrl_t *const p_ctrl)
```

Disables specified CTSU control block. Implements `ctsu_api_t::close`.

**Return values**

FSP_SUCCESS	CTSU successfully configured.
FSP_ERR_ASSERTION	Null pointer passed as a parameter.
FSP_ERR_NOT_OPEN	Module is not open.

◆ **R\_CTSU\_VersionGet()**

```
fsp_err_t R_CTSU_VersionGet ( fsp_version_t *const p_version)
```

Return CTSU HAL driver version. Implements `ctsu_api_t::versionGet`.

**Return values**

FSP_SUCCESS	Version information successfully read.
FSP_ERR_ASSERTION	Null pointer passed as a parameter

**4.2.11 Digital to Analog Converter (r\_dac)**

## Modules

**Functions**



```
fsp_err_t R_DAC_Open (dac_ctrl_t *p_api_ctrl, dac_cfg_t const *const p_cfg)
```

```
fsp_err_t R_DAC_Write (dac_ctrl_t *p_api_ctrl, uint16_t value)
```

```
fsp_err_t R_DAC_Start (dac_ctrl_t *p_api_ctrl)
```

```
fsp_err_t R_DAC_Stop (dac_ctrl_t *p_api_ctrl)
```

```
fsp_err_t R_DAC_Close (dac_ctrl_t *p_api_ctrl)
```

```
fsp_err_t R_DAC_VersionGet (fsp_version_t *p_version)
```

## Detailed Description

Driver for the DAC12 peripheral on RA MCUs. This module implements the [DAC Interface](#).

## Overview

### Features

The DAC module outputs one of 4096 voltage levels between the positive and negative reference voltages.

- Supports setting left-justified or right-justified 12-bit value format for the 16-bit input data registers
- Supports output amplifiers on selected MCUs
- Supports charge pump on selected MCUs
- Supports synchronization with the Analog-to-Digital Converter (ADC) module

## Configuration

### Note

For MCUs supporting more than one channel, the following configuration options are shared by all the DAC channels:

- Synchronize with ADC
- Data Format
- Charge Pump

### Build Time Configurations for r\_dac

The following build time configurations are defined in fsp\_cfg/r\_dac\_cfg.h:

Configuration	Options	Default	Description
Parameter Checking	<ul style="list-style-type: none"> <li>• Default (BSP)</li> <li>• Enabled</li> <li>• Disabled</li> </ul>	Default (BSP)	If selected code for parameter checking is included in the build.

### Configurations for Driver > Analog > DAC Driver on r\_dac

This module can be added to the Stacks tab via New Stack > Driver > Analog > DAC Driver on r\_dac.

Non-secure callable guard functions can be generated for this module by right clicking the module in the RA Configuration tool and checking the "Non-secure Callable" box.

Configuration	Options	Default	Description
Name	Name must be a valid C symbol	g_dac0	Module name.
Channel	Value must be an integer greater than or equal to 0	0	Specify the hardware channel.
Synchronize with ADC	<ul style="list-style-type: none"> <li>Enabled</li> <li>Disabled</li> </ul>	Disabled	Enable DA/AD synchronization.
Data Format	<ul style="list-style-type: none"> <li>Right Justified</li> <li>Left Justified</li> </ul>	Right Justified	Specify the DAC data format.
Output Amplifier	MCU Specific Options		Enable the DAC output amplifier.
Charge Pump (Requires MOCO active)	MCU Specific Options		Enable the DAC charge pump.
ELC Trigger Source	MCU Specific Options		ELC event source that will trigger the DAC to start a conversion.

## Clock Configuration

The DAC peripheral module uses PCLKB as its clock source.

## Pin Configuration

The DAN pins are used as analog outputs. Each DAC channel has one output pin.

The AVCC0 and AVSS0 pins are power and ground supply pins for the DAC and ADC.

The VREFH and VREFL pins are top and ground voltage reference pins for the DAC and ADC.

## Usage Notes

### Charge Pump

The charge pump must be enabled when using DAC pin output while operating at  $AV_{CC} < 2.7V$ .

*Note*

*The MOCO must be running to use the charge pump.*

*If the DAC output is to be routed to an internal signal, do not enable the charge pump.*

### Synchronization with ADC

When ADC synchronization is enabled and an ADC conversion is in progress, if a DAC conversion is started it will automatically be delayed until after the ADC conversion is complete.

### Limitations

- For MCUs supporting ADC unit 1:
  - Once synchronization between DAC and ADC unit 1 is turned on during R\_DAC\_Open synchronization cannot be turned off by the driver. In order to desynchronize DAC with ADC unit 1, manually clear DAADSCR.DAADST to 0 when the ADCSR.ADST bit is 0 and ADC unit 1 is halted.
  - The DAC module can only be synchronized with ADC unit 1.
  - For MCUs having more than 1 DAC channel, both channels are synchronized with ADC unit 1 if synchronization is enabled.

## Examples

### Basic Example

This is a basic example of minimal use of the R\_DAC in an application. This example shows how this driver can be used for basic Digital to Analog Conversion operations.

```
void basic_example (void)
{
    fsp_err_t err;
    uint16_t value;
    /* Pin configuration: Output enable DA0 as Analog. */
    /* Initialize the DAC channel */
    err = R_DAC_Open(&g_dac_ctrl, &g_dac_cfg);
    /* Handle any errors. This function should be defined by the user. */
    handle_error(err);
    value = (uint16_t) DAC_EXAMPLE_VALUE_ABC;
    err = R_DAC_Write(&g_dac_ctrl, value);
    handle_error(err);
    err = R_DAC_Start(&g_dac_ctrl);
    handle_error(err);
}
```

### Data Structures

struct [dac\\_instance\\_ctrl\\_t](#)

struct [dac\\_extended\\_cfg\\_t](#)

### Data Structure Documentation

#### ◆ [dac\\_instance\\_ctrl\\_t](#)

struct [dac\\_instance\\_ctrl\\_t](#)

DAC instance control block.

◆ **dac\_extended\_cfg\_t**

struct dac_extended_cfg_t		
DAC extended configuration		
Data Fields		
bool	enable_charge_pump	Enable DAC charge pump available on selected MCUs.
bool	output_amplifier_enabled	Output amplifier enable available on selected MCUs.
<a href="#">dac_data_format_t</a>	data_format	Data format.

**Function Documentation**◆ **R\_DAC\_Open()**

```
fsp_err_t R_DAC_Open ( dac_ctrl_t* p_api_ctrl, dac_cfg_t const *const p_cfg )
```

Perform required initialization described in hardware manual. Implements [dac\\_api\\_t::open](#). Configures a single DAC channel, starts the channel, and provides a handle for use with the DAC API Write and Close functions. Must be called once prior to calling any other DAC API functions. After a channel is opened, Open should not be called again for the same channel without calling Close first.

**Return values**

FSP_SUCCESS	The channel was successfully opened.
FSP_ERR_ASSERTION	Parameter check failure due to one or more reasons below: <ol style="list-style-type: none"> <li>1. One or both of the following parameters may be NULL: p_api_ctrl or p_cfg</li> <li>2. data_format value in p_cfg is out of range.</li> <li>3. Extended configuration structure is set to NULL for MCU supporting charge pump.</li> </ol>
FSP_ERR_IP_CHANNEL_NOT_PRESENT	Channel ID requested in p_cfg may not be available on the devices.
FSP_ERR_ALREADY_OPEN	The control structure is already opened.

◆ **R\_DAC\_Write()**

```
fsp_err_t R_DAC_Write ( dac_ctrl_t* p_api_ctrl, uint16_t value )
```

Write data to the D/A converter and enable the output if it has not been enabled.

**Return values**

FSP_SUCCESS	Data is successfully written to the D/A Converter.
FSP_ERR_ASSERTION	p_api_ctrl is NULL.
FSP_ERR_NOT_OPEN	Channel associated with p_ctrl has not been opened.

◆ **R\_DAC\_Start()**

```
fsp_err_t R_DAC_Start ( dac_ctrl_t* p_api_ctrl)
```

Start the D/A conversion output if it has not been started.

**Return values**

FSP_SUCCESS	The channel is started successfully.
FSP_ERR_ASSERTION	p_api_ctrl is NULL.
FSP_ERR_IN_USE	Attempt to re-start a channel.
FSP_ERR_NOT_OPEN	Channel associated with p_ctrl has not been opened.

◆ **R\_DAC\_Stop()**

```
fsp_err_t R_DAC_Stop ( dac_ctrl_t* p_api_ctrl)
```

Stop the D/A conversion and disable the output signal.

**Return values**

FSP_SUCCESS	The control is successfully stopped.
FSP_ERR_ASSERTION	p_api_ctrl is NULL.
FSP_ERR_NOT_OPEN	Channel associated with p_ctrl has not been opened.

◆ **R\_DAC\_Close()**

```
fsp_err_t R_DAC_Close ( dac_ctrl_t * p_api_ctrl)
```

Stop the D/A conversion, stop output, and close the DAC channel.

**Return values**

FSP_SUCCESS	The channel is successfully closed.
FSP_ERR_ASSERTION	p_api_ctrl is NULL.
FSP_ERR_NOT_OPEN	Channel associated with p_ctrl has not been opened.

◆ **R\_DAC\_VersionGet()**

```
fsp_err_t R_DAC_VersionGet ( fsp_version_t * p_version)
```

Get version and store it in provided pointer p\_version.

**Return values**

FSP_SUCCESS	Successfully retrieved version information.
FSP_ERR_ASSERTION	p_version is NULL.

**4.2.12 Digital to Analog Converter (r\_dac8)**

## Modules

**Functions**

```
fsp_err_t R_DAC8_Open (dac_ctrl_t *const p_ctrl, dac_cfg_t const *const p_cfg)
```

```
fsp_err_t R_DAC8_Close (dac_ctrl_t *const p_ctrl)
```

```
fsp_err_t R_DAC8_Write (dac_ctrl_t *const p_ctrl, uint16_t value)
```

```
fsp_err_t R_DAC8_Start (dac_ctrl_t *const p_ctrl)
```

```
fsp_err_t R_DAC8_Stop (dac_ctrl_t *const p_ctrl)
```

```
fsp_err_t R_DAC8_VersionGet (fsp_version_t *p_version)
```

**Detailed Description**

Driver for the DAC8 peripheral on RA MCUs. This module implements the [DAC Interface](#).

## Overview

### Features

The DAC8 module outputs one of 256 voltage levels between the positive and negative reference voltages. DAC8 on selected MCUs have below features

- Charge pump control
- Synchronization with the Analog-to-Digital Converter (ADC) module
- Multiple Operation Modes
  - Normal
  - Real-Time (Event Link)

## Configuration

### Note

For MCUs supporting more than one channel, the following configuration options are shared by all the DAC8 channels:

- Synchronize with ADC
- Charge Pump

### Build Time Configurations for r\_dac8

The following build time configurations are defined in fsp\_cfg/r\_dac8\_cfg.h:

Configuration	Options	Default	Description
Parameter Checking	<ul style="list-style-type: none"> <li>• Default (BSP)</li> <li>• Enabled</li> <li>• Disabled</li> </ul>	Default (BSP)	If selected code for parameter checking is included in the build.

### Configurations for Driver > Analog > DAC8 Driver on r\_dac8

This module can be added to the Stacks tab via New Stack > Driver > Analog > DAC8 Driver on r\_dac8.

Configuration	Options	Default	Description
Name	Name must be a valid C symbol	g_dac8_0	Module name.
Channel	Value must be an integer greater than or equal to 0	0	Specify the hardware channel.
D/A A/D Synchronous Conversion	MCU Specific Options		Synchronize the DAC8 update with the ADC to reduce interference with A/D conversions.
DAC Mode	MCU Specific Options		Select the DAC

operating mode

Real-time Trigger Event MCU Specific Options

Specify the event used to trigger conversion in Real-time mode. This setting is only valid when Real-time mode is enabled.

Charge Pump (Requires MOCO active) MCU Specific Options

Enable the DAC charge pump.

## Clock Configuration

The DAC8 peripheral module uses the PCLKB as its clock source.

## Pin Configuration

The DA8\_n pins are used as analog outputs. Each DAC8 channel has one output pin.

The AVCC0 and AVSS0 pins are power and ground supply and reference pins for the DAC8.

# Usage Notes

## Charge Pump

The charge pump must be enabled when using DAC8 pin output while operating at  $AV_{CC} < 2.7V$ .

*Note*

*The MOCO must be running to use the charge pump.*

*If DAC8 output is to be routed to an internal signal, do not enable the charge pump.*

## Synchronization with ADC

When ADC synchronization is enabled and an ADC conversion is in progress, if a DAC8 conversion is started it will automatically be delayed until after the ADC conversion is complete.

## Real-time Mode

When Real-time mode is selected, the DAC8 will perform a conversion each time the selected ELC event is received.

## Limitations

- Synchronization between DAC8 and ADC is activated when calling R\_DAC8\_Open. At this point synchronization cannot be deactivated by the driver. In order to desynchronize DAC8 with ADC, manually clear DACADSCR.DACADST to 0 while the ADCSR.ADST bit is 0 and the ADC is halted.
- For MCUs having more than 1 DAC8 channel, both channels are synchronized with ADC if synchronization is enabled.

# Examples

## Basic Example



This is a basic example of minimal use of the R\_DAC8 in an application. This example shows how this driver can be used for basic 8 bit Digital to Analog Conversion operations.

```
dac8_instance_ctrl_t g_dac8_ctrl;
dac_cfg_t g_dac8_cfg =
{
    .channel          = 0U,
    .ad_da_synchronized = false,
    .p_extend         = &g_dac8_cfg_extend
};
void basic_example (void)
{
    fsp_err_t err;
    uint16_t value;
    /* Pin configuration: Output enable DA8_0(RA2A1) as Analog. */
    /* Initialize the DAC8 channel */
    err = R_DAC8_Open(&g_dac8_ctrl, &g_dac8_cfg);
    /* Handle any errors. This function should be defined by the user. */
    handle_error(err);
    value = (uint8_t) DAC8_EXAMPLE_VALUE_ABC;
    /* Write value to DAC module */
    err = R_DAC8_Write(&g_dac8_ctrl, value);
    handle_error(err);
    /* Start DAC8 conversion */
    err = R_DAC8_Start(&g_dac8_ctrl);
    handle_error(err);
}
```

## Data Structures

struct [dac8\\_instance\\_ctrl\\_t](#)

struct [dac8\\_extended\\_cfg\\_t](#)

## Enumerations

enum [dac8\\_mode\\_t](#)

## Data Structure Documentation

◆ **dac8\_instance\_ctrl\_t**

struct dac8\_instance\_ctrl\_t

DAC8 instance control block. DO NOT INITIALIZE.

◆ **dac8\_extended\_cfg\_t**

struct dac8\_extended\_cfg\_t

DAC8 extended configuration

## Data Fields

bool	enable_charge_pump	Enable DAC charge pump.
dac8_mode_t	dac_mode	DAC mode.

**Enumeration Type Documentation**◆ **dac8\_mode\_t**

enum dac8\_mode\_t

## Enumerator

DAC8_MODE_NORMAL	DAC Normal mode.
DAC8_MODE_REAL_TIME	DAC Real-time (event link) mode.

**Function Documentation**

◆ **R\_DAC8\_Open()**

```
fsp_err_t R_DAC8_Open ( dac_ctrl_t *const p_ctrl, dac_cfg_t const *const p_cfg )
```

Perform required initialization described in hardware manual.

Implements `dac_api_t::open`.

Configures a single DAC channel. Must be called once prior to calling any other DAC API functions. After a channel is opened, Open should not be called again for the same channel without calling Close first.

**Return values**

FSP_SUCCESS	The channel was successfully opened.
FSP_ERR_ASSERTION	One or both of the following parameters may be NULL: p_ctrl or p_cfg
FSP_ERR_ALREADY_OPEN	The instance control structure has already been opened.
FSP_ERR_IP_CHANNEL_NOT_PRESENT	An invalid channel was requested.
FSP_ERR_NOT_ENABLED	Setting DACADSCR is not enabled when ADCSR.ADST = 0.

**Note**

*This function is reentrant for different channels. It is not reentrant for the same channel.*

◆ **R\_DAC8\_Close()**

```
fsp_err_t R_DAC8_Close ( dac_ctrl_t *const p_ctrl)
```

Stop the D/A conversion, stop output, and close the DAC channel.

**Return values**

FSP_SUCCESS	The channel is successfully closed.
FSP_ERR_ASSERTION	p_ctrl is NULL.
FSP_ERR_NOT_OPEN	Channel associated with p_instance_ctrl has not been opened.

◆ **R\_DAC8\_Write()**

```
fsp_err_t R_DAC8_Write ( dac_ctrl_t *const p_ctrl, uint16_t value )
```

Write data to the D/A converter.

**Return values**

FSP_SUCCESS	Data is successfully written to the D/A Converter.
FSP_ERR_ASSERTION	p_ctrl is NULL.
FSP_ERR_NOT_OPEN	Channel associated with p_instance_ctrl has not been opened.
FSP_ERR_OVERFLOW	Data overflow when data value exceeds 8-bit limit.

◆ **R\_DAC8\_Start()**

```
fsp_err_t R_DAC8_Start ( dac_ctrl_t *const p_ctrl)
```

Start the D/A conversion output.

**Return values**

FSP_SUCCESS	The channel is started successfully.
FSP_ERR_ASSERTION	p_ctrl is NULL.
FSP_ERR_NOT_OPEN	Channel associated with p_instance_ctrl has not been opened.
FSP_ERR_IN_USE	Attempt to re-start a channel.

◆ **R\_DAC8\_Stop()**

```
fsp_err_t R_DAC8_Stop ( dac_ctrl_t *const p_ctrl)
```

Stop the D/A conversion and disable the output signal.

**Return values**

FSP_SUCCESS	The control is successfully stopped.
FSP_ERR_ASSERTION	p_ctrl is NULL.
FSP_ERR_NOT_OPEN	Channel associated with p_instance_ctrl has not been opened.

**◆ R\_DAC8\_VersionGet()**

```
fsp_err_t R_DAC8_VersionGet ( fsp_version_t * p_version)
```

Get version and store it in provided pointer p\_version.

**Return values**

FSP_SUCCESS	Successfully retrieved version information.
FSP_ERR_ASSERTION	p_version is NULL.

**4.2.13 Direct Memory Access Controller (r\_dmac)**

## Modules

**Functions**

```
fsp_err_t R_DMAC_Open (transfer_ctrl_t *const p_api_ctrl, transfer_cfg_t const *const p_cfg)
```

```
fsp_err_t R_DMAC_Reconfigure (transfer_ctrl_t *const p_api_ctrl, transfer_info_t *p_info)
```

```
fsp_err_t R_DMAC_Reset (transfer_ctrl_t *const p_api_ctrl, void const *volatile p_src, void *volatile p_dest, uint16_t const num_transfers)
```

```
fsp_err_t R_DMAC_SoftwareStart (transfer_ctrl_t *const p_api_ctrl, transfer_start_mode_t mode)
```

```
fsp_err_t R_DMAC_SoftwareStop (transfer_ctrl_t *const p_api_ctrl)
```

```
fsp_err_t R_DMAC_Enable (transfer_ctrl_t *const p_api_ctrl)
```

```
fsp_err_t R_DMAC_Disable (transfer_ctrl_t *const p_api_ctrl)
```

```
fsp_err_t R_DMAC_InfoGet (transfer_ctrl_t *const p_api_ctrl, transfer_properties_t *const p_info)
```

```
fsp_err_t R_DMAC_Close (transfer_ctrl_t *const p_api_ctrl)
```

```
fsp_err_t R_DMAC_VersionGet (fsp_version_t *const p_version)
```

**Detailed Description**

Driver for the DMAC peripheral on RA MCUs. This module implements the [Transfer Interface](#).

## Overview

The Direct Memory Access Controller (DMAC) transfers data from one memory location to another without using the CPU.

### Features

- Supports multiple transfer modes
  - Normal transfer
  - Repeat transfer
  - Block transfer
- Address increment, decrement, fixed, or offset modes
- Triggered by ELC events
  - Some exceptions apply, see the Event table in the Event Numbers section of the Interrupt Controller Unit chapter of the hardware manual
- Supports 1, 2, and 4 byte data units

## Configuration

### Build Time Configurations for r\_dmac

The following build time configurations are defined in fsp\_cfg/r\_dmac\_cfg.h:

Configuration	Options	Default	Description
Parameter Checking	<ul style="list-style-type: none"> <li>• Default (BSP)</li> <li>• Enabled</li> <li>• Disabled</li> </ul>	Default (BSP)	If selected code for parameter checking is included in the build.

### Configurations for Driver > Transfer > Transfer Driver on r\_dmac

This module can be added to the Stacks tab via New Stack > Driver > Transfer > Transfer Driver on r\_dmac .

Configuration	Options	Default	Description
Name	Name must be a valid C symbol	g_transfer0	Module name.
Channel	Value must be a non-negative integer	0	Specify the hardware channel.
Mode	<ul style="list-style-type: none"> <li>• Normal</li> <li>• Repeat</li> <li>• Block</li> </ul>	Normal	Select the transfer mode. Normal: One transfer per activation, transfer ends after Number of Transfers; Repeat: One transfer per activation, Repeat Area address reset after Number of Transfers, transfer ends after Number of

			Blocks; Block: Number of Blocks per activation, Repeat Area address reset after Number of Transfers, transfer ends after Number of Blocks.
Transfer Size	<ul style="list-style-type: none"> <li>• 1 Byte</li> <li>• 2 Bytes</li> <li>• 4 Bytes</li> </ul>	2 Bytes	Select the transfer size.
Destination Address Mode	<ul style="list-style-type: none"> <li>• Fixed</li> <li>• Offset addition</li> <li>• Incremented</li> <li>• Decrementd</li> </ul>	Fixed	Select the address mode for the destination.
Source Address Mode	<ul style="list-style-type: none"> <li>• Fixed</li> <li>• Offset addition</li> <li>• Incremented</li> <li>• Decrementd</li> </ul>	Fixed	Select the address mode for the source.
Repeat Area (Unused in Normal Mode)	<ul style="list-style-type: none"> <li>• Destination</li> <li>• Source</li> </ul>	Source	Select the repeat area. Either the source or destination address resets to its initial value after completing Number of Transfers in Repeat or Block mode.
Destination Pointer	Manual Entry	NULL	Specify the transfer destination pointer.
Source Pointer	Manual Entry	NULL	Specify the transfer source pointer.
Number of Transfers	Value must be a non-negative integer	1	Specify the number of transfers.
Number of Blocks (Valid only in Repeat and Block Mode)	Value must be a non-negative integer	0	Specify the number of blocks to transfer in Repeat or Block mode.
Activation Source	MCU Specific Options		Select the DMAC transfer start event. If no ELC event is chosen then software start can be used.
Callback	Name must be a valid C symbol	NULL	A user callback that is called at the end of the transfer.
Context	Manual Entry	NULL	Pointer to the context structure passed through the callback argument.
Transfer End Interrupt	MCU Specific Options		Select the transfer end

Priority			interrupt priority.
Interrupt Frequency	<ul style="list-style-type: none"> <li>Interrupt after all transfers have completed</li> <li>Interrupt after each block, or repeat size is transferred</li> </ul>	Interrupt after all transfers have completed	Select to have interrupt after each transfer or after last transfer.
Offset value (Valid only when address mode is '\Offset\')	Value must be a 24 bit signed integer.	1	Offset value is added to the address after each transfer.

## Clock Configuration

The DMAC peripheral module uses ICLK as the clock source. The ICLK frequency is set by using the **Clocks** tab of the RA Configuration editor prior to a build, or by using the CGC module at run-time.

## Pin Configuration

This module does not use I/O pins.

# Usage Notes

## Transfer Modes

The DMAC Module supports three modes of operation.

- **Normal Mode** - In normal mode, a single data unit is transferred every time the configured ELC event is received by the DMAC channel. A data unit can be 1-byte, 2-bytes, or 4-bytes. The source and destination addresses can be fixed, increment, decrement, or add an offset to the next data unit after each transfer. A 16-bit counter decrements after each transfer. When the counter reaches 0, transfers will no longer be triggered by the ELC event and the CPU can be interrupted to signal that all transfers have finished.
- **Repeat Mode** - Repeat mode works the same way as normal mode, however the length is limited to an integer in the range[1,1024]. When the transfer counter reaches 0, the counter is reset to its configured value, the repeat area (source or destination address) resets to its starting address and the block count remaining will decrement by 1. When the block count reaches 0, transfers will no longer be triggered by the ELC event and the CPU may be interrupted to signal that all transfers have finished.
- **Block Mode** - In block mode, the amount of data units transferred by each interrupt can be set to an integer in the range [1,1024]. The number of blocks to transfer can also be configured to a 16-bit number. After each block transfer the repeat area (source or destination address) will reset to the original address and the other address will be incremented or decremented to the next block.

## Selecting the DTC or DMAC

The Transfer API is implemented by both DTC and the DMAC so that applications can switch between the DTC and the DMAC. When selecting between them, consider these factors:

	DTC	DMAC
Repeat Mode	<ul style="list-style-type: none"> <li>Repeats forever</li> </ul>	<ul style="list-style-type: none"> <li>Configurable number of</li> </ul>



	<ul style="list-style-type: none"> <li>• Max repeat size is 256 x 4 bytes</li> </ul>	<ul style="list-style-type: none"> <li>• repeats</li> <li>• Max repeat size is 1024 x 4 bytes</li> </ul>
Block Mode	<ul style="list-style-type: none"> <li>• Max block size is 256 x 4 bytes</li> </ul>	<ul style="list-style-type: none"> <li>• Max block size is 1024 x 4 bytes</li> </ul>
Channels	<ul style="list-style-type: none"> <li>• One instance per interrupt</li> </ul>	<ul style="list-style-type: none"> <li>• MCU specific (8 channels or less)</li> </ul>
Chained Transfers	<ul style="list-style-type: none"> <li>• Supported</li> </ul>	<ul style="list-style-type: none"> <li>• Not Supported</li> </ul>
Software Trigger	<ul style="list-style-type: none"> <li>• Must use the software ELC event</li> </ul>	<ul style="list-style-type: none"> <li>• Has support for software trigger without using software ELC event</li> <li>• Supports TRANSFER_START_MODE_SINGLE and TRANSFER_START_MODE_REPEAT</li> </ul>
Offset Address Mode	<ul style="list-style-type: none"> <li>• Not supported</li> </ul>	<ul style="list-style-type: none"> <li>• Supported</li> </ul>

## Interrupts

The DTC and DMAC interrupts behave differently. The DTC uses the configured IELSR event IRQ as the interrupt source whereas each DMAC channel has its own IRQ.

The `transfer_info_t::irq` setting also behaves a little differently depending on which mode is selected.

## Normal Mode

	DTC	DMAC
TRANSFER_IRQ_EACH	Interrupt after each transfer	N/A
TRANSFER_IRQ_END	Interrupt after last transfer	Interrupt after last transfer

## Repeat Mode

	DTC	DMAC
TRANSFER_IRQ_EACH	Interrupt after each transfer	Interrupt after each repeat
TRANSFER_IRQ_END	Interrupt after each repeat	Interrupt after last transfer

## Block Mode

	DTC	DMAC
TRANSFER_IRQ_EACH	Interrupt after each block	Interrupt after each block
TRANSFER_IRQ_END	Interrupt after last block	Interrupt after last block

## Additional Considerations

- The DTC requires a moderate amount of RAM (one `transfer_info_t` struct per open instance + `DTC_VECTOR_TABLE_SIZE`).
- The DTC stores transfer information in RAM and writes back to RAM after each transfer

whereas the DMAC stores all transfer information in registers.

- When transfers are configured for more than one activation source, the DTC must fetch the transfer info from RAM on each interrupt. This can cause a higher latency between transfers.

## Offset Address Mode

When the source or destination mode is configured to offset mode, a configurable offset is added to the source or destination pointer after each transfer. The offset is a signed 24 bit number.

## Examples

### Basic Example

This is a basic example of minimal use of the DMAC in an application. In this case, one or more events have been routed to the DMAC for handling so it only needs to be enabled to start accepting transfers.

```
void dmac_minimal_example (void)
{
    /* Open the transfer instance with initial configuration. */
    fsp_err_t err = R_DMAC_Open(&g_transfer_ctrl, &g_transfer_cfg);
    /* Handle any errors. This function should be defined by the user. */
    handle_error(err);
    /* Enable the DMAC so that it responds to transfer requests. */
    err = R_DMAC_Enable(&g_transfer_ctrl);
    handle_error(err);
}
```

### CRC32 Example

In this example the DMAC is used to feed the CRC peripheral to perform a CRC32 operation.

```
volatile bool g_transfer_complete = false;
void dmac_callback (dmac_callback_args_t * cb_data)
{
    FSP_PARAMETER_NOT_USED(cb_data);
    g_transfer_complete = true;
}
void dmac_crc_example (void)
{
```

```
uint8_t p_src[TRANSFER_LENGTH];
/* Initialize p_src to [ABC..OP] */
for (uint32_t i = 0; i < TRANSFER_LENGTH; i++)
{
    p_src[i] = (uint8_t) ('A' + (i % 26));
}
/* Set transfer source address to p_src */
g_transfer_cfg.p_info->p_src = (void *) p_src;
/* Set transfer destination address to the CRC data input register */
g_transfer_cfg.p_info->p_dest = (void *) &R_CRC->CRCDIR;
/* Open the transfer instance with initial configuration. */
fsp_err_t err = R_DMAC_Open(&g_transfer_ctrl, &g_transfer_cfg);
/* Handle any errors. This function should be defined by the user. */
handle_error(err);
/* Enable DMAC transfers. */
(void) R_DMAC_Enable(&g_transfer_ctrl);
/* Open the CRC module. */
err = R_CRC_Open(&g_crc_ctrl, &g_crc_cfg);
handle_error(err);
/* Clear the transfer complete flag. */
g_transfer_complete = false;
/* Trigger the transfer using software. */
err = R_DMAC_SoftwareStart(&g_transfer_ctrl, TRANSFER_START_MODE_SINGLE);
handle_error(err);
while (!g_transfer_complete)
{
    /* Wait for transfer complete interrupt */
}
/* Get CRC result and perform final XOR. */
uint32_t crc32;
(void) R_CRC_CalculatedValueGet(&g_crc_ctrl, &crc32);
crc32 ^= CRC32_FINAL_XOR_VALUE;
/* Verify that the CRC32 is calculated correctly. */
/* CRC32("ABCD...NOP") = 0xE0E8FF4D. */
```

```

const uint32_t expected_crc32 = 0xE0E8FF4D;
if (expected_crc32 != crc32)
{
/* Handle any CRC errors. This function should be defined by the user. */
    handle_crc_error();
}
}

```

## Data Structures

struct [dmac\\_instance\\_ctrl\\_t](#)

struct [dmac\\_callback\\_args\\_t](#)

struct [dmac\\_extended\\_cfg\\_t](#)

## Macros

#define [DMAC\\_MAX\\_NORMAL\\_TRANSFER\\_LENGTH](#)

#define [DMAC\\_MAX\\_REPEAT\\_TRANSFER\\_LENGTH](#)

#define [DMAC\\_MAX\\_BLOCK\\_TRANSFER\\_LENGTH](#)

#define [DMAC\\_MAX\\_REPEAT\\_COUNT](#)

#define [DMAC\\_MAX\\_BLOCK\\_COUNT](#)

## Data Structure Documentation

### ◆ [dmac\\_instance\\_ctrl\\_t](#)

struct [dmac\\_instance\\_ctrl\\_t](#)

Control block used by driver. DO NOT INITIALIZE - this structure will be initialized in [transfer\\_api\\_t::open](#).

### ◆ [dmac\\_callback\\_args\\_t](#)

struct [dmac\\_callback\\_args\\_t](#)

Callback function parameter data.

#### Data Fields

void const \*

[p\\_context](#)

Placeholder for user data. Set in [r\\_transfer\\_t::open](#) function in [transfer\\_cfg\\_t](#).

### ◆ [dmac\\_extended\\_cfg\\_t](#)

struct dmac_extended_cfg_t	
DMAC transfer configuration extension. This extension is required.	
<b>Data Fields</b>	
uint8_t	channel
	Channel number, does not apply to all HAL drivers.
IRQn_Type	irq
	DMAC interrupt number.
uint8_t	ipl
	DMAC interrupt priority.
int32_t	offset
	Offset value used with transfer_addr_mode_t::TRANSFER_ADDR_MODE_OFFSET.
elc_event_t	activation_source
void(*	p_callback)(dmac_callback_args_t *cb_data)
void const *	p_context
<b>Field Documentation</b>	
◆ <b>activation_source</b>	
elc_event_t dmac_extended_cfg_t::activation_source	
Select which event will trigger the transfer.	
<i>Note</i>	
<i>Select ELC_EVENT_NONE for software activation in order to use softwareStart and softwareStart to trigger transfers.</i>	

**◆ p\_callback**

```
void(* dmac_extended_cfg_t::p_callback) (dmac_callback_args_t *cb_data)
```

Callback for transfer end interrupt.

**◆ p\_context**

```
void const* dmac_extended_cfg_t::p_context
```

Placeholder for user data. Passed to the user p\_callback in [dmac\\_callback\\_args\\_t](#).

**Macro Definition Documentation****◆ DMAC\_MAX\_NORMAL\_TRANSFER\_LENGTH**

```
#define DMAC_MAX_NORMAL_TRANSFER_LENGTH
```

Max configurable number of transfers in TRANSFER\_MODE\_NORMAL.

**◆ DMAC\_MAX\_REPEAT\_TRANSFER\_LENGTH**

```
#define DMAC_MAX_REPEAT_TRANSFER_LENGTH
```

Max number of transfers per repeat for TRANSFER\_MODE\_REPEAT.

**◆ DMAC\_MAX\_BLOCK\_TRANSFER\_LENGTH**

```
#define DMAC_MAX_BLOCK_TRANSFER_LENGTH
```

Max number of transfers per block in TRANSFER\_MODE\_BLOCK

**◆ DMAC\_MAX\_REPEAT\_COUNT**

```
#define DMAC_MAX_REPEAT_COUNT
```

Max configurable number of repeats to transfer in TRANSFER\_MODE\_REPEAT

**◆ DMAC\_MAX\_BLOCK\_COUNT**

```
#define DMAC_MAX_BLOCK_COUNT
```

Max configurable number of blocks to transfer in TRANSFER\_MODE\_BLOCK

**Function Documentation**

◆ **R\_DMAM\_Open()**

```
fsp_err_t R_DMAM_Open ( transfer_ctrl_t *const p_api_ctrl, transfer_cfg_t const *const p_cfg )
```

Configure a DMAM channel.

**Return values**

FSP_SUCCESS	Successful open.
FSP_ERR_ASSERTION	An input parameter is invalid.
FSP_ERR_IP_CHANNEL_NOT_PRESENT	The configured channel is invalid.
FSP_ERR_IRQ_BSP_DISABLED	The IRQ associated with the activation source is not enabled in the BSP.
FSP_ERR_ALREADY_OPEN	The control structure is already opened.

◆ **R\_DMAM\_Reconfigure()**

```
fsp_err_t R_DMAM_Reconfigure ( transfer_ctrl_t *const p_api_ctrl, transfer_info_t * p_info )
```

Reconfigure the transfer with new transfer info.

**Return values**

FSP_SUCCESS	Transfer is configured and will start when trigger occurs.
FSP_ERR_ASSERTION	An input parameter is invalid.
FSP_ERR_NOT_ENABLED	DMAM is not enabled. The current configuration must not be valid.
FSP_ERR_NOT_OPEN	Handle is not initialized. Call R_DMAM_Open to initialize the control block.

◆ **R\_DMAM\_Reset()**

```
fsp_err_t R_DMAM_Reset ( transfer_ctrl_t *const p_api_ctrl, void const *volatile p_src, void *volatile p_dest, uint16_t const num_transfers )
```

Reset transfer source, destination, and number of transfers.

**Return values**

FSP_SUCCESS	Transfer reset successfully.
FSP_ERR_ASSERTION	An input parameter is invalid.
FSP_ERR_NOT_ENABLED	DMAC is not enabled. The current configuration must not be valid.
FSP_ERR_NOT_OPEN	Handle is not initialized. Call R_DMAM_Open to initialize the control block.

◆ **R\_DMAM\_SoftwareStart()**

```
fsp_err_t R_DMAM_SoftwareStart ( transfer_ctrl_t *const p_api_ctrl, transfer_start_mode_t mode )
```

If the mode is TRANSFER\_START\_MODE\_SINGLE initiate a single transfer with software. If the mode is TRANSFER\_START\_MODE\_REPEAT continue triggering transfers until all of the transfers are completed.

**Return values**

FSP_SUCCESS	Transfer started written successfully.
FSP_ERR_ASSERTION	An input parameter is invalid.
FSP_ERR_NOT_OPEN	Handle is not initialized. Call R_DMAM_Open to initialize the control block.
FSP_ERR_UNSUPPORTED	Handle was not configured for software activation.



◆ **R\_DMAC\_SoftwareStop()**

`fsp_err_t R_DMAC_SoftwareStop ( transfer_ctrl_t *const p_api_ctrl)`

Stop software transfers if they were started with TRANSFER\_START\_MODE\_REPEAT.

**Return values**

FSP_SUCCESS	Transfer stopped written successfully.
FSP_ERR_ASSERTION	An input parameter is invalid.
FSP_ERR_NOT_OPEN	Handle is not initialized. Call R_DMAC_Open to initialize the control block.

◆ **R\_DMAC\_Enable()**

`fsp_err_t R_DMAC_Enable ( transfer_ctrl_t *const p_api_ctrl)`

Enable transfers for the configured activation source.

**Return values**

FSP_SUCCESS	Counter value written successfully.
FSP_ERR_ASSERTION	An input parameter is invalid.
FSP_ERR_NOT_OPEN	Handle is not initialized. Call R_DMAC_Open to initialize the control block.

◆ **R\_DMAC\_Disable()**

`fsp_err_t R_DMAC_Disable ( transfer_ctrl_t *const p_api_ctrl)`

Disable transfers so that they are no longer triggered by the activation source.

**Return values**

FSP_SUCCESS	Counter value written successfully.
FSP_ERR_ASSERTION	An input parameter is invalid.
FSP_ERR_NOT_OPEN	Handle is not initialized. Call R_DMAC_Open to initialize the control block.

◆ **R\_DMAC\_InfoGet()**

```
fsp_err_t R_DMAC_InfoGet ( transfer_ctrl_t *const p_api_ctrl, transfer_properties_t *const p_info )
```

Set driver specific information in provided pointer.

**Return values**

FSP_SUCCESS	Information has been written to p_info.
FSP_ERR_NOT_OPEN	Handle is not initialized. Call R_DMAC_Open to initialize the control block.
FSP_ERR_ASSERTION	An input parameter is invalid.

◆ **R\_DMAC\_Close()**

```
fsp_err_t R_DMAC_Close ( transfer_ctrl_t *const p_api_ctrl)
```

Disable transfer and clean up internal data. Implements `transfer_api_t::close`.

**Return values**

FSP_SUCCESS	Successful close.
FSP_ERR_ASSERTION	An input parameter is invalid.
FSP_ERR_NOT_OPEN	Handle is not initialized. Call R_DMAC_Open to initialize the control block.

◆ **R\_DMAC\_VersionGet()**

```
fsp_err_t R_DMAC_VersionGet ( fsp_version_t *const p_version)
```

Set driver version based on compile time macros.

**Return values**

FSP_SUCCESS	Successful close.
FSP_ERR_ASSERTION	An input parameter is invalid.

**4.2.14 Data Operation Circuit (r\_doc)**

Modules

## Functions

`fsp_err_t` `R_DOC_Open` (`doc_ctrl_t *const p_api_ctrl`, `doc_cfg_t const *const p_cfg`)

`fsp_err_t` `R_DOC_Close` (`doc_ctrl_t *const p_api_ctrl`)

`fsp_err_t` `R_DOC_StatusGet` (`doc_ctrl_t *const p_api_ctrl`, `doc_status_t *const p_status`)

`fsp_err_t` `R_DOC_Write` (`doc_ctrl_t *const p_api_ctrl`, `uint16_t data`)

`fsp_err_t` `R_DOC_VersionGet` (`fsp_version_t *const p_version`)

`fsp_err_t` `R_DOC_CallbackSet` (`doc_ctrl_t *const p_api_ctrl`, `void(*p_callback)(doc_callback_args_t *)`, `void const *const p_context`, `doc_callback_args_t *const p_callback_memory`)

## Detailed Description

Driver for the DOC peripheral on RA MCUs. This module implements the [DOC Interface](#).

## Overview

### Features

The DOC HAL module peripheral is used to compare, add or subtract 16-bit data and can detect the following events:

- A match or mismatch between data values
- Overflow of an addition operation
- Underflow of a subtraction operation

A user-defined callback can be created to inform the CPU when any of above events occur.

## Configuration

### Build Time Configurations for r\_doc

The following build time configurations are defined in `fsp_cfg/r_doc_cfg.h`:

Configuration	Options	Default	Description
Parameter Checking	<ul style="list-style-type: none"> <li>• Default (BSP)</li> <li>• Enabled</li> <li>• Disabled</li> </ul>	Default (BSP)	If selected code for parameter checking is included in the build.

### Configurations for Driver > Monitoring > Data Operation Circuit Driver on r\_doc

This module can be added to the Stacks tab via New Stack > Driver > Monitoring > Data Operation Circuit Driver on r\_doc. Non-secure callable guard functions can be generated for this module by

right clicking the module in the RA Configuration tool and checking the "Non-secure Callable" box.

Configuration	Options	Default	Description
Name	Name must be a valid C symbol	g_doc0	Module name.
Event	<ul style="list-style-type: none"> <li>• Comparison mismatch</li> <li>• Comparison match</li> <li>• Addition overflow</li> <li>• Subtraction underflow</li> </ul>	Comparison mismatch	Select the event that will trigger the DOC interrupt.
Reference/Initial Data	Value must be a 16 bit integer between 0 and 65535	0	Enter Initial Value for Addition/Subtraction or enter reference value for comparison.
Callback	Name must be a valid C symbol	NULL	A user callback function must be provided. This will be called from the interrupt service routine (ISR) when the configured DOC event occurs.
DOC Interrupt Priority	MCU Specific Options		Select the DOC interrupt priority.

## Clock Configuration

The DOC HAL module does not require a specific clock configuration.

## Pin Configuration

The DOC HAL module does not require and specific pin configurations.

## Usage Notes

### DMAC/DTC Integration

DOC can be used with [Direct Memory Access Controller \(r\\_dmac\)](#) or [Data Transfer Controller \(r\\_dtc\)](#) to write to the input register without CPU intervention. DMAC is more useful for most DOC applications because it can be started directly from software. To write DOC input data with DTC/DMAC, set `transfer_info_t::p_dest` to `R_DOC->DODIR`.

## Examples

### Basic Example

This is a basic example of minimal use of the R\_DOC in an application. This example shows how this

driver can be used for continuous 16 bit addition operation while reading the result at every overflow event.

```
#define DOC_EXAMPLE_VALUE 0xF000
uint32_t g_callback_event_counter = 0;
/* This callback is called when DOC overflow event occurs. It is registered in
doc_cfg_t when R_DOC_Open is
 * called. */
void doc_callback (doc_callback_args_t * p_args)
{
    FSP_PARAMETER_NOT_USED(p_args);
    g_callback_event_counter++;
}
void basic_example (void)
{
    fsp_err_t    err;
    doc_status_t result;
    /* Initialize the DOC module for addition with initial value specified in
doc_cfg_t::doc_data. */
    err = R_DOC_Open(&g_doc_ctrl, &g_doc_cfg);
    /* Handle any errors. This function should be defined by the user. */
    handle_error(err);
    /* Write data to the DOC Data Input Register and read the result of addition from
status register when an
 * interrupt occurs. */
    for (int i = 0; i < 5; i++)
    {
        err = R_DOC_Write(&g_doc_ctrl, DOC_EXAMPLE_VALUE);
        handle_error(err);
    }
    if (g_callback_event_counter >= 1)
    {
        /* Read the result of the operation */
        err = R_DOC_StatusGet(&g_doc_ctrl, &result);
        handle_error(err);
    }
}
```

```

}
}

```

## Function Documentation

### ◆ R\_DOC\_Open()

```
fsp_err_t R_DOC_Open ( doc_ctrl_t *const p_api_ctrl, doc_cfg_t const *const p_cfg )
```

Opens and configures the Data Operation Circuit (DOC) in comparison, addition or subtraction mode and sets initial data for addition or subtraction, or reference data for comparison.

Example:

```

/* Initialize the DOC module for addition with initial value specified in
doc_cfg_t::doc_data. */
err = R_DOC_Open(&g_doc_ctrl, &g_doc_cfg);

```

#### Return values

FSP_SUCCESS	DOC successfully configured.
FSP_ERR_ALREADY_OPEN	Module already open.
FSP_ERR_ASSERTION	One or more pointers point to NULL or callback is NULL or the interrupt vector is invalid.

### ◆ R\_DOC\_Close()

```
fsp_err_t R_DOC_Close ( doc_ctrl_t *const p_api_ctrl)
```

Closes the module driver. Enables module stop mode.

#### Return values

FSP_SUCCESS	Module successfully closed.
FSP_ERR_NOT_OPEN	Driver not open.
FSP_ERR_ASSERTION	Pointer pointing to NULL.

#### Note

*This function will disable the DOC interrupt in the NVIC.*

◆ **R\_DOC\_StatusGet()**

```
fsp_err_t R_DOC_StatusGet ( doc_ctrl_t*const p_api_ctrl, doc_status_t*const p_status )
```

Returns the result of addition/subtraction.

Example:

```
/* Read the result of the operation */
    err = R_DOC_StatusGet(&g_doc_ctrl, &result);
    handle_error(err);
```

**Return values**

FSP_SUCCESS	Status successfully read.
FSP_ERR_NOT_OPEN	Driver not open.
FSP_ERR_ASSERTION	One or more pointers point to NULL.

◆ **R\_DOC\_Write()**

```
fsp_err_t R_DOC_Write ( doc_ctrl_t*const p_api_ctrl, uint16_t data )
```

Writes to the DODIR - DOC Input Register.

Example:

```
err = R_DOC_Write(&g_doc_ctrl, DOC_EXAMPLE_VALUE);
    handle_error(err);
```

**Return values**

FSP_SUCCESS	Values successfully written to the registers.
FSP_ERR_NOT_OPEN	Driver not open.
FSP_ERR_ASSERTION	One or more pointers point to NULL.

◆ **R\_DOC\_VersionGet()**

```
fsp_err_t R_DOC_VersionGet ( fsp_version_t*const p_version)
```

Returns DOC HAL driver version.

**Return values**

FSP_SUCCESS	Version information successfully read.
FSP_ERR_ASSERTION	Pointer pointing to NULL.

### ◆ R\_DOC\_CallbackSet()

```
fsp_err_t R_DOC_CallbackSet ( doc_ctrl_t *const p_api_ctrl, void (*)(doc_callback_args_t *)
p_callback, void const *const p_context, doc_callback_args_t *const p_callback_memory )
```

Updates the user callback and has option of providing memory for callback structure. Implements `doc_api_t::callbackSet`

#### Return values

FSP_SUCCESS	Callback updated successfully.
FSP_ERR_ASSERTION	A required pointer is NULL.
FSP_ERR_NOT_OPEN	The control block has not been opened.

## 4.2.15 D/AVE 2D Port Interface (r\_drw)

### Modules

Driver for the DRW peripheral on RA MCUs. This module is a port of D/AVE 2D.

## Overview

### Note

*The D/AVE 2D Port Interface (D1 layer) is a HAL layer for the D/AVE D2 layer API and does not provide any interfaces to the user. Consult the [TES Dave2D Driver Documentation](#) for further information on using the D2 API.*

*For cross-platform compatibility purposes the D1 and D2 APIs are not bound by the FSP coding guidelines for function names and general module functionality.*

## Configuration

### Build Time Configurations for r\_drw

The following build time configurations are defined in `fsp_cfg/r_drw_cfg.h`:

Configuration	Options	Default	Description
Allow Indirect Mode	<ul style="list-style-type: none"> <li>Enabled</li> <li>Disabled</li> </ul>	Enabled	Enable indirect mode to allow no-copy mode for <code>d2_adddlist</code> (see the <a href="#">TES Dave2D Driver Documentation</a> for details).



Memory Allocation	<ul style="list-style-type: none"> <li>• Default</li> <li>• Custom</li> </ul>	Default	<p>Set Memory Allocation to Default to use built-in dynamic memory allocation for the D2 heap. This will use an RTOS heap if configured; otherwise, standard C malloc and free will be used.</p> <p>Set to Custom to define your own allocation scheme for the D2 heap. In this case, the developer will need to define the following functions:</p> <pre>void * d1_malloc(size_t size) void d1_free(void * ptr)</pre>
-------------------	-------------------------------------------------------------------------------	---------	------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------

### Configurations for Driver > Graphics > D/AVE 2D Port Interface on r\_drw

This module can be added to the Stacks tab via New Stack > Driver > Graphics > D/AVE 2D Port Interface on r\_drw.

Configuration	Options	Default	Description
D2 Device Handle Name	Name must be a valid C symbol	d2_handle0	Set the name for the d2_device handle used when calling D2 layer functions.
DRW Interrupt Priority	MCU Specific Options		Select the DRW_INT (display list completion) interrupt priority.

### Heap Size

The D1 port layer allows the D2 driver to allocate memory as needed. There are three ways the driver can accomplish this:

1. Allocate memory using the main heap
2. Allocate memory using a heap provided by an RTOS
3. Allocate memory via user-provided functions

When the "Memory Allocation" configuration option is set to "Default" the driver will use an RTOS implementation if available and the main heap otherwise. Setting the option to "Custom" allows the user to define their own scheme using the following prototypes:

```
void * d1_malloc(size_t size);
void d1_free(void * ptr);
```

### Warning

If there is no RTOS-based allocation scheme the main heap will be used. Be sure that it is enabled by setting the "Heap size (bytes)" property under RA Common on the **BSP** tab of the RA Configuration editor.

### Note

*It is recommended to add 32KB of additional heap space for the D2 driver until the actual usage can be determined in your application.*

### Interrupt

The D1 port includes one interrupt to handle various events like display list completion or bus error. This interrupt is managed internally by the D2 driver and no callback function is available.

## Usage Notes

### Limitations

Developers should be aware of the following limitations when using the DRW engine:

- The DRW module supports two additional interrupt types - bus error and render complete. These interrupts are not needed for D2 layer operation and thus are not supported.
- If the DRW module is stopped during rendering the render will continue once the module is started again. If this behavior is undesirable in your application it is recommended to call `d2_flushframe` before stopping the peripheral.

### 4.2.16 Data Transfer Controller (r\_dtc)

#### Modules

#### Functions

fsp_err_t	R_DTC_Open (transfer_ctrl_t *const p_api_ctrl, transfer_cfg_t const *const p_cfg)
-----------	-----------------------------------------------------------------------------------

fsp_err_t	R_DTC_Reconfigure (transfer_ctrl_t *const p_api_ctrl, transfer_info_t *p_info)
-----------	--------------------------------------------------------------------------------

fsp_err_t	R_DTC_Reset (transfer_ctrl_t *const p_api_ctrl, void const *volatile p_src, void *volatile p_dest, uint16_t const num_transfers)
-----------	----------------------------------------------------------------------------------------------------------------------------------

fsp_err_t	R_DTC_SoftwareStart (transfer_ctrl_t *const p_api_ctrl, transfer_start_mode_t mode)
-----------	-------------------------------------------------------------------------------------

fsp_err_t	R_DTC_SoftwareStop (transfer_ctrl_t *const p_api_ctrl)
-----------	--------------------------------------------------------

fsp_err_t	R_DTC_Enable (transfer_ctrl_t *const p_api_ctrl)
-----------	--------------------------------------------------

```
fsp_err_t R_DTC_Disable (transfer_ctrl_t *const p_api_ctrl)
```

```
fsp_err_t R_DTC_InfoGet (transfer_ctrl_t *const p_api_ctrl, transfer_properties_t *const p_properties)
```

```
fsp_err_t R_DTC_Close (transfer_ctrl_t *const p_api_ctrl)
```

```
fsp_err_t R_DTC_VersionGet (fsp_version_t *const p_version)
```

## Detailed Description

Driver for the DTC peripheral on RA MCUs. This module implements the [Transfer Interface](#).

## Overview

The Data Transfer Controller (DTC) transfers data from one memory location to another without using the CPU.

The DTC uses a RAM based vector table. Each entry in the vector table corresponds to an entry in the ISR vector table. When the DTC is triggered by an interrupt, it reads the DTC vector table, fetches the transfer information, and then executes the transfer. After the transfer is executed, the DTC writes the updated transfer info back to the location pointed to by the DTC vector table.

## Features

- Supports multiple transfer modes
  - Normal transfer
  - Repeat transfer
  - Block transfer
- Chain transfers
- Address increment, decrement or fixed modes
- Can be triggered by any event that has reserved a slot in the interrupt vector table.
  - Some exceptions apply, see the Event table in the Event Numbers section of the Interrupt Controller Unit chapter of the hardware manual
- Supports 1, 2, and 4 byte data units

## Configuration

### Build Time Configurations for r\_dtc

The following build time configurations are defined in fsp\_cfg/r\_dtc\_cfg.h:

Configuration	Options	Default	Description
Parameter Checking	<ul style="list-style-type: none"> <li>• Default (BSP)</li> <li>• Enabled</li> <li>• Disabled</li> </ul>	Default (BSP)	If selected code for parameter checking is included in the build.
Linker section to keep DTC vector table	Manual Entry	.fsp_dtc_vector_table	Section to place the DTC vector table.

**Configurations for Driver > Transfer > Transfer Driver on r\_dtc**

This module can be added to the Stacks tab via New Stack > Driver > Transfer > Transfer Driver on r\_dtc .

Configuration	Options	Default	Description
Name	Name must be a valid C symbol	g_transfer0	Module name.
Mode	<ul style="list-style-type: none"> <li>• Normal</li> <li>• Repeat</li> <li>• Block</li> </ul>	Normal	Select the transfer mode. Select the transfer mode. Normal: One transfer per activation, transfer ends after Number of Transfers; Repeat: One transfer per activation, Repeat Area address reset after Number of Transfers, transfer repeats until stopped; Block: Number of Blocks per activation, Repeat Area address reset after Number of Transfers, transfer ends after Number of Blocks.
Transfer Size	<ul style="list-style-type: none"> <li>• 1 Byte</li> <li>• 2 Bytes</li> <li>• 4 Bytes</li> </ul>	2 Bytes	Select the transfer size.
Destination Address Mode	<ul style="list-style-type: none"> <li>• Fixed</li> <li>• Incremented</li> <li>• Decrementd</li> </ul>	Fixed	Select the address mode for the destination.
Source Address Mode	<ul style="list-style-type: none"> <li>• Fixed</li> <li>• Incremented</li> <li>• Decrementd</li> </ul>	Fixed	Select the address mode for the source.
Repeat Area (Unused in Normal Mode)	<ul style="list-style-type: none"> <li>• Destination</li> <li>• Source</li> </ul>	Source	Select the repeat area. Either the source or destination address resets to its initial value after completing Number of Transfers in Repeat or Block mode.
Interrupt Frequency	<ul style="list-style-type: none"> <li>• After all transfers have completed</li> <li>• After each transfer</li> </ul>	After all transfers have completed	Select to have interrupt after each transfer or after last transfer.
Number of Transfers	Value must be a non-	0	Specify the number of

	negative integer		transfers.
Number of Blocks (Valid only in Block Mode)	Must be a valid non-negative integer with a maximum configurable value of 65536. Applicable only in Block Mode.	0	Specify the number of blocks to transfer in Block mode.
Activation Source	MCU Specific Options		Select the DTC transfer start event.

## Clock Configuration

The DTC peripheral module uses ICLK as the clock source. The ICLK frequency is set by using the **Clocks** tab of the RA Configuration editor prior to a build or by using the CGC module at runtime.

## Pin Configuration

This module does not use I/O pins.

# Usage Notes

## Transfer Modes

The DTC Module supports three modes of operation.

- **Normal Mode** - In normal mode, a single data unit is transferred every time an interrupt is received by the DTC. A data unit can be 1-byte, 2-bytes, or 4-bytes. The source and destination addresses can be fixed, increment or decrement to the next data unit after each transfer. A 16-bit counter (length) decrements after each transfer. When the counter reaches 0, transfers will no longer be triggered by the interrupt source and the CPU can be interrupted to signal that all transfers have finished.
- **Repeat Mode** - Repeat mode works the same way as normal mode, however the length is limited to an integer in the range[1,256]. When the transfer counter reaches 0, the counter is reset to its configured value and the repeat area (source or destination address) resets to its starting address and transfers will still be triggered by the interrupt.
- **Block Mode** - In block mode, the amount of data units transferred by each interrupt can be set to an integer in the range [1,256]. The number of blocks to transfer can also be configured to a 16-bit number. After each block transfer the repeat area (source or destination address) will reset to the original address and the other address will be incremented or decremented to the next block.

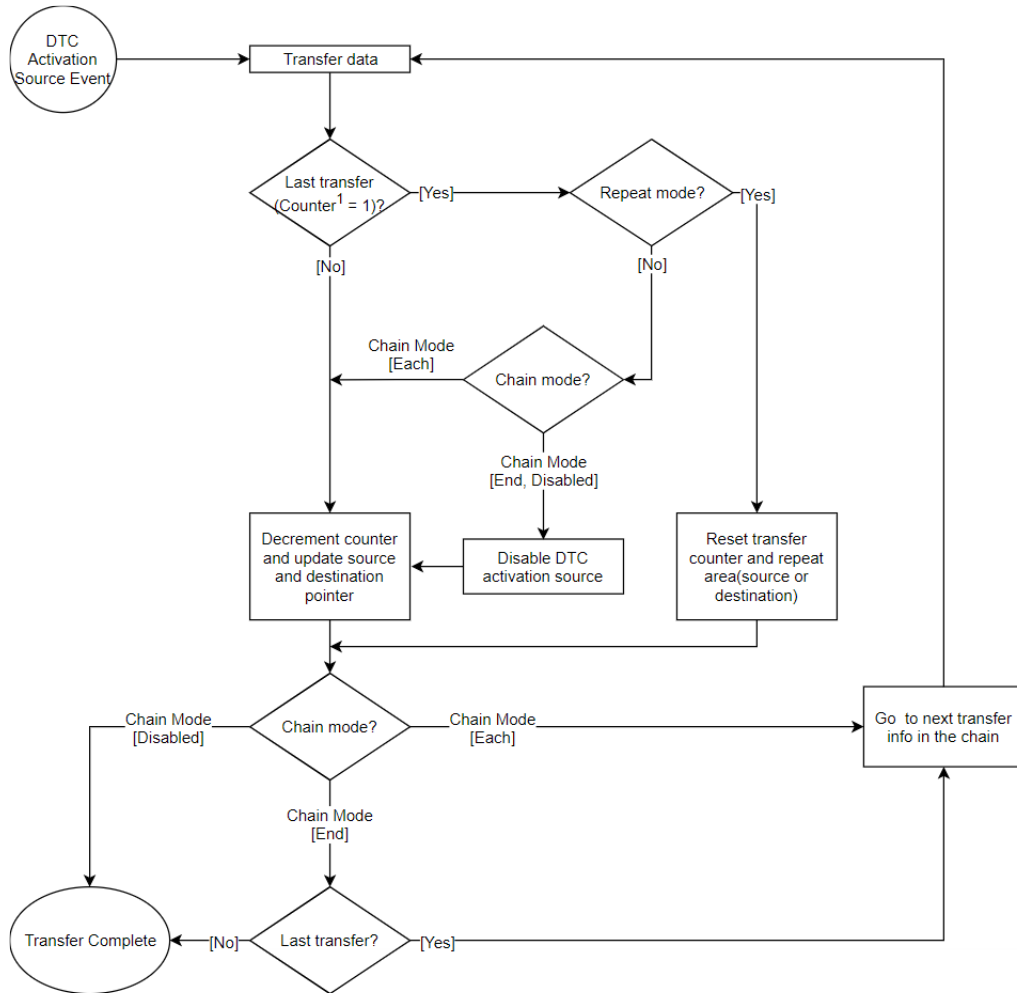
### Note

1. The source and destination address of the transfer must be aligned to the configured data unit.
2. In normal mode the length can be set to [0,65535]. When the length is set to 0, than the transaction will execute 65536 transfers not 0.
3. In block mode, num\_blocks can be set to [0,65535]. When the length is set to 0, than the transaction will execute 65536 transfers not 0.

## Chaining Transfers

Multiple transfers can be configured for the same interrupt source by specifying an array of `transfer_info_t` structs instead of just passing a pointer to one. In this configuration, every

`transfer_info_t` struct must be configured for a chain mode except for the last one. There are two types of chain mode; `CHAIN_MODE_EACH` and `CHAIN_MODE_END`. If a transfer is configured in `CHAIN_MODE_EACH` then it triggers the next transfer in the chain after it completes each transfer. If a transfer is configured in `CHAIN_MODE_END` then it triggers the next transfer in the chain after it completes its last transfer.



1. Counter refers to `transfer_info_t::length` in normal and repeat mode and `transfer_info_t::num_blocks` in block mode.

Figure 155: DTC Transfer Flowchart

### Selecting the DTC or DMAC

The Transfer API is implemented by both DTC and the DMAC so that applications can switch between the DTC and the DMAC. When selecting between them, consider these factors:

	DTC	DMAC
Repeat Mode	<ul style="list-style-type: none"> <li>Repeats forever</li> <li>Max repeat size is 256 x 4 bytes</li> </ul>	<ul style="list-style-type: none"> <li>Configurable number of repeats</li> <li>Max repeat size is 1024 x 4 bytes</li> </ul>
Block Mode	<ul style="list-style-type: none"> <li>Max block size is 256 x 4 bytes</li> </ul>	<ul style="list-style-type: none"> <li>Max block size is 1024 x 4 bytes</li> </ul>

Channels	<ul style="list-style-type: none"> <li>• One instance per interrupt</li> </ul>	<ul style="list-style-type: none"> <li>• MCU specific (8 channels or less)</li> </ul>
Chained Transfers	<ul style="list-style-type: none"> <li>• Supported</li> </ul>	<ul style="list-style-type: none"> <li>• Not Supported</li> </ul>
Software Trigger	<ul style="list-style-type: none"> <li>• Must use the software ELC event</li> </ul>	<ul style="list-style-type: none"> <li>• Has support for software trigger without using software ELC event</li> <li>• Supports TRANSFER_START_MODE_SINGLE and TRANSFER_START_MODE_REPEAT</li> </ul>
Offset Address Mode	<ul style="list-style-type: none"> <li>• Not supported</li> </ul>	<ul style="list-style-type: none"> <li>• Supported</li> </ul>

### Additional Considerations

- The DTC requires a moderate amount of RAM (one `transfer_info_t` struct per open instance + `DTC_VECTOR_TABLE_SIZE`).
- The DTC stores transfer information in RAM and writes back to RAM after each transfer whereas the DMAC stores all transfer information in registers.
- When transfers are configured for more than one activation source, the DTC must fetch the transfer info from RAM on each interrupt. This can cause a higher latency between transfers.
- The DTC interrupts the CPU using the activation source's IRQ. Each DMAC channel has its own IRQ.

### Interrupts

The DTC and DMAC interrupts behave differently. The DTC uses the configured IELSR event IRQ as the interrupt source whereas each DMAC channel has its own IRQ.

The `transfer_info_t::irq` setting also behaves a little differently depending on which mode is selected.

### Normal Mode

	DTC	DMAC
TRANSFER_IRQ_EACH	Interrupt after each transfer	N/A
TRANSFER_IRQ_END	Interrupt after last transfer	Interrupt after last transfer

### Repeat Mode

	DTC	DMAC
TRANSFER_IRQ_EACH	Interrupt after each transfer	Interrupt after each repeat
TRANSFER_IRQ_END	Interrupt after each repeat	Interrupt after last transfer

### Block Mode

	DTC	DMAC
TRANSFER_IRQ_EACH	Interrupt after each block	Interrupt after each block
TRANSFER_IRQ_END	Interrupt after last block	Interrupt after last block

*Note*

$DTC\_VECTOR\_TABLE\_SIZE = (ICU\_NVIC\_IRQ\_SOURCES \times 4) \text{ Bytes}$

## Peripheral Interrupts and DTC

When an interrupt is configured to trigger DTC transfers, the peripheral ISR will trigger on the following conditions:

- Each transfer completed (transfer\_info\_t::irq = TRANSFER\_IRQ\_EACH)
- Last transfer completed (transfer\_info\_t::irq = TRANSFER\_IRQ\_END)

For example, if SCI1\_RXI is configured to trigger DTC transfers and a SCI1\_RXI event occurs, the interrupt will not fire until the DTC transfer is completed. If the DTC transfer\_info\_t::irq is configured to only interrupt on the last transfer, than no RXI interrupts will occur until the last transfer is completed.

*Note*

1. The DTC activation source must be enabled in the NVIC in order to trigger DTC transfers (Modules that are designed to integrate the R\_DTC module will automatically handle this).
2. The DTC prioritizes activation sources by granting the smaller interrupt vector numbers higher priority. The priority of interrupts to the CPU is determined by the NVIC priority.

## Low Power Modes

DTCST must be set to 0 before transitioning to any of the following:

- Module-stop state
- Software Standby mode without Snooze mode transition
- Deep Software Standby mode

*Note*

1. R\_LPM Module stops the DTC before entering deep software standby mode and software standby without snooze mode transition.
2. For more information see 18.9 and 18.10 in the RA6M3 manual R01UH0886EJ0100.

## Limitations

Developers should be aware of the following limitations when using the DTC:

- If the DTC is configured to service many different activation sources, the system could run in to performance issues due to memory contention. To address this issue, it is recommended that the DTC vector table and transfer information be moved to their own dedicated memory area (Ex: SRAM0, SRAM1, SRAMHS). This allows memory accesses from different BUS Masters (CPU, DTC, DMAC, EDMAC and Graphics IPs) to occur in parallel.

## Examples

### Basic Example

This is a basic example of minimal use of the DTC in an application.

```
void dtc_minimal_example (void)
{
```



```

/* Open the transfer instance with initial configuration. */
fsp_err_t err = R_DTC_Open(&g_transfer_ctrl, &g_transfer_cfg);
/* Handle any errors. This function should be defined by the user. */
    handle_error(err);
/* Enable the DTC to handle incoming transfer requests. */
    err = R_DTC_Enable(&g_transfer_ctrl);
    handle_error(err);
}

```

## Data Structures

struct [dtc\\_extended\\_cfg\\_t](#)

struct [dtc\\_instance\\_ctrl\\_t](#)

## Macros

#define [DTC\\_MAX\\_NORMAL\\_TRANSFER\\_LENGTH](#)

#define [DTC\\_MAX\\_REPEAT\\_TRANSFER\\_LENGTH](#)

#define [DTC\\_MAX\\_BLOCK\\_TRANSFER\\_LENGTH](#)

#define [DTC\\_MAX\\_BLOCK\\_COUNT](#)

## Data Structure Documentation

### ◆ [dtc\\_extended\\_cfg\\_t](#)

struct <a href="#">dtc_extended_cfg_t</a>		
DTC transfer configuration extension. This extension is required.		
Data Fields		
IRQn_Type	activation_source	Select which IRQ will trigger the transfer.

### ◆ [dtc\\_instance\\_ctrl\\_t](#)

struct <a href="#">dtc_instance_ctrl_t</a>
Control block used by driver. DO NOT INITIALIZE - this structure will be initialized in <a href="#">transfer_api_t::open</a> .

## Macro Definition Documentation

**◆ DTC\_MAX\_NORMAL\_TRANSFER\_LENGTH**

```
#define DTC_MAX_NORMAL_TRANSFER_LENGTH
```

Max configurable number of transfers in NORMAL MODE

**◆ DTC\_MAX\_REPEAT\_TRANSFER\_LENGTH**

```
#define DTC_MAX_REPEAT_TRANSFER_LENGTH
```

Max number of transfers per repeat for REPEAT MODE

**◆ DTC\_MAX\_BLOCK\_TRANSFER\_LENGTH**

```
#define DTC_MAX_BLOCK_TRANSFER_LENGTH
```

Max number of transfers per block in BLOCK MODE

**◆ DTC\_MAX\_BLOCK\_COUNT**

```
#define DTC_MAX_BLOCK_COUNT
```

Max configurable number of blocks to transfer in BLOCK MODE

**Function Documentation**

---

◆ **R\_DTC\_Open()**

```
fsp_err_t R_DTC_Open ( transfer_ctrl_t *const p_api_ctrl, transfer_cfg_t const *const p_cfg )
```

Configure the vector table if it hasn't been configured, enable the Module and copy the pointer to the transfer info into the DTC vector table. Implements [transfer\\_api\\_t::open](#).

Example:

```
/* Open the transfer instance with initial configuration. */
fsp_err_t err = R_DTC_Open(&g_transfer_ctrl, &g_transfer_cfg);
```

**Return values**

FSP_SUCCESS	Successful open. Transfer transfer info pointer copied to DTC Vector table. Module started. DTC vector table configured.
FSP_ERR_ASSERTION	An input parameter is invalid.
FSP_ERR_UNSUPPORTED	Address Mode Offset is selected.
FSP_ERR_ALREADY_OPEN	The control structure is already opened.
FSP_ERR_IN_USE	The index for this IRQ in the DTC vector table is already configured.
FSP_ERR_IRQ_BSP_DISABLED	The IRQ associated with the activation source is not enabled in the BSP.

◆ **R\_DTC\_Reconfigure()**

```
fsp_err_t R_DTC_Reconfigure ( transfer_ctrl_t *const p_api_ctrl, transfer_info_t * p_info )
```

Copy pointer to transfer info into the DTC vector table and enable transfer in ICU. Implements [transfer\\_api\\_t::reconfigure](#).

**Return values**

FSP_SUCCESS	Transfer is configured and will start when trigger occurs.
FSP_ERR_ASSERTION	An input parameter is invalid.
FSP_ERR_NOT_OPEN	Handle is not initialized. Call R_DTC_Open to initialize the control block.
FSP_ERR_NOT_ENABLED	Transfer source address is NULL or is not aligned correctly. Transfer destination address is NULL or is not aligned correctly.

**Note**

*p\_info must persist until all transfers are completed.*

◆ **R\_DTC\_Reset()**

```
fsp_err_t R_DTC_Reset ( transfer_ctrl_t *const p_api_ctrl, void const *volatile p_src, void *volatile p_dest, uint16_t const num_transfers )
```

Reset transfer source, destination, and number of transfers. Implements [transfer\\_api\\_t::reset](#).

**Return values**

FSP_SUCCESS	Transfer reset successfully (transfers are enabled).
FSP_ERR_ASSERTION	An input parameter is invalid.
FSP_ERR_NOT_OPEN	Handle is not initialized. Call R_DTC_Open to initialize the control block.
FSP_ERR_NOT_ENABLED	Transfer source address is NULL or is not aligned correctly. Transfer destination address is NULL or is not aligned correctly.

◆ **R\_DTC\_SoftwareStart()**

```
fsp_err_t R_DTC_SoftwareStart ( transfer_ctrl_t *const p_api_ctrl, transfer_start_mode_t mode )
```

Placeholder for unsupported softwareStart function. Implements [transfer\\_api\\_t::softwareStart](#).

**Return values**

FSP_ERR_UNSUPPORTED	DTC software start is not supported.
---------------------	--------------------------------------

◆ **R\_DTC\_SoftwareStop()**

```
fsp_err_t R_DTC_SoftwareStop ( transfer_ctrl_t *const p_api_ctrl)
```

Placeholder for unsupported softwareStop function. Implements [transfer\\_api\\_t::softwareStop](#).

**Return values**

FSP_ERR_UNSUPPORTED	DTC software stop is not supported.
---------------------	-------------------------------------

◆ **R\_DTC\_Enable()**

```
fsp_err_t R_DTC_Enable ( transfer_ctrl_t *const p_api_ctrl)
```

Enable transfers on this activation source. Implements [transfer\\_api\\_t::enable](#).

Example:

```
/* Enable the DTC to handle incoming transfer requests. */
err = R_DTC_Enable(&g_transfer_ctrl);
handle_error(err);
```

**Return values**

FSP_SUCCESS	Transfers will be triggered by the activation source
FSP_ERR_ASSERTION	An input parameter is invalid.
FSP_ERR_UNSUPPORTED	Address Mode Offset is selected.
FSP_ERR_NOT_OPEN	Handle is not initialized. Call R_DTC_Open to initialize the control block.

◆ **R\_DTC\_Disable()**

```
fsp_err_t R_DTC_Disable ( transfer_ctrl_t *const p_api_ctrl)
```

Disable transfer on this activation source. Implements [transfer\\_api\\_t::disable](#).

**Return values**

FSP_SUCCESS	Transfers will not occur on activation events.
FSP_ERR_NOT_OPEN	Handle is not initialized. Call R_DTC_Open to initialize the control block.
FSP_ERR_ASSERTION	An input parameter is invalid.

## ◆ R\_DTC\_InfoGet()

```
fsp_err_t R_DTC_InfoGet ( transfer_ctrl_t *const p_api_ctrl, transfer_properties_t *const p_properties )
```

Provides information about this transfer. Implements [transfer\\_api\\_t::infoGet](#).

**Return values**

FSP_SUCCESS	p_info updated with current instance information.
FSP_ERR_NOT_OPEN	Handle is not initialized. Call R_DTC_Open to initialize the control block.
FSP_ERR_ASSERTION	An input parameter is invalid.

## ◆ R\_DTC\_Close()

```
fsp_err_t R_DTC_Close ( transfer_ctrl_t *const p_api_ctrl)
```

Disables DTC activation in the ICU, then clears transfer data from the DTC vector table. Implements [transfer\\_api\\_t::close](#).

**Return values**

FSP_SUCCESS	Successful close.
FSP_ERR_ASSERTION	An input parameter is invalid.
FSP_ERR_NOT_OPEN	Handle is not initialized. Call R_DTC_Open to initialize the control block.

## ◆ R\_DTC\_VersionGet()

```
fsp_err_t R_DTC_VersionGet ( fsp_version_t *const p_version)
```

Get the driver version based on compile time macros. Implements [transfer\\_api\\_t::versionGet](#).

**Return values**

FSP_SUCCESS	Version information written to p_version.
FSP_ERR_ASSERTION	An input parameter is invalid.

## 4.2.17 Event Link Controller (r\_elc)

### Modules

#### Functions

fsp\_err\_t R\_ELC\_Open (elc\_ctrl\_t \*const p\_ctrl, elc\_cfg\_t const \*const p\_cfg)

fsp\_err\_t R\_ELC\_Close (elc\_ctrl\_t \*const p\_ctrl)

fsp\_err\_t R\_ELC\_SoftwareEventGenerate (elc\_ctrl\_t \*const p\_ctrl,  
elc\_software\_event\_t event\_number)

fsp\_err\_t R\_ELC\_LinkSet (elc\_ctrl\_t \*const p\_ctrl, elc\_peripheral\_t peripheral,  
elc\_event\_t signal)

fsp\_err\_t R\_ELC\_LinkBreak (elc\_ctrl\_t \*const p\_ctrl, elc\_peripheral\_t peripheral)

fsp\_err\_t R\_ELC\_Enable (elc\_ctrl\_t \*const p\_ctrl)

fsp\_err\_t R\_ELC\_Disable (elc\_ctrl\_t \*const p\_ctrl)

fsp\_err\_t R\_ELC\_VersionGet (fsp\_version\_t \*const p\_version)

#### Detailed Description

Driver for the ELC peripheral on RA MCUs. This module implements the [ELC Interface](#).

## Overview

The event link controller (ELC) uses the event requests generated by various peripheral modules as source signals to connect (link) them to different modules, allowing direct cooperation between the modules without central processing unit (CPU) intervention. The conceptual diagram below illustrates a potential setup where a pin interrupt triggers a timer which later triggers an ADC conversion and CTSU scan, while at the same time a serial communication interrupt automatically starts a data transfer. These tasks would be automatically handled without the need for polling or interrupt management.

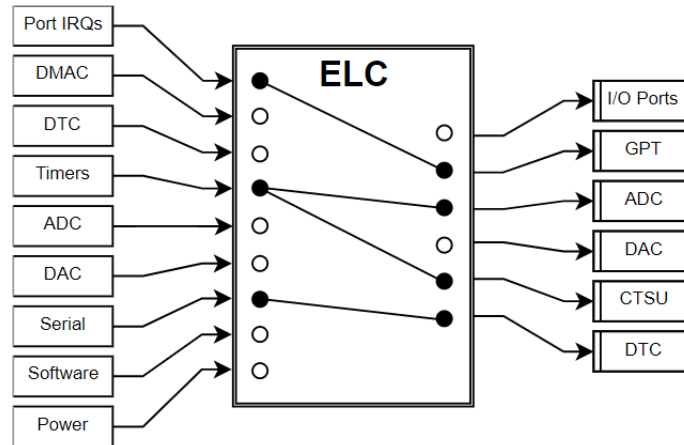


Figure 156: Event Link Controller Conceptual Diagram

In essence, the ELC is an array of multiplexers to route a wide variety of interrupt signals to a subset of peripheral functions. Events are linked by setting the multiplexer for the desired function to the desired signal (through `R_ELC_LinkSet`). The diagram below illustrates one peripheral output of the ELC. In this example, a conversion start is triggered for ADC0 Group A when the GPT0 counter overflows:

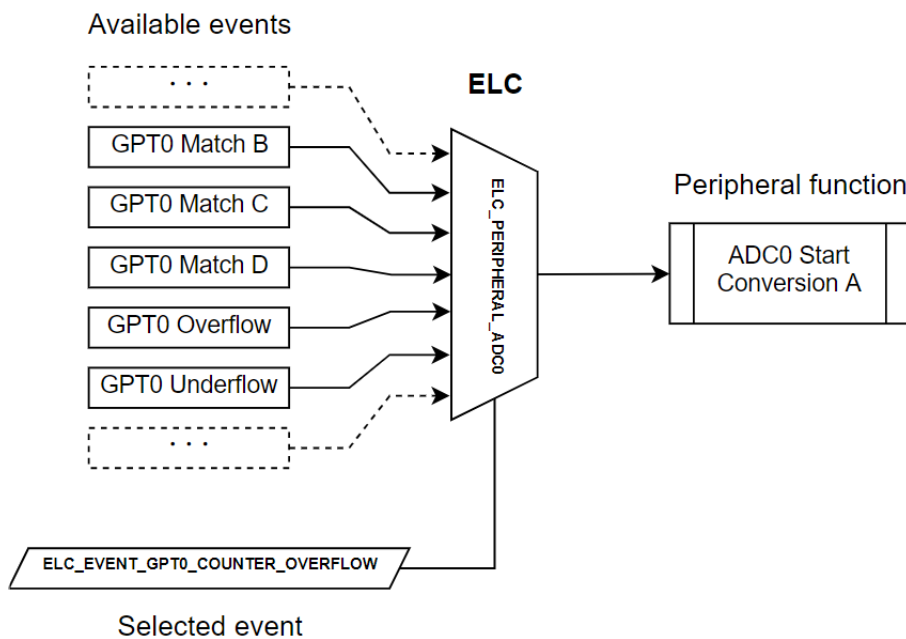


Figure 157: ELC Example

## Features

The ELC HAL module can perform the following functions:

- Initialize the ELC to a pre-defined set of links
- Create an event link between two blocks
- Break an event link between two blocks
- Generate one of two software events that interrupt the CPU
- Globally enable or disable event links



A variety of functions can be activated via events, including:

- General-purpose timer (GPT) control
- ADC and DAC conversion start
- Synchronized I/O port output (ports 1-4 only)
- Capacitive touch unit (CTSU) measurement activation

#### Note

The available sources and peripherals may differ between devices. A full list of selectable peripherals and events is available in the User's Manual for your device.

Some peripherals have specific settings related to ELC event generation and/or reception. Details on how to enable event functionality for each peripheral are located in the usage notes for the related module(s) as well as in the User's Manual for your device.

## Configuration

#### Note

Event links will be automatically generated based on the selections made in module properties. To view the currently linked events check the [Event Links tab in the RA Configuration editor](#).

Calling [R\\_ELC\\_Open](#) followed by [R\\_ELC\\_Enable](#) will automatically link all events shown in the Event Links tab.

To manually link an event to a peripheral at runtime perform the following steps:

1. Configure the operation of the destination peripheral (including any configuration necessary to receive events)
2. Use [R\\_ELC\\_LinkSet](#) to set the desired event link to the peripheral
3. Use [R\\_ELC\\_Enable](#) to enable transmission of event signals
4. Configure the signaling module to output the desired event (typically an interrupt)

To disable the event, either use [R\\_ELC\\_LinkBreak](#) to clear the link for a specific event or [R\\_ELC\\_Disable](#) to globally disable event linking.

#### Note

The ELC module needs no pin, clocking or interrupt configuration; it is merely a mechanism to connect signals between peripherals. However, when linking I/O Ports via the ELC the relevant I/O pins need to be configured as inputs or outputs.

### Build Time Configurations for r\_elc

The following build time configurations are defined in `fsp_cfg/r_elc_cfg.h`:

Configuration	Options	Default	Description
Parameter Checking	<ul style="list-style-type: none"> <li>• Default (BSP)</li> <li>• Enabled</li> <li>• Disabled</li> </ul>	Default (BSP)	If selected code for parameter checking is included in the build.

### Configurations for Driver > System > ELC Driver on r\_elc

This module can be added to the Stacks tab via [New Stack > Driver > System > ELC Driver on r\\_elc](#). Non-secure callable guard functions can be generated for this module by right clicking the module in the RA Configuration tool and checking the "Non-secure Callable" box.

Configuration	Options	Default	Description
---------------	---------	---------	-------------

Name	ELC instance name <code>g_elc</code> must be <code>g_elc</code> to match <code>elc_cfg_t</code> data structure created in <code>elc_data.c</code>	Module name. Fixed to <code>g_elc</code> .
------	------------------------------------------------------------------------------------------------------------------------------------------------------	--------------------------------------------

## Usage Notes

### Limitations

Developers should be aware of the following limitations when using the ELC:

- To link events it is necessary for the ELC and the related modules to be enabled. The ELC cannot operate if the related modules are in the module stop state or the MCU is in a low power consumption mode for which the module is stopped.
- If two modules are linked across clock domains there may be a 1 to 2 cycle delay between event signaling and reception. The delay timing is based on the frequency of the slowest clock.

## Examples

### Basic Example

Below is a basic example of minimal use of event linking in an application.

```
/* This struct is automatically generated based on the events configured by
peripherals in the RA Configuration editor. */
static const elc_cfg_t g_elc_cfg =
{
    .link[ELC_PERIPHERAL_GPT_A] = ELC_EVENT_ICU_IRQ0,
    .link[ELC_PERIPHERAL_IOPORT1] = ELC_EVENT_GPT0_COUNTER_OVERFLOW
};

void elc_basic_example (void)
{
    fsp_err_t err = FSP_SUCCESS;

    /* Initializes the software and sets the links defined in the control structure. */
    err = R_ELC_Open(&g_elc_ctrl, &g_elc_cfg);

    /* Handle any errors. This function should be defined by the user. */
    handle_error(err);

    /* Create or modify a link between a peripheral function and an event source. */
    err = R_ELC_LinkSet(&g_elc_ctrl, ELC_PERIPHERAL_ADC0,
ELC_EVENT_GPT0_COUNTER_OVERFLOW);
    handle_error(err);
}
```

```
/* Globally enable event linking in the ELC. */  
err = R_ELC_Enable(&g_elc_ctrl);  
handle_error(err);  
}
```

## Software-Generated Events

This example demonstrates how to use a software-generated event to signal a peripheral. This can be useful when the desired event source is not supported by the ELC hardware.

```
/* Interrupt handler for peripheral event not supported by the ELC */  
void peripheral_isr (void)  
{  
    fsp_err_t err;  
    /* Generate an event signal through software to the linked peripheral. */  
    err = R_ELC_SoftwareEventGenerate(&g_elc_ctrl, ELC_SOFTWARE_EVENT_0);  
    handle_error(err);  
}  
void elc_software_event (void)  
{  
    fsp_err_t err = FSP_SUCCESS;  
    /* Open the module. */  
    err = R_ELC_Open(&g_elc_ctrl, &g_elc_cfg);  
    /* Handle any errors. This function should be defined by the user. */  
    handle_error(err);  
    /* Link ADC0 conversion start to software event 0. */  
    err = R_ELC_LinkSet(&g_elc_ctrl, ELC_PERIPHERAL_ADC0,  
ELC_EVENT_ELC_SOFTWARE_EVENT_0);  
    handle_error(err);  
    while (true)  
    {  
        /* Application code here. */  
    }  
}
```

## Data Structures

```
struct elc_instance_ctrl_t
```

## Data Structure Documentation

### ◆ elc\_instance\_ctrl\_t

```
struct elc_instance_ctrl_t
```

ELC private control block. DO NOT MODIFY. Initialization occurs when `R_ELC_Open()` is called.

## Function Documentation

### ◆ R\_ELC\_Open()

```
fsp_err_t R_ELC_Open ( elc_ctrl_t *const p_ctrl, elc_cfg_t const *const p_cfg )
```

Initialize all the links in the Event Link Controller. Implements `elc_api_t::open`

The configuration structure passed in to this function includes links for every event source included in the ELC and sets them all at once. To set or clear an individual link use `R_ELC_LinkSet` and `R_ELC_LinkBreak` respectively.

Example:

```
/* Initializes the software and sets the links defined in the control structure. */
err = R_ELC_Open(&g_elc_ctrl, &g_elc_cfg);
```

#### Return values

FSP_SUCCESS	Initialization was successful
FSP_ERR_ASSERTION	p_ctrl or p_cfg was NULL
FSP_ERR_ALREADY_OPEN	The module is currently open

### ◆ R\_ELC\_Close()

```
fsp_err_t R_ELC_Close ( elc_ctrl_t *const p_ctrl)
```

Globally disable ELC linking. Implements `elc_api_t::close`

#### Return values

FSP_SUCCESS	The ELC was successfully disabled
FSP_ERR_ASSERTION	p_ctrl was NULL
FSP_ERR_NOT_OPEN	The module has not been opened

◆ **R\_ELC\_SoftwareEventGenerate()**

```
fsp_err_t R_ELC_SoftwareEventGenerate ( elc_ctrl_t *const p_ctrl, elc_software_event_t
event_number )
```

Generate a software event in the Event Link Controller. Implements `elc_api_t::softwareEventGenerate`

Example:

```
/* Generate an event signal through software to the linked peripheral. */
err = R_ELC_SoftwareEventGenerate(&g_elc_ctrl, ELC_SOFTWARE_EVENT_0);
handle_error(err);
```

**Return values**

FSP_SUCCESS	Initialization was successful
FSP_ERR_ASSERTION	Invalid event number or p_ctrl was NULL
FSP_ERR_NOT_OPEN	The module has not been opened

◆ **R\_ELC\_LinkSet()**

```
fsp_err_t R_ELC_LinkSet ( elc_ctrl_t *const p_ctrl, elc_peripheral_t peripheral, elc_event_t signal )
```

Create a single event link. Implements `elc_api_t::linkSet`

Example:

```
/* Create or modify a link between a peripheral function and an event source. */
err = R_ELC_LinkSet(&g_elc_ctrl, ELC_PERIPHERAL_ADC0,
ELC_EVENT_GPT0_COUNTER_OVERFLOW);
handle_error(err);
```

**Return values**

FSP_SUCCESS	Initialization was successful
FSP_ERR_ASSERTION	p_ctrl was NULL
FSP_ERR_NOT_OPEN	The module has not been opened

◆ **R\_ELC\_LinkBreak()**

```
fsp_err_t R_ELC_LinkBreak ( elc_ctrl_t *const p_ctrl, elc_peripheral_t peripheral )
```

Break an event link. Implements `elc_api_t::linkBreak`

**Return values**

FSP_SUCCESS	Event link broken
FSP_ERR_ASSERTION	p_ctrl was NULL
FSP_ERR_NOT_OPEN	The module has not been opened

◆ **R\_ELC\_Enable()**

```
fsp_err_t R_ELC_Enable ( elc_ctrl_t *const p_ctrl)
```

Enable the operation of the Event Link Controller. Implements `elc_api_t::enable`

**Return values**

FSP_SUCCESS	ELC enabled.
FSP_ERR_ASSERTION	p_ctrl was NULL
FSP_ERR_NOT_OPEN	The module has not been opened

◆ **R\_ELC\_Disable()**

```
fsp_err_t R_ELC_Disable ( elc_ctrl_t *const p_ctrl)
```

Disable the operation of the Event Link Controller. Implements `elc_api_t::disable`

**Return values**

FSP_SUCCESS	ELC disabled.
FSP_ERR_ASSERTION	p_ctrl was NULL
FSP_ERR_NOT_OPEN	The module has not been opened

◆ **R\_ELC\_VersionGet()**

```
fsp_err_t R_ELC_VersionGet ( fsp_version_t *const p_version)
```

Get the driver version based on compile time macros. Implements [elc\\_api\\_t::versionGet](#)

**Return values**

FSP_SUCCESS	Successful close.
FSP_ERR_ASSERTION	p_version is NULL.

**4.2.18 Ethernet (r\_ether)**

## Modules

**Functions**

```
fsp_err_t R_ETHER_Open (ether_ctrl_t *const p_ctrl, ether_cfg_t const *const p_cfg)
```

After ETHERC, EDMAC and PHY-LSI are reset in software, an auto negotiation of PHY-LSI is begun. Afterwards, the link signal change interrupt is permitted. Implements [ether\\_api\\_t::open](#). [More...](#)

```
fsp_err_t R_ETHER_Close (ether_ctrl_t *const p_ctrl)
```

Disables interrupts. Removes power and releases hardware lock. Implements [ether\\_api\\_t::close](#). [More...](#)

```
fsp_err_t R_ETHER_Read (ether_ctrl_t *const p_ctrl, void *const p_buffer, uint32_t *const length_bytes)
```

Receive Ethernet frame. Receives data to the location specified by the pointer to the receive buffer. In zero copy mode, the address of the receive buffer is returned. In non zero copy mode, the received data in the internal buffer is copied to the pointer passed by the argument. Implements [ether\\_api\\_t::read](#). [More...](#)

```
fsp_err_t R_ETHER_BufferRelease (ether_ctrl_t *const p_ctrl)
```

Move to the next buffer in the circular receive buffer list. Implements [ether\\_api\\_t::bufferRelease](#). [More...](#)

```
fsp_err_t R_ETHER_Write (ether_ctrl_t *const p_ctrl, void *const p_buffer, uint32_t const frame_length)
```

Transmit Ethernet frame. Transmits data from the location specified by the pointer to the transmit buffer, with the data size equal to the specified frame length. In the non zero copy mode, transmits data after being copied to the internal buffer. Implements [ether\\_api\\_t::write](#). [More...](#)

`fsp_err_t` [R\\_ETHER\\_LinkProcess](#) (`ether_ctrl_t *const p_ctrl`)

The Link up processing, the Link down processing, and the magic packet detection processing are executed. Implements [ether\\_api\\_t::linkProcess](#). [More...](#)

`fsp_err_t` [R\\_ETHER\\_WakeOnLANEnable](#) (`ether_ctrl_t *const p_ctrl`)

The setting of ETHERC is changed from normal sending and receiving mode to magic packet detection mode. Implements [ether\\_api\\_t::wakeOnLANEnable](#). [More...](#)

`fsp_err_t` [R\\_ETHER\\_VersionGet](#) (`fsp_version_t *const p_version`)

Provides API and code version in the user provided pointer. Implements [ether\\_api\\_t::versionGet](#). [More...](#)

## Detailed Description

Driver for the Ethernet peripheral on RA MCUs. This module implements the [Ethernet Interface](#).

## Overview

This module performs Ethernet frame transmission and reception using an Ethernet controller and an Ethernet DMA controller.

## Features

The Ethernet module supports the following features:

- Transmit/receive processing
- Optional zero-copy buffering
- Callback function with returned event code
- Magic packet detection mode support
- Auto negotiation support
- Flow control support
- Multicast filtering support
- Broadcast filtering support
- Promiscuous mode support

## Configuration

### Build Time Configurations for r\_ether



The following build time configurations are defined in fsp\_cfg/r\_ether\_cfg.h:

Configuration	Options	Default	Description
Parameter Checking	<ul style="list-style-type: none"> <li>• Default (BSP)</li> <li>• Enabled</li> <li>• Disabled</li> </ul>	Default (BSP)	If selected code for parameter checking is included in the build.
ET0_LINKSTA Pin Status Flag	<ul style="list-style-type: none"> <li>• Fall -&gt; Rise</li> <li>• Rise -&gt; Fall</li> </ul>	Fall -> Rise	Specify the polarity of the link signal output by the PHY-LSI. When 0 is specified, link-up and link-down correspond respectively to the fall and rise of the LINKSTA signal. When 1 is specified, link-up and link-down correspond respectively to the rise and fall of the LINKSTA signal.
Link Signal Change Flag	<ul style="list-style-type: none"> <li>• Unused</li> <li>• Used</li> </ul>	Unused	Use LINKSTA signal for detect link status changes 0 = unused (use PHY-LSI status register) 1 = use (use LINKSTA signal)

### Configurations for Driver > Network > Ethernet Driver on r\_ether

This module can be added to the Stacks tab via New Stack > Driver > Network > Ethernet Driver on r\_ether.

Configuration	Options	Default	Description
General > Name	Name must be a valid C symbol	g_ether0	Module name.
General > Channel	0	0	Select the ether channel number.
General > MAC address	Must be a valid MAC address	00:11:22:33:44:55	MAC address of this channel.
General > Zero-copy Mode	<ul style="list-style-type: none"> <li>• Disable</li> <li>• Enable</li> </ul>	Disable	Enable or disable zero-copy mode.
General > Flow control functionality	<ul style="list-style-type: none"> <li>• Disable</li> <li>• Enable</li> </ul>	Disable	Enable or disable flow control.
Filters > Multicast Mode	<ul style="list-style-type: none"> <li>• Disable</li> <li>• Enable</li> </ul>	Enable	Enable or disable multicast frame reception.
Filters > Promiscuous Mode	<ul style="list-style-type: none"> <li>• Disable</li> <li>• Enable</li> </ul>	Disable	Enable this option to receive packets addressed to other

NICs.

Filters > Broadcast filter	Must be a valid non-negative integer with maximum configurable value of 65535.	0	Limit of the number of broadcast frames received continuously
Buffers > Number of TX buffer	Must be an integer from 1 to 8	1	Number of transmit buffers
Buffers > Number of RX buffer	Must be an integer from 1 to 8	1	Number of receive buffers
Buffers > Buffer size	Must be at least 1514 which is the maximum Ethernet frame size	1514	Size of Ethernet buffer
Interrupts > Interrupt priority	MCU Specific Options		Select the EDMAC interrupt priority.
Interrupts > Callback	Name must be a valid C symbol	NULL	Callback provided when an ISR occurs

## Interrupt Configuration

The first [R\\_ETHER\\_Open](#) function call sets EINT interrupts. The user could provide callback function which would be invoked when EINT interrupt handler has been completed. The callback arguments will contain information about a channel number, the ETHERC and EDMAC status, the event code, and a pointer to the user defined context.

## Callback Configuration

The user could provide callback function which would be invoked when either a magic packet or a link signal change is detected. When the callback function is called, a variable in which the channel number for which the detection occurred and a constant shown in Table 2.4 are stored is passed as an argument. If the value of this argument is to be used outside the callback function, its value should be copied into, for example, a global variable.

## Clock Configuration

The clock for this module is derived from the following peripheral clock for each MCU group:

MCU Group	Peripheral Clock
RA6M2	PCLKA
RA6M3	PCLKA
RA6M4	PCLKA

Note

1. When using ETHERC, the PCLKA frequency is in the range  $12.5 \text{ MHz} \leq PCLKA \leq 120 \text{ MHz}$ .
2. When using ETHERC,  $PCLKA = ICLK$ .

## Pin Configuration

To use the Ethernet module, input/output signals of the peripheral function have to be allocated to pins with the multi-function pin controller (MPC). Please perform the pin setting before calling the [R\\_ETHER\\_Open](#) function.

## Usage Notes

### Ethernet Frame Format

The Ethernet module supports the Ethernet II/IEEE 802.3 frame format.

### Frame Format for Data Transmission and Reception

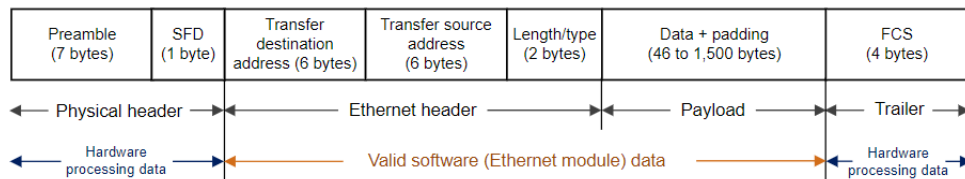


Figure 158: Frame Format Image

The preamble and SFD signal the start of an Ethernet frame. The FCS contains the CRC of the Ethernet frame and is calculated on the transmitting side. When data is received the CRC value of the frame is calculated in hardware, and the Ethernet frame is discarded if the values do not match. When the hardware determines that the data is normal, the valid range of receive data is: (transmission destination address) + (transmission source address) + (length/type) + (data).

### PAUSE Frame Format

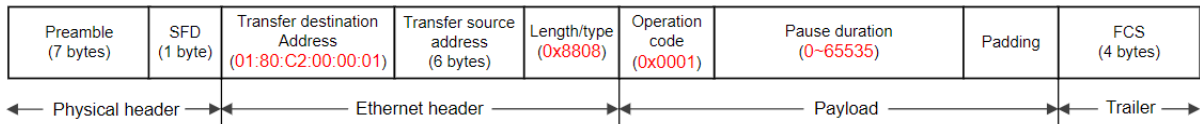


Figure 159: Pause Frame Format Image

The transmission destination address is specified as 01:80:C2:00:00:01 (a multicast address reserved for PAUSE frames). At the start of the payload the length/type is specified as 0x8808 and the operation code as 0x0001. The pause duration in the payload is specified by the value of the automatic PAUSE (AP) bits in the automatic PAUSE frame setting register (APR), or the manual PAUSE time setting (MP) bits in the manual PAUSE frame setting register (MPR).

### Magic Packet Frame Format

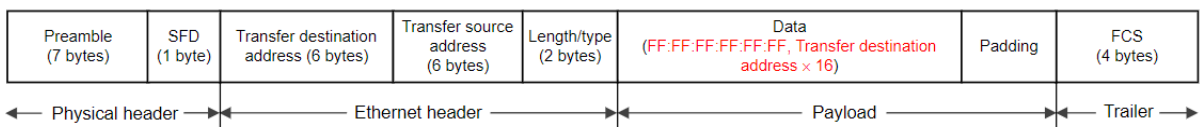


Figure 160: Magic Packet Frame Format Image

In a Magic Packet, the value FF:FF:FF:FF:FF:FF followed by the transmission destination address repeated 16 times is inserted somewhere in the Ethernet frame data.

## Limitations

### Memory alignment limitation for Ethernet buffer

The Ethernet Driver has several alignment constraints:

- 16-byte alignment for the descriptor
- 32-byte aligned write buffer for `R_ETHER_Write` when zero copy mode is enabled

### Functional limitations in TrustZone Security Extensions

The Ethernet Driver has several security constraints:

MCU	Has Security Extension	Support Flat project	Support TZ project	
			Secure	Non-Secure
RA6M2	-	x	-	-
RA6M3	-	x	-	-
RA6M4	- *1	x	-	x

Note

1. ETHERC/EDMAC is always Non-secure peripheral in this MCU.

## Examples

### ETHER Basic Example

This is a basic example of minimal use of the ETHER in an application.

Note

In this example zero-copy mode is disabled and there are no restrictions on buffer alignment.

```
#define ETHER_EXAMPLE_MAXIMUM_ETHERNET_FRAME_SIZE (1514)
#define ETHER_EXAMPLE_TRANSMIT_ETHERNET_FRAME_SIZE (60)
#define ETHER_EXAMPLE_SOURCE_MAC_ADDRESS 0x74, 0x90, 0x50, 0x00, 0x79, 0x01
#define ETHER_EXAMPLE_DESTINATION_MAC_ADDRESS 0x74, 0x90, 0x50, 0x00, 0x79, 0x02
#define ETHER_EXAMPLE_FRAME_TYPE 0x00, 0x2E
#define ETHER_EXAMPLE_PAYLOAD 0x00, 0x00, 0x00, 0x00, 0x00, 0x00, 0x00, 0x00, 0x00,
0x00, \
    0x00, 0x00, 0x00, 0x00, 0x00, 0x00, 0x00, 0x00, 0x00, 0x00, \
    0x00, 0x00, 0x00, 0x00, 0x00, 0x00, 0x00, 0x00, 0x00, 0x00, \
    0x00, 0x00, 0x00, 0x00, 0x00, 0x00, 0x00, 0x00, 0x00, 0x00, \
```

```
/* Receive data buffer */
static uint8_t gp_read_buffer[ETHER_EXAMPLE_MAXIMUM_ETHERNET_FRAME_SIZE] = {0};
/* Transmit data buffer */
static uint8_t gp_send_data[ETHER_EXAMPLE_TRANSMIT_ETHERNET_FRAME_SIZE] =
{
    ETHER_EXAMPLE_DESTINATION_MAC_ADDRESS, /* Destination MAC address */
    ETHER_EXAMPLE_SOURCE_MAC_ADDRESS,      /* Source MAC address */
    ETHER_EXAMPLE_FRAME_TYPE,              /* Type field */
    ETHER_EXAMPLE_PAYLOAD                   /* Payload value (46byte) */
};
void ether_basic_example (void)
{
    fsp_err_t err = FSP_SUCCESS;
    /* Source MAC Address */
    static uint8_t mac_address_source[6] = {ETHER_EXAMPLE_SOURCE_MAC_ADDRESS};
    uint32_t read_data_size = 0;
    g_ether0_cfg.p_mac_address = mac_address_source;
    /* Open the ether instance with initial configuration. */
    err = R_ETHER_Open(&g_ether0_ctrl, &g_ether0_cfg);
    /* Handle any errors. This function should be defined by the user. */
    handle_error(err);
do
    {
        /* When the Ethernet link status read from the PHY-LSI Basic Status register is link-
up,
        * Initializes the module and make auto negotiation. */
        err = R_ETHER_LinkProcess(&g_ether0_ctrl);
        } while (FSP_SUCCESS != err);
    /* Transmission is non-blocking. */
    /* User data copy to internal buffer and is transferred by DMA in the background. */
    err = R_ETHER_Write(&g_ether0_ctrl, (void *) gp_send_data, sizeof(gp_send_data));
    handle_error(err);
    /* received data copy to user buffer from internal buffer. */
    err = R_ETHER_Read(&g_ether0_ctrl, (void *) gp_read_buffer, &read_data_size);
```

```
    handle_error(err);

    /* Disable transmission and receive function and close the ether instance. */
    R_ETHER_Close(&g_ether0_ctrl);
}
```

## ETHER Advanced Example

The example demonstrates using send and receive function in zero copy mode. Transmit buffers must be 32-byte aligned and the receive buffer must be released once its contents have been used.

```
#define ETHER_EXAMPLE_FLAG_ON (1U)
#define ETHER_EXAMPLE_FLAG_OFF (0U)
#define ETHER_EXAMPLE_ETHER_ISR_EE_FR_MASK (1UL << 18)
#define ETHER_EXAMPLE_ETHER_ISR_EE_TC_MASK (1UL << 21)
#define ETHER_EXAMPLE_ETHER_ISR_EC_MPD_MASK (1UL << 1)
#define ETHER_EXAMPLE_ALIGNMENT_32_BYTE (32)

static volatile uint32_t g_example_receive_complete = 0;
static volatile uint32_t g_example_transfer_complete = 0;
static volatile uint32_t g_example_magic_packet_done = 0;

/* The data buffer must be 32-byte aligned when using zero copy mode. */
static uint8_t gp_send_data_nocopy[ETHER_EXAMPLE_TRANSMIT_ETHERNET_FRAME_SIZE]
BSP_ALIGN_VARIABLE(32) =
{
    ETHER_EXAMPLE_DESTINATION_MAC_ADDRESS, /* Destination MAC address */
    ETHER_EXAMPLE_SOURCE_MAC_ADDRESS,     /* Source MAC address */
    ETHER_EXAMPLE_FRAME_TYPE,             /* Type field */
    ETHER_EXAMPLE_PAYLOAD                  /* Payload value (46byte) */
};

void ether_example_callback (ether_callback_args_t * p_args) {
    switch (p_args->event)
    {
        case ETHER_EVENT_INTERRUPT:
            {
                if (ETHER_EXAMPLE_ETHER_ISR_EC_MPD_MASK == (p_args->status_ecsr &
ETHER_EXAMPLE_ETHER_ISR_EC_MPD_MASK))
```

```
    {
        g_example_magic_packet_done = ETHER_EXAMPLE_FLAG_ON;
    }

    if (ETHER_EXAMPLE_ETHER_ISR_EE_TC_MASK == (p_args->status_eesr &
ETHER_EXAMPLE_ETHER_ISR_EE_TC_MASK))
    {
        g_example_transfer_complete = ETHER_EXAMPLE_FLAG_ON;
    }

    if (ETHER_EXAMPLE_ETHER_ISR_EE_FR_MASK == (p_args->status_eesr &
ETHER_EXAMPLE_ETHER_ISR_EE_FR_MASK))
    {
        g_example_receive_complete = ETHER_EXAMPLE_FLAG_ON;
    }

    break;
}

default:
    {
    }
}
}

void ether_advanced_example (void) {
    fsp_err_t err = FSP_SUCCESS;
    /* Source MAC Address */
    static uint8_t mac_address_source[6] = {ETHER_EXAMPLE_SOURCE_MAC_ADDRESS};
    static uint8_t * p_read_buffer_nocopy;
    uint32_t      read_data_size = 0;
    g_ether0_cfg.p_mac_address = mac_address_source;
    g_ether0_cfg.zerocopy      = ETHER_ZEROCOPY_ENABLE;
    g_ether0_cfg.p_callback = (void (*)(ether_callback_args_t
*))ether_example_callback;
    /* Open the ether instance with initial configuration. */
    err = R_ETHER_Open(&g_ether0_ctrl, &g_ether0_cfg);
    /* Handle any errors. This function should be defined by the user. */
    handle_error(err);
}
```

```
do
{
/* When the Ethernet link status read from the PHY-LSI Basic Status register is link-
up,
* Initializes the module and make auto negotiation. */
err = R_ETHER_LinkProcess(&g_ether0_ctrl);
} while (FSP_SUCCESS != err);
/* Set user buffer to TX descriptor and enable transmission. */
err = R_ETHER_Write(&g_ether0_ctrl, (void *) gp_send_data_nocopy, sizeof
(gp_send_data_nocopy));
if (FSP_SUCCESS == err)
{
/* Wait for the transmission to complete. */
/* Data array should not change in zero copy mode until transfer complete. */
while (ETHER_EXAMPLE_FLAG_ON != g_example_transfer_complete)
{
;
}
}
/* Get receive buffer from RX descriptor. */
err = R_ETHER_Read(&g_ether0_ctrl, (void *) &p_read_buffer_nocopy,
&read_data_size);
handle_error(err);
/* Process received data here */
/* Release receive buffer to RX descriptor. */
err = R_ETHER_BufferRelease(&g_ether0_ctrl);
handle_error(err);
/* Disable transmission and receive function and close the ether instance. */
R_ETHER_Close(&g_ether0_ctrl);
}
```

## Data Structures

struct [ether\\_instance\\_ctrl\\_t](#)

## Enumerations



enum [ether\\_previous\\_link\\_status\\_t](#)enum [ether\\_link\\_change\\_t](#)enum [ether\\_magic\\_packet\\_t](#)enum [ether\\_link\\_establish\\_status\\_t](#)

## Data Structure Documentation

### ◆ ether\_instance\_ctrl\_t

struct ether_instance_ctrl_t		
ETHER control block. DO NOT INITIALIZE. Initialization occurs when <a href="#">ether_api_t::open</a> is called.		
Data Fields		
uint32_t	open	Used to determine if the channel is configured.
<a href="#">ether_cfg_t</a> const *	p_ether_cfg	Pointer to initial configurations.
<a href="#">ether_instance_descriptor_t</a> *	p_rx_descriptor	Pointer to the currently referenced transmit descriptor.
<a href="#">ether_instance_descriptor_t</a> *	p_tx_descriptor	Pointer to the currently referenced receive descriptor.
void *	p_reg_etherc	Base register of ethernet controller for this channel.
void *	p_reg_edmac	Base register of EDMA controller for this channel.
<a href="#">ether_previous_link_status_t</a>	previous_link_status	Previous link status.
<a href="#">ether_link_change_t</a>	link_change	status of link change
<a href="#">ether_magic_packet_t</a>	magic_packet	status of magic packet detection
<a href="#">ether_link_establish_status_t</a>	link_establish_status	Current Link status.

## Enumeration Type Documentation

### ◆ ether\_previous\_link\_status\_t

enum <a href="#">ether_previous_link_status_t</a>	
Enumerator	
ETHER_PREVIOUS_LINK_STATUS_DOWN	Previous link status is down.
ETHER_PREVIOUS_LINK_STATUS_UP	Previous link status is up.

## ◆ ether\_link\_change\_t

enum ether_link_change_t	
Enumerator	
ETHER_LINK_CHANGE_NO_CHANGE	Link status is no change.
ETHER_LINK_CHANGE_LINK_DOWN	Link status changes to down.
ETHER_LINK_CHANGE_LINK_UP	Link status changes to up.

## ◆ ether\_magic\_packet\_t

enum ether_magic_packet_t	
Enumerator	
ETHER_MAGIC_PACKET_NOT_DETECTED	Magic packet is not detected.
ETHER_MAGIC_PACKET_DETECTED	Magic packet is detected.

## ◆ ether\_link\_establish\_status\_t

enum ether_link_establish_status_t	
Enumerator	
ETHER_LINK_ESTABLISH_STATUS_DOWN	Link establish status is down.
ETHER_LINK_ESTABLISH_STATUS_UP	Link establish status is up.

## Function Documentation

---

◆ **R\_ETHER\_Open()**

```
fsp_err_t R_ETHER_Open ( ether_ctrl_t *const p_ctrl, ether_cfg_t const *const p_cfg )
```

After ETHERC, EDMAC and PHY-LSI are reset in software, an auto negotiation of PHY-LSI is begun. Afterwards, the link signal change interrupt is permitted. Implements [ether\\_api\\_t::open](#).

**Return values**

FSP_SUCCESS	Channel opened successfully.
FSP_ERR_ASSERTION	Pointer to ETHER control block or configuration structure is NULL.
FSP_ERR_ALREADY_OPEN	Control block has already been opened or channel is being used by another instance. Call close() then open() to reconfigure.
FSP_ERR_ETHER_ERROR_PHY_COMMUNICATION	Initialization of PHY-LSI failed.
FSP_ERR_INVALID_CHANNEL	Invalid channel number is given.
FSP_ERR_INVALID_POINTER	Pointer to MAC address is NULL.
FSP_ERR_INVALID_ARGUMENT	Interrupt is not enabled.
FSP_ERR_ETHER_PHY_ERROR_LINK	Initialization of PHY-LSI failed.

◆ **R\_ETHER\_Close()**

```
fsp_err_t R_ETHER_Close ( ether_ctrl_t *const p_ctrl)
```

Disables interrupts. Removes power and releases hardware lock. Implements [ether\\_api\\_t::close](#).

**Return values**

FSP_SUCCESS	Channel successfully closed.
FSP_ERR_ASSERTION	Pointer to ETHER control block is NULL.
FSP_ERR_NOT_OPEN	The control block has not been opened

◆ **R\_ETHER\_Read()**

```
fsp_err_t R_ETHER_Read ( ether_ctrl_t *const p_ctrl, void *const p_buffer, uint32_t *const length_bytes )
```

Receive Ethernet frame. Receives data to the location specified by the pointer to the receive buffer. In zero copy mode, the address of the receive buffer is returned. In non zero copy mode, the received data in the internal buffer is copied to the pointer passed by the argument. Implements [ether\\_api\\_t::read](#).

**Return values**

FSP_SUCCESS	Processing completed successfully.
FSP_ERR_ASSERTION	Pointer to ETHER control block is NULL.
FSP_ERR_NOT_OPEN	The control block has not been opened.
FSP_ERR_ETHER_ERROR_NO_DATA	There is no data in receive buffer.
FSP_ERR_ETHER_ERROR_LINK	Auto-negotiation is not completed, and reception is not enabled.
FSP_ERR_ETHER_ERROR_MAGIC_PACKET_MODE	As a Magic Packet is being detected, transmission and reception is not enabled.
FSP_ERR_ETHER_ERROR_FILTERING	Multicast Frame filter is enable, and Multicast Address Frame is received.
FSP_ERR_INVALID_POINTER	Value of the pointer is NULL.

◆ **R\_ETHER\_BufferRelease()**

```
fsp_err_t R_ETHER_BufferRelease ( ether_ctrl_t *const p_ctrl)
```

Move to the next buffer in the circular receive buffer list. Implements [ether\\_api\\_t::bufferRelease](#).

**Return values**

FSP_SUCCESS	Processing completed successfully.
FSP_ERR_ASSERTION	Pointer to ETHER control block is NULL.
FSP_ERR_NOT_OPEN	The control block has not been opened
FSP_ERR_ETHER_ERROR_LINK	Auto-negotiation is not completed, and reception is not enabled.
FSP_ERR_ETHER_ERROR_MAGIC_PACKET_MODE	As a Magic Packet is being detected, transmission and reception is not enabled.

◆ **R\_ETHER\_Write()**

```
fsp_err_t R_ETHER_Write ( ether_ctrl_t *const p_ctrl, void *const p_buffer, uint32_t const
frame_length )
```

Transmit Ethernet frame. Transmits data from the location specified by the pointer to the transmit buffer, with the data size equal to the specified frame length. In the non zero copy mode, transmits data after being copied to the internal buffer. Implements `ether_api_t::write`.

**Return values**

FSP_SUCCESS	Processing completed successfully.
FSP_ERR_ASSERTION	Pointer to ETHER control block is NULL.
FSP_ERR_NOT_OPEN	The control block has not been opened.
FSP_ERR_ETHER_ERROR_LINK	Auto-negotiation is not completed, and reception is not enabled.
FSP_ERR_ETHER_ERROR_MAGIC_PACKET_MODE	As a Magic Packet is being detected, transmission and reception is not enabled.
FSP_ERR_ETHER_ERROR_TRANSMIT_BUFFER_FULL	Transmit buffer is not empty.
FSP_ERR_INVALID_POINTER	Value of the pointer is NULL.
FSP_ERR_INVALID_ARGUMENT	Value of the send frame size is out of range.

◆ **R\_ETHER\_LinkProcess()**

```
fsp_err_t R_ETHER_LinkProcess ( ether_ctrl_t *const p_ctrl)
```

The Link up processing, the Link down processing, and the magic packet detection processing are executed. Implements `ether_api_t::linkProcess`.

**Return values**

FSP_SUCCESS	Link is up.
FSP_ERR_ASSERTION	Pointer to ETHER control block is NULL.
FSP_ERR_NOT_OPEN	The control block has not been opened.
FSP_ERR_ETHER_ERROR_LINK	Link is down.
FSP_ERR_ETHER_ERROR_PHY_COMMUNICATION	When reopening the PHY interface initialization of the PHY-LSI failed.
FSP_ERR_ALREADY_OPEN	When reopening the PHY interface it was already opened.
FSP_ERR_INVALID_CHANNEL	When reopening the PHY interface an invalid channel was passed.
FSP_ERR_INVALID_POINTER	When reopening the PHY interface the MAC address pointer was NULL.
FSP_ERR_INVALID_ARGUMENT	When reopening the PHY interface the interrupt was not enabled.
FSP_ERR_ETHER_PHY_ERROR_LINK	Initialization of the PHY-LSI failed.

◆ **R\_ETHER\_WakeOnLANEnable()**

```
fsp_err_t R_ETHER_WakeOnLANEnable ( ether_ctrl_t *const p_ctrl)
```

The setting of ETHERC is changed from normal sending and receiving mode to magic packet detection mode. Implements `ether_api_t::wakeOnLANEnable`.

**Return values**

FSP_SUCCESS	Processing completed successfully.
FSP_ERR_ASSERTION	Pointer to ETHER control block is NULL.
FSP_ERR_NOT_OPEN	The control block has not been opened.
FSP_ERR_ETHER_ERROR_LINK	Auto-negotiation is not completed, and reception is not enabled.
FSP_ERR_ETHER_PHY_ERROR_LINK	Initialization of PHY-LSI failed.

## ◆ R\_ETHER\_VersionGet()

```
__INLINE fsp_err_t R_ETHER_VersionGet ( fsp_version_t *const p_version)
```

Provides API and code version in the user provided pointer. Implements `ether_api_t::versionGet`.

**Return values**

FSP_SUCCESS	Version information stored in provided p_version.
FSP_ERR_ASSERTION	p_version is NULL.

**4.2.19 Ethernet PHY (r\_ether\_phy)**

## Modules

**Functions**

`fsp_err_t` `R_ETHER_PHY_Open` (`ether_phy_ctrl_t *const p_ctrl, ether_phy_cfg_t const *const p_cfg`)

Resets Ethernet PHY device. Implements `ether_phy_api_t::open`.  
[More...](#)

`fsp_err_t` `R_ETHER_PHY_Close` (`ether_phy_ctrl_t *const p_ctrl`)

Close Ethernet PHY device. Implements `ether_phy_api_t::close`.  
[More...](#)

`fsp_err_t` `R_ETHER_PHY_StartAutoNegotiate` (`ether_phy_ctrl_t *const p_ctrl`)

Starts auto-negotiate. Implements `ether_phy_api_t::startAutoNegotiate`. [More...](#)

`fsp_err_t` `R_ETHER_PHY_LinkPartnerAbilityGet` (`ether_phy_ctrl_t *const p_ctrl, uint32_t *const p_line_speed_duplex, uint32_t *const p_local_pause, uint32_t *const p_partner_pause`)

Reports the other side's physical capability. Implements `ether_phy_api_t::linkPartnerAbilityGet`. [More...](#)

`fsp_err_t` `R_ETHER_PHY_LinkStatusGet` (`ether_phy_ctrl_t *const p_ctrl`)

Returns the status of the physical link. Implements `ether_phy_api_t::linkStatusGet`. [More...](#)

```
fsp_err_t R_ETHER_PHY_VersionGet (fsp_version_t *const p_version)
```

Provides API and code version in the user provided pointer.  
Implements [ether\\_phy\\_api\\_t::versionGet](#). [More...](#)

## Detailed Description

The Ethernet PHY module (r\_ether\_phy) provides an API for standard Ethernet PHY communications applications that use the ETHERC peripheral. It implements the [Ethernet PHY Interface](#).

## Overview

The Ethernet PHY module is used to setup and manage an external Ethernet PHY device for use with the on-chip Ethernet Controller (ETHERC) peripheral. It performs auto-negotiation to determine the optimal connection parameters between link partners. Once initialized the connection between the external PHY and the onboard controller is automatically managed in hardware.

## Features

The Ethernet PHY module supports the following features:

- Auto negotiation support
- Flow control support
- Link status check support

## Configuration

### Build Time Configurations for r\_ether\_phy

The following build time configurations are defined in fsp\_cfg/r\_ether\_phy\_cfg.h:

Configuration	Options	Default	Description
Parameter Checking	<ul style="list-style-type: none"> <li>• Default (BSP)</li> <li>• Enabled</li> <li>• Disabled</li> </ul>	Default (BSP)	If selected code for parameter checking is included in the build.
Select PHY	<ul style="list-style-type: none"> <li>• Default</li> <li>• Other</li> <li>• KSZ8091RNB</li> <li>• KSZ8041</li> <li>• DP83620</li> </ul>	Default	Select PHY chip to use. Selecting 'Default' will automatically choose the correct option when using a Renesas development board.
Reference Clock	<ul style="list-style-type: none"> <li>• Default</li> <li>• Enabled</li> <li>• Disabled</li> </ul>	Default	Select whether to use the RMI reference clock. Selecting 'Default' will automatically choose the correct option when using a Renesas development board.



## Configurations for Driver > Network > Ethernet Driver on r\_ether\_phy

This module can be added to the Stacks tab via New Stack > Driver > Network > Ethernet Driver on r\_ether\_phy.

Configuration	Options	Default	Description
Name	Name must be a valid C symbol	g_ether_phy0	Module name.
Channel	<ul style="list-style-type: none"> <li>• 0</li> <li>• 1</li> </ul>	0	Select the Ethernet controller channel number.
PHY-LSI Address	Specify a value between 0 and 31.	0	Specify the address of the PHY-LSI used.
PHY-LSI Reset Completion Timeout	Specify a value between 0x1 and 0xFFFFFFFF.	0x00020000	Specify the number of times to read the PHY-LSI control register while waiting for reset completion. This value should be adjusted experimentally based on the PHY-LSI used.
Select MII type	<ul style="list-style-type: none"> <li>• MII</li> <li>• RMII</li> </ul>	MII	Specify whether to use MII or RMII.
MII/RMII Register Access Wait-time	Specify a value between 0x1 and 0x7FFFFFFF.	8	Specify the bit timing for MII/RMII register accesses during PHY initialization. This value should be adjusted experimentally based on the PHY-LSI used.
Flow Control	<ul style="list-style-type: none"> <li>• Disable</li> <li>• Enable</li> </ul>	Disable	Select whether to enable or disable flow control.

## Usage Notes

### Note

See the [example](#) below for details on how to initialize the Ethernet PHY module.

### Accessing the MII and RMII Registers

Use the PIR register to access the MII and RMII registers in the PHY-LSI. Serial data in the MII and RMII management frame format is transmitted and received through the ET0\_MDC and ET0\_MDIO pins controlled by software.

### MII and RMII management frame format

The below table lists the MII and RMII management frame formats.

Access type	MII and RMII management frame								
	Item	PRE	ST	OP	PHYAD	REGAD	TA	DATA	IDLE
	Number of bits	32	2	2	5	5	2	16	1
Read		1...1	01	10	00001	RRRRR	Z0	DDDDD DDDDD DDDDD D	Z
Write		1...1	01	01	00001	RRRRR	10	DDDDD DDDDD DDDDD D	Z

**Note**

- *PRE (preamble): Send 32 consecutive 1s.*
  - *ST (start of frame): Send 01b.*
  - *OP (operation code): Send 10b for read or 01b for write.*
  - *PHYAD (PHY address): Up to 32 PHY-LSIs can be connected to one MAC. PHY-LSIs are selected with these 5 bits. When the PHY-LSI address is 1, send 00001b.*
  - *REGAD (register address): One register is selected from up to 32 registers in the PHY-LSI. When the register address is 1, send 00001b.*
  - *TA (turnaround): Use 2-bit turnaround time to avoid contention between the register address and data during a read operation.*
- Send 10b during a write operation. Release the bus for 1 bit during a read operation (Z is output). (This is indicated as Z0 because 0 is output from the PHY-LSI on the next clock cycle.)*
- *DATA (data): 16-bit data. Sequentially send or receive starting from the MSB.*
  - *IDLE (IDLE condition): Wait time before inputting the next MII or RMII management format. Release the bus during a write operation (Z is output). No control is required, because a bus was already released during a read operation.*

**Limitations**

- The r\_ether\_phy module may need to be customized for PHY devices other than the ones currently supported (KSZ8091RNB, KSZ8041 and DP83620). Use the existing code as a starting point for creating a custom implementation.

**Examples****ETHER PHY Basic Example**

This is a basic example of minimal use of the ETHER PHY in an application.

```
void ether_phy_basic_example (void)
{
    fsp_err_t err = FSP_SUCCESS;

    g_ether_phy0_ctrl.open    = 0U;

    g_ether_phy0_cfg.channel = 0;

    /* Initializes the module. */
}
```

```

err = R_ETHER_PHY_Open(&g_ether_phy0_ctrl, &g_ether_phy0_cfg);
/* Handle any errors. This function should be defined by the user. */
handle_error(err);
/* Start auto negotiation. */
err = R_ETHER_PHY_StartAutoNegotiate(&g_ether_phy0_ctrl);
handle_error(err);
/* Polling until link is established. */
while (FSP_SUCCESS != R_ETHER_PHY_LinkStatusGet(&g_ether_phy0_ctrl))
{
/* Do nothing */
}
/* Get link partner ability from phy interface. */
err = R_ETHER_PHY_LinkPartnerAbilityGet(&g_ether_phy0_ctrl,
                                         &g_ether_phy0_line_speed_duplex,
                                         &g_ether_phy0_local_pause,
                                         &g_ether_phy0_partner_pause);

handle_error(err);
/* Check current link status. */
err = R_ETHER_PHY_LinkStatusGet(&g_ether_phy0_ctrl);
handle_error(err);
}

```

## Data Structures

struct [ether\\_phy\\_instance\\_ctrl\\_t](#)

## Data Structure Documentation

### ◆ ether\_phy\_instance\_ctrl\_t

struct ether_phy_instance_ctrl_t		
ETHER PHY control block. DO NOT INITIALIZE. Initialization occurs when <a href="#">ether_phy_api_t::open</a> is called.		
Data Fields		
uint32_t	open	Used to determine if the channel is configured.
<a href="#">ether_phy_cfg_t</a> const *	p_ether_phy_cfg	Pointer to initial configurations.
volatile uint32_t *	p_reg_pir	Pointer to ETHERC peripheral registers.

uint32_t	local_advertise	Capabilities bitmap for local advertising.
----------	-----------------	--------------------------------------------

## Function Documentation

### ◆ R\_ETHER\_PHY\_Open()

```
fsp_err_t R_ETHER_PHY_Open ( ether_phy_ctrl_t *const p_ctrl, ether_phy_cfg_t const *const p_cfg )
```

Resets Ethernet PHY device. Implements `ether_phy_api_t::open`.

#### Return values

FSP_SUCCESS	Channel opened successfully.
FSP_ERR_ASSERTION	Pointer to ETHER_PHY control block or configuration structure is NULL.
FSP_ERR_ALREADY_OPEN	Control block has already been opened or channel is being used by another instance. Call <code>close()</code> then <code>open()</code> to reconfigure.
FSP_ERR_INVALID_CHANNEL	Invalid channel number is given.
FSP_ERR_INVALID_POINTER	Pointer to <code>p_cfg</code> is NULL.
FSP_ERR_TIMEOUT	PHY-LSI Reset wait timeout.

### ◆ R\_ETHER\_PHY\_Close()

```
fsp_err_t R_ETHER_PHY_Close ( ether_phy_ctrl_t *const p_ctrl)
```

Close Ethernet PHY device. Implements `ether_phy_api_t::close`.

#### Return values

FSP_SUCCESS	Channel successfully closed.
FSP_ERR_ASSERTION	Pointer to ETHER_PHY control block is NULL.
FSP_ERR_NOT_OPEN	The control block has not been opened

◆ **R\_ETHER\_PHY\_StartAutoNegotiate()**

```
fsp_err_t R_ETHER_PHY_StartAutoNegotiate ( ether_phy_ctrl_t *const p_ctrl)
```

Starts auto-negotiate. Implements `ether_phy_api_t::startAutoNegotiate`.

**Return values**

FSP_SUCCESS	ETHER_PHY successfully starts auto-negotiate.
FSP_ERR_ASSERTION	Pointer to ETHER_PHY control block is NULL.
FSP_ERR_NOT_OPEN	The control block has not been opened

◆ **R\_ETHER\_PHY\_LinkPartnerAbilityGet()**

```
fsp_err_t R_ETHER_PHY_LinkPartnerAbilityGet ( ether_phy_ctrl_t *const p_ctrl, uint32_t *const p_line_speed_duplex, uint32_t *const p_local_pause, uint32_t *const p_partner_pause )
```

Reports the other side's physical capability. Implements `ether_phy_api_t::linkPartnerAbilityGet`.

**Return values**

FSP_SUCCESS	ETHER_PHY successfully get link partner ability.
FSP_ERR_ASSERTION	Pointer to ETHER_PHY control block is NULL.
FSP_ERR_INVALID_POINTER	Pointer to arguments are NULL.
FSP_ERR_NOT_OPEN	The control block has not been opened
FSP_ERR_ETHER_PHY_ERROR_LINK	PHY-LSI is not link up.
FSP_ERR_ETHER_PHY_NOT_READY	The auto-negotiation isn't completed

◆ **R\_ETHER\_PHY\_LinkStatusGet()**

```
fsp_err_t R_ETHER_PHY_LinkStatusGet ( ether_phy_ctrl_t *const p_ctrl)
```

Returns the status of the physical link. Implements `ether_phy_api_t::linkStatusGet`.

**Return values**

FSP_SUCCESS	ETHER_PHY successfully get link partner ability.
FSP_ERR_ASSERTION	Pointer to ETHER_PHY control block is NULL.
FSP_ERR_NOT_OPEN	The control block has not been opened
FSP_ERR_ETHER_PHY_ERROR_LINK	PHY-LSI is not link up.

◆ **R\_ETHER\_PHY\_VersionGet()**

```
__INLINE fsp_err_t R_ETHER_PHY_VersionGet ( fsp_version_t *const p_version)
```

Provides API and code version in the user provided pointer. Implements `ether_phy_api_t::versionGet`.

**Parameters**

[in]	p_version	Version number set here
------	-----------	-------------------------

**Return values**

FSP_SUCCESS	Version information stored in provided p_version.
FSP_ERR_ASSERTION	p_version is NULL.

**4.2.20 High-Performance Flash Driver (r\_flash\_hp)**

## Modules

**Functions**

fsp\_err\_t `R_FLASH_HP_Open` (flash\_ctrl\_t \*const p\_api\_ctrl, flash\_cfg\_t const \*const p\_cfg)

fsp\_err\_t `R_FLASH_HP_Write` (flash\_ctrl\_t \*const p\_api\_ctrl, uint32\_t const src\_address, uint32\_t flash\_address, uint32\_t const num\_bytes)

fsp\_err\_t `R_FLASH_HP_Erase` (flash\_ctrl\_t \*const p\_api\_ctrl, uint32\_t const address, uint32\_t const num\_blocks)

fsp\_err\_t `R_FLASH_HP_BlankCheck` (flash\_ctrl\_t \*const p\_api\_ctrl, uint32\_t const address, uint32\_t num\_bytes, flash\_result\_t \*blank\_check\_result)

fsp\_err\_t `R_FLASH_HP_Close` (flash\_ctrl\_t \*const p\_api\_ctrl)

fsp\_err\_t `R_FLASH_HP_StatusGet` (flash\_ctrl\_t \*const p\_api\_ctrl, flash\_status\_t \*const p\_status)

fsp\_err\_t `R_FLASH_HP_AccessWindowSet` (flash\_ctrl\_t \*const p\_api\_ctrl, uint32\_t const start\_addr, uint32\_t const end\_addr)

fsp\_err\_t `R_FLASH_HP_AccessWindowClear` (flash\_ctrl\_t \*const p\_api\_ctrl)

fsp\_err\_t `R_FLASH_HP_IdCodeSet` (flash\_ctrl\_t \*const p\_api\_ctrl, uint8\_t const \*const p\_id\_code, flash\_id\_code\_mode\_t mode)

```
fsp_err_t R_FLASH_HP_Reset (flash_ctrl_t *const p_api_ctrl)
```

```
fsp_err_t R_FLASH_HP_UpdateFlashClockFreq (flash_ctrl_t *const p_api_ctrl)
```

```
fsp_err_t R_FLASH_HP_StartUpAreaSelect (flash_ctrl_t *const p_api_ctrl,
flash_startup_area_swap_t swap_type, bool is_temporary)
```

```
fsp_err_t R_FLASH_HP_CallbackSet (flash_ctrl_t *const p_api_ctrl,
void(*p_callback)(flash_callback_args_t *), void const *const
p_context, flash_callback_args_t *const p_callback_memory)
```

```
fsp_err_t R_FLASH_HP_VersionGet (fsp_version_t *const p_version)
```

```
fsp_err_t R_FLASH_HP_InfoGet (flash_ctrl_t *const p_api_ctrl, flash_info_t
*const p_info)
```

## Detailed Description

Driver for the flash memory on RA high-performance MCUs. This module implements the [Flash Interface](#).

## Overview

The Flash HAL module APIs allow an application to write, erase and blank check both the data and ROM flash areas that reside within the MCU. The amount of flash memory available varies across MCU parts.

## Features

The R\_FLASH\_HP module has the following key features:

- Blocking and non-blocking erasing, writing and blank-checking of data flash.
- Blocking erasing, writing and blank-checking of code flash.
- Callback functions for completion of non-blocking data flash operations.
- Access window (write protection) for ROM Flash, allowing only specified areas of code flash to be erased or written.
- Boot block-swapping.
- ID code programming support.

## Configuration

### Build Time Configurations for r\_flash\_hp

The following build time configurations are defined in fsp\_cfg/r\_flash\_hp\_cfg.h:

Configuration	Options	Default	Description
Parameter Checking	<ul style="list-style-type: none"> <li>• Default (BSP)</li> <li>• Enabled</li> <li>• Disabled</li> </ul>	Default (BSP)	If selected code for parameter checking is included in the build.

Code Flash Programming Enable	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Disabled	Controls whether or not code-flash programming is enabled. Disabling reduces the amount of ROM and RAM used by the API.
Data Flash Programming Enable	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Enabled	Controls whether or not data-flash programming is enabled. Disabling reduces the amount of ROM used by the API.

### Configurations for Driver > Storage > Flash Driver on r\_flash\_hp

This module can be added to the Stacks tab via New Stack > Driver > Storage > Flash Driver on r\_flash\_hp. Non-secure callable guard functions can be generated for this module by right clicking the module in the RA Configuration tool and checking the "Non-secure Callable" box.

Configuration	Options	Default	Description
Name	Name must be a valid C symbol	g_flash0	Module name.
Data Flash Background Operation	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Enabled	Enabling allows Flash API calls that reference data-flash to return immediately, with the operation continuing in the background.
Callback	Name must be a valid C symbol	NULL	A user callback function can be specified. Callback function called when a dataflash BGO operation completes or errors.
Flash Ready Interrupt Priority	MCU Specific Options		Select the flash ready interrupt priority.
Flash Error Interrupt Priority	MCU Specific Options		Select the flash error interrupt priority.

### Clock Configuration

Flash uses FCLK as the clock source depending on the MCU. When writing and erasing the clock source must be at least 4 MHz.

### Pin Configuration

This module does not use I/O pins.



## Usage Notes

### Warning

It is highly recommended that the developer reviews sections 5 and 6 of the Flash Memory section of the target MCUs Hardware User's Manual prior to using the r\_flash\_hp module. In particular, understanding ID Code and Access Window functionality can help avoid unrecoverable flash scenarios.

### Data Flash Background Operation (BGO) Precautions

When using the data flash BGO (Background Operation) mode, you can still access the user ROM, RAM and external memory. You must ensure that the data flash is not accessed during a data flash operation. This includes interrupts that may access the data flash.

### Code Flash Precautions

Code flash cannot be accessed while writing, erasing or blank checking code flash. Code flash cannot be accessed while modifying the access window, selecting the startup area or setting the ID code. In order to support modifying code flash all supporting code must reside in RAM. This is only done when code flash programming is enabled. BGO mode is not supported for code flash, so a code flash operation will not return before the operation has completed. By default, the vector table resides in the code flash. If an interrupt occurs during the code flash operation, then code flash will be accessed to fetch the interrupt's starting address and an error will occur. The simplest work-around is to disable interrupts during code flash operations. Another option is to copy the vector table to RAM, update the VTOR (Vector Table Offset Register) accordingly and ensure that any interrupt service routines execute out of RAM. Similarly, you must insure that if in a multi-threaded environment, threads running from code flash cannot become active while a code flash operation is in progress.

### Flash Clock (FCLK)

The flash clock source is the clock used by the Flash peripheral in performing all Flash operations. As part of the [flash\\_api\\_t::open](#) function the Flash clock source is checked will return FSP\_ERR\_FCLK if it is invalid. Once the Flash API has been opened, if the flash clock source frequency is changed, the [flash\\_api\\_t::updateFlashClockFreq](#) API function must be called to inform the API of the change. Failure to do so could result in flash operation failures and possibly damage the part.

### Interrupts

Enable the flash ready interrupt only if you plan to use the data flash BGO. In this mode, the application can initiate a data flash operation and then be asynchronously notified of its completion, or an error, using a user supplied-callback function. The callback function is passed a structure containing event information that indicates the source of the callback event (for example, [flash\\_api\\_t::FLASH\\_EVENT\\_ERASE\\_COMPLETE](#)) When the FLASH FRDYI interrupt is enabled, the corresponding ISR will be defined in the flash driver. The ISR will call a user-callback function if one was registered with the [flash\\_api\\_t::open](#) API.

### Note

*The Flash HP supports an additional flash-error interrupt and if the BGO mode is enabled for the FLASH HP then both the Flash Ready Interrupt and Flash Error Interrupts must be enabled (assigned a priority).*

### Limitations

- Write operations must be aligned on page boundaries and must be a multiple of the page

- boundary size.
- Erase operations will erase the entire block the provided address resides in.
  - Data flash is better suited for storing data as it can be erased and written to while code is still executing from code flash. Data flash is also guaranteed for a larger number of reprogramming/erasure cycles than code flash.
  - Read values of erased data flash blocks are not guaranteed to be 0xFF. Blank check should be used to determine if memory has been erased but not yet programmed.

## Examples

### High-Performance Flash Basic Example

This is a basic example of erasing and writing to data flash and code flash.

```
#define FLASH_DF_BLOCK_0 0x40100000U /* 64 B: 0x40100000 - 0x4010003F */
#define FLASH_CF_BLOCK_8 0x00010000 /* 32 KB: 0x00010000 - 0x00017FFF */
#define FLASH_DATA_BLOCK_SIZE (1024)
#define FLASH_HP_EXAMPLE_WRITE_SIZE 32
uint8_t      g_dest[TRANSFER_LENGTH];
uint8_t      g_src[TRANSFER_LENGTH];
flash_result_t blank_check_result;
void r_flash_hp_basic_example (void)
{
    /* Initialize p_src to known data */
    for (uint32_t i = 0; i < TRANSFER_LENGTH; i++)
    {
        g_src[i] = (uint8_t) ('A' + (i % 26));
    }
    /* Open the flash hp instance. */
    fsp_err_t err = R_FLASH_HP_Open(&g_flash_ctrl, &g_flash_cfg);
    handle_error(err);
    /* Erase 1 block of data flash starting at block 0. */
    err = R_FLASH_HP_Erase(&g_flash_ctrl, FLASH_DF_BLOCK_0, 1);
    handle_error(err);
    /* Check if block 0 is erased. */
    err = R_FLASH_HP_BlankCheck(&g_flash_ctrl, FLASH_DF_BLOCK_0,
FLASH_DATA_BLOCK_SIZE, &blank_check_result);
    handle_error(err);
    /* Verify the previously erased area is blank */
```

```
if (FLASH_RESULT_NOT_BLANK == blank_check_result)
{
    handle_error(FSP_ERR_BLANK_CHECK_FAILED);
}

/* Write 32 bytes to the first block of data flash. */
err = R_FLASH_HP_Write(&g_flash_ctrl, (uint32_t) g_src, FLASH_DF_BLOCK_0,
FLASH_HP_EXAMPLE_WRITE_SIZE);
handle_error(err);
if (0 != memcmp(g_src, (uint8_t *) FLASH_DF_BLOCK_0, FLASH_HP_EXAMPLE_WRITE_SIZE))
{
    handle_error(FSP_ERR_WRITE_FAILED);
}

/* Disable interrupts to prevent vector table access while code flash is in P/E
mode. */
__disable_irq();

/* Erase 1 block of code flash starting at block 10. */
err = R_FLASH_HP_Erase(&g_flash_ctrl, FLASH_CF_BLOCK_8, 1);
handle_error(err);

/* Write 32 bytes to the first block of data flash. */
err = R_FLASH_HP_Write(&g_flash_ctrl, (uint32_t) g_src, FLASH_CF_BLOCK_8,
FLASH_HP_EXAMPLE_WRITE_SIZE);
handle_error(err);

/* Enable interrupts after code flash operations are complete. */
__enable_irq();
if (0 != memcmp(g_src, (uint8_t *) FLASH_CF_BLOCK_8, FLASH_HP_EXAMPLE_WRITE_SIZE))
{
    handle_error(FSP_ERR_WRITE_FAILED);
}
}
```

## High-Performance Flash Advanced Example

This example demonstrates using BGO to do non-blocking operations on the data flash.

```
bool interrupt_called;
```

```
flash_event_t flash_event;

static flash_cfg_t g_flash_bgo_example_cfg =
{
    .p_callback      = flash_callback,
    .p_context       = 0,
    .p_extend        = NULL,
    .data_flash_bgo = true,
    .ipl             = 5,
    .irq             = BSP_VECTOR_FLASH_HP_FRDYI_ISR,
};

void r_flash_hp_bgo_example (void)
{
    /* Initialize p_src to known data */
    for (uint32_t i = 0; i < TRANSFER_LENGTH; i++)
    {
        g_src[i] = (uint8_t) ('A' + (i % 26));
    }

    /* Open the flash hp instance. */
    fsp_err_t err = R_FLASH_HP_Open(&g_flash_ctrl, &g_flash_bgo_example_cfg);
    /* Handle any errors. This function should be defined by the user. */
    handle_error(err);

    interrupt_called = false;

    /* Erase 1 block of data flash starting at block 0. */
    err = R_FLASH_HP_Erase(&g_flash_ctrl, FLASH_DF_BLOCK_0, 1);
    handle_error(err);

    while (!interrupt_called)
    {
        ;
    }

    if (FLASH_EVENT_ERASE_COMPLETE != flash_event)
    {
        handle_error(FSP_ERR_ERASE_FAILED);
    }

    interrupt_called = false;
}
```

```
/* Write 32 bytes to the first block of data flash. */
err = R_FLASH_HP_Write(&g_flash_ctrl, (uint32_t) g_src, FLASH_DF_BLOCK_0,
FLASH_HP_EXAMPLE_WRITE_SIZE);

handle_error(err);

flash_status_t status;

/* Wait until the current flash operation completes. */
do
{
err = R_FLASH_HP_StatusGet(&g_flash_ctrl, &status);
} while ((FSP_SUCCESS == err) && (FLASH_STATUS_BUSY == status));

/* If the interrupt wasn't called process the error. */
if (!interrupt_called)
{
handle_error(FSP_ERR_WRITE_FAILED);
}

/* If the event wasn't a write complete process the error. */
if (FLASH_EVENT_WRITE_COMPLETE != flash_event)
{
handle_error(FSP_ERR_WRITE_FAILED);
}

/* Verify the data was written correctly. */
if (0 != memcmp(g_src, (uint8_t *) FLASH_DF_BLOCK_0, FLASH_HP_EXAMPLE_WRITE_SIZE))
{
handle_error(FSP_ERR_WRITE_FAILED);
}
}

void flash_callback (flash_callback_args_t * p_args)
{
interrupt_called = true;

flash_event      = p_args->event;
}
```

## Data Structures

```
struct flash_hp_instance_ctrl_t
```

## Enumerations

enum [flash\\_bgo\\_operation\\_t](#)

## Data Structure Documentation

### ◆ flash\_hp\_instance\_ctrl\_t

struct flash\_hp\_instance\_ctrl\_t

Flash HP instance control block. DO NOT INITIALIZE.

#### Data Fields

uint32_t	<a href="#">opened</a>
	To check whether api has been opened or not.
<a href="#">flash_bgo_operation_t</a>	<a href="#">current_operation</a>
	Operation in progress, for example, FLASH_OPERATION_CF_ERASE.

## Enumeration Type Documentation

### ◆ flash\_bgo\_operation\_t

enum [flash\\_bgo\\_operation\\_t](#)

Possible Flash operation states

## Function Documentation

◆ **R\_FLASH\_HP\_Open()**

```
fsp_err_t R_FLASH_HP_Open ( flash_ctrl_t *const p_api_ctrl, flash_cfg_t const *const p_cfg )
```

Initializes the high performance flash peripheral. Implements `flash_api_t::open`.

The Open function initializes the Flash.

Example:

```
/* Open the flash hp instance. */
fsp_err_t err = R_FLASH_HP_Open(&g_flash_ctrl, &g_flash_cfg);
```

**Return values**

FSP_SUCCESS	Initialization was successful and timer has started.
FSP_ERR_ALREADY_OPEN	The flash control block is already open.
FSP_ERR_ASSERTION	NULL provided for p_ctrl or p_cfg.
FSP_ERR_IRQ_BSP_DISABLED	Caller is requesting BGO but the Flash interrupts are not enabled.
FSP_ERR_FCLK	FCLK must be a minimum of 4 MHz for Flash operations.

◆ **R\_FLASH\_HP\_Write()**

```
fsp_err_t R_FLASH_HP_Write ( flash_ctrl_t *const p_api_ctrl, uint32_t const src_address, uint32_t
flash_address, uint32_t const num_bytes )
```

Writes to the specified Code or Data Flash memory area. Implements `flash_api_t::write`.

Example:

```
/* Write 32 bytes to the first block of data flash. */
err = R_FLASH_HP_Write(&g_flash_ctrl, (uint32_t) g_src, FLASH_DF_BLOCK_0,
FLASH_HP_EXAMPLE_WRITE_SIZE);
```

**Return values**

FSP_SUCCESS	Operation successful. If BGO is enabled this means the operation was started successfully.
FSP_ERR_IN_USE	The Flash peripheral is busy with a prior on-going transaction.
FSP_ERR_NOT_OPEN	The Flash API is not Open.
FSP_ERR_CMD_LOCKED	FCU is in locked state, typically as a result of attempting to Write an area that is protected by an Access Window.
FSP_ERR_WRITE_FAILED	Status is indicating a Programming error for the requested operation. This may be returned if the requested Flash area is not blank.
FSP_ERR_TIMEOUT	Timed out waiting for FCU operation to complete.
FSP_ERR_INVALID_SIZE	Number of bytes provided was not a multiple of the programming size or exceeded the maximum range.
FSP_ERR_INVALID_ADDRESS	Invalid address was input or address not on programming boundary.
FSP_ERR_ASSERTION	NULL provided for p_ctrl.
FSP_ERR_PE_FAILURE	Failed to enter or exit P/E mode.



### ◆ R\_FLASH\_HP\_Erase()

```
fsp_err_t R_FLASH_HP_Erase ( flash_ctrl_t *const p_api_ctrl, uint32_t const address, uint32_t const num_blocks )
```

Erases the specified Code or Data Flash blocks. Implements `flash_api_t::erase` by the `block_erase_address`.

#### Note

*Code flash may contain blocks of different sizes. When erasing code flash it is important to take this into consideration to prevent erasing a larger address space than desired.*

#### Example:

```
/* Erase 1 block of data flash starting at block 0. */
err = R_FLASH_HP_Erase(&g_flash_ctrl, FLASH_DF_BLOCK_0, 1);
```

#### Return values

FSP_SUCCESS	Successful open.
FSP_ERR_INVALID_BLOCKS	Invalid number of blocks specified
FSP_ERR_INVALID_ADDRESS	Invalid address specified. If the address is in code flash then code flash programming must be enabled.
FSP_ERR_IN_USE	Other flash operation in progress, or API not initialized
FSP_ERR_CMD_LOCKED	FCU is in locked state, typically as a result of attempting to Erase an area that is protected by an Access Window.
FSP_ERR_ASSERTION	NULL provided for p_ctrl
FSP_ERR_NOT_OPEN	The Flash API is not Open.
FSP_ERR_ERASE_FAILED	Status is indicating a Erase error.
FSP_ERR_TIMEOUT	Timed out waiting for the FCU to become ready.
FSP_ERR_PE_FAILURE	Failed to enter or exit P/E mode.

◆ **R\_FLASH\_HP\_BlankCheck()**

```
fsp_err_t R_FLASH_HP_BlankCheck ( flash_ctrl_t *const p_api_ctrl, uint32_t const address, uint32_t
num_bytes, flash_result_t * p_blank_check_result )
```

Performs a blank check on the specified address area. Implements `flash_api_t::blankCheck`.

Example:

```
/* Check if block 0 is erased. */
err = R_FLASH_HP_BlankCheck(&g_flash_ctrl, FLASH_DF_BLOCK_0,
FLASH_DATA_BLOCK_SIZE, &blank_check_result);
handle_error(err);
```

**Return values**

FSP_SUCCESS	Blank check operation completed with result in <code>p_blank_check_result</code> , or blank check started and in-progress (BGO mode).
FSP_ERR_INVALID_ADDRESS	Invalid data flash address was input.
FSP_ERR_INVALID_SIZE	'num_bytes' was either too large or not aligned for the CF/DF boundary size.
FSP_ERR_IN_USE	Other flash operation in progress or API not initialized.
FSP_ERR_ASSERTION	NULL provided for <code>p_ctrl</code> .
FSP_ERR_CMD_LOCKED	FCU is in locked state, typically as a result of attempting to Erase an area that is protected by an Access Window.
FSP_ERR_NOT_OPEN	The Flash API is not Open.
FSP_ERR_TIMEOUT	Timed out waiting for the FCU to become ready.
FSP_ERR_PE_FAILURE	Failed to enter or exit P/E mode.
FSP_ERR_BLANK_CHECK_FAILED	Blank check operation failed.

◆ **R\_FLASH\_HP\_Close()**

```
fsp_err_t R_FLASH_HP_Close ( flash_ctrl_t *const p_api_ctrl)
```

Releases any resources that were allocated by the Open() or any subsequent Flash operations. Implements `flash_api_t::close`.

**Return values**

FSP_SUCCESS	Successful close.
FSP_ERR_NOT_OPEN	The control block is not open.
FSP_ERR_ASSERTION	NULL provided for p_ctrl or p_cfg.

◆ **R\_FLASH\_HP\_StatusGet()**

```
fsp_err_t R_FLASH_HP_StatusGet ( flash_ctrl_t *const p_api_ctrl, flash_status_t *const p_status )
```

Query the FLASH peripheral for its status. Implements `flash_api_t::statusGet`.

Example:

```
flash_status_t status;

/* Wait until the current flash operation completes. */
do
{
    err = R_FLASH_HP_StatusGet(&g_flash_ctrl, &status);
} while ((FSP_SUCCESS == err) && (FLASH_STATUS_BUSY == status));
```

**Return values**

FSP_SUCCESS	FLASH peripheral is ready to use.
FSP_ERR_ASSERTION	NULL provided for p_ctrl.
FSP_ERR_NOT_OPEN	The Flash API is not Open.

### ◆ R\_FLASH\_HP\_AccessWindowSet()

```
fsp_err_t R_FLASH_HP_AccessWindowSet ( flash_ctrl_t *const p_api_ctrl, uint32_t const start_addr,
uint32_t const end_addr )
```

Configure an access window for the Code Flash memory using the provided start and end address. An access window defines a contiguous area in Code Flash for which programming/erase is enabled. This area is on block boundaries. The block containing start\_addr is the first block. The block containing end\_addr is the last block. The access window then becomes first block -> last block inclusive. Anything outside this range of Code Flash is then write protected.

#### Note

*If the start address and end address are set to the same value, then the access window is effectively removed. This accomplishes the same functionality as R\_FLASH\_HP\_AccessWindowClear().*

Implements [flash\\_api\\_t::accessWindowSet](#).

#### Return values

FSP_SUCCESS	Access window successfully configured.
FSP_ERR_INVALID_ADDRESS	Invalid settings for start_addr and/or end_addr.
FSP_ERR_IN_USE	FLASH peripheral is busy with a prior operation.
FSP_ERR_ASSERTION	NULL provided for p_ctrl.
FSP_ERR_UNSUPPORTED	Code Flash Programming is not enabled.
FSP_ERR_NOT_OPEN	Flash API has not yet been opened.
FSP_ERR_PE_FAILURE	Failed to enter or exit Code Flash P/E mode.
FSP_ERR_TIMEOUT	Timed out waiting for the FCU to become ready.
FSP_ERR_WRITE_FAILED	Status is indicating a Programming error for the requested operation.
FSP_ERR_CMD_LOCKED	FCU is in locked state, typically as a result of having received an illegal command.

◆ **R\_FLASH\_HP\_AccessWindowClear()**

```
fsp_err_t R_FLASH_HP_AccessWindowClear ( flash_ctrl_t *const p_api_ctrl)
```

Remove any access window that is currently configured in the Code Flash. Subsequent to this call all Code Flash is writable. Implements `flash_api_t::accessWindowClear`.

**Return values**

FSP_SUCCESS	Access window successfully removed.
FSP_ERR_IN_USE	FLASH peripheral is busy with a prior operation.
FSP_ERR_ASSERTION	NULL provided for p_ctrl.
FSP_ERR_UNSUPPORTED	Code Flash Programming is not enabled.
FSP_ERR_NOT_OPEN	Flash API has not yet been opened.
FSP_ERR_PE_FAILURE	Failed to enter or exit Code Flash P/E mode.
FSP_ERR_TIMEOUT	Timed out waiting for the FCU to become ready.
FSP_ERR_WRITE_FAILED	Status is indicating a Programming error for the requested operation.
FSP_ERR_CMD_LOCKED	FCU is in locked state, typically as a result of having received an illegal command.

◆ **R\_FLASH\_HP\_IdCodeSet()**

```
fsp_err_t R_FLASH_HP_IdCodeSet ( flash_ctrl_t *const p_api_ctrl, uint8_t const *const p_id_code,
flash_id_code_mode_t mode )
```

Implements `flash_api_t::idCodeSet`.

**Return values**

FSP_SUCCESS	ID Code successfully configured.
FSP_ERR_IN_USE	FLASH peripheral is busy with a prior operation.
FSP_ERR_ASSERTION	NULL provided for p_ctrl.
FSP_ERR_UNSUPPORTED	Code Flash Programming is not enabled.
FSP_ERR_NOT_OPEN	Flash API has not yet been opened.
FSP_ERR_PE_FAILURE	Failed to enter or exit Code Flash P/E mode.
FSP_ERR_TIMEOUT	Timed out waiting for the FCU to become ready.
FSP_ERR_WRITE_FAILED	Status is indicating a Programming error for the requested operation.
FSP_ERR_CMD_LOCKED	FCU is in locked state, typically as a result of having received an illegal command.

◆ **R\_FLASH\_HP\_Reset()**

```
fsp_err_t R_FLASH_HP_Reset ( flash_ctrl_t *const p_api_ctrl)
```

Reset the FLASH peripheral. Implements `flash_api_t::reset`.

No attempt is made to check if the flash is busy before executing the reset since the assumption is that a reset will terminate any existing operation.

**Return values**

FSP_SUCCESS	Flash circuit successfully reset.
FSP_ERR_ASSERTION	NULL provided for p_ctrl.
FSP_ERR_NOT_OPEN	The control block is not open.
FSP_ERR_PE_FAILURE	Failed to enter or exit P/E mode.
FSP_ERR_TIMEOUT	Timed out waiting for the FCU to become ready.
FSP_ERR_CMD_LOCKED	FCU is in locked state, typically as a result of having received an illegal command.

### ◆ R\_FLASH\_HP\_UpdateFlashClockFreq()

`fsp_err_t R_FLASH_HP_UpdateFlashClockFreq ( flash_ctrl_t *const p_api_ctrl)`

Indicate to the already open Flash API that the FCLK has changed. Implements `flash_api_t::updateFlashClockFreq`.

This could be the case if the application has changed the system clock, and therefore the FCLK. Failure to call this function subsequent to changing the FCLK could result in damage to the flash macro.

#### Return values

FSP_SUCCESS	Start-up area successfully toggled.
FSP_ERR_IN_USE	Flash is busy with an on-going operation.
FSP_ERR_ASSERTION	NULL provided for p_ctrl
FSP_ERR_NOT_OPEN	Flash API has not yet been opened.
FSP_ERR_FCLK	FCLK is not within the acceptable range.

### ◆ R\_FLASH\_HP\_StartUpAreaSelect()

```
fsp_err_t R_FLASH_HP_StartUpAreaSelect ( flash_ctrl_t *const p_api_ctrl, flash_startup_area_swap_t swap_type, bool is_temporary )
```

Selects which block, Default (Block 0) or Alternate (Block 1), is used as the startup area block. The provided parameters determine which block will become the active startup block and whether that action will be immediate (but temporary), or permanent subsequent to the next reset. Doing a temporary switch might appear to have limited usefulness. If there is an access window in place such that Block 0 is write protected, then one could do a temporary switch, update the block and switch them back without having to touch the access window. Implements [flash\\_api\\_t::startupAreaSelect](#).

#### Return values

FSP_SUCCESS	Start-up area successfully toggled.
FSP_ERR_IN_USE	FLASH peripheral is busy with a prior operation.
FSP_ERR_ASSERTION	NULL provided for p_ctrl.
FSP_ERR_NOT_OPEN	The control block is not open.
FSP_ERR_UNSUPPORTED	Code Flash Programming is not enabled.
FSP_ERR_PE_FAILURE	Failed to enter or exit Code Flash P/E mode.
FSP_ERR_TIMEOUT	Timed out waiting for the FCU to become ready.
FSP_ERR_WRITE_FAILED	Status is indicating a Programming error for the requested operation.
FSP_ERR_CMD_LOCKED	FCU is in locked state, typically as a result of having received an illegal command.



◆ **R\_FLASH\_HP\_CallbackSet()**

```
fsp_err_t R_FLASH_HP_CallbackSet ( flash_ctrl_t *const p_api_ctrl, void(*) (flash_callback_args_t *)
p_callback, void const *const p_context, flash_callback_args_t *const p_callback_memory )
```

Updates the user callback with the option to provide memory for the callback argument structure. Implements `flash_api_t::callbackSet`.

**Return values**

FSP_SUCCESS	Callback updated successfully.
FSP_ERR_ASSERTION	A required pointer is NULL.
FSP_ERR_NOT_OPEN	The control block has not been opened.
FSP_ERR_NO_CALLBACK_MEMORY	<code>p_callback</code> is non-secure and <code>p_callback_memory</code> is either secure or NULL.

◆ **R\_FLASH\_HP\_VersionGet()**

```
fsp_err_t R_FLASH_HP_VersionGet ( fsp_version_t *const p_version)
```

This function gets FLASH HAL driver version

**Return values**

FSP_SUCCESS	Operation performed successfully
FSP_ERR_ASSERTION	Null pointer

◆ **R\_FLASH\_HP\_InfoGet()**

```
fsp_err_t R_FLASH_HP_InfoGet ( flash_ctrl_t *const p_api_ctrl, flash_info_t *const p_info )
```

Returns the information about the flash regions. Implements `flash_api_t::infoGet`.

**Return values**

FSP_SUCCESS	Successful retrieved the request information.
FSP_ERR_NOT_OPEN	The control block is not open.
FSP_ERR_ASSERTION	NULL provided for <code>p_ctrl</code> or <code>p_info</code> .

**4.2.21 Low-Power Flash Driver (r\_flash\_lp)**

## Modules

### Functions

fsp_err_t	R_FLASH_LP_Open (flash_ctrl_t *const p_api_ctrl, flash_cfg_t const *const p_cfg)
fsp_err_t	R_FLASH_LP_Write (flash_ctrl_t *const p_api_ctrl, uint32_t const src_address, uint32_t flash_address, uint32_t const num_bytes)
fsp_err_t	R_FLASH_LP_Erase (flash_ctrl_t *const p_api_ctrl, uint32_t const address, uint32_t const num_blocks)
fsp_err_t	R_FLASH_LP_BlankCheck (flash_ctrl_t *const p_api_ctrl, uint32_t const address, uint32_t num_bytes, flash_result_t *blank_check_result)
fsp_err_t	R_FLASH_LP_Close (flash_ctrl_t *const p_api_ctrl)
fsp_err_t	R_FLASH_LP_StatusGet (flash_ctrl_t *const p_api_ctrl, flash_status_t *const p_status)
fsp_err_t	R_FLASH_LP_AccessWindowSet (flash_ctrl_t *const p_api_ctrl, uint32_t const start_addr, uint32_t const end_addr)
fsp_err_t	R_FLASH_LP_AccessWindowClear (flash_ctrl_t *const p_api_ctrl)
fsp_err_t	R_FLASH_LP_IdCodeSet (flash_ctrl_t *const p_api_ctrl, uint8_t const *const p_id_code, flash_id_code_mode_t mode)
fsp_err_t	R_FLASH_LP_Reset (flash_ctrl_t *const p_api_ctrl)
fsp_err_t	R_FLASH_LP_StartUpAreaSelect (flash_ctrl_t *const p_api_ctrl, flash_startup_area_swap_t swap_type, bool is_temporary)
fsp_err_t	R_FLASH_LP_CallbackSet (flash_ctrl_t *const p_api_ctrl, void(*p_callback)(flash_callback_args_t *), void const *const p_context, flash_callback_args_t *const p_callback_memory)
fsp_err_t	R_FLASH_LP_UpdateFlashClockFreq (flash_ctrl_t *const p_api_ctrl)
fsp_err_t	R_FLASH_LP_VersionGet (fsp_version_t *const p_version)
fsp_err_t	R_FLASH_LP_InfoGet (flash_ctrl_t *const p_api_ctrl, flash_info_t *const p_info)

### Detailed Description

Driver for the flash memory on RA low-power MCUs. This module implements the [Flash Interface](#).

## Overview

The Flash HAL module APIs allow an application to write, erase and blank check both the data and code flash areas that reside within the MCU. The amount of flash memory available varies across MCU parts.

### Features

The Low-Power Flash HAL module has the following key features:

- Blocking and non-blocking erasing, writing and blank-checking of data flash.
- Blocking erasing, writing and blank checking of code flash.
- Callback functions for completion of non-blocking data flash operations.
- Access window (write protection) for code flash, allowing only specified areas of code flash to be erased or written.
- Boot block-swapping.
- ID code programming support.

## Configuration

### Build Time Configurations for r\_flash\_lp

The following build time configurations are defined in fsp\_cfg/r\_flash\_lp\_cfg.h:

Configuration	Options	Default	Description
Parameter Checking	<ul style="list-style-type: none"> <li>• Default (BSP)</li> <li>• Enabled</li> <li>• Disabled</li> </ul>	Default (BSP)	If selected code for parameter checking is included in the build.
Code Flash Programming	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Disabled	Controls whether or not code-flash programming is enabled. Disabling reduces the amount of ROM and RAM used by the API.
Data Flash Programming	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Enabled	Controls whether or not data-flash programming is enabled. Disabling reduces the amount of ROM used by the API.

### Configurations for Driver > Storage > Flash Driver on r\_flash\_lp

This module can be added to the Stacks tab via New Stack > Driver > Storage > Flash Driver on r\_flash\_lp.

Configuration	Options	Default	Description
Name	Name must be a valid C symbol	g_flash0	Module name.

Data Flash Background Operation	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Enabled	Enabling allows Flash API calls that reference data-flash to return immediately, with the operation continuing in the background.
Callback	Name must be a valid C symbol	NULL	A user callback function can be specified. Callback function called when a dataflash BGO operation completes or errors.
Flash Ready Interrupt Priority	MCU Specific Options		Select the flash ready interrupt priority.

## Clock Configuration

Flash either uses FCLK or ICLK as the clock source depending on the MCU. When writing and erasing the clock source must be at least 4 MHz.

## Pin Configuration

This module does not use I/O pins.

## Usage Notes

### Warning

It is highly recommended that the developer reviews sections 5 and 6 of the Flash Memory section of the target MCUs Hardware User's Manual prior to using the r\_flash\_lp module. In particular, understanding ID Code and Access Window functionality can help avoid unrecoverable flash scenarios.

## Data Flash Background Operation (BGO) Precautions

When using the data flash BGO, the code flash, RAM and external memory can still be accessed. You must ensure that the data flash is not accessed during a data flash operation. This includes interrupts that may access the data flash.

## Code Flash Precautions

Code flash cannot be accessed while writing, erasing or blank checking code flash. Code flash cannot be accessed while modifying the access window, selecting the startup area or setting the ID code. In order to support modifying code flash all supporting code must reside in RAM. This is only done when code flash programming is enabled. BGO mode is not supported for code flash, so a code flash operation will not return before the operation has completed. By default, the vector table resides in the code flash. If an interrupt occurs during the code flash operation, then code flash will be accessed to fetch the interrupt's starting address and an error will occur. The simplest work-around is to disable interrupts during code flash operations. Another option is to copy the vector table to RAM, update the VTOR (Vector Table Offset Register) accordingly and ensure that any interrupt service routines execute out of RAM. Similarly, you must insure that if in a multi-threaded environment, threads running from code flash cannot become active while a code flash operation is in progress.

## Flash Clock Source

The flash clock source is the clock used by the Flash peripheral in performing all Flash operations. As part of the `flash_api_t::open` function the Flash clock source is checked will return `FSP_ERR_FCLK` if it is invalid. Once the Flash API has been opened, if the flash clock source frequency is changed, the `flash_api_t::updateFlashClockFreq` API function must be called to inform the API of the change. Failure to do so could result in flash operation failures and possibly damage the part.

## Interrupts

Enable the flash ready interrupt only if you plan to use the data flash BGO. In this mode, the application can initiate a data flash operation and then be asynchronously notified of its completion, or an error, using a user supplied-callback function. The callback function is passed a structure containing event information that indicates the source of the callback event (for example, `flash_api_t::FLASH_EVENT_ERASE_COMPLETE`) When the FLASH FRDYI interrupt is enabled, the corresponding ISR will be defined in the flash driver. The ISR will call a user-callback function if one was registered with the `flash_api_t::open` API.

### Note

*The Flash HP supports an additional flash-error interrupt and if the BGO mode is enabled for the FLASH HP then both the Flash Ready Interrupt and Flash Error Interrupts must be enabled (assigned a priority).*

## Limitations

- Write operations must be aligned on page boundaries and must be a multiple of the page boundary size.
- Erase operations will erase the entire block the provided address resides in.
- Data flash is better suited for storing data as it can be erased and written to while code is still executing from code flash. Data flash is also guaranteed for a larger number of reprogramming/erasure cycles than code flash.
- Read values of erased blocks are not guaranteed to be 0xFF. Blank check should be used to determine if memory has been erased but not yet programmed.

## Examples

### Low-Power Flash Basic Example

This is a basic example of erasing and writing to data flash and code flash.

```
#define FLASH_DF_BLOCK_0 0x40100000U /* 1 KB: 0x40100000 - 0x401003FF */
#define FLASH_CF_BLOCK_10 0x00005000 /* 2 KB: 0x00005000 - 0x000057FF */
#define FLASH_DATA_BLOCK_SIZE (1024)
#define FLASH_LP_EXAMPLE_WRITE_SIZE 32
uint8_t      g_dest[TRANSFER_LENGTH];
uint8_t      g_src[TRANSFER_LENGTH];
flash_result_t blank_check_result;
void R_FLASH_LP_basic_example (void)
{
```

```
/* Initialize p_src to known data */
for (uint32_t i = 0; i < TRANSFER_LENGTH; i++)
{
    g_src[i] = (uint8_t) ('A' + (i % 26));
}

/* Open the flash lp instance. */
fsp_err_t err = R_FLASH_LP_Open(&g_flash_ctrl, &g_flash_cfg);
    handle_error(err);

/* Erase 1 block of data flash starting at block 0. */
err = R_FLASH_LP_Erase(&g_flash_ctrl, FLASH_DF_BLOCK_0, 1);
    handle_error(err);

/* Check if block 0 is erased. */
err = R_FLASH_LP_BlankCheck(&g_flash_ctrl, FLASH_DF_BLOCK_0,
FLASH_DATA_BLOCK_SIZE, &blank_check_result);
    handle_error(err);

/* Verify the previously erased area is blank */
if (FLASH_RESULT_NOT_BLANK == blank_check_result)
{
    handle_error(FSP_ERR_BLANK_CHECK_FAILED);
}

/* Write 32 bytes to the first block of data flash. */
err = R_FLASH_LP_Write(&g_flash_ctrl, (uint32_t) g_src, FLASH_DF_BLOCK_0,
FLASH_LP_EXAMPLE_WRITE_SIZE);
    handle_error(err);

if (0 != memcmp(g_src, (uint8_t *) FLASH_DF_BLOCK_0, FLASH_LP_EXAMPLE_WRITE_SIZE))
{
    handle_error(FSP_ERR_WRITE_FAILED);
}

/* Disable interrupts to prevent vector table access while code flash is in P/E
mode. */
__disable_irq();

/* Erase 1 block of code flash starting at block 10. */
err = R_FLASH_LP_Erase(&g_flash_ctrl, FLASH_CF_BLOCK_10, 1);
    handle_error(err);
```

```
/* Write 32 bytes to the first block of data flash. */
err = R_FLASH_LP_Write(&g_flash_ctrl, (uint32_t) g_src, FLASH_CF_BLOCK_10,
FLASH_LP_EXAMPLE_WRITE_SIZE);

handle_error(err);

/* Enable interrupts after code flash operations are complete. */
__enable_irq();

if (0 != memcmp(g_src, (uint8_t *) FLASH_CF_BLOCK_10, FLASH_LP_EXAMPLE_WRITE_SIZE))
{
    handle_error(FSP_ERR_WRITE_FAILED);
}
}
```

### Low-Power Flash Advanced Example

This example demonstrates using BGO to do non-blocking operations on the data flash.

```
bool interrupt_called;
flash_event_t flash_event;
static flash_cfg_t g_flash_bgo_example_cfg =
{
    .p_callback    = flash_callback,
    .p_context     = 0,
    .p_extend      = NULL,
    .data_flash_bgo = true,
    .ipl           = 5,
    .irq           = BSP_VECTOR_FLASH_LP_FRDYI_ISR,
};

void R_FLASH_LP_bgo_example (void)
{
    /* Initialize p_src to known data */
    for (uint32_t i = 0; i < TRANSFER_LENGTH; i++)
    {
        g_src[i] = (uint8_t) ('A' + (i % 26));
    }

    /* Open the flash lp instance. */
```

```
fsp_err_t err = R_FLASH_LP_Open(&g_flash_ctrl, &g_flash_bgo_example_cfg);
/* Handle any errors. This function should be defined by the user. */
    handle_error(err);
    interrupt_called = false;
/* Erase 1 block of data flash starting at block 0. */
    err = R_FLASH_LP_Erase(&g_flash_ctrl, FLASH_DF_BLOCK_0, 1);
    handle_error(err);
while (!interrupt_called)
    {
        ;
    }
if (FLASH_EVENT_ERASE_COMPLETE != flash_event)
    {
        handle_error(FSP_ERR_ERASE_FAILED);
    }
    interrupt_called = false;
/* Write 32 bytes to the first block of data flash. */
    err = R_FLASH_LP_Write(&g_flash_ctrl, (uint32_t) g_src, FLASH_DF_BLOCK_0,
FLASH_LP_EXAMPLE_WRITE_SIZE);
    handle_error(err);
    flash_status_t status;
/* Wait until the current flash operation completes. */
do
    {
        err = R_FLASH_LP_StatusGet(&g_flash_ctrl, &status);
    } while ((FSP_SUCCESS == err) && (FLASH_STATUS_BUSY == status));
/* If the interrupt wasn't called process the error. */
if (!interrupt_called)
    {
        handle_error(FSP_ERR_WRITE_FAILED);
    }
/* If the event wasn't a write complete process the error. */
if (FLASH_EVENT_WRITE_COMPLETE != flash_event)
    {
```



```
    handle_error(FSP_ERR_WRITE_FAILED);
}

/* Verify the data was written correctly. */
if (0 != memcmp(g_src, (uint8_t *) FLASH_DF_BLOCK_0, FLASH_LP_EXAMPLE_WRITE_SIZE))
{
    handle_error(FSP_ERR_WRITE_FAILED);
}
}

void flash_callback (flash_callback_args_t * p_args)
{
    interrupt_called = true;
    flash_event      = p_args->event;
}
}
```

## Data Structures

```
struct flash_lp_instance_ctrl_t
```

## Data Structure Documentation

### ◆ flash\_lp\_instance\_ctrl\_t

```
struct flash_lp_instance_ctrl_t
```

Flash instance control block. DO NOT INITIALIZE. Initialization occurs when [R\\_FLASH\\_LP\\_Open\(\)](#) is called.

## Function Documentation

◆ **R\_FLASH\_LP\_Open()**

```
fsp_err_t R_FLASH_LP_Open ( flash_ctrl_t *const p_api_ctrl, flash_cfg_t const *const p_cfg )
```

Initialize the Low Power flash peripheral. Implements `flash_api_t::open`.

The Open function initializes the Flash.

This function must be called once prior to calling any other FLASH API functions. If a user supplied callback function is supplied, then the Flash Ready interrupt will be configured to call the users callback routine with an Event type describing the source of the interrupt for Data Flash operations.

Example:

```
/* Open the flash lp instance. */
fsp_err_t err = R_FLASH_LP_Open(&g_flash_ctrl, &g_flash_cfg);
```

**Note**

*Providing a callback function in the supplied `p_cfg->callback` field automatically configures the Flash for Data Flash to operate in non-blocking background operation (BGO) mode.*

**Return values**

FSP_SUCCESS	Initialization was successful and timer has started.
FSP_ERR_ASSERTION	NULL provided for <code>p_ctrl</code> , <code>p_cfg</code> or <code>p_callback</code> if BGO is enabled.
FSP_ERR_IRQ_BSP_DISABLED	Caller is requesting BGO but the Flash interrupts are not enabled.
FSP_ERR_FCLK	FCLK must be a minimum of 4 MHz for Flash operations.
FSP_ERR_ALREADY_OPEN	Flash Open() has already been called.
FSP_ERR_TIMEOUT	Failed to exit P/E mode after configuring flash.

◆ **R\_FLASH\_LP\_Write()**

```
fsp_err_t R_FLASH_LP_Write ( flash_ctrl_t *const p_api_ctrl, uint32_t const src_address, uint32_t
flash_address, uint32_t const num_bytes )
```

Write to the specified Code or Data Flash memory area. Implements `flash_api_t::write`.

Example:

```
/* Write 32 bytes to the first block of data flash. */
err = R_FLASH_LP_Write(&g_flash_ctrl, (uint32_t) g_src, FLASH_DF_BLOCK_0,
FLASH_LP_EXAMPLE_WRITE_SIZE);
```

**Return values**

FSP_SUCCESS	Operation successful. If BGO is enabled this means the operation was started successfully.
FSP_ERR_IN_USE	The Flash peripheral is busy with a prior on-going transaction.
FSP_ERR_NOT_OPEN	The Flash API is not Open.
FSP_ERR_WRITE_FAILED	Status is indicating a Programming error for the requested operation. This may be returned if the requested Flash area is not blank.
FSP_ERR_TIMEOUT	Timed out waiting for FCU operation to complete.
FSP_ERR_INVALID_SIZE	Number of bytes provided was not a multiple of the programming size or exceeded the maximum range.
FSP_ERR_INVALID_ADDRESS	Invalid address was input or address not on programming boundary.
FSP_ERR_ASSERTION	NULL provided for p_ctrl.

◆ **R\_FLASH\_LP\_Erase()**

```
fsp_err_t R_FLASH_LP_Erase ( flash_ctrl_t *const p_api_ctrl, uint32_t const address, uint32_t const num_blocks )
```

Erase the specified Code or Data Flash blocks. Implements `flash_api_t::erase`.

Example:

```
/* Erase 1 block of data flash starting at block 0. */
err = R_FLASH_LP_Erase(&g_flash_ctrl, FLASH_DF_BLOCK_0, 1);
```

**Return values**

FSP_SUCCESS	Successful open.
FSP_ERR_INVALID_BLOCKS	Invalid number of blocks specified
FSP_ERR_INVALID_ADDRESS	Invalid address specified
FSP_ERR_IN_USE	Other flash operation in progress, or API not initialized
FSP_ERR_ASSERTION	NULL provided for p_ctrl
FSP_ERR_NOT_OPEN	The Flash API is not Open.
FSP_ERR_TIMEOUT	Timed out waiting for FCU to be ready.
FSP_ERR_ERASE_FAILED	Status is indicating a Erase error.

◆ **R\_FLASH\_LP\_BlankCheck()**

```
fsp_err_t R_FLASH_LP_BlankCheck ( flash_ctrl_t *const p_api_ctrl, uint32_t const address, uint32_t
num_bytes, flash_result_t * p_blank_check_result )
```

Perform a blank check on the specified address area. Implements `flash_api_t::blankCheck`.

Example:

```
/* Check if block 0 is erased. */
err = R_FLASH_LP_BlankCheck(&g_flash_ctrl, FLASH_DF_BLOCK_0,
FLASH_DATA_BLOCK_SIZE, &blank_check_result);
handle_error(err);
```

**Return values**

FSP_SUCCESS	Blankcheck operation completed with result in p_blank_check_result, or blankcheck started and in-progress (BGO mode).
FSP_ERR_INVALID_ADDRESS	Invalid data flash address was input
FSP_ERR_INVALID_SIZE	'num_bytes' was either too large or not aligned for the CF/DF boundary size.
FSP_ERR_IN_USE	Flash is busy with an on-going operation.
FSP_ERR_ASSERTION	NULL provided for p_ctrl
FSP_ERR_NOT_OPEN	Flash API has not yet been opened.
FSP_ERR_TIMEOUT	Timed out waiting for the FCU to become ready.
FSP_ERR_BLANK_CHECK_FAILED	An error occurred during blank checking.

◆ **R\_FLASH\_LP\_Close()**

```
fsp_err_t R_FLASH_LP_Close ( flash_ctrl_t *const p_api_ctrl)
```

Release any resources that were allocated by the Flash API. Implements `flash_api_t::close`.

**Return values**

FSP_SUCCESS	Successful close.
FSP_ERR_ASSERTION	NULL provided for p_ctrl or p_cfg.
FSP_ERR_NOT_OPEN	Flash API has not yet been opened.
FSP_ERR_IN_USE	The flash is currently in P/E mode.

**◆ R\_FLASH\_LP\_StatusGet()**

```
fsp_err_t R_FLASH_LP_StatusGet ( flash_ctrl_t *const p_api_ctrl, flash_status_t *const p_status )
```

Query the FLASH for its status. Implements `flash_api_t::statusGet`.

Example:

```
flash_status_t status;

/* Wait until the current flash operation completes. */
do
{
    err = R_FLASH_LP_StatusGet(&g_flash_ctrl, &status);
} while ((FSP_SUCCESS == err) && (FLASH_STATUS_BUSY == status));
```

**Return values**

FSP_SUCCESS	Flash is ready and available to accept commands.
FSP_ERR_ASSERTION	NULL provided for p_ctrl
FSP_ERR_NOT_OPEN	Flash API has not yet been opened.

### ◆ R\_FLASH\_LP\_AccessWindowSet()

```
fsp_err_t R_FLASH_LP_AccessWindowSet ( flash_ctrl_t *const p_api_ctrl, uint32_t const start_addr,
uint32_t const end_addr )
```

Configure an access window for the Code Flash memory. Implements `flash_api_t::accessWindowSet`.

An access window defines a contiguous area in Code Flash for which programming/erase is enabled. This area is on block boundaries. The block containing `start_addr` is the first block. The block containing `end_addr` is the last block. The access window then becomes first block (inclusive) -> last block (exclusive). Anything outside this range of Code Flash is then write protected. As an example, if you wanted to place an accesswindow on Code Flash Blocks 0 and 1, such that only those two blocks were writable, you would need to specify (address in block 0, address in block 2) as the respective start and end address.

#### Note

*If the start address and end address are set to the same value, then the access window is effectively removed. This accomplishes the same functionality as `R_FLASH_LP_AccessWindowClear()`.*

The invalid address and programming boundaries supported and enforced by this function are dependent on the MCU in use as well as the part package size. Please see the User manual and/or requirements document for additional information.

#### Parameters

	<code>p_api_ctrl</code>	The p api control
[in]	<code>start_addr</code>	The start address
[in]	<code>end_addr</code>	The end address

#### Return values

<code>FSP_SUCCESS</code>	Access window successfully configured.
<code>FSP_ERR_INVALID_ADDRESS</code>	Invalid settings for <code>start_addr</code> and/or <code>end_addr</code> .
<code>FSP_ERR_IN_USE</code>	FLASH peripheral is busy with a prior operation.
<code>FSP_ERR_ASSERTION</code>	NULL provided for <code>p_ctrl</code> .
<code>FSP_ERR_UNSUPPORTED</code>	Code Flash Programming is not enabled.
<code>FSP_ERR_NOT_OPEN</code>	Flash API has not yet been opened.
<code>FSP_ERR_TIMEOUT</code>	Timed out waiting for the FCU to become ready.
<code>FSP_ERR_WRITE_FAILED</code>	Status is indicating a Programming error for the requested operation.

◆ **R\_FLASH\_LP\_AccessWindowClear()**

```
fsp_err_t R_FLASH_LP_AccessWindowClear ( flash_ctrl_t *const p_api_ctrl)
```

Remove any access window that is configured in the Code Flash. Implements `flash_api_t::accessWindowClear`. On successful return from this call all Code Flash is writable.

**Return values**

FSP_SUCCESS	Access window successfully removed.
FSP_ERR_IN_USE	FLASH peripheral is busy with a prior operation.
FSP_ERR_ASSERTION	NULL provided for p_ctrl.
FSP_ERR_UNSUPPORTED	Code Flash Programming is not enabled.
FSP_ERR_NOT_OPEN	Flash API has not yet been opened.
FSP_ERR_TIMEOUT	Timed out waiting for the FCU to become ready.
FSP_ERR_WRITE_FAILED	Status is indicating a Programming error for the requested operation.

◆ **R\_FLASH\_LP\_IdCodeSet()**

```
fsp_err_t R_FLASH_LP_IdCodeSet ( flash_ctrl_t *const p_api_ctrl, uint8_t const *const p_id_code, flash_id_code_mode_t mode )
```

Write the ID code provided to the id code registers. Implements `flash_api_t::idCodeSet`.

**Return values**

FSP_SUCCESS	ID code successfully configured.
FSP_ERR_IN_USE	FLASH peripheral is busy with a prior operation.
FSP_ERR_ASSERTION	NULL provided for p_ctrl.
FSP_ERR_UNSUPPORTED	Code Flash Programming is not enabled.
FSP_ERR_NOT_OPEN	Flash API has not yet been opened.
FSP_ERR_TIMEOUT	Timed out waiting for completion of extra command.
FSP_ERR_WRITE_FAILED	Status is indicating a Programming error for the requested operation.



◆ **R\_FLASH\_LP\_Reset()**

```
fsp_err_t R_FLASH_LP_Reset ( flash_ctrl_t *const p_api_ctrl)
```

Reset the FLASH peripheral. Implements `flash_api_t::reset`.

No attempt is made to check if the flash is busy before executing the reset since the assumption is that a reset will terminate any existing operation.

**Return values**

FSP_SUCCESS	Flash circuit successfully reset.
FSP_ERR_ASSERTION	NULL provided for p_ctrl
FSP_ERR_NOT_OPEN	Flash API has not yet been opened.

◆ **R\_FLASH\_LP\_StartUpAreaSelect()**

```
fsp_err_t R_FLASH_LP_StartUpAreaSelect ( flash_ctrl_t *const p_api_ctrl, flash_startup_area_swap_t swap_type, bool is_temporary )
```

Select which block is used as the startup area block. Implements `flash_api_t::startupAreaSelect`.

Selects which block - Default (Block 0) or Alternate (Block 1) is used as the startup area block. The provided parameters determine which block will become the active startup block and whether that action will be immediate (but temporary), or permanent subsequent to the next reset. Doing a temporary switch might appear to have limited usefulness. If there is an access window in place such that Block 0 is write protected, then one could do a temporary switch, update the block and switch them back without having to touch the access window.

**Return values**

FSP_SUCCESS	Start-up area successfully toggled.
FSP_ERR_IN_USE	Flash is busy with an on-going operation.
FSP_ERR_ASSERTION	NULL provided for p_ctrl
FSP_ERR_NOT_OPEN	Flash API has not yet been opened.
FSP_ERR_WRITE_FAILED	Status is indicating a Programming error for the requested operation.
FSP_ERR_TIMEOUT	Timed out waiting for the FCU to become ready.
FSP_ERR_UNSUPPORTED	Code Flash Programming is not enabled. Cannot set FLASH_STARTUP_AREA_BTFLG when the temporary flag is false.

◆ **R\_FLASH\_LP\_CallbackSet()**

```
fsp_err_t R_FLASH_LP_CallbackSet ( flash_ctrl_t *const p_api_ctrl, void (*)(flash_callback_args_t *)
p_callback, void const *const p_context, flash_callback_args_t *const p_callback_memory )
```

Stub function Implements `flash_api_t::callbackSet`.

**Return values**

FSP_ERR_UNSUPPORTED	Function has not been implemented.
---------------------	------------------------------------

◆ **R\_FLASH\_LP\_UpdateFlashClockFreq()**

```
fsp_err_t R_FLASH_LP_UpdateFlashClockFreq ( flash_ctrl_t *const p_api_ctrl)
```

Indicate to the already open Flash API that the FCLK has changed. Implements `flash_api_t::updateFlashClockFreq`.

This could be the case if the application has changed the system clock, and therefore the FCLK. Failure to call this function subsequent to changing the FCLK could result in damage to the flash macro.

**Return values**

FSP_SUCCESS	Start-up area successfully toggled.
FSP_ERR_IN_USE	Flash is busy with an on-going operation.
FSP_ERR_FCLK	Invalid flash clock source frequency.
FSP_ERR_ASSERTION	NULL provided for p_ctrl
FSP_ERR_NOT_OPEN	Flash API has not yet been opened.
FSP_ERR_TIMEOUT	Timed out waiting for the FCU to become ready.

◆ **R\_FLASH\_LP\_VersionGet()**

```
fsp_err_t R_FLASH_LP_VersionGet ( fsp_version_t *const p_version)
```

Get Flash LP driver version.

**Return values**

FSP_SUCCESS	Operation performed successfully
FSP_ERR_ASSERTION	Null Pointer

◆ **R\_FLASH\_LP\_InfoGet()**

```
fsp_err_t R_FLASH_LP_InfoGet ( flash_ctrl_t *const p_api_ctrl, flash_info_t *const p_info )
```

Returns the information about the flash regions. Implements `flash_api_t::infoGet`.

**Return values**

FSP_SUCCESS	Successful retrieved the request information.
FSP_ERR_ASSERTION	NULL provided for p_ctrl or p_info.
FSP_ERR_NOT_OPEN	The flash is not open.

**4.2.22 Graphics LCD Controller (r\_glcddc)**

## Modules

**Functions**

```
fsp_err_t R_GLCDC_Open (display_ctrl_t *const p_api_ctrl, display_cfg_t const *const p_cfg)
```

```
fsp_err_t R_GLCDC_Close (display_ctrl_t *const p_api_ctrl)
```

```
fsp_err_t R_GLCDC_Start (display_ctrl_t *const p_api_ctrl)
```

```
fsp_err_t R_GLCDC_Stop (display_ctrl_t *const p_api_ctrl)
```

```
fsp_err_t R_GLCDC_LayerChange (display_ctrl_t const *const p_api_ctrl, display_runtime_cfg_t const *const p_cfg, display_frame_layer_t layer)
```

```
fsp_err_t R_GLCDC_BufferChange (display_ctrl_t const *const p_api_ctrl, uint8_t *const framebuffer, display_frame_layer_t layer)
```

```
fsp_err_t R_GLCDC_ColorCorrection (display_ctrl_t const *const p_api_ctrl, display_correction_t const *const p_correction)
```

```
fsp_err_t R_GLCDC_ClutUpdate (display_ctrl_t const *const p_api_ctrl, display_clut_cfg_t const *const p_clut_cfg, display_frame_layer_t layer)
```

```
fsp_err_t R_GLCDC_ClutEdit (display_ctrl_t const *const p_api_ctrl, display_frame_layer_t layer, uint8_t index, uint32_t color)
```

```
fsp_err_t R_GLCDC_StatusGet (display_ctrl_t const *const p_api_ctrl, display_status_t *const status)
```

```
fsp_err_t R_GLCDC_VersionGet (fsp_version_t *p_version)
```

## Detailed Description

Driver for the GLCDC peripheral on RA MCUs. This module implements the [Display Interface](#).

## Overview

The GLCDC is a multi-stage graphics output peripheral designed to automatically generate timing and data signals for LCD panels. As part of its internal pipeline the two internal graphics layers can be repositioned, alpha blended, color corrected, dithered and converted to and from a wide variety of pixel formats.

## Features

The following features are available:

Feature	Options
Input color formats	ARGB8888, ARGB4444, ARGB1555, RGB888 (32-bit), RGB565, CLUT 8bpp, CLUT 4bpp, CLUT 1bpp
Output color formats	RGB888, RGB666, RGB565, Serial RGB888 (8-bit parallel)
Correction processes	Alpha blending, positioning, brightness and contrast, gamma correction, dithering
Timing signals	Dot clock, Vsync, Hsync, Vertical and horizontal data enable (DE)
Maximum resolution	Up to 1020 x 1008 pixels (dependent on sync signal width)
Maximum dot clock	60MHz for serial RGB mode, 54MHz otherwise
Internal clock divisors	1-9, 12, 16, 24, 32
Interrupts	Vsync (line detect), Layer 1 underflow, Layer 2 underflow
Other functions	Byte-order and endianness control, line repeat function

## Configuration

### Build Time Configurations for r\_glcdc

The following build time configurations are defined in fsp\_cfg/r\_glcdc\_cfg.h:

Configuration	Options	Default	Description
---------------	---------	---------	-------------

Parameter Checking	<ul style="list-style-type: none"> <li>• Default (BSP)</li> <li>• Enabled</li> <li>• Disabled</li> </ul>	Default (BSP)	If selected, code for parameter checking is included in the build.
Color Correction	<ul style="list-style-type: none"> <li>• On</li> <li>• Off</li> </ul>	Off	If selected, code to adjust brightness, contrast and gamma settings is included in the build. When disabled all color correction configuration options are ignored.

### Configurations for Driver > Graphics > Display Driver on r\_glcdc

This module can be added to the Stacks tab via New Stack > Driver > Graphics > Display Driver on r\_glcdc.

Configuration	Options	Default	Description
General > Name	Name must be a valid C symbol	g_display0	Module name.
Interrupts > Callback Function	Name must be a valid C symbol	NULL	A user callback function can be defined here.
Interrupts > Line Detect Interrupt Priority	MCU Specific Options		Select the line detect (Vsync) interrupt priority.
Interrupts > Underflow 1 Interrupt Priority	MCU Specific Options		Select the underflow interrupt priority for layer 1.
Interrupts > Underflow 2 Interrupt Priority	MCU Specific Options		Select the underflow interrupt priority for layer 2.
Input > Graphics Layer 1 > General > Enabled	<ul style="list-style-type: none"> <li>• Yes</li> <li>• No</li> </ul>	Yes	Specify Used if the graphics layer 1 is used. If so a framebuffer will be automatically generated based on the specified height and horizontal stride.
Input > Graphics Layer 1 > General > Horizontal size	Value must be between 16 and 1016	480	Specify the number of horizontal pixels.
Input > Graphics Layer 1 > General > Vertical size	Value must be between 16 and 1020	272	Specify the number of vertical pixels.
Input > Graphics Layer	Must be a valid non-	0	Specify the horizontal

1 > General > Horizontal position	negative integer with a maximum configurable value of 4091		offset in pixels of the graphics layer from the background layer.
Input > Graphics Layer 1 > General > Vertical position	Must be a valid non-negative integer with a maximum configurable value of 4094	0	Specify the vertical offset in pixels of the graphics layer from the background layer.
Input > Graphics Layer 1 > General > Color format	<ul style="list-style-type: none"> <li>• ARGB8888 (32-bit)</li> <li>• RGB888 (32-bit)</li> <li>• RGB565 (16-bit)</li> <li>• ARGB1555 (16-bit)</li> <li>• ARGB4444 (16-bit)</li> <li>• CLUT8 (8-bit)</li> <li>• CLUT4 (4-bit)</li> <li>• CLUT1 (1-bit)</li> </ul>	RGB565 (16-bit)	Specify the graphics layer Input format. If selecting CLUT formats, you must write the CLUT table data before starting output.
Input > Graphics Layer 1 > General > Line descending mode	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Disabled	Select Used if the framebuffer starts from the bottom of the line.
Input > Graphics Layer 1 > Background Color > Alpha	Value must be between 0 and 255	255	Based on the alpha value, either the graphics Layer 2 (foreground graphics layer) is blended into the graphics Layer 1 (background graphics layer) or the graphics Layer 1 is blended into the monochrome background layer.
Input > Graphics Layer 1 > Background Color > Red	Value must be between 0 and 255	255	Red component of the background color for layer 1.
Input > Graphics Layer 1 > Background Color > Green	Value must be between 0 and 255	255	Green component of the background color for layer 1.
Input > Graphics Layer 1 > Background Color > Blue	Value must be between 0 and 255	255	Blue component of the background color for layer 1.
Input > Graphics Layer 1 > Framebuffer > Framebuffer name	This property must be a valid C symbol	fb_background	Specify the name for the framebuffer for Layer 1.
Input > Graphics Layer 1 > Framebuffer > Number of framebuffers	Must be a valid non-negative integer with a maximum configurable value of 65535	2	Number of framebuffers allocated for Graphics Layer 1.
Input > Graphics Layer	Manual Entry	.bss	Specify the section in

## 1 > Framebuffer > Section for framebuffer allocation

which to allocate the framebuffer. When Arm Compiler 6 is used to place this memory in on-chip SRAM, the section name must be .bss or start with .bss. to avoid consuming unnecessary ROM space.

Input > Graphics Layer 1 > Line Repeat > Enable	<ul style="list-style-type: none"> <li>• On</li> <li>• Off</li> </ul>	Off	Select On if the display will be repeated from a smaller section of the framebuffer.
Input > Graphics Layer 1 > Line Repeat > Repeat count	Must be a valid non-negative integer with a maximum configurable value of 65535 i.e (vertical size) x (lines repeat times) must be equal to the panel vertical size	0	Specify the number of times the image is repeated.
Input > Graphics Layer 1 > Fading > Mode	<ul style="list-style-type: none"> <li>• None</li> <li>• Fade-in</li> <li>• Fade-out</li> </ul>	None	Select the fade method.
Input > Graphics Layer 1 > Fading > Speed	Value must be between 0 and 255	0	Specify the number of frames for the fading transition to complete.
Input > Graphics Layer 2 > General > Enabled	<ul style="list-style-type: none"> <li>• Yes</li> <li>• No</li> </ul>	No	Specify Used if the graphics layer 2 is used. If so a framebuffer will be automatically generated based on the specified height and horizontal stride.
Input > Graphics Layer 2 > General > Horizontal size	Value must be between 16 and 1016	480	Specify the number of horizontal pixels.
Input > Graphics Layer 2 > General > Vertical size	Value must be between 16 and 1020	272	Specify the number of vertical pixels.
Input > Graphics Layer 2 > General > Horizontal position	Must be a valid non-negative integer with a maximum configurable value of 4091	0	Specify the horizontal offset in pixels of the graphics layer from the background layer.
Input > Graphics Layer 2 > General > Vertical position	Must be a valid non-negative integer with a maximum configurable	0	Specify the vertical offset in pixels of the graphics layer from the

Input > Graphics Layer 2 > General > Color format	value of 4094	<ul style="list-style-type: none"> <li>• ARGB8888 (32-bit)</li> <li>• RGB888 (32-bit)</li> <li>• RGB565 (16-bit)</li> <li>• ARGB1555 (16-bit)</li> <li>• ARGB4444 (16-bit)</li> <li>• CLUT8 (8-bit)</li> <li>• CLUT4 (4-bit)</li> <li>• CLUT1 (1-bit)</li> </ul>	RGB565 (16-bit)	background layer. Specify the graphics layer Input format. If selecting CLUT formats, you must write the CLUT table data before starting output.
Input > Graphics Layer 2 > General > Line descending mode		<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Disabled	Select Used if the framebuffer starts from the bottom of the line.
Input > Graphics Layer 2 > Background Color > Alpha	Value must be between 0 and 255		255	Based on the alpha value, either the graphics Layer 2 (foreground graphics layer) is blended into the graphics Layer 1 (background graphics layer) or the graphics Layer 1 is blended into the monochrome background layer.
Input > Graphics Layer 2 > Background Color > Red	Value must be between 0 and 255		255	Red component of the background color for layer 2.
Input > Graphics Layer 2 > Background Color > Green	Value must be between 0 and 255		255	Green component of the background color for layer 2.
Input > Graphics Layer 2 > Background Color > Blue	Value must be between 0 and 255		255	Blue component of the background color for layer 2.
Input > Graphics Layer 2 > Framebuffer > Framebuffer name	This property must be a valid C symbol		fb_foreground	Specify the name for the framebuffer for Layer 2.
Input > Graphics Layer 2 > Framebuffer > Number of framebuffers	Must be a valid non-negative integer with a maximum configurable value of 65535		2	Number of framebuffers allocated for Graphics Layer 2.
Input > Graphics Layer 2 > Framebuffer > Section for framebuffer allocation	Manual Entry		.bss	Specify the section in which to allocate the framebuffer. When Arm Compiler 6 is used to place this memory in on-chip SRAM, the section name must be



Input > Graphics Layer 2 > Line Repeat > Enable	<ul style="list-style-type: none"> <li>• On</li> <li>• Off</li> </ul>	Off	.bss or start with .bss. to avoid consuming unnecessary ROM space.
Input > Graphics Layer 2 > Line Repeat > Repeat count	Must be a valid non-negative integer with a maximum configurable value of 65535 i.e (vertical size) x (lines repeat times) must be equal to the panel vertical size	0	Specify the number of times the image is repeated.
Input > Graphics Layer 2 > Fading > Mode	<ul style="list-style-type: none"> <li>• None</li> <li>• Fade-in</li> <li>• Fade-out</li> </ul>	None	Select the fade method.
Input > Graphics Layer 2 > Fading > Speed	Value must be between 0 and 255	0	Specify the number of frames for the fading transition to complete.
Output > Timing > Horizontal total cycles	Value must be between 24 and 1024	525	Specify the total cycles in a horizontal line. Set to the number of cycles defined in the data sheet of LCD panel sheet in your system
Output > Timing > Horizontal active video cycles	Value must be between 16 and 1016	480	Specify the number of active video cycles in a horizontal line (including front and back porch). Set to the number of cycles defined in the data sheet of LCD panel sheet in your system.
Output > Timing > Horizontal back porch cycles	Value must be between 6 and 1006	40	Specify the number of back porch cycles in a horizontal line. Back porch starts from the beginning of Hsync cycles, which means back porch cycles contain Hsync cycles. Set to the number of cycles defined in the data sheet of LCD panel sheet in your system.

Output > Timing > Horizontal sync signal cycles	Value must be between 0 and 1023	1	Specify the number of Hsync signal assertion cycles. Set to the number of cycles defined in the data sheet of LCD panel sheet in your system.
Output > Timing > Horizontal sync signal polarity	<ul style="list-style-type: none"> <li>• Low active</li> <li>• High active</li> </ul>	Low active	Select the polarity of Hsync signal to match your system.
Output > Timing > Vertical total lines	Value must be between 20 and 1024	316	Specify number of total lines in a frame (including front and back porch).
Output > Timing > Vertical active video lines	Value must be between 16 and 1020	272	Specify the number of active video lines in a frame.
Output > Timing > Vertical back porch lines	Value must be between 3 and 1007	8	Specify the number of back porch lines in a frame. Back porch starts from the beginning of Vsync lines, which means back porch lines contain Vsync lines.
Output > Timing > Vertical sync signal lines	Value must be between 0 and 1023	1	Specify the Vsync signal assertion lines in a frame.
Output > Timing > Vertical sync signal polarity	<ul style="list-style-type: none"> <li>• Low active</li> <li>• High active</li> </ul>	Low active	Select the polarity of Vsync signal to match to your system.
Output > Timing > Data Enable Signal Polarity	<ul style="list-style-type: none"> <li>• Low active</li> <li>• High active</li> </ul>	High active	Select the polarity of Data Enable signal to match to your system.
Output > Timing > Sync edge	<ul style="list-style-type: none"> <li>• Rising edge</li> <li>• Falling edge</li> </ul>	Rising edge	Select the polarity of Sync signals to match to your system.
Output > Format > Color format	<ul style="list-style-type: none"> <li>• 24bits RGB888</li> <li>• 18bits RGB666</li> <li>• 16bits RGB565</li> <li>• 8bits serial</li> </ul>	16bits RGB565	Specify the graphics layer output format to match to your LCD panel.
Output > Format > Color order	<ul style="list-style-type: none"> <li>• RGB</li> <li>• BGR</li> </ul>	RGB	Select data order for output signal to LCD panel.
Output > Format > Endian	<ul style="list-style-type: none"> <li>• Little endian</li> <li>• Big endian</li> </ul>	Little endian	Select data endianness for output signal to LCD panel.

Output > Background > Alpha	Value must be between 0 and 255	255	Alpha component of the background color.
Output > Background > Red	Value must be between 0 and 255	0	Red component of the background color.
Output > Background > Green	Value must be between 0 and 255	0	Green component of the background color.
Output > Background > Blue	Value must be between 0 and 255	0	Blue component of the background color.
CLUT > Enabled	<ul style="list-style-type: none"> <li>• Yes</li> <li>• No</li> </ul>	No	Specify Used if selecting CLUT formats for a graphics layer input format. If used, a buffer (CLUT_buffer) will be automatically generated based on the selected pixel width.
CLUT > Size	Must be a valid non-negative integer with a maximum configurable value of 256	256	Specify the number of entries for the CLUT source data buffer. Each entry consumes 4 bytes (1 word).
TCON > Hsync pin select	<ul style="list-style-type: none"> <li>• Not used</li> <li>• LCD_TCON0</li> <li>• LCD_TCON1</li> <li>• LCD_TCON2</li> <li>• LCD_TCON3</li> </ul>	LCD_TCON0	Select the TCON pin used for the Hsync signal to match to your system.
TCON > Vsync pin select	<ul style="list-style-type: none"> <li>• Not used</li> <li>• LCD_TCON0</li> <li>• LCD_TCON1</li> <li>• LCD_TCON2</li> <li>• LCD_TCON3</li> </ul>	LCD_TCON1	Select TCON pin used for Vsync signal to match to your system.
TCON > Data enable (DE) pin select	<ul style="list-style-type: none"> <li>• Not used</li> <li>• LCD_TCON0</li> <li>• LCD_TCON1</li> <li>• LCD_TCON2</li> <li>• LCD_TCON3</li> </ul>	LCD_TCON2	Select TCON pin used for DataEnable signal to match to your system.
TCON > Panel clock source	<ul style="list-style-type: none"> <li>• Internal clock (GLCDCLK)</li> <li>• External clock (LCD_EXTCLK)</li> </ul>	Internal clock (GLCDCLK)	Choose between an internal GLCDCLK generated from PCLKA or an external clock provided to the LCD_EXTCLK pin.
TCON > Panel clock division ratio	Refer to the RA Configuration tool for available options.	1/24	Select the clock source divider value.
Color Correction > Brightness > Enabled	<ul style="list-style-type: none"> <li>• Yes</li> <li>• No</li> </ul>	No	Enable brightness color correction.

Color Correction > Brightness > Red channel	Value must be between 0 and 1023	512	Red component of the brightness calibration. This value is divided by 512 to determine gain.
Color Correction > Brightness > Green channel	Value must be between 0 and 1023	512	Green component of the brightness calibration. This value is divided by 512 to determine gain.
Color Correction > Brightness > Blue channel	Value must be between 0 and 1023	512	Blue component of the brightness calibration. This value is divided by 512 to determine gain.
Color Correction > Contrast > Enabled	<ul style="list-style-type: none"> <li>• Yes</li> <li>• No</li> </ul>	No	Enable contrast color correction.
Color Correction > Contrast > Red channel gain	Value must be between 0 and 255	128	Red component of the contrast calibration. This value is divided by 128 to determine gain.
Color Correction > Contrast > Green channel gain	Value must be between 0 and 255	128	Green component of the contrast calibration. This value is divided by 128 to determine gain.
Color Correction > Contrast > Blue channel gain	Value must be between 0 and 255	128	Blue component of the contrast calibration. This value is divided by 128 to determine gain.
Color Correction > Gamma > Red	<ul style="list-style-type: none"> <li>• On</li> <li>• Off</li> </ul>	Off	Enable gamma color correction for the red channel.
Color Correction > Gamma > Green	<ul style="list-style-type: none"> <li>• On</li> <li>• Off</li> </ul>	Off	Enable gamma color correction for the green channel.
Color Correction > Gamma > Blue	<ul style="list-style-type: none"> <li>• On</li> <li>• Off</li> </ul>	Off	Enable gamma color correction for the blue channel.
Color Correction > Process order	<ul style="list-style-type: none"> <li>• Brightness/contrast first</li> <li>• Gamma first</li> </ul>	Brightness/contrast first	Select the color correction processing order.
Dithering > Enabled	<ul style="list-style-type: none"> <li>• Yes</li> <li>• No</li> </ul>	No	Enable dithering to reduce the effect of color banding.
Dithering > Mode	<ul style="list-style-type: none"> <li>• Truncate</li> <li>• Round off</li> <li>• 2x2 Pattern</li> </ul>	Truncate	Select the dithering mode.
Dithering > Pattern A	<ul style="list-style-type: none"> <li>• Pattern 00</li> </ul>	Pattern 11	Select the dithering

	<ul style="list-style-type: none"> <li>• Pattern 01</li> <li>• Pattern 10</li> <li>• Pattern 11</li> </ul>		pattern.
Dithering > Pattern B	<ul style="list-style-type: none"> <li>• Pattern 00</li> <li>• Pattern 01</li> <li>• Pattern 10</li> <li>• Pattern 11</li> </ul>	Pattern 11	Select the dithering pattern.
Dithering > Pattern C	<ul style="list-style-type: none"> <li>• Pattern 00</li> <li>• Pattern 01</li> <li>• Pattern 10</li> <li>• Pattern 11</li> </ul>	Pattern 11	Select the dithering pattern.
Dithering > Pattern D	<ul style="list-style-type: none"> <li>• Pattern 00</li> <li>• Pattern 01</li> <li>• Pattern 10</li> <li>• Pattern 11</li> </ul>	Pattern 11	Select the dithering pattern.

## Clock Configuration

The peripheral clock for this module is PCLKA.

The dot clock is typically generated from the PLL with a maximum output frequency of 54 MHz in most pixel formats (60 MHz for serial RGB). Optionally, a clock signal can be provided to the LCD\_EXTCLK pin for finer framerate control (60 MHz maximum input). With either clock source dividers of 1-9, 12, 16, 24 and 32 may be used. Clocks must be initialized and settled prior to starting this module.

## Pin Configuration

This module controls a variety of pins necessary for LCD data and timing signal output:

Pin Name	Function	Notes
LCD_EXTCLK	External clock signal input	The maximum input clock frequency is 60MHz.
LCD_CLK	Dot clock output	The maximum output frequency is 54MHz (60MHz in serial RGB mode).
LCD_DATAn	Pixel data output lines	Pin assignment and color order is based on the output block configuration. See the RA6M3 User's Manual (R01UH0886EJ0100) section 58.1.4 "Output Control for Data Format" for details.
LCD_TCONn	Panel timing signal output	These pins can be configured to output vertical and horizontal synchronization and data valid signals.

### Note

*There are two banks of pins listed for the GLCDC in the RA6M3 User's Manual (\_A and \_B). In most cases the \_B*

*bank will be used as `_A` conflicts with SDRAM pins. In either case, it is generally recommended to only use pins from only one bank at a time as this allows for superior signal routing both inside and outside the package. If `_A` and `_B` pins must be mixed be sure to note the timing precision penalty detailed in Table 60.33 in in the RA6M3 User's Manual.*

## Usage Notes

### Overview

The GLCDC peripheral is a combination of several sub-peripherals that form a pixel data processing pipeline. Each block passes pixel data to the next but otherwise they are disconnected from one another - in other words, changing timing block parameters does not affect the output generation block configuration and vice versa.

### Initial Configuration

During `R_GLCDC_Open` all configured parameters are set in the GLCDC peripheral fully preparing it for operation. Once opened, calling `R_GLCDC_Start` is typically all that is needed for basic operation. Background generation, timing and output parameters are not configurable at runtime, though layer control and color correction options can be altered.

### Framebuffer Allocation

The framebuffer should be allocated in the highest-speed region available (excluding SRAMHS) without displacing the stack, heap and other program-critical structures. While the RA6M3 does contain a relatively large 640K of on-chip SRAM, for many screen sizes and color depths SDRAM will be required. Regardless of the placement two rules must be followed to ensure correct operation of the GLCDC:

- The framebuffer must be aligned on a 64-byte boundary
- The horizontal stride of the buffer must be a multiple of 64 bytes

#### Note

*Framebuffers allocated through the RA Configuraton tool automatically follow the alignment and size requirements.*

If your framebuffer will be placed into internal SRAM please note the following best practices:

- The framebuffer should ideally not be placed in the SRAMHS block of SRAM as there is no speed advantage for doing so. In particular, it is important to ensure the framebuffer does not push the stack or any heaps outside of SRAMHS to preserve CPU performance.
- It is recommended to not cross the boundary between SRAM0 and SRAM1 with a single framebuffer for performance reasons.
- If double-buffering is desired (and possible within SRAM), place one framebuffer in SRAM0 and the other in SRAM1.

If you are using SRAM for the framebuffer, to ensure correct placement you will need to edit the linker script to add new sections. Below is an example of the required edits in the GCC and IAR formats:

### GCC Linker

```
/*  
Linker File for RA6M3 MCU
```

```
*/
/* Linker script to configure memory regions. */
MEMORY
{
    FLASH (rx)      : ORIGIN = 0x00000000, LENGTH = 0x0200000 /* 2M */
    RAM (rwx)       : ORIGIN = 0x1FFE0000, LENGTH = 0x00A0000 /* 640K */
    FB0 (rwx)       : ORIGIN = 0x20000000, LENGTH = 0x0080000 /* 512K */ // Section
for framebuffer 0 (or only framebuffer)
    FB1 (rwx)       : ORIGIN = 0x20040000, LENGTH = 0x0040000 /* 256K */ // Section
for framebuffer 1
    DATA_FLASH (rx) : ORIGIN = 0x40100000, LENGTH = 0x0010000 /* 64K */
    QSPI_FLASH (rx)  : ORIGIN = 0x60000000, LENGTH = 0x4000000 /* 64M */
    SDRAM (rwx)      : ORIGIN = 0x90000000, LENGTH = 0x2000000 /* 32M */
    ID_CODE (rx)     : ORIGIN = 0x0100A150, LENGTH = 0x10 /* 16 bytes */
}
// ...
.noinit (NOLOAD):
{
    . = ALIGN(4);
    __noinit_start = .;
    KEEP(*(.noinit*))
    __noinit_end = .;
} > RAM
/* Place framebuffer sections first, then the rest of RAM */
.fb0 :
{
    . = ALIGN(64);
    __fb0_start = .;
    *(.fb0*);
    __fb0_end = .;
} > FB0
.fb1 :
{
    . = ALIGN(64);
```

```

    __fb1_start = .;
    *(.fb1*);
    __fb1_end = .;
} > FB1
.bss :
{
    . = ALIGN(4);
    __bss_start__ = .;
    *(.bss*)
    *(COMMON)
    . = ALIGN(4);
    __bss_end__ = .;
} > RAM
// ...

```

## IAR Linker

### Note

*The IAR linker does not place items correctly when sections overlap. As a result, it is advised to place your framebuffer(s) as high as possible in the SRAM region in the linker script to maximize the RAM available for everything else. The below is a general case that should be used unedited only if RAM usage (excluding framebuffers) is less than 128K.*

```

/* ... */
/*-Memory Regions-*/
define symbol region_VECT_start      = 0x00000000;
define symbol region_VECT_end        = 0x000003FF;
define symbol region_ROMREG_start    = 0x00000400;
define symbol region_ROMREG_end      = 0x000004FF;
define symbol region_FLASH_start     = 0x00000500;
define symbol region_FLASH_end       = 0x001FFFFFFF;
define symbol region_RAM_start       = 0x1FFE0000;
define symbol region_RAM_end         = 0x1FFFFFFF; /* RAM limited to SRAMHS */
define symbol region_FB0_start       = 0x20000000;
define symbol region_FB0_end         = 0x2003FFFF; /* SRAM0 dedicated to framebuffer 0
*/
define symbol region_FB1_start       = 0x20040000;

```



```

define symbol region_FB1_end      = 0x2007FFFF; /* SRAM1 dedicated to framebuffer 1
*/
define symbol region_DF_start     = 0x40100000;
define symbol region_DF_end      = 0x4010FFFF;
define symbol region_SDRAM_start  = 0x90000000;
define symbol region_SDRAM_end   = 0x91FFFFFF;
define symbol region_QSPI_start   = 0x60000000;
define symbol region_QSPI_end    = 0x63FFFFFF;
/* ... */

define memory mem with size      = 4G;
define region VECT_region        = mem:[from region_VECT_start   to region_VECT_end];
define region ROMREG_region      = mem:[from region_ROMREG_start to region_ROMREG_end];
define region FLASH_region       = mem:[from region_FLASH_start  to
region_FLASH_end];
define region RAM_region         = mem:[from region_RAM_start     to region_RAM_end];
define region FB0_region         = mem:[from region_FB0_start     to region_FB0_end]; /*
Define framebuffer 0 region */
define region FB1_region         = mem:[from region_FB1_start     to region_FB1_end]; /*
Define framebuffer 1 region */
define region DF_region          = mem:[from region_DF_start     to region_DF_end];
define region SDRAM_region       = mem:[from region_SDRAM_start  to
region_SDRAM_end];
define region QSPI_region        = mem:[from region_QSPI_start    to region_QSPI_end];
/* ... */

define block START_OF_RAM with fixed order { rw section .fsp_dtc_vector_table,
                                             block RAM_CODE };

place at start of RAM_region { block START_OF_RAM };
/* Place framebuffer sections first, then the rest of RAM */
place in FB0_region { rw section .fb0 };
place in FB1_region { rw section .fb1 };
place in RAM_region   { rw,
                       rw section .noinit,
                       rw section .bss,
                       rw section .data,

```

```
rw section HEAP,
rw section .stack };
```

### Graphics Layers and Timing Parameters

The GLCDC synthesizes graphics data through two configurable graphics layers onto a background layer. The background is used as a solid-color canvas upon which to composite data from the graphics layers. The two graphics layers are blended on top of each other (Layer 2 above Layer 1) and overlaid on the background layer based on their individual configuration. The placement of the layers (as well as LCD timing parameters) are detailed in Figure 1. The colors of the dimensions indicate which element of the `display_cfg_t` struct is being referenced - for example, the width of the background layer would be `[display_cfg].output.htiming.display_cyc` as shown in the figure below.

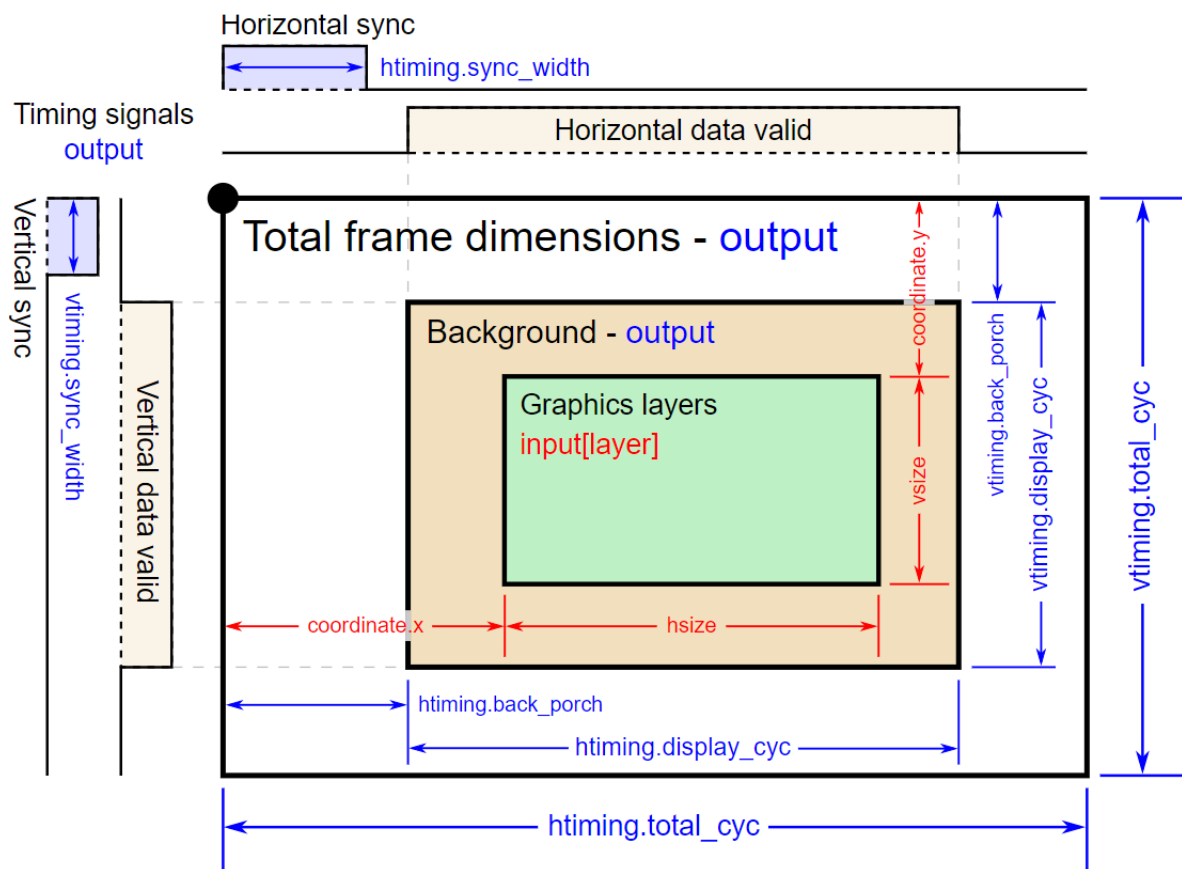


Figure 161: GLCDC layers and timing

*Note*

The data enable signal (if configured) is the logical AND of the horizontal and vertical data valid signals. In the GLCDC layers and timing figure, only one graphics layer is shown for simplicity. Additionally, in most applications the graphics layer(s) will be the same dimensions as the background layer.

### Runtime Configuration Options

*Note*

All runtime configurations detailed below are also automatically configured during *R\_GLCDC\_Open* based on the options selected in the RA Configuration editor.

## Blend processing

Control of layer positioning, alpha blending and fading is possible at runtime via [R\\_GLCDC\\_LayerChange](#). This function takes a [display\\_runtime\\_cfg\\_t](#) parameter which contains the same input and layer elements as the [display\\_cfg\\_t](#) control block. Refer to the documentation for [display\\_runtime\\_cfg\\_t](#) as well as the [Examples](#) below to see what options are configurable.

## Brightness and contrast

Brightness and contrast correction can be controlled through [R\\_GLCDC\\_ColorCorrection](#). The [display\\_correction\\_t](#) parameter is used to control enabling, disabling and gain values for both corrections as shown below:

```
display_correction_t correction;
/* Brightness values are 0-1023 with +512 offset being neutral */
correction.brightness.r = 512;
correction.brightness.g = 512;
correction.brightness.b = 512;
/* Contrast values are 0-255 representing gain of 0-2 (128 is gain of 1) */
correction.contrast.r = 128;
correction.contrast.g = 128;
correction.contrast.b = 128;
/* Brightness and contrast correction can be enabled or disabled independent of one
another */
correction.brightness.enable = true;
correction.contrast.enable = true;
/* Enable correction */
R_GLCDC_ColorCorrection(&g_disp_ctrl, &correction);
```

## Color Look-Up Table (CLUT) Modes

The GLCDC supports 1-, 4- and 8-bit color look-up table (CLUT) formats for input pixel data. By using these modes the framebuffer size in memory can be reduced significantly, allowing even high-resolution displays to be buffered in on-chip SRAM. To enable CLUT modes for a layer the color format must be set to a CLUT mode (either at startup or through [R\\_GLCDC\\_LayerChange](#)) in addition to filling the CLUT as appropriate via [R\\_GLCDC\\_ClutUpdate](#) as shown below:

```
/* Basic 4-bit (16-color) CLUT definition */
uint32_t clut_4[16] =
{
```

```

    0xFF000000,          // Black
    0xFFFFFFFF,        // White
    0xFF0000FF,        // Blue
    0xFF0080FF,        // Turquoise
    0xFF00FFFF,        // Cyan
    0xFF00FF80,        // Mint Green
    0xFF00FF00,        // Green
    0xFF80FF00,        // Lime Green
    0xFFFF0000,        // Yellow
    0xFFFF8000,        // Orange
    0xFFFF0000,        // Red
    0xFFFF0080,        // Pink
    0xFFFF00FF,        // Magenta
    0xFF8000FF,        // Purple
    0xFF808080,        // Gray
    0x00000000         // Transparent
};

/* Define the CLUT configuration */
display_clut_cfg_t clut_cfg =
{
    .start = 0,
    .size  = 16,
    .p_base = clut_4
};

/* Update the CLUT in the GLCDC */
R_GLCDC_ClutUpdate(&g_disp_ctrl, &clut_cfg, DISPLAY_FRAME_LAYER_1);

```

**Note**

*If individual elements of the CLUT must be changed or if elements must be changed one at a time (for instance, when using emWin) it is recommended to use R\_GLCDC\_ClutEdit to avoid repeated memcpy operations.*

**Other Configuration Options****Gamma correction**

Gamma correction is performed based on a gain curved defined in the RA Configuration editor. Each point on the curve is defined by a threshold and a gain value - each gain value represents a multiplier from 0x-2x (set as 0-2047) that sets the Y-value of the slope of the gain curve, while each

threshold interval sets the X-value respectively. For a more detailed explanation refer to the RA6M3 User's Manual (R01UH0886EJ0100) Figure 58.12 "Calculation of gamma correction value" and the related description above it.

When setting threshold values three rules must be followed:

- Each threshold value must be greater than the previous value
- Threshold values must be greater than zero and less than 1024
- Threshold values can equal the previous value only if they are 1023 (maximum)

Note

*Gamma correction can only be applied via [R\\_GLCDC\\_Open](#).*

## Dithering

Dithering is a method of pixel blending that allows for smoother transitions between colors when using a limited palette. A full description of dithering is outside the scope of this document. For more information on the pattern settings and how to configure them refer to the RA6M3 User's Manual (R01UH0886EJ0100) Figure 58.13 "Configuration of dither correction block" and Figure 58.14 "Addition value selection method for 2x2 pattern dither".

## Bus Utilization

Note

*The data provided in this section consists of estimates only. Experimentation is necessary to obtain real-world performance data on any platform.*

While the GLCDC is very flexible in size and color depth of displays there are considerations to be made in the tradeoff between color depth, framerate and bus utilization. Below is a table showing estimates of the load at various resolutions, framerates and color depths based on a PLL frequency of 120MHz (default) and an effective SDRAM throughput of 60 MB/sec. Bus utilization percentages are provided for the following use cases:

- Static image display (**GLCDC only**): One read
- Redrawing one framebuffer every display frame (**minimal redraw**): One write, one read
- Blitting one buffer to another then redrawing the entire buffer every display frame (**worst case**): Two writes, three reads

Name	Width	Height	Input color depth (bits)	Framerate (FPS)	Buffer size (bytes)	SRAM use	SRAM bus (GLCDC only)	SDRAM bus (GLCDC only)	SRAM bus (minimal redraw)	SDRAM bus (minimal redraw)	SRAM bus (worst case)	SDRAM bus (worst case)
HQVGA	240	160	8	60	38400	6%	1%	4%	2%	8%	5%	19%
HQVGA	240	160	16	60	76800	12%	2%	8%	4%	15%	10%	38%
QVGA	320	240	16	60	153600	23%	4%	15%	8%	31%	19%	77%
WQVGA	400	240	8	60	96000	15%	2%	10%	5%	19%	12%	48%

WQV GA	400	240	16	60	1920 00	29%	5%	19%	10%	38%	24%	96%
HVGA	480	320	16	60	3072 00	47%	8%	31%	15%	61%	38%	154%
VGA	640	480	16	30	6144 00	—	—	31%	—	61%	—	154%
WVG A	800	480	8	60	3840 00	59%	10%	38%	19%	77%	48%	192%
WVG A	800	480	16	30	7680 00	—	—	38%	—	77%	—	192%
WVG A	800	480	32	15	1536 000	—	—	38%	—	77%	—	192%
FWVG A	960	480	8	30	4608 00	70%	6%	23%	12%	46%	29%	115%
FWVG A	960	480	16	30	9216 00	—	—	46%	—	92%	—	230%
qHD	960	540	8	30	5184 00	79%	6%	26%	13%	52%	32%	130%

**Note**

Bus utilization values over 100% indicate that the bandwidth for that bus is exceeded in that scenario and GLCDC underflow and/or dropped frames may result depending on the bus priority setting. **It is recommended to avoid these scenarios if at all possible by reducing the buffer drawing rate, number of draw/copy operations or the input color depth.** Relaxing vertical timing (increasing total line count) or increasing the clock divider are the easiest ways to increase the time per frame.

**Limitations**

Developers should be aware of the following limitations when using the GLCDC API:

- Due to a limitation of the GLCDC hardware, if the horizontal back porch is less than the number of pixels in a graphics burst read (64 bytes) for a layer and the layer is positioned at a negative X-value then the layer X-position will be locked to the nearest 64-byte boundary, rounded toward zero.
- The GLCDC peripheral offers a chroma-key function that can be used to perform a green-screen-like color replacement. This functionality is not exposed through the GLCDC API. See the descriptions for GRn.AB7 through .AB9 in the RA6M3 User's Manual for further details.
- Use of R\_GLCDC\_ClutUpdate and R\_GLCDC\_ClutEdit may not be mixed on the same frame.

**Examples****Basic Example**

This is a basic example showing the minimum code required to initialize and start the GLCDC module. If the entire display can be drawn within the vertical blanking period no further code may be necessary.

```
void glcdc_init (void)
```

```
{
    fsp_err_t err;
    // Open the GLCDC driver
    err = R_GLCDC_Open(&g_disp_ctrl, &g_disp_cfg);
    /* Handle any errors. This function should be defined by the user. */
    handle_error(err);
    // Start display output
    err = R_GLCDC_Start(&g_disp_ctrl);
    handle_error(err);
}
```

## Layer Transitions

This example demonstrates how to set up and execute both a sliding and fading layer transition. This is most useful in static image transition scenarios as switching between two actively-drawing graphics layers may require up to four framebuffers to eliminate tearing.

```
volatile uint32_t g_vsync_count = 0;
/* Callback function for GLCDC interrupts */
static void glcdc_callback (display_callback_args_t * p_args)
{
    if (p_args->event == DISPLAY_EVENT_LINE_DETECTION)
    {
        g_vsync_count++;
    }
}
/* Simple wait that returns 1 if no Vsync happened within the timeout period */
uint8_t vsync_wait (void)
{
    uint32_t timeout_timer = GLCDC_VSYNC_TIMEOUT;
    g_vsync_count = 0;
    while (!g_vsync_count && --timeout_timer)
    {
        /* Spin here until DISPLAY_EVENT_LINE_DETECTION callback or timeout */
    }
    return timeout_timer ? 0 : 1;
}
```

```
}
/* Initiate a fade on Layer 2
 *
 * Parameters:
 * direction True for fade in, false for fade out
 * speed number of frames over which to fade
 */
void glcdc_layer_transition_fade (display_runtime_cfg_t * disp_rt_cfg, bool
direction, uint16_t speed)
{
    fsp_err_t err;
    if (direction)
    {
        /* Set the runtime struct to the desired buffer */
        disp_rt_cfg->input.p_base      = (uint32_t *) g_framebuffer_1;
        disp_rt_cfg->layer.fade_control = DISPLAY_FADE_CONTROL_FADEIN;
    }
    else
    {
        disp_rt_cfg->layer.fade_control = DISPLAY_FADE_CONTROL_FADEOUT;
    }
    /* Ensure speed is at least 1 frame */
    if (!speed)
    {
        speed = 1;
    }
    /* Set the fade speed to the desired change in alpha per frame */
    disp_rt_cfg->layer.fade_speed = UINT8_MAX / speed;
    /* Initiate the fade (will start on the next Vsync) */
    err = R_GLCDC_LayerChange(&g_disp_ctrl, disp_rt_cfg, DISPLAY_FRAME_LAYER_2);
    handle_error(err);
}
/* Slide Layer 1 out to the left while sliding Layer 2 in from the right */
void glcdc_layer_transition_sliding (display_runtime_cfg_t * disp_rt_cfg_in,
```



```
display_runtime_cfg_t * disp_rt_cfg_out)
{
    fsp_err_t err;

    /* Set the config for the incoming layer to be just out of bounds on the right side
    */
    disp_rt_cfg_in->input.p_base      = (uint32_t *) g_framebuffer_1;
    disp_rt_cfg_in->layer.coordinate.x = DISPLAY_WIDTH;

    /* Move layer 1 out and layer 2 in at a fixed rate of 4 pixels per frame */
    for (int32_t x = disp_rt_cfg_in->layer.coordinate.x; x >= 0; x -= 4)
    {
        /* Wait for a Vsync before starting */
        vsync_wait();

        /* Set the X-coordinate of both layers then update them */
        disp_rt_cfg_out->layer.coordinate.x = (int16_t) (x - DISPLAY_WIDTH);
        disp_rt_cfg_in->layer.coordinate.x = (int16_t) x;

        err = R_GLCDC_LayerChange(&g_disp_ctrl, disp_rt_cfg_out, DISPLAY_FRAME_LAYER_1
    );

        handle_error(err);

        err = R_GLCDC_LayerChange(&g_disp_ctrl, disp_rt_cfg_in, DISPLAY_FRAME_LAYER_2
    );

        handle_error(err);
    }
}
```

## Double-Buffering

Using a double-buffer allows one to be output to the LCD while the other is being drawn to memory, eliminating tearing and in some cases reducing bus load. The following is a basic example showing integration of the line detect (Vsync) interrupt to set the timing for buffer swapping and drawing.

```
/* User-defined function to draw the current display to a framebuffer */
void display_draw (uint8_t * framebuffer)
{
    FSP_PARAMETER_NOT_USED(framebuffer);

    /* Draw buffer here */
}
```

```
/* This function is an example of a basic double-buffered display thread */
void display_thread (void)
{
    uint8_t * p_framebuffer = NULL;
    fsp_err_t err;
    /* Initialize and start the R_GLCDC module */
    glcdc_init();
    while (1)
    {
        /* Swap the active framebuffer */
        p_framebuffer = (p_framebuffer == g_framebuffer_0) ? g_framebuffer_1 :
g_framebuffer_0;
        /* Draw the new framebuffer now */
        display_draw(p_framebuffer);
        /* Now that the framebuffer is ready, update the GLCDC buffer pointer on the next
Vsync */
        err = R_GLCDC_BufferChange(&g_disp_ctrl, p_framebuffer, DISPLAY_FRAME_LAYER_1
);
        handle_error(err);
        /* Wait for a Vsync event */
        vsync_wait();
    }
}
```

## Data Structures

struct [glcdc\\_instance\\_ctrl\\_t](#)

struct [glcdc\\_extended\\_cfg\\_t](#)

## Enumerations

enum [glcdc\\_clk\\_src\\_t](#)

enum [glcdc\\_panel\\_clk\\_div\\_t](#)

enum [glcdc\\_tcon\\_pin\\_t](#)

enum [glcdc\\_bus\\_arbitration\\_t](#)

enum [glcdc\\_correction\\_proc\\_order\\_t](#)enum [glcdc\\_tcon\\_signal\\_select\\_t](#)enum [glcdc\\_clut\\_plane\\_t](#)enum [glcdc\\_dithering\\_mode\\_t](#)enum [glcdc\\_dithering\\_pattern\\_t](#)enum [glcdc\\_input\\_interface\\_format\\_t](#)enum [glcdc\\_output\\_interface\\_format\\_t](#)enum [glcdc\\_dithering\\_output\\_format\\_t](#)

## Data Structure Documentation

### ◆ [glcdc\\_instance\\_ctrl\\_t](#)

struct [glcdc\\_instance\\_ctrl\\_t](#)

Display control block. DO NOT INITIALIZE.

### ◆ [glcdc\\_extended\\_cfg\\_t](#)

struct [glcdc\\_extended\\_cfg\\_t](#)

GLCDC hardware specific configuration

#### Data Fields

<a href="#">glcdc_tcon_pin_t</a>	tcon_hsync	GLCDC TCON output pin select.
<a href="#">glcdc_tcon_pin_t</a>	tcon_vsync	GLCDC TCON output pin select.
<a href="#">glcdc_tcon_pin_t</a>	tcon_de	GLCDC TCON output pin select.
<a href="#">glcdc_correction_proc_order_t</a>	correction_proc_order	Correction control route select.
<a href="#">glcdc_clk_src_t</a>	clksrc	Clock Source selection.
<a href="#">glcdc_panel_clk_div_t</a>	clock_div_ratio	Clock divide ratio for dot clock.
<a href="#">glcdc_dithering_mode_t</a>	dithering_mode	Dithering mode.
<a href="#">glcdc_dithering_pattern_t</a>	dithering_pattern_A	Dithering pattern A.
<a href="#">glcdc_dithering_pattern_t</a>	dithering_pattern_B	Dithering pattern B.
<a href="#">glcdc_dithering_pattern_t</a>	dithering_pattern_C	Dithering pattern C.
<a href="#">glcdc_dithering_pattern_t</a>	dithering_pattern_D	Dithering pattern D.

## Enumeration Type Documentation

◆ **glcdc\_clk\_src\_t**

enum glcdc_clk_src_t	
Clock source select	
Enumerator	
GLCDC_CLK_SRC_INTERNAL	Internal.
GLCDC_CLK_SRC_EXTERNAL	External.

◆ **glcdc\_panel\_clk\_div\_t**

enum glcdc_panel_clk_div_t	
Clock frequency division ratio	
Enumerator	
GLCDC_PANEL_CLK_DIVISOR_1	Division Ratio 1/1.
GLCDC_PANEL_CLK_DIVISOR_2	Division Ratio 1/2.
GLCDC_PANEL_CLK_DIVISOR_3	Division Ratio 1/3.
GLCDC_PANEL_CLK_DIVISOR_4	Division Ratio 1/4.
GLCDC_PANEL_CLK_DIVISOR_5	Division Ratio 1/5.
GLCDC_PANEL_CLK_DIVISOR_6	Division Ratio 1/6.
GLCDC_PANEL_CLK_DIVISOR_7	Division Ratio 1/7.
GLCDC_PANEL_CLK_DIVISOR_8	Division Ratio 1/8.
GLCDC_PANEL_CLK_DIVISOR_9	Division Ratio 1/9.
GLCDC_PANEL_CLK_DIVISOR_12	Division Ratio 1/12.
GLCDC_PANEL_CLK_DIVISOR_16	Division Ratio 1/16.
GLCDC_PANEL_CLK_DIVISOR_24	Division Ratio 1/24.
GLCDC_PANEL_CLK_DIVISOR_32	Division Ratio 1/32.

◆ **glcdc\_tcon\_pin\_t**

enum <code>glcdc_tcon_pin_t</code>	
LCD TCON output pin select	
Enumerator	
<code>GLCDC_TCON_PIN_NONE</code>	No output.
<code>GLCDC_TCON_PIN_0</code>	<code>LCD_TCON0</code> .
<code>GLCDC_TCON_PIN_1</code>	<code>LCD_TCON1</code> .
<code>GLCDC_TCON_PIN_2</code>	<code>LCD_TCON2</code> .
<code>GLCDC_TCON_PIN_3</code>	<code>LCD_TCON3</code> .

◆ **glcdc\_bus\_arbitration\_t**

enum <code>glcdc_bus_arbitration_t</code>	
Bus Arbitration setting	
Enumerator	
<code>GLCDC_BUS_ARBITRATION_ROUNDROBIN</code>	Round robin.
<code>GLCDC_BUS_ARBITRATION_FIX_PRIORITY</code>	Fixed.

◆ **glcdc\_correction\_proc\_order\_t**

enum <code>glcdc_correction_proc_order_t</code>	
Correction circuit sequence control	
Enumerator	
<code>GLCDC_CORRECTION_PROC_ORDER_BRIGHTNESS_CONTRAST2GAMMA</code>	Brightness -> contrast -> gamma correction.
<code>GLCDC_CORRECTION_PROC_ORDER_GAMMA2BRIGHTNESS_CONTRAST</code>	Gamma correction -> brightness -> contrast.

◆ **glcdc\_tcon\_signal\_select\_t**

enum <a href="#">glcdc_tcon_signal_select_t</a>	
Timing signals for driving the LCD panel	
Enumerator	
GLCDC_TCON_SIGNAL_SELECT_STVA_VS	STVA/VS.
GLCDC_TCON_SIGNAL_SELECT_STVB_VE	STVB/VE.
GLCDC_TCON_SIGNAL_SELECT_STHA_HS	STH/SP/HS.
GLCDC_TCON_SIGNAL_SELECT_STHB_HE	STB/LP/HE.
GLCDC_TCON_SIGNAL_SELECT_DE	DE.

◆ **glcdc\_clut\_plane\_t**

enum <a href="#">glcdc_clut_plane_t</a>	
Clock phase adjustment for serial RGB output	
Enumerator	
GLCDC_CLUT_PLANE_0	GLCDC CLUT plane 0.
GLCDC_CLUT_PLANE_1	GLCDC CLUT plane 1.

◆ **glcdc\_dithering\_mode\_t**

enum <a href="#">glcdc_dithering_mode_t</a>	
Dithering mode	
Enumerator	
GLCDC_DITHERING_MODE_TRUNCATE	No dithering (truncate)
GLCDC_DITHERING_MODE_ROUND_OFF	Dithering with round off.
GLCDC_DITHERING_MODE_2X2PATTERN	Dithering with 2x2 pattern.

◆ **glcdc\_dithering\_pattern\_t**

enum <code>glcdc_dithering_pattern_t</code>	
Dithering mode	
Enumerator	
<code>GLCDC_DITHERING_PATTERN_00</code>	2x2 pattern '00'
<code>GLCDC_DITHERING_PATTERN_01</code>	2x2 pattern '01'
<code>GLCDC_DITHERING_PATTERN_10</code>	2x2 pattern '10'
<code>GLCDC_DITHERING_PATTERN_11</code>	2x2 pattern '11'

◆ **glcdc\_input\_interface\_format\_t**

enum <code>glcdc_input_interface_format_t</code>	
Output interface format	
Enumerator	
<code>GLCDC_INPUT_INTERFACE_FORMAT_RGB565</code>	Input interface format RGB565.
<code>GLCDC_INPUT_INTERFACE_FORMAT_RGB888</code>	Input interface format RGB888.
<code>GLCDC_INPUT_INTERFACE_FORMAT_ARGB1555</code>	Input interface format ARGB1555.
<code>GLCDC_INPUT_INTERFACE_FORMAT_ARGB4444</code>	Input interface format ARGB4444.
<code>GLCDC_INPUT_INTERFACE_FORMAT_ARGB8888</code>	Input interface format ARGB8888.
<code>GLCDC_INPUT_INTERFACE_FORMAT_CLUT8</code>	Input interface format CLUT8.
<code>GLCDC_INPUT_INTERFACE_FORMAT_CLUT4</code>	Input interface format CLUT4.
<code>GLCDC_INPUT_INTERFACE_FORMAT_CLUT1</code>	Input interface format CLUT1.

◆ **glcdc\_output\_interface\_format\_t**

enum <code>glcdc_output_interface_format_t</code>	
Output interface format	
Enumerator	
<code>GLCDC_OUTPUT_INTERFACE_FORMAT_RGB888</code>	Output interface format RGB888.
<code>GLCDC_OUTPUT_INTERFACE_FORMAT_RGB666</code>	Output interface format RGB666.
<code>GLCDC_OUTPUT_INTERFACE_FORMAT_RGB565</code>	Output interface format RGB565.
<code>GLCDC_OUTPUT_INTERFACE_FORMAT_SERIAL_RGB</code>	Output interface format Serial RGB.

◆ **glcdc\_dithering\_output\_format\_t**

enum <code>glcdc_dithering_output_format_t</code>	
Dithering output format	
Enumerator	
<code>GLCDC_DITHERING_OUTPUT_FORMAT_RGB888</code>	Dithering output format RGB888.
<code>GLCDC_DITHERING_OUTPUT_FORMAT_RGB666</code>	Dithering output format RGB666.
<code>GLCDC_DITHERING_OUTPUT_FORMAT_RGB565</code>	Dithering output format RGB565.

**Function Documentation**



◆ **R\_GLCDC\_Open()**

```
fsp_err_t R_GLCDC_Open ( display_ctrl_t *const p_api_ctrl, display_cfg_t const *const p_cfg )
```

Open GLCDC module. Implements `display_api_t::open`.

**Return values**

FSP_SUCCESS	Device was opened successfully.
FSP_ERR_ALREADY_OPEN	Device was already open.
FSP_ERR_ASSERTION	Pointer to the control block or the configuration structure is NULL.
FSP_ERR_CLOCK_GENERATION	Dot clock cannot be generated from clock source.
FSP_ERR_INVALID_TIMING_SETTING	Invalid panel timing parameter.
FSP_ERR_INVALID_LAYER_SETTING	Invalid layer setting found.
FSP_ERR_INVALID_ALIGNMENT	Input buffer alignment invalid.
FSP_ERR_INVALID_GAMMA_SETTING	Invalid gamma correction setting found
FSP_ERR_INVALID_BRIGHTNESS_SETTING	Invalid brightness correction setting found

**Note**

*PCLKA must be supplied to Graphics LCD Controller (GLCDC) and GLCDC pins must be set in IOPORT before calling this API.*

◆ **R\_GLCDC\_Close()**

```
fsp_err_t R_GLCDC_Close ( display_ctrl_t *const p_api_ctrl)
```

Close GLCDC module. Implements `display_api_t::close`.

**Return values**

FSP_SUCCESS	Device was closed successfully.
FSP_ERR_ASSERTION	Pointer to the control block is NULL.
FSP_ERR_NOT_OPEN	The function call is performed when the driver state is not equal to <code>DISPLAY_STATE_CLOSED</code> .
FSP_ERR_INVALID_UPDATE_TIMING	A function call is performed when the GLCDC is updating register values internally.

**Note**

*This API can be called when the driver is not in `DISPLAY_STATE_CLOSED` state. It returns an error if the register update operation for the background screen generation block is being held.*

◆ **R\_GLCDC\_Start()**

```
fsp_err_t R_GLCDC_Start ( display_ctrl_t *const p_api_ctrl)
```

Start GLCDC module. Implements `display_api_t::start`.

**Return values**

FSP_SUCCESS	Device was started successfully.
FSP_ERR_NOT_OPEN	GLCDC module has not been opened.
FSP_ERR_ASSERTION	Pointer to the control block is NULL.

**Note**

*This API can be called when the driver is not in `DISPLAY_STATE_OPENED` status.*

◆ **R\_GLCDC\_Stop()**

```
fsp_err_t R_GLCDC_Stop ( display_ctrl_t *const p_api_ctrl)
```

Stop GLCDC module. Implements `display_api_t::stop`.

**Return values**

FSP_SUCCESS	Device was stopped successfully
FSP_ERR_ASSERTION	Pointer to the control block is NULL
FSP_ERR_INVALID_MODE	Function call is performed when the driver state is not <code>DISPLAY_STATE_DISPLAYING</code> .
FSP_ERR_INVALID_UPDATE_TIMING	The function call is performed while the GLCDC is updating register values internally.

**Note**

*This API can be called when the driver is in the `DISPLAY_STATE_DISPLAYING` state. It returns an error if the register update operation for the background screen generation blocks, the graphics data I/F blocks, or the output control block is being held.*

◆ **R\_GLCDC\_LayerChange()**

```
fsp_err_t R_GLCDC_LayerChange ( display_ctrl_t const *const p_api_ctrl, display_runtime_cfg_t
const *const p_cfg, display_frame_layer_t layer )
```

Change layer parameters of GLCDC module at runtime. Implements `display_api_t::layerChange`.

**Return values**

FSP_SUCCESS	Changed layer parameters of GLCDC module successfully.
FSP_ERR_ASSERTION	Pointer to the control block or the configuration structure is NULL.
FSP_ERR_INVALID_MODE	A function call is performed when the driver state is not DISPLAY_STATE_DISPLAYING.
FSP_ERR_INVALID_UPDATE_TIMING	A function call is performed while the GLCDC is updating register values internally.

**Note**

*This API can be called when the driver is in DISPLAY\_STATE\_DISPLAYING state. It returns an error if the register update operation for the background screen generation blocks or the graphics data I/F block is being held.*

◆ **R\_GLCDC\_BufferChange()**

```
fsp_err_t R_GLCDC_BufferChange ( display_ctrl_t const *const p_api_ctrl, uint8_t *const
framebuffer, display_frame_layer_t layer )
```

Change the framebuffer pointer for a layer. Implements `display_api_t::bufferChange`.

**Return values**

FSP_SUCCESS	Changed layer parameters of GLCDC module successfully.
FSP_ERR_ASSERTION	Pointer to the control block is NULL.
FSP_ERR_INVALID_MODE	A function call is performed when the driver state is not DISPLAY_STATE_DISPLAYING.
FSP_ERR_INVALID_ALIGNMENT	The framebuffer pointer is not 64-byte aligned.
FSP_ERR_INVALID_UPDATE_TIMING	A function call is performed while the GLCDC is updating register values internally.

**Note**

*This API can be called when the driver is in DISPLAY\_STATE\_OPENED state or higher. It returns an error if the register update operation for the background screen generation blocks or the graphics data I/F block is being held.*

◆ **R\_GLCDC\_ColorCorrection()**

```
fsp_err_t R_GLCDC_ColorCorrection ( display_ctrl_t const *const p_api_ctrl, display_correction_t const *const p_correction )
```

Perform color correction through the GLCDC module. Implements `display_api_t::correction`.

**Return values**

FSP_SUCCESS	Color correction by GLCDC module was performed successfully.
FSP_ERR_ASSERTION	Pointer to the control block or the display correction structure is NULL.
FSP_ERR_INVALID_MODE	Function call is performed when the driver state is not DISPLAY_STATE_DISPLAYING.
FSP_ERR_INVALID_UPDATE_TIMING	A function call is performed while the GLCDC is updating registers internally.
FSP_ERR_INVALID_BRIGHTNESS_SETTING	Invalid brightness correction setting found

**Note**

*This API can be called when the driver is in the DISPLAY\_STATE\_DISPLAYING state. It returns an error if the register update operation for the background screen generation blocks or the output control block is being held.*

◆ **R\_GLCDC\_ClutUpdate()**

```
fsp_err_t R_GLCDC_ClutUpdate ( display_ctrl_t const *const p_api_ctrl, display_clut_cfg_t const *const p_clut_cfg, display_frame_layer_t layer )
```

Write an entire color look-up table (CLUT) in the GLCDC module. Implements `display_api_t::clut`.

**Return values**

FSP_SUCCESS	CLUT written successfully.
FSP_ERR_ASSERTION	Pointer to the control block or CLUT source data is NULL.
FSP_ERR_INVALID_UPDATE_TIMING	R_GLCDC_ClutEdit was already used to edit the specified CLUT this frame.
FSP_ERR_INVALID_CLUT_ACCESS	Illegal CLUT entry or size is specified.

**Note**

*This API can be called any time. The written data will be used after the next vertical sync event.*

◆ **R\_GLCDC\_ClutEdit()**

```
fsp_err_t R_GLCDC_ClutEdit ( display_ctrl_t const *const p_api_ctrl, display_frame_layer_t layer,
uint8_t index, uint32_t color )
```

Update an element of a color look-up table (CLUT) in the GLCDC module. Implements `display_api_t::clutEdit`.

**Return values**

FSP_SUCCESS	CLUT element updated successfully.
FSP_ERR_ASSERTION	Pointer to the control block is NULL.

*Note*

*This API can be called any time. The written data will be used after the next vertical sync event.*

◆ **R\_GLCDC\_StatusGet()**

```
fsp_err_t R_GLCDC_StatusGet ( display_ctrl_t const *const p_api_ctrl, display_status_t *const
p_status )
```

Get status of GLCDC module. Implements `display_api_t::statusGet`.

**Return values**

FSP_SUCCESS	Got status successfully.
FSP_ERR_ASSERTION	Pointer to the control block or the status structure is NULL.

*Note*

*The GLCDC hardware starts the fading processing at the first Vsync after the previous LayerChange() call is held. Due to this behavior of the hardware, this API may not return DISPLAY\_FADE\_STATUS\_FADING\_UNDERWAY as the fading status, if it is called before the first Vsync after LayerChange() is called. In this case, the API returns DISPLAY\_FADE\_STATUS\_PENDING, instead of DISPLAY\_FADE\_STATUS\_NOT\_UNDERWAY.*

◆ **R\_GLCDC\_VersionGet()**

```
fsp_err_t R_GLCDC_VersionGet ( fsp_version_t * p_version)
```

Get version of R\_GLCDC module. Implements `display_api_t::versionGet`.

**Return values**

FSP_SUCCESS	Got version information successfully.
-------------	---------------------------------------

*Note*

*This function is re-entrant.*

## 4.2.23 General PWM Timer (r\_gpt)

### Modules

#### Functions

fsp_err_t	R_GPT_Open (timer_ctrl_t *const p_ctrl, timer_cfg_t const *const p_cfg)
fsp_err_t	R_GPT_Stop (timer_ctrl_t *const p_ctrl)
fsp_err_t	R_GPT_Start (timer_ctrl_t *const p_ctrl)
fsp_err_t	R_GPT_Reset (timer_ctrl_t *const p_ctrl)
fsp_err_t	R_GPT_Enable (timer_ctrl_t *const p_ctrl)
fsp_err_t	R_GPT_Disable (timer_ctrl_t *const p_ctrl)
fsp_err_t	R_GPT_PeriodSet (timer_ctrl_t *const p_ctrl, uint32_t const period_counts)
fsp_err_t	R_GPT_DutyCycleSet (timer_ctrl_t *const p_ctrl, uint32_t const duty_cycle_counts, uint32_t const pin)
fsp_err_t	R_GPT_InfoGet (timer_ctrl_t *const p_ctrl, timer_info_t *const p_info)
fsp_err_t	R_GPT_StatusGet (timer_ctrl_t *const p_ctrl, timer_status_t *const p_status)
fsp_err_t	R_GPT_CounterSet (timer_ctrl_t *const p_ctrl, uint32_t counter)
fsp_err_t	R_GPT_OutputEnable (timer_ctrl_t *const p_ctrl, gpt_io_pin_t pin)
fsp_err_t	R_GPT_OutputDisable (timer_ctrl_t *const p_ctrl, gpt_io_pin_t pin)
fsp_err_t	R_GPT_AdcTriggerSet (timer_ctrl_t *const p_ctrl, gpt_adc_compare_match_t which_compare_match, uint32_t compare_match_value)
fsp_err_t	R_GPT_CallbackSet (timer_ctrl_t *const p_api_ctrl, void(*p_callback)(timer_callback_args_t *), void const *const p_context, timer_callback_args_t *const p_callback_memory)
fsp_err_t	R_GPT_Close (timer_ctrl_t *const p_ctrl)
fsp_err_t	R_GPT_VersionGet (fsp_version_t *const p_version)

#### Detailed Description

Driver for the GPT32 and GPT16 peripherals on RA MCUs. This module implements the [Timer Interface](#).

## Overview

The GPT module can be used to count events, measure external input signals, generate a periodic interrupt, or output a periodic or PWM signal to a GTIOC pin.

This module supports the GPT peripherals GPT32EH, GPT32E, GPT32, and GPT16. GPT16 is a 16-bit timer. The other peripherals (GPT32EH, GPT32E, and GPT32) are 32-bit timers. The 32-bit timers are all treated the same in this module from the API perspective.

## Features

The GPT module has the following features:

- Supports periodic mode, one-shot mode, and PWM mode.
- Supports count source of PCLK, GTETRГ pins, GTIOC pins, or ELC events.
- Supports debounce filter on GTIOC pins.
- Signal can be output to a pin.
- Configurable period (counts per timer cycle).
- Configurable duty cycle in PWM mode.
- Supports runtime reconfiguration of period.
- Supports runtime reconfiguration of duty cycle in PWM mode.
- APIs are provided to start, stop, and reset the counter.
- APIs are provided to get the current period, source clock frequency, and count direction.
- APIs are provided to get the current timer status and counter value.
- Supports start, stop, clear, count up, count down, and capture by external sources from GTETRГ pins, GTIOC pins, or ELC events.
- Supports symmetric and asymmetric PWM waveform generation.
- Supports automatic addition of dead time.
- Supports generating ELC events to start an ADC scan at a compare match value (see [Event Link Controller \(r\\_elc\)](#)) and updating the compare match value.
- Supports linking with a POEG channel to automatically disable GPT output when an error condition is detected.
- Supports setting the counter value while the timer is stopped.
- Supports enabling and disabling output pins.
- Supports skipping up to seven overflow/underflow (crest/trough) interrupts at a time

## Selecting a Timer

RA MCUs have two timer peripherals: the General PWM Timer (GPT) and the Asynchronous General Purpose Timer (AGT). When selecting between them, consider these factors:

	GPT	AGT
Low Power Modes	The GPT can operate in sleep mode.	The AGT can operate in all low power modes.
Available Channels	The number of GPT channels is device specific. All currently supported MCUs have at least 7 GPT channels.	All MCUs have 2 AGT channels.
Timer Resolution	All MCUs have at least one	The AGT timers are 16-bit

	32-bit GPT timer.	timers.
Clock Source	The GPT runs off PCLKD with a configurable divider up to 1024. It can also be configured to count ELC events or external pulses.	The AGT runs off PCLKB, LOCO, or subclock.

## Configuration

### Build Time Configurations for r\_gpt

The following build time configurations are defined in fsp\_cfg/r\_gpt\_cfg.h:

Configuration	Options	Default	Description
Parameter Checking	<ul style="list-style-type: none"> <li>Default (BSP)</li> <li>Enabled</li> <li>Disabled</li> </ul>	Default (BSP)	If selected code for parameter checking is included in the build.
Pin Output Support	<ul style="list-style-type: none"> <li>Disabled</li> <li>Enabled</li> <li>Enabled with Extra Features</li> </ul>	Disabled	If selected code for outputting a waveform to a pin is included in the build.
Write Protect Enable	<ul style="list-style-type: none"> <li>Enabled</li> <li>Disabled</li> </ul>	Disabled	If selected write protection is applied to all GPT channels.

### Configurations for Driver > Timers > Timer Driver on r\_gpt

This module can be added to the Stacks tab via New Stack > Driver > Timers > Timer Driver on r\_gpt. Non-secure callable guard functions can be generated for this module by right clicking the module in the RA Configuration tool and checking the "Non-secure Callable" box.

Configuration	Options	Default	Description
General > Name	Name must be a valid C symbol	g_timer0	Module name.
General > Channel	Channel number must exist on this MCU	0	Specify the hardware channel.
General > Mode	<ul style="list-style-type: none"> <li>Periodic</li> <li>One-Shot</li> <li>PWM</li> <li>Triangle-Wave Symmetric PWM</li> <li>Triangle-Wave Asymmetric PWM</li> </ul>	Periodic	Mode selection. Periodic: Generates periodic interrupts or square waves. One-shot: Generate a single interrupt or a pulse wave. Note: One-shot mode is implemented in software. ISRs must be enabled for one-shot even if callback is



unused.  
 PWM: Generates basic PWM waveforms.  
 Triangle-Wave Symmetric PWM: Generates symmetric PWM waveforms with duty cycle determined by compare match set during a crest interrupt and updated at the next trough.  
 Triangle-Wave Asymmetric PWM: Generates asymmetric PWM waveforms with duty cycle determined by compare match set during a crest/trough interrupt and updated at the next trough/crest.

General > Period	Value must be a non-negative integer less than or equal to 0x4000000000	0x100000000	Specify the timer period in units selected below. Setting the period to 0x100000000 raw counts results in the maximum period. Set the period to 0x100000000 raw counts for a free running timer or an input capture configuration. The period can be set up to 0x4000000000, which will use a divider of 1024 with the maximum period.
General > Period Unit	<ul style="list-style-type: none"> <li>• Raw Counts</li> <li>• Nanoseconds</li> <li>• Microseconds</li> <li>• Milliseconds</li> <li>• Seconds</li> <li>• Hertz</li> <li>• Kilohertz</li> </ul>	Raw Counts	Unit of the period specified above
Output > Duty Cycle Percent (only applicable in PWM mode)	Value must be between 0 and 100	50	Specify the timer duty cycle percent. Only used in PWM mode.
Output > GTIOCA Output Enabled	<ul style="list-style-type: none"> <li>• True</li> <li>• False</li> </ul>	False	Enable the output of GTIOCA on a pin.

Output > GTIOCA Stop Level	<ul style="list-style-type: none"> <li>Pin Level Low</li> <li>Pin Level High</li> </ul>	Pin Level Low	Select the behavior of the output pin when the timer is stopped.
Output > GTIOCB Output Enabled	<ul style="list-style-type: none"> <li>True</li> <li>False</li> </ul>	False	Enable the output of GTIOCB on a pin.
Output > GTIOCB Stop Level	<ul style="list-style-type: none"> <li>Pin Level Low</li> <li>Pin Level High</li> </ul>	Pin Level Low	Select the behavior of the output pin when the timer is stopped.
Input > Count Up Source	MCU Specific Options		Select external source that will increment the counter. If any count up source is selected, the timer will count the external sources only. It will not count PCLKD cycles.
Input > Count Down Source	MCU Specific Options		Select external source that will decrement the counter. If any count down source is selected, the timer will count the external sources only. It will not count PCLKD cycles.
Input > Start Source	MCU Specific Options		Select external source that will start the timer.  For pulse width measurement, set the Start Source and the Clear Source to the trigger edge (the edge to start the measurement), and set the Stop Source and Capture Source (either A or B) to the opposite edge (the edge to stop the measurement).
			For pulse period measurement, set the Start Source, the Clear Source, and the Capture Source (either A or B) to the trigger edge (the edge to start the measurement).
Input > Stop Source	MCU Specific Options		Select external source that will stop the timer.
Input > Clear Source	MCU Specific Options		Select external source

			that will clear the timer.
Input > Capture A Source	MCU Specific Options		Select external source that will trigger a capture A event.
Input > Capture B Source	MCU Specific Options		Select external source that will trigger a capture B event.
Input > Noise Filter A Sampling Clock Select	<ul style="list-style-type: none"> <li>• No Filter</li> <li>• Filter PCLKD / 1</li> <li>• Filter PCLKD / 4</li> <li>• Filter PCLKD / 16</li> <li>• Filter PCLKD / 64</li> </ul>	No Filter	Select the input filter for GTIOCA.
Input > Noise Filter B Sampling Clock Select	<ul style="list-style-type: none"> <li>• No Filter</li> <li>• Filter PCLKD / 1</li> <li>• Filter PCLKD / 4</li> <li>• Filter PCLKD / 16</li> <li>• Filter PCLKD / 64</li> </ul>	No Filter	Select the input filter for GTIOCB.
Interrupts > Callback	Name must be a valid C symbol	NULL	A user callback function can be specified here. If this callback function is provided, it will be called from the interrupt service routine (ISR) each time the timer period elapses
Interrupts > Overflow/Crest Interrupt Priority	MCU Specific Options		Select the overflow interrupt priority. This is the crest interrupt for triangle-wave PWM.
Interrupts > Capture A Interrupt Priority	MCU Specific Options		Select the interrupt priority for capture A.
Interrupts > Capture B Interrupt Priority	MCU Specific Options		Select the interrupt priority for capture B.
Interrupts > Trough Interrupt Priority	MCU Specific Options		Select the interrupt priority for the trough interrupt (triangle-wave PWM only).
Extra Features > Output Disable > POEG Link	<ul style="list-style-type: none"> <li>• POEG Channel 0</li> <li>• POEG Channel 1</li> <li>• POEG Channel</li> </ul>	POEG Channel 0	Select which POEG to link this GPT channel to.

	2		
	• POEG Channel		
	3		
Extra Features > Output Disable > Output Disable POEG Trigger	<ul style="list-style-type: none"> <li>• Dead Time Error</li> <li>• GTIOCA and GTIOCB High Level</li> <li>• GTIOCA and GTIOCB Low Level</li> </ul>		Select which errors send an output disable trigger to POEG. Dead time error is only available on GPT32E and GPT32EH variants.
Extra Features > Output Disable > GTIOCA Disable Setting	<ul style="list-style-type: none"> <li>• Disable Prohibited</li> <li>• Set Hi Z</li> <li>• Level Low</li> <li>• Level High</li> </ul>	Disable Prohibited	Select the disable setting for GTIOCA.
Extra Features > Output Disable > GTIOCB Disable Setting	<ul style="list-style-type: none"> <li>• Disable Prohibited</li> <li>• Set Hi Z</li> <li>• Level Low</li> <li>• Level High</li> </ul>	Disable Prohibited	Select the disable setting for GTIOCB.
Extra Features > ADC Trigger > Start Event Trigger (GPTE/GPTEH only)	<ul style="list-style-type: none"> <li>• Trigger Event A/D Converter Start Request A During Up Counting</li> <li>• Trigger Event A/D Converter Start Request A During Down Counting</li> <li>• Trigger Event A/D Converter Start Request B During Up Counting</li> <li>• Trigger Event A/D Converter Start Request B During Down Counting</li> </ul>		Select which A/D converter start request interrupts to generate and at which point in the cycle to generate them. This value only applies to the GPT32E and GPT32EH variants.
Extra Features > Dead Time > Dead Time Count Up (Raw Counts)	Must be a valid non-negative integer with a maximum configurable value of 4294967295 (0xffffffff).	0	Select the dead time to apply during up counting. This value also applies during down counting for the GPT32 and GPT16 variants.
Extra Features > Dead Time > Dead Time Count Down (Raw	Must be a valid non-negative integer with a maximum configurable	0	Select the dead time to apply during down counting. This value

Counts) (GPTE/GPTEH only)	value of 4294967295 (0xffffffff).		only applies to the GPT32E and GPT32EH variants.
Extra Features > ADC Trigger (GPTE/GPTEH only) > ADC A Compare Match (Raw Counts)	Must be a valid non-negative integer with a maximum configurable value of 4294967295 (0xffffffff).	0	Select the compare match value that generates a GPTn AD TRIG A event. This value only applies to the GPT32E and GPT32EH variants.
Extra Features > ADC Trigger (GPTE/GPTEH only) > ADC B Compare Match (Raw Counts)	Must be a valid non-negative integer with a maximum configurable value of 4294967295 (0xffffffff).	0	Select the compare match value that generates a GPTn AD TRIG B event. This value only applies to the GPT32E and GPT32EH variants.
Extra Features > Interrupt Skipping (GPTE/GPTEH only) > Interrupt to Count	<ul style="list-style-type: none"> <li>• None</li> <li>• Overflow and Underflow (sawtooth)</li> <li>• Crest (triangle)</li> <li>• Trough (triangle)</li> </ul>	None	Select the count source for interrupt skipping. The interrupt skip counter increments after each source event. All crest/overflow and trough/underflow interrupts are skipped when the interrupt skip counter is non-zero. This value only applies to the GPT32E and GPT32EH variants.
Extra Features > Interrupt Skipping (GPTE/GPTEH only) > Interrupt Skip Count	<ul style="list-style-type: none"> <li>• 0</li> <li>• 1</li> <li>• 2</li> <li>• 3</li> <li>• 4</li> <li>• 5</li> <li>• 6</li> <li>• 7</li> </ul>	0	Select the number of interrupts to skip. This value only applies to the GPT32E and GPT32EH variants.
Extra Features > Interrupt Skipping (GPTE/GPTEH only) > Skip ADC Events	<ul style="list-style-type: none"> <li>• None</li> <li>• ADC A Compare Match</li> <li>• ADC B Compare Match</li> <li>• ADC A and B Compare Match</li> </ul>	module.driver.timer.interrupt_skip.adc.none	Select ADC events to suppress when the interrupt skip count is not zero. This value only applies to the GPT32E and GPT32EH variants.
Extra Features > Extra Features	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Disabled	Select whether to enable extra features on this channel.

## Clock Configuration

The GPT clock is based on the PCLKD frequency. You can set the PCLKD frequency using the **Clocks** tab of the RA Configuration editor or by using the CGC Interface at run-time.

## Pin Configuration

This module can use GTETRGA, GTETRGB, GTETRGC, GTETRGD, GTIOCA and GTIOCB pins as count sources.

This module can use GTIOCA and GTIOCB pins as output pins for periodic or PWM signals.

This module can use GTIOCA and GTIOCB as input pins to measure input signals.

## Usage Notes

### Maximum Period for GPT32

The RA Configuration editor will automatically calculate the period count value and source clock divider based on the selected period time, units and clock speed.

When the selected period unit is "Raw counts", the maximum period setting is 0x4000000000 on a 32-bit timer or 0x0x4000000 on a 16-bit timer. This will configure the timer with the maximum period and a count clock divisor of 128.

#### Note

*When manually changing the timer period counts the maximum value for a 32-bit GPT is 0x100000000. This number overflows the 32-bit value for `timer_cfg_t::period_counts`. To configure the timer for the maximum period, set `timer_cfg_t::period_counts` to 0.*

### Updating Period and Duty Cycle

The period and duty cycle are updated after the next counter overflow after calling `R_GPT_PeriodSet()` or `R_GPT_DutyCycleSet()`. To force them to update before the next counter overflow, call `R_GPT_Reset()` while the counter is running.

### One-Shot Mode

The GPT timer does not support one-shot mode natively. One-shot mode is achieved by stopping the timer in the interrupt service routine before the callback is called. If the interrupt is not serviced before the timer period expires again, the timer generates more than one event. The callback is only called once in this case, but multiple events may be generated if the timer is linked to the [Data Transfer Controller \(r\\_dtc\)](#).

### One-Shot Mode Output

The output waveform in one-shot mode is one PCLKD cycle less than the configured period. The configured period must be at least 2 counts to generate an output pulse.

Examples of one-shot signals that can be generated by this module are shown below:

## GPT One-Shot Output

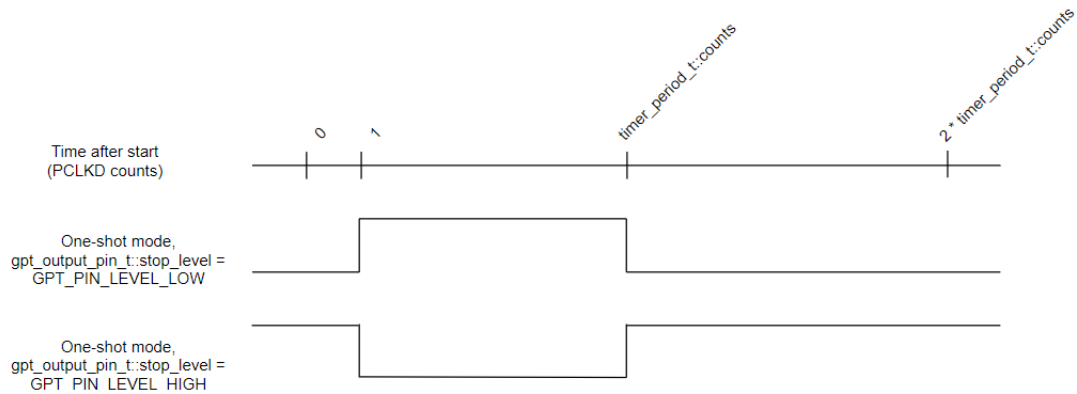


Figure 162: GPT One-Shot Output

## Periodic Output

The GTIOC pin toggles twice each time the timer expires in periodic mode. This is achieved by defining a PWM wave at a 50 percent duty cycle so that the period of the resulting square wave (from rising edge to rising edge) matches the period of the GPT timer. Since the periodic output is actually a PWM output, the time at the stop level is one cycle shorter than the time opposite the stop level for odd period values.

Examples of periodic signals that can be generated by this module are shown below:

## GPT Periodic Output

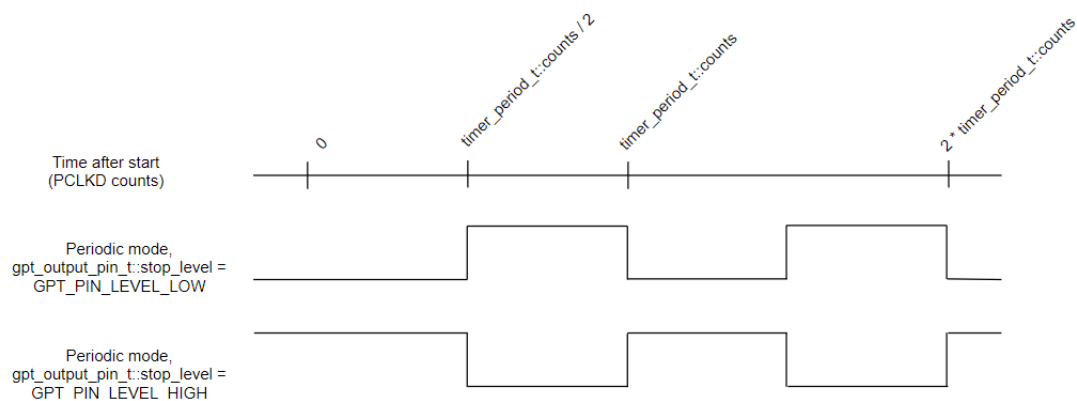


Figure 163: GPT Periodic Output

## PWM Output

The PWM output signal is high at the beginning of the cycle and low at the end of the cycle.

Examples of PWM signals that can be generated by this module are shown below:

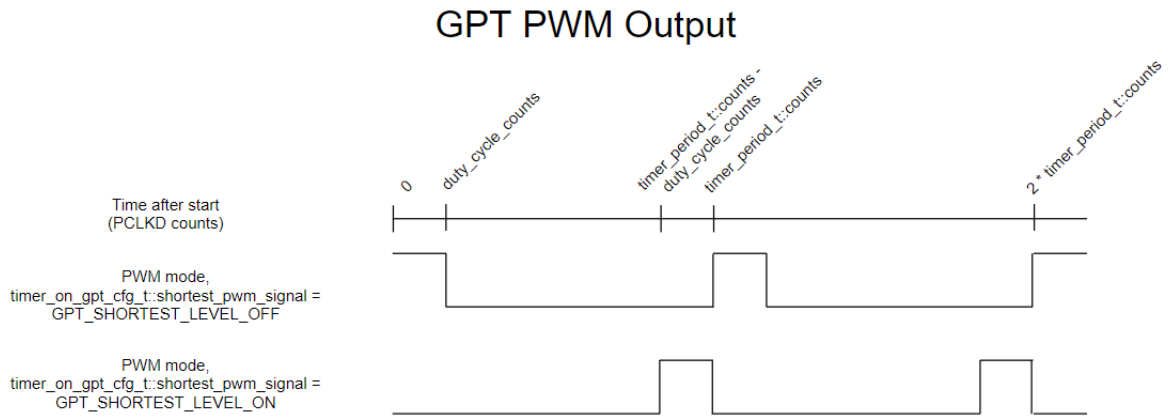


Figure 164: GPT PWM Output

### Triangle-Wave PWM Output

Examples of PWM signals that can be generated by this module are shown below. The `duty_cycle_counts` can be modified using `R_GPT_DutyCycleSet()` in the crest interrupt and updated at the following trough for symmetric PWM or modified in both the crest/trough interrupts and updated at the following trough/crest for asymmetric PWM.

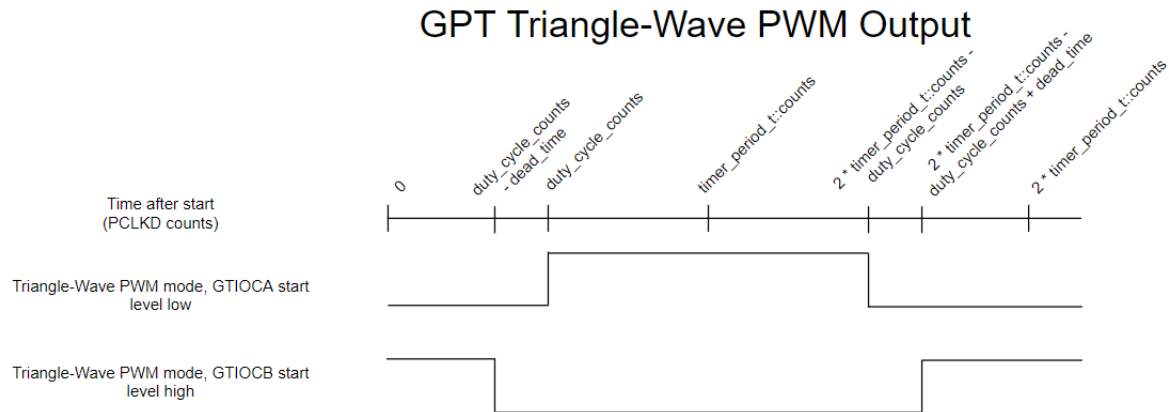


Figure 165: GPT Triangle-Wave PWM Output

### Event Counting

Event counting can be done by selecting up or down counting sources from GTETRГ pins, ELC events, or GTIOC pins. In event counting mode, the GPT counter is not affected by PCLKD.

*Note*

*In event counting mode, the application must call `R_GPT_Start()` to enable event counting. The counter will not change after calling `R_GPT_Start()` until an event occurs.*

### Pulse Measurement

If the capture edge occurs before the start edge in pulse measurement, the first capture is invalid (0).

### Controlling GPT with GTETRГ Edges



The GPT timer can be configured to stop, start, clear, count up, or count down when a GTETRG rising or falling edge occurs.

#### Note

*The GTETRG pins are shared by all GPT channels.  
GTETRG pins require POEG to be on (example code for this is provided in GPT Free Running Counter Example).  
If input filtering is required on the GTETRG pins, that must also be handled outside this module.*

## Controlling GPT with ELC Events

The GPT timer can be configured to stop, start, clear, count up, or count down when an ELC event occurs.

#### Note

*The configurable ELC GPT sources are shared by all GPT channels.  
The event links for the ELC must be configured outside this module.*

## Triggering ELC Events with GPT

The GPT timer can trigger the start of other peripherals. The [Event Link Controller \(r\\_elc\)](#) guide provides a list of all available peripherals.

## Enabling External Sources for Start, Stop, Clear, or Capture

`R_GPT_Enable()` must be called when external sources are used for start, stop, clear, or capture.

## Interrupt Skipping

When an interrupt skipping source is selected a hardware counter will increment each time the selected event occurs. Each interrupt past the first (up to the specified skip count) will be suppressed. If ADC events are selected for skipping they will also be suppressed except during the timer period leading to the selected interrupt skipping event (see below diagram).

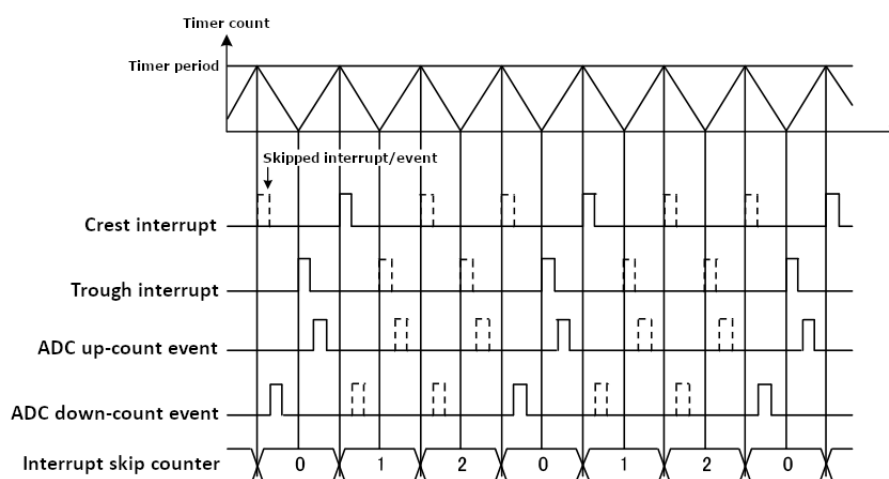


Figure 166: Crest interrupt skipping in triangle-wave PWM modes (skip count 2)

## Examples

## GPT Basic Example

This is a basic example of minimal use of the GPT in an application.

```
void gpt_basic_example (void)
{
    fsp_err_t err = FSP_SUCCESS;
    /* Initializes the module. */
    err = R_GPT_Open(&g_timer0_ctrl, &g_timer0_cfg);
    /* Handle any errors. This function should be defined by the user. */
    handle_error(err);
    /* Start the timer. */
    (void) R_GPT_Start(&g_timer0_ctrl);
}
```

## GPT Callback Example

This is an example of a timer callback.

```
/* Example callback called when timer expires. */
void timer_callback (timer_callback_args_t * p_args)
{
    if (TIMER_EVENT_CYCLE_END == p_args->event)
    {
        /* Add application code to be called periodically here. */
    }
}
```

## GPT Free Running Counter Example

To use the GPT as a free running counter, select periodic mode and set the the Period to 0xFFFFFFFF for a 32-bit timer or 0xFFFF for a 16-bit timer.

```
void gpt_counter_example (void)
{
    fsp_err_t err = FSP_SUCCESS;
    /* (Optional) If event count mode is used to count edges on a GTETRQ pin, POEG must
```

```

be started to use GTETRGR.

 * Reference Note 1 of Table 23.2 "GPT functions" in the RA6M3 manual
R01UH0886EJ0100. */

R_BSP_MODULE_START(FSP_IP_POEG, 0U);

/* Initializes the module. */
err = R_GPT_Open(&g_timer0_ctrl, &g_timer0_cfg);
/* Handle any errors. This function should be defined by the user. */
handle_error(err);

/* Start the timer. */
(void) R_GPT_Start(&g_timer0_ctrl);
/* (Optional) Stop the timer. */
(void) R_GPT_Stop(&g_timer0_ctrl);
/* Read the current counter value. Counter value is in status.counter. */
timer_status_t status;
(void) R_GPT_StatusGet(&g_timer0_ctrl, &status);
}

```

## GPT Input Capture Example

This is an example of using the GPT to capture pulse width or pulse period measurements.

```

/* Example callback called when a capture occurs. */
uint64_t g_captured_time = 0U;
uint32_t g_capture_overflows = 0U;
void timer_capture_callback (timer_callback_args_t * p_args)
{
    if ((TIMER_EVENT_CAPTURE_A == p_args->event) || (TIMER_EVENT_CAPTURE_B ==
p_args->event))
    {
        /* (Optional) Get the current period if not known. */
        timer_info_t info;
        (void) R_GPT_InfoGet(&g_timer0_ctrl, &info);
        uint64_t period = info.period_counts;

        /* The maximum period is one more than the maximum 32-bit number, but will be
reflected as 0 in

```

```
* timer_info_t::period_counts. */
if (0U == period)
{
    period = UINT32_MAX + 1U;
}
g_captured_time = (period * g_capture_overflows) + p_args->capture;
g_capture_overflows = 0U;
}
if (TIMER_EVENT_CYCLE_END == p_args->event)
{
    /* An overflow occurred during capture. This must be accounted for at the
application layer. */
    g_capture_overflows++;
}
}
void gpt_capture_example (void)
{
    fsp_err_t err = FSP_SUCCESS;
    /* Initializes the module. */
    err = R_GPT_Open(&g_timer0_ctrl, &g_timer0_cfg);
    /* Handle any errors. This function should be defined by the user. */
    handle_error(err);
    /* Enable captures. Captured values arrive in the interrupt. */
    (void) R_GPT_Enable(&g_timer0_ctrl);
    /* (Optional) Disable captures. */
    (void) R_GPT_Disable(&g_timer0_ctrl);
}
```

### GPT Period Update Example

This an example of updating the period.

```
#define GPT_EXAMPLE_MSEC_PER_SEC (1000)
#define GPT_EXAMPLE_DESIRED_PERIOD_MSEC (20)
/* This example shows how to calculate a new period value at runtime. */
```

```
void gpt_period_calculation_example (void)
{
    fsp_err_t err = FSP_SUCCESS;
    /* Initializes the module. */
    err = R_GPT_Open(&g_timer0_ctrl, &g_timer0_cfg);
    /* Handle any errors. This function should be defined by the user. */
    handle_error(err);
    /* Start the timer. */
    (void) R_GPT_Start(&g_timer0_ctrl);
    /* Get the source clock frequency (in Hz). There are 3 ways to do this in FSP:
    * - If the PCLKD frequency has not changed since reset, the source clock frequency
    is
    * BSP_STARTUP_PCLKD_HZ >> timer_cfg_t::source_div
    * - Use the R_GPT_InfoGet function (it accounts for the divider).
    * - Calculate the current PCLKD frequency using
    R_FSP_SystemClockHzGet(FSP_PRIV_CLOCK_PCLKD) and right shift
    * by timer_cfg_t::source_div.
    *
    * This example uses the 3rd option (R_FSP_SystemClockHzGet).
    */
    uint32_t pclkd_freq_hz = R_FSP_SystemClockHzGet(FSP_PRIV_CLOCK_PCLKD) >>
    g_timer0_cfg.source_div;
    /* Calculate the desired period based on the current clock. Note that this
    calculation could overflow if the
    * desired period is larger than UINT32_MAX / pclkd_freq_hz. A cast to uint64_t is
    used to prevent this. */
    uint32_t period_counts =
        (uint32_t) (((uint64_t) pclkd_freq_hz * GPT_EXAMPLE_DESIRED_PERIOD_MSEC) /
    GPT_EXAMPLE_MSEC_PER_SEC);
    /* Set the calculated period. */
    err = R_GPT_PeriodSet(&g_timer0_ctrl, period_counts);
    handle_error(err);
}
```

## GPT Duty Cycle Update Example

This an example of updating the duty cycle.

```
#define GPT_EXAMPLE_DESIRED_DUTY_CYCLE_PERCENT (25)
#define GPT_EXAMPLE_MAX_PERCENT (100)
/* This example shows how to calculate a new duty cycle value at runtime. */
void gpt_duty_cycle_calculation_example (void)
{
    fsp_err_t err = FSP_SUCCESS;
    /* Initializes the module. */
    err = R_GPT_Open(&g_timer0_ctrl, &g_timer0_cfg);
    /* Handle any errors. This function should be defined by the user. */
    handle_error(err);
    /* Start the timer. */
    (void) R_GPT_Start(&g_timer0_ctrl);
    /* Get the current period setting. */
    timer_info_t info;
    (void) R_GPT_InfoGet(&g_timer0_ctrl, &info);
    uint32_t current_period_counts = info.period_counts;
    /* Calculate the desired duty cycle based on the current period. Note that if the
period could be larger than
    * UINT32_MAX / 100, this calculation could overflow. A cast to uint64_t is used to
prevent this. The cast is
    * not required for 16-bit timers. */
    uint32_t duty_cycle_counts =
        (uint32_t) (((uint64_t) current_period_counts *
GPT_EXAMPLE_DESIRED_DUTY_CYCLE_PERCENT) /
        GPT_EXAMPLE_MAX_PERCENT);
    /* Set the calculated duty cycle. */
    err = R_GPT_DutyCycleSet(&g_timer0_ctrl, duty_cycle_counts, GPT_IO_PIN_GTIOCB);
    handle_error(err);
}
```

## GPT A/D Converter Start Request Example

This is an example of using the GPT to start the ADC at a configurable A/D converter compare match value.

```
#if ((1U << GPT_EXAMPLE_CHANNEL) & (BSP_FEATURE_GPTEH_CHANNEL_MASK |
BSP_FEATURE_GPTE_CHANNEL_MASK))
/* This example shows how to configure the GPT to generate an A/D start request at an
A/D start request compare
 * match value. This example can only be used with GPTE or GPTEH variants. */
void gpt_adc_start_request_example (void)
{
    fsp_err_t err = FSP_SUCCESS;
    /* Initialize and configure the ELC. */
    err = R_ELC_Open(&g_elc_ctrl, &g_elc_cfg);
    /* Handle any errors. This function should be defined by the user. */
    handle_error(err);
    /* Configure the ELC to start a scan on ADC unit 0 when GPT channel 0. Note: This is
typically configured in
 * g_elc_cfg and already set during R_ELC_Open. */
    err = R_ELC_LinkSet(&g_elc_ctrl, ELC_PERIPHERAL_ADC0, ELC_EVENT_GPT0_AD_TRIG_A);
    handle_error(err);
    /* Globally enable ELC events. */
    err = R_ELC_Enable(&g_elc_ctrl);
    handle_error(err);
    /* Initialize the ADC to start a scan based on an ELC event trigger. Set
adc_cfg_t::trigger to
 * ADC_TRIGGER_SYNC_ELC. */
    err = R_ADC_Open(&g_adc0_ctrl, &g_adc0_cfg);
    handle_error(err);
    err = R_ADC_ScanCfg(&g_adc0_ctrl, &g_adc0_channel_cfg);
    handle_error(err);
    /* Enable ELC triggers by calling R_ADC_ScanStart(). */
    (void) R_ADC_ScanStart(&g_adc0_ctrl);
    /* Initializes the GPT module. Configure gpt_extended_pwm_cfg_t::adc_trigger to set
when the A/D start request
 * is generated. Set gpt_extended_pwm_cfg_t::adc_a_compare_match to set the desired
```

```

compare match value. */
    err = R_GPT_Open(&g_timer0_ctrl, &g_timer0_cfg);
    handle_error(err);

/* Start the timer. A/D converter start request events are generated each time the
counter is equal to the
* A/D start request compare match value. */
    (void) R_GPT_Start(&g_timer0_ctrl);
}
#endif

```

## Data Structures

struct [gpt\\_output\\_pin\\_t](#)

struct [gpt\\_instance\\_ctrl\\_t](#)

struct [gpt\\_extended\\_pwm\\_cfg\\_t](#)

struct [gpt\\_extended\\_cfg\\_t](#)

## Enumerations

enum [gpt\\_io\\_pin\\_t](#)

enum [gpt\\_pin\\_level\\_t](#)

enum [gpt\\_source\\_t](#)

enum [gpt\\_capture\\_filter\\_t](#)

enum [gpt\\_adc\\_trigger\\_t](#)

enum [gpt\\_poeg\\_link\\_t](#)

enum [gpt\\_output\\_disable\\_t](#)

enum [gpt\\_gtioc\\_disable\\_t](#)

enum [gpt\\_adc\\_compare\\_match\\_t](#)

enum [gpt\\_interrupt\\_skip\\_source\\_t](#)

enum [gpt\\_interrupt\\_skip\\_count\\_t](#)

enum [gpt\\_interrupt\\_skip\\_adc\\_t](#)



## Data Structure Documentation

### ◆ gpt\_output\_pin\_t

struct gpt_output_pin_t		
Configurations for output pins.		
Data Fields		
bool	output_enabled	Set to true to enable output, false to disable output.
<a href="#">gpt_pin_level_t</a>	stop_level	Select a stop level from <a href="#">gpt_pin_level_t</a> .

### ◆ gpt\_instance\_ctrl\_t

struct gpt_instance_ctrl_t		
Channel control block. DO NOT INITIALIZE. Initialization occurs when <a href="#">timer_api_t::open</a> is called.		

### ◆ gpt\_extended\_pwm\_cfg\_t

struct gpt_extended_pwm_cfg_t		
GPT extension for advanced PWM features.		
Data Fields		
uint8_t	trough_ipl	Trough interrupt priority.
IRQn_Type	trough_irq	Trough interrupt.
<a href="#">gpt_poeg_link_t</a>	poeg_link	Select which POEG channel controls output disable for this GPT channel.
<a href="#">gpt_output_disable_t</a>	output_disable	Select which trigger sources request output disable from POEG.
<a href="#">gpt_adc_trigger_t</a>	adc_trigger	Select trigger sources to start A/D conversion.
uint32_t	dead_time_count_up	Set a dead time value for counting up.
uint32_t	dead_time_count_down	Set a dead time value for counting down (available on GPT32E and GPT32EH only)
uint32_t	adc_a_compare_match	Select the compare match value used to trigger an A/D conversion start request using ELC_EVENT_GPT<channel>_AD_TRIG_A.
uint32_t	adc_b_compare_match	Select the compare match value used to trigger an A/D

		conversion start request using ELC_EVENT_GPT<channel>_AD_TRIG_B.
<a href="#">gpt_interrupt_skip_source_t</a>	interrupt_skip_source	Interrupt source to count for interrupt skipping.
<a href="#">gpt_interrupt_skip_count_t</a>	interrupt_skip_count	Number of interrupts to skip between events.
<a href="#">gpt_interrupt_skip_adc_t</a>	interrupt_skip_adc	ADC events to skip when interrupt skipping is enabled.
<a href="#">gpt_gtioc_disable_t</a>	gtioca_disable_setting	Select how to configure GTIOCA when output is disabled.
<a href="#">gpt_gtioc_disable_t</a>	gtiocb_disable_setting	Select how to configure GTIOCB when output is disabled.

#### ◆ gpt\_extended\_cfg\_t

struct gpt_extended_cfg_t		
GPT extension configures the output pins for GPT.		
Data Fields		
<a href="#">gpt_output_pin_t</a>	gtioca	Configuration for GPT I/O pin A.
<a href="#">gpt_output_pin_t</a>	gtiocb	Configuration for GPT I/O pin B.
<a href="#">gpt_shortest_level_t</a>	shortest_pwm_signal	
<a href="#">gpt_source_t</a>	start_source	Event sources that trigger the timer to start.
<a href="#">gpt_source_t</a>	stop_source	Event sources that trigger the timer to stop.
<a href="#">gpt_source_t</a>	clear_source	Event sources that trigger the timer to clear.
<a href="#">gpt_source_t</a>	capture_a_source	Event sources that trigger capture of GTIOCA.
<a href="#">gpt_source_t</a>	capture_b_source	Event sources that trigger capture of GTIOCB.
<a href="#">gpt_source_t</a>	count_up_source	Event sources that trigger a single up count. If GPT_SOURCE_NONE is selected for both count_up_source and count_down_source, then the timer count source is PCLK.
<a href="#">gpt_source_t</a>	count_down_source	Event sources that trigger a single down count. If GPT_SOURCE_NONE is selected for both count_up_source and count_down_source, then the timer count source is PCLK.

<a href="#">gpt_capture_filter_t</a>	capture_filter_gtioca	
<a href="#">gpt_capture_filter_t</a>	capture_filter_gtiocb	
uint8_t	capture_a_ipi	Capture A interrupt priority.
uint8_t	capture_b_ipi	Capture B interrupt priority.
IRQn_Type	capture_a_irq	Capture A interrupt.
IRQn_Type	capture_b_irq	Capture B interrupt.
<a href="#">gpt_extended_pwm_cfg_t</a> const *	p_pwm_cfg	Advanced PWM features, optional.

## Enumeration Type Documentation

### ◆ gpt\_io\_pin\_t

enum <a href="#">gpt_io_pin_t</a>	
Input/Output pins, used to select which duty cycle to update in <a href="#">R_GPT_DutyCycleSet()</a> .	
Enumerator	
GPT_IO_PIN_GTIOCA	GTIOCA.
GPT_IO_PIN_GTIOCB	GTIOCB.
GPT_IO_PIN_GTIOCA_AND_GTIOCB	GTIOCA and GTIOCB.

### ◆ gpt\_pin\_level\_t

enum <a href="#">gpt_pin_level_t</a>	
Level of GPT pin	
Enumerator	
GPT_PIN_LEVEL_LOW	Pin level low.
GPT_PIN_LEVEL_HIGH	Pin level high.

## ◆ gpt\_source\_t

enum gpt_source_t	
Sources can be used to start the timer, stop the timer, count up, or count down. These enumerations represent a bitmask. Multiple sources can be ORed together.	
Enumerator	
GPT_SOURCE_NONE	No active event sources.
GPT_SOURCE_GTETRGA_RISING	Action performed on GTETRGA rising edge.
GPT_SOURCE_GTETRGA_FALLING	Action performed on GTETRGA falling edge.
GPT_SOURCE_GTETRGB_RISING	Action performed on GTETRGB rising edge.
GPT_SOURCE_GTETRGB_FALLING	Action performed on GTETRGB falling edge.
GPT_SOURCE_GTETRGC_RISING	Action performed on GTETRGC rising edge.
GPT_SOURCE_GTETRGC_FALLING	Action performed on GTETRGC falling edge.
GPT_SOURCE_GTETRGD_RISING	Action performed on GTETRGB rising edge.
GPT_SOURCE_GTETRGD_FALLING	Action performed on GTETRGB falling edge.
GPT_SOURCE_GTIOCA_RISING_WHILE_GTIOCB_LOW	Action performed when GTIOCA input rises while GTIOCB is low.
GPT_SOURCE_GTIOCA_RISING_WHILE_GTIOCB_HIGH	Action performed when GTIOCA input rises while GTIOCB is high.
GPT_SOURCE_GTIOCA_FALLING_WHILE_GTIOCB_LOW	Action performed when GTIOCA input falls while GTIOCB is low.
GPT_SOURCE_GTIOCA_FALLING_WHILE_GTIOCB_HIGH	Action performed when GTIOCA input falls while GTIOCB is high.
GPT_SOURCE_GTIOCB_RISING_WHILE_GTIOCA_LOW	Action performed when GTIOCB input rises while GTIOCA is low.
GPT_SOURCE_GTIOCB_RISING_WHILE_GTIOCA_HIGH	Action performed when GTIOCB input rises while GTIOCA is high.
GPT_SOURCE_GTIOCB_FALLING_WHILE_GTIOCA_LOW	Action performed when GTIOCB input falls while GTIOCA is low.
GPT_SOURCE_GTIOCB_FALLING_WHILE_GTIOCA_HIGH	Action performed when GTIOCB input falls while GTIOCA is high.

GPT_SOURCE_GPT_A	Action performed on ELC GPTA event.
GPT_SOURCE_GPT_B	Action performed on ELC GPTB event.
GPT_SOURCE_GPT_C	Action performed on ELC GPTC event.
GPT_SOURCE_GPT_D	Action performed on ELC GPTD event.
GPT_SOURCE_GPT_E	Action performed on ELC GPTE event.
GPT_SOURCE_GPT_F	Action performed on ELC GPTF event.
GPT_SOURCE_GPT_G	Action performed on ELC GPTG event.
GPT_SOURCE_GPT_H	Action performed on ELC GPTH event.

#### ◆ gpt\_capture\_filter\_t

enum gpt_capture_filter_t	
Input capture signal noise filter (debounce) setting. Only available for input signals GTIOCxA and GTIOCxB. The noise filter samples the external signal at intervals of the PCLK divided by one of the values. When 3 consecutive samples are at the same level (high or low), then that level is passed on as the observed state of the signal. See "Noise Filter Function" in the hardware manual, GPT section.	
Enumerator	
GPT_CAPTURE_FILTER_NONE	None - no filtering.
GPT_CAPTURE_FILTER_PCLKD_DIV_1	PCLK/1 - fast sampling.
GPT_CAPTURE_FILTER_PCLKD_DIV_4	PCLK/4.
GPT_CAPTURE_FILTER_PCLKD_DIV_16	PCLK/16.
GPT_CAPTURE_FILTER_PCLKD_DIV_64	PCLK/64 - slow sampling.

◆ **gpt\_adc\_trigger\_t**

enum <a href="#">gpt_adc_trigger_t</a>	
Trigger options to start A/D conversion.	
Enumerator	
GPT_ADC_TRIGGER_NONE	None - no output disable request.
GPT_ADC_TRIGGER_UP_COUNT_START_ADC_A	Request A/D conversion from ADC unit 0 at up counting compare match of <a href="#">gpt_extended_pwm_cfg_t::adc_a_compare_match</a> .
GPT_ADC_TRIGGER_DOWN_COUNT_START_ADC_A	Request A/D conversion from ADC unit 0 at down counting compare match of <a href="#">gpt_extended_pwm_cfg_t::adc_a_compare_match</a> .
GPT_ADC_TRIGGER_UP_COUNT_START_ADC_B	Request A/D conversion from ADC unit 1 at up counting compare match of <a href="#">gpt_extended_pwm_cfg_t::adc_b_compare_match</a> .
GPT_ADC_TRIGGER_DOWN_COUNT_START_ADC_B	Request A/D conversion from ADC unit 1 at down counting compare match of <a href="#">gpt_extended_pwm_cfg_t::adc_b_compare_match</a> .

◆ **gpt\_poeg\_link\_t**

enum <a href="#">gpt_poeg_link_t</a>	
POEG channel to link to this channel.	
Enumerator	
GPT_POEG_LINK_POEG0	Link this GPT channel to POEG channel 0 (GTETRGA)
GPT_POEG_LINK_POEG1	Link this GPT channel to POEG channel 1 (GTETRGB)
GPT_POEG_LINK_POEG2	Link this GPT channel to POEG channel 2 (GTETRGC)
GPT_POEG_LINK_POEG3	Link this GPT channel to POEG channel 3 (GTETRGD)

◆ **gpt\_output\_disable\_t**

enum <code>gpt_output_disable_t</code>	
Select trigger to send output disable request to POEG.	
Enumerator	
<code>GPT_OUTPUT_DISABLE_NONE</code>	None - no output disable request.
<code>GPT_OUTPUT_DISABLE_DEAD_TIME_ERROR</code>	Request output disable if a dead time error occurs.
<code>GPT_OUTPUT_DISABLE_GTIOCA_GTIOCB_HIGH</code>	Request output disable if GTIOCA and GTIOCB are high at the same time.
<code>GPT_OUTPUT_DISABLE_GTIOCA_GTIOCB_LOW</code>	Request output disable if GTIOCA and GTIOCB are low at the same time.

◆ **gpt\_gtioc\_disable\_t**

enum <code>gpt_gtioc_disable_t</code>	
Disable level options for GTIOC pins.	
Enumerator	
<code>GPT_GTIOC_DISABLE_PROHIBITED</code>	Do not allow output disable.
<code>GPT_GTIOC_DISABLE_SET_HI_Z</code>	Set GTIOC to high impedance when output is disabled.
<code>GPT_GTIOC_DISABLE_LEVEL_LOW</code>	Set GTIOC level low when output is disabled.
<code>GPT_GTIOC_DISABLE_LEVEL_HIGH</code>	Set GTIOC level high when output is disabled.

◆ **gpt\_adc\_compare\_match\_t**

enum <code>gpt_adc_compare_match_t</code>	
Trigger options to start A/D conversion.	
Enumerator	
<code>GPT_ADC_COMPARE_MATCH_ADC_A</code>	Set A/D conversion start request value for GPT A/D converter start request A.
<code>GPT_ADC_COMPARE_MATCH_ADC_B</code>	Set A/D conversion start request value for GPT A/D converter start request B.

◆ **gpt\_interrupt\_skip\_source\_t**

enum <a href="#">gpt_interrupt_skip_source_t</a>	
Interrupt skipping modes	
Enumerator	
GPT_INTERRUPT_SKIP_SOURCE_NONE	Do not skip interrupts.
GPT_INTERRUPT_SKIP_SOURCE_OVERFLOW_UNDERFLOW	Count and skip overflow and underflow interrupts.
GPT_INTERRUPT_SKIP_SOURCE_CREST	Count crest interrupts for interrupt skipping. Skip the number of crest and trough interrupts configured in <a href="#">gpt_interrupt_skip_count_t</a> . When the interrupt does fire, the trough interrupt fires before the crest interrupt.
GPT_INTERRUPT_SKIP_SOURCE_TROUGH	Count trough interrupts for interrupt skipping. Skip the number of crest and trough interrupts configured in <a href="#">gpt_interrupt_skip_count_t</a> . When the interrupt does fire, the crest interrupt fires before the trough interrupt.

◆ **gpt\_interrupt\_skip\_count\_t**

enum <a href="#">gpt_interrupt_skip_count_t</a>	
Number of interrupts to skip between events	
Enumerator	
GPT_INTERRUPT_SKIP_COUNT_0	Do not skip interrupts.
GPT_INTERRUPT_SKIP_COUNT_1	Skip one interrupt.
GPT_INTERRUPT_SKIP_COUNT_2	Skip two interrupts.
GPT_INTERRUPT_SKIP_COUNT_3	Skip three interrupts.
GPT_INTERRUPT_SKIP_COUNT_4	Skip four interrupts.
GPT_INTERRUPT_SKIP_COUNT_5	Skip five interrupts.
GPT_INTERRUPT_SKIP_COUNT_6	Skip six interrupts.
GPT_INTERRUPT_SKIP_COUNT_7	Skip seven interrupts.



**◆ gpt\_interrupt\_skip\_adc\_t**

enum gpt_interrupt_skip_adc_t	
ADC events to skip during interrupt skipping	
Enumerator	
GPT_INTERRUPT_SKIP_ADC_NONE	Do not skip ADC events.
GPT_INTERRUPT_SKIP_ADC_A	Skip ADC A events.
GPT_INTERRUPT_SKIP_ADC_B	Skip ADC B events.
GPT_INTERRUPT_SKIP_ADC_A_AND_B	Skip ADC A and B events.

**Function Documentation**

◆ **R\_GPT\_Open()**

```
fsp_err_t R_GPT_Open ( timer_ctrl_t *const p_ctrl, timer_cfg_t const *const p_cfg )
```

Initializes the timer module and applies configurations. Implements `timer_api_t::open`.

GPT hardware does not support one-shot functionality natively. When using one-shot mode, the timer will be stopped in an ISR after the requested period has elapsed.

The GPT implementation of the general timer can accept a `gpt_extended_cfg_t` extension parameter.

Example:

```
/* Initializes the module. */
err = R_GPT_Open(&g_timer0_ctrl, &g_timer0_cfg);
```

**Return values**

FSP_SUCCESS	Initialization was successful and timer has started.
FSP_ERR_ASSERTION	A required input pointer is NULL or the source divider is invalid.
FSP_ERR_ALREADY_OPEN	Module is already open.
FSP_ERR_IRQ_BSP_DISABLED	<code>timer_cfg_t::mode</code> is <code>TIMER_MODE_ONE_SHOT</code> or <code>timer_cfg_t::p_callback</code> is not NULL, but ISR is not enabled. ISR must be enabled to use one-shot mode or callback.
FSP_ERR_INVALID_MODE	Triangle wave PWM is only supported if <code>GPT_CFG_OUTPUT_SUPPORT_ENABLE</code> is 2.
FSP_ERR_IP_CHANNEL_NOT_PRESENT	The channel requested in the <code>p_cfg</code> parameter is not available on this device.

◆ **R\_GPT\_Stop()**

```
fsp_err_t R_GPT_Stop ( timer_ctrl_t *const p_ctrl)
```

Stops timer. Implements `timer_api_t::stop`.

Example:

```
/* (Optional) Stop the timer. */
(void) R_GPT_Stop(&g_timer0_ctrl);
```

**Return values**

FSP_SUCCESS	Timer successfully stopped.
FSP_ERR_ASSERTION	p_ctrl was NULL.
FSP_ERR_NOT_OPEN	The instance is not opened.

◆ **R\_GPT\_Start()**

```
fsp_err_t R_GPT_Start ( timer_ctrl_t *const p_ctrl)
```

Starts timer. Implements `timer_api_t::start`.

Example:

```
/* Start the timer. */
(void) R_GPT_Start(&g_timer0_ctrl);
```

**Return values**

FSP_SUCCESS	Timer successfully started.
FSP_ERR_ASSERTION	p_ctrl was NULL.
FSP_ERR_NOT_OPEN	The instance is not opened.

◆ **R\_GPT\_Reset()**

```
fsp_err_t R_GPT_Reset ( timer_ctrl_t *const p_ctrl)
```

Resets the counter value to 0. Implements `timer_api_t::reset`.

**Note**

*This function also updates to the new period if no counter overflow has occurred since the last call to `R_GPT_PeriodSet()`.*

**Return values**

FSP_SUCCESS	Counter value written successfully.
FSP_ERR_ASSERTION	p_ctrl was NULL.
FSP_ERR_NOT_OPEN	The instance is not opened.

◆ **R\_GPT\_Enable()**

```
fsp_err_t R_GPT_Enable ( timer_ctrl_t *const p_ctrl)
```

Enables external event triggers that start, stop, clear, or capture the counter. Implements `timer_api_t::enable`.

**Example:**

```
/* Enable captures. Captured values arrive in the interrupt. */
(void) R_GPT_Enable(&g_timer0_ctrl);
```

**Return values**

FSP_SUCCESS	External events successfully enabled.
FSP_ERR_ASSERTION	p_ctrl was NULL.
FSP_ERR_NOT_OPEN	The instance is not opened.

◆ **R\_GPT\_Disable()**

```
fsp_err_t R_GPT_Disable ( timer_ctrl_t *const p_ctrl)
```

Disables external event triggers that start, stop, clear, or capture the counter. Implements [timer\\_api\\_t::disable](#).

**Note**

*The timer could be running after [R\\_GPT\\_Disable\(\)](#). To ensure it is stopped, call [R\\_GPT\\_Stop\(\)](#).*

Example:

```
/* (Optional) Disable captures. */
(void) R_GPT_Disable(&g_timer0_ctrl);
```

**Return values**

FSP_SUCCESS	External events successfully disabled.
FSP_ERR_ASSERTION	p_ctrl was NULL.
FSP_ERR_NOT_OPEN	The instance is not opened.

◆ **R\_GPT\_PeriodSet()**

```
fsp_err_t R_GPT_PeriodSet ( timer_ctrl_t *const p_ctrl, uint32_t const period_counts )
```

Sets period value provided. If the timer is running, the period will be updated after the next counter overflow. If the timer is stopped, this function resets the counter and updates the period. Implements [timer\\_api\\_t::periodSet](#).

**Warning**

If periodic output is used, the duty cycle buffer registers are updated after the period buffer register. If this function is called while the timer is running and a GPT overflow occurs during processing, the duty cycle will not be the desired 50% duty cycle until the counter overflow after processing completes.

Example:

```
/* Get the source clock frequency (in Hz). There are 3 ways to do this in FSP:
 * - If the PCLKD frequency has not changed since reset, the source clock frequency
is
 * BSP_STARTUP_PCLKD_HZ >> timer_cfg_t::source_div
 * - Use the R_GPT_InfoGet function (it accounts for the divider).
 * - Calculate the current PCLKD frequency using
R_FSP_SystemClockHzGet(FSP_PRIV_CLOCK_PCLKD) and right shift
 * by timer_cfg_t::source_div.
 *
```

```

* This example uses the 3rd option (R_FSP_SystemClockHzGet).
*/
uint32_t pclkd_freq_hz = R_FSP_SystemClockHzGet(FSP_PRIV_CLOCK_PCLKD) >>
g_timer0_cfg.source_div;
/* Calculate the desired period based on the current clock. Note that this
calculation could overflow if the
* desired period is larger than UINT32_MAX / pclkd_freq_hz. A cast to uint64_t is
used to prevent this. */
uint32_t period_counts =
    (uint32_t) (((uint64_t) pclkd_freq_hz * GPT_EXAMPLE_DESIRED_PERIOD_MSEC) /
GPT_EXAMPLE_MSEC_PER_SEC);
/* Set the calculated period. */
err = R_GPT_PeriodSet(&g_timer0_ctrl, period_counts);
handle_error(err);

```

**Return values**

FSP_SUCCESS	Period value written successfully.
FSP_ERR_ASSERTION	p_ctrl was NULL.
FSP_ERR_NOT_OPEN	The instance is not opened.

**◆ R\_GPT\_DutyCycleSet()**

```

fsp_err_t R_GPT_DutyCycleSet ( timer_ctrl_t *const p_ctrl, uint32_t const duty_cycle_counts,
uint32_t const pin )

```

Sets duty cycle on requested pin. Implements `timer_api_t::dutyCycleSet`.

Duty cycle is updated in the buffer register. The updated duty cycle is reflected after the next cycle end (counter overflow).

**Example:**

```

/* Get the current period setting. */
timer_info_t info;
(void) R_GPT_InfoGet(&g_timer0_ctrl, &info);
uint32_t current_period_counts = info.period_counts;
/* Calculate the desired duty cycle based on the current period. Note that if the
period could be larger than
* UINT32_MAX / 100, this calculation could overflow. A cast to uint64_t is used to

```

```

prevent this. The cast is
 * not required for 16-bit timers. */
uint32_t duty_cycle_counts =
    (uint32_t) (((uint64_t) current_period_counts *
GPT_EXAMPLE_DESIRED_DUTY_CYCLE_PERCENT) /
    GPT_EXAMPLE_MAX_PERCENT);
/* Set the calculated duty cycle. */
err = R_GPT_DutyCycleSet(&g_timer0_ctrl, duty_cycle_counts, GPT_IO_PIN_GTIOCB);
handle_error(err);

```

### Parameters

[in]	p_ctrl	Pointer to instance control block.
[in]	duty_cycle_counts	Duty cycle to set in counts.
[in]	pin	Use gpt_io_pin_t to select GPT_IO_PIN_GTIOCA or GPT_IO_PIN_GTIOCB

### Return values

FSP_SUCCESS	Duty cycle updated successfully.
FSP_ERR_ASSERTION	p_ctrl was NULL or the pin is not one of gpt_io_pin_t
FSP_ERR_NOT_OPEN	The instance is not opened.
FSP_ERR_INVALID_ARGUMENT	Duty cycle is larger than period.
FSP_ERR_UNSUPPORTED	GPT_CFG_OUTPUT_SUPPORT_ENABLE is 0.

◆ **R\_GPT\_InfoGet()**

```
fsp_err_t R_GPT_InfoGet ( timer_ctrl_t*const p_ctrl, timer_info_t*const p_info )
```

Get timer information and store it in provided pointer p\_info. Implements `timer_api_t::infoGet`.

Example:

```
/* (Optional) Get the current period if not known. */
timer_info_t info;
(void) R_GPT_InfoGet(&g_timer0_ctrl, &info);
uint64_t period = info.period_counts;

/* The maximum period is one more than the maximum 32-bit number, but will be
reflected as 0 in
* timer_info_t::period_counts. */
if (0U == period)
{
    period = UINT32_MAX + 1U;
}
```

**Return values**

FSP_SUCCESS	Period, count direction, frequency, and ELC event written to caller's structure successfully.
FSP_ERR_ASSERTION	p_ctrl or p_info was NULL.
FSP_ERR_NOT_OPEN	The instance is not opened.



◆ **R\_GPT\_StatusGet()**

```
fsp_err_t R_GPT_StatusGet ( timer_ctrl_t *const p_ctrl, timer_status_t *const p_status )
```

Get current timer status and store it in provided pointer p\_status. Implements `timer_api_t::statusGet`.

Example:

```
/* Read the current counter value. Counter value is in status.counter. */
timer_status_t status;

(void) R_GPT_StatusGet(&g_timer0_ctrl, &status);
```

**Return values**

FSP_SUCCESS	Current timer state and counter value set successfully.
FSP_ERR_ASSERTION	p_ctrl or p_status was NULL.
FSP_ERR_NOT_OPEN	The instance is not opened.

◆ **R\_GPT\_CounterSet()**

```
fsp_err_t R_GPT_CounterSet ( timer_ctrl_t *const p_ctrl, uint32_t counter )
```

Set counter value.

*Note*

*Do not call this API while the counter is counting. The counter value can only be updated while the counter is stopped.*

**Return values**

FSP_SUCCESS	Counter value updated.
FSP_ERR_ASSERTION	p_ctrl or p_status was NULL.
FSP_ERR_NOT_OPEN	The instance is not opened.
FSP_ERR_IN_USE	The timer is running. Stop the timer before calling this function.

◆ **R\_GPT\_OutputEnable()**

```
fsp_err_t R_GPT_OutputEnable ( timer_ctrl_t *const p_ctrl, gpt_io_pin_t pin )
```

Enable output for GTIOCA and/or GTIOCB.

**Return values**

FSP_SUCCESS	Output is enabled.
FSP_ERR_ASSERTION	p_ctrl or p_status was NULL.
FSP_ERR_NOT_OPEN	The instance is not opened.

◆ **R\_GPT\_OutputDisable()**

```
fsp_err_t R_GPT_OutputDisable ( timer_ctrl_t *const p_ctrl, gpt_io_pin_t pin )
```

Disable output for GTIOCA and/or GTIOCB.

**Return values**

FSP_SUCCESS	Output is disabled.
FSP_ERR_ASSERTION	p_ctrl or p_status was NULL.
FSP_ERR_NOT_OPEN	The instance is not opened.

◆ **R\_GPT\_AdcTriggerSet()**

```
fsp_err_t R_GPT_AdcTriggerSet ( timer_ctrl_t *const p_ctrl, gpt_adc_compare_match_t  
which_compare_match, uint32_t compare_match_value )
```

Set A/D converter start request compare match value.

**Return values**

FSP_SUCCESS	Counter value updated.
FSP_ERR_ASSERTION	p_ctrl or p_status was NULL.
FSP_ERR_NOT_OPEN	The instance is not opened.

◆ **R\_GPT\_CallbackSet()**

```
fsp_err_t R_GPT_CallbackSet ( timer_ctrl_t *const p_api_ctrl, void (*)(timer_callback_args_t *)
p_callback, void const *const p_context, timer_callback_args_t *const p_callback_memory )
```

Updates the user callback with the option to provide memory for the callback argument structure. Implements `timer_api_t::callbackSet`.

**Return values**

FSP_SUCCESS	Callback updated successfully.
FSP_ERR_ASSERTION	A required pointer is NULL.
FSP_ERR_NOT_OPEN	The control block has not been opened.
FSP_ERR_NO_CALLBACK_MEMORY	<code>p_callback</code> is non-secure and <code>p_callback_memory</code> is either secure or NULL.

◆ **R\_GPT\_Close()**

```
fsp_err_t R_GPT_Close ( timer_ctrl_t *const p_ctrl)
```

Stops counter, disables output pins, and clears internal driver data. Implements `timer_api_t::close`.

**Return values**

FSP_SUCCESS	Successful close.
FSP_ERR_ASSERTION	<code>p_ctrl</code> was NULL.
FSP_ERR_NOT_OPEN	The instance is not opened.

◆ **R\_GPT\_VersionGet()**

```
fsp_err_t R_GPT_VersionGet ( fsp_version_t *const p_version)
```

Sets driver version based on compile time macros. Implements `timer_api_t::versionGet`.

**Return values**

FSP_SUCCESS	Version stored in <code>p_version</code> .
FSP_ERR_ASSERTION	<code>p_version</code> was NULL.

## 4.2.24 General PWM Timer Three-Phase Motor Control Driver (r\_gpt\_three\_phase)

### Modules

#### Functions

fsp\_err\_t R\_GPT\_THREE\_PHASE\_Open (three\_phase\_ctrl\_t \*const p\_ctrl, three\_phase\_cfg\_t const \*const p\_cfg)

fsp\_err\_t R\_GPT\_THREE\_PHASE\_Stop (three\_phase\_ctrl\_t \*const p\_ctrl)

fsp\_err\_t R\_GPT\_THREE\_PHASE\_Start (three\_phase\_ctrl\_t \*const p\_ctrl)

fsp\_err\_t R\_GPT\_THREE\_PHASE\_Reset (three\_phase\_ctrl\_t \*const p\_ctrl)

fsp\_err\_t R\_GPT\_THREE\_PHASE\_DutyCycleSet (three\_phase\_ctrl\_t \*const p\_ctrl, three\_phase\_duty\_cycle\_t \*const p\_duty\_cycle)

fsp\_err\_t R\_GPT\_THREE\_PHASE\_CallbackSet (three\_phase\_ctrl\_t \*const p\_ctrl, void(\*p\_callback)(timer\_callback\_args\_t \*), void const \*const p\_context, timer\_callback\_args\_t \*const p\_callback\_memory)

fsp\_err\_t R\_GPT\_THREE\_PHASE\_Close (three\_phase\_ctrl\_t \*const p\_ctrl)

fsp\_err\_t R\_GPT\_THREE\_PHASE\_VersionGet (fsp\_version\_t \*const p\_version)

#### Detailed Description

Driver for 3-phase motor control using the GPT peripheral on RA MCUs. This module implements the [Three-Phase Interface](#).

## Overview

The General PWM Timer (GPT) Three-Phase driver provides basic functionality for synchronously starting and stopping three PWM channels for use in 3-phase motor control applications. A function is additionally provided to allow setting duty cycle values for all three channels, optionally with double-buffering.

#### Features

The GPT Three-Phase driver provides the following functions:

- Synchronize configuration of three GPT channels
- Synchronously start, stop and reset all three GPT channels
- Set duty cycle on all three channels with one function

## Configuration

## Build Time Configurations for r\_gpt\_three\_phase

The following build time configurations are defined in fsp\_cfg/r\_gpt\_three\_phase\_cfg.h:

Configuration	Options	Default	Description
Parameter Checking	<ul style="list-style-type: none"> <li>• Default (BSP)</li> <li>• Enabled</li> <li>• Disabled</li> </ul>	Default (BSP)	If selected code for parameter checking is included in the build.

## Configurations for Driver > Timers > Three-Phase PWM Driver on r\_gpt\_three\_phase

This module can be added to the Stacks tab via New Stack > Driver > Timers > Three-Phase PWM Driver on r\_gpt\_three\_phase. Non-secure callable guard functions can be generated for this module by right clicking the module in the RA Configuration tool and checking the "Non-secure Callable" box.

Configuration	Options	Default	Description
General > Name	Name must be a valid C symbol	g_three_phase0	Module name.
General > Mode	<ul style="list-style-type: none"> <li>• Triangle-Wave Symmetric PWM</li> <li>• Triangle-Wave Asymmetric PWM</li> </ul>	Triangle-Wave Symmetric PWM	<p>Mode selection.</p> <p>Triangle-Wave Symmetric PWM: Generates symmetric PWM waveforms with duty cycle determined by compare match set during a crest interrupt and updated at the next trough.</p> <p>Triangle-Wave Asymmetric PWM: Generates asymmetric PWM waveforms with duty cycle determined by compare match set during a crest/trough interrupt and updated at the next trough/crest.</p>
General > Period	Value must be a non-negative integer less than or equal to 0x4000000000	15	Specify the timer period in units selected below. Setting the period to 0x100000000 raw counts results in the maximum period. Set the period to 0x100000000 raw counts for a free running timer or an input capture configuration. The period can be set up to 0x4000000000, which

will use a divider of 1024 with the maximum period.

General > Period Unit	<ul style="list-style-type: none"> <li>• Raw Counts</li> <li>• Nanoseconds</li> <li>• Microseconds</li> <li>• Milliseconds</li> <li>• Seconds</li> <li>• Hertz</li> <li>• Kilohertz</li> </ul>	Kilohertz	Unit of the period specified above
General > GPT U-Channel	Value must be an integer greater than or equal to 0	0	Specify the GPT channel for U signal output.
General > GPT V-Channel	Value must be an integer greater than or equal to 0	1	Specify the GPT channel for V signal output.
General > GPT W-Channel	Value must be an integer greater than or equal to 0	2	Specify the GPT channel for W signal output.
General > Callback Channel	<ul style="list-style-type: none"> <li>• U-Channel</li> <li>• V-Channel</li> <li>• W-Channel</li> </ul>	U-Channel	Specify the GPT channel to set a callback for when using R_GPT_THREE_PHASE_CallbackSet.
General > Buffer Mode	<ul style="list-style-type: none"> <li>• Single Buffer</li> <li>• Double Buffer</li> </ul>	Single Buffer	When Double Buffer is selected the 'duty_buffer' array in <a href="#">three_phase_duty_cycle_t</a> is used as a buffer for the 'duty' array. This allows setting the duty cycle for the next two crest/trough events in asymmetric mode with only one call to R_GPT_THREE_PHASE_DutyCycleSet.
General > GTIOCA Stop Level	<ul style="list-style-type: none"> <li>• Pin Level Low</li> <li>• Pin Level High</li> </ul>	Pin Level Low	Select the behavior of the output pin when the timer is stopped.
General > GTIOCB Stop Level	<ul style="list-style-type: none"> <li>• Pin Level Low</li> <li>• Pin Level High</li> </ul>	Pin Level Low	Select the behavior of the output pin when the timer is stopped.
Extra Features > Dead Time > Dead Time Count Up (Raw Counts)	Must be a valid non-negative integer with a maximum configurable value of 4294967295 (0xffffffff).	0	Select the dead time to apply during up counting. This value also applies during down counting for the GPT32 and GPT16

Extra Features > Dead Time > Dead Time Count Down (Raw Counts) (GPTE/GPTEH only)	Must be a valid non-negative integer with a maximum configurable value of 4294967295 (0xffffffff).	0	variants.  Select the dead time to apply during down counting. This value only applies to the GPT32E and GPT32EH variants.
----------------------------------------------------------------------------------	----------------------------------------------------------------------------------------------------	---	----------------------------------------------------------------------------------------------------------------------------------

## Clock Configuration

Please refer to the [General PWM Timer \(r\\_gpt\)](#) section for more information.

## Pin Configuration

Please refer to the [General PWM Timer \(r\\_gpt\)](#) section for more information.

## Usage Notes

### Warning

Be sure the GTIOCA/B stop level and dead time values are set appropriately for your application before attempting to drive a motor. Failure to do so may result in damage to the motor drive circuitry and/or the motor itself if the timer is stopped by software.

## Initial Setup

The following should be configured once the GPT Three-Phase module has been added to a project:

1. Set "Pin Output Support" in one of the GPT submodules to "Enabled with Extra Features"
2. Configure common settings in the GPT Three-Phase module properties
3. Set the crest and trough interrupt priority and callback function in **one** of the three GPT submodules (if desired)
4. Set the "Extra Features -> Output Disable" settings in each GPT submodule as needed for your application

### Note

*Because all three modules are operated synchronously with the same period interrupts only need to be enabled in one of the three GPT modules.*

## Buffer Modes

There are two buffering modes available for duty cycle values - single- and double-buffered. In single buffer mode only the values specified in the duty array element of [three\\_phase\\_duty\\_cycle\\_t](#) are used by [R\\_GPT\\_THREE\\_PHASE\\_DutyCycleSet](#). At the next trough or crest event the output duty cycle will be internally updated to the set values.

In double buffer mode the `duty_buffer` array values are used as buffer values for the duty elements. Once passed to [R\\_GPT\\_THREE\\_PHASE\\_DutyCycleSet](#), the next trough or crest event will update the output duty cycle to the values specified in `duty` as before. However, at the following crest or trough event the output duty cycle will be updated to the values in `duty_buffer`. This allows the duty cycle for both sides of an asymmetric PWM waveform to be set at only one trough or crest event per period instead of at every event.

## Examples

## GPT Three-Phase Basic Example

This is a basic example of minimal use of the GPT Three-Phase module in an application. The duty cycle is updated at every timer trough with the previously loaded buffer value, then the duty cycle buffer is reloaded in the trough interrupt callback.

```
void gpt_callback (timer_callback_args_t * p_args)
{
    fsp_err_t          err;
    three_phase_duty_cycle_t duty_cycle;
    if (TIMER_EVENT_TROUGH == p_args->event)
    {
        /* Update duty cycle values (example) */
        duty_cycle.duty[THREE_PHASE_CHANNEL_U] =
get_duty_counts(THREE_PHASE_CHANNEL_U);
        duty_cycle.duty[THREE_PHASE_CHANNEL_V] =
get_duty_counts(THREE_PHASE_CHANNEL_V);
        duty_cycle.duty[THREE_PHASE_CHANNEL_W] =
get_duty_counts(THREE_PHASE_CHANNEL_W);
        /* Update duty cycle values */
        err = R_GPT_THREE_PHASE_DutyCycleSet(&g_gpt_three_phase_ctrl, &duty_cycle);
        handle_error(err);
    }
    else
    {
        /* Handle crest event. */
    }
}

void gpt_three_phase_basic_example (void)
{
    fsp_err_t err = FSP_SUCCESS;
    /* Initializes the module. */
    err = R_GPT_THREE_PHASE_Open(&g_gpt_three_phase_ctrl, &g_gpt_three_phase_cfg);
    /* Handle any errors. This function should be defined by the user. */
    handle_error(err);
    /* Start the timer. */
}
```



```
(void) R_GPT_THREE_PHASE_Start(&g_gpt_three_phase_ctrl);
}
```

## Data Structures

```
struct gpt_three_phase_instance_ctrl_t
```

## Data Structure Documentation

### ◆ gpt\_three\_phase\_instance\_ctrl\_t

```
struct gpt_three_phase_instance_ctrl_t
```

Channel control block. DO NOT INITIALIZE. Initialization occurs when `three_phase_api_t::open` is called.

## Function Documentation

### ◆ R\_GPT\_THREE\_PHASE\_Open()

```
fsp_err_t R_GPT_THREE_PHASE_Open ( three_phase_ctrl_t *const p_ctrl, three_phase_cfg_t const *const p_cfg )
```

Initializes the 3-phase timer module (and associated timers) and applies configurations. Implements `three_phase_api_t::open`.

Example:

```
/* Initializes the module. */
err = R_GPT_THREE_PHASE_Open(&g_gpt_three_phase_ctrl, &g_gpt_three_phase_cfg);
```

### Return values

FSP_SUCCESS	Initialization was successful.
FSP_ERR_ASSERTION	A required input pointer is NULL.
FSP_ERR_ALREADY_OPEN	Module is already open.

◆ **R\_GPT\_THREE\_PHASE\_Stop()**

```
fsp_err_t R_GPT_THREE_PHASE_Stop ( three_phase_ctrl_t *const p_ctrl)
```

Stops all timers synchronously. Implements `three_phase_api_t::stop`.

**Return values**

FSP_SUCCESS	Timers successfully stopped.
FSP_ERR_ASSERTION	p_ctrl was NULL.
FSP_ERR_NOT_OPEN	The instance is not opened.

◆ **R\_GPT\_THREE\_PHASE\_Start()**

```
fsp_err_t R_GPT_THREE_PHASE_Start ( three_phase_ctrl_t *const p_ctrl)
```

Starts all timers synchronously. Implements `three_phase_api_t::start`.

Example:

```
/* Start the timer. */
(void) R_GPT_THREE_PHASE_Start(&g_gpt_three_phase_ctrl);
```

**Return values**

FSP_SUCCESS	Timers successfully started.
FSP_ERR_ASSERTION	p_ctrl was NULL.
FSP_ERR_NOT_OPEN	The instance is not opened.

◆ **R\_GPT\_THREE\_PHASE\_Reset()**

```
fsp_err_t R_GPT_THREE_PHASE_Reset ( three_phase_ctrl_t *const p_ctrl)
```

Resets the counter values to 0. Implements `three_phase_api_t::reset`.

**Return values**

FSP_SUCCESS	Counters were reset successfully.
FSP_ERR_ASSERTION	p_ctrl was NULL.
FSP_ERR_NOT_OPEN	The instance is not opened.

### ◆ R\_GPT\_THREE\_PHASE\_DutyCycleSet()

```
fsp_err_t R_GPT_THREE_PHASE_DutyCycleSet ( three_phase_ctrl_t *const p_ctrl,
three_phase_duty_cycle_t *const p_duty_cycle )
```

Sets duty cycle for all three timers. Implements `three_phase_api_t::dutyCycleSet`.

In symmetric PWM mode duty cycle values are reflected after the next trough. In asymmetric PWM mode values are reflected at the next trough OR crest, whichever comes first.

When double-buffering is enabled the values in `three_phase_duty_cycle_t::duty_buffer` are set to the double-buffer registers. When values are reflected the first time the single buffer values (`three_phase_duty_cycle_t::duty`) are used. On the second reflection the `duty_buffer` values are used. In asymmetric PWM mode this enables both count-up and count-down PWM values to be set at trough (or crest) exclusively.

#### Note

*It is recommended to call this function in a high-priority callback to ensure that it is not interrupted and that no GPT events occur during setting that would result in a duty cycle buffer load operation.*

#### Example:

```
/* Update duty cycle values */
err = R_GPT_THREE_PHASE_DutyCycleSet(&g_gpt_three_phase_ctrl, &duty_cycle);
handle_error(err);
```

#### Return values

FSP_SUCCESS	Duty cycle updated successfully.
FSP_ERR_ASSERTION	p_ctrl was NULL
FSP_ERR_NOT_OPEN	The instance is not opened.
FSP_ERR_INVALID_ARGUMENT	One or more duty cycle count values was outside the range 0..(period - 1).

### ◆ R\_GPT\_THREE\_PHASE\_CallbackSet()

```
fsp_err_t R_GPT_THREE_PHASE_CallbackSet ( three_phase_ctrl_t *const p_ctrl,
void(*) (timer_callback_args_t *) p_callback, void const *const p_context, timer_callback_args_t
*const p_callback_memory )
```

Updates the user callback for the GPT U-channel with the option to provide memory for the callback argument structure. Implements `three_phase_api_t::callbackSet`.

#### Return values

FSP_SUCCESS	Callback updated successfully.
FSP_ERR_ASSERTION	A required pointer is NULL.
FSP_ERR_NOT_OPEN	The control block has not been opened.

◆ **R\_GPT\_THREE\_PHASE\_Close()**

```
fsp_err_t R_GPT_THREE_PHASE_Close ( three_phase_ctrl_t *const p_ctrl)
```

Stops counters, disables output pins, and clears internal driver data. Implements `three_phase_api_t::close`.

**Return values**

FSP_SUCCESS	Successful close.
FSP_ERR_ASSERTION	p_ctrl was NULL.
FSP_ERR_NOT_OPEN	The instance is not opened.

◆ **R\_GPT\_THREE\_PHASE\_VersionGet()**

```
fsp_err_t R_GPT_THREE_PHASE_VersionGet ( fsp_version_t *const p_version)
```

Sets driver version based on compile time macros. Implements `three_phase_api_t::versionGet`.

**Return values**

FSP_SUCCESS	Version stored in p_version.
FSP_ERR_ASSERTION	p_version was NULL.

**4.2.25 Interrupt Controller Unit (r\_icu)**

## Modules

**Functions**

```
fsp_err_t R_ICU_ExternalIrqOpen (external_irq_ctrl_t *const p_api_ctrl,
external_irq_cfg_t const *const p_cfg)
```

```
fsp_err_t R_ICU_ExternalIrqEnable (external_irq_ctrl_t *const p_api_ctrl)
```

```
fsp_err_t R_ICU_ExternalIrqDisable (external_irq_ctrl_t *const p_api_ctrl)
```

```
fsp_err_t R_ICU_ExternalIrqVersionGet (fsp_version_t *const p_version)
```

```
fsp_err_t R_ICU_ExternalIrqCallbackSet (external_irq_ctrl_t *const p_api_ctrl,
void(*p_callback)(external_irq_callback_args_t *), void const *const
p_context, external_irq_callback_args_t *const p_callback_memory)
```

```
fsp_err_t R_ICU_ExternalIrqClose (external_irq_ctrl_t *const p_api_ctrl)
```

## Detailed Description

Driver for the ICU peripheral on RA MCUs. This module implements the [External IRQ Interface](#).

## Overview

The Interrupt Controller Unit (ICU) controls which event signals are linked to the NVIC, DTC, and DMAC modules. The R\_ICU software module only implements the [External IRQ Interface](#). The external\_irq interface is for configuring interrupts to fire when a trigger condition is detected on an external IRQ pin.

### Note

*Multiple instances are used when more than one external interrupt is needed. Configure each instance with different channels and properties as needed for the specific interrupt.*

## Features

- Supports configuring interrupts for IRQ pins on the target MCUs
  - Enabling and disabling interrupt generation.
  - Configuring interrupt trigger on rising edge, falling edge, both edges, or low level signal.
  - Enabling and disabling the IRQ noise filter.
- Supports configuring a user callback function, which will be invoked by the HAL module when an external pin interrupt is generated.

## Configuration

### Build Time Configurations for r\_icu

The following build time configurations are defined in fsp\_cfg/r\_icu\_cfg.h:

Configuration	Options	Default	Description
Parameter Checking	<ul style="list-style-type: none"> <li>• Default (BSP)</li> <li>• Enabled</li> <li>• Disabled</li> </ul>	Default (BSP)	If selected code for parameter checking is included in the build.

### Configurations for Driver > Input > External IRQ Driver on r\_icu

This module can be added to the Stacks tab via New Stack > Driver > Input > External IRQ Driver on r\_icu. Non-secure callable guard functions can be generated for this module by right clicking the module in the RA Configuration tool and checking the "Non-secure Callable" box.

Configuration	Options	Default	Description
Name	Name must be a valid C symbol	g_external_irq0	Module name.
Channel	Value must be an integer between 0 and 15	0	Specify the hardware channel.

Trigger	<ul style="list-style-type: none"> <li>Falling</li> <li>Rising</li> <li>Both Edges</li> <li>Low Level</li> </ul>	Rising	Select the signal edge or state that triggers an interrupt.
Digital Filtering	<ul style="list-style-type: none"> <li>Enabled</li> <li>Disabled</li> </ul>	Disabled	Select if the digital noise filter should be enabled.
Digital Filtering Sample Clock (Only valid when Digital Filtering is Enabled)	<ul style="list-style-type: none"> <li>PCLK / 1</li> <li>PCLK / 8</li> <li>PCLK / 32</li> <li>PCLK / 64</li> </ul>	PCLK / 64	Select the clock divider for the digital noise filter.
Callback	Name must be a valid C symbol	NULL	A user callback function can be provided here. If this callback function is provided, it is called from the interrupt service routine (ISR) each time the IRQn triggers
Pin Interrupt Priority	MCU Specific Options		Select the PIN interrupt priority.

## Clock Configuration

The ICU peripheral module doesn't require any specific clock settings.

*Note*

*The digital filter uses PCLKB as the clock source for sampling the IRQ pin.*

## Pin Configuration

The pin for the external interrupt channel must be configured as an input with IRQ Input Enabled.

## Usage Notes

### Digital Filter

The digital filter is used to reject trigger conditions that are too short. The trigger condition must be longer than three periods of the filter clock. The filter clock frequency is determined by PCLKB and the `external_irq_pclk_div_t` setting.

$$\text{MIN\_PULSE\_WIDTH} = \text{EXTERNAL\_IRQ\_PCLKB\_DIV} / \text{PCLKB\_FREQUENCY} * 3$$

### DMAC/DTC

When using an External IRQ pin to trigger a DMAC/DTC transfer, the External IRQ pin must be opened before the transfer instance is opened.

## Examples

## Basic Example

This is a basic example of minimal use of the ICU in an application.

```
#define ICU_IRQN_PIN BSP_IO_PORT_02_PIN_06
#define ICU_IRQN 6
/* Called from icu_irq_isr */
void external_irq_callback (external_irq_callback_args_t * p_args)
{
    (void) p_args;
    g_external_irq_complete = 1;
}
void simple_example ()
{
    /* Example Configuration */
    external_irq_cfg_t icu_cfg =
    {
        .channel      = ICU_IRQN,
        .trigger      = EXTERNAL_IRQ_TRIG_RISING,
        .filter_enable = false,
        .pclk_div     = EXTERNAL_IRQ_PCLK_DIV_BY_1,
        .p_callback   = external_irq_callback,
        .p_context    = 0,
        .ipl          = 0,
        .irq          = (IRQn_Type) 0,
    };
    /* Configure the external interrupt. */
    fsp_err_t err = R_ICU_ExternalIrqOpen(&g_icu_ctrl, &icu_cfg);
    handle_error(err);
    /* Enable the external interrupt. */
    /* Enable not required when used with ELC or DMAC. */
    err = R_ICU_ExternalIrqEnable(&g_icu_ctrl);
    handle_error(err);
    while (0 == g_external_irq_complete)
    {
        /* Wait for interrupt. */
    }
}
```

```

}
}

```

## Data Structures

struct [icu\\_instance\\_ctrl\\_t](#)

## Data Structure Documentation

### ◆ icu\_instance\_ctrl\_t

struct [icu\\_instance\\_ctrl\\_t](#)

ICU private control block. DO NOT MODIFY. Initialization occurs when [R\\_ICU\\_ExtrenalIrqOpen](#) is called.

#### Data Fields

uint32_t	<a href="#">open</a>
	Used to determine if channel control block is in use.
IRQn_Type	<a href="#">irq</a>
	NVIC interrupt number.
uint8_t	<a href="#">channel</a>
	Channel.
void const *	<a href="#">p_context</a>

## Field Documentation

### ◆ p\_context

void const\* [icu\\_instance\\_ctrl\\_t::p\\_context](#)

Placeholder for user data. Passed to the user callback in [external\\_irq\\_callback\\_args\\_t](#).

## Function Documentation



◆ **R\_ICU\_ExternalIrqOpen()**

```
fsp_err_t R_ICU_ExternalIrqOpen ( external_irq_ctrl_t *const p_api_ctrl, external_irq_cfg_t const
*const p_cfg )
```

Configure an IRQ input pin for use with the external interrupt interface. Implements [external\\_irq\\_api\\_t::open](#).

The Open function is responsible for preparing an external IRQ pin for operation.

**Return values**

FSP_SUCCESS	Open successful.
FSP_ERR_ASSERTION	One of the following is invalid: <ul style="list-style-type: none"> <li>• p_ctrl or p_cfg is NULL</li> </ul>
FSP_ERR_ALREADY_OPEN	The channel specified has already been opened. No configurations were changed. Call the associated Close function to reconfigure the channel.
FSP_ERR_IP_CHANNEL_NOT_PRESENT	The channel requested in p_cfg is not available on the device selected in r_bsp_cfg.h.
FSP_ERR_INVALID_ARGUMENT	p_cfg->p_callback is not NULL, but ISR is not enabled. ISR must be enabled to use callback function.

**Note**

*This function is reentrant for different channels. It is not reentrant for the same channel.*

◆ **R\_ICU\_ExternalIrqEnable()**

```
fsp_err_t R_ICU_ExternalIrqEnable ( external_irq_ctrl_t *const p_api_ctrl)
```

Enable external interrupt for specified channel at NVIC. Implements [external\\_irq\\_api\\_t::enable](#).

**Return values**

FSP_SUCCESS	Interrupt Enabled successfully.
FSP_ERR_ASSERTION	The p_ctrl parameter was null.
FSP_ERR_NOT_OPEN	The channel is not opened.
FSP_ERR_IRQ_BSP_DISABLED	Requested IRQ is not defined in this system

◆ **R\_ICU\_ExternalIrqDisable()**

```
fsp_err_t R_ICU_ExternalIrqDisable ( external_irq_ctrl_t *const p_api_ctrl)
```

Disable external interrupt for specified channel at NVIC. Implements `external_irq_api_t::disable`.

**Return values**

FSP_SUCCESS	Interrupt disabled successfully.
FSP_ERR_ASSERTION	The p_ctrl parameter was null.
FSP_ERR_NOT_OPEN	The channel is not opened.
FSP_ERR_IRQ_BSP_DISABLED	Requested IRQ is not defined in this system

◆ **R\_ICU\_ExternalIrqVersionGet()**

```
fsp_err_t R_ICU_ExternalIrqVersionGet ( fsp_version_t *const p_version)
```

Set driver version based on compile time macros. Implements `external_irq_api_t::versionGet`.

**Return values**

FSP_SUCCESS	Successful close.
FSP_ERR_ASSERTION	The parameter p_version is NULL.

◆ **R\_ICU\_ExternalIrqCallbackSet()**

```
fsp_err_t R_ICU_ExternalIrqCallbackSet ( external_irq_ctrl_t *const p_api_ctrl,
void(*) (external_irq_callback_args_t *) p_callback, void const *const p_context,
external_irq_callback_args_t *const p_callback_memory )
```

Updates the user callback and has option of providing memory for callback structure. Implements `external_irq_api_t::callbackSet`

**Return values**

FSP_SUCCESS	Callback updated successfully.
FSP_ERR_ASSERTION	A required pointer is NULL.
FSP_ERR_NOT_OPEN	The control block has not been opened.

### ◆ R\_ICU\_ExternalIrqClose()

`fsp_err_t R_ICU_ExternalIrqClose ( external_irq_ctrl_t *const p_api_ctrl)`

Close the external interrupt channel. Implements `external_irq_api_t::close`.

#### Return values

FSP_SUCCESS	Successfully closed.
FSP_ERR_ASSERTION	The parameter <code>p_ctrl</code> is NULL.
FSP_ERR_NOT_OPEN	The channel is not opened.

## 4.2.26 I2C Master on IIC (r\_iic\_master)

### Modules

#### Functions

`fsp_err_t R_IIC_MASTER_Open (i2c_master_ctrl_t *const p_api_ctrl, i2c_master_cfg_t const *const p_cfg)`

`fsp_err_t R_IIC_MASTER_Read (i2c_master_ctrl_t *const p_api_ctrl, uint8_t *const p_dest, uint32_t const bytes, bool const restart)`

`fsp_err_t R_IIC_MASTER_Write (i2c_master_ctrl_t *const p_api_ctrl, uint8_t *const p_src, uint32_t const bytes, bool const restart)`

`fsp_err_t R_IIC_MASTER_Abort (i2c_master_ctrl_t *const p_api_ctrl)`

`fsp_err_t R_IIC_MASTER_SlaveAddressSet (i2c_master_ctrl_t *const p_api_ctrl, uint32_t const slave, i2c_master_addr_mode_t const addr_mode)`

`fsp_err_t R_IIC_MASTER_Close (i2c_master_ctrl_t *const p_api_ctrl)`

`fsp_err_t R_IIC_MASTER_VersionGet (fsp_version_t *const p_version)`

`fsp_err_t R_IIC_MASTER_CallbackSet (i2c_master_ctrl_t *const p_api_ctrl, void(*p_callback)(i2c_master_callback_args_t *), void const *const p_context, i2c_master_callback_args_t *const p_callback_memory)`

#### Detailed Description

Driver for the IIC peripheral on RA MCUs. This module implements the [I2C Master Interface](#).

## Overview

The I2C master on IIC HAL module supports transactions with an I2C Slave device. Callbacks must be provided which are invoked when a transmit or receive operation has completed. The callback argument will contain information about the transaction status, bytes transferred and a pointer to the user defined context.

### Features

- Supports multiple transmission rates
  - Standard Mode Support with up to 100-kHz transaction rate.
  - Fast Mode Support with up to 400-kHz transaction rate.
  - Fast Mode Plus Support with up to 1-MHz transaction rate.
- I2C Master Read from a slave device.
- I2C Master Write to a slave device.
- Abort any in-progress transactions.
- Set the address of the slave device.
- Non-blocking behavior is achieved by the use of callbacks.
- Additional build-time features
  - Optional (build time) DTC support for read and write respectively.
  - Optional (build time) support for 10-bit slave addressing.

## Configuration

### Build Time Configurations for r\_iic\_master

The following build time configurations are defined in fsp\_cfg/r\_iic\_master\_cfg.h:

Configuration	Options	Default	Description
Parameter Checking	<ul style="list-style-type: none"> <li>• Default (BSP)</li> <li>• Enabled</li> <li>• Disabled</li> </ul>	Default (BSP)	If selected code for parameter checking is included in the build.
DTC on Transmission and Reception	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Disabled	If enabled, DTC instances will be included in the build for both transmission and reception.
10-bit slave addressing	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Disabled	If enabled, the driver will support 10-bit slave addressing mode along with the default 7-bit slave addressing mode.

### Configurations for Driver > Connectivity > I2C Master Driver on r\_iic\_master

This module can be added to the Stacks tab via New Stack > Driver > Connectivity > I2C Master Driver on r\_iic\_master. Non-secure callable guard functions can be generated for this module by right clicking the module in the RA Configuration tool and checking the "Non-secure Callable" box.

Configuration	Options	Default	Description
---------------	---------	---------	-------------

Name	Name must be a valid C symbol	g_i2c_master0	Module name.
Channel	Value must be a non-negative integer	0	Specify the IIC channel.
Rate	<ul style="list-style-type: none"> <li>Standard</li> <li>Fast-mode</li> <li>Fast-mode plus</li> </ul>	Standard	Select the transfer rate.
Rise Time (ns)	Value must be a non-negative integer	120	Set the rise time (tr) in nanoseconds.
Fall Time (ns)	Value must be a non-negative integer	120	Set the fall time (tf) in nanoseconds.
Duty Cycle (%)	Value must be an integer between 0 and 100	50	Set the SCL duty cycle.
Slave Address	Value must be non-negative	0x00	Specify the slave address.
Address Mode	<ul style="list-style-type: none"> <li>7-Bit</li> <li>10-Bit</li> </ul>	7-Bit	Select the slave address mode. Ensure 10-bit slave addressing is enabled in the configuration to use 10-Bit setting here.
Timeout Mode	<ul style="list-style-type: none"> <li>Short Mode</li> <li>Long Mode</li> </ul>	Short Mode	Select the timeout mode to detect bus hang.
Callback	Name must be a valid C symbol	NULL	A user callback function must be provided. This will be called from the interrupt service routine (ISR) upon IIC transaction completion reporting the transaction status.
Interrupt Priority Level	MCU Specific Options		Select the interrupt priority level. This is set for TXI, RXI, TEI and ERI interrupts.

## Clock Configuration

The IIC peripheral module uses the PCLKB as its clock source. The actual I2C transfer rate will be calculated and set by the tooling depending on the selected transfer rate. If the PCLKB is configured in such a manner that the selected internal rate cannot be achieved, an error will be returned.

## Pin Configuration

The IIC peripheral module uses pins on the MCU to communicate to external devices. I/O pins must be selected and configured as required by the external device. An I2C channel would consist of two

pins - SDA and SCL for data/address and clock respectively.

## Usage Notes

### Interrupt Configuration

- The IIC error (EEI), receive buffer full (RXI), transmit buffer empty (TXI) and transmit end (TEI) interrupts for the selected channel used must be enabled in the properties of the selected device.
- Set equal priority levels for all the interrupts mentioned above. Setting the interrupts to different priority levels could result in improper operation.

### IIC Master Rate Calculation

- The RA Configuration editor calculates the internal baud-rate setting based on the configured transfer rate. The closest possible baud-rate that can be achieved (less than or equal to the requested rate) at the current PCLKB settings is calculated and used.
- If a valid clock rate could not be calculated, an error is returned by the tool.

### Enabling DTC with the IIC

- DTC transfer support is configurable and is disabled from the build by default. IIC driver provides two DTC instances for transmission and reception respectively. The DTC instances can be enabled individually during configuration.
- For further details on DTC please refer [Data Transfer Controller \(r\\_dtc\)](#)

### Multiple Devices on the Bus

- A single IIC instance can be used to communicate with multiple slave devices on the same channel by using the SlaveAddressSet API.

### Multi-Master Support

- If multiple masters are connected on the same bus, the I2C Master is capable of detecting bus busy state before initiating the communication.

### Restart

- IIC master can hold the the bus after an I2C transaction by issuing Restart. This will mimic a stop followed by start condition.

## Examples

### Basic Example

This is a basic example of minimal use of the r\_iic\_master in an application. This example shows how this driver can be used for basic read and write operations.

```
iic_master_instance_ctrl_t g_i2c_device_ctrl_1;  
i2c_master_cfg_t g_i2c_device_cfg_1 =  
{  
    .channel = I2C_CHANNEL,
```

```
.rate          = I2C_MASTER_RATE_FAST,
.slave         = I2C_SLAVE_EEPROM,
.addr_mode    = I2C_MASTER_ADDR_MODE_7BIT,
.p_callback   = i2c_callback,    // Callback
.p_context    = &g_i2c_device_ctrl_1,
.p_transfer_tx = NULL,
.p_transfer_rx = NULL,
.p_extend     = &g_iic_master_cfg_extend
};

void i2c_callback (i2c_master_callback_args_t * p_args)
{
    g_i2c_callback_event = p_args->event;
}

void basic_example (void)
{
    fsp_err_t err;
    uint32_t i;
    uint32_t timeout_ms = I2C_TRANSACTION_BUSY_DELAY;
    /* Initialize the IIC module */
    err = R_IIC_MASTER_Open(&g_i2c_device_ctrl_1, &g_i2c_device_cfg_1);
    /* Handle any errors. This function should be defined by the user. */
    handle_error(err);
    /* Write some data to the transmit buffer */
    for (i = 0; i < I2C_BUFFER_SIZE_BYTES; i++)
    {
        g_i2c_tx_buffer[i] = (uint8_t) i;
    }
    /* Send data to I2C slave */
    g_i2c_callback_event = I2C_MASTER_EVENT_ABORTED;
    err = R_IIC_MASTER_Write(&g_i2c_device_ctrl_1, &g_i2c_tx_buffer[0],
I2C_BUFFER_SIZE_BYTES, false);
    handle_error(err);
    /* Since there is nothing else to do, block until Callback triggers*/
    while ((I2C_MASTER_EVENT_TX_COMPLETE != g_i2c_callback_event) && timeout_ms)
```

```
{
R_BSP_SoftwareDelay(1U, BSP_DELAY_UNITS_MILLISECONDS);
    timeout_ms--;
}
if (I2C_MASTER_EVENT_ABORTED == g_i2c_callback_event)
{
    __BKPT(0);
}
/* Read data back from the I2C slave */
g_i2c_callback_event = I2C_MASTER_EVENT_ABORTED;
timeout_ms          = I2C_TRANSACTION_BUSY_DELAY;
err = R_IIC_MASTER_Read(&g_i2c_device_ctrl_1, &g_i2c_rx_buffer[0],
I2C_BUFFER_SIZE_BYTES, false);
    handle_error(err);
/* Since there is nothing else to do, block until Callback triggers*/
while ((I2C_MASTER_EVENT_RX_COMPLETE != g_i2c_callback_event) && timeout_ms)
{
R_BSP_SoftwareDelay(1U, BSP_DELAY_UNITS_MILLISECONDS);
    timeout_ms--;
}
if (I2C_MASTER_EVENT_ABORTED == g_i2c_callback_event)
{
    __BKPT(0);
}
/* Verify the read data */
if (0U != memcmp(g_i2c_tx_buffer, g_i2c_rx_buffer, I2C_BUFFER_SIZE_BYTES))
{
    __BKPT(0);
}
}
```

### Multiple Slave devices on the same channel (bus)

This example demonstrates how a single IIC driver can be used to communicate with different slave devices which are on the same channel.



*Note*

The callback function from the first example applies to this example as well.

```
iic_master_instance_ctrl_t g_i2c_device_ctrl_2;
i2c_master_cfg_t g_i2c_device_cfg_2 =
{
    .channel          = I2C_CHANNEL,
    .rate             = I2C_MASTER_RATE_STANDARD,
    .slave            = I2C_SLAVE_TEMP_SENSOR,
    .addr_mode        = I2C_MASTER_ADDR_MODE_7BIT,
    .p_callback        = i2c_callback,    // Callback
    .p_context        = &g_i2c_device_ctrl_2,
    .p_transfer_tx    = NULL,
    .p_transfer_rx    = NULL,
    .p_extend         = &g_iic_master_cfg_extend
};

void single_channel_multi_slave (void)
{
    fsp_err_t err;

    uint32_t timeout_ms = I2C_TRANSACTION_BUSY_DELAY;

    err = R_IIC_MASTER_Open(&g_i2c_device_ctrl_2, &g_i2c_device_cfg_2);
    /* Handle any errors. This function should be defined by the user. */
    handle_error(err);

    /* Clear the receive buffer */
    memset(g_i2c_rx_buffer, '0', I2C_BUFFER_SIZE_BYTES);

    /* Read data from I2C slave */
    g_i2c_callback_event = I2C_MASTER_EVENT_ABORTED;

    err = R_IIC_MASTER_Read(&g_i2c_device_ctrl_2, &g_i2c_rx_buffer[0],
I2C_BUFFER_SIZE_BYTES, false);

    handle_error(err);

    while ((I2C_MASTER_EVENT_RX_COMPLETE != g_i2c_callback_event) && timeout_ms)
    {
        R_BSP_SoftwareDelay(1U, BSP_DELAY_UNITS_MILLISECONDS);

        timeout_ms--;
    }
}
```

```
if (I2C_MASTER_EVENT_ABORTED == g_i2c_callback_event)
{
    __BKPT(0);
}

/* Send data to I2C slave on the same channel */
err = R_IIC_MASTER_SlaveAddressSet(&g_i2c_device_ctrl_2,
I2C_SLAVE_DISPLAY_ADAPTER, I2C_MASTER_ADDR_MODE_7BIT);

handle_error(err);

g_i2c_tx_buffer[0] = 0xAA; // NOLINT
g_i2c_tx_buffer[1] = 0xBB; // NOLINT
g_i2c_callback_event = I2C_MASTER_EVENT_ABORTED;
timeout_ms = I2C_TRANSACTION_BUSY_DELAY;

err = R_IIC_MASTER_Write(&g_i2c_device_ctrl_2, &g_i2c_tx_buffer[0], 2U, false);
handle_error(err);

while ((I2C_MASTER_EVENT_TX_COMPLETE != g_i2c_callback_event) && timeout_ms)
{
    R_BSP_SoftwareDelay(1U, BSP_DELAY_UNITS_MILLISECONDS);
    timeout_ms--;
}

if (I2C_MASTER_EVENT_ABORTED == g_i2c_callback_event)
{
    __BKPT(0);
}
}
```

## Data Structures

struct [iic\\_master\\_clock\\_settings\\_t](#)

struct [iic\\_master\\_instance\\_ctrl\\_t](#)

struct [iic\\_master\\_extended\\_cfg\\_t](#)

## Enumerations

enum [iic\\_master\\_timeout\\_mode\\_t](#)

## Data Structure Documentation

### ◆ [iic\\_master\\_clock\\_settings\\_t](#)

struct iic_master_clock_settings_t		
I2C clock settings		
Data Fields		
uint8_t	cks_value	Internal Reference Clock Select.
uint8_t	brh_value	High-level period of SCL clock.
uint8_t	brl_value	Low-level period of SCL clock.

## ◆ iic\_master\_instance\_ctrl\_t

struct iic_master_instance_ctrl_t		
I2C control structure. DO NOT INITIALIZE.		

## ◆ iic\_master\_extended\_cfg\_t

struct iic_master_extended_cfg_t		
R_IIC extended configuration		
Data Fields		
iic_master_timeout_mode_t	timeout_mode	Timeout Detection Time Select: Long Mode = 0 and Short Mode = 1.
iic_master_clock_settings_t	clock_settings	I2C Clock settings.

## Enumeration Type Documentation

## ◆ iic\_master\_timeout\_mode\_t

enum iic_master_timeout_mode_t	
I2C Timeout mode parameter definition	
Enumerator	
IIC_MASTER_TIMEOUT_MODE_LONG	Timeout Detection Time Select: Long Mode -> TMOS = 0.
IIC_MASTER_TIMEOUT_MODE_SHORT	Timeout Detection Time Select: Short Mode -> TMOS = 1.

## Function Documentation

◆ **R\_IIC\_MASTER\_Open()**

```
fsp_err_t R_IIC_MASTER_Open ( i2c_master_ctrl_t *const p_api_ctrl, i2c_master_cfg_t const *const p_cfg )
```

Opens the I2C device.

**Return values**

FSP_SUCCESS	Requested clock rate was set exactly.
FSP_ERR_ALREADY_OPEN	Module is already open.
FSP_ERR_IP_CHANNEL_NOT_PRESENT	Channel is not available on this MCU.
FSP_ERR_ASSERTION	Parameter check failure due to one or more reasons below: <ul style="list-style-type: none"> <li>1. p_api_ctrl or p_cfg is NULL.</li> <li>2. extended parameter is NULL.</li> <li>3. Callback parameter is NULL.</li> <li>4. Set the rate to fast mode plus on a channel which does not support it.</li> <li>5. Invalid IRQ number assigned</li> </ul>

◆ **R\_IIC\_MASTER\_Read()**

```
fsp_err_t R_IIC_MASTER_Read ( i2c_master_ctrl_t *const p_api_ctrl, uint8_t *const p_dest, uint32_t const bytes, bool const restart )
```

Performs a read from the I2C device. The caller will be notified when the operation has completed (successfully) by an I2C\_MASTER\_EVENT\_RX\_COMPLETE in the callback.

**Return values**

FSP_SUCCESS	Function executed without issue.
FSP_ERR_ASSERTION	p_api_ctrl, p_dest or bytes is NULL.
FSP_ERR_INVALID_SIZE	Provided number of bytes more than uint16_t size (65535) while DTC is used for data transfer.
FSP_ERR_IN_USE	Bus busy condition. Another transfer was in progress.
FSP_ERR_NOT_OPEN	Handle is not initialized. Call R_IIC_MASTER_Open to initialize the control block.

◆ **R\_IIC\_MASTER\_Write()**

```
fsp_err_t R_IIC_MASTER_Write ( i2c_master_ctrl_t *const p_api_ctrl, uint8_t *const p_src, uint32_t
const bytes, bool const restart )
```

Performs a write to the I2C device. The caller will be notified when the operation has completed (successfully) by an I2C\_MASTER\_EVENT\_TX\_COMPLETE in the callback.

**Return values**

FSP_SUCCESS	Function executed without issue.
FSP_ERR_ASSERTION	p_api_ctrl or p_src is NULL.
FSP_ERR_INVALID_SIZE	Provided number of bytes more than uint16_t size (65535) while DTC is used for data transfer.
FSP_ERR_IN_USE	Bus busy condition. Another transfer was in progress.
FSP_ERR_NOT_OPEN	Handle is not initialized. Call R_IIC_MASTER_Open to initialize the control block.

◆ **R\_IIC\_MASTER\_Abort()**

```
fsp_err_t R_IIC_MASTER_Abort ( i2c_master_ctrl_t *const p_api_ctrl)
```

Safely aborts any in-progress transfer and forces the IIC peripheral into ready state.

**Return values**

FSP_SUCCESS	Channel was reset successfully.
FSP_ERR_ASSERTION	p_api_ctrl is NULL.
FSP_ERR_NOT_OPEN	Handle is not initialized. Call R_IIC_MASTER_Open to initialize the control block.

**Note**

*A callback will not be invoked in case an in-progress transfer gets aborted by calling this API.*

◆ **R\_IIC\_MASTER\_SlaveAddressSet()**

```
fsp_err_t R_IIC_MASTER_SlaveAddressSet ( i2c_master_ctrl_t *const p_api_ctrl, uint32_t const slave, i2c_master_addr_mode_t const addr_mode )
```

Sets address and addressing mode of the slave device. This function is used to set the device address and addressing mode of the slave without reconfiguring the entire bus.

**Return values**

FSP_SUCCESS	Address of the slave is set correctly.
FSP_ERR_ASSERTION	Pointer to control structure is NULL.
FSP_ERR_IN_USE	Another transfer was in-progress.
FSP_ERR_NOT_OPEN	Handle is not initialized. Call R_IIC_MASTER_Open to initialize the control block.

◆ **R\_IIC\_MASTER\_Close()**

```
fsp_err_t R_IIC_MASTER_Close ( i2c_master_ctrl_t *const p_api_ctrl)
```

Closes the I2C device. May power down IIC peripheral. This function will safely terminate any in-progress I2C transfers.

**Return values**

FSP_SUCCESS	Device closed without issue.
FSP_ERR_ASSERTION	p_api_ctrl is NULL.
FSP_ERR_NOT_OPEN	Handle is not initialized. Call R_IIC_MASTER_Open to initialize the control block.

*Note*

*A callback will not be invoked in case an in-progress transfer gets aborted by calling this API.*

◆ **R\_IIC\_MASTER\_VersionGet()**

```
fsp_err_t R_IIC_MASTER_VersionGet ( fsp_version_t *const p_version)
```

Gets version information and stores it in the provided version structure.

**Return values**

FSP_SUCCESS	Successful version get.
FSP_ERR_ASSERTION	p_version is NULL.

**◆ R\_IIC\_MASTER\_CallbackSet()**

```
fsp_err_t R_IIC_MASTER_CallbackSet ( i2c_master_ctrl_t *const p_api_ctrl,
void(*) (i2c_master_callback_args_t *) p_callback, void const *const p_context,
i2c_master_callback_args_t *const p_callback_memory )
```

Updates the user callback and has option of providing memory for callback structure. Implements `i2c_master_api_t::callbackSet`

**Return values**

FSP_SUCCESS	Callback updated successfully.
FSP_ERR_ASSERTION	A required pointer is NULL.
FSP_ERR_NOT_OPEN	The control block has not been opened.

**4.2.27 I2C Slave on IIC (r\_iic\_slave)**

## Modules

**Functions**

```
fsp_err_t R_IIC_SLAVE_Open (i2c_slave_ctrl_t *const p_api_ctrl, i2c_slave_cfg_t
const *const p_cfg)
```

```
fsp_err_t R_IIC_SLAVE_Read (i2c_slave_ctrl_t *const p_api_ctrl, uint8_t *const
p_dest, uint32_t const bytes)
```

```
fsp_err_t R_IIC_SLAVE_Write (i2c_slave_ctrl_t *const p_api_ctrl, uint8_t *const
p_src, uint32_t const bytes)
```

```
fsp_err_t R_IIC_SLAVE_Close (i2c_slave_ctrl_t *const p_api_ctrl)
```

```
fsp_err_t R_IIC_SLAVE_VersionGet (fsp_version_t *const p_version)
```

```
fsp_err_t R_IIC_SLAVE_CallbackSet (i2c_slave_ctrl_t *const p_api_ctrl,
void(*p_callback)(i2c_slave_callback_args_t *), void const *const
p_context, i2c_slave_callback_args_t *const p_callback_memory)
```

**Detailed Description**

Driver for the IIC peripheral on RA MCUs. This module implements the [I2C Slave Interface](#).

**Overview****Features**

- Supports multiple transmission rates
  - Standard Mode Support with up to 100-kHz transaction rate.
  - Fast Mode Support with up to 400-kHz transaction rate.
  - Fast Mode Plus Support with up to 1-MHz transaction rate.
- Reads data written by master device.
- Write data which is read by master device.
- Can accept 0x00 as slave address.
- Can be assigned a 10-bit address.
- Clock stretching is supported and can be implemented via callbacks.
- Provides Transmission/Reception transaction size in the callback.
- I2C Slave can notify the following events via callbacks: Transmission/Reception Request, Transmission/Reception Request for more data, Transmission/Reception Completion, Error Condition.

## Configuration

### Build Time Configurations for r\_iic\_slave

The following build time configurations are defined in fsp\_cfg/r\_iic\_slave\_cfg.h:

Configuration	Options	Default	Description
Parameter Checking	<ul style="list-style-type: none"> <li>• Default (BSP)</li> <li>• Enabled</li> <li>• Disabled</li> </ul>	Default (BSP)	If selected code for parameter checking is included in the build.

### Configurations for Driver > Connectivity > I2C Slave Driver on r\_iic\_slave

This module can be added to the Stacks tab via New Stack > Driver > Connectivity > I2C Slave Driver on r\_iic\_slave. Non-secure callable guard functions can be generated for this module by right clicking the module in the RA Configuration tool and checking the "Non-secure Callable" box.

Configuration	Options	Default	Description
Name	Name must be a valid C symbol	g_i2c_slave0	Module name.
Channel	Value must be a non-negative integer	0	Specify the IIC channel.
Rate	<ul style="list-style-type: none"> <li>• Standard</li> <li>• Fast-mode</li> <li>• Fast-mode plus</li> </ul>	Standard	Select the transfer rate.
Internal Reference Clock	<ul style="list-style-type: none"> <li>• PCLKB / 1</li> <li>• PCLKB / 2</li> <li>• PCLKB / 4</li> <li>• PCLKB / 8</li> <li>• PCLKB / 16</li> <li>• PCLKB / 32</li> <li>• PCLKB / 64</li> <li>• PCLKB / 128</li> </ul>	PCLKB / 1	Select the internal reference clock for IIC slave. The internal reference clock is used only to determine the clock frequency of the noise filter samples.
Digital Noise Filter Stage Select	<ul style="list-style-type: none"> <li>• Disabled</li> <li>• Single-stage filter</li> </ul>	3-stage filter	Select the number of digital filter stages for IIC Slave.



		<ul style="list-style-type: none"> <li>• 2-stage filter</li> <li>• 3-stage filter</li> <li>• 4-stage filter</li> </ul>		
Slave Address	Value must be non-negative		0x00	Specify the slave address.
General Call	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>		Disabled	Allows the slave to respond to general call address: 0x00.
Address Mode	<ul style="list-style-type: none"> <li>• 7-Bit</li> <li>• 10-Bit</li> </ul>		7-Bit	Select the slave address mode.
Callback	Name must be a valid C symbol		NULL	A user callback function must be provided. This will be called from the interrupt service routine (ISR) to report I2C Slave transaction events and status.
Interrupt Priority Level	MCU Specific Options			Select the interrupt priority level. This is set for TXI, RXI, TEI and ERI interrupts.

## Clock Configuration

The IIC peripheral module uses the PCLKB as its clock source. The actual I2C transfer rate will be calculated and set by the tooling depending on the selected transfer rate. If the PCLKB is configured in such a manner that the selected transfer rate cannot be achieved, an error will be returned.

## Pin Configuration

The IIC peripheral module uses pins on the MCU to communicate to external devices. I/O pins must be selected and configured as required by the external device. An I2C channel would consist of two pins - SDA and SCL for data/address and clock respectively.

# Usage Notes

## Interrupt Configuration

- The IIC error (EEI), receive buffer full (RXI), transmit buffer empty (TXI) and transmit end (TEI) interrupts for the selected channel must be enabled in the properties of the selected device.

## Callback

- A callback function must be provided which will be invoked for the cases below:
  - An I2C Master initiates a transmission or reception: I2C\_SLAVE\_EVENT\_TX\_REQUEST; I2C\_SLAVE\_EVENT\_RX\_REQUEST
  - A Transmission or reception has been completed: I2C\_SLAVE\_EVENT\_TX\_COMPLETE; I2C\_SLAVE\_EVENT\_RX\_COMPLETE
  - An I2C Master is requesting to read or write more data:

- I2C\_SLAVE\_EVENT\_TX\_MORE\_REQUEST; I2C\_SLAVE\_EVENT\_RX\_MORE\_REQUEST
- Error conditions: I2C\_SLAVE\_EVENT\_ABORTED
- An I2C Master initiates a general call by passing 0x00 as slave address: I2C\_SLAVE\_EVENT\_GENERAL\_CALL
- The callback arguments will contain information about the transaction status/events, bytes transferred and a pointer to the user defined context.
- Clock stretching is enabled by the use of callbacks. This means that the IIC slave can hold the clock line SCL LOW to force the I2C Master into a wait state.
- The table below shows I2C Slave event handling expected in user code:

IIC Slave Callback Event	IIC Slave API expected to be called
I2C_SLAVE_EVENT_ABORTED	Handle event based on application
I2C_SLAVE_EVENT_RX_COMPLETE	Handle event based on application
I2C_SLAVE_EVENT_TX_COMPLETE	Handle event based on application
I2C_SLAVE_EVENT_RX_REQUEST	R_IIC_SLAVE_Read API. If the slave is a Write Only device call this API with 0 bytes to send a NACK to the master.
I2C_SLAVE_EVENT_TX_REQUEST	R_IIC_SLAVE_Write API
I2C_SLAVE_EVENT_RX_MORE_REQUEST	R_IIC_SLAVE_Read API. If the slave cannot read any more data call this API with 0 bytes to send a NACK to the master.
I2C_SLAVE_EVENT_TX_MORE_REQUEST	R_IIC_SLAVE_Write API
I2C_SLAVE_EVENT_GENERAL_CALL	R_IIC_SLAVE_Read

- If parameter checking is enabled and R\_IIC\_SLAVE\_Read API is not called for I2C\_SLAVE\_EVENT\_RX\_REQUEST and/or I2C\_SLAVE\_EVENT\_RX\_MORE\_REQUEST, the slave will send a NACK to the master and would eventually timeout.
- R\_IIC\_SLAVE\_Write API is not called for I2C\_SLAVE\_EVENT\_TX\_REQUEST and/or I2C\_SLAVE\_EVENT\_TX\_MORE\_REQUEST:
  - Slave timeout is less than Master timeout: The slave will timeout and release the bus causing the master to read 0xFF for every remaining byte.
  - Slave timeout is more than Master timeout: The master will timeout first followed by the slave.

## IIC Slave Rate Calculation

- The RA Configuration editor calculates the internal baud-rate setting based on the configured transfer rate. The closest possible baud-rate that can be achieved (less than or equal to the requested rate) at the current PCLKB settings is calculated and used.

## Examples

### Basic Example

This is a basic example of minimal use of the R\_IIC\_SLAVE in an application. This example shows how this driver can be used for basic read and write operations.

```
iic_master_instance_ctrl_t g_i2c_master_ctrl;
i2c_master_cfg_t g_i2c_master_cfg =
{
    .channel      = I2C_MASTER_CHANNEL_2,
    .rate        = I2C_MASTER_RATE_STANDARD,
    .slave       = I2C_7BIT_ADDR_IIC_SLAVE,
    .addr_mode   = I2C_MASTER_ADDR_MODE_7BIT,
    .p_callback  = i2c_master_callback, // Callback
    .p_context   = &g_i2c_master_ctrl,
    .p_transfer_tx = NULL,
    .p_transfer_rx = NULL,
    .p_extend    = &g_iic_master_cfg_extend_standard_mode
};
iic_slave_instance_ctrl_t g_i2c_slave_ctrl;
i2c_slave_cfg_t g_i2c_slave_cfg =
{
    .channel      = I2C_SLAVE_CHANNEL_0,
    .rate        = I2C_SLAVE_RATE_STANDARD,
    .slave       = I2C_7BIT_ADDR_IIC_SLAVE,
    .addr_mode   = I2C_SLAVE_ADDR_MODE_7BIT,
    .p_callback  = i2c_slave_callback, // Callback
    .p_context   = &g_i2c_slave_ctrl,
    .p_extend    = &g_iic_slave_cfg_extend_standard_mode
};
void i2c_master_callback (i2c_master_callback_args_t * p_args)
{
    g_i2c_master_callback_event = p_args->event;
}
void i2c_slave_callback (i2c_slave_callback_args_t * p_args)
{
    g_i2c_slave_callback_event = p_args->event;
    if ((p_args->event == I2C_SLAVE_EVENT_RX_COMPLETE) || (p_args->event ==
I2C_SLAVE_EVENT_TX_COMPLETE))
    {
```

```
/* Transaction Successful */
}

else if ((p_args->event == I2C_SLAVE_EVENT_RX_REQUEST) || (p_args->event ==
I2C_SLAVE_EVENT_RX_MORE_REQUEST))
{
/* Read from Master */
err = R_IIC_SLAVE_Read(&g_i2c_slave_ctrl, g_i2c_slave_buffer,
g_slave_transfer_length);
handle_error(err);
}

else if ((p_args->event == I2C_SLAVE_EVENT_TX_REQUEST) || (p_args->event ==
I2C_SLAVE_EVENT_TX_MORE_REQUEST))
{
/* Write to master */
err = R_IIC_SLAVE_Write(&g_i2c_slave_ctrl, g_i2c_slave_buffer,
g_slave_transfer_length);
handle_error(err);
}
else
{
/* Error Event - reported through g_i2c_slave_callback_event */
}
}

void basic_example (void)
{
uint32_t i;
uint32_t timeout_ms = I2C_TRANSACTION_BUSY_DELAY;
g_slave_transfer_length = I2C_BUFFER_SIZE_BYTES;

/* Pin connections:
* Channel 0 SDA <--> Channel 2 SDA
* Channel 0 SCL <--> Channel 2 SCL
*/

/* Initialize the IIC Slave module */
err = R_IIC_SLAVE_Open(&g_i2c_slave_ctrl, &g_i2c_slave_cfg);
```

```
/* Handle any errors. This function should be defined by the user. */
    handle_error(err);

/* Initialize the IIC Master module */
    err = R_IIC_MASTER_Open(&g_i2c_master_ctrl, &g_i2c_master_cfg);
    handle_error(err);

/* Write some data to the transmit buffer */
for (i = 0; i < I2C_BUFFER_SIZE_BYTES; i++)
    {
        g_i2c_master_tx_buffer[i] = (uint8_t) i;
    }

/* Send data to I2C slave */
    g_i2c_master_callback_event = I2C_MASTER_EVENT_ABORTED;
    g_i2c_slave_callback_event = I2C_SLAVE_EVENT_ABORTED;
    err = R_IIC_MASTER_Write(&g_i2c_master_ctrl, &g_i2c_master_tx_buffer[0],
I2C_BUFFER_SIZE_BYTES, false);
    handle_error(err);

/* Since there is nothing else to do, block until Callback triggers
 * The Slave Callback will call the R_IIC_SLAVE_Read API to service the Master Write
Request.
 */
while ((I2C_MASTER_EVENT_TX_COMPLETE != g_i2c_master_callback_event ||
I2C_SLAVE_EVENT_RX_COMPLETE != g_i2c_slave_callback_event) && timeout_ms)
    {
        R_BSP_SoftwareDelay(1U, BSP_DELAY_UNITS_MILLISECONDS);
        timeout_ms--;
    }
if ((I2C_MASTER_EVENT_ABORTED == g_i2c_master_callback_event) ||
    (I2C_SLAVE_EVENT_ABORTED == g_i2c_slave_callback_event))
    {
        __BKPT(0);
    }

/* Read data back from the I2C slave */
    g_i2c_master_callback_event = I2C_MASTER_EVENT_ABORTED;
    g_i2c_slave_callback_event = I2C_SLAVE_EVENT_ABORTED;
```

```

    timeout_ms = I2C_TRANSACTION_BUSY_DELAY;

    err = R_IIC_MASTER_Read(&g_i2c_master_ctrl, &g_i2c_master_rx_buffer[0],
I2C_BUFFER_SIZE_BYTES, false);

    handle_error(err);

    /* Since there is nothing else to do, block until Callback triggers
    * The Slave Callback will call the R_IIC_SLAVE_Write API to service the Master Read
Request.
    */

    while ((I2C_MASTER_EVENT_RX_COMPLETE != g_i2c_master_callback_event ||
I2C_SLAVE_EVENT_TX_COMPLETE != g_i2c_slave_callback_event) && timeout_ms)
    {
R_BSP_SoftwareDelay(1U, BSP_DELAY_UNITS_MILLISECONDS);

        timeout_ms--;
    }

    if ((I2C_MASTER_EVENT_ABORTED == g_i2c_master_callback_event) ||
        (I2C_SLAVE_EVENT_ABORTED == g_i2c_slave_callback_event))
    {
        __BKPT(0);
    }

    /* Verify the read data */
    if (0U != memcmp(g_i2c_master_tx_buffer, g_i2c_master_rx_buffer,
I2C_BUFFER_SIZE_BYTES))
    {
        __BKPT(0);
    }
}

```

## Data Structures

struct [iic\\_slave\\_clock\\_settings\\_t](#)

struct [iic\\_slave\\_extended\\_cfg\\_t](#)

## Data Structure Documentation

### ◆ iic\_slave\_clock\_settings\_t

struct [iic\\_slave\\_clock\\_settings\\_t](#)

I2C clock settings		
Data Fields		
uint8_t	cks_value	Internal Reference Clock Select.
uint8_t	brl_value	Low-level period of SCL clock.
uint8_t	digital_filter_stages	Number of digital filter stages based on brl_value.

#### ◆ iic\_slave\_extended\_cfg\_t

struct iic_slave_extended_cfg_t		
R_IIC_SLAVE extended configuration		
Data Fields		
iic_slave_clock_settings_t	clock_settings	I2C Clock settings.

## Function Documentation

#### ◆ R\_IIC\_SLAVE\_Open()

```
fsp_err_t R_IIC_SLAVE_Open ( i2c_slave_ctrl_t *const p_api_ctrl, i2c_slave_cfg_t const *const p_cfg )
```

Opens the I2C slave device.

#### Return values

FSP_SUCCESS	I2C slave device opened successfully.
FSP_ERR_ALREADY_OPEN	Module is already open.
FSP_ERR_IP_CHANNEL_NOT_PRESENT	Channel is not available on this MCU.
FSP_ERR_ASSERTION	Parameter check failure due to one or more reasons below: <ol style="list-style-type: none"> <li>1. p_api_ctrl or p_cfg is NULL.</li> <li>2. extended parameter is NULL.</li> <li>3. Callback parameter is NULL.</li> <li>4. Set the rate to fast mode plus on a channel which does not support it.</li> <li>5. Invalid IRQ number assigned</li> </ol>

◆ **R\_IIC\_SLAVE\_Read()**

```
fsp_err_t R_IIC_SLAVE_Read ( i2c_slave_ctrl_t *const p_api_ctrl, uint8_t *const p_dest, uint32_t
const bytes )
```

Performs a read from the I2C Master device.

This function will fail if there is already an in-progress I2C transfer on the associated channel. Otherwise, the I2C slave read operation will begin. The caller will be notified when the operation has finished by an I2C\_SLAVE\_EVENT\_RX\_COMPLETE in the callback. In case the master continues to write more data, an I2C\_SLAVE\_EVENT\_RX\_MORE\_REQUEST will be issued via callback. In case of errors, an I2C\_SLAVE\_EVENT\_ABORTED will be issued via callback.

**Return values**

FSP_SUCCESS	Function executed without issue
FSP_ERR_ASSERTION	p_api_ctrl, bytes or p_dest is NULL.
FSP_ERR_IN_USE	Another transfer was in progress.
FSP_ERR_NOT_OPEN	Device is not open.

◆ **R\_IIC\_SLAVE\_Write()**

```
fsp_err_t R_IIC_SLAVE_Write ( i2c_slave_ctrl_t *const p_api_ctrl, uint8_t *const p_src, uint32_t
const bytes )
```

Performs a write to the I2C Master device.

This function will fail if there is already an in-progress I2C transfer on the associated channel. Otherwise, the I2C slave write operation will begin. The caller will be notified when the operation has finished by an I2C\_SLAVE\_EVENT\_TX\_COMPLETE in the callback. In case the master continues to read more data, an I2C\_SLAVE\_EVENT\_TX\_MORE\_REQUEST will be issued via callback. In case of errors, an I2C\_SLAVE\_EVENT\_ABORTED will be issued via callback.

**Return values**

FSP_SUCCESS	Function executed without issue.
FSP_ERR_ASSERTION	p_api_ctrl or p_src is NULL.
FSP_ERR_IN_USE	Another transfer was in progress.
FSP_ERR_NOT_OPEN	Device is not open.



◆ **R\_IIC\_SLAVE\_Close()**

```
fsp_err_t R_IIC_SLAVE_Close ( i2c_slave_ctrl_t *const p_api_ctrl)
```

Closes the I2C device.

**Return values**

FSP_SUCCESS	Device closed successfully.
FSP_ERR_NOT_OPEN	Device not opened.
FSP_ERR_ASSERTION	p_api_ctrl is NULL.

◆ **R\_IIC\_SLAVE\_VersionGet()**

```
fsp_err_t R_IIC_SLAVE_VersionGet ( fsp_version_t *const p_version)
```

Gets version information and stores it in the provided version structure.

**Return values**

FSP_SUCCESS	Successful version get.
FSP_ERR_ASSERTION	p_version is NULL.

◆ **R\_IIC\_SLAVE\_CallbackSet()**

```
fsp_err_t R_IIC_SLAVE_CallbackSet ( i2c_slave_ctrl_t *const p_api_ctrl,
void(*) (i2c_slave_callback_args_t *) p_callback, void const *const p_context,
i2c_slave_callback_args_t *const p_callback_memory )
```

Updates the user callback and has option of providing memory for callback structure. Implements `i2c_slave_api_t::callbackSet`

**Return values**

FSP_SUCCESS	Callback updated successfully.
FSP_ERR_ASSERTION	A required pointer is NULL.
FSP_ERR_NOT_OPEN	The control block has not been opened.

**4.2.28 I/O Ports (r\_ioport)**

Modules

**Functions**

fsp_err_t	R_IOPORT_Open (ioport_ctrl_t *const p_ctrl, const ioport_cfg_t *p_cfg)
fsp_err_t	R_IOPORT_Close (ioport_ctrl_t *const p_ctrl)
fsp_err_t	R_IOPORT_PinsCfg (ioport_ctrl_t *const p_ctrl, const ioport_cfg_t *p_cfg)
fsp_err_t	R_IOPORT_PinCfg (ioport_ctrl_t *const p_ctrl, bsp_io_port_pin_t pin, uint32_t cfg)
fsp_err_t	R_IOPORT_PinEventInputRead (ioport_ctrl_t *const p_ctrl, bsp_io_port_pin_t pin, bsp_io_level_t *p_pin_event)
fsp_err_t	R_IOPORT_PinEventOutputWrite (ioport_ctrl_t *const p_ctrl, bsp_io_port_pin_t pin, bsp_io_level_t pin_value)
fsp_err_t	R_IOPORT_PinRead (ioport_ctrl_t *const p_ctrl, bsp_io_port_pin_t pin, bsp_io_level_t *p_pin_value)
fsp_err_t	R_IOPORT_PinWrite (ioport_ctrl_t *const p_ctrl, bsp_io_port_pin_t pin, bsp_io_level_t level)
fsp_err_t	R_IOPORT_PortDirectionSet (ioport_ctrl_t *const p_ctrl, bsp_io_port_t port, ioport_size_t direction_values, ioport_size_t mask)
fsp_err_t	R_IOPORT_PortEventInputRead (ioport_ctrl_t *const p_ctrl, bsp_io_port_t port, ioport_size_t *event_data)
fsp_err_t	R_IOPORT_PortEventOutputWrite (ioport_ctrl_t *const p_ctrl, bsp_io_port_t port, ioport_size_t event_data, ioport_size_t mask_value)
fsp_err_t	R_IOPORT_PortRead (ioport_ctrl_t *const p_ctrl, bsp_io_port_t port, ioport_size_t *p_port_value)
fsp_err_t	R_IOPORT_PortWrite (ioport_ctrl_t *const p_ctrl, bsp_io_port_t port, ioport_size_t value, ioport_size_t mask)
fsp_err_t	R_IOPORT_EthernetModeCfg (ioport_ctrl_t *const p_ctrl, ioport_ethernet_channel_t channel, ioport_ethernet_mode_t mode)
fsp_err_t	R_IOPORT_VersionGet (fsp_version_t *p_data)

## Detailed Description

Driver for the I/O Ports peripheral on RA MCUs. This module implements the [I/O Port Interface](#).

## Overview

The I/O port pins operate as general I/O port pins, I/O pins for peripheral modules, interrupt input pins, analog I/O, port group function for the ELC, or bus control pins.

## Features

The IOPORT HAL module can configure the following pin settings:

- Pin direction
- Default output state
- Pull-up
- NMOS/PMOS
- Drive strength
- Event edge trigger (falling, rising or both)
- Whether the pin is to be used as an IRQ pin
- Whether the pin is to be used as an analog pin
- Peripheral connection

The module also provides the following functionality:

- Read/write GPIO pins/ports
- Sets event output data
- Reads event input data

## Configuration

The I/O PORT HAL module must be configured by the user for the desired operation. The operating state of an I/O pin can be set via the RA Configuraton tool. When the project is built a pin configuration file is created. The BSP will automatically configure the MCU IO ports accordingly at startup using the same API functions mentioned in this document.

### Build Time Configurations for r\_ioport

The following build time configurations are defined in fsp\_cfg/r\_ioport\_cfg.h:

Configuration	Options	Default	Description
Parameter Checking	<ul style="list-style-type: none"> <li>• Default (BSP)</li> <li>• Enabled</li> <li>• Disabled</li> </ul>	Default (BSP)	If selected code for parameter checking is included in the build.

### Configurations for Driver > System > I/O Port Driver on r\_ioport

This module can be added to the Stacks tab via New Stack > Driver > System > I/O Port Driver on r\_ioport.

Configuration	Options	Default	Description
Name	Name must be a valid C symbol	g_ioport	Module name.
Port 1 ELC Trigger Source	MCU Specific Options		ELC source that will trigger PORT1
Port 2 ELC Trigger	MCU Specific Options		ELC source that will

Source		trigger PORT2
Port 3 ELC Trigger Source	MCU Specific Options	ELC source that will trigger PORT3
Port 4 ELC Trigger Source	MCU Specific Options	ELC source that will trigger PORT4

## Clock Configuration

The I/O PORT HAL module does not require a specific clock configuration.

## Pin Configuration

The IOPORT module is used for configuring pins.

# Usage Notes

## Port Group Function for ELC

Depending on pin configuration, the IOPORT module can perform automatic reads and writes on ports 1-4 on receipt of an ELC event.

When an event is received by a port, the state of the input pins on the port is saved in a hardware register. Simultaneously, the state of output pins on the port is set or cleared based on settings configured by the user. The functions [R\\_IOPORT\\_PinEventInputRead](#) and [R\\_IOPORT\\_PortEventInputRead](#) allow reading the last event input state of a pin or port, and event-triggered pin output can be configured through [R\\_IOPORT\\_PinEventOutputWrite](#) and [R\\_IOPORT\\_PortEventOutputWrite](#).

In addition, each pin on ports 1-4 can be configured to trigger an ELC event on rising, falling or both edges. This event can be used to activate other modules when the pin changes state.

### Note

*The number of ELC-aware ports vary across MCUs. Refer to the Hardware User's Manual for your device for more details.*

# Examples

## Basic Example

This is a basic example of minimal use of the IOPORT in an application.

```
void basic_example ()
{
    bsp_io_level_t readLevel;
    fsp_err_t      err;

    /* Initialize the IOPORT module and configure the pins
     * Note: The default pin configuration name in the RA Configuraton tool is
     * g_bsp_pin_cfg */
}
```

```
err = R_IOPORT_Open(&g_ioport_ctrl, &g_bsp_pin_cfg);
/* Handle any errors. This function should be defined by the user. */
handle_error(err);
/* Call R_IOPORT_PinsCfg if the configuration was not part of initial configurations
made in open */
err = R_IOPORT_PinsCfg(&g_ioport_ctrl, &g_runtime_pin_cfg);
handle_error(err);
/* Set Pin 00 of Port 06 to High */
err = R_IOPORT_PinWrite(&g_ioport_ctrl, BSP_IO_PORT_06_PIN_00, BSP_IO_LEVEL_HIGH
);
handle_error(err);
/* Read Pin 00 of Port 06*/
err = R_IOPORT_PinRead(&g_ioport_ctrl, BSP_IO_PORT_06_PIN_00, &readLevel);
handle_error(err);
}
```

## Blinky Example

This example uses IOPORT to configure and toggle a pin to blink an LED.

```
void blinky_example ()
{
    fsp_err_t err;
    /* Initialize the IOPORT module and configure the pins */
    err = R_IOPORT_Open(&g_ioport_ctrl, &g_bsp_pin_cfg);
    /* Handle any errors. This function should be defined by the user. */
    handle_error(err);
    /* Configure Pin as output
    * Call the R_IOPORT_PinCfg if the configuration was not part of initial
configurations made in open */
    err = R_IOPORT_PinCfg(&g_ioport_ctrl, BSP_IO_PORT_06_PIN_00,
BSP_IO_DIRECTION_OUTPUT);
    handle_error(err);
    bsp_io_level_t level = BSP_IO_LEVEL_LOW;
    while (1)
```

```
{
/* Determine the next state of the LEDs */
if (BSP_IO_LEVEL_LOW == level)
{
    level = BSP_IO_LEVEL_HIGH;
}
else
{
    level = BSP_IO_LEVEL_LOW;
}
/* Update LED on RA6M3-PK */
err = R_IOPORT_PinWrite(&g_ioport_ctrl, BSP_IO_PORT_06_PIN_00, level);
handle_error(err);
/* Delay */
R_BSP_SoftwareDelay(100, BSP_DELAY_UNITS_MILLISECONDS); // NOLINT
}
}
```

## ELC Example

This is an example of using IOPORT with ELC events. The ELC event system allows the captured data to be stored when it occurs and then read back at a later time.

```
static elc_instance_ctrl_t g_elc_ctrl;
static elc_cfg_t g_elc_cfg;
void ioport_elc_example ()
{
    bsp_io_level_t eventValue;
    fsp_err_t err;
    /* Initializes the software and sets the links defined in the control structure. */
    err = R_ELC_Open(&g_elc_ctrl, &g_elc_cfg);
    /* Handle any errors. This function should be defined by the user. */
    handle_error(err);
    /* Create or modify a link between a peripheral function and an event source. */
    err = R_ELC_LinkSet(&g_elc_ctrl, (elc_peripheral_t) ELC_PERIPHERAL_IOPORT2,
```

```

ELC_EVENT_ELC_SOFTWARE_EVENT_0);

    handle_error(err);

    /* Globally enable event linking in the ELC. */
    err = R_ELC_Enable(&g_elc_ctrl);
    handle_error(err);

    /* Initialize the IOPORT module and configure the pins */
    err = R_IOPORT_Open(&g_ioport_ctrl, &g_bsp_pin_cfg);
    handle_error(err);

    /* Call the R_IOPORT_PinCfg if the configuration was not part of initial
configurations made in open */
    err = R_IOPORT_PinCfg(&g_ioport_ctrl, BSP_IO_PORT_02_PIN_00,
BSP_IO_DIRECTION_INPUT);
    handle_error(err);

    /* Generate an event signal through software to the linked peripheral. */
    err = R_ELC_SoftwareEventGenerate(&g_elc_ctrl, ELC_SOFTWARE_EVENT_0);
    handle_error(err);

    /* Read Pin Event Input. The data(BSP_IO_LEVEL_HIGH/ BSP_IO_LEVEL_LOW) from
BSP_IO_PORT_02_PIN_00 is read into the
    * EIDR bit */
    err = R_IOPORT_PinEventInputRead(&g_ioport_ctrl, BSP_IO_PORT_02_PIN_00,
&eventValue);
    handle_error(err);
}

```

## Data Structures

struct [ioport\\_instance\\_ctrl\\_t](#)

## Enumerations

enum [ioport\\_port\\_pin\\_t](#)

## Data Structure Documentation

### ◆ [ioport\\_instance\\_ctrl\\_t](#)

struct [ioport\\_instance\\_ctrl\\_t](#)

IOPORT private control block. DO NOT MODIFY. Initialization occurs when [R\\_IOPORT\\_Open\(\)](#) is called.

## Enumeration Type Documentation

### ◆ ioport\_port\_pin\_t

enum ioport_port_pin_t	
Superset list of all possible IO port pins.	
Enumerator	
IOPORT_PORT_00_PIN_00	IO port 0 pin 0.
IOPORT_PORT_00_PIN_01	IO port 0 pin 1.
IOPORT_PORT_00_PIN_02	IO port 0 pin 2.
IOPORT_PORT_00_PIN_03	IO port 0 pin 3.
IOPORT_PORT_00_PIN_04	IO port 0 pin 4.
IOPORT_PORT_00_PIN_05	IO port 0 pin 5.
IOPORT_PORT_00_PIN_06	IO port 0 pin 6.
IOPORT_PORT_00_PIN_07	IO port 0 pin 7.
IOPORT_PORT_00_PIN_08	IO port 0 pin 8.
IOPORT_PORT_00_PIN_09	IO port 0 pin 9.
IOPORT_PORT_00_PIN_10	IO port 0 pin 10.
IOPORT_PORT_00_PIN_11	IO port 0 pin 11.
IOPORT_PORT_00_PIN_12	IO port 0 pin 12.
IOPORT_PORT_00_PIN_13	IO port 0 pin 13.
IOPORT_PORT_00_PIN_14	IO port 0 pin 14.
IOPORT_PORT_00_PIN_15	IO port 0 pin 15.
IOPORT_PORT_01_PIN_00	IO port 1 pin 0.
IOPORT_PORT_01_PIN_01	IO port 1 pin 1.
IOPORT_PORT_01_PIN_02	IO port 1 pin 2.
IOPORT_PORT_01_PIN_03	IO port 1 pin 3.
IOPORT_PORT_01_PIN_04	



	IO port 1 pin 4.
IOPORT_PORT_01_PIN_05	IO port 1 pin 5.
IOPORT_PORT_01_PIN_06	IO port 1 pin 6.
IOPORT_PORT_01_PIN_07	IO port 1 pin 7.
IOPORT_PORT_01_PIN_08	IO port 1 pin 8.
IOPORT_PORT_01_PIN_09	IO port 1 pin 9.
IOPORT_PORT_01_PIN_10	IO port 1 pin 10.
IOPORT_PORT_01_PIN_11	IO port 1 pin 11.
IOPORT_PORT_01_PIN_12	IO port 1 pin 12.
IOPORT_PORT_01_PIN_13	IO port 1 pin 13.
IOPORT_PORT_01_PIN_14	IO port 1 pin 14.
IOPORT_PORT_01_PIN_15	IO port 1 pin 15.
IOPORT_PORT_02_PIN_00	IO port 2 pin 0.
IOPORT_PORT_02_PIN_01	IO port 2 pin 1.
IOPORT_PORT_02_PIN_02	IO port 2 pin 2.
IOPORT_PORT_02_PIN_03	IO port 2 pin 3.
IOPORT_PORT_02_PIN_04	IO port 2 pin 4.
IOPORT_PORT_02_PIN_05	IO port 2 pin 5.
IOPORT_PORT_02_PIN_06	IO port 2 pin 6.
IOPORT_PORT_02_PIN_07	IO port 2 pin 7.
IOPORT_PORT_02_PIN_08	IO port 2 pin 8.
IOPORT_PORT_02_PIN_09	IO port 2 pin 9.
IOPORT_PORT_02_PIN_10	IO port 2 pin 10.
IOPORT_PORT_02_PIN_11	IO port 2 pin 11.
IOPORT_PORT_02_PIN_12	

	IO port 2 pin 12.
IOPORT_PORT_02_PIN_13	IO port 2 pin 13.
IOPORT_PORT_02_PIN_14	IO port 2 pin 14.
IOPORT_PORT_02_PIN_15	IO port 2 pin 15.
IOPORT_PORT_03_PIN_00	IO port 3 pin 0.
IOPORT_PORT_03_PIN_01	IO port 3 pin 1.
IOPORT_PORT_03_PIN_02	IO port 3 pin 2.
IOPORT_PORT_03_PIN_03	IO port 3 pin 3.
IOPORT_PORT_03_PIN_04	IO port 3 pin 4.
IOPORT_PORT_03_PIN_05	IO port 3 pin 5.
IOPORT_PORT_03_PIN_06	IO port 3 pin 6.
IOPORT_PORT_03_PIN_07	IO port 3 pin 7.
IOPORT_PORT_03_PIN_08	IO port 3 pin 8.
IOPORT_PORT_03_PIN_09	IO port 3 pin 9.
IOPORT_PORT_03_PIN_10	IO port 3 pin 10.
IOPORT_PORT_03_PIN_11	IO port 3 pin 11.
IOPORT_PORT_03_PIN_12	IO port 3 pin 12.
IOPORT_PORT_03_PIN_13	IO port 3 pin 13.
IOPORT_PORT_03_PIN_14	IO port 3 pin 14.
IOPORT_PORT_03_PIN_15	IO port 3 pin 15.
IOPORT_PORT_04_PIN_00	IO port 4 pin 0.
IOPORT_PORT_04_PIN_01	IO port 4 pin 1.
IOPORT_PORT_04_PIN_02	IO port 4 pin 2.
IOPORT_PORT_04_PIN_03	IO port 4 pin 3.
IOPORT_PORT_04_PIN_04	

	IO port 4 pin 4.
IOPORT_PORT_04_PIN_05	IO port 4 pin 5.
IOPORT_PORT_04_PIN_06	IO port 4 pin 6.
IOPORT_PORT_04_PIN_07	IO port 4 pin 7.
IOPORT_PORT_04_PIN_08	IO port 4 pin 8.
IOPORT_PORT_04_PIN_09	IO port 4 pin 9.
IOPORT_PORT_04_PIN_10	IO port 4 pin 10.
IOPORT_PORT_04_PIN_11	IO port 4 pin 11.
IOPORT_PORT_04_PIN_12	IO port 4 pin 12.
IOPORT_PORT_04_PIN_13	IO port 4 pin 13.
IOPORT_PORT_04_PIN_14	IO port 4 pin 14.
IOPORT_PORT_04_PIN_15	IO port 4 pin 15.
IOPORT_PORT_05_PIN_00	IO port 5 pin 0.
IOPORT_PORT_05_PIN_01	IO port 5 pin 1.
IOPORT_PORT_05_PIN_02	IO port 5 pin 2.
IOPORT_PORT_05_PIN_03	IO port 5 pin 3.
IOPORT_PORT_05_PIN_04	IO port 5 pin 4.
IOPORT_PORT_05_PIN_05	IO port 5 pin 5.
IOPORT_PORT_05_PIN_06	IO port 5 pin 6.
IOPORT_PORT_05_PIN_07	IO port 5 pin 7.
IOPORT_PORT_05_PIN_08	IO port 5 pin 8.
IOPORT_PORT_05_PIN_09	IO port 5 pin 9.
IOPORT_PORT_05_PIN_10	IO port 5 pin 10.
IOPORT_PORT_05_PIN_11	IO port 5 pin 11.
IOPORT_PORT_05_PIN_12	

	IO port 5 pin 12.
IOPORT_PORT_05_PIN_13	IO port 5 pin 13.
IOPORT_PORT_05_PIN_14	IO port 5 pin 14.
IOPORT_PORT_05_PIN_15	IO port 5 pin 15.
IOPORT_PORT_06_PIN_00	IO port 6 pin 0.
IOPORT_PORT_06_PIN_01	IO port 6 pin 1.
IOPORT_PORT_06_PIN_02	IO port 6 pin 2.
IOPORT_PORT_06_PIN_03	IO port 6 pin 3.
IOPORT_PORT_06_PIN_04	IO port 6 pin 4.
IOPORT_PORT_06_PIN_05	IO port 6 pin 5.
IOPORT_PORT_06_PIN_06	IO port 6 pin 6.
IOPORT_PORT_06_PIN_07	IO port 6 pin 7.
IOPORT_PORT_06_PIN_08	IO port 6 pin 8.
IOPORT_PORT_06_PIN_09	IO port 6 pin 9.
IOPORT_PORT_06_PIN_10	IO port 6 pin 10.
IOPORT_PORT_06_PIN_11	IO port 6 pin 11.
IOPORT_PORT_06_PIN_12	IO port 6 pin 12.
IOPORT_PORT_06_PIN_13	IO port 6 pin 13.
IOPORT_PORT_06_PIN_14	IO port 6 pin 14.
IOPORT_PORT_06_PIN_15	IO port 6 pin 15.
IOPORT_PORT_07_PIN_00	IO port 7 pin 0.
IOPORT_PORT_07_PIN_01	IO port 7 pin 1.
IOPORT_PORT_07_PIN_02	IO port 7 pin 2.
IOPORT_PORT_07_PIN_03	IO port 7 pin 3.
IOPORT_PORT_07_PIN_04	

	IO port 7 pin 4.
IOPORT_PORT_07_PIN_05	IO port 7 pin 5.
IOPORT_PORT_07_PIN_06	IO port 7 pin 6.
IOPORT_PORT_07_PIN_07	IO port 7 pin 7.
IOPORT_PORT_07_PIN_08	IO port 7 pin 8.
IOPORT_PORT_07_PIN_09	IO port 7 pin 9.
IOPORT_PORT_07_PIN_10	IO port 7 pin 10.
IOPORT_PORT_07_PIN_11	IO port 7 pin 11.
IOPORT_PORT_07_PIN_12	IO port 7 pin 12.
IOPORT_PORT_07_PIN_13	IO port 7 pin 13.
IOPORT_PORT_07_PIN_14	IO port 7 pin 14.
IOPORT_PORT_07_PIN_15	IO port 7 pin 15.
IOPORT_PORT_08_PIN_00	IO port 8 pin 0.
IOPORT_PORT_08_PIN_01	IO port 8 pin 1.
IOPORT_PORT_08_PIN_02	IO port 8 pin 2.
IOPORT_PORT_08_PIN_03	IO port 8 pin 3.
IOPORT_PORT_08_PIN_04	IO port 8 pin 4.
IOPORT_PORT_08_PIN_05	IO port 8 pin 5.
IOPORT_PORT_08_PIN_06	IO port 8 pin 6.
IOPORT_PORT_08_PIN_07	IO port 8 pin 7.
IOPORT_PORT_08_PIN_08	IO port 8 pin 8.
IOPORT_PORT_08_PIN_09	IO port 8 pin 9.
IOPORT_PORT_08_PIN_10	IO port 8 pin 10.
IOPORT_PORT_08_PIN_11	IO port 8 pin 11.
IOPORT_PORT_08_PIN_12	

	IO port 8 pin 12.
IOPORT_PORT_08_PIN_13	IO port 8 pin 13.
IOPORT_PORT_08_PIN_14	IO port 8 pin 14.
IOPORT_PORT_08_PIN_15	IO port 8 pin 15.
IOPORT_PORT_09_PIN_00	IO port 9 pin 0.
IOPORT_PORT_09_PIN_01	IO port 9 pin 1.
IOPORT_PORT_09_PIN_02	IO port 9 pin 2.
IOPORT_PORT_09_PIN_03	IO port 9 pin 3.
IOPORT_PORT_09_PIN_04	IO port 9 pin 4.
IOPORT_PORT_09_PIN_05	IO port 9 pin 5.
IOPORT_PORT_09_PIN_06	IO port 9 pin 6.
IOPORT_PORT_09_PIN_07	IO port 9 pin 7.
IOPORT_PORT_09_PIN_08	IO port 9 pin 8.
IOPORT_PORT_09_PIN_09	IO port 9 pin 9.
IOPORT_PORT_09_PIN_10	IO port 9 pin 10.
IOPORT_PORT_09_PIN_11	IO port 9 pin 11.
IOPORT_PORT_09_PIN_12	IO port 9 pin 12.
IOPORT_PORT_09_PIN_13	IO port 9 pin 13.
IOPORT_PORT_09_PIN_14	IO port 9 pin 14.
IOPORT_PORT_09_PIN_15	IO port 9 pin 15.
IOPORT_PORT_10_PIN_00	IO port 10 pin 0.
IOPORT_PORT_10_PIN_01	IO port 10 pin 1.
IOPORT_PORT_10_PIN_02	IO port 10 pin 2.
IOPORT_PORT_10_PIN_03	IO port 10 pin 3.
IOPORT_PORT_10_PIN_04	

	IO port 10 pin 4.
IOPORT_PORT_10_PIN_05	IO port 10 pin 5.
IOPORT_PORT_10_PIN_06	IO port 10 pin 6.
IOPORT_PORT_10_PIN_07	IO port 10 pin 7.
IOPORT_PORT_10_PIN_08	IO port 10 pin 8.
IOPORT_PORT_10_PIN_09	IO port 10 pin 9.
IOPORT_PORT_10_PIN_10	IO port 10 pin 10.
IOPORT_PORT_10_PIN_11	IO port 10 pin 11.
IOPORT_PORT_10_PIN_12	IO port 10 pin 12.
IOPORT_PORT_10_PIN_13	IO port 10 pin 13.
IOPORT_PORT_10_PIN_14	IO port 10 pin 14.
IOPORT_PORT_10_PIN_15	IO port 10 pin 15.
IOPORT_PORT_11_PIN_00	IO port 11 pin 0.
IOPORT_PORT_11_PIN_01	IO port 11 pin 1.
IOPORT_PORT_11_PIN_02	IO port 11 pin 2.
IOPORT_PORT_11_PIN_03	IO port 11 pin 3.
IOPORT_PORT_11_PIN_04	IO port 11 pin 4.
IOPORT_PORT_11_PIN_05	IO port 11 pin 5.
IOPORT_PORT_11_PIN_06	IO port 11 pin 6.
IOPORT_PORT_11_PIN_07	IO port 11 pin 7.
IOPORT_PORT_11_PIN_08	IO port 11 pin 8.
IOPORT_PORT_11_PIN_09	IO port 11 pin 9.
IOPORT_PORT_11_PIN_10	IO port 11 pin 10.
IOPORT_PORT_11_PIN_11	IO port 11 pin 11.
IOPORT_PORT_11_PIN_12	

	IO port 11 pin 12.
IOPORT_PORT_11_PIN_13	IO port 11 pin 13.
IOPORT_PORT_11_PIN_14	IO port 11 pin 14.
IOPORT_PORT_11_PIN_15	IO port 11 pin 15.

## Function Documentation

### ◆ R\_IOPORT\_Open()

`fsp_err_t R_IOPORT_Open ( ioport_ctrl_t *const p_ctrl, const ioport_cfg_t * p_cfg )`

Initializes internal driver data, then calls pin configuration function to configure pins.

#### Return values

FSP_SUCCESS	Pin configuration data written to PFS register(s)
FSP_ERR_ASSERTION	NULL pointer
FSP_ERR_ALREADY_OPEN	Module is already open.

### ◆ R\_IOPORT\_Close()

`fsp_err_t R_IOPORT_Close ( ioport_ctrl_t *const p_ctrl )`

Resets IOPORT registers. Implements `ioport_api_t::close`

#### Return values

FSP_SUCCESS	The IOPORT was successfully uninitialized
FSP_ERR_ASSERTION	p_ctrl was NULL
FSP_ERR_NOT_OPEN	The module has not been opened



◆ **R\_IOPORT\_PinsCfg()**

```
fsp_err_t R_IOPORT_PinsCfg ( ioport_ctrl_t *const p_ctrl, const ioport_cfg_t * p_cfg )
```

Configures the functions of multiple pins by loading configuration data into pin PFS registers. Implements `ioport_api_t::pinsCfg`.

This function initializes the supplied list of PmnPFS registers with the supplied values. This data can be generated by the Pins tab of the RA Configuration editor or manually by the developer. Different pin configurations can be loaded for different situations such as low power modes and testing.

**Return values**

FSP_SUCCESS	Pin configuration data written to PFS register(s)
FSP_ERR_NOT_OPEN	The module has not been opened
FSP_ERR_ASSERTION	NULL pointer

◆ **R\_IOPORT\_PinCfg()**

```
fsp_err_t R_IOPORT_PinCfg ( ioport_ctrl_t *const p_ctrl, bsp_io_port_pin_t pin, uint32_t cfg )
```

Configures the settings of a pin. Implements `ioport_api_t::pinCfg`.

**Return values**

FSP_SUCCESS	Pin configured
FSP_ERR_NOT_OPEN	The module has not been opened
FSP_ERR_ASSERTION	NULL pointer

**Note**

*This function is re-entrant for different pins. This function will change the configuration of the pin with the new configuration. For example it is not possible with this function to change the drive strength of a pin while leaving all the other pin settings unchanged. To achieve this the original settings with the required change will need to be written using this function.*

### ◆ R\_IOPORT\_PinEventInputRead()

```
fsp_err_t R_IOPORT_PinEventInputRead ( ioport_ctrl_t *const p_ctrl, bsp_io_port_pin_t pin,
bsp_io_level_t * p_pin_event )
```

Reads the value of the event input data of a specific pin. Implements `ioport_api_t::pinEventInputRead`.

The pin event data is captured in response to a trigger from the ELC. This function enables this data to be read. Using the event system allows the captured data to be stored when it occurs and then read back at a later time.

#### Return values

FSP_SUCCESS	Pin read
FSP_ERR_ASSERTION	NULL pointer
FSP_ERR_NOT_OPEN	The module has not been opened
FSP_ERR_INVALID_ARGUMENT	Port is not valid ELC PORT.

#### Note

*This function is re-entrant.*

### ◆ R\_IOPORT\_PinEventOutputWrite()

```
fsp_err_t R_IOPORT_PinEventOutputWrite ( ioport_ctrl_t *const p_ctrl, bsp_io_port_pin_t pin,
bsp_io_level_t pin_value )
```

This function writes the event output data value to a pin. Implements `ioport_api_t::pinEventOutputWrite`.

Using the event system enables a pin state to be stored by this function in advance of being output on the pin. The output to the pin will occur when the ELC event occurs.

#### Return values

FSP_SUCCESS	Pin event data written
FSP_ERR_INVALID_ARGUMENT	Port or Pin or value not valid
FSP_ERR_NOT_OPEN	The module has not been opened
FSP_ERR_ASSERTION	NULL pointer

#### Note

*This function is re-entrant for different ports.*

◆ **R\_IOPORT\_PinRead()**

```
fsp_err_t R_IOPORT_PinRead ( ioport_ctrl_t *const p_ctrl, bsp_io_port_pin_t pin, bsp_io_level_t *
p_pin_value )
```

Reads the level on a pin. Implements `ioport_api_t::pinRead`.

**Return values**

FSP_SUCCESS	Pin read
FSP_ERR_ASSERTION	NULL pointer
FSP_ERR_NOT_OPEN	The module has not been opened

*Note*

*This function is re-entrant for different pins.*

◆ **R\_IOPORT\_PinWrite()**

```
fsp_err_t R_IOPORT_PinWrite ( ioport_ctrl_t *const p_ctrl, bsp_io_port_pin_t pin, bsp_io_level_t
level )
```

Sets a pin's output either high or low. Implements `ioport_api_t::pinWrite`.

**Return values**

FSP_SUCCESS	Pin written to
FSP_ERR_INVALID_ARGUMENT	The pin and/or level not valid
FSP_ERR_NOT_OPEN	The module has not been opene
FSP_ERR_ASSERTION	NULL pointerd

*Note*

*This function is re-entrant for different pins. This function makes use of the PCNTR3 register to atomically modify the level on the specified pin on a port.*

### ◆ R\_IOPORT\_PortDirectionSet()

```
fsp_err_t R_IOPORT_PortDirectionSet ( ioport_ctrl_t *const p_ctrl, bsp_io_port_t port, ioport_size_t
direction_values, ioport_size_t mask )
```

Sets the direction of individual pins on a port. Implements `ioport_api_t::portDirectionSet()`.

Multiple pins on a port can be set to inputs or outputs at once. Each bit in the mask parameter corresponds to a pin on the port. For example, bit 7 corresponds to pin 7, bit 6 to pin 6, and so on. If a bit is set to 1 then the corresponding pin will be changed to an input or an output as specified by the direction values. If a mask bit is set to 0 then the direction of the pin will not be changed.

#### Return values

FSP_SUCCESS	Port direction updated
FSP_ERR_INVALID_ARGUMENT	The port and/or mask not valid
FSP_ERR_NOT_OPEN	The module has not been opened
FSP_ERR_ASSERTION	NULL pointer

#### Note

*This function is re-entrant for different ports.*

### ◆ R\_IOPORT\_PortEventInputRead()

```
fsp_err_t R_IOPORT_PortEventInputRead ( ioport_ctrl_t *const p_ctrl, bsp_io_port_t port,
ioport_size_t * p_event_data )
```

Reads the value of the event input data. Implements `ioport_api_t::portEventInputRead()`.

The event input data for the port will be read. Each bit in the returned value corresponds to a pin on the port. For example, bit 7 corresponds to pin 7, bit 6 to pin 6, and so on.

The port event data is captured in response to a trigger from the ELC. This function enables this data to be read. Using the event system allows the captured data to be stored when it occurs and then read back at a later time.

#### Return values

FSP_SUCCESS	Port read
FSP_ERR_INVALID_ARGUMENT	Port not a valid ELC port
FSP_ERR_ASSERTION	NULL pointer
FSP_ERR_NOT_OPEN	The module has not been opened

#### Note

*This function is re-entrant for different ports.*

### ◆ R\_IOPORT\_PortEventOutputWrite()

```
fsp_err_t R_IOPORT_PortEventOutputWrite ( ioport_ctrl_t *const p_ctrl, bsp_io_port_t port,
ioport_size_t event_data, ioport_size_t mask_value )
```

This function writes the set and reset event output data for a port. Implements `ioport_api_t::portEventOutputWrite`.

Using the event system enables a port state to be stored by this function in advance of being output on the port. The output to the port will occur when the ELC event occurs.

The input value will be written to the specified port when an ELC event configured for that port occurs. Each bit in the value parameter corresponds to a bit on the port. For example, bit 7 corresponds to pin 7, bit 6 to pin 6, and so on. Each bit in the mask parameter corresponds to a pin on the port.

#### Return values

FSP_SUCCESS	Port event data written
FSP_ERR_INVALID_ARGUMENT	Port or Mask not valid
FSP_ERR_NOT_OPEN	The module has not been opened
FSP_ERR_ASSERTION	NULL pointer

#### Note

*This function is re-entrant for different ports.*

### ◆ R\_IOPORT\_PortRead()

```
fsp_err_t R_IOPORT_PortRead ( ioport_ctrl_t *const p_ctrl, bsp_io_port_t port, ioport_size_t *
p_port_value )
```

Reads the value on an IO port. Implements `ioport_api_t::portRead`.

The specified port will be read, and the levels for all the pins will be returned. Each bit in the returned value corresponds to a pin on the port. For example, bit 7 corresponds to pin 7, bit 6 to pin 6, and so on.

#### Return values

FSP_SUCCESS	Port read
FSP_ERR_ASSERTION	NULL pointer
FSP_ERR_NOT_OPEN	The module has not been opened

#### Note

*This function is re-entrant for different ports.*

### ◆ R\_IOPORT\_PortWrite()

```
fsp_err_t R_IOPORT_PortWrite ( ioport_ctrl_t *const p_ctrl, bsp_io_port_t port, ioport_size_t value,
ioport_size_t mask )
```

Writes to multiple pins on a port. Implements `ioport_api_t::portWrite`.

The input value will be written to the specified port. Each bit in the value parameter corresponds to a bit on the port. For example, bit 7 corresponds to pin 7, bit 6 to pin 6, and so on. Each bit in the mask parameter corresponds to a pin on the port.

Only the bits with the corresponding bit in the mask value set will be updated. For example, value = 0xFFFF, mask = 0x0003 results in only bits 0 and 1 being updated.

#### Return values

FSP_SUCCESS	Port written to
FSP_ERR_INVALID_ARGUMENT	The port and/or mask not valid
FSP_ERR_NOT_OPEN	The module has not been opened
FSP_ERR_ASSERTION	NULL pointerd

#### Note

*This function is re-entrant for different ports. This function makes use of the PCNTR3 register to atomically modify the levels on the specified pins on a port.*

### ◆ R\_IOPORT\_EthernetModeCfg()

```
fsp_err_t R_IOPORT_EthernetModeCfg ( ioport_ctrl_t *const p_ctrl, ioport_ethernet_channel_t
channel, ioport_ethernet_mode_t mode )
```

Configures Ethernet channel PHY mode. Implements `ioport_api_t::pinEthernetModeCfg`.

#### Return values

FSP_SUCCESS	Ethernet PHY mode set
FSP_ERR_INVALID_ARGUMENT	Channel or mode not valid
FSP_ERR_UNSUPPORTED	Ethernet configuration not supported on this device.
FSP_ERR_NOT_OPEN	The module has not been opened
FSP_ERR_ASSERTION	NULL pointer

#### Note

*This function is not re-entrant.*

### ◆ R\_IOPORT\_VersionGet()

`fsp_err_t R_IOPORT_VersionGet ( fsp_version_t * p_data)`

Returns IOPort HAL driver version. Implements `ioport_api_t::versionGet`.

#### Return values

FSP_SUCCESS	Version information read
FSP_ERR_ASSERTION	The parameter p_data is NULL

#### Note

*This function is reentrant.*

## 4.2.29 Independent Watchdog Timer (r\_iwdt)

### Modules

#### Functions

`fsp_err_t R_IWDT_Refresh (wdt_ctrl_t *const p_api_ctrl)`

`fsp_err_t R_IWDT_Open (wdt_ctrl_t *const p_api_ctrl, wdt_cfg_t const *const p_cfg)`

`fsp_err_t R_IWDT_StatusClear (wdt_ctrl_t *const p_api_ctrl, const wdt_status_t status)`

`fsp_err_t R_IWDT_StatusGet (wdt_ctrl_t *const p_api_ctrl, wdt_status_t *const p_status)`

`fsp_err_t R_IWDT_CounterGet (wdt_ctrl_t *const p_api_ctrl, uint32_t *const p_count)`

`fsp_err_t R_IWDT_TimeoutGet (wdt_ctrl_t *const p_api_ctrl, wdt_timeout_values_t *const p_timeout)`

`fsp_err_t R_IWDT_CallbackSet (wdt_ctrl_t *const p_ctrl, void(*p_callback)(wdt_callback_args_t *), void const *const p_context, wdt_callback_args_t *const p_callback_memory)`

`fsp_err_t R_IWDT_VersionGet (fsp_version_t *const p_data)`

### Detailed Description

Driver for the IWDT peripheral on RA MCUs. This module implements the [WDT Interface](#).

## Overview

The independent watchdog timer is used to recover from unexpected errors in an application. The timer must be refreshed periodically in the permitted count window by the application. If the count is allowed to underflow or refresh occurs outside of the valid refresh period, the IWDT resets the device or generates an NMI.

### Features

The IWDT HAL module has the following key features:

- When the IWDT underflows or is refreshed outside of the permitted refresh window, one of the following events can occur:
  - Resetting of the device
  - Generation of an NMI
- The IWDT begins counting at reset.

### Selecting a Watchdog

RA MCUs have two watchdog peripherals: the watchdog timer (WDT) and the independent watchdog timer (IWDT). When selecting between them, consider these factors:

	WDT	IWDT
Start Mode	The WDT can be started from the application (register start mode) or configured by hardware to start automatically (auto start mode).	The IWDT can only be configured by hardware to start automatically.
Clock Source	The WDT runs off a peripheral clock.	The IWDT has its own clock source which improves safety.

## Configuration

### Build Time Configurations for r\_iwdt

The following build time configurations are defined in fsp\_cfg/r\_iwdt\_cfg.h:

Configuration	Options	Default	Description
Parameter Checking	<ul style="list-style-type: none"> <li>• Default (BSP)</li> <li>• Enabled</li> <li>• Disabled</li> </ul>	Default (BSP)	If selected code for parameter checking is included in the build.

### Configurations for Driver > Monitoring > Watchdog Driver on r\_iwdt

This module can be added to the Stacks tab via New Stack > Driver > Monitoring > Watchdog Driver on r\_iwdt. Non-secure callable guard functions can be generated for this module by right clicking the module in the RA Configuration tool and checking the "Non-secure Callable" box.

Configuration	Options	Default	Description
---------------	---------	---------	-------------



Name	Name must be a valid C symbol	g_wdt0	Module name.
NMI callback	Name must be a valid C symbol	NULL	A user callback function can be provided here. If this callback function is provided, it is called from the interrupt service routine (ISR) when the watchdog triggers.

*Note*

The IWDT has additional configurable settings in the OFS0 register in the **BSP** tab properties window. These settings include the following:

- Start Mode
- Timeout Period
- Dedicated Clock Frequency Divisor
- Window End Position
- Window Start Position
- Reset Interrupt Request Select
- Stop Control

Review the OFS0 properties window to see additional details.

**Clock Configuration**

The IWDT clock is based on the IWDTCLK frequency. You can set the IWDTCLK frequency divider using the **BSP** tab of the RA Configuration editor.

**Pin Configuration**

This module does not use I/O pins.

**Usage Notes****NMI Interrupt**

The independent watchdog timer uses the NMI, which is enabled by default. No special configuration is required. When the NMI is triggered, the callback function registered during open is called.

**Period Calculation**

The IWDT operates from IWDTCLK. With a IWDTCLK of 15000 Hz, the maximum time from the last refresh to device reset or NMI generation will be just below 35 seconds as detailed below.

IWDTCLK = 15000 Hz  
 Clock division ratio = IWDTCLK / 256  
 Timeout period = 2048 cycles  
 WDT clock frequency = 15000 Hz / 256 = 58.59 Hz  
 Cycle time = 1 / 58.59 Hz = 17.067 ms  
 Timeout = 17.067 ms x 2048 cycles = 34.95 seconds

**Limitations**

Developers should be aware of the following limitations when using the IWDT:

- When using a J-Link debugger the IWDT counter does not count and therefore will not reset the device or generate an NMI. To enable the watchdog to count and generate a reset or NMI while debugging, add this line of code in the application:

```
/* (Optional) Enable the IWDT to count and generate NMI or reset when the
 * debugger is connected. */
R_DEBUG->DBGSTOPPCR_b.DBGSTOP_IWDT = 0;
```

- If the IWDT is configured to stop the counter in low power mode, then your application must restart the watchdog by calling `R_IWDT_Refresh()` after the MCU wakes from low power mode.

## Examples

### IWDT Basic Example

This is a basic example of minimal use of the IWDT in an application.

```
void iwdt_basic_example (void)
{
    fsp_err_t err = FSP_SUCCESS;

    /* In auto start mode, the IWDT starts counting immediately when the MCU is powered
    on. */

    /* Initializes the module. */
    err = R_IWDT_Open(&g_iwdt0_ctrl, &g_iwdt0_cfg);

    /* Handle any errors. This function should be defined by the user. */
    handle_error(err);

    while (true)
    {
        /* Application work here. */

        /* Refresh before the counter underflows to prevent reset or NMI based on the
        setting. */
        (void) R_IWDT_Refresh(&g_iwdt0_ctrl);
    }
}
```

### IWDT Advanced Example

This example demonstrates using a start window and gives an example callback to handle an NMI

generated by an underflow or refresh error.

```
#define IWDT_TIMEOUT_COUNTS (2048U)
#define IWDT_MAX_COUNTER (IWDT_TIMEOUT_COUNTS - 1U)
#define IWDT_START_WINDOW_75 ((IWDT_MAX_COUNTER * 3) / 4)
/* Example callback called when a watchdog NMI occurs. */
void iwdt_callback (wdt_callback_args_t * p_args)
{
    FSP_PARAMETER_NOT_USED(p_args);
    fsp_err_t err = FSP_SUCCESS;
    /* (Optional) Determine the source of the NMI. */
    wdt_status_t status = WDT_STATUS_NO_ERROR;
    err = R_IWDT_StatusGet(&g_iwdt0_ctrl, &status);
    handle_error(err);
    /* (Optional) Log source of NMI and any other debug information. */
    /* (Optional) Clear the error flags. */
    err = R_IWDT_StatusClear(&g_iwdt0_ctrl, status);
    handle_error(err);
    /* (Optional) Issue a software reset to reset the MCU. */
    __NVIC_SystemReset();
}
void iwdt_advanced_example (void)
{
    fsp_err_t err = FSP_SUCCESS;
    /* (Optional) Enable the IWDT to count and generate NMI or reset when the
    * debugger is connected. */
    R_DEBUG->DBGSTOPPCR_b.DBGSTOP_IWDT = 0;
    /* (Optional) Check if the IWDTRF flag is set to know if the system is
    * recovering from a IWDT reset. */
    if (R_SYSTEM->RSTSR1_b.IWDTRF)
    {
        /* Clear the flag. */
        R_SYSTEM->RSTSR1 = 0U;
    }
    /* Open the module. */
```

```

    err = R_IWDT_Open(&g_iwdt0_ctrl, &g_iwdt0_cfg);
/* Handle any errors. This function should be defined by the user. */
    handle_error(err);
/* Initialize other application code. */
/* Do not call R_IWDT_Refresh() in auto start mode unless the
 * counter is in the acceptable refresh window. */
    (void) R_IWDT_Refresh(&g_iwdt0_ctrl);
while (true)
    {
/* Application work here. */
/* (Optional) If there is a chance the application takes less time than
 * the start window, verify the IWDT counter is past the start window
 * before refreshing the IWDT. */
        uint32_t iwdt_counter = 0U;
do
    {
/* Read the current IWDT counter value. */
        err = R_IWDT_CounterGet(&g_iwdt0_ctrl, &iwdt_counter);
        handle_error(err);
        } while (iwdt_counter >= IWDT_START_WINDOW_75);
/* Refresh before the counter underflows to prevent reset or NMI. */
        (void) R_IWDT_Refresh(&g_iwdt0_ctrl);
    }
}

```

## Data Structures

struct [iwdt\\_instance\\_ctrl\\_t](#)

## Data Structure Documentation

### ◆ iwdt\_instance\_ctrl\_t

struct iwdt_instance_ctrl_t	
IWDT control block. DO NOT INITIALIZE. Initialization occurs when <a href="#">wdt_api_t::open</a> is called.	
<b>Data Fields</b>	
uint32_t	<a href="#">wdt_open</a>
	Indicates whether the open() API has been successfully called.

void const *	<a href="#">p_context</a>
	Placeholder for user data. Passed to the user callback in <a href="#">wdt_callback_args_t</a> .
R_IWDT_Type *	<a href="#">p_reg</a>
	Pointer to register base address.
void(*	<a href="#">p_callback</a> )(wdt_callback_args_t *p_args)
	Callback provided when a WDT NMI ISR occurs.

## Function Documentation

### ◆ R\_IWDT\_Refresh()

```
fsp_err_t R_IWDT_Refresh ( wdt_ctrl_t *const p_api_ctrl)
```

Refresh the Independent Watchdog Timer. If the refresh fails due to being performed outside of the permitted refresh period the device will either reset or trigger an NMI ISR to run.

Example:

```
/* Refresh before the counter underflows to prevent reset or NMI based on the
setting. */
(void) R_IWDT_Refresh(&g_iwdt0_ctrl);
```

#### Return values

FSP_SUCCESS	IWDT successfully refreshed.
FSP_ERR_ASSERTION	One or more parameters are NULL pointers.
FSP_ERR_NOT_OPEN	The driver has not been opened. Perform <a href="#">R_IWDT_Open()</a> first.

◆ **R\_IWDT\_Open()**

```
fsp_err_t R_IWDT_Open ( wdt_ctrl_t *const p_api_ctrl, wdt_cfg_t const *const p_cfg )
```

Register the IWDT NMI callback.

Example:

```
/* Initializes the module. */
err = R_IWDT_Open(&g_iwdt0_ctrl, &g_iwdt0_cfg);
```

**Return values**

FSP_SUCCESS	IWDT successfully configured.
FSP_ERR_ASSERTION	Null Pointer.
FSP_ERR_NOT_ENABLED	An attempt to open the IWDT when the OFS0 register is not configured for auto-start mode.
FSP_ERR_ALREADY_OPEN	Module is already open. This module can only be opened once.
FSP_ERR_INVALID_STATE	The security state of the NMI and the module do not match.

◆ **R\_IWDT\_StatusClear()**

```
fsp_err_t R_IWDT_StatusClear ( wdt_ctrl_t *const p_api_ctrl, const wdt_status_t status )
```

Clear the IWDT status and error flags. Implements `wdt_api_t::statusClear`.

Example:

```
/* (Optional) Clear the error flags. */
err = R_IWDT_StatusClear(&g_iwdt0_ctrl, status);
handle_error(err);
```

**Return values**

FSP_SUCCESS	IWDT flag(s) successfully cleared.
FSP_ERR_ASSERTION	Null pointer as a parameter.
FSP_ERR_NOT_OPEN	The driver has not been opened. Perform <a href="#">R_IWDT_Open()</a> first.

◆ **R\_IWDT\_StatusGet()**

```
fsp_err_t R_IWDT_StatusGet ( wdt_ctrl_t*const p_api_ctrl, wdt_status_t*const p_status )
```

Read the IWDT status flags. When the IWDT is configured to output a reset on underflow or refresh error reading the status and error flags can be read after reset to establish if the IWDT caused the reset. Reading the status and error flags in NMI output mode indicates whether the IWDT generated the NMI interrupt.

Indicates both status and error conditions.

Example:

```
/* (Optional) Determine the source of the NMI. */
wdt_status_t status = WDT_STATUS_NO_ERROR;
err = R_IWDT_StatusGet(&g_iwdt0_ctrl, &status);
handle_error(err);
```

**Return values**

FSP_SUCCESS	IWDT status successfully read.
FSP_ERR_ASSERTION	Null pointer as a parameter.
FSP_ERR_NOT_OPEN	The driver has not been opened. Perform <a href="#">R_IWDT_Open()</a> first.

◆ **R\_IWDT\_CounterGet()**

```
fsp_err_t R_IWDT_CounterGet ( wdt_ctrl_t*const p_api_ctrl, uint32_t*const p_count )
```

Read the current count value of the IWDT. Implements [wdt\\_api\\_t::counterGet](#).

Example:

```
/* Read the current IWDT counter value. */
err = R_IWDT_CounterGet(&g_iwdt0_ctrl, &iwdt_counter);
handle_error(err);
```

**Return values**

FSP_SUCCESS	IWDT current count successfully read.
FSP_ERR_ASSERTION	Null pointer passed as a parameter.
FSP_ERR_NOT_OPEN	The driver has not been opened. Perform <a href="#">R_IWDT_Open()</a> first.

◆ **R\_IWDT\_TimeoutGet()**

```
fsp_err_t R_IWDT_TimeoutGet ( wdt_ctrl_t *const p_api_ctrl, wdt_timeout_values_t *const p_timeout )
```

Read timeout information for the watchdog timer. Implements `wdt_api_t::timeoutGet`.

**Return values**

FSP_SUCCESS	IWDT timeout information retrieved successfully.
FSP_ERR_ASSERTION	One or more parameters are NULL pointers.
FSP_ERR_NOT_OPEN	The driver has not been opened. Perform <code>R_IWDT_Open()</code> first.

◆ **R\_IWDT\_CallbackSet()**

```
fsp_err_t R_IWDT_CallbackSet ( wdt_ctrl_t *const p_ctrl, void(*) (wdt_callback_args_t *) p_callback, void const *const p_context, wdt_callback_args_t *const p_callback_memory )
```

Updates the user callback and has option of providing memory for callback structure. Implements `wdt_api_t::callbackSet`

**Return values**

FSP_SUCCESS	Callback updated successfully.
FSP_ERR_ASSERTION	A required pointer is NULL.
FSP_ERR_NOT_OPEN	The control block has not been opened.

◆ **R\_IWDT\_VersionGet()**

```
fsp_err_t R_IWDT_VersionGet ( fsp_version_t *const p_data)
```

Return IWDT HAL driver version. Implements `wdt_api_t::versionGet`.

**Return values**

FSP_SUCCESS	Call successful.
FSP_ERR_ASSERTION	Null pointer passed as a parameter.



## 4.2.30 JPEG Codec (r\_jpeg)

### Modules

#### Functions

fsp_err_t	R_JPEG_Open (jpeg_ctrl_t *const p_api_ctrl, jpeg_cfg_t const *const p_cfg)
fsp_err_t	R_JPEG_OutputBufferSet (jpeg_ctrl_t *p_api_ctrl, void *output_buffer, uint32_t output_buffer_size)
fsp_err_t	R_JPEG_InputBufferSet (jpeg_ctrl_t *const p_api_ctrl, void *p_data_buffer, uint32_t data_buffer_size)
fsp_err_t	R_JPEG_StatusGet (jpeg_ctrl_t *p_api_ctrl, jpeg_status_t *p_status)
fsp_err_t	R_JPEG_Close (jpeg_ctrl_t *p_api_ctrl)
fsp_err_t	R_JPEG_VersionGet (fsp_version_t *p_version)
fsp_err_t	R_JPEG_EncodeImageSizeSet (jpeg_ctrl_t *const p_api_ctrl, jpeg_encode_image_size_t *p_image_size)
fsp_err_t	R_JPEG_DecomposeLinesDecodedGet (jpeg_ctrl_t *const p_api_ctrl, uint32_t *const p_lines)
fsp_err_t	R_JPEG_DecomposeHorizontalStrideSet (jpeg_ctrl_t *p_api_ctrl, uint32_t horizontal_stride)
fsp_err_t	R_JPEG_DecomposeImageSizeGet (jpeg_ctrl_t *p_api_ctrl, uint16_t *p_horizontal_size, uint16_t *p_vertical_size)
fsp_err_t	R_JPEG_DecomposeImageSubsampleSet (jpeg_ctrl_t *const p_api_ctrl, jpeg_decode_subsample_t horizontal_subsample, jpeg_decode_subsample_t vertical_subsample)
fsp_err_t	R_JPEG_DecomposePixelFormatGet (jpeg_ctrl_t *p_api_ctrl, jpeg_color_space_t *p_color_space)
fsp_err_t	R_JPEG_ModeSet (jpeg_ctrl_t *const p_api_ctrl, jpeg_mode_t mode)

#### Detailed Description

Driver for the JPEG peripheral on RA MCUs. This module implements the [JPEG Codec Interface](#).

## Overview

The JPEG Codec is a hardware block providing accelerated JPEG image encode and decode functionality independent of the CPU. Images can optionally be partially processed facilitating

streaming applications.

## Features

The JPEG Codec provides a number of options useful in a variety of applications:

- Basic encoding and decoding
- Streaming input and/or output
- Decoding JPEGs of unknown size
- Shrink (sub-sample) an image during the decoding process
- Rearrange input and output byte order (byte, word and/or longword swap)
- JPEG error detection

The specifications for the codec are as follows:

Feature	Options
Decompression input formats	Baseline JPEG Y'CbCr 4:4:4, 4:2:2, 4:2:0 and 4:1:1
Decompression output formats	ARGB8888, RGB565
Compression input formats	Raw Y'CbCr 4:2:2 only
Compression output formats	Baseline JPEG Y'CbCr 4:2:2 only
Byte reordering	Byte, halfword and/or word swapping on input and output
Interrupt sources	Image size acquired, input/output data pause, decode complete, error
Compatible image sizes	See <a href="#">Minimum Coded Unit (MCU)</a> below

## Configuration

### Build Time Configurations for r\_jpeg

The following build time configurations are defined in fsp\_cfg/r\_jpeg\_cfg.h:

Configuration	Options	Default	Description
Parameter Checking	<ul style="list-style-type: none"> <li>• Default (BSP)</li> <li>• Enabled</li> <li>• Disabled</li> </ul>	Default (BSP)	If selected, code for parameter checking is included in the build.
Decode Support	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Enabled	If selected, code for decoding JPEG images is included in the build.
Encode Support	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Disabled	If selected, code for encoding JPEG images is included in the build.

### Configurations for Driver > Graphics > JPEG Codec Driver on r\_jpeg

This module can be added to the Stacks tab via New Stack > Driver > Graphics > JPEG Codec Driver on r\_jpeg.

Configuration	Options	Default	Description
General > Name	Name must be a valid C symbol	g_jpeg0	Module name.
General > Default mode	<ul style="list-style-type: none"> <li>Decode</li> <li>Encode</li> </ul>	Decode	Set the mode to use when calling R_JPEG_Open. This parameter is only used when both Encode and Decode support are enabled.
Decode > Input byte order	MCU Specific Options		Select the byte order of the input data for decoding.
Decode > Output byte order	MCU Specific Options		Select the byte order of the output data for decoding.
Decode > Output color format	<ul style="list-style-type: none"> <li>ARGB8888 (32-bit)</li> <li>RGB565 (16-bit)</li> </ul>	RGB565 (16-bit)	Select the output pixel format for decode operations.
Decode > Output alpha (ARGB8888 only)	Value must be an 8-bit integer (0-255)	255	Specify the alpha value to apply to each output pixel when ARGB8888 format is chosen.
Decode > Callback	Name must be a valid C symbol	NULL	If a callback function is provided it will be called from the interrupt service routine (ISR) each time a related IRQ triggers.
Encode > Horizontal resolution	Value cannot be greater than 65535 and must be a non-negative integer divisible by 16	480	Horizontal resolution of the raw image (in pixels). This value can be configured at runtime via R_JPEG_ImageSizeSet.
Encode > Vertical resolution	Value cannot be greater than 65535 and must be a non-negative integer divisible by 8	272	Vertical resolution of the raw image. This value can be configured at runtime via R_JPEG_ImageSizeSet.
Encode > Horizontal stride	Value cannot be greater than 65535 and must be a non-negative integer	480	Horizontal stride of the raw image buffer (in pixels). This value can be configured at

runtime via  
R\_JPEG\_ImageSizeSet.

Encode > Input byte order	MCU Specific Options		Select the byte order of the input data for encoding.
Encode > Output byte order	MCU Specific Options		Select the byte order of the output data for encoding.
Encode > Reset interval	Value cannot be greater than 65535 and must be a non-negative integer	512	Set the number of MCUs between RST markers. A value of 0 will disable DRI and RST marker output.
Encode > Quality factor	Value must be between 1 and 100 and must be an integer	50	Set the quality factor for encoding (1-100). Lower values produce smaller images at the cost of image quality.
Encode > Callback	Name must be a valid C symbol	NULL	If a callback function is provided it will be called from the interrupt service routine (ISR) each time a related IRQ triggers.
Interrupts > Decode Process Interrupt Priority	MCU Specific Options		Select the decompression interrupt priority.
Interrupts > Data Transfer Interrupt Priority	MCU Specific Options		Select the data transfer interrupt priority.

## Clock Configuration

The peripheral clock for this module is PCLKA. No clocks are provided by this module.

## Pin Configuration

This module does not have any input or output pin connections.

# Usage Notes

## Overview

The JPEG Codec contains both decode and encode hardware. While these two functions are largely independent in configuration only one can be used at a time.

To switch from decode to encode mode (or vice versa) use [R\\_JPEG\\_ModeSet](#) while the JPEG Codec is idle.

## Status

The status value (`jpeg_status_t`) provided by the callback and by `R_JPEG_StatusGet` is a bitfield that encompasses all potential status indication conditions. One or more statuses can be set simultaneously.

## Decoding Process

JPEG decoding can be performed in several ways depending on the application:

- To perform the simplest decode operation where all dimensions are known:
  - Set the input buffer, stride and output buffer then wait for a callback with status `JPEG_STATUS_OPERATION_COMPLETE`.
- To pause after decoding the JPEG header (in order to acquire image dimensions and secure an output buffer):
  - Call `R_JPEG_InputBufferSet` before setting the output buffer and wait for a callback with status `JPEG_STATUS_IMAGE_SIZE_READY`.
- To decode a partial JPEG image then pause until the next chunk is available:
  - Specify a size smaller than the full JPEG data when calling `R_JPEG_InputBufferSet`.
- To pause decoding once an output buffer is filled:
  - Specify a size smaller than the full decoded image when calling `R_JPEG_OutputBufferSet`.

The flowchart below illustrates the steps necessary to handle any decode operation. The statuses given in blue are part of `jpeg_status_t` with the `JPEG_DECODE_STATUS` prefix omitted.

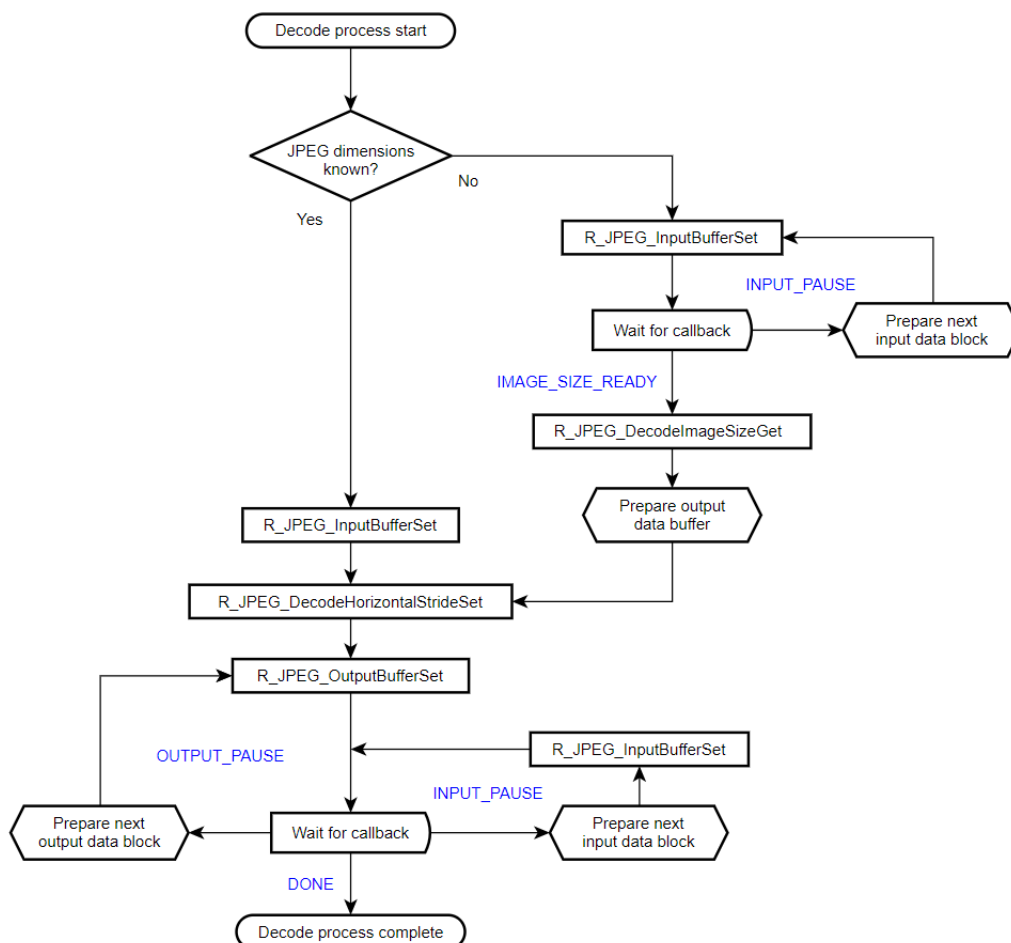


Figure 167: JPEG Decode Operational Flow

## Encoding Process

As compared to decoding, encoding is fairly straightforward. The only option available is to stream input data if desired. The flowchart below details the steps needed to compress an image.

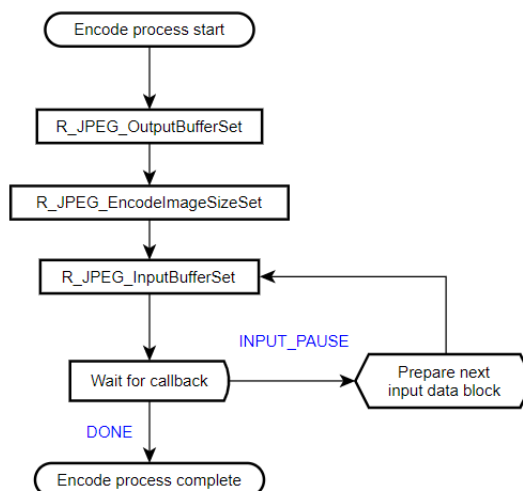


Figure 168: JPEG Encode Operational Flow

## Handling Failed Operations

If an encode or decode operation fails or times out while the codec is running, the peripheral must be reset before it is used again. To reset the JPEG Codec simply close and re-open the module by calling [R\\_JPEG\\_Close](#) followed by [R\\_JPEG\\_Open](#).

## Limitations

Developers should be aware of the following limitations when using the JPEG API.

### Minimum Coded Unit (MCU)

The JPEG Codec can only correctly process images that are an even increment of minimum coded units (MCUs). In other words, depending on the format the width and height of an image to be encoded or decoded must be divisible by the following:

Format	Horizontal	Vertical
Y'CbCr 4:4:4	8 pixels	8 lines
Y'CbCr 4:2:2	16 pixels	8 lines
Y'CbCr 4:1:1	32 pixels	8 lines
Y'CbCr 4:2:0	16 pixels	16 lines

## Encoding Input Format

The encoding unit only supports Y'CbCr 4:2:2 input. Raw RGB888 data can be converted to this format as follows:

```

y = (0.299000f * r) + (0.587000f * g) + (0.114000f * b);
cb = 128 - (0.168736f * r) - (0.331264f * g) + (0.500000f * b);
cr = 128 + (0.500000f * r) - (0.418688f * g) - (0.081312f * b);

```

While these equations are mathematically simple they do use the floating-point unit. To speed things up we can multiply the coefficients by 256/256...

```

y = ((76.5440f * r) + (150.272f * g) + (29.1840f * b)) / 256;
cb = 128 - ((43.1964f * r) - (84.8036f * g) + (128.000f * b)) / 256;
cr = 128 + ((128.000f * r) - (107.184f * g) - (20.8159f * b)) / 256;

```

...which allows the formulas to be calculated entirely with shifts and addition (coefficients rounded to the nearest integer):

```

y = ( (r << 6) + (r << 3) + (r << 2) + r
      + (g << 7) + (g << 4) + (g << 2) + (g << 1)
      + (b << 4) + (b << 3) + (b << 2) + b
    ) >> 8;

cb = 128 - ( (r << 5) + (r << 3) + (r << 1) + r
            + (g << 6) + (g << 4) + (g << 2) + g
            - (b << 7)
          ) >> 8;

cr = 128 + ( (r << 7)
            - (g << 6) - (g << 5) - (g << 3) - (g << 1) - g
            - (b << 4) - (b << 2) - b
          ) >> 8;

```

To compose the final Y'CbCr 4:2:2 data the chroma of every two pixels must be averaged. **In addition, the JPEG Codec expects chrominance values to be in the range -127..127 instead of the standard 1..255.**

```

cb = (uint8_t) ((int8_t) ((cb0 + cb1 + 1) >> 1) - 128);
cr = (uint8_t) ((int8_t) ((cr0 + cr1 + 1) >> 1) - 128);

```

Finally, the below equation composes two 4:2:2 output pixels at a time with standard byte order

(JPEG\_DATA\_ORDER\_NORMAL):

```
out = y0 + (cb << 8) + (y1 << 16) + (cr << 24);
```

*Note*

*RGB565 pixels must be upscaled to RGB888 before using the above formulas. Refer to the below example on [Y'CbCr Conversion](#) for implementation details.*

## Examples

### Basic Decode Example

This is a basic example showing the minimum code required to initialize the JPEG Codec and decode an image.

```
void jpeg_decode_basic (void)
{
    fsp_err_t err;
    /* Open JPEG Codec */
    err = R_JPEG_Open(&g_jpeg_ctrl, &g_jpeg_cfg);
    /* Handle any errors. This function should be defined by the user. */
    handle_error(err);
    /* Set input buffer */
    err = R_JPEG_InputBufferSet(&g_jpeg_ctrl, JPEG_PTR, JPEG_SIZE_BYTES);
    handle_error(err);
    /* Set horizontal stride of output buffer */
    err = R_JPEG_DecodeHorizontalStrideSet(&g_jpeg_ctrl, JPEG_HSIZE);
    handle_error(err);
    /* Set output buffer */
    err = R_JPEG_OutputBufferSet(&g_jpeg_ctrl, decode_buffer, sizeof(decode_buffer));
    handle_error(err);
    /* Wait for decode completion */
    jpeg_status_t status = (jpeg_status_t) 0;
    while (!(status & (JPEG_STATUS_OPERATION_COMPLETE | JPEG_STATUS_ERROR)))
    {
        err = R_JPEG_StatusGet(&g_jpeg_ctrl, &status);
        handle_error(err);
    }
}
```



```
}
```

## Streaming Input/Output Example

In this example JPEG data is read in 512-byte chunks. Decoding is paused when a chunk is read and once the JPEG header is decoded. The image is decoded 16 lines at a time.

### Note

*Streaming is always bypassed when a given buffer's size encompasses the entire input or output image, respectively. Though this example decodes via smaller chunks the input and output data are still contiguous for ease of demonstration. Refer to the comments for further insight as to how to implement streaming with different JPEG/output buffer size combinations.*

```
#define JPEG_INPUT_SIZE_BYTES 512U
/* JPEG Codec status */
static volatile jpeg_status_t g_jpeg_status = JPEG_STATUS_NONE;
/* JPEG event flag */
static volatile uint8_t jpeg_event = 0;
/* Callback function for JPEG decode interrupts */
void jpeg_decode_callback (jpeg_callback_args_t * p_args)
{
    /* Get JPEG Codec status */
    g_jpeg_status = p_args->status;
    /* Set JPEG flag */
    jpeg_event = 1;
}
/* Simple wait that returns 1 if no event happened within the timeout period */
static uint8_t jpeg_event_wait (void)
{
    uint32_t timeout_timer = JPEG_EVENT_TIMEOUT;
    while (!jpeg_event && --timeout_timer)
    {
        /* Spin here until an event callback or timeout */
    }
    jpeg_event = 0;
    return timeout_timer ? 0 : 1;
}
/* Decode a JPEG image to a buffer using streaming input and output */
```

```
void jpeg_decode_streaming (void)
{
    uint8_t      * p_jpeg = (uint8_t *) JPEG_PTR;
    jpeg_status_t status = (jpeg_status_t) 0;
    uint8_t      timeout = 0;
    fsp_err_t    err;
    /* Number of input bytes to read at a time */
    uint32_t input_bytes = JPEG_INPUT_SIZE_BYTES;
    /* Open JPEG unit and start decode */
    err = R_JPEG_Open(&g_jpeg_ctrl, &g_jpeg_cfg);
    /* Handle any errors. This function should be defined by the user. */
    handle_error(err);
    while (!(status & JPEG_STATUS_ERROR) && !timeout)
    {
        /* Set the input buffer to read `input_bytes` bytes at a time */
        err = R_JPEG_InputBufferSet(&g_jpeg_ctrl, p_jpeg, input_bytes);
        handle_error(err);
        /* This delay is required for streaming input mode to function correctly.
         * (Without this delay the JPEG Codec will not correctly locate markers in the file
         header.) */
        R_BSP_SoftwareDelay(10, BSP_DELAY_UNITS_MICROSECONDS);
        /* Wait for a callback */
        timeout = jpeg_event_wait();
        /* Get the status from the callback */
        status = g_jpeg_status;
        /* Break if the header has finished decoding */
        if (status & JPEG_STATUS_IMAGE_SIZE_READY)
        {
            break;
        }
        /* Move pointer to next block of input data (if needed) */
        p_jpeg = (uint8_t *) ((uint32_t) p_jpeg + input_bytes);
    }
    /* Get image size */
}
```

```
uint16_t horizontal;
uint16_t vertical;
err = R_JPEG_DecodeImageSizeGet(&g_jpeg_ctrl, &horizontal, &vertical);
handle_error(err);
/* Prepare output data buffer here if needed (already allocated in this example) */
uint8_t * p_output = decode_buffer;
/* Set horizontal stride */
err = R_JPEG_DecodeHorizontalStrideSet(&g_jpeg_ctrl, horizontal);
handle_error(err);
/* Calculate the number of bytes that will fit in the buffer (16 lines in this
example) */
uint32_t output_size = horizontal * 16U * 4U;
/* Start decoding by setting the output buffer */
err = R_JPEG_OutputBufferSet(&g_jpeg_ctrl, p_output, output_size);
handle_error(err);
while (!(status & JPEG_STATUS_ERROR) && !timeout)
{
/* Wait for a callback */
timeout = jpeg_event_wait();
/* Get the status from the callback */
status = g_jpeg_status;
/* Break if decoding is complete */
if (status & JPEG_STATUS_OPERATION_COMPLETE)
{
break;
}
if (status & JPEG_STATUS_OUTPUT_PAUSE)
{
/* Draw the JPEG work buffer to the framebuffer here (if needed) */
/* Move pointer to next block of output data (if needed) */
p_output += output_size;
/* Set the output buffer to the next 16-line block */
err = R_JPEG_OutputBufferSet(&g_jpeg_ctrl, p_output, output_size);
handle_error(err);
}
```

```
    }
    if (status & JPEG_STATUS_INPUT_PAUSE)
    {
        /* Get next block of input data */
        p_jpeg = (uint8_t *) ((uint32_t) p_jpeg + input_bytes);
        /* Set the new input buffer pointer */
        err = R_JPEG_InputBufferSet(&g_jpeg_ctrl, p_jpeg, input_bytes);
        handle_error(err);
    }
}
/* Close driver to allow encode operations if needed */
err = R_JPEG_Close(&g_jpeg_ctrl);
handle_error(err);
}
```

## Encode Example

This is a basic example showing the minimum code required to initialize the JPEG Codec and encode an image.

### Note

*This example assumes image dimensions are provided in the configuration. If this is not the case, [R\\_JPEG\\_EncodeImageSizeSet](#) must be used to set the size before calling [R\\_JPEG\\_InputBufferSet](#).*

```
void jpeg_encode_basic (void)
{
    fsp_err_t err;
    /* Open JPEG Codec */
    err = R_JPEG_Open(&g_jpeg_ctrl, &g_jpeg_cfg);
    /* Handle any errors. This function should be defined by the user. */
    handle_error(err);
    /* Set output buffer */
    err = R_JPEG_OutputBufferSet(&g_jpeg_ctrl, jpeg_buffer, sizeof(jpeg_buffer));
    handle_error(err);
    /* Set input buffer */
    err = R_JPEG_InputBufferSet(&g_jpeg_ctrl, RAW_YCBCR_IMAGE_PTR, IMAGE_SIZE_BYTES);
    handle_error(err);
}
```

```
/* Wait for decode completion */
jpeg_status_t status = (jpeg_status_t) 0;
while (!(status & JPEG_STATUS_OPERATION_COMPLETE))
{
    err = R_JPEG_StatusGet(&g_jpeg_ctrl, &status);
    handle_error(err);
}
}
```

### Streaming Encode Example

In this example the raw input data is provided in smaller chunks. This can help significantly reduce buffer size and improve throughput when streaming in raw data from an outside source.

```
/* Callback function for JPEG encode interrupts */
void jpeg_encode_callback (jpeg_callback_args_t * p_args)
{
    /* Get JPEG Codec status */
    g_jpeg_status = p_args->status;
    /* Set JPEG flag */
    jpeg_event = 1;
}

void jpeg_encode_streaming (void)
{
    uint8_t timeout = 0;
    uint8_t * p_chunk = (uint8_t *) RAW_YCBCR_IMAGE_PTR;
    fsp_err_t err;
    /* Open JPEG Codec */
    err = R_JPEG_Open(&g_jpeg_ctrl, &g_jpeg_cfg);
    /* Handle any errors. This function should be defined by the user. */
    handle_error(err);
    /* Set output buffer */
    err = R_JPEG_OutputBufferSet(&g_jpeg_ctrl, jpeg_buffer, sizeof(jpeg_buffer));
    handle_error(err);
    /* Set the image size */
```

```
jpeg_encode_image_size_t image_size;

image_size.horizontal_resolution    = X_RESOLUTION;
image_size.vertical_resolution      = Y_RESOLUTION;
image_size.horizontal_stride_pixels = H_STRIDE;
err = R_JPEG_EncodeImageSizeSet(&g_jpeg_ctrl, &image_size);
handle_error(err);

/* Calculate the size of the input data chunk (16 lines in this example) */
uint32_t chunk_size = H_STRIDE * 16U * YCBCR_BYTES_PER_PIXEL;

while (!timeout)
{
/* Set the input buffer */
    err = R_JPEG_InputBufferSet(&g_jpeg_ctrl, p_chunk, chunk_size);
    handle_error(err);

/* Wait for a callback */
    timeout = jpeg_event_wait();

if (g_jpeg_status & JPEG_STATUS_OPERATION_COMPLETE)
    {
/* Encode complete */
break;
    }

if (g_jpeg_status & JPEG_STATUS_INPUT_PAUSE)
    {
/* Load next block of input data here (if needed) */
        p_chunk += chunk_size;
    }
}
}
```

## Y'CbCr Conversion

The below function is provided as a reference for how to convert RGB values to Y'CbCr for use with the JPEG Codec.

### Note

*This function is only partially optimized for clarity. Further application-specific size- or speed-based optimizations should be considered when implementing in an actual project.*

```
#define RGB565_G_MASK 0x07E0
#define RGB565_B_MASK 0x001F
#define C_0 128
typedef enum e_pixel_format
{
    PIXEL_FORMAT_ARGB8888,
    PIXEL_FORMAT_RGB565
} pixel_format_t;
/* 5-bit to 8-bit LUT */
const uint8_t lut_32[] =
{
    0,  8,  16, 25, 33, 41, 49, 58,
    66, 74, 82, 90, 99, 107, 115, 123,
    132, 140, 148, 156, 165, 173, 181, 189,
    197, 206, 214, 222, 230, 239, 247, 255
};
/* 6-bit to 8-bit LUT */
const uint8_t lut_64[] =
{
    0,  4,  8,  12, 16, 20, 24, 28,
    32, 36, 40, 45, 49, 53, 57, 61,
    65, 69, 73, 77, 81, 85, 89, 93,
    97, 101, 105, 109, 113, 117, 121, 125,
    130, 134, 138, 142, 146, 150, 154, 158,
    162, 166, 170, 174, 178, 182, 186, 190,
    194, 198, 202, 206, 210, 215, 219, 223,
    227, 231, 235, 239, 243, 247, 251, 255
};
void bitmap_rgb2ycbcr(uint32_t * out, uint8_t * in, uint32_t len, pixel_format_t
format);
/*****
*****
* Convert an RGB buffer to Y'CbCr 4:2:2.
*

```

```
* NOTE: The width (in pixels) of the image to be converted must be divisible by 2.
*
* Parameters:
* out Pointer to output buffer
* in Pointer to input buffer
* len Length of input buffer (in pixels)
* format Input buffer format (ARGB8888 or RGB565)
*****
*****/
void bitmap_rgb2ycbcr (uint32_t * out, uint8_t * in, uint32_t len, pixel_format_t
format)
{
    uint16_t in0;
    uint16_t in1;
    uint32_t r0;
    uint32_t g0;
    uint32_t b0;
    uint32_t r1;
    uint32_t g1;
    uint32_t b1;
    uint8_t y0;
    uint8_t y1;
    uint8_t cb0;
    uint8_t cr0;
    uint8_t cb1;
    uint8_t cr1;

    /* Divide length by 2 as we're working with two pixels at a time */
    len >>= 1;

    /* Perform the conversion */
    while (len)
    {
        /* Get R, G and B channel values */
        if (format == PIXEL_FORMAT_RGB565)
        {
```



```
/* Get next two 16-bit values */
    in0 = *((uint16_t *) in);
    in += 2;
    in1 = *((uint16_t *) in);
    in += 2;

/* Decompose into individual channels */
    r0 = in0 >> 11;
    g0 = (in0 & RGB565_G_MASK) >> 5;
    b0 = in0 & RGB565_B_MASK;
    r1 = in1 >> 11;
    g1 = (in1 & RGB565_G_MASK) >> 5;
    b1 = in1 & RGB565_B_MASK;
}
else
{
/* Get each ARGB8888 channel in sequence, skipping alpha */
    b0 = *in++;
    g0 = *in++;
    r0 = *in++;
    in++;
    b1 = *in++;
    g1 = *in++;
    r1 = *in++;
    in++;
}

/* Convert RGB565 data to RGB888 */
if (PIXEL_FORMAT_RGB565 == format)
{
    r0 = lut_32[r0];
    g0 = lut_64[g0];
    b0 = lut_32[b0];
    r1 = lut_32[r1];
    g1 = lut_64[g1];
    b1 = lut_32[b1];
}
```

```

    }

    /* Calculate Y'CbCr 4:4:4 values for the two pixels */
    /* Algorithm based on method shown here: https://sistenix.com/rgb2ycbcr.html */
    /* Original coefficients from https://en.wikipedia.org/wiki/YCbCr#JPEG_conversion */
    y0 = (uint8_t) (((r0 << 6) + (r0 << 3) + (r0 << 2) + r0 +
                    (g0 << 7) + (g0 << 4) + (g0 << 2) + (g0 << 1) +
                    (b0 << 4) + (b0 << 3) + (b0 << 2) + b0
                    ) >> 8);

    cb0 = (uint8_t) (C_0 - (((r0 << 5) + (r0 << 3) + (r0 << 1) + r0 +
                            (g0 << 6) + (g0 << 4) + (g0 << 2) + g0 -
                            (b0 << 7)
                            ) >> 8));

    cr0 = (uint8_t) (C_0 + (((r0 << 7) -
                            (g0 << 6) - (g0 << 5) - (g0 << 3) - (g0 << 1) - g0 -
                            (b0 << 4) - (b0 << 2) - b0
                            ) >> 8));

    y1 = (uint8_t) (((r1 << 6) + (r1 << 3) + (r1 << 2) + r1 +
                    (g1 << 7) + (g1 << 4) + (g1 << 2) + (g1 << 1) +
                    (b1 << 4) + (b1 << 3) + (b1 << 2) + b1
                    ) >> 8);

    cb1 = (uint8_t) (C_0 - (((r1 << 5) + (r1 << 3) + (r1 << 1) + r1 +
                            (g1 << 6) + (g1 << 4) + (g1 << 2) + g1 -
                            (b1 << 7)
                            ) >> 8));

    cr1 = (uint8_t) (C_0 + (((r1 << 7) -
                            (g1 << 6) - (g1 << 5) - (g1 << 3) - (g1 << 1) - g1 -
                            (b1 << 4) - (b1 << 2) - b1
                            ) >> 8));

    /* The above code is based on the floating point method shown here: */
    // y0 = (uint8_t) ((0.299F * (float) r0) + (0.587F * (float) g0) + (0.114F * (float)
b0));
    // y1 = (uint8_t) ((0.299F * (float) r1) + (0.587F * (float) g1) + (0.114F * (float)
b1));
    // cb0 = (uint8_t) (128.0F - (0.168736F * (float) r0) - (0.331264F * (float) g0) +

```

```

(0.5F * (float) b0));
// cb1 = (uint8_t) (128.0F - (0.168736F * (float) r1) - (0.331264F * (float) g1) +
(0.5F * (float) b1));
// cr0 = (uint8_t) (128.0F + (0.5F * (float) r0) - (0.418688F * (float) g0) -
(0.081312F * (float) b0));
// cr1 = (uint8_t) (128.0F + (0.5F * (float) r1) - (0.418688F * (float) g1) -
(0.081312F * (float) b1));
/* NOTE: The JPEG Codec expects signed instead of unsigned chrominance values. */
/* Convert chrominance to -127..127 instead of 1..255 */
    cb0 = (uint8_t) ((int8_t) ((cb0 + cb1 + 1) >> 1) - C_0);
    cr0 = (uint8_t) ((int8_t) ((cr0 + cr1 + 1) >> 1) - C_0);
/* Convert the two 4:4:4 values into 4:2:2 by averaging the chroma, then write to
output */
    *out++ = (uint32_t) (y0 + (cb0 << 8) + (y1 << 16) + (cr0 << 24));
    len--;
}
}

```

## Data Structures

struct [jpeg\\_instance\\_ctrl\\_t](#)

## Data Structure Documentation

### ◆ jpeg\_instance\_ctrl\_t

struct jpeg_instance_ctrl_t		
JPEG Codec module control block. DO NOT INITIALIZE. Initialization occurs when jpeg_api_t::open is called.		
Data Fields		
uint32_t	open	JPEG Codec driver status.
<a href="#">jpeg_status_t</a>	status	JPEG Codec operational status.
<a href="#">fsp_err_t</a>	error_code	JPEG Codec error code (if any).
<a href="#">jpeg_mode_t</a>	mode	Current mode (decode or encode).
uint32_t	horizontal_stride_bytes	Horizontal Stride settings.
uint32_t	output_buffer_size	Output buffer size.
<a href="#">jpeg_cfg_t</a> const *	p_cfg	JPEG Decode configuration struct.

void const *	p_extend	JPEG Codec hardware dependent configuration */.
jpeg_decode_pixel_format_t	pixel_format	Pixel format.
uint16_t	total_lines_decoded	Track the number of lines decoded so far.
jpeg_decode_subsampling_t	horizontal_subsampling	Horizontal sub-sample setting.
uint16_t	lines_to_encode	Number of lines to encode.
uint16_t	vertical_resolution	vertical size
uint16_t	total_lines_encoded	Number of lines encoded.

## Function Documentation

### ◆ R\_JPEG\_Open()

```
fsp_err_t R_JPEG_Open ( jpeg_ctrl_t *const p_api_ctrl, jpeg_cfg_t const *const p_cfg )
```

Initialize the JPEG Codec module.

#### Note

*This function configures the JPEG Codec for operation and sets up the registers for data format and pixel format based on user-supplied configuration parameters. Interrupts are enabled to support callbacks.*

#### Return values

FSP_SUCCESS	JPEG Codec module is properly configured and is ready to take input data.
FSP_ERR_ALREADY_OPEN	JPEG Codec is already open.
FSP_ERR_ASSERTION	Pointer to the control block or the configuration structure is NULL.
FSP_ERR_IRQ_BSP_DISABLED	JEDI interrupt does not have an IRQ number.
FSP_ERR_INVALID_ARGUMENT	(Encode only) Quality factor, horizontal resolution and/or vertical resolution are invalid.
FSP_ERR_INVALID_ALIGNMENT	(Encode only) The horizontal resolution (at 16bpp) is not divisible by 8 bytes.

## ◆ R\_JPEG\_OutputBufferSet()

```
fsp_err_t R_JPEG_OutputBufferSet ( jpeg_ctrl_t * p_api_ctrl, void * p_output_buffer, uint32_t
output_buffer_size )
```

Assign a buffer to the JPEG Codec for storing output data.

### Note

*In Decode mode, the number of image lines to be decoded depends on the size of the buffer and the horizontal stride settings. Once the output buffer size is known, the horizontal stride value is known, and the input pixel format is known (the input pixel format is obtained by the JPEG decoder from the JPEG headers), the driver automatically computes the number of lines that can be decoded into the output buffer. After these lines are decoded, the JPEG engine pauses and a callback function is triggered, so the application is able to provide the next buffer for the JPEG module to resume the operation.*

The JPEG decoding operation automatically starts after both the input buffer and the output buffer are set and the output buffer is big enough to hold at least eight lines of decoded image data.

### Return values

FSP_SUCCESS	The output buffer is properly assigned to JPEG codec device.
FSP_ERR_ASSERTION	Pointer to the control block or output_buffer is NULL or output_buffer_size is 0.
FSP_ERR_INVALID_ALIGNMENT	Buffer starting address is not 8-byte aligned.
FSP_ERR_NOT_OPEN	JPEG not opened.
FSP_ERR_JPEG_UNSUPPORTED_IMAGE_SIZE	The number of horizontal pixels exceeds horizontal memory stride.
FSP_ERR_JPEG_BUFFERSIZE_NOT_ENOUGH	Invalid buffer size.
FSP_ERR_IN_USE	The output buffer cannot be changed during codec operation.

## ◆ R\_JPEG\_InputBufferSet()

```
fsp_err_t R_JPEG_InputBufferSet ( jpeg_ctrl_t *const p_api_ctrl, void * p_data_buffer, uint32_t data_buffer_size )
```

Assign an input data buffer to the JPEG codec for processing.

### Note

*After the amount of data is processed, the JPEG driver triggers a callback function with the flag JPEG\_PRV\_OPERATION\_INPUT\_PAUSE set. The application supplies the next chunk of data to the driver so processing can resume.*

*The JPEG decoding operation automatically starts after both the input buffer and the output buffer are set, and the output buffer is big enough to hold at least one line of decoded image data.*

If zero is provided for the decode data buffer size the JPEG Codec will never pause for more input data and will continue to read until either an image has been fully decoded or an error condition occurs.

### Note

*When encoding images the minimum data buffer size is 8 lines by 16 Y'CbCr 4:2:2 pixels (256 bytes). This corresponds to one minimum coded unit (MCU) of the resulting JPEG output.*

### Return values

FSP_SUCCESS	The input data buffer is properly assigned to JPEG Codec device.
FSP_ERR_ASSERTION	Pointer to the control block is NULL, or the pointer to the input_buffer is NULL, or the input_buffer_size is 0.
FSP_ERR_INVALID_ALIGNMENT	Buffer starting address is not 8-byte aligned.
FSP_ERR_NOT_OPEN	JPEG not opened.
FSP_ERR_IN_USE	The input buffer cannot be changed while the codec is running.
FSP_ERR_INVALID_CALL	In encode mode the output buffer must be set first.
FSP_ERR_JPEG_IMAGE_SIZE_ERROR	The buffer size is smaller than the minimum coded unit (MCU).

◆ **R\_JPEG\_StatusGet()**

```
fsp_err_t R_JPEG_StatusGet ( jpeg_ctrl_t* p_api_ctrl, jpeg_status_t* p_status )
```

Get the status of the JPEG codec. This function can also be used to poll the device.

**Return values**

FSP_SUCCESS	The status information is successfully retrieved.
FSP_ERR_ASSERTION	Pointer to the control block or p_status is NULL.
FSP_ERR_NOT_OPEN	JPEG is not opened.

◆ **R\_JPEG\_Close()**

```
fsp_err_t R_JPEG_Close ( jpeg_ctrl_t* p_api_ctrl)
```

Cancel an outstanding JPEG codec operation and close the device.

**Return values**

FSP_SUCCESS	The input data buffer is properly assigned to JPEG Codec device.
FSP_ERR_ASSERTION	Pointer to the control block is NULL.
FSP_ERR_NOT_OPEN	JPEG not opened.

◆ **R\_JPEG\_VersionGet()**

```
fsp_err_t R_JPEG_VersionGet ( fsp_version_t* p_version)
```

Get the version of the JPEG Codec driver.

**Return values**

FSP_SUCCESS	Version number returned successfully.
FSP_ERR_ASSERTION	The parameter p_version is NULL.

## ◆ R\_JPEG\_EncodeImageSizeSet()

```
fsp_err_t R_JPEG_EncodeImageSizeSet ( jpeg_ctrl_t *const p_api_ctrl, jpeg_encode_image_size_t *
p_image_size )
```

Set the image dimensions for an encode operation.

**Note**

*Image dimensions must be set before setting the input buffer.*

**Return values**

FSP_SUCCESS	Image size was successfully written to the JPEG Codec.
FSP_ERR_ASSERTION	Pointer to the control block or p_image_size is NULL.
FSP_ERR_INVALID_ALIGNMENT	Horizontal stride is not 8-byte aligned.
FSP_ERR_INVALID_ARGUMENT	Horizontal or vertical resolution is invalid or zero.
FSP_ERR_NOT_OPEN	JPEG not opened.
FSP_ERR_IN_USE	Image parameters cannot be changed while the codec is running.

## ◆ R\_JPEG\_DecodeLinesDecodedGet()

```
fsp_err_t R_JPEG_DecodeLinesDecodedGet ( jpeg_ctrl_t * p_api_ctrl, uint32_t * p_lines )
```

Returns the number of lines decoded into the output buffer.

**Note**

*Use this function to retrieve the number of image lines written to the output buffer after a partial decode operation. Combined with the horizontal stride settings and the output pixel format the application can compute the amount of data to read from the output buffer.*

**Return values**

FSP_SUCCESS	Line count successfully returned.
FSP_ERR_ASSERTION	Pointer to the control block or p_lines is NULL.
FSP_ERR_NOT_OPEN	JPEG not opened.



### ◆ R\_JPEG\_DeCodeHorizontalStrideSet()

```
fsp_err_t R_JPEG_DeCodeHorizontalStrideSet ( jpeg_ctrl_t * p_api_ctrl, uint32_t horizontal_stride )
```

Configure horizontal stride setting for decode operations.

#### Note

*If the image size is known prior to the open call and/or the output buffer stride is constant, pass the horizontal stride value in the `jpeg_cfg_t` structure. Otherwise, after the image size becomes available use this function to set the output buffer horizontal stride value.*

#### Return values

FSP_SUCCESS	Horizontal stride value is properly configured.
FSP_ERR_ASSERTION	Pointer to the control block is NULL.
FSP_ERR_INVALID_ALIGNMENT	Horizontal stride is zero or is not 8-byte aligned.
FSP_ERR_NOT_OPEN	JPEG not opened.

### ◆ R\_JPEG\_DeCodeImageSizeGet()

```
fsp_err_t R_JPEG_DeCodeImageSizeGet ( jpeg_ctrl_t * p_api_ctrl, uint16_t * p_horizontal_size, uint16_t * p_vertical_size )
```

Obtain the size of an image being decoded.

#### Return values

FSP_SUCCESS	The image size is available and the horizontal and vertical values are stored in the memory pointed to by <code>p_horizontal_size</code> and <code>p_vertical_size</code> .
FSP_ERR_ASSERTION	Pointer to the control block is NULL and/or size is not ready.
FSP_ERR_NOT_OPEN	JPEG is not opened.

◆ **R\_JPEG\_DecodeImageSubsampleSet()**

```
fsp_err_t R_JPEG_DecodeImageSubsampleSet ( jpeg_ctrl_t *const p_api_ctrl,
jpeg_decode_subsample_t horizontal_subsample, jpeg_decode_subsample_t vertical_subsample )
```

Configure horizontal and vertical subsampling.

**Note**

*This function can be used to scale the output of decoded image data.*

**Return values**

FSP_SUCCESS	Horizontal stride value is properly configured.
FSP_ERR_ASSERTION	Pointer to the control block is NULL.
FSP_ERR_NOT_OPEN	JPEG not opened.

◆ **R\_JPEG\_DecodePixelFormatGet()**

```
fsp_err_t R_JPEG_DecodePixelFormatGet ( jpeg_ctrl_t * p_api_ctrl, jpeg_color_space_t *
p_color_space )
```

Get the color format of the JPEG being decoded.

**Return values**

FSP_SUCCESS	The color format was successfully retrieved.
FSP_ERR_ASSERTION	Pointer to the control block is NULL.
FSP_ERR_NOT_OPEN	JPEG is not opened.

**◆ R\_JPEG\_ModeSet()**

```
fsp_err_t R_JPEG_ModeSet ( jpeg_ctrl_t *const p_api_ctrl, jpeg_mode_t mode )
```

Switch between encode and decode mode (or vice-versa).

**Note**

*The codec must not be idle in order to switch modes.*

**Return values**

FSP_SUCCESS	Mode changed successfully.
FSP_ERR_ASSERTION	p_api_ctrl is NULL.
FSP_ERR_NOT_OPEN	Module is not open.
FSP_ERR_IN_USE	JPEG Codec is currently in use.
FSP_ERR_INVALID_ARGUMENT	(Encode only) Quality factor, horizontal resolution and/or vertical resolution are invalid.
FSP_ERR_INVALID_ALIGNMENT	(Encode only) The horizontal resolution (at 16bpp) is not divisible by 8 bytes.

**4.2.31 Key Interrupt (r\_kint)**

## Modules

**Functions**

```
fsp_err_t R_KINT_Open (keymatrix_ctrl_t *const p_api_ctrl, keymatrix_cfg_t
const *const p_cfg)
```

```
fsp_err_t R_KINT_Enable (keymatrix_ctrl_t *const p_api_ctrl)
```

```
fsp_err_t R_KINT_Disable (keymatrix_ctrl_t *const p_api_ctrl)
```

```
fsp_err_t R_KINT_Close (keymatrix_ctrl_t *const p_api_ctrl)
```

```
fsp_err_t R_KINT_VersionGet (fsp_version_t *const p_version)
```

**Detailed Description**

Driver for the KINT peripheral on RA MCUs. This module implements the [Key Matrix Interface](#).

**Overview**

The KINT module configures the Key Interrupt (KINT) peripheral to detect rising or falling edges on

any of the KINT channels. When such an event is detected on any of the configured pins, the module generates an interrupt.

## Features

- Detect rising or falling edges on KINT channels
- Callback for notifying the application when edges are detected on the configured channels

## Configuration

### Build Time Configurations for r\_kint

The following build time configurations are defined in fsp\_cfg/r\_kint\_cfg.h:

Configuration	Options	Default	Description
Parameter Checking	<ul style="list-style-type: none"> <li>• Default (BSP)</li> <li>• Enabled</li> <li>• Disabled</li> </ul>	Default (BSP)	If selected code for parameter checking is included in the build.

### Configurations for Driver > Input > Key Matrix Driver on r\_kint

This module can be added to the Stacks tab via New Stack > Driver > Input > Key Matrix Driver on r\_kint.

Configuration	Options	Default	Description
General > Name	Name must be a valid C symbol	g_kint0	Module name.
Input > Key Interrupt Flag Mask	<ul style="list-style-type: none"> <li>• Channel 0</li> <li>• Channel 1</li> <li>• Channel 2</li> <li>• Channel 3</li> <li>• Channel 4</li> <li>• Channel 5</li> <li>• Channel 6</li> <li>• Channel 7</li> </ul>		Select channels to enable.
Interrupts > Trigger Type	<ul style="list-style-type: none"> <li>• Falling Edge</li> <li>• Rising Edge</li> </ul>	Rising Edge	Specifies if the enabled channels detect a rising edge or a falling edge. NOTE: either all channels detecting a rising edge or all channels detecting a falling edge.
Interrupts > Callback	Name must be a valid C symbol	kint_callback	A user callback function can be provided. If this callback function is provided, it will be called from the

interrupt service routine (ISR) each time the IRQ triggers.

Select the key interrupt priority.

Interrupts > Key  
Interrupt Priority

MCU Specific Options

## Clock Configuration

The KINT peripheral runs on PCLKB.

## Pin Configuration

The KRn pins are key switch matrix row input pins.

# Usage Notes

## Connecting a Switch Matrix

The KINT module is designed to scan the rows of a switch matrix where each row is connected to a number of columns through switches. A periodic timer (or other mechanism) sets one column pin high at a time. Any switches that are pressed on the driven column cause a rising (or falling) edge on the row pin (KRn) causing an interrupt.

### Note

*In applications where multiple keys may be pressed at the same time it is recommended to put a diode inline with each switch to prevent ghosting.*

## Handling Multiple Pins

When an edge is detected on multiple pins at the same time, a single IRQ will be generated. A mask of all the pins that detected an edge will be passed to the callback.

# Examples

## Basic Example

This is a basic example of minimal use of the KINT in an application.

```
static volatile uint32_t g_channel_mask;
static volatile uint32_t g_kint_edge_detected = 0U;
/* Called from key_int_isr */
void r_kint_callback (keymatrix_callback_args_t * p_args)
{
    g_channel_mask      = p_args->channel_mask;
    g_kint_edge_detected = 1U;
}
void r_kint_example ()
```

```

{
/* Configure the KINT. */
fsp_err_t err = R_KINT_Open(&g_kint_ctrl, &g_kint_cfg);
/* Handle any errors. This function should be defined by the user. */
    handle_error(err);
/* Enable the KINT. */
    err = R_KINT_Enable(&g_kint_ctrl);
    handle_error(err);
while (0 == g_kint_edge_detected)
    {
/* Wait for interrupt. */
    }
}

```

## Data Structures

struct [kint\\_instance\\_ctrl\\_t](#)

## Data Structure Documentation

### ◆ kint\_instance\_ctrl\_t

struct [kint\\_instance\\_ctrl\\_t](#)

Channel instance control block. DO NOT INITIALIZE. Initialization occurs when [keymatrix\\_api\\_t::open](#) is called.

## Function Documentation

### ◆ R\_KINT\_Open()

[fsp\\_err\\_t](#) R\_KINT\_Open ( [keymatrix\\_ctrl\\_t](#)\*const *p\_api\_ctrl*, [keymatrix\\_cfg\\_t](#) const \*const *p\_cfg* )

Configure all the Key Input (KINT) channels and provides a handle for use with the rest of the KINT API functions. Implements [keymatrix\\_api\\_t::open](#).

#### Return values

FSP_SUCCESS	Initialization was successful.
FSP_ERR_ASSERTION	One of the following parameters may be NULL: <i>p_cfg</i> , or <i>p_ctrl</i> or the callback.
FSP_ERR_ALREADY_OPEN	The module has already been opened.
FSP_ERR_IP_CHANNEL_NOT_PRESENT	The channel mask is invalid.

◆ **R\_KINT\_Enable()**

```
fsp_err_t R_KINT_Enable ( keymatrix_ctrl_t *const p_api_ctrl)
```

This function enables interrupts for the KINT peripheral after clearing any pending requests. Implements [keymatrix\\_api\\_t::enable](#).

**Return values**

FSP_SUCCESS	Interrupt disabled successfully.
FSP_ERR_ASSERTION	The p_ctrl parameter was null.
FSP_ERR_NOT_OPEN	The peripheral is not opened.

◆ **R\_KINT\_Disable()**

```
fsp_err_t R_KINT_Disable ( keymatrix_ctrl_t *const p_api_ctrl)
```

This function disables interrupts for the KINT peripheral. Implements [keymatrix\\_api\\_t::disable](#).

**Return values**

FSP_SUCCESS	Interrupt disabled successfully.
FSP_ERR_ASSERTION	The p_ctrl parameter was null.
FSP_ERR_NOT_OPEN	The channel is not opened.

◆ **R\_KINT\_Close()**

```
fsp_err_t R_KINT_Close ( keymatrix_ctrl_t *const p_api_ctrl)
```

Clear the KINT configuration and disable the KINT IRQ. Implements [keymatrix\\_api\\_t::close](#).

**Return values**

FSP_SUCCESS	Successful close.
FSP_ERR_ASSERTION	The parameter p_ctrl is NULL.
FSP_ERR_NOT_OPEN	The module is not opened.

**◆ R\_KINT\_VersionGet()**

```
fsp_err_t R_KINT_VersionGet ( fsp_version_t *const p_version)
```

Set driver version based on compile time macros.

**Return values**

FSP_SUCCESS	Successful return.
FSP_ERR_ASSERTION	The parameter p_version is NULL.

**4.2.32 Low Power Modes (r\_lpm)**

## Modules

**Functions**

```
fsp_err_t R_LPM_Open (lpm_ctrl_t *const p_api_ctrl, lpm_cfg_t const *const p_cfg)
```

```
fsp_err_t R_LPM_Close (lpm_ctrl_t *const p_api_ctrl)
```

```
fsp_err_t R_LPM_LowPowerReconfigure (lpm_ctrl_t *const p_api_ctrl, lpm_cfg_t const *const p_cfg)
```

```
fsp_err_t R_LPM_LowPowerModeEnter (lpm_ctrl_t *const p_api_ctrl)
```

```
fsp_err_t R_LPM_VersionGet (fsp_version_t *const p_version)
```

```
fsp_err_t R_LPM_IoKeepClear (lpm_ctrl_t *const p_api_ctrl)
```

**Detailed Description**

Driver for the LPM peripheral on RA MCUs. This module implements the [Low Power Modes Interface](#).

**Overview**

The low power modes driver is used to configure and place the device into the desired low power mode. Various sources can be configured to wake from standby, request snooze mode, end snooze mode or end deep standby mode.

**Features**

The LPM HAL module has the following key features:



- Supports the following low power modes:
  - Deep Software Standby mode (On supported MCUs)
  - Software Standby mode
  - Sleep mode
  - Snooze mode
- Supports reducing power consumption when in deep software standby mode through internal power supply control and by resetting the states of I/O ports.
- Supports disabling and enabling the MCU's other hardware peripherals

## Configuration

### Build Time Configurations for r\_lpm

The following build time configurations are defined in fsp\_cfg/r\_lpm\_cfg.h:

Configuration	Options	Default	Description
Parameter Checking	<ul style="list-style-type: none"> <li>• Default (BSP)</li> <li>• Enabled</li> <li>• Disabled</li> </ul>	Default (BSP)	If selected code for parameter checking is included in the build.

### Configurations for Driver > Power > Low Power Modes Driver on r\_lpm

This module can be added to the Stacks tab via New Stack > Driver > Power > Low Power Modes Driver on r\_lpm. Non-secure callable guard functions can be generated for this module by right clicking the module in the RA Configuration tool and checking the "Non-secure Callable" box.

Configuration	Options	Default	Description
General > Name	Name must be a valid C symbol	g_lpm0	Module name.
General > Low Power Mode	MCU Specific Options		Power mode to be entered.
General > Output port state in standby and deep standby	MCU Specific Options		Select the state of output pins during standby. Applies to address output, data output, and other bus control output pins.
Standby Options > Wake Sources	MCU Specific Options		Enable wake from standby from these Sources.
Standby Options > Snooze Request Source	MCU Specific Options		Select the event that will enter snooze.
Standby Options > Snooze End Sources	MCU Specific Options		Enable wake from snooze from these sources.
Standby Options > DTC state in Snooze Mode	<ul style="list-style-type: none"> <li>• Disabled</li> <li>• Enabled</li> </ul>	Disabled	Enable wake from snooze from this source.

Standby Options > Snooze Cancel Source	MCU Specific Options	Select an interrupt source to cancel snooze.
Deep Standby Options > > I/O Port Retention	MCU Specific Options	Select the state of the IO Pins after exiting deep standby mode.
Deep Standby Options > > Power-Supply Control	MCU Specific Options	Select the state of the internal power supply in deep standby mode.
Deep Standby Options > > Cancel Sources	MCU Specific Options	Enable wake from deep standby using these sources.
Deep Standby Options > > Cancel Edges	MCU Specific Options	Falling edge trigger is default. Select sources to enable wake from deep standby with rising edge.

## Clock Configuration

This module does not have any selectable clock sources.

## Pin Configuration

This module does not use I/O pins.

# Usage Notes

## Sleep Mode

At power on, by default sleep is set as the low-power mode. Sleep mode is the most convenient low-power mode available, as it does not require any special configuration (other than configuring and enabling a suitable interrupt or event to wake the MCU from sleep) to return to normal program-execution mode. The states of the SRAM, the processor registers, and the hardware peripherals are all maintained in sleep mode, and the time needed to enter and wake from sleep is minimal. Any interrupt causes the MCU device to wake from sleep mode, including the SysTick interrupt used by the RTOS scheduler.

## Software Standby Mode

In software-standby mode, the CPU, as well as most of the on-chip peripheral functions and all of the internal oscillators, are stopped. The contents of the CPU internal registers and SRAM data, the states of on-chip peripheral functions, and I/O Ports are all retained. Software-standby mode allows significant reduction in power consumption, because most of the oscillators are stopped in this mode. Like sleep mode, standby mode requires an interrupt or event be configured and enabled to wake up.

## Snooze Mode

Snooze mode can be used with some MCU peripherals to execute basic tasks while keeping the MCU

in a low-power state. Many core peripherals and all clocks can be selected to run during Snooze, allowing for more flexible low-power configuration than Software Standby mode. To enable Snooze, select "Software Standby mode with Snooze mode enabled" for the "Low Power Mode" configuration option. Snooze mode settings (including entry/exit sources) are available under "Standby Options".

## Deep Software Standby Mode

Deep Software Standby Mode is only available on some MCU devices. The MCU always wakes from Deep Software Standby Mode by going through reset, either by the negation of the reset pin or by one of the wakeup sources configurable in the "Deep Standby Options" configuration group.

The Reset Status Registers can be used to determine if the reset occurred after coming out of deep software standby. For example, `R_SYSTEM->RSTSR0_b.DPSRSTF` is set to 1 after a deep software standby reset.

I/O Port Retention can be enabled to maintain I/O port configuration across a deep software standby reset. Retention can be cancelled through the [R\\_LPM\\_IoKeepClear](#) API.

## Limitations

Developers should be aware of the following limitations when using the LPM:

- Flash stop (code flash disable) is not supported. See the section "Flash Operation Control Register (FLSTOP)" of the RA2/RA4 Family Hardware User's Manual.
- Reduced SRAM retention area in software standby mode is not supported. See the section "Power Save Memory Control Register (PSMCR)" of the RA4 Hardware User's Manual.
- Only one Snooze Request Source can be used at a time.
- When using Snooze mode with SCI0 RXD as the snooze source the system clock must be HOCO and the MOCO, Main Oscillator and PLL clocks must be turned off.
- If the main oscillator or PLL with main oscillator source is used for the system clock, the wake time from standby mode can be affected by the Main Oscillator Wait Time Setting in the MOSCWTCR register. This register setting is available to be changed through the Main Oscillator Wait Time setting in the CGC module properties. See the "Wakeup Timing and Duration" table in Electrical Characteristics for more information.

## Examples

### LPM Sleep Example

This is a basic example of minimal use of the LPM in an application. The LPM instance is opened and the configured low-power mode is entered.

```
void r_lpm_sleep (void)
{
    fsp_err_t err = R_LPM_Open(&g_lpm_ctrl, &g_lpm_cfg_sleep);
    /* Handle any errors. This function should be defined by the user. */
    handle_error(err);
    err = R_LPM_LowPowerModeEnter(&g_lpm_ctrl);
    handle_error(err);
}
```

## LPM Deep Software Standby Example

```
void r_lpm_deep_software_standby (void)
{
    fsp_err_t err;

    err = R_LPM_Open(&g_lpm_ctrl, &g_lpm_cfg_deep_software_standby);
    /* Handle any errors. This function should be defined by the user. */
    handle_error(err);

    /* Check the Deep Software Standby Reset Flag. */
    if (1U == R_SYSTEM->RSTSR0_b.DPSRSTF)
    {
        /* Clear the IOKEEP bit to allow I/O Port use. */
        err = R_LPM_IoKeepClear(&g_lpm_ctrl);
        handle_error(err);
    }

    /* Add user code here. */

    /* Reconfigure the module to set the IOKEEP bit before entering deep software
standby. */
    err = R_LPM_LowPowerReconfigure(&g_lpm_ctrl, &g_lpm_cfg_deep_software_standby);
    handle_error(err);

    err = R_LPM_LowPowerModeEnter(&g_lpm_ctrl);

    /* Code after R_LPM_LowPowerModeEnter when using Deep Software Standby never be
executed.

    * Deep software standby exits by resetting the MCU. */
    handle_error(err);
}
```

## Data Structures

```
struct lpm_instance_ctrl_t
```

## Data Structure Documentation

### ◆ lpm\_instance\_ctrl\_t

```
struct lpm_instance_ctrl_t
```

LPM private control block. DO NOT MODIFY. Initialization occurs when [R\\_LPM\\_Open\(\)](#) is called.

## Function Documentation

### ◆ R\_LPM\_Open()

```
fsp_err_t R_LPM_Open ( lpm_ctrl_t *const p_api_ctrl, lpm_cfg_t const *const p_cfg )
```

Perform any necessary initialization

#### Return values

FSP_SUCCESS	LPM instance opened
FSP_ERR_ASSERTION	Null Pointer
FSP_ERR_ALREADY_OPEN	LPM instance is already open
FSP_ERR_UNSUPPORTED	This MCU does not support Deep Software Standby
FSP_ERR_INVALID_ARGUMENT	One of the following: <ul style="list-style-type: none"> <li>• Invalid snooze entry source</li> <li>• Invalid snooze end sources</li> </ul>
FSP_ERR_INVALID_MODE	One of the following: <ul style="list-style-type: none"> <li>• Invalid low power mode</li> <li>• Invalid DTC option for snooze mode</li> <li>• Invalid deep standby end sources</li> <li>• Invalid deep standby end sources edges</li> <li>• Invalid power supply option for deep standby</li> <li>• Invalid IO port option for deep standby</li> <li>• Invalid output port state setting for standby or deep standby</li> <li>• Invalid sources for wake from standby mode</li> <li>• Invalid power supply option for standby</li> <li>• Invalid IO port option for standby</li> <li>• Invalid standby end sources</li> <li>• Invalid standby end sources edges</li> </ul>

**◆ R\_LPM\_Close()**`fsp_err_t R_LPM_Close ( lpm_ctrl_t *const p_api_ctrl)`

Close the LPM Instance

**Return values**

FSP_SUCCESS	LPM Software lock initialized
FSP_ERR_NOT_OPEN	LPM instance is not open
FSP_ERR_ASSERTION	Null Pointer

### ◆ R\_LPM\_LowPowerReconfigure()

```
fsp_err_t R_LPM_LowPowerReconfigure ( lpm_ctrl_t *const p_api_ctrl, lpm_cfg_t const *const p_cfg )
```

Configure a low power mode

NOTE: This function does not enter the low power mode, it only configures parameters of the mode. Execution of the WFI instruction is what causes the low power mode to be entered.

#### Return values

FSP_SUCCESS	Low power mode successfully applied
FSP_ERR_ASSERTION	Null Pointer
FSP_ERR_NOT_OPEN	LPM instance is not open
FSP_ERR_UNSUPPORTED	This MCU does not support Deep Software Standby
FSP_ERR_INVALID_ARGUMENT	One of the following: <ul style="list-style-type: none"> <li>Invalid snooze entry source</li> <li>Invalid snooze end sources</li> </ul>
FSP_ERR_INVALID_MODE	One of the following: <ul style="list-style-type: none"> <li>Invalid low power mode</li> <li>Invalid DTC option for snooze mode</li> <li>Invalid deep standby end sources</li> <li>Invalid deep standby end sources edges</li> <li>Invalid power supply option for deep standby</li> <li>Invalid IO port option for deep standby</li> <li>Invalid output port state setting for standby or deep standby</li> <li>Invalid sources for wake from standby mode</li> <li>Invalid power supply option for standby</li> <li>Invalid IO port option for standby</li> <li>Invalid standby end sources</li> <li>Invalid standby end sources edges</li> </ul>

◆ **R\_LPM\_LowPowerModeEnter()**

```
fsp_err_t R_LPM_LowPowerModeEnter ( lpm_ctrl_t *const p_api_ctrl)
```

Enter low power mode (sleep/standby/deep standby) using WFI macro.

Function will return after waking from low power mode.

**Return values**

FSP_SUCCESS	Successful.
FSP_ERR_ASSERTION	Null pointer.
FSP_ERR_NOT_OPEN	LPM instance is not open
FSP_ERR_INVALID_MODE	One of the following: <ul style="list-style-type: none"> <li>• HOCO was not system clock when using snooze mode with SCIO/RXD0.</li> <li>• HOCO was not stable when using snooze mode with SCIO/RXD0.</li> <li>• MOCO was running when using snooze mode with SCIO/RXD0.</li> <li>• MAIN OSCILLATOR was running when using snooze mode with SCIO/RXD0.</li> <li>• PLL was running when using snooze mode with SCIO/RXD0.</li> <li>• Unable to disable oscillator stop detect when using standby or deep standby.</li> </ul>

◆ **R\_LPM\_VersionGet()**

```
fsp_err_t R_LPM_VersionGet ( fsp_version_t *const p_version)
```

Get the driver version based on compile time macros.

**Return values**

FSP_SUCCESS	Successful close.
FSP_ERR_ASSERTION	p_version is NULL.



**◆ R\_LPM\_IoKeepClear()**

```
fsp_err_t R_LPM_IoKeepClear ( lpm_ctrl_t *const p_api_ctrl)
```

Clear the IOKEEP bit after deep software standby

**Return values**

FSP_SUCCESS	DPSBYCR_b.IOKEEP bit cleared Successfully.
FSP_ERR_UNSUPPORTED	Deep standby mode not supported on this MCU.

**4.2.33 Low Voltage Detection (r\_lvd)**

## Modules

**Functions**

```
fsp_err_t R_LVD_Open (lvd_ctrl_t *const p_api_ctrl, lvd_cfg_t const *const p_cfg)
```

```
fsp_err_t R_LVD_Close (lvd_ctrl_t *const p_api_ctrl)
```

```
fsp_err_t R_LVD_StatusGet (lvd_ctrl_t *const p_api_ctrl, lvd_status_t *p_lvd_status)
```

```
fsp_err_t R_LVD_StatusClear (lvd_ctrl_t *const p_api_ctrl)
```

```
fsp_err_t R_LVD_VersionGet (fsp_version_t *const p_version)
```

```
fsp_err_t R_LVD_CallbackSet (lvd_ctrl_t *const p_api_ctrl, void(*p_callback)(lvd_callback_args_t *), void const *const p_context, lvd_callback_args_t *const p_callback_memory)
```

**Detailed Description**

Driver for the LVD peripheral on RA MCUs. This module implements the [Low Voltage Detection Interface](#).

**Overview**

The Low Voltage Detection module configures the voltage monitors to detect when  $V_{CC}$  crosses a specified threshold.

**Features**

The LVD HAL module supports the following functions:

- Two run-time configurable voltage monitors (Voltage Monitor 1, Voltage Monitor 2)
  - Configurable voltage threshold
  - Digital filter (Available on specific MCUs)
  - Support for both interrupt or polling
    - NMI or maskable interrupt can be configured
  - Rising, falling, or both edge event detection
  - Support for resetting the MCU when  $V_{CC}$  falls below configured threshold.

## Configuration

### Build Time Configurations for r\_lvd

The following build time configurations are defined in fsp\_cfg/r\_lvd\_cfg.h:

Configuration	Options	Default	Description
Parameter Checking	<ul style="list-style-type: none"> <li>• Default (BSP)</li> <li>• Enabled</li> <li>• Disabled</li> </ul>	Default (BSP)	If selected code for parameter checking is included in the build.

### Configurations for Driver > Power > Low Voltage Detection Driver on r\_lvd

This module can be added to the Stacks tab via New Stack > Driver > Power > Low Voltage Detection Driver on r\_lvd. Non-secure callable guard functions can be generated for this module by right clicking the module in the RA Configuration tool and checking the "Non-secure Callable" box.

Configuration	Options	Default	Description
Name	Name must be a valid C symbol	g_lvd	Module name.
Monitor Number	MCU Specific Options		Select the LVD monitor.
Digital Filter	MCU Specific Options		Enable the digital filter and select the digital filter clock divider.
Voltage Threshold	MCU Specific Options		Select the low voltage detection threshold.
Detection Response	<ul style="list-style-type: none"> <li>• Maskable interrupt</li> <li>• Non-maskable interrupt</li> <li>• Reset MCU (Only available for falling edge)</li> <li>• No response (Voltage monitor status will be polled)</li> </ul>	No response (Voltage monitor status will be polled)	Select what happens when the voltage crosses the threshold voltage.
Voltage Slope	<ul style="list-style-type: none"> <li>• Falling voltage</li> </ul>	Falling voltage	Select detection on

	<ul style="list-style-type: none"> <li>• Rising voltage</li> <li>• Rising or falling voltage</li> </ul>		rising voltage, falling voltage or both.
Negation Delay	<ul style="list-style-type: none"> <li>• Delay from reset</li> <li>• Delay from voltage returning to normal range</li> </ul>	Delay from reset	Negation of the monitor signal can either be delayed from the reset event or from voltage returning to normal range.
Monitor Interrupt Callback	Name must be a valid C symbol.	NULL	A user callback function can be provided. If this callback function is provided, it will be called from the interrupt service routine (ISR) each time the IRQ triggers.
LVD Monitor Interrupt Priority	MCU Specific Options		Select the LVD Monitor interrupt priority.

## Clock Configuration

The LOCO clock must be enabled in order to use the digital filter.

## Pin Configuration

This module does not use I/O pins.

## Usage Notes

### Startup Edge Detection

If  $V_{CC}$  is below the threshold prior to configuring the voltage monitor for falling edge detection, the monitor will immediately detect the a falling edge condition. If  $V_{CC}$  is above the threshold prior to configuring the monitor for rising edge detection, the monitor will not detect a rising edge condition until  $V_{CC}$  falls below the threshold and then rises above it again.

### Voltage Monitor 0

The LVD HAL module only supports configuring voltage monitor 1 and voltage monitor 2. Voltage monitor 0 can be configured by setting the appropriate bits in the OFS1 register. This means that voltage monitor 0 settings cannot be changed at runtime.

Voltage monitor 0 supports the following features

- Configurable Voltage Threshold ( $V_{DET0}$ )
- Reset the device when  $V_{CC}$  falls below  $V_{DET0}$

### Limitations

- The digital filter must be disabled when using voltage monitors in Software Standby or Deep Software Standby.

- Deep Software Standby mode is not possible if the voltage monitor is configured to reset the MCU.
- When the detection response is set to reset, only voltage falling edge detection is possible.

## Examples

### Basic Example

This is a basic example of minimal use of the LVD in an application.

```
void basic_example (void)
{
    fsp_err_t err = R_LVD_Open(&g_lvd_ctrl, &g_lvd_cfg);
    handle_error(err);
    while (1)
    {
        lvd_status_t status;
        err = R_LVD_StatusGet(&g_lvd_ctrl, &status);
        handle_error(err);
        if (LVD_THRESHOLD_CROSSING_DETECTED == status.crossing_detected)
        {
            err = R_LVD_StatusClear(&g_lvd_ctrl);
            handle_error(err);
            /* Do something */
        }
    }
}
```

### Interrupt Example

This is a basic example of using a LVD instance that is configured to generate an interrupt.

```
void interrupt_example (void)
{
    fsp_err_t err = R_LVD_Open(&g_lvd_ctrl, &g_lvd_cfg);
    /* Handle any errors. This function should be defined by the user. */
    handle_error(err);
    while (1)
```

```
{
/* Application Process */
/* Application will be interrupted when Vcc crosses the configured threshold. */
}
}
/* Called when Vcc crosses configured threshold. */
void lvd_callback (lvd_callback_args_t * p_args)
{
if (LVD_CURRENT_STATE_BELOW_THRESHOLD == p_args->current_state)
{
/* Do Something */
}
}
```

## Reset Example

This is a basic example of using a LVD instance that is configured to reset the MCU.

```
void reset_example (void)
{
if (1U == R_SYSTEM->RSTSR0_b.LVD1RF)
{
/* The system is coming out of reset because Vcc crossed configured voltage
threshold. */
/* Clear Voltage Monitor 1 Reset Detect Flag. */
R_SYSTEM->RSTSR0_b.LVD1RF = 0;
}
fsp_err_t err = R_LVD_Open(&g_lvd_ctrl, &g_lvd_cfg);
/* Handle any errors. This function should be defined by the user. */
handle_error(err);
while (1)
{
/* Application Process */
/* Application will reset when Vcc crosses the configured threshold. */
}
```

}

## Data Structures

```
struct lvd_instance_ctrl_t
```

## Data Structure Documentation

### ◆ lvd\_instance\_ctrl\_t

```
struct lvd_instance_ctrl_t
```

LVD instance control structure

## Function Documentation

### ◆ R\_LVD\_Open()

```
fsp_err_t R_LVD_Open ( lvd_ctrl_t *const p_api_ctrl, lvd_cfg_t const *const p_cfg )
```

Initializes a voltage monitor and detector according to the passed-in configuration structure.

#### Parameters

[in]	p_api_ctrl	Pointer to the control structure for the driver instance
[in]	p_cfg	Pointer to the configuration structure for the driver instance

#### Note

Digital filter is not to be used with standby modes.

Startup time can take on the order of milliseconds for some configurations.

Example:

```
fsp_err_t err = R_LVD_Open(&g_lvd_ctrl, &g_lvd_cfg);
```

#### Return values

FSP_SUCCESS	Successful
FSP_ERR_ASSERTION	Requested configuration was invalid
FSP_ERR_ALREADY_OPEN	The instance was already opened
FSP_ERR_IN_USE	Another instance is already using the desired monitor
FSP_ERR_UNSUPPORTED	Digital filter was enabled on a device that does not support it

◆ **R\_LVD\_Close()**

```
fsp_err_t R_LVD_Close ( lvd_ctrl_t *const p_api_ctrl)
```

Disables the LVD peripheral. Closes the driver instance.

**Parameters**

[in]	p_api_ctrl	Pointer to the control block structure for the driver instance
------	------------	----------------------------------------------------------------

**Return values**

FSP_SUCCESS	Successful
FSP_ERR_ASSERTION	An argument was NULL
FSP_ERR_NOT_OPEN	Driver is not open

◆ **R\_LVD\_StatusGet()**

```
fsp_err_t R_LVD_StatusGet ( lvd_ctrl_t *const p_api_ctrl, lvd_status_t * p_lvd_status )
```

Get the current state of the monitor (threshold crossing detected, voltage currently above or below threshold).

**Parameters**

[in]	p_api_ctrl	Pointer to the control structure for the driver instance
[out]	p_lvd_status	Pointer to status structure

Example:

```
err = R_LVD_StatusGet(&g_lvd_ctrl, &status);
```

**Return values**

FSP_SUCCESS	Successful
FSP_ERR_ASSERTION	An argument was NULL
FSP_ERR_NOT_OPEN	Driver is not open

◆ **R\_LVD\_StatusClear()**

```
fsp_err_t R_LVD_StatusClear ( lvd_ctrl_t *const p_api_ctrl)
```

Clears the latched status of the monitor.

**Parameters**

[in]	p_api_ctrl	Pointer to the control structure for the driver instance
------	------------	----------------------------------------------------------

**Return values**

FSP_SUCCESS	Successful
FSP_ERR_ASSERTION	An argument was NULL
FSP_ERR_NOT_OPEN	Driver is not open

◆ **R\_LVD\_VersionGet()**

```
fsp_err_t R_LVD_VersionGet ( fsp_version_t *const p_version)
```

Returns the LVD driver version based on compile time macros.

**Parameters**

[in]	p_version	Pointer to the version structure
------	-----------	----------------------------------

**Return values**

FSP_SUCCESS	Successful
FSP_ERR_ASSERTION	p_version was NULL

◆ **R\_LVD\_CallbackSet()**

```
fsp_err_t R_LVD_CallbackSet ( lvd_ctrl_t *const p_api_ctrl, void(*)(lvd_callback_args_t *)  
p_callback, void const *const p_context, lvd_callback_args_t *const p_callback_memory )
```

Updates the user callback and has option of providing memory for callback structure. Implements `lvd_api_t::callbackSet`

**Return values**

FSP_SUCCESS	Callback updated successfully.
FSP_ERR_ASSERTION	A required pointer is NULL.
FSP_ERR_NOT_OPEN	The control block has not been opened.



## 4.2.34 Operational Amplifier (r\_opamp)

### Modules

#### Functions

fsp_err_t	R_OPAMP_Open (opamp_ctrl_t *const p_api_ctrl, opamp_cfg_t const *const p_cfg)
fsp_err_t	R_OPAMP_InfoGet (opamp_ctrl_t *const p_api_ctrl, opamp_info_t *const p_info)
fsp_err_t	R_OPAMP_Start (opamp_ctrl_t *const p_api_ctrl, uint32_t const channel_mask)
fsp_err_t	R_OPAMP_Stop (opamp_ctrl_t *const p_api_ctrl, uint32_t const channel_mask)
fsp_err_t	R_OPAMP_StatusGet (opamp_ctrl_t *const p_api_ctrl, opamp_status_t *const p_status)
fsp_err_t	R_OPAMP_Trim (opamp_ctrl_t *const p_api_ctrl, opamp_trim_cmd_t const cmd, opamp_trim_args_t const *const p_args)
fsp_err_t	R_OPAMP_Close (opamp_ctrl_t *const p_api_ctrl)
fsp_err_t	R_OPAMP_VersionGet (fsp_version_t *const p_version)

#### Detailed Description

Driver for the OPAMP peripheral on RA MCUs. This module implements the [OPAMP Interface](#).

## Overview

The OPAMP HAL module provides a high level API for signal amplification applications and supports the OPAMP peripheral available on RA MCUs.

#### Features

- Low power or high-speed mode
- Start by software or AGT compare match
- Stop by software or ADC conversion end (stop by ADC conversion end only supported on op-amp channels configured to start by AGT compare match)
- Trimming available on some MCUs (see hardware manual)

## Configuration

## Build Time Configurations for r\_opamp

The following build time configurations are defined in fsp\_cfg/r\_opamp\_cfg.h:

Configuration	Options	Default	Description
Parameter Checking	<ul style="list-style-type: none"> <li>• Default (BSP)</li> <li>• Enabled</li> <li>• Disabled</li> </ul>	Default (BSP)	If selected code for parameter checking is included in the build.

## Configurations for Driver > Analog > Operational Amplifier Driver on r\_opamp

This module can be added to the Stacks tab via New Stack > Driver > Analog > Operational Amplifier Driver on r\_opamp.

Configuration	Options	Default	Description
Name	Name must be a valid C symbol	g_opamp0	Module name.
AGT Start Trigger Configuration (N/A unless AGT Start Trigger is Selected for the Channel)	<ul style="list-style-type: none"> <li>• AGT1 Compare Match Starts OPAMPs 0 and 2 if configured for AGT Start, AGT0 Compare Match Starts OPAMPs 1 and 3 if configured for AGT Start</li> <li>• AGT1 Compare Match Starts OPAMPs 0 and 1 if configured for AGT Start, AGT0 Compare Match Starts OPAMPs 2 and 3 if configured for AGT Start</li> <li>• AGT1 Compare Match Starts all OPAMPs configured for AGT Start</li> </ul>	AGT1 Compare Match Starts all OPAMPs configured for AGT Start	Configure which AGT channel event triggers which op-amp channel. The AGT compare match event only starts the op-amp channel if the AGT Start trigger is selected in the Trigger configuration for the channel.
Power Mode	MCU Specific Options		Configure the op-amp based on power or speed requirements. This setting affects the minimum required stabilization time. Middle speed is not available for all MCUs.

Trigger Channel 0	MCU Specific Options		Select the event triggers to start or stop op-amp channel 0. If the event trigger is selected for start, the start() API enables the event trigger for this channel. If the event trigger is selected for stop, the stop() API disables the event trigger for this channel.
Trigger Channel 1	MCU Specific Options		Select the event triggers to start or stop op-amp channel 1. If the event trigger is selected for start, the start() API enables the event trigger for this channel. If the event trigger is selected for stop, the stop() API disables the event trigger for this channel.
Trigger Channel 2	<ul style="list-style-type: none"> <li>• Software Start</li> <li>• Software Stop</li> <li>• AGT Start</li> <li>• Software Stop</li> <li>• AGT Start ADC</li> <li>• Stop</li> </ul>	Software Start Software Stop	Select the event triggers to start or stop op-amp channel 2. If the event trigger is selected for start, the start() API enables the event trigger for this channel. If the event trigger is selected for stop, the stop() API disables the event trigger for this channel.
Trigger Channel 3	MCU Specific Options		Select the event triggers to start or stop op-amp channel 3. If the event trigger is selected for start, the start() API enables the event trigger for this channel. If the event trigger is selected for stop, the stop() API disables the event trigger for this channel.
OPAMP AMP0OS	MCU Specific Options		Select output to connect to AMP0O pin
OPAMP AMP0PS	MCU Specific Options		Select input to connect to AMP0+ pin

OPAMP AMP0MS	MCU Specific Options	Select input to connect to AMP0- pin
OPAMP AMP1PS	MCU Specific Options	Select input to connect to AMP1+ pin
OPAMP AMP1MS	MCU Specific Options	Select input to connect to AMP1- pin
OPAMP AMP2PS	MCU Specific Options	Select input to connect to AMP2+ pin
OPAMP AMP2MS	MCU Specific Options	Select input to connect to AMP2- pin

## Clock Configuration

The OPAMP runs on PCLKB.

## Pin Configuration

To use the OPAMP HAL module, the port pins for the channels receiving the analog input must be set as inputs on the **Pins** tab of the RA Configuration editor.

Refer to the most recent FSP Release Notes for any additional operational limitations for this module.

# Usage Notes

## Trimming the OPAMP

- On MCUs that support trimming, the op-amp trim register is set to the factory default after the Open API is called.
- This function allows the application to trim the operational amplifier to a user setting, which overwrites the factory default trim values.
- Supported on selected MCUs. See hardware manual for details.
- Not supported if configured for low power mode (OPAMP\_MODE\_LOW\_POWER).
- This function is not reentrant. Only one side of one op-amp can be trimmed at a time. Complete the procedure for one side of one channel before calling the trim API with the command OPAMP\_TRIM\_CMD\_START again.
  - The trim procedure works as follows:
    - Call trim() for the Pch (+) side input with command OPAMP\_TRIM\_CMD\_START.
    - Connect a fixed voltage to the Pch (+) input.
    - Connect the Nch (-) input to the op-amp output to create a voltage follower.
    - Ensure the op-amp is operating and stabilized.
    - Call trim() for the Pch (+) side input with command OPAMP\_TRIM\_CMD\_START.
    - Measure the fixed voltage connected to the Pch (+) input using the SAR ADC and save the value (referred to as A later in this procedure).
    - Iterate over the following loop 5 times:
      - Call trim() for the Pch (+) side input with command OPAMP\_TRIM\_CMD\_NEXT\_STEP.
      - Measure the op-amp output using the SAR ADC (referred to as B in the next step).
      - If  $A \leq B$ , call trim() for the Pch (+) side input with command OPAMP\_TRIM\_CMD\_CLEAR\_BIT.
    - Call trim() for the Nch (-) side input with command OPAMP\_TRIM\_CMD\_START.
    - Measure the fixed voltage connected to the Pch (+) input using the SAR ADC and

- save the value (referred to as A later in this procedure).
- Iterate over the following loop 5 times:
    - Call trim() for the Nch (-) side input with command OPAMP\_TRIM\_CMD\_NEXT\_STEP.
    - Measure the op-amp output using the SAR ADC (referred to as B in the next step).
    - If  $A \leq B$ , call trim() for the Nch (-) side input with command OPAMP\_TRIM\_CMD\_CLEAR\_BIT.

## Examples

### Basic Example

This is a basic example of minimal use of the R\_OPAMP in an application. The example demonstrates configuring OPAMP channel 0 for high speed mode, starting the OPAMP and reading the status of the OPAMP channel running. It also verifies that the stabilization wait time is the expected time for selected power mode

```
#define OPAMP_EXAMPLE_CHANNEL (0U)

void basic_example (void)
{
    fsp_err_t err;

    /* Initialize the OPAMP module. */
    err = R_OPAMP_Open(&g_opamp_ctrl, &g_opamp_cfg);

    /* Handle any errors. This function should be defined by the user. */
    handle_error(err);

    /* Start the OPAMP module. */
    err = R_OPAMP_Start(&g_opamp_ctrl, 1 << OPAMP_EXAMPLE_CHANNEL);

    handle_error(err);

    /* Look up the required stabilization wait time. */
    opamp_info_t info;

    err = R_OPAMP_InfoGet(&g_opamp_ctrl, &info);

    handle_error(err);

    /* Wait for the OPAMP to stabilize. */
    R_BSP_SoftwareDelay(info.min_stabilization_wait_us, BSP_DELAY_UNITS_MICROSECONDS);
}
```

### Trim Example

This example demonstrates the typical trimming procedure for opamp channel 0 using [R\\_OPAMP\\_Trim\(\)](#) API.

```
#ifndef OPAMP_EXAMPLE_CHANNEL
#define OPAMP_EXAMPLE_CHANNEL (0U)
#endif

#ifndef OPAMP_EXAMPLE_ADC_CHANNEL
#define OPAMP_EXAMPLE_ADC_CHANNEL (ADC_CHANNEL_2)
#endif

#define ADC_SCAN_END_DELAY (100U)
#define OPAMP_TRIM_LOOP_COUNT (5)
#define ADC_SCAN_END_MAX_TIMEOUT (0xFFFF)

uint32_t g_callback_event_counter = 0;
opamp_trim_args_t trim_args_ch =
{
    .channel = OPAMP_EXAMPLE_CHANNEL,
    .input = OPAMP_TRIM_INPUT_PCH
};

/* This callback is called when ADC Scan Complete event is generated. */
void adc_callback (adc_callback_args_t * p_args)
{
    FSP_PARAMETER_NOT_USED(p_args);
    g_callback_event_counter++;
}

void trimming_example (void)
{
    fsp_err_t err;

    /* On RA2A1, configure negative feedback and put DAC12 signal on AMP0+ Pin. */
    g_opamp_cfg_extend.plus_input_select_opamp0 = OPAMP_PLUS_INPUT_AMP0P7;
    g_opamp_cfg_extend.minus_input_select_opamp0 = OPAMP_MINUS_INPUT_AMP0M7;

    /* Initialize the OPAMP module. */
    err = R_OPAMP_Open(&g_opamp_ctrl, &g_opamp_cfg);

    /* Handle any errors. This function should be defined by the user. */
    handle_error(err);

    /* Start the OPAMP module. */
    err = R_OPAMP_Start(&g_opamp_ctrl, 1 << OPAMP_EXAMPLE_CHANNEL);
    handle_error(err);
}
```

```
/* Look up the required stabilization wait time. */
opamp_info_t info;
err = R_OPAMP_InfoGet(&g_opamp_ctrl, &info);
handle_error(err);
/* Wait for the OPAMP to stabilize. */
R_BSP_SoftwareDelay(info.min_stabilization_wait_us, BSP_DELAY_UNITS_MICROSECONDS);
/* Call trim() for the Pch (+) side input */
trim_procedure(&trim_args_ch);
handle_error(err);
trim_args_ch.input = OPAMP_TRIM_INPUT_NCH;
/* Call trim() for the Nch (-) side input */
trim_procedure(&trim_args_ch);
}
void trim_procedure (opamp_trim_args_t * trim_args)
{
    fsp_err_t err;
    /* Call trim() for the selected channel and input with command OPAMP_TRIM_CMD_START.
    */
    err = R_OPAMP_Trim(&g_opamp_ctrl, OPAMP_TRIM_CMD_START, trim_args);
    handle_error(err);
    /* Measure the fixed voltage connected to the channel input using the SAR ADC and
    save the value
    * (referred to as result_a later in this procedure). */
    /* Reset the ADC callback counter */
    g_callback_event_counter = 0;
    err = R_ADC_ScanStart(&g_adc_ctrl);
    handle_error(err);
    /* Wait for ADC scan complete flag */
    uint32_t timeout = ADC_SCAN_END_MAX_TIMEOUT;
    while (g_callback_event_counter == 0 && timeout != 0)
    {
        timeout--;
    }
    if (0 == timeout)
```

```
{
    err = FSP_ERR_TIMEOUT;
    handle_error(err);
}

uint16_t result_a;
err = R_ADC_Read(&g_adc_ctrl, OPAMP_EXAMPLE_ADC_CHANNEL, &result_a);
handle_error(err);

/* Iterate over the following loop 5 times: */
/* Call trim() with command OPAMP_TRIM_CMD_NEXT_STEP for the selected channel and
given input. */
uint8_t count = OPAMP_TRIM_LOOP_COUNT;
while (count > 0)
{
    count--;
    err = R_OPAMP_Trim(&g_opamp_ctrl, OPAMP_TRIM_CMD_NEXT_STEP, trim_args);
    handle_error(err);
}
/* Reset the ADC callback counter */
g_callback_event_counter = 0;
/* Read converted value after trim completes. */
err = R_ADC_ScanStart(&g_adc_ctrl);
handle_error(err);
/* Wait for ADC scan complete flag */
timeout = ADC_SCAN_END_MAX_TIMEOUT;
while (g_callback_event_counter == 0 && timeout != 0)
{
    timeout--;
}
if (0 == timeout)
{
    err = FSP_ERR_TIMEOUT;
    handle_error(err);
}

uint16_t result_b;
err = R_ADC_Read(&g_adc_ctrl, OPAMP_EXAMPLE_ADC_CHANNEL, &result_b);
```



```

    handle_error(err);

    /* Measure the op-amp output using the SAR ADC (referred to as result_b in the next
step). */

    /* If result_a <= result_b, call trim() for the selected channel and input with
command OPAMP_TRIM_CMD_CLEAR_BIT. */
    if (result_a <= result_b)
    {
        err = R_OPAMP_Trim(&g_opamp_ctrl, OPAMP_TRIM_CMD_CLEAR_BIT, trim_args);
        handle_error(err);
    }
}
}

```

## Data Structures

struct [opamp\\_extended\\_cfg\\_t](#)

struct [opamp\\_instance\\_ctrl\\_t](#)

## Macros

#define [OPAMP\\_CODE\\_VERSION\\_MAJOR](#)

## Enumerations

enum [opamp\\_trigger\\_t](#)

enum [opamp\\_agt\\_link\\_t](#)

enum [opamp\\_mode\\_t](#)

enum [opamp\\_plus\\_input\\_t](#)

enum [opamp\\_minus\\_input\\_t](#)

enum [opamp\\_output\\_t](#)

## Variables

const [opamp\\_api\\_t](#) [g\\_opamp\\_on\\_opamp](#)

## Data Structure Documentation

### ◆ [opamp\\_extended\\_cfg\\_t](#)

struct [opamp\\_extended\\_cfg\\_t](#)

OPAMP configuration extension. This extension is required and must be provided in `opamp_cfg_t::p_extend`.

Data Fields		
<code>opamp_agt_link_t</code>	<code>agt_link</code>	Configure which AGT links are paired to which channel. Only applies to channels if <code>OPAMP_TRIGGER_AGT_START_SOFTWARE_STOP</code> or <code>OPAMP_TRIGGER_AGT_START_ADC_STOP</code> is selected for the channel.
<code>opamp_mode_t</code>	<code>mode</code>	Low power, middle speed, or high speed mode.
<code>opamp_trigger_t</code>	<code>trigger_channel_0</code>	Start and stop triggers for channel 0.
<code>opamp_trigger_t</code>	<code>trigger_channel_1</code>	Start and stop triggers for channel 1.
<code>opamp_trigger_t</code>	<code>trigger_channel_2</code>	Start and stop triggers for channel 2.
<code>opamp_trigger_t</code>	<code>trigger_channel_3</code>	Start and stop triggers for channel 3.
<code>opamp_plus_input_t</code>	<code>plus_input_select_opamp0</code>	OPAMP0+ connection.
<code>opamp_minus_input_t</code>	<code>minus_input_select_opamp0</code>	OPAMP0- connection.
<code>opamp_output_t</code>	<code>output_select_opamp0</code>	OPAMP0O connection.
<code>opamp_plus_input_t</code>	<code>plus_input_select_opamp1</code>	OPAMP1+ connection.
<code>opamp_minus_input_t</code>	<code>minus_input_select_opamp1</code>	OPAMP1- connection.
<code>opamp_plus_input_t</code>	<code>plus_input_select_opamp2</code>	OPAMP2+ connection.
<code>opamp_minus_input_t</code>	<code>minus_input_select_opamp2</code>	OPAMP2- connection.

#### ◆ `opamp_instance_ctrl_t`

```
struct opamp_instance_ctrl_t
```

OPAMP instance control block. DO NOT INITIALIZE. Initialized in `opamp_api_t::open()`.

## Macro Definition Documentation

#### ◆ `OPAMP_CODE_VERSION_MAJOR`

```
#define OPAMP_CODE_VERSION_MAJOR
```

Version of code that implements the API defined in this file

## Enumeration Type Documentation

◆ **opamp\_trigger\_t**

enum <code>opamp_trigger_t</code>	
Start and stop trigger for the op-amp.	
Enumerator	
<code>OPAMP_TRIGGER_SOFTWARE_START_SOFTWARE_STOP</code>	Start and stop with APIs.
<code>OPAMP_TRIGGER_AGT_START_SOFTWARE_STOP</code>	Start by AGT compare match and stop with API.
<code>OPAMP_TRIGGER_AGT_START_ADC_STOP</code>	Start by AGT compare match and stop after ADC conversion.

◆ **opamp\_agt\_link\_t**

enum <code>opamp_agt_link_t</code>	
Which AGT timer starts the op-amp. Only applies to channels if <code>OPAMP_TRIGGER_AGT_START_SOFTWARE_STOP</code> or <code>OPAMP_TRIGGER_AGT_START_ADC_STOP</code> is selected for the channel. If <code>OPAMP_TRIGGER_SOFTWARE_START_SOFTWARE_STOP</code> is selected for a channel, then no AGT compare match event will start that op-amp channel.	
Enumerator	
<code>OPAMP_AGT_LINK_AGT1_OPAMP_0_2_AGT0_OPA_MP_1_3</code>	OPAMP channel 0 and 2 are started by AGT1 compare match. OPAMP channel 1 and 3 are started by AGT0 compare match.
<code>OPAMP_AGT_LINK_AGT1_OPAMP_0_1_AGT0_OPA_MP_2_3</code>	OPAMP channel 0 and 1 are started by AGT1 compare match. OPAMP channel 2 and 3 are started by AGT0 compare match.
<code>OPAMP_AGT_LINK_AGT1_OPAMP_0_1_2_3</code>	All OPAMP channels are started by AGT1 compare match.

◆ **opamp\_mode\_t**

enum <code>opamp_mode_t</code>	
Op-amp mode.	
Enumerator	
OPAMP_MODE_LOW_POWER	Low power mode.
OPAMP_MODE_MIDDLE_SPEED	Middle speed mode (not supported on all MCUs)
OPAMP_MODE_HIGH_SPEED	High speed mode.

◆ **opamp\_plus\_input\_t**

enum <code>opamp_plus_input_t</code>	
Options to connect AMPnPS pins.	
Enumerator	
OPAMP_PLUS_INPUT_NONE	No Connection.
OPAMP_PLUS_INPUT_AMPPS0	Set AMPPS0. See hardware manual for channel specific options.
OPAMP_PLUS_INPUT_AMPPS1	Set AMPPS1. See hardware manual for channel specific options.
OPAMP_PLUS_INPUT_AMPPS2	Set AMPPS2. See hardware manual for channel specific options.
OPAMP_PLUS_INPUT_AMPPS3	Set AMPPS3. See hardware manual for channel specific options.
OPAMP_PLUS_INPUT_AMPPS7	Set AMPPS7. See hardware manual for channel specific options.

◆ **opamp\_minus\_input\_t**

enum <code>opamp_minus_input_t</code>	
Options to connect AMPnMS pins.	
Enumerator	
OPAMP_MINUS_INPUT_NONE	No Connection.
OPAMP_MINUS_INPUT_AMPMS0	Set AMPMS0. See hardware manual for channel specific options.
OPAMP_MINUS_INPUT_AMPMS1	Set AMPMS1. See hardware manual for channel specific options.
OPAMP_MINUS_INPUT_AMPMS2	Set AMPMS2. See hardware manual for channel specific options.
OPAMP_MINUS_INPUT_AMPMS3	Set AMPMS3. See hardware manual for channel specific options.
OPAMP_MINUS_INPUT_AMPMS4	Set AMPMS4. See hardware manual for channel specific options.
OPAMP_MINUS_INPUT_AMPMS7	Set AMPMS7. See hardware manual for channel specific options.

◆ **opamp\_output\_t**

enum <code>opamp_output_t</code>	
Options to connect AMP0OS pin.	
Enumerator	
OPAMP_OUTPUT_NONE	No Connection.
OPAMP_OUTPUT_AMPOS0	Set AMPOS0. See hardware manual for channel specific options.
OPAMP_OUTPUT_AMPOS1	Set AMPOS1. See hardware manual for channel specific options.
OPAMP_OUTPUT_AMPOS2	Set AMPOS2. See hardware manual for channel specific options.
OPAMP_OUTPUT_AMPOS3	Set AMPOS3. See hardware manual for channel specific options.

## Function Documentation

### ◆ R\_OPAMP\_Open()

```
fsp_err_t R_OPAMP_Open ( opamp_ctrl_t *const p_api_ctrl, opamp_cfg_t const *const p_cfg )
```

Applies power to the OPAMP and initializes the hardware based on the user configuration. Implements `opamp_api_t::open`.

The op-amp is not operational until the `opamp_api_t::start` is called. If the op-amp is configured to start after AGT compare match, the op-amp is not operational until `opamp_api_t::start` and the associated AGT compare match event occurs.

Some MCUs have switches that must be set before starting the op-amp. These switches must be set in the application code after `opamp_api_t::open` and before `opamp_api_t::start`.

Example:

```
/* Initialize the OPAMP module. */
err = R_OPAMP_Open(&g_opamp_ctrl, &g_opamp_cfg);
```

### Return values

FSP_SUCCESS	Configuration successful.
FSP_ERR_ASSERTION	An input pointer is NULL.
FSP_ERR_ALREADY_OPEN	Control block is already opened.
FSP_ERR_INVALID_ARGUMENT	An attempt to configure OPAMP in middle speed mode on MCU that does not support middle speed mode.

◆ **R\_OPAMP\_InfoGet()**

```
fsp_err_t R_OPAMP_InfoGet ( opamp_ctrl_t*const p_api_ctrl, opamp_info_t*const p_info )
```

Provides the minimum stabilization wait time in microseconds. Implements `opamp_api_t::infoGet`.

• **Example:**

```
/* Look up the required stabilization wait time. */
opamp_info_t info;

err = R_OPAMP_InfoGet(&g_opamp_ctrl, &info);

handle_error(err);

/* Wait for the OPAMP to stabilize. */
R_BSP_SoftwareDelay(info.min_stabilization_wait_us,
BSP_DELAY_UNITS_MICROSECONDS);
```

**Return values**

FSP_SUCCESS	information on <code>opamp_power_mode</code> stored in <code>p_info</code> .
FSP_ERR_ASSERTION	An input pointer was NULL.
FSP_ERR_NOT_OPEN	Instance control block is not open.

◆ **R\_OPAMP\_Start()**

```
fsp_err_t R_OPAMP_Start ( opamp_ctrl_t *const p_api_ctrl, uint32_t const channel_mask )
```

If the OPAMP is configured for hardware triggers, enables hardware triggers. Otherwise, starts the op-amp. Implements `opamp_api_t::start`.

Some MCUs have switches that must be set before starting the op-amp. These switches must be set in the application code after `opamp_api_t::open` and before `opamp_api_t::start`.

Example:

```
/* Start the OPAMP module. */
err = R_OPAMP_Start(&g_opamp_ctrl, 1 << OPAMP_EXAMPLE_CHANNEL);
handle_error(err);
```

**Return values**

FSP_SUCCESS	Op-amp started or hardware triggers enabled successfully.
FSP_ERR_ASSERTION	An input pointer was NULL.
FSP_ERR_NOT_OPEN	Instance control block is not open.
FSP_ERR_INVALID_ARGUMENT	channel_mask includes a channel that does not exist on this MCU.

◆ **R\_OPAMP\_Stop()**

```
fsp_err_t R_OPAMP_Stop ( opamp_ctrl_t *const p_api_ctrl, uint32_t const channel_mask )
```

Stops the op-amp. If the OPAMP is configured for hardware triggers, disables hardware triggers. Implements `opamp_api_t::stop`.

**Return values**

FSP_SUCCESS	Op-amp stopped or hardware triggers disabled successfully.
FSP_ERR_ASSERTION	An input pointer was NULL.
FSP_ERR_NOT_OPEN	Instance control block is not open.
FSP_ERR_INVALID_ARGUMENT	channel_mask includes a channel that does not exist on this MCU.



### ◆ R\_OPAMP\_StatusGet()

```
fsp_err_t R_OPAMP_StatusGet ( opamp_ctrl_t *const p_api_ctrl, opamp_status_t *const p_status )
```

Provides the operating status for each op-amp in a bitmask. This bit is set when operation begins, before the stabilization wait time has elapsed. Implements `opamp_api_t::statusGet`.

#### Return values

FSP_SUCCESS	Operating status of each op-amp provided in <code>p_status</code> .
FSP_ERR_ASSERTION	An input pointer was NULL.
FSP_ERR_NOT_OPEN	Instance control block is not open.

### ◆ R\_OPAMP\_Trim()

```
fsp_err_t R_OPAMP_Trim ( opamp_ctrl_t *const p_api_ctrl, opamp_trim_cmd_t const cmd,
opamp_trim_args_t const *const p_args )
```

On MCUs that support trimming, the op-amp trim register is set to the factory default after `open()`. This function allows the application to trim the operational amplifier to a user setting, which overwrites the factory default factory trim values.

Not supported on all MCUs. See hardware manual for details. Not supported if configured for low power mode (`OPAMP_MODE_LOW_POWER`).

This function is not reentrant. Only one side of one op-amp can be trimmed at a time. Complete the procedure for one side of one channel before calling `trim()` with command `OPAMP_TRIM_CMD_START` again.

Implements `opamp_api_t::trim`.

Reference: Section 37.9 "User Offset Trimming" RA2A1 hardware manual R01UM0008EU0130. The trim procedure works as follows:

- Call `trim()` for the Pch (+) side input with command `OPAMP_TRIM_CMD_START`.
- Connect a fixed voltage to the Pch (+) input.
- Connect the Nch (-) input to the op-amp output to create a voltage follower.
- Ensure the op-amp is operating and stabilized.
- Call `trim()` for the Pch (+) side input with command `OPAMP_TRIM_CMD_START`.
- Measure the fixed voltage connected to the Pch (+) input using the SAR ADC and save the value (referred to as A later in this procedure).
- Iterate over the following loop 5 times:
  - Call `trim()` for the Pch (+) side input with command `OPAMP_TRIM_CMD_NEXT_STEP`.
  - Measure the op-amp output using the SAR ADC (referred to as B in the next step).
  - If  $A \leq B$ , call `trim()` for the Pch (+) side input with command `OPAMP_TRIM_CMD_CLEAR_BIT`.
- Call `trim()` for the Nch (-) side input with command `OPAMP_TRIM_CMD_START`.
- Measure the fixed voltage connected to the Pch (+) input using the SAR ADC and save the value (referred to as A later in this procedure).
- Iterate over the following loop 5 times:
  - Call `trim()` for the Nch (-) side input with command `OPAMP_TRIM_CMD_NEXT_STEP`.

- Measure the op-amp output using the SAR ADC (referred to as B in the next step).
- If  $A \leq B$ , call trim() for the Nch (-) side input with command OPAMP\_TRIM\_CMD\_CLEAR\_BIT.

**Return values**

FSP_SUCCESS	Conversion result in p_data.
FSP_ERR_UNSUPPORTED	Trimming is not supported on this MCU.
FSP_ERR_INVALID_STATE	The command is not valid in the current state of the trim state machine.
FSP_ERR_INVALID_ARGUMENT	The requested channel is not operating or the trim procedure is not in progress for this channel/input combination.
FSP_ERR_INVALID_MODE	Trim is not allowed in low power mode.
FSP_ERR_ASSERTION	An input pointer was NULL.
FSP_ERR_NOT_OPEN	Instance control block is not open.

**◆ R\_OPAMP\_Close()**

`fsp_err_t R_OPAMP_Close ( opamp_ctrl_t *const p_api_ctrl)`

Stops the op-amps. Implements `opamp_api_t::close`.

**Return values**

FSP_SUCCESS	Instance control block closed successfully.
FSP_ERR_ASSERTION	An input pointer was NULL.
FSP_ERR_NOT_OPEN	Instance control block is not open.

**◆ R\_OPAMP\_VersionGet()**

`fsp_err_t R_OPAMP_VersionGet ( fsp_version_t *const p_version)`

Gets the API and code version. Implements `opamp_api_t::versionGet`.

**Return values**

FSP_SUCCESS	Version information available in p_version.
FSP_ERR_ASSERTION	The parameter p_version is NULL.

**Variable Documentation**

◆ **g\_opamp\_on\_opamp**const [opamp\\_api\\_t](#) g\_opamp\_on\_opamp

OPAMP Implementation of OPAMP interface.

**4.2.35 Octa Serial Peripheral Interface Flash (r\_ospi)**

## Modules

**Functions**

fsp_err_t	<a href="#">R_OSPI_Open</a> ( <a href="#">spi_flash_ctrl_t</a> *p_ctrl, <a href="#">spi_flash_cfg_t</a> const *const p_cfg)
-----------	-----------------------------------------------------------------------------------------------------------------------------

fsp_err_t	<a href="#">R_OSPI_Close</a> ( <a href="#">spi_flash_ctrl_t</a> *p_ctrl)
-----------	--------------------------------------------------------------------------

fsp_err_t	<a href="#">R_OSPI_DirectWrite</a> ( <a href="#">spi_flash_ctrl_t</a> *p_ctrl, uint8_t const *const p_src, uint32_t const bytes, bool const read_after_write)
-----------	---------------------------------------------------------------------------------------------------------------------------------------------------------------

fsp_err_t	<a href="#">R_OSPI_DirectRead</a> ( <a href="#">spi_flash_ctrl_t</a> *p_ctrl, uint8_t *const p_dest, uint32_t const bytes)
-----------	----------------------------------------------------------------------------------------------------------------------------

fsp_err_t	<a href="#">R_OSPI_DirectTransfer</a> ( <a href="#">spi_flash_ctrl_t</a> *p_ctrl, <a href="#">spi_flash_direct_transfer_t</a> *const p_transfer, <a href="#">spi_flash_direct_transfer_dir_t</a> direction)
-----------	-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------

fsp_err_t	<a href="#">R_OSPI_SpiProtocolSet</a> ( <a href="#">spi_flash_ctrl_t</a> *p_ctrl, <a href="#">spi_flash_protocol_t</a> spi_protocol)
-----------	--------------------------------------------------------------------------------------------------------------------------------------

fsp_err_t	<a href="#">R_OSPI_XipEnter</a> ( <a href="#">spi_flash_ctrl_t</a> *p_ctrl)
-----------	-----------------------------------------------------------------------------

fsp_err_t	<a href="#">R_OSPI_XipExit</a> ( <a href="#">spi_flash_ctrl_t</a> *p_ctrl)
-----------	----------------------------------------------------------------------------

fsp_err_t	<a href="#">R_OSPI_Write</a> ( <a href="#">spi_flash_ctrl_t</a> *p_ctrl, uint8_t const *const p_src, uint8_t *const p_dest, uint32_t byte_count)
-----------	--------------------------------------------------------------------------------------------------------------------------------------------------

fsp_err_t	<a href="#">R_OSPI_Erase</a> ( <a href="#">spi_flash_ctrl_t</a> *p_ctrl, uint8_t *const p_device_address, uint32_t byte_count)
-----------	--------------------------------------------------------------------------------------------------------------------------------

fsp_err_t	<a href="#">R_OSPI_StatusGet</a> ( <a href="#">spi_flash_ctrl_t</a> *p_ctrl, <a href="#">spi_flash_status_t</a> *const p_status)
-----------	----------------------------------------------------------------------------------------------------------------------------------

fsp_err_t	<a href="#">R_OSPI_BankSet</a> ( <a href="#">spi_flash_ctrl_t</a> *p_ctrl, uint32_t bank)
-----------	-------------------------------------------------------------------------------------------

fsp_err_t	<a href="#">R_OSPI_VersionGet</a> ( <a href="#">fsp_version_t</a> *const p_version)
-----------	-------------------------------------------------------------------------------------

## Detailed Description

Driver for the OSPI peripheral on RA MCUs. This module implements the [SPI Flash Interface](#).

## Overview

The OSPI peripheral interfaces with an external OctaFlash chip to perform data I/O Operations.

### Features

The OSPI driver has the following key features:

- Perform data I/O Operation in both SPI and OPI modes
- Can be configured with OctaFlash device on either of the 2 channels
- Memory mapped read access to the OctaFlash
- Programming the OctaFlash device using single continuous write
- Erasing the OctaFlash device
- Sending device specific commands and reading back responses
- Entering and exiting XIP (Single Continuous Read) mode
- 3 byte addressing for SPI
- 4 byte addressing for SPI and OPI
- Auto-calibration for OPI mode (SOPI and DOPI)

## Configuration

### Build Time Configurations for r\_ospi

The following build time configurations are defined in driver/r\_ospi\_cfg.h:

Configuration	Options	Default	Description
Parameter Checking Enable	<ul style="list-style-type: none"> <li>• Default (BSP)</li> <li>• Enabled</li> <li>• Disabled</li> </ul>	Default (BSP)	If selected code for parameter checking is included in the build.

### Configurations for Driver > Storage > OSPI Driver on r\_ospi

This module can be added to the Stacks tab via New Stack > Driver > Storage > OSPI Driver on r\_ospi.

Configuration	Options	Default	Description
General > Single Continuous Mode > Read Idle Time	Must be an integer greater than 0	100	Specify the read idle time.
General > Single Continuous Mode > Write Idle Time	Must be an integer greater than 0	100	Specify the write idle time.
General > Name	Name must be a valid C symbol	g_ospi0	Module name.
General > Channel	Channel should be 0 or 1	0	Specify the OSPI chip select line to use.

General > Flash Size	Must be an integer greater than 0	0x04000000U	Specify the OctaFlash size in bytes.
General > SPI Protocol	<ul style="list-style-type: none"> <li>• SPI</li> <li>• Single data rate OPI</li> <li>• Dual data rate OPI</li> </ul>	SPI	Select the initial SPI protocol. SPI protocol can be changed on the OctaFlash using <a href="#">R_OSPI_DirectTransfer()</a> .
General > Address Bytes	<ul style="list-style-type: none"> <li>• 3</li> <li>• 4</li> </ul>	4	Select the number of address bytes.
General > Page Size Bytes	Must be an integer greater than 0	256	The maximum number of bytes allowed for a single write.
OPI Mode > Auto-Calibration > Data latching delay	Must be a valid non-negative integer	0x80	Set this to 0 to enable auto-calibration. 0x80 is the default value calculated at 3.3V and 25°C
OPI Mode > Auto-Calibration > Auto-Calibration Address	Must be a valid non-negative integer	0x00	Set the address of the read/write destination to be performed for auto-calibration.
OPI Mode > Command Definitions > Page Program Command	Manual Entry	0x12ED	The command to program a page in OPI mode.
OPI Mode > Command Definitions > Read Command	Manual Entry	0xEC13	The command to read in SOPI mode (8READ).
OPI Mode > Command Definitions > Dual Read Command	Manual Entry	0xEE11	The command to read in DOPI mode (8DTRD).
OPI Mode > Command Definitions > Write Enable Command	Manual Entry	0x06F9	The command to enable write in OPI mode.
OPI Mode > Command Definitions > Status Command	Manual Entry	0x05FA	The command to query the status of a write or erase command in OPI mode.
OPI Mode > Command Length Bytes	Must be an integer between 1 and 2	2	Command length in bytes
OPI Mode > Memory Read Dummy Cycles	Must be an integer between 6 and 10	10	Memory read dummy cycles
SPI Mode > Command Definitions > Page Program Command	Manual Entry	0x12	The command to program a page in SPI mode.
SPI Mode > Command	Manual Entry	0x13	The command to read

Definitions > Read Command				in SPI mode.
SPI Mode > Command Definitions > Write Enable Command	Manual Entry	0x06		The command to enable write in SPI mode.
SPI Mode > Command Definitions > Status Command	Manual Entry	0x05		The command to query the status of a write or erase command in SPI mode.
Common Command Definitions > Sector Erase Command	Manual Entry	0x21DE		The command to erase a sector. Set Sector Erase Size to 0 if unused.
Common Command Definitions > Block Erase Command	Manual Entry	0xDC23		The command to erase a block. Set Block Erase Size to 0 if unused.
Common Command Definitions > Chip Erase Command	Manual Entry	0xC738		The command to erase the entire chip. Set Chip Erase Command to 0 if unused.
Common Command Definitions > Write Status Bit	Must be an integer between 0 and 7	0		Which bit contains the write in progress status returned from the Write Status Command.
Common Command Definitions > Sector Erase Size	Must be an integer greater than or equal to 0	4096		The sector erase size. Set Sector Erase Size to 0 if Sector Erase is not supported.
Common Command Definitions > Block Erase Size	Must be an integer greater than or equal to 0	65536		The block erase size. Set Block Erase Size to 0 if Block Erase is not supported.
Chip Select Timing Setting > Memory Mapped Read Command Interval	<ul style="list-style-type: none"> <li>• 2</li> <li>• 5</li> <li>• 7</li> <li>• 9</li> <li>• 11</li> <li>• 13</li> <li>• 15</li> <li>• 17</li> </ul>	2		Memory mapped read command execution interval setting in OCTACLK units
Chip Select Timing Setting > Memory Mapped Write Command Interval	<ul style="list-style-type: none"> <li>• 2</li> <li>• 5</li> <li>• 7</li> <li>• 9</li> <li>• 11</li> <li>• 13</li> <li>• 15</li> </ul>	2		Memory mapped write command execution interval setting in OCTACLK units

Chip Select Timing Setting > Command Interval	<ul style="list-style-type: none"> <li>• 17</li> <li>• 2</li> <li>• 5</li> <li>• 7</li> <li>• 9</li> <li>• 11</li> <li>• 13</li> <li>• 15</li> <li>• 17</li> </ul>	2	Command execution interval setting in OCTACLK units
Chip Select Timing Setting > Memory Mapped Read Pull-up Timing	<ul style="list-style-type: none"> <li>• 5 SPI/SOPI</li> <li>• 6 SPI/SOPI</li> <li>• 7 SPI/SOPI, 6.5 DOPI</li> <li>• 8 SPI/SOPI, 7.5 DOPI</li> <li>• 9 SPI/SOPI, 8.5 DOPI</li> </ul>	5 SPI/SOPI	Memory mapped read signal pull-up timing setting in OCTACLK units
Chip Select Timing Setting > Memory Mapped Write Pull-up Timing	<ul style="list-style-type: none"> <li>• 2 SPI/SOPI, 1.5 DOPI</li> <li>• 3 SPI/SOPI, 2.5 DOPI</li> <li>• 4 SPI/SOPI, 3.5 DOPI</li> <li>• 5 SPI/SOPI, 4.5 DOPI</li> <li>• 6 SPI/SOPI, 5.5 DOPI</li> <li>• 7 SPI/SOPI, 6.5 DOPI</li> <li>• 8 SPI/SOPI, 7.5 DOPI</li> <li>• 9 SPI/SOPI, 8.5 DOPI</li> </ul>	2 SPI/SOPI, 1.5 DOPI	Memory mapped write signal pull-up timing setting in OCTACLK units
Chip Select Timing Setting > Pull-up Timing	<ul style="list-style-type: none"> <li>• 5 SPI/SOPI</li> <li>• 6 SPI/SOPI</li> <li>• 7 SPI/SOPI, 6.5 DOPI</li> <li>• 8 SPI/SOPI, 7.5 DOPI</li> <li>• 9 SPI/SOPI, 8.5 DOPI</li> </ul>	5 SPI/SOPI	Signal pull-up timing setting in OCTACLK units
Chip Select Timing Setting > Memory Mapped Read Pull-down Timing	<ul style="list-style-type: none"> <li>• 3 SPI/SOPI, 2.5 DOPI</li> <li>• 4 SPI/SOPI, 3.5 DOPI</li> <li>• 5 SPI/SOPI, 4.5 DOPI</li> </ul>	3 SPI/SOPI, 2.5 DOPI	Memory mapped read signal pull-down timing setting in OCTACLK units
Chip Select Timing Setting > Memory Mapped Write Pull-down Timing	<ul style="list-style-type: none"> <li>• 3 SPI/SOPI, 2.5 DOPI</li> <li>• 4 SPI/SOPI, 3.5 DOPI</li> </ul>	3 SPI/SOPI, 2.5 DOPI	Memory mapped write signal pull-down timing setting in OCTACLK units

	<ul style="list-style-type: none"> <li>• 5 SPI/SOPI, 4.5 DOPI</li> </ul>		
Chip Select Timing Setting > Pull-down Timing	<ul style="list-style-type: none"> <li>• 3 SPI/SOPI, 2.5 DOPI</li> <li>• 4 SPI/SOPI, 3.5 DOPI</li> <li>• 5 SPI/SOPI, 4.5 DOPI</li> </ul>	3 SPI/SOPI, 2.5 DOPI	Signal pull-down timing setting in OCTACLK units

## Clock Configuration

The OSPI clock is derived from PCLKA.

## Pin Configuration

The following pins are available to connect to an external OSPI device:

- OMCLK: OSPI clock output
- OMDQS: OSPI data strobe signal
- OMCS0: OSPI device 0 select
- OMCS1: OSPI device 1 select
- OMSIO0: Data 0 I/O
- OMSIO1: Data 1 I/O
- OMSIO2: Data 2 I/O
- OMSIO3: Data 3 I/O
- OMSIO4: Data 4 I/O
- OMSIO5: Data 5 I/O
- OMSIO6: Data 6 I/O
- OMSIO7: Data 7 I/O

### Note

*Data pins must be configured with IOPORT\_CFG\_DRIVE\_HS\_HIGH.*

*Chip Select pins should be configured with at least IOPORT\_CFG\_DRIVE\_MEDIUM.*

## Usage Notes

### OSPI Memory Mapped Access

After [R\\_OSPI\\_Open\(\)](#) completes successfully, the OctaFlash device contents are mapped to address 0x68000000 (channel 0) or 0x70000000 (channel 1) based on the channel configured and can be read like on-chip flash. Channel 0 supports 128 MB while Channel 1 supports 256 MB of address space.

### Auto-calibration

Auto-calibration procedure is triggered automatically when the 'Data latching delay' field in the configurator properties is set to 0. The user application is responsible for setting the appropriate preamble pattern before calling [R\\_OSPI\\_Open\(\)](#) with SOPI/DOPI mode or changing the SPI protocol to SOPI/DOPI using [R\\_OSPI\\_SpiProtocolSet\(\)](#) API. The appropriate preamble pattern can be written to the desired address using the [R\\_OSPI\\_Write\(\)](#) API while in the SPI mode. Ensure that the same address is passed through the configurator. If the OctaFlash chip is already in SOPI/DOPI mode, the preamble pattern must be programmed using the debugger before calling [R\\_OSPI\\_Open\(\)](#).

### Chip Select Latencies



Chip select latencies can be set through the configurator. The default settings support SOPI and SPI at minimum latency. In case the driver is opened in SPI mode and will be switched to DOPI mode later using `R_OSPI_SpiProtocolSet()`, please select latencies required for DOPI before calling `R_OSPI_Open()`.

## OctaFlash Commands

- Set the erase commands based on intended mode of operation (SPI or OPI). These commands cannot be changed during run-time.
- Read, Write and Status commands for both SPI and OPI are configured allowing switching between the modes at run-time.

## Limitations

Developers should be aware of the following limitations when using the OSPI driver:

- Single continuous read in SPI mode is not supported by the peripheral. The maximum amount of data that can be read using a single read command is 4-bytes (When doing a 32-bit access).
- Fast Reads would be slower than regular reads as the SPI mode cannot be operated with an OMCLK greater than 50MHz.

## Examples

### Basic Example

This is a basic example of minimal use of the OSPI in an application.

```
#define OSPI_EXAMPLE_DATA_LENGTH (1024)
uint8_t g_dest[OSPI_EXAMPLE_DATA_LENGTH];

/* Place data in the .ospi_flash section to flash it during programming. */
const uint8_t g_src[OSPI_EXAMPLE_DATA_LENGTH] BSP_PLACE_IN_SECTION(".ospi_flash") =
"ABCDEFGHIJKLMNOPQRSTUVWXYZ";

/* Place code in the .code_in_ospi section to flash it during programming. */
void r_ospi_example_function(void) BSP_PLACE_IN_SECTION(".code_in_ospi")
__attribute__((noinline));

void r_ospi_example_function (void)
{
    /* Add code here. */
}

void r_ospi_basic_example (void)
{
    /* Open the OSPI instancee */
    fsp_err_t err = R_OSPI_Open(&g_ospi0_ctrl, &g_ospi0_cfg);
```

```
    handle_error(err);

    /* (Optional) Change SPI to DOPI mode */
    r_ospi_example_spi_to_dopi();

    /* After R_OSPI_Open() and any required device specific initialization, data can be
read directly from the OSPI flash. */
    memcpy(&g_dest[0], &g_src[0], OSPI_EXAMPLE_DATA_LENGTH);

    /* After R_OSPI_Open() and any required device specific initialization, functions in
the OSPI flash can be called. */
    r_ospi_example_function();
}
```

### Reading Status Register Example (R\_OSPI\_DirectWrite, R\_OSPI\_DirectRead)

This is an example of using R\_OSPI\_DirectWrite followed by R\_OSPI\_DirectRead to send the read status register command and read back the status register from the device.

```
#define OSPI_COMMAND_READ_STATUS_REGISTER (0x05U)

void r_ospi_direct_example (void)
{
    spi_flash_direct_transfer_t ospi_test_direct_transfer =
    {
        .command      = OSPI_TEST_READ_STATUS_COMMAND_SPI_MODE,
        .address      = 0U,
        .data         = 0U,
        .command_length = 1U,
        .address_length = 0U,
        .data_length  = 0U,
        .dummy_cycles = 0U
    };

    /* Open the OSPI instance. */
    fsp_err_t err = R_OSPI_Open(&g_ospi0_ctrl, &g_ospi0_cfg);
    handle_error(err);

    /* Write Enable */
    err = R_OSPI_DirectTransfer(&g_ospi0_ctrl, &ospi_test_direct_transfer,
SPI_FLASH_DIRECT_TRANSFER_DIR_WRITE);
}
```

```

    handle_error(err);
/* Read Status Register */
    ospi_test_direct_transfer.command      = OSPI_TEST_READ_STATUS_COMMAND_SPI_MODE;
    ospi_test_direct_transfer.data_length = 1U;
    err = R_OSPI_DirectTransfer(&g_ospi0_ctrl, &ospi_test_direct_transfer,
SPI_FLASH_DIRECT_TRANSFER_DIR_READ);
    handle_error(err);
/* Check if Write Enable is set */
if (OSPI_WEN_BIT_MASK != (ospi_test_direct_transfer.data & OSPI_WEN_BIT_MASK))
    {
        __BKPT(0);
    }
}

```

### Auto-calibration Example (R\_OSPI\_DirectOpen, R\_OSPI\_DirectWrite, R\_OSPI\_SpiProtocolSet)

This is an example of using R\_OSPI\_SpiProtocolSet to change the operating mode from SPI to SOPI and allow the driver to initiate auto-calibration.

```

#define OSPI_DOPI_PREAMBLE_PATTERN_LENGTH_BYTES (16U)
#define OSPI_EXAMPLE_PREAMBLE_ADDRESS (0x68000000U) /* Device connected to CS0 */
const uint8_t g_preamble_bytes[OSPI_DOPI_PREAMBLE_PATTERN_LENGTH_BYTES] =
{
    0x00, 0x00, 0xFF, 0xFF, 0xFF, 0x00, 0x08, 0x00, 0x00, 0xF7, 0xFF, 0x00, 0x08,
0xF7, 0x00, 0xF7
};
void ospi_example_wait_until_wip (void)
{
    fsp_err_t          err = FSP_SUCCESS;
    spi_flash_status_t status;

    status.write_in_progress = true;
    uint32_t timeout = UINT32_MAX;
    while ((status.write_in_progress) && (--timeout))
    {
        err = R_OSPI_StatusGet(&g_ospi0_ctrl, &status);
    }
}

```

```
        handle_error(err);
    }
    if (0 == timeout)
    {
        handle_error(err);
    }
}

void r_ospi_auto_calibrate_example (void)
{
    /* Open the OSPI instance. */
    /* Set data_latch_delay_clocks to 0x0 to enable auto-calibration */
    fsp_err_t err = R_OSPI_Open(&g_ospi0_ctrl, &g_ospi0_cfg);

    handle_error(err);

    uint8_t * preamble_pattern_addr = (uint8_t *) OSPI_EXAMPLE_PREAMBLE_ADDRESS;
    err = R_OSPI_Write(&g_ospi0_ctrl, g_preamble_bytes, preamble_pattern_addr,
OSPI_EXAMPLE_PREAMBLE_ADDRESS);

    handle_error(err);

    /* Wait until write has been completed */
    ospi_example_wait_until_wip();

    /* Change from SPI to DOPI mode */
    r_ospi_example_spi_to_dopi();
}
```

## OSPI Data and IAR

When using the IAR compiler, OSPI data must be const qualified to be downloaded by the debugger.

### Data Structures

struct [ospi\\_instance\\_ctrl\\_t](#)

### Enumerations

enum [ospi\\_device\\_number\\_t](#)

enum [ospi\\_command\\_cs\\_pullup\\_clocks\\_t](#)

enum [ospi\\_command\\_cs\\_pulldown\\_clocks\\_t](#)

## Data Structure Documentation

### ◆ `ospi_instance_ctrl_t`

```
struct ospi_instance_ctrl_t
```

Instance control block. DO NOT INITIALIZE. Initialization occurs when `spi_flash_api_t::open` is called

## Enumeration Type Documentation

### ◆ `ospi_device_number_t`

```
enum ospi_device_number_t
```

Enumerator

OSPI_DEVICE_NUMBER_0	Device connected to Chip-Select 0.
OSPI_DEVICE_NUMBER_1	Device connected to Chip-Select 1.

### ◆ `ospi_command_cs_pullup_clocks_t`

```
enum ospi_command_cs_pullup_clocks_t
```

Enumerator

OSPI_COMMAND_CS_PULLUP_CLOCKS_2	1.5 clocks DOPI mode; 2 Clocks all other modes; Unsupported for DOPI Read
OSPI_COMMAND_CS_PULLUP_CLOCKS_3	2.5 clocks DOPI mode; 3 Clocks all other modes; Unsupported for DOPI Read
OSPI_COMMAND_CS_PULLUP_CLOCKS_4	3.5 clocks DOPI mode; 4 Clocks all other modes; Unsupported for DOPI Read
OSPI_COMMAND_CS_PULLUP_CLOCKS_5	4.5 clocks DOPI mode; 5 Clocks all other modes; Unsupported for DOPI Read
OSPI_COMMAND_CS_PULLUP_CLOCKS_6	5.5 clocks DOPI mode; 6 Clocks all other modes; Unsupported for DOPI Read
OSPI_COMMAND_CS_PULLUP_CLOCKS_7	6.5 clocks DOPI mode; 7 Clocks all other modes
OSPI_COMMAND_CS_PULLUP_CLOCKS_8	7.5 clocks DOPI mode; 8 Clocks all other modes
OSPI_COMMAND_CS_PULLUP_CLOCKS_9	8.5 clocks DOPI mode; 9 Clocks all other modes

◆ **ospi\_command\_cs\_pulldown\_clocks\_t**

enum <code>ospi_command_cs_pulldown_clocks_t</code>	
Enumerator	
<code>OSPI_COMMAND_CS_PULLDOWN_CLOCKS_3</code>	2.5 clocks DOPI mode; 3 Clocks all other modes
<code>OSPI_COMMAND_CS_PULLDOWN_CLOCKS_4</code>	3.5 clocks DOPI mode; 4 Clocks all other modes
<code>OSPI_COMMAND_CS_PULLDOWN_CLOCKS_5</code>	4.5 clocks DOPI mode; 5 Clocks all other modes

**Function Documentation**◆ **R\_OSPI\_Open()**

```
fsp_err_t R_OSPI_Open ( spi_flash_ctrl_t* p_ctrl, spi_flash_cfg_t const *const p_cfg )
```

Open the OSPI driver module. After the driver is open, the OSPI can be accessed like internal flash memory.

Implements `spi_flash_api_t::open`.

Example:

```
/* Open the OSPI instancee */
fsp_err_t err = R_OSPI_Open(&g_ospi0_ctrl, &g_ospi0_cfg);
```

**Return values**

<code>FSP_SUCCESS</code>	Configuration was successful.
<code>FSP_ERR_ASSERTION</code>	The parameter <code>p_ctrl</code> or <code>p_cfg</code> is NULL.
<code>FSP_ERR_ALREADY_OPEN</code>	Driver has already been opened with the same <code>p_ctrl</code> .
<code>FSP_ERR_CALIBRATE_FAILED</code>	Failed to perform auto-calibrate.

◆ **R\_OSPI\_Close()**

```
fsp_err_t R_OSPI_Close ( spi_flash_ctrl_t* p_ctrl)
```

Close the OSPI driver module.

Implements `spi_flash_api_t::close`.

**Return values**

FSP_SUCCESS	Configuration was successful.
FSP_ERR_ASSERTION	p_instance_ctrl is NULL.
FSP_ERR_NOT_OPEN	Driver is not opened.

◆ **R\_OSPI\_DirectWrite()**

```
fsp_err_t R_OSPI_DirectWrite ( spi_flash_ctrl_t* p_ctrl, uint8_t const*const p_src, uint32_t const bytes, bool const read_after_write )
```

Writes raw data directly to the OctaFlash. API not supported. Use `R_OSPI_DirectTransfer`

Implements `spi_flash_api_t::directWrite`.

**Return values**

FSP_ERR_UNSUPPORTED	API not supported by OSPI.
---------------------	----------------------------

◆ **R\_OSPI\_DirectRead()**

```
fsp_err_t R_OSPI_DirectRead ( spi_flash_ctrl_t* p_ctrl, uint8_t*const p_dest, uint32_t const bytes )
```

Reads raw data directly from the OctaFlash. API not supported. Use `R_OSPI_DirectTransfer`.

Implements `spi_flash_api_t::directRead`.

**Return values**

FSP_ERR_UNSUPPORTED	API not supported by OSPI.
---------------------	----------------------------

◆ **R\_OSPI\_DirectTransfer()**

```
fsp_err_t R_OSPI_DirectTransfer ( spi_flash_ctrl_t * p_ctrl, spi_flash_direct_transfer_t *const
p_transfer, spi_flash_direct_transfer_dir_t direction )
```

Read/Write raw data directly with the OctaFlash.

Implements `spi_flash_api_t::directTransfer`.

Example:

```
/* Write Enable */
err = R_OSPI_DirectTransfer(&g_ospi0_ctrl, &ospi_test_direct_transfer,
SPI_FLASH_DIRECT_TRANSFER_DIR_WRITE);
handle_error(err);
```

**Return values**

FSP_SUCCESS	The flash was programmed successfully.
FSP_ERR_ASSERTION	A required pointer is NULL.
FSP_ERR_NOT_OPEN	Driver is not opened.

◆ **R\_OSPI\_SpiProtocolSet()**

```
fsp_err_t R_OSPI_SpiProtocolSet ( spi_flash_ctrl_t * p_ctrl, spi_flash_protocol_t spi_protocol )
```

Sets the SPI protocol.

Implements `spi_flash_api_t::spiProtocolSet`.

**Return values**

FSP_SUCCESS	SPI protocol updated on MCU peripheral.
FSP_ERR_ASSERTION	A required pointer is NULL.
FSP_ERR_NOT_OPEN	Driver is not opened.
FSP_ERR_CALIBRATE_FAILED	Failed to perform auto-calibrate.



◆ **R\_OSPI\_XipEnter()**

```
fsp_err_t R_OSPI_XipEnter ( spi_flash_ctrl_t * p_ctrl)
```

Enters Single Continuous Read/Write mode.

Implements `spi_flash_api_t::xipEnter`.

**Return values**

FSP_SUCCESS	The flash was programmed successfully.
FSP_ERR_ASSERTION	A required pointer is NULL.
FSP_ERR_NOT_OPEN	Driver is not opened.

◆ **R\_OSPI\_XipExit()**

```
fsp_err_t R_OSPI_XipExit ( spi_flash_ctrl_t * p_ctrl)
```

Exits XIP (execute in place) mode.

Implements `spi_flash_api_t::xipExit`.

**Return values**

FSP_SUCCESS	The flash was programmed successfully.
FSP_ERR_ASSERTION	A required pointer is NULL.
FSP_ERR_NOT_OPEN	Driver is not opened.

◆ **R\_OSPI\_Write()**

```
fsp_err_t R_OSPI_Write ( spi_flash_ctrl_t * p_ctrl, uint8_t const *const p_src, uint8_t *const p_dest,
uint32_t byte_count )
```

Program a page of data to the flash.

Implements `spi_flash_api_t::write`.

Example:

```
err = R_OSPI_Write(&g_ospi0_ctrl, g_preamble_bytes, preamble_pattern_addr,
OSPI_EXAMPLE_PREAMBLE_ADDRESS);
handle_error(err);
```

**Return values**

FSP_SUCCESS	The flash was programmed successfully.
FSP_ERR_ASSERTION	p_instance_ctrl, p_dest or p_src is NULL, or byte_count crosses a page boundary.
FSP_ERR_NOT_OPEN	Driver is not opened.
FSP_ERR_DEVICE_BUSY	Another Write/Erase transaction is in progress.

◆ **R\_OSPI\_Erase()**

```
fsp_err_t R_OSPI_Erase ( spi_flash_ctrl_t * p_ctrl, uint8_t *const p_device_address, uint32_t
byte_count )
```

Erase a block or sector of flash. The byte\_count must exactly match one of the erase sizes defined in `spi_flash_cfg_t`. For chip erase, byte\_count must be SPI\_FLASH\_ERASE\_SIZE\_CHIP\_ERASE.

Implements `spi_flash_api_t::erase`.

**Return values**

FSP_SUCCESS	The command to erase the flash was executed successfully.
FSP_ERR_ASSERTION	p_instance_ctrl or p_device_address is NULL, byte_count doesn't match an erase size defined in <code>spi_flash_cfg_t</code> , or byte_count is set to 0.
FSP_ERR_NOT_OPEN	Driver is not opened.
FSP_ERR_DEVICE_BUSY	The device is busy.

◆ **R\_OSPI\_StatusGet()**

```
fsp_err_t R_OSPI_StatusGet ( spi_flash_ctrl_t* p_ctrl, spi_flash_status_t*const p_status )
```

Gets the write or erase status of the flash.

Implements `spi_flash_api_t::statusGet`.

Example:

```
err = R_OSPI_StatusGet(&g_ospi0_ctrl, &status);
handle_error(err);
```

**Return values**

FSP_SUCCESS	The write status is in p_status.
FSP_ERR_ASSERTION	p_instance_ctrl or p_status is NULL.
FSP_ERR_NOT_OPEN	Driver is not opened.

◆ **R\_OSPI\_BankSet()**

```
fsp_err_t R_OSPI_BankSet ( spi_flash_ctrl_t* p_ctrl, uint32_t bank )
```

Selects the bank to access.

Implements `spi_flash_api_t::bankSet`.

**Return values**

FSP_ERR_UNSUPPORTED	API not supported by OSPI.
---------------------	----------------------------

◆ **R\_OSPI\_VersionGet()**

```
fsp_err_t R_OSPI_VersionGet ( fsp_version_t*const p_version)
```

Get the driver version based on compile time macros.

Implements `spi_flash_api_t::versionGet`.

**Return values**

FSP_SUCCESS	Successful close.
FSP_ERR_ASSERTION	p_version is NULL.

**4.2.36 Parallel Data Capture (r\_pdc)**

## Modules

### Functions

`fsp_err_t` [R\\_PDC\\_Open](#) (`pdc_ctrl_t *const p_api_ctrl`, `pdc_cfg_t const *const p_cfg`)

Powers on PDC, handles required initialization described in the hardware manual. [More...](#)

`fsp_err_t` [R\\_PDC\\_Close](#) (`pdc_ctrl_t *const p_api_ctrl`)

Stops and closes the transfer interface, disables and powers off the PDC, clears internal driver data and disables interrupts. [More...](#)

`fsp_err_t` [R\\_PDC\\_CaptureStart](#) (`pdc_ctrl_t *const p_api_ctrl`, `uint8_t *const p_buffer`)

Starts a capture. Enables interrupts. [More...](#)

`fsp_err_t` [R\\_PDC\\_VersionGet](#) (`fsp_version_t *const p_version`)

Return PDC HAL driver version. [More...](#)

### Detailed Description

Driver for the PDC peripheral on RA MCUs. This module implements the [PDC Interface](#).

## Overview

The PDC peripheral supports interfacing with external cameras by accepting timing and data signals in order to capture incoming data. A callback is invoked every time a frame of data is accepted.

### Features

- Capture incoming data into a user defined buffer
- Data bytes per pixel can be configured
- Endianess of the incoming data can be specified
- Supports configuring capture width and height
- Supports configuring vertical and horizontal sync polarity
- Horizontal and Vertical position for image/data capture can be specified
- External clock to the camera module can be adjusted
- Choice between DMA and DTC to transfer out the captured data
- The specified user callback is invoked when a data frame is captured

## Configuration

### Build Time Configurations for r\_pdc

The following build time configurations are defined in fsp\_cfg/r\_pdc\_cfg.h:

Configuration	Options	Default	Description
Parameter Checking	<ul style="list-style-type: none"> <li>Default (BSP)</li> <li>Enabled</li> <li>Disabled</li> </ul>	Default (BSP)	If selected code for parameter checking is included in the build.

### Configurations for Driver > Graphics > PDC Driver on r\_pdc

This module can be added to the Stacks tab via New Stack > Driver > Graphics > PDC Driver on r\_pdc.

Configuration	Options	Default	Description
General > Name	Name must be a valid C symbol	g_pdc0	Module name.
Input > Signal polarity > HSYNC	<ul style="list-style-type: none"> <li>High</li> <li>Low</li> </ul>	High	Specify the active polarity of the HSYNC signal.
Input > Signal polarity > VSYNC	<ul style="list-style-type: none"> <li>High</li> <li>Low</li> </ul>	High	Specify the active polarity of the VSYNC signal.
Input > Capture Specifications > Number of pixels to capture horizontally	Value must be an integer greater than 0	640	Specify the number of horizontal pixels to capture.
Input > Capture Specifications > Number of lines to capture vertically	Value must be an integer greater than 0	480	Specify the number of vertical pixels to capture.
Input > Capture Specifications > Horizontal pixel to start capture from	Value must be an integer	0	Specify the horizontal pixel to start capturing image data from. Allows an image smaller than the native resolution of a camera to be captured.
Input > Capture Specifications > Line to start capture from	Value must be an integer	0	Specify the vertical line to start capturing image data from. Allows an image smaller than the native resolution of a camera to be captured.
Input > Bytes per pixel	Value must be an integer greater than 0	2	Specify the number of bytes per pixel of the captured image data.
Input > Clock divider	<ul style="list-style-type: none"> <li>CLK/2</li> <li>CLK/4</li> </ul>	CLK/2	Specify the clock divider of the clock

	<ul style="list-style-type: none"> <li>• CLK/6</li> <li>• CLK/8</li> <li>• CLK/10</li> <li>• CLK/12</li> <li>• CLK/14</li> <li>• CLK/16</li> </ul>		input to the PDC peripheral.
Input > Endianness	<ul style="list-style-type: none"> <li>• Little</li> <li>• Big</li> </ul>	Little	Specify the endianness of the captured image data.
Output > Buffer > Image buffer name	Name must be a valid C symbol	g_user_buffer	Specify the name of the data buffer to create or set to NULL, if it is to be created by the user external to the PDC driver.
Output > Buffer > Image buffer section	This property must be a valid section name	.bss	Specify the RAM section for the image data buffer. Typically .bss (internal RAM) or .sdram. When Arm Compiler 6 is used to place this memory in on-chip SRAM, the section name must be .bss or start with .bss. to avoid consuming unnecessary ROM space.
Output > Buffer > Number of image buffers	Value must be an integer greater than 0	1	Specify the number of buffers to create.
Interrupts > Callback	Name must be a valid C symbol	g_pdc_user_callback	A user callback function must be provided. This callback is invoked for every successful frame capture and any error conditions
Interrupts > PDC Interrupt Priority	MCU Specific Options		Select the PDC interrupt priority.
Interrupts > DTC Interrupt Priority	MCU Specific Options		Select the DTC interrupt priority.

## Clock Configuration

The PDC peripheral module uses the PCLKB as its clock source. The maximum clock to the camera module is PCLKB / 2.

## Pin Configuration

The PCKO pin is a clock output and should be connected to the clock input of the camera. The PIXCLK

pin is a clock input and should be connected to the output pixel clock of the camera. Likewise, the HSYNC and VSYNC pins must be connected to the horizontal and vertical sync signals of the camera, respectively. The PIXD0-PIXD7 pins are the 8-bit data bus input and should be connected to the relevant output pins of the camera.

#### Note

*Camera control and serial communication pins must be configured separately and are not controlled by this module.*

## Usage Notes

### Interrupt Configuration

- PDC error interrupts are used by this module for reporting errors such as overrun, underrun, vertical line number setting and horizontal byte number setting errors.
- In addition to the PDC error interrupts, DMA or DTC interrupts are also used internally to perform data transfer from this peripheral to the specified image buffer.
- Receive data ready interrupt is used as activation source for DMA and DTC trigger.

### Enabling Transfer Modules

- An option to select between DMAC or DTC is provided with DMA as the default transfer choice.
- For further details on DMA please refer [Direct Memory Access Controller \(r\\_dmac\)](#)
- For further details on DTC please refer [Data Transfer Controller \(r\\_dtc\)](#)

### PDC setup with external camera

- Before configuring the external camera device the PDC Open API must be called in order to start clock output.
- Ensure that the memory pointed to by p\_buffer is both valid and large enough to store a complete image.
- The amount of space required (in bytes) can be calculated as: size (bytes) = image width (pixels) \* image height (lines) \* number of bytes per pixel
- Ensure that the size above is divisible by and aligned to 32 bytes.

## Examples

### Basic Example

This is a basic example of minimal use of the PDC in an application. This example shows how this driver can be used for capturing data from an external I/O device such as an image sensor.

```
void g_pdc_user_callback (pdc_callback_args_t * p_args)
{
    if (PDC_EVENT_TRANSFER_COMPLETE == p_args->event)
    {
        g_capture_ready = true;
    }
}
```

```
void basic_example (void)
{
    fsp_err_t err;

    /* Initialize the PDC module */
    err = R_PDC_Open(&g_pdc0_ctrl, &g_pdc0_cfg);

    /* Handle any errors. This function should be defined by the user. */
    handle_error(err);

    /* Initialize the camera module at this point. This implementation is camera vendor
specific. */
    camera_module_initialization();

    /* Initialize capture ready flag to false. This gets set to true in PDC callback
upon successful frame capture. */
    g_capture_ready = false;
    err = R_PDC_CaptureStart(&g_pdc0_ctrl, g_user_buffer);
    handle_error(err);

    uint32_t timeout_ms = PDC_DELAY_MS;

    /* Since there is nothing else to do, block until Callback triggers*/
    while ((true != g_capture_ready) && timeout_ms)
    {
        R_BSP_SoftwareDelay(1U, BSP_DELAY_UNITS_MILLISECONDS);
        timeout_ms--;;
    }
    if (0U == timeout_ms)
    {
        __BKPT(0);
    }
}

static void camera_module_initialization (void)
{
    /* Camera vendor specific initialization to be done here */
}
```

## Data Structures

```
struct pdc_instance_ctrl_t
```



## Data Structure Documentation

---

### ◆ pdc\_instance\_ctrl\_t

struct pdc_instance_ctrl_t
PDC instance control block. DO NOT INITIALIZE.

## Function Documentation

---

◆ **R\_PDC\_Open()**

```
fsp_err_t R_PDC_Open ( pdc_ctrl_t *const p_api_ctrl, pdc_cfg_t const *const p_cfg )
```

Powers on PDC, handles required initialization described in the hardware manual.

Implements `pdc_api_t::open`.

The Open function provides initial configuration for the PDC module. It powers on the module and enables the PCLKO output and the PIXCLK input. Further initialization requires the PIXCLK input to be running in order to be able to reset the PDC as part of its initialization. This clock is input from a camera module and so the reset and further initialization is performed in `pdc_api_t::captureStart`. This function should be called once prior to calling any other PDC API functions. After the PDC is opened the Open function should not be called again without first calling the Close function.

Example:

```
/* Initialize the PDC module */
err = R_PDC_Open(&g_pdc0_ctrl, &g_pdc0_cfg);
```

**Return values**

FSP_SUCCESS	Initialization was successful.
FSP_ERR_ASSERTION	One or more of the following parameters is NULL <ol style="list-style-type: none"> <li>1. p_cfg is NULL</li> <li>2. p_api_ctrl is NULL</li> <li>3. The pointer to the transfer interface in the p_cfg parameter is NULL</li> <li>3. Callback parameter is NULL.</li> <li>4. Invalid IRQ number assigned</li> </ol>
FSP_ERR_INVALID_ARGUMENT	One or more of the following parameters is incorrect <ol style="list-style-type: none"> <li>1. bytes_per_pixel is zero</li> <li>2. x_capture_pixels is zero</li> <li>3. y_capture_pixels is zero</li> <li>4. x_capture_start_pixel + x_capture_pixels is greater than 4095, OR</li> <li>5. y_capture_start_pixel + y_capture_pixels is greater than 4095</li> </ol>
FSP_ERR_ALREADY_OPEN	Module is already open.

◆ **R\_PDC\_Close()**

```
fsp_err_t R_PDC_Close ( pdc_ctrl_t *const p_api_ctrl)
```

Stops and closes the transfer interface, disables and powers off the PDC, clears internal driver data and disables interrupts.

Implements `pdc_api_t::close`.

**Return values**

FSP_SUCCESS	Successful close.
FSP_ERR_ASSERTION	<code>p_api_ctrl</code> is NULL
FSP_ERR_NOT_OPEN	Open has not been successfully called.

◆ **R\_PDC\_CaptureStart()**

```
fsp_err_t R_PDC_CaptureStart ( pdc_ctrl_t *const p_api_ctrl, uint8_t *const p_buffer )
```

Starts a capture. Enables interrupts.

Implements `pdc_api_t::captureStart`.

Sets up the transfer interface to transfer data from the PDC into the specified buffer. Configures the PDC settings as previously set by the `pdc_api_t::open` API. These settings are configured here as the PIXCLK input must be active for the PDC reset operation. When a capture is complete the callback registered during `pdc_api_t::open` API call will be called.

Example:

```
err = R_PDC_CaptureStart(&g_pdc0_ctrl, g_user_buffer);
handle_error(err);
```

**Return values**

FSP_SUCCESS	Capture start successful.
FSP_ERR_ASSERTION	One or more of the following parameters is NULL <ul style="list-style-type: none"> <li>1. <code>p_api_ctrl</code> is NULL</li> <li>2. <code>p_buffer</code> is NULL while <code>p_buffer</code> field of the control structure is NULL</li> </ul>
FSP_ERR_NOT_OPEN	Open has not been successfully called.
FSP_ERR_IN_USE	PDC transfer is already in progress.
FSP_ERR_TIMEOUT	Reset operation timed out.

**◆ R\_PDC\_VersionGet()**

```
fsp_err_t R_PDC_VersionGet ( fsp_version_t *const p_version)
```

Return PDC HAL driver version.

Implements `pdc_api_t::versionGet`.

**Return values**

FSP_SUCCESS	Version information successfully read.
FSP_ERR_ASSERTION	p_version is NULL

**Note**

*This function is reentrant.*

**4.2.37 Port Output Enable for GPT (r\_poeg)**

## Modules

**Functions**

```
fsp_err_t R_POEG_Open (poeg_ctrl_t *const p_ctrl, poeg_cfg_t const *const p_cfg)
```

```
fsp_err_t R_POEG_StatusGet (poeg_ctrl_t *const p_ctrl, poeg_status_t *const p_status)
```

```
fsp_err_t R_POEG_CallbackSet (poeg_ctrl_t *const p_ctrl, void(*p_callback)(poeg_callback_args_t *), void const *const p_context, poeg_callback_args_t *const p_callback_memory)
```

```
fsp_err_t R_POEG_OutputDisable (poeg_ctrl_t *const p_ctrl)
```

```
fsp_err_t R_POEG_Reset (poeg_ctrl_t *const p_ctrl)
```

```
fsp_err_t R_POEG_Close (poeg_ctrl_t *const p_ctrl)
```

```
fsp_err_t R_POEG_VersionGet (fsp_version_t *const p_version)
```

**Detailed Description**

Driver for the POEG peripheral on RA MCUs. This module implements the [POEG Interface](#).

**Overview**

The POEG module can be used to configure events to disable GPT GTIOC output pins.

## Features

The POEG module has the following features:

- Supports disabling GPT output pins based on GTETRГ input pin level.
- Supports disabling GPT output pins based on comparator crossing events (configurable in the [High-Speed Analog Comparator \(r\\_acmphs\)](#) driver).
- Supports disabling GPT output pins when GTIOC pins are the same level (configurable in the [General PWM Timer \(r\\_gpt\)](#) driver).
- Supports disabling GPT output pins when main oscillator stop is detected.
- Supports disabling GPT output pins by software API.
- Supports notifying the application when GPT output pins are disabled by POEG.
- Supports resetting POEG status.

## Configuration

### Build Time Configurations for r\_poeg

The following build time configurations are defined in fsp\_cfg/r\_poeg\_cfg.h:

Configuration	Options	Default	Description
Parameter Checking	<ul style="list-style-type: none"> <li>• Default (BSP)</li> <li>• Enabled</li> <li>• Disabled</li> </ul>	Default (BSP)	If selected code for parameter checking is included in the build.

### Configurations for Driver > Timers > Port Output Enable for GPT on r\_poeg

This module can be added to the Stacks tab via New Stack > Driver > Timers > Port Output Enable for GPT on r\_poeg. Non-secure callable guard functions can be generated for this module by right clicking the module in the RA Configuration tool and checking the "Non-secure Callable" box.

Configuration	Options	Default	Description
General > Name	Name must be a valid C symbol	g_poeg0	Module name.
General > Channel	Must be a valid POEG channel	0	Specify the hardware channel.
General > Trigger	MCU Specific Options		Select the trigger sources that will enable POEG. Software disable is always supported. This configuration can only be set once after reset. It cannot be modified after the initial setting.
Input > GTETRГ Polarity	<ul style="list-style-type: none"> <li>• Active High</li> <li>• Active Low</li> </ul>	Active High	Select the polarity of the GTETRГ pin. Only applicable if GTETRГ pin is selected under

Input > GTETRGR Noise Filter	<ul style="list-style-type: none"> <li>• Disabled</li> <li>• PCLKB/1</li> <li>• PCLKB/8</li> <li>• PCLKB/32</li> <li>• PCLKB/128</li> </ul>	Disabled	Trigger. Configure the noise filter for the GTETRGR pin. Only applicable if GTETRGR pin is selected under Trigger.
Interrupts > Callback	Name must be a valid C symbol	NULL	A user callback function can be specified here. If this callback function is provided, it will be called from the interrupt service routine (ISR) when GPT output pins are disabled by POEG.
Interrupts > Interrupt Priority	MCU Specific Options		Select the POEG interrupt priority.

## Clock Configuration

The POEG clock is based on the PCLKB frequency.

## Pin Configuration

This module can use GTETRGA, GTETRGR, GTETRGC, or GTETRGD as an input signal to disable GPT output pins.

## Usage Notes

### POEG GTETRGR Pin and Channel

The POEG channel number corresponds to the GTETRGR input pin that can be used with the channel. GTETRGA must be used with POEG channel 0, GTETRGR must be used with POEG channel 1, etc.

### Limitations

The user should be aware of the following limitations when using POEG:

- The POEG trigger source can only be set once per channel. Modifying the POEG trigger source after it is set is not allowed by the hardware.
- The POEG cannot be disabled using this API. The interrupt is disabled in [R\\_POEG\\_Close\(\)](#), but the POEG will still disable the GPT output pins if a trigger is detected even if the module is closed.

## Examples

### POEG Basic Example

This is a basic example of minimal use of the POEG in an application.



```
void poeg_basic_example (void)
{
    fsp_err_t err = FSP_SUCCESS;
    /* Initializes the POEG. */
    err = R_POEG_Open(&g_poeg0_ctrl, &g_poeg0_cfg);
    /* Handle any errors. This function should be defined by the user. */
    handle_error(err);
}
```

### POEG Callback Example

This is an example of a using the POEG callback to restore GPT output operation.

```
/* Example callback called when POEG disables GPT output pins. */
void poeg_callback (poeg_callback_args_t * p_args)
{
    FSP_PARAMETER_NOT_USED(p_args);
    /* (Optional) Determine the cause of the POEG event. */
    poeg_status_t status;
    (void) R_POEG_StatusGet(&g_poeg0_ctrl, &status);
    /* Correct the cause of the POEG event before resetting POEG. */
    /* Reset the POEG before exiting the callback. */
    (void) R_POEG_Reset(&g_poeg0_ctrl);
    /* Wait for the status to clear after reset before exiting the callback to ensure
the interrupt does not fire
    * again. */
    do
    {
        (void) R_POEG_StatusGet(&g_poeg0_ctrl, &status);
    } while (POEG_STATE_NO_DISABLE_REQUEST != status.state);
    /* Alternatively, if the POEG cannot be reset, disable the POEG interrupt to prevent
it from firing continuously.
    * Update the 0 in the macro below to match the POEG channel number. */
    NVIC_DisableIRQ(VECTOR_NUMBER_POEG0_EVENT);
}
```

## Data Structures

```
struct poeg_instance_ctrl_t
```

## Data Structure Documentation

### ◆ poeg\_instance\_ctrl\_t

```
struct poeg_instance_ctrl_t
```

Channel control block. DO NOT INITIALIZE. Initialization occurs when `poeg_api_t::open` is called.

## Function Documentation

### ◆ R\_POEG\_Open()

```
fsp_err_t R_POEG_Open ( poeg_ctrl_t *const p_ctrl, poeg_cfg_t const *const p_cfg )
```

Initializes the POEG module and applies configurations. Implements `poeg_api_t::open`.

#### Note

*The `poeg_cfg_t::trigger` setting can only be configured once after reset. Reopening with a different trigger configuration is not possible.*

#### Example:

```
/* Initializes the POEG. */
err = R_POEG_Open(&g_poeg0_ctrl, &g_poeg0_cfg);
```

## Return values

FSP_SUCCESS	Initialization was successful.
FSP_ERR_ASSERTION	A required input pointer is NULL or the source divider is invalid.
FSP_ERR_ALREADY_OPEN	Module is already open.
FSP_ERR_IRQ_BSP_DISABLED	<code>poeg_cfg_t::p_callback</code> is not NULL, but ISR is not enabled. ISR must be enabled to use callback.
FSP_ERR_IP_CHANNEL_NOT_PRESENT	The channel requested in the <code>p_cfg</code> parameter is not available on this device.



◆ **R\_POEG\_StatusGet()**

```
fsp_err_t R_POEG_StatusGet ( poeg_ctrl_t *const p_ctrl, poeg_status_t *const p_status )
```

Get current POEG status and store it in provided pointer p\_status. Implements `poeg_api_t::statusGet`.

Example:

```
/* (Optional) Determine the cause of the POEG event. */
poeg_status_t status;

(void) R_POEG_StatusGet(&g_poeg0_ctrl, &status);
```

**Return values**

FSP_SUCCESS	Current POEG state stored successfully.
FSP_ERR_ASSERTION	p_ctrl or p_status was NULL.
FSP_ERR_NOT_OPEN	The instance is not opened.

◆ **R\_POEG\_CallbackSet()**

```
fsp_err_t R_POEG_CallbackSet ( poeg_ctrl_t *const p_ctrl, void (*)(poeg_callback_args_t *)
p_callback, void const *const p_context, poeg_callback_args_t *const p_callback_memory )
```

Updates the user callback with the option to provide memory for the callback argument structure. Implements `poeg_api_t::callbackSet`.

**Return values**

FSP_SUCCESS	Callback updated successfully.
FSP_ERR_ASSERTION	A required pointer is NULL.
FSP_ERR_NOT_OPEN	The control block has not been opened.
FSP_ERR_NO_CALLBACK_MEMORY	p_callback is non-secure and p_callback_memory is either secure or NULL.

◆ **R\_POEG\_OutputDisable()**

```
fsp_err_t R_POEG_OutputDisable ( poeg_ctrl_t *const p_ctrl)
```

Disables GPT output pins. Implements `poeg_api_t::outputDisable`.

**Return values**

FSP_SUCCESS	GPT output pins successfully disabled.
FSP_ERR_ASSERTION	p_ctrl was NULL.
FSP_ERR_NOT_OPEN	The instance is not opened.

◆ **R\_POEG\_Reset()**

```
fsp_err_t R_POEG_Reset ( poeg_ctrl_t *const p_ctrl)
```

Resets status flags. Implements `poeg_api_t::reset`.

**Note**

*Status flags are only reset if the original POEG trigger is resolved. Check the status using [R\\_POEG\\_StatusGet](#) after calling this function to verify the status is cleared.*

**Example:**

```
/* Correct the cause of the POEG event before resetting POEG. */
/* Reset the POEG before exiting the callback. */
(void) R_POEG_Reset(&g_poeg0_ctrl);
/* Wait for the status to clear after reset before exiting the callback to ensure
the interrupt does not fire
* again. */
do
{
(void) R_POEG_StatusGet(&g_poeg0_ctrl, &status);
} while (POEG_STATE_NO_DISABLE_REQUEST != status.state);
```

**Return values**

FSP_SUCCESS	Function attempted to clear status flags.
FSP_ERR_ASSERTION	p_ctrl was NULL.
FSP_ERR_NOT_OPEN	The instance is not opened.

◆ **R\_POEG\_Close()**

```
fsp_err_t R_POEG_Close ( poeg_ctrl_t *const p_ctrl)
```

Disables POEG interrupt. Implements `poeg_api_t::close`.

**Note**

*This function does not disable the POEG.*

**Return values**

FSP_SUCCESS	Successful close.
FSP_ERR_ASSERTION	p_ctrl was NULL.
FSP_ERR_NOT_OPEN	The instance is not opened.

◆ **R\_POEG\_VersionGet()**

```
fsp_err_t R_POEG_VersionGet ( fsp_version_t *const p_version)
```

Sets driver version based on compile time macros. Implements `poeg_api_t::versionGet`.

**Return values**

FSP_SUCCESS	Version stored in p_version.
FSP_ERR_ASSERTION	p_version was NULL.

**4.2.38 Quad Serial Peripheral Interface Flash (r\_qsapi)**

## Modules

**Functions**

```
fsp_err_t R_QSPI_Open (spi_flash_ctrl_t *p_ctrl, spi_flash_cfg_t const *const p_cfg)
```

```
fsp_err_t R_QSPI_Close (spi_flash_ctrl_t *p_ctrl)
```

```
fsp_err_t R_QSPI_DirectWrite (spi_flash_ctrl_t *p_ctrl, uint8_t const *const p_src, uint32_t const bytes, bool const read_after_write)
```

```
fsp_err_t R_QSPI_DirectRead (spi_flash_ctrl_t *p_ctrl, uint8_t *const p_dest, uint32_t const bytes)
```

```
fsp_err_t R_QSPI_SpiProtocolSet (spi_flash_ctrl_t *p_ctrl, spi_flash_protocol_t
```

	spi_protocol)
fsp_err_t	R_QSPI_XipEnter (spi_flash_ctrl_t *p_ctrl)
fsp_err_t	R_QSPI_XipExit (spi_flash_ctrl_t *p_ctrl)
fsp_err_t	R_QSPI_Write (spi_flash_ctrl_t *p_ctrl, uint8_t const *const p_src, uint8_t *const p_dest, uint32_t byte_count)
fsp_err_t	R_QSPI_Erase (spi_flash_ctrl_t *p_ctrl, uint8_t *const p_device_address, uint32_t byte_count)
fsp_err_t	R_QSPI_StatusGet (spi_flash_ctrl_t *p_ctrl, spi_flash_status_t *const p_status)
fsp_err_t	R_QSPI_BankSet (spi_flash_ctrl_t *p_ctrl, uint32_t bank)
fsp_err_t	R_QSPI_VersionGet (fsp_version_t *const p_version)

## Detailed Description

Driver for the QSPI peripheral on RA MCUs. This module implements the [SPI Flash Interface](#).

## Overview

### Features

The QSPI driver has the following key features:

- Memory mapped read access to the QSPI flash
- Programming the QSPI flash device
- Erasing the QSPI flash device
- Sending device specific commands and reading back responses
- Entering and exiting QPI mode
- Entering and exiting XIP mode
- 3 or 4 byte addressing

## Configuration

### Build Time Configurations for r\_qspi

The following build time configurations are defined in driver/r\_qspi\_cfg.h:

Configuration	Options	Default	Description
Parameter Checking Enable	<ul style="list-style-type: none"> <li>• Default (BSP)</li> <li>• Enabled</li> <li>• Disabled</li> </ul>	Default (BSP)	If selected code for parameter checking is included in the build.
Support Multiple Line Program in Extended	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Disabled	If selected code for programming on

SPI Mode

multiple lines in extended SPI mode is included in the build.

### Configurations for Driver > Storage > QSPI Driver on r\_qspi

This module can be added to the Stacks tab via New Stack > Driver > Storage > QSPI Driver on r\_qspi.

Configuration	Options	Default	Description
General > Name	Name must be a valid C symbol	g_qspi0	Module name.
General > SPI Protocol	<ul style="list-style-type: none"> <li>Extended SPI</li> <li>QPI</li> </ul>	Extended SPI	Select the initial SPI protocol. SPI protocol can be changed in R_QSPI_Direct().
General > Address Bytes	<ul style="list-style-type: none"> <li>3</li> <li>4</li> <li>4 with 4-byte read code</li> </ul>	3	Select the number of address bytes. Selecting '4 with 4-byte read code' converts the default read code determined in Read Mode to the 4-byte version. If 4-byte mode is selected without using 4-byte commands, the application must issue the EN4B command using R_QSPI_Direct().
General > Read Mode	<ul style="list-style-type: none"> <li>Standard</li> <li>Fast Read</li> <li>Fast Read Dual Output</li> <li>Fast Read Dual I/O</li> <li>Fast Read Quad Output</li> <li>Fast Read Quad I/O</li> </ul>	Fast Read Quad I/O	Select the read mode for memory mapped access.
General > Dummy Clocks for Fast Read	Refer to the RA Configuration tool for available options.	Default	Select the number of dummy clocks for fast read operations. Default is 6 clocks for Fast Read Quad I/O, 4 clocks for Fast Read Dual I/O, and 8 clocks for other fast read instructions including Fast Read Quad Output, Fast Read Dual Output, and Fast Read

General > Page Size Bytes	Must be an integer greater than 0	256	The maximum number of bytes allowed for a single write.
Command Definitions > Page Program Command	Must be an 8-bit QSPI command	0x02	The command to program a page. If 'Support Multiple Line Program in Extended SPI Mode' is Enabled, this command must use the same number of data lines as the selected read mode.
Command Definitions > Page Program Address Lines	<ul style="list-style-type: none"> <li>• 1</li> <li>• 2</li> <li>• 4</li> </ul>	1	Select the number of lines to use for the address bytes during write operations. This can be determined by referencing the datasheet for the external QSPI. It should either be 1 or match the number of data lines used for memory mapped fast read operations.
Command Definitions > Write Enable Command	Must be an 8-bit QSPI command	0x06	The command to enable write.
Command Definitions > Status Command	Must be an 8-bit QSPI command	0x05	The command to query the status of a write or erase command.
Command Definitions > Write Status Bit	Must be an integer between 0 and 7	0	Which bit contains the write in progress status returned from the Write Status Command.
Command Definitions > Sector Erase Command	Must be an 8-bit QSPI command	0x20	The command to erase a sector. Set Sector Erase Size to 0 if unused.
Command Definitions > Sector Erase Size	Must be an integer greater than or equal to 0	4096	The sector erase size. Set Sector Erase Size to 0 if Sector Erase is not supported.
Command Definitions > Block Erase Command	Must be an 8-bit QSPI command	0xD8	The command to erase a block. Set Block Erase Size to 0 if unused.
Command Definitions	Must be an integer	65536	The block erase size.

> Block Erase Size	greater than or equal to 0		Set Block Erase Size to 0 if Block Erase is not supported.
Command Definitions > Block Erase 32KB Command	Must be an 8-bit QSPI command	0x52	The command to erase a 32KB block. Set Block Erase Size to 0 if unused.
Command Definitions > Block Erase 32KB Size	Must be an integer greater than or equal to 0	32768	The block erase 32KB size. Set Block Erase 32KB Size to 0 if Block Erase 32KB is not supported.
Command Definitions > Chip Erase Command	Must be an 8-bit QSPI command	0xC7	The command to erase the entire chip. Set Chip Erase Command to 0 if unused.
Command Definitions > XIP Enter M7-M0	Must be an 8-bit QSPI command	0x20	How to set M7-M0 to enter XIP mode.
Command Definitions > XIP Exit M7-M0	Must be an 8-bit QSPI command	0xFF	How to set M7-M0 exit XIP mode.
Bus Timing > QSPKCLK Divisor	Refer to the RA Configuration tool for available options.	2	Select the divisor to apply to PCLK to get QSPCLK.
Bus Timing > Minimum QSSL Deselect Cycles	Refer to the RA Configuration tool for available options.	4 QSPCLK	Define the minimum number of QSPCLK cycles for QSSL to remain high between operations.

## Clock Configuration

The QSPI clock is derived from PCLKA.

## Pin Configuration

The following pins are available to connect to an external QSPI device:

- QSPCLK: QSPI clock output
- QSSL: QSPI slave select
- QIO0: Data 0 I/O
- QIO1: Data 1 I/O
- QIO2: Data 2 I/O
- QIO3: Data 3 I/O

### Note

*It is recommended to configure the pins with `IOPORT_CFG_DRIVE_HIGH`.*

## Usage Notes

### QSPI Memory Mapped Access

After `R_QSPI_Open()` completes successfully, the QSPI flash device contents are mapped to address 0x60000000 and can be read like on-chip flash.

## Limitations

Developers should be aware of the following limitations when using the QSPI driver:

- Only P305-P310 are currently supported by the J-Link driver to flash the QSPI.
- The default J-Link downloader requires the device to be in extended SPI mode (not QPI mode).

## Examples

### Basic Example

This is a basic example of minimal use of the QSPI in an application.

```
#define QSPI_EXAMPLE_DATA_LENGTH (1024)
uint8_t g_dest[QSPI_EXAMPLE_DATA_LENGTH];
/* Place data in the .qspi_flash section to flash it during programming. */
const uint8_t g_src[QSPI_EXAMPLE_DATA_LENGTH] BSP_PLACE_IN_SECTION(".qspi_flash") =
"ABCDEFGHIJKLMNPOQRSTUVWXYZ";
/* Place code in the .code_in_qspi section to flash it during programming. */
void r_qspi_example_function(void) BSP_PLACE_IN_SECTION(".code_in_qspi")
__attribute__((noinline));
void r_qspi_example_function (void)
{
    /* Add code here. */
}
void r_qspi_basic_example (void)
{
    /* Open the QSPI instance. */
    fsp_err_t err = R_QSPI_Open(&g_qspi0_ctrl, &g_qspi0_cfg);
    handle_error(err);
    /* (Optional) Send device specific initialization commands. */
    r_qspi_example_init();
    /* After R_QSPI_Open() and any required device specific initialization, data can be
read directly from the QSPI flash. */
    memcpy(&g_dest[0], &g_src[0], QSPI_EXAMPLE_DATA_LENGTH);
    /* After R_QSPI_Open() and any required device specific initialization, functions in
```



```
the QSPI flash can be called. */
    r_qspi_example_function();
}
```

## Initialization Command Structure Example

This is an example of the types of commands that can be used to initialize the QSPI.

```
#define QSPI_COMMAND_WRITE_ENABLE (0x06U)
#define QSPI_COMMAND_WRITE_STATUS_REGISTER (0x01U)
#define QSPI_COMMAND_ENTER_QPI_MODE (0x38U)
#define QSPI_EXAMPLE_STATUS_REGISTER_1 (0x40)
#define QSPI_EXAMPLE_STATUS_REGISTER_2 (0x00)
static void r_qspi_example_init (void)
{
    /* Write status registers */
    /* Write one byte to enable writing to the status register, then deassert QSSL. */
    uint8_t data[4];
    fsp_err_t err;
    data[0] = QSPI_COMMAND_WRITE_ENABLE;
    err = R_QSPI_DirectWrite(&g_qspi0_ctrl, &data[0], 1, false);
    handle_error(err);
    /* Write 3 bytes, including the write status register command followed by values for
both status registers. In the
    * status registers, set QE to 1 and other bits to their default setting. After all
data is written, deassert the
    * QSSL line. */
    data[0] = QSPI_COMMAND_WRITE_STATUS_REGISTER;
    data[1] = QSPI_EXAMPLE_STATUS_REGISTER_1;
    data[2] = QSPI_EXAMPLE_STATUS_REGISTER_2;
    err = R_QSPI_DirectWrite(&g_qspi0_ctrl, &data[0], 3, false);
    handle_error(err);
    /* Wait for status register to update. */
    spi_flash_status_t status;
    do
```

```

{
    (void) R_QSPI_StatusGet(&g_qspi0_ctrl, &status);
} while (true == status.write_in_progress);
/* Write one byte to enter QSPI mode, then deassert QSSL. After entering QPI mode on
the device, change the SPI
* protocol to QPI mode on the MCU peripheral. */
data[0] = QSPI_COMMAND_ENTER_QPI_MODE;
err     = R_QSPI_DirectWrite(&g_qspi0_ctrl, &data[0], 1, false);
handle_error(err);
(void) R_QSPI_SpiProtocolSet(&g_qspi0_ctrl, SPI_FLASH_PROTOCOL_QPI);
}

```

### Reading Status Register Example (R\_QSPI\_DirectWrite, R\_QSPI\_DirectRead)

This is an example of using R\_QSPI\_DirectWrite followed by R\_QSPI\_DirectRead to send the read status register command and read back the status register from the device.

```

#define QSPI_COMMAND_READ_STATUS_REGISTER (0x05U)
void r_qspi_direct_example (void)
{
    /* Read a status register. */
    /* Write one byte to read the status register. Do not deassert QSSL. */
    uint8_t data;
    fsp_err_t err;
    data = QSPI_COMMAND_READ_STATUS_REGISTER;
    err = R_QSPI_DirectWrite(&g_qspi0_ctrl, &data, 1, true);
    handle_error(err);
    /* Read one byte. After all data is read, deassert the QSSL line. */
    err = R_QSPI_DirectRead(&g_qspi0_ctrl, &data, 1);
    handle_error(err);
    /* Status register contents are available in variable 'data'. */
}

```

### Querying Device Size Example (R\_QSPI\_DirectWrite, R\_QSPI\_DirectRead)

This is an example of using R\_QSPI\_DirectWrite followed by R\_QSPI\_DirectRead to query the device

size.

```
#define QSPI_EXAMPLE_COMMAND_READ_ID (0x9F)
#define QSPI_EXAMPLE_COMMAND_READ_SFDP (0x5A)
void r_qspi_size_example (void)
{
    /* Many QSPI devices support more than one way to query the device size. Consult the
    datasheet for your
    * QSPI device to determine which of these methods are supported (if any). */
    uint32_t device_size_bytes;
    fsp_err_t err;
#ifdef QSPI_EXAMPLE_COMMAND_READ_ID
    /* This example shows how to get the device size by reading the manufacturer ID. */
    uint8_t data[4];
    data[0] = QSPI_EXAMPLE_COMMAND_READ_ID;
    err = R_QSPI_DirectWrite(&g_qspi0_ctrl, &data[0], 1, true);
    handle_error(err);
    /* Read 3 bytes. The third byte often represents the size of the QSPI, where the
    size of the QSPI = 2 ^ N. */
    err = R_QSPI_DirectRead(&g_qspi0_ctrl, &data[0], 3);
    handle_error(err);
    device_size_bytes = 1U << data[2];
    FSP_PARAMETER_NOT_USED(device_size_bytes);
#endif
#ifdef QSPI_EXAMPLE_COMMAND_READ_SFDP
    /* Read the JEDEC SFDP header to locate the JEDEC flash parameters table. Reference
    JESD216 "Serial Flash
    * Discoverable Parameters (SFDP)". */
    /* Send the standard 0x5A command followed by 3 address bytes (SFDP header is at
    address 0). */
    uint8_t buffer[16];
    memset(&buffer[0], 0, sizeof(buffer));
    buffer[0] = QSPI_EXAMPLE_COMMAND_READ_SFDP;
    err = R_QSPI_DirectWrite(&g_qspi0_ctrl, &buffer[0], 4, true);
    handle_error(err);

```

```
/* Read out 16 bytes (1 dummy byte followed by 15 data bytes). */
err = R_QSPI_DirectRead(&g_qspi0_ctrl, &buffer[0], 16);
handle_error(err);

/* Read the JEDEC flash parameters to locate the memory size. */
/* Send the standard 0x5A command followed by 3 address bytes (located in big endian
order at offset 0xC-0xE).
* These bytes are accessed at 0xD-0xF because the first byte read is a dummy byte.
*/
buffer[0] = QSPI_EXAMPLE_COMMAND_READ_SFDP;
buffer[1] = buffer[0xF];
buffer[2] = buffer[0xE];
buffer[3] = buffer[0xD];
err      = R_QSPI_DirectWrite(&g_qspi0_ctrl, &buffer[0], 4, true);
handle_error(err);

/* Read out 9 bytes (1 dummy byte followed by 8 data bytes). */
err = R_QSPI_DirectRead(&g_qspi0_ctrl, &buffer[0], 9);
handle_error(err);

/* Read the memory density (located in big endian order at offset 0x4-0x7). These
bytes are accessed at 0x5-0x8
* because the first byte read is a dummy byte. */
uint32_t memory_density = (uint32_t) ((buffer[8] << 24) | (buffer[7] << 16) |
(buffer[6] << 8) | buffer[5]);
if ((1U << 31) & memory_density)
{
/* For densities 4 gigabits and above, bit-31 is set to 1b. The field 30:0 defines
'N' where the density is
* computed as 2^N bits (N must be >= 32). This code subtracts 3 from N to divide by
8 to get the size in
* bytes instead of bits. */
device_size_bytes = 1U << ((memory_density & ~(1U << 31)) - 3U);
}
else
{
/* For densities 2 gigabits or less, bit-31 is set to 0b. The field 30:0 defines the
```

```
size in bits. This
 * code divides the memory density by 8 to get the size in bytes instead of bits. */
    device_size_bytes = (memory_density / 8) + 1;
}
FSP_PARAMETER_NOT_USED(device_size_bytes);
#endif
}
```

## Data Structures

struct [qspi\\_instance\\_ctrl\\_t](#)

## Enumerations

enum [qspi\\_qssl\\_min\\_high\\_level\\_t](#)

enum [qspi\\_qspclk\\_div\\_t](#)

## Data Structure Documentation

### ◆ [qspi\\_instance\\_ctrl\\_t](#)

struct [qspi\\_instance\\_ctrl\\_t](#)

Instance control block. DO NOT INITIALIZE. Initialization occurs when [spi\\_flash\\_api\\_t::open](#) is called

## Enumeration Type Documentation

◆ **qspi\_qssl\_min\_high\_level\_t**

enum qspi_qssl_min_high_level_t	
Enumerator	
QSPI_QSSL_MIN_HIGH_LEVEL_1_QSPCLK	QSSL deselected for at least 1 QSPCLK.
QSPI_QSSL_MIN_HIGH_LEVEL_2_QSPCLK	QSSL deselected for at least 2 QSPCLK.
QSPI_QSSL_MIN_HIGH_LEVEL_3_QSPCLK	QSSL deselected for at least 3 QSPCLK.
QSPI_QSSL_MIN_HIGH_LEVEL_4_QSPCLK	QSSL deselected for at least 4 QSPCLK.
QSPI_QSSL_MIN_HIGH_LEVEL_5_QSPCLK	QSSL deselected for at least 5 QSPCLK.
QSPI_QSSL_MIN_HIGH_LEVEL_6_QSPCLK	QSSL deselected for at least 6 QSPCLK.
QSPI_QSSL_MIN_HIGH_LEVEL_7_QSPCLK	QSSL deselected for at least 7 QSPCLK.
QSPI_QSSL_MIN_HIGH_LEVEL_8_QSPCLK	QSSL deselected for at least 8 QSPCLK.
QSPI_QSSL_MIN_HIGH_LEVEL_9_QSPCLK	QSSL deselected for at least 9 QSPCLK.
QSPI_QSSL_MIN_HIGH_LEVEL_10_QSPCLK	QSSL deselected for at least 10 QSPCLK.
QSPI_QSSL_MIN_HIGH_LEVEL_11_QSPCLK	QSSL deselected for at least 11 QSPCLK.
QSPI_QSSL_MIN_HIGH_LEVEL_12_QSPCLK	QSSL deselected for at least 12 QSPCLK.
QSPI_QSSL_MIN_HIGH_LEVEL_13_QSPCLK	QSSL deselected for at least 13 QSPCLK.
QSPI_QSSL_MIN_HIGH_LEVEL_14_QSPCLK	QSSL deselected for at least 14 QSPCLK.
QSPI_QSSL_MIN_HIGH_LEVEL_15_QSPCLK	QSSL deselected for at least 15 QSPCLK.
QSPI_QSSL_MIN_HIGH_LEVEL_16_QSPCLK	QSSL deselected for at least 16 QSPCLK.

◆ **qspi\_qspclk\_div\_t**

enum <code>qspi_qspclk_div_t</code>	
Enumerator	
<code>QSPI_QSPCLK_DIV_2</code>	$QSPCLK = PCLK / 2.$
<code>QSPI_QSPCLK_DIV_3</code>	$QSPCLK = PCLK / 3.$
<code>QSPI_QSPCLK_DIV_4</code>	$QSPCLK = PCLK / 4.$
<code>QSPI_QSPCLK_DIV_5</code>	$QSPCLK = PCLK / 5.$
<code>QSPI_QSPCLK_DIV_6</code>	$QSPCLK = PCLK / 6.$
<code>QSPI_QSPCLK_DIV_7</code>	$QSPCLK = PCLK / 7.$
<code>QSPI_QSPCLK_DIV_8</code>	$QSPCLK = PCLK / 8.$
<code>QSPI_QSPCLK_DIV_9</code>	$QSPCLK = PCLK / 9.$
<code>QSPI_QSPCLK_DIV_10</code>	$QSPCLK = PCLK / 10.$
<code>QSPI_QSPCLK_DIV_11</code>	$QSPCLK = PCLK / 11.$
<code>QSPI_QSPCLK_DIV_12</code>	$QSPCLK = PCLK / 12.$
<code>QSPI_QSPCLK_DIV_13</code>	$QSPCLK = PCLK / 13.$
<code>QSPI_QSPCLK_DIV_14</code>	$QSPCLK = PCLK / 14.$
<code>QSPI_QSPCLK_DIV_15</code>	$QSPCLK = PCLK / 15.$
<code>QSPI_QSPCLK_DIV_16</code>	$QSPCLK = PCLK / 16.$
<code>QSPI_QSPCLK_DIV_17</code>	$QSPCLK = PCLK / 17.$
<code>QSPI_QSPCLK_DIV_18</code>	$QSPCLK = PCLK / 18.$
<code>QSPI_QSPCLK_DIV_19</code>	$QSPCLK = PCLK / 19.$
<code>QSPI_QSPCLK_DIV_20</code>	$QSPCLK = PCLK / 20.$
<code>QSPI_QSPCLK_DIV_22</code>	$QSPCLK = PCLK / 22.$
<code>QSPI_QSPCLK_DIV_24</code>	$QSPCLK = PCLK / 24.$
<code>QSPI_QSPCLK_DIV_26</code>	

	QSPCLK = PCLK / 26.
QSPI_QSPCLK_DIV_28	QSPCLK = PCLK / 28.
QSPI_QSPCLK_DIV_30	QSPCLK = PCLK / 30.
QSPI_QSPCLK_DIV_32	QSPCLK = PCLK / 32.
QSPI_QSPCLK_DIV_34	QSPCLK = PCLK / 34.
QSPI_QSPCLK_DIV_36	QSPCLK = PCLK / 36.
QSPI_QSPCLK_DIV_38	QSPCLK = PCLK / 38.
QSPI_QSPCLK_DIV_40	QSPCLK = PCLK / 40.
QSPI_QSPCLK_DIV_42	QSPCLK = PCLK / 42.
QSPI_QSPCLK_DIV_44	QSPCLK = PCLK / 44.
QSPI_QSPCLK_DIV_46	QSPCLK = PCLK / 46.
QSPI_QSPCLK_DIV_48	QSPCLK = PCLK / 48.

## Function Documentation

### ◆ R\_QSPI\_Open()

`fsp_err_t R_QSPI_Open ( spi_flash_ctrl_t * p_ctrl, spi_flash_cfg_t const *const p_cfg )`

Open the QSPI driver module. After the driver is open, the QSPI can be accessed like internal flash memory starting at address 0x60000000.

Implements `spi_flash_api_t::open`.

#### Return values

FSP_SUCCESS	Configuration was successful.
FSP_ERR_ASSERTION	The parameter <code>p_instance_ctrl</code> or <code>p_cfg</code> is NULL.
FSP_ERR_ALREADY_OPEN	Driver has already been opened with the same <code>p_instance_ctrl</code> .



◆ **R\_QSPI\_Close()**

```
fsp_err_t R_QSPI_Close ( spi_flash_ctrl_t * p_ctrl)
```

Close the QSPI driver module.

Implements `spi_flash_api_t::close`.

**Return values**

FSP_SUCCESS	Configuration was successful.
FSP_ERR_ASSERTION	<code>p_instance_ctrl</code> is NULL.
FSP_ERR_NOT_OPEN	Driver is not opened.

◆ **R\_QSPI\_DirectWrite()**

```
fsp_err_t R_QSPI_DirectWrite ( spi_flash_ctrl_t * p_ctrl, uint8_t const *const p_src, uint32_t const bytes, bool const read_after_write )
```

Writes raw data directly to the QSPI.

Implements `spi_flash_api_t::directWrite`.

**Return values**

FSP_SUCCESS	The flash was programmed successfully.
FSP_ERR_ASSERTION	A required pointer is NULL.
FSP_ERR_NOT_OPEN	Driver is not opened.
FSP_ERR_INVALID_MODE	This function can't be called when XIP mode is enabled.
FSP_ERR_DEVICE_BUSY	The device is busy.

◆ **R\_QSPI\_DirectRead()**

```
fsp_err_t R_QSPI_DirectRead ( spi_flash_ctrl_t * p_ctrl, uint8_t *const p_dest, uint32_t const bytes )
```

Reads raw data directly from the QSPI. This API can only be called after R\_QSPI\_DirectWrite with read\_after\_write set to true.

Implements `spi_flash_api_t::directRead`.

**Return values**

FSP_SUCCESS	The flash was programmed successfully.
FSP_ERR_ASSERTION	A required pointer is NULL.
FSP_ERR_NOT_OPEN	Driver is not opened.
FSP_ERR_INVALID_MODE	This function must be called after R_QSPI_DirectWrite with read_after_write set to true.

◆ **R\_QSPI\_SpiProtocolSet()**

```
fsp_err_t R_QSPI_SpiProtocolSet ( spi_flash_ctrl_t * p_ctrl, spi_flash_protocol_t spi_protocol )
```

Sets the SPI protocol.

Implements `spi_flash_api_t::spiProtocolSet`.

**Return values**

FSP_SUCCESS	SPI protocol updated on MCU peripheral.
FSP_ERR_ASSERTION	A required pointer is NULL.
FSP_ERR_NOT_OPEN	Driver is not opened.
FSP_ERR_INVALID_ARGUMENT	Invalid SPI protocol requested.

◆ **R\_QSPI\_XipEnter()**

```
fsp_err_t R_QSPI_XipEnter ( spi_flash_ctrl_t * p_ctrl)
```

Enters XIP (execute in place) mode.

Implements `spi_flash_api_t::xipEnter`.

**Return values**

FSP_SUCCESS	The flash was programmed successfully.
FSP_ERR_ASSERTION	A required pointer is NULL.
FSP_ERR_NOT_OPEN	Driver is not opened.

◆ **R\_QSPI\_XipExit()**

```
fsp_err_t R_QSPI_XipExit ( spi_flash_ctrl_t * p_ctrl)
```

Exits XIP (execute in place) mode.

Implements `spi_flash_api_t::xipExit`.

**Return values**

FSP_SUCCESS	The flash was programmed successfully.
FSP_ERR_ASSERTION	A required pointer is NULL.
FSP_ERR_NOT_OPEN	Driver is not opened.

◆ **R\_QSPI\_Write()**

```
fsp_err_t R_QSPI_Write ( spi_flash_ctrl_t * p_ctrl, uint8_t const *const p_src, uint8_t *const p_dest,
uint32_t byte_count )
```

Program a page of data to the flash.

Implements `spi_flash_api_t::write`.

**Return values**

FSP_SUCCESS	The flash was programmed successfully.
FSP_ERR_ASSERTION	<code>p_instance_ctrl</code> , <code>p_dest</code> or <code>p_src</code> is NULL, or <code>byte_count</code> crosses a page boundary.
FSP_ERR_NOT_OPEN	Driver is not opened.
FSP_ERR_INVALID_MODE	This function can't be called when XIP mode is enabled.
FSP_ERR_DEVICE_BUSY	The device is busy.

◆ **R\_QSPI\_Erase()**

```
fsp_err_t R_QSPI_Erase ( spi_flash_ctrl_t * p_ctrl, uint8_t *const p_device_address, uint32_t
byte_count )
```

Erase a block or sector of flash. The `byte_count` must exactly match one of the erase sizes defined in `spi_flash_cfg_t`. For chip erase, `byte_count` must be `SPI_FLASH_ERASE_SIZE_CHIP_ERASE`.

Implements `spi_flash_api_t::erase`.

**Return values**

FSP_SUCCESS	The command to erase the flash was executed successfully.
FSP_ERR_ASSERTION	<code>p_instance_ctrl</code> or <code>p_device_address</code> is NULL, or <code>byte_count</code> doesn't match an erase size defined in <code>spi_flash_cfg_t</code> , or device is in XIP mode.
FSP_ERR_NOT_OPEN	Driver is not opened.
FSP_ERR_INVALID_MODE	This function can't be called when XIP mode is enabled.
FSP_ERR_DEVICE_BUSY	The device is busy.

◆ **R\_QSPI\_StatusGet()**

```
fsp_err_t R_QSPI_StatusGet ( spi_flash_ctrl_t * p_ctrl, spi_flash_status_t *const p_status )
```

Gets the write or erase status of the flash.

Implements `spi_flash_api_t::statusGet`.

**Return values**

FSP_SUCCESS	The write status is in p_status.
FSP_ERR_ASSERTION	p_instance_ctrl or p_status is NULL.
FSP_ERR_NOT_OPEN	Driver is not opened.
FSP_ERR_INVALID_MODE	This function can't be called when XIP mode is enabled.

◆ **R\_QSPI\_BankSet()**

```
fsp_err_t R_QSPI_BankSet ( spi_flash_ctrl_t * p_ctrl, uint32_t bank )
```

Selects the bank to access. A bank is a 64MB sliding access window into the QSPI device flash memory space. To access chip address 0x4000000, select bank 1, then read from internal flash address 0x60000000. To access chip address 0x8001000, select bank 2, then read from internal flash address 0x60001000.

This function is not required for memory devices less than or equal to 512 Mb (64MB).

Implements `spi_flash_api_t::bankSet`.

**Return values**

FSP_SUCCESS	Bank successfully selected.
FSP_ERR_ASSERTION	A required pointer is NULL.
FSP_ERR_NOT_OPEN	Driver is not opened.

◆ **R\_QSPI\_VersionGet()**

```
fsp_err_t R_QSPI_VersionGet ( fsp_version_t *const p_version)
```

Get the driver version based on compile time macros.

Implements `spi_flash_api_t::versionGet`.

**Return values**

FSP_SUCCESS	Successful close.
FSP_ERR_ASSERTION	p_version is NULL.

## 4.2.39 Realtime Clock (r\_rtc)

### Modules

#### Functions

fsp\_err\_t R\_RTC\_Open (rtc\_ctrl\_t \*const p\_ctrl, rtc\_cfg\_t const \*const p\_cfg)

fsp\_err\_t R\_RTC\_Close (rtc\_ctrl\_t \*const p\_ctrl)

fsp\_err\_t R\_RTC\_CalendarTimeSet (rtc\_ctrl\_t \*const p\_ctrl, rtc\_time\_t \*const p\_time)

fsp\_err\_t R\_RTC\_CalendarTimeGet (rtc\_ctrl\_t \*const p\_ctrl, rtc\_time\_t \*const p\_time)

fsp\_err\_t R\_RTC\_CalendarAlarmSet (rtc\_ctrl\_t \*const p\_ctrl, rtc\_alarm\_time\_t \*const p\_alarm)

fsp\_err\_t R\_RTC\_CalendarAlarmGet (rtc\_ctrl\_t \*const p\_ctrl, rtc\_alarm\_time\_t \*const p\_alarm)

fsp\_err\_t R\_RTC\_PeriodicIrqRateSet (rtc\_ctrl\_t \*const p\_ctrl, rtc\_periodic\_irq\_select\_t const rate)

fsp\_err\_t R\_RTC\_ErrorAdjustmentSet (rtc\_ctrl\_t \*const p\_ctrl, rtc\_error\_adjustment\_cfg\_t const \*const err\_adj\_cfg)

fsp\_err\_t R\_RTC\_InfoGet (rtc\_ctrl\_t \*const p\_ctrl, rtc\_info\_t \*const p\_rtc\_info)

fsp\_err\_t R\_RTC\_VersionGet (fsp\_version\_t \*version)

fsp\_err\_t R\_RTC\_CallbackSet (rtc\_ctrl\_t \*const p\_ctrl, void(\*p\_callback)(rtc\_callback\_args\_t \*), void const \*const p\_context, rtc\_callback\_args\_t \*const p\_callback\_memory)

#### Detailed Description

Driver for the RTC peripheral on RA MCUs. This module implements the [RTC Interface](#).

## Overview

The RTC HAL module configures the RTC module and controls clock, calendar and alarm functions. A callback can be used to respond to the alarm and periodic interrupt.

#### Features

- RTC time and date get and set.
- RTC time and date alarm get and set.
- RTC alarm and periodic event notification.

The RTC HAL module supports three different interrupt types:

- An alarm interrupt generated on a match of any combination of year, month, day, day of the week, hour, minute or second
- A periodic interrupt generated every 2, 1, 1/2, 1/4, 1/8, 1/16, 1/32, 1/64, 1/128, or 1/256 second(s)
- A carry interrupt is used internally when reading time from the RTC calendar to get accurate time readings.

#### Note

See section "23.3.5 Reading 64-Hz Counter and Time" of the RA6M3 manual R01UH0886EJ0100 for more details.

A user-defined callback function can be registered (in the `rtc_api_t::open` API call) and will be called from the interrupt service routine (ISR) for alarm and periodic interrupt. When called, it is passed a pointer to a structure (`rtc_callback_args_t`) that holds a user-defined context pointer and an indication of which type of interrupt was fired.

### Date and Time validation

"Parameter Checking" needs to be enabled if date and time validation is required for `calendarTimeSet` and `calendarAlarmSet` APIs. If "Parameter Checking" is enabled, the 'day of the week' field is automatically calculated and updated by the driver for the provided date. When using the `calendarAlarmSet` API, only the fields which have their corresponding match flag set are written to the registers. Other register fields are reset to default value.

### Sub-Clock error adjustment (Time Error Adjustment Function)

The time error adjustment function is used to correct errors, running fast or slow, in the time caused by variation in the precision of oscillation by the sub-clock oscillator. Because 32,768 cycles of the sub-clock oscillator constitute 1 second of operation when the sub-clock oscillator is selected, the clock runs fast if the sub-clock frequency is high and slow if the sub-clock frequency is low. The time error adjustment functions include:

- Automatic adjustment
- Adjustment by software

The error adjustment is reset every time RTC is reconfigured or time is set.

#### Note

RTC driver configurations do not do error adjustment internally while initializing the driver. Application must make calls to the error adjustment APIs for desired adjustment. See section 26.3.8 "Time Error Adjustment Function" of the RA6M3 manual R01UH0886EJ0100 for more details on this feature

## Configuration

### Build Time Configurations for r\_rtc

The following build time configurations are defined in `fsp_cfg/r_rtc_cfg.h`:

--	--	--	--

Configuration	Options	Default	Description
Parameter Checking	<ul style="list-style-type: none"> <li>• Default (BSP)</li> <li>• Enabled</li> <li>• Disabled</li> </ul>	Default (BSP)	If selected code for parameter checking is included in the build.

### Configurations for Driver > Timers > RTC Driver on r\_rtc

This module can be added to the Stacks tab via New Stack > Driver > Timers > RTC Driver on r\_rtc. Non-secure callable guard functions can be generated for this module by right clicking the module in the RA Configuration tool and checking the "Non-secure Callable" box.

Configuration	Options	Default	Description
Name	Name must be a valid C symbol	g_rtc0	Module name.
Clock Source	<ul style="list-style-type: none"> <li>• Sub-Clock</li> <li>• LOCO</li> </ul>	LOCO	Select the RTC clock source.
Frequency Comparison Value (LOCO)	Value must be a positive integer between 7 and 511	255	Frequency comparison value when using LOCO
Automatic Adjustment Mode	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Enabled	Enable/ Disable the Error Adjustment mode
Automatic Adjustment Period	<ul style="list-style-type: none"> <li>• 10 Seconds</li> <li>• 1 Minute</li> <li>• NONE</li> </ul>	10 Seconds	Select the Error Adjustment Period for Automatic Adjustment
Adjustment Type (Plus-Minus)	<ul style="list-style-type: none"> <li>• NONE</li> <li>• Addition</li> <li>• Subtraction</li> </ul>	NONE	Select the Error Adjustment type
Error Adjustment Value	Value must be a positive integer less than equal to 63	0	Specify the Adjustment Value (the number of sub-clock cycles) from the prescaler
Callback	Name must be a valid C symbol	NULL	A user callback function can be provided. If this callback function is provided, it will be called from the interrupt service routine (ISR).
Alarm Interrupt Priority	MCU Specific Options		Select the alarm interrupt priority.
Period Interrupt Priority	MCU Specific Options		Select the period interrupt priority.
Carry Interrupt Priority	MCU Specific Options		Select the carry interrupt priority.

*Note*



See 23.2.20 Frequency Register (RFRH/RFRL) of the RA6M3 manual R01UH0886EJ0100) for more details

## Interrupt Configuration

To activate interrupts for the RTC module, the desired interrupts must be enabled, The underlying implementation will be expected to handle any interrupts it can support and notify higher layers via callback.

## Clock Configuration

The RTC HAL module can use the following clock sources:

- LOCO (Low Speed On-Chip Oscillator) with less accuracy
- Sub-clock oscillator with increased accuracy

The LOCO is the default selection during configuration.

## Pin Configuration

This module does not use I/O pins.

# Usage Notes

## System Initialization

- RTC driver does not start the sub-clock. The application is responsible for ensuring required clocks are started and stable before accessing MCU peripheral registers.

### Warning

The subclock can take seconds to stabilize. The RA startup code does not wait for subclock stabilization unless the subclock is the main clock source. When running AGT or RTC off the subclock, the application must ensure the subclock is stable before starting operation.

- Carry interrupt priority must be set to avoid incorrect time returned from `calendarTimeGet` API during roll-over.
- Even when only running in Periodic Interrupt mode `R_RTC_CalendarTimeSet` must be called successfully to start the RTC.

## Limitations

Developers should be aware of the following limitations when using the RTC: Below features are not supported by the driver

- Binary-count mode
- The `R_RTC_CalendarTimeGet()` cannot be used from an interrupt that has higher priority than the carry interrupt. Also, it must not be called with interrupts disabled globally, as this API internally uses carry interrupt for its processing. API may return incorrect time if this is done.

# Examples

## RTC Basic Example

This is a basic example of minimal use of the RTC in an application.

```
/* rtc_time_t is an alias for the C Standard time.h struct 'tm' */
rtc_time_t set_time =
{
    .tm_sec = 10,
    .tm_min = 11,
    .tm_hour = 12,
    .tm_mday = 6,
    .tm_wday = 3,
    .tm_mon = 11,
    .tm_year = YEARS_SINCE_1900,
};

rtc_time_t get_time;

void rtc_example ()
{
    fsp_err_t err = FSP_SUCCESS;
    /* Initialize the RTC module */
    err = R_RTC_Open(&g_rtc0_ctrl, &g_rtc0_cfg);
    /* Handle any errors. This function should be defined by the user. */
    handle_error(err);
    /* Set the calendar time */
    R_RTC_CalendarTimeSet(&g_rtc0_ctrl, &set_time);
    /* Get the calendar time */
    R_RTC_CalendarTimeGet(&g_rtc0_ctrl, &get_time);
}
```

### RTC Periodic interrupt example

This is an example of periodic interrupt in RTC.

```
void rtc_periodic_irq_example ()
{
    fsp_err_t err = FSP_SUCCESS;
    /* Initialize the RTC module*/
    err = R_RTC_Open(&g_rtc0_ctrl, &g_rtc0_cfg);
    /* Handle any errors. This function should be defined by the user. */
}
```

```
    handle_error(err);

    /* R_RTC_CalendarTimeSet must be called at least once to start the RTC */
    R_RTC_CalendarTimeSet(&g_rtc0_ctrl, &set_time);

    /* Set the periodic interrupt rate to 1 second */
    R_RTC_PeriodicIrqRateSet(&g_rtc0_ctrl, RTC_PERIODIC_IRQ_SELECT_1_SECOND);

    /* Wait for the periodic interrupt */
    while (1)
    {
        /* Wait for interrupt */
    }
}
```

### RTC Alarm interrupt example

This is an example of alarm interrupt in RTC.

```
void rtc_alarm_irq_example ()
{
    fsp_err_t err = FSP_SUCCESS;

    /*Initialize the RTC module*/
    err = R_RTC_Open(&g_rtc0_ctrl, &g_rtc0_cfg);

    /* Handle any errors. This function should be defined by the user. */
    handle_error(err);

    R_RTC_CalendarTimeSet(&g_rtc0_ctrl, &set_time1.time);
    R_RTC_CalendarAlarmSet(&g_rtc0_ctrl, &set_time1);

    /* Wait for the Alarm interrupt */
    while (1)
    {
        /* Wait for interrupt */
    }
}
```

### RTC Error Adjustment example

This is an example of modifying error adjustment in RTC.

```

void rtc_erroradj_example ()
{
    fsp_err_t err = FSP_SUCCESS;
    /*Initialize the RTC module*/
    R_RTC_Open(&g_rtc0_ctrl, &g_rtcl_cfg);
    R_RTC_CalendarTimeSet(&g_rtc0_ctrl, &set_time1.time);
    /* Modify Error Adjustment after RTC is running */
    err = R_RTC_ErrorAdjustmentSet(&g_rtc0_ctrl, &err_cfg2);
    handle_error(err);
}

```

## Data Structures

struct [rtc\\_instance\\_ctrl\\_t](#)

## Data Structure Documentation

### ◆ [rtc\\_instance\\_ctrl\\_t](#)

struct <a href="#">rtc_instance_ctrl_t</a>	
Channel control block. DO NOT INITIALIZE. Initialization occurs when <a href="#">rtc_api_t::open</a> is called	
Data Fields	
uint32_t	<a href="#">open</a>
	Whether or not driver is open.
const <a href="#">rtc_cfg_t</a> *	<a href="#">p_cfg</a>
	Pointer to initial configurations.
volatile bool	<a href="#">carry_isr_triggered</a>
	Was the carry isr triggered.

## Function Documentation

◆ **R\_RTC\_Open()**

```
fsp_err_t R_RTC_Open ( rtc_ctrl_t *const p_ctrl, rtc_cfg_t const *const p_cfg )
```

Opens and configures the RTC driver module. Implements `rtc_api_t::open`. Configuration includes clock source, and interrupt callback function.

Example:

```
/* Initialize the RTC module */
err = R_RTC_Open(&g_rtc0_ctrl, &g_rtc0_cfg);
```

**Return values**

FSP_SUCCESS	Initialization was successful and RTC has started.
FSP_ERR_ASSERTION	Invalid p_ctrl or p_cfg pointer.
FSP_ERR_ALREADY_OPEN	Module is already open.
FSP_ERR_INVALID_ARGUMENT	Invalid time parameter field.

◆ **R\_RTC\_Close()**

```
fsp_err_t R_RTC_Close ( rtc_ctrl_t *const p_ctrl)
```

Close the RTC driver. Implements `rtc_api_t::close`

**Return values**

FSP_SUCCESS	De-Initialization was successful and RTC driver closed.
FSP_ERR_ASSERTION	Invalid p_ctrl.
FSP_ERR_NOT_OPEN	Driver not open already for close.

◆ **R\_RTC\_CalendarTimeSet()**

```
fsp_err_t R_RTC_CalendarTimeSet ( rtc_ctrl_t *const p_ctrl, rtc_time_t *const p_time )
```

Set the calendar time.

Implements `rtc_api_t::calendarTimeSet`.

**Return values**

FSP_SUCCESS	Calendar time set operation was successful.
FSP_ERR_ASSERTION	Invalid input argument.
FSP_ERR_NOT_OPEN	Driver not open already for operation.
FSP_ERR_INVALID_ARGUMENT	Invalid time parameter field.

◆ **R\_RTC\_CalendarTimeGet()**

```
fsp_err_t R_RTC_CalendarTimeGet ( rtc_ctrl_t *const p_ctrl, rtc_time_t *const p_time )
```

Get the calendar time.

**Warning**

Do not call this function from a critical section or from an interrupt with higher priority than the carry interrupt, or the time returned may be inaccurate.

Implements `rtc_api_t::calendarTimeGet`

**Return values**

FSP_SUCCESS	Calendar time get operation was successful.
FSP_ERR_ASSERTION	Invalid input argument.
FSP_ERR_NOT_OPEN	Driver not open already for operation.
FSP_ERR_IRQ_BSP_DISABLED	User IRQ parameter not valid

◆ **R\_RTC\_CalendarAlarmSet()**

```
fsp_err_t R_RTC_CalendarAlarmSet ( rtc_ctrl_t *const p_ctrl, rtc_alarm_time_t *const p_alarm )
```

Set the calendar alarm time.

Implements `rtc_api_t::calendarAlarmSet`.

**Precondition**

The calendar counter must be running before the alarm can be set.

**Return values**

FSP_SUCCESS	Calendar alarm time set operation was successful.
FSP_ERR_INVALID_ARGUMENT	Invalid time parameter field.
FSP_ERR_ASSERTION	Invalid input argument.
FSP_ERR_NOT_OPEN	Driver not open already for operation.
FSP_ERR_IRQ_BSP_DISABLED	User IRQ parameter not valid

◆ **R\_RTC\_CalendarAlarmGet()**

```
fsp_err_t R_RTC_CalendarAlarmGet ( rtc_ctrl_t *const p_ctrl, rtc_alarm_time_t *const p_alarm )
```

Get the calendar alarm time.

Implements `rtc_api_t::calendarAlarmGet`

**Return values**

FSP_SUCCESS	Calendar alarm time get operation was successful.
FSP_ERR_ASSERTION	Invalid input argument.
FSP_ERR_NOT_OPEN	Driver not open already for operation.

◆ **R\_RTC\_PeriodicIrqRateSet()**

```
fsp_err_t R_RTC_PeriodicIrqRateSet ( rtc_ctrl_t *const p_ctrl, rtc_periodic_irq_select_t const rate )
```

Set the periodic interrupt rate and enable periodic interrupt.

Implements `rtc_api_t::periodicIrqRateSet`

**Note**

To start the RTC `R_RTC_CalendarTimeSet` must be called at least once.

Example:

```
/* Set the periodic interrupt rate to 1 second */
R_RTC_PeriodicIrqRateSet(&g_rtc0_ctrl, RTC_PERIODIC_IRQ_SELECT_1_SECOND);
```

**Return values**

FSP_SUCCESS	The periodic interrupt rate was successfully set.
FSP_ERR_ASSERTION	Invalid input argument.
FSP_ERR_NOT_OPEN	Driver not open already for operation.
FSP_ERR_IRQ_BSP_DISABLED	User IRQ parameter not valid

◆ **R\_RTC\_ErrorAdjustmentSet()**

```
fsp_err_t R_RTC_ErrorAdjustmentSet ( rtc_ctrl_t *const p_ctrl, rtc_error_adjustment_cfg_t const
*const err_adj_cfg )
```

This function sets time error adjustment

Implements `rtc_api_t::errorAdjustmentSet`

**Return values**

FSP_SUCCESS	Time error adjustment successful.
FSP_ERR_ASSERTION	Invalid input argument.
FSP_ERR_NOT_OPEN	Driver not open for operation.
FSP_ERR_UNSUPPORTED	The clock source is not sub-clock.
FSP_ERR_INVALID_ARGUMENT	Invalid error adjustment value.



◆ **R\_RTC\_InfoGet()**

```
fsp_err_t R_RTC_InfoGet ( rtc_ctrl_t *const p_ctrl, rtc_info_t *const p_rtc_info )
```

Set RTC clock source and running status information and store it in provided pointer p\_rtc\_info

Implements `rtc_api_t::infoGet`

**Return values**

FSP_SUCCESS	Get information Successful.
FSP_ERR_ASSERTION	Invalid input argument.
FSP_ERR_NOT_OPEN	Driver not open already for operation.

◆ **R\_RTC\_VersionGet()**

```
fsp_err_t R_RTC_VersionGet ( fsp_version_t * p_version)
```

Get driver version based on compile time macros.

Implements `rtc_api_t::versionGet`

**Return values**

FSP_SUCCESS	Successful close.
FSP_ERR_ASSERTION	The parameter p_version is NULL.

◆ **R\_RTC\_CallbackSet()**

```
fsp_err_t R_RTC_CallbackSet ( rtc_ctrl_t *const p_ctrl, void(*) (rtc_callback_args_t *) p_callback, void const *const p_context, rtc_callback_args_t *const p_callback_memory )
```

Updates the user callback and has option of providing memory for callback structure. Implements `rtc_api_t::callbackSet`

**Return values**

FSP_SUCCESS	Baud rate was successfully changed.
FSP_ERR_ASSERTION	Pointer to RTC control block is NULL or the RTC is not configured to use the internal clock.
FSP_ERR_NOT_OPEN	The control block has not been opened

## 4.2.40 Serial Communications Interface (SCI) I2C (r\_sci\_i2c)

### Modules

#### Functions

fsp_err_t	R_SCI_I2C_VersionGet (fsp_version_t *const p_version)
fsp_err_t	R_SCI_I2C_Open (i2c_master_ctrl_t *const p_api_ctrl, i2c_master_cfg_t const *const p_cfg)
fsp_err_t	R_SCI_I2C_Close (i2c_master_ctrl_t *const p_api_ctrl)
fsp_err_t	R_SCI_I2C_Read (i2c_master_ctrl_t *const p_api_ctrl, uint8_t *const p_dest, uint32_t const bytes, bool const restart)
fsp_err_t	R_SCI_I2C_Write (i2c_master_ctrl_t *const p_api_ctrl, uint8_t *const p_src, uint32_t const bytes, bool const restart)
fsp_err_t	R_SCI_I2C_Abort (i2c_master_ctrl_t *const p_api_ctrl)
fsp_err_t	R_SCI_I2C_SlaveAddressSet (i2c_master_ctrl_t *const p_api_ctrl, uint32_t const slave, i2c_master_addr_mode_t const addr_mode)
fsp_err_t	R_SCI_I2C_CallbackSet (i2c_master_ctrl_t *const p_api_ctrl, void(*p_callback)(i2c_master_callback_args_t *), void const *const p_context, i2c_master_callback_args_t *const p_callback_memory)

#### Detailed Description

Driver for the SCI peripheral on RA MCUs. This module implements the [I2C Master Interface](#).

## Overview

The Simple I2C master on SCI HAL module supports transactions with an I2C Slave device. Callbacks must be provided which would be invoked when a transmission or receive has been completed. The callback arguments will contain information about the transaction status, bytes transferred and a pointer to the user defined context.

#### Features

- Supports multiple transmission rates
  - Standard Mode Support with up to 100 kHz transaction rate.
  - Fast Mode Support with up to 400 kHz transaction rate.
- SDA Delay in nanoseconds can be specified as a part of the configuration.
- I2C Master Read from a slave device.
- I2C Master Write to a slave device.
- Abort any in-progress transactions.
- Set the address of the slave device.
- Non-blocking behavior is achieved by the use of callbacks.
- Additional build-time features
  - Optional (build time) DTC support for read and write respectively.

- Optional (build time) support for 10-bit slave addressing.

## Configuration

### Build Time Configurations for r\_sci\_i2c

The following build time configurations are defined in fsp\_cfg/r\_sci\_i2c\_cfg.h:

Configuration	Options	Default	Description
Parameter Checking	<ul style="list-style-type: none"> <li>• Default (BSP)</li> <li>• Enabled</li> <li>• Disabled</li> </ul>	Default (BSP)	If selected code for parameter checking is included in the build.
DTC on Transmission and Reception	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Disabled	If enabled, DTC instances will be included in the build for both transmission and reception.
10-bit slave addressing	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Disabled	If enabled, the driver will support 10-bit slave addressing mode along with the default 7-bit slave addressing mode.

### Configurations for Driver > Connectivity > I2C Master Driver on r\_sci\_i2c

This module can be added to the Stacks tab via New Stack > Driver > Connectivity > I2C Master Driver on r\_sci\_i2c. Non-secure callable guard functions can be generated for this module by right clicking the module in the RA Configuration tool and checking the "Non-secure Callable" box.

Configuration	Options	Default	Description
Name	Name must be a valid C symbol	g_i2c0	Module name.
Channel	Value must be an integer between 0 and 9	0	Select the SCI channel.
Slave Address	Value must be a hex value	0x00	Specify the slave address.
Address Mode	<ul style="list-style-type: none"> <li>• 7-Bit</li> <li>• 10-Bit</li> </ul>	7-Bit	Select the address mode.
Rate	<ul style="list-style-type: none"> <li>• Standard</li> <li>• Fast-mode</li> </ul>	Standard	Select the I2C data rate.
SDA Output Delay (nano seconds)	Must be a valid non-negative integer with maximum configurable value of 300	300	Specify the SDA output delay in nanoseconds.
Noise filter setting	<ul style="list-style-type: none"> <li>• Use clock signal divided by 1</li> </ul>	Use clock signal divided by 1 with noise	Select the sampling clock for the digital

	<ul style="list-style-type: none"> <li>with noise filter</li> <li>Use clock signal divided by 2 with noise filter</li> <li>Use clock signal divided by 4 with noise filter</li> <li>Use clock signal divided by 8 with noise filter</li> </ul>	filter	noise filter
Bit Rate Modulation	<ul style="list-style-type: none"> <li>Enable</li> <li>Disable</li> </ul>	Enable	Enabling bitrate modulation reduces the percent error of the actual bitrate with respect to the requested baud rate. It does this by modulating the number of cycles per clock output pulse, so the clock is no longer a square wave.
Callback	Name must be a valid C symbol	sci_i2c_master_callback	A user callback function can be provided. If this callback function is provided, it will be called from the interrupt service routine (ISR).
Interrupt Priority Level	MCU Specific Options		Select the interrupt priority level. This is set for TXI, RXI (if used), TEI interrupts.
RX Interrupt Priority Level [Only used when DTC is enabled]	MCU Specific Options		Select the interrupt priority level. This is set for RXI only when DTC is enabled.

## Clock Configuration

The clock for this module is derived from the following peripheral clock for each MCU group:

MCU Group	Peripheral Clock
RA2A1	PCLKB
RA4M1	PCLKA
RA4W1	PCLKA
RA6M1	PCLKA

---

RA6M2	PCLKA
RA6M3	PCLKA
RA6M4	PCLKA

The actual I2C transfer rate will be calculated and set by the tooling depending on the selected transfer rate and the SDA delay. If the PCLK is configured in such a manner that the selected internal rate cannot be achieved, an error will be returned.

### Pin Configuration

The SCI I2C peripheral module uses pins on the MCU to communicate to external devices. I/O pins must be selected and configured as required by the external device. An I2C channel would consist of two pins - SDA and SCL for data/address and clock respectively.

## Usage Notes

### Interrupt Configuration

- Receive buffer full (RXI), transmit buffer empty (TXI) and transmit end (TEI) interrupts for the selected channel used must be enabled in the properties of the selected device.
- Set equal priority levels for all the interrupts mentioned above. Setting the interrupts to different priority levels could result in improper operation.

### SCI I2C Master Rate Calculation

- The RA Configuration editor calculates the internal baud-rate setting based on the configured transfer rate and SDA Delay. The closest possible baud-rate that can be achieved (less than or equal to the requested rate) at the current PCLK settings is calculated and used.
- If a valid clock rate could not be calculated, an error is returned by the tool.

### Enabling DTC with the SCI I2C

- DTC transfer support is configurable and is disabled from the build by default. SCI I2C driver provides two DTC instances for transmission and reception respectively.
- For further details on DTC please refer [Data Transfer Controller \(r\\_dtc\)](#)

### Multiple Devices on the Bus

- A single SCI I2C instance can be used to communicate with multiple slave devices on the same channel by using the SlaveAddressSet API.

### Restart

- SCI I2C master can hold the the bus after an I2C transaction by issuing Restart. This will mimic a stop followed by start condition.

## Examples

### Basic Example

This is a basic example of minimal use of the r\_sci\_i2c in an application. This example shows how

this driver can be used for basic read and write operations.

```
void basic_example (void)
{
    fsp_err_t err;

    uint32_t i;

    uint32_t timeout_ms = I2C_TRANSACTION_BUSY_DELAY;

    /* Initialize the IIC module */
    err = R_SCI_I2C_Open(&g_i2c_device_ctrl_1, &g_i2c_device_cfg_1);
    /* Handle any errors. This function should be defined by the user. */
    handle_error(err);

    /* Write some data to the transmit buffer */
    for (i = 0; i < I2C_BUFFER_SIZE_BYTES; i++)
    {
        g_i2c_tx_buffer[i] = (uint8_t) i;
    }

    /* Send data to I2C slave */
    g_i2c_callback_event = I2C_MASTER_EVENT_ABORTED;
    err = R_SCI_I2C_Write(&g_i2c_device_ctrl_1, &g_i2c_tx_buffer[0],
I2C_BUFFER_SIZE_BYTES, false);
    handle_error(err);

    /* Since there is nothing else to do, block until Callback triggers*/
    while ((I2C_MASTER_EVENT_TX_COMPLETE != g_i2c_callback_event) && timeout_ms)
    {
        R_BSP_SoftwareDelay(1U, BSP_DELAY_UNITS_MILLISECONDS);
        timeout_ms--;
    }
    if (I2C_MASTER_EVENT_ABORTED == g_i2c_callback_event)
    {
        __BKPT(0);
    }

    /* Read data back from the I2C slave */
    g_i2c_callback_event = I2C_MASTER_EVENT_ABORTED;
    timeout_ms          = I2C_TRANSACTION_BUSY_DELAY;
    err = R_SCI_I2C_Read(&g_i2c_device_ctrl_1, &g_i2c_rx_buffer[0],
```

```
I2C_BUFFER_SIZE_BYTES, false);
    handle_error(err);
    /* Since there is nothing else to do, block until Callback triggers*/
    while ((I2C_MASTER_EVENT_RX_COMPLETE != g_i2c_callback_event) && timeout_ms)
    {
        R_BSP_SoftwareDelay(1U, BSP_DELAY_UNITS_MILLISECONDS);
        timeout_ms--;
    }
    if (I2C_MASTER_EVENT_ABORTED == g_i2c_callback_event)
    {
        __BKPT(0);
    }
    /* Verify the read data */
    if (0U != memcmp(g_i2c_tx_buffer, g_i2c_rx_buffer, I2C_BUFFER_SIZE_BYTES))
    {
        __BKPT(0);
    }
}
```

### Multiple Slave devices on the same channel (bus)

This example demonstrates how a single SCI I2C driver can be used to communicate with different slave devices which are on the same channel.

```
void single_channel_multi_slave (void)
{
    fsp_err_t err;
    uint32_t timeout_ms = I2C_TRANSACTION_BUSY_DELAY;
    err = R_SCI_I2C_Open(&g_i2c_device_ctrl_2, &g_i2c_device_cfg_2);
    /* Handle any errors. This function should be defined by the user. */
    handle_error(err);
    /* Clear the receive buffer */
    memset(g_i2c_rx_buffer, '0', I2C_BUFFER_SIZE_BYTES);
    /* Read data from I2C slave */
    g_i2c_callback_event = I2C_MASTER_EVENT_ABORTED;
```

```
err = R_SCI_I2C_Read(&g_i2c_device_ctrl_2, &g_i2c_rx_buffer[0],
I2C_BUFFER_SIZE_BYTES, false);
handle_error(err);
while ((I2C_MASTER_EVENT_RX_COMPLETE != g_i2c_callback_event) && timeout_ms)
{
R_BSP_SoftwareDelay(1U, BSP_DELAY_UNITS_MILLISECONDS);
timeout_ms--;
}
if (I2C_MASTER_EVENT_ABORTED == g_i2c_callback_event)
{
__BKPT(0);
}
/* Send data to I2C slave on the same channel */
err = R_SCI_I2C_SlaveAddressSet(&g_i2c_device_ctrl_2, I2C_SLAVE_DISPLAY_ADAPTER,
I2C_MASTER_ADDR_MODE_7BIT);
handle_error(err);
g_i2c_tx_buffer[0] = (uint8_t) I2C_EXAMPLE_DATA_1;
g_i2c_tx_buffer[1] = (uint8_t) I2C_EXAMPLE_DATA_2;
g_i2c_callback_event = I2C_MASTER_EVENT_ABORTED;
timeout_ms = I2C_TRANSACTION_BUSY_DELAY;
err = R_SCI_I2C_Write(&g_i2c_device_ctrl_2, &g_i2c_tx_buffer[0], 2U, false);
handle_error(err);
while ((I2C_MASTER_EVENT_TX_COMPLETE != g_i2c_callback_event) && timeout_ms)
{
R_BSP_SoftwareDelay(1U, BSP_DELAY_UNITS_MILLISECONDS);
timeout_ms--;
}
if (I2C_MASTER_EVENT_ABORTED == g_i2c_callback_event)
{
__BKPT(0);
}
}
```

## Data Structures

```
struct sci_i2c_clock_settings_t
```



```
struct sci_i2c_instance_ctrl_t
```

```
struct sci_i2c_extended_cfg_t
```

## Data Structure Documentation

### ◆ sci\_i2c\_clock\_settings\_t

struct sci_i2c_clock_settings_t		
I2C clock settings		
Data Fields		
bool	bitrate_modulation	Bit-rate Modulation Function enable or disable.
uint8_t	brr_value	Bit rate register settings.
uint8_t	clk_divisor_value	Clock Select settings.
uint8_t	mddr_value	Modulation Duty Register settings.
uint8_t	cycles_value	SDA Delay Output Cycles Select.
uint8_t	snfr_value	Noise Filter Setting Register value.

### ◆ sci\_i2c\_instance\_ctrl\_t

struct sci_i2c_instance_ctrl_t	
I2C control structure. DO NOT INITIALIZE.	

### ◆ sci\_i2c\_extended\_cfg\_t

struct sci_i2c_extended_cfg_t		
SCI I2C extended configuration		
Data Fields		
<a href="#">sci_i2c_clock_settings_t</a>	clock_settings	I2C Clock settings.

## Function Documentation

◆ **R\_SCI\_I2C\_VersionGet()**

```
fsp_err_t R_SCI_I2C_VersionGet ( fsp_version_t *const p_version)
```

Sets driver version based on compile time macros.

**Return values**

FSP_SUCCESS	Successful version get.
FSP_ERR_ASSERTION	The parameter p_version is NULL.

◆ **R\_SCI\_I2C\_Open()**

```
fsp_err_t R_SCI_I2C_Open ( i2c_master_ctrl_t *const p_api_ctrl, i2c_master_cfg_t const *const p_cfg )
```

Opens the I2C device.

**Return values**

FSP_SUCCESS	Requested clock rate was set exactly.
FSP_ERR_ALREADY_OPEN	Module is already open.
FSP_ERR_ASSERTION	Parameter check failure due to one or more reasons below: <ul style="list-style-type: none"> <li>1. p_api_ctrl or p_cfg is NULL.</li> <li>2. extended parameter is NULL.</li> <li>3. Callback parameter is NULL.</li> <li>4. Clock rate requested is greater than 400KHz</li> <li>5. Invalid IRQ number assigned</li> </ul>

◆ **R\_SCI\_I2C\_Close()**

```
fsp_err_t R_SCI_I2C_Close ( i2c_master_ctrl_t *const p_api_ctrl)
```

Closes the I2C device. Power down I2C peripheral.

This function will safely terminate any in-progress I2C transfer with the device. If a transfer is aborted, the user will be notified via callback with an abort event. Since the callback is optional, this function will also return a specific error code in this situation.

**Return values**

FSP_SUCCESS	Device closed without issue.
FSP_ERR_ASSERTION	The parameter p_ctrl is NULL.
FSP_ERR_NOT_OPEN	Device was not even opened.

◆ **R\_SCI\_I2C\_Read()**

```
fsp_err_t R_SCI_I2C_Read ( i2c_master_ctrl_t *const p_api_ctrl, uint8_t *const p_dest, uint32_t
const bytes, bool const restart )
```

Performs a read from the I2C device. The caller will be notified when the operation has completed (successfully) by an I2C\_MASTER\_EVENT\_RX\_COMPLETE in the callback.

**Return values**

FSP_SUCCESS	Function executed without issue.
FSP_ERR_ASSERTION	The parameter p_ctrl, p_dest is NULL, bytes is 0.
FSP_ERR_INVALID_SIZE	Provided number of bytes more than uint16_t size (65535) while DTC is used for data transfer.
FSP_ERR_NOT_OPEN	Device was not even opened.

◆ **R\_SCI\_I2C\_Write()**

```
fsp_err_t R_SCI_I2C_Write ( i2c_master_ctrl_t *const p_api_ctrl, uint8_t *const p_src, uint32_t
const bytes, bool const restart )
```

Performs a write to the I2C device.

This function will fail if there is already an in-progress I2C transfer on the associated channel. Otherwise, the I2C write operation will begin. When no callback is provided by the user, this function performs a blocking write. Otherwise, the write operation is non-blocking and the caller will be notified when the operation has finished by an I2C\_EVENT\_TX\_COMPLETE in the callback.

**Return values**

FSP_SUCCESS	Function executed without issue.
FSP_ERR_ASSERTION	p_ctrl, p_src is NULL.
FSP_ERR_INVALID_SIZE	Provided number of bytes more than uint16_t size (65535) while DTC is used for data transfer.
FSP_ERR_NOT_OPEN	Device was not even opened.

◆ **R\_SCI\_I2C\_Abort()**

```
fsp_err_t R_SCI_I2C_Abort ( i2c_master_ctrl_t *const p_api_ctrl)
```

Aborts any in-progress transfer and forces the I2C peripheral into a ready state.

This function will safely terminate any in-progress I2C transfer with the device. If a transfer is aborted, the user will be notified via callback with an abort event. Since the callback is optional, this function will also return a specific error code in this situation.

**Return values**

FSP_SUCCESS	Transaction was aborted without issue.
FSP_ERR_ASSERTION	p_ctrl is NULL.
FSP_ERR_NOT_OPEN	Device was not even opened.

◆ **R\_SCI\_I2C\_SlaveAddressSet()**

```
fsp_err_t R_SCI_I2C_SlaveAddressSet ( i2c_master_ctrl_t *const p_api_ctrl, uint32_t const slave,
i2c_master_addr_mode_t const addr_mode )
```

Sets address and addressing mode of the slave device.

This function is used to set the device address and addressing mode of the slave without reconfiguring the entire bus.

**Return values**

FSP_SUCCESS	Address of the slave is set correctly.
FSP_ERR_ASSERTION	p_ctrl or address is NULL.
FSP_ERR_NOT_OPEN	Device was not even opened.
FSP_ERR_IN_USE	An I2C Transaction is in progress.

**◆ R\_SCI\_I2C\_CallbackSet()**

```
fsp_err_t R_SCI_I2C_CallbackSet ( i2c_master_ctrl_t *const p_api_ctrl,
void(*) (i2c_master_callback_args_t *) p_callback, void const *const p_context,
i2c_master_callback_args_t *const p_callback_memory )
```

Updates the user callback and has option of providing memory for callback structure. Implements `i2c_master_api_t::callbackSet`

**Return values**

FSP_SUCCESS	Callback updated successfully.
FSP_ERR_ASSERTION	A required pointer is NULL.
FSP_ERR_NOT_OPEN	The control block has not been opened.

**4.2.41 Serial Communications Interface (SCI) SPI (r\_sci\_spi)**

## Modules

**Functions**

```
fsp_err_t R_SCI_SPI_Open (spi_ctrl_t *p_api_ctrl, spi_cfg_t const *const p_cfg)
```

```
fsp_err_t R_SCI_SPI_Read (spi_ctrl_t *const p_api_ctrl, void *p_dest, uint32_t
const length, spi_bit_width_t const bit_width)
```

```
fsp_err_t R_SCI_SPI_Write (spi_ctrl_t *const p_api_ctrl, void const *p_src,
uint32_t const length, spi_bit_width_t const bit_width)
```

```
fsp_err_t R_SCI_SPI_WriteRead (spi_ctrl_t *const p_api_ctrl, void const *p_src,
void *p_dest, uint32_t const length, spi_bit_width_t const bit_width)
```

```
fsp_err_t R_SCI_SPI_CallbackSet (spi_ctrl_t *const p_api_ctrl,
void(*p_callback)(spi_callback_args_t *), void const *const p_context,
spi_callback_args_t *const p_callback_memory)
```

```
fsp_err_t R_SCI_SPI_Close (spi_ctrl_t *const p_api_ctrl)
```

```
fsp_err_t R_SCI_SPI_VersionGet (fsp_version_t *p_version)
```

```
fsp_err_t R_SCI_SPI_CalculateBitrate (uint32_t bitrate, sci_spi_div_setting_t
*sclk_div, bool use_mddr)
```

**Detailed Description**

Driver for the SCI peripheral on RA MCUs. This module implements the [SPI Interface](#).

## Overview

### Features

- Standard SPI Modes
  - Master or Slave Mode
  - Clock Polarity (CPOL)
    - CPOL=0 SCLK is low when idle
    - CPOL=1 SCLK is high when idle
  - Clock Phase (CPHA)
    - CPHA=0 Data Sampled on the even edge of SCLK
    - CPHA=1 Data Sampled on the odd edge of SCLK
  - MSB/LSB first
- Configurable bit rate
- DTC Support
- Callback Events
  - Transfer Complete
  - RX Overflow Error (The SCI shift register is copied to the data register before previous data was read)

## Configuration

### Build Time Configurations for r\_sci\_spi

The following build time configurations are defined in fsp\_cfg/r\_sci\_spi\_cfg.h:

Configuration	Options	Default	Description
Parameter Checking	<ul style="list-style-type: none"> <li>• Default (BSP)</li> <li>• Enabled</li> <li>• Disabled</li> </ul>	Default (BSP)	If selected code for parameter checking is included in the build.
DTC Support	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Enabled	If support for transferring data using the DTC will be compiled in.

### Configurations for Driver > Connectivity > SPI Driver on r\_sci\_spi

This module can be added to the Stacks tab via New Stack > Driver > Connectivity > SPI Driver on r\_sci\_spi. Non-secure callable guard functions can be generated for this module by right clicking the module in the RA Configuration tool and checking the "Non-secure Callable" box.

Configuration	Options	Default	Description
Name	Name must be a valid C symbol	g_spi0	Module name.
Channel	Value must be a non-negative integer	0	Select the SCI channel.
Operating Mode	<ul style="list-style-type: none"> <li>• Master</li> <li>• Slave</li> </ul>	Master	Select the SPI operating mode.

Clock Phase	<ul style="list-style-type: none"> <li>• Data sampling on odd edge, data variation on even edge</li> <li>• Data sampling on even edge, data variation on odd edge</li> </ul>	Data sampling on odd edge, data variation on even edge	Select the clock edge to sample data.
Clock Polarity	<ul style="list-style-type: none"> <li>• Low when idle</li> <li>• High when idle</li> </ul>	Low when idle	Select clock level when idle.
Mode Fault Error	<ul style="list-style-type: none"> <li>• Enable</li> <li>• Disable</li> </ul>	Disable	Detect master/slave mode conflicts.
Bit Order	<ul style="list-style-type: none"> <li>• MSB First</li> <li>• LSB First</li> </ul>	MSB First	Select the data bit order.
Callback	Name must be a valid C symbol	sci_spi_callback	A user callback function that is called from the sci spi interrupts when a transfer is completed or an error has occurred.
Receive Interrupt Priority	MCU Specific Options		Select the receive interrupt priority.
Transmit Interrupt Priority	MCU Specific Options		Select the transmit interrupt priority.
Transmit End Interrupt Priority	MCU Specific Options		Select the transmit end interrupt priority.
Error Interrupt Priority	MCU Specific Options		Select the error interrupt priority.
Bitrate	Value must be an integer greater than 0	8000000	Enter the desired bitrate.
Bitrate Modulation	<ul style="list-style-type: none"> <li>• Disabled</li> <li>• Enabled</li> </ul>	Disabled	Enabling bitrate modulation reduces the percent error of the actual bitrate with respect to the requested baud rate. It does this by modulating the number of cycles per clock output pulse, so the clock is no longer a square wave.

## Clock Configuration

The clock for this module is derived from the following peripheral clock for each MCU group:

MCU Group	Peripheral Clock
RA2A1	PCLKB
RA4M1	PCLKA
RA4W1	PCLKA
RA6M1	PCLKA
RA6M2	PCLKA
RA6M3	PCLKA
RA6M4	PCLKA

### Pin Configuration

This module uses SCIn\_MOSI, SCIn\_MISO, SCIn\_SPCK, and SCIn\_SS pins to communicate with on board devices.

#### Note

*At high bit rates, it might be necessary to configure the pins with `IOPORT_CFG_DRIVE_HIGH`.*

## Usage Notes

### Transfer Complete Event

The transfer complete event is triggered when all of the data has been transferred. In slave mode if the SS pin is de-asserted then no transfer complete event is generated until the SS pin is asserted and the remaining data is transferred.

### Performance

At high bit rates, interrupts may not be able to service transfers fast enough. In master mode this means there will be a delay between each data frame. In slave mode this could result in RX Overflow errors.

In order to improve performance at high bit rates, it is recommended that the instance be configured to service transfers using the DTC.

### Transmit From RXI Interrupt

After every byte, the SCI SPI peripheral generates a transmit buffer empty interrupt and a receive buffer full interrupt. Whenever possible, the SCI\_SPI module handles both interrupts in the receive buffer full interrupt. This improves performance when the DTC is not being used.

### Slave Select Pin

- In master mode the slave select pin must be driven in software.
- In slave mode the hardware handles the slave select pin and will only transfer data when the SS pin is low.

### Bit Rate Modulation

Depending on the peripheral clock frequency, the desired bit rate may not be achievable. With bit rate modulation, the device can remove a configurable number of input clock pulses to the internal



bit rate counter in order to create the desired bit rate. This has the effect of changing the period of individual bits in order to achieve the desired average bit rate. For more information see section 34.9 Bit Rate Modulation Function in the RA6M3 manual.

## Examples

### Basic Example

This is a basic example of minimal use of the SCI\_SPI in an application.

```
static volatile bool g_transfer_complete = false;
static void r_sci_spi_callback (spi_callback_args_t * p_args)
{
    if (SPI_EVENT_TRANSFER_COMPLETE == p_args->event)
    {
        g_transfer_complete = true;
    }
}

void sci_spi_basic_example (void)
{
    uint8_t tx_buffer[TRANSFER_SIZE];
    uint8_t rx_buffer[TRANSFER_SIZE];
    /* Configure Slave Select Line 1 */
    R_BSP_PinWrite(SLAVE_SELECT_LINE_1, BSP_IO_LEVEL_HIGH);
    /* Configure Slave Select Line 2 */
    R_BSP_PinWrite(SLAVE_SELECT_LINE_2, BSP_IO_LEVEL_HIGH);
    fsp_err_t err = FSP_SUCCESS;
    /* Initialize the SPI module. */
    err = R_SCI_SPI_Open(&g_spi_ctrl, &g_spi_cfg);
    /* Handle any errors. This function should be defined by the user. */
    handle_error(err);
    /* Assert Slave Select Line 1 */
    R_BSP_PinWrite(SLAVE_SELECT_LINE_1, BSP_IO_LEVEL_LOW);
    /* Start a write/read transfer */
    g_transfer_complete = false;
    err = R_SCI_SPI_WriteRead(&g_spi_ctrl, tx_buffer, rx_buffer, TRANSFER_SIZE,
SPI_BIT_WIDTH_8_BITS);
    handle_error(err);
}
```

```
/* Wait for SPI_EVENT_TRANSFER_COMPLETE callback event. */
while (false == g_transfer_complete)
{
    ;
}

/* De-assert Slave Select Line 1 */
R_BSP_PinWrite(SLAVE_SELECT_LINE_1, BSP_IO_LEVEL_HIGH);

/* Wait for minimum time required between transfers. */
R_BSP_SoftwareDelay(SSL_NEXT_ACCESS_DELAY, BSP_DELAY_UNITS_MICROSECONDS);

/* Assert Slave Select Line 2 */
R_BSP_PinWrite(SLAVE_SELECT_LINE_2, BSP_IO_LEVEL_LOW);

/* Start a write/read transfer */
g_transfer_complete = false;
err = R_SCI_SPI_WriteRead(&g_spi_ctrl, tx_buffer, rx_buffer, TRANSFER_SIZE,
SPI_BIT_WIDTH_8_BITS);

handle_error(err);

/* Wait for SPI_EVENT_TRANSFER_COMPLETE callback event. */
while (false == g_transfer_complete)
{
    ;
}

/* De-assert Slave Select Line 2 */
R_BSP_PinWrite(SLAVE_SELECT_LINE_2, BSP_IO_LEVEL_HIGH);
}
```

## Function Documentation

---

◆ **R\_SCI\_SPI\_Open()**

```
fsp_err_t R_SCI_SPI_Open ( spi_ctrl_t * p_api_ctrl, spi_cfg_t const *const p_cfg )
```

Initialize a channel for SPI communication mode. Implements `spi_api_t::open`.

This function performs the following tasks:

- Performs parameter checking and processes error conditions.
- Enables the clock for the SCI channel.
- Initializes the associated registers with default value and the user-configurable options.
- Provides the channel handle for use with other API functions.

**Parameters**

p_api_ctrl	Pointer to the control structure.
p_cfg	Pointer to a configuration structure.

**Return values**

FSP_SUCCESS	Channel initialized successfully.
FSP_ERR_ASSERTION	An input parameter is invalid or NULL.
FSP_ERR_ALREADY_OPEN	The instance has already been opened.
FSP_ERR_IP_CHANNEL_NOT_PRESENT	The channel number is invalid.

## ◆ R\_SCI\_SPI\_Read()

```
fsp_err_t R_SCI_SPI_Read ( spi_ctrl_t *const p_api_ctrl, void * p_dest, uint32_t const length,
spi_bit_width_t const bit_width )
```

Receive data from an SPI device. Implements `spi_api_t::read`.

The function performs the following tasks:

- Performs parameter checking and processes error conditions.
- Enable transmitter.
- Enable receiver.
- Enable interrupts.
- Start data transmission by writing data to the TXD register.
- Receive data from receive buffer full interrupt occurs and copy data to the buffer of destination.
- Complete data reception via receive buffer full interrupt and transmitting dummy data.
- Disable transmitter.
- Disable receiver.
- Disable interrupts.

### Parameters

	<code>p_api_ctrl</code>	Pointer to the control structure.
	<code>p_dest</code>	Pointer to the destination buffer.
[in]	<code>length</code>	The number of bytes to transfer.
[in]	<code>bit_width</code>	Invalid for SCI_SPI (Set to SPI_BIT_WIDTH_8_BITS).

### Return values

FSP_SUCCESS	Read operation successfully completed.
FSP_ERR_ASSERTION	One of the following invalid parameters passed: <ul style="list-style-type: none"> <li>• Pointer <code>p_api_ctrl</code> is NULL</li> <li>• Bit width is not 8 bits</li> <li>• Length is equal to 0</li> <li>• Pointer to destination is NULL</li> </ul>
FSP_ERR_NOT_OPEN	The channel has not been opened. Open the channel first.
FSP_ERR_UNSUPPORTED	The given <code>bit_width</code> is not supported.
FSP_ERR_IN_USE	A transfer is already in progress.

### Returns

See [Common Error Codes](#) or functions called by this function for other possible return codes. This function calls:

- `transfer_api_t::reconfigure`

## ◆ R\_SCI\_SPI\_Write()

```
fsp_err_t R_SCI_SPI_Write ( spi_ctrl_t *const p_api_ctrl, void const * p_src, uint32_t const length,
spi_bit_width_t const bit_width )
```

Transmit data to a SPI device. Implements `spi_api_t::write`.

The function performs the following tasks:

- Performs parameter checking and processes error conditions.
- Enable transmitter.
- Enable interrupts.
- Start data transmission with data via transmit buffer empty interrupt.
- Copy data from source buffer to the SPI data register for transmission.
- Complete data transmission via transmit buffer empty interrupt.
- Disable transmitter.
- Disable receiver.
- Disable interrupts.

### Parameters

	<code>p_api_ctrl</code>	Pointer to the control structure.
	<code>p_src</code>	Pointer to the source buffer.
[in]	<code>length</code>	The number of bytes to transfer.
[in]	<code>bit_width</code>	Invalid for SCI_SPI (Set to SPI_BIT_WIDTH_8_BITS).

### Return values

FSP_SUCCESS	Write operation successfully completed.
FSP_ERR_ASSERTION	One of the following invalid parameters passed: <ul style="list-style-type: none"> <li>• Pointer <code>p_api_ctrl</code> is NULL</li> <li>• Pointer to source is NULL</li> <li>• Length is equal to 0</li> <li>• Bit width is not equal to 8 bits</li> </ul>
FSP_ERR_NOT_OPEN	The channel has not been opened. Open the channel first.
FSP_ERR_UNSUPPORTED	The given <code>bit_width</code> is not supported.
FSP_ERR_IN_USE	A transfer is already in progress.

### Returns

See [Common Error Codes](#) or functions called by this function for other possible return codes. This function calls:

- `transfer_api_t::reconfigure`

### ◆ R\_SCI\_SPI\_WriteRead()

```
fsp_err_t R_SCI_SPI_WriteRead ( spi_ctrl_t *const p_api_ctrl, void const * p_src, void * p_dest,
uint32_t const length, spi_bit_width_t const bit_width )
```

Simultaneously transmit data to SPI device while receiving data from SPI device (full duplex). Implements `spi_api_t::writeRead`.

The function performs the following tasks:

- Performs parameter checking and processes error conditions.
- Enable transmitter.
- Enable receiver.
- Enable interrupts.
- Start data transmission using transmit buffer empty interrupt (or by writing to the TDR register).
- Copy data from source buffer to the SPI data register for transmission.
- Receive data from receive buffer full interrupt and copy data to the destination buffer.
- Complete data transmission and reception via transmit end interrupt.
- Disable transmitter.
- Disable receiver.
- Disable interrupts.

#### Parameters

	<code>p_api_ctrl</code>	Pointer to the control structure.
	<code>p_src</code>	Pointer to the source buffer.
	<code>p_dest</code>	Pointer to the destination buffer.
[in]	<code>length</code>	The number of bytes to transfer.
[in]	<code>bit_width</code>	Invalid for SCI_SPI (Set to <code>SPI_BIT_WIDTH_8_BITS</code> ).

#### Return values

<code>FSP_SUCCESS</code>	Write operation successfully completed.
<code>FSP_ERR_ASSERTION</code>	One of the following invalid parameters passed: <ul style="list-style-type: none"> <li>• Pointer <code>p_api_ctrl</code> is NULL</li> <li>• Pointer to source is NULL</li> <li>• Pointer to destination is NULL</li> <li>• Length is equal to 0</li> <li>• Bit width is not equal to 8 bits</li> </ul>
<code>FSP_ERR_NOT_OPEN</code>	The channel has not been opened. Open the channel first.
<code>FSP_ERR_UNSUPPORTED</code>	The given <code>bit_width</code> is not supported.
<code>FSP_ERR_IN_USE</code>	A transfer is already in progress.

**Returns**

See [Common Error Codes](#) or functions called by this function for other possible return codes. This function calls:

- [transfer\\_api\\_t::reconfigure](#)

**◆ R\_SCI\_SPI\_CallbackSet()**

```
fsp_err_t R_SCI_SPI_CallbackSet ( spi_ctrl_t *const p_api_ctrl, void(*) (spi_callback_args_t *)
p_callback, void const *const p_context, spi_callback_args_t *const p_callback_memory )
```

Updates the user callback and has option of providing memory for callback structure. Implements [spi\\_api\\_t::callbackSet](#)

**Return values**

FSP_SUCCESS	Callback updated successfully.
FSP_ERR_ASSERTION	A required pointer is NULL.
FSP_ERR_NOT_OPEN	The control block has not been opened.

**◆ R\_SCI\_SPI\_Close()**

```
fsp_err_t R_SCI_SPI_Close ( spi_ctrl_t *const p_api_ctrl)
```

Disable the SCI channel and set the instance as not open. Implements [spi\\_api\\_t::close](#).

**Parameters**

p_api_ctrl	Pointer to an opened instance.
------------	--------------------------------

**Return values**

FSP_SUCCESS	Channel successfully closed.
FSP_ERR_ASSERTION	The parameter p_api_ctrl is NULL.
FSP_ERR_NOT_OPEN	The channel has not been opened. Open the channel first.

◆ **R\_SCI\_SPI\_VersionGet()**

```
fsp_err_t R_SCI_SPI_VersionGet ( fsp_version_t * p_version)
```

Get the version information of the underlying driver. Implements `spi_api_t::versionGet`.

**Parameters**

p_version	Pointer to version structure.
-----------	-------------------------------

**Return values**

FSP_SUCCESS	Successful version get.
FSP_ERR_ASSERTION	The parameter p_version is NULL.

◆ **R\_SCI\_SPI\_CalculateBitrate()**

```
fsp_err_t R_SCI_SPI_CalculateBitrate ( uint32_t bitrate, sci_spi_div_setting_t * sclk_div, bool use_mddr )
```

Calculate the register settings required to achieve the desired bitrate.

**Parameters**

[in]	bitrate	bitrate [bps]. For example, 250,000; 500,00; 2,500,000 (max), etc.
	sclk_div	Pointer to <code>sci_spi_div_setting_t</code> used to configure baudrate settings.
[in]	use_mddr	Calculate the divider settings for use with MDDR.

**Return values**

FSP_SUCCESS	Baud rate is set successfully.
FSP_ERR_ASSERTION	Baud rate is not achievable.

**Note**

*The application must pause for 1 bit time after the BRR register is loaded before transmitting/receiving to allow time for the clock to settle.*

**4.2.42 Serial Communications Interface (SCI) UART (r\_sci\_uart)**

## Modules



## Functions

fsp_err_t	R_SCI_UART_Open (uart_ctrl_t *const p_api_ctrl, uart_cfg_t const *const p_cfg)
fsp_err_t	R_SCI_UART_Read (uart_ctrl_t *const p_api_ctrl, uint8_t *const p_dest, uint32_t const bytes)
fsp_err_t	R_SCI_UART_Write (uart_ctrl_t *const p_api_ctrl, uint8_t const *const p_src, uint32_t const bytes)
fsp_err_t	R_SCI_UART_BaudSet (uart_ctrl_t *const p_api_ctrl, void const *const p_baud_setting)
fsp_err_t	R_SCI_UART_InfoGet (uart_ctrl_t *const p_api_ctrl, uart_info_t *const p_info)
fsp_err_t	R_SCI_UART_Close (uart_ctrl_t *const p_api_ctrl)
fsp_err_t	R_SCI_UART_VersionGet (fsp_version_t *p_version)
fsp_err_t	R_SCI_UART_Abort (uart_ctrl_t *const p_api_ctrl, uart_dir_t communication_to_abort)
fsp_err_t	R_SCI_UART_BaudCalculate (uint32_t baudrate, bool bitrate_modulation, uint32_t baud_rate_error_x_1000, baud_setting_t *const p_baud_setting)
fsp_err_t	R_SCI_UART_CallbackSet (uart_ctrl_t *const p_api_ctrl, void(*p_callback)(uart_callback_args_t *), void const *const p_context, uart_callback_args_t *const p_callback_memory)

## Detailed Description

Driver for the SCI peripheral on RA MCUs. This module implements the [UART Interface](#).

## Overview

### Features

The SCI UART module supports the following features:

- Full-duplex UART communication
- Interrupt-driven data transmission and reception
- Invoking the user-callback function with an event code (RX/TX complete, TX data empty, RX char, error, etc)
- Baud-rate change at run-time
- Bit rate modulation and noise cancellation
- RS232 CTS/RTS hardware flow control (with an associated pin)
- RS485 Half/Full Duplex flow control

- Integration with the DTC transfer module
- Abort in-progress read/write operations
- FIFO support on supported channels

## Configuration

### Build Time Configurations for r\_sci\_uart

The following build time configurations are defined in fsp\_cfg/r\_sci\_uart\_cfg.h:

Configuration	Options	Default	Description
Parameter Checking	<ul style="list-style-type: none"> <li>• Default (BSP)</li> <li>• Enabled</li> <li>• Disabled</li> </ul>	Default (BSP)	If selected code for parameter checking is included in the build.
FIFO Support	<ul style="list-style-type: none"> <li>• Enable</li> <li>• Disable</li> </ul>	Disable	Enable FIFO support for the SCI_UART module.
DTC Support	<ul style="list-style-type: none"> <li>• Enable</li> <li>• Disable</li> </ul>	Disable	Enable DTC support for the SCI_UART module.
RS232/RS485 Flow Control Support	<ul style="list-style-type: none"> <li>• Enable</li> <li>• Disable</li> </ul>	Disable	Enable RS232 and RS485 flow control support using a user provided pin.

### Configurations for Driver > Connectivity > UART Driver on r\_sci\_uart

This module can be added to the Stacks tab via New Stack > Driver > Connectivity > UART Driver on r\_sci\_uart. Non-secure callable guard functions can be generated for this module by right clicking the module in the RA Configuration tool and checking the "Non-secure Callable" box.

Configuration	Options	Default	Description
General > Name	Name must be a valid C symbol	g_uart0	Module name.
General > Channel	Value must be an integer between 0 and 9	0	Select the SCI channel.
General > Data Bits	<ul style="list-style-type: none"> <li>• 8bits</li> <li>• 7bits</li> <li>• 9bits</li> </ul>	8bits	Select the number of bits per word.
General > Parity	<ul style="list-style-type: none"> <li>• None</li> <li>• Odd</li> <li>• Even</li> </ul>	None	Select the parity mode.
General > Stop Bits	<ul style="list-style-type: none"> <li>• 1bit</li> <li>• 2bits</li> </ul>	1bit	Select the number of stop bits.
Baud > Baud Rate	Value must be an integer greater than 0	115200	Enter the desired baud rate.
Baud > Baud Rate Modulation	<ul style="list-style-type: none"> <li>• Disabled</li> <li>• Enabled</li> </ul>	Disabled	Enabling baud rate modulation reduces the

percent error of the actual baud rate with respect to the requested baud rate. It does this by modulating the number of cycles per clock, so some bits are slightly longer than others.

Maximum percent error allowed during baud calculation. This is used by the algorithm to determine whether or not to consider using less accurate alternative register settings.

NOTE: The baud calculation does not show an error in the tool if this percent error was not achieved. The calculated percent error is recorded in a comment in the generated [baud\\_setting\\_t](#) structure.

Baud > Max Error (%)	Must be a valid non negative integer with a maximum configurable value of 100	5	
Flow Control > CTS/RTS Selection	<ul style="list-style-type: none"> <li>RTS (CTS is disabled)</li> <li>CTS (Note that RTS is available when enabling External RTS Operation mode which uses 1 GPIO pin)</li> </ul>	RTS (CTS is disabled)	Select CTS or RTS for the CTSn/RTSn pin of SCI channel n. The SCI hardware supports either the CTS or the RTS control signal on this pin but not both.
Flow Control > UART Communication Mode	<ul style="list-style-type: none"> <li>RS232</li> <li>RS485 Half Duplex</li> <li>RS485 Full Duplex</li> </ul>	RS232	Select the UART communication mode as either RS232 or RS485.
Flow Control > Pin Control	<ul style="list-style-type: none"> <li>Enabled</li> <li>Disabled</li> </ul>	Disabled	Enables pin control for external RTS in RS232 mode RS485 mode.
Flow Control > RTS Port	Refer to the RA Configuration tool for available options.	Disabled	Specify the flow control pin port for the MCU.
Flow Control > RTS Pin	Refer to the RA	Disabled	Specify the flow control

	Configuration tool for available options.		pin for the MCU.
Extra > Clock Source	<ul style="list-style-type: none"> <li>Internal Clock</li> <li>Internal Clock With Output on SCK</li> <li>External Clock 8x baud rate</li> <li>External Clock 16x baud rate</li> </ul>	Internal Clock	Selection of the clock source to be used in the baud-rate clock generator. When internal clock is used the baud rate can be output on the SCK pin.
Extra > Start bit detection	<ul style="list-style-type: none"> <li>Falling Edge</li> <li>Low Level</li> </ul>	Falling Edge	Start bit detected as falling edge or low level.
Extra > Noise Filter	<ul style="list-style-type: none"> <li>Enable</li> <li>Disable</li> </ul>	Disable	Enable the digital noise filter on RXDn pin. The digital noise filter block in SCI consists of two-stage flipflop circuits.
Extra > Receive FIFO Trigger Level	<ul style="list-style-type: none"> <li>One</li> <li>Max</li> </ul>	Max	Unused if the channel has no FIFO or if DTC is used for reception. Set to One to get a callback immediately when each byte is received. Set to Max to get a callback when FIFO is full or after 15 bit times with no data (fewer interrupts).
Interrupts > Callback	Name must be a valid C symbol	user_uart_callback	A user callback function can be provided. If this callback function is provided, it will be called from the interrupt service routine (ISR).
Interrupts > Receive Interrupt Priority	MCU Specific Options		Select the receive interrupt priority.
Interrupts > Transmit Data Empty Interrupt Priority	MCU Specific Options		Select the transmit interrupt priority.
Interrupts > Transmit End Interrupt Priority	MCU Specific Options		Select the transmit end interrupt priority.
Interrupts > Error Interrupt Priority	MCU Specific Options		Select the error interrupt priority.

## Clock Configuration

The clock for this module is derived from the following peripheral clock for each MCU group:

MCU Group	Peripheral Clock
RA2A1	PCLKB
RA4M1	PCLKA
RA4W1	PCLKA
RA6M1	PCLKA
RA6M2	PCLKA
RA6M3	PCLKA
RA6M4	PCLKA

The clock source for the baud-rate clock generator can be selected from the internal clock, the external clock times 8 or the external clock times 16. The external clock is supplied to the SCK pin.

### Pin Configuration

This module uses TXD and RXD to communicate to external devices. CTS or RTS can be controlled by the hardware. If both are desired a GPIO pin can be used for RTS. When the internal clock is the source for the baud-rate generator the SCK pin can be used to output a clock with the same frequency as the bit rate.

## Usage Notes

### Limitations

- Transfer size must be less than or equal to 64K bytes if DTC interface is used for transfer. [uart\\_api\\_t::infoGet](#) API can be used to get the max transfer size allowed.
- Reception is still enabled after [uart\\_api\\_t::communicationAbort](#) API is called. Any characters received after abort and before the next call to read will arrive via the callback function with event `UART_EVENT_RX_CHAR`.
- When using 9-bit reception with DTC, clear the upper 7 bits of data before processing the read data. The upper 7 bits contain status flags that are part of the register used to read data in 9-bit mode.

## Examples

### SCI UART Example

```
uint8_t g_dest[TRANSFER_LENGTH];
uint8_t g_src[TRANSFER_LENGTH];
uint8_t g_out_of_band_received[TRANSFER_LENGTH];
uint32_t g_transfer_complete = 0;
uint32_t g_receive_complete = 0;
uint32_t g_out_of_band_index = 0;
```

```
void r_sci_uart_basic_example (void)
{
    /* Initialize p_src to known data */
    for (uint32_t i = 0; i < TRANSFER_LENGTH; i++)
    {
        g_src[i] = (uint8_t) ('A' + (i % 26));
    }

    /* Open the transfer instance with initial configuration. */
    fsp_err_t err = R_SCI_UART_Open(&g_uart0_ctrl, &g_uart0_cfg);
    handle_error(err);

    err = R_SCI_UART_Read(&g_uart0_ctrl, g_dest, TRANSFER_LENGTH);
    handle_error(err);

    err = R_SCI_UART_Write(&g_uart0_ctrl, g_src, TRANSFER_LENGTH);
    handle_error(err);

    while (!g_transfer_complete)
    {
    }

    while (!g_receive_complete)
    {
    }
}

void example_callback (uart_callback_args_t * p_args)
{
    /* Handle the UART event */
    switch (p_args->event)
    {
        /* Received a character */
        case UART_EVENT_RX_CHAR:
        {
            /* Only put the next character in the receive buffer if there is space for it */
            if (sizeof(g_out_of_band_received) > g_out_of_band_index)
            {
                /* Write either the next one or two bytes depending on the receive data size */
                if (UART_DATA_BITS_8 >= g_uart0_cfg.data_bits)

```

```
    {
        g_out_of_band_received[g_out_of_band_index++] = (uint8_t)
p_args->data;
    }
    else
    {
        uint16_t * p_dest = (uint16_t *)
&g_out_of_band_received[g_out_of_band_index];
        *p_dest          = (uint16_t) p_args->data;
        g_out_of_band_index += 2;
    }
}
break;
}

/* Receive complete */
case UART_EVENT_RX_COMPLETE:
    {
        g_receive_complete = 1;
    }
break;

/* Transmit complete */
case UART_EVENT_TX_COMPLETE:
    {
        g_transfer_complete = 1;
    }
break;
}
default:
    {
    }
}
}
```

## SCI UART Baud Set Example

```
#define SCI_UART_BAUDRATE_19200 (19200)
```

```

void r_sci_uart_baud_example (void)
{
    baud_setting_t baud_setting;
    uint32_t      baud_rate          = SCI_UART_BAUDRATE_19200;
    bool          enable_bitrate_modulation = false;
    uint32_t      error_rate_x_1000   = 5;
    fsp_err_t err = R_SCI_UART_BaudCalculate(baud_rate, enable_bitrate_modulation,
error_rate_x_1000, &baud_setting);
    handle_error(err);
    err = R_SCI_UART_BaudSet(&g_uart0_ctrl, (void *) &baud_setting);
    handle_error(err);
}

```

## Data Structures

struct [sci\\_uart\\_instance\\_ctrl\\_t](#)

struct [baud\\_setting\\_t](#)

struct [sci\\_uart\\_extended\\_cfg\\_t](#)

## Enumerations

enum [sci\\_clk\\_src\\_t](#)

enum [uart\\_mode\\_t](#)

enum [sci\\_uart\\_rx\\_fifo\\_trigger\\_t](#)

enum [sci\\_uart\\_start\\_bit\\_detect\\_t](#)

enum [sci\\_uart\\_noise\\_cancellation\\_t](#)

enum [sci\\_uart\\_ctsrts\\_config\\_t](#)

## Data Structure Documentation

### ◆ [sci\\_uart\\_instance\\_ctrl\\_t](#)

struct [sci\\_uart\\_instance\\_ctrl\\_t](#)

UART instance control block.

### ◆ [baud\\_setting\\_t](#)



struct baud_setting_t		
Register settings to acheive a desired baud rate and modulation duty.		
Data Fields		
union <a href="#">baud_setting_t</a>	<code>__unnamed__</code>	
<code>uint8_t</code>	<code>cks: 2</code>	CKS value to get divisor (CKS = N)
<code>uint8_t</code>	<code>brr</code>	Bit Rate Register setting.
<code>uint8_t</code>	<code>mddr</code>	Modulation Duty Register setting.

◆ **sci\_uart\_extended\_cfg\_t**

struct sci_uart_extended_cfg_t		
UART on SCI device Configuration		
Data Fields		
<a href="#">sci_clk_src_t</a>	<code>clock</code>	The source clock for the baud-rate generator. If internal optionally output baud rate on SCK.
<a href="#">sci_uart_start_bit_detect_t</a>	<code>rx_edge_start</code>	Start reception on falling edge.
<a href="#">sci_uart_noise_cancellation_t</a>	<code>noise_cancel</code>	Noise cancellation setting.
<a href="#">baud_setting_t</a> *	<code>p_baud_setting</code>	Register settings for a desired baud rate.
<a href="#">sci_uart_rx_fifo_trigger_t</a>	<code>rx_fifo_trigger</code>	Receive FIFO trigger level, unused if channel has no FIFO or if DTC is used.
<a href="#">uart_mode_t</a>	<code>uart_mode</code>	UART communication mode selection.
<a href="#">bsp_io_port_pin_t</a>	<code>flow_control_pin</code>	UART Driver Enable pin.
<a href="#">sci_uart_ctsrts_config_t</a>	<code>ctsrts_en</code>	CTS/RTS function of the SSn pin.

**Enumeration Type Documentation**

◆ **sci\_clk\_src\_t**

enum sci_clk_src_t	
Enumeration for SCI clock source	
Enumerator	
SCI_UART_CLOCK_INT	Use internal clock for baud generation.
SCI_UART_CLOCK_INT_WITH_BAUDRATE_OUTPUT	Use internal clock for baud generation and output on SCK.
SCI_UART_CLOCK_EXT8X	Use external clock 8x baud rate.
SCI_UART_CLOCK_EXT16X	Use external clock 16x baud rate.

◆ **uart\_mode\_t**

enum uart_mode_t	
UART communication mode definition	
Enumerator	
UART_MODE_RS232	Enables RS232 communication mode.
UART_MODE_RS485_HD	Enables RS485 half duplex communication mode.
UART_MODE_RS485_FD	Enables RS485 full duplex communication mode.

◆ **sci\_uart\_rx\_fifo\_trigger\_t**

enum sci_uart_rx_fifo_trigger_t	
Receive FIFO trigger configuration.	
Enumerator	
SCI_UART_RX_FIFO_TRIGGER_1	Callback after each byte is received without buffering.
SCI_UART_RX_FIFO_TRIGGER_MAX	Callback when FIFO is full or after 15 bit times with no data (fewer interrupts)

◆ **sci\_uart\_start\_bit\_detect\_t**

enum <code>sci_uart_start_bit_detect_t</code>	
Asynchronous Start Bit Edge Detection configuration.	
Enumerator	
<code>SCI_UART_START_BIT_LOW_LEVEL</code>	Detect low level on RXDn pin as start bit.
<code>SCI_UART_START_BIT_FALLING_EDGE</code>	Detect falling level on RXDn pin as start bit.

◆ **sci\_uart\_noise\_cancellation\_t**

enum <code>sci_uart_noise_cancellation_t</code>	
Noise cancellation configuration.	
Enumerator	
<code>SCI_UART_NOISE_CANCELLATION_DISABLE</code>	Disable noise cancellation.
<code>SCI_UART_NOISE_CANCELLATION_ENABLE</code>	Enable noise cancellation.

◆ **sci\_uart\_ctsrts\_config\_t**

enum <code>sci_uart_ctsrts_config_t</code>	
CTS/RTS function of the SSn pin.	
Enumerator	
<code>SCI_UART_CTSRTS_RTS_OUTPUT</code>	Disable CTS function (RTS output function is enabled)
<code>SCI_UART_CTSRTS_CTS_INPUT</code>	Enable CTS function.

**Function Documentation**

◆ **R\_SCI\_UART\_Open()**

```
fsp_err_t R_SCI_UART_Open ( uart_ctrl_t *const p_api_ctrl, uart_cfg_t const *const p_cfg )
```

Configures the UART driver based on the input configurations. If reception is enabled at compile time, reception is enabled at the end of this function. Implements [uart\\_api\\_t::open](#)

**Return values**

FSP_SUCCESS	Channel opened successfully.
FSP_ERR_ASSERTION	Pointer to UART control block or configuration structure is NULL.
FSP_ERR_IP_CHANNEL_NOT_PRESENT	The requested channel does not exist on this MCU.
FSP_ERR_ALREADY_OPEN	Control block has already been opened or channel is being used by another instance. Call close() then open() to reconfigure.

**Returns**

See [Common Error Codes](#) or functions called by this function for other possible return codes. This function calls:

- [transfer\\_api\\_t::open](#)

◆ **R\_SCI\_UART\_Read()**

```
fsp_err_t R_SCI_UART_Read ( uart_ctrl_t *const p_api_ctrl, uint8_t *const p_dest, uint32_t const bytes )
```

Receives user specified number of bytes into destination buffer pointer. Implements [uart\\_api\\_t::read](#)

**Return values**

FSP_SUCCESS	Data reception successfully ends.
FSP_ERR_ASSERTION	Pointer to UART control block is NULL. Number of transfers outside the max or min boundary when transfer instance used
FSP_ERR_INVALID_ARGUMENT	Destination address or data size is not valid for 9-bit mode.
FSP_ERR_NOT_OPEN	The control block has not been opened
FSP_ERR_IN_USE	A previous read operation is still in progress.
FSP_ERR_UNSUPPORTED	SCI_UART_CFG_RX_ENABLE is set to 0

**Returns**

See [Common Error Codes](#) or functions called by this function for other possible return codes. This function calls:

- [transfer\\_api\\_t::reset](#)

**Note**

*If 9-bit data length is specified at R\_SCI\_UART\_Open call, p\_dest must be aligned 16-bit boundary.*

◆ **R\_SCI\_UART\_Write()**

```
fsp_err_t R_SCI_UART_Write ( uart_ctrl_t *const p_api_ctrl, uint8_t const *const p_src, uint32_t const bytes )
```

Transmits user specified number of bytes from the source buffer pointer. Implements [uart\\_api\\_t::write](#)

**Return values**

FSP_SUCCESS	Data transmission finished successfully.
FSP_ERR_ASSERTION	Pointer to UART control block is NULL. Number of transfers outside the max or min boundary when transfer instance used
FSP_ERR_INVALID_ARGUMENT	Source address or data size is not valid for 9-bit mode.
FSP_ERR_NOT_OPEN	The control block has not been opened
FSP_ERR_IN_USE	A UART transmission is in progress
FSP_ERR_UNSUPPORTED	SCI_UART_CFG_TX_ENABLE is set to 0

**Returns**

See [Common Error Codes](#) or functions called by this function for other possible return codes. This function calls:

- [transfer\\_api\\_t::reset](#)

**Note**

*If 9-bit data length is specified at R\_SCI\_UART\_Open call, p\_src must be aligned on a 16-bit boundary.*

◆ **R\_SCI\_UART\_BaudSet()**

```
fsp_err_t R_SCI_UART_BaudSet ( uart_ctrl_t *const p_api_ctrl, void const *const p_baud_setting )
```

Updates the baud rate using the clock selected in Open. p\_baud\_setting is a pointer to a [baud\\_setting\\_t](#) structure. Implements [uart\\_api\\_t::baudSet](#)

**Warning**

This terminates any in-progress transmission.

**Return values**

FSP_SUCCESS	Baud rate was successfully changed.
FSP_ERR_ASSERTION	Pointer to UART control block is NULL or the UART is not configured to use the internal clock.
FSP_ERR_NOT_OPEN	The control block has not been opened

## ◆ R\_SCI\_UART\_InfoGet()

```
fsp_err_t R_SCI_UART_InfoGet ( uart_ctrl_t *const p_api_ctrl, uart_info_t *const p_info )
```

Provides the driver information, including the maximum number of bytes that can be received or transmitted at a time. Implements `uart_api_t::infoGet`

**Return values**

FSP_SUCCESS	Information stored in provided p_info.
FSP_ERR_ASSERTION	Pointer to UART control block is NULL.
FSP_ERR_NOT_OPEN	The control block has not been opened

## ◆ R\_SCI\_UART\_Close()

```
fsp_err_t R_SCI_UART_Close ( uart_ctrl_t *const p_api_ctrl)
```

Aborts any in progress transfers. Disables interrupts, receiver, and transmitter. Closes lower level transfer drivers if used. Removes power. Implements `uart_api_t::close`

**Return values**

FSP_SUCCESS	Channel successfully closed.
FSP_ERR_ASSERTION	Pointer to UART control block is NULL.
FSP_ERR_NOT_OPEN	The control block has not been opened

## ◆ R\_SCI\_UART\_VersionGet()

```
fsp_err_t R_SCI_UART_VersionGet ( fsp_version_t * p_version)
```

Provides API and code version in the user provided pointer. Implements `uart_api_t::versionGet`

**Parameters**

[in]	p_version	Version number set here
------	-----------	-------------------------

**Return values**

FSP_SUCCESS	Version information stored in provided p_version.
FSP_ERR_ASSERTION	p_version is NULL.

◆ **R\_SCI\_UART\_Abort()**

```
fsp_err_t R_SCI_UART_Abort ( uart_ctrl_t *const p_api_ctrl, uart_dir_t communication_to_abort )
```

Provides API to abort ongoing transfer. Transmission is aborted after the current character is transmitted. Reception is still enabled after abort(). Any characters received after abort() and before the transfer is reset in the next call to read(), will arrive via the callback function with event UART\_EVENT\_RX\_CHAR. Implements [uart\\_api\\_t::communicationAbort](#)

**Return values**

FSP_SUCCESS	UART transaction aborted successfully.
FSP_ERR_ASSERTION	Pointer to UART control block is NULL.
FSP_ERR_NOT_OPEN	The control block has not been opened.
FSP_ERR_UNSUPPORTED	The requested Abort direction is unsupported.

**Returns**

See [Common Error Codes](#) or functions called by this function for other possible return codes. This function calls:

- [transfer\\_api\\_t::disable](#)

◆ **R\_SCI\_UART\_BaudCalculate()**

```
fsp_err_t R_SCI_UART_BaudCalculate ( uint32_t baudrate, bool bitrate_modulation, uint32_t
baud_rate_error_x_1000, baud_setting_t*const p_baud_setting )
```

Calculates baud rate register settings. Evaluates and determines the best possible settings set to the baud rate related registers.

**Parameters**

[in]	baudrate	Baud rate [bps]. For example, 19200, 57600, 115200, etc.
[in]	bitrate_modulation	Enable bitrate modulation
[in]	baud_rate_error_x_1000	<baud_rate_percent_error> x 1000 required for module to function. Absolute max baud_rate_error is 15000 (15%).
[out]	p_baud_setting	Baud setting information stored here if successful

**Return values**

FSP_SUCCESS	Baud rate is set successfully
FSP_ERR_ASSERTION	Null pointer
FSP_ERR_INVALID_ARGUMENT	Baud rate is '0', source clock frequency could not be read, or error in calculated baud rate is larger than 10%.

◆ **R\_SCI\_UART\_CallbackSet()**

```
fsp_err_t R_SCI_UART_CallbackSet ( uart_ctrl_t*const p_api_ctrl, void(*)(uart_callback_args_t*)
p_callback, void const*const p_context, uart_callback_args_t*const p_callback_memory )
```

Updates the user callback and has option of providing memory for callback structure. Implements `uart_api_t::callbackSet`

**Return values**

FSP_SUCCESS	Callback updated successfully.
FSP_ERR_ASSERTION	A required pointer is NULL.
FSP_ERR_NOT_OPEN	The control block has not been opened.



## 4.2.43 Sigma Delta Analog to Digital Converter (r\_sdadc)

### Modules

#### Functions

fsp\_err\_t R\_SDADC\_Open (adc\_ctrl\_t \*p\_ctrl, adc\_cfg\_t const \*const p\_cfg)

fsp\_err\_t R\_SDADC\_ScanCfg (adc\_ctrl\_t \*p\_ctrl, void const \*const p\_extend)

fsp\_err\_t R\_SDADC\_InfoGet (adc\_ctrl\_t \*p\_ctrl, adc\_info\_t \*p\_adc\_info)

fsp\_err\_t R\_SDADC\_ScanStart (adc\_ctrl\_t \*p\_ctrl)

fsp\_err\_t R\_SDADC\_ScanStop (adc\_ctrl\_t \*p\_ctrl)

fsp\_err\_t R\_SDADC\_StatusGet (adc\_ctrl\_t \*p\_ctrl, adc\_status\_t \*p\_status)

fsp\_err\_t R\_SDADC\_Read (adc\_ctrl\_t \*p\_ctrl, adc\_channel\_t const reg\_id, uint16\_t \*const p\_data)

fsp\_err\_t R\_SDADC\_Read32 (adc\_ctrl\_t \*p\_ctrl, adc\_channel\_t const reg\_id, uint32\_t \*const p\_data)

fsp\_err\_t R\_SDADC\_OffsetSet (adc\_ctrl\_t \*const p\_ctrl, adc\_channel\_t const reg\_id, int32\_t const offset)

fsp\_err\_t R\_SDADC\_Calibrate (adc\_ctrl\_t \*const p\_ctrl, void \*const p\_extend)

fsp\_err\_t R\_SDADC\_Close (adc\_ctrl\_t \*p\_ctrl)

fsp\_err\_t R\_SDADC\_VersionGet (fsp\_version\_t \*const p\_version)

#### Detailed Description

Driver for the SDADC24 peripheral on RA MCUs. This module implements the [ADC Interface](#).

## Overview

### Features

The SDADC module supports the following features:

- 24 bit maximum resolution
- Configure scans to include:
  - Multiple analog channels
  - Outputs of OPAMP0 (P side) and OPAMP1 (N side) of SDADC channel 4
- Configurable scan start trigger:
  - Software scan triggers
  - Hardware scan triggers (timer expiration, for example)

- Configurable scan mode:
  - Single scan mode, where each trigger starts a single scan
  - Continuous scan mode, where all channels are scanned continuously
- Supports averaging converted samples
- Optional callback when single conversion, entire scan, or calibration completes
- Supports reading converted data
- Sample and hold support

## Selecting an ADC

All RA MCUs have an [Analog to Digital Converter \(r\\_adc\)](#). Only select RA MCUs have an SDADC. When selecting between them, consider these factors. Refer to the hardware manual for details.

	ADC	SDADC
Availability	Available on all RA MCUs.	Available on select RA MCUs.
Resolution	The ADC has a maximum resolution of 12, 14, or 16 bits depending on the MCU.	The SDADC has a maximum accuracy of 24 bits.
Number of Channels	The ADC has more channels than the SDADC.	The SDADC 5 channels, one of which is tied to OPAMP0 and OPAMP1.
Frequency	The ADC sampling time is shorter (more samples per second).	The SDADC sampling time is longer (fewer samples per second).
Settling Time	The ADC does not have a settling time when switching between channels.	The SDADC requires a settling time when switching between channels.

## Configuration

### Build Time Configurations for r\_sdadc

The following build time configurations are defined in fsp\_cfg/r\_sdadc\_cfg.h:

Configuration	Options	Default	Description
Parameter Checking	<ul style="list-style-type: none"> <li>• Default (BSP)</li> <li>• Enabled</li> <li>• Disabled</li> </ul>	Default (BSP)	If selected code for parameter checking is included in the build.

### Configurations for Driver > Analog > ADC Driver on r\_sdadc

This module can be added to the Stacks tab via New Stack > Driver > Analog > ADC Driver on r\_sdadc.

Configuration	Options	Default	Description
Name	Name must be a valid C symbol	g_adc0	Module name.

Mode	<ul style="list-style-type: none"> <li>• Single Scan</li> <li>• Continuous Scan</li> </ul>	Continuous Scan	In single scan mode, all channels are converted once per start trigger, and conversion stops after all enabled channels are scanned. In continuous scan mode, conversion starts after a start trigger, then continues until stopped in software.
Resolution	<ul style="list-style-type: none"> <li>• 16 Bit</li> <li>• 24 Bit</li> </ul>	24 Bit	Select 24-bit or 16-bit resolution.
Alignment	<ul style="list-style-type: none"> <li>• Right</li> <li>• Left</li> </ul>	Right	Select left or right alignment.
Trigger	MCU Specific Options		Select conversion start trigger. Conversion can be started in software, or conversion can be started when a hardware event occurs if the hardware event is linked to the SDADC peripheral using the ELC API.
Vref Source	<ul style="list-style-type: none"> <li>• Internal</li> <li>• External</li> </ul>	Internal	Vref can be source internally and output on the SBIAS pin, or Vref can be input from VREFI.
Vref Voltage	<ul style="list-style-type: none"> <li>• 0.8 V</li> <li>• 1.0 V</li> <li>• 1.2 V</li> <li>• 1.4 V</li> <li>• 1.6 V</li> <li>• 1.8 V</li> <li>• 2.0 V</li> <li>• 2.2 V</li> <li>• 2.4 V</li> </ul>	1.0 V	Select Vref voltage. If Vref is input externally, the voltage on VREFI must match the voltage selected within 3%.
Callback	Name must be a valid C symbol	NULL	Enter the name of the callback function to be called when conversion completes or a scan ends.
Conversion End Interrupt Priority	MCU Specific Options		[Required] Select the interrupt priority for the conversion end interrupt.
Scan End Interrupt	MCU Specific Options		[Optional] Select the

Priority		interrupt priority for the scan end interrupt.
Calibration End Interrupt Priority	MCU Specific Options	[Optional] Select the interrupt priority for the calibration end interrupt.

### Configurations for Driver > Analog > SDADC Channel Configuration on r\_sdadc

This module can be added to the Stacks tab via New Stack > Driver > Analog > SDADC Channel Configuration on r\_sdadc.

Configuration	Options	Default	Description
Input	<ul style="list-style-type: none"> <li>Differential</li> <li>Single Ended</li> </ul>	Differential	Select differential or single-ended input.
Stage 1 Gain	<ul style="list-style-type: none"> <li>1</li> <li>2</li> <li>3</li> <li>4</li> <li>8</li> </ul>	1	Select the gain for stage 1 of the PGA. Must be 1 for single-ended input.
Stage 2 Gain	<ul style="list-style-type: none"> <li>1</li> <li>2</li> <li>4</li> <li>8</li> </ul>	1	Select the gain for stage 2 of the PGA. Must be 1 for single-ended input.
Oversampling Ratio	<ul style="list-style-type: none"> <li>64</li> <li>128</li> <li>256</li> <li>512</li> <li>1024</li> <li>2048</li> </ul>	256	Select the oversampling ratio for the PGA. Must be 256 for single-ended input.
Polarity (Valid for Single-Ended Input Only)	<ul style="list-style-type: none"> <li>Positive</li> <li>Negative</li> </ul>	Positive	Select positive or negative polarity for single-ended input. VBIAS (1.0 V typical) is connected on the opposite input.
Conversions to Average per Result	<ul style="list-style-type: none"> <li>Do Not Average (Interrupt after Each Conversion)</li> <li>Average 8</li> <li>Average 16</li> <li>Average 32</li> <li>Average 64</li> </ul>	Do Not Average (Interrupt after Each Conversion)	Select the number of conversions to average for each result. The AD_C_EVENT_CONVERSION_END event occurs after each average, or after each individual conversion if averaging is disabled.
Invert (Valid for Negative Single-Ended Input Only)	<ul style="list-style-type: none"> <li>Result Not Inverted</li> <li>Result Inverted</li> </ul>	Result Not Inverted	Select whether to invert negative single-ended input. When the result is inverted, the lowest measurable

voltage gives a result of 0, and the highest measurable voltage gives a result of  $2^{\text{resolution}} - 1$ .

Number of conversions on this channel before AUTOSCAN moves to the next channel. When all conversions of all channels are complete, the ADC\_EVENT\_SCAN\_END event occurs.

Number of Conversions Per Scan      Refer to the RA Configuration tool for available options.      1

## Clock Configuration

The SDADC clock is configurable on the clocks tab.

The SDADC clock must be 4 MHz when the SDADC is used.

## Pin Configuration

The ANSDnP (n = 0-3) pins are analog input channels that can be used with the SDADC.

# Usage Notes

## Scan Procedure

In this document, the term "scan" refers to the AUTOSCAN feature of the SDADC, which works as follows:

1. Conversions are performed on enabled channels in ascending order of channel number. All conversions required for a single channel are completed before the sequencer moves to the next channel.
2. Conversions are performed at the rate (in Hz) of the SDADC oversampling clock frequency / oversampling ratio (configured per channel). The FSP uses the normal mode SDADC oversampling clock frequency.
3. If averaging is enabled for the channel, the number of conversions to average are performed before each conversion end interrupt occurs.
4. If the number of conversions for the channel is more than 1, SDADC performs the number of conversions requested. These are performed consecutively. There is a settling time associated with switching channels. Performing all of the requested conversions for each channel at a time avoids this settling time after the first conversion.

If averaging is enabled for the channel, each averaged result counts as a single conversion.

5. Continues to the next enabled channel only after completing all conversions requested.
6. After all enabled channels are scanned, a scan end interrupt occurs. The driver supports single-scan and continuous scan operation modes.
  - Single-scan mode performs one scan per trigger (hardware trigger or software start using `R_SDADC_ScanStart`).

- In continuous scan mode, the scan is restarted after each scan completes. A single trigger is required to start continuous operation of the SDADC.

## When Interrupts Are Not Enabled

If interrupts are not enabled, the `R_SDADC_StatusGet()` API can be used to poll the SDADC to determine when the scan has completed. The `R_SDADC_Read()` API function is used to access the converted SDADC result. This applies to both normal scans and calibration scans.

## Calibration

Calibration is required to use the SDADC if any channel is configured for differential mode. Call `R_SDADC_Calibrate()` after open, and prior to any other function, then wait for a calibration complete event before using the SDADC. `R_SDADC_Calibrate()` should not be called if all channels are configured for single-ended mode.

# Examples

## Basic Example

This is a basic example of minimal use of the SDADC in an application.

```
void sdadc_basic_example (void)
{
    fsp_err_t err = FSP_SUCCESS;
    /* Initializes the module. */
    err = R_SDADC_Open(&g_adc0_ctrl, &g_adc0_cfg);
    /* Handle any errors. This function should be defined by the user. */
    handle_error(err);
    /* Calibrate all differential channels. */
    sdadc_calibrate_args_t calibrate_args;
    calibrate_args.mode      = SDADC_CALIBRATION_INTERNAL_GAIN_OFFSET;
    calibrate_args.channel = ADC_CHANNEL_0;
    err = R_SDADC_Calibrate(&g_adc0_ctrl, &calibrate_args);
    handle_error(err);
    /* Wait for calibration to complete. */
    adc_status_t status;
    status.state = ADC_STATE_SCAN_IN_PROGRESS;
    while (ADC_STATE_SCAN_IN_PROGRESS == status.state)
    {
        R_SDADC_StatusGet(&g_adc0_ctrl, &status);
    }
}
```

```
/* In software trigger mode, start a scan by calling R_SDADC_ScanStart(). In other
modes, enable external
* triggers by calling R_SDADC_ScanStart(). */
(void) R_SDADC_ScanStart(&g_adc0_ctrl);
/* Wait for conversion to complete. */
status.state = ADC_STATE_SCAN_IN_PROGRESS;
while (ADC_STATE_SCAN_IN_PROGRESS == status.state)
{
R_SDADC_StatusGet(&g_adc0_ctrl, &status);
}
/* Read converted data. */
uint32_t channell_conversion_result;
R_SDADC_Read32(&g_adc0_ctrl, ADC_CHANNEL_1, &channell_conversion_result);
}
```

## Using DTC or DMAC with the SDADC

If desired, the DTC or DMAC can be used to store each conversion result in a circular buffer. An example configuration is below.

```
/* Example DTC transfer settings to used with SDADC. */
/* The transfer length should match the total number of conversions per scan. This
example assumes the SDADC is
* configured to scan channel 1 three times, then channel 2 and channel 4 once, for a
total of 5 conversions. */
#define SDADC_EXAMPLE_TRANSFER_LENGTH (5)
uint32_t g_sdadc_example_buffer[SDADC_EXAMPLE_TRANSFER_LENGTH];
transfer_info_t g_sdadc_transfer_info =
{
.dest_addr_mode = TRANSFER_ADDR_MODE_INCREMENTED,
.repeat_area = TRANSFER_REPEAT_AREA_DESTINATION,
.irq = TRANSFER_IRQ_END,
.chain_mode = TRANSFER_CHAIN_MODE_DISABLED,
.src_addr_mode = TRANSFER_ADDR_MODE_FIXED,
.mode = TRANSFER_MODE_REPEAT,
}
```

```
/* NOTE: The data transferred will contain a 24-bit converted value in bits 23:0.
Bit 24 contains a status flag
* indicating if the result overflowed or not. Bits 27:25 contain the channel number
+ 1. The settings for
* resolution and alignment and ignored when DTC or DMAC is used. */
.size = TRANSFER_SIZE_4_BYTE,
/* NOTE: It is strongly recommended to enable averaging on all channels or no
channels when using DTC with SDADC
* because the result register is different when averaging is used. If averaging is
enabled on all channels,
* set transfer_info_t::p_src to &R_SDADC->ADAR. */
.p_src = (void const *) &R_SDADC0->ADCR,
.p_dest = &g_sdadc_example_buffer[0],
.length = SDADC_EXAMPLE_TRANSFER_LENGTH,
};
void sdadc_dtc_example (void)
{
    fsp_err_t err = FSP_SUCCESS;
    /* Initializes the module. */
    err = R_SDADC_Open(&g_adc0_ctrl, &g_adc0_cfg);
    /* Handle any errors. This function should be defined by the user. */
    handle_error(err);
    /* Calibrate all differential channels. */
    sdadc_calibrate_args_t calibrate_args;
    calibrate_args.mode = SDADC_CALIBRATION_INTERNAL_GAIN_OFFSET;
    calibrate_args.channel = ADC_CHANNEL_0;
    err = R_SDADC_Calibrate(&g_adc0_ctrl, &calibrate_args);
    handle_error(err);
    /* Wait for calibration to complete. */
    adc_status_t status;
    status.state = ADC_STATE_SCAN_IN_PROGRESS;
    while (ADC_STATE_SCAN_IN_PROGRESS == status.state)
    {
        R_SDADC_StatusGet(&g_adc0_ctrl, &status);
    }
}
```



```
    }

    /* In software trigger mode, start a scan by calling R_SDADC_ScanStart(). In other
modes, enable external
    * triggers by calling R_SDADC_ScanStart(). */
    (void) R_SDADC_ScanStart(&g_adc0_ctrl);

    /* After each conversion, the converted data is transferred to the next index in
g_sdadc_example_buffer. After
    * the entire scan completes, the index in g_sdadc_example_buffer resets. The data
in g_sdadc_example_buffer
    * is:
    * - g_sdadc_example_buffer[0] = SDADC channel 1 conversion 0
    * - g_sdadc_example_buffer[1] = SDADC channel 1 conversion 1
    * - g_sdadc_example_buffer[2] = SDADC channel 1 conversion 2
    * - g_sdadc_example_buffer[3] = SDADC channel 2 conversion 0
    * - g_sdadc_example_buffer[4] = SDADC channel 4 conversion 0
    **/
    /* At any point in the application after the first scan completes, the most
recent data for channel 2 can be read
    * from the buffer like this. Shifting removes the unrelated bits in the result
register and propagates the sign
    * bit so the value can be interpreted as a signed result. This assumes channel 2 is
configured in differential
    * mode. */
    int32_t channel_2_data = (int32_t) (g_sdadc_example_buffer[3] << 8) >> 8;
    FSP_PARAMETER_NOT_USED(channel_2_data);
}
```

## Data Structures

struct [sdadc\\_calibrate\\_args\\_t](#)

struct [sdadc\\_channel\\_cfg\\_t](#)

struct [sdadc\\_scan\\_cfg\\_t](#)

struct [sdadc\\_extended\\_cfg\\_t](#)

struct [sdadc\\_instance\\_ctrl\\_t](#)

## Enumerations

enum [sdadc\\_vref\\_src\\_t](#)enum [sdadc\\_vref\\_voltage\\_t](#)enum [sdadc\\_channel\\_input\\_t](#)enum [sdadc\\_channel\\_stage\\_1\\_gain\\_t](#)enum [sdadc\\_channel\\_stage\\_2\\_gain\\_t](#)enum [sdadc\\_channel\\_oversampling\\_t](#)enum [sdadc\\_channel\\_polarity\\_t](#)enum [sdadc\\_channel\\_average\\_t](#)enum [sdadc\\_channel\\_inversion\\_t](#)enum [sdadc\\_channel\\_count\\_formula\\_t](#)enum [sdadc\\_calibration\\_t](#)

## Data Structure Documentation

### ◆ [sdadc\\_calibrate\\_args\\_t](#)

struct <a href="#">sdadc_calibrate_args_t</a>		
Structure to pass to the <a href="#">adc_api_t::calibrate</a> p_extend argument.		
Data Fields		
<a href="#">adc_channel_t</a>	channel	Which channel to calibrate.
<a href="#">sdadc_calibration_t</a>	mode	Calibration mode.

### ◆ [sdadc\\_channel\\_cfg\\_t](#)

struct <a href="#">sdadc_channel_cfg_t</a>		
SDADC per channel configuration.		

### ◆ [sdadc\\_scan\\_cfg\\_t](#)

struct <a href="#">sdadc_scan_cfg_t</a>		
SDADC active channel configuration		
Data Fields		
uint32_t	scan_mask	Channels/bits: bit 0 is ch0; bit 15 is ch15.

### ◆ [sdadc\\_extended\\_cfg\\_t](#)

struct sdadc_extended_cfg_t		
SDADC configuration extension. This extension is required and must be provided in <a href="#">adc_cfg_t::p_extend</a> .		
Data Fields		
uint8_t	conv_end_ipl	Conversion end interrupt priority.
IRQn_Type	conv_end_irq	
<a href="#">sdadc_vref_src_t</a>	vref_src	Source of Vref (internal or external)
<a href="#">sdadc_vref_voltage_t</a>	vref_voltage	Voltage of Vref, required for both internal and external Vref. If Vref is from an external source, the voltage must match the specified voltage within 3%.
<a href="#">sdadc_channel_cfg_t</a> const *	p_channel_cfgs[SDADC_MAX_NUM_CHANNELS]	Configuration for each channel, set to NULL if unused.

#### ◆ sdadc\_instance\_ctrl\_t

struct sdadc_instance_ctrl_t
ADC instance control block. DO NOT INITIALIZE. Initialized in <a href="#">adc_api_t::open()</a> .

## Enumeration Type Documentation

#### ◆ sdadc\_vref\_src\_t

enum sdadc_vref_src_t	
Source of Vref.	
Enumerator	
SDADC_VREF_SRC_INTERNAL	Vref is internally sourced, can be output as SBIAS.
SDADC_VREF_SRC_EXTERNAL	Vref is externally sourced from the VREFI pin.

◆ **sdadc\_vref\_voltage\_t**

enum <code>sdadc_vref_voltage_t</code>	
Voltage of Vref.	
Enumerator	
<code>SDADC_VREF_VOLTAGE_800_MV</code>	Vref is 0.8 V.
<code>SDADC_VREF_VOLTAGE_1000_MV</code>	Vref is 1.0 V.
<code>SDADC_VREF_VOLTAGE_1200_MV</code>	Vref is 1.2 V.
<code>SDADC_VREF_VOLTAGE_1400_MV</code>	Vref is 1.4 V.
<code>SDADC_VREF_VOLTAGE_1600_MV</code>	Vref is 1.6 V.
<code>SDADC_VREF_VOLTAGE_1800_MV</code>	Vref is 1.8 V.
<code>SDADC_VREF_VOLTAGE_2000_MV</code>	Vref is 2.0 V.
<code>SDADC_VREF_VOLTAGE_2200_MV</code>	Vref is 2.2 V.
<code>SDADC_VREF_VOLTAGE_2400_MV</code>	Vref is 2.4 V (only valid for external Vref)

◆ **sdadc\_channel\_input\_t**

enum <code>sdadc_channel_input_t</code>	
Per channel input mode.	
Enumerator	
<code>SDADC_CHANNEL_INPUT_DIFFERENTIAL</code>	Differential input.
<code>SDADC_CHANNEL_INPUT_SINGLE_ENDED</code>	Single-ended input.

◆ **sdadc\_channel\_stage\_1\_gain\_t**

enum <code>sdadc_channel_stage_1_gain_t</code>	
Per channel stage 1 gain options.	
Enumerator	
<code>SDADC_CHANNEL_STAGE_1_GAIN_1</code>	Gain of 1.
<code>SDADC_CHANNEL_STAGE_1_GAIN_2</code>	Gain of 2.
<code>SDADC_CHANNEL_STAGE_1_GAIN_3</code>	Gain of 3 (only valid for stage 1)
<code>SDADC_CHANNEL_STAGE_1_GAIN_4</code>	Gain of 4.
<code>SDADC_CHANNEL_STAGE_1_GAIN_8</code>	Gain of 8.

◆ **sdadc\_channel\_stage\_2\_gain\_t**

enum <code>sdadc_channel_stage_2_gain_t</code>	
Per channel stage 2 gain options.	
Enumerator	
<code>SDADC_CHANNEL_STAGE_2_GAIN_1</code>	Gain of 1.
<code>SDADC_CHANNEL_STAGE_2_GAIN_2</code>	Gain of 2.
<code>SDADC_CHANNEL_STAGE_2_GAIN_4</code>	Gain of 4.
<code>SDADC_CHANNEL_STAGE_2_GAIN_8</code>	Gain of 8.

◆ **sdadc\_channel\_oversampling\_t**

enum <code>sdadc_channel_oversampling_t</code>	
Per channel oversampling ratio.	
Enumerator	
<code>SDADC_CHANNEL_OVERSAMPLING_64</code>	Oversampling ratio of 64.
<code>SDADC_CHANNEL_OVERSAMPLING_128</code>	Oversampling ratio of 128.
<code>SDADC_CHANNEL_OVERSAMPLING_256</code>	Oversampling ratio of 256.
<code>SDADC_CHANNEL_OVERSAMPLING_512</code>	Oversampling ratio of 512.
<code>SDADC_CHANNEL_OVERSAMPLING_1024</code>	Oversampling ratio of 1024.
<code>SDADC_CHANNEL_OVERSAMPLING_2048</code>	Oversampling ratio of 2048.

◆ **sdadc\_channel\_polarity\_t**

enum <code>sdadc_channel_polarity_t</code>	
Per channel polarity, valid for single-ended input only.	
Enumerator	
<code>SDADC_CHANNEL_POLARITY_POSITIVE</code>	Positive-side single-ended input.
<code>SDADC_CHANNEL_POLARITY_NEGATIVE</code>	Negative-side single-ended input.

◆ **sdadc\_channel\_average\_t**

enum <code>sdadc_channel_average_t</code>	
Per channel number of conversions to average before conversion end callback.	
Enumerator	
<code>SDADC_CHANNEL_AVERAGE_NONE</code>	Do not average (callback for each conversion)
<code>SDADC_CHANNEL_AVERAGE_8</code>	Average 8 samples for each conversion end callback.
<code>SDADC_CHANNEL_AVERAGE_16</code>	Average 16 samples for each conversion end callback.
<code>SDADC_CHANNEL_AVERAGE_32</code>	Average 32 samples for each conversion end callback.
<code>SDADC_CHANNEL_AVERAGE_64</code>	Average 64 samples for each conversion end callback.

◆ **sdadc\_channel\_inversion\_t**

enum <code>sdadc_channel_inversion_t</code>	
Per channel polarity, valid for negative-side single-ended input only.	
Enumerator	
<code>SDADC_CHANNEL_INVERSION_OFF</code>	Do not invert conversion result.
<code>SDADC_CHANNEL_INVERSION_ON</code>	Invert conversion result.

◆ **sdadc\_channel\_count\_formula\_t**

enum <code>sdadc_channel_count_formula_t</code>	
Select a formula to specify the number of conversions. The following symbols are used in the formulas:	
<ul style="list-style-type: none"> <li>• N: Number of conversions</li> <li>• n: <code>sdadc_channel_cfg_t::coefficient_n</code>, do not set to 0 if m is 0</li> <li>• m: <code>sdadc_channel_cfg_t::coefficient_m</code>, do not set to 0 if n is 0</li> </ul> Either m or n must be non-zero.	
Enumerator	
<code>SDADC_CHANNEL_COUNT_FORMULA_EXPONENTIAL</code>	$N = 32 * (2 ^ n - 1) + m * 2 ^ n.$
<code>SDADC_CHANNEL_COUNT_FORMULA_LINEAR</code>	$N = (32 * n) + m.$

◆ **sdadc\_calibration\_t**

enum <code>sdadc_calibration_t</code>	
Calibration mode.	
Enumerator	
<code>SDADC_CALIBRATION_INTERNAL_GAIN_OFFSET</code>	Use internal reference to calibrate offset and gain.
<code>SDADC_CALIBRATION_EXTERNAL_OFFSET</code>	Use external reference to calibrate offset.
<code>SDADC_CALIBRATION_EXTERNAL_GAIN</code>	Use external reference to calibrate gain.

**Function Documentation**



◆ **R\_SDADC\_Open()**

```
fsp_err_t R_SDADC_Open ( adc_ctrl_t * p_ctrl, adc_cfg_t const *const p_cfg )
```

Applies power to the SDADC and initializes the hardware based on the user configuration. As part of this initialization, the SDADC clock is configured and enabled. If an interrupt priority is non-zero, enables an interrupt which will call a callback to notify the user when a conversion, scan, or calibration is complete. [R\\_SDADC\\_Calibrate\(\)](#) must be called after this function before using the SDADC if any channels are used in differential mode. Implements [adc\\_api\\_t::open\(\)](#).

**Note**

*This function delays at least 2 ms as required by the SDADC power on procedure.*

**Return values**

FSP_SUCCESS	Configuration successful.
FSP_ERR_ASSERTION	An input pointer is NULL or an input parameter is invalid.
FSP_ERR_ALREADY_OPEN	Control block is already open.
FSP_ERR_IRQ_BSP_DISABLED	A required interrupt is disabled

◆ **R\_SDADC\_ScanCfg()**

```
fsp_err_t R_SDADC_ScanCfg ( adc_ctrl_t * p_ctrl, void const *const p_extend )
```

Configures the enabled channels of the ADC. Pass a pointer to [sdadc\\_scan\\_cfg\\_t](#) to p\_extend. Implements [adc\\_api\\_t::scanCfg\(\)](#).

**Return values**

FSP_SUCCESS	Information stored in p_adc_info.
FSP_ERR_ASSERTION	An input pointer is NULL or an input parameter is invalid.
FSP_ERR_NOT_OPEN	Instance control block is not open.

◆ **R\_SDADC\_InfoGet()**

```
fsp_err_t R_SDADC_InfoGet ( adc_ctrl_t* p_ctrl, adc_info_t* p_adc_info )
```

Returns the address of the lowest number configured channel, the total number of results to be read in order to read the results of all configured channels, the size of each result, and the ELC event enumerations. Implements `adc_api_t::infoGet()`.

**Return values**

FSP_SUCCESS	Information stored in p_adc_info.
FSP_ERR_ASSERTION	An input pointer was NULL.
FSP_ERR_NOT_OPEN	Instance control block is not open.

◆ **R\_SDADC\_ScanStart()**

```
fsp_err_t R_SDADC_ScanStart ( adc_ctrl_t* p_ctrl)
```

If the SDADC is configured for hardware triggers, enables hardware triggers. Otherwise, starts a scan. Implements `adc_api_t::scanStart()`.

**Return values**

FSP_SUCCESS	Scan started or hardware triggers enabled successfully.
FSP_ERR_ASSERTION	An input pointer was NULL.
FSP_ERR_NOT_OPEN	Instance control block is not open.
FSP_ERR_IN_USE	A conversion or calibration is in progress.

◆ **R\_SDADC\_ScanStop()**

```
fsp_err_t R_SDADC_ScanStop ( adc_ctrl_t* p_ctrl)
```

If the SDADC is configured for hardware triggers, disables hardware triggers. Otherwise, stops any in-progress scan started by software. Implements `adc_api_t::scanStop()`.

**Return values**

FSP_SUCCESS	Scan stopped or hardware triggers disabled successfully.
FSP_ERR_ASSERTION	An input pointer was NULL.
FSP_ERR_NOT_OPEN	Instance control block is not open.

◆ **R\_SDADC\_StatusGet()**

```
fsp_err_t R_SDADC_StatusGet ( adc_ctrl_t * p_ctrl, adc_status_t * p_status )
```

Returns the status of a scan started by software, including calibration scans. It is not possible to determine the status of a scan started by a hardware trigger. Implements `adc_api_t::scanStatusGet()`.

**Return values**

FSP_SUCCESS	No software scan or calibration is in progress.
FSP_ERR_ASSERTION	An input pointer was NULL.
FSP_ERR_NOT_OPEN	Instance control block is not open.

◆ **R\_SDADC\_Read()**

```
fsp_err_t R_SDADC_Read ( adc_ctrl_t * p_ctrl, adc_channel_t const reg_id, uint16_t *const p_data )
```

Reads the most recent conversion result from a channel. Truncates 24-bit results to the upper 16 bits. Implements `adc_api_t::read()`.

**Note**

*The result stored in p\_data is signed when the SDADC channel is configured in differential mode. Do not use this API if the conversion end interrupt (SDADC0\_ADI) is used to trigger the DTC unless the interrupt mode is set to TRANSFER\_IRQ\_EACH.*

**Return values**

FSP_SUCCESS	Conversion result in p_data.
FSP_ERR_ASSERTION	An input pointer was NULL or an input parameter was invalid.
FSP_ERR_NOT_OPEN	Instance control block is not open.

◆ **R\_SDADC\_Read32()**

```
fsp_err_t R_SDADC_Read32 ( adc_ctrl_t * p_ctrl, adc_channel_t const reg_id, uint32_t *const p_data )
```

Reads the most recent conversion result from a channel. Implements `adc_api_t::read32()`.

**Note**

*The result stored in p\_data is signed when the SDADC channel is configured in differential mode. When the SDADC is configured for 24-bit resolution and right alignment, the sign bit is bit 23, and the upper 8 bits are 0. When the SDADC is configured for 16-bit resolution and right alignment, the sign bit is bit 15, and the upper 16 bits are 0.*

*Do not use this API if the conversion end interrupt (SDADC0\_ADI) is used to trigger the DTC unless the interrupt mode is set to TRANSFER\_IRQ\_EACH.*

**Return values**

FSP_SUCCESS	Conversion result in p_data.
FSP_ERR_ASSERTION	An input pointer was NULL or an input parameter was invalid.
FSP_ERR_NOT_OPEN	Instance control block is not open.

◆ **R\_SDADC\_OffsetSet()**

```
fsp_err_t R_SDADC_OffsetSet ( adc_ctrl_t *const p_ctrl, adc_channel_t const reg_id, int32_t const offset )
```

Sets the offset. Offset is applied after stage 1 of the input channel. Offset can only be applied when the channel is configured for differential input. Implements `adc_api_t::offsetSet()`.

Note: The offset is cleared if `adc_api_t::calibrate()` is called. The offset can be re-applied if necessary after the the callback with event `ADC_EVENT_CALIBRATION_COMPLETE` is called.

**Parameters**

[in]	p_ctrl	See p_instance_ctrl in <code>adc_api_t::offsetSet()</code> .
[in]	reg_id	See reg_id in <code>adc_api_t::offsetSet()</code> .
[in]	offset	Must be between -15 and 15, offset (mV) = 10.9376 mV * offset_steps / stage 1 gain.

**Return values**

FSP_SUCCESS	Offset updated successfully.
FSP_ERR_ASSERTION	An input pointer was NULL or an input parameter was invalid.
FSP_ERR_IN_USE	A conversion or calibration is in progress.
FSP_ERR_NOT_OPEN	Instance control block is not open.

### ◆ R\_SDADC\_Calibrate()

`fsp_err_t R_SDADC_Calibrate ( adc_ctrl_t *const p_ctrl, void *const p_extend )`

Requires `sdadc_calibrate_args_t` passed to `p_extend`. Calibrates the specified channel. Calibration is not required or supported for single-ended mode. Calibration must be completed for differential mode before using the SDADC. A callback with the event `ADC_EVENT_CALIBRATION_COMPLETE` is called when calibration completes. Implements `adc_api_t::calibrate()`.

During external offset calibration, apply a differential voltage of 0 to `ANSDnP - ANSDnN`, where `n` is the input channel and `ANSDnP` is `OPAMP0` for channel 4 and `ANSDnN` is `OPAMP1` for channel 4. Complete external offset calibration before external gain calibration.

During external gain calibration apply a voltage between  $0.4 \text{ V} / \text{total\_gain}$  and  $0.8 \text{ V} / \text{total\_gain}$ . The differential voltage applied during calibration is corrected to a conversion result of `0x7FFFFFFF`, which is the maximum possible positive differential measurement.

This function clears the offset value. If offset is required after calibration, it must be reapplied after calibration is complete using `adc_api_t::offsetSet`.

#### Return values

<code>FSP_SUCCESS</code>	Calibration began successfully.
<code>FSP_ERR_ASSERTION</code>	An input pointer was NULL.
<code>FSP_ERR_IN_USE</code>	A conversion or calibration is in progress.
<code>FSP_ERR_NOT_OPEN</code>	Instance control block is not open.

### ◆ R\_SDADC\_Close()

`fsp_err_t R_SDADC_Close ( adc_ctrl_t * p_ctrl)`

Stops any scan in progress, disables interrupts, and powers down the SDADC peripheral. Implements `adc_api_t::close()`.

#### Note

*This function delays at least 3 us as required by the SDADC24 stop procedure.*

#### Return values

<code>FSP_SUCCESS</code>	Instance control block closed successfully.
<code>FSP_ERR_ASSERTION</code>	An input pointer was NULL.
<code>FSP_ERR_NOT_OPEN</code>	Instance control block is not open.

◆ **R\_SDADC\_VersionGet()**

```
fsp_err_t R_SDADC_VersionGet ( fsp_version_t *const p_version)
```

Gets the API and code version. Implements `adc_api_t::versionGet()`.

**Return values**

FSP_SUCCESS	Version information available in <code>p_version</code> .
FSP_ERR_ASSERTION	The parameter <code>p_version</code> is NULL.

**4.2.44 SD/MMC Host Interface (r\_sdhi)**

## Modules

**Functions**

```
fsp_err_t R_SDHI_Open (sdmmc_ctrl_t *const p_api_ctrl, sdmmc_cfg_t const *const p_cfg)
```

```
fsp_err_t R_SDHI_MediaInit (sdmmc_ctrl_t *const p_api_ctrl, sdmmc_device_t *const p_device)
```

```
fsp_err_t R_SDHI_Read (sdmmc_ctrl_t *const p_api_ctrl, uint8_t *const p_dest, uint32_t const start_sector, uint32_t const sector_count)
```

```
fsp_err_t R_SDHI_Write (sdmmc_ctrl_t *const p_api_ctrl, uint8_t const *const p_source, uint32_t const start_sector, uint32_t const sector_count)
```

```
fsp_err_t R_SDHI_Readlo (sdmmc_ctrl_t *const p_api_ctrl, uint8_t *const p_data, uint32_t const function, uint32_t const address)
```

```
fsp_err_t R_SDHI_Writelo (sdmmc_ctrl_t *const p_api_ctrl, uint8_t *const p_data, uint32_t const function, uint32_t const address, sdmmc_io_write_mode_t const read_after_write)
```

```
fsp_err_t R_SDHI_ReadloExt (sdmmc_ctrl_t *const p_api_ctrl, uint8_t *const p_dest, uint32_t const function, uint32_t const address, uint32_t *const count, sdmmc_io_transfer_mode_t transfer_mode, sdmmc_io_address_mode_t address_mode)
```

```
fsp_err_t R_SDHI_WriteloExt (sdmmc_ctrl_t *const p_api_ctrl, uint8_t const *const p_source, uint32_t const function, uint32_t const address, uint32_t const count, sdmmc_io_transfer_mode_t transfer_mode, sdmmc_io_address_mode_t address_mode)
```

```
fsp_err_t R_SDHI_IoIntEnable (sdmmc_ctrl_t *const p_api_ctrl, bool enable)
```

```
fsp_err_t R_SDHI_StatusGet (sdmmc_ctrl_t *const p_api_ctrl, sdmmc_status_t *const p_status)
```

```
fsp_err_t R_SDHI_Erase (sdmmc_ctrl_t *const p_api_ctrl, uint32_t const start_sector, uint32_t const sector_count)
```

```
fsp_err_t R_SDHI_CallbackSet (sdmmc_ctrl_t *const p_api_ctrl, void(*p_callback)(sdmmc_callback_args_t *), void const *const p_context, sdmmc_callback_args_t *const p_callback_memory)
```

```
fsp_err_t R_SDHI_Close (sdmmc_ctrl_t *const p_api_ctrl)
```

```
fsp_err_t R_SDHI_VersionGet (fsp_version_t *const p_version)
```

## Detailed Description

Driver for the SD/MMC Host Interface (SDHI) peripheral on RA MCUs. This module implements the [SD/MMC Interface](#).

## Overview

### Features

- Supports the following memory devices: SDSC (SD Standard Capacity), SDHC (SD High Capacity), SDXC (SD Extended Capacity) and eMMC (embedded Multi Media Card)
  - Supports reading, writing and erasing SD memory devices
  - Supports 1, 4 or 8-bit data bus (8-bit bus is supported for eMMC only)
  - Supports detection of device write protection (SD cards only)
  - Supports high speed mode
- Automatically configures the clock to the maximum clock rate supported by both host (MCU) and device
- Supports hardware acceleration using DMAC or DTC
- Supports callback notification when an operation completes or an error occurs

## Configuration

### Build Time Configurations for r\_sdhi

The following build time configurations are defined in fsp\_cfg/r\_sdhi\_cfg.h:

Configuration	Options	Default	Description
Parameter Checking Enable	<ul style="list-style-type: none"> <li>• Default (BSP)</li> <li>• Enabled</li> <li>• Disabled</li> </ul>	Default (BSP)	If selected code for parameter checking is included in the build.
Unaligned Access Support	<ul style="list-style-type: none"> <li>• Disabled</li> <li>• Enabled</li> </ul>	Enabled	If enabled, code for supporting buffers that are not aligned on a



4-byte boundary is included in the build. Only disable this if all buffers passed to the driver are 4-byte aligned.

SD Support	<ul style="list-style-type: none"> <li>• Disabled</li> <li>• Enabled</li> </ul>	Enabled	If selected code for SD card support is included in the build.
eMMC Support	<ul style="list-style-type: none"> <li>• Disabled</li> <li>• Enabled</li> </ul>	Disabled	If selected code for eMMC device support is included in the build.

### Configurations for Driver > Storage > SD/MMC Driver on r\_sdhi

This module can be added to the Stacks tab via New Stack > Driver > Storage > SD/MMC Driver on r\_sdhi. Non-secure callable guard functions can be generated for this module by right clicking the module in the RA Configuration tool and checking the "Non-secure Callable" box.

Configuration	Options	Default	Description
Name	Name must be a valid C symbol	g_sdmmc0	Module name.
Channel	Value must be a non-negative integer	0	Select the channel.
Bus Width	MCU Specific Options		Select the bus width.
Block Size	Value must be an integer between 1 and 512	512	Select the media block size. Must be 512 for SD cards or eMMC devices. Must be 1-512 for SDIO.
Card Detection	<ul style="list-style-type: none"> <li>• Not Used</li> <li>• CD Pin</li> </ul>	CD Pin	Select the card detection method.
Write Protection	<ul style="list-style-type: none"> <li>• Not Used</li> <li>• WP Pin</li> </ul>	WP Pin	Select whether or not to use the write protect pin. Select Not Used if the MCU or device does not have a write protect pin.
Callback	Name must be a valid C symbol	NULL	A user callback function can be provided. If this callback function is provided, it will be called from the interrupt service routine (ISR).
Access Interrupt Priority	MCU Specific Options		Select the access interrupt priority.

---

Card Interrupt Priority	MCU Specific Options	Select the card interrupt priority.
DTC Interrupt Priority	MCU Specific Options	Select the DTC interrupt priority.

### Interrupt Configurations:

The following interrupts are required to use the r\_sdhi module:

Using SD/MMC with DTC:

- Access Interrupt
- DTC Interrupt

Using SD/MMC with DMAC:

- Access Interrupt
- DMAC Interrupt (in DMAC instance)

The Card interrupt is optional and only available on MCU packages that have the SDnCD pin (n = channel number).

### Clock Configuration

The SDMMC MCU peripheral (SDHI) uses the PCLKA for its clock source. The SDMMC driver selects the optimal built-in divider based on the PCLKA frequency and the maximum clock rate allowed by the device obtained at media initialization.

### Pin Configuration

The SDMMC driver supports the following pins (n = channel number):

- SDnCLK
- SDnCMD
- SDnDAT0
- SDnDAT1
- SDnDAT2
- SDnDAT3
- SDnDAT4 (not available on all MCUs)
- SDnDAT5 (not available on all MCUs)
- SDnDAT6 (not available on all MCUs)
- SDnDAT7 (not available on all MCUs)
- SDnCD (not available on all MCUs)
- SDnWP

The drive capacity for each pin should be set to "Medium" or "High" for most hardware designs. This can be configured in the **Pins** tab of the RA Configuration editor by selecting the pin under Pin Selection -> Ports.

## Usage Notes

### Card Detection

When Card Detection is configured to "CD Pin" in the RA Configuration editor, card detection is

enabled during [R\\_SDHI\\_Open\(\)](#).

[R\\_SDHI\\_StatusGet\(\)](#) can be called to retrieve the current status of the card (including whether a card is present). If the Card Interrupt Priority is enabled, a callback is called when a card is inserted or removed.

If a card is removed and reinserted, [R\\_SDHI\\_MediaInit\(\)](#) must be called before reading from the card or writing to the card.

### DMA Request Interrupt Priority

When data transfers are not 4-byte aligned or not a multiple of 4 bytes, a software copy of the block size (up to 512 bytes) is done in the DMA Request interrupt. This blocks all other interrupts that are a lower or equal priority to the access interrupt until the software copy is complete.

### Timing Notes for R\_SDHI\_MediaInit

The [R\\_SDHI\\_MediaInit\(\)](#) API completes the entire device identification and configuration process. This involves several command-response cycles at a bus width of 1 bit and a bus speed of 400 kHz or less.

### Limitations

Developers should be aware of the following limitations when using the SDHI:

### Blocking Calls

The following functions block execution until the response is received for at least one command:

- [R\\_SDHI\\_MediaInit](#)
- [R\\_SDHI\\_Erase](#)

Once the function returns the status of the operation can be determined via [R\\_SDHI\\_StatusGet](#) or through receipt of a callback.

#### Note

*Due to the variability in clocking configurations it is recommended to determine blocking delays experimentally on the target system.*

### Data Alignment and Size

Data transfers should be 4-byte aligned and a multiple of 4 bytes in size whenever possible. This recommendation applies to the `read()`, `write()`, `readloExt()`, and `writeloExt()` APIs. When data transfers are 4-byte aligned and a multiple of 4-bytes, the `r_sdhi` driver is zero copy and takes full advantage of hardware acceleration by the DMAC or DTC. When data transfers are not 4-byte aligned or not a multiple of 4 bytes an extra CPU interrupt is required for each block transferred and a software copy is used to move data to the destination buffer.

## Examples

### Basic Example

This is a basic example of minimal use of the `r_sdhi` in an application.

```
uint8_t g_dest[SDHI_MAX_BLOCK_SIZE] BSP_ALIGN_VARIABLE(4);
uint8_t g_src[SDHI_MAX_BLOCK_SIZE] BSP_ALIGN_VARIABLE(4);
uint32_t g_transfer_complete = 0;
void r_sdhi_basic_example (void)
{
    /* Initialize g_src to known data */
    for (uint32_t i = 0; i < SDHI_MAX_BLOCK_SIZE; i++)
    {
        g_src[i] = (uint8_t) ('A' + (i % 26));
    }
    /* Open the SDHI driver. */
    fsp_err_t err = R_SDHI_Open(&g_sdmmc0_ctrl, &g_sdmmc0_cfg);
    handle_error(err);
    /* A device shall be ready to accept the first command within 1ms from detecting VDD
min. Reference section 6.4.1.1
    * "Power Up Time of Card" in the SD Physical Layer Simplified Specification Version
6.00. */
    R_BSP_SoftwareDelay(1U, BSP_DELAY_UNITS_MILLISECONDS);
    /* Initialize the SD card. This should not be done until the card is plugged in for
SD devices. */
    err = R_SDHI_MediaInit(&g_sdmmc0_ctrl, NULL);
    handle_error(err);
    err = R_SDHI_Write(&g_sdmmc0_ctrl, g_src, 3, 1);
    handle_error(err);
    while (!g_transfer_complete)
    {
        /* Wait for transfer. */
    }
    err = R_SDHI_Read(&g_sdmmc0_ctrl, g_dest, 3, 1);
    handle_error(err);
    while (!g_transfer_complete)
    {
        /* Wait for transfer. */
    }
}
```

```
}  
  
/* The callback is called when a transfer completes. */  
void r_sdhi_example_callback (sdmmc_callback_args_t * p_args)  
{  
    if (SDMMC_EVENT_TRANSFER_COMPLETE == p_args->event)  
    {  
        g_transfer_complete = 1;  
    }  
}
```

### Card Detection Example

This is an example of using SDHI when the card may not be plugged in. The card detection interrupt must be enabled to use this example.

```
bool g_card_inserted = false;  
void r_sdhi_card_detect_example (void)  
{  
    /* Open the SDHI driver. This enables the card detection interrupt. */  
    fsp_err_t err = R_SDHI_Open(&g_sdmmc0_ctrl, &g_sdmmc0_cfg);  
    /* Handle any errors. This function should be defined by the user. */  
    handle_error(err);  
    /* Check if card is inserted. */  
    sdmmc_status_t status;  
    err = R_SDHI_StatusGet(&g_sdmmc0_ctrl, &status);  
    handle_error(err);  
    if (!status.card_inserted)  
    {  
        while (!g_card_inserted)  
        {  
            /* Wait for a card insertion interrupt. */  
        }  
    }  
    /* A device shall be ready to accept the first command within 1ms from detecting VDD  
    min. Reference section 6.4.1.1
```

```
* "Power Up Time of Card" in the SD Physical Layer Simplified Specification Version
6.00. */
R_BSP_SoftwareDelay(1U, BSP_DELAY_UNITS_MILLISECONDS);
/* Initialize the SD card after card insertion is detected. */
err = R_SDHI_MediaInit(&g_sdmmc0_ctrl, NULL);
handle_error(err);
}
/* The callback is called when a card detection event occurs if the card detection
interrupt is enabled. */
void r_sdhi_card_detect_example_callback (sdmmc_callback_args_t * p_args)
{
    if (SDMMC_EVENT_CARD_INSERTED == p_args->event)
    {
        g_card_inserted = true;
    }
    if (SDMMC_EVENT_CARD_REMOVED == p_args->event)
    {
        g_card_inserted = false;
    }
}
```

## Function Documentation

---

◆ **R\_SDHI\_Open()**

```
fsp_err_t R_SDHI_Open ( sdmmc_ctrl_t *const p_api_ctrl, sdmmc_cfg_t const *const p_cfg )
```

Opens the driver. Resets SDHI, and enables card detection interrupts if card detection is enabled. [R\\_SDHI\\_MediaInit](#) must be called after this function before any other functions can be used.

Implements [sdmmc\\_api\\_t::open\(\)](#).

Example:

```
/* Open the SDHI driver. */
fsp_err_t err = R_SDHI_Open(&g_sdmmc0_ctrl, &g_sdmmc0_cfg);
```

**Return values**

FSP_SUCCESS	Module is now open.
FSP_ERR_ASSERTION	Null Pointer or block size is not in the valid range of 1-512. Block size must be 512 bytes for SD cards and eMMC devices. It is configurable for SDIO only.
FSP_ERR_ALREADY_OPEN	Driver has already been opened with this instance of the control structure.
FSP_ERR_IRQ_BSP_DISABLED	Access interrupt is not enabled.
FSP_ERR_IP_CHANNEL_NOT_PRESENT	Requested channel does not exist on this MCU.

### ◆ R\_SDHI\_MediaInit()

```
fsp_err_t R_SDHI_MediaInit ( sdmmc_ctrl_t *const p_api_ctrl, sdmmc_device_t *const p_device )
```

Initializes the SDHI hardware and completes identification and configuration for the SD or eMMC device. This procedure requires several sequential commands. This function blocks until all identification and configuration commands are complete.

Implements `sdmmc_api_t::mediaInit()`.

Example:

```
/* A device shall be ready to accept the first command within 1ms from detecting VDD
min. Reference section 6.4.1.1
 * "Power Up Time of Card" in the SD Physical Layer Simplified Specification Version
6.00. */
R_BSP_SoftwareDelay(1U, BSP_DELAY_UNITS_MILLISECONDS);
/* Initialize the SD card. This should not be done until the card is plugged in for
SD devices. */
err = R_SDHI_MediaInit(&g_sdmmc0_ctrl, NULL);
```

#### Return values

FSP_SUCCESS	Module is now ready for read/write access.
FSP_ERR_ASSERTION	Null Pointer or block size is not in the valid range of 1-512. Block size must be 512 bytes for SD cards and eMMC devices. It is configurable for SDIO only.
FSP_ERR_NOT_OPEN	Driver has not been initialized.
FSP_ERR_CARD_INIT_FAILED	Device was not identified as an SD card, eMMC device, or SDIO card.
FSP_ERR_RESPONSE	Device did not respond or responded with an error.
FSP_ERR_DEVICE_BUSY	Device is holding DAT0 low (device is busy) or another operation is ongoing.



### ◆ R\_SDHI\_Read()

```
fsp_err_t R_SDHI_Read ( sdmmc_ctrl_t *const p_api_ctrl, uint8_t *const p_dest, uint32_t const
start_sector, uint32_t const sector_count )
```

Reads data from an SD or eMMC device. Up to 0x10000 sectors can be read at a time. Implements `sdmmc_api_t::read()`.

A callback with the event `SDMMC_EVENT_TRANSFER_COMPLETE` is called when the read data is available.

Example:

```
err = R_SDHI_Read(&g_sdmmc0_ctrl, g_dest, 3, 1);
```

#### Return values

FSP_SUCCESS	Data read successfully.
FSP_ERR_ASSERTION	NULL pointer.
FSP_ERR_NOT_OPEN	Driver has not been initialized.
FSP_ERR_CARD_NOT_INITIALIZED	Card was unplugged.
FSP_ERR_DEVICE_BUSY	Driver is busy with a previous operation.

### ◆ R\_SDHI\_Write()

```
fsp_err_t R_SDHI_Write ( sdmmc_ctrl_t *const p_api_ctrl, uint8_t const *const p_source, uint32_t
const start_sector, uint32_t const sector_count )
```

Writes data to an SD or eMMC device. Up to 0x10000 sectors can be written at a time. Implements `sdmmc_api_t::write()`.

A callback with the event `SDMMC_EVENT_TRANSFER_COMPLETE` is called when the all data has been written and the device is no longer holding `DAT0` low to indicate it is busy.

Example:

```
err = R_SDHI_Write(&g_sdmmc0_ctrl, g_src, 3, 1);
```

#### Return values

FSP_SUCCESS	Card write finished successfully.
FSP_ERR_ASSERTION	Handle or Source address is NULL.
FSP_ERR_NOT_OPEN	Driver has not been initialized.
FSP_ERR_CARD_NOT_INITIALIZED	Card was unplugged.
FSP_ERR_DEVICE_BUSY	Driver is busy with a previous operation.
FSP_ERR_CARD_WRITE_PROTECTED	SD card is Write Protected.
FSP_ERR_WRITE_FAILED	Write operation failed.

◆ **R\_SDHI\_Readlo()**

```
fsp_err_t R_SDHI_Readlo ( sdmmc_ctrl_t *const p_api_ctrl, uint8_t *const p_data, uint32_t const
function, uint32_t const address )
```

The Read function reads a one byte register from an SDIO card. Implements `sdmmc_api_t::readlo()`.

This function blocks until the command is sent and the response is received. `p_data` contains the register value read when this function returns.

**Return values**

FSP_SUCCESS	Data read successfully.
FSP_ERR_ASSERTION	NULL pointer.
FSP_ERR_NOT_OPEN	Driver has not been initialized.
FSP_ERR_CARD_NOT_INITIALIZED	Card was unplugged.
FSP_ERR_UNSUPPORTED	SDIO support disabled in SDHI_CFG_SDIO_SUPPORT_ENABLE.
FSP_ERR_RESPONSE	Device did not respond or responded with an error.
FSP_ERR_DEVICE_BUSY	Device is holding DAT0 low (device is busy) or another operation is ongoing.

◆ **R\_SDHI\_Writelo()**

```
fsp_err_t R_SDHI_Writelo ( sdmmc_ctrl_t *const p_api_ctrl, uint8_t *const p_data, uint32_t const
function, uint32_t const address, sdmmc_io_write_mode_t const read_after_write )
```

Writes a one byte register to an SDIO card. Implements `sdmmc_api_t::writelo()`.

This function blocks until the command is sent and the response is received. The register has been written when this function returns. If `read_after_write` is true, `p_data` contains the register value read when this function returns.

**Return values**

FSP_SUCCESS	Card write finished successfully.
FSP_ERR_ASSERTION	Handle or Source address is NULL.
FSP_ERR_NOT_OPEN	Driver has not been initialized.
FSP_ERR_CARD_NOT_INITIALIZED	Card was unplugged.
FSP_ERR_WRITE_FAILED	Write operation failed.
FSP_ERR_UNSUPPORTED	SDIO support disabled in SDHI_CFG_SDIO_SUPPORT_ENABLE.
FSP_ERR_RESPONSE	Device did not respond or responded with an error.
FSP_ERR_DEVICE_BUSY	Device is holding DAT0 low (device is busy) or another operation is ongoing.

◆ **R\_SDHI\_ReadloExt()**

```
fsp_err_t R_SDHI_ReadloExt ( sdmmc_ctrl_t *const p_api_ctrl, uint8_t *const p_dest, uint32_t const
function, uint32_t const address, uint32_t *const count, sdmmc_io_transfer_mode_t
transfer_mode, sdmmc_io_address_mode_t address_mode )
```

Reads data from an SDIO card function. Implements `sdmmc_api_t::readloExt()`.

This function blocks until the command is sent and the response is received. A callback with the event `SDMMC_EVENT_TRANSFER_COMPLETE` is called when the read data is available.

**Return values**

FSP_SUCCESS	Data read successfully.
FSP_ERR_ASSERTION	NULL pointer, or count is not in the valid range of 1-512 for byte mode or 1-511 for block mode.
FSP_ERR_NOT_OPEN	Driver has not been initialized.
FSP_ERR_CARD_NOT_INITIALIZED	Card was unplugged.
FSP_ERR_DEVICE_BUSY	Driver is busy with a previous operation.
FSP_ERR_UNSUPPORTED	SDIO support disabled in <code>SDHI_CFG_SDIO_SUPPORT_ENABLE</code> .

◆ **R\_SDHI\_WritelExt()**

```
fsp_err_t R_SDHI_WritelExt ( sdmmc_ctrl_t *const p_api_ctrl, uint8_t const *const p_source,
uint32_t const function, uint32_t const address, uint32_t const count, sdmmc_io_transfer_mode_t
transfer_mode, sdmmc_io_address_mode_t address_mode )
```

Writes data to an SDIO card function. Implements `sdmmc_api_t::writelExt()`.

This function blocks until the command is sent and the response is received. A callback with the event `SDMMC_EVENT_TRANSFER_COMPLETE` is called when the all data has been written.

**Return values**

FSP_SUCCESS	Card write finished successfully.
FSP_ERR_ASSERTION	NULL pointer, or count is not in the valid range of 1-512 for byte mode or 1-511 for block mode.
FSP_ERR_NOT_OPEN	Driver has not been initialized.
FSP_ERR_CARD_NOT_INITIALIZED	Card was unplugged.
FSP_ERR_DEVICE_BUSY	Driver is busy with a previous operation.
FSP_ERR_WRITE_FAILED	Write operation failed.
FSP_ERR_UNSUPPORTED	SDIO support disabled in <code>SDHI_CFG_SDIO_SUPPORT_ENABLE</code> .

◆ **R\_SDHI\_IoIntEnable()**

```
fsp_err_t R_SDHI_IoIntEnable ( sdmmc_ctrl_t *const p_api_ctrl, bool enable )
```

Enables or disables the SDIO Interrupt. Implements `sdmmc_api_t::IoIntEnable()`.

**Return values**

FSP_SUCCESS	Card enabled or disabled SDIO interrupts successfully.
FSP_ERR_NOT_OPEN	Driver has not been initialized.
FSP_ERR_ASSERTION	NULL pointer.
FSP_ERR_DEVICE_BUSY	Driver is busy with a previous operation.
FSP_ERR_UNSUPPORTED	SDIO support disabled in <code>SDHI_CFG_SDIO_SUPPORT_ENABLE</code> .

◆ **R\_SDHI\_StatusGet()**

```
fsp_err_t R_SDHI_StatusGet ( sdmmc_ctrl_t *const p_api_ctrl, sdmmc_status_t *const p_status )
```

Provides driver status. Implements `sdmmc_api_t::statusGet()`.

**Return values**

FSP_SUCCESS	Status stored in p_status.
FSP_ERR_ASSERTION	NULL pointer.
FSP_ERR_NOT_OPEN	Driver has not been initialized.

◆ **R\_SDHI\_Erase()**

```
fsp_err_t R_SDHI_Erase ( sdmmc_ctrl_t *const p_api_ctrl, uint32_t const start_sector, uint32_t const sector_count )
```

Erases sectors of an SD card or eMMC device. Implements `sdmmc_api_t::erase()`.

This function blocks until the erase command is sent. Poll the status to determine when erase is complete.

**Return values**

FSP_SUCCESS	Erase operation requested.
FSP_ERR_ASSERTION	A required pointer is NULL or an argument is invalid.
FSP_ERR_NOT_OPEN	Driver has not been initialized.
FSP_ERR_CARD_NOT_INITIALIZED	Card was unplugged.
FSP_ERR_CARD_WRITE_PROTECTED	SD card is Write Protected.
FSP_ERR_RESPONSE	Device did not respond or responded with an error.
FSP_ERR_DEVICE_BUSY	Device is holding DAT0 low (device is busy) or another operation is ongoing.

◆ **R\_SDHI\_CallbackSet()**

```
fsp_err_t R_SDHI_CallbackSet ( sdmmc_ctrl_t *const p_api_ctrl, void(*) (sdmmc_callback_args_t *)
p_callback, void const *const p_context, sdmmc_callback_args_t *const p_callback_memory )
```

Updates the user callback with the option to provide memory for the callback argument structure. Implements `sdmmc_api_t::callbackSet`.

**Return values**

FSP_SUCCESS	Callback updated successfully.
FSP_ERR_ASSERTION	A required pointer is NULL.
FSP_ERR_NOT_OPEN	The control block has not been opened.
FSP_ERR_NO_CALLBACK_MEMORY	<code>p_callback</code> is non-secure and <code>p_callback_memory</code> is either secure or NULL.

◆ **R\_SDHI\_Close()**

```
fsp_err_t R_SDHI_Close ( sdmmc_ctrl_t *const p_api_ctrl)
```

Closes an open SD/MMC device. Implements `sdmmc_api_t::close()`.

**Return values**

FSP_SUCCESS	Successful close.
FSP_ERR_ASSERTION	The parameter <code>p_ctrl</code> is NULL.
FSP_ERR_NOT_OPEN	Driver has not been initialized.

◆ **R\_SDHI\_VersionGet()**

```
fsp_err_t R_SDHI_VersionGet ( fsp_version_t *const p_version)
```

Returns the version of the firmware and API. Implements `sdmmc_api_t::versionGet()`.

**Return values**

FSP_SUCCESS	Function executed successfully.
FSP_ERR_ASSERTION	Null Pointer.

**4.2.45 Segment LCD Controller (r\_slcdc)**

## Modules

## Functions

fsp_err_t	R_SLCDC_Open (slcdc_ctrl_t *const p_ctrl, slcdc_cfg_t const *const p_cfg)
fsp_err_t	R_SLCDC_Write (slcdc_ctrl_t *const p_ctrl, uint8_t const start_segment, uint8_t const *p_data, uint8_t const segment_count)
fsp_err_t	R_SLCDC_Modify (slcdc_ctrl_t *const p_ctrl, uint8_t const segment_number, uint8_t const data_mask, uint8_t const data)
fsp_err_t	R_SLCDC_Start (slcdc_ctrl_t *const p_ctrl)
fsp_err_t	R_SLCDC_Stop (slcdc_ctrl_t *const p_ctrl)
fsp_err_t	R_SLCDC_SetContrast (slcdc_ctrl_t *const p_ctrl, slcdc_contrast_t const contrast)
fsp_err_t	R_SLCDC_SetDisplayArea (slcdc_ctrl_t *const p_ctrl, slcdc_display_area_t const display_area)
fsp_err_t	R_SLCDC_Close (slcdc_ctrl_t *const p_ctrl)
fsp_err_t	R_SLCDC_VersionGet (fsp_version_t *p_version)

## Detailed Description

Driver for the SLCDC peripheral on RA MCUs. This module implements the [SLCDC Interface](#).

## Overview

The segment LCD controller (SLCDC) utilizes two to four reference voltages to provide AC signals for driving traditional segment LCD panels. Depending on the LCD and MCU package, up to 272 segments can be driven. A built-in link to the RTC allows for up to 152 segments to switch between two patterns at regular intervals. An on-chip boost driver can be used to provide configurable reference voltages up to 5.25V allowing for simple contrast adjustment.

## Features

The SLCDC module can perform the following functions:

- Initialize, start and stop the SLCDC
- Set and modify the output pattern
- Blink between two patterns based on a periodic RTC interrupt signal
- Adjust display contrast (only when using internal voltage boosting)

## Configuration



## Build Time Configurations for r\_slcdc

The following build time configurations are defined in fsp\_cfg/r\_slcdc\_cfg.h:

Configuration	Options	Default	Description
Parameter Checking	<ul style="list-style-type: none"> <li>• Default (BSP)</li> <li>• Enabled</li> <li>• Disabled</li> </ul>	Default (BSP)	If selected code for parameter checking is included in the build.

## Configurations for Driver > Graphics > Segment LCD Driver on r\_slcdc

This module can be added to the Stacks tab via New Stack > Driver > Graphics > Segment LCD Driver on r\_slcdc.

Configuration	Options	Default	Description
General > Name	Name must be a valid C symbol	g_slcdc0	Module Name
Clock > Source	<ul style="list-style-type: none"> <li>• LOCO</li> <li>• SOSC</li> <li>• MOSC</li> <li>• HOCO</li> </ul>	HOCO	Select the clock source.
Clock > Divisor	Refer to the RA Configuration tool for available options.	(HOCO/MOSC) 16384	Select the clock divisor.
Output > Bias method	<ul style="list-style-type: none"> <li>• 1/2 bias</li> <li>• 1/3 bias</li> <li>• 1/4 bias</li> </ul>	1/2 bias	Select the bias method. This determines the number of voltage levels used to create the waveforms.
Output > Timeslice	<ul style="list-style-type: none"> <li>• Static</li> <li>• 2-slice</li> <li>• 3-slice</li> <li>• 4-slice</li> <li>• 8-slice</li> </ul>	Static	Select the LCD time slice. The number of slices should match the number of common (COM) pins for your LCD panel.
Output > Waveform	<ul style="list-style-type: none"> <li>• Waveform A</li> <li>• Waveform B</li> </ul>	Waveform A	Select the LCD waveform.
Output > Drive method	<ul style="list-style-type: none"> <li>• External resistance division</li> <li>• Internal voltage boosting</li> <li>• Capacitor split</li> </ul>	External resistance division	Select the LCD drive method.
Output > Default contrast	Refer to the RA Configuration tool for available options.	0	Select the default contrast level.

## Valid Configurations

Though there are many setting combinations only a limited subset are supported by the SLCDC peripheral hardware:

Waveform	Slices	Bias	External Resistance	Internal Boost	Capacitor Split
A	8	1/4	Available	Available	—
A	4	1/3	Available	Available	Available
A	3	1/3	Available	Available	Available
A	3	1/2	Available	—	—
A	2	1/2	Available	—	—
A	Static	—	Available	—	—
B	8	1/4	Available	Available	Available
B	4	1/3	Available	Available	—

### Clock Configuration

The SLCDC clock can be sourced from the main clock (MOSC), sub-clock (SOSC), HOCO or LOCO. Dividers of 4 to 1024 are available for SOSC/LOCO and 256 to 524288 for MOSC/HOCO. It is recommended to adjust the divisor such that the resulting clock provides a frame frequency of 32-128 Hz.

#### Note

*Make sure your desired source clock is enabled and running before starting SLCDC output.  
Do not set the segment LCD clock over 512 Hz when using internal boost or capacitor split modes.*

### Pin Configuration

This module controls a variety of pins necessary for segment LCD voltage generation and signal output:

Pin Name	Function	Notes
SEGn	Segment data output	Connect these signals to the segment pins of the LCD.
COMn	Common signal output	Connect these signals to the common pins of the LCD.
VLn	Voltage reference	These pins should be connected to passive components based on the selected drive method (see section 45.7 "Supplying LCD Drive Voltages VL1, VL2, VL3, and VL4" in the RA4M1 User's Manual (R01UH0887EJ0100)).
CAPH, CAPL	Drive voltage generator capacitor	Connect a nonpolar 0.47uF capacitor across these pins when using internal boost or capacitor split modes. This pin

is not needed when using resistance division.

## Interrupt Configuration

The SLCDC provides no interrupt signals.

### Note

*Blinking output timing is driven directly from the RTC periodic interrupt. Once the interrupt is enabled setting the display to SLCDC\_DISP\_BLINK will swap between A- and B-pattern each time it occurs. The ELC is not required for this functionality.*

## Usage Notes

### Limitations

Developers should be aware of the following limitations when using the SLCDC:

- Different packages provide different numbers of segment pins. Check the User's Manual for your device to confirm availability and mapping of segment signals.
- When using internal boost mode a delay of 5ms is required between calling R\_SLCDC\_Open and R\_SLCDC\_Start to allow the boost circuit to charge.
- When using the internal boost or capacitor split method do not set the segment LCD clock higher than 512 Hz.

## Examples

### Basic Example

Below is a basic example of minimal use of the SLCDC in an application. The SLCDC driver is initialized, output is started and a pattern is written to the segment registers.

```
void slcdc_init (void)
{
    fsp_err_t err;

    /* Open SLCDC driver */
    err = R_SLCDC_Open(&g_slcdc_ctrl, &g_slcdc_cfg);

    /* Handle any errors. This function should be defined by the user. */
    handle_error(err);

    /* When using internal boost mode this delay is required to allow the boost circuit
to charge. See RA4M1 User's
    * Manual (R01UH0887EJ0100) 8.2.18 "Segment LCD Source Clock Control Register
(SLCDSCKCR)" for details. */
    R_BSP_SoftwareDelay(5, BSP_DELAY_UNITS_MILLISECONDS);

    /* Start SLCDC output */
    err = R_SLCDC_Start(&g_slcdc_ctrl);
}
```

```
    handle_error(err);
/* Write pattern to display */
    err = R_SLCDC_Write(&g_slcdc_ctrl, 0, segment_data, NUM_SEGMENTS);
    handle_error(err);
}
```

#### Note

While the SLCDC is running, pattern data is constantly being output. No latching or buffering is required when writing or reading segment data.

## Blinking Output

This example demonstrates how to set up blinking output using the RTC periodic interrupt. In this example it is assumed that the SLCDC has already been started.

```
void slcdc_blink (void)
{
    fsp_err_t err;
/* Open RTC and set time/date */
    err = R_RTC_Open(&r_rtc_ctrl, &r_rtc_cfg);
/* Handle any errors. This function should be defined by the user. */
    handle_error(err);
    err = R_RTC_CalendarTimeSet(&r_rtc_ctrl, &g_rtc_time);
    handle_error(err);
/* Set RTC periodic interrupt to 2 Hz (display blink cycle will be 1 Hz) */
    err = R_RTC_PeriodicIrqRateSet(&r_rtc_ctrl,
RTC_PERIODIC_IRQ_SELECT_1_DIV_BY_2_SECOND);
    handle_error(err);
/* Set display to blink */
    err = R_SLCDC_SetDisplayArea(&g_slcdc_ctrl, SLCDC_DISP_BLINK);
    handle_error(err);
/* Display will now continuously blink */
}
```

## Data Structures

```
struct slcdc_instance_ctrl_t
```

## Data Structure Documentation

### ◆ slcdc\_instance\_ctrl\_t

```
struct slcdc_instance_ctrl_t
```

SLCDC control block. DO NOT INITIALIZE. Initialization occurs when `slcdc_api_t::open` is called

## Function Documentation

### ◆ R\_SLCDC\_Open()

```
fsp_err_t R_SLCDC_Open ( slcdc_ctrl_t *const p_ctrl, slcdc_cfg_t const *const p_cfg )
```

Opens the SLCDC driver. Implements `slcdc_api_t::open`.

#### Return values

FSP_SUCCESS	Device was opened successfully.
FSP_ERR_ASSERTION	Pointer to the control block or the configuration structure is NULL.
FSP_ERR_ALREADY_OPEN	Module is already open.
FSP_ERR_UNSUPPORTED	Invalid display mode.

### ◆ R\_SLCDC\_Write()

```
fsp_err_t R_SLCDC_Write ( slcdc_ctrl_t *const p_ctrl, uint8_t const start_segment, uint8_t const *p_data, uint8_t const segment_count )
```

Writes a sequence of display data to the segment data registers. Implements `slcdc_api_t::write`.

#### Return values

FSP_SUCCESS	Data was written successfully.
FSP_ERR_ASSERTION	Pointer to the control block or data is NULL.
FSP_ERR_INVALID_ARGUMENT	Segment index is (or will be) out of range.
FSP_ERR_NOT_OPEN	Device is not opened or initialized.

◆ **R\_SLCDC\_Modify()**

```
fsp_err_t R_SLCDC_Modify ( slcdc_ctrl_t *const p_ctrl, uint8_t const segment, uint8_t const data,
uint8_t const data_mask )
```

Modifies a single segment register based on a mask and the desired data. Implements `slcdc_api_t::modify`.

**Return values**

FSP_SUCCESS	Device was opened successfully.
FSP_ERR_ASSERTION	Pointer to the control block structure is NULL.
FSP_ERR_INVALID_ARGUMENT	Invalid parameter in the argument.
FSP_ERR_NOT_OPEN	Device is not opened or initialized

◆ **R\_SLCDC\_Start()**

```
fsp_err_t R_SLCDC_Start ( slcdc_ctrl_t *const p_ctrl)
```

Starts output of LCD signals. Implements `slcdc_api_t::start`.

**Return values**

FSP_SUCCESS	Device was opened successfully.
FSP_ERR_ASSERTION	Pointer to the control block structure is NULL.
FSP_ERR_NOT_OPEN	Device is not opened or initialized

◆ **R\_SLCDC\_Stop()**

```
fsp_err_t R_SLCDC_Stop ( slcdc_ctrl_t *const p_ctrl)
```

Stops output of LCD signals. Implements `slcdc_api_t::stop`.

**Return values**

FSP_SUCCESS	Device was opened successfully.
FSP_ERR_ASSERTION	Pointer to the control block structure is NULL.
FSP_ERR_NOT_OPEN	Device is not opened or initialized

◆ **R\_SLCDC\_SetContrast()**

```
fsp_err_t R_SLCDC_SetContrast ( slcdc_ctrl_t *const p_ctrl, slcdc_contrast_t const contrast )
```

Sets contrast to the specified level. Implements `slcdc_api_t::setContrast`.

**Note**

*Contrast can be adjusted when the SLCDC is operating in internal boost mode only. The range of values is 0-5 when 1/4 bias setting is used and 0-15 otherwise. See RA4M1 User's Manual (R01UH0887EJ0100) section 45.2.4 "LCD Boost Level Control Register (VLCD)" for voltage levels at each setting.*

**Return values**

FSP_SUCCESS	Device was opened successfully.
FSP_ERR_ASSERTION	Pointer to the control block structure is NULL.
FSP_ERR_NOT_OPEN	Device is not opened or initialized
FSP_ERR_UNSUPPORTED	Unsupported operation

◆ **R\_SLCDC\_SetDisplayArea()**

```
fsp_err_t R_SLCDC_SetDisplayArea ( slcdc_ctrl_t *const p_ctrl, slcdc_display_area_t const display_area )
```

Sets output to Waveform A, Waveform B or blinking output. Implements `slcdc_api_t::setDisplayArea`.

**Return values**

FSP_SUCCESS	Device was opened successfully.
FSP_ERR_ASSERTION	Pointer to the control block structure is NULL.
FSP_ERR_UNSUPPORTED	Pattern selection has no effect in 8-time-slice mode.
FSP_ERR_NOT_OPEN	Device is not opened or initialized.

◆ **R\_SLCDC\_Close()**

```
fsp_err_t R_SLCDC_Close ( slcdc_ctrl_t *const p_ctrl)
```

Closes the SLCDC driver. Implements `slcdc_api_t::close`.

**Return values**

FSP_SUCCESS	Device was closed successfully.
FSP_ERR_ASSERTION	Pointer to the control block structure is NULL.
FSP_ERR_NOT_OPEN	Device is not opened or initialized

◆ **R\_SLCDC\_VersionGet()**

```
fsp_err_t R_SLCDC_VersionGet ( fsp_version_t *const p_version)
```

Retrieve the API version number. Implements `slcdc_api_t::versionGet`.

**Return values**

FSP_SUCCESS	Successful return.
FSP_ERR_ASSERTION	p_version is NULL.

**4.2.46 Serial Peripheral Interface (r\_spi)**

## Modules

**Functions**

```
fsp_err_t R_SPI_Open (spi_ctrl_t *p_api_ctrl, spi_cfg_t const *const p_cfg)
```

```
fsp_err_t R_SPI_Read (spi_ctrl_t *const p_api_ctrl, void *p_dest, uint32_t const length, spi_bit_width_t const bit_width)
```

```
fsp_err_t R_SPI_Write (spi_ctrl_t *const p_api_ctrl, void const *p_src, uint32_t const length, spi_bit_width_t const bit_width)
```

```
fsp_err_t R_SPI_WriteRead (spi_ctrl_t *const p_api_ctrl, void const *p_src, void *p_dest, uint32_t const length, spi_bit_width_t const bit_width)
```

```
fsp_err_t R_SPI_Close (spi_ctrl_t *const p_api_ctrl)
```



```
fsp_err_t R_SPI_VersionGet (fsp_version_t *p_version)
```

```
fsp_err_t R_SPI_CalculateBitrate (uint32_t bitrate, rspck_div_setting_t
*spck_div)
```

```
fsp_err_t R_SPI_CallbackSet (spi_ctrl_t *const p_api_ctrl,
void(*p_callback)(spi_callback_args_t *), void const *const p_context,
spi_callback_args_t *const p_callback_memory)
```

## Detailed Description

Driver for the SPI peripheral on RA MCUs. This module implements the [SPI Interface](#).

## Overview

### Features

- Standard SPI Modes
  - Master or Slave Mode
  - Clock Polarity (CPOL)
    - CPOL=0 SCLK is low when idle
    - CPOL=1 SCLK is high when idle
  - Clock Phase (CPHA)
    - CPHA=0 Data Sampled on the even edge of SCLK (Master Mode Only)
    - CPHA=1 Data Sampled on the odd edge of SCLK
  - MSB/LSB first
  - 8-Bit, 16-Bit, 32-Bit data frames
    - Hardware endian swap in 16-Bit and 32-Bit mode
  - 3-Wire (clock synchronous) or 4-Wire (SPI) Mode
- Configurable bitrate
- Supports Full Duplex or Transmit Only Mode
- DTC Support
- Callback Events
  - Transfer Complete
  - RX Overflow Error (The SPI shift register is copied to the data register before previous data was read)
  - TX Underrun Error (No data to load into shift register for transmitting)
  - Parity Error (When parity is enabled and a parity error is detected)

## Configuration

### Build Time Configurations for r\_spi

The following build time configurations are defined in fsp\_cfg/r\_spi\_cfg.h:

Configuration	Options	Default	Description
Parameter Checking	<ul style="list-style-type: none"> <li>• Default (BSP)</li> <li>• Enabled</li> <li>• Disabled</li> </ul>	Default (BSP)	If selected code for parameter checking is included in the build.

Enable Support for using DTC	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Enabled	If enabled, DTC instances will be included in the build for both transmission and reception.
Enable Transmitting from RXI Interrupt	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Disabled	If enabled, all operations will be handled from the RX (receive) interrupt. This setting only provides a performance boost when DTC is not used. In addition, Transmit Only mode is not supported when this configuration is enabled.

### Configurations for Driver > Connectivity > SPI Driver on r\_spi

This module can be added to the Stacks tab via New Stack > Driver > Connectivity > SPI Driver on r\_spi. Non-secure callable guard functions can be generated for this module by right clicking the module in the RA Configuration tool and checking the "Non-secure Callable" box.

Configuration	Options	Default	Description
Name	Name must be a valid C symbol	g_spi0	Module name.
Channel	Select channel 0 or channel 1	0	Select the SPI channel.
Receive Interrupt Priority	MCU Specific Options		Select the interrupt priority for all SPI interrupts.
Transmit Buffer Empty Interrupt Priority	MCU Specific Options		Select the interrupt priority for all SPI interrupts.
Transfer Complete Interrupt Priority	MCU Specific Options		Select the interrupt priority for all SPI interrupts.
Error Interrupt Priority	MCU Specific Options		Select the interrupt priority for all SPI interrupts.
Operating Mode	<ul style="list-style-type: none"> <li>• Master</li> <li>• Slave</li> </ul>	Master	Select the SPI operating mode.
Clock Phase	<ul style="list-style-type: none"> <li>• Data sampling on odd edge, data variation on even edge</li> <li>• Data sampling on even edge,</li> </ul>	Data sampling on odd edge, data variation on even edge	Select the clock edge to sample data.

		data variation on odd edge		
Clock Polarity	<ul style="list-style-type: none"> <li>• Low when idle</li> <li>• High when idle</li> </ul>	Low when idle		Select clock level when idle.
Mode Fault Error	<ul style="list-style-type: none"> <li>• Enable</li> <li>• Disable</li> </ul>	Disable		Detect master/slave mode conflicts.
Bit Order	<ul style="list-style-type: none"> <li>• MSB First</li> <li>• LSB First</li> </ul>	MSB First		Select the data bit order.
Callback	Name must be a valid C symbol	spi_callback		A user callback function can be provided. If this callback function is provided, it will be called from the interrupt service routine (ISR).
SPI Mode	<ul style="list-style-type: none"> <li>• SPI Operation</li> <li>• Clock Synchronous Operation</li> </ul>	Clock Synchronous Operation		Select the clock sync mode.
Full or Transmit Only Mode	<ul style="list-style-type: none"> <li>• Full Duplex</li> <li>• Transmit Only</li> </ul>	Full Duplex		Select Full Duplex or Transmit Only Mode.
Slave Select Polarity	<ul style="list-style-type: none"> <li>• Active Low</li> <li>• Active High</li> </ul>	Active Low		Select the slave select active level.
Select SSL(Slave Select)	<ul style="list-style-type: none"> <li>• SSL0</li> <li>• SSL1</li> <li>• SSL2</li> <li>• SSL3</li> </ul>	SSL0		Select which slave to use.
MOSI Idle State	<ul style="list-style-type: none"> <li>• MOSI Idle Value Fixing Disable</li> <li>• MOSI Idle Value Fixing Low</li> <li>• MOSI Idle Value Fixing High</li> </ul>	MOSI Idle Value Fixing Disable		Select the MOSI idle level if MOSI idle is enabled.
Parity Mode	<ul style="list-style-type: none"> <li>• Disabled</li> <li>• Odd</li> <li>• Even</li> </ul>	Disabled		Select the parity mode if parity is enabled.
Byte Swapping	<ul style="list-style-type: none"> <li>• Disable</li> <li>• Enable</li> </ul>	Disable		Select the byte swap mode for 16/32-Bit Data Frames.
Bitrate	Value must be an integer greater than 0	16000000		Enter the desired bitrate, change the bitrate to a value supported by MCU.
Clock Delay	<ul style="list-style-type: none"> <li>• SPI_DELAY_COUNT_1</li> <li>• SPI_DELAY_COUNT_2</li> </ul>	SPI_DELAY_COUNT_1		Configure the number of SPI clock cycles before each data

	<ul style="list-style-type: none"> <li>NT_2</li> <li>• SPI_DELAY_COU</li> <li>NT_3</li> <li>• SPI_DELAY_COU</li> <li>NT_4</li> <li>• SPI_DELAY_COU</li> <li>NT_5</li> <li>• SPI_DELAY_COU</li> <li>NT_6</li> <li>• SPI_DELAY_COU</li> <li>NT_7</li> <li>• SPI_DELAY_COU</li> <li>NT_8</li> </ul>		frame.
SSL Negation Delay	<ul style="list-style-type: none"> <li>• SPI_DELAY_COU</li> <li>NT_1</li> <li>• SPI_DELAY_COU</li> <li>NT_2</li> <li>• SPI_DELAY_COU</li> <li>NT_3</li> <li>• SPI_DELAY_COU</li> <li>NT_4</li> <li>• SPI_DELAY_COU</li> <li>NT_5</li> <li>• SPI_DELAY_COU</li> <li>NT_6</li> <li>• SPI_DELAY_COU</li> <li>NT_7</li> <li>• SPI_DELAY_COU</li> <li>NT_8</li> </ul>	SPI_DELAY_COUNT_1	Configure the number of SPI clock cycles after each data frame.
Next Access Delay	<ul style="list-style-type: none"> <li>• SPI_DELAY_COU</li> <li>NT_1</li> <li>• SPI_DELAY_COU</li> <li>NT_2</li> <li>• SPI_DELAY_COU</li> <li>NT_3</li> <li>• SPI_DELAY_COU</li> <li>NT_4</li> <li>• SPI_DELAY_COU</li> <li>NT_5</li> <li>• SPI_DELAY_COU</li> <li>NT_6</li> <li>• SPI_DELAY_COU</li> <li>NT_7</li> <li>• SPI_DELAY_COU</li> <li>NT_8</li> </ul>	SPI_DELAY_COUNT_1	Configure the number of SPI clock cycles between each data frame.

### Clock Configuration

The clock for this module is derived from the following peripheral clock for each MCU group:

MCU Group	Peripheral Clock
RA2A1	PCLKB

---

RA4M1	PCLKA
RA4W1	PCLKA
RA6M1	PCLKA
RA6M2	PCLKA
RA6M3	PCLKA
RA6M4	PCLKA

## Pin Configuration

This module uses MOSI, MISO, RSPCK, and SSL pins to communicate with on board devices.

### Note

*At high bitrates, it might be necessary to configure the pins with `IOPORT_CFG_DRIVE_HIGH`.*

## Usage Notes

### Performance

At high bitrates, interrupts may not be able to service transfers fast enough. In master mode this means there will be a delay between each data frame. In slave mode this could result in TX Underrun and RX Overflow errors.

In order to improve performance at high bitrates, it is recommended that the instance be configured to service transfers using the DTC.

Another way to improve performance is to transfer the data in 16/32 bit wide data frames when possible. A typical use-case where this is possible is when reading/writing to a block device.

### Transmit From RXI Interrupt

After every data frame the SPI peripheral generates a transmit buffer empty interrupt and a receive buffer full interrupt. It is possible to configure the driver to handle transmit buffer empty interrupts in the receive buffer full isr. This only improves performance when the DTC is not being used.

### Note

*Configuring the module to use RX DTC instance without also providing a TX DTC instance results in an invalid configuration when RXI transmit is enabled.*

*Transmit Only mode is not supported when Transmit from RXI is enabled.*

### Clock Auto-Stopping

In master mode, if the Receive Buffer Full Interrupts are not handled fast enough, instead of generating a RX Overflow error, the last clock cycle will be stretched until the receive buffer is read.

### Parity Mode

When parity mode is configured, the LSB of each data frame is used as a parity bit. When odd parity is selected, the LSB is set such that there are an odd number of ones in the data frame. When even parity is selected, the LSB is set such that there are an even number of ones in the data frame.

### Limitations

Developers should be aware of the following limitations when using the SPI:

- In master mode, the driver will only configure 4-Wire mode if the device supports SSL Level Keeping (SSLKP bit in SPCMD0) and will return FSP\_ERR\_UNSUPPORTED if configured for 4-Wire mode on devices without SSL Level Keeping. Without SSL Level Keeping, the SSL pin is toggled after every data frame. In most cases this is not desirable behavior so it is recommended that the SSL pin be driven in software if SSL Level Keeping is not present on the device.
- In order to use CPHA=0 setting in slave mode, the master must toggle the SSL pin after every data frame (Even if the device supports SSL Level Keeping). Because of this hardware limitation, the module will return FSP\_ERR\_UNSUPPORTED when it is configured to use CPHA=0 setting in slave mode.
- The module does not support communicating with multiple slaves using different SSL pins. In order to achieve this, the module must either be closed and re-opened to change the SSL pin or drive SSL in software. It is recommended that SSL be driven in software when controlling multiple slave devices.
- The SPI peripheral has a minimum 3 SPI CLK delay between each data frame.

## Examples

### Basic Example

This is a basic example of minimal use of the SPI in an application.

```
static volatile bool g_transfer_complete = false;

void spi_basic_example (void)
{
    uint8_t tx_buffer[TRANSFER_SIZE];
    uint8_t rx_buffer[TRANSFER_SIZE];

    fsp_err_t err = FSP_SUCCESS;

    /* Initialize the SPI module. */
    err = R_SPI_Open(&g_spi_ctrl, &g_spi_cfg);

    /* Handle any errors. This function should be defined by the user. */
    handle_error(err);

    /* Start a write/read transfer */
    err = R_SPI_WriteRead(&g_spi_ctrl, tx_buffer, rx_buffer, TRANSFER_SIZE,
SPI_BIT_WIDTH_8_BITS);
    handle_error(err);

    /* Wait for SPI_EVENT_TRANSFER_COMPLETE callback event. */
    while (false == g_transfer_complete)
    {
        ;
    }
}
```

```
}  
  
static void r_spi_callback (spi_callback_args_t * p_args)  
{  
    if (SPI_EVENT_TRANSFER_COMPLETE == p_args->event)  
    {  
        g_transfer_complete = true;  
    }  
}
```

### Driving Software Slave Select Line

This is an example of communicating with multiple slave devices by asserting SSL in software.

```
void spi_software_ssl_example (void)  
{  
    uint8_t tx_buffer[TRANSFER_SIZE];  
    uint8_t rx_buffer[TRANSFER_SIZE];  
    /* Configure Slave Select Line 1 */  
    R_BSP_PinWrite(SLAVE_SELECT_LINE_1, BSP_IO_LEVEL_HIGH);  
    /* Configure Slave Select Line 2 */  
    R_BSP_PinWrite(SLAVE_SELECT_LINE_2, BSP_IO_LEVEL_HIGH);  
    fsp_err_t err = FSP_SUCCESS;  
    /* Initialize the SPI module. */  
    err = R_SPI_Open(&g_spi_ctrl, &g_spi_cfg);  
    /* Handle any errors. This function should be defined by the user. */  
    handle_error(err);  
    /* Assert Slave Select Line 1 */  
    R_BSP_PinWrite(SLAVE_SELECT_LINE_1, BSP_IO_LEVEL_LOW);  
    /* Start a write/read transfer */  
    g_transfer_complete = false;  
    err = R_SPI_WriteRead(&g_spi_ctrl, tx_buffer, rx_buffer,  
TRANSFER_SIZE, SPI_BIT_WIDTH_8_BITS);  
    handle_error(err);  
    /* Wait for SPI_EVENT_TRANSFER_COMPLETE callback event. */  
    while (false == g_transfer_complete)
```

```
{
    ;
}

/* De-assert Slave Select Line 1 */
R_BSP_PinWrite(SLAVE_SELECT_LINE_1, BSP_IO_LEVEL_HIGH);
/* Wait for minimum time required between transfers. */
R_BSP_SoftwareDelay(SSL_NEXT_ACCESS_DELAY, BSP_DELAY_UNITS_MICROSECONDS);
/* Assert Slave Select Line 2 */
R_BSP_PinWrite(SLAVE_SELECT_LINE_2, BSP_IO_LEVEL_LOW);
/* Start a write/read transfer */
g_transfer_complete = false;
err = R_SPI_WriteRead(&g_spi_ctrl, tx_buffer, rx_buffer,
TRANSFER_SIZE, SPI_BIT_WIDTH_8_BITS);
    handle_error(err);
/* Wait for SPI_EVENT_TRANSFER_COMPLETE callback event. */
while (false == g_transfer_complete)
    {
        ;
    }
/* De-assert Slave Select Line 2 */
R_BSP_PinWrite(SLAVE_SELECT_LINE_2, BSP_IO_LEVEL_HIGH);
}
```

## Configuring the SPI Clock Divider Registers

This example demonstrates how to set the SPI clock divisors at runtime.

```
void spi_bitrate_example (void)
{
    fsp_err_t err = FSP_SUCCESS;

    g_spi_cfg.p_extend = &g_spi_extended_cfg;

    /* Configure SPI Clock divider to achieve largest bitrate less than or equal to the
desired bitrate. */

    err = R_SPI_CalculateBitrate(BITRATE, &(g_spi_extended_cfg.spck_div));

    handle_error(err);
}
```



```

/* Initialize the SPI module. */
err = R_SPI_Open(&g_spi_ctrl, &g_spi_cfg);
/* Handle any errors. This function should be defined by the user. */
handle_error(err);
}

```

## Data Structures

struct [rspck\\_div\\_setting\\_t](#)

struct [spi\\_extended\\_cfg\\_t](#)

struct [spi\\_instance\\_ctrl\\_t](#)

## Enumerations

enum [spi\\_ssl\\_mode\\_t](#)

enum [spi\\_communication\\_t](#)

enum [spi\\_ssl\\_polarity\\_t](#)

enum [spi\\_ssl\\_select\\_t](#)

enum [spi\\_mosi\\_idle\\_value\\_fixing\\_t](#)

enum [spi\\_parity\\_t](#)

enum [spi\\_byte\\_swap\\_t](#)

enum [spi\\_delay\\_count\\_t](#)

## Data Structure Documentation

### ◆ [rspck\\_div\\_setting\\_t](#)

struct <a href="#">rspck_div_setting_t</a>		
SPI Clock Divider settings.		
Data Fields		
uint8_t	spbr	SPBR register setting.
uint8_t	brdv: 2	BRDV setting in SPCMD0.

### ◆ [spi\\_extended\\_cfg\\_t](#)

struct <a href="#">spi_extended_cfg_t</a>	
Extended SPI interface configuration	

Data Fields		
<a href="#">spi_ssl_mode_t</a>	spi_clksyn	Select spi or clock syn mode operation.
<a href="#">spi_communication_t</a>	spi_comm	Select full-duplex or transmit-only communication.
<a href="#">spi_ssl_polarity_t</a>	ssl_polarity	Select SSLn signal polarity.
<a href="#">spi_ssl_select_t</a>	ssl_select	Select which slave to use: 0-SSL0, 1-SSL1, 2-SSL2, 3-SSL3.
<a href="#">spi_mosi_idle_value_fixing_t</a>	mosi_idle	Select MOSI idle fixed value and selection.
<a href="#">spi_parity_t</a>	parity	Select parity and enable/disable parity.
<a href="#">spi_byte_swap_t</a>	byte_swap	Select byte swap mode.
<a href="#">rspck_div_setting_t</a>	spck_div	Register values for configuring the SPI Clock Divider.
<a href="#">spi_delay_count_t</a>	spck_delay	SPI Clock Delay Register Setting.
<a href="#">spi_delay_count_t</a>	ssl_negation_delay	SPI Slave Select Negation Delay Register Setting.
<a href="#">spi_delay_count_t</a>	next_access_delay	SPI Next-Access Delay Register Setting.

#### ◆ spi\_instance\_ctrl\_t

struct spi_instance_ctrl_t	
Channel control block. DO NOT INITIALIZE. Initialization occurs when <a href="#">spi_api_t::open</a> is called.	
Data Fields	
uint32_t	<a href="#">open</a>
	Indicates whether the <a href="#">open()</a> API has been successfully called.
<a href="#">spi_cfg_t</a> const *	<a href="#">p_cfg</a>
	Pointer to instance configuration.
R_SPI0_Type *	<a href="#">p_regs</a>
	Base register for this channel.
void const *	<a href="#">p_tx_data</a>

	Buffer to transmit.
void *	<a href="#">p_rx_data</a>
	Buffer to receive.
uint32_t	<a href="#">tx_count</a>
	Number of Data Frames to transfer (8-bit, 16-bit, 32-bit)
uint32_t	<a href="#">rx_count</a>
	Number of Data Frames to transfer (8-bit, 16-bit, 32-bit)
uint32_t	<a href="#">count</a>
	Number of Data Frames to transfer (8-bit, 16-bit, 32-bit)
<a href="#">spi_bit_width_t</a>	<a href="#">bit_width</a>
	Bits per Data frame (8-bit, 16-bit, 32-bit)

## Enumeration Type Documentation

### ◆ [spi\\_ssl\\_mode\\_t](#)

enum <a href="#">spi_ssl_mode_t</a>	
3-Wire or 4-Wire mode.	
Enumerator	
<a href="#">SPI_SSL_MODE_SPI</a>	SPI operation (4-wire method)
<a href="#">SPI_SSL_MODE_CLK_SYN</a>	Clock Synchronous operation (3-wire method)

## ◆ spi\_communication\_t

enum spi_communication_t	
Transmit Only (Half Duplex), or Full Duplex.	
Enumerator	
SPI_COMMUNICATION_FULL_DUPLEX	Full-Duplex synchronous serial communication.
SPI_COMMUNICATION_TRANSMIT_ONLY	Transit only serial communication.

## ◆ spi\_ssl\_polarity\_t

enum spi_ssl_polarity_t	
Slave Select Polarity.	
Enumerator	
SPI_SSLP_LOW	SSLP signal polarity active low.
SPI_SSLP_HIGH	SSLP signal polarity active high.

## ◆ spi\_ssl\_select\_t

enum spi_ssl_select_t	
The Slave Select Line	
Enumerator	
SPI_SSL_SELECT_SSL0	Select SSL0.
SPI_SSL_SELECT_SSL1	Select SSL1.
SPI_SSL_SELECT_SSL2	Select SSL2.
SPI_SSL_SELECT_SSL3	Select SSL3.

## ◆ spi\_mosi\_idle\_value\_fixing\_t

enum spi_mosi_idle_value_fixing_t	
MOSI Idle Behavior.	
Enumerator	
SPI_MOSI_IDLE_VALUE_FIXING_DISABLE	MOSI output value=value set in MOIFV bit.
SPI_MOSI_IDLE_VALUE_FIXING_LOW	MOSIn level low during MOSI idling.
SPI_MOSI_IDLE_VALUE_FIXING_HIGH	MOSIn level high during MOSI idling.

## ◆ spi\_parity\_t

enum spi_parity_t	
Parity Mode	
Enumerator	
SPI_PARITY_MODE_DISABLE	Disable parity.
SPI_PARITY_MODE_ODD	Select even parity.
SPI_PARITY_MODE_EVEN	Select odd parity.

## ◆ spi\_byte\_swap\_t

enum spi_byte_swap_t	
Byte Swapping Enable/Disable.	
Enumerator	
SPI_BYTE_SWAP_DISABLE	Disable Byte swapping for 16/32-Bit transfers.
SPI_BYTE_SWAP_ENABLE	Enable Byte swapping for 16/32-Bit transfers.

## ◆ spi\_delay\_count\_t

enum spi_delay_count_t	
Delay count for SPI delay settings.	
Enumerator	
SPI_DELAY_COUNT_1	Set RSPCK delay count to 1 RSPCK.
SPI_DELAY_COUNT_2	Set RSPCK delay count to 2 RSPCK.
SPI_DELAY_COUNT_3	Set RSPCK delay count to 3 RSPCK.
SPI_DELAY_COUNT_4	Set RSPCK delay count to 4 RSPCK.
SPI_DELAY_COUNT_5	Set RSPCK delay count to 5 RSPCK.
SPI_DELAY_COUNT_6	Set RSPCK delay count to 6 RSPCK.
SPI_DELAY_COUNT_7	Set RSPCK delay count to 7 RSPCK.
SPI_DELAY_COUNT_8	Set RSPCK delay count to 8 RSPCK.

**Function Documentation**

◆ **R\_SPI\_Open()**

```
fsp_err_t R_SPI_Open ( spi_ctrl_t * p_api_ctrl, spi_cfg_t const *const p_cfg )
```

This function initializes a channel for SPI communication mode. Implements [spi\\_api\\_t::open](#).

This function performs the following tasks:

- Performs parameter checking and processes error conditions.
- Configures the peripheral registers according to the configuration.
- Initialize the control structure for use in other [SPI Interface](#) functions.

**Return values**

FSP_SUCCESS	Channel initialized successfully.
FSP_ERR_ALREADY_OPEN	Instance was already initialized.
FSP_ERR_ASSERTION	An invalid argument was given in the configuration structure.
FSP_ERR_UNSUPPORTED	A requested setting is not possible on this device with the current build configuration.
FSP_ERR_IP_CHANNEL_NOT_PRESENT	The channel number is invalid.

**Returns**

See [Common Error Codes](#) or functions called by this function for other possible return codes. This function calls: [transfer\\_api\\_t::open](#)

*Note*

*This function is reentrant.*

◆ **R\_SPI\_Read()**

```
fsp_err_t R_SPI_Read ( spi_ctrl_t *const p_api_ctrl, void * p_dest, uint32_t const length, spi_bit_width_t const bit_width )
```

This function receives data from a SPI device. Implements [spi\\_api\\_t::read](#).

The function performs the following tasks:

- Performs parameter checking and processes error conditions.
- Sets up the instance to complete a SPI read operation.

**Return values**

FSP_SUCCESS	Read operation successfully completed.
FSP_ERR_ASSERTION	NULL pointer to control or destination parameters or transfer length is zero.
FSP_ERR_NOT_OPEN	The channel has not been opened. Open channel first.
FSP_ERR_IN_USE	A transfer is already in progress.

◆ **R\_SPI\_Write()**

```
fsp_err_t R_SPI_Write ( spi_ctrl_t *const p_api_ctrl, void const * p_src, uint32_t const length,
spi_bit_width_t const bit_width )
```

This function transmits data to a SPI device using the TX Only Communications Operation Mode. Implements `spi_api_t::write`.

The function performs the following tasks:

- Performs parameter checking and processes error conditions.
- Sets up the instance to complete a SPI write operation.

**Return values**

FSP_SUCCESS	Write operation successfully completed.
FSP_ERR_ASSERTION	NULL pointer to control or source parameters or transfer length is zero.
FSP_ERR_NOT_OPEN	The channel has not been opened. Open the channel first.
FSP_ERR_IN_USE	A transfer is already in progress.

◆ **R\_SPI\_WriteRead()**

```
fsp_err_t R_SPI_WriteRead ( spi_ctrl_t *const p_api_ctrl, void const * p_src, void * p_dest, uint32_t
const length, spi_bit_width_t const bit_width )
```

This function simultaneously transmits and receive data. Implements `spi_api_t::writeRead`.

The function performs the following tasks:

- Performs parameter checking and processes error conditions.
- Sets up the instance to complete a SPI writeRead operation.

**Return values**

FSP_SUCCESS	Write operation successfully completed.
FSP_ERR_ASSERTION	NULL pointer to control, source or destination parameters or transfer length is zero.
FSP_ERR_NOT_OPEN	The channel has not been opened. Open the channel first.
FSP_ERR_IN_USE	A transfer is already in progress.



◆ **R\_SPI\_Close()**

```
fsp_err_t R_SPI_Close ( spi_ctrl_t *const p_api_ctrl)
```

This function manages the closing of a channel by the following task. Implements `spi_api_t::close`.

Disables SPI operations by disabling the SPI bus.

- Disables the SPI peripheral.
- Disables all the associated interrupts.
- Update control structure so it will not work with [SPI Interface](#) functions.

**Return values**

FSP_SUCCESS	Channel successfully closed.
FSP_ERR_ASSERTION	A required pointer argument is NULL.
FSP_ERR_NOT_OPEN	The channel has not been opened. Open the channel first.

◆ **R\_SPI\_VersionGet()**

```
fsp_err_t R_SPI_VersionGet ( fsp_version_t * p_version)
```

This function gets the version information of the underlying driver. Implements `spi_api_t::versionGet`.

**Return values**

FSP_SUCCESS	Successful version get.
FSP_ERR_ASSERTION	The parameter <code>p_version</code> is NULL.

◆ **R\_SPI\_CalculateBitrate()**

```
fsp_err_t R_SPI_CalculateBitrate ( uint32_t bitrate, rspck_div_setting_t * spck_div )
```

Calculates the SPBR register value and the BRDV bits for a desired bitrate. If the desired bitrate is faster than the maximum bitrate, than the bitrate is set to the maximum bitrate. If the desired bitrate is slower than the minimum bitrate, than an error is returned.

**Parameters**

[in]	bitrate	Desired bitrate
[out]	spck_div	Memory location to store bitrate register settings.

**Return values**

FSP_SUCCESS	Valid spbr and brdv values were calculated
FSP_ERR_UNSUPPORTED	Bitrate is not achievable

◆ **R\_SPI\_CallbackSet()**

```
fsp_err_t R_SPI_CallbackSet ( spi_ctrl_t *const p_api_ctrl, void(*)(spi_callback_args_t *) p_callback, void const *const p_context, spi_callback_args_t *const p_callback_memory )
```

Updates the user callback and has option of providing memory for callback structure. Implements `spi_api_t::callbackSet`

**Return values**

FSP_SUCCESS	Callback updated successfully.
FSP_ERR_ASSERTION	A required pointer is NULL.
FSP_ERR_NOT_OPEN	The control block has not been opened.

**4.2.47 Serial Sound Interface (r\_ssi)**

## Modules

**Functions**

```
fsp_err_t R_SSI_Open (i2s_ctrl_t *const p_ctrl, i2s_cfg_t const *const p_cfg)
```

```
fsp_err_t R_SSI_Stop (i2s_ctrl_t *const p_ctrl)
```

```
fsp_err_t R_SSI_StatusGet (i2s_ctrl_t *const p_ctrl, i2s_status_t *const
```

	p_status)
fsp_err_t	R_SSI_Write (i2s_ctrl_t *const p_ctrl, void const *const p_src, uint32_t const bytes)
fsp_err_t	R_SSI_Read (i2s_ctrl_t *const p_ctrl, void *const p_dest, uint32_t const bytes)
fsp_err_t	R_SSI_WriteRead (i2s_ctrl_t *const p_ctrl, void const *const p_src, void *const p_dest, uint32_t const bytes)
fsp_err_t	R_SSI_Mute (i2s_ctrl_t *const p_ctrl, i2s_mute_t const mute_enable)
fsp_err_t	R_SSI_Close (i2s_ctrl_t *const p_ctrl)
fsp_err_t	R_SSI_VersionGet (fsp_version_t *const p_version)
fsp_err_t	R_SSI_CallbackSet (i2s_ctrl_t *const p_api_ctrl, void(*p_callback)(i2s_callback_args_t*), void const *const p_context, i2s_callback_args_t *const p_callback_memory)

## Detailed Description

Driver for the SSIE peripheral on RA MCUs. This module implements the [I2S Interface](#).

## Overview

### Features

The SSI module supports the following features:

- Transmission and reception of uncompressed audio data using the standard I2S protocol in master mode
- Full-duplex I2S communication (channel 0 only)
- Integration with the DTC transfer module
- Internal connection to GPT timer output to generate the audio clock
- Callback function notification when all data is loaded into the SSI FIFO

## Configuration

### Build Time Configurations for r\_ssi

The following build time configurations are defined in fsp\_cfg/r\_ssi\_cfg.h:

Configuration	Options	Default	Description
Parameter Checking	<ul style="list-style-type: none"> <li>• Default (BSP)</li> <li>• Enabled</li> <li>• Disabled</li> </ul>	Default (BSP)	If selected code for parameter checking is included in the build.

DTC Support	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Enabled	If code for DTC transfer support is included in the build.
-------------	---------------------------------------------------------------------------------	---------	------------------------------------------------------------

### Configurations for Driver > Connectivity > I2S Driver on r\_ssi

This module can be added to the Stacks tab via New Stack > Driver > Connectivity > I2S Driver on r\_ssi. Non-secure callable guard functions can be generated for this module by right clicking the module in the RA Configuration tool and checking the "Non-secure Callable" box.

Configuration	Options	Default	Description
Name	Name must be a valid C symbol	g_i2s0	Module name.
Channel	Value must be an integer between 0 and 1	0	Specify the I2S channel.
Bit Depth	<ul style="list-style-type: none"> <li>• 8 Bits</li> <li>• 16 Bits</li> <li>• 18 Bits</li> <li>• 20 Bits</li> <li>• 22 Bits</li> <li>• 24 Bits</li> <li>• 32 Bits</li> </ul>	16 Bits	Select the bit depth of one sample of audio data.
Word Length	<ul style="list-style-type: none"> <li>• 8 Bits</li> <li>• 16 Bits</li> <li>• 24 Bits</li> <li>• 32 Bits</li> <li>• 48 Bits</li> <li>• 64 Bits</li> <li>• 128 Bits</li> <li>• 256 Bits</li> </ul>	16 Bits	Select the word length of audio data. Must be at least as large as Data bits.
WS Continue Mode	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Disabled	Enable WS continue mode to output the word select (WS) pin even when transmission is idle.
Bit Clock Source	<ul style="list-style-type: none"> <li>• External AUDIO_CLK</li> <li>• Internal AUDIO_CLK</li> </ul>	External AUDIO_CLK	Select AUDIO_CLK for external signal to AUDIO_CLK input pin or GTIOC1A for internal connection to GPT channel 1 GTIOC1A.
Bit Clock Divider	Refer to the RA Configuration tool for available options.	Audio Clock / 1	Select divider used to generate bit clock from audio clock.
Callback	Name must be a valid C symbol	NULL	A user callback function can be provided. If this callback function is provided, it will be

called from all three interrupt service routines (ISR).

Transmit Interrupt Priority	MCU Specific Options	Select the transmit interrupt priority.
Receive Interrupt Priority	MCU Specific Options	Select the receive interrupt priority.
Idle/Error Interrupt Priority	MCU Specific Options	Select the Idle/Error interrupt priority.

## Clock Configuration

The SSI peripheral runs on PCLKB. The PCLKB frequency can be configured on the **Clocks** tab of the RA Configuration editor. The SSI audio clock can optionally be supplied from an external source through the AUDIO\_CLK pin in master mode.

## Pin Configuration

The SSI uses the following pins:

- AUDIO\_CLK (optional, master mode only): The AUDIO\_CLK pin is used to supply the audio clock from an external source.
- SSIBCKn: Bit clock pin for channel n
- SSILRCKn/SSIFSn: Channel selection pin for channel n
- SSIRXD0: Reception pin for channel 0
- SSITXD0: Transmission pin for channel 0
- SSIDATA1: Transmission or reception pin for channel 1

## Usage Notes

### SSI Frames

An SSI frame is 2 samples worth of data. The frame boundary (end of previous frame, start of next frame) is on the falling edge of the SSILRCKn signal.

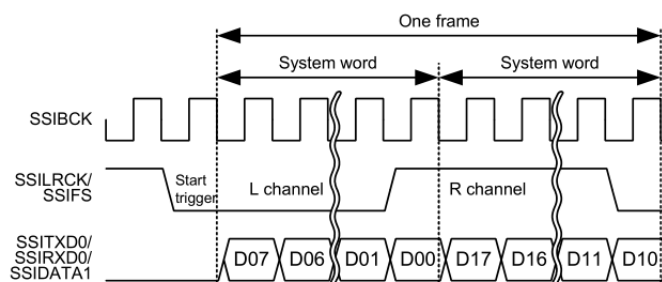


Figure 169: SSI Frame Diagram (8-bit word, 8-bit samples)

### Note

*If the word length is longer than the sample bit depth, padding bits (0) will be added after the sample.*

### Audio Data

Only uncompressed PCM data is supported.

Data arrays have the following size, alignment, and length based on the "Bit Depth" setting:

Bit Depth	Array Data Type	Required Alignment	Required Length (bytes)
8 Bits	8-bit integer	1 byte alignment	Multiple of 2
16 Bits	16-bit integer	2 byte alignment	Multiple of 4
18 Bits	32-bit integer, right justified	4 byte alignment	Multiple of 8
20 Bits	32-bit integer, right justified	4 byte alignment	Multiple of 8
22 Bits	32-bit integer, right justified	4 byte alignment	Multiple of 8
24 Bits	32-bit integer, right justified	4 byte alignment	Multiple of 8
32 Bits	32-bit integer	4 byte alignment	Multiple of 8

*Note*

*The length of the array must be a multiple of 2 when the data type is the recommended data type. The 2 represents the frame size (left and right channel) of I2S communication. The SSIE peripheral does not support odd read/write lengths in I2S mode.*

## Audio Clock

The audio clock is only required for master mode.

### Audio Clock Frequency

The bit clock frequency is the product of the sampling frequency and channels and bits per system word:

$$\text{bit\_clock (Hz)} = \text{sampling\_frequency (Hz)} * \text{channels} * \text{system\_word\_bits}$$

I2S data always has 2 channels.

For example, the bit clock for transmitting 2 channels of 16-bit data (using a 16-bit system word) at 44100 Hz would be:

$$44100 * 2 * 16 = 1,411,200 \text{ Hz}$$

The audio clock frequency is used to generate the bit clock frequency. It must be a multiple of the bit clock frequency. Refer to the Bit Clock Divider configuration for divider options. The input audio clock frequency must be:

$$\text{audio\_clock (Hz)} = \text{desired\_bit\_clock (Hz)} * \text{bit\_clock\_divider}$$

To get a bit clock of 1.4 MHz from an audio clock of 2.8 MHz, select the divider Audio Clock / 2.

### Audio Clock Source

The audio clock source can come from:

- An external source input to the AUDIO\_CLK pin
- An internal connection to the GPT timer output

#### Note

*When using the internal GPT timer output, Pin Output Support must be Enabled, and GTIOCA Output Enabled must be True.*

*See the SSIE section in the MCU hardware manual for information about which GPT channel may be used.*

## Limitations

Developers should be aware of the following limitations when using the SSI:

- When using channel 1, full duplex communication is not possible. Only transmission or reception is possible.
- SSI must go idle before changing the communication mode (between read only, write only, and full duplex)

## Examples

### Basic Example

This is a basic example of minimal use of the SSI in an application.

```
#define SSI_EXAMPLE_SAMPLES_TO_TRANSFER (1024)
#define SSI_EXAMPLE_TONE_FREQUENCY_HZ (800)
int16_t g_src[SSI_EXAMPLE_SAMPLES_TO_TRANSFER];
int16_t g_dest[SSI_EXAMPLE_SAMPLES_TO_TRANSFER];
void ssi_basic_example (void)
{
    fsp_err_t err = FSP_SUCCESS;

    /* Create a stereo sine wave. Using formula sample = sin(2 * pi * tone_frequency * t
    / sampling_frequency) */

    uint32_t freq = SSI_EXAMPLE_TONE_FREQUENCY_HZ;
    for (uint32_t t = 0; t < SSI_EXAMPLE_SAMPLES_TO_TRANSFER / 2; t += 1)
    {
        float input = (((float) (freq * t)) * (M_TWOPI)) /
        SSI_EXAMPLE_AUDIO_SAMPLING_FREQUENCY_HZ;

        g_src[2 * t] = (int16_t) ((INT16_MAX * sinf(input)));
        g_src[2 * t + 1] = (int16_t) ((INT16_MAX * sinf(input)));
    }

    /* Initialize the module. */
```

```

err = R_SSI_Open(&g_i2s_ctrl, &g_i2s_cfg);

/* Handle any errors. This function should be defined by the user. */
handle_error(err);

/* Transfer data. */
(void) R_SSI_WriteRead(&g_i2s_ctrl,
                      (uint8_t *) &g_src[0],
                      (uint8_t *) &g_dest[0],
                      SSI_EXAMPLE_SAMPLES_TO_TRANSFER * sizeof(int16_t));
}

```

## Streaming Example

This is an example of using SSI to stream audio data. This application uses a double buffer to store PCM sine wave data. It starts transmitting in the main loop, then loads the next buffer if it is ready in the callback. If the next buffer is not ready, a flag is set in the callback so the application knows to restart transmission in the main loop.

This example also checks the return code of `R_SSI_Write()` because `R_SSI_Write()` can return an error if a transmit overflow occurs before the FIFO is reloaded. If a transmit overflow occurs before the FIFO is reloaded, the SSI will be stopped in the error interrupt, and it cannot be restarted until the `I2S_EVENT_IDLE` callback is received.

```

#define SSI_STREAMING_EXAMPLE_AUDIO_SAMPLING_FREQUENCY_HZ (22050)
#define SSI_STREAMING_EXAMPLE_SAMPLES_PER_CHUNK (1024)
#define SSI_STREAMING_EXAMPLE_TONE_FREQUENCY_HZ (800)

int16_t      g_stream_src[2][SSI_EXAMPLE_SAMPLES_TO_TRANSFER];
uint32_t     g_buffer_index      = 0;
volatile bool g_send_data_in_main_loop = true;
volatile bool g_data_ready      = false;

/* Example callback called when SSI is ready for more data. */
void ssi_example_callback (i2s_callback_args_t * p_args)
{
    /* Reload the FIFO if we hit the transmit watermark or restart transmission if the
    SSI is idle because it was
    * stopped after a transmit FIFO overflow. */
    if ((I2S_EVENT_TX_EMPTY == p_args->event) || (I2S_EVENT_IDLE == p_args->event))
    {
        if (g_data_ready)

```



```
{
/* Reload FIFO and handle errors. */
    ssi_example_write();
}
else
{
/* Data was not ready yet, send it in the main loop. */
    g_send_data_in_main_loop = true;
}
}
/* Load the transmit FIFO and check for error conditions. */
void ssi_example_write (void)
{
/* Transfer data. This call is non-blocking. */
fsp_err_t err = R_SSI_Write(&g_i2s_ctrl,
                            (uint8_t *) &g_stream_src[g_buffer_index][0],
                            SSI_STREAMING_EXAMPLE_SAMPLES_PER_CHUNK * sizeof
(int16_t));
if (FSP_SUCCESS == err)
{
/* Switch the buffer after data is sent. */
    g_buffer_index = !g_buffer_index;
/* Allow loop to calculate next buffer only if transmission was successful. */
    g_data_ready = false;
}
else
{
/* Getting here most likely means a transmit overflow occurred before the FIFO could
be reloaded. The
* application must wait until the SSI is idle, then restart transmission. In this
example, the idle
* callback transmits data or resets the flag g_send_data_in_main_loop. */
}
}
```

```
}
/* Calculate samples. This example is just a sine wave. For this type of data, it
would be better to calculate
 * one period and loop it. This example should be updated for the audio data used by
the application. */
void ssi_example_calculate_samples (uint32_t buffer_index)
{
    static uint32_t t = 0U;
    /* Create a stereo sine wave. Using formula sample = sin(2 * pi * tone_frequency * t
/ sampling_frequency) */
    uint32_t freq = SSI_STREAMING_EXAMPLE_TONE_FREQUENCY_HZ;
    for (uint32_t i = 0; i < SSI_STREAMING_EXAMPLE_SAMPLES_PER_CHUNK / 2; i += 1)
    {
        float input = (((float) (freq * t)) * M_TWOPHI) /
SSI_STREAMING_EXAMPLE_AUDIO_SAMPLING_FREQUENCY_HZ;
        t++;
        /* Store sample twice, once for left channel and once for right channel. */
        int16_t sample = (int16_t) ((INT16_MAX * sinf(input)));
        g_stream_src[buffer_index][2 * i] = sample;
        g_stream_src[buffer_index][2 * i + 1] = sample;
    }
    /* Data is ready to be sent in the interrupt. */
    g_data_ready = true;
}
void ssi_streaming_example (void)
{
    fsp_err_t err = FSP_SUCCESS;
    /* Initialize the module. */
    err = R_SSI_Open(&g_i2s_ctrl, &g_i2s_cfg);
    /* Handle any errors. This function should be defined by the user. */
    handle_error(err);
    while (true)
    {
        /* Prepare data in a buffer that is not currently used for transmission. */
```

```

    ssi_example_calculate_samples(g_buffer_index);
/* Send data in main loop the first time, and if it was not ready in the interrupt.
*/
if (g_send_data_in_main_loop)
    {
/* Clear flag. */
    g_send_data_in_main_loop = false;
/* Reload FIFO and handle errors. */
    ssi_example_write();
    }
/* If the next buffer is ready, wait for the data to be sent in the interrupt. */
while (g_data_ready)
    {
/* Do nothing. */
    }
    }
}

```

## Data Structures

struct [ssi\\_instance\\_ctrl\\_t](#)

struct [ssi\\_extended\\_cfg\\_t](#)

## Enumerations

enum [ssi\\_audio\\_clock\\_t](#)

enum [ssi\\_clock\\_div\\_t](#)

## Data Structure Documentation

### ◆ [ssi\\_instance\\_ctrl\\_t](#)

struct [ssi\\_instance\\_ctrl\\_t](#)

Channel instance control block. DO NOT INITIALIZE. Initialization occurs when [i2s\\_api\\_t::open](#) is called.

### ◆ [ssi\\_extended\\_cfg\\_t](#)

struct [ssi\\_extended\\_cfg\\_t](#)

SSI configuration extension. This extension is optional.

Data Fields		
<code>ssi_audio_clock_t</code>	<code>audio_clock</code>	Audio clock source, default is SSI_AUDIO_CLOCK_EXTERNAL.
<code>ssi_clock_div_t</code>	<code>bit_clock_div</code>	Select bit clock division ratio.

## Enumeration Type Documentation

### ◆ `ssi_audio_clock_t`

enum <code>ssi_audio_clock_t</code>	
Audio clock source.	
Enumerator	
SSI_AUDIO_CLOCK_EXTERNAL	Audio clock source is the AUDIO_CLK input pin.
SSI_AUDIO_CLOCK_INTERNAL	Audio clock source is internal connection to a MCU specific GPT channel output.

◆ **ssi\_clock\_div\_t**

enum <code>ssi_clock_div_t</code>	
Bit clock division ratio. Bit clock frequency = audio clock frequency / bit clock division ratio.	
Enumerator	
<code>SSI_CLOCK_DIV_1</code>	Clock divisor 1.
<code>SSI_CLOCK_DIV_2</code>	Clock divisor 2.
<code>SSI_CLOCK_DIV_4</code>	Clock divisor 4.
<code>SSI_CLOCK_DIV_6</code>	Clock divisor 6.
<code>SSI_CLOCK_DIV_8</code>	Clock divisor 8.
<code>SSI_CLOCK_DIV_12</code>	Clock divisor 12.
<code>SSI_CLOCK_DIV_16</code>	Clock divisor 16.
<code>SSI_CLOCK_DIV_24</code>	Clock divisor 24.
<code>SSI_CLOCK_DIV_32</code>	Clock divisor 32.
<code>SSI_CLOCK_DIV_48</code>	Clock divisor 48.
<code>SSI_CLOCK_DIV_64</code>	Clock divisor 64.
<code>SSI_CLOCK_DIV_96</code>	Clock divisor 96.
<code>SSI_CLOCK_DIV_128</code>	Clock divisor 128.

**Function Documentation**

◆ **R\_SSI\_Open()**

```
fsp_err_t R_SSI_Open ( i2s_ctrl_t *const p_ctrl, i2s_cfg_t const *const p_cfg )
```

Opens the SSI. Implements [i2s\\_api\\_t::open](#).

This function sets this clock divisor and the configurations specified in [i2s\\_cfg\\_t](#). It also opens the timer and transfer instances if they are provided.

**Return values**

FSP_SUCCESS	Ready for I2S communication.
FSP_ERR_ASSERTION	The pointer to p_ctrl or p_cfg is null.
FSP_ERR_ALREADY_OPEN	The control block has already been opened.
FSP_ERR_IP_CHANNEL_NOT_PRESENT	Channel number is not available on this MCU.

**Returns**

See [Common Error Codes](#) or functions called by this function for other possible return codes. This function calls:

- [transfer\\_api\\_t::open](#)

◆ **R\_SSI\_Stop()**

```
fsp_err_t R_SSI_Stop ( i2s_ctrl_t *const p_ctrl)
```

Stops SSI. Implements [i2s\\_api\\_t::stop](#).

This function disables both transmission and reception, and disables any transfer instances used.

The SSI will stop on the next frame boundary. Do not restart SSI until it is idle.

**Return values**

FSP_SUCCESS	I2S communication stop request issued.
FSP_ERR_ASSERTION	The pointer to p_ctrl was null.
FSP_ERR_NOT_OPEN	The channel is not opened.

**Returns**

See [Common Error Codes](#) or lower level drivers for other possible return codes.

◆ **R\_SSI\_StatusGet()**

```
fsp_err_t R_SSI_StatusGet ( i2s_ctrl_t *const p_ctrl, i2s_status_t *const p_status )
```

Gets SSI status and stores it in provided pointer p\_status. Implements `i2s_api_t::statusGet`.

**Return values**

FSP_SUCCESS	Information stored successfully.
FSP_ERR_ASSERTION	The p_instance_ctrl or p_status parameter was null.
FSP_ERR_NOT_OPEN	The channel is not opened.

◆ **R\_SSI\_Write()**

```
fsp_err_t R_SSI_Write ( i2s_ctrl_t *const p_ctrl, void const *const p_src, uint32_t const bytes )
```

Writes data buffer to SSI. Implements `i2s_api_t::write`.

This function resets the transfer if the transfer interface is used, or writes the length of data that fits in the FIFO then stores the remaining write buffer in the control block to be written in the ISR.

Write() cannot be called if another write(), read() or writeRead() operation is in progress. Write can be called when the SSI is idle, or after the I2S\_EVENT\_TX\_EMPTY event.

**Return values**

FSP_SUCCESS	Write initiated successfully.
FSP_ERR_ASSERTION	The pointer to p_ctrl or p_src was null, or bytes requested was 0.
FSP_ERR_IN_USE	Another transfer is in progress, data was not written.
FSP_ERR_NOT_OPEN	The channel is not opened.
FSP_ERR_UNDERFLOW	A transmit underflow error is pending. Wait for the SSI to go idle before resuming communication.

**Returns**

See [Common Error Codes](#) or functions called by this function for other possible return codes. This function calls:

- `transfer_api_t::reset`

◆ **R\_SSI\_Read()**

```
fsp_err_t R_SSI_Read ( i2s_ctrl_t *const p_ctrl, void *const p_dest, uint32_t const bytes )
```

Reads data into provided buffer. Implements `i2s_api_t::read`.

This function resets the transfer if the transfer interface is used, or reads the length of data available in the FIFO then stores the remaining read buffer in the control block to be filled in the ISR.

Read() cannot be called if another write(), read() or writeRead() operation is in progress. Read can be called when the SSI is idle, or after the I2S\_EVENT\_RX\_FULL event.

**Return values**

FSP_SUCCESS	Read initiated successfully.
FSP_ERR_IN_USE	Peripheral is in the wrong mode or not idle.
FSP_ERR_ASSERTION	The pointer to p_ctrl or p_dest was null, or bytes requested was 0.
FSP_ERR_NOT_OPEN	The channel is not opened.
FSP_ERR_OVERFLOW	A receive overflow error is pending. Wait for the SSI to go idle before resuming communication.

**Returns**

See [Common Error Codes](#) or functions called by this function for other possible return codes. This function calls:

- [transfer\\_api\\_t::reset](#)



◆ **R\_SSI\_WriteRead()**

```
fsp_err_t R_SSI_WriteRead ( i2s_ctrl_t *const p_ctrl, void const *const p_src, void *const p_dest,
uint32_t const bytes )
```

Writes from source buffer and reads data into destination buffer. Implements [i2s\\_api\\_t::writeRead](#).

This function calls [R\\_SSI\\_Write](#) and [R\\_SSI\\_Read](#).

[writeRead\(\)](#) cannot be called if another [write\(\)](#), [read\(\)](#) or [writeRead\(\)](#) operation is in progress. [writeRead\(\)](#) can be called when the SSI is idle, or after the [I2S\\_EVENT\\_RX\\_FULL](#) event.

**Return values**

FSP_SUCCESS	Write and read initiated successfully.
FSP_ERR_IN_USE	Peripheral is in the wrong mode or not idle.
FSP_ERR_ASSERTION	An input parameter was invalid.
FSP_ERR_NOT_OPEN	The channel is not opened.
FSP_ERR_UNDERFLOW	A transmit underflow error is pending. Wait for the SSI to go idle before resuming communication.
FSP_ERR_OVERFLOW	A receive overflow error is pending. Wait for the SSI to go idle before resuming communication.

**Returns**

See [Common Error Codes](#) or functions called by this function for other possible return codes. This function calls:

- [transfer\\_api\\_t::reset](#)

◆ **R\_SSI\_Mute()**

```
fsp_err_t R_SSI_Mute ( i2s_ctrl_t *const p_ctrl, i2s_mute_t const mute_enable )
```

Mutes SSI on the next frame boundary. Implements [i2s\\_api\\_t::mute](#).

Data is still written while mute is enabled, but the transmit line outputs zeros.

**Return values**

FSP_SUCCESS	Transmission is muted.
FSP_ERR_ASSERTION	The pointer to <a href="#">p_ctrl</a> was null.
FSP_ERR_NOT_OPEN	The channel is not opened.

◆ **R\_SSI\_Close()**

```
fsp_err_t R_SSI_Close ( i2s_ctrl_t *const p_ctrl)
```

Closes SSI. Implements `i2s_api_t::close`.

This function powers down the SSI and closes the lower level timer and transfer drivers if they are used.

**Return values**

FSP_SUCCESS	Device closed successfully.
FSP_ERR_ASSERTION	The pointer to <code>p_ctrl</code> was null.
FSP_ERR_NOT_OPEN	The channel is not opened.

◆ **R\_SSI\_VersionGet()**

```
fsp_err_t R_SSI_VersionGet ( fsp_version_t *const p_version)
```

Sets driver version based on compile time macros.

**Return values**

FSP_SUCCESS	Successful close.
FSP_ERR_ASSERTION	The parameter <code>p_version</code> is NULL.

◆ **R\_SSI\_CallbackSet()**

```
fsp_err_t R_SSI_CallbackSet ( i2s_ctrl_t *const p_api_ctrl, void(*) (i2s_callback_args_t *) p_callback, void const *const p_context, i2s_callback_args_t *const p_callback_memory )
```

Updates the user callback and has option of providing memory for callback structure. Implements `i2s_api_t::callbackSet`

**Return values**

FSP_SUCCESS	Callback updated successfully.
FSP_ERR_ASSERTION	A required pointer is NULL.
FSP_ERR_NOT_OPEN	The control block has not been opened.

**4.2.48 USB (r\_usb\_basic)**

## Modules

## Functions

`fsp_err_t` [R\\_USB\\_Open](#) (`usb_ctrl_t *const p_api_ctrl, usb_cfg_t const *const p_cfg`)  
 Applies power to the USB module specified in the argument (`p_ctrl`).  
[More...](#)

`fsp_err_t` [R\\_USB\\_Close](#) (`usb_ctrl_t *const p_api_ctrl`)  
 Terminates power to the USB module specified in argument (`p_ctrl`).  
 USB0 module stops when `USB_IP0` is specified to the member  
 (module), USB1 module stops when `USB_IP1` is specified to the  
 member (module). [More...](#)

`fsp_err_t` [R\\_USB\\_Read](#) (`usb_ctrl_t *const p_api_ctrl, uint8_t *p_buf, uint32_t size, uint8_t destination`)  
 Bulk/interrupt data transfer and control data transfer. [More...](#)

`fsp_err_t` [R\\_USB\\_Write](#) (`usb_ctrl_t *const p_api_ctrl, uint8_t const *const p_buf, uint32_t size, uint8_t destination`)  
 Bulk/Interrupt data transfer and control data transfer. [More...](#)

`fsp_err_t` [R\\_USB\\_Stop](#) (`usb_ctrl_t *const p_api_ctrl, usb_transfer_t direction, uint8_t destination`)  
 Requests a data read/write transfer be terminated when a data  
 read/write transfer is being performed. [More...](#)

`fsp_err_t` [R\\_USB\\_Suspend](#) (`usb_ctrl_t *const p_api_ctrl`)  
 Sends a SUSPEND signal from the USB module assigned to the  
 member (module) of the `usb_ctrl_t` structure. [More...](#)

`fsp_err_t` [R\\_USB\\_Resume](#) (`usb_ctrl_t *const p_api_ctrl`)  
 Sends a RESUME signal from the USB module assigned to the  
 member (module) of the `usb_ctrl_t` structure. [More...](#)

`fsp_err_t` [R\\_USB\\_VbusSet](#) (`usb_ctrl_t *const p_api_ctrl, uint16_t state`)  
 Specifies starting or stopping the VBUS supply. [More...](#)

`fsp_err_t` [R\\_USB\\_InfoGet](#) (`usb_ctrl_t *const p_api_ctrl, usb_info_t *p_info,`

uint8\_t destination)

Obtains completed USB-related events. [More...](#)

[fsp\\_err\\_t](#) [R\\_USB\\_PipeRead](#) (usb\_ctrl\_t \*const p\_api\_ctrl, uint8\_t \*p\_buf, uint32\_t size, uint8\_t pipe\_number)

Requests a data read (bulk/interrupt transfer) via the pipe specified in the argument. [More...](#)

[fsp\\_err\\_t](#) [R\\_USB\\_PipeWrite](#) (usb\_ctrl\_t \*const p\_api\_ctrl, uint8\_t \*p\_buf, uint32\_t size, uint8\_t pipe\_number)

Requests a data write (bulk/interrupt transfer). [More...](#)

[fsp\\_err\\_t](#) [R\\_USB\\_PipeStop](#) (usb\_ctrl\_t \*const p\_api\_ctrl, uint8\_t pipe\_number)

Terminates a data read/write operation. [More...](#)

[fsp\\_err\\_t](#) [R\\_USB\\_UsedPipesGet](#) (usb\_ctrl\_t \*const p\_api\_ctrl, uint16\_t \*p\_pipe, uint8\_t destination)

Gets the selected pipe number (number of the pipe that has completed initialization) via bit map information. [More...](#)

[fsp\\_err\\_t](#) [R\\_USB\\_PipeInfoGet](#) (usb\_ctrl\_t \*const p\_api\_ctrl, usb\_pipe\_t \*p\_info, uint8\_t pipe\_number)

Gets the following pipe information regarding the pipe specified in the argument (p\_ctrl) member (pipe): endpoint number, transfer type, transfer direction and maximum packet size. [More...](#)

[fsp\\_err\\_t](#) [R\\_USB\\_PullUp](#) (usb\_ctrl\_t \*const p\_api\_ctrl, uint8\_t state)

This API enables or disables pull-up of D+/D- line. [More...](#)

[fsp\\_err\\_t](#) [R\\_USB\\_EventGet](#) (usb\_ctrl\_t \*const p\_api\_ctrl, usb\_status\_t \*event)

Obtains completed USB related events. (OS-less Only) [More...](#)

[fsp\\_err\\_t](#) [R\\_USB\\_VersionGet](#) (fsp\_version\_t \*const p\_version)

Returns the version of this module. [More...](#)

[fsp\\_err\\_t](#) [R\\_USB\\_Callback](#) (usb\_callback\_t \*p\_callback)

Register a callback function to be called upon completion of a USB

related event. (RTOS only) [More...](#)

`fsp_err_t` [R\\_USB\\_HostControlTransfer](#) (`usb_ctrl_t *const p_api_ctrl, usb_setup_t *p_setup, uint8_t *p_buf, uint8_t device_address`)

Performs settings and transmission processing when transmitting a setup packet. [More...](#)

`fsp_err_t` [R\\_USB\\_PeriControlDataGet](#) (`usb_ctrl_t *const p_api_ctrl, uint8_t *p_buf, uint32_t size`)

Receives data sent by control transfer. [More...](#)

`fsp_err_t` [R\\_USB\\_PeriControlDataSet](#) (`usb_ctrl_t *const p_api_ctrl, uint8_t *p_buf, uint32_t size`)

Performs transfer processing for control transfer. [More...](#)

`fsp_err_t` [R\\_USB\\_PeriControlStatusSet](#) (`usb_ctrl_t *const p_api_ctrl, usb_setup_status_t status`)

Set the response to the setup packet. [More...](#)

`fsp_err_t` [R\\_USB\\_RemoteWakeup](#) (`usb_ctrl_t *const p_api_ctrl`)

Sends a remote wake-up signal to the connected Host. [More...](#)

`fsp_err_t` [R\\_USB\\_ModuleNumberGet](#) (`usb_ctrl_t *const p_api_ctrl, uint8_t *module_number`)

This API gets the module number. [More...](#)

`fsp_err_t` [R\\_USB\\_ClassTypeGet](#) (`usb_ctrl_t *const p_api_ctrl, usb_class_t *class_type`)

This API gets the class type. [More...](#)

`fsp_err_t` [R\\_USB\\_DeviceAddressGet](#) (`usb_ctrl_t *const p_api_ctrl, uint8_t *device_address`)

This API gets the device address. [More...](#)

`fsp_err_t` [R\\_USB\\_PipeNumberGet](#) (`usb_ctrl_t *const p_api_ctrl, uint8_t *pipe_number`)

This API gets the pipe number. [More...](#)

`fsp_err_t R_USB_DeviceStateGet (usb_ctrl_t *const p_api_ctrl, uint16_t *state)`

This API gets the state of the device. [More...](#)

`fsp_err_t R_USB_DataSizeGet (usb_ctrl_t *const p_api_ctrl, uint32_t *data_size)`

This API gets the data size. [More...](#)

`fsp_err_t R_USB_SetupGet (usb_ctrl_t *const p_api_ctrl, usb_setup_t *setup)`

This API gets the setup type. [More...](#)

## Detailed Description

Driver for the USB peripheral on RA MCUs. This module implements the [USB Interface](#).

## Overview

The USB module operates in combination with the device class drivers provided by Renesas to form a complete USB stack.

## Features

The USB module has the following key features:

- USB Host mode
  - Enumerates Low/Full/High-speed devices (see note below)
  - Automatic transfer error determination and retry
- USB Peripheral mode
  - Supports USB1.1/2.0/3.0 hosts
- Automatic processing of device connect/disconnect, suspend/resume, and USB bus reset
- Up to 10 pipes
  - Control transfers supported on pipe 0
  - Data transfer on pipes 1 to 9 (Bulk or Interrupt)
- Functions with or without an RTOS

### Note

*Supported speeds are dependent on the MCU.*

## Configuration

### Build Time Configurations for r\_usb\_basic

The following build time configurations are defined in `fsp_cfg/r_usb_basic_cfg.h`:

Configuration	Options	Default	Description
Parameter Checking	<ul style="list-style-type: none"> <li>• Default (BSP)</li> <li>• Enabled</li> </ul>	Default (BSP)	If selected code for parameter checking is

	<ul style="list-style-type: none"> <li>• Disabled</li> </ul>		included in the build.
PLL Frequency	<ul style="list-style-type: none"> <li>• 24MHz</li> <li>• 20MHz</li> <li>• 12MHz</li> <li>• Other</li> </ul>	24MHz	Specify the PLL frequency supplied to the USB module. This setting only applies to USB1 (not USB0).
CPU Bus Access Wait Cycles	Refer to the RA Configuration tool for available options.	9 cycles	This setting controls the delay for consecutive USB peripheral register access. Set this value to a number of CPU cycles that is equivalent to 40.8ns or more.
Battery Charging	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Enabled	Specify whether or not to include battery charging functionality.
Power IC Shutdown Polarity	<ul style="list-style-type: none"> <li>• Active High</li> <li>• Active Low</li> </ul>	Active High	Select the polarity of the Shutdown signal on the power supply IC (if provided).
Dedicated Charging Port (DCP) Mode	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Disabled	When enabled, USB communication is disabled and the port is used for charging only.
Notifications for SET_INTERFACE/SET_FEATURE/CLEAR_FEATURE	<ul style="list-style-type: none"> <li>• Disabled</li> <li>• Enabled</li> </ul>	Enabled	When enabled, the application will receive notifications for SET_INTERFACE, SET_FEATURE and CLEAR_FEATURE messages.
Double Buffering	<ul style="list-style-type: none"> <li>• Disabled</li> <li>• Enabled</li> </ul>	Enabled	When enabled, the FIFOs for Pipes 1-5 are double-buffered.
Continuous Transfer Mode	<ul style="list-style-type: none"> <li>• Disabled</li> <li>• Enabled</li> </ul>	Disabled	Enable or disable continuous transfer mode.
DMA Support	<ul style="list-style-type: none"> <li>• Disable</li> <li>• Enable</li> </ul>	Disable	Enable or disable DMA support for the USB module.
DMA Source Address	<ul style="list-style-type: none"> <li>• DMA Disabled</li> <li>• FS Address</li> <li>• HS Address</li> </ul>	DMA Disabled	Set this to match the speed mode when DMA is enabled. Otherwise, set to 'DMA Disabled'.
DMA Destination Address	<ul style="list-style-type: none"> <li>• DMA Disabled</li> <li>• FS Address</li> </ul>	DMA Disabled	Set this to match the speed mode when DMA

- HS Address

is enabled. Otherwise, set to 'DMA Disabled'.

### Configurations for Middleware > USB > USB Driver on r\_usb\_basic

Configuration	Options	Default	Description
Name	Name must be a valid C symbol	g_basic0	Module name.
USB Mode	<ul style="list-style-type: none"> <li>• Host mode</li> <li>• Peri mode</li> </ul>	Host mode	Select the usb mode.
USB Speed	<ul style="list-style-type: none"> <li>• Full Speed</li> <li>• Hi Speed</li> <li>• Low Speed</li> </ul>	Full Speed	Select the USB speed.
USB Module Number	<ul style="list-style-type: none"> <li>• USB_IP0 Port</li> <li>• USB_IP1 Port</li> </ul>	USB_IP0 Port	Specify the USB module number to be used.
USB Device Class	<ul style="list-style-type: none"> <li>• Peripheral Communications Device Class</li> <li>• Peripheral Human Interface Device Class</li> <li>• Peripheral Mass Storage Class</li> <li>• Peripheral Vendor-defined Class</li> <li>• Host Communications Device Class</li> <li>• Host Human Interface Device Class</li> <li>• Host Mass Storage Class</li> <li>• Host Vendor-defined Class</li> </ul>	Peripheral Communications Device Class	Select the USB device class.
USB Descriptor	USB Descriptor must be a valid C symbol.	g_usb_descriptor	Enter the name of the descriptor to be used. For how to create a descriptor structure, refer to the Descriptor definition chapter in the usb_basic manual. Specify NULL when using the Host class.
USB Compliance Callback	Compliance Callback must be a valid C symbol.	NULL	Set the callback for compliance tests here.



USBFS Interrupt Priority	MCU Specific Options		Select the interrupt priority used by the main USBFS ISR.
USBFS Resume Priority	MCU Specific Options		Select the interrupt priority used by the USBFS Resume ISR.
USBFS D0FIFO Interrupt Priority	MCU Specific Options		Select the interrupt priority used by the USBFS D0FIFO.
USBFS D1FIFO Interrupt Priority	MCU Specific Options		Select the interrupt priority used by the USBFS D1FIFO.
USBHS Interrupt Priority	MCU Specific Options		Select the interrupt priority used by the main USBHS ISR.
USBHS D0FIFO Interrupt Priority	MCU Specific Options		Select the interrupt priority used by the USBHS D0FIFO ISR.
USBHS D1FIFO Interrupt Priority	MCU Specific Options		Select the interrupt priority used by the USBHS D1FIFO ISR.
USB RTOS Callback	Enter the address of the function.	NULL	If an RTOS is used, set the callback function here.
USB Callback Context	Enter the address of the context.	NULL	If an RTOS is used, set the callback context here.

## Clock Configuration

The USB module uses PLL as the clock source. The PLL frequency can be set in the **Clocks** tab of the configuration editor or by using the CGC Interface at run-time.

## Pin Configuration

In peripheral mode the USB\_VBUS and/or USBHS\_VBUS pins are used to detect the USB connection status (connected or disconnected) and should be connected to the USB VBUS signal.

*Note*

*USB\_VBUS and USBHS\_VBUS are 5V-tolerant pins.*

In host mode the USBHS\_VBUSEN, USBHS\_OVRCURA and USBHS\_OVRCURB pins should be connected to the relevant pins of an external power supply IC, if available. These pins will be used to manage the USB VBUS supply.

## DMA Configuration

When using DMA with USB the following properties must be configured for each DMAC module:

Config Name	Select Name	Description
-------------	-------------	-------------

Transfer Size	2 Bytes 4 Bytes	In FS mode, select "2 Bytes" In HS mode, select "4 Bytes"
Activation source	USBFS FIFO 0 USBFS FIFO 1 USBHS FIFO 0 USBHS FIFO 1	USB FS Reception USB FS Transmission USB HS Reception USB HS Transmission

## Descriptor definition

In Peripheral mode, the `usb_descriptor_t` structure stores descriptor information including the device and configuration descriptors. The values set in this structure are sent to the USB host as part of enumeration.

```
typedef struct usb_descriptor
{
    uint8_t *p_device;    /* Pointer to device descriptor */
    uint8_t *p_config_f; /* Pointer to full-speed configuration descriptor */
    uint8_t *p_config_h; /* Pointer to high-speed configuration descriptor (HS only)
*/
    uint8_t *p_qualifier; /* Pointer to device qualifier descriptor (HS only) */
    uint8_t **pp_string; /* Pointer to string descriptor table */
    uint8_t num_string;  /* Number of strings in table */
} usb_descriptor_t;
```

### Note

*Even in high-speed mode the full-speed configuration must be made available:*

```
/* Example USB FS descriptor struct */
usb_descriptor_t g_usb_descriptor =
{
    smp_device,
    smp_config_f,
    NULL,
    NULL,
    smp_str_table,
    3,
};

/* Example USB HS descriptor struct */
usb_descriptor_t g_usb_descriptor =
```

```
{  
    smp_device,  
    smp_config_f,  
    smp_config_h,  
    smp_qualifier,  
    smp_str_table,  
    3,  
};
```

## String Descriptor

This USB driver requires string descriptors to be registered in the string descriptor table. Use the following format to define the elements:

```
/* String descriptor 0 is reserved for language ID information */  
uint8_t str_descriptor_0[]  
{  
    0x04,      /* Length */  
    0x03,      /* Descriptor type */  
    0x09, 0x04 /* Language ID */  
};  
uint8_t str_descriptor_manufacturer[] =  
{  
    0x10,      /* Length */  
    0x03,      /* Descriptor type */  
    'R', 0x00,  
    'E', 0x00,  
    'N', 0x00,  
    'E', 0x00,  
    'S', 0x00,  
    'A', 0x00,  
    'S', 0x00  
};  
uint8_t str_descriptor_product[] =  
{
```

```
    0x12,      /* Length */
    0x03,      /* Descriptor type */
    'C', 0x00,
    'D', 0x00,
    'C', 0x00,
    '_', 0x00,
    'D', 0x00,
    'E', 0x00,
    'M', 0x00,
    'O', 0x00
};
/* String descriptor table */
uint8_t * smp_str_table[] =
{
    str_descriptor_0,      /* Index: 0 */
    str_descriptor_manufacturer, /* Index: 1 */
    str_descriptor_product, /* Index: 2 */
};
```

#### Note

Set the string index values in the device/configuration descriptors (*iManufacturer*, *iConfiguration* etc.) to the index of the desired string in the string descriptor table. For example, in the table below, the manufacturer is described in *str\_descriptor\_manufacturer* and the value of *iManufacturer* in the device descriptor is **1**.

## Other Descriptors

Refer to the Universal Serial Bus Revision 2.0 specification (<http://www.usb.org/developers/docs/>) for details on how to construct the device, configuration and qualifier descriptors.

## Usage Notes

### Program Structure

USB applications (whether using an RTOS or not) should be written as an event-handling loop. Either a callback function (RTOS only) or `R_USB_EventGet` should be used to provide event data to the application loop where a switch statement handles the event.

#### Note

The `USB_STATUS_CONFIGURED` event should be confirmed before calling `R_USB_Read` or `R_USB_Write`.

### Limitations

Developers should be aware of the following limitations when using the USB driver:

- The current USB driver does not support hub.
- In USB host mode, the module does not support suspend during data transfers. Execute suspend only after confirming that all transfers are complete.
- Multiconfigurations are not supported.
- This driver does not support CPU transfers using the D0FIFO/D1FIFO register.
- Only one device-class driver may be used at a time.
- The USB Hi-Speed module only supports Hi-Speed operation.
- In USB host mode, this USB driver does not support the composite device.
- The user can not specify DMA transfer to USB IP0 and IP1 modules at the same time when using USB multi-port feature. USB multi-port function: Simultaneous operation feature of USB Host and Peripheral.

## TrustZone

The USB driver for FreeRTOS cannot be allocated in Secure region.

## UCLK setting

Enable UCLK in "Clocks" tab on e2 studio when using the following MCU.

1. RA6M4

# Examples

## USB Basic Example

This is a basic example of minimal use of the USB in an application.

```
void usb_basic_example (void)
{
    usb_event_info_t event_info;
    usb_status_t     event;

    g_usb_on_usb.open(&g_basic0_ctrl, &g_basic0_cfg);
    /* Loop back between PC(TerminalSoft) and USB MCU */
    while (1)
    {
        g_usb_on_usb.eventGet(&event_info, &event);
        switch (event)
        {
            case USB_STATUS_CONFIGURED:
            case USB_STATUS_WRITE_COMPLETE:
                g_usb_on_usb.read(&g_basic0_ctrl, g_buf, DATA_LEN, USB_CLASS_PCDC);
                break;
        }
    }
}
```

```
case USB_STATUS_READ_COMPLETE:
    g_usb_on_usb.write(&g_basic0_ctrl, g_buf, event_info.data_size,
USB_CLASS_PCDC);
    break;
case USB_STATUS_REQUEST: /* Receive Class Request */
    if (USB_PCDC_SET_LINE_CODING == (event_info.setup.request_type & USB_BREQUEST))
        {
            g_usb_on_usb.periControlDataGet(&g_basic0_ctrl, (uint8_t *)
&g_line_coding, LINE_CODING_LENGTH);
        }
    else if (USB_PCDC_GET_LINE_CODING == (event_info.setup.request_type & USB_BREQUEST))
        {
            g_usb_on_usb.periControlDataSet(&g_basic0_ctrl, (uint8_t *)
&g_line_coding, LINE_CODING_LENGTH);
        }
    else
        {
            g_usb_on_usb.periControlStatusSet(&g_basic0_ctrl,
USB_SETUP_STATUS_ACK);
        }
    break;
case USB_STATUS_SUSPEND:
case USB_STATUS_DETACH:
    break;
default:
    break;
}
}
} /* End of function usb_main() */
```

## Typedefs

```
typedef usb_event_info_t usb_instance_ctrl_t
```

## Typedef Documentation

◆ **usb\_instance\_ctrl\_t**

```
typedef usb_event_info_t usb_instance_ctrl_t
```

ICU private control block. DO NOT MODIFY. Initialization occurs when R\_ICU\_ExternalIrqOpen is called.

**Function Documentation**◆ **R\_USB\_Open()**

```
fsp_err_t R_USB_Open ( usb_ctrl_t *const p_api_ctrl, usb_cfg_t const *const p_cfg )
```

Applies power to the USB module specified in the argument (p\_ctrl).

**Return values**

FSP_SUCCESS	Success in open.
FSP_ERR_USB_BUSY	Specified USB module now in use.
FSP_ERR_ASSERTION	Parameter is NULL error.
FSP_ERR_USB_FAILED	The function could not be completed successfully.
FSP_ERR_USB_PARAMETER	Parameter error.

**Note**

*Do not call this API in the following function.*

*(1). Interrupt function.*

*(2). Callback function ( for RTOS ).*

◆ **R\_USB\_Close()**

```
fsp_err_t R_USB_Close ( usb_ctrl_t *const p_api_ctrl)
```

Terminates power to the USB module specified in argument (p\_ctrl). USB0 module stops when USB\_IP0 is specified to the member (module), USB1 module stops when USB\_IP1 is specified to the member (module).

**Return values**

FSP_SUCCESS	Success.
FSP_ERR_USB_FAILED	The function could not be completed successfully.
FSP_ERR_USB_NOT_OPEN	USB module is not open.
FSP_ERR_ASSERTION	Parameter is NULL error.
FSP_ERR_USB_PARAMETER	Parameter error.

**Note**

*Do not call this API in the following function.*

*(1). Interrupt function.*

*(2). Callback function ( for RTOS ).*



◆ **R\_USB\_Read()**

```
fsp_err_t R_USB_Read ( usb_ctrl_t *const p_api_ctrl, uint8_t * p_buf, uint32_t size, uint8_t destination )
```

Bulk/interrupt data transfer and control data transfer.

## 1. Bulk/interrupt data transfer

Requests USB data read (bulk/interrupt transfer). The read data is stored in the area specified by argument (p\_buf). After data read is completed, confirm the operation by checking the return value (USB\_STATUS\_READ\_COMPLETE) of the R\_USB\_GetEvent function. The received data size is set in member (size) of the usb\_ctrl\_t structure. To figure out the size of the data when a read is complete, check the return value (USB\_STATUS\_READ\_COMPLETE) of the R\_USB\_GetEvent function, and then refer to the member (size) of the usb\_ctrl\_t structure.

## 2. Control data transfer

The R\_USB\_Read function is used to receive data in the data stage and the R\_USB\_Write function is used to send data to the USB host.

**Return values**

FSP_SUCCESS	Successfully completed (Data read request completed).
FSP_ERR_USB_FAILED	The function could not be completed successfully.
FSP_ERR_USB_BUSY	Data receive request already in process for USB device with same device address.
FSP_ERR_ASSERTION	Parameter is NULL error.
FSP_ERR_USB_PARAMETER	Parameter error.

**Note**

*The address specified in the argument p\_buf must be 4-byte aligned.*

*Do not call this API in the following function.*

*(1). Interrupt function.*

*(2). Callback function ( for RTOS ).*

## ◆ R\_USB\_Write()

```
fsp_err_t R_USB_Write ( usb_ctrl_t *const p_api_ctrl, uint8_t const *const p_buf, uint32_t size,
uint8_t destination )
```

Bulk/Interrupt data transfer and control data transfer.

### 1. Bulk/Interrupt data transfer

Requests USB data write (bulk/interrupt transfer). Stores write data in area specified by argument (p\_buf). Set the device class type in usb\_ctrl\_t structure member (type). Confirm after data write is completed by checking the return value (USB\_STATUS\_WRITE\_COMPLETE) of the R\_USB\_GetEvent function. To request the transmission of a NULL packet, assign **USB\_NULL(0)** to the third argument (size).

### 2. Control data transfer

The R\_USB\_Read function is used to receive data in the data stage and the R\_USB\_Write function is used to send data to the USB host.

## Return values

FSP_SUCCESS	Successfully completed. (Data write request completed)
FSP_ERR_USB_FAILED	The function could not be completed successfully.
FSP_ERR_USB_BUSY	Data write request already in process for USB device with same device address.
FSP_ERR_ASSERTION	Parameter is NULL error.
FSP_ERR_USB_PARAMETER	Parameter error.

## Note

*The address specified in the argument p\_buf must be 4-byte aligned.*

*Do not call this API in the following function.*

*(1). Interrupt function.*

*(2). Callback function ( for RTOS ).*

◆ **R\_USB\_Stop()**

```
fsp_err_t R_USB_Stop ( usb_ctrl_t *const p_api_ctrl, usb_transfer_t direction, uint8_t destination )
```

Requests a data read/write transfer be terminated when a data read/write transfer is being performed.

To stop a data read, set USB\_TRANSFER\_READ as the argument (type); to stop a data write, specify USB\_WRITE as the argument (type).

**Return values**

FSP_SUCCESS	Successfully completed. (stop completed)
FSP_ERR_USB_FAILED	The function could not be completed successfully.
FSP_ERR_ASSERTION	Parameter is NULL error.
FSP_ERR_USB_BUSY	Stop processing is called multiple times.
FSP_ERR_USB_PARAMETER	Parameter error.

**Note**

Do not call this API in the following function.

- (1). Interrupt function.
- (2). Callback function ( for RTOS ).

◆ **R\_USB\_Suspend()**

```
fsp_err_t R_USB_Suspend ( usb_ctrl_t *const p_api_ctrl)
```

Sends a SUSPEND signal from the USB module assigned to the member (module) of the usb\_ctrl\_t structure.

After the suspend request is completed, confirm the operation with the return value (USB\_STATUS\_SUSPEND) of the R\_USB\_EventGet function.

**Return values**

FSP_SUCCESS	Successfully completed.
FSP_ERR_USB_FAILED	The function could not be completed successfully.
FSP_ERR_USB_BUSY	During a suspend request to the specified USB module, or when the USB module is already in the suspended state.
FSP_ERR_ASSERTION	Parameter is NULL error.
FSP_ERR_USB_PARAMETER	Parameter error.

**Note**

Do not call this API in the following function.

- (1). Interrupt function.
- (2). Callback function ( for RTOS ).

◆ **R\_USB\_Resume()**

```
fsp_err_t R_USB_Resume ( usb_ctrl_t *const p_api_ctrl)
```

Sends a RESUME signal from the USB module assigned to the member (module) of the usb\_ctrl\_t structure.

After the resume request is completed, confirm the operation with the return value (USB\_STATUS\_RESUME) of the R\_USB\_EventGet function

**Return values**

FSP_SUCCESS	Successfully completed.
FSP_ERR_USB_FAILED	The function could not be completed successfully.
FSP_ERR_USB_BUSY	Resume already requested for same device address. (USB host mode only)
FSP_ERR_USB_NOT_SUSPEND	USB device is not in the SUSPEND state.
FSP_ERR_ASSERTION	Parameter is NULL error.
FSP_ERR_USB_PARAMETER	Parameter error.

**Note**

Do not call this API in the following function.

(1). Interrupt function.

(2). Callback function ( for RTOS ).

◆ **R\_USB\_VbusSet()**

```
fsp_err_t R_USB_VbusSet ( usb_ctrl_t *const p_api_ctrl, uint16_t state )
```

Specifies starting or stopping the VBUS supply.

**Return values**

FSP_SUCCESS	Successful completion. (VBUS supply start/stop completed)
FSP_ERR_USB_FAILED	The function could not be completed successfully.
FSP_ERR_ASSERTION	Parameter is NULL error.
FSP_ERR_USB_PARAMETER	Parameter error.

**Note**

Do not call this API in the following function.

(1). Interrupt function.

(2). Callback function ( for RTOS ).

◆ **R\_USB\_InfoGet()**

```
fsp_err_t R_USB_InfoGet ( usb_ctrl_t *const p_api_ctrl, usb_info_t * p_info, uint8_t destination )
```

Obtains completed USB-related events.

**Return values**

FSP_SUCCESS	Successful completion. (VBUS supply start/stop completed)
FSP_ERR_ASSERTION	Parameter is NULL error.
FSP_ERR_USB_FAILED	The function could not be completed successfully.
FSP_ERR_USB_PARAMETER	Parameter error.

◆ **R\_USB\_PipeRead()**

```
fsp_err_t R_USB_PipeRead ( usb_ctrl_t *const p_api_ctrl, uint8_t * p_buf, uint32_t size, uint8_t pipe_number )
```

Requests a data read (bulk/interrupt transfer) via the pipe specified in the argument.

The read data is stored in the area specified in the argument (p\_buf). After the data read is completed, confirm the operation with the R\_USB\_GetEvent function return value(USB\_STATUS\_READ\_COMPLETE). To figure out the size of the data when a read is complete, check the return value (USB\_STATUS\_READ\_COMPLETE) of the R\_USB\_GetEvent function, and then refer to the member (size) of the usb\_ctrl\_t structure.

**Return values**

FSP_SUCCESS	Successfully completed.
FSP_ERR_USB_BUSY	Specified pipe now handling data receive/send request.
FSP_ERR_USB_FAILED	The function could not be completed successfully.
FSP_ERR_ASSERTION	Parameter is NULL error.
FSP_ERR_USB_PARAMETER	Parameter error.

**Note**

The address specified in the argument p\_buf must be 4-byte aligned.

Do not call this API in the following function.

- (1). Interrupt function.
- (2). Callback function ( for RTOS ).

◆ **R\_USB\_PipeWrite()**

```
fsp_err_t R_USB_PipeWrite ( usb_ctrl_t *const p_api_ctrl, uint8_t * p_buf, uint32_t size, uint8_t pipe_number )
```

Requests a data write (bulk/interrupt transfer).

The write data is stored in the area specified in the argument (p\_buf). After data write is completed, confirm the operation with the return value (USB\_STATUS\_WRITE\_COMPLETE) of the EventGet function. To request the transmission of a NULL packet, assign USB\_NULL (0) to the third argument (size).

**Return values**

FSP_SUCCESS	Successfully completed.
FSP_ERR_USB_BUSY	Specified pipe now handling data receive/send request.
FSP_ERR_USB_FAILED	The function could not be completed successfully.
FSP_ERR_ASSERTION	Parameter is NULL error.
FSP_ERR_USB_PARAMETER	Parameter error.

**Note**

The address specified in the argument p\_buf must be 4-byte aligned.

Do not call this API in the following function.

(1). Interrupt function.

(2). Callback function ( for RTOS ).

◆ **R\_USB\_PipeStop()**

```
fsp_err_t R_USB_PipeStop ( usb_ctrl_t *const p_api_ctrl, uint8_t pipe_number )
```

Terminates a data read/write operation.

**Return values**

FSP_SUCCESS	Successfully completed. (Stop request completed)
FSP_ERR_USB_FAILED	The function could not be completed successfully.
FSP_ERR_ASSERTION	Parameter is NULL error.
FSP_ERR_USB_PARAMETER	Parameter error.

**Note**

Do not call this API in the following function.

(1). Interrupt function.

(2). Callback function ( for RTOS ).

### ◆ R\_USB\_UsedPipesGet()

```
fsp_err_t R_USB_UsedPipesGet ( usb_ctrl_t *const p_api_ctrl, uint16_t * p_pipe, uint8_t destination )
```

Gets the selected pipe number (number of the pipe that has completed initialization) via bit map information.

The bit map information is stored in the area specified in argument (p\_pipe). Based on the information (module member and address member) assigned to the usb\_ctrl\_t structure, obtains the PIPE information of that USB device.

#### Return values

FSP_SUCCESS	Successfully completed.
FSP_ERR_USB_FAILED	The function could not be completed successfully.
FSP_ERR_ASSERTION	Parameter is NULL error.
FSP_ERR_USB_PARAMETER	Parameter error.

### ◆ R\_USB\_PipeInfoGet()

```
fsp_err_t R_USB_PipeInfoGet ( usb_ctrl_t *const p_api_ctrl, usb_pipe_t * p_info, uint8_t pipe_number )
```

Gets the following pipe information regarding the pipe specified in the argument (p\_ctrl) member (pipe): endpoint number, transfer type, transfer direction and maximum packet size.

The obtained pipe information is stored in the area specified in the argument (p\_info).

#### Return values

FSP_SUCCESS	Successfully completed.
FSP_ERR_USB_FAILED	The function could not be completed successfully.
FSP_ERR_ASSERTION	Parameter is NULL error.
FSP_ERR_USB_PARAMETER	Parameter error.

◆ **R\_USB\_PullUp()**

```
fsp_err_t R_USB_PullUp ( usb_ctrl_t *const p_api_ctrl, uint8_t state )
```

This API enables or disables pull-up of D+/D- line.

**Return values**

FSP_SUCCESS	Successful completion. (Pull-up enable/disable setting completed)
FSP_ERR_USB_FAILED	The function could not be completed successfully.
FSP_ERR_ASSERTION	Parameter is NULL error.
FSP_ERR_USB_PARAMETER	Parameter error.

**Note**

Do not call this API in the following function.

(1). Interrupt function.

(2). Callback function ( for RTOS ).

◆ **R\_USB\_EventGet()**

```
fsp_err_t R_USB_EventGet ( usb_ctrl_t *const p_api_ctrl, usb_status_t * event )
```

Obtains completed USB related events. (OS-less Only)

In USB host mode, the device address value of the USB device that completed an event is specified in the `usb_ctrl_t` structure member (address) specified by the event's argument. In USB peripheral mode, `USB_NULL` is specified in member (address). If this function is called in the RTOS execution environment, a failure is returned.

**Return values**

FSP_SUCCESS	Event Get Success.
FSP_ERR_USB_FAILED	If called in the RTOS environment, an error is returned.

**Note**

Do not use the same variable as the first argument of `R_USB_Open` for the first argument.

Do not call this API in the interrupt function.



◆ **R\_USB\_VersionGet()**

```
fsp_err_t R_USB_VersionGet ( fsp_version_t *const p_version)
```

Returns the version of this module.

The version number is encoded such that the top two bytes are the major version number and the bottom two bytes are the minor version number.

**Return values**

FSP_SUCCESS	Success.
FSP_ERR_ASSERTION	Failed in acquiring version information.

◆ **R\_USB\_Callback()**

```
fsp_err_t R_USB_Callback ( usb_callback_t * p_callback)
```

Register a callback function to be called upon completion of a USB related event. (RTOS only)

This function registers a callback function to be called when a USB-related event has completed. If this function is called in the OS-less execution environment, a failure is returned.

**Return values**

FSP_SUCCESS	Successfully completed.
FSP_ERR_USB_FAILED	If this function is called in the OS-less execution environment, a failure is returned.
FSP_ERR_ASSERTION	Parameter is NULL error.

**Note**

*Do not call this API in the interrupt function.*

◆ **R\_USB\_HostControlTransfer()**

```
fsp_err_t R_USB_HostControlTransfer ( usb_ctrl_t *const p_api_ctrl, usb_setup_t * p_setup, uint8_t * p_buf, uint8_t device_address )
```

Performs settings and transmission processing when transmitting a setup packet.

**Return values**

FSP_SUCCESS	Successful completion.
FSP_ERR_USB_FAILED	The function could not be completed successfully.
FSP_ERR_ASSERTION	Parameter is NULL error.
FSP_ERR_USB_PARAMETER	Parameter error.
FSP_ERR_USB_BUSY	Specified pipe now handling data receive/send request.

**Note**

The address specified in the argument *p\_buf* must be 4-byte aligned.

Do not call this API in the following function.

(1). Interrupt function.

(2). Callback function ( for RTOS ).

◆ **R\_USB\_PeriControlDataGet()**

```
fsp_err_t R_USB_PeriControlDataGet ( usb_ctrl_t *const p_api_ctrl, uint8_t * p_buf, uint32_t size )
```

Receives data sent by control transfer.

**Return values**

FSP_SUCCESS	Successful completion.
FSP_ERR_USB_FAILED	The function could not be completed successfully.
FSP_ERR_ASSERTION	Parameter is NULL error.
FSP_ERR_USB_BUSY	Specified pipe now handling data receive/send request.
FSP_ERR_USB_PARAMETER	Parameter error.

**Note**

The address specified in the argument *p\_buf* must be 4-byte aligned.

Do not call this API in the following function.

(1). Interrupt function.

(2). Callback function ( for RTOS ).

◆ **R\_USB\_PeriControlDataSet()**

```
fsp_err_t R_USB_PeriControlDataSet ( usb_ctrl_t *const p_api_ctrl, uint8_t * p_buf, uint32_t size )
```

Performs transfer processing for control transfer.

**Return values**

FSP_SUCCESS	Successful completion.
FSP_ERR_USB_FAILED	The function could not be completed successfully.
FSP_ERR_ASSERTION	Parameter is NULL error.
FSP_ERR_USB_BUSY	Specified pipe now handling data receive/send request.
FSP_ERR_USB_PARAMETER	Parameter error.

**Note**

The address specified in the argument *p\_buf* must be 4-byte aligned.

Do not call this API in the following function.

(1). Interrupt function.

(2). Callback function ( for RTOS ).

◆ **R\_USB\_PeriControlStatusSet()**

```
fsp_err_t R_USB_PeriControlStatusSet ( usb_ctrl_t *const p_api_ctrl, usb_setup_status_t status )
```

Set the response to the setup packet.

**Return values**

FSP_SUCCESS	Successful completion.
FSP_ERR_USB_FAILED	The function could not be completed successfully.
FSP_ERR_ASSERTION	Parameter is NULL error.

**Note**

Do not call this API in the following function.

(1). Interrupt function.

(2). Callback function ( for RTOS ).

◆ **R\_USB\_RemoteWakeup()**

```
fsp_err_t R_USB_RemoteWakeup ( usb_ctrl_t *const p_api_ctrl)
```

Sends a remote wake-up signal to the connected Host.

**Return values**

FSP_SUCCESS	Successful completion.
FSP_ERR_USB_FAILED	The function could not be completed successfully.
FSP_ERR_ASSERTION	Parameter is NULL error.
FSP_ERR_USB_NOT_SUSPEND	Device is not suspended.
FSP_ERR_USB_BUSY	The device is in resume operation.

**Note**

Do not call this API in the following function.

(1). Interrupt function.

(2). Callback function ( for RTOS ).

◆ **R\_USB\_ModuleNumberGet()**

```
fsp_err_t R_USB_ModuleNumberGet ( usb_ctrl_t *const p_api_ctrl, uint8_t * module_number )
```

This API gets the module number.

**Return values**

FSP_SUCCESS	Successful completion.
-------------	------------------------

◆ **R\_USB\_ClassTypeGet()**

```
fsp_err_t R_USB_ClassTypeGet ( usb_ctrl_t *const p_api_ctrl, usb_class_t * class_type )
```

This API gets the class type.

**Return values**

FSP_SUCCESS	Successful completion.
-------------	------------------------

◆ **R\_USB\_DeviceAddressGet()**

```
fsp_err_t R_USB_DeviceAddressGet ( usb_ctrl_t*const p_api_ctrl, uint8_t* device_address )
```

This API gets the device address.

**Return values**

FSP_SUCCESS	Successful completion.
-------------	------------------------

◆ **R\_USB\_PipeNumberGet()**

```
fsp_err_t R_USB_PipeNumberGet ( usb_ctrl_t*const p_api_ctrl, uint8_t* pipe_number )
```

This API gets the pipe number.

**Return values**

FSP_SUCCESS	Successful completion.
-------------	------------------------

◆ **R\_USB\_DeviceStateGet()**

```
fsp_err_t R_USB_DeviceStateGet ( usb_ctrl_t*const p_api_ctrl, uint16_t* state )
```

This API gets the state of the device.

**Return values**

FSP_SUCCESS	Successful completion.
-------------	------------------------

◆ **R\_USB\_DataSizeGet()**

```
fsp_err_t R_USB_DataSizeGet ( usb_ctrl_t*const p_api_ctrl, uint32_t* data_size )
```

This API gets the data size.

**Return values**

FSP_SUCCESS	Successful completion.
-------------	------------------------

**◆ R\_USB\_SetupGet()**

```
fsp_err_t R_USB_SetupGet ( usb_ctrl_t *const p_api_ctrl, usb_setup_t * setup )
```

This API gets the setup type.

**Return values**

FSP_SUCCESS	Successful completion.
-------------	------------------------

**4.2.49 USB Host Communications Device Class Driver (r\_usb\_hcdc)****Modules**

This module provides a USB Host Communications Device Class (HDCD) driver. It implements the [USB HDCD Interface](#).

**Functions**

Refer to [USB \(r\\_usb\\_basic\)](#) for the common API (r\_usb\_basic) to be called from the application.

**Detailed Description****Overview**

The r\_usb\_hcdc module, when used in combination with the r\_usb\_basic module, operates as a USB Host Communications Device Class (HDCD) driver. The HDCD conforms to the PSTN device subclass abstract control model of the USB Communications Device Class (CDC) specification and enables communication with a CDC peripheral device.

**Features**

The r\_usb\_hcdc module has the following key features:

- Checks for connected devices
- Implementation of communication line settings
- Acquisition of the communication line state
- Data transfer to and from a CDC peripheral device

**Configuration****Build Time Configurations for r\_usb\_hcdc**

The following build time configurations are defined in fsp\_cfg/r\_usb\_hcdc\_cfg.h:

Configuration	Options	Default	Description
---------------	---------	---------	-------------

Target Peripheral Device Class ID	<ul style="list-style-type: none"> <li>• CDC class supported device</li> <li>• Vendor class device</li> </ul>	CDC class supported device	Specify the device class ID of the CDC device to be connected.
Bulk Input Transfer Pipe	<ul style="list-style-type: none"> <li>• USB PIPE1</li> <li>• USB PIPE2</li> <li>• USB PIPE3</li> <li>• USB PIPE4</li> <li>• USB PIPE5</li> </ul>	USB PIPE1	Select the USB pipe to use for bulk input transfers.
Bulk Output Transfer Pipe	<ul style="list-style-type: none"> <li>• USB PIPE1</li> <li>• USB PIPE2</li> <li>• USB PIPE3</li> <li>• USB PIPE4</li> <li>• USB PIPE5</li> </ul>	USB PIPE2	Select the USB pipe to use for bulk output transfers.
Interrupt In Pipe	<ul style="list-style-type: none"> <li>• USB PIPE6</li> <li>• USB PIPE7</li> <li>• USB PIPE8</li> <li>• USB PIPE9</li> </ul>	USB PIPE6	Select the USB pipe to use for interrupts.

### Configurations for Middleware > USB > USB HCDC driver on r\_usb\_hcdc

This module can be added to the Stacks tab via New Stack > Middleware > USB > USB HCDC driver on r\_usb\_hcdc.

Configuration	Options	Default	Description
Name	Name must be a valid C symbol	g_hcdc0	Module name.

#### Note

Refer to the [USB \(r\\_usb\\_basic\)](#) module for hardware configuration options.

### Clock Configuration

Refer to the [USB \(r\\_usb\\_basic\)](#) module.

### Pin Configuration

Refer to the [USB \(r\\_usb\\_basic\)](#) module.

## Usage Notes

### Communications Device Class (CDC), PSTN and ACM

This software conforms to the Abstract Control Model (ACM) subclass of the Communications Device Class specification as defined in the "USB Communications Class Subclass Specification for PSTN Devices", Revision 1.2. The Abstract Control Model subclass is a technology that bridges the gap between USB devices and earlier modems (employing RS-232C connections) enabling use of application programs designed for older modems.

### Basic Functions

The main functions of H CDC are the following:

- Verify connected devices
- Make communication line settings
- Acquire the communication line state
- Transfer data to and from the CDC peripheral device

### Abstract Control Model Class Requests - Host to Device

This driver supports the following class requests:

Request	Code	Description
SendEncapsulatedCommand	0x00	Transmits an AT command as defined by the protocol used by the device (normally 0 for USB).
GetEncapsulatedResponse	0x01	Requests a response to a command transmitted by SendEncapsulatedCommand.
SetCommFeature	0x02	Enables or disables features such as device-specific 2-byte code and country setting.
GetCommFeature	0x03	Acquires the enabled/disabled state of features such as device-specific 2-byte code and country setting.
ClearCommFeature	0x04	Restores the default enabled/disabled settings of features such as device-specific 2-byte code and country setting.
SetLineCoding	0x20	Makes communication line settings (communication speed, data length, parity bit, and stop bit length).
GetLineCoding	0x21	Acquires the communication line setting state.
SetControlLineState	0x22	Makes communication line control signal (RTS, DTR) settings.
SendBreak	0x23	Transmits a break signal.

#### Note

*For more information about Abstract Control Model requests, refer to Table 11 "Requests - Abstract Control Model" in the "USB Communications Class Subclass Specification for PSTN Devices", Revision 1.2.*

The expected data format for each command is shown below followed by dependent structures.

bmRequestTyp	bRequest	wValue	wIndex	wLength	Data
--------------	----------	--------	--------	---------	------



e					
0x21	SEND_ENCAPSULATED_COMMAND (0x00)	0x0000	0x0000	Data length	usb_hcdc_encapsulated_t
0x21	GET_ENCAPSULATED_RESPONSE (0x01)	0x0000	0x0000	Data length	usb_hcdc_encapsulated_t
0x21	SET_COMM_FEATURE (0x02)	usb_hcdc_feature_selector_t	0x0000	Data length	usb_hcdc_comfeature_t
0x21	GET_COMM_FEATURE (0x03)	usb_hcdc_feature_selector_t	0x0000	Data length	usb_hcdc_comfeature_t
0x21	CLEAR_COMM_FEATURE (0x04)	usb_hcdc_feature_selector_t	0x0000	Data length	None
0x21	SET_LINE_CODING (0x20)	0x0000	0x0000	0x0000	usb_hcdc_linecoding_t
0xA1	GET_LINE_CODING (0x21)	0x0000	0x0000	0x0007	usb_hcdc_linecoding_t
0x21	SET_CONTROL_LINE_STATE (0x22)	usb_hcdc_control_line_state_t	0x0000	0x0000	None
0x21	SEND_BREAK (0x23)	usb_hcdc_break_duration_t	0x0000	0x0000	None

### ACM Notifications from Device to Host

The following class notifications are supported:

Notification	Code	Description
RESPONSE_AVAILABLE	0x01	Response to GET_ENCAPSULATED_RESPONSE
SERIAL_STATE	0x20	Notification of serial line state

The data types returned are as follows:

bmRequestType	bRequest	wValue	wIndex	wLength	Data
0xA1	RESPONSE_AVAILABLE (0x01)	0x0000	0x0000	0x0000	None
0xA1	SERIAL_STATE (0x20)	0x0000	0x0000	0x0002	usb_hcdc_serialstate_t

#### Note

The host is notified with SERIAL\_STATE whenever a change in the UART port state is detected.

## Limitations

This driver is subject to the following limitations:

- Suspend is not supported when a data transfer is in progress. Confirm that data transfer has completed before executing suspend.
- Use of compound USB devices with CDC class support is not supported.
- This module must be incorporated into a project using r\_usb\_basic and does not provide any public APIs.
- This driver does not support Low-speed.

## Examples

### USB HCDC Loopback Example

The main functions of the HCDC loopback example are as follows:

1. Virtual UART control settings are configured by transmitting the class request SET\_LINE\_CODING to the CDC device.
2. Sends receive (Bulk In transfer) requests to a CDC peripheral device and receives data.
3. Loops received data back to the peripheral by means of Bulk Out transfers.

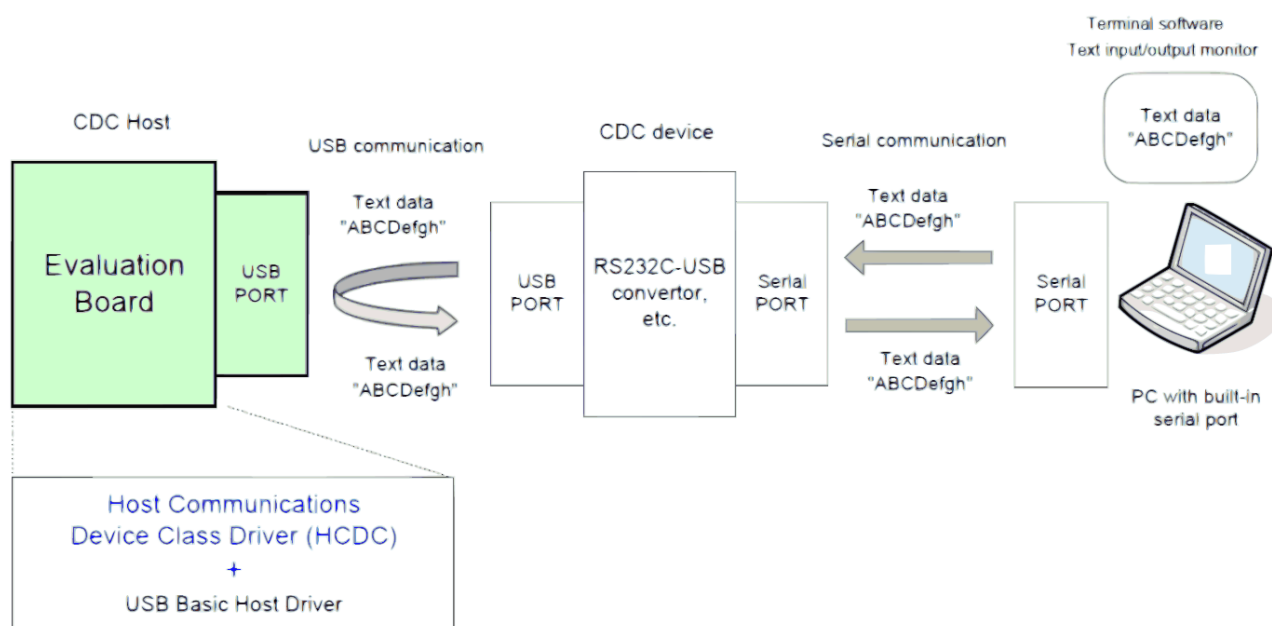


Figure 170: Data Transfer (Loopback)

The main loop performs loopback processing in which data received from a CDC peripheral device is transmitted unaltered back to the peripheral.

```
#define SET_LINE_CODING (USB_CDC_SET_LINE_CODING | USB_HOST_TO_DEV | USB_CLASS |
USB_INTERFACE)

#define GET_LINE_CODING (USB_CDC_GET_LINE_CODING | USB_DEV_TO_HOST | USB_CLASS |
```

```
USB_INTERFACE)

#define SET_CONTROL_LINE_STATE (USB_CDC_SET_CONTROL_LINE_STATE | USB_HOST_TO_DEV |
USB_CLASS | USB_INTERFACE)

#define COM_SPEED (9600U)

#define COM_DATA_BIT (8U)

#define COM_STOP_BIT (0)

#define COM_PARITY_BIT (0)

#define LINE_CODING_LENGTH (7)

void usb_basic_example (void)
{
    usb_status_t    event;

    usb_event_info_t event_info;

    g_usb_on_usb.open(&g_basic0_ctrl, &g_basic0_cfg);

    while (1)
    {
        /* Get USB event data */
        g_usb_on_usb.eventGet(&event_info, &event);

        /* Handle the received event (if any) */
        switch (event)
        {
            case USB_STATUS_CONFIGURED:
                /* Configure virtual UART settings */
                set_line_coding(&g_basic0_ctrl, event_info.device_address); /* CDC
Class request "SetLineCoding" */
                break;

            case USB_STATUS_READ_COMPLETE:
                if (USB_CLASS_HCDC == event_info.type)
                {
                    if (event_info.data_size > 0)
                    {
                        /* Send the received data back to the connected peripheral */
                        g_usb_on_usb.write(&g_basic0_ctrl, g_snd_buf,
event_info.data_size, USB_DEVICE_ADDRESS_1);
                    }
                }
            }
    }
}
```

```
else
{
/* Send the data reception request when the zero-length packet is received. */
g_usb_on_usb.read(&g_basic0_ctrl, g_rcv_buf, CDC_DATA_LEN,
USB_DEVICE_ADDRESS_1);
}
}
else /* USB_HCDCC */
{
/* Control Class notification "SerialState" receive start */
g_usb_on_usb.read(&g_basic0_ctrl,
(uint8_t *) &g_serial_state,
USB_HCDC_SERIAL_STATE_MSG_LEN,
USB_DEVICE_ADDRESS_1);
}
break;
case USB_STATUS_WRITE_COMPLETE:
/* Start receive operation */
g_usb_on_usb.read(&g_basic0_ctrl, g_rcv_buf, CDC_DATA_LEN,
USB_DEVICE_ADDRESS_1);
break;
case USB_STATUS_REQUEST_COMPLETE:
if (USB_CDC_SET_LINE_CODING == (event_info.setup.request_type & USB_BREQUEST))
{
/* Set virtual RTS/DTR signal state */
set_control_line_state(&g_basic0_ctrl, event_info.device_address);
/* CDC Class request "SetControlLineState" */
}
/* Check Complete request "SetControlLineState" */
else if (USB_CDC_SET_CONTROL_LINE_STATE == (event_info.setup.request_type &
USB_BREQUEST))
{
/* Read back virtual UART settings */
get_line_coding(&g_basic0_ctrl, event_info.device_address); /* CDC
```

```
Class request "SetLineCoding" */
    }

else if (USB_CDC_GET_LINE_CODING == (event_info.setup.request_type & USB_BREQUEST))
    {
/* Now that setup is complete, start loopback operation */
        g_usb_on_usb.read(&g_basic0_ctrl, g_snd_buf, CDC_DATA_LEN,
USB_DEVICE_ADDRESS_1);
    }

else
    {
/* Unsupported request */
    }

break;

default:
/* Other event */
break;
    }
}

void set_control_line_state (usb_instance_ctrl_t * p_ctrl, uint8_t device_address)
{
    usb_setup_t setup;
    setup.request_type = SET_CONTROL_LINE_STATE; /*
bRequestCode:SET_CONTROL_LINE_STATE, bmRequestType */
    setup.request_value = 0x0000; /* wValue:Zero */
    setup.request_index = 0x0000; /* wIndex:Interface */
    setup.request_length = 0x0000; /* wLength:Zero */
    g_usb_on_usb.hostControlTransfer(p_ctrl, &setup, (uint8_t *) &g_usb_dummy,
device_address);
}

void set_line_coding (usb_instance_ctrl_t * p_ctrl, uint8_t device_address)
{
    usb_setup_t setup;
    g_com_parm.dwdte_rate = (usb_hcdc_line_speed_t) COM_SPEED;
```

```

    g_com_parm.bchar_format = (usb_hcdc_stop_bit_t) COM_STOP_BIT;
    g_com_parm.bparity_type = (usb_hcdc_parity_bit_t) COM_PARITY_BIT;
    g_com_parm.bdata_bits   = (usb_hcdc_data_bit_t) COM_DATA_BIT;

    setup.request_type      = SET_LINE_CODING;      /* bRequestCode:SET_LINE_CODING,
bmRequestType */

    setup.request_value     = 0x0000;              /* wValue:Zero */
    setup.request_index     = 0x0000;              /* wIndex:Interface */
    setup.request_length    = LINE_CODING_LENGTH; /* Data:Line Coding Structure */
/* Request Control transfer */

    g_usb_on_usb.hostControlTransfer(p_ctrl, &setup, (uint8_t *) &g_com_parm,
device_address);
}

void get_line_coding (usb_instance_ctrl_t * p_ctrl, uint8_t device_address)
{
    usb_setup_t setup;

    setup.request_type      = GET_LINE_CODING;      /* bRequestCode:GET_LINE_CODING,
bmRequestType */

    setup.request_value     = 0x0000;              /* wValue:Zero */
    setup.request_index     = 0x0000;              /* wIndex:Interface */
    setup.request_length    = LINE_CODING_LENGTH; /* Data:Line Coding Structure */
/* Request Control transfer */

    g_usb_on_usb.hostControlTransfer(p_ctrl, &setup, (uint8_t *) &g_com_parm,
device_address);
}

```

## 4.2.50 USB Host Human Interface Device Class Driver (r\_usb\_hhid)

### Modules

#### Functions

**fsp\_err\_t** [R\\_USB\\_HHID\\_TypeGet](#) (usb\_ctrl\_t \*const p\_api\_ctrl, uint8\_t \*p\_type, uint8\_t device\_address)

Get HID protocol.(USB Mouse/USB Keyboard/Other Type.) [More...](#)

**fsp\_err\_t** [R\\_USB\\_HHID\\_MaxPacketSizeGet](#) (usb\_ctrl\_t \*const p\_api\_ctrl,

```
uint16_t *p_size, uint8_t direction, uint8_t device_address)
```

Obtains max packet size for the connected HID device. The max packet size is set to the area. Set the direction (USB\_HID\_IN/USB\_HID\_OUT). [More...](#)

## Detailed Description

This module provides a USB Host Human Interface Device Class Driver (HHID). It implements the [USB HHID Interface](#).

## Overview

The r\_usb\_hhid module combines with the r\_usb\_basic module to provide a USB Host Human Interface Device Class (HHID) driver. The HHID driver conforms to the USB Human Interface Device class specifications and implements communication with a HID device.

## Features

The r\_usb\_hhid module has the following key features:

- Data communication with a connected HID device (USB mouse, keyboard etc.)
- Issuing of HID class requests to a connected HID device
- Supports Interrupt OUT transfer

## Configuration

### Build Time Configurations for r\_usb\_hhid

The following build time configurations are defined in fsp\_cfg/r\_usb\_hhid\_cfg.h:

Configuration	Options	Default	Description
Interrupt In Pipe	<ul style="list-style-type: none"> <li>• USB PIPE6</li> <li>• USB PIPE7</li> <li>• USB PIPE8</li> <li>• USB PIPE9</li> </ul>	USB PIPE6	Select the pipe number to use for input interrupt events.
Interrupt Out Pipe	<ul style="list-style-type: none"> <li>• USB PIPE6</li> <li>• USB PIPE7</li> <li>• USB PIPE8</li> <li>• USB PIPE9</li> </ul>	USB PIPE9	Select the pipe number to use for output interrupt events.

### Configurations for Middleware > USB > USB HHID driver on r\_usb\_hhid

This module can be added to the Stacks tab via New Stack > Middleware > USB > USB HHID driver on r\_usb\_hhid. Non-secure callable guard functions can be generated for this module by right clicking the module in the RA Configuration tool and checking the "Non-secure Callable" box.

Configuration	Options	Default	Description
Name	Name must be a valid	g_hhid0	Module name.

## C symbol

**Clock Configuration**

Refer to the [USB \(r\\_usb\\_basic\)](#) module.

**Pin Configuration**

Refer to the [USB \(r\\_usb\\_basic\)](#) module.

**Usage Notes***Note*

*This driver is not guaranteed to provide USB HID operation in all scenarios. The developer must verify correct operation when connected to the targeted USB peripherals.*

**Class Requests**

The class requests supported by this driver are shown below:

Request	Code	Description
USB_GET_REPORT	0x01	Receives a report from the HID device.
USB_SET_REPORT	0x09	Sends a report to the HID device.
USB_GET_IDLE	0x02	Receives a duration (time) from the HID device.
USB_SET_IDLE	0x0A	Sends a duration (time) to the HID device.
USB_GET_PROTOCOL	0x03	Reads a protocol from the HID device.
USB_SET_PROTOCOL	0x0B	Sends a protocol to the HID device.
USB_GET_REPORT_DESCRIPTOR	0x06	Requests a report descriptor.
USB_GET_HID_DESCRIPTOR	0x06	Requests a HID descriptor.

**Data Format**

The boot protocol data format of data received from the keyboard or mouse through interrupt-IN transfers is shown below:

offset	Keyboard (8 Bytes)	Mouse (3 Bytes)
0 (Top Byte)	Modifier keys	b0 : Button 1 b1 : Button 2 b2 : Button 3 b3-b7 : Reserved
+1	Reserved	X displacement



---

+2	Keycode 1	Y displacement
+3	Keycode 2	-
+4	Keycode 3	-
+5	Keycode 4	-
+6	Keycode 5	-
+7	Keycode 6	-

### Limitations

- The HID driver does not analyze the report descriptor. This driver determines the report format from the interface protocol.
- This driver does not support DMA transfers.
- This driver does not support High-speed.
- The transfer rates of Full-speed and Low-speed are the same when the max packet sizes of Full-speed and Low-speed are the same.

## Examples

### USB HHID Example

The main functions of the application are as follows:

1. Performs enumeration and initialization of HID devices.
2. Transfers data to and from a connected HID device (mouse or keyboard). Data received from the device is read and discarded.
3. When an RTOS is used, the USB driver calls the callback (`usb_apl_callback`) in order to pass events to the main loop through a queue.

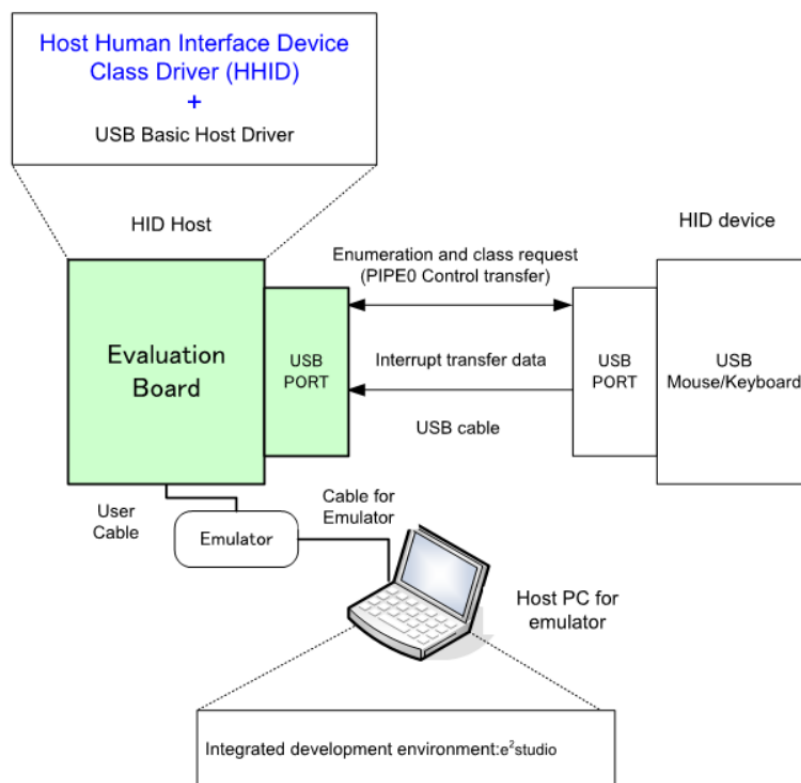


Figure 171: Example Operating Environment

## Application Processing (for RTOS)

The main loop performs processing to receive data from the HID device as part of the main routine. An overview of the processing performed by the loop is shown below.

1. When a USB-related event has completed, the USB driver calls the callback function (`usb_apl_callback`). In the callback function (`usb_apl_callback`), the application task (APL) is notified of the USB completion event using the real-time OS functionality.
2. In APL, information regarding the USB completion event was notified from the callback function is retrieved using the real-time OS functionality.
3. If the USB completion event (the event member of the `usb_ctrl_t` structure) retrieved in step 2 above is `USB_STATUS_CONFIGURED`, APL sends the class request (`SET_PROTOCOL`) to the HID device.
4. If the USB completion event (the event member of the `usb_ctrl_t` structure) retrieved in step 2 above is `USB_STATUS_REQUEST_COMPLETE`, APL performs a data reception request to receive data transmitted from the HID device by calling the `R_USB_Read` function.
5. The above processing is repeated.

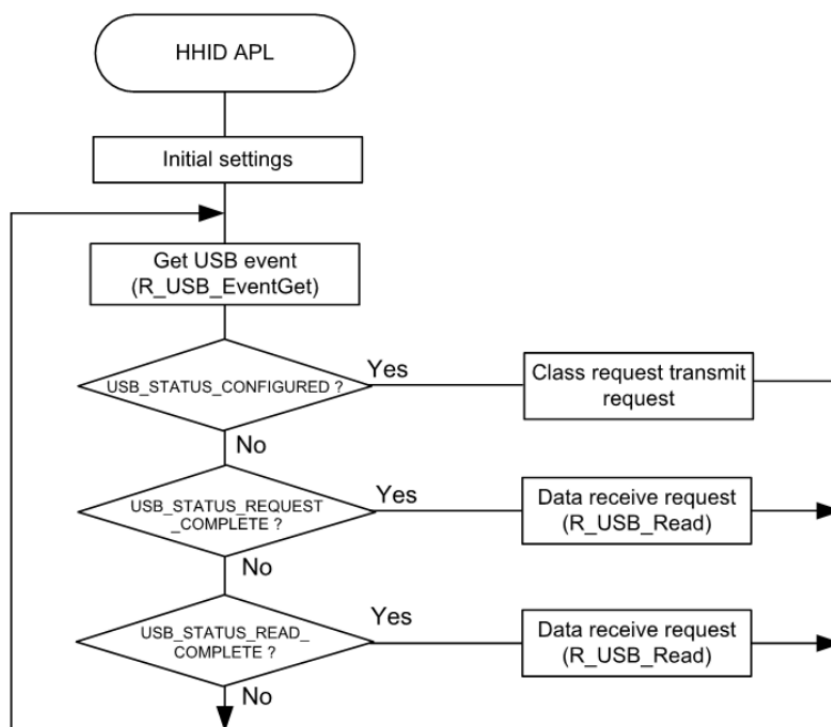


Figure 172: Main Loop (Normal mode)

### Application Processing (for Non-OS)

The main loop performs processing to receive data from the HID device as part of the main routine. An overview of the processing of the main loop is presented below.

1. When the R\_USB\_GetEvent function is called after an HID device attaches to the USB host and enumeration completes, USB\_STATUS\_CONFIGURED is set as the return value. When the APL confirms USB\_STATUS\_CONFIGURED, it calls the R\_USB\_Write function to request transmission of data to the HID device.
2. When the R\_USB\_GetEvent function is called after sending of class request SET\_PROTOCOL to the HID device has completed, USB\_STATUS\_REQUEST\_COMPLETE is set as the return value. When the APL confirms USB\_STATUS\_REQUEST\_COMPLETE, it calls the R\_USB\_Read function to make a data receive request for data sent by the HID device.
3. When the R\_USB\_GetEvent function is called after reception of data from the HID device has completed, USB\_STATUS\_READ\_COMPLETE is set as the return value. When the APL confirms USB\_STATUS\_READ\_COMPLETE, it calls the R\_USB\_Read function to make a data receive request for data sent by the HID device.
4. The processing in step 3, above, is repeated.

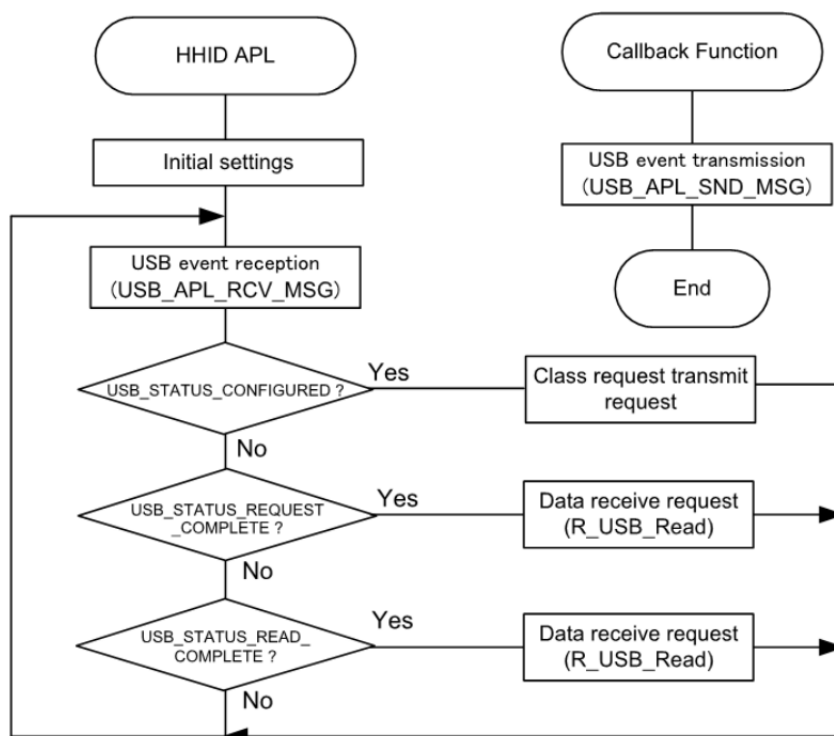


Figure 173: Main Loop (Normal mode)

```

/*****
 * Macro definitions
 *****/
#define SET_PROTOCOL (USB_HID_SET_PROTOCOL | USB_HOST_TO_DEV | USB_CLASS |
USB_INTERFACE)
#define BOOT_PROTOCOL (0)
#define USB_FS_DEVICE_ADDRESS_1 (1)
/*****
 * Private global variables and functions
 *****/
static const usb_hhid_api_t g_hhid_on_usb =
{
    .typeGet          = R_USB_HHID_TypeGet,
    .maxPacketSizeGet = R_USB_HHID_MaxPacketSizeGet,
};
/*****
 * Function Name : r_usb_hhid_example
 * Description : Host HID application main process
 *****/
    
```

```
* Arguments : none
* Return value : none
*****/
static void r_usb_hhid_example (void)
{
#if (BSP_CFG_RTOS == 2)
    usb_event_info_t * p_mess;
#endif /* (BSP_CFG_RTOS == 2) */
    usb_status_t     event;
    usb_event_info_t event_info;
    uint16_t         offset = 0;
    g_usb_on_usb.open(&g_basic0_ctrl, &g_basic0_cfg);
    while (1)
    {
#if (BSP_CFG_RTOS == 2)
        USB_APL_RCV_MSG(USB_APL_MBX, (usb_msg_t **) &p_mess);
        event_info = *p_mess;
        event      = event_info.event;
#else /* (BSP_CFG_RTOS == 2) */
        g_usb_on_usb.eventGet(&event_info, &event); /* Get event code */
#endif /* (BSP_CFG_RTOS == 2) */
        switch (event)
        {
        case USB_STATUS_CONFIGURED:
            {
                g_hhid_on_usb.typeGet(&g_basic0_ctrl, &g_hid_type,
USB_FS_DEVICE_ADDRESS_1);
                g_hhid_on_usb.maxPacketSizeGet(&g_basic0_ctrl, &g_mxps, USB_HID_IN,
USB_FS_DEVICE_ADDRESS_1);
                /* Send the HID request (SetProtocol) to HID device */
                set_protocol(&g_basic0_ctrl, BOOT_PROTOCOL, USB_FS_DEVICE_ADDRESS_1);
                break;
            }
        case USB_STATUS_READ_COMPLETE:
```

```

        {
            offset = hid_memcpy(g_store_buf, g_buf, offset, g_mxps);
            g_usb_on_usb.read(&g_basic0_ctrl, g_buf, (uint32_t) g_mxps,
USB_FS_DEVICE_ADDRESS_1);
        }
        break;
    }
    case USB_STATUS_REQUEST_COMPLETE:
        {
            if (USB_HID_SET_PROTOCOL == (event_info.setup.request_type & USB_BREQUEST))
                {
                    g_usb_on_usb.read(&g_basic0_ctrl, g_buf, (uint32_t) g_mxps,
USB_FS_DEVICE_ADDRESS_1);
                }
            break;
        }
    default:
        {
            break;
        }
    }
}
} /* End of function usb_main */
/*****
* Function Name : set_protocol
* Description : Sending SetProtocol request to HID device
* Arguments : usb_ctrl_t *p_ctrl : Pointer to usb_instance_ctrl_t structure.
* : uint8_t ptorocol: Protocol Type
* : uint8_t device_address: Device address that sends this request
* Return value : none
*****/
static void set_protocol (usb_instance_ctrl_t * p_ctrl, uint8_t protocol, uint8_t
device_address)
{
    usb_setup_t setup;

```

```

    setup.request_type    =
SET_PROTOCOL; /*
bRequestCode:SET_PROTOCOL, bmRequestType */
    setup.request_value =
protocol; /* wValue: Protocol
Type */
    setup.request_index =
0x0000; /* wIndex:Interface */
    setup.request_length =
0x0000; /* wLength:Zero */
    g_usb_on_usb.hostControlTransfer(p_ctrl, &setup, (uint8_t *) &g_setup_data,
device_address); /* Request Control transfer */
} /* End of function set_protocol */
/*****
* Function Name : hid_memcpy
* Description : Copy received hhid data to the application buffer
* Arguments : uint8_t *p_dest : Pointer to application buffer
* : uint8_t *p_src : Pointer to received buffer
* : uint16_t offset : Application buffer offset
* : uint16_t size : Size of received hhid data
* Return value : uint16_t offset + i: Offset
*****/
static uint16_t hid_memcpy (uint8_t * p_dest, uint8_t * p_src, uint16_t offset,
uint16_t size)
{
    uint16_t i;
    for (i = 0; i < size; i++)
    {
        if ((offset + i) == BUFSIZE)
        {
            offset = 0;
        }
        *(p_dest + offset + i) = *(p_src + i);
    }
}

```

```
return (uint16_t) (offset + i);
} /* End of function hid_memcpy */
```

## Function Documentation

### ◆ R\_USB\_HHID\_TypeGet()

```
fsp_err_t R_USB_HHID_TypeGet ( usb_ctrl_t *const p_api_ctrl, uint8_t * p_type, uint8_t device_address )
```

Get HID protocol.(USB Mouse/USB Keyboard/Other Type.)

#### Return values

FSP_SUCCESS	Success.
FSP_ERR_USB_FAILED	The function could not be completed successfully.
FSP_ERR_ASSERTION	Parameter Null pointer error.
FSP_ERR_USB_PARAMETER	Parameter error.

### ◆ R\_USB\_HHID\_MaxPacketSizeGet()

```
fsp_err_t R_USB_HHID_MaxPacketSizeGet ( usb_ctrl_t *const p_api_ctrl, uint16_t * p_size, uint8_t direction, uint8_t device_address )
```

Obtains max packet size for the connected HID device. The max packet size is set to the area. Set the direction (USB\_HID\_IN/USB\_HID\_OUT).

#### Return values

FSP_SUCCESS	Success.
FSP_ERR_USB_FAILED	The function could not be completed successfully.
FSP_ERR_ASSERTION	Parameter Null pointer error.
FSP_ERR_USB_PARAMETER	Parameter error.

## 4.2.51 USB Host Mass Storage Class Driver (r\_usb\_hmsc)

### Modules

#### Functions

```
FSP_HEADER fsp_err_t R_USB_HMSC_StorageCommand (usb_ctrl_t *const p_api_ctrl, uint8_t
```



\*buf, uint8\_t command, uint8\_t destination)

Processing for MassStorage(ATAPI) command. [More...](#)

`fsp_err_t R_USB_HMSC_DriveNumberGet` (usb\_ctrl\_t \*const p\_api\_ctrl, uint8\_t \*p\_drive, uint8\_t destination)

Get number of Storage drive. [More...](#)

`fsp_err_t R_USB_HMSC_SemaphoreGet` (void)

Get a semaphore. (RTOS only) [More...](#)

`fsp_err_t R_USB_HMSC_SemaphoreRelease` (void)

Release a semaphore. (RTOS only) [More...](#)

`fsp_err_t R_USB_HMSC_StorageReadSector` (uint16\_t drive\_number, uint8\_t \*const buff, uint32\_t sector\_number, uint16\_t sector\_count)

Read sector information. [More...](#)

`fsp_err_t R_USB_HMSC_StorageWriteSector` (uint16\_t drive\_number, uint8\_t const \*const buff, uint32\_t sector\_number, uint16\_t sector\_count)

Write sector information. [More...](#)

## Detailed Description

This module provides a USB Host Mass Storage Class (HMSC) driver. It implements the [USB HMSC Interface](#).

## Overview

The r\_usb\_hmsc module, when used in combination with the r\_usb\_basic module, operates as a USB Host Mass Storage Class (HMSC) driver. It is built on the USB Mass Storage Class Bulk-Only Transport (BOT) protocol. It is possible to communicate with BOT-compatible USB storage devices by combining this module with a file system and storage device driver.

### Note

*This module should be used in combination with the FreeRTOS+FAT File System.*

## Features

The r\_usb\_hmsc module has the following key features:

- Checking of connected USB storage devices to determine whether or not operation is supported

- Storage command communication using the BOT protocol
- Support for SFF-8070i (ATAPI) USB mass storage subclass
- Sharing of a single pipe for IN/OUT directions or multiple devices
- Supports up to 4 connected USB storage devices

## Class Requests

The class requests supported by this driver are shown below.

Request	Description
GetMaxLun	Gets the maximum number of units that are supported.
MassStorageReset	Cancels a protocol error.

## Storage Commands

This driver supports the following storage commands:

- TEST\_UNIT\_READY
- MODE\_SELECT10
- MODE\_SENSE10
- PREVENT\_ALLOW
- READ\_FORMAT\_CAPACITY
- READ10
- WRITE10

## Configuration

Refer to the [USB \(r\\_usb\\_basic\)](#) module.

### Clock Configuration

Refer to the [USB \(r\\_usb\\_basic\)](#) module.

### Pin Configuration

Refer to the [USB \(r\\_usb\\_basic\)](#) module.

## Usage Notes

### Warning

Due to the wide variety of USB mass storage device implementations, this driver is not guaranteed to work with all devices. When implementing the driver it is important to verify correct operation with the mass storage devices that the end user is expected to use.

### Limitations

1. Some MSC devices may be unable to connect because they are not recognized as storage devices.
2. MSC devices that return values of 1 or higher in response to the GetMaxLun command (mass storage class command) are not supported.
3. A maximum of 4 USB storage devices can be connected.

4. Only USB storage devices with a sector size of 512 bytes can be connected.
5. A device that does not respond to the READ\_CAPACITY command operates as a device with a sector size of 512 bytes.
6. The continuous transfer mode cannot be used when using DMA.
7. This module must be incorporated into a project using r\_usb\_basic and does not provide any public APIs.
8. This driver does not support Low-speed.

## Examples

### USB HMSC Example

#### Example Operating Environment

The following shows an example operating environment for the HMSC.

Refer to the associated instruction manuals for details on setting up the evaluation board and using the emulator, etc.

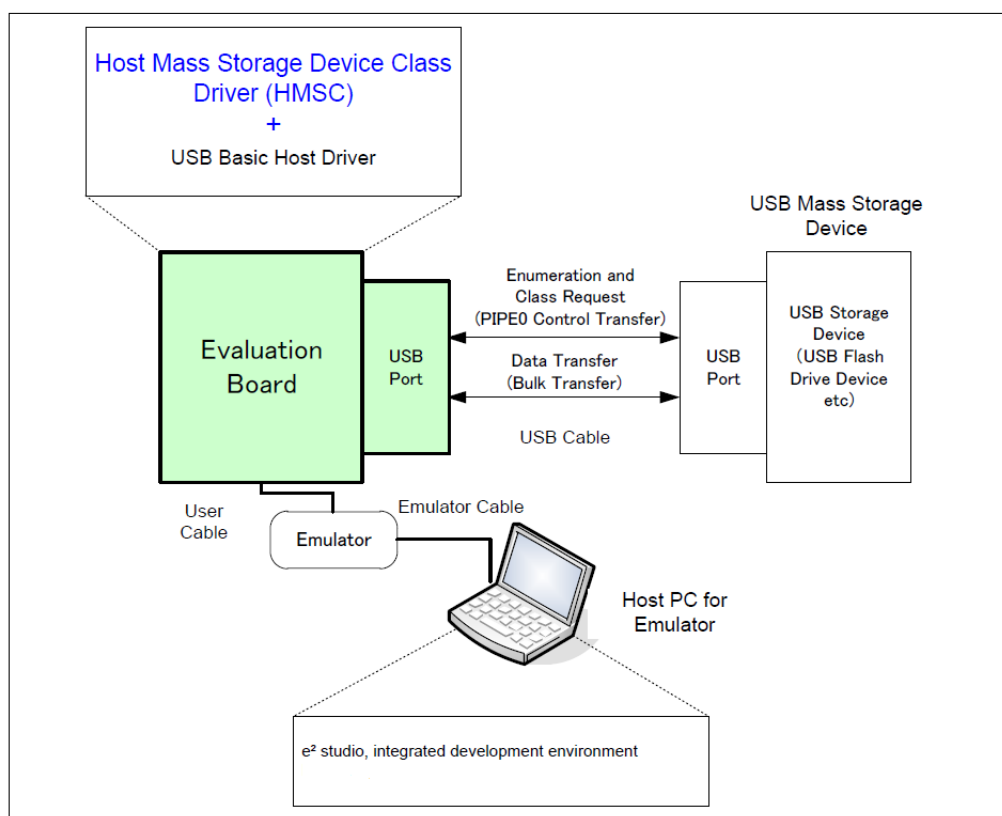


Figure 174: Example Operating Environment

### Application Specifications

The main functions of the application are as follows:

1. Performs enumeration and drive recognition processing on MSC devices.
2. After the above processing finishes, the application writes the file hmscdemo.txt to the

MSC device once.

3. After writing the above file, the APL repeatedly reads the file hmscdemo.txt. It continues to read the file repeatedly until the switch is pressed again.

## Application Processing (for RTOS)

This application has two tasks. An overview of the processing in these two tasks is provided below.

### usb\_apl\_task

1. After start up, MCU pin setting, USB controller initialization, and application program initialization are performed.
2. The MSC device is attached to the kit. When enumeration and drive recognition processing have completed, the USB driver calls the callback function (usb\_apl\_callback). In the callback function (usb\_apl\_callback), the application task is notified of the USB completion event using the FreeRTOS functionality.
3. In the application task, information regarding the USB completion event about which notification was received from the callback function is retrieved using the real-time OS functionality.
4. If the USB completion event (the event member of the usb\_ctrl\_t structure) retrieved in step 2 above is USB\_STS\_CONFIGURED then, based on the USB completion event, the MSC device is mounted and the file is written to the MSC device.
5. If the USB completion event (the event member of the usb\_ctrl\_t structure) retrieved in step 2 above is USB\_STS\_DETACH, the application initializes the variables for state management.

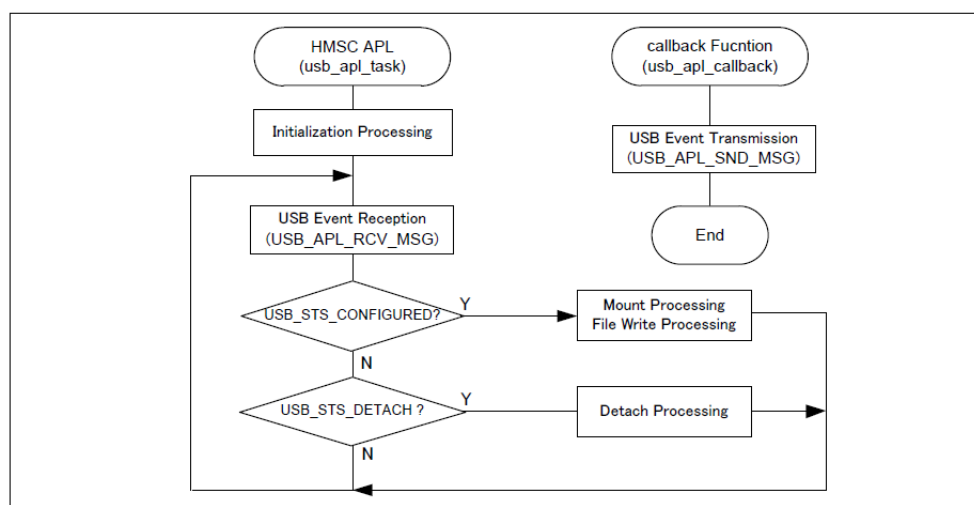


Figure 175: usb\_apl\_task

### file\_read\_task

Of the application tasks `usb_apl_task` and `file_read_task`, `file_read_task` is processed while `usb_apl_task` is in the wait state. This task performs file read processing on the file that was written to the MSC device (hmscdemo.txt).

### Example Code

Note

For example code refer to the [FreeRTOS + FAT example](#).

## Function Documentation

### ◆ R\_USB\_HMSC\_StorageCommand()

```
fsp_err_t R_USB_HMSC_StorageCommand ( usb_ctrl_t *const p_api_ctrl, uint8_t * buf, uint8_t
command, uint8_t destination )
```

Processing for MassStorage(ATAPI) command.

#### Return values

FSP_SUCCESS	Success.
FSP_ERR_USB_FAILED	The function could not be completed successfully.
FSP_ERR_ASSERTION	Parameter Null pointer error.
FSP_ERR_USB_PARAMETER	Parameter error.

### ◆ R\_USB\_HMSC\_DriveNumberGet()

```
fsp_err_t R_USB_HMSC_DriveNumberGet ( usb_ctrl_t *const p_api_ctrl, uint8_t * p_drive, uint8_t
destination )
```

Get number of Storage drive.

#### Return values

FSP_SUCCESS	Success.
FSP_ERR_USB_FAILED	The function could not be completed successfully.
FSP_ERR_ASSERTION	Parameter Null pointer error.
FSP_ERR_USB_PARAMETER	Parameter error.

### ◆ R\_USB\_HMSC\_SemaphoreGet()

```
fsp_err_t R_USB_HMSC_SemaphoreGet ( void )
```

Get a semaphore. (RTOS only)

If this function is called in the OS less execution environment, a failure is returned.

#### Return values

FSP_SUCCESS	Success.
FSP_ERR_USB_FAILED	The function could not be completed successfully.

◆ **R\_USB\_HMSSC\_SemaphoreRelease()**

```
fsp_err_t R_USB_HMSSC_SemaphoreRelease ( void )
```

Release a semaphore. (RTOS only)

If this function is called in the OS less execution environment, a failure is returned.

**Return values**

FSP_SUCCESS	Success.
FSP_ERR_USB_FAILED	The function could not be completed successfully.

◆ **R\_USB\_HMSSC\_StorageReadSector()**

```
fsp_err_t R_USB_HMSSC_StorageReadSector ( uint16_t drive_number, uint8_t *const buff, uint32_t sector_number, uint16_t sector_count )
```

Read sector information.

**Return values**

FSP_SUCCESS	Success.
FSP_ERR_USB_FAILED	The function could not be completed successfully.
FSP_ERR_ASSERTION	Parameter Null pointer error.
FSP_ERR_USB_PARAMETER	Parameter error.

**Note**

*The address specified in the argument buff must be 4-byte aligned.*

**◆ R\_USB\_HMSSC\_StorageWriteSector()**

```
fsp_err_t R_USB_HMSSC_StorageWriteSector ( uint16_t drive_number, uint8_t const *const buff,
uint32_t sector_number, uint16_t sector_count )
```

Write sector information.

**Return values**

FSP_SUCCESS	Success.
FSP_ERR_USB_FAILED	The function could not be completed successfully.
FSP_ERR_ASSERTION	Parameter Null pointer error.
FSP_ERR_USB_PARAMETER	Parameter error.

*Note*

The address specified in the argument *buff* must be 4-byte aligned.

**4.2.52 USB Peripheral Communications Device Class (r\_usb\_pcdc)****Modules**

This module provides a USB Peripheral Communications Device Class Driver (PCDC). It implements the [USB PCDC Interface](#).

**Functions**

Refer to [USB \(r\\_usb\\_basic\)](#) for the common API (r\_usb\_basic) to be called from the application.

**Detailed Description****Overview**

The r\_usb\_pcdc module combines with the r\_usb\_basic module to provide a USB Peripheral Communications Device Class (PCDC) driver. The PCDC driver conforms to Abstract Control Model of the USB Communications Device Class (CDC) specification and enables communication with a CDC host device.

**Features**

The r\_usb\_pcdc module has the following key features:

- Data transfer to and from a USB host
- Response to CDC class requests
- Supports CDC notifications

## Configuration

### Build Time Configurations for r\_usb\_pcdc

The following build time configurations are defined in fsp\_cfg/r\_usb\_pcdc\_cfg.h:

Configuration	Options	Default	Description
Bulk Input Transfer Pipe	<ul style="list-style-type: none"> <li>• USB PIPE1</li> <li>• USB PIPE2</li> <li>• USB PIPE3</li> <li>• USB PIPE4</li> <li>• USB PIPE5</li> </ul>	USB PIPE1	Select the USB pipe to use for bulk input transfers.
Bulk Output Transfer Pipe	<ul style="list-style-type: none"> <li>• USB PIPE1</li> <li>• USB PIPE2</li> <li>• USB PIPE3</li> <li>• USB PIPE4</li> <li>• USB PIPE5</li> </ul>	USB PIPE2	Select the USB pipe to use for bulk output transfers.
Interrupt Output Pipe	<ul style="list-style-type: none"> <li>• USB PIPE6</li> <li>• USB PIPE7</li> <li>• USB PIPE8</li> <li>• USB PIPE9</li> </ul>	USB PIPE6	Select the USB pipe to use for interrupts.

### Configurations for Middleware > USB > USB PCDC driver on r\_usb\_pcdc

This module can be added to the Stacks tab via New Stack > Middleware > USB > USB PCDC driver on r\_usb\_pcdc.

Configuration	Options	Default	Description
Name	Name must be a valid C symbol	g_pcdc0	Module name.

#### Note

Refer to the [USB \(r\\_usb\\_basic\)](#) module for hardware configuration options.

### Clock Configuration

Refer to the [USB \(r\\_usb\\_basic\)](#) module.

### Pin Configuration

Refer to the [USB \(r\\_usb\\_basic\)](#) module.

## Usage Notes

### Abstract Control Model Overview

The Abstract Control Model subclass of CDC is a technology that bridges the gap between USB devices and earlier modems (employing RS-232C connections), enabling use of application programs designed for older modems.



## Class Requests (Host to Peripheral)

This driver notifies the application when receiving the following class requests:

Request	Code	Description
SetLineCoding	0x20	Sets communication line settings (bitrate, data length, parity, and stop bit length)
GetLineCoding	0x21	Acquires the communication line setting state
SetControlLineState	0x22	Set communication line control signals (RTS, DTR)

### Note

For details concerning the Abstract Control Model requests, refer to Table 11 "Requests - Abstract Control Model" in the "USB Communications Class Subclass Specification for PSTN Devices", Revision 1.2.

## Data Format of Class Requests

The data format of supported class requests is described below:

bmRequestType	bRequest	wValue	wIndex	wLength	Data
0x21	SET_LINE_CODING (0x20)	0x0000	0x0000	0x0007	<a href="#">usb_pcdc_linecoding_t</a>
0xA1	GET_LINE_CODING (0x21)	0x0000	0x0000	0x0007	<a href="#">usb_pcdc_linecoding_t</a>
0x21	SET_CONTROL_LINE_STATE (0x22)	<a href="#">usb_pcdc_ctrllinestate_t</a>	0x0000	0x0000	None

## Class Notifications (Peripheral to Host)

The following class notifications are supported:

Notification	Code	Description
SERIAL_STATE	0x20	Notification of serial line state

The data types returned are as follows:

bmRequestType	bRequest	wValue	wIndex	wLength	Data
0xA1	SERIAL_STATE (0x20)	0x0000	0x0000	0x0002	<a href="#">usb_serial_state_bitmap_t</a>

### Note

The host is notified with SERIAL\_STATE whenever a change in the UART port state is detected. This driver will automatically detect overrun, parity and framing errors. A state notification is performed when a transition from

*normal to error state is detected.*

## Virtual COM-port Usage

When connected to a PC the CDC device can be used as a virtual COM port. After enumeration, the CDC class requests `GetLineCoding` and `SetControlLineState` are executed by the target, and the CDC device is registered in Windows Device Manager as a virtual COM device.

Registering the CDC device as a virtual COM-port in Windows Device Manager enables data communication with the CDC device via a terminal app such as `PuTTY`. When changing settings of the serial port in the terminal application, the UART setting is propagated to the firmware via the class request `SetLineCoding`.

Data input (or file transmission) from the terminal app window is transmitted to the board using endpoint 2 (EP2); data from the board side is transmitted to the PC using EP1.

When the last packet of data received is the maximum packet size, and the terminal determines that there is continuous data, the received data may not be displayed in the terminal. If the received data is smaller than the maximum packet size, the data received up to that point is displayed in the terminal.

## Limitations

- This module must be incorporated into a project using `r_usb_basic` and does not provide any public APIs.
- This driver does not support Low-speed.

## Examples

### USB PCDC Loopback Example

The main functions of the PCDC loopback example are as follows:

1. Receives virtual UART configuration data from the host terminal
2. Loops all other received data back to the host terminal

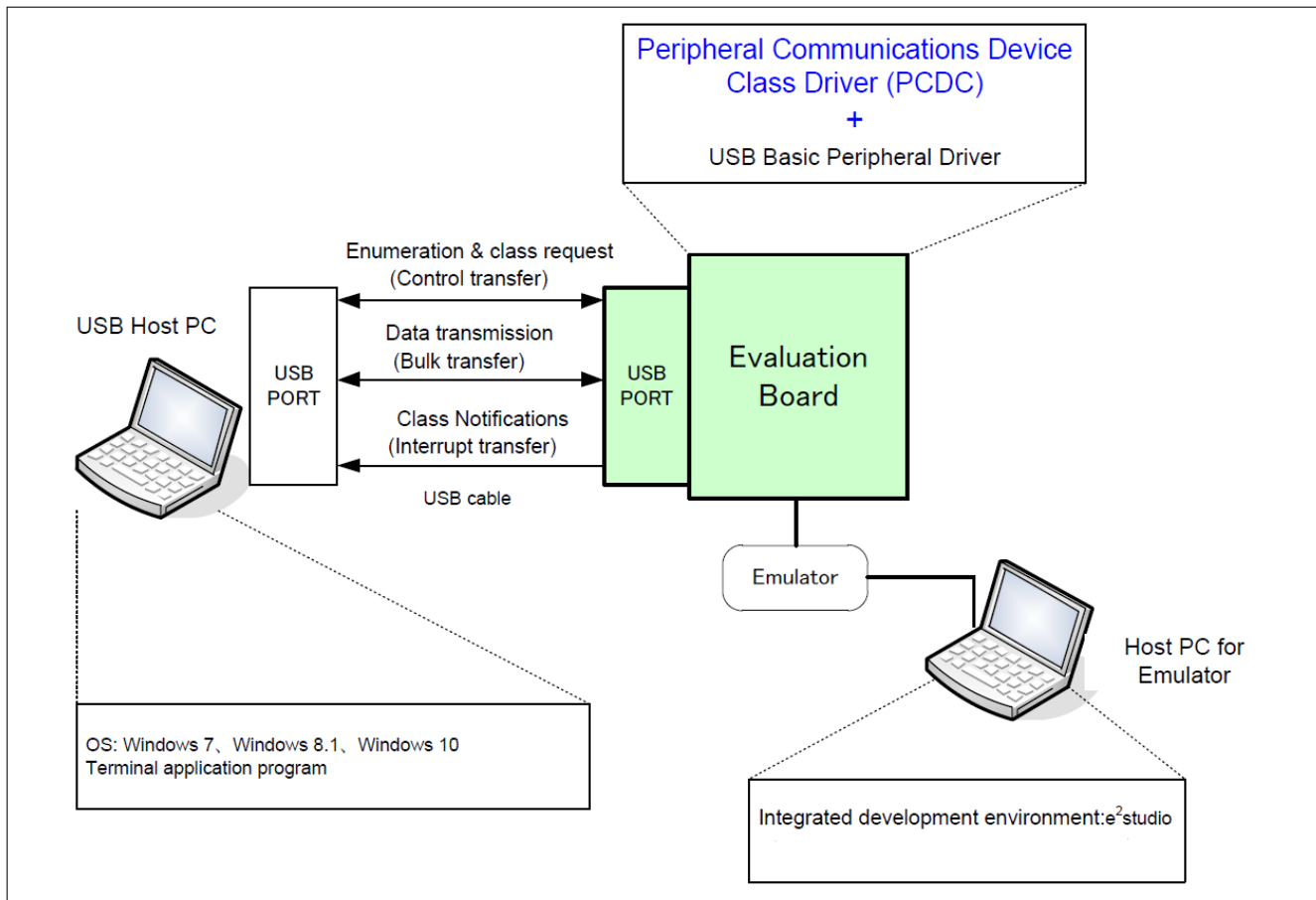


Figure 176: Example Operating Environment

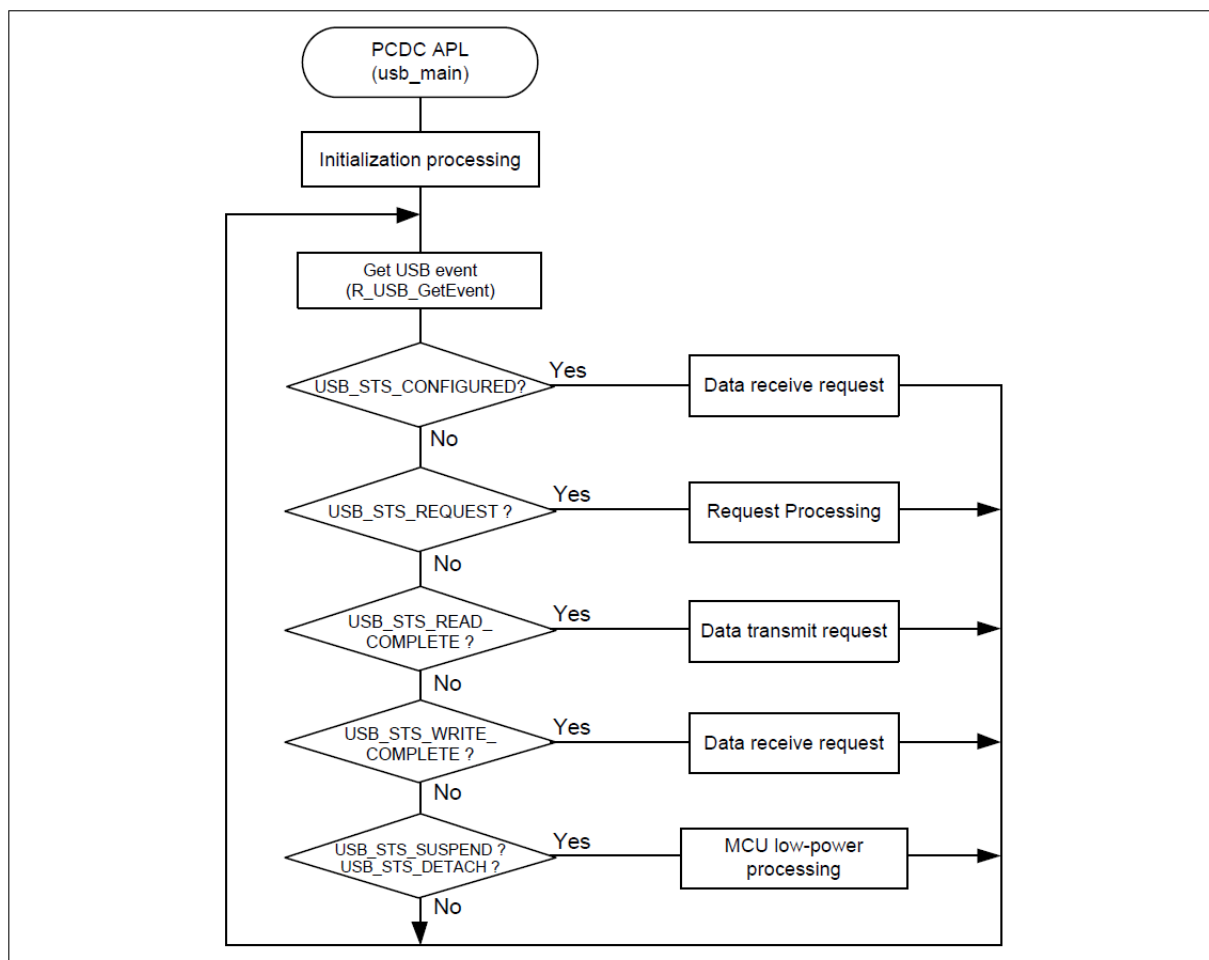


Figure 177: Main Loop processing (Echo mode)

```

void usb_basic_example (void)
{
    usb_event_info_t event_info;
    usb_status_t event;
    g_usb_on_usb.open(&g_basic0_ctrl, &g_basic0_cfg);
    while (1)
    {
        /* Get USB event data */
        g_usb_on_usb.eventGet(&event_info, &event);
        /* Handle the received event (if any) */
        switch (event)
        {
            case USB_STATUS_CONFIGURED:

```

```
case USB_STATUS_WRITE_COMPLETE:
/* Initialization complete; get data from host */
    g_usb_on_usb.read(&g_basic0_ctrl, g_buf, DATA_LEN, USB_CLASS_PCDC);
break;
case USB_STATUS_READ_COMPLETE:
/* Loop back received data to host */
    g_usb_on_usb.write(&g_basic0_ctrl, g_buf, event_info.data_size,
USB_CLASS_PCDC);
break;
case USB_STATUS_REQUEST: /* Receive Class Request */
if (USB_PCDC_SET_LINE_CODING == (event_info.setup.request_type & USB_BREQUEST))
    {
/* Configure virtual UART settings */
    g_usb_on_usb.periControlDataGet(&g_basic0_ctrl, (uint8_t *)
&g_line_coding, LINE_CODING_LENGTH);
    }
else if (USB_PCDC_GET_LINE_CODING == (event_info.setup.request_type & USB_BREQUEST))
    {
/* Send virtual UART settings back to host */
    g_usb_on_usb.periControlDataSet(&g_basic0_ctrl, (uint8_t *)
&g_line_coding, LINE_CODING_LENGTH);
    }
else
    {
/* ACK all other status requests */
    g_usb_on_usb.periControlStatusSet(&g_basic0_ctrl,
USB_SETUP_STATUS_ACK);
    }
break;
case USB_STATUS_SUSPEND:
case USB_STATUS_DETACH:
break;
default:
break;
```



## Descriptor

A template for PCDC descriptors can be found in `ra/fsp/src/r_usb_pcdc/r_usb_pcdc_descriptor.c.template`. Also, please be sure to use your vendor ID.

### 4.2.53 USB Peripheral Human Interface Device Class (r\_usb\_phid)

#### Modules

This module is USB Peripheral Human Interface Device Class Driver (PHID). It implements the [USB PHID Interface](#).

#### Functions

Refer to [USB \(r\\_usb\\_basic\)](#) for the common API (`r_usb_basic`) to be called from the application.

#### Detailed Description

## Overview

The `r_usb_phid` module combines with the `r_usb_basic` module to provide a USB Peripheral Human Interface Device Class (PHID) driver. The PHID driver conforms to the USB Human Interface Device class specifications and implements communication with a HID host.

#### Features

The `r_usb_phid` module has the following functions:

- Data transfer to and from a USB host
- Response to HID class requests
- Response to function references from the HID host

#### Note

*This driver is not guaranteed to provide USB HID operation in all scenarios. The developer must verify correct operation when connected to the targeted USB hosts.*

## Configuration

### Build Time Configurations for r\_usb\_phid

The following build time configurations are defined in fsp\_cfg/r\_usb\_phid\_cfg.h:

Configuration	Options	Default	Description
Interrupt In Pipe	<ul style="list-style-type: none"> <li>• USB PIPE6</li> <li>• USB PIPE7</li> <li>• USB PIPE8</li> <li>• USB PIPE9</li> </ul>	USB PIPE6	Select the pipe number for input interrupt events.
Interrupt Out Pipe	<ul style="list-style-type: none"> <li>• USB PIPE6</li> <li>• USB PIPE7</li> <li>• USB PIPE8</li> <li>• USB PIPE9</li> </ul>	USB PIPE7	Select the pipe number for output interrupt events.

### Configurations for Middleware > USB > USB PHID driver on r\_usb\_phid

This module can be added to the Stacks tab via New Stack > Middleware > USB > USB PHID driver on r\_usb\_phid.

Configuration	Options	Default	Description
Name	Name must be a valid C symbol	g_phid0	Module name.

### Clock Configuration

Refer to the [USB \(r\\_usb\\_basic\)](#) module.

### Pin Configuration

Refer to the [USB \(r\\_usb\\_basic\)](#) module.

## Usage Notes

### Class Requests (Host to Peripheral)

This driver notifies the application when receiving the following class requests:

Request	Code	Description
Get_Report	0x01	Receives a report from the HID host
Set_Report	0x09	Sends a report to the HID host
Get_Idle	0x02	Receives a duration (time) from the HID host
Set_Idle	0x0A	Sends a duration (time) to the HID host
Get_Protocol	0x03	Reads a protocol from the HID host
Set_Protocol	0x0B	Sends a protocol to the HID host

Get\_Descriptor 0x06 Transmits a report or HID descriptor

The data format of supported class requests is described below:

bmRequestType	bRequest	wValue	wIndex	wLength	Data
0xA1	GET_REPORT (0x01)	ReportType & ReportID	Interface	ReportLength	Report
0x21	SET_REPORT (0x09)	ReportType & ReportID	Interface	ReportLength	Report
0xA1	GET_IDLE (0x02)	0 & ReportID	Interface	1	Idle rate
0x21	SET_IDLE (0x0A)	Duration & ReportID	Interface	0	Idle rate
0xA1	GET_PROTOCOL (0x03)	0	Interface	0	0 (Boot) or 1 (Report)
0x21	SET_PROTOCOL (0x0B)	0 (Boot) or 1 (Report)	Interface	0	Not applicable

### Descriptors

A template for PHID descriptors can be found in `ra/fsp/src/r_usb_phid/r_usb_phid_descriptor.c.template`. Be sure to replace the vendor ID with your own.

### Limitations

- This driver does not support USB Hi-speed mode.

## Examples



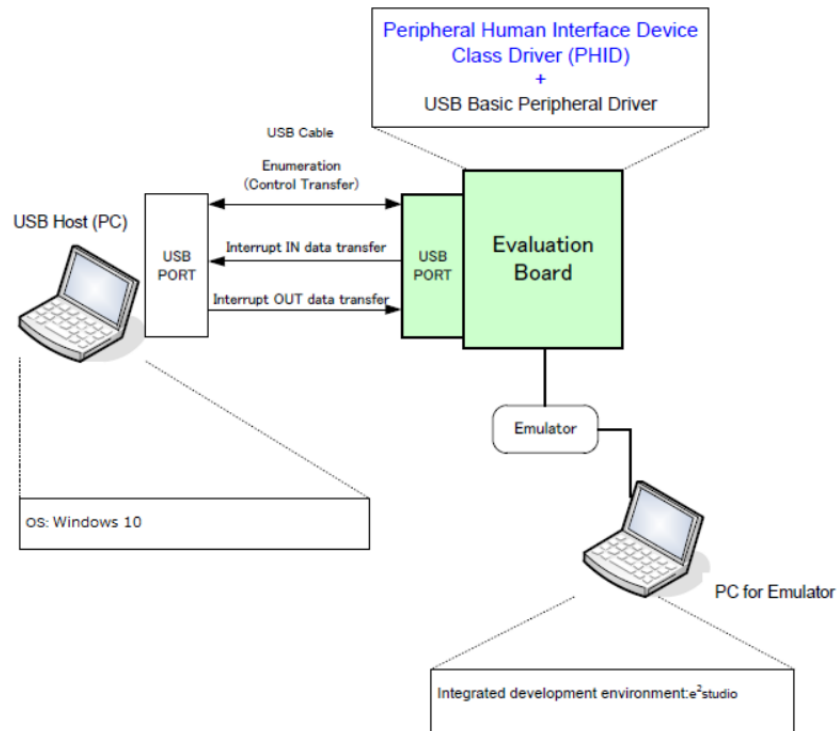


Figure 178: Example Operating Environment

### USB PHID Example (no RTOS)

This is a minimal example for implementing PHID in a non-RTOS application.

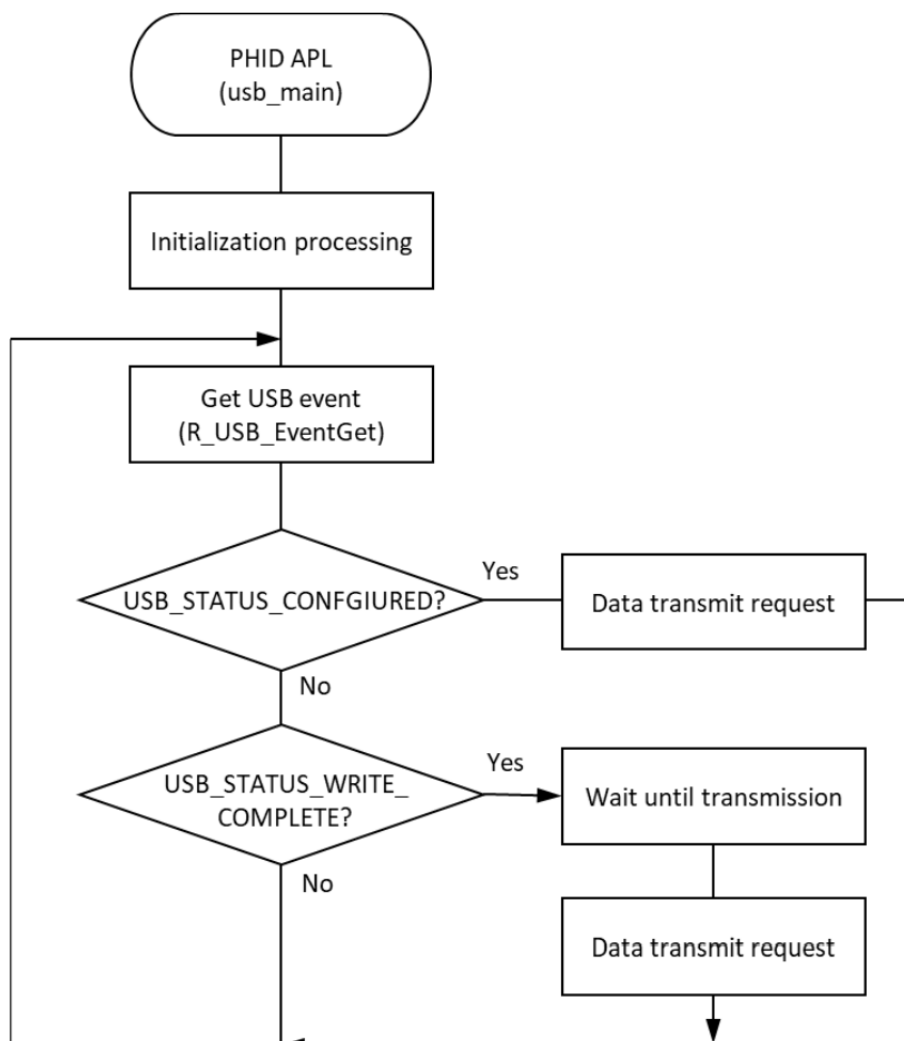


Figure 179: Main Loop processing for non-RTOS example

```

#define USB_RECEIVE_REPORT_DESCRIPTOR (76)
#define USB_RECEIVE_HID_DESCRIPTOR (9)
#define USB_WAIT_1000MS (1000)
#define SW_ACTIVE 0
#define SW_R_PFS->PORT[0].PIN[8].PmnPFS_b.PIDR
#define SW_PDR R_PFS->PORT[0].PIN[8].PmnPFS_b.PDR
#define SW_PMR R_PFS->PORT[0].PIN[8].PmnPFS_b.PMR
static uint8_t g_buf[] = {0, 0, 0, 0, 0, 0, 0, 0}; /* HID data */
static const uint8_t g_zero_data[] = {0, 0, 0, 0, 0, 0, 0, 0}; /* zero data */
static uint16_t g_numlock = 0;
static uint8_t g_idle = 0;
uint8_t          g_remote_wakeup_enable = USB_OFF;
uint8_t          g_status                = NO_WRITING;

```

```
/*
 * Function Name : usb_cpu_getkeyno
 * Description : input key port
 * Arguments : none
 * Return value : uint16_t : key_no
 */
uint8_t usb_cpu_getkeyno (void)
{
    uint8_t key_buf = 0;
    if (SW_ACTIVE == SW)
    {
        if (sw_on_count[0] < SW_ON_THRESHOLD)
        {
            sw_on_count[0]++;
        }
    }
    else
    {
        if (sw_on_count[0] >= SW_ON_THRESHOLD)
        {
            key_buf |= SW_PUSH;
        }
        sw_on_count[0] = 0;
    }
    return key_buf;
}

void set_key_data (uint8_t * p_buf)
{
    static uint8_t key_data;
    key_data = KBD_CODE_A;
    *(p_buf + 2) = key_data;
}

void usb_basic_example (void)
{
```

```
usb_event_info_t event_info;

usb_status_t     event;

uint8_t         * p_idle_value;

uint8_t         sw_data;

usb_info_t      info;

fsp_err_t       ret_code = FSP_SUCCESS;

uint8_t         send_data[16] BSP_ALIGN_VARIABLE(4);

g_usb_on_usb.open(&g_basic0_ctrl, &g_basic0_cfg);

set_key_data(g_buf);

while (1)
{
    g_usb_on_usb.eventGet(&event_info, &event);

switch (event)
{
case USB_STATUS_CONFIGURED:
break;

case USB_STATUS_WRITE_COMPLETE:
if (DATA_WRITING == g_status)
{
    g_status = ZERO_WRITING;
    g_usb_on_usb.write(&g_basic0_ctrl, (uint8_t *) g_zero_data,
DATA_LEN, USB_CLASS_PHID); /* Sending the zero data (8 bytes) */
}
else
{
    g_status = DATA_WRITING;
    usb_cpu_delay_xms(USB_WAIT_1000MS);
    g_usb_on_usb.write(&g_basic0_ctrl, g_buf, DATA_LEN, USB_CLASS_PHID
);
}

break;

case USB_STATUS_REQUEST: /*
Receive Class Request */

if (USB_SET_REPORT == (event_info.setup.request_type & USB_BREQUEST))
```

```
{
    g_usb_on_usb.read(&g_basic0_ctrl, (uint8_t *) &g_numlock, 2,
USB_CLASS_PHID); /* Get the NumLock data (NumLock data is not used) */
}
else if (USB_GET_DESCRIPTOR == (event_info.setup.request_type & USB_BREQUEST))
{
    if (USB_GET_REPORT_DESCRIPTOR == event_info.setup.request_value)
    {
        g_usb_on_usb.periControlDataSet(&g_basic0_ctrl, (uint8_t *)
g_apl_report,
USB_RECEIVE_REPORT_DESCRIPTOR);
    }
    else if (USB_GET_HID_DESCRIPTOR == event_info.setup.request_value)
    {
        for (uint8_t i = 0; i < USB_RECEIVE_HID_DESCRIPTOR; i++)
        {
            send_data[i] = g_apl_configuration[18 + i];
        }
        /* Configuration Descriptor address set. */
        g_usb_on_usb.periControlDataSet(&g_basic0_ctrl, send_data,
USB_RECEIVE_HID_DESCRIPTOR);
    }
    else
    {
        g_usb_on_usb.periControlStatusSet(&g_basic0_ctrl,
USB_SETUP_STATUS_STALL);
    }
}
else if (USB_SET_IDLE == (event_info.setup.request_type & USB_BREQUEST))
{
    /* Get SetIdle value */
    p_idle_value = (uint8_t *) &event_info.setup.request_value;
    g_idle = p_idle_value[1];
}
```

```
        g_usb_on_usb.periControlStatusSet(&g_basic0_ctrl,
USB_SETUP_STATUS_ACK);
    }
    else if (USB_GET_IDLE == (event_info.setup.request_type & USB_BREQUEST))
    {
        g_usb_on_usb.periControlDataSet(&g_basic0_ctrl, &g_idle, 1);
    }
    else if (USB_SET_PROTOCOL == (event_info.setup.request_type & USB_BREQUEST))
    {
        g_usb_on_usb.periControlStatusSet(&g_basic0_ctrl,
USB_SETUP_STATUS_ACK);
    }
    else if (USB_GET_PROTOCOL == (event_info.setup.request_type & USB_BREQUEST))
    {
        g_usb_on_usb.periControlStatusSet(&g_basic0_ctrl,
USB_SETUP_STATUS_STALL);
    }
    else
    {
        g_usb_on_usb.periControlStatusSet(&g_basic0_ctrl,
USB_SETUP_STATUS_STALL);
    }
    break;
case USB_STATUS_REQUEST_COMPLETE: /* Complete Class Request */
if (USB_SET_IDLE == (event_info.setup.request_type & USB_BREQUEST))
    {
        p_idle_value = (uint8_t *) &event_info.setup.request_value;
        g_idle = p_idle_value[1];
    }
    else if (USB_SET_PROTOCOL == (event_info.setup.request_type & USB_BREQUEST))
    {
        /* None */
    }
    else
```

```
    {
        g_status = DATA_WRITING;
        g_usb_on_usb.write(&g_basic0_ctrl, g_buf, DATA_LEN, USB_CLASS_PHID
);
    }
break;
case USB_STATUS_SUSPEND:
break;
case USB_STATUS_DETACH:
    g_remote_wakeup_enable = USB_OFF;
break;
default:
break;
}
ret_code = g_usb_on_usb.infoGet(&g_basic0_ctrl, &info, NULL);
if (FSP_SUCCESS == ret_code)
{
    sw_data = usb_cpu_getkeyno();
if (USB_STATUS_SUSPEND == info.device_status)
{
if (0 != (sw_data & SW_PUSH))
{
    g_usb_on_usb.remoteWakeup(&g_basic0_ctrl);
}
}
}
}
} /* End of function usb_basic_example() */
```

## USB PHID Example (RTOS)

This is a minimal example for implementing PHID in an RTOS application.

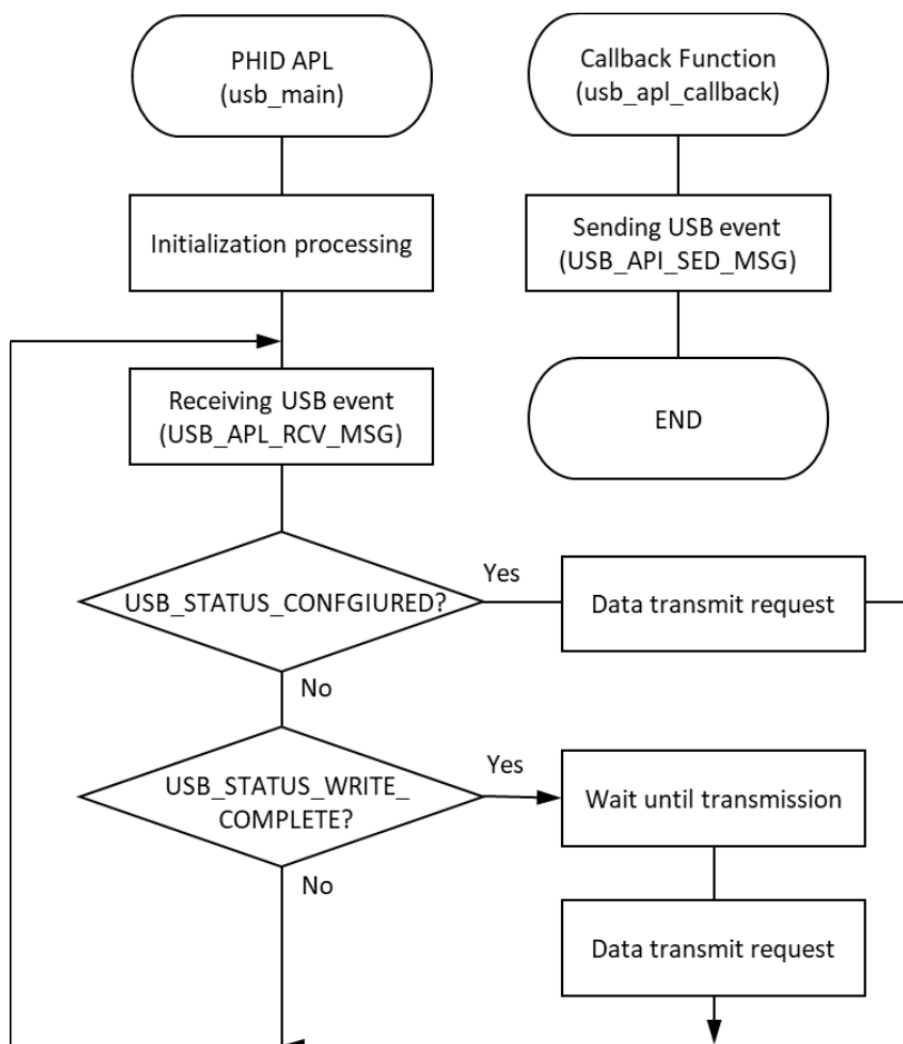


Figure 180: Main Loop processing for RTOS example

```

#define USB_APL_MBX (0)

void usb_apl_callback (usb_event_info_t * p_api_event, usb_hdl_t cur_task,
usb_onoff_t usb_state)
{
    (void) usb_state;
    (void) cur_task;
    USB_APL_SND_MSG(USB_APL_MBX, (usb_msg_t *) p_api_event);
} /* End of function usb_apl_callback */

/*****
* Function Name : usb_apl_rec_msg
* Description : Receive a message to the specified id (mailbox).
* Argument : uint8_t id : ID number (mailbox).
* : usb_msg_t** mess : Message pointer
*****/

```



```

* : usb_tm_t tm : Timeout Value
* Return : uint16_t : USB_OK / USB_ERROR
*****/
usb_er_t usb_apl_rec_msg (uint8_t id, usb_msg_t ** mess, usb_tm_t tm)
{
    BaseType_t    err;
    QueueHandle_t handle;
    usb_er_t      result;
    if (NULL == mess)
    {
        return USB_APL_ERROR;
    }
    handle = (*(g_apl_mbx_table[id]));
    *mess = NULL;
    err = xQueueReceive(handle, (void *) mess, (tm));
    if ((pdTRUE == err) && (NULL != (*mess)))
    {
        result = USB_APL_OK;
    }
    else
    {
        result = USB_APL_ERROR;
    }
    return result;
}
/*****
* Function Name : usb_apl_snd_msg
* Description : Send a message to the specified id (mailbox).
* Argument : uint8_t id : ID number (mailbox).
* : usb_msg_t* mess : Message pointer
* Return : usb_er_t : USB_OK / USB_ERROR
*****/
usb_er_t usb_apl_snd_msg (uint8_t id, usb_msg_t * mess)
{

```

```
BaseType_t    err;
QueueHandle_t handle;
usb_er_t      result;

if (NULL == mess)
{
return USB_APL_ERROR;
}

handle = (*(g_apl_mbx_table[id]));
err = xQueueSend(handle, (const void *) &mess, (TickType_t) (0));

if (pdTRUE == err)
{
    result = USB_APL_OK;
}
else
{
    result = USB_APL_ERROR;
}

return result;
}

/* RTOS-enabled HID example */
void usb_basic_example_rtos (void)
{
    usb_event_info_t * p_mess;
    usb_event_info_t  event_info;
    uint8_t           * p_idle_value;
    uint8_t           sw_data;
    usb_info_t        info;
    fsp_err_t         ret_code = FSP_SUCCESS;
    uint8_t           send_data[16] BSP_ALIGN_VARIABLE(4);
    g_usb_on_usb.open(&g_basic0_ctrl, &g_basic0_cfg);
    set_key_data(g_buf);

    /* Loop back between PC(TerminalSoft) and USB MCU */
    while (1)
    {
```

```
    USB_APL_RCV_MSG(USB_APL_MBX, (usb_msg_t **) &p_mess);

    event_info = *p_mess;

    switch (event_info.event)
    {
    case USB_STATUS_CONFIGURED:
        break;

    case USB_STATUS_WRITE_COMPLETE:
        if (DATA_WRITING == g_status)
        {
            g_status = ZERO_WRITING;
            g_usb_on_usb.write(&g_basic0_ctrl, (uint8_t *) g_zero_data,
DATA_LEN, USB_CLASS_PHID); /* Sending the zero data (8 bytes) */
        }
        else
        {
            g_status = DATA_WRITING;
            usb_cpu_delay_xms(USB_WAIT_1000MS);
            g_usb_on_usb.write(&g_basic0_ctrl, g_buf, DATA_LEN, USB_CLASS_PHID
);
        }
        break;

    case USB_STATUS_REQUEST: /*
Receive Class Request */
        if (USB_SET_REPORT == (event_info.setup.request_type & USB_BREQUEST))
        {
            g_usb_on_usb.read(&g_basic0_ctrl, (uint8_t *) &g_numlock, 2,
USB_CLASS_PHID); /* Get the NumLock data (NumLock data is not used) */
        }
        else if (USB_GET_DESCRIPTOR == (event_info.setup.request_type & USB_BREQUEST))
        {
            if (USB_GET_REPORT_DESCRIPTOR == event_info.setup.request_value)
            {
                g_usb_on_usb.periControlDataSet(&g_basic0_ctrl, (uint8_t *)
g_apl_report,
```

```
USB_RECEIVE_REPORT_DESCRIPTOR);
    }
else if (USB_GET_HID_DESCRIPTOR == event_info.setup.request_value)
    {
for (uint8_t i = 0; i < USB_RECEIVE_HID_DESCRIPTOR; i++)
    {
        send_data[i] = g_apl_configuration[18 + i];
    }
/* Configuration Descriptor address set. */
    g_usb_on_usb.periControlDataSet(&g_basic0_ctrl, send_data,
USB_RECEIVE_HID_DESCRIPTOR);
    }
else
    {
        g_usb_on_usb.periControlStatusSet(&g_basic0_ctrl,
USB_SETUP_STATUS_STALL);
    }
    }
else if (USB_SET_IDLE == (event_info.setup.request_type & USB_BREQUEST))
    {
/* Get SetIdle value */
        p_idle_value = (uint8_t *) &event_info.setup.request_value;
        g_idle = p_idle_value[1];
        g_usb_on_usb.periControlStatusSet(&g_basic0_ctrl,
USB_SETUP_STATUS_ACK);
    }
else if (USB_GET_IDLE == (event_info.setup.request_type & USB_BREQUEST))
    {
        g_usb_on_usb.periControlDataSet(&g_basic0_ctrl, &g_idle, 1);
    }
else if (USB_SET_PROTOCOL == (event_info.setup.request_type & USB_BREQUEST))
    {
        g_usb_on_usb.periControlStatusSet(&g_basic0_ctrl,
```

```
USB_SETUP_STATUS_ACK);
    }
else if (USB_GET_PROTOCOL == (event_info.setup.request_type & USB_BREQUEST))
    {
        g_usb_on_usb.periControlStatusSet(&g_basic0_ctrl,
USB_SETUP_STATUS_STALL);
    }
else
    {
        g_usb_on_usb.periControlStatusSet(&g_basic0_ctrl,
USB_SETUP_STATUS_STALL);
    }
break;
case USB_STATUS_REQUEST_COMPLETE: /* Complete Class Request */
if (USB_SET_IDLE == (event_info.setup.request_type & USB_BREQUEST))
    {
        p_idle_value = (uint8_t *) &event_info.setup.request_value;
        g_idle = p_idle_value[1];
    }
else if (USB_SET_PROTOCOL == (event_info.setup.request_type & USB_BREQUEST))
    {
        /* None */
    }
else
    {
        g_status = DATA_WRITING;
        g_usb_on_usb.write(&g_basic0_ctrl, g_buf, DATA_LEN, USB_CLASS_PHID
);
    }
break;
case USB_STATUS_SUSPEND:
break;
case USB_STATUS_DETACH:
    g_remote_wakeup_enable = USB_OFF;
```

```
break;
default:
break;
    }
    ret_code = g_usb_on_usb.infoGet(&g_basic0_ctrl, &info, NULL);
if (FSP_SUCCESS == ret_code)
    {
        sw_data = usb_cpu_getkeyno();
if (USB_STATUS_SUSPEND == info.device_status)
    {
if (0 != (sw_data & SW_PUSH))
    {
        g_usb_on_usb.remoteWakeup(&g_basic0_ctrl);
    }
    }
    }
}
} /* End of function usb_basic_example_rtos() */
```

## 4.2.54 USB Peripheral Mass Storage Class (r\_usb\_pmsc)

### Modules

This module provides a USB Peripheral Mass Storage Class (PMSC) driver. It implements the [USB PMSC Interface](#).

### Functions

Refer to [USB \(r\\_usb\\_basic\)](#) for the common API (r\_usb\_basic) to be called from the application.

### Detailed Description

## Overview

The r\_usb\_pmsc module combines with the r\_usb\_basic module to provide USB Peripheral It operates as a Mass Storage class driver (hereinafter referred to as PMSC).

The USB peripheral mass storage class driver (PMSC) comprises a USB mass storage class bulk-only transport (BOT) protocol.

When combined with a USB peripheral control driver and media driver, it enables communication with a USB host as a BOT-compatible storage device.

## Features

The r\_usb\_pmsc module has the following key features:

- Storage command control using the BOT protocol
- Supports SFF-8070i (ATAPI)
- Response to mass storage device class requests from a USB host

## Configuration

### Build Time Configurations for r\_usb\_pmsc

The following build time configurations are defined in fsp\_cfg/r\_usb\_pmsc\_cfg.h:

Configuration	Options	Default	Description
Bulk Input Transfer Pipe	<ul style="list-style-type: none"> <li>• USB PIPE1</li> <li>• USB PIPE2</li> <li>• USB PIPE3</li> <li>• USB PIPE4</li> <li>• USB PIPE5</li> </ul>	USB PIPE1	Select the USB pipe to use for bulk input transfers.
Bulk Output Transfer Pipe	<ul style="list-style-type: none"> <li>• USB PIPE1</li> <li>• USB PIPE2</li> <li>• USB PIPE3</li> <li>• USB PIPE4</li> <li>• USB PIPE5</li> </ul>	USB PIPE2	Select the USB pipe to use for bulk output transfers.
Vendor Information	Vendor Information must be 8 bytes long; pad with spaces if shorter.	Vendor	Specify the vendor information field (part of the Inquiry command response).
Product Information	Product Information must be 16 bytes long; pad with spaces if shorter.	Mass Storage	Specify the product information field (part of the Inquiry command response).
Product Revision Level.	Product Revision Level must be 4 bytes long; pad with spaces if shorter.	1.00	Specify the product revision level field (part of the Inquiry command response).
Number of Transfer Sectors	Please enter a number between 1 and 255.	8	Specify the maximum sector size to request with one data transfer.

### Configurations for Middleware > USB > USB PMSC driver on r\_usb\_pmsc

This module can be added to the Stacks tab via New Stack > Middleware > USB > USB PMSC driver on r\_usb\_pmsc.

Configuration	Options	Default	Description
---------------	---------	---------	-------------

Name Name must be a valid C symbol g\_pmsc0 Module name.

Refer to the [USB \(r\\_usb\\_basic\)](#) module for hardware configuration options.

### Clock Configuration

Refer to the [USB \(r\\_usb\\_basic\)](#) module.

### Pin Configuration

Refer to the [USB \(r\\_usb\\_basic\)](#) module.

## Usage Notes

### Class Requests

The class requests supported by this driver are shown below.

Request	Code	Description
Bulk-Only Mass Storage Reset	0xFF	Resets the connection interface to the mass storage device.
Get Max Logical Unit Number	0xFE	Reports the logical numbers supported by the device.

### Storage Commands

This driver supports the following storage commands.

Command	Code	Description
TEST_UNIT_READY	0x00	Checks the state of the peripheral device.
REQUEST_SENSE	0x03	Gets the error information of the previous storage command execution result.
INQUIRY	0x12	Gets the parameter information of the logical unit.
READ_FORMAT_CAPACITY	0x23	Gets the formattable capacity.
READ_CAPACITY	0x25	Gets the capacity information of the logical unit.
READ10	0x28	Reads data.
WRITE10	0x1A	Writes data.
MODE_SENSE10	0x5A	Gets the parameters of the logical unit.

#### Note

A *STALL* or *FAIL* error is sent to the host upon receipt of any command not listed in the above table.



## BOT Protocol Overview

BOT (USB MSC Bulk-Only Transport) is a transfer protocol that encapsulates command, data, and status (results of commands) using only two endpoints (one bulk in and one bulk out). The ATAPI storage commands and the response status are embedded in a Command Block Wrapper (CBW) and a Command Status Wrapper (CSW). The below image shows an overview of how the BOT protocol progresses with command and status data flowing between USB host and peripheral.

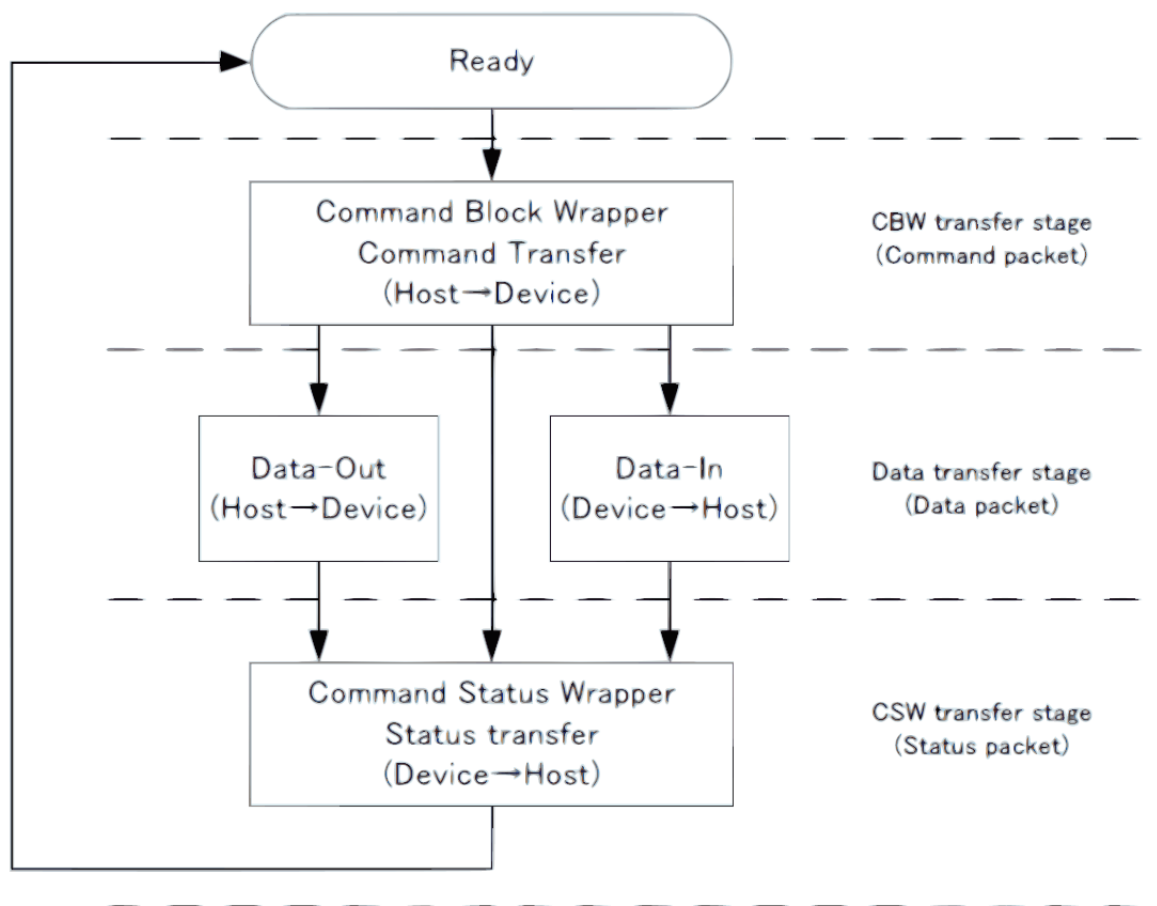


Figure 181: BOT protocol Overview

## Block Media Interface

PMSC implements a block media interface to enable access to higher-level modules. If the block media interface supports multiple media, users can select any media to access.

### Note

When the user develops the storage media driver, be sure to define the instance named "g\_rm\_block\_media0".

## Limitations

1. The driver always returns 0 in response to the GetMaxLun command.
2. The driver supports a sector size of 512 bytes only.
3. The only media currently supported by the block media interface is an SD card. The card must be inserted before initializing the driver.
4. When using DMA for Hi-Speed transfers continuous transfer mode must not be used in the USB Basic driver.

5. The storage area must be formatted before use.
6. When using the SD/MMC Block Media Implementation (rm\_block\_media\_sdmmc), "Card Detection" must be set to "Not Used" in the SD/MMC Host Interface (r\_sdhi) settings.
7. The driver does not support Low-speed.

## Examples

### USB PMSC Example

In this example, when the evaluation board is connected to the host PC it is recognized as a removable disk and reading/writing files is possible. The FAT type is either FAT12, FAT16, or FAT32 depending on the size of the media used.

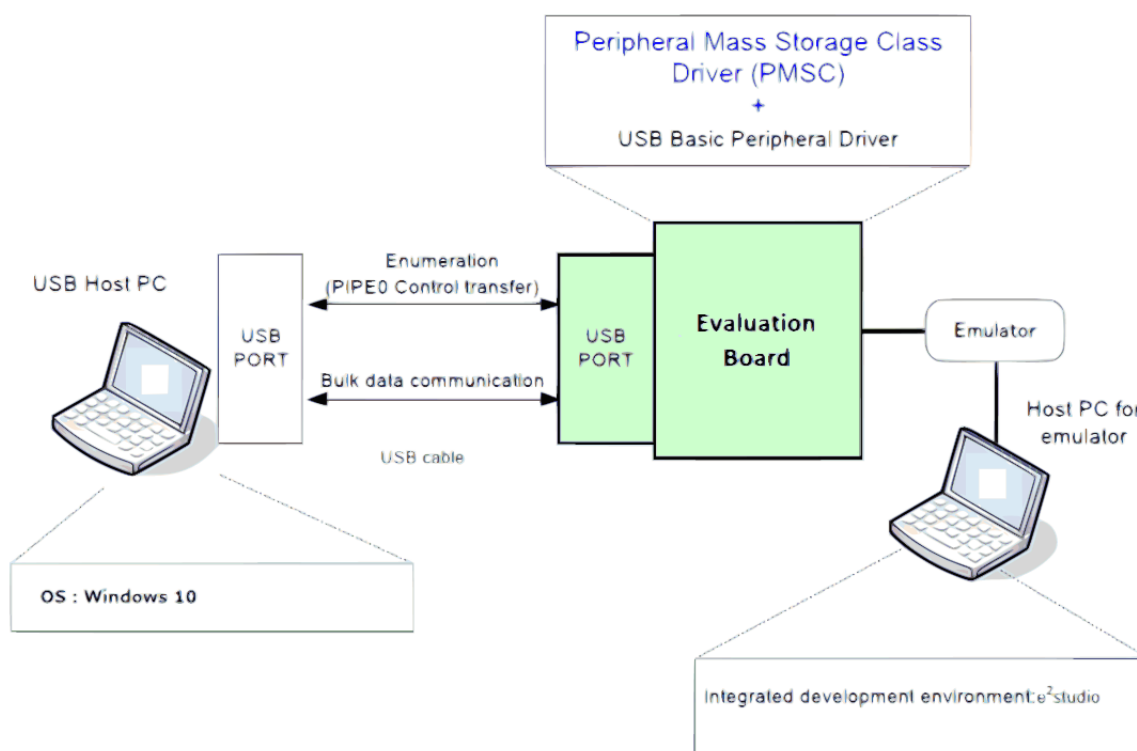


Figure 182: Example Operating Environment

```
void usb_pmsc_example (void)
{
    usb_event_info_t usb_event;
#if (BSP_CFG_RTOS == 2)
    usb_event_info_t * p_mess;
#else
    usb_status_t event;
#endif

    g_usb_on_usb.open(&g_basic0_ctrl, &g_basic0_cfg);
    /* Loop back between PC(TerminalSoft) and USB MCU */
}
```

```
while (1)
{
#if (BSP_CFG_RTOS == 2)
    USB_APL_RCV_MSG(USB_APL_MBX, (usb_msg_t **) &p_mess);
    usb_event = *p_mess;
    /* Analyzing the received message */
    switch (usb_event.event)
#else /* (BSP_CFG_RTOS == 2) */
    g_usb_on_usb.eventGet(&usb_event, &event);
    switch (event)
#endif /* (BSP_CFG_RTOS == 2) */
    {
    case USB_STATUS_CONFIGURED:
        {
        break;
        }
    case USB_STATUS_SUSPEND:
    case USB_STATUS_DETACH:
        {
#if USB_SUPPORT_LPW == USB_APL_ENABLE
// @@ low_power_mcu();
#endif /* USB_SUPPORT_LPW == USB_APL_ENABLE */
        break;
        }
    default:
        {
        break;
        }
    }
} /* End of function usb_main() */
```

## Descriptor

A template for PMSC descriptors can be found in `ra/fsp/src/r_usb_pmsc/r_usb_pmsc_descriptor.c.template`. Also, please be sure to use your vendor ID.

## 4.2.55 Watchdog Timer (r\_wdt)

### Modules

#### Functions

`fsp_err_t` `R_WDT_Refresh` (`wdt_ctrl_t *const p_ctrl`)

`fsp_err_t` `R_WDT_Open` (`wdt_ctrl_t *const p_ctrl`, `wdt_cfg_t const *const p_cfg`)

`fsp_err_t` `R_WDT_StatusClear` (`wdt_ctrl_t *const p_ctrl`, `const wdt_status_t status`)

`fsp_err_t` `R_WDT_StatusGet` (`wdt_ctrl_t *const p_ctrl`, `wdt_status_t *const p_status`)

`fsp_err_t` `R_WDT_CounterGet` (`wdt_ctrl_t *const p_ctrl`, `uint32_t *const p_count`)

`fsp_err_t` `R_WDT_TimeoutGet` (`wdt_ctrl_t *const p_ctrl`, `wdt_timeout_values_t *const p_timeout`)

`fsp_err_t` `R_WDT_CallbackSet` (`wdt_ctrl_t *const p_ctrl`, `void(*p_callback)(wdt_callback_args_t *)`, `void const *const p_context`, `wdt_callback_args_t *const p_callback_memory`)

`fsp_err_t` `R_WDT_VersionGet` (`fsp_version_t *const p_version`)

#### Detailed Description

Driver for the WDT peripheral on RA MCUs. This module implements the [WDT Interface](#).

## Overview

The watchdog timer is used to recover from unexpected errors in an application. The watchdog timer must be refreshed periodically in the permitted count window by the application. If the count is allowed to underflow or refresh occurs outside of the valid refresh period, the WDT resets the device or generates an NMI.

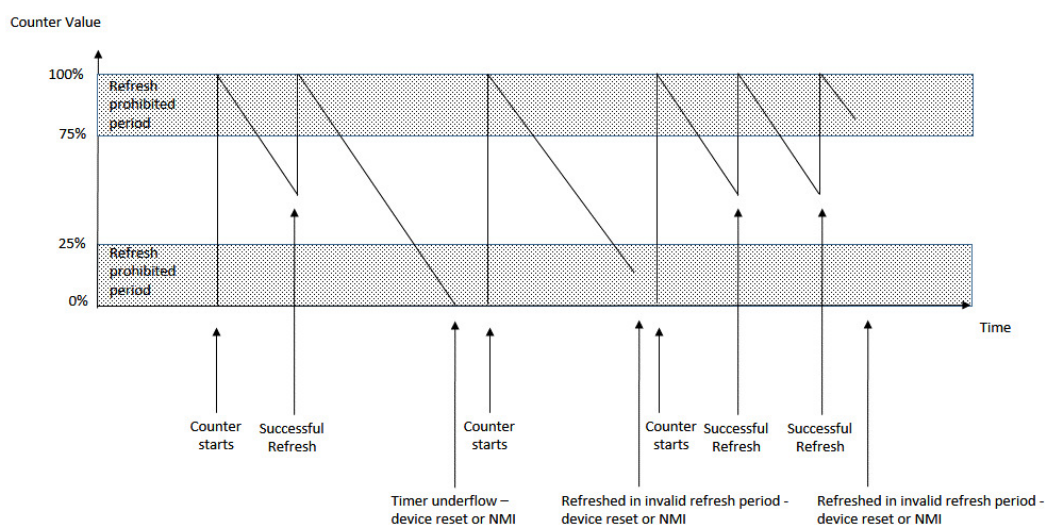


Figure 183: Watchdog Timer Operation Example

## Features

The WDT HAL module has the following key features:

- When the WDT underflows or is refreshed outside of the permitted refresh window, one of the following events can occur:
  - Resetting of the device
  - Generation of an NMI
- The WDT has two supported modes:
  - In auto start mode, the WDT begins counting at reset.
  - In register start mode, the WDT can be started from the application.

## Selecting a Watchdog

RA MCUs have two watchdog peripherals: the watchdog timer (WDT) and the independent watchdog timer (IWDT). When selecting between them, consider these factors:

	WDT	IWDT
Start Mode	The WDT can be started from the application (register start mode) or configured by hardware to start automatically (auto start mode).	The IWDT can only be configured by hardware to start automatically.
Clock Source	The WDT runs off a peripheral clock.	The IWDT has its own clock source which improves safety.

## Configuration

When using register start mode, configure the watchdog timer on the Stacks tab.

### Note

When using auto start mode, configurations on the **Stacks** tab are ignored. Configure the watchdog using the **OFS** settings on the **BSP** tab.

### Build Time Configurations for r\_wdt

The following build time configurations are defined in fsp\_cfg/r\_wdt\_cfg.h:

Configuration	Options	Default	Description
Parameter Checking	<ul style="list-style-type: none"> <li>Default (BSP)</li> <li>Enabled</li> <li>Disabled</li> </ul>	Default (BSP)	If selected code for parameter checking is included in the build.
Register Start NMI Support	<ul style="list-style-type: none"> <li>Enabled</li> <li>Disabled</li> </ul>	Disabled	If enabled, code for NMI support in register start mode is included in the build.

### Configurations for Driver > Monitoring > Watchdog Driver on r\_wdt

This module can be added to the Stacks tab via New Stack > Driver > Monitoring > Watchdog Driver on r\_wdt. Non-secure callable guard functions can be generated for this module by right clicking the module in the RA Configuration tool and checking the "Non-secure Callable" box.

Configuration	Options	Default	Description
Name	Name must be a valid C symbol	g_wdt0	Module name.
Timeout	<ul style="list-style-type: none"> <li>1,024 Cycles</li> <li>4,096 Cycles</li> <li>8,192 Cycles</li> <li>16,384 Cycles</li> </ul>	16,384 Cycles	Select the watchdog timeout in cycles.
Clock Division Ratio	<ul style="list-style-type: none"> <li>PCLK/4</li> <li>PCLK/64</li> <li>PCLK/128</li> <li>PCLK/512</li> <li>PCLK/2048</li> <li>PCLK/8192</li> </ul>	PCLK/8192	Select the watchdog clock divisor.
Window Start Position	<ul style="list-style-type: none"> <li>100% (Window Position Not Specified)</li> <li>75%</li> <li>50%</li> <li>25%</li> </ul>	100% (Window Position Not Specified)	Select the allowed watchdog refresh start point.
Window End Position	<ul style="list-style-type: none"> <li>0% (Window Position Not Specified)</li> </ul>	0% (Window Position Not Specified)	Select the allowed watchdog refresh end

	Specified)		point.
	<ul style="list-style-type: none"> <li>• 25%</li> <li>• 50%</li> <li>• 75%</li> </ul>		
Reset Control	<ul style="list-style-type: none"> <li>• Reset Output</li> <li>• NMI Generated</li> </ul>	Reset Output	Select what happens when the watchdog timer expires.
Stop Control	<ul style="list-style-type: none"> <li>• WDT Count Enabled in Low Power Mode</li> <li>• WDT Count Disabled in Low Power Mode</li> </ul>	WDT Count Disabled in Low Power Mode	Select the watchdog state in low power mode.
NMI Callback	Name must be a valid C symbol	NULL	A user callback function must be provided if the WDT is configured to generate an NMI when the timer underflows or a refresh error occurs. If this callback function is provided, it will be called from the NMI handler each time the watchdog triggers.

## Clock Configuration

The WDT clock is based on the PCLKB frequency. You can set the PCLKB frequency using the **Clocks** tab of the RA Configuration editor or by using the CGC Interface at run-time. The maximum timeout period with PCLKB running at 60 MHz is approximately 2.2 seconds.

## Pin Configuration

This module does not use I/O pins.

# Usage Notes

## NMI Interrupt

The watchdog timer uses the NMI, which is enabled by default. No special configuration is required. When the NMI is triggered, the callback function registered during open is called.

### Note

*When using the WDT in software start mode with NMI and the timer underflows, the WDT status must be reset by calling [R\\_WDT\\_StatusClear](#) before restarting the timer via [R\\_WDT\\_Refresh](#).*

## Period Calculation

The WDT operates from PCLKB. With a PCLKB of 60 MHz, the maximum time from the last refresh to device reset or NMI generation will be just over 2.2 seconds as detailed below.

PLCKB = 60 MHz

Clock division ratio = PCLKB / 8192  
Timeout period = 16384 cycles  
WDT clock frequency = 60 MHz / 8192 = 7.324 kHz  
Cycle time = 1 / 7.324 kHz = 136.53 us  
Timeout = 136.53 us x 16384 cycles = 2.23 seconds

## Limitations

Developers should be aware of the following limitations when using the WDT:

- When using a J-Link debugger the WDT counter does not count and therefore will not reset the device or generate an NMI. To enable the watchdog to count and generate a reset or NMI while debugging, add this line of code in the application:

```
/* (Optional) Enable the WDT to count and generate NMI or reset when the
 * debugger is connected. */
R_DEBUG->DBGSTOPCR_b.DBGSTOP_WDT = 0;
```

- If the WDT is configured to stop the counter in low power mode, then your application must restart the watchdog by calling `R_WDT_Refresh()` after the MCU wakes from low power mode.

## Examples

### WDT Basic Example

This is a basic example of minimal use of the WDT in an application.

```
void wdt_basic_example (void)
{
    fsp_err_t err = FSP_SUCCESS;

    /* In auto start mode, the WDT starts counting immediately when the MCU is powered
    on. */

    /* Initializes the module. */
    err = R_WDT_Open(&g_wdt0_ctrl, &g_wdt0_cfg);

    /* Handle any errors. This function should be defined by the user. */
    handle_error(err);

    /* In register start mode, start the watchdog by calling R_WDT_Refresh. */
    err = R_WDT_Refresh(&g_wdt0_ctrl);
    handle_error(err);

    while (true)
    {
        /* Application work here. */
    }
}
```



```
/* Refresh before the counter underflows to prevent reset or NMI. */
    err = R_WDT_Refresh(&g_wdt0_ctrl);
    handle_error(err);
}
}
```

## WDT Advanced Example

This example demonstrates using a start window and gives an example callback to handle an NMI generated by an underflow or refresh error.

```
#define WDT_TIMEOUT_COUNTS (16384U)
#define WDT_MAX_COUNTER (WDT_TIMEOUT_COUNTS - 1U)
#define WDT_START_WINDOW_75 ((WDT_MAX_COUNTER * 3) / 4)
/* Example callback called when a watchdog NMI occurs. */
void wdt_callback (wdt_callback_args_t * p_args)
{
    FSP_PARAMETER_NOT_USED(p_args);
    fsp_err_t err = FSP_SUCCESS;
    /* (Optional) Determine the source of the NMI. */
    wdt_status_t status = WDT_STATUS_NO_ERROR;
    err = R_WDT_StatusGet(&g_wdt0_ctrl, &status);
    handle_error(err);
    /* (Optional) Log source of NMI and any other debug information. */
    /* (Optional) Clear the error flags. */
    err = R_WDT_StatusClear(&g_wdt0_ctrl, status);
    handle_error(err);
    /* (Register start mode) In register start mode, call R_WDT_Refresh() to
    * continue using the watchdog after an error. */
    err = R_WDT_Refresh(&g_wdt0_ctrl);
    handle_error(err);
    /* (Optional) Issue a software reset to reset the MCU. */
    __NVIC_SystemReset();
}
void wdt_advanced_example (void)
```

```
{
    fsp_err_t err = FSP_SUCCESS;

    /* (Optional) Enable the WDT to count and generate NMI or reset when the
     * debugger is connected. */
    R_DEBUG->DBGSTOPCR_b.DBGSTOP_WDT = 0;

    /* (Optional) Check if the WDTRF flag is set to know if the system is
     * recovering from a WDT reset. */
    if (R_SYSTEM->RSTSR1_b.WDTRF)
    {
        /* Clear the flag. */
        R_SYSTEM->RSTSR1 = 0U;
    }

    /* Open the module. */
    err = R_WDT_Open(&g_wdt0_ctrl, &g_wdt0_cfg);

    /* Handle any errors. This function should be defined by the user. */
    handle_error(err);

    /* Initialize other application code. */
    /* (Register start mode) Call R_WDT_Refresh() to start the WDT in register
     * start mode. Do not call R_WDT_Refresh() in auto start mode unless the
     * counter is in the acceptable refresh window. */
    err = R_WDT_Refresh(&g_wdt0_ctrl);
    handle_error(err);

    while (true)
    {
        /* Application work here. */
        /* (Optional) If there is a chance the application takes less time than
         * the start window, verify the WDT counter is past the start window
         * before refreshing the WDT. */
        uint32_t wdt_counter = 0U;

    do
        {
            /* Read the current WDT counter value. */
            err = R_WDT_CounterGet(&g_wdt0_ctrl, &wdt_counter);
            handle_error(err);
        }
```

```

    } while (wdt_counter >= WDT_START_WINDOW_75);

/* Refresh before the counter underflows to prevent reset or NMI. */
err = R_WDT_Refresh(&g_wdt0_ctrl);
handle_error(err);
}
}

```

## Data Structures

```
struct wdt_instance_ctrl_t
```

## Data Structure Documentation

### ◆ wdt\_instance\_ctrl\_t

```
struct wdt_instance_ctrl_t
```

WDT private control block. DO NOT MODIFY. Initialization occurs when [R\\_WDT\\_Open\(\)](#) is called.

## Function Documentation

### ◆ R\_WDT\_Refresh()

```
fsp_err_t R_WDT_Refresh ( wdt_ctrl_t *const p_ctrl)
```

Refresh the watchdog timer. Implements [wdt\\_api\\_t::refresh](#).

In addition to refreshing the watchdog counter this function can be used to start the counter in register start mode.

Example:

```

/* Refresh before the counter underflows to prevent reset or NMI. */
err = R_WDT_Refresh(&g_wdt0_ctrl);
handle_error(err);

```

### Return values

FSP_SUCCESS	WDT successfully refreshed.
FSP_ERR_ASSERTION	p_ctrl is NULL.
FSP_ERR_NOT_OPEN	Instance control block is not initialized.

### Note

*This function only returns FSP\_SUCCESS. If the refresh fails due to being performed outside of the permitted refresh period the device will either reset or trigger an NMI ISR to run.*

◆ **R\_WDT\_Open()**

```
fsp_err_t R_WDT_Open ( wdt_ctrl_t *const p_ctrl, wdt_cfg_t const *const p_cfg )
```

Configure the WDT in register start mode. In auto-start\_mode the NMI callback can be registered. Implements `wdt_api_t::open`.

This function should only be called once as WDT configuration registers can only be written to once so subsequent calls will have no effect.

Example:

```
/* Initializes the module. */
err = R_WDT_Open(&g_wdt0_ctrl, &g_wdt0_cfg);
```

**Return values**

FSP_SUCCESS	WDT successfully configured.
FSP_ERR_ASSERTION	Null pointer, or one or more configuration options is invalid.
FSP_ERR_ALREADY_OPEN	Module is already open. This module can only be opened once.
FSP_ERR_INVALID_STATE	The security state of the NMI and the module do not match.

**Note**

*In auto start mode the only valid configuration option is for registering the callback for the NMI ISR if NMI output has been selected.*

◆ **R\_WDT\_StatusClear()**

```
fsp_err_t R_WDT_StatusClear ( wdt_ctrl_t *const p_ctrl, const wdt_status_t status )
```

Clear the WDT status and error flags. Implements `wdt_api_t::statusClear`.

Example:

```
/* (Optional) Clear the error flags. */
err = R_WDT_StatusClear(&g_wdt0_ctrl, status);
handle_error(err);
```

**Return values**

FSP_SUCCESS	WDT flag(s) successfully cleared.
FSP_ERR_ASSERTION	Null pointer as a parameter.
FSP_ERR_NOT_OPEN	Instance control block is not initialized.
FSP_ERR_UNSUPPORTED	This function is only valid if the watchdog generates an NMI when an error occurs.

**Note**

*When the WDT is configured to output a reset on underflow or refresh error reading the status and error flags serves no purpose as they will always indicate that no underflow has occurred and there is no refresh error. Reading the status and error flags is only valid when interrupt request output is enabled.*

## ◆ R\_WDT\_StatusGet()

```
fsp_err_t R_WDT_StatusGet ( wdt_ctrl_t*const p_ctrl, wdt_status_t*const p_status )
```

Read the WDT status flags. Implements `wdt_api_t::statusGet`.

Indicates both status and error conditions.

Example:

```
/* (Optional) Determine the source of the NMI. */
wdt_status_t status = WDT_STATUS_NO_ERROR;
err = R_WDT_StatusGet(&g_wdt0_ctrl, &status);
handle_error(err);
```

**Return values**

FSP_SUCCESS	WDT status successfully read.
FSP_ERR_ASSERTION	Null pointer as a parameter.
FSP_ERR_NOT_OPEN	Instance control block is not initialized.
FSP_ERR_UNSUPPORTED	This function is only valid if the watchdog generates an NMI when an error occurs.

**Note**

*When the WDT is configured to output a reset on underflow or refresh error reading the status and error flags serves no purpose as they will always indicate that no underflow has occurred and there is no refresh error. Reading the status and error flags is only valid when interrupt request output is enabled.*

## ◆ R\_WDT\_CounterGet()

```
fsp_err_t R_WDT_CounterGet ( wdt_ctrl_t*const p_ctrl, uint32_t*const p_count )
```

Read the current count value of the WDT. Implements `wdt_api_t::counterGet`.

Example:

```
/* Read the current WDT counter value. */
err = R_WDT_CounterGet(&g_wdt0_ctrl, &wdt_counter);
handle_error(err);
```

**Return values**

FSP_SUCCESS	WDT current count successfully read.
FSP_ERR_ASSERTION	Null pointer passed as a parameter.
FSP_ERR_NOT_OPEN	Instance control block is not initialized.

◆ **R\_WDT\_TimeoutGet()**

```
fsp_err_t R_WDT_TimeoutGet ( wdt_ctrl_t *const p_ctrl, wdt_timeout_values_t *const p_timeout )
```

Read timeout information for the watchdog timer. Implements `wdt_api_t::timeoutGet`.

**Return values**

FSP_SUCCESS	WDT timeout information retrieved successfully.
FSP_ERR_ASSERTION	Null Pointer.
FSP_ERR_NOT_OPEN	Instance control block is not initialized.

◆ **R\_WDT\_CallbackSet()**

```
fsp_err_t R_WDT_CallbackSet ( wdt_ctrl_t *const p_ctrl, void(*)(wdt_callback_args_t *) p_callback, void const *const p_context, wdt_callback_args_t *const p_callback_memory )
```

Updates the user callback and has option of providing memory for callback structure. Implements `wdt_api_t::callbackSet`

**Return values**

FSP_SUCCESS	Callback updated successfully.
FSP_ERR_ASSERTION	A required pointer is NULL.
FSP_ERR_NOT_OPEN	The control block has not been opened.

◆ **R\_WDT\_VersionGet()**

```
fsp_err_t R_WDT_VersionGet ( fsp_version_t *const p_version)
```

Return WDT HAL driver version. Implements `wdt_api_t::versionGet`.

**Return values**

FSP_SUCCESS	Version information successfully read.
FSP_ERR_ASSERTION	Null pointer passed as a parameter

**4.2.56 AWS PKCS11 PAL (rm\_aws\_pkcs11\_pal)**

## Modules

PKCS#11 PAL layer implementation for use by FreeRTOS TLS.

## Overview

*Note*

*The PKCS#11 PAL Interface does not provide any interfaces to the user. Consult the AWS documentation for more info: <https://docs.aws.amazon.com/freertos/latest/portingguide/afr-porting-pkcs.html>.*

## Configuration

There is no user configuration for this module

### Data Flash Usage

The current implementation utilizes 16K of Data flash of which 8K is used for storage and the other 8K is used for backup.

## Usage Notes

### Limitations

- Interrupts are disabled while write or erase operations are being performed.
- Credentials are stored on data flash with no tamper protection other than SHA256 for integrity.
- Credential access is not limited in any way. The credential access and tamper issues can be resolved by updating the implementation to use code flash instead of data flash and using the Secure MPU to control access to it.

### 4.2.57 AWS PKCS11 PAL LITTLEFS (rm\_aws\_pkcs11\_pal\_littlefs)

[Modules](#)

PKCS#11 PAL LittleFS layer implementation for use by FreeRTOS TLS.

## Overview

*Note*

*The PKCS#11 PAL LittleFS Interface does not provide any interfaces to the user. Consult the AWS documentation for more info: <https://docs.aws.amazon.com/freertos/latest/portingguide/afr-porting-pkcs.html>.*



## Configuration

There is no user configuration for this module

## Usage Notes

The current implementation utilizes [LittleFS Flash Port \(rm\\_littlefs\\_flash\)](#) for storage.

### Limitations

- Credential access is not limited in any way.

## 4.2.58 Bluetooth Low Energy Abstraction (rm\_ble\_abs)

### Modules

#### Functions

`fsp_err_t` [RM\\_BLE\\_ABS\\_Open](#) (`ble_abs_ctrl_t *const p_ctrl`, `ble_abs_cfg_t const *const p_cfg`)

`fsp_err_t` [RM\\_BLE\\_ABS\\_Close](#) (`ble_abs_ctrl_t *const p_ctrl`)  
Close the BLE channel. Implements `ble_abs_api_t::close`. [More...](#)

`fsp_err_t` [RM\\_BLE\\_ABS\\_Reset](#) (`ble_abs_ctrl_t *const p_ctrl`, `ble_event_cb_t init_callback`)

`fsp_err_t` [RM\\_BLE\\_ABS\\_VersionGet](#) (`fsp_version_t *const p_version`)

`fsp_err_t` [RM\\_BLE\\_ABS\\_StartLegacyAdvertising](#) (`ble_abs_ctrl_t *const p_ctrl`, `ble_abs_legacy_advertising_parameter_t const *const p_advertising_parameter`)

`fsp_err_t` [RM\\_BLE\\_ABS\\_StartExtendedAdvertising](#) (`ble_abs_ctrl_t *const p_ctrl`, `ble_abs_extend_advertising_parameter_t const *const p_advertising_parameter`)

`fsp_err_t` [RM\\_BLE\\_ABS\\_StartNonConnectableAdvertising](#) (`ble_abs_ctrl_t *const p_ctrl`, `ble_abs_non_connectable_advertising_parameter_t const *const p_advertising_parameter`)

`fsp_err_t` [RM\\_BLE\\_ABS\\_StartPeriodicAdvertising](#) (`ble_abs_ctrl_t *const p_ctrl`, `ble_abs_periodic_advertising_parameter_t const *const p_advertising_parameter`)

`fsp_err_t` [RM\\_BLE\\_ABS\\_StartScanning](#) (`ble_abs_ctrl_t *const p_ctrl`, `ble_abs_scan_parameter_t const *const p_scan_parameter`)

```
fsp_err_t RM_BLE_ABS_CreateConnection (ble_abs_ctrl_t *const p_ctrl,
ble_abs_connection_parameter_t const *const
p_connection_parameter)
```

```
fsp_err_t RM_BLE_ABS_SetLocalPrivacy (ble_abs_ctrl_t *const p_ctrl, uint8_t
const *const p_lc_irk, uint8_t privacy_mode)
```

```
fsp_err_t RM_BLE_ABS_StartAuthentication (ble_abs_ctrl_t *const p_ctrl,
uint16_t connection_handle)
```

## Detailed Description

Middleware for the Bluetooth peripheral on RA MCUs. This module implements the [BLE ABS Interface](#).

## Overview

This module provides BLE GAP functionality that complies with the Bluetooth Core Specification version 5.0 specified by the Bluetooth SIG. This module is configured via the [QE for BLE](#). QE for BLE provides standard services defined by standardization organization and custom services defined by user. [Bluetooth LE Profile API Document User's Manual](#) describes the APIs for standard services.

## Features

The Bluetooth Low Energy Abstraction module supports the following features:

- following GAP Role support
  - Central: The device that sends a connection request to the Peripheral device.
  - Peripheral: The device that accepts a connection request from Central and establishes a connection.
  - Observer : The device that scans for advertising.
  - Broadcaster : The device that sends advertising.
- LE 2M PHY
  - BLE communication is supported on the 2 Msym/s PHY.
- LE Coded PHY -Supports BLE communication on the Coded PHY. This enables communication over longer distances than 1M PHY and 2M PHY.
- LE Advertising Extensions
  - Up to four independent adverts can be executed simultaneously.
  - The size of Advertising Data/Scan Response Data has been expanded to a maximum of 1650 bytes.
  - Periodic Advertising is available.
- LE Channel Selection Algorithm #2
  - With the hopping channel selection algorithm added in Version 5.0, the machine that selects the channel It is possible.
- High Duty Cycle Non-Connectable Advertising
  - The ability to support non-connectable advertising with a minimum interval of up to 20 msec.
- LE Secure Connections
  - Elliptic curve Diffie-Hellman key sharing (ECDH) for pairing with passive eavesdropping support.
- Link Layer privacy

- This feature avoids being tracked by other BLE devices by periodically changing the Bluetooth device address.
- Link Layer Extended Scanner Filter policies
  - Scan Filter support for Resolvable private addresses.
- LE Data Packet Length Extension
  - This function expands the packet size of BLE data communications. It is possible to scale up to 251 bytes.
- LE L2CAP Connection Oriented Channel Support
  - The ability to support communication using the L2CAP credit based flow control channel.
- Low Duty Cycle Directed Advertising
  - The ability to support the advertising of the Low Duty Cycle for reconnecting to a known device.
- LE Link Layer Topology
  - It supports both Master and Slave roles and can operate as Master when connected to one remote device and as Slave when connected to another remote device.
- LE Ping
  - This function checks whether the link is maintained or not by requesting the transmission of packets containing MIC after link encryption.

### BLE Library Configuration

There are three types of BLE Protocol Stacks, and the functions provided are different depending on the type of BLE Protocol Stack you select.

BLE library feature	All	Balance	Compact
GAP Role	Central Peripheral Observer Broadcaster	Central Peripheral Observer Broadcaster	Peripheral Broadcaster
LE 2M PHY	Yes	Yes	No
LE Coded PHY	Yes	Yes	No
LE Advertising Extensions	Yes	No	No
LE Channel Selection Algorithm #2	Yes	Yes	No
High Duty Cycle Non-Connectable Advertising	Yes	Yes	Yes
LE Secure Connections	Yes	Yes	Yes
Link Layer privacy	Yes	Yes	Yes
Link Layer Extended Scanner Filter policies	Yes	Yes	No
LE Data Packet Length Extension	Yes	Yes	Yes
LE L2CAP Connection Oriented Channel Support	Yes	No	No

Low Duty Cycle Directed Advertising	Yes	Yes	Yes
LE Link Layer Topology	Yes	Yes	No
LE Ping	Yes	Yes	Yes
32-bit UUID Support in LE	Yes	Yes	Yes

## Target Devices

The Bluetooth Low Energy Abstraction module supports the following devices.

- RA4W1

## Configuration

### Build Time Configurations for rm\_ble\_abs

The following build time configurations are defined in fsp\_cfg/rm\_ble\_abs\_cfg.h:

Configuration	Options	Default	Description
Debug Public Address	Manual Entry	{0xFF,0xFF,0xFF,0x50,0x90,0x74}	Public Address of firmware initial value.
Debug Random Address	Manual Entry	{0xFF,0xFF,0xFF,0xFF,0xFF,0xFF}	Random Address of firmware initial value.
Maximum number of connections	Value must be greater than 1	7	Maximum number of connections.
Maximum connection data length	Value must be greater than 27	251	Maximum connection data length.
Maximum advertising data length	Value must be greater than 31	1650	Maximum advertising data length.
Maximum advertising set number	Value must be greater than 1	4	Maximum advertising set number.
Maximum periodic sync set number.	Value must be greater than 1	2	Maximum periodic sync set number.
Store Security Data	<ul style="list-style-type: none"> <li>• Disable</li> <li>• Enable</li> </ul>	Disable	Store Security Data in DataFlash.
Data Flash Block for Security Data	Value must be greater than 0	0	Data Flash Block for Security Data Management.
Remote Device Bonding Number	Value must be greater than 1	7	Number of remote device bonding information.
Connection Event Start Notify	<ul style="list-style-type: none"> <li>• Disable notify</li> <li>• Enable notify</li> </ul>	Disable notify	Set Connection event start notify enable/disable.

Connection Event Close Notify	<ul style="list-style-type: none"> <li>• Disable notify</li> <li>• Enable notify</li> </ul>	Disable notify	Set Connection event close notify enable/disable.
Advertising Event Start Notify	<ul style="list-style-type: none"> <li>• Disable notify</li> <li>• Enable notify</li> </ul>	Disable notify	Set Advertising event start notify enable/disable.
Advertising Event Close Notify	<ul style="list-style-type: none"> <li>• Disable notify</li> <li>• Enable notify</li> </ul>	Disable notify	Set Advertising event close notify enable/disable.
Scanning Event Start Notify	<ul style="list-style-type: none"> <li>• Disable notify</li> <li>• Enable notify</li> </ul>	Disable notify	Set Scanning event start notify enable/disable.
Scanning Event Close Notify	<ul style="list-style-type: none"> <li>• Disable notify</li> <li>• Enable notify</li> </ul>	Disable notify	Set Scanning event close notify enable/disable.
Initiating Event Start Notify	<ul style="list-style-type: none"> <li>• Disable notify</li> <li>• Enable notify</li> </ul>	Disable notify	Set Initiating event start notify enable/disable.
Initiating Event Close Notify	<ul style="list-style-type: none"> <li>• Disable notify</li> <li>• Enable notify</li> </ul>	Disable notify	Set Initiating event close notify enable/disable.
RF Deep Sleep Start Notify	<ul style="list-style-type: none"> <li>• Disable notify</li> <li>• Enable notify</li> </ul>	Disable notify	Set RF_DEEP_SLEEP start notify enable/disable.
RF Deep Sleep Wakeup Notify	<ul style="list-style-type: none"> <li>• Disable notify</li> <li>• Enable notify</li> </ul>	Disable notify	Set RF_DEEP_SLEEP wakeup notify enable/disable.
Bluetooth dedicated clock	Value must be greater than 0	6	Load capacitance adjustment.
DC-DC Converter	<ul style="list-style-type: none"> <li>• Disable DC-DC Converter</li> <li>• Enable DC-DC Converter</li> </ul>	Disable DC-DC Converter	Set DC-DC converter for RF part.
Slow Clock Source	<ul style="list-style-type: none"> <li>• Use RF_LOCO</li> <li>• Use External 32.768kHz</li> </ul>	Use RF_LOCO	Set slow clock source for RF part.
MCU CLKOUT Port	<ul style="list-style-type: none"> <li>• P109</li> <li>• P205</li> </ul>	P109	When BLE_ABS_CFG_RF_EXTERNAL_32K_ENABLE = 1, Set port of MCU CLKOUT.
MCU CLKOUT Frequency Output	<ul style="list-style-type: none"> <li>• MCU CLKOUT frequency 32.768kHz</li> <li>• MCU CLKOUT frequency 16.384kHz</li> </ul>	MCU CLKOUT frequency 32.768kHz	When BLE_ABS_CFG_RF_EXTERNAL_32K_ENABLE = 1, set frequency output from CLKOUT of MCU part.

Sleep Clock Accuracy(SCA)	Value must be greater than 0	250	When BLE_ABS_CFG_RF_EXTERNAL_32K_ENAB LE = 1, set Sleep Clock Accuracy(SCA) for RF slow clock.
Transmission Power Maximum Value	<ul style="list-style-type: none"> <li>max +0dBm</li> <li>max +4dBm</li> </ul>	max +4dBm	Set transmission power maximum value.
Transmission Power Default Value	<ul style="list-style-type: none"> <li>High 0dBm(Transmission Power Maximum Value = +0dBm) / +4dBm(Transmission Power Maximum Value = +4dBm)</li> <li>Mid 0dBm(Transmission Power Maximum Value = +0dBm) / 0dBm(Transmission Power Maximum Value = +4dBm)</li> <li>Low -18dBm(Transmission Power Maximum Value = +0dBm) / -20dBm(Transmission Power Maximum Value = +4dBm)</li> </ul>	High 0dBm(Transmission Power Maximum Value = +0dBm) / +4dBm(Transmission Power Maximum Value = +4dBm)	Set default transmit power. Default transmit power is dependent on the configuration of Maximum transmission power(BLE_ABS_CFG_RF_MAX_TX_POW).
CLKOUT_RF Output	<ul style="list-style-type: none"> <li>No output</li> <li>4MHz output</li> <li>2MHz output</li> <li>1MHz output</li> </ul>	No output	Set CLKOUT_RF output setting.
RF_DEEP_SLEEP Transition	<ul style="list-style-type: none"> <li>Disable</li> <li>Enable</li> </ul>	Enable	Set RF_DEEP_SLEEP transition.
MCU Main Clock Frequency	Value must be greater than 1000	8000	Set MCU Main Clock Frequency (kHz). Set clock source according to your board environment. HOCO: don't care. / Main Clock: 1000 to 20000 kHz / PLL Circuit: 4000 to 12500 kHz
Code Flash(ROM) Device Data Block	Value must be greater than -1	255	Device specific data block on Code Flash (ROM).

Device Specific Data Flash Block	Value must be greater than -1	-1	Device specific data block on E2 Data Flash.
MTU Size Configured	Value must be greater than 23	247	MTU Size configured by GATT MTU exchange procedure.
Timer Slot Maximum Number	Manual Entry	10	The maximum number of timer slot.
Parameter Checking	<ul style="list-style-type: none"> <li>• Default (BSP)</li> <li>• Enabled</li> <li>• Disabled</li> </ul>	Default (BSP)	Specify whether to include code for API parameter checking. Valid settings include.

### Configurations for Driver > Network > BLE Abstraction Driver on rm\_ble\_abs

This module can be added to the Stacks tab via New Stack > Driver > Network > BLE Abstraction Driver on rm\_ble\_abs.

Configuration	Options	Default	Description
Interrupts > Callback provided when an ISR occurs	Name must be a valid C symbol	NULL	Callback provided when BLE ABS ISR occurs
Name	Name must be a valid C symbol	g_ble_abs0	Module name.
Gap callback	Name must be a valid C symbol	gap_cb	A user callback function must be provided if the BLE_ABS is configured to generate a GAP. If QE is used, set to NULL.
Vendor specific callback	Name must be a valid C symbol	vs_cb	A user callback function must be provided if the BLE_ABS is configured to generate a Vendor Specific. If QE is used, set to NULL.
Pairing parameters	Name must be a valid C symbol	gs_abs_pairing_param	Set pairing parameters.
GATT server callback parameter	Name must be a valid C symbol	gs_abs_gatts_cb_param	Set GATT server callback parameter. If QE is used, set to NULL.
GATT server callback number	Must be a valid number	2	The number of GATT Server callback functions.
GATT client callback parameter	Name must be a valid C symbol	gs_abs_gattc_cb_param	Set GATT client callback parameter. If

			QE is used, set to NULL.
GATT client callback number	Must be a valid number	2	The number of GATT Server callback functions.
IO capabilities of local device.	<ul style="list-style-type: none"> <li>• BLE_GAP_IOCAP_DISPLAY_ONLY</li> <li>• BLE_GAP_IOCAP_DISPLAY_YESNO</li> <li>• BLE_GAP_IOCAP_KEYBOARD_ONLY</li> <li>• BLE_GAP_IOCAP_NOINPUT_NOOUTPUT</li> <li>• BLE_GAP_IOCAP_KEYBOARD_DISPLAY</li> </ul>	BLE_GAP_IOCAP_NOINPUT_NOOUTPUT	Select IO capabilities of local device.
MITM protection policy.	<ul style="list-style-type: none"> <li>• BLE_GAP_SEC_MITM_BEST Effort</li> <li>• BLE_GAP_SEC_MITM_STRICT</li> </ul>	BLE_GAP_SEC_MITM_BEST Effort	Select MITM protection policy.
Determine whether to accept only Secure Connections or not.	<ul style="list-style-type: none"> <li>• BLE_GAP_SC_BEST Effort</li> <li>• BLE_GAP_SC_STRICT</li> </ul>	BLE_GAP_SC_BEST Effort	Select determine whether to accept only Secure Connections or not.
Type of keys to be distributed from local device.	<ul style="list-style-type: none"> <li>• BLE_GAP_KEY_DIST_ENCKEY</li> <li>• BLE_GAP_KEY_DIST_IDKEY</li> <li>• BLE_GAP_KEY_DIST_SIGNKEY</li> </ul>	BLE_GAP_KEY_DIST_ENCKEY	Select type of keys to be distributed from local device.
Type of keys which local device requests a remote device to distribute.	Must be a valid number	0	Set type of keys which local device requests a remote device to distribute.
Maximum LTK size.	Must be a valid number	16	Set Maximum LTK size.

## Clock Configuration

### Note

*System clock (ICLK): 8 MHz or more*

*Peripheral module clock A (PCLKA): 8MHz or more*

*The BLE Protocol Stack is optimized for ICLK and PCLKA frequencies of 32 MHz.*

*It is recommended that the clock be set so that the ICLK and PCLKA frequencies are 32MHz in order to get the best performance from the BLE.*

## Pin Configuration



This module does not use I/O pins.

## Usage Notes

### Limitations

Developers should be aware of the following limitations when using the BLE\_ABS:

## Examples

### BLE\_ABS Basic Example

This is a basic example of minimal use of the BLE\_ABS in an application.

```
#define BLE_ABS_EVENT_FLAG_STACK_ON (0x01 << 0)
#define BLE_ABS_EVENT_FLAG_CONN_IND (0x01 << 1)
#define BLE_ABS_EVENT_FLAG_ADV_ON (0x01 << 2)
#define BLE_ABS_EVENT_FLAG_ADV_OFF (0x01 << 3)
#define BLE_ABS_EVENT_FLAG_DISCONN_IND (0x01 << 4)
#define BLE_ABS_EVENT_FLAG_RSLV_LIST_CONF_COMP (0x01 << 5)
#define BLE_ABS_EXAMPLE_SHORTENED_LOCAL_NAME 'E', 'x', 'a', 'm', 'p', 'l', 'e'
#define BLE_ABS_EXAMPLE_COMPLETE_LOCAL_NAME 'T', 'E', 'S', 'T', '_', 'E', 'x', 'a',
'm', 'p', 'l', 'e'
#define BLE_ABS_EXAMPLE_SLOW_ADVERTISING_INTERVAL (0x00000640)
void ble_abs_peripheral_example (void)
{
    fsp_err_t      err      = FSP_SUCCESS;
    volatile uint32_t timeout = UINT16_MAX * UINT8_MAX * 8;
    uint8_t * p_lc_irk      = NULL;
    uint8_t  privacy_mode = BLE_GAP_NET_PRIV_MODE;
    uint8_t advertising_data[] =
    {
        /* Flags */
        0x02,
        0x01,
        (0x1a),
        /* Shortened Local Name */
        0x08,
        0x08,
```

```
    BLE_ABS_EXAMPLE_SHORTENED_LOCAL_NAME ,
};

/* Scan Response Data */
uint8_t scan_response_data[] =
{
/* Complete Local Name */
    0x0D,
    0x09,
    BLE_ABS_EXAMPLE_COMPLETE_LOCAL_NAME ,
};

ble_abs_legacy_advertising_parameter_t legacy_advertising_parameter =
{
    .p_peer_address          =
NULL,
    .slow_advertising_interval =
BLE_ABS_EXAMPLE_SLOW_ADVERTISING_INTERVAL,
    .slow_advertising_period  =
0x0000,
    .p_advertising_data       =
advertising_data,
    .advertising_data_length  = sizeof
(advertising_data),
    .p_scan_response_data     =
scan_response_data,
    .scan_response_data_length = sizeof
(scan_response_data),
    .advertising_filter_policy = BLE_ABS_ADVERTISING_FILTER_ALLOW_ANY
,
    .advertising_channel_map   = (BLE_GAP_ADV_CH_37 | BLE_GAP_ADV_CH_38 |
BLE_GAP_ADV_CH_39),
    .own_bluetooth_address_type = BLE_GAP_ADDR_PUBLIC
,
    .own_bluetooth_address     = {0},
};
```

```
    g_ble_event_flag = 0;
/* Open the module. */
    err = RM_BLE_ABS_Open(&g_ble_abs0_ctrl, &g_ble_abs0_cfg);
/* Handle any errors. This function should be defined by the user. */
    handle_error(err);
/* Wait BLE_GAP_EVENT_STACK_ON event is notified. */
while (!(BLE_ABS_EVENT_FLAG_STACK_ON & g_ble_event_flag) && (--timeout > 0U))
    {
    R_BLE_Execute();
    }
/* Set local privacy. */
    err = RM_BLE_ABS_SetLocalPrivacy(&g_ble_abs0_ctrl, p_lc_irk, privacy_mode);
/* Handle any errors. This function should be defined by the user. */
    handle_error(err);
/* Wait BLE_GAP_EVENT_RSLV_LIST_CONF_COMP event is notified. */
while (!(BLE_ABS_EVENT_FLAG_RSLV_LIST_CONF_COMP & g_ble_event_flag) && (--timeout >
0U))
    {
    R_BLE_Execute();
    }
    time_out_handle_error(timeout);
    g_ble_event_flag = 0;
    timeout = UINT16_MAX * UINT8_MAX * 8;
/* Start advertising. */
    err = RM_BLE_ABS_StartLegacyAdvertising(&g_ble_abs0_ctrl,
&legacy_advertising_parameter);
/* Handle any errors. This function should be defined by the user. */
    handle_error(err);
while (!(BLE_ABS_EVENT_FLAG_CONN_IND & g_ble_event_flag) && (--timeout > 0U))
    {
    if (BLE_ABS_EVENT_FLAG_ADV_OFF & g_ble_event_flag)
        {
        /* Restart advertise, when stop advertising. */
        err = RM_BLE_ABS_StartLegacyAdvertising(&g_ble_abs0_ctrl,
```

```
&legacy_advertising_parameter);
if (FSP_SUCCESS == err)
{
    g_ble_event_flag &= (uint16_t) ~BLE_ABS_EVENT_FLAG_ADV_OFF;
}
else if (FSP_ERR_INVALID_STATE == err)
{
    /* BLE driver state is busy. */
    ;
}
else
{
    /* Handle any errors. This function should be defined by the user. */
    handle_error(err);
}
}
else if ((timeout % BLE_ABS_RETRY_INTERVAL) == 0U)
{
    /* Stop advertising after a certain amount of time */
    R_BLE_GAP_StopAdv(g_advertising_handle);
}
else
{
    ;
}
R_BLE_Execute();
}
time_out_handle_error(timeout);
/* Clean up & Close BLE driver */
g_ble_event_flag = 0;
/* Close BLE driver */
err = RM_BLE_ABS_Close(&g_ble_abs0_ctrl);
/* Handle any errors. This function should be defined by the user. */
handle_error(err);
```

```
}

#define BLE_ABS_EVENT_FLAG_STACK_ON (0x01 << 0)
#define BLE_ABS_EVENT_FLAG_CONN_IND (0x01 << 1)
#define BLE_ABS_EVENT_FLAG_ADV_REPT_IND (0x01 << 2)
#define BLE_ABS_EVENT_FLAG_ADV_OFF (0x01 << 3)
#define BLE_ABS_EVENT_FLAG_PAIRING_COMP (0x01 << 4)
#define BLE_ABS_EVENT_FLAG_SCAN_TIMEOUT (0x01 << 5)
#define BLE_ABS_EXAMPLE_FAST_SCAN_INTERVAL (0x0060)
#define BLE_ABS_EXAMPLE_FAST_SCAN_WINDOW (0x0030)
#define BLE_ABS_EXAMPLE_SLOW_SCAN_INTERVAL (0x0800)
#define BLE_ABS_EXAMPLE_SLOW_SCAN_WINDOW (0x0012)
#define BLE_ABS_EXAMPLE_FAST_SCAN_PERIOD (0x0BB8)
#define BLE_ABS_EXAMPLE_SLOW_SCAN_PERIOD (0x0000)
#define BLE_ABS_EXAMPLE_CONNECTION_INTERVAL (0x0028)
#define BLE_ABS_EXAMPLE_SUPERVISION_TIMEOUT (0x0200)
#define BLE_ABS_SCAN_FILTER_DATA_LENGTH (12)
/* Scan filter data (data type: Complete Local Name) */
static uint8_t g_filter_data[] =
{
    BLE_ABS_EXAMPLE_COMPLETE_LOCAL_NAME
};
/* Connection phy parameters */
ble_abs_connection_phy_parameter_t g_connection_phy_parameter =
{
    .connection_interval = BLE_ABS_EXAMPLE_CONNECTION_INTERVAL, /* 50.0(ms) */
    .supervision_timeout = BLE_ABS_EXAMPLE_SUPERVISION_TIMEOUT, /* 5,120(ms) */
    .connection_slave_latency = 0x0000,
};
/* Connection device address */
ble_device_address_t g_connection_device_address;
/* Connection parameters */
ble_abs_connection_parameter_t g_connection_parameter =
{
```

```

.p_connection_phy_parameter_1M = &g_connection_phy_parameter,
.p_device_address              = &g_connection_device_address,
.filter_parameter              = BLE_GAP_INIT_FILT_USE_ADDR,
.connection_timeout            = 0x05, /* 5(s) */
};

void ble_abs_central_example (void)
{
    fsp_err_t      err      = FSP_SUCCESS;
    volatile uint32_t timeout = UINT16_MAX * UINT8_MAX * 8;
    g_connection_handle = BLE_GAP_INVALID_CONN_HDL;
    static ble_abs_scan_phy_parameter_t scan_phy_parameter =
    {
        .fast_scan_interval = BLE_ABS_EXAMPLE_FAST_SCAN_INTERVAL, /* 60.0(ms) */
        .fast_scan_window   = BLE_ABS_EXAMPLE_FAST_SCAN_WINDOW,   /* 30.0(ms) */
        .slow_scan_interval = BLE_ABS_EXAMPLE_SLOW_SCAN_INTERVAL, /* 1,280.0(ms) */
        .slow_scan_window   = BLE_ABS_EXAMPLE_SLOW_SCAN_WINDOW,   /* 11.25(ms) */
        .scan_type           = BLE_GAP_SCAN_ACTIVE
    };
    /* Scan parameters */
    ble_abs_scan_parameter_t scan_parameter =
    {
        .p_phy_parameter_1M      = &scan_phy_parameter,
        .fast_scan_period        = BLE_ABS_EXAMPLE_FAST_SCAN_PERIOD, /* 30,000(ms)
*/
        .slow_scan_period        = BLE_ABS_EXAMPLE_SLOW_SCAN_PERIOD,
        .p_filter_data           = g_filter_data,
        .filter_data_length      = (uint16_t) BLE_ABS_SCAN_FILTER_DATA_LENGTH,
        .filter_ad_type          = 0x09, /* Data type:
Complete Local Name */
        .device_scan_filter_policy = BLE_GAP_SCAN_ALLOW_ADV_ALL,
        .filter_duplicate        = BLE_GAP_SCAN_FILT_DUPLIC_ENABLE,
    };
    g_ble_event_flag = 0;
    /* Open the module. */

```

```
err = RM_BLE_ABS_Open(&g_ble_abs0_ctrl, &g_ble_abs0_cfg);
/* Handle any errors. This function should be defined by the user. */
handle_error(err);
/* Connection parameters */
while (!(BLE_ABS_EVENT_FLAG_STACK_ON & g_ble_event_flag) && (--timeout > 0U))
{
R_BLE_Execute();
}
/* Start scanning. */
err = RM_BLE_ABS_StartScanning(&g_ble_abs0_ctrl, &scan_parameter);
/* Handle any errors. This function should be defined by the user. */
handle_error(err);
while ((BLE_ABS_EVENT_FLAG_ADV_REPT_IND & g_ble_event_flag) && (--timeout > 0U))
{
if ((BLE_ABS_EVENT_FLAG_SCAN_TIMEOUT & g_ble_event_flag) || (BLE_GAP_EVENT_SCAN_OFF
& g_ble_event_flag))
{
g_ble_event_flag &= (uint16_t) ~BLE_ABS_EVENT_FLAG_ADV_OFF;
g_ble_event_flag &= (uint16_t) ~BLE_ABS_EVENT_FLAG_SCAN_TIMEOUT;
/* Start scanning. */
err = RM_BLE_ABS_StartScanning(&g_ble_abs0_ctrl, &scan_parameter);
/* Handle any errors. This function should be defined by the user. */
handle_error(err);
}
else if ((timeout % BLE_ABS_RETRY_INTERVAL) == 0U)
{
/* Stop scanning after a certain amount of time */
R_BLE_GAP_StopScan();
}
else
{
;
}
R_BLE_Execute();
```

```
    }
    g_ble_event_flag = 0;
    time_out_handle_error(timeout);
    timeout = UINT16_MAX * UINT8_MAX * 8;
    /* Create connection with remote device. */
    err = RM_BLE_ABS_CreateConnection(&g_ble_abs0_ctrl, &g_connection_parameter);
    /* Handle any errors. This function should be defined by the user. */
    handle_error(err);
    /* Wait BLE_GAP_EVENT_CONN_IND event is notified. */
    while (!(BLE_ABS_EVENT_FLAG_CONN_IND & g_ble_event_flag) && (--timeout > 0U))
    {
        R_BLE_Execute();
    }
    time_out_handle_error(timeout);
    g_ble_event_flag = 0;
    timeout = UINT16_MAX * UINT8_MAX * 8;
    /* Start authentication with remote device. */
    err = RM_BLE_ABS_StartAuthentication(&g_ble_abs0_ctrl, g_connection_handle);
    /* Handle any errors. This function should be defined by the user. */
    handle_error(err);
    /* Wait BLE_GAP_EVENT_PAIRING_COMP event is notified. */
    while (!(BLE_ABS_EVENT_FLAG_PAIRING_COMP & g_ble_event_flag) && (--timeout > 0U))
    {
        R_BLE_Execute();
    }
    time_out_handle_error(timeout);
    /* Clean up & Close BLE driver */
    g_ble_event_flag = 0;
    err = RM_BLE_ABS_Close(&g_ble_abs0_ctrl);
    /* Handle any errors. This function should be defined by the user. */
    handle_error(err);
}
```

## Data Structures

```
struct abs_advertising_parameter_t
```



```
struct abs_scan_parameter_t
```

```
struct ble_abs_instance_ctrl_t
```

```
struct st_ble_rf_notify_t
```

This structure is RF event notify management. [More...](#)

## Typedefs

```
typedef void(* ble_abs_timer_cb_t) (uint32_t timer_hdl)
```

```
typedef void(* ble_mcu_clock_change_cb_t) (void)
```

`ble_mcu_clock_change_cb_t` is the callback function type to use `CLKOUT_RF` as the MCU main clock source. [More...](#)

```
typedef void(* ble_rf_notify_cb_t) (uint32_t)
```

`ble_rf_notify_cb_t` is the RF event notify callback function type. [More...](#)

## Enumerations

```
enum e_ble_timer_type_t
```

## Data Structure Documentation

### ◆ abs\_advertising\_parameter\_t

struct abs_advertising_parameter_t		
advertising set parameters structure		
Data Fields		
union <a href="#">abs_advertising_parameter_t</a>	advertising_parameter	Advertising parameters.
uint32_t	advertising_status	Advertising status.
<a href="#">ble_device_address_t</a>	remote_device_address	Remote device address for direct advertising.

### ◆ abs\_scan\_parameter\_t

struct abs_scan_parameter_t		
scan parameters structure		
Data Fields		
<a href="#">ble_abs_scan_parameter_t</a>	scan_parameter	Scan parameters.

<a href="#">ble_abs_scan_phy_parameter_t</a>	scan_phy_parameter_1M	1M phy parameters for scan.
<a href="#">ble_abs_scan_phy_parameter_t</a>	scan_phy_parameter_coded	Coded phy parameters for scan. */.
uint32_t	scan_status	

#### ◆ ble\_abs\_instance\_ctrl\_t

struct ble_abs_instance_ctrl_t		
BLE ABS private control block. DO NOT MODIFY. Initialization occurs when <a href="#">RM_BLE_ABS_Open()</a> is called.		
Data Fields		
uint32_t	open	Indicates whether the <a href="#">open()</a> API has been successfully called.
void const *	p_context	Placeholder for user data. Passed to the user callback in <a href="#">ble_abs_callback_args_t</a> .
<a href="#">ble_gap_application_callback_t</a>	abs_gap_callback	GAP callback function.
<a href="#">ble_vendor_specific_application_callback_t</a>	abs_vendor_specific_callback	Vendor specific callback function.
uint32_t	connection_timer_handle	Cancel a request for connection timer.
uint32_t	advertising_timer_handle	Advertising timer for legacy advertising.
<a href="#">abs_advertising_parameter_t</a>	advertising_set s[ <a href="#">BLE_MAX_NO_OF_ADV_SETS_SUPPORTED</a> ]	Advertising set information.
<a href="#">abs_scan_parameter_t</a>	abs_scan	Scan information.
<a href="#">st_ble_dev_addr_t</a>	loc_bd_addr	Local device address.
uint8_t	privacy_mode	Privacy mode.
uint32_t	set_privacy_status	Local privacy status.
<a href="#">ble_abs_timer_t</a>	timer[ <a href="#">BLE_ABS_CFG_TIMER_NUMBER_OF_SLOT</a> ]	
uint32_t	current_timeout_ms	Current timeout.
uint32_t	elapsed_timeout_ms	Elapsed timeout.
<a href="#">ble_abs_cfg_t</a> const *	p_cfg	Pointer to the BLE ABS configuration block.

#### ◆ st\_ble\_rf\_notify\_t

struct st_ble_rf_notify_t		
This structure is RF event notify management.		

Data Fields		
uint32_t	enable	Set enable/disable of each RF event notification.  Bit0 Notify Connection event start(0:Disable/1:Enable) Bit1 Notify Advertising event start(0:Disable/1:Enable) Bit2 Notify Scanning event start(0:Disable/1:Enable) Bit3 Notify Initiating event start(0:Disable/1:Enable) Bit4 Notify Connection event close(0:Disable/1:Enable) Bit5 Notify Advertising event close(0:Disable/1:Enable) Bit6 Notify Scanning event close(0:Disable/1:Enable) Bit7 Notify Initiating event close(0:Disable/1:Enable) Bit8 Notify RF_DEEP_SLEEP event start(0:Disable/1:Enable) Bit9 Notify RF_DEEP_SLEEP event close(0:Disable/1:Enable) Other Bit: Reserved for future use.
<a href="#">ble_rf_notify_cb_t</a>	start_cb	Set callback function pointer for RF event start.
<a href="#">ble_rf_notify_cb_t</a>	close_cb	Set callback function pointer for RF event close.
<a href="#">ble_rf_notify_cb_t</a>	dsleep_cb	Set callback function pointer for RF_DEEP_SLEEP.

## Typedef Documentation

### ◆ ble\_abs\_timer\_cb\_t

```
typedef void(* ble_abs_timer_cb_t) (uint32_t timer_hdl)
```

The timer callback invoked when the timer expired.

◆ **ble\_mcu\_clock\_change\_cb\_t**

ble_mcu_clock_change_cb_t	
ble_mcu_clock_change_cb_t is the callback function type to use CLKOUT_RF as the MCU main clock source.	
<b>Parameters</b>	
none	
<b>Returns</b>	
none	

◆ **ble\_rf\_notify\_cb\_t**

ble_rf_notify_cb_t		
ble_rf_notify_cb_t is the RF event notify callback function type.		
<b>Parameters</b>		
[in]	uint32_t	The information of RF event notification.
<b>Returns</b>		
none		

**Enumeration Type Documentation**◆ **e\_ble\_timer\_type\_t**

enum e_ble_timer_type_t	
The timer type.	
Enumerator	
BLE_TIMER_ONE_SHOT	One shot timer type
BLE_TIMER_PERIODIC	Periodic timer type

**Function Documentation**

◆ **RM\_BLE\_ABS\_Open()**

```
fsp_err_t RM_BLE_ABS_Open ( ble_abs_ctrl_t *const p_ctrl, ble_abs_cfg_t const *const p_cfg )
```

Host stack is initialized with this function. Before using All the R\_BLE APIs, it's necessary to call this function. A callback functions are registered with this function. In order to receive the GAP, GATT, Vendor specific event, it's necessary to register a callback function. The result of this API call is notified in BLE\_GAP\_EVENT\_STACK\_ON event. Implements [ble\\_abs\\_api\\_t::open](#).

Example:

```
/* Open the module. */
err = RM_BLE_ABS_Open(&g_ble_abs0_ctrl, &g_ble_abs0_cfg);
```

**Return values**

FSP_SUCCESS	Channel opened successfully.
FSP_ERR_ASSERTION	Null pointer presented.
FSP_ERR_INVALID_CHANNEL	The channel number is invalid.
FSP_ERR_ALREADY_OPEN	Requested channel is already open in a different configuration.
FSP_ERR_INVALID_ARGUMENT	Invalid input parameter.

◆ **RM\_BLE\_ABS\_Close()**

```
fsp_err_t RM_BLE_ABS_Close ( ble_abs_ctrl_t *const p_ctrl)
```

Close the BLE channel. Implements [ble\\_abs\\_api\\_t::close](#).

Example:

```
/* Close BLE driver */
err = RM_BLE_ABS_Close(&g_ble_abs0_ctrl);
```

**Return values**

FSP_SUCCESS	Channel closed successfully.
FSP_ERR_ASSERTION	Null pointer presented.
FSP_ERR_NOT_OPEN	Control block not open.

◆ **RM\_BLE\_ABS\_Reset()**

```
fsp_err_t RM_BLE_ABS_Reset ( ble_abs_ctrl_t *const p_ctrl, ble_event_cb_t init_callback )
```

BLE is reset with this function. The process is carried out in the following order. [R\\_BLE\\_Close\(\)](#) -> [R\\_BLE\\_GAP\\_Terminate\(\)](#) -> [R\\_BLE\\_Open\(\)](#) -> [R\\_BLE\\_SetEvent\(\)](#). The `init_cb` callback initializes the others (Host Stack, timer, etc...). Implements `ble_abs_api_t::reset`.

**Return values**

FSP_SUCCESS	Channel closed successfully.
FSP_ERR_ASSERTION	Null pointer presented.
FSP_ERR_NOT_OPEN	Control block not open.

◆ **RM\_BLE\_ABS\_VersionGet()**

```
fsp_err_t RM_BLE_ABS_VersionGet ( fsp_version_t *const p_version)
```

Get BLE module code and API versions. Implements `ble_abs_api_t::versionGet`.

**Return values**

FSP_SUCCESS	Operation succeeded.
FSP_ERR_ASSERTION	The parameter <code>p_version</code> is NULL.

### ◆ RM\_BLE\_ABS\_StartLegacyAdvertising()

```
fsp_err_t RM_BLE_ABS_StartLegacyAdvertising ( ble_abs_ctrl_t *const p_ctrl,
ble_abs_legacy_advertising_parameter_t const *const p_advertising_parameter )
```

Start Legacy Advertising after setting advertising parameters, advertising data and scan response data. The legacy advertising uses the advertising set whose advertising handle is 0. The advertising type is connectable and scannable(ADV\_IND). The address type of local device is Public Identity Address or RPA(If the resolving list contains no matching entry, use the public address.). Scan request event(BLE\_GAP\_EVENT\_SCAN\_REQ\_RECV) is not notified. Implements [ble\\_abs\\_api\\_t::startLegacyAdvertising](#)

Example:

```
/* Start advertising. */
err = RM_BLE_ABS_StartLegacyAdvertising(&g_ble_abs0_ctrl,
&legacy_advertising_parameter);
```

#### Return values

FSP_SUCCESS	Operation succeeded
FSP_ERR_ASSERTION	p_instance_ctrl is specified as NULL.
FSP_ERR_NOT_OPEN	Control block not open.
FSP_ERR_INVALID_STATE	Host stack hasn't been initialized.
FSP_ERR_INVALID_POINTER	p_advertising_parameter is specified as NULL.
FSP_ERR_INVALID_ARGUMENT	The advertising parameter is out of range.

### ◆ RM\_BLE\_ABS\_StartExtendedAdvertising()

```
fsp_err_t RM_BLE_ABS_StartExtendedAdvertising ( ble_abs_ctrl_t *const p_ctrl,
ble_abs_extend_advertising_parameter_t const *const p_advertising_parameter )
```

Start Extended Advertising after setting advertising parameters, advertising data. The extended advertising uses the advertising set whose advertising handle is 1. The advertising type is connectable and non-scannable. The address type of local device is Public Identity Address or RPA(If the resolving list contains no matching entry, use the public address.). Scan request event(BLE\_GAP\_EVENT\_SCAN\_REQ\_RECV) is not notified. Implements [ble\\_abs\\_api\\_t::startExtendedAdvertising](#)

#### Return values

FSP_SUCCESS	Operation succeeded.
FSP_ERR_ASSERTION	p_instance_ctrl is specified as NULL.
FSP_ERR_NOT_OPEN	Control block not open.
FSP_ERR_INVALID_POINTER	p_advertising_parameter is specified as NULL.
FSP_ERR_INVALID_STATE	Host stack hasn't been initialized.
FSP_ERR_INVALID_ARGUMENT	The advertising parameter is out of range.
FSP_ERR_UNSUPPORTED	Subordinate modules do not support this feature.



### ◆ RM\_BLE\_ABS\_StartNonConnectableAdvertising()

```
fsp_err_t RM_BLE_ABS_StartNonConnectableAdvertising ( ble_abs_ctrl_t *const p_ctrl,
ble_abs_non_connectable_advertising_parameter_t const *const p_advertising_parameter )
```

Start Non-Connectable Advertising after setting advertising parameters, advertising data. The non-connectable advertising uses the advertising set whose advertising handle is 2. The advertising type is non-connectable and non-scannable. The address type of local device is Public Identity Address or RPA(If the resolving list contains no matching entry, use the public address.). Scan request event(BLE\_GAP\_EVENT\_SCAN\_REQ\_RECV) is not notified. Secondary Advertising Max Skip is 0. Implements [ble\\_abs\\_api\\_t::startNonConnectableAdvertising](#).

#### Return values

FSP_SUCCESS	Operation succeeded.
FSP_ERR_ASSERTION	p_instance_ctrl is specified as NULL.
FSP_ERR_NOT_OPEN	Control block not open.
FSP_ERR_INVALID_POINTER	p_advertising_parameter is specified as NULL.
FSP_ERR_INVALID_STATE	Host stack hasn't been initialized.
FSP_ERR_INVALID_ARGUMENT	The advertising parameter is out of range.

### ◆ RM\_BLE\_ABS\_StartPeriodicAdvertising()

```
fsp_err_t RM_BLE_ABS_StartPeriodicAdvertising ( ble_abs_ctrl_t *const p_ctrl,
ble_abs_periodic_advertising_parameter_t const *const p_advertising_parameter )
```

Start Periodic Advertising after setting advertising parameters, periodic advertising parameters, advertising data and periodic advertising data. The periodic advertising uses the advertising set whose advertising handle is 3. The advertising type is non-connectable and non-scannable. The address type of local device is Public Identity Address or RPA(If the resolving list contains no matching entry, use the public address.). Scan request event(BLE\_GAP\_EVENT\_SCAN\_REQ\_RECV) is not notified. Secondary Advertising Max Skip is 0. Implements [ble\\_abs\\_api\\_t::startPeriodicAdvertising](#)

#### Return values

FSP_SUCCESS	Operation succeeded.
FSP_ERR_ASSERTION	p_instance_ctrl is specified as NULL.
FSP_ERR_NOT_OPEN	Control block not open.
FSP_ERR_INVALID_POINTER	p_advertising_parameter is specified as NULL.
FSP_ERR_INVALID_ARGUMENT	The advertising parameter is out of range.
FSP_ERR_UNSUPPORTED	Subordinate modules do not support this feature.

### ◆ RM\_BLE\_ABS\_StartScanning()

```
fsp_err_t RM_BLE_ABS_StartScanning ( ble_abs_ctrl_t *const p_ctrl, ble_abs_scan_parameter_t
const *const p_scan_parameter )
```

Start scanning after setting scan parameters. The scanner address type is Public Identity Address. Fast scan is followed by slow scan. The end of fast scan or slow scan is notified with BLE\_GAP\_EVENT\_SCAN\_TO event. If fast\_period is 0, only slow scan is carried out. If scan\_period is 0, slow scan continues. Implements `ble_abs_api_t::startScanning`.

Example:

```
/* Start scanning. */
err = RM_BLE_ABS_StartScanning(&g_ble_abs0_ctrl, &scan_parameter);
```

#### Return values

FSP_SUCCESS	Operation succeeded.
FSP_ERR_ASSERTION	p_instance_ctrl is specified as NULL.
FSP_ERR_NOT_OPEN	Control block not open.
FSP_ERR_INVALID_POINTER	p_scan_parameter is specified as NULL.
FSP_ERR_INVALID_ARGUMENT	The scan parameter is out of range.

### ◆ RM\_BLE\_ABS\_CreateConnection()

```
fsp_err_t RM_BLE_ABS_CreateConnection ( ble_abs_ctrl_t *const p_ctrl,
ble_abs_connection_parameter_t const *const p_connection_parameter )
```

Request create connection. The initiator address type is Public Identity Address. The scan interval is 60ms and the scan window is 30ms in case of 1M PHY or 2M PHY. The scan interval is 180ms and the scan window is 90ms in case of coded PHY. The Minimum CE Length and the Maximum CE Length are 0xFFFF. When the request for a connection has been received by the Controller, BLE\_GAP\_EVENT\_CREATE\_CONN\_COMP event is notified. When a link has been established, BLE\_GAP\_EVENT\_CONN\_IND event is notified. Implements [ble\\_abs\\_api\\_t::createConnection](#).

Example:

```
/* Create connection with remote device. */
err = RM_BLE_ABS_CreateConnection(&g_ble_abs0_ctrl, &g_connection_parameter);
```

#### Return values

FSP_SUCCESS	Operation succeeded.
FSP_ERR_ASSERTION	p_instance_ctrl is specified as NULL.
FSP_ERR_NOT_OPEN	Control block not open.
FSP_ERR_INVALID_POINTER	p_connection_parameter is specified as NULL.
FSP_ERR_INVALID_ARGUMENT	The create connection parameter is out of range.
FSP_ERR_BLE_ABS_NOT_FOUND	Couldn't find a valid timer.
FSP_ERR_BLE_ABS_INVALID_OPERATION	Invalid operation for the selected timer.

### ◆ RM\_BLE\_ABS\_SetLocalPrivacy()

```
fsp_err_t RM_BLE_ABS_SetLocalPrivacy ( ble_abs_ctrl_t *const p_ctrl, uint8_t const *const p_lc_irk,
uint8_t privacy_mode )
```

Generate a IRK, add it to the resolving list, set privacy mode and enable RPA function. Register vendor specific callback function, if IRK is generated by this function. After configuring local device privacy, BLE\_GAP\_ADDR\_RPA\_ID\_PUBLIC is specified as own device address in the advertising/scan/create connection API. Implements [ble\\_abs\\_api\\_t::setLocalPrivacy](#)

Example:

```
/* Set local privacy. */
err = RM_BLE_ABS_SetLocalPrivacy(&g_ble_abs0_ctrl, p_lc_irk, privacy_mode);
```

#### Return values

FSP_SUCCESS	Operation succeeded.
FSP_ERR_ASSERTION	p_instance_ctrl is specified as NULL.
FSP_ERR_NOT_OPEN	Control block not open.
FSP_ERR_INVALID_ARGUMENT	The privacy_mode parameter is out of range.
FSP_ERR_BLE_ABS_INVALID_OPERATION	Host stack hasn't been initialized. configuring the resolving list or privacy mode.

### ◆ RM\_BLE\_ABS\_StartAuthentication()

```
fsp_err_t RM_BLE_ABS_StartAuthentication ( ble_abs_ctrl_t *const p_ctrl, uint16_t
connection_handle )
```

Start pairing or encryption. If pairing has been done, start encryption. The pairing parameters are configured by [RM\\_BLE\\_ABS\\_Open\(\)](#) or [R\\_BLE\\_GAP\\_SetPairingParams\(\)](#). If the pairing parameters are configure by [RM\\_BLE\\_ABS\\_Open\(\)](#),

- bonding policy is that bonding information is stored.
- Key press notification is not supported. Implements [ble\\_abs\\_api\\_t::startAuthentication](#).

Example:

```
/* Start authentication with remote device. */
err = RM_BLE_ABS_StartAuthentication(&g_ble_abs0_ctrl, g_connection_handle);
```

#### Return values

FSP_SUCCESS	Operation succeeded.
FSP_ERR_ASSERTION	p_instance_ctrl or connection_handle are specified as NULL.
FSP_ERR_NOT_OPEN	Control block not open.
FSP_ERR_INVALID_ARGUMENT	The connection handle parameter is out of range.

## 4.2.59 SD/MMC Block Media Implementation (rm\_block\_media\_sdmmc)

Modules

### Functions

```
fsp_err_t RM_BLOCK_MEDIA_SDMMC_Open (rm_block_media_ctrl_t *const
p_ctrl, rm_block_media_cfg_t const *const p_cfg)
```

```
fsp_err_t RM_BLOCK_MEDIA_SDMMC_MediaInit (rm_block_media_ctrl_t *const
p_ctrl)
```

```
fsp_err_t RM_BLOCK_MEDIA_SDMMC_Read (rm_block_media_ctrl_t *const
p_ctrl, uint8_t *const p_dest_address, uint32_t const block_address,
uint32_t const num_blocks)
```

```
fsp_err_t RM_BLOCK_MEDIA_SDMMC_Write (rm_block_media_ctrl_t *const
p_ctrl, uint8_t const *const p_src_address, uint32_t const
block_address, uint32_t const num_blocks)
```

```
fsp_err_t RM_BLOCK_MEDIA_SDMMC_Erase (rm_block_media_ctrl_t *const
```

p\_ctrl, uint32\_t const block\_address, uint32\_t const num\_blocks)

fsp\_err\_t RM\_BLOCK\_MEDIA\_SDMMC\_CallbackSet (rm\_block\_media\_ctrl\_t \*const p\_ctrl, void(\*p\_callback)(rm\_block\_media\_callback\_args\_t \*), void const \*const p\_context, rm\_block\_media\_callback\_args\_t \*const p\_callback\_memory)

fsp\_err\_t RM\_BLOCK\_MEDIA\_SDMMC\_StatusGet (rm\_block\_media\_ctrl\_t \*const p\_api\_ctrl, rm\_block\_media\_status\_t \*const p\_status)

fsp\_err\_t RM\_BLOCK\_MEDIA\_SDMMC\_InfoGet (rm\_block\_media\_ctrl\_t \*const p\_ctrl, rm\_block\_media\_info\_t \*const p\_info)

fsp\_err\_t RM\_BLOCK\_MEDIA\_SDMMC\_Close (rm\_block\_media\_ctrl\_t \*const p\_ctrl)

fsp\_err\_t RM\_BLOCK\_MEDIA\_SDMMC\_VersionGet (fsp\_version\_t \*const p\_version)

## Detailed Description

Middleware to implement the block media interface on SD cards. This module implements the [Block Media Interface](#).

## Overview

### Features

The SD/MMC implementation of the block media interface has the following key features:

- Reading, writing, and erasing data from an SD card
- Callback called when card insertion or removal is detected
- Provides media information such as sector size and total number of sectors.

## Configuration

### Build Time Configurations for rm\_block\_media\_sdmmc

The following build time configurations are defined in driver/rm\_block\_media\_sdmmc\_cfg.h:

Configuration	Options	Default	Description
Parameter Checking	<ul style="list-style-type: none"> <li>• Default (BSP)</li> <li>• Enabled</li> <li>• Disabled</li> </ul>	Default (BSP)	If selected code for parameter checking is included in the build.

### Configurations for Middleware > Storage > Block Media Implementation on rm\_block\_media\_sdmmc

This module can be added to the Stacks tab via New Stack > Middleware > Storage > Block Media Implementation on rm\_block\_media\_sdmmc. Non-secure callable guard functions can be generated

for this module by right clicking the module in the RA Configuration tool and checking the "Non-secure Callable" box.

Configuration	Options	Default	Description
Name	Name must be a valid C symbol	g_rm_block_media0	Module name.
Callback	Name must be a valid C symbol	NULL	A user callback function can be provided. If this callback function is provided, it will be called when a card is inserted or removed.

### Clock Configuration

This module has no required clock configurations.

### Pin Configuration

This module does not use I/O pins.

## Examples

### Basic Example

This is a basic example of minimal use of the SD/MMC block media implementation in an application.

```
#define RM_BLOCK_MEDIA_SDMMC_BLOCK_SIZE (512)
uint8_t g_dest[RM_BLOCK_MEDIA_SDMMC_BLOCK_SIZE] BSP_ALIGN_VARIABLE(4);
uint8_t g_src[RM_BLOCK_MEDIA_SDMMC_BLOCK_SIZE] BSP_ALIGN_VARIABLE(4);
uint32_t g_transfer_complete = 0;
void rm_block_media_sdmme_basic_example (void)
{
    /* Initialize g_src to known data */
    for (uint32_t i = 0; i < RM_BLOCK_MEDIA_SDMMC_BLOCK_SIZE; i++)
    {
        g_src[i] = (uint8_t) ('A' + (i % 26));
    }

    /* Open the RM_BLOCK_MEDIA_SDMMC driver. */
    fsp_err_t err = RM_BLOCK_MEDIA_SDMMC_Open(&g_rm_block_media0_ctrl,
&g_rm_block_media0_cfg);

    /* Handle any errors. This function should be defined by the user. */
}
```

```

    handle_error(err);

    /* A device shall be ready to accept the first command within 1ms from detecting VDD
    min. Reference section 6.4.1.1

    * "Power Up Time of Card" in the SD Physical Layer Simplified Specification Version
    6.00. */

    R_BSP_SoftwareDelay(1U, BSP_DELAY_UNITS_MILLISECONDS);

    /* Initialize the SD card. This should not be done until the card is plugged in for
    SD devices. */

    err = RM_BLOCK_MEDIA_SDMMC_MediaInit(&g_rm_block_media0_ctrl);
    handle_error(err);

    /* Write a block of data to sector 3 of an SD card. */

    err = RM_BLOCK_MEDIA_SDMMC_Write(&g_rm_block_media0_ctrl, g_src, 3, 1);
    handle_error(err);

    /* Read a block of data from sector 3 of an SD card. */

    err = RM_BLOCK_MEDIA_SDMMC_Read(&g_rm_block_media0_ctrl, g_dest, 3, 1);
    handle_error(err);
}

```

## Function Documentation

### ◆ RM\_BLOCK\_MEDIA\_SDMMC\_Open()

```
fsp_err_t RM_BLOCK_MEDIA_SDMMC_Open ( rm_block_media_ctrl_t *const p_ctrl,
rm_block_media_cfg_t const *const p_cfg )
```

Opens the module.

Implements `rm_block_media_api_t::open()`.

#### Return values

FSP_SUCCESS	Module is available and is now open.
FSP_ERR_ASSERTION	An input parameter is invalid.
FSP_ERR_ALREADY_OPEN	Module has already been opened with this instance of the control structure.

#### Returns

See [Common Error Codes](#) or functions called by this function for other possible return codes. This function calls:

- `sdmmc_api_t::open`



◆ **RM\_BLOCK\_MEDIA\_SDMMC\_MediaInit()**

```
fsp_err_t RM_BLOCK_MEDIA_SDMMC_MediaInit ( rm_block_media_ctrl_t *const p_ctrl)
```

Initializes the SD or eMMC device. This procedure requires several sequential commands. This function blocks until all identification and configuration commands are complete.

Implements `rm_block_media_api_t::mediaInit()`.

**Return values**

FSP_SUCCESS	Module is initialized and ready to access the memory device.
FSP_ERR_ASSERTION	An input parameter is invalid.
FSP_ERR_NOT_OPEN	Module is not open.

**Returns**

See [Common Error Codes](#) or functions called by this function for other possible return codes. This function calls:

- `sdmmc_api_t::mediaInit`

◆ **RM\_BLOCK\_MEDIA\_SDMMC\_Read()**

```
fsp_err_t RM_BLOCK_MEDIA_SDMMC_Read ( rm_block_media_ctrl_t *const p_ctrl, uint8_t *const p_dest_address, uint32_t const block_address, uint32_t const num_blocks )
```

Reads data from an SD or eMMC device. Up to 0x10000 sectors can be read at a time. Implements `rm_block_media_api_t::read()`.

This function blocks until the data is read into the destination buffer.

**Return values**

FSP_SUCCESS	Data read successfully.
FSP_ERR_ASSERTION	An input parameter is invalid.
FSP_ERR_NOT_OPEN	Module is not open.
FSP_ERR_NOT_INITIALIZED	Module has not been initialized.

**Returns**

See [Common Error Codes](#) or functions called by this function for other possible return codes. This function calls:

- `sdmmc_api_t::read`

### ◆ RM\_BLOCK\_MEDIA\_SDMMC\_Write()

```
fsp_err_t RM_BLOCK_MEDIA_SDMMC_Write ( rm_block_media_ctrl_t *const p_ctrl, uint8_t const
*const p_src_address, uint32_t const block_address, uint32_t const num_blocks )
```

Writes data to an SD or eMMC device. Up to 0x10000 sectors can be written at a time. Implements [rm\\_block\\_media\\_api\\_t::write\(\)](#).

This function blocks until the write operation completes.

#### Return values

FSP_SUCCESS	Write finished successfully.
FSP_ERR_ASSERTION	An input parameter is invalid.
FSP_ERR_NOT_OPEN	Module is not open.
FSP_ERR_NOT_INITIALIZED	Module has not been initialized.

#### Returns

See [Common Error Codes](#) or functions called by this function for other possible return codes. This function calls:

- [sdmmc\\_api\\_t::write](#)

### ◆ RM\_BLOCK\_MEDIA\_SDMMC\_Erase()

```
fsp_err_t RM_BLOCK_MEDIA_SDMMC_Erase ( rm_block_media_ctrl_t *const p_ctrl, uint32_t const
block_address, uint32_t const num_blocks )
```

Erases sectors of an SD card or eMMC device. Implements [rm\\_block\\_media\\_api\\_t::erase\(\)](#).

This function blocks until erase is complete.

#### Return values

FSP_SUCCESS	Erase operation requested.
FSP_ERR_ASSERTION	An input parameter is invalid.
FSP_ERR_NOT_OPEN	Module is not open.
FSP_ERR_NOT_INITIALIZED	Module has not been initialized.

#### Returns

See [Common Error Codes](#) or functions called by this function for other possible return codes. This function calls:

- [sdmmc\\_api\\_t::erase](#)
- [sdmmc\\_api\\_t::statusGet](#)

◆ **RM\_BLOCK\_MEDIA\_SDMMC\_CallbackSet()**

```
fsp_err_t RM_BLOCK_MEDIA_SDMMC_CallbackSet ( rm_block_media_ctrl_t *const p_ctrl,
void(*) (rm_block_media_callback_args_t *) p_callback, void const *const p_context,
rm_block_media_callback_args_t *const p_callback_memory )
```

Updates the user callback with the option to provide memory for the callback argument structure. Implements `rm_block_media_api_t::callbackSet`.

**Return values**

FSP_SUCCESS	Callback updated successfully.
FSP_ERR_ASSERTION	A required pointer is NULL.
FSP_ERR_NOT_OPEN	The control block has not been opened.
FSP_ERR_NO_CALLBACK_MEMORY	<code>p_callback</code> is non-secure and <code>p_callback_memory</code> is either secure or NULL.

◆ **RM\_BLOCK\_MEDIA\_SDMMC\_StatusGet()**

```
fsp_err_t RM_BLOCK_MEDIA_SDMMC_StatusGet ( rm_block_media_ctrl_t *const p_api_ctrl,
rm_block_media_status_t *const p_status )
```

Provides driver status. Implements `rm_block_media_api_t::statusGet()`.

**Return values**

FSP_SUCCESS	Status stored in <code>p_status</code> .
FSP_ERR_ASSERTION	NULL pointer.
FSP_ERR_NOT_OPEN	Module is not open.

◆ **RM\_BLOCK\_MEDIA\_SDMMC\_InfoGet()**

```
fsp_err_t RM_BLOCK_MEDIA_SDMMC_InfoGet ( rm_block_media_ctrl_t *const p_ctrl,
rm_block_media_info_t *const p_info )
```

Retrieves module information. Implements `rm_block_media_api_t::infoGet()`.

**Return values**

FSP_SUCCESS	Erase operation requested.
FSP_ERR_ASSERTION	An input parameter is invalid.
FSP_ERR_NOT_OPEN	Module is not open.
FSP_ERR_NOT_INITIALIZED	Module has not been initialized.

◆ **RM\_BLOCK\_MEDIA\_SDMMC\_Close()**

```
fsp_err_t RM_BLOCK_MEDIA_SDMMC_Close ( rm_block_media_ctrl_t *const p_ctrl)
```

Closes an open SD/MMC device. Implements `rm_block_media_api_t::close()`.

**Return values**

FSP_SUCCESS	Successful close.
FSP_ERR_ASSERTION	An input parameter is invalid.
FSP_ERR_NOT_OPEN	Module is not open.

◆ **RM\_BLOCK\_MEDIA\_SDMMC\_VersionGet()**

```
fsp_err_t RM_BLOCK_MEDIA_SDMMC_VersionGet ( fsp_version_t *const p_version)
```

Returns the version of the firmware and API. Implements `rm_block_media_api_t::versionGet()`.

**Return values**

FSP_SUCCESS	Function executed successfully.
FSP_ERR_ASSERTION	Null Pointer.

**4.2.60 USB HMSC Block Media Implementation (rm\_block\_media\_usb)**

## Modules

**Functions**

```
fsp_err_t RM_BLOCK_MEDIA_USB_Open (rm_block_media_ctrl_t *const p_ctrl,
rm_block_media_cfg_t const *const p_cfg)
```

```
fsp_err_t RM_BLOCK_MEDIA_USB_MediaInit (rm_block_media_ctrl_t *const
p_ctrl)
```

```
fsp_err_t RM_BLOCK_MEDIA_USB_Read (rm_block_media_ctrl_t *const p_ctrl,
uint8_t *const p_dest_address, uint32_t const block_address,
uint32_t const num_blocks)
```

```
fsp_err_t RM_BLOCK_MEDIA_USB_Write (rm_block_media_ctrl_t *const p_ctrl,
uint8_t const *const p_src_address, uint32_t const block_address,
uint32_t const num_blocks)
```

```
fsp_err_t RM_BLOCK_MEDIA_USB_Erase (rm_block_media_ctrl_t *const p_ctrl,
uint32_t const block_address, uint32_t const num_blocks)
```

```
fsp_err_t RM_BLOCK_MEDIA_USB_CallbackSet (rm_block_media_ctrl_t *const
p_ctrl, void(*p_callback)(rm_block_media_callback_args_t *), void
const *const p_context, rm_block_media_callback_args_t *const
p_callback_memory)
```

```
fsp_err_t RM_BLOCK_MEDIA_USB_StatusGet (rm_block_media_ctrl_t *const
p_api_ctrl, rm_block_media_status_t *const p_status)
```

```
fsp_err_t RM_BLOCK_MEDIA_USB_InfoGet (rm_block_media_ctrl_t *const p_ctrl,
rm_block_media_info_t *const p_info)
```

```
fsp_err_t RM_BLOCK_MEDIA_USB_Close (rm_block_media_ctrl_t *const p_ctrl)
```

```
fsp_err_t RM_BLOCK_MEDIA_USB_VersionGet (fsp_version_t *const p_version)
```

## Detailed Description

Middleware to implement the block media interface on USB mass storage devices. This module implements the [Block Media Interface](#).

## Overview

### Features

The USB implementation of the block media interface has the following key features:

- Reading, writing, and erasing data from a USB mass storage device
- Callback called when device insertion or removal is detected
- Provides media information such as sector size and total number of sectors.

## Configuration

### Build Time Configurations for rm\_block\_media\_usb

The following build time configurations are defined in driver/rm\_block\_media\_usb\_cfg.h:

Configuration	Options	Default	Description
Parameter Checking Enable	<ul style="list-style-type: none"> <li>• Default (BSP)</li> <li>• Enabled</li> <li>• Disabled</li> </ul>	Default (BSP)	If selected code for parameter checking is included in the build.

### Configurations for Middleware > Storage > Block Media Implementation on rm\_block\_media\_usb

This module can be added to the Stacks tab via New Stack > Middleware > Storage > Block Media Implementation on rm\_block\_media\_usb.

Configuration	Options	Default	Description
Name	Name must be a valid	g_rm_block_media0	Module name.

	C symbol		
Callback	Name must be a valid C symbol	NULL	A user callback function can be provided. If this callback function is provided, it will be called when a device is attached or removed.
Pointer to user context	Name must be a valid C symbol	NULL	A user context can be provided. If this context is provided, it will be passed to callback function when a device is attached or removed.

*Note*

*RM\_BLOCK\_MEDIA\_USB\_MediaInit function must be called after receiving the insert event notification.*

**Clock Configuration**

This module has no required clock configurations.

**Pin Configuration**

This module does not use I/O pins.

**Examples****Basic Example**

This is a basic example of minimal use of the USB mass storage block media implementation in an application.

```
#define RM_BLOCK_MEDIA_USB_BLOCK_SIZE (512)
volatile bool g_usb_inserted = false;
uint8_t      g_dest[RM_BLOCK_MEDIA_USB_BLOCK_SIZE] BSP_ALIGN_VARIABLE(4);
uint8_t      g_src[RM_BLOCK_MEDIA_USB_BLOCK_SIZE] BSP_ALIGN_VARIABLE(4);
void rm_block_media_usb_basic_example (void)
{
    /* Initialize g_src to known data */
    for (uint32_t i = 0; i < RM_BLOCK_MEDIA_USB_BLOCK_SIZE; i++)
    {
        g_src[i] = (uint8_t) ('A' + (i % 26));
    }
    /* Open the RM_BLOCK_MEDIA_USB driver. */
}
```

```
fsp_err_t err = RM_BLOCK_MEDIA_USB_Open(&g_rm_block_media0_ctrl,
&g_rm_block_media0_cfg);

/* Handle any errors. This function should be defined by the user. */
    handle_error(err);

while (!g_usb_inserted)
    {
/* Wait for a card insertion interrupt. */
    }

/* Initialize the mass storage device. This should not be done until the device is
plugged in and initialized. */
    err = RM_BLOCK_MEDIA_USB_MediaInit(&g_rm_block_media0_ctrl);
    handle_error(err);

/* Write a block of data to sector 3 of an USB mass storage device. */
    err = RM_BLOCK_MEDIA_USB_Write(&g_rm_block_media0_ctrl, g_src, 3, 1);
    handle_error(err);

/* Read a block of data from sector 3 of an USB mass storage device. */
    err = RM_BLOCK_MEDIA_USB_Read(&g_rm_block_media0_ctrl, g_dest, 3, 1);
    handle_error(err);
}
```

## Device Insertion

This is an example of using a callback to determine when a mass storage device is plugged in and enumerated.

```
/* The callback is called when a media insertion event occurs. */
void rm_block_media_usb_media_insertion_example_callback
(rm_block_media_callback_args_t * p_args)
{
    if (RM_BLOCK_MEDIA_EVENT_MEDIA_INSERTED == p_args->event)
        {
            g_usb_inserted = true;
        }

    if (RM_BLOCK_MEDIA_EVENT_MEDIA_REMOVED == p_args->event)
        {
```

```

    g_usb_inserted = false;
}
}

```

## Function Documentation

### ◆ RM\_BLOCK\_MEDIA\_USB\_Open()

```
fsp_err_t RM_BLOCK_MEDIA_USB_Open ( rm_block_media_ctrl_t *const p_ctrl,
rm_block_media_cfg_t const *const p_cfg )
```

Opens the module.

Implements `rm_block_media_api_t::open()`.

#### Return values

FSP_SUCCESS	Module is available and is now open.
FSP_ERR_ASSERTION	An input parameter is invalid.
FSP_ERR_ALREADY_OPEN	Module has already been opened with this instance of the control structure.

#### Returns

See [Common Error Codes](#) or functions called by this function for other possible return codes.

### ◆ RM\_BLOCK\_MEDIA\_USB\_MediaInit()

```
fsp_err_t RM_BLOCK_MEDIA_USB_MediaInit ( rm_block_media_ctrl_t *const p_ctrl)
```

Initializes the USB device.

Implements `rm_block_media_api_t::mediaInit()`.

#### Return values

FSP_SUCCESS	Module is initialized and ready to access the memory device.
FSP_ERR_ASSERTION	An input parameter is invalid.
FSP_ERR_NOT_OPEN	Module is not open.



### ◆ RM\_BLOCK\_MEDIA\_USB\_Read()

```
fsp_err_t RM_BLOCK_MEDIA_USB_Read ( rm_block_media_ctrl_t *const p_ctrl, uint8_t *const
p_dest_address, uint32_t const block_address, uint32_t const num_blocks )
```

Reads data from an USB device. Implements [rm\\_block\\_media\\_api\\_t::read\(\)](#).

This function blocks until the data is read into the destination buffer.

#### Return values

FSP_SUCCESS	Data read successfully.
FSP_ERR_ASSERTION	An input parameter is invalid.
FSP_ERR_NOT_OPEN	Module is not open.
FSP_ERR_NOT_INITIALIZED	Module has not been initialized.

#### Returns

See [Common Error Codes](#) or functions called by this function for other possible return codes.

### ◆ RM\_BLOCK\_MEDIA\_USB\_Write()

```
fsp_err_t RM_BLOCK_MEDIA_USB_Write ( rm_block_media_ctrl_t *const p_ctrl, uint8_t const *const
p_src_address, uint32_t const block_address, uint32_t const num_blocks )
```

Writes data to an USB device. Implements [rm\\_block\\_media\\_api\\_t::write\(\)](#).

This function blocks until the write operation completes.

#### Return values

FSP_SUCCESS	Write finished successfully.
FSP_ERR_ASSERTION	An input parameter is invalid.
FSP_ERR_NOT_OPEN	Module is not open.
FSP_ERR_NOT_INITIALIZED	Module has not been initialized.

#### Returns

See [Common Error Codes](#) or functions called by this function for other possible return codes.

### ◆ RM\_BLOCK\_MEDIA\_USB\_Erase()

```
fsp_err_t RM_BLOCK_MEDIA_USB_Erase ( rm_block_media_ctrl_t *const p_ctrl, uint32_t const
block_address, uint32_t const num_blocks )
```

Erases sectors of an USB device. Implements `rm_block_media_api_t::erase()`.

This function blocks until erase is complete.

#### Return values

FSP_SUCCESS	Erase operation requested.
FSP_ERR_ASSERTION	An input parameter is invalid.
FSP_ERR_NOT_OPEN	Module is not open.
FSP_ERR_NOT_INITIALIZED	Module has not been initialized.

#### Returns

See [Common Error Codes](#) or functions called by this function for other possible return codes.

### ◆ RM\_BLOCK\_MEDIA\_USB\_CallbackSet()

```
fsp_err_t RM_BLOCK_MEDIA_USB_CallbackSet ( rm_block_media_ctrl_t *const p_ctrl,
void(*) (rm_block_media_callback_args_t *) p_callback, void const *const p_context,
rm_block_media_callback_args_t *const p_callback_memory )
```

Updates the user callback with the option to provide memory for the callback argument structure. Implements `rm_block_media_api_t::callbackSet`.

#### Note

*This function is currently unsupported for Block Media over USB.*

#### Return values

FSP_ERR_UNSUPPORTED	CallbackSet is not currently supported for Block Media over USB.
---------------------	------------------------------------------------------------------

◆ **RM\_BLOCK\_MEDIA\_USB\_StatusGet()**

```
fsp_err_t RM_BLOCK_MEDIA_USB_StatusGet ( rm_block_media_ctrl_t *const p_api_ctrl,
rm_block_media_status_t *const p_status )
```

Provides driver status. Implements `rm_block_media_api_t::statusGet()`.

**Return values**

FSP_SUCCESS	Status stored in p_status.
FSP_ERR_ASSERTION	NULL pointer.
FSP_ERR_NOT_OPEN	Module is not open.
FSP_ERR_NOT_INITIALIZED	Module has not been initialized.

**Returns**

See [Common Error Codes](#) or functions called by this function for other possible return codes.

◆ **RM\_BLOCK\_MEDIA\_USB\_InfoGet()**

```
fsp_err_t RM_BLOCK_MEDIA_USB_InfoGet ( rm_block_media_ctrl_t *const p_ctrl,
rm_block_media_info_t *const p_info )
```

Retrieves module information. Implements `rm_block_media_api_t::infoGet()`.

**Return values**

FSP_SUCCESS	Erase operation requested.
FSP_ERR_ASSERTION	An input parameter is invalid.
FSP_ERR_NOT_OPEN	Module is not open.
FSP_ERR_NOT_INITIALIZED	Module has not been initialized.

◆ **RM\_BLOCK\_MEDIA\_USB\_Close()**

```
fsp_err_t RM_BLOCK_MEDIA_USB_Close ( rm_block_media_ctrl_t *const p_ctrl)
```

Closes an open USB device. Implements `rm_block_media_api_t::close()`.

**Return values**

FSP_SUCCESS	Successful close.
FSP_ERR_ASSERTION	An input parameter is invalid.
FSP_ERR_NOT_OPEN	Module is not open.

### ◆ RM\_BLOCK\_MEDIA\_USB\_VersionGet()

```
fsp_err_t RM_BLOCK_MEDIA_USB_VersionGet ( fsp_version_t *const p_version)
```

Returns the version of the firmware and API. Implements `rm_block_media_api_t::versionGet()`.

#### Return values

FSP_SUCCESS	Function executed successfully.
FSP_ERR_ASSERTION	Null Pointer.

## 4.2.61 SEGGER emWin Port (rm\_emwin\_port)

### Modules

SEGGER emWin port for RA MCUs.

## Overview

The SEGGER emWin RA Port module provides the configuration and hardware acceleration support necessary for use of emWin on RA products. The port provides full integration with the graphics peripherals (GLCDC, DRW and JPEG) as well as FreeRTOS.

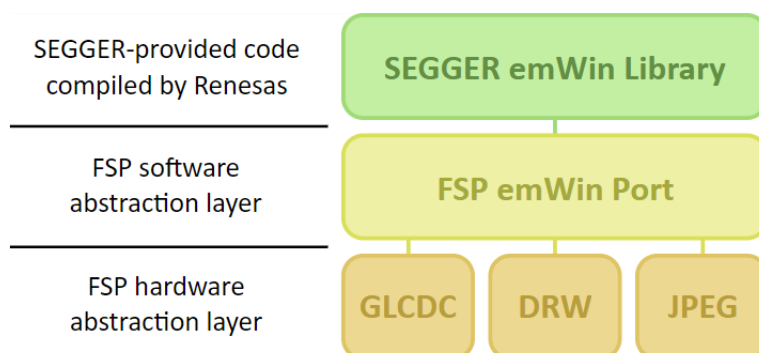


Figure 184: SEGGER emWin FSP Port Block Diagram

#### Note

*This port layer primarily enables hardware acceleration and background handling of many display operations and does not contain code intended to be directly called by the user. Please consult the SEGGER emWin User Guide (UM03001) for details on how to use emWin in your project.*

### Hardware Acceleration

The following functions are currently performed with hardware acceleration:

- DRW Engine (r\_drw)
  - Drawing bitmaps (ARGB8888 and RGB565)
  - 4bpp font rendering
  - Rectangle fill
  - Line and shape drawing
  - Anti-aliased operations
    - Circle stroke and fill
    - Polygon stroke and fill
    - Lines and arcs
- JPEG Codec (r\_jpeg)
  - JPEG decoding
- Graphics LCD Controller (r\_glcdc)
  - Brightness, contrast and gamma correction
  - Pixel format conversion (framebuffer to LCD)

## Configuration

### Build Time Configurations for rm\_emwin\_port

The following build time configurations are defined in fsp\_cfg/rm\_emwin\_port\_cfg.h:

Configuration	Options	Default	Description
Memory Allocation > GUI Heap Size	Value must be a non-negative integer	32768	Set the size of the heap to be allocated for use exclusively by emWin.
Memory Allocation > Section for GUI Heap	Manual Entry	.noinit	Specify the section in which to allocate the GUI heap. When Arm Compiler 6 is used to place this memory in on-chip SRAM, the section name must be .bss or start with .bss. to avoid consuming unnecessary ROM space.
Memory Allocation > Maximum Layers	Value must be a non-negative integer	16	Set the maximum number of available display layers in emWin.  This setting is not related to GLCDC Layer 1 or 2.
Memory Allocation > AA Font Conversion Buffer Size	Value must be a non-negative integer	400	Set the size of the conversion buffer for anti-aliased font glyphs. This should be set to the size (in bytes) of the largest AA character to be rendered.

Configuration > Multi-thread Support	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Enabled	Enable or disable multithreading support.
Configuration > Number of emWin-supported threads	Manual Entry	5	If multithreading support is enabled this configuration specifies the number of different tasks that can call emWin functions.
Configuration > Touch Panel Support	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Enabled	Enable or disable touch panel support.
Configuration > Mouse Support	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Disabled	Enable or disable support for mouse input.
Configuration > Memory Devices	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Enabled	Enable or disable support for memory devices, which allow the user to allocate their own memory in the GUI heap.
Configuration > Text Rotation	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Disabled	Enable or disable support for displaying rotated text.
Configuration > Window Manager	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Enabled	Enable or disable the emWin Window Manager (WM).
Configuration > Bidirectional Text	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Disabled	Enable or disable support for bidirectional text (such as Arabic or Hebrew).
Configuration > Debug Logging Level	<ul style="list-style-type: none"> <li>• None (0)</li> <li>• Parameter checking only (1)</li> <li>• All checks enabled (2)</li> <li>• Log errors (3)</li> <li>• Log warnings (4)</li> <li>• Log all messages (5)</li> </ul>	All checks enabled (2)	Set the debug logging level.
LCD Settings > Wait for Vertical Sync	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Enabled	When enabled emWin will wait for a vertical sync event each time the display is updated. If an RTOS is used the thread will yield; otherwise each frame will block until Vsync.

JPEG Decoding > General > Input Alignment	<ul style="list-style-type: none"> <li>• 8-byte aligned (faster)</li> <li>• Unaligned (slower)</li> </ul>	Unaligned (slower)	<p>WARNING: Disabling vertical sync will result in tearing. It is recommended to always leave this setting Enabled if an RTOS is used.</p> <p>Setting this option to 8-bit alignment can allow the hardware JPEG Codec to directly read JPEG data. This speeds up JPEG decoding operations and reduces RAM overhead, but all JPEG images must reside on an 8-byte boundary.</p> <p>When this option is enabled the input buffer is not allocated.</p>
JPEG Decoding > General > Double- Buffer Output	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Disabled	<p>Enable this option to configure JPEG decoding operations to use a double-buffered output pipeline. This allows the JPEG to be rendered to the display at the same time as decoding at the cost of additional RAM usage.</p> <p>Enabling this option automatically allocates double the output buffer size.</p>
JPEG Decoding > General > Error Timeout	Value must be a non-negative integer	50	<p>Set the timeout for JPEG decoding operations (in RTOS ticks) in the event of a decode error.</p>
JPEG Decoding > Buffers > Input Buffer Size	Value must be a non-negative integer	0x1000	<p>Set the size of the JPEG decode input buffer (in bytes). This buffer is used to ensure 8-byte alignment of input data. Specifying a size smaller than the size of the JPEG to decode will use additional interrupts to stream</p>

JPEG Decoding > Buffers > Output Buffer Size	Value must be a non- negative integer	0x3C00	data in during the decoding process.  Set the size of the JPEG decode output buffer (in bytes). An output buffer smaller than the size of a decoded image will use additional interrupts to stream the data into a framebuffer.
JPEG Decoding > Buffers > Section for Buffers	Manual Entry	.noinit	Unless you are sure of the subsampling used in and the size of the input JPEG images it is recommended to allocate at least 16 framebuffer lines of memory.  Specify the section in which to allocate the JPEG work buffers. When Arm Compiler 6 is used to place this memory in on-chip SRAM, the section name must be .bss or start with .bss. to avoid consuming unnecessary ROM space.

## Hardware Configuration

No clocks or pins are directly required by this module. Please consult the submodules' documentation for their requirements.

## Usage Notes

### Getting Started

To get started with emWin in an RA project the following must be performed:

1. Open the RA Configuration editor for your project
2. Add emWin to your project in the Stacks view by clicking **New Stack -> SEGGER -> SEGGER emWin**
3. Ensure the configuration options for emWin are set as necessary for your application
4. Set the properties for the GLCDC module to match the timing and memory requirements of your display panel
5. Set the JPEG decode color depth to the desired value (if applicable)
6. Ensure interrupts on all modules are enabled:
  - GLCDC Vertical Position (Vpos) Interrupt



- DRW Interrupt (if applicable)
  - JPEG Encode/Decode and Data Transfer Interrupts (if applicable)
7. Click Generate Project Content to save and commit configuration changes
  8. (Non-RTOS projects only) Before calling GUI\_Init, call g\_hal\_init to initialize the framebuffer address.

At this point the project is now ready to build with emWin. Please refer to the SEGGER emWin User Guide (UM03001) as well as demo and sample code for details on how to create a GUI application.

## Using Hardware Acceleration

In most cases there is no need to perform additional configuration to ensure the DRW Engine is used. However, there are some guidelines that should be followed depending on the item in question:

- Bitmaps:
  - ARGB8888, RGB888 and RGB565 bitmaps require no additional settings.
- Anti-aliased shapes:
  - Anti-aliased lines, circles, polygons, polygon outlines and arcs are rendered with the DRW Engine.
- Anti-aliased (4bpp) fonts:
  - Set the text mode to GUI\_TM\_TRANS or create the relevant widget with WM\_CF\_HASTRANS set.
  - Ensure the "AA Font Conversion Buffer Size" configuration option is set to a size equal to or greater than the size (in bytes) of the largest glyph.
- 8bpp palletized images:
  - When creating these images ensure transparency is not enabled as the SEGGER method for this is not compatible with the DRW Engine.
- RLE-encoded images:
  - Hardware acceleration is not available for SEGGER's RLE format.

## Multi-thread Support

When the "Multi-thread Support" configuration is enabled, emWin can be called from multiple threads. This comes with advantages and disadvantages:

Advantages:

- High flexibility in development of applications
- Threads can pend and post on emWin events

Disadvantages:

- Slightly higher RAM/ROM use
- Large GUI projects can become difficult to debug

*Note*

*Multi-thread support is independent of RTOS support. RTOS support is managed internally and cannot be manually configured.*

## Limitations

Developers should be aware of the following limitations when using SEGGER emWin with FSP:

- Hardware acceleration is not available when using color modes lower than 16 bits.
- Support for rotated screen modes is in development.

- Hardware acceleration is not available for SEGGER's RLE image format.

## Examples

### Basic Example

This is a basic example demonstrating a very simple emWin application. The screen is cleared to white and "Hello World!" is printed in the center.

#### Note

*emWin manages the GLCDC, DRW and JPEG Codec submodules internally; they do not need to be opened directly.*

```
#include "DIALOG.h"
#define COLOR_WHITE 0x00FFFFFFU
#define COLOR_BLACK 0x00000000U
#define GUI_DRAW_DELAY 100
static void _cbMain (WM_MESSAGE * pMsg)
{
    GUI_RECT Rect;
    switch (pMsg->MsgId)
    {
    case WM_CREATE:
        {
        break;
        }
    case WM_PAINT:
        {
        /* Clear background to white */
            GUI_SetBkColor(COLOR_WHITE);
            GUI_Clear();

        /* Draw "Hello World!" in black in the center */
            WM_GetClientRect(&Rect);
            GUI_SetColor(COLOR_BLACK);
            GUI_DispStringInRect("Hello World!", &Rect, GUI_TA_VCENTER |
GUI_TA_HCENTER);
        break;
        }
    default:
```

```
    {
        WM_DefaultProc(pMsg);
    }
    break;
}
}
void emWinTask (void)
{
    int32_t xSize;
    int32_t ySize;
    /* Initialize emWin */
    GUI_Init();
    /* Get screen dimensions */
    xSize = LCD_GetXSize();
    ySize = LCD_GetYSize();
    /* Create main window */
    WM_CreateWindowAsChild(0, 0, xSize, ySize, WM_HBKWIN, WM_CF_SHOW, _cbMain, 0);
    /* Enter main drawing loop */
    while (1)
    {
        GUI_Delay(GUI_DRAW_DELAY);
    }
}
```

**Note**

For further example code please consult SEGGER emWin documentation, which can be downloaded [here](#), as well as the Quick Start Guide and example project(s) provided with your Evaluation Kit (if applicable).

## 4.2.62 FreeRTOS+FAT Port (rm\_freertos\_plus\_fat)

### Modules

### Functions

`fsp_err_t` **RM\_FREERTOS\_PLUS\_FAT\_Open** (rm\_freertos\_plus\_fat\_ctrl\_t \*const p\_ctrl, rm\_freertos\_plus\_fat\_cfg\_t const \*const p\_cfg)

fsp_err_t	RM_FREERTOS_PLUS_FAT_MediaInit (rm_freertos_plus_fat_ctrl_t *const p_ctrl, rm_freertos_plus_fat_device_t *const p_device)
fsp_err_t	RM_FREERTOS_PLUS_FAT_DiskInit (rm_freertos_plus_fat_ctrl_t *const p_ctrl, rm_freertos_plus_fat_disk_cfg_t const *const p_disk_cfg, FF_Disk_t *const p_disk)
fsp_err_t	RM_FREERTOS_PLUS_FAT_DiskDeinit (rm_freertos_plus_fat_ctrl_t *const p_ctrl, FF_Disk_t *const p_disk)
fsp_err_t	RM_FREERTOS_PLUS_FAT_InfoGet (rm_freertos_plus_fat_ctrl_t *const p_ctrl, FF_Disk_t *const p_disk, rm_freertos_plus_fat_info_t *const p_info)
fsp_err_t	RM_FREERTOS_PLUS_FAT_Close (rm_freertos_plus_fat_ctrl_t *const p_ctrl)
fsp_err_t	RM_FREERTOS_PLUS_FAT_VersionGet (fsp_version_t *const p_version)

## Detailed Description

Middleware for the FAT File System control on RA MCUs.

## Overview

This module provides the hardware port layer for FreeRTOS+FAT file system. After initializing this module, refer to the FreeRTOS+FAT API reference to use the file system:

[https://www.freertos.org/FreeRTOS-Plus/FreeRTOS\\_Plus\\_FAT/index.html](https://www.freertos.org/FreeRTOS-Plus/FreeRTOS_Plus_FAT/index.html)

## Features

The FreeRTOS+FAT port module supports the following features:

- Callbacks for insertion and removal for removable devices.
- Helper function to initialize FF\_Disk\_t
- Blocking read and write port functions that use FreeRTOS task notification to pend if FreeRTOS is used
- FreeRTOS is optional

## Configuration

### Build Time Configurations for rm\_freertos\_plus\_fat

The following build time configurations are defined in fsp\_cfg/middleware/rm\_freertos\_plus\_fat\_cfg.h:

Configuration	Options	Default	Description
Parameter Checking	<ul style="list-style-type: none"> <li>• Default (BSP)</li> <li>• Enabled</li> <li>• Disabled</li> </ul>	Default (BSP)	If selected code for parameter checking is included in the build.

**Configurations for FreeRTOS+ > FreeRTOS+FAT Port for RA**

Configuration	Options	Default	Description
Name	Name must be a valid C symbol	g_rm_freertos_plus_fat 0	Module name.
Total Number of Sectors	Must be a non-negative integer	31293440	Enter the total number of sectors on the device. If this is not known, update <code>rm_freertos_plus_fat_disk_cfg_t::num_blocks</code> after calling <a href="#">RM_FREERTOS_PLUS_FAT_MediaInit()</a> .
Sector Size (bytes)	Must be a power of 2 multiple of 512	512	Select the sector size. Must match the underlying media sector size and at least 512. If this is not known, update <code>rm_freertos_plus_fat_disk_cfg_t::num_blocks</code> after calling <a href="#">RM_FREERTOS_PLUS_FAT_MediaInit()</a> .
Cache Size (bytes)	Must be a power of 2 multiple of 512	1024	Select the cache size. Must be a multiple of the sector size and at least 2 times the sector size.
Partition Number	Must be a non-negative integer	0	Select the partition number for this disk.
Callback	Name must be a valid C symbol	NULL	A user callback function can be provided. If this callback function is provided, it will be called when a card is inserted or removed.

## Usage Notes

### Pending during Read/Write

If the underlying driver supports non-blocking operations, the FreeRTOS+FAT port pends the active FreeRTOS task during read and write operations so other tasks can run in the background.

If FreeRTOS is not used, the FreeRTOS+FAT port spins in a while loop waiting for read and write operations to complete.

## FreeRTOS+FAT without FreeRTOS

To use FreeRTOS+FAT without FreeRTOS, copy FreeRTOSConfigMinimal.h to one of your project's include paths and rename it FreeRTOSConfig.h.

Also, update the Malloc function to malloc and the Free function to free in the Common configurations.

## Examples

### Basic Example

This is a basic example of FreeRTOS+FAT in an application.

```
#define RM_FREERTOS_PLUS_FAT_EXAMPLE_FILE_NAME "TEST_FILE.txt"
#define RM_FREERTOS_PLUS_FAT_EXAMPLE_BUFFER_SIZE_BYTES (10240)
#define RM_FREERTOS_PLUS_FAT_EXAMPLE_PARTITION_NUMBER (0)
extern rm_freertos_plus_fat_instance_ctrl_t g_freertos_plus_fat0_ctrl;
extern const rm_freertos_plus_fat_cfg_t g_freertos_plus_fat0_cfg;
extern const rm_freertos_plus_fat_disk_cfg_t g_rm_freertos_plus_fat_disk_cfg;
extern uint8_t g_file_data[RM_FREERTOS_PLUS_FAT_EXAMPLE_BUFFER_SIZE_BYTES];
extern uint8_t g_read_buffer[RM_FREERTOS_PLUS_FAT_EXAMPLE_BUFFER_SIZE_BYTES];
void rm_freertos_plus_fat_example (void)
{
    /* Open media driver.*/
    fsp_err_t err = RM_FREERTOS_PLUS_FAT_Open(&g_freertos_plus_fat0_ctrl,
&g_freertos_plus_fat0_cfg);
    /* Handle any errors. This function should be defined by the user. */
    handle_error(err);
    /* Initialize the media and the disk. If the media is removable, it must be inserted
before calling
    * RM_FREERTOS_PLUS_FAT_MediaInit. */
    rm_freertos_plus_fat_device_t device;
    err = RM_FREERTOS_PLUS_FAT_MediaInit(&g_freertos_plus_fat0_ctrl, &device);
    handle_error(err);
    /* Initialize one disk for each partition used in the application. */
    FF_Disk_t disk;
    err = RM_FREERTOS_PLUS_FAT_DiskInit(&g_freertos_plus_fat0_ctrl,
&g_rm_freertos_plus_fat_disk_cfg, &disk);
```

```
    handle_error(err);

    /* Mount each disk. This assumes the disk is already partitioned and formatted. */
    FF_Error_t ff_err = FF_Mount(&disk,
RM_FREERTOS_PLUS_FAT_EXAMPLE_PARTITION_NUMBER);

    handle_ff_error(ff_err);

    /* Add the disk to the file system. */
    FF_FS_Add("/", &disk);

    /* Open a source file for writing. */
    FF_FILE * pxSourceFile = ff_fopen((const char *)
RM_FREERTOS_PLUS_FAT_EXAMPLE_FILE_NAME, "w");

    assert(NULL != pxSourceFile);

    /* Write file data. */
    size_t size_return = ff_fwrite(g_file_data, sizeof(g_file_data), 1, pxSourceFile);
    assert(1 == size_return);

    /* Close the file. */
    int close_err = ff_fclose(pxSourceFile);
    assert(0 == close_err);

    /* Open the source file in read mode. */
    pxSourceFile = ff_fopen((const char *) RM_FREERTOS_PLUS_FAT_EXAMPLE_FILE_NAME,
"r");

    assert(NULL != pxSourceFile);

    /* Read file data. */
    size_return = ff_fread(g_read_buffer, sizeof(g_file_data), 1, pxSourceFile);
    assert(1 == size_return);

    /* Close the file. */
    close_err = ff_fclose(pxSourceFile);
    assert(0 == close_err);

    /* Verify the file data read matches the file written. */
    assert(0U == memcmp(g_file_data, g_read_buffer, sizeof(g_file_data)));
}
```

## Format Example

This shows how to partition and format a disk if it is not already partitioned and formatted.

```
void rm_freertos_plus_fat_format_example (void)
{
    /* Open media driver.*/
    fsp_err_t err = RM_FREERTOS_PLUS_FAT_Open(&g_freertos_plus_fat0_ctrl,
&g_freertos_plus_fat0_cfg);
    /* Handle any errors. This function should be defined by the user. */
    handle_error(err);
    /* Initialize the media and the disk. If the media is removable, it must be inserted
before calling
    * RM_FREERTOS_PLUS_FAT_MediaInit. */
    rm_freertos_plus_fat_device_t device;
    err = RM_FREERTOS_PLUS_FAT_MediaInit(&g_freertos_plus_fat0_ctrl, &device);
    handle_error(err);
    /* Initialize one disk for each partition used in the application. */
    FF_Disk_t disk;
    err = RM_FREERTOS_PLUS_FAT_DiskInit(&g_freertos_plus_fat0_ctrl,
&g_rm_freertos_plus_fat_disk_cfg, &disk);
    handle_error(err);
    /* Try to mount the disk. If the disk is not formatted, mount will fail. */
    FF_Error_t ff_err = FF_Mount(&disk,
RM_FREERTOS_PLUS_FAT_EXAMPLE_PARTITION_NUMBER);
    if (FF_isERR((uint32_t) ff_err))
    {
        /* The disk is likely not formatted. Partition and format the disk, then mount
again. */
        FF_PartitionParameters_t partition_params;
        partition_params.ulSectorCount = device.sector_count;
        partition_params.ulHiddenSectors = 1;
        partition_params.ulInterSpace = 0;
        memset(partition_params.xSizes, 0, sizeof(partition_params.xSizes));
        partition_params.xSizes[RM_FREERTOS_PLUS_FAT_EXAMPLE_PARTITION_NUMBER] =
            (BaseType_t) partition_params.ulSectorCount - 1;
        partition_params.xPrimaryCount = 1;
        partition_params.eSizeType = eSizeIsSectors;
    }
}
```



```
    ff_err = FF_Partition(&disk, &partition_params);
    handle_ff_error(ff_err);

    ff_err = FF_Format(&disk, RM_FREERTOS_PLUS_FAT_EXAMPLE_PARTITION_NUMBER,
pdFALSE, pdFALSE);
    handle_ff_error(ff_err);

    ff_err = FF_Mount(&disk, RM_FREERTOS_PLUS_FAT_EXAMPLE_PARTITION_NUMBER);
    handle_ff_error(ff_err);
}
}
```

## Media Insertion Example

This shows how to use the callback to wait for media insertion.

```
#if 2 == BSP_CFG_RTOS
static EventGroupHandle_t xUSBEventGroupHandle = NULL;
#else
volatile uint32_t g_rm_freertos_plus_fat_insertion_events = 0;
volatile uint32_t g_rm_freertos_plus_fat_removal_events = 0;
#endif

/* Callback called by media driver when a removable device is inserted or removed. */
void rm_freertos_plus_fat_test_callback (rm_freertos_plus_fat_callback_args_t *
p_args)
{
#if 2 == BSP_CFG_RTOS
    /* Post an event if FreeRTOS is available. */
    BaseType_t xHigherPriorityTaskWoken = pdFALSE;
    xEventGroupSetBitsFromISR(xUSBEventGroupHandle, p_args->event,
&xHigherPriorityTaskWoken);
    portYIELD_FROM_ISR(xHigherPriorityTaskWoken);
#else
    /* If FreeRTOS is not used, set a global flag. */
    if (p_args->event & RM_FREERTOS_PLUS_FAT_EVENT_MEDIA_INSERTED)
    {
        g_rm_freertos_plus_fat_insertion_events++;
    }
}
}
```

```
    }
    if (p_args->event & RM_FREERTOS_PLUS_FAT_EVENT_MEDIA_REMOVED)
    {
        g_rm_freertos_plus_fat_removal_events++;
    }
#endif
}

void rm_freertos_plus_fat_media_insertion_example (void)
{
#if 2 == BSP_CFG_RTOS
    /* Create event flags if FreeRTOS is used. */
    xUSBEventGroupHandle = xEventGroupCreate();
    TEST_ASSERT_NOT_EQUAL(NULL, xUSBEventGroupHandle);
#endif
    /* Open media driver.*/
    fsp_err_t err = RM_FREERTOS_PLUS_FAT_Open(&g_freertos_plus_fat0_ctrl,
&g_freertos_plus_fat0_cfg);
    /* Handle any errors. This function should be defined by the user. */
    handle_error(err);
    /* Wait for media insertion. */
#if 2 == BSP_CFG_RTOS
        EventBits_t xEventGroupValue = xEventGroupWaitBits(xUSBEventGroupHandle,
RM_FREERTOS_PLUS_FAT_EVENT_MEDIA_INSERTED,
                                                                pdTRUE,
                                                                pdFALSE,
                                                                portMAX_DELAY);

        assert(RM_FREERTOS_PLUS_FAT_EVENT_MEDIA_INSERTED ==
(RM_FREERTOS_PLUS_FAT_EVENT_MEDIA_INSERTED & xEventGroupValue));
#else
    while (0U == g_rm_freertos_plus_fat_insertion_events)
    {
        /* Wait for media insertion. */
    }
#endif
}
```

```
/* Initialize the media and the disk. If the media is removable, it must be inserted
before calling
 * RM_FREERTOS_PLUS_FAT_MediaInit. */
rm_freertos_plus_fat_device_t device;

err = RM_FREERTOS_PLUS_FAT_MediaInit(&g_freertos_plus_fat0_ctrl, &device);
handle_error(err);
/* Initialize one disk for each partition used in the application. */
FF_Disk_t disk;

err = RM_FREERTOS_PLUS_FAT_DiskInit(&g_freertos_plus_fat0_ctrl,
&g_rm_freertos_plus_fat_disk_cfg, &disk);

handle_error(err);
}
```

## Media Insertion Example for USB

This shows how to use the callback to read and write to USB media.

```
void rm_freertos_plus_fat_usb_example (void)
{
#if 2 == BSP_CFG_RTOS
/* Create event flags if FreeRTOS is used. */
xUSBEventGroupHandle = xEventGroupCreate();
#endif

/* Open media driver.*/
fsp_err_t err = RM_FREERTOS_PLUS_FAT_Open(&g_freertos_plus_fat0_ctrl,
&g_freertos_plus_fat0_cfg);

/* Handle any errors. This function should be defined by the user. */
handle_error(err);

/* Wait for the USB media to be attached. */
#if 2 == BSP_CFG_RTOS
EventBits_t xEventGroupValue = xEventGroupWaitBits(xUSBEventGroupHandle,
RM_FREERTOS_PLUS_FAT_EVENT_MEDIA_INSERTED,
pdTRUE,
pdFALSE,
portMAX_DELAY);
```

```
    assert(RM_FREERTOS_PLUS_FAT_EVENT_MEDIA_INSERTED ==
(RM_FREERTOS_PLUS_FAT_EVENT_MEDIA_INSERTED & xEventGroupValue));
#else
    while (0U == g_rm_freertos_plus_fat_insertion_events)
    {
        /* Wait for the USB media to be attached. */
    }
#endif

    /* Initialize the media and the disk. If the media is removable, it must be inserted
before calling
    * RM_FREERTOS_PLUS_FAT_MediaInit. */
    rm_freertos_plus_fat_device_t device;

    err = RM_FREERTOS_PLUS_FAT_MediaInit(&g_freertos_plus_fat0_ctrl, &device);
    handle_error(err);

    /* Initialize one disk for each partition used in the application. */
    FF_Disk_t disk;

    err = RM_FREERTOS_PLUS_FAT_DiskInit(&g_freertos_plus_fat0_ctrl,
&g_rm_freertos_plus_fat_disk_cfg, &disk);

    handle_error(err);

    /* Mount each disk. This assumes the disk is already partitioned and formatted. */
    FF_Error_t ff_err = FF_Mount(&disk,
RM_FREERTOS_PLUS_FAT_EXAMPLE_PARTITION_NUMBER);

    handle_ff_error(ff_err);

    /* Add the disk to the file system. */
    FF_FS_Add("/", &disk);

    /* Open a source file for writing. */
    FF_FILE * pxSourceFile = ff_fopen((const char *)
RM_FREERTOS_PLUS_FAT_EXAMPLE_FILE_NAME, "w");

    assert(NULL != pxSourceFile);

    /* Write file data. */
    size_t size_return = ff_fwrite(g_file_data, sizeof(g_file_data), 1, pxSourceFile);
    assert(1 == size_return);

    /* Close the file. */
    int close_err = ff_fclose(pxSourceFile);
```

```
    assert(0 == close_err);

    /* Open the source file in read mode. */
    pxSourceFile = ff_fopen((const char *) RM_FREERTOS_PLUS_FAT_EXAMPLE_FILE_NAME,
    "r");

    assert(NULL != pxSourceFile);

    /* Read file data. */
    size_return = ff_fread(g_read_buffer, sizeof(g_file_data), 1, pxSourceFile);
    assert(1 == size_return);

    /* Close the file. */
    close_err = ff_fclose(pxSourceFile);
    assert(0 == close_err);

    /* Verify the file data read matches the file written. */
    assert(0U == memcmp(g_file_data, g_read_buffer, sizeof(g_file_data)));
}
```

## Data Structures

struct [rm\\_freertos\\_plus\\_fat\\_instance\\_ctrl\\_t](#)

## Data Structure Documentation

### ◆ [rm\\_freertos\\_plus\\_fat\\_instance\\_ctrl\\_t](#)

struct [rm\\_freertos\\_plus\\_fat\\_instance\\_ctrl\\_t](#)

FreeRTOS plus FAT private control block. DO NOT MODIFY. Initialization occurs when `RM_FREERTOS_PLUS_FAT_Open` is called.

## Function Documentation

### ◆ RM\_FREERTOS\_PLUS\_FAT\_Open()

```
fsp_err_t RM_FREERTOS_PLUS_FAT_Open ( rm_freertos_plus_fat_ctrl_t *const p_ctrl,
rm_freertos_plus_fat_cfg_t const *const p_cfg )
```

Initializes lower layer media device.

Implements `rm_freertos_plus_fat_api_t::open()`.

#### Return values

FSP_SUCCESS	Success.
FSP_ERR_ASSERTION	An input parameter was invalid.
FSP_ERR_ALREADY_OPEN	Module is already open.
FSP_ERR_OUT_OF_MEMORY	Not enough memory to create semaphore.

#### Returns

See [Common Error Codes](#) or functions called by this function for other possible return codes. This function calls:

- `rm_block_media_api_t::open`

### ◆ RM\_FREERTOS\_PLUS\_FAT\_MediaInit()

```
fsp_err_t RM_FREERTOS_PLUS_FAT_MediaInit ( rm_freertos_plus_fat_ctrl_t *const p_ctrl,
rm_freertos_plus_fat_device_t *const p_device )
```

Initializes the media device. This function blocks until all identification and configuration commands are complete.

Implements `rm_freertos_plus_fat_api_t::mediaInit()`.

#### Return values

FSP_SUCCESS	Module is initialized and ready to access the memory device.
FSP_ERR_ASSERTION	An input parameter is invalid.
FSP_ERR_NOT_OPEN	Module has not been initialized.

#### Returns

See [Common Error Codes](#) or functions called by this function for other possible return codes. This function calls:

- `rm_block_media_api_t::mediaInit`
- `rm_block_media_api_t::infoGet`

◆ **RM\_FREERTOS\_PLUS\_FAT\_DiskInit()**

```
fsp_err_t RM_FREERTOS_PLUS_FAT_DiskInit ( rm_freertos_plus_fat_ctrl_t *const p_ctrl,
rm_freertos_plus_fat_disk_cfg_t const *const p_disk_cfg, FF_Disk_t *const p_disk )
```

Initializes a FreeRTOS+FAT disk structure. This function calls FF\_CreateIOManger.

Implements `rm_freertos_plus_fat_api_t::diskInit()`.

**Return values**

FSP_SUCCESS	Module is initialized and ready to access the memory device.
FSP_ERR_ASSERTION	An input parameter is invalid.
FSP_ERR_NOT_OPEN	Module has not been initialized.
FSP_ERR_INTERNAL	Call to FF_CreateIOManger failed.

◆ **RM\_FREERTOS\_PLUS\_FAT\_DiskDeinit()**

```
fsp_err_t RM_FREERTOS_PLUS_FAT_DiskDeinit ( rm_freertos_plus_fat_ctrl_t *const p_ctrl, FF_Disk_t
*const p_disk )
```

Deinitializes a FreeRTOS+FAT disk structure. This function calls FF\_DeleteIOManger.

Implements `rm_freertos_plus_fat_api_t::diskDeinit()`.

**Return values**

FSP_SUCCESS	Module is initialized and ready to access the memory device.
FSP_ERR_ASSERTION	An input parameter is invalid.
FSP_ERR_NOT_OPEN	Module has not been initialized.

◆ **RM\_FREERTOS\_PLUS\_FAT\_InfoGet()**

```
fsp_err_t RM_FREERTOS_PLUS_FAT_InfoGet ( rm_freertos_plus_fat_ctrl_t *const p_ctrl, FF_Disk_t
*const p_disk, rm_freertos_plus_fat_info_t *const p_info )
```

Get partition information. This function can only be called after [rm\\_freertos\\_plus\\_fat\\_api\\_t::diskInit\(\)](#).

Implements [rm\\_freertos\\_plus\\_fat\\_api\\_t::infoGet\(\)](#).

**Return values**

FSP_SUCCESS	Information stored in p_info.
FSP_ERR_ASSERTION	An input parameter was invalid.
FSP_ERR_NOT_OPEN	Module not open.

◆ **RM\_FREERTOS\_PLUS\_FAT\_Close()**

```
fsp_err_t RM_FREERTOS_PLUS_FAT_Close ( rm_freertos_plus_fat_ctrl_t *const p_ctrl)
```

Closes media device.

Implements [rm\\_freertos\\_plus\\_fat\\_api\\_t::close\(\)](#).

**Return values**

FSP_SUCCESS	Media device closed.
FSP_ERR_ASSERTION	An input parameter was invalid.
FSP_ERR_NOT_OPEN	Module not open.

**Returns**

See [Common Error Codes](#) or functions called by this function for other possible return codes. This function calls:

- [rm\\_block\\_media\\_api\\_t::close](#)

◆ **RM\_FREERTOS\_PLUS\_FAT\_VersionGet()**

```
fsp_err_t RM_FREERTOS_PLUS_FAT_VersionGet ( fsp_version_t *const p_version)
```

Returns the version of this module.

Implements [rm\\_freertos\\_plus\\_fat\\_api\\_t::versionGet\(\)](#).

**Return values**

FSP_SUCCESS	Success.
FSP_ERR_ASSERTION	Failed in acquiring version information.



## 4.2.63 FreeRTOS Plus TCP (rm\_freertos\_plus\_tcp)

### Modules

Middleware for using TCP on RA MCUs.

## Overview

FreeRTOS Plus TCP is a TCP stack created for use with FreeRTOS.

This module provides the NetworkInterface required to use FreeRTOS Plus TCP with the [Ethernet \(r\\_ether\)](#) driver.

Please refer to the [FreeRTOS Plus TCP documentation](#) for further details.

## Configuration

### Build Time Configurations for FreeRTOS\_Plus\_TCP

The following build time configurations are defined in aws/FreeRTOSIPConfig.h:

Configuration	Options	Default	Description
Print debug messages	<ul style="list-style-type: none"> <li>Disable</li> <li>Enable</li> </ul>	Disable	If ipconfigHAS_DEBUG_PRINTF is set to 1 then FreeRTOS_debug_printf should be defined to the function used to print out the debugging messages.
Print info messages	<ul style="list-style-type: none"> <li>Disable</li> <li>Enable</li> </ul>	Disable	Set to 1 to print out non debugging messages, for example the output of the FreeRTOS_netstat() command, and ping replies. If ipconfigHAS_PRINTF is set to 1 then FreeRTOS_printf should be set to the function used to print out the messages.
Byte order of the target MCU	pdFREERTOS_LITTLE_ENDIAN	pdFREERTOS_LITTLE_ENDIAN	Define the byte order of the target MCU
IP/TCP/UDP checksums	<ul style="list-style-type: none"> <li>Disable</li> </ul>	Enable	If the network

		<ul style="list-style-type: none"> <li>• Enable</li> </ul>		card/driver includes checksum offloading (IP/TCP/UDP checksums) then set <code>configDRIVER_INCLUDE_D_RX_IP_CHECKSUM</code> to 1 to prevent the software stack repeating the checksum calculations.
Receive Block Time	Value must be an integer		10000	Amount of time <code>FreeRTOS_recv()</code> will block for. The timeouts can be set per socket, using <code>setsockopt()</code> .
Send Block Time	Value must be an integer		10000	Amount of time <code>FreeRTOS_send()</code> will block for. The timeouts can be set per socket, using <code>setsockopt()</code> .
DNS caching	<ul style="list-style-type: none"> <li>• Disable</li> <li>• Enable</li> </ul>		Enable	DNS caching
DNS Request Attempts	Value must be an integer		2	When a cache is present, <code>ipconfigDNS_REQUEST_ATTEMPTS</code> can be kept low and also DNS may use small timeouts.
IP stack task priority	Manual Entry		<code>configMAX_PRIORITIES - 2</code>	Set the priority of the task that executes the IP stack.
Stack size in words (not bytes)	Manual Entry		<code>configMINIMAL_STACK_SIZE * 5</code>	The size, in words (not bytes), of the stack allocated to the FreeRTOS+TCP stack.
Network Events call <code>vApplicationIPNetworkEventHook</code>	<ul style="list-style-type: none"> <li>• Disable</li> <li>• Enable</li> </ul>		Enable	<code>vApplicationIPNetworkEventHook</code> is called when the network connects or disconnects.
Max UDP send block time	Manual Entry		<code>15000 / portTICK_PERIOD_MS</code>	Max UDP send block time
Use DHCP	<ul style="list-style-type: none"> <li>• Disable</li> <li>• Enable</li> </ul>		Enable	If <code>ipconfigUSE_DHCP</code> is 1 then FreeRTOS+TCP will attempt to retrieve an IP address, netmask, DNS server address and gateway address from a DHCP

DHCP Register Hostname	<ul style="list-style-type: none"> <li>• Disable</li> <li>• Enable</li> </ul>	Enable	server. Register hostname when using DHCP
DHCP Uses Unicast	<ul style="list-style-type: none"> <li>• Disable</li> <li>• Enable</li> </ul>	Enable	DHCP uses unicast.
DHCP Send Discover After Auto IP	<ul style="list-style-type: none"> <li>• Disable</li> <li>• Enable</li> </ul>	Disable	DHCP Send Discover After Auto IP
DHCP callback function	<ul style="list-style-type: none"> <li>• Disable</li> <li>• Enable</li> </ul>	Disable	Provide an implementation of the DHCP callback function (xApplicationDHCPHook)
Interval between transmissions	Manual Entry	120000 / portTICK_PERIOD_MS	When ipconfigUSE_DHCP is set to 1, DHCP requests will be sent out at increasing time intervals until either a reply is received from a DHCP server and accepted, or the interval between transmissions reaches ipconfigMAXIMUM_DISCOVER_TX_PERIOD.
ARP Cache Entries	Value must be an integer	6	The maximum number of entries that can exist in the ARP table at any one time
ARP Request Retransmissions	Value must be an integer	5	ARP requests that do not result in an ARP response will be retransmitted a maximum of ipconfigMAX_ARP_RETRANSMISSIONS times before the ARP request is aborted.
Maximum time before ARP table entry becomes stale	Value must be an integer	150	The maximum time between an entry in the ARP table being created or refreshed and the entry being removed because it is stale
Use string for IP Address	<ul style="list-style-type: none"> <li>• Disable</li> <li>• Enable</li> </ul>	Enable	Take an IP in decimal dot format (for example, "192.168.0.1") as its parameter FreeRTOS_in

			et_addr_quick() takes an IP address as four separate numerical octets (for example, 192, 168, 0, 1) as its parameters
Total number of available network buffers	Value must be an integer	10	Define the total number of network buffer that are available to the IP stack
Set the maximum number of events	Please enter a valid function name without spaces or funny characters	ipconfigNUM_NETWORK_BUFFER_DESCRIPTOR + 5	Set the maximum number of events that can be queued for processing at any one time. The event queue must be a minimum of 5 greater than the total number of network buffers
Enable FreeRTOS_sendto() without calling Bind	<ul style="list-style-type: none"> <li>• Enable</li> <li>• Disable</li> </ul>	Disable	Set to 1 then calling FreeRTOS_sendto() on a socket that has not yet been bound will result in the IP stack automatically binding the socket to a port number from the range socketAUTO_PORT_ALLLOCATION_START_NUMBER to 0xffff. If ipconfigALLOW_SOCKET_SEND_WITHOUT_BIND is set to 0 then calling FreeRTOS_sendto() on a socket that has not yet been bound will result in the send operation being aborted.
TTL values for UDP packets	Value must be an integer	128	Define the Time To Live (TTL) values used in outgoing UDP packets
TTL values for TCP packets	Value must be an integer	128	Defines the Time To Live (TTL) values used in outgoing TCP packets
Use TCP and all its features	<ul style="list-style-type: none"> <li>• Disable</li> <li>• Enable</li> </ul>	Enable	Use TCP and all its features
Let TCP use windowing mechanism	<ul style="list-style-type: none"> <li>• Disable</li> <li>• Enable</li> </ul>	Disable	Let TCP use windowing mechanism

Maximum number of bytes the payload of a network frame can contain	Value must be an integer	1500	Maximum number of bytes the payload of a network frame can contain
Basic DNS client or resolver	<ul style="list-style-type: none"> <li>• Disable</li> <li>• Enable</li> </ul>	Enable	Set ipconfigUSE_DNS to 1 to include a basic DNS client/resolver. DNS is used through the FreeRTOS_gethostbyname() API function.
Reply to incoming ICMP echo (ping) requests	<ul style="list-style-type: none"> <li>• Disable</li> <li>• Enable</li> </ul>	Enable	If ipconfigREPLY_TO_INCOMING_PINGS is set to 1 then the IP stack will generate replies to incoming ICMP echo (ping) requests.
FreeRTOS_SendPingRequest() is available	<ul style="list-style-type: none"> <li>• Disable</li> <li>• Enable</li> </ul>	Disable	If ipconfigSUPPORT_OUTGOING_PINGS is set to 1 then the FreeRTOS_SendPingRequest() API function is available.
FreeRTOS_select() (and associated) API function is available	<ul style="list-style-type: none"> <li>• Disable</li> <li>• Enable</li> </ul>	Disable	If ipconfigSUPPORT_SELECT_FUNCTION is set to 1 then the FreeRTOS_select() (and associated) API function is available
Filter out non Ethernet II frames.	<ul style="list-style-type: none"> <li>• Disable</li> <li>• Enable</li> </ul>	Enable	If ipconfigFILTER_OUT_NON_ETHERNET_II_FRAMES is set to 1 then Ethernet frames that are not in Ethernet II format will be dropped. This option is included for potential future IP stack developments
Responsibility of the Ethernet interface to filter out packets	<ul style="list-style-type: none"> <li>• Disable</li> <li>• Enable</li> </ul>	Disable	If ipconfigETHERNET_DRIVER_FILTERS_FRAME_TYPES is set to 1 then it is the responsibility of the Ethernet interface to filter out packets that are of no interest.
Send RST packets, when receive unknown packets.	<ul style="list-style-type: none"> <li>• Disable</li> <li>• Enable</li> </ul>	Enable	TCP will not send RST packets in reply to TCP unknown or out-of-order packets
Block time to simulate MAC interrupts	Please enter a valid function name without spaces or funny	20 / portTICK_PERIOD_MS	The windows simulator cannot really simulate MAC interrupts, and

	characters		needs to block occasionally to allow other tasks to run
Access 32-bit fields in the IP packets	Value must be an integer	2	To access 32-bit fields in the IP packets with 32-bit memory instructions, all packets will be stored 32-bit-aligned, plus 16-bits. This has to do with the contents of the IP-packets: all 32-bit fields are 32-bit-aligned, plus 16-bit
Size of the pool of TCP window descriptors	Value must be an integer	240	Define the size of the pool of TCP window descriptors
Size of Rx buffer for TCP sockets	Value must be an integer	3000	Define the size of Rx buffer for TCP sockets
Size of Tx buffer for TCP sockets	Value must be an integer	3000	Define the size of Tx buffer for TCP sockets
TCP keep-alive	<ul style="list-style-type: none"> <li>• Disable</li> <li>• Enable</li> </ul>	Enable	TCP keep-alive is available or not
TCP keep-alive interval	Value must be an integer	120	TCP keep-alive interval in second
The socket semaphore to unblock the MQTT task (USER_SEMAPHORE)	<ul style="list-style-type: none"> <li>• Disable</li> <li>• Enable</li> </ul>	Disable	The socket semaphore is used to unblock the MQTT task
The socket semaphore to unblock the MQTT task (WAKE_CALLBACK)	<ul style="list-style-type: none"> <li>• Disable</li> <li>• Enable</li> </ul>	Enable	The socket semaphore is used to unblock the MQTT task
The socket semaphore to unblock the MQTT task (USE_CALLBACKS)	<ul style="list-style-type: none"> <li>• Disable</li> <li>• Enable</li> </ul>	Disable	The socket semaphore is used to unblock the MQTT task
The socket semaphore to unblock the MQTT task (TX_DRIVER)	<ul style="list-style-type: none"> <li>• Disable</li> <li>• Enable</li> </ul>	Disable	The socket semaphore is used to unblock the MQTT task
The socket semaphore to unblock the MQTT task (RX_DRIVER)	<ul style="list-style-type: none"> <li>• Disable</li> <li>• Enable</li> </ul>	Disable	The socket semaphore is used to unblock the MQTT task
Possible optimisation for expert users	<ul style="list-style-type: none"> <li>• Disable</li> <li>• Enable</li> </ul>	Disable	Possible optimisation for expert users - requires network driver support. It is useful when there is high network traffic. If non-

zero value then instead of passing received packets into the IP task one at a time the network interface can chain received packets together and pass them into the IP task in one go. If set to 0 then only one buffer will be sent at a time.

## Usage Notes

In order to use the NetworkInterface implementation provided by Renesas for RA devices:

- Configure an `r_ether` instance and provide a pointer to the instance of the NetworkInterface as follows:

```
/* Reference used by the NetworkInterface to access the ethernet instance. */
extern ether_instance_t const * gp_freertos_ether;
...
/* Make it reference the configured ether instance. */
ether_instance_t const * gp_freertos_ether = &g_ether_instance;
```

- Follow the TCP stack initialization procedure as described here: [FreeRTOS+TCP Networking Tutorial: Initializing the TCP/IP Stack](#)

### Note

*The MAC address passed to `FreeRTOS_IPInit` must match the MAC address configured in the `r_ether` instance. `g_ether_instance` must have `vEtherISRcallback` configured as the callback.*

*The `xApplicationGetRandomNumber` and `ulApplicationGetNextSequenceNumber` functions should be implemented in systems using FreeRTOS Plus TCP without Secure Sockets.*

*To connect to a server using an IP address the macro `ipconfigINCLUDE_FULL_INET_ADDR` must be set to 1.*

## Limitations

- Zero-copy is not currently supported by the NetworkInterface.

## 4.2.64 FreeRTOS Port (rm\_freertos\_port)

### Modules

FreeRTOS port for RA MCUs.

## Overview

### Note

*The FreeRTOS Port does not provide any interfaces to the user. Consult the FreeRTOS documentation at <https://www.freertos.org/Documentation> for further information.*

### Features

The RA FreeRTOS port supports the following features:

- Standard FreeRTOS configurations
- Hardware stack monitor

## Configuration

### Build Time Configurations for all

The following build time configurations are defined in aws/FreeRTOSConfig.h:

Configuration	Options	Default	Description
General > Custom FreeRTOSConfig.h	Manual Entry		Add a path to your custom FreeRTOSConfig.h file. It can be used to override some or all of the configurations defined here, and to define additional configurations.
General > Use Preemption	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Enabled	Set to Enabled to use the preemptive RTOS scheduler, or Disabled to use the cooperative RTOS scheduler.
General > Use Port Optimised Task Selection	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Disabled	Some FreeRTOS ports have two methods of selecting the next task to execute - a generic method, and a method that is specific to that port.  The Generic method: Is used when Use Port Optimized Task Selection is set to 0, or when a port specific method is not implemented. Can be used with all



FreeRTOS ports.  
Is completely written in C, making it less efficient than a port specific method.  
Does not impose a limit on the maximum number of available priorities.

A port specific method:  
Is not available for all ports.  
Is used when Use Port Optimized Task Selection is Enabled.  
Relies on one or more architecture specific assembly instructions (typically a Count Leading Zeros [CLZ] or equivalent instruction) so can only be used with the architecture for which it was specifically written.  
Is more efficient than the generic method.  
Typically imposes a limit of 32 on the maximum number of available priorities.

Set Use Tickless Idle to Enabled to use the low power tickless mode, or Disabled to keep the tick interrupt running at all times. Low power tickless implementations are not provided for all FreeRTOS ports.

Enter the frequency in Hz at which the internal clock that drives the peripheral used to generate the tick interrupt will be executing - this is normally the same clock that drives the internal CPU clock. This value is required in order to correctly

General > Use Tickless Idle

- Enabled
- Disabled

Disabled

General > Cpu Clock Hz

Manual Entry

SystemCoreClock

---

General > Tick Rate Hz	Must be an integer and greater than 0	1000	configure timer peripherals.  The frequency of the RTOS tick interrupt. The tick interrupt is used to measure time. Therefore a higher tick frequency means time can be measured to a higher resolution. However, a high tick frequency also means that the RTOS kernel will use more CPU time so be less efficient. The RTOS demo applications all use a tick rate of 1000Hz. This is used to test the RTOS kernel and is higher than would normally be required.  More than one task can share the same priority. The RTOS scheduler will share processor time between tasks of the same priority by switching between the tasks during each RTOS tick. A high tick rate frequency will therefore also have the effect of reducing the 'time slice' given to each task.
General > Max Priorities	Must be an integer and greater than 0	5	The number of priorities available to the application tasks. Any number of tasks can share the same priority. Each available priority consumes RAM within the RTOS kernel so this value should not be set any higher than actually required by your application.
General > Minimal Stack Size	Must be an integer and greater than 0	128	The size of the stack used by the idle task.

Generally this should not be reduced from the value set in the FreeRTOSConfig.h file provided with the demo application for the port you are using. Like the stack size parameter to the xTaskCreate() and xTaskCreateStatic() functions, the stack size is specified in words, not bytes. If each item placed on the stack is 32-bits, then a stack size of 100 means 400 bytes (each 32-bit stack item consuming 4 bytes).

The maximum permissible length of the descriptive name given to a task when the task is created. The length is specified in the number of characters including the NULL termination byte.

Time is measured in 'ticks' - which is the number of times the tick interrupt has executed since the RTOS kernel was started. The tick count is held in a variable of type TickType\_t. Defining configUSE\_16\_BIT\_TICKS as 1 causes TickType\_t to be defined (typedef'ed) as an unsigned 16bit type. Defining configUSE\_16\_BIT\_TICKS as 0 causes TickType\_t to be defined (typedef'ed) as an unsigned 32bit type.

Using a 16-bit type will greatly improve

General > Max Task Name Len      Must be an integer and greater than 0      16

General > Use 16-bit Ticks      Disabled      Disabled

performance on 8- and 16-bit architectures, but limits the maximum specifiable time period to 65535 'ticks'. Therefore, assuming a tick frequency of 250Hz, the maximum time a task can delay or block when a 16bit counter is used is 262 seconds, compared to 17179869 seconds when using a 32-bit counter.

This parameter controls the behaviour of tasks at the idle priority. It only has an effect if: The preemptive scheduler is being used. The application creates tasks that run at the idle priority. If Use Time Slicing is Enabled then tasks that share the same priority will time slice. If none of the tasks get preempted then it might be assumed that each task at a given priority will be allocated an equal amount of processing time - and if the priority is above the idle priority then this is indeed the case. When tasks share the idle priority the behaviour can be slightly different. If Idle Should Yield is Enabled then the idle task will yield immediately if any other task at the idle priority is ready to run. This ensures the minimum amount of time is spent in the idle task when application

General > Idle Should Yield

- Enabled
- Disabled

Enabled

tasks are available for scheduling. This behaviour can however have undesirable effects (depending on the needs of your application) as depicted below:

The diagram above shows the execution pattern of four tasks that are all running at the idle priority. Tasks A, B and C are application tasks. Task I is the idle task. A context switch occurs with regular period at times T0, T1, ..., T6. When the idle task yields task A starts to execute - but the idle task has already consumed some of the current time slice. This results in task I and task A effectively sharing the same time slice. The application tasks B and C therefore get more processing time than the application task A.

This situation can be avoided by:

If appropriate, using an idle hook in place of separate tasks at the idle priority. Creating all application tasks at a priority greater than the idle priority. Setting Idle Should Yield to Disabled. Setting Idle Should Yield to Disabled prevents the idle task from yielding processing time until the end of its time

slice. This ensure all tasks at the idle priority are allocated an equal amount of processing time (if none of the tasks get pre-empted) - but at the cost of a greater proportion of the total processing time being allocated to the idle task.

Setting Use Task Notifications to Enabled will include direct to task notification functionality and its associated API in the build.

Setting Use Task Notifications to Disabled will exclude direct to task notification functionality and its associated API from the build.

Each task consumes 8 additional bytes of RAM when direct to task notifications are included in the build.

Set to Enabled to include mutex functionality in the build, or Disabled to omit mutex functionality from the build. Readers should familiarise themselves with the differences between mutexes and binary semaphores in relation to the FreeRTOS functionality.

Set to Enabled to include recursive mutex functionality in the build, or Disabled to omit recursive mutex functionality from the build.

General > Use Task Notifications

- Enabled
- Disabled

Enabled

General > Use Mutexes

- Enabled
- Disabled

Disabled

General > Use Recursive Mutexes

- Enabled
- Disabled

Disabled

General > Use Counting Semaphores	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Enabled	Set to Enabled to include counting semaphore functionality in the build, or Disabled to omit counting semaphore functionality from the build.
General > Queue Registry Size	Must be an integer and greater than 0	10	<p>The queue registry has two purposes, both of which are associated with RTOS kernel aware debugging: It allows a textual name to be associated with a queue for easy queue identification within a debugging GUI.</p> <p>It contains the information required by a debugger to locate each registered queue and semaphore. The queue registry has no purpose unless you are using a RTOS kernel aware debugger. Registry Size defines the maximum number of queues and semaphores that can be registered. Only those queues and semaphores that you want to view using a RTOS kernel aware debugger need be registered. See the API reference documentation for <code>vQueueAddToRegistry()</code> and <code>vQueueUnregisterQueue()</code> for more information.</p>
General > Use Queue Sets	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Disabled	Set to Enabled to include queue set functionality (the ability to block, or pend, on multiple queues and semaphores), or

General > Use Time Slicing	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Disabled	<p>Disabled to omit queue set functionality.</p> <p>If Use Time Slicing is Enabled, FreeRTOS uses prioritised preemptive scheduling with time slicing. That means the RTOS scheduler will always run the highest priority task that is in the Ready state, and will switch between tasks of equal priority on every RTOS tick interrupt. If Use Time Slicing is Disabled then the RTOS scheduler will still run the highest priority task that is in the Ready state, but will not switch between tasks of equal priority just because a tick interrupt has occurred.</p>
General > Use Newlib Reentrant	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Disabled	<p>If Use Newlib Reentrant is Enabled then a newlib reent structure will be allocated for each created task. Note Newlib support has been included by popular demand, but is not used by the FreeRTOS maintainers themselves. FreeRTOS is not responsible for resulting newlib operation. User must be familiar with newlib and must provide system-wide implementations of the necessary stubs. Be warned that (at the time of writing) the current newlib design implements a system-wide malloc() that must be provided with locks.</p>
General > Enable Backward Compatibility	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Disabled	<p>The FreeRTOS.h header file includes a set of #define macros that</p>



map the names of data types used in versions of FreeRTOS prior to version 8.0.0 to the names used in FreeRTOS version 8.0.0. The macros allow application code to update the version of FreeRTOS they are built against from a pre 8.0.0 version to a post 8.0.0 version without modification. Setting `Enable Backward Compatibility` to `Disabled` in `FreeRTOSConfig.h` excludes the macros from the build, and in so doing allowing validation that no pre version 8.0.0 names are being used.

Sets the number of indexes in each task's thread local storage array.

Sets the type used to specify the stack depth in calls to `xTaskCreate()`, and various other places stack sizes are used (for example, when returning the stack high water mark). Older versions of FreeRTOS specified stack sizes using variables of type `UBaseType_t`, but that was found to be too restrictive on 8-bit microcontrollers. `Stack Depth Type` removes that restriction by enabling application developers to specify the type to use.

FreeRTOS Message buffers use variables of type `Message Buffer`

General > Num Thread Local Storage Pointers	Must be an integer and greater than 0	5	
General > Stack Depth Type	Manual Entry		<code>uint32_t</code>
General > Message Buffer Length Type	Manual Entry		<code>size_t</code>

Length Type to store the length of each message. If Message Buffer Length Type is not defined then it will default to size\_t. If the messages stored in a message buffer will never be larger than 255 bytes then defining Message Buffer Length Type to uint8\_t will save 3 bytes per message on a 32-bit microcontroller. Likewise if the messages stored in a message buffer will never be larger than 65535 bytes then defining Message Buffer Length Type to uint16\_t will save 2 bytes per message on a 32-bit microcontroller.

The highest interrupt priority that can be used by any interrupt service routine that makes calls to interrupt safe FreeRTOS API functions. DO NOT CALL INTERRUPT SAFE FREERTOS API FUNCTIONS FROM ANY INTERRUPT THAT HAS A HIGHER PRIORITY THAN THIS! (higher priorities are lower numeric values)

Below is explanation for macros that are set based on this value from FreeRTOS website.

In the RA port, configKERNEL\_INTERRUPT\_PRIORITY is not used and the kernel runs at the lowest priority.

General > Library Max  
Syscall Interrupt  
Priority

MCU Specific Options

Note in the following discussion that only API functions that end in "FromISR" can be called from within an interrupt service routine.

`configMAX_SYSCALL_INTERRUPT_PRIORITY` sets the highest interrupt priority from which interrupt safe FreeRTOS API functions can be called.

A full interrupt nesting model is achieved by setting `configMAX_SYSCALL_INTERRUPT_PRIORITY` above (that is, at a higher priority level) than `configKERNEL_INTERRUPT_PRIORITY`. This means the FreeRTOS kernel does not completely disable interrupts, even inside critical sections. Further, this is achieved without the disadvantages of a segmented kernel architecture.

Interrupts that do not call API functions can execute at priorities above `configMAX_SYSCALL_INTERRUPT_PRIORITY` and therefore never be delayed by the RTOS kernel execution.

A special note for ARM Cortex-M users: Please read the page dedicated to interrupt priority settings on ARM Cortex-M devices. As a minimum, remember that ARM Cortex-M cores use numerically low priority numbers to represent

HIGH priority interrupts, which can seem counter-intuitive and is easy to forget! If you wish to assign an interrupt a low priority do NOT assign it a priority of 0 (or other low numeric value) as this can result in the interrupt actually having the highest priority in the system - and therefore potentially make your system crash if this priority is above configMAX\_SYSCALL\_INTERRUPT\_PRIORITY.

The lowest priority on a ARM Cortex-M core is in fact 255 - however different ARM Cortex-M vendors implement a different number of priority bits and supply library functions that expect priorities to be specified in different ways. For example, on the RA6M3 the lowest priority you can specify is 15 - and the highest priority you can specify is 0.

The semantics of the configASSERT() macro are the same as the standard C assert() macro. An assertion is triggered if the parameter passed into configASSERT() is zero. configASSERT() is called throughout the FreeRTOS source files to check how the application is using FreeRTOS. It is highly recommended to develop FreeRTOS applications with configASSERT()

General &gt; Assert

Manual Entry

if (!(x)) {\_\_BKPT(0);}

defined.

The example definition (shown at the top of the file and replicated below) calls `vAssertCalled()`, passing in the file name and line number of the triggering `configASSERT()` call (`__FILE__` and `__LINE__` are standard macros provided by most compilers). This is just for demonstration as `vAssertCalled()` is not a FreeRTOS function, `configASSERT()` can be defined to take whatever action the application writer deems appropriate.

It is normal to define `configASSERT()` in such a way that it will prevent the application from executing any further. This is for two reasons; stopping the application at the point of the assertion allows the cause of the assertion to be debugged, and executing past a triggered assertion will probably result in a crash anyway.

Note defining `configASSERT()` will increase both the application code size and execution time. When the application is stable the additional overhead can be removed by simply commenting out the `configASSERT()` definition in `FreeRTOSConfig.h`.

```

/* Define
configASSERT() to call
vAssertCalled() if the
assertion fails. The
assertion
has failed if the value
of the parameter
passed into
configASSERT() equals
zero. */
#define configASSERT(
( x ) ) if( ( x ) == 0 )
vAssertCalled( __FILE__,
__LINE__ )
If running FreeRTOS
under the control of a
debugger, then
configASSERT() can be
defined to just disable
interrupts and sit in a
loop, as demonstrated
below. That will have
the effect of stopping
the code on the line
that failed the assert
test - pausing the
debugger will then
immediately take you
to the offending line so
you can see why it
failed.

```

```

/* Define
configASSERT() to
disable interrupts and
sit in a loop. */
#define configASSERT(
( x ) ) if( ( x ) == 0 ) { t
askDISABLE_INTERRUPTS(); for( ;; ); }

```

General > Include  
Application Defined  
Privileged Functions

- Enabled
  - Disabled
- Disabled

Include Application Defined Privileged Functions is only used by FreeRTOS MPU. If Include Application Defined Privileged Functions is Enabled then the application writer must provide a header file called "application\_defined\_privileged\_functions.h", in which functions the application writer

needs to execute in privileged mode can be implemented. Note that, despite having a .h extension, the header file should contain the implementation of the C functions, not just the functions' prototypes.

Functions implemented in "application\_defined\_privileged\_functions.h" must save and restore the processor's privilege state using the prvRaisePrivilege() function and portRESET\_PRIVILEGE() macro respectively. For example, if a library provided print function accesses RAM that is outside of the control of the application writer, and therefore cannot be allocated to a memory protected user mode task, then the print function can be encapsulated in a privileged function using the following code:

```
void MPU_debug_printf(
const char *pcMessage
)
{
/* State the privilege
level of the processor
when the function was
called. */
BaseType_t
xRunningPrivileged =
prvRaisePrivilege();

/* Call the library
function, which now
has access to all RAM.
*/
debug_printf(
pcMessage );
```

```

/* Reset the processor
privilege level to its
original value. */
portRESET_PRIVILEGE(
xRunningPrivileged );
}

```

This technique should only be use during development, and not deployment, as it circumvents the memory protection.

Set to Enabled if you wish to use an idle hook, or Disabled to omit an idle hook.

The kernel uses a call to `pvPortMalloc()` to allocate memory from the heap each time a task, queue or semaphore is created. The official FreeRTOS download includes four sample memory allocation schemes for this purpose. The schemes are implemented in the `heap_1.c`, `heap_2.c`, `heap_3.c`, `heap_4.c` and `heap_5.c` source files respectively. Use Malloc Failed Hook is only relevant when one of these three sample schemes is being used. The `malloc()` failed hook function is a hook (or callback) function that, if defined and configured, will be called if `pvPortMalloc()` ever returns `NULL`. `NULL` will be returned only if there is insufficient FreeRTOS heap memory remaining for the requested allocation to succeed.

If Use Malloc Failed

Hooks > Use Idle Hook

- Enabled
- Disabled

Enabled

Hooks > Use Malloc  
Failed Hook

- Enabled
- Disabled

Disabled



Hook is Enabled then the application must define a malloc() failed hook function. If Use Malloc Failed Hook is set to Disabled then the malloc() failed hook function will not be called, even if one is defined. Malloc() failed hook functions must have the name and prototype shown below.

```
void vApplicationMallocFailedHook( void );
```

If Use Timers and Use Daemon Task Startup Hook are both Enabled then the application must define a hook function that has the exact name and prototype as shown below. The hook function will be called exactly once when the RTOS daemon task (also known as the timer service task) executes for the first time. Any application initialisation code that needs the RTOS to be running can be placed in the hook function.

```
void vApplicationDaemonTaskStartupHook( void );
```

Set to Enabled if you wish to use an tick hook, or Disabled to omit an tick hook.

The stack overflow detection page describes the use of this parameter. This is not recommended for RA MCUs with hardware stack monitor support. RA MCU designs should enable

Hooks > Use Daemon Task Startup Hook

- Enabled
- Disabled

Disabled

Hooks > Use Tick Hook

- Enabled
- Disabled

Disabled

Hooks > Check For Stack Overflow

- Enabled
- Disabled

Disabled

Stats > Use Trace Facility	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Disabled	<p>the RA hardware stack monitor instead.</p> <p>Set to Enabled if you wish to include additional structure members and functions to assist with execution visualisation and tracing.</p>
Stats > Use Stats Formatting Functions	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Disabled	<p>Set Use Trace Facility and Use Stats Formatting Functions to Enabled to include the vTaskList() and vTaskGetRunTimeStats() functions in the build. Setting either to Disabled will omit vTaskList() and vTaskGetRunTimeStats() from the build.</p>
Stats > Generate Run Time Stats	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Disabled	<p>The Run Time Stats page describes the use of this parameter.</p>
Memory Allocation > Support Static Allocation	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Enabled	<p>If Support Static Allocation is Enabled then RTOS objects can be created using RAM provided by the application writer. If Support Static Allocation is Disabled then RTOS objects can only be created using RAM allocated from the FreeRTOS heap.</p> <p>If Support Static Allocation is left undefined it will default to 0.</p> <p>If Support Static Allocation is Enabled then the application writer must also provide two callback functions: vApplicationGetIdleTaskMemory() to provide the memory for use by the RTOS Idle task, and (if Use</p>

Timers is Enabled) vApplicationGetTimerTaskMemory() to provide memory for use by the RTOS Daemon/Timer Service task. Examples are provided below.

```
/* Support Static Allocation is Enabled, so the application must provide an implementation of vApplicationGetIdleTaskMemory() to provide the memory that is used by the Idle task. */  
void vApplicationGetIdleTaskMemory(  
    StaticTask_t **ppxIdleTaskTCBBuffer,<br>  
    StackType_t **ppxIdleTaskStackBuffer,<br>  
    uint32_t *puxIdleTaskStackSize )  
{  
    /* If the buffers to be provided to the Idle task are declared inside this function then they must be declared static - otherwise they will be allocated on the stack and so not exists after this function exits. */  
    static StaticTask_t xIdleTaskTCB;  
    static StackType_t uxIdleTaskStack[ configMINIMAL_STACK_SIZE ];  
  
    /* Pass out a pointer to the StaticTask_t structure in which the Idle task's state will be stored. */  
    *ppxIdleTaskTCBBuffer =  
  
    /* Pass out the array that will be used as the Idle task's stack. */
```

```
*ppxIdleTaskStackBuffer = uxIdleTaskStack;
```

```
/* Pass out the size of the array pointed to by *ppxIdleTaskStackBuffer.
```

```
Note that, as the array is necessarily of type StackType_t, configMINIMAL_STACK_SIZE is specified in words, not bytes. */
*pullIdleTaskStackSize = configMINIMAL_STACK_SIZE;
}
/*-----*/
-----*/
```

```
/* Support Static Allocation and Use Timers are both Enabled, so the application must provide an implementation of vApplicationGetTimerTaskMemory() to provide the memory that is used by the Timer service task. */
void vApplicationGetTimerTaskMemory(
    StaticTask_t **ppxTimerTaskTCBBuffer, <br>
    StackType_t **ppxTimerTaskStackBuffer, <br>
    uint32_t *pulTimerTaskStackSize )
{
    /* If the buffers to be provided to the Timer task are declared inside this function then they must be declared static - otherwise they will be allocated on the stack and so not exist after this function exits. */
    static StaticTask_t xTimerTaskTCB;
```

```
static StackType_t
uxTimerTaskStack[ configTIMER_TASK_STACK_
DEPTH ];
```

```
/* Pass out a pointer to
the StaticTask_t
structure in which the
Timer
task's state will be
stored. */
*ppxTimerTaskTCBBuffer =
```

```
/* Pass out the array
that will be used as the
Timer task's stack. */
*ppxTimerTaskStackBuffer =
uxTimerTaskStack;
```

```
/* Pass out the size of
the array pointed to by
*ppxTimerTaskStackBuffer.
```

```
Note that, as the array
is necessarily of type
StackType_t,
configTIMER_TASK_STACK_DEPTH
is specified in words, not bytes. */
*puTimerTaskStackSize = configTIMER_TASK_
STACK_DEPTH;
}
```

Examples of the callback functions that must be provided by the application to supply the RAM used by the Idle and Timer Service tasks if Support Static Allocation is Enabled.

See the Static Vs Dynamic Memory Allocation page for more information.

If Support Dynamic Allocation is Enabled then RTOS objects can be created using RAM

Memory Allocation >  
Support Dynamic  
Allocation

- Enabled
  - Disabled
- Disabled

that is automatically allocated from the FreeRTOS heap. If Support Dynamic Allocation is set to 0 then RTOS objects can only be created using RAM provided by the application writer.

See the Static Vs Dynamic Memory Allocation page for more information.

The total amount of RAM available in the FreeRTOS heap. This value will only be used if Support Dynamic Allocation is Enabled and the application makes use of one of the sample memory allocation schemes provided in the FreeRTOS source code download. See the memory configuration section for further details.

By default the FreeRTOS heap is declared by FreeRTOS and placed in memory by the linker. Setting Application Allocated Heap to Enabled allows the heap to instead be declared by the application writer, which allows the application writer to place the heap wherever they like in memory.

If heap\_1.c, heap\_2.c or heap\_4.c is used, and Application Allocated Heap is Enabled, then the application writer must provide a uint8\_t array with the exact name and dimension as shown below. The

Memory Allocation > Total Heap Size      Must be an integer and greater than 0      1024

Memory Allocation > Application Allocated Heap      • Enabled      Disabled  
 • Disabled

array will be used as the FreeRTOS heap. How the array is placed at a specific memory location is dependent on the compiler being used - refer to your compiler's documentation.

```
uint8_t ucHeap[
configTOTAL_HEAP_SIZE
];
```

Set to Enabled to include software timer functionality, or Disabled to omit software timer functionality. See the FreeRTOS software timers page for a full description.

Sets the priority of the software timer service/daemon task. See the FreeRTOS software timers page for a full description.

Sets the length of the software timer command queue. See the FreeRTOS software timers page for a full description.

Sets the stack depth allocated to the software timer service/daemon task. See the FreeRTOS software timers page for a full description.

Include vTaskPrioritySet() function in build

Include uxTaskPriorityGet() function in build

Include vTaskDelete() function in build

Include

Timers > Use Timers	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Enabled
---------------------	---------------------------------------------------------------------------------	---------

Timers > Timer Task Priority	Must be an integer and greater than 0	3
------------------------------	---------------------------------------	---

Timers > Timer Queue Length	Must be an integer and greater than 0	10
-----------------------------	---------------------------------------	----

Timers > Timer Task Stack Depth	Must be an integer and greater than 0	128
---------------------------------	---------------------------------------	-----

Optional Functions > vTaskPrioritySet() Function	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Enabled
--------------------------------------------------	---------------------------------------------------------------------------------	---------

Optional Functions > uxTaskPriorityGet() Function	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Enabled
---------------------------------------------------	---------------------------------------------------------------------------------	---------

Optional Functions > vTaskDelete() Function	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Enabled
---------------------------------------------	---------------------------------------------------------------------------------	---------

Optional Functions >	<ul style="list-style-type: none"> <li>• Enabled</li> </ul>	Enabled
----------------------	-------------------------------------------------------------	---------

vTaskSuspend() Function	• Disabled		vTaskSuspend() function in build
Optional Functions > xResumeFromISR() Function	• Enabled • Disabled	Enabled	Include xResumeFromISR() function in build
Optional Functions > vTaskDelayUntil() Function	• Enabled • Disabled	Enabled	Include vTaskDelayUntil() function in build
Optional Functions > vTaskDelay() Function	• Enabled • Disabled	Enabled	Include vTaskDelay() function in build
Optional Functions > x TaskGetSchedulerState ( ) Function	• Enabled • Disabled	Enabled	Include xTaskGetSched ulerState() function in build
Optional Functions > x TaskGetCurrentTaskHa ndle() Function	• Enabled • Disabled	Enabled	Include xTaskGetCurre ntTaskHandle() function in build
Optional Functions > u xTaskGetStackHighWat erMark() Function	• Enabled • Disabled	Disabled	Include uxTaskGetStac kHighWaterMark() function in build
Optional Functions > x TaskGetIdleTaskHandle ( ) Function	• Enabled • Disabled	Disabled	Include xTaskGetIdleTa skHandle() function in build
Optional Functions > eTaskGetState() Function	• Enabled • Disabled	Disabled	Include eTaskGetState() function in build
Optional Functions > x EventGroupSetBitFromI SR() Function	• Enabled • Disabled	Enabled	Include xEventGroupSe tBitFromISR() function in build
Optional Functions > x TimerPendFunctionCall( ) Function	• Enabled • Disabled	Disabled	Include xTimerPendFun ctionCall() function in build
Optional Functions > xTaskAbortDelay() Function	• Enabled • Disabled	Disabled	Include xTaskAbortDelay() function in build
Optional Functions > xTaskGetHandle() Function	• Enabled • Disabled	Disabled	Include xTaskGetHandle() function in build
Optional Functions > xTaskResumeFromISR() Function	• Enabled • Disabled	Enabled	Include xTaskResumeFromISR() function in build
RA > Hardware Stack Monitor	• Enabled • Disabled	Disabled	Include RA stack monitor
Logging > Print String Function	Manual Entry	printf(x)	
Logging > Logging Max	Manual Entry	192	



Message Length

Logging > Logging	• Disabled	Disabled
Include Time and Task Name	• Enabled	

## Clock Configuration

The FreeRTOS port uses the SysTick timer as the system clock. The timer rate is configured in the FreeRTOS component under General > Tick Rate Hz.

## Pin Configuration

This module does not use I/O pins.

# Usage Notes

## Hardware Stack Monitor

The hardware stack monitor generates an NMI if the PSP goes out of the memory area for the stack allocated for the current task. A callback can be registered using [R\\_BSP\\_GroupIrqWrite\(\)](#) to be called whenever a stack overflow or underflow of the PSP for a particular thread is detected.

## Stack Monitor Underflow Detection

By default the hardware stack monitor only checks for overflow of the process stack. To check for underflow define `configRECORD_STACK_HIGH_ADDRESS` as 1 on the command line.

## Low Power Modes

When FreeRTOS is configured to use tickless idle, the idle task executes `WFI()` when no task is ready to run. If the MCU is configured to enter software standby mode or deep software standby mode when the idle task executes `WFI()`, the RA FreeRTOS port changes the low power mode to sleep mode so the idle task can wake from SysTick. The low power mode settings are restored when the MCU wakes from sleep mode.

## TrustZone Integration

When using an RTOS in a TrustZone project, ARM recommends keeping the RTOS in the non-secure project. Tasks may call non-secure callable functions if the task has allocated a secure context (using `portALLOCATE_SECURE_CONTEXT`).

The secure context can be freed by deleting the thread or using the `portCLEAN_UP_TCB(pxTCB)` macro.

# Examples

## Stack Monitor Example

This is an example of using the stack monitor in an application.

```
#if BSP_FEATURE_BSP_HAS_SP_MON
void stack_monitor_callback(bsp_grp_irq_t irq);
```

```
void rm_freertos_port_stack_monitor_example(void);
void stack_monitor_callback (bsp_grp_irq_t irq)
{
    FSP_PARAMETER_NOT_USED(irq);
    if (1U == R_MPU_SPMON->SP[0].CTL_b.ERROR)
    {
        /* Handle main stack monitor error here. */
    }
    if (1U == R_MPU_SPMON->SP[1].CTL_b.ERROR)
    {
        /* Handle process stack monitor error here. */
    }
}
void rm_freertos_port_stack_monitor_example (void)
{
    /* Register a callback to be called when the stack goes outside the allocated stack
area. */
    R_BSP_GroupIrqWrite(BSP_GRP_IRQ_MPU_STACK, stack_monitor_callback);
}
#endif
```

## TrustZone Example

This is an example of calling portALLOCATE\_SECURE\_CONTEXT before calling any non-secure callable functions in a task.

```
void rm_freertos_port_trustzone_thread_example (void)
{
    /* When FreeRTOS is used in a non-secure TrustZone application,
portALLOCATE_SECURE_CONTEXT must be called prior
    * to calling any non-secure callable function in a task. The parameter is unused in
the FSP implementation. */
    portALLOCATE_SECURE_CONTEXT(0);
    rm_freertos_port_nsc_function();
}
```

## 4.2.65 RTOS Context Management (rm\_tz\_context)

### Modules

RTOS Context Management for RA MCUs.

## Overview

Add this module to a secure TrustZone project to allow the associated non-secure project to use an RTOS. It is used by an RTOS port for RA MCUs (for example, the [FreeRTOS Port \(rm\\_freertos\\_port\)](#), which is automatically added to RA projects when FreeRTOS is selected during project creation).

### Note

*The RTOS Context Management module does not provide any interfaces to the user. To use this module to port an RTOS, consult the Arm documentation at [https://arm-software.github.io/CMSIS\\_5/Core/html/group\\_\\_context\\_\\_trustzone\\_\\_functions.html](https://arm-software.github.io/CMSIS_5/Core/html/group__context__trustzone__functions.html) for further information.*

## Configuration

### Build Time Configurations for rm\_tz\_context

The following build time configurations are defined in fsp\_cfg/rm\_tz\_context\_cfg.h:

Configuration	Options	Default	Description
Process Stack Slots	Value must be a non-negative integer greater than 0	8	The maximum number of threads that can allocate a secure context. For applications using FreeRTOS, the Idle task requires 1 context as well.
Process Stack Size	Value must be a non-negative multiple of 8	256	The maximum stack size of all non-secure callable functions.

### Clock Configuration

This module does not use peripheral clocks.

### Pin Configuration

This module does not use I/O pins.

## Usage Notes

## TrustZone Integration

When using an RTOS in a TrustZone project, ARM recommends keeping the RTOS in the non-secure project. Tasks may call non-secure callable functions if the task has allocated a secure context. To allocate a secure context, reference the documentation for the RTOS port used. For example, reference [TrustZone Integration](#) when FreeRTOS is used.

### 4.2.66 LittleFS Flash Port (rm\_littlefs\_flash)

#### Modules

#### Functions

fsp\_err\_t RM\_LITTLEFS\_FLASH\_Open (rm\_littlefs\_ctrl\_t \*const p\_ctrl,  
rm\_littlefs\_cfg\_t const \*const p\_cfg)

fsp\_err\_t RM\_LITTLEFS\_FLASH\_Close (rm\_littlefs\_ctrl\_t \*const p\_ctrl)

fsp\_err\_t RM\_LITTLEFS\_FLASH\_VersionGet (fsp\_version\_t \*const p\_version)

#### Detailed Description

Middleware for the LittleFS File System control on RA MCUs.

## Overview

This module provides the hardware port layer for the LittleFS file system. After initializing this module, refer to the LittleFS documentation to use the file system:

<https://github.com/ARMmbed/littlefs>

## Configuration

### Build Time Configurations for rm\_littlefs\_flash

The following build time configurations are defined in fsp\_cfg/rm\_littlefs\_flash\_cfg.h:

Configuration	Options	Default	Description
Parameter Checking Enable	<ul style="list-style-type: none"> <li>Default (BSP)</li> <li>Enabled</li> <li>Disabled</li> </ul>	Default (BSP)	If selected code for parameter checking is included in the build.

### Configurations for Middleware > LittleFS on Flash

Configuration	Options	Default	Description
Name	Name must be a valid C symbol	g_rm_littlefs0	Module name.
Read Size	Must be a non-negative	1	Minimum size of a

	integer		block read. All read operations will be a multiple of this value.
Program Size	Must be a non-negative integer	4	Minimum size of a block program. All program operations will be a multiple of this value.
Block Size (bytes)	Must be a multiple of 64	128	Size of an erasable block. This does not impact RAM consumption and may be larger than the physical erase size. However, non-inlined files take up at minimum one block. Must be a multiple of the read and program sizes.
Block Count	Manual Entry	(BSP_DATA_FLASH_SIZE_BYTES/128)	Number of erasable blocks on the device.
Block Cycles	Must be an integer	1024	Number of erase cycles before LittleFS evicts metadata logs and moves the metadata to another block. Suggested values are in the range 100-1000, with large values having better performance at the cost of less consistent wear distribution. Set to -1 to disable block-level wear-leveling.
Cache Size	Must be a non-negative integer	64	Size of block caches. Each cache buffers a portion of a block in RAM. The LittleFS needs a read cache, a program cache, and one additional cache per file. Larger caches can improve performance by storing more data and reducing the number of disk accesses. Must be a multiple of the read and program sizes, and a factor of the block

size.

Lookahead Size	Must be a non-negative multiple of 8	16	Size of the lookahead buffer in bytes. A larger lookahead buffer increases the number of blocks found during an allocation pass. The lookahead buffer is stored as a compact bitmap, so each byte of RAM can track 8 blocks. Must be a multiple of 8.
----------------	--------------------------------------	----	-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------

## Common LittleFS Configuration

### Build Time Configurations for LittleFS

The following build time configurations are defined in arm/littlefs/lfs\_util.h:

Configuration	Options	Default	Description
Custom lfs_util.h	Manual Entry		Add a path to your custom lfs_util.h file. It can be used to override some or all of the configurations defined here, and to define additional configurations.
Use Malloc	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Enabled	Configures the use of malloc by LittleFS.
Use Assert	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Enabled	Configures the use of assert by LittleFS.
Debug Messages	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Enabled	Configures debug messages.
Warning Messages	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Enabled	Configures warning messages.
Error Messages	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Enabled	Configures error messages.
Trace Messages	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Disabled	Configures trace messages.
Intrinsics	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Enabled	Configures intrinsic functions such as <code>__builtin_clz</code> .
Instance Name for STDIO wrapper	Name must be a valid C symbol	g_rm_littlefs0	The <code>rm_littlefs</code> instance name to use with the STDIO wrapper.

# Usage Notes

## Blocking Read/Write/Erase

The LittleFS port blocks on Read/Write/Erase calls until the operation has completed.

## Memory Constraints

The block size defined in the LittleFS configuration must be a multiple of the data flash erase size of the MCU. It must be greater than 104bytes which is the minimum block size of a LittleFS block. For information about data flash erase sizes refer to the "Specifications of the code flash memory and data flash memory" table of the "Flash Memory" chapter's "Overview" section.

## Limitations

This module is not thread safe.

# Examples

## Basic Example

This is a basic example of LittleFS on Flash in an application.

```
extern const rm_littlefs_cfg_t g_rm_littlefs_flash0_cfg;
#ifdef LFS_NO_MALLOC
static uint8_t g_file_buffer[LFS_CACHE_SIZE];
static struct lfs_file_config g_file_cfg =
{
    .buffer = g_file_buffer
};
#endif
void rm_littlefs_example (void)
{
    uint8_t    buffer[30];
    lfs_file_t file;
    /* Open LittleFS Flash port.*/
    fsp_err_t err = RM_LITTLEFS_FLASH_Open(&g_rm_littlefs_flash0_ctrl,
&g_rm_littlefs_flash0_cfg);
    /* Handle any errors. This function should be defined by the user. */
    handle_error(err);
    /* Format the filesystem. */
    int lfs_err = lfs_format(&g_rm_littlefs_flash0_lfs, &g_rm_littlefs_flash0_lfs_cfg);
    handle_lfs_error(lfs_err);
}
```

```
/* Mount the filesystem. */
    lfs_err = lfs_mount(&g_rm_littlefs_flash0_lfs, &g_rm_littlefs_flash0_lfs_cfg);
    handle_lfs_error(lfs_err);

/* Create a breakfast directory. */
    lfs_err = lfs_mkdir(&g_rm_littlefs_flash0_lfs, "breakfast");
    handle_lfs_error(lfs_err);

/* Create a file toast in the breakfast directory. */
    const char * path = "breakfast/toast";

#ifdef LFS_NO_MALLOC
    /*****
    *****/
    * By default LittleFS uses malloc to allocate buffers. This can be disabled in the
    RA Configuration editor.
    * Buffers will be generated from the configuration for the read, program and
    lookahead buffers.
    * When opening a file a unique buffer must be passed in for use as a file buffer.
    * The buffer size must be equal to the cache size.
    *****/
    *****/
    lfs_err = lfs_file_opencfg(&g_rm_littlefs_flash0_lfs,
                               &file,
                               path,
                               LFS_O_WRONLY | LFS_O_CREAT | LFS_O_APPEND,
                               &g_file_cfg);

    handle_lfs_error(lfs_err);
#else
    lfs_err = lfs_file_open(&g_rm_littlefs_flash0_lfs, &file, path, LFS_O_WRONLY |
LFS_O_CREAT | LFS_O_APPEND);
    handle_lfs_error(lfs_err);
#endif

    const char * contents = "butter";
    lfs_size_t len = strlen(contents);

/* Apply butter to toast 10 times. */
    for (uint32_t i = 0; i < 10; i++)
```



```
{
    lfs_err = lfs_file_write(&g_rm_littlefs_flash0_lfs, &file, contents, len);
if (lfs_err < 0)
    {
        handle_lfs_error(lfs_err);
    }
}

/* Close the file. */
lfs_err = lfs_file_close(&g_rm_littlefs_flash0_lfs, &file);
handle_lfs_error(lfs_err);

/* Unmount the filesystem. */
lfs_err = lfs_unmount(&g_rm_littlefs_flash0_lfs);
handle_lfs_error(lfs_err);

/* Remount the filesystem. */
lfs_err = lfs_mount(&g_rm_littlefs_flash0_lfs, &g_rm_littlefs_flash0_lfs_cfg);
handle_lfs_error(lfs_err);

/* Open breakfast/toast. */
#ifdef LFS_NO_MALLOC
    lfs_err = lfs_file_opencfg(&g_rm_littlefs_flash0_lfs, &file, path, LFS_O_RDONLY,
&g_file_cfg);
    handle_lfs_error(lfs_err);
#else
    lfs_err = lfs_file_open(&g_rm_littlefs_flash0_lfs, &file, path, LFS_O_RDONLY);
    handle_lfs_error(lfs_err);
#endif

    handle_lfs_error(lfs_err);

/* Verify the toast is buttered the correct amount. */
for (uint32_t i = 0; i < 10; i++)
    {
        lfs_err = lfs_file_read(&g_rm_littlefs_flash0_lfs, &file, buffer, len);
if (lfs_err < 0)
    {
        handle_lfs_error(lfs_err);
    }
    }
```

```

if (0 != memcmp(buffer, contents, len))
{
    handle_error(FSP_ERR_ASSERTION);
}
}

/* Close the file. */
lfs_err = lfs_file_close(&g_rm_littlefs_flash0_lfs, &file);
handle_lfs_error(lfs_err);
}

```

## Function Documentation

### ◆ RM\_LITTLEFS\_FLASH\_Open()

`fsp_err_t` RM\_LITTLEFS\_FLASH\_Open ( `rm_littlefs_ctrl_t` \*const *p\_ctrl*, `rm_littlefs_cfg_t` const \*const *p\_cfg* )

Opens the driver and initializes lower layer driver.

Implements `rm_littlefs_api_t::open()`.

#### Return values

FSP_SUCCESS	Success.
FSP_ERR_ASSERTION	An input parameter was invalid.
FSP_ERR_ALREADY_OPEN	Module is already open.
FSP_ERR_INVALID_SIZE	The provided block size is invalid.
FSP_ERR_INVALID_ARGUMENT	Flash BGO mode must be disabled.

#### Returns

See [Common Error Codes](#) or functions called by this function for other possible return codes. This function calls:

- `flash_api_t::open`

◆ **RM\_LITTLEFS\_FLASH\_Close()**

```
fsp_err_t RM_LITTLEFS_FLASH_Close ( rm_littlefs_ctrl_t *const p_ctrl)
```

Closes the lower level driver.

Implements `rm_littlefs_api_t::close()`.

**Return values**

FSP_SUCCESS	Media device closed.
FSP_ERR_ASSERTION	An input parameter was invalid.
FSP_ERR_NOT_OPEN	Module not open.

**Returns**

See [Common Error Codes](#) or functions called by this function for other possible return codes. This function calls:

- `flash_api_t::close`

◆ **RM\_LITTLEFS\_FLASH\_VersionGet()**

```
fsp_err_t RM_LITTLEFS_FLASH_VersionGet ( fsp_version_t *const p_version)
```

Returns the version of this module.

Implements `rm_littlefs_api_t::versionGet()`.

**Return values**

FSP_SUCCESS	Success.
FSP_ERR_ASSERTION	Failed in acquiring version information.

**4.2.67 Motor Current (rm\_motor\_current)****Modules****Functions**

```
fsp_err_t RM_MOTOR_CURRENT_Open (motor_current_ctrl_t *const p_ctrl,
motor_current_cfg_t const *const p_cfg)
```

Opens and configures the Motor Current Module. Implements `motor_current_api_t::open`. [More...](#)

```
fsp_err_t RM_MOTOR_CURRENT_Close (motor_current_ctrl_t *const p_ctrl)
```

Disables specified Motor Current Module. Implements `motor_current_api_t::close`. [More...](#)

`fsp_err_t RM_MOTOR_CURRENT_Reset (motor_current_ctrl_t *const p_ctrl)`

Reset variables of Motor Current Module. Implements `motor_current_api_t::reset`. [More...](#)

`fsp_err_t RM_MOTOR_CURRENT_Run (motor_current_ctrl_t *const p_ctrl)`

Run(Start) the Current Control. Implements `motor_current_api_t::run`. [More...](#)

`fsp_err_t RM_MOTOR_CURRENT_ParameterSet (motor_current_ctrl_t *const p_ctrl, motor_current_input_t const *const p_st_input)`

Set (Input) Parameter Data. Implements `motor_current_api_t::parameterSet`. [More...](#)

`fsp_err_t RM_MOTOR_CURRENT_CurrentReferenceSet (motor_current_ctrl_t *const p_ctrl, float const id_reference, float const iq_reference)`

Set Current Reference Data. Implements `motor_current_api_t::currentReferenceSet`. [More...](#)

`fsp_err_t RM_MOTOR_CURRENT_SpeedPhaseSet (motor_current_ctrl_t *const p_ctrl, float const speed, float const phase)`

Set Current Speed & rotor phase Data. Implements `motor_current_api_t::speedPhaseSet`. [More...](#)

`fsp_err_t RM_MOTOR_CURRENT_CurrentSet (motor_current_ctrl_t *const p_ctrl, motor_current_input_current_t const *const p_st_current, motor_current_input_voltage_t const *const p_st_voltage)`

Set d/q-axis Current & Voltage Data. Implements `motor_current_api_t::currentSet`. [More...](#)

`fsp_err_t RM_MOTOR_CURRENT_ParameterGet (motor_current_ctrl_t *const p_ctrl, motor_current_output_t *const p_st_output)`

Get Output Parameters. Implements `motor_current_api_t::parameterGet`. [More...](#)

`fsp_err_t RM_MOTOR_CURRENT_CurrentGet (motor_current_ctrl_t *const p_ctrl, float *const p_id, float *const p_iq)`

Get d/q-axis Current. Implements `motor_current_api_t::currentGet`. [More...](#)

`fsp_err_t RM_MOTOR_CURRENT_PhaseVoltageGet (motor_current_ctrl_t *const p_ctrl, motor_current_get_voltage_t *const p_voltage)`

Gets the set phase voltage. Implements `motor_current_api_t::phaseVoltageGet`. More...

`fsp_err_t RM_MOTOR_CURRENT_ParameterUpdate (motor_current_ctrl_t *const p_ctrl, motor_current_cfg_t const *const p_cfg)`

Update the parameters of Current Control. Implements `motor_current_api_t::parameterUpdate`. More...

`fsp_err_t RM_MOTOR_CURRENT_VersionGet (fsp_version_t *const p_version)`

### Detailed Description

Calculation process for the motor control on RA MCUs. This module implements the [Interface](#).

## Overview

The motor current is used to control the electric current of motor rotation in an application. This module should be called cyclically after the A/D conversion of electric current of each phase in an application. This module calculates each phase voltage with input current reference, electric current and rotor angle.

## BLOCK DIAGRAM OF SENSORLESS VECTOR CONTROL

It is a block diagram of sensorless vector control. This shows the correspondence between modules and functional blocks.

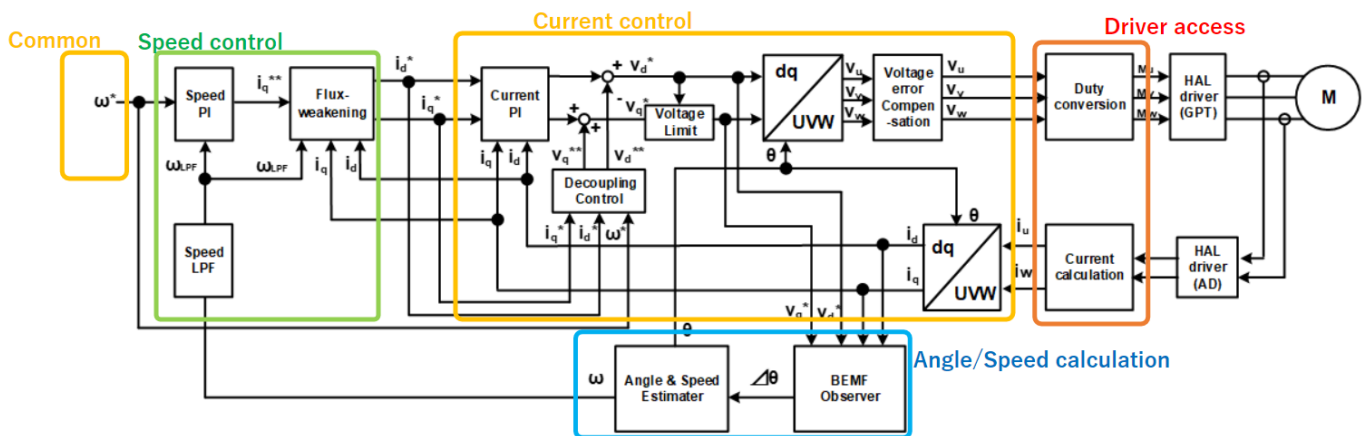


Figure 185: Image of Current Control Module(yellow block)

### Features

The Motor Current Module has below features.

- Calculate each phase(U/V/W) voltage.
- Decoupling Control.
- Voltage Error Compensation.

## Configuration

### Build Time Configurations for rm\_motor\_current

The following build time configurations are defined in fsp\_cfg/rm\_motor\_current\_cfg.h:

Configuration	Options	Default	Description
Parameter Checking	<ul style="list-style-type: none"> <li>• Default (BSP)</li> <li>• Enabled</li> <li>• Disabled</li> </ul>	Default (BSP)	If selected code for parameter checking is included in the build.

### Configurations for Middleware > Motor > Motor Current Controller on rm\_motor\_current

This module can be added to the Stacks tab via New Stack > Middleware > Motor > Motor Current Controller on rm\_motor\_current.

Configuration	Options	Default	Description
General > Name	Name must be a valid C symbol	g_motor_current0	Module name.
General > Current Control Decimation	Manual Entry	0	Decimation of Current Control.
General > PWM Carrier Frequency[kHz]	Manual Entry	20.0F	PWM Carrier Frequency.
General > Limit of electric current	Manual Entry	12.0F	Limit of electric current.
General > Voltage error compensation	<ul style="list-style-type: none"> <li>• Disable</li> <li>• Enable</li> </ul>	Enable	Select enable/disable Voltage error compensation.
General > Voltage error compensation table of voltage 1	Manual Entry	0.326F	Voltage error compensation table of voltage.
General > Voltage error compensation table of voltage 2	Manual Entry	0.535F	Voltage error compensation table of voltage.
General > Voltage error compensation table of voltage 3	Manual Entry	0.726F	Voltage error compensation table of voltage.
General > Voltage error compensation table of voltage 4	Manual Entry	0.846F	Voltage error compensation table of voltage.
General > Voltage error compensation table of voltage 5	Manual Entry	0.874F	Voltage error compensation table of voltage.

General > Voltage error compensation table of current 1	Manual Entry	0.047F	Voltage error compensation table of current.
General > Voltage error compensation table of current 2	Manual Entry	0.082F	Voltage error compensation table of current.
General > Voltage error compensation table of current 3	Manual Entry	0.161F	Voltage error compensation table of current.
General > Voltage error compensation table of current 4	Manual Entry	0.407F	Voltage error compensation table of current.
General > Voltage error compensation table of current 5	Manual Entry	0.862F	Voltage error compensation table of current.
Interrupts > Callback	Name must be a valid C symbol	NULL	A user callback function. If this callback function is provided, it is called at A/D conversion finish interrupt.
Design Parameter > Current PI Loop Omega	Manual Entry	300.0F	Current PI Loop Omega
Design Parameter > Current PI Loop Zeta	Manual Entry	1.0F	Current PI Loop Zeta
Motor Parameter > Pole Pair	Manual Entry	2	Pole Pair
Motor Parameter > Resistance[ohm]	Manual Entry	8.5F	Resistance
Motor Parameter > Inductance of d-axis[H]	Manual Entry	0.0045F	Inductance of d-axis
Motor Parameter > Inductance of q-axis[H]	Manual Entry	0.0045F	Inductance of q-axis
Motor Parameter > Inertia[kgm^2]	Manual Entry	0.02159F	Inertia
Motor Parameter > Nominal Current[Arms]	Manual Entry	0.0000028F	Nominal Current

### Clock Configuration

This module doesn't depend on clock setting, because this module is a simple calculation process.

### Pin Configuration

This module does not use I/O pins.

## Usage Notes

### Limitations

- Set the Period of Current Control with none-negative value.
- Set the Reference Voltage with none-negative value.

## Examples

### Basic Example

This is a basic example of minimal use of the Motor Current in an application.

```
void motor_current_basic_example (void)
{
    motor_current_input_current_t temp_input_current;
    motor_current_input_voltage_t temp_input_voltage;
    motor_current_get_voltage_t temp_get_voltage;
    fsp_err_t err = FSP_SUCCESS;
    /* Initializes the module. */
    err = RM_MOTOR_CURRENT_Open(g_test_motor_current.p_ctrl,
g_test_motor_current.p_cfg);
    handle_error(err);
    /* Basically run this module at A/D conversion finish interrupt.
    * This implementation is an example. */
    // while (true)
    {
        /* Application work here. */
        /* Set current reference before get phase voltage */
        (void) RM_MOTOR_CURRENT_CurrentReferenceSet(g_test_motor_current.p_ctrl, 1.0F,
1.0F);
        /* Set speed and phase data before get phase voltage */
        (void) RM_MOTOR_CURRENT_SpeedPhaseSet(g_test_motor_current.p_ctrl, 104.72F,
1.0F);

        temp_input_current.iu    = 1.0F;
        temp_input_current.iv    = 1.0F;
        temp_input_current.iw    = 1.0F;
        temp_input_voltage.vdc   = 24.0F;
    }
}
```



```
temp_input_voltage.va_max = 24.0F;
/* Set electric current and voltage before get phase voltage */
(void) RM_MOTOR_CURRENT_CurrentSet(g_test_motor_current.p_ctrl,
temp_input_current, temp_input_voltage);
/* Activate the process. */
(void) RM_MOTOR_CURRENT_Run(g_test_motor_current.p_ctrl);
/* Get d/q-axis current*/
(void) RM_MOTOR_CURRENT_CurrentGet(g_test_motor_current.p_ctrl, &f_get_id,
&f_get_iq);
/* Get the flag of PI control */
(void) RM_MOTOR_CURRENT_PhaseVolageGet(g_test_motor_current.p_ctrl,
&temp_get_voltage);
/* Get Output Parameter */
(void) RM_MOTOR_CURRENT_ParameterGet(g_test_motor_current.p_ctrl,
&test_output);
(void) RM_MOTOR_CURRENT_ParameterUpdate(g_test_motor_current.p_ctrl,
g_test_motor_current.p_cfg);
}
/* Reset the process. */
(void) RM_MOTOR_CURRENT_Reset(g_test_motor_current.p_ctrl);
/* Close the module. */
(void) RM_MOTOR_CURRENT_Close(g_test_motor_current.p_ctrl);
}
```

## Function Documentation

---

◆ **RM\_MOTOR\_CURRENT\_Open()**

```
fsp_err_t RM_MOTOR_CURRENT_Open ( motor_current_ctrl_t *const p_ctrl, motor_current_cfg_t
const *const p_cfg )
```

Opens and configures the Motor Current Module. Implements `motor_current_api_t::open`.

**Return values**

FSP_SUCCESS	Motor Current successfully configured.
FSP_ERR_ASSERTION	Null pointer, or one or more configuration options is invalid.
FSP_ERR_ALREADY_OPEN	Module is already open. This module can only be opened once.
FSP_ERR_INVALID_ARGUMENT	Configuration parameter error.

◆ **RM\_MOTOR\_CURRENT\_Close()**

```
fsp_err_t RM_MOTOR_CURRENT_Close ( motor_current_ctrl_t *const p_ctrl)
```

Disables specified Motor Current Module. Implements `motor_current_api_t::close`.

**Return values**

FSP_SUCCESS	Successfully closed.
FSP_ERR_ASSERTION	Null pointer.
FSP_ERR_NOT_OPEN	Module is not open.

◆ **RM\_MOTOR\_CURRENT\_Reset()**

```
fsp_err_t RM_MOTOR_CURRENT_Reset ( motor_current_ctrl_t *const p_ctrl)
```

Reset variables of Motor Current Module. Implements `motor_current_api_t::reset`.

**Return values**

FSP_SUCCESS	Successfully reset.
FSP_ERR_ASSERTION	Null pointer.
FSP_ERR_NOT_OPEN	Module is not open.

◆ **RM\_MOTOR\_CURRENT\_Run()**

```
fsp_err_t RM_MOTOR_CURRENT_Run ( motor_current_ctrl_t *const p_ctrl)
```

Run(Start) the Current Control. Implements `motor_current_api_t::run`.

**Return values**

FSP_SUCCESS	Successfully reset.
FSP_ERR_ASSERTION	Null pointer.
FSP_ERR_NOT_OPEN	Module is not open.

◆ **RM\_MOTOR\_CURRENT\_ParameterSet()**

```
fsp_err_t RM_MOTOR_CURRENT_ParameterSet ( motor_current_ctrl_t *const p_ctrl,
motor_current_input_t const *const p_st_input )
```

Set (Input) Parameter Data. Implements `motor_current_api_t::parameterSet`.

**Return values**

FSP_SUCCESS	Successfully data is set.
FSP_ERR_ASSERTION	Null pointer.
FSP_ERR_NOT_OPEN	Module is not open.
FSP_ERR_INVALID_ARGUMENT	Input argument error.

◆ **RM\_MOTOR\_CURRENT\_CurrentReferenceSet()**

```
fsp_err_t RM_MOTOR_CURRENT_CurrentReferenceSet ( motor_current_ctrl_t *const p_ctrl, float
const id_reference, float const iq_reference )
```

Set Current Reference Data. Implements `motor_current_api_t::currentReferenceSet`.

**Return values**

FSP_SUCCESS	Successfully data is set.
FSP_ERR_ASSERTION	Null pointer.
FSP_ERR_NOT_OPEN	Module is not open.

◆ **RM\_MOTOR\_CURRENT\_SpeedPhaseSet()**

```
fsp_err_t RM_MOTOR_CURRENT_SpeedPhaseSet ( motor_current_ctrl_t *const p_ctrl, float const speed, float const phase )
```

Set Current Speed & rotor phase Data. Implements [motor\\_current\\_api\\_t::speedPhaseSet](#).

**Return values**

FSP_SUCCESS	Successfully data is set.
FSP_ERR_ASSERTION	Null pointer.
FSP_ERR_NOT_OPEN	Module is not open.

◆ **RM\_MOTOR\_CURRENT\_CurrentSet()**

```
fsp_err_t RM_MOTOR_CURRENT_CurrentSet ( motor_current_ctrl_t *const p_ctrl, motor_current_input_current_t const *const p_st_current, motor_current_input_voltage_t const *const p_st_voltage )
```

Set d/q-axis Current & Voltage Data. Implements [motor\\_current\\_api\\_t::currentSet](#).

**Return values**

FSP_SUCCESS	Successfully data is set.
FSP_ERR_ASSERTION	Null pointer.
FSP_ERR_NOT_OPEN	Module is not open.
FSP_ERR_INVALID_ARGUMENT	Input parameter error.

◆ **RM\_MOTOR\_CURRENT\_ParameterGet()**

```
fsp_err_t RM_MOTOR_CURRENT_ParameterGet ( motor_current_ctrl_t *const p_ctrl, motor_current_output_t *const p_st_output )
```

Get Output Parameters. Implements [motor\\_current\\_api\\_t::parameterGet](#).

**Return values**

FSP_SUCCESS	Successfully data is set.
FSP_ERR_ASSERTION	Null pointer.
FSP_ERR_NOT_OPEN	Module is not open.
FSP_ERR_INVALID_ARGUMENT	Input parameter error.

◆ **RM\_MOTOR\_CURRENT\_CurrentGet()**

```
fsp_err_t RM_MOTOR_CURRENT_CurrentGet ( motor_current_ctrl_t *const p_ctrl, float *const p_id,
float *const p_iq )
```

Get d/q-axis Current. Implements [motor\\_current\\_api\\_t::currentGet](#).

**Return values**

FSP_SUCCESS	Successfully data is set.
FSP_ERR_ASSERTION	Null pointer.
FSP_ERR_NOT_OPEN	Module is not open.
FSP_ERR_INVALID_ARGUMENT	Input parameter error.

◆ **RM\_MOTOR\_CURRENT\_PhaseVoltageGet()**

```
fsp_err_t RM_MOTOR_CURRENT_PhaseVoltageGet ( motor_current_ctrl_t *const p_ctrl,
motor_current_get_voltage_t *const p_voltage )
```

Gets the set phase voltage. Implements [motor\\_current\\_api\\_t::phaseVoltageGet](#).

**Return values**

FSP_SUCCESS	Successfully data culated.
FSP_ERR_ASSERTION	Null pointer.
FSP_ERR_NOT_OPEN	Module is not open.
FSP_ERR_INVALID_ARGUMENT	Input parameter error.

◆ **RM\_MOTOR\_CURRENT\_ParameterUpdate()**

```
fsp_err_t RM_MOTOR_CURRENT_ParameterUpdate ( motor_current_ctrl_t *const p_ctrl,
motor_current_cfg_t const *const p_cfg )
```

Update the parameters of Current Control. Implements [motor\\_current\\_api\\_t::parameterUpdate](#).

**Return values**

FSP_SUCCESS	Successfully data was updated.
FSP_ERR_ASSERTION	Null pointer.
FSP_ERR_NOT_OPEN	Module is not open.

### ◆ RM\_MOTOR\_CURRENT\_VersionGet()

`fsp_err_t RM_MOTOR_CURRENT_VersionGet ( fsp_version_t *const p_version)`

Return Motor Speed Control module version. Implements `motor_current_api_t::versionGet`.

#### Return values

FSP_SUCCESS	Version information successfully read.
FSP_ERR_ASSERTION	Null pointer passed as a parameter

## 4.2.68 Motor Driver (rm\_motor\_driver)

### Modules

#### Functions

`fsp_err_t RM_MOTOR_DRIVER_Open (motor_driver_ctrl_t *const p_ctrl, motor_driver_cfg_t const *const p_cfg)`

Opens and configures the Motor Driver module. Implements `motor_driver_api_t::open`. [More...](#)

`fsp_err_t RM_MOTOR_DRIVER_Close (motor_driver_ctrl_t *const p_ctrl)`

Disables specified Motor Driver Module. Implements `motor_driver_api_t::close`. [More...](#)

`fsp_err_t RM_MOTOR_DRIVER_Reset (motor_driver_ctrl_t *const p_ctrl)`

Reset variables of Motor Driver Module. Implements `motor_driver_api_t::reset`. [More...](#)

`fsp_err_t RM_MOTOR_DRIVER_PhaseVoltageSet (motor_driver_ctrl_t *const p_ctrl, float const u_voltage, float const v_voltage, float const w_voltage)`

Set Phase Voltage Data to calculate PWM duty. Implements `motor_driver_api_t::phaseVoltageSet`. [More...](#)

`fsp_err_t RM_MOTOR_DRIVER_CurrentGet (motor_driver_ctrl_t *const p_ctrl, motor_driver_current_get_t *const p_current_get)`

Get calculated phase Current, Vdc & Va\_max data. Implements `motor_driver_api_t::currentGet`. [More...](#)

`fsp_err_t RM_MOTOR_DRIVER_FlagCurrentOffsetGet (motor_driver_ctrl_t *const p_ctrl, uint8_t *const p_flag_offset)`

Get the flag of finish current offset detection. Implements `motor_driver_api_t::flagCurrentOffsetGet`. [More...](#)

`fsp_err_t RM_MOTOR_DRIVER_CurrentOffsetRestart (motor_driver_ctrl_t *const p_ctrl)`

Restart the current offset detection. Implements `motor_driver_api_t::currentOffsetRestart`. [More...](#)

`fsp_err_t RM_MOTOR_DRIVER_ParameterUpdate (motor_driver_ctrl_t *const p_ctrl, motor_driver_cfg_t const *const p_cfg)`

Update the parameters of Driver Module. Implements `motor_driver_api_t::parameterUpdate`. [More...](#)

`fsp_err_t RM_MOTOR_DRIVER_VersionGet (fsp_version_t *const p_version)`

## Detailed Description

Calculation process for the motor control on RA MCUs. This module implements the [MOTOR\\_DRIVER Interface](#).

## Overview

The motor driver module is used to translate phase voltage to PWM duty and output PWM, and detect phase current and main line voltage. This module should be called cyclically at included A/D Conversion finish interrupt.

# BLOCK DIAGRAM OF SENSORLESS VECTOR CONTROL

It is a block diagram of sensorless vector control. This shows the correspondence between modules and functional blocks.

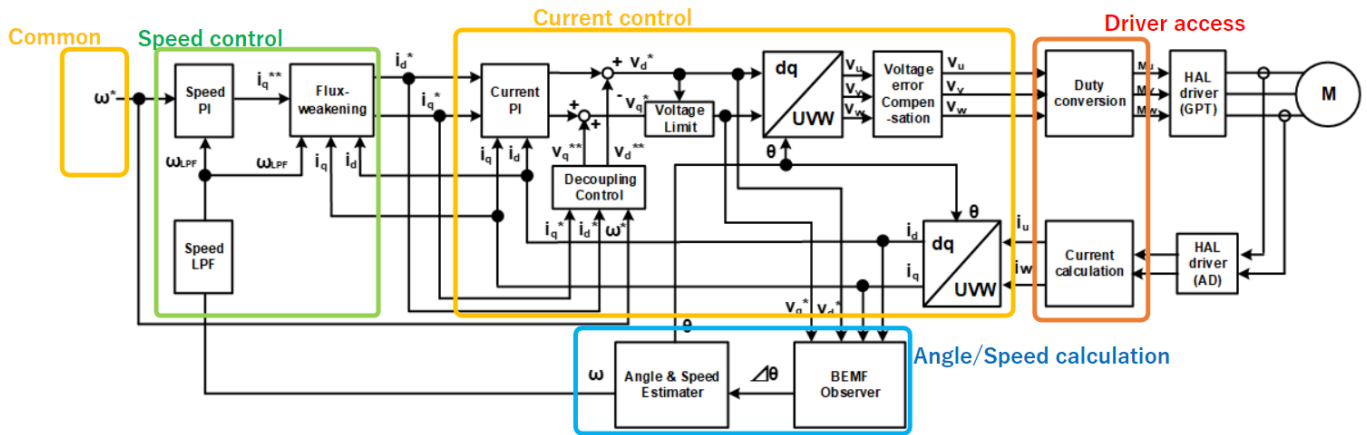


Figure 186: Image of Driver Module (red block)

## Features

The Motor Driver Module has below features.

- Calculate each phase(U/V/W) PWM duty according to reference and output PWM.
- Detect each phase current and main line voltage.
- Detect and correct A/D offset at phase current channel

## Configuration

### Build Time Configurations for rm\_motor\_driver

The following build time configurations are defined in fsp\_cfg/rm\_motor\_driver\_cfg.h:

Configuration	Options	Default	Description
Parameter Checking	<ul style="list-style-type: none"> <li>• Default (BSP)</li> <li>• Enabled</li> <li>• Disabled</li> </ul>	Default (BSP)	If selected code for parameter checking is included in the build.

### Configurations for Middleware > Motor > ADC and PWM Modulation Driver on rm\_motor\_driver

This module can be added to the Stacks tab via New Stack > Middleware > Motor > ADC and PWM Modulation Driver on rm\_motor\_driver .

Configuration	Options	Default	Description
General > Name	Name must be a valid C symbol	g_motor_driver0	Module name.
General > PWM Timer Frequency[MHz]	Manual Entry	120	GPT PWM Timer Frequency



General > PWM Carrier Frequency[Microseconds]	Manual Entry	20	GPT PWM Carrier Frequency
General > Dead Time[Raw Counts]	Manual Entry	240	GPT PWM Dead Time
General > Current Range[A]	Manual Entry	20.0F	Current Range to measure(Maximum input current)
General > Voltage Range[V]	Manual Entry	111.0F	Voltage Range to measure(Maximum input Main Line Voltage)
General > Counts for current offset measurement	Manual Entry	500	How many times to measure current offset
General > A/D conversion channel for U Phase current	Manual Entry	0	Specify the A/D channel for U Phase current
General > A/D conversion channel for W Phase current	Manual Entry	2	Specify the A/D channel for W Phase current
General > A/D conversion channel for Main Line Voltage	Manual Entry	5	Specify the A/D channel for Main Line Voltage
General > GTIOCA Stop Level	<ul style="list-style-type: none"> <li>• Pin Level Low</li> <li>• Pin Level High</li> </ul>	Pin Level Low	Select the behavior of the output pin when the timer is stopped.
General > GTIOCB Stop Level	<ul style="list-style-type: none"> <li>• Pin Level Low</li> <li>• Pin Level High</li> </ul>	Pin Level Low	Select the behavior of the output pin when the timer is stopped.
Modulation > Maximum Duty	Manual Entry	0.9375F	Maximum Duty of PWM
Interrupts > Callback	Name must be a valid C symbol	NULL	A user callback function. If this callback function is provided, it is called at A/D conversion finish interrupt.

## Clock Configuration

Set used clock with included GPT timer.

## Pin Configuration

Depend on included GPT Three Phase Module and ADC Module.

## Usage Notes

### Limitations

Basically no limitation exists.

## Examples

### Basic Example

This is a basic example of minimal use of the Motor Driver in an application.

```
void motor_driver_basic_example (void)
{
    fsp_err_t err = FSP_SUCCESS;

    /* Initializes the module. */
    err = RM_MOTOR_DRIVER_Open(&g_motor_driver0.p_ctrl, &g_motor_driver0.p_cfg);
    handle_error(err);

    /* Basically run this module at cyclic interrupt (e.g. included GPT PWM Carrier
    interrupt).

    * This implementation is an example. */
    // while (true)
    {
        /* Application work here. */
        /* Get electric current, main line voltage and maximum voltage component */
        (void) RM_MOTOR_DRIVER_CurrentGet(&g_motor_driver0.p_ctrl, &f_get_iu,
        &f_get_iw, &f_get_vdc, &f_get_va_max);

        /* Get the flag of A/D converted current offset */
        (void) RM_MOTOR_DRIVER_FlagCurrentOffsetGet(&g_motor_driver0.p_ctrl,
        &ul_get_flg_offset);

        // Perform current control process here

        /* Set phase voltage */
        (void) RM_MOTOR_DRIVER_PhaseVoltageSet(&g_motor_driver0.p_ctrl, 1.0F, 1.0F,
        1.0F);

        (void) RM_MOTOR_DRIVER_ParameterUpdate(&g_motor_driver0.p_ctrl,
        &g_motor_driver0.p_cfg);
    }

    (void) RM_MOTOR_DRIVER_Reset(&g_motor_driver0.p_ctrl);
}
```

```
//

(void) RM_MOTOR_DRIVER_Close(&g_motor_driver0.p_ctrl);
}
```

## Function Documentation

### ◆ RM\_MOTOR\_DRIVER\_Open()

`fsp_err_t RM_MOTOR_DRIVER_Open ( motor_driver_ctrl_t *const p_ctrl, motor_driver_cfg_t const *const p_cfg )`

Opens and configures the Motor Driver module. Implements `motor_driver_api_t::open`.

#### Return values

FSP_SUCCESS	Motor Driver successfully configured.
FSP_ERR_ASSERTION	Null pointer, or one or more configuration options is invalid.
FSP_ERR_ALREADY_OPEN	Module is already open. This module can only be opened once.

### ◆ RM\_MOTOR\_DRIVER\_Close()

`fsp_err_t RM_MOTOR_DRIVER_Close ( motor_driver_ctrl_t *const p_ctrl)`

Disables specified Motor Driver Module. Implements `motor_driver_api_t::close`.

#### Return values

FSP_SUCCESS	Successfully closed.
FSP_ERR_ASSERTION	Null pointer.
FSP_ERR_NOT_OPEN	Module is not open.

◆ **RM\_MOTOR\_DRIVER\_Reset()**

```
fsp_err_t RM_MOTOR_DRIVER_Reset ( motor_driver_ctrl_t *const p_ctrl)
```

Reset variables of Motor Driver Module. Implements `motor_driver_api_t::reset`.

**Return values**

FSP_SUCCESS	Successfully reset.
FSP_ERR_ASSERTION	Null pointer.
FSP_ERR_NOT_OPEN	Module is not open.

◆ **RM\_MOTOR\_DRIVER\_PhaseVoltageSet()**

```
fsp_err_t RM_MOTOR_DRIVER_PhaseVoltageSet ( motor_driver_ctrl_t *const p_ctrl, float const u_voltage, float const v_voltage, float const w_voltage )
```

Set Phase Voltage Data to calculate PWM duty. Implements `motor_driver_api_t::phaseVoltageSet`.

**Return values**

FSP_SUCCESS	Successfully data is set.
FSP_ERR_ASSERTION	Null pointer.
FSP_ERR_NOT_OPEN	Module is not open.

◆ **RM\_MOTOR\_DRIVER\_CurrentGet()**

```
fsp_err_t RM_MOTOR_DRIVER_CurrentGet ( motor_driver_ctrl_t *const p_ctrl, motor_driver_current_get_t *const p_current_get )
```

Get calculated phase Current, Vdc & Va\_max data. Implements `motor_driver_api_t::currentGet`.

**Return values**

FSP_SUCCESS	Successfully data is set.
FSP_ERR_ASSERTION	Null pointer.
FSP_ERR_NOT_OPEN	Module is not open.
FSP_ERR_INVALID_ARGUMENT	Input parameter error.

◆ **RM\_MOTOR\_DRIVER\_FlagCurrentOffsetGet()**

```
fsp_err_t RM_MOTOR_DRIVER_FlagCurrentOffsetGet ( motor_driver_ctrl_t *const p_ctrl, uint8_t *const p_flag_offset )
```

Get the flag of finish current offset detection. Implements `motor_driver_api_t::flagCurrentOffsetGet`.

**Return values**

FSP_SUCCESS	Successfully data is set.
FSP_ERR_ASSERTION	Null pointer.
FSP_ERR_NOT_OPEN	Module is not open.
FSP_ERR_INVALID_ARGUMENT	Input parameter error.

◆ **RM\_MOTOR\_DRIVER\_CurrentOffsetRestart()**

```
fsp_err_t RM_MOTOR_DRIVER_CurrentOffsetRestart ( motor_driver_ctrl_t *const p_ctrl)
```

Restart the current offset detection. Implements `motor_driver_api_t::currentOffsetRestart`.

**Return values**

FSP_SUCCESS	Successfully data is set.
FSP_ERR_ASSERTION	Null pointer.
FSP_ERR_NOT_OPEN	Module is not open.

◆ **RM\_MOTOR\_DRIVER\_ParameterUpdate()**

```
fsp_err_t RM_MOTOR_DRIVER_ParameterUpdate ( motor_driver_ctrl_t *const p_ctrl, motor_driver_cfg_t const *const p_cfg )
```

Update the parameters of Driver Module. Implements `motor_driver_api_t::parameterUpdate`.

**Return values**

FSP_SUCCESS	Successfully data was updated.
FSP_ERR_ASSERTION	Null pointer.
FSP_ERR_NOT_OPEN	Module is not open.

### ◆ RM\_MOTOR\_DRIVER\_VersionGet()

`fsp_err_t RM_MOTOR_DRIVER_VersionGet ( fsp_version_t *const p_version)`

Return Motor Driver Module version. Implements `motor_driver_api_t::versionGet`.

#### Return values

FSP_SUCCESS	Version information successfully read.
FSP_ERR_ASSERTION	Null pointer passed as a parameter

## 4.2.69 Motor Angle and Speed Estimation (rm\_motor\_estimate)

### Modules

#### Functions

`fsp_err_t RM_MOTOR_ESTIMATE_Open (motor_angle_ctrl_t *const p_ctrl, motor_angle_cfg_t const *const p_cfg)`  
 Opens and configures the Angle Estimation module. Implements `motor_angle_api_t::open`. [More...](#)

`fsp_err_t RM_MOTOR_ESTIMATE_Close (motor_angle_ctrl_t *const p_ctrl)`  
 Disables specified Angle Estimation module. Implements `motor_angle_api_t::close`. [More...](#)

`fsp_err_t RM_MOTOR_ESTIMATE_Reset (motor_angle_ctrl_t *const p_ctrl)`  
 Reset variables of Angle Estimation module. Implements `motor_angle_api_t::reset`. [More...](#)

`fsp_err_t RM_MOTOR_ESTIMATE_CurrentSet (motor_angle_ctrl_t *const p_ctrl, motor_angle_current_t *const p_st_current, motor_angle_voltage_reference_t *const p_st_voltage)`  
 Set d/q-axis Current Data & Voltage Reference. Implements `motor_angle_api_t::currentSet`. [More...](#)

`fsp_err_t RM_MOTOR_ESTIMATE_SpeedSet (motor_angle_ctrl_t *const p_ctrl, float const speed_ctrl, float const damp_speed)`  
 Set Speed Information. Implements `motor_angle_api_t::speedSet`. [More...](#)

`fsp_err_t RM_MOTOR_ESTIMATE_FlagPiCtrlSet (motor_angle_ctrl_t *const p_ctrl, uint32_t const flag_pi)`

Set the flag of PI Control runs. Implements `motor_angle_api_t::flagPiCtrlSet`. [More...](#)

`fsp_err_t RM_MOTOR_ESTIMATE_AngleSpeedGet (motor_angle_ctrl_t *const p_ctrl, float *const p_angle, float *const p_speed, float *const p_phase_err)`

Gets the current rotor's angle and rotation speed. Implements `motor_angle_api_t::angleSpeedGet`. [More...](#)

`fsp_err_t RM_MOTOR_ESTIMATE_EstimatedComponentGet (motor_angle_ctrl_t *const p_ctrl, float *const p_ed, float *const p_eq)`

Gets estimated d/q-axis component. Implements `motor_angle_api_t::estimatedComponentGet`. [More...](#)

`fsp_err_t RM_MOTOR_ESTIMATE_ParameterUpdate (motor_angle_ctrl_t *const p_ctrl, motor_angle_cfg_t const *const p_cfg)`

Update the parameters of Angle&Speed Estimation. Implements `motor_angle_api_t::parameterUpdate`. [More...](#)

`fsp_err_t RM_MOTOR_ESTIMATE_VersionGet (fsp_version_t *const p_version)`

## Detailed Description

Calculation process for the motor control on RA MCUs. This module implements the [MOTOR ANGLE Interface](#).

## Overview

The motor angle and speed estimation module is used to calculate rotor angle and rotational speed in an application. This module should be called cyclically after the A/D conversion of electric current of each phase in an application.

# BLOCK DIAGRAM OF SENSORLESS VECTOR CONTROL

It is a block diagram of sensorless vector control. This shows the correspondence between modules and functional blocks.

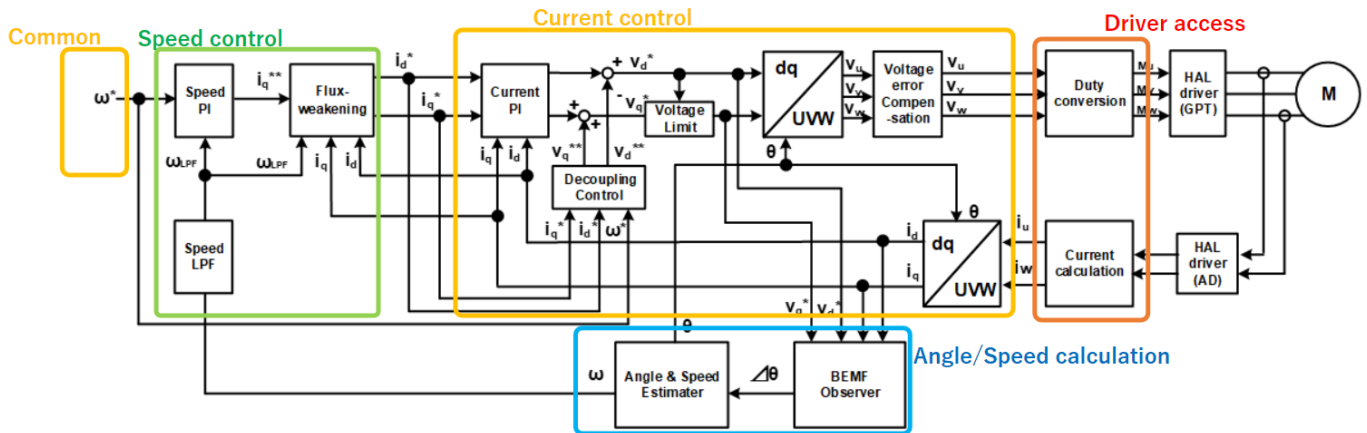


Figure 187: Image of Angle and Speed Estimation Module(blue block)

## Features

The Motor Angle and Speed Estimation Module has below features.

- Calculate rotor angle [radian].
- Calculate rotational speed [radian/second].

## Configuration

### Build Time Configurations for rm\_motor\_estimate

The following build time configurations are defined in fsp\_cfg/rm\_motor\_estimate\_cfg.h:

Configuration	Options	Default	Description
Parameter Checking	<ul style="list-style-type: none"> <li>• Default (BSP)</li> <li>• Enabled</li> <li>• Disabled</li> </ul>	Default (BSP)	If selected code for parameter checking is included in the build.

### Configurations for Middleware > Motor > Motor Angle Driver on rm\_motor\_estimate

This module can be added to the Stacks tab via New Stack > Middleware > Motor > Motor Angle Driver on rm\_motor\_estimate.

Configuration	Options	Default	Description
Motor > Number of pole pairs	Manual Entry	2	Number of pole pairs
Motor > Resistance	Manual Entry	8.5F	Resistance
Motor > D-axis inductance	Manual Entry	0.0045F	D-axis inductance



Motor > Q-axis inductance	Manual Entry	0.0045F	Q-axis inductance
Motor > Rotor inertia	Manual Entry	0.0000028F	Rotor inertia
Motor > Permanent magnetic flux	Manual Entry	0.02159F	Permanent magnetic flux
Name	Name must be a valid C symbol	g_motor_angle0	Module name.
Openloop damping	<ul style="list-style-type: none"> <li>• Disable</li> <li>• Enable</li> </ul>	Enable	Openloop damping functionally enable or disable
Natural frequency of BEMF observer	Manual Entry	1000.0F	Natural frequency of BEMF observer
Damping ratio of BEMF observer	Manual Entry	1.0F	Damping ratio of BEMF observer
Natural frequency of PLL Speed estimate loop	Manual Entry	20.0F	Natural frequency of PLL Speed estimate loop
Damping ratio of PLL Speed estimate loop	Manual Entry	1.0F	Damping ratio of PLL Speed estimate loop
Control period	Manual Entry	0.00005F	Control period

### Clock Configuration

This module doesn't depend on clock setting, because this module is a simple calculation process.

### Pin Configuration

This module does not use I/O pins.

## Usage Notes

### Limitations

Developers should be aware of the following limitations when using the Motor Angle and Speed Estimation:

## Examples

### Basic Example

This is a basic example of minimal use of the Motor Angle and Speed Estimation in an application.

```
void motor_estimate_basic_example (void)
{
    fsp_err_t          err = FSP_SUCCESS;
    motor_angle_current_t smp1_current;
```

```
motor_angle_voltage_reference_t smpl_voltage;
/* Initializes the module. */
err = RM_MOTOR_ESTIMATE_Open(&g_mtr_angle0_ctrl, &g_mtr_angle_set0_cfg);
handle_error(err);
/* Basically run this module at A/D conversion finish interrupt.
 * This implementation is an example. */
while (true)
{
/* Application work here. */
/* Set PI Control Flag before get Angle/Speed and Estimated Component */
(void) RM_MOTOR_ESTIMATE_FlagPiCtrlSet(&g_mtr_angle0_ctrl, 1U);
smpl_current.id = 1.0F;
smpl_current.iq = 1.0F;
smpl_voltage.vd = 10.0F;
smpl_voltage.vq = 10.0F;
/* Set Current and Speed data before get Angle/Speed and Estimated Component */
(void) RM_MOTOR_ESTIMATE_CurrentSet(&g_mtr_angle0_ctrl, smpl_current,
smpl_voltage);
/* Set Internal Speed Reference & damping speed data before get Angle/Speed and
Estimated Component */
(void) RM_MOTOR_ESTIMATE_SpeedSet(&g_mtr_angle0_ctrl, 104.27F, 10.0F);
/* Get Angle/Speed data */
(void) RM_MOTOR_ESTIMATE_AngleSpeedGet(&g_mtr_angle0_ctrl, &f_get_angle,
&f_get_speed, &f_get_phase_err);
/* Get Estimated Component */
(void) RM_MOTOR_ESTIMATE_EstimatedComponentGet(&g_mtr_angle0_ctrl, &f_get_ed,
&f_get_eq);
}
}
```

## Function Documentation

---

◆ **RM\_MOTOR\_ESTIMATE\_Open()**

```
fsp_err_t RM_MOTOR_ESTIMATE_Open ( motor_angle_ctrl_t *const p_ctrl, motor_angle_cfg_t const *const p_cfg )
```

Opens and configures the Angle Estimation module. Implements `motor_angle_api_t::open`.

**Return values**

FSP_SUCCESS	MTR_ANGL_EST successfully configured.
FSP_ERR_ASSERTION	Null pointer, or one or more configuration options is invalid.
FSP_ERR_ALREADY_OPEN	Module is already open. This module can only be opened once.
FSP_ERR_INVALID_ARGUMENT	Configuration parameter error.

◆ **RM\_MOTOR\_ESTIMATE\_Close()**

```
fsp_err_t RM_MOTOR_ESTIMATE_Close ( motor_angle_ctrl_t *const p_ctrl)
```

Disables specified Angle Estimation module. Implements `motor_angle_api_t::close`.

**Return values**

FSP_SUCCESS	Successfully closed.
FSP_ERR_ASSERTION	Null pointer.
FSP_ERR_NOT_OPEN	Module is not open.

◆ **RM\_MOTOR\_ESTIMATE\_Reset()**

```
fsp_err_t RM_MOTOR_ESTIMATE_Reset ( motor_angle_ctrl_t *const p_ctrl)
```

Reset variables of Angle Estimation module. Implements `motor_angle_api_t::reset`.

**Return values**

FSP_SUCCESS	Successfully closed.
FSP_ERR_ASSERTION	Null pointer.
FSP_ERR_NOT_OPEN	Module is not open.

◆ **RM\_MOTOR\_ESTIMATE\_CurrentSet()**

```
fsp_err_t RM_MOTOR_ESTIMATE_CurrentSet ( motor_angle_ctrl_t *const p_ctrl,
motor_angle_current_t *const p_st_current, motor_angle_voltage_reference_t *const p_st_voltage
)
```

Set d/q-axis Current Data & Voltage Reference. Implements `motor_angle_api_t::currentSet`.

**Return values**

FSP_SUCCESS	Successfully closed.
FSP_ERR_ASSERTION	Null pointer.
FSP_ERR_NOT_OPEN	Module is not open.

◆ **RM\_MOTOR\_ESTIMATE\_SpeedSet()**

```
fsp_err_t RM_MOTOR_ESTIMATE_SpeedSet ( motor_angle_ctrl_t *const p_ctrl, float const
speed_ctrl, float const damp_speed )
```

Set Speed Information. Implements `motor_angle_api_t::speedSet`.

**Return values**

FSP_SUCCESS	Successfully closed.
FSP_ERR_ASSERTION	Null pointer.
FSP_ERR_NOT_OPEN	Module is not open.

◆ **RM\_MOTOR\_ESTIMATE\_FlagPiCtrlSet()**

```
fsp_err_t RM_MOTOR_ESTIMATE_FlagPiCtrlSet ( motor_angle_ctrl_t *const p_ctrl, uint32_t const
flag_pi )
```

Set the flag of PI Control runs. Implements `motor_angle_api_t::flagPiCtrlSet`.

**Return values**

FSP_SUCCESS	Successfully closed.
FSP_ERR_ASSERTION	Null pointer.
FSP_ERR_NOT_OPEN	Module is not open.

◆ **RM\_MOTOR\_ESTIMATE\_AngleSpeedGet()**

```
fsp_err_t RM_MOTOR_ESTIMATE_AngleSpeedGet ( motor_angle_ctrl_t *const p_ctrl, float *const p_angle, float *const p_speed, float *const p_phase_err )
```

Gets the current rotor's angle and rotation speed. Implements [motor\\_angle\\_api\\_t::angleSpeedGet](#).

**Return values**

FSP_SUCCESS	Successfully data calculated.
FSP_ERR_ASSERTION	Null pointer.
FSP_ERR_NOT_OPEN	Module is not open.

◆ **RM\_MOTOR\_ESTIMATE\_EstimatedComponentGet()**

```
fsp_err_t RM_MOTOR_ESTIMATE_EstimatedComponentGet ( motor_angle_ctrl_t *const p_ctrl, float *const p_ed, float *const p_eq )
```

Gets estimated d/q-axis component. Implements [motor\\_angle\\_api\\_t::estimatedComponentGet](#).

**Return values**

FSP_SUCCESS	Successfully data gotten.
FSP_ERR_ASSERTION	Null pointer.
FSP_ERR_NOT_OPEN	Module is not open.

◆ **RM\_MOTOR\_ESTIMATE\_ParameterUpdate()**

```
fsp_err_t RM_MOTOR_ESTIMATE_ParameterUpdate ( motor_angle_ctrl_t *const p_ctrl, motor_angle_cfg_t const *const p_cfg )
```

Update the parameters of Angle&Speed Estimation. Implements [motor\\_angle\\_api\\_t::parameterUpdate](#).

**Return values**

FSP_SUCCESS	Successfully data is update.
FSP_ERR_ASSERTION	Null pointer.
FSP_ERR_NOT_OPEN	Module is not open.

### ◆ RM\_MOTOR\_ESTIMATE\_VersionGet()

fsp\_err\_t RM\_MOTOR\_ESTIMATE\_VersionGet ( fsp\_version\_t \*const p\_version)

Return Motor Angle Estimation Middle module version. Implements [motor\\_angle\\_api\\_t::versionGet](#).

#### Return values

FSP_SUCCESS	Version information successfully read.
FSP_ERR_ASSERTION	Null pointer passed as a parameter

## 4.2.70 Motor Speed (rm\_motor\_speed)

### Modules

#### Functions

fsp\_err\_t RM\_MOTOR\_SPEED\_Open (motor\_speed\_ctrl\_t \*const p\_ctrl,  
motor\_speed\_cfg\_t const \*const p\_cfg)

Opens and configures the Motor Speed Module. Implements [motor\\_speed\\_api\\_t::open](#). [More...](#)

fsp\_err\_t RM\_MOTOR\_SPEED\_Close (motor\_speed\_ctrl\_t \*const p\_ctrl)

Disables specified Motor Speed Module. Implements [motor\\_speed\\_api\\_t::close](#). [More...](#)

fsp\_err\_t RM\_MOTOR\_SPEED\_Reset (motor\_speed\_ctrl\_t \*const p\_ctrl)

Reset the variables of Motor Speed Module. Implements [motor\\_speed\\_api\\_t::reset](#). [More...](#)

fsp\_err\_t RM\_MOTOR\_SPEED\_Run (motor\_speed\_ctrl\_t \*const p\_ctrl)

Run(Start) the Motor Speed Control. Implements [motor\\_speed\\_api\\_t::run](#). [More...](#)

fsp\_err\_t RM\_MOTOR\_SPEED\_SpeedReferenceSet (motor\_speed\_ctrl\_t \*const  
p\_ctrl, float const speed\_reference\_rpm)

Set Speed Reference Data. Implements [motor\\_speed\\_api\\_t::speedReferenceSet](#). [More...](#)

fsp\_err\_t RM\_MOTOR\_SPEED\_ParameterSet (motor\_speed\_ctrl\_t \*const p\_ctrl,

motor\_speed\_input\_t const \*const p\_st\_input)

Set Input parameters. Implements [motor\\_speed\\_api\\_t::parameterSet](#). [More...](#)

fsp\_err\_t [RM\\_MOTOR\\_SPEED\\_SpeedControl](#) (motor\_speed\_ctrl\_t \*const p\_ctrl)

Calculates the d/q-axis current reference.(Main process of Speed Control) Implements [motor\\_speed\\_api\\_t::speedControl](#). [More...](#)

fsp\_err\_t [RM\\_MOTOR\\_SPEED\\_ParameterGet](#) (motor\_speed\_ctrl\_t \*const p\_ctrl, motor\_speed\_output\_t \*const p\_st\_output)

Get Speed Control Parameters. Implements [motor\\_speed\\_api\\_t::parameterGet](#). [More...](#)

fsp\_err\_t [RM\\_MOTOR\\_SPEED\\_ParameterUpdate](#) (motor\_speed\_ctrl\_t \*const p\_ctrl, motor\_speed\_cfg\_t const \*const p\_cfg)

Update the parameters of Speed Control Calculation. Implements [motor\\_speed\\_api\\_t::parameterUpdate](#). [More...](#)

fsp\_err\_t [RM\\_MOTOR\\_SPEED\\_VersionGet](#) (fsp\_version\_t \*const p\_version)

## Detailed Description

Calculation process for the motor control on RA MCUs. This module implements the [MOTOR SPEED Interface](#).

## Overview

The motor speed is used to control the speed of motor rotation in an application. This module should be called cyclically in an application (e.g. in cyclic timer interrupt). This module calculates d/q-axis current reference with input speed reference, current rotational speed, and d/q-axis current.

# BLOCK DIAGRAM OF SENSORLESS VECTOR CONTROL

It is a block diagram of sensorless vector control. This shows the correspondence between modules and functional blocks.

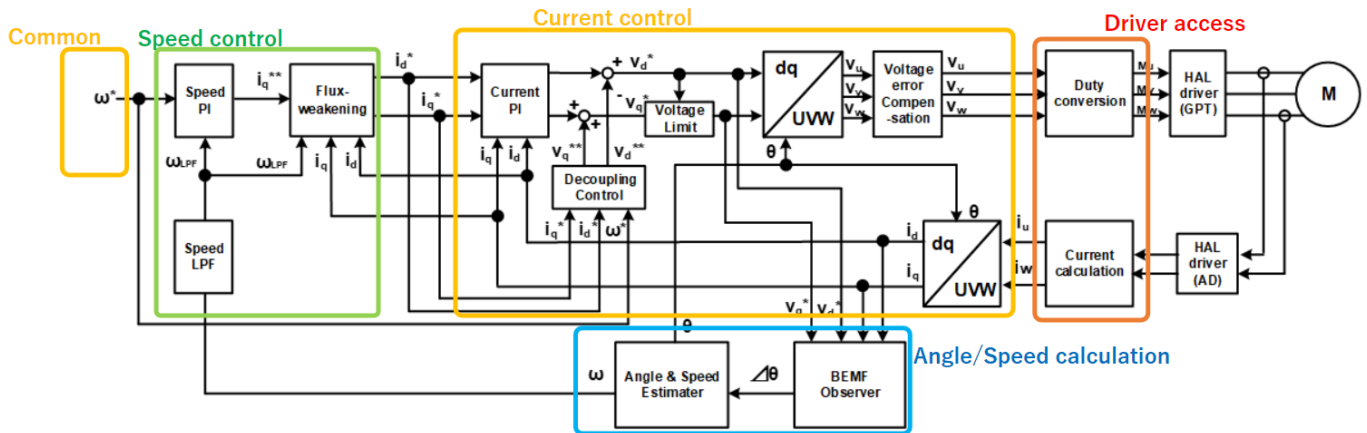


Figure 188: Image of Speed Module(green block)

## Features

The Motor Speed Module has below features.

- Calculate d/q-axis electric current reference.
- Flux weakening process at high speed rotation.
- Open Loop Damping Control at Sensorless type.
- Low pass filter of input rotational speed

## Configuration

### Build Time Configurations for rm\_motor\_speed

The following build time configurations are defined in fsp\_cfg/rm\_motor\_speed\_cfg.h:

Configuration	Options	Default	Description
Parameter Checking	<ul style="list-style-type: none"> <li>• Default (BSP)</li> <li>• Enabled</li> <li>• Disabled</li> </ul>	Default (BSP)	If selected code for parameter checking is included in the build.

### Configurations for Middleware > Motor > Motor Speed Controller on rm\_motor\_speed

This module can be added to the Stacks tab via New Stack > Middleware > Motor > Motor Speed Controller on rm\_motor\_speed.

Configuration	Options	Default	Description
General > Name	Name must be a valid C symbol	g_motor_speed0	Module name.
General > Speed Control Period[sec]	Manual Entry	0.0005F	Period of Speed Control function.



General > Step of speed climbing[rpm]	Manual Entry	0.5F	Step of speed change at start of open-loop.
General > Maximum rotational speed[rpm]	Manual Entry	2650	Maximum rotational speed (Limit speed).
General > Speed LPF Omega	Manual Entry	10.0F	Design parameter for Speed LPF.
General > Speed at Id climbing[rpm]	Manual Entry	500	From this speed d-axis current is controlled climbing.
General > Limit of q-axis current[A]	Manual Entry	0.42F	Limit of q-axis current.
General > Step of speed feedback at open-loop	Manual Entry	0.20F	Step of speed feedback at open-loop.
General > Open-Loop Damping	<ul style="list-style-type: none"> <li>• Disable</li> <li>• Enable</li> </ul>	Enable	Select enable/disable Open-Loop Damping Control.
General > Flux Weakening	<ul style="list-style-type: none"> <li>• Disable</li> <li>• Enable</li> </ul>	Enable	Select enable/disable Flux Weakening Control.
General > Torque compensation for sensorless transition	<ul style="list-style-type: none"> <li>• Disable</li> <li>• Enable</li> </ul>	Enable	Select enable/disable Torque compensation for sensorless transition.
Open-Loop > Step of d-axis current climbing	Manual Entry	0.3F	Step of d-axis current climbing
Open-Loop > Step of d-axis current descending	Manual Entry	0.3F	Step of d-axis current descending
Open-Loop > Step of q-axis current descending ratio	Manual Entry	1.0F	Step of q-axis current descending ratio
Open-Loop > Reference of q-axis current	Manual Entry	0.3F	Reference of q-axis current
Open-Loop > Threshold of speed control descending	Manual Entry	600	When rotational speed reaches this speed, d-axis current is controlled descending.
Open-Loop > Threshold of speed control climbing	Manual Entry	500	Until rotational speed reaches this speed, d-axis current is controlled climbing.
Open-Loop > Period between open-loop to	Manual Entry	0.025F	Margin time between open-loop control

BEMF[sec]				changes to BEMF PI control.
Open-Loop > Phase error[deg] to decide sensor-less switch timing	Manual Entry	10		Phase error[deg] to decide sensor-less switch timing.
Design Parameter > Speed PI Loop Omega	Manual Entry	5.0F		Speed PI Loop Omega
Design Parameter > Speed PI Loop Zeta	Manual Entry	1.0F		Speed PI Loop Zeta
Design Parameter > Estimated d-axis HPF Omega	Manual Entry	2.5F		HPF cutoff frequency for ed [Hz]
Design Parameter > Open-loop damping Zeta	Manual Entry	1.0F		Damping ratio of open-loop damping control
Design Parameter > Cutoff frequency of Phase error LPF	Manual Entry	10.0F		Cutoff frequency of Phase error LPF
Motor Parameter > Pole Pair	Manual Entry	2		Pole Pair
Motor Parameter > Resistance[ohm]	Manual Entry	8.5F		Resistance
Motor Parameter > Inductance of d-axis[H]	Manual Entry	0.0045F		Inductance of d-axis
Motor Parameter > Inductance of q-axis[H]	Manual Entry	0.0045F		Inductance of q-axis
Motor Parameter > Inertia[kgm <sup>2</sup> ]	Manual Entry	0.02159F		Inertia
Motor Parameter > Nominal Current[Arms]	Manual Entry	0.0000028F		Nominal Current
Interrupts > Callback	Name must be a valid C symbol	NULL		A user callback function. If this callback function is provided, it is called at timer interrupt.
Interrupts > Input data	Name must be a valid C symbol	NULL		Structure for Speed control Input. If you set this content, Speed Control function read these data automatically. (No need to use Set API.)
Interrupts > Output data	Name must be a valid C symbol	NULL		Structure for Speed control Output. If you

set this content, Speed Control function write need data automatically. (No need to use Get API.)

## Clock Configuration

This module doesn't depend on clock setting, because this module is a simple calculation process.

## Pin Configuration

This module does not use I/O pins.

# Usage Notes

## Limitations

- Set the Period of Speed Control with none-negative value.
- Set the limit of speed change step with none-negative value.
- Set the maximum speed with none-negative value.

# Examples

## Basic Example

This is a basic example of minimal use of the Motor Speed in an application.

```
void motor_speed_basic_example (void)
{
    fsp_err_t err = FSP_SUCCESS;

    /* Initializes the module. */
    err = RM_MOTOR_SPEED_Open(g_motor_speed0.p_ctrl, g_motor_speed0.p_cfg);
    handle_error(err);

    /* Set speed reference before get current reference */
    (void) RM_MOTOR_SPEED_SpeedReferenceSet(g_motor_speed0.p_ctrl, 104.72F);

    /* Basically run this module at cyclic interrupt (e.g. AGT timer).
     * This implementation is an example. */
    // while (true)
    {
        /* Application work here. */

        /* Set input parameter data before get current reference */
        (void) RM_MOTOR_SPEED_ParameterSet(g_motor_speed0.p_ctrl,
&g_test_speed_input);
    }
}
```

```

/* Activate Speed Process */
    (void) RM_MOTOR_SPEED_Run(g_motor_speed0.p_ctrl);
/* Perform Speed Control Process */
    (void) RM_MOTOR_SPEED_SpeedControl(g_motor_speed0.p_ctrl);
/* Get output parameters */
    (void) RM_MOTOR_SPEED_ParameterGet(g_motor_speed0.p_ctrl,
&g_test_speed_output);
//

/* Update parameters */
    (void) RM_MOTOR_SPEED_ParameterUpdate(g_motor_speed0.p_ctrl,
&g_motor_speed0.p_cfg);
}
/* Reset Speed Control */
    (void) RM_MOTOR_SPEED_Reset(g_motor_speed0.p_ctrl);
/* Close Speed Control */
    (void) RM_MOTOR_SPEED_Close(g_motor_speed0.p_ctrl);
}

```

## Function Documentation

### ◆ RM\_MOTOR\_SPEED\_Open()

`fsp_err_t RM_MOTOR_SPEED_Open ( motor_speed_ctrl_t *const p_ctrl, motor_speed_cfg_t const *const p_cfg )`

Opens and configures the Motor Speed Module. Implements `motor_speed_api_t::open`.

#### Return values

FSP_SUCCESS	Motor Speed Module successfully configured.
FSP_ERR_ASSERTION	Null pointer, or one or more configuration options is invalid.
FSP_ERR_ALREADY_OPEN	Module is already open. This module can only be opened once.
FSP_ERR_INVALID_ARGUMENT	Configuration parameter error.

◆ **RM\_MOTOR\_SPEED\_Close()**

`fsp_err_t RM_MOTOR_SPEED_Close ( motor_speed_ctrl_t *const p_ctrl)`

Disables specified Motor Speed Module. Implements `motor_speed_api_t::close`.

**Return values**

FSP_SUCCESS	Successfully closed.
FSP_ERR_ASSERTION	Null pointer.
FSP_ERR_NOT_OPEN	Module is not open.

◆ **RM\_MOTOR\_SPEED\_Reset()**

`fsp_err_t RM_MOTOR_SPEED_Reset ( motor_speed_ctrl_t *const p_ctrl)`

Reset the variables of Motor Speed Module. Implements `motor_speed_api_t::reset`.

**Return values**

FSP_SUCCESS	Successfully reset.
FSP_ERR_ASSERTION	Null pointer.
FSP_ERR_NOT_OPEN	Module is not open.

◆ **RM\_MOTOR\_SPEED\_Run()**

`fsp_err_t RM_MOTOR_SPEED_Run ( motor_speed_ctrl_t *const p_ctrl)`

Run(Start) the Motor Speed Control. Implements `motor_speed_api_t::run`.

**Return values**

FSP_SUCCESS	Successfully start.
FSP_ERR_ASSERTION	Null pointer.
FSP_ERR_NOT_OPEN	Module is not open.

◆ **RM\_MOTOR\_SPEED\_SpeedReferenceSet()**

```
fsp_err_t RM_MOTOR_SPEED_SpeedReferenceSet ( motor_speed_ctrl_t *const p_ctrl, float const speed_reference_rpm )
```

Set Speed Reference Data. Implements `motor_speed_api_t::speedReferenceSet`.

**Return values**

FSP_SUCCESS	Successfully data is set.
FSP_ERR_ASSERTION	Null pointer.
FSP_ERR_NOT_OPEN	Module is not open.

◆ **RM\_MOTOR\_SPEED\_ParameterSet()**

```
fsp_err_t RM_MOTOR_SPEED_ParameterSet ( motor_speed_ctrl_t *const p_ctrl, motor_speed_input_t const *const p_st_input )
```

Set Input parameters. Implements `motor_speed_api_t::parameterSet`.

**Return values**

FSP_SUCCESS	Successfully data is set.
FSP_ERR_ASSERTION	Null pointer.
FSP_ERR_NOT_OPEN	Module is not open.
FSP_ERR_INVALID_ARGUMENT	Output pointer is NULL.

◆ **RM\_MOTOR\_SPEED\_SpeedControl()**

```
fsp_err_t RM_MOTOR_SPEED_SpeedControl ( motor_speed_ctrl_t *const p_ctrl)
```

Calculates the d/q-axis current reference.(Main process of Speed Control) Implements `motor_speed_api_t::speedControl`.

**Return values**

FSP_SUCCESS	Successfully data culated.
FSP_ERR_ASSERTION	Null pointer.
FSP_ERR_NOT_OPEN	Module is not open.

◆ **RM\_MOTOR\_SPEED\_ParameterGet()**

```
fsp_err_t RM_MOTOR_SPEED_ParameterGet ( motor_speed_ctrl_t *const p_ctrl,
motor_speed_output_t *const p_st_output )
```

Get Speed Control Parameters. Implements [motor\\_speed\\_api\\_t::parameterGet](#).

**Return values**

FSP_SUCCESS	Successfully the flag is gotten.
FSP_ERR_ASSERTION	Null pointer.
FSP_ERR_NOT_OPEN	Module is not open.
FSP_ERR_INVALID_ARGUMENT	Output pointer is NULL.

◆ **RM\_MOTOR\_SPEED\_ParameterUpdate()**

```
fsp_err_t RM_MOTOR_SPEED_ParameterUpdate ( motor_speed_ctrl_t *const p_ctrl,
motor_speed_cfg_t const *const p_cfg )
```

Update the parameters of Speed Control Calculation. Implements [motor\\_speed\\_api\\_t::parameterUpdate](#).

**Return values**

FSP_SUCCESS	Successfully data was updated.
FSP_ERR_ASSERTION	Null pointer.
FSP_ERR_NOT_OPEN	Module is not open.
FSP_ERR_INVALID_ARGUMENT	Configuration parameter error.

◆ **RM\_MOTOR\_SPEED\_VersionGet()**

```
fsp_err_t RM_MOTOR_SPEED_VersionGet ( fsp_version_t *const p_version)
```

Return Motor Speed Control module version. Implements [motor\\_speed\\_api\\_t::versionGet](#).

**Return values**

FSP_SUCCESS	Version information successfully read.
FSP_ERR_ASSERTION	Null pointer passed as a parameter

**4.2.71 Crypto Middleware (rm\_psa\_crypto)**

## Modules

### Functions

`fsp_err_t` `RM_PSA_CRYPTOTRNG_Read` (`uint8_t *const p_rngbuf`, `uint32_t num_req_bytes`, `uint32_t *p_num_gen_bytes`)

Reads requested length of random data from the TRNG. Generate nbytes of random bytes and store them in `p_rngbuf` buffer. [More...](#)

`int` `mbedtls_platform_setup` (`mbedtls_platform_context *ctx`)

`void` `mbedtls_platform_teardown` (`mbedtls_platform_context *ctx`)

### Detailed Description

Hardware acceleration for the mbedCrypto implementation of the ARM PSA Crypto API.

## Overview

#### Note

*The PSA Crypto module does not provide any interfaces to the user. This release uses the mbed-Crypto version 3.1.0 which conforms to the PSA Crypto API 1.0 beta3 specification. Consult the ARM mbedCrypto documentation at [https://github.com/ARMmbed/mbed-crypto/blob/mbedcrypto-3.1.0/docs/getting\\_started.md](https://github.com/ARMmbed/mbed-crypto/blob/mbedcrypto-3.1.0/docs/getting_started.md) for further information.*

### Features

The PSA\_Crypto module provides hardware support for the following PSA Crypto operations

- SHA256 calculation
- SHA224 calculation
- AES
  - Keybits - 128, 256
  - Plain-Text Key Generation
  - Wrapped Key Generation
  - Encryption and Decryption with no padding and with PKCS7 padding.
  - CBC, CTR and GCM modes
  - Export and Import for Plaintext and Wrapped keys
- ECC
  - Curves:
    - SECP256R1
    - SECP256K1
    - Brainpool256R1 (Unavailable on RA6M4)
    - SECP384R1
    - Brainpool384R1 (Unavailable on RA6M4)
  - Plain-Text Key Generation (Unavailable on RA6M4)
  - Wrapped Key Generation
  - Signing and Verification
  - Export and Import for Plaintext and Wrapped keys
- RSA
  - Keybits - 2048. Verification only for 3072 and 4096 bits



- Plain-Text Key Generation (Unavailable on RA6M4)
- Wrapped Key Generation
- Signature Generation
- Verification
- Encryption and Decryption with PKCS1V15 and OAEP padding
- Export and Import for Plaintext and Wrapped keys
- Random number generation
- Persistent Key Storage

## Configuration

### Build Time Configurations for mbedCrypto

The following build time configurations are defined in arm/mbedtls/config.h:

Configuration	Options	Default	Description
Hardware Acceleration > Key Format > AES	MCU Specific Options		Select AES key formats used
Hardware Acceleration > Key Format > ECC	MCU Specific Options		Select ECC key formats used
Hardware Acceleration > Key Format > RSA	MCU Specific Options		Select RSA key formats used
Hardware Acceleration > Hash > SHA256/224	MCU Specific Options		Defines MBEDTLS_SHA256_ALT and MBEDTLS_SHA256_PROCESS_ALT.
Hardware Acceleration > Cipher > AES	MCU Specific Options		Defines MBEDTLS_AES_ALT, MBEDTLS_AES_SETKEY_ENC_ALT, MBEDTLS_AES_SETKEY_DEC_ALT, MBEDTLS_AES_ENCRYPT_ALT and MBEDTLS_AES_DECRYPT_ALT
Hardware Acceleration > Public Key Cryptography (PKC) > ECC	MCU Specific Options		Defines MBEDTLS_ECP_ALT
Hardware Acceleration > Public Key Cryptography (PKC) > ECDSA	MCU Specific Options		Defines MBEDTLS_ECDSA_SIGN_ALT and MBEDTLS_ECDSA_VERIFY_ALT
Hardware Acceleration > Public Key Cryptography (PKC) > RSA	MCU Specific Options		Defines MBEDTLS_RSA_ALT.
Hardware Acceleration > Public Key	MCU Specific Options		Enables RSA 3072 Verify.

Cryptography (PKC) >  
RSA 3072 Verify

Hardware Acceleration    MCU Specific Options  
> Public Key  
Cryptography (PKC) >  
RSA 4096 Verify

Enables RSA 4096  
Verify.

Hardware Acceleration    Enabled  
> TRNG

Enabled

Defines MBEDTLS\_ENT  
ROPY\_HARDWARE\_ALT.

Hardware Acceleration    Enabled  
> Secure Crypto  
Engine Initialization

Enabled

MBEDTLS\_PLATFORM\_S  
ETUP\_TEARDOWN\_ALT

Platform > Alternate >  
MBEDTLS\_PLATFORM\_E  
XIT\_ALT

- Define
- Undefine

Undefine

MBEDTLS\_PLATFORM\_E  
XIT\_ALT

Platform > Alternate >  
MBEDTLS\_PLATFORM\_T  
IME\_ALT

- Define
- Undefine

Undefine

MBEDTLS\_PLATFORM\_T  
IME\_ALT

Platform > Alternate >  
MBEDTLS\_PLATFORM\_F  
PRINTF\_ALT

- Define
- Undefine

Undefine

MBEDTLS\_PLATFORM\_F  
PRINTF\_ALT

Platform > Alternate >  
MBEDTLS\_PLATFORM\_P  
RINTF\_ALT

- Define
- Undefine

Undefine

MBEDTLS\_PLATFORM\_P  
RINTF\_ALT

Platform > Alternate >  
MBEDTLS\_PLATFORM\_S  
NPRINTF\_ALT

- Define
- Undefine

Undefine

MBEDTLS\_PLATFORM\_S  
NPRINTF\_ALT

Platform > Alternate >  
MBEDTLS\_PLATFORM\_V  
SNPRINTF\_ALT

- Define
- Undefine

Undefine

MBEDTLS\_PLATFORM\_V  
SNPRINTF\_ALT

Platform > Alternate >  
MBEDTLS\_PLATFORM\_N  
V\_SEED\_ALT

- Define
- Undefine

Undefine

MBEDTLS\_PLATFORM\_N  
V\_SEED\_ALT

Platform > Alternate >  
MBEDTLS\_PLATFORM\_Z  
EROIZE\_ALT

- Define
- Undefine

Undefine

MBEDTLS\_PLATFORM\_Z  
EROIZE\_ALT

Platform > Alternate >  
MBEDTLS\_PLATFORM\_G  
MTIME\_R\_ALT

- Define
- Undefine

Undefine

MBEDTLS\_PLATFORM\_G  
MTIME\_R\_ALT

Platform >  
MBEDTLS\_HAVE\_ASM

- Define
- Undefine

Undefine

MBEDTLS\_HAVE\_ASM

Platform > MBEDTLS\_N  
O\_UDBL\_DIVISION

- Define
- Undefine

Undefine

MBEDTLS\_NO\_UDBL\_DI  
VISION

Platform > MBEDTLS\_N  
O\_64BIT\_MULTIPLICATI  
ON

- Define
- Undefine

Undefine

MBEDTLS\_NO\_64BIT\_M  
ULTIPLICATION

Platform > MBEDTLS_HAVE_SSE2	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_HAVE_SSE2
Platform > MBEDTLS_HAVE_TIME	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_HAVE_TIME
Platform > MBEDTLS_H AVE_TIME_DATE	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_HAVE_TIME_ DATE
Platform > MBEDTLS_P LATFORM_MEMORY	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Define	MBEDTLS_PLATFORM_ MEMORY
Platform > MBEDTLS_P LATFORM_NO_STD_FUN CTIONS	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_PLATFORM_N O_STD_FUNCTIONS
Platform > MBEDTLS_TIMING_ALT	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_TIMING_ALT
Platform > MBEDTLS_N O_PLATFORM_ENTROPY	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Define	MBEDTLS_NO_PLATFORM ENTROPY
Platform > MBEDTLS_ENTROPY_C	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Define	MBEDTLS_ENTROPY_C
Platform > MBEDTLS_PLATFORM_C	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Define	MBEDTLS_PLATFORM_C
Platform > MBEDTLS_P LATFORM_STD_CALLOC	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_PLATFORM_S TD_CALLOC
Platform > MBEDTLS_P LATFORM_STD_CALLOC value	Manual Entry	calloc	MBEDTLS_PLATFORM_S TD_CALLOC value
Platform > MBEDTLS_P LATFORM_STD_FREE	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_PLATFORM_S TD_FREE
Platform > MBEDTLS_P LATFORM_STD_FREE value	Manual Entry	free	MBEDTLS_PLATFORM_S TD_FREE value
Platform > MBEDTLS_P LATFORM_STD_EXIT	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_PLATFORM_S TD_EXIT
Platform > MBEDTLS_P LATFORM_STD_EXIT value	Manual Entry	exit	MBEDTLS_PLATFORM_S TD_EXIT value
Platform > MBEDTLS_P LATFORM_STD_TIME	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_PLATFORM_S TD_TIME
Platform > MBEDTLS_P LATFORM_STD_TIME value	Manual Entry	time	MBEDTLS_PLATFORM_S TD_TIME value
Platform > MBEDTLS_P LATFORM_STD_FPRINTF	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_PLATFORM_S TD_FPRINTF
Platform > MBEDTLS_P LATFORM_STD_FPRINTF value	Manual Entry	fprintf	MBEDTLS_PLATFORM_S TD_FPRINTF value

Platform > MBEDTLS_PLATFORM_STD_PRINTF	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_PLATFORM_STD_PRINTF
Platform > MBEDTLS_PLATFORM_STD_PRINTF value	Manual Entry	printf	MBEDTLS_PLATFORM_STD_PRINTF value
Platform > MBEDTLS_PLATFORM_STD_SNPRINTF	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_PLATFORM_STD_SNPRINTF
Platform > MBEDTLS_PLATFORM_STD_SNPRINTF value	Manual Entry	snprintf	MBEDTLS_PLATFORM_STD_SNPRINTF value
Platform > MBEDTLS_PLATFORM_STD_EXIT_SUCCESS	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_PLATFORM_STD_EXIT_SUCCESS
Platform > MBEDTLS_PLATFORM_STD_EXIT_SUCCESS value	Manual Entry	0	MBEDTLS_PLATFORM_STD_EXIT_SUCCESS value
Platform > MBEDTLS_PLATFORM_STD_EXIT_FAILURE	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_PLATFORM_STD_EXIT_FAILURE
Platform > MBEDTLS_PLATFORM_STD_EXIT_FAILURE value	Manual Entry	1	MBEDTLS_PLATFORM_STD_EXIT_FAILURE value
Platform > MBEDTLS_PLATFORM_STD_NV_SEED_READ	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_PLATFORM_STD_NV_SEED_READ
Platform > MBEDTLS_PLATFORM_STD_NV_SEED_READ value	Manual Entry	mbdtdls_platform_std_nv_seed_read	MBEDTLS_PLATFORM_STD_NV_SEED_READ value
Platform > MBEDTLS_PLATFORM_STD_NV_SEED_WRITE	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_PLATFORM_STD_NV_SEED_WRITE
Platform > MBEDTLS_PLATFORM_STD_NV_SEED_WRITE value	Manual Entry	mbdtdls_platform_std_nv_seed_write	MBEDTLS_PLATFORM_STD_NV_SEED_WRITE value
Platform > MBEDTLS_PLATFORM_STD_NV_SEED_FILE	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_PLATFORM_STD_NV_SEED_FILE
Platform > MBEDTLS_PLATFORM_STD_NV_SEED_FILE value	Manual Entry		MBEDTLS_PLATFORM_STD_NV_SEED_FILE value
Platform > MBEDTLS_PLATFORM_C_ALLOC_MACRO	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_PLATFORM_C_ALLOC_MACRO
Platform > MBEDTLS_PLATFORM_C_ALLOC value	Manual Entry	calloc	MBEDTLS_PLATFORM_C_ALLOC

LATFORM_CALLOC_MACRO value			ALLOC_MACRO value
Platform > MBEDTLS_PLATFORM_FREE_MACRO	<ul style="list-style-type: none"> <li>Define</li> <li>Undefine</li> </ul>	Undefine	MBEDTLS_PLATFORM_FREE_MACRO
Platform > MBEDTLS_PLATFORM_FREE_MACRO value	Manual Entry	free	MBEDTLS_PLATFORM_FREE_MACRO value
Platform > MBEDTLS_PLATFORM_EXIT_MACRO	<ul style="list-style-type: none"> <li>Define</li> <li>Undefine</li> </ul>	Undefine	MBEDTLS_PLATFORM_EXIT_MACRO
Platform > MBEDTLS_PLATFORM_EXIT_MACRO value	Manual Entry	exit	MBEDTLS_PLATFORM_EXIT_MACRO value
Platform > MBEDTLS_PLATFORM_TIME_MACRO	<ul style="list-style-type: none"> <li>Define</li> <li>Undefine</li> </ul>	Undefine	MBEDTLS_PLATFORM_TIME_MACRO
Platform > MBEDTLS_PLATFORM_TIME_MACRO value	Manual Entry	time	MBEDTLS_PLATFORM_TIME_MACRO value
Platform > MBEDTLS_PLATFORM_TIME_TYPE_MACRO	<ul style="list-style-type: none"> <li>Define</li> <li>Undefine</li> </ul>	Undefine	MBEDTLS_PLATFORM_TIME_TYPE_MACRO
Platform > MBEDTLS_PLATFORM_TIME_TYPE_MACRO value	Manual Entry	time_t	MBEDTLS_PLATFORM_TIME_TYPE_MACRO value
Platform > MBEDTLS_PLATFORM_FPRINTF_MACRO	<ul style="list-style-type: none"> <li>Define</li> <li>Undefine</li> </ul>	Undefine	MBEDTLS_PLATFORM_FPRINTF_MACRO
Platform > MBEDTLS_PLATFORM_FPRINTF_MACRO value	Manual Entry	fprintf	MBEDTLS_PLATFORM_FPRINTF_MACRO value
Platform > MBEDTLS_PLATFORM_PRINTF_MACRO	<ul style="list-style-type: none"> <li>Define</li> <li>Undefine</li> </ul>	Undefine	MBEDTLS_PLATFORM_PRINTF_MACRO
Platform > MBEDTLS_PLATFORM_PRINTF_MACRO value	Manual Entry	printf	MBEDTLS_PLATFORM_PRINTF_MACRO value
Platform > MBEDTLS_PLATFORM_SNPRINTF_MACRO	<ul style="list-style-type: none"> <li>Define</li> <li>Undefine</li> </ul>	Undefine	MBEDTLS_PLATFORM_SNPRINTF_MACRO
Platform > MBEDTLS_PLATFORM_SNPRINTF_MACRO value	Manual Entry	snprintf	MBEDTLS_PLATFORM_SNPRINTF_MACRO value
Platform > MBEDTLS_PLATFORM_VSNPRINTF_MACRO	<ul style="list-style-type: none"> <li>Define</li> <li>Undefine</li> </ul>	Undefine	MBEDTLS_PLATFORM_VSNPRINTF_MACRO

Platform > MBEDTLS_PLATFORM_VSNPRINTF_MACRO value	Manual Entry	vsnprintf	MBEDTLS_PLATFORM_VSNPRINTF_MACRO value
Platform > MBEDTLS_PLATFORM_NV_SEED_READ_MACRO	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_PLATFORM_NV_SEED_READ_MACRO
Platform > MBEDTLS_PLATFORM_NV_SEED_READ_MACRO value	Manual Entry	mbbedtls_platform_std_nv_seed_read	MBEDTLS_PLATFORM_NV_SEED_READ_MACRO value
Platform > MBEDTLS_PARAM_FAILED	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_PARAM_FAILED
Platform > MBEDTLS_PLATFORM_NV_SEED_WRITE_MACRO	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_PLATFORM_NV_SEED_WRITE_MACRO
Platform > MBEDTLS_PLATFORM_NV_SEED_WRITE_MACRO value	Manual Entry	mbbedtls_platform_std_nv_seed_write	MBEDTLS_PLATFORM_NV_SEED_WRITE_MACRO value
General > PSA_CRYPTO_SECURE	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	PSA_CRYPTO_SECURE
General > MBEDTLS_DEPRECATED_WARNING	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_DEPRECATED_WARNING
General > MBEDTLS_DEPRECATED_REMOVED	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Define	MBEDTLS_DEPRECATED_REMOVED
General > MBEDTLS_CHECK_PARAMS	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Define	MBEDTLS_CHECK_PARAMS
General > MBEDTLS_CHECK_PARAMS_ASSERT	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_CHECK_PARAMS_ASSERT
General > MBEDTLS_ERROR_STRERROR_DUMMY	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Define	MBEDTLS_ERROR_STRERROR_DUMMY
General > MBEDTLS_MEMORY_DEBUG	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_MEMORY_DEBUG
General > MBEDTLS_MEMORY_BACKTRACE	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_MEMORY_BACKTRACE
General > MBEDTLS_PSA_CRYPTO_SPM	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_PSA_CRYPTO_SPM
General > MBEDTLS_SELF_TEST	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_SELF_TEST
General > MBEDTLS_THREADING_ALT	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Define	MBEDTLS_THREADING_ALT
General > MBEDTLS_THREADING_PTHREAD	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_THREADING_PTHREAD
General > MBEDTLS_USE_PSA_CRYPTO	Undefine	Undefine	MBEDTLS_USE_PSA_CRYPTO

General > MBEDTLS_VERSION_FEATURES	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Define	MBEDTLS_VERSION_FEATURES
General > MBEDTLS_ERROR_C	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Define	MBEDTLS_ERROR_C
General > MBEDTLS_MEMORY_BUFFER_ALLOC_C	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_MEMORY_BUFFER_ALLOC_C
General > MBEDTLS_PSA_CRYPTOA_C	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Define	MBEDTLS_PSA_CRYPTOA_C
General > MBEDTLS_PSA_CRYPTOA_SE_C	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_PSA_CRYPTOA_SE_C
General > MBEDTLS_THREADING_C	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Define	MBEDTLS_THREADING_C
General > MBEDTLS_TIMING_C	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_TIMING_C
General > MBEDTLS_VERSION_C	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Define	MBEDTLS_VERSION_C
General > MBEDTLS_MEMORY_ALIGN_MULTIPLE	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_MEMORY_ALIGN_MULTIPLE
General > MBEDTLS_MEMORY_ALIGN_MULTIPLE value	Manual Entry	4	MBEDTLS_MEMORY_ALIGN_MULTIPLE value
Cipher > Alternate > MBEDTLS_ARC4_ALT	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_ARC4_ALT
Cipher > Alternate > MBEDTLS_ARIA_ALT	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_ARIA_ALT
Cipher > Alternate > MBEDTLS_BLOWFISH_ALT	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_BLOWFISH_ALT
Cipher > Alternate > MBEDTLS_CAMELLIA_ALT	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_CAMELLIA_ALT
Cipher > Alternate > MBEDTLS_CCM_ALT	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_CCM_ALT
Cipher > Alternate > MBEDTLS_CHACHA20_ALT	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_CHACHA20_ALT
Cipher > Alternate > MBEDTLS_CHACHAPOLY_ALT	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_CHACHAPOLY_ALT
Cipher > Alternate > MBEDTLS_CMAC_ALT	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_CMAC_ALT
Cipher > Alternate > MBEDTLS_DES_ALT	<ul style="list-style-type: none"> <li>• Define</li> </ul>	Undefine	MBEDTLS_DES_ALT

MBEDTLS_DES_ALT	• Undefine		
Cipher > Alternate > MBEDTLS_GCM_ALT	• Define • Undefine	Undefine	MBEDTLS_GCM_ALT
Cipher > Alternate > MBEDTLS_NIST_KW_ALT	• Define • Undefine	Undefine	MBEDTLS_NIST_KW_ALT
Cipher > Alternate > MBEDTLS_XTEA_ALT	• Define • Undefine	Undefine	MBEDTLS_XTEA_ALT
Cipher > Alternate > MBEDTLS_DES_SETKEY_ALT	• Define • Undefine	Undefine	MBEDTLS_DES_SETKEY_ALT
Cipher > Alternate > MBEDTLS_DES_CRYPT_ECB_ALT	• Define • Undefine	Undefine	MBEDTLS_DES_CRYPT_ECB_ALT
Cipher > Alternate > MBEDTLS_DES3_CRYPT_ECB_ALT	• Define • Undefine	Undefine	MBEDTLS_DES3_CRYPT_ECB_ALT
Cipher > AES > MBEDTLS_AES_ROM_TABLES	• Define • Undefine	Undefine	MBEDTLS_AES_ROM_TABLES
Cipher > AES > MBEDTLS_AES_FEWER_TABLES	• Define • Undefine	Undefine	MBEDTLS_AES_FEWER_TABLES
Cipher > MBEDTLS_CAMELLIA_SMALL_MEMORY	• Define • Undefine	Undefine	MBEDTLS_CAMELLIA_SMALL_MEMORY
Cipher > MBEDTLS_CIPHER_MODE_CBC	• Define • Undefine	Define	MBEDTLS_CIPHER_MODE_CBC
Cipher > MBEDTLS_CIPHER_MODE_CFB	• Define • Undefine	Define	MBEDTLS_CIPHER_MODE_CFB
Cipher > MBEDTLS_CIPHER_MODE_CTR	• Define • Undefine	Define	MBEDTLS_CIPHER_MODE_CTR
Cipher > MBEDTLS_CIPHER_MODE_OFB	• Define • Undefine	Undefine	MBEDTLS_CIPHER_MODE_OFB
Cipher > MBEDTLS_CIPHER_MODE_XTS	• Define • Undefine	Undefine	MBEDTLS_CIPHER_MODE_XTS
Cipher > MBEDTLS_CIPHER_NULL_CIPHER	• Define • Undefine	Undefine	MBEDTLS_CIPHER_NULL_CIPHER
Cipher > MBEDTLS_CIPHER_PADDING_PKCS7	• Define • Undefine	Define	MBEDTLS_CIPHER_PADDING_PKCS7
Cipher > MBEDTLS_CIPHER_PADDING_ONE_AND_ZEROS	• Define • Undefine	Define	MBEDTLS_CIPHER_PADDING_ONE_AND_ZEROS
Cipher > MBEDTLS_CIPHER_PADDING_ZEROS_AND_LEN	• Define • Undefine	Define	MBEDTLS_CIPHER_PADDING_ZEROS_AND_LEN



## AND\_LEN

Cipher > MBEDTLS_CIPHER_PADDING_ZEROS	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Define	MBEDTLS_CIPHER_PADDING_ZEROS
Cipher > MBEDTLS_AES_C	Define	Define	MBEDTLS_AES_C
Cipher > MBEDTLS_ARC4_C	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_ARC4_C
Cipher > MBEDTLS_BLOWFISH_C	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_BLOWFISH_C
Cipher > MBEDTLS_CAMELLIA_C	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_CAMELLIA_C
Cipher > MBEDTLS_ARIA_C	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_ARIA_C
Cipher > MBEDTLS_CCM_C	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Define	MBEDTLS_CCM_C
Cipher > MBEDTLS_CHACHA20_C	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_CHACHA20_C
Cipher > MBEDTLS_CHACHAPOLY_C	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_CHACHAPOLY_C
Cipher > MBEDTLS_CIPHER_C	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Define	MBEDTLS_CIPHER_C
Cipher > MBEDTLS_DES_C	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_DES_C
Cipher > MBEDTLS_GCM_C	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Define	MBEDTLS_GCM_C
Cipher > MBEDTLS_NIST_KW_C	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_NIST_KW_C
Cipher > MBEDTLS_XTEA_C	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_XTEA_C
Public Key Cryptography (PKC) > DHM > Alternate > MBEDTLS_DHM_ALT	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_DHM_ALT
Public Key Cryptography (PKC) > DHM > MBEDTLS_DHM_C	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_DHM_C
Public Key Cryptography (PKC) > ECC > Alternate > MBEDTLS_ECJPAKE_ALT	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_ECJPAKE_ALT
Public Key Cryptography (PKC) > MBEDTLS_ECDSA_GENKEY_ALT	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_ECDSA_GENKEY_ALT

ECC > Alternate > MBE  
DTLS\_ECDSA\_GENKEY\_  
ALT

Public Key  
Cryptography (PKC) >  
ECC > Alternate > MBE  
DTLS\_ECP\_INTERNAL\_A  
LT

- Define
- Undefine

Undefine

MBEDTLS\_ECP\_INTERN  
AL\_ALT

Public Key  
Cryptography (PKC) >  
ECC > Alternate > MBE  
DTLS\_ECP\_RANDOMIZE  
\_JAC\_ALT

- Define
- Undefine

Undefine

MBEDTLS\_ECP\_RAND  
MIZE\_JAC\_ALT

Public Key  
Cryptography (PKC) >  
ECC > Alternate > MBE  
DTLS\_ECP\_ADD\_MIXED  
\_ALT

- Define
- Undefine

Undefine

MBEDTLS\_ECP\_ADD\_M  
IXED\_ALT

Public Key  
Cryptography (PKC) >  
ECC > Alternate > MBE  
DTLS\_ECP\_DOUBLE\_JAC  
\_ALT

- Define
- Undefine

Undefine

MBEDTLS\_ECP\_DOUB  
LE\_JAC\_ALT

Public Key  
Cryptography (PKC) >  
ECC > Alternate > MBE  
DTLS\_ECP\_NORMALIZE\_  
JAC\_MANY\_ALT

- Define
- Undefine

Undefine

MBEDTLS\_ECP\_NORM  
ALIZE\_JAC\_MANY\_ALT

Public Key  
Cryptography (PKC) >  
ECC > Alternate > MBE  
DTLS\_ECP\_NORMALIZE\_  
JAC\_ALT

- Define
- Undefine

Undefine

MBEDTLS\_ECP\_NORM  
ALIZE\_JAC\_ALT

Public Key  
Cryptography (PKC) >  
ECC > Alternate > MBE  
DTLS\_ECP\_DOUBLE\_AD  
D\_MXZ\_ALT

- Define
- Undefine

Undefine

MBEDTLS\_ECP\_DOUB  
LE\_ADD\_MXZ\_ALT

Public Key  
Cryptography (PKC) >  
ECC > Alternate > MBE  
DTLS\_ECP\_RANDOMIZE  
\_MXZ\_ALT

- Define
- Undefine

Undefine

MBEDTLS\_ECP\_RAND  
MIZE\_MXZ\_ALT

Public Key  
Cryptography (PKC) >  
ECC > Alternate > MBE  
DTLS\_ECP\_NORMALIZE\_  
MXZ\_ALT

- Define
- Undefine

Undefine

MBEDTLS\_ECP\_NORM  
ALIZE\_MXZ\_ALT

Public Key

- Define

Undefine

MBEDTLS\_ECP\_DP\_SEC

Cryptography (PKC) > ECC > Curves > MBED TLS_ECP_DP_SECP192R 1_ENABLED	<ul style="list-style-type: none"> <li>• Undefine</li> </ul>		P192R1_ENABLED
Public Key Cryptography (PKC) > ECC > Curves > MBED TLS_ECP_DP_SECP224R 1_ENABLED	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_ECP_DP_SEC P224R1_ENABLED
Public Key Cryptography (PKC) > ECC > Curves > MBED TLS_ECP_DP_SECP256R 1_ENABLED	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Define	MBEDTLS_ECP_DP_SEC P256R1_ENABLED
Public Key Cryptography (PKC) > ECC > Curves > MBED TLS_ECP_DP_SECP384R 1_ENABLED	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_ECP_DP_SEC P384R1_ENABLED
Public Key Cryptography (PKC) > ECC > Curves > MBED TLS_ECP_DP_SECP521R 1_ENABLED	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_ECP_DP_SEC P521R1_ENABLED
Public Key Cryptography (PKC) > ECC > Curves > MBED TLS_ECP_DP_SECP192K 1_ENABLED	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_ECP_DP_SEC P192K1_ENABLED
Public Key Cryptography (PKC) > ECC > Curves > MBED TLS_ECP_DP_SECP224K 1_ENABLED	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_ECP_DP_SEC P224K1_ENABLED
Public Key Cryptography (PKC) > ECC > Curves > MBED TLS_ECP_DP_SECP256K 1_ENABLED	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_ECP_DP_SEC P256K1_ENABLED
Public Key Cryptography (PKC) > ECC > Curves > MBED TLS_ECP_DP_BP256R1_ ENABLED	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_ECP_DP_BP2 56R1_ENABLED
Public Key Cryptography (PKC) > ECC > Curves > MBED TLS_ECP_DP_BP384R1_ ENABLED	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_ECP_DP_BP3 84R1_ENABLED

Public Key Cryptography (PKC) > ECC > Curves > MBED TLS_ECP_DP_BP512R1_ ENABLED	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_ECP_DP_BP512R1_ENABLED
Public Key Cryptography (PKC) > ECC > Curves > MBED TLS_ECP_DP_CURVE25519_ENABLED	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_ECP_DP_CURVE25519_ENABLED
Public Key Cryptography (PKC) > ECC > Curves > MBED TLS_ECP_DP_CURVE448_ENABLED	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_ECP_DP_CURVE448_ENABLED
Public Key Cryptography (PKC) > ECC > MBEDTLS_ECDH_ _GEN_PUBLIC_ALT	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_ECDH_GEN_PUBLIC_ALT
Public Key Cryptography (PKC) > ECC > MBEDTLS_ECDH_ _COMPUTE_SHARED_ALT	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_ECDH_COMPUTE_SHARED_ALT
Public Key Cryptography (PKC) > ECC > MBEDTLS_ECP_NIST_OPTIM	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_ECP_NIST_OPTIM
Public Key Cryptography (PKC) > ECC > MBEDTLS_ECP_RESTARTABLE	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_ECP_RESTARTABLE
Public Key Cryptography (PKC) > ECC > MBEDTLS_ECDH_LEGACY_CONTEXT	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_ECDH_LEGACY_CONTEXT
Public Key Cryptography (PKC) > ECC > MBEDTLS_ECDSA_DETERMINISTIC	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_ECDSA_DETERMINISTIC
Public Key Cryptography (PKC) > ECC > MBEDTLS_PK_PARSE_EC_EXTENDED	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_PK_PARSE_EC_EXTENDED
Public Key Cryptography (PKC) > ECC > MBEDTLS_ECDH_C	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_ECDH_C

Public Key Cryptography (PKC) > ECC > MBEDTLS_ECDSA_C	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Define	MBEDTLS_ECDSA_C
Public Key Cryptography (PKC) > ECC > MBEDTLS_ECP_C	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Define	MBEDTLS_ECP_C
Public Key Cryptography (PKC) > ECC > MBEDTLS_ECJPAKE_C	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_ECJPAKE_C
Public Key Cryptography (PKC) > ECC > MBEDTLS_ECP_ MAX_BITS	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_ECP_MAX_BITS
Public Key Cryptography (PKC) > ECC > MBEDTLS_ECP_ MAX_BITS value	Manual Entry	521	MBEDTLS_ECP_MAX_BITS value
Public Key Cryptography (PKC) > ECC > MBEDTLS_ECP_ WINDOW_SIZE	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_ECP_WINDOW_SIZE
Public Key Cryptography (PKC) > ECC > MBEDTLS_ECP_ WINDOW_SIZE value	Manual Entry	6	MBEDTLS_ECP_WINDOW_SIZE value
Public Key Cryptography (PKC) > ECC > MBEDTLS_ECP_ FIXED_POINT_OPTIM	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_ECP_FIXED_POINT_OPTIM
Public Key Cryptography (PKC) > ECC > MBEDTLS_ECP_ FIXED_POINT_OPTIM value	Manual Entry	1	MBEDTLS_ECP_FIXED_POINT_OPTIM value
Public Key Cryptography (PKC) > ECC > MBEDTLS_ECDH_ VARIANT_EVEREST_ENABLED	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_ECDH_VARIANT_EVEREST_ENABLED
Public Key Cryptography (PKC) > RSA > MBEDTLS_PK_RSA_ ALT_SUPPORT	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_PK_RSA_ALT_SUPPORT
Public Key Cryptography (PKC) > RSA >	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Define	MBEDTLS_RSA_NO_CRT

MBEDTLS_RSA_NO_CRT			
Public Key Cryptography (PKC) > RSA > MBEDTLS_RSA_C	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Define	MBEDTLS_RSA_C
Public Key Cryptography (PKC) > MBEDTLS_GENPRIME	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Define	MBEDTLS_GENPRIME
Public Key Cryptography (PKC) > MBEDTLS_PKCS1_V15	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Define	MBEDTLS_PKCS1_V15
Public Key Cryptography (PKC) > MBEDTLS_PKCS1_V21	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Define	MBEDTLS_PKCS1_V21
Public Key Cryptography (PKC) > MBEDTLS_ASN1_PARSE_C	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Define	MBEDTLS_ASN1_PARSE_C
Public Key Cryptography (PKC) > MBEDTLS_ASN1_WRITE_C	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Define	MBEDTLS_ASN1_WRITE_C
Public Key Cryptography (PKC) > MBEDTLS_BASE64_C	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Define	MBEDTLS_BASE64_C
Public Key Cryptography (PKC) > MBEDTLS_BIGNUM_C	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Define	MBEDTLS_BIGNUM_C
Public Key Cryptography (PKC) > MBEDTLS_OID_C	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Define	MBEDTLS_OID_C
Public Key Cryptography (PKC) > MBEDTLS_PEM_PARSE_C	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Define	MBEDTLS_PEM_PARSE_C
Public Key Cryptography (PKC) > MBEDTLS_PEM_WRITE_C	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Define	MBEDTLS_PEM_WRITE_C
Public Key Cryptography (PKC) > MBEDTLS_PK_C	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Define	MBEDTLS_PK_C
Public Key Cryptography (PKC) > MBEDTLS_PK_PARSE_C	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Define	MBEDTLS_PK_PARSE_C
Public Key Cryptography (PKC) >	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Define	MBEDTLS_PK_WRITE_C

MBEDTLS_PK_WRITE_C				
Public Key Cryptography (PKC) > MBEDTLS_PKCS5_C	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Define		MBEDTLS_PKCS5_C
Public Key Cryptography (PKC) > MBEDTLS_PKCS12_C	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Define		MBEDTLS_PKCS12_C
Public Key Cryptography (PKC) > MBEDTLS_MPI_WINDOW_SIZE	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine		MBEDTLS_MPI_WINDOW_SIZE
Public Key Cryptography (PKC) > MBEDTLS_MPI_WINDOW_SIZE value	Manual Entry	6		MBEDTLS_MPI_WINDOW_SIZE value
Public Key Cryptography (PKC) > MBEDTLS_MPI_MAX_SIZE	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine		MBEDTLS_MPI_MAX_SIZE
Public Key Cryptography (PKC) > MBEDTLS_MPI_MAX_SIZE value	Manual Entry	1024		MBEDTLS_MPI_MAX_SIZE value
Hash > Alternate > MBEDTLS_MD2_ALT	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine		MBEDTLS_MD2_ALT
Hash > Alternate > MBEDTLS_MD4_ALT	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine		MBEDTLS_MD4_ALT
Hash > Alternate > MBEDTLS_MD5_ALT	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine		MBEDTLS_MD5_ALT
Hash > Alternate > MB EDTLS_RIPEMD160_ALT	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine		MBEDTLS_RIPEMD160_ALT
Hash > Alternate > MBEDTLS_SHA1_ALT	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine		MBEDTLS_SHA1_ALT
Hash > Alternate > MBEDTLS_SHA512_ALT	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine		MBEDTLS_SHA512_ALT
Hash > Alternate > MB EDTLS_MD2_PROCESS_ALT	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine		MBEDTLS_MD2_PROCESS_ALT
Hash > Alternate > MB EDTLS_MD4_PROCESS_ALT	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine		MBEDTLS_MD4_PROCESS_ALT
Hash > Alternate > MB EDTLS_MD5_PROCESS_ALT	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine		MBEDTLS_MD5_PROCESS_ALT
Hash > Alternate > MB	<ul style="list-style-type: none"> <li>• Define</li> </ul>	Undefine		MBEDTLS_RIPEMD160_

EDTLS_RIPEMD160_PROCESS_ALT	<ul style="list-style-type: none"> <li>• Undefine</li> </ul>		PROCESS_ALT
Hash > Alternate > MBEDTLS_SHA1_PROCESS_ALT	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_SHA1_PROCESS_ALT
Hash > Alternate > MBEDTLS_SHA512_PROCESS_ALT	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_SHA512_PROCESS_ALT
Hash > MBEDTLS_SHA256_SMALLER	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_SHA256_SMALLER
Hash > MBEDTLS_SHA512_SMALLER	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_SHA512_SMALLER
Hash > MBEDTLS_SHA512_NO_SHA384	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_SHA512_NO_SHA384
Hash > MBEDTLS_MD_C	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Define	MBEDTLS_MD_C
Hash > MBEDTLS_MD2_C	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_MD2_C
Hash > MBEDTLS_MD4_C	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_MD4_C
Hash > MBEDTLS_MD5_C	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Define	MBEDTLS_MD5_C
Hash > MBEDTLS_RIPEMD160_C	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Define	MBEDTLS_RIPEMD160_C
Hash > MBEDTLS_SHA1_C	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Define	MBEDTLS_SHA1_C
Hash > MBEDTLS_SHA256_C	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Define	MBEDTLS_SHA256_C
Hash > MBEDTLS_SHA512_C	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_SHA512_C
Message Authentication Code (MAC) > Alternate > MBEDTLS_POLY1305_ALT	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_POLY1305_ALT
Message Authentication Code (MAC) > MBEDTLS_CMAC_C	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_CMAC_C
Message Authentication Code (MAC) > MBEDTLS_HKDF_C	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Define	MBEDTLS_HKDF_C
Message > MBEDTLS_HMAC_DRBG	<ul style="list-style-type: none"> <li>• Define</li> </ul>	Undefine	MBEDTLS_HMAC_DRBG



Authentication Code (MAC) > MBEDTLS_HMAC_DRBG_C	<ul style="list-style-type: none"> <li>• Undefine</li> </ul>		_C
Message Authentication Code (MAC) > MBEDTLS_POLY1305_C	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_POLY1305_C
RNG > MBEDTLS_TEST_NULL_ENTROPY	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_TEST_NULL_ENTROPY
RNG > MBEDTLS_NO_DEFAULT_ENTROPY_SOURCES	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_NO_DEFAULT_ENTROPY_SOURCES
RNG > MBEDTLS_ENTROPY_FORCE_SHA256	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_ENTROPY_FORCE_SHA256
RNG > MBEDTLS_ENTROPY_NV_SEED	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_ENTROPY_NV_SEED
RNG > MBEDTLS_PSA_INJECT_ENTROPY	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_PSA_INJECT_ENTROPY
RNG > MBEDTLS_CTR_DRBG_C	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Define	MBEDTLS_CTR_DRBG_C
RNG > MBEDTLS_CTR_DRBG_C_ALT	Define	Define	MBEDTLS_CTR_DRBG_C_ALT
RNG > MBEDTLS_HAVEGE_C	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_HAVEGE_C
RNG > MBEDTLS_CTR_DRBG_ENTROPY_LEN	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	RNG MBEDTLS_CTR_DRBG_ENTROPY_LEN
RNG > MBEDTLS_CTR_DRBG_ENTROPY_LEN value	Manual Entry	48	RNG value MBEDTLS_CTR_DRBG_ENTROPY_LEN
RNG > MBEDTLS_CTR_DRBG_RESEED_INTERVAL	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	RNG MBEDTLS_CTR_DRBG_RESEED_INTERVAL
RNG > MBEDTLS_CTR_DRBG_RESEED_INTERVAL value	Manual Entry	10000	RNG value MBEDTLS_CTR_DRBG_RESEED_INTERVAL
RNG > MBEDTLS_CTR_DRBG_MAX_INPUT	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_CTR_DRBG_MAX_INPUT
RNG > MBEDTLS_CTR_DRBG_MAX_INPUT value	Manual Entry	256	MBEDTLS_CTR_DRBG_MAX_INPUT value
RNG > MBEDTLS_CTR_DRBG_MAX_REQUEST	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_CTR_DRBG_MAX_REQUEST
RNG > MBEDTLS_CTR_DRBG_MAX_REQUEST	Manual Entry	1024	MBEDTLS_CTR_DRBG_MAX_REQUEST value

value

RNG > MBEDTLS_CTR_DRBG_MAX_SEED_INPUT	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_CTR_DRBG_MAX_SEED_INPUT
RNG > MBEDTLS_CTR_DRBG_MAX_SEED_INPUT value	Manual Entry	384	MBEDTLS_CTR_DRBG_MAX_SEED_INPUT value
RNG > MBEDTLS_CTR_DRBG_USE_128_BIT_KEY	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_CTR_DRBG_USE_128_BIT_KEY
RNG > MBEDTLS_HMAC_DRBG_RESEED_INTERVAL	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_HMAC_DRBG_RESEED_INTERVAL
RNG > MBEDTLS_HMAC_DRBG_RESEED_INTERVAL value	Manual Entry	10000	MBEDTLS_HMAC_DRBG_RESEED_INTERVAL value
RNG > MBEDTLS_HMAC_DRBG_MAX_INPUT	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_HMAC_DRBG_MAX_INPUT
RNG > MBEDTLS_HMAC_DRBG_MAX_INPUT value	Manual Entry	256	MBEDTLS_HMAC_DRBG_MAX_INPUT value
RNG > MBEDTLS_HMAC_DRBG_MAX_REQUEST	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_HMAC_DRBG_MAX_REQUEST
RNG > MBEDTLS_HMAC_DRBG_MAX_REQUEST value	Manual Entry	1024	MBEDTLS_HMAC_DRBG_MAX_REQUEST value
RNG > MBEDTLS_HMAC_DRBG_MAX_SEED_INPUT	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_HMAC_DRBG_MAX_SEED_INPUT
RNG > MBEDTLS_HMAC_DRBG_MAX_SEED_INPUT value	Manual Entry	384	MBEDTLS_HMAC_DRBG_MAX_SEED_INPUT value
RNG > MBEDTLS_ENTROPY_MAX_SOURCES	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_ENTROPY_MAX_SOURCES
RNG > MBEDTLS_ENTROPY_MAX_SOURCES value	Manual Entry	20	MBEDTLS_ENTROPY_MAX_SOURCES value
RNG > MBEDTLS_ENTROPY_MAX_GATHER	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_ENTROPY_MAX_GATHER
RNG > MBEDTLS_ENTROPY_MAX_GATHER value	Manual Entry	128	MBEDTLS_ENTROPY_MAX_GATHER value
RNG > MBEDTLS_ENTROPY_MIN_HARDWARE	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_ENTROPY_MIN_HARDWARE

RNG > MBEDTLS_ENTROPY_MIN_HARDWARE value	Manual Entry	32	MBEDTLS_ENTROPY_MIN_HARDWARE value
Storage > MBEDTLS_FS_IO	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_FS_IO
Storage > MBEDTLS_PSA_CRYPTO_KEY_FILE_ID_ENCODES_OWNER	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_PSA_CRYPTO_KEY_FILE_ID_ENCODES_OWNER
Storage > MBEDTLS_PSA_CRYPTO_STORAGE_C	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_PSA_CRYPTO_STORAGE_C
Storage > MBEDTLS_PSA_ITS_FILE_C	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_PSA_ITS_FILE_C

## SHA256 Configuration

To enable hardware acceleration for the SHA256/224 calculation, the macro `MBEDTLS_SHA256_ALT` and `MBEDTLS_SHA256_PROCESS_ALT` must be defined in the configuration file. By default SHA256 is enabled. SHA256 can be disabled, but SHA512 then needs to be enabled (software version) because the PSA implementation uses it for the entropy accumulator. This can be done using the RA Configuration editor.

## AES Configuration

To enable hardware acceleration for the AES128/256 operation, the macro `MBEDTLS_AES_SETKEY_ENC_ALT`, `MBEDTLS_AES_SETKEY_DEC_ALT`, `MBEDTLS_AES_ENCRYPT_ALT` and `MBEDTLS_AES_DECRYPT_ALT` must be defined in the configuration file. By default AES is enabled. AES cannot be disabled because the PSA implementation requires it for the CTR\_DRBG random number generator. This can be done using the RA Configuration editor.

## ECC Configuration

To enable hardware acceleration for the ECC Key Generation operation, the macro `MBEDTLS_ECP_ALT` must be defined in the configuration file. For ECDSA, the macros `MBEDTLS_ECDSA_SIGN_ALT` and `MBEDTLS_ECDSA_VERIFY_ALT` must be defined. By default ECC, ECDSA and ECDHE are enabled. To disable ECC, undefine `MBEDTLS_ECP_C`, `MBEDTLS_ECDSA_C` and `MBEDTLS_ECDH_C`. This can be done using the RA Configuration editor.

## RSA Configuration

To enable hardware acceleration for the RSA2048 operation, the macro `MBEDTLS_RSA_ALT` must be defined in the configuration file. By default RSA is enabled. To disable RSA, undefine `MBEDTLS_RSA_C`, `MBEDTLS_PK_C`, `MBEDTLS_PK_PARSE_C`, `MBEDTLS_PK_WRITE_C`. This can be done using the RA Configuration editor.

## Wrapped Key Usage

To use the Secure Crypto Engine to generate and use wrapped keys, use `PSA_KEY_LIFETIME_VOLATILE_WRAPPED` when setting the key lifetime. Wrapped keys can also be generated by using `PSA_KEY_LIFETIME_PERSISTENT_WRAPPED` to generate persistent keys as described in the next section. Setting the key's lifetime attribute using this value will cause the SCE to use wrapped key mode for all operations related to that key. The user can use the export functionality to save the wrapped keys to user ROM and import it later for usage. This mode requires that Wrapped Key functionality for the algorithm is enabled in the project configuration.

*Note*

*On the RA6M4 devices, only the RSA public key can be exported. A file system must be used to store the internally generated private key.*

## Persistent Key Storage

Persistent key storage can be enabled by defining `MBEDTLS_FS_IO`, `MBEDTLS_PSA_CRYPTOSTORAGE_C`, and `MBEDTLS_PSA_ITS_FILE_C`. The key lifetime must also be specified as either `PSA_KEY_LIFETIME_PERSISTENT` or `PSA_KEY_LIFETIME_PERSISTENT_WRAPPED`. A lower level storage module must be added in the RA Configuration editor and initialized in the code before generating persistent keys. Persistent storage supports the use of plaintext and vendor keys. Refer to the lower level storage module documentation for information on how it should be initialized. To generate a persistent key the key must be assigned a unique id prior to calling generate using the `psa_set_key_id` api.

```
if (PSA_KEY_LIFETIME_IS_PERSISTENT(lifetime))
{
/* Set the id to a positive integer. */
psa_set_key_id(&attributes, (psa_key_id_t) 5);
}
```

## Platform Configuration

To run the mbedCrypto implementation of the PSA Crypto API on the MCU, the macro `MBEDTLS_PLATFORM_SETUP_TEAR_DOWN_ALT` must be defined in the configuration file. This enables code that will initialize the SCE. Parameter checking (General|`MBEDTLS_CHECK_PARAMS`) is enabled by default. To reduce code size, disable parameter checking.

## Random Number Configuration

To run the mbedCrypto implementation of the PSA Crypto API on the MCU, the macro `MBEDTLS_ENTROPY_HARDWARE_ALT` must be defined in the configuration file. This enables using the TRNG as an entropy source. None of the other cryptographic operations (even in software only mode) will work without this feature.

# Usage Notes

## Hardware Initialization

`mbedtls_platform_setup()` must be invoked before using the PSA Crypto API to ensure that the SCE peripheral is initialized.

## Memory Usage

In general, depending on the mbedCrypto features being used a heap size of 0x1000 to 0x5000 bytes is required. The total allocated heap should be the **sum** of the heap requirements of the individual algorithms:

Algorithm	Required Heap (bytes)
-----------	-----------------------

SHA256/224	None
AES	0x200
Hardware ECC	0x400
Software ECC	0x1800
RSA	0x1500

A minimum stack of 0x1000 is required where the module is used. This is either the main stack in a bare metal application or the task stack of the task used for crypto operations.

### Limitations

- Only little endian mode is supported.

### RA6M4 Usage

The crypto capabilities on the RA6M4 are different resulting in the below usage limitations with mbedCrypto:

- The module includes **both** wrapped and plaintext keys code irrespective of whether the application requires it.
- Plaintext key generation is not supported for RSA and ECC; only wrapped keys can be generated.

### Using PSA Crypto with TrustZone

Unlike FSP drivers, PSA Crypto cannot be configured as Non-secure callable in the RA Configurator for a secure project. The reason for this is that in order to achieve the security objective of controlling access to protected keys, both the PSA Crypto code as well as the keys must be placed in the secure region. Since the PSA Crypto API requires access to the keys directly during initialization and later via a key handle, allowing non-secure code to use the API by making it Non-secure callable will require the keys to be stored in non-secure memory.

This section will provide a short explanation of how to add PSA Crypto to a secure project and have it usable by the non-secure project without exposing the keys. In this example the secure project will contain an RSA private key and the non-secure project is expected to be able to perform sign and verify operations using that key.

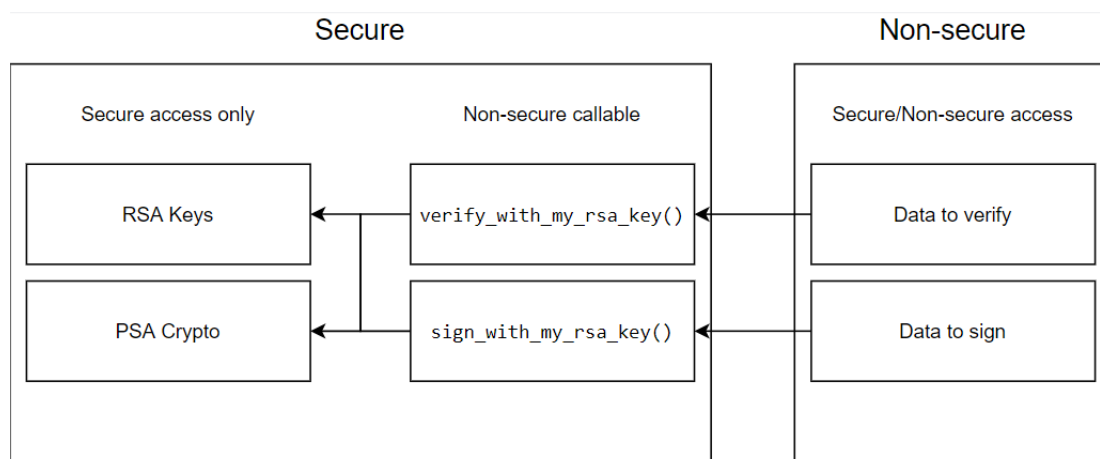


Figure 189: PSA Crypto Non-secure callable example

- Secure project
  - During secure project boot-up, `psa_crypto_init()` is called.
  - The RSA private key is programmed into secure flash either at the factory or by calling `psa_generate_key()` in persistent mode. Note that the data-flash area used by the LittleFS will have to be in the secure region if the key is generated as a persistent.
  - `psa_import_key()/psa_open_key()` are called with the resultant handle held in secure RAM.
  - The Non-secure callable section contains the following **user-defined** functions
    - `verify_with_my_rsa_key(input_signature, input_hash, verification_result)`
      - The implementation of this function in secure region will call `psa_verify_hash()` and return the result via `verification_result`.
    - `sign_with_my_rsa_key(input_hash, output_signature)`
      - The implementation of this function in secure region will call `psa_sign_hash()` and return the signature via `output_signature`.
  
- Non-secure project
  - Calls `verify_with_my_rsa_key()` to verify a signature. The implementation will use the public key that is present in the secure project.
  - Calls `sign_with_my_rsa_key()` to generate a signature. The implementation will use the private key that is present on the secure project.

For more details on how to add user-code to the Non-secure callable region refer to the "Security Design with Arm TrustZone - IP Protection (R11AN0467EU0100)" Application Note.

## Examples

### Hash Example

This is an example on calculating the SHA256 hash using the PSA Crypto API.

```
const uint8_t NIST_SHA256ShortMsgLen200[] =
{
    0x2e, 0x7e, 0xa8, 0x4d, 0xa4, 0xbc, 0x4d, 0x7c, 0xfb, 0x46, 0x3e, 0x3f, 0x2c,
0x86, 0x47, 0x05,
    0x7a, 0xff, 0xf3, 0xfb, 0xec, 0xec, 0xa1, 0xd2, 00
};
const uint8_t NIST_SHA256ShortMsgLen200_expected[] =
{
    0x76, 0xe3, 0xac, 0xbc, 0x71, 0x88, 0x36, 0xf2, 0xdf, 0x8a, 0xd2, 0xd0, 0xd2,
0xd7, 0x6f, 0x0c,
    0xfa, 0x5f, 0xea, 0x09, 0x86, 0xbe, 0x91, 0x8f, 0x10, 0xbc, 0xee, 0x73, 0x0d,
```

```
0xf4, 0x41, 0xb9
};
void psa_crypto_sha256_example (void)
{
    psa_algorithm_t      alg          = PSA_ALG_SHA_256;
    psa_hash_operation_t operation    = {0};
    size_t               expected_hash_len = PSA_HASH_SIZE(alg);
    uint8_t              actual_hash[PSA_HASH_MAX_SIZE];
    size_t               actual_hash_len;
    mbedtls_platform_context ctx = {0};
    /* Setup the platform; initialize the SCE and the TRNG */
    if (PSA_SUCCESS != mbedtls_platform_setup(&ctx))
    {
        /* Platform initialization failed */
        debugger_break();
    }
    else if (PSA_SUCCESS != psa_hash_setup(&operation, alg))
    {
        /* Hash setup failed */
        debugger_break();
    }
    else if (PSA_SUCCESS != psa_hash_update(&operation, NIST_SHA256ShortMsgLen200,
sizeof(NIST_SHA256ShortMsgLen200)))
    {
        /* Hash calculation failed */
        debugger_break();
    }
    else if (PSA_SUCCESS != psa_hash_finish(&operation, &actual_hash[0], sizeof
(actual_hash), &actual_hash_len))
    {
        /* Reading calculated hash failed */
        debugger_break();
    }
    else if (0 != memcmp(&actual_hash[0], &NIST_SHA256ShortMsgLen200_expected[0],
```

```
actual_hash_len))
{
    /* Hash compare of calculated value with expected value failed */
    debugger_break();
}
else if (0 != memcmp(&expected_hash_len, &actual_hash_len, sizeof
(expected_hash_len)))
{
    /* Hash size compare of calculated value with expected value failed */
    debugger_break();
}
else
{
    /* SHA256 calculation succeeded */
    debugger_break();
}

/* De-initialize the platform. This is currently a placeholder function which does
not do anything. */
mbedtls_platform_teardown(&ctx);
}
```

## AES Example

This is an example on using the PSA Crypto API to generate an AES256 key, encrypting and decrypting multi-block data and using PKCS7 padding.

```
static psa_status_t cipher_operation (psa_cipher_operation_t * operation,
const uint8_t      * input,
size_t             input_size,
size_t             part_size,
uint8_t            * output,
size_t             output_size,
size_t             * output_len)
{
    psa_status_t status;
```



```
size_t      bytes_to_write = 0;
size_t      bytes_written = 0;
size_t      len            = 0;
    *output_len = 0;
while (bytes_written != input_size)
    {
        bytes_to_write = (input_size - bytes_written > part_size ?
                           part_size :
                           input_size - bytes_written);
        status = psa_cipher_update(operation,
                                    input + bytes_written,
                                    bytes_to_write,
                                    output + *output_len,
                                    output_size - *output_len,
                                    &len);

        if (PSA_SUCCESS != status)
            {
                return status;
            }
        bytes_written += bytes_to_write;
        *output_len   += len;
    }
    status = psa_cipher_finish(operation, output + *output_len, output_size -
*output_len, &len);
    if (PSA_SUCCESS != status)
        {
            return status;
        }
        *output_len += len;
    return status;
}
void psa_crypto_aes256cbcmultipart_example (void)
{
    enum
```

```
{
    block_size = PSA_BLOCK_CIPHER_BLOCK_SIZE(PSA_KEY_TYPE_AES),
    key_bits   = 256,
    input_size = 100,
    part_size  = 10,
};

mbedtls_platform_context ctx          = {0};
const psa_algorithm_t    alg          = PSA_ALG_CBC_PKCS7;
psa_cipher_operation_t  operation_1 = PSA_CIPHER_OPERATION_INIT;
psa_cipher_operation_t  operation_2 = PSA_CIPHER_OPERATION_INIT;
size_t iv_len           = 0;
psa_key_handle_t        key_handle    = 0;
size_t                  encrypted_length = 0;
size_t                  decrypted_length = 0;
uint8_t                 iv[block_size] = {0};
uint8_t                 input[input_size] = {0};
uint8_t                 encrypted_data[input_size + block_size] = {0};
uint8_t                 decrypted_data[input_size + block_size] = {0};
psa_key_attributes_t    attributes = PSA_KEY_ATTRIBUTES_INIT;
/* Setup the platform; initialize the SCE */
if (PSA_SUCCESS != mbedtls_platform_setup(&ctx))
{
    /* Platform initialization failed */
    debugger_break();
}
if (PSA_SUCCESS != psa_crypto_init())
{
    /* PSA Crypto Initialization failed */
    debugger_break();
}
/* Set key attributes */
psa_set_key_usage_flags(&attributes, PSA_KEY_USAGE_ENCRYPT |
PSA_KEY_USAGE_DECRYPT);
psa_set_key_algorithm(&attributes, alg);
```

```
    psa_set_key_type(&attributes, PSA_KEY_TYPE_AES);
    psa_set_key_bits(&attributes, key_bits);
    psa_key_lifetime_t lifetime = PSA_KEY_LIFETIME_VOLATILE;
/* To use wrapped keys instead of plaintext:
 * - Use PSA_KEY_LIFETIME_VOLATILE_WRAPPED or PSA_KEY_LIFETIME_PERSISTENT_WRAPPED.
 * - To use persistent keys:
 * - The file system must be initialized prior to calling the generate/import key
functions.
 * - Refer to the littlefs example to see how to format and mount the filesystem. */
    psa_set_key_lifetime(&attributes, lifetime);
if (PSA_KEY_LIFETIME_IS_PERSISTENT(lifetime))
    {
/* Set the id to a positive integer. */
        psa_set_key_id(&attributes, (psa_key_id_t) 5);
    }
if (PSA_SUCCESS != psa_generate_random(input, sizeof(input)))
    {
/* Random number generation for input data failed */
        debugger_break();
    }
else if (PSA_SUCCESS != psa_generate_key(&attributes, &key_handle))
    {
/* Generating AES 256 key and allocating to key slot failed */
        debugger_break();
    }
else if (PSA_SUCCESS != psa_cipher_encrypt_setup(&operation_1, key_handle, alg))
    {
/* Initializing the encryption (with PKCS7 padding) operation handle failed */
        debugger_break();
    }
else if (PSA_SUCCESS != psa_cipher_generate_iv(&operation_1, iv, sizeof(iv),
&iv_len))
    {
/* Generating the random IV failed */
```

```
        debugger_break();
    }
    else if (PSA_SUCCESS !=
            cipher_operation(&operation_1, input, input_size, part_size,
encrypted_data, sizeof(encrypted_data),
                            &encrypted_length))
    {
        /* Encryption failed */
        debugger_break();
    }
    else if (PSA_SUCCESS != psa_cipher_abort(&operation_1))
    {
        /* Terminating the encryption operation failed */
        debugger_break();
    }
    else if (PSA_SUCCESS != psa_cipher_decrypt_setup(&operation_2, key_handle, alg))
    {
        /* Initializing the decryption (with PKCS7 padding) operation handle failed */
        debugger_break();
    }
    else if (PSA_SUCCESS != psa_cipher_set_iv(&operation_2, iv, sizeof(iv)))
    {
        /* Setting the IV failed */
        debugger_break();
    }
    else if (PSA_SUCCESS !=
            cipher_operation(&operation_2, encrypted_data, encrypted_length,
part_size, decrypted_data,
                            sizeof(decrypted_data), &decrypted_length))
    {
        /* Decryption failed */
        debugger_break();
    }
    else if (PSA_SUCCESS != psa_cipher_abort(&operation_2))
```

```
{
/* Terminating the decryption operation failed */
    debugger_break();
}
else if (0 != memcmp(input, decrypted_data, sizeof(input)))
{
/* Comparing the input data with decrypted data failed */
    debugger_break();
}
else if (PSA_SUCCESS != psa_destroy_key(key_handle))
{
/* Destroying the key handle failed */
    debugger_break();
}
else
{
/* All the operations succeeded */
}
/* Close the SCE */
mbedtls_platform_teardown(&ctx);
}
```

## ECC Example

This is an example on using the PSA Crypto API to generate an ECC-P256R1 key, signing and verifying data after hashing it first using SHA256.

### Note

*Unlike RSA, ECDSA does not have any padding schemes. Thus the hash argument for the ECC sign operation MUST have a size larger than or equal to the curve size; i.e. for PSA\_ECC\_CURVE\_SECP256R1 the payload size must be at least 256/8 bytes. nist.fips.186-4: " A hash function that provides a lower security strength than the security strength associated with the bit length of 'n' ordinarily should not be used, since this would reduce the security strength of the digital signature process to a level no greater than that provided by the hash function."*

```
#define ECC_256_BIT_LENGTH 256
#define ECC_256_EXPORTED_SIZE 500
uint8_t exportedECC_SECP256R1Key[ECC_256_EXPORTED_SIZE];
size_t exportedECC_SECP256R1Keylength = 0;
```

```
void psa_ecc256R1_example (void)
{
/* This example generates an ECC-P256R1 keypair, performs signing and verification
operations.

* It then exports the generated key into ASN1 DER format to a RAM array which can
then be programmed to flash.

* It then re-imports that key, and performs signing and verification operations. */
unsigned char      payload[] = "ASYMMETRIC_INPUT_FOR_SIGN.....";
unsigned char      signature1[PSA_SIGNATURE_MAX_SIZE] = {0};
unsigned char      signature2[PSA_SIGNATURE_MAX_SIZE] = {0};
size_t            signature_length1 = 0;
size_t            signature_length2 = 0;

    psa_key_attributes_t  attributes          = PSA_KEY_ATTRIBUTES_INIT;
    psa_key_attributes_t  read_attributes     = PSA_KEY_ATTRIBUTES_INIT;
    mbedtls_platform_context ctx              = {0};
    psa_key_handle_t      ecc_key_handle     = {0};
    psa_hash_operation_t  hash_operation     = {0};
    uint8_t               payload_hash[PSA_HASH_MAX_SIZE];
    size_t                payload_hash_len;
    if (PSA_SUCCESS != mbedtls_platform_setup(&ctx))
    {
        debugger_break();
    }
    if (PSA_SUCCESS != psa_crypto_init())
    {
        debugger_break();
    }
/* Set key attributes */
    psa_set_key_usage_flags(&attributes, PSA_KEY_USAGE_SIGN_HASH |
PSA_KEY_USAGE_VERIFY_HASH | PSA_KEY_USAGE_EXPORT);

    psa_set_key_algorithm(&attributes, PSA_ALG_ECDSA(PSA_ALG_SHA_256));
    psa_set_key_type(&attributes, PSA_KEY_TYPE_ECC_KEY_PAIR(PSA_ECC_CURVE_SECP_R1));
    psa_set_key_bits(&attributes, ECC_256_BIT_LENGTH);

/* To use wrapped keys instead of plaintext:
```

```
* - Use PSA_KEY_LIFETIME_VOLATILE_WRAPPED or PSA_KEY_LIFETIME_PERSISTENT_WRAPPED.
* - To use persistent keys:
* - The file system must be initialized prior to calling the generate/import key
functions.
* - Refer to the littlefs example to see how to format and mount the filesystem. */
psa_set_key_lifetime(&attributes, PSA_KEY_LIFETIME_VOLATILE);
/* Generate ECC P256R1 Key pair */
if (PSA_SUCCESS != psa_generate_key(&attributes, &ecc_key_handle))
{
    debugger_break();
}
/* Test the key information */
if (PSA_SUCCESS != psa_get_key_attributes(ecc_key_handle, &read_attributes))
{
    debugger_break();
}
/* Calculate the hash of the message */
if (PSA_SUCCESS != psa_hash_setup(&hash_operation, PSA_ALG_SHA_256))
{
    debugger_break();
}
if (PSA_SUCCESS != psa_hash_update(&hash_operation, payload, sizeof(payload)))
{
    debugger_break();
}
if (PSA_SUCCESS !=
    psa_hash_finish(&hash_operation, &payload_hash[0], sizeof(payload_hash),
&payload_hash_len))
{
    debugger_break();
}
/* Sign message using the private key
* NOTE: The hash argument (payload_hash here) MUST have a size equal to the curve
size;
```

```
* i.e. for SECP256R1 the payload size must be 256/8 bytes.
* Similarly for SECP384R1 the payload size must be 384/8 bytes.
* nist.fips.186-4: " A hash function that provides a lower security strength than
* the security strength associated with the bit length of 'n' ordinarily should not
be used, since this
* would reduce the security strength of the digital signature process to a level no
greater than that
* provided by the hash function." */
if (PSA_SUCCESS !=
    psa_sign_hash(ecc_key_handle, PSA_ALG_ECDSA(PSA_ALG_SHA_256), payload_hash,
payload_hash_len, signature1,
sizeof(signature1), &signature_length1))
{
    debugger_break();
}
/* Verify the signature1 using the public key */
if (PSA_SUCCESS !=
    psa_verify_hash(ecc_key_handle, PSA_ALG_ECDSA(PSA_ALG_SHA_256), payload_hash,
payload_hash_len, signature1,
signature_length1))
{
    debugger_break();
}
/* Export the key. The exported key can then be save to flash for later usage. */
if (PSA_SUCCESS !=
    psa_export_key(ecc_key_handle, exportedECC_SECP256R1Key, sizeof
(exportedECC_SECP256R1Key),
&exportedECC_SECP256R1Keylength))
{
    debugger_break();
}
/* Destroy the key and handle */
if (PSA_SUCCESS != psa_destroy_key(ecc_key_handle))
{
```



```
        debugger_break();
    }

    /* Import the previously exported key pair */
    if (PSA_SUCCESS !=
        psa_import_key(&attributes, exportedECC_SECP256R1Key,
exportedECC_SECP256R1Keylength, &ecc_key_handle))
    {
        debugger_break();
    }

    /* Sign message using the private key */
    if (PSA_SUCCESS !=
        psa_sign_hash(ecc_key_handle, PSA_ALG_ECDSA(PSA_ALG_SHA_256), payload_hash,
payload_hash_len, signature2,
sizeof(signature2), &signature_length2))
    {
        debugger_break();
    }

    /* Verify signature2 using the public key */
    if (PSA_SUCCESS !=
        psa_verify_hash(ecc_key_handle, PSA_ALG_ECDSA(PSA_ALG_SHA_256), payload_hash,
payload_hash_len, signature2,
signature_length2))
    {
        debugger_break();
    }

    /* Signatures cannot be compared since ECC signatures vary for the same data unless
Deterministic ECC is used which is not supported by the HW.
    * Only the verification operation can be used to validate signatures. */
}
```

## RSA Example

This is an example on using the PSA Crypto API to generate an RSA2048 key, encrypting and decrypting multi-block data and using PKCS7 padding.

```

#define RSA_2048_BIT_LENGTH 2048
#define RSA_2048_EXPORTED_SIZE 1210
/* The RSA 2048 key pair export in der format is roughly as follows
 * RSA private keys:
 * RSAPrivateKey ::= SEQUENCE { ----- 1 + 3
 * version Version, ----- 1 + 1 + 1
 * modulus INTEGER, ----- n ----- 1 + 3 + 256 + 1
 * publicExponent INTEGER, ----- e ----- 1 + 4
 * privateExponent INTEGER, ----- d ----- 1 + 3 + 256 (276
for Wrapped)
 * prime1 INTEGER, ----- p ----- 1 + 3 + (256 / 2)
 * prime2 INTEGER, ----- q ----- 1 + 3 + (256 / 2)
 * exponent1 INTEGER, ----- d mod (p-1) ----- 1 + 2 + (256 / 2) (4 for
Wrapped)
 * exponent2 INTEGER, ----- d mod (q-1) ----- 1 + 2 + (256 / 2) (4 for
Wrapped)
 * coefficient INTEGER, ----- (inverse of q) mod p - 1 + 2 + (256 / 2) (4
for Wrapped)
 * otherPrimeInfos OtherPrimeInfos OPTIONAL ----- 0 (not
supported)
 * }
 */
uint8_t exportedRSA2048Key[RSA_2048_EXPORTED_SIZE];
size_t exportedRSA2048Keylength = 0;
void psa_rsa2048_example (void)
{
/* This example generates an RSA2048 keypair, performs signing and verification
operations.
 * It then exports the generated key into ASN1 DER format to a RAM array which can
then be programmed to flash.
 * It then re-imports that key, and performs signing and verification operations. */
mbedtls_platform_context ctx = {0};
psa_key_handle_t key_handle = {0};
unsigned char payload[] = "ASYMMETRIC_INPUT_FOR_SIGN";

```

```
unsigned char      signature1[PSA_SIGNATURE_MAX_SIZE] = {0};
unsigned char      signature2[PSA_SIGNATURE_MAX_SIZE] = {0};
size_t            signature_length1 = 0;
size_t            signature_length2 = 0;
psa_key_attributes_t attributes          = PSA_KEY_ATTRIBUTES_INIT;
psa_key_attributes_t read_attributes     = PSA_KEY_ATTRIBUTES_INIT;
if (PSA_SUCCESS != mbedtls_platform_setup(&ctx))
{
    debugger_break();
}
if (PSA_SUCCESS != psa_crypto_init())
{
    debugger_break();
}
/* Set key attributes */
psa_set_key_usage_flags(&attributes, PSA_KEY_USAGE_SIGN_HASH |
PSA_KEY_USAGE_VERIFY_HASH | PSA_KEY_USAGE_EXPORT);
psa_set_key_algorithm(&attributes, PSA_ALG_RSA_PKCS1V15_SIGN_RAW);
psa_set_key_type(&attributes, PSA_KEY_TYPE_RSA_KEY_PAIR);
psa_set_key_bits(&attributes, RSA_2048_BIT_LENGTH);
/* To use wrapped keys instead of plaintext:
 * - Use PSA_KEY_LIFETIME_VOLATILE_WRAPPED or PSA_KEY_LIFETIME_PERSISTENT_WRAPPED.
 * - To use persistent keys:
 * - The file system must be initialized prior to calling the generate/import key
functions.
 * - Refer to the littlefs example to see how to format and mount the filesystem. */
psa_set_key_lifetime(&attributes, PSA_KEY_LIFETIME_VOLATILE);
/* Generate RSA 2048 Key pair */
if (PSA_SUCCESS != psa_generate_key(&attributes, &key_handle))
{
    debugger_break();
}
/* Test the key information */
if (PSA_SUCCESS != psa_get_key_attributes(key_handle, &read_attributes))
```

```
{
    debugger_break();
}
/* Sign message using the private key */
if (PSA_SUCCESS !=
    psa_sign_hash(key_handle, PSA_ALG_RSA_PKCS1V15_SIGN_RAW, payload, sizeof
(payload), signature1,
sizeof(signature1), &signature_length1))
{
    debugger_break();
}
/* Verify the signature1 using the public key */
if (PSA_SUCCESS !=
    psa_verify_hash(key_handle, PSA_ALG_RSA_PKCS1V15_SIGN_RAW, payload,
sizeof(payload), signature1,
signature_length1))
{
    debugger_break();
}
/* Export the key */
if (PSA_SUCCESS !=
    psa_export_key(key_handle, exportedRSA2048Key, sizeof(exportedRSA2048Key),
&exportedRSA2048Keylength))
{
    debugger_break();
}
/* Destroy the key and handle */
if (PSA_SUCCESS != psa_destroy_key(key_handle))
{
    debugger_break();
}
/* Import the previously exported key pair */
if (PSA_SUCCESS != psa_import_key(&attributes, exportedRSA2048Key,
exportedRSA2048Keylength, &key_handle))
```

```
{
    debugger_break();
}
/* Sign message using the private key */
if (PSA_SUCCESS !=
    psa_sign_hash(key_handle, PSA_ALG_RSA_PKCS1V15_SIGN_RAW, payload, sizeof
(payload), signature2,
sizeof(signature2), &signature_length2))
{
    debugger_break();
}
/* Verify signature2 using the public key */
if (PSA_SUCCESS !=
    psa_verify_hash(key_handle, PSA_ALG_RSA_PKCS1V15_SIGN_RAW, payload,
sizeof(payload), signature2,
signature_length2))
{
    debugger_break();
}
/* Compare signatures to verify that the same signature was generated */
if (0 != memcmp(signature2, signature1, signature_length2))
{
    debugger_break();
}
mbedtls_psa_crypto_free();
mbedtls_platform_teardown(&ctx);
}
```

## Function Documentation

---

◆ **RM\_PSA\_CRYPTO\_TRNG\_Read()**

```
fsp_err_t RM_PSA_CRYPTO_TRNG_Read ( uint8_t*const p_rngbuf, uint32_t num_req_bytes,
uint32_t* p_num_gen_bytes )
```

Reads requested length of random data from the TRNG. Generate nbytes of random bytes and store them in p\_rngbuf buffer.

**Return values**

FSP_SUCCESS	Random number generation successful
FSP_ERR_ASSERTION	NULL input parameter(s).
FSP_ERR_CRYPTO_UNKNOWN	An unknown error occurred.

**Returns**

See [Common Error Codes](#) or functions called by this function for other possible return codes. This function calls:

- s\_generate\_16byte\_random\_data

◆ **mbedtls\_platform\_setup()**

```
int mbedtls_platform_setup ( mbedtls_platform_context * ctx)
```

This function initializes the SCE and the TRNG. It **must** be invoked before the crypto library can be used. This implementation is used if MBEDTLS\_PLATFORM\_SETUP\_TEARDOWN\_ALT is defined.

Example:

```
mbedtls_platform_context ctx = {0};
/* Setup the platform; initialize the SCE and the TRNG */
if (PSA_SUCCESS != mbedtls_platform_setup(&ctx))
```

**Return values**

0	Initialization was successful.
MBEDTLS_ERR_PLATFORM_HW_ACCEL_FAILED	SCE Initialization error.

### ◆ mbedtls\_platform\_teardown()

```
void mbedtls_platform_teardown ( mbedtls_platform_context * ctx)
```

This implementation is used if MBEDTLS\_PLATFORM\_SETUP\_TEARDOWN\_ALT is defined. It is intended to de-initialize any items that were initialized in the [mbedtls\\_platform\\_setup\(\)](#) function, but currently is only a placeholder function.

Example:

```
/* De-initialize the platform. This is currently a placeholder function which does
not do anything. */
mbedtls_platform_teardown(&ctx);
```

#### Return values

N/A	
-----	--

## 4.2.72 Capacitive Touch Middleware (rm\_touch)

### Modules

#### Functions

**fsp\_err\_t** [RM\\_TOUCH\\_Open](#) ([touch\\_ctrl\\_t](#) \*const p\_ctrl, [touch\\_cfg\\_t](#) const \*const p\_cfg)

Opens and configures the TOUCH Middle module. Implements [touch\\_api\\_t::open](#). [More...](#)

**fsp\_err\_t** [RM\\_TOUCH\\_ScanStart](#) ([touch\\_ctrl\\_t](#) \*const p\_ctrl)

This function should be called each time a periodic timer expires. If initial offset tuning is enabled, The first several calls are used to tuning for the sensors. Before starting the next scan, first get the data with [RM\\_TOUCH\\_DataGet\(\)](#). If a different control block scan should be run, check the scan is complete before executing. Implements [touch\\_api\\_t::scanStart](#). [More...](#)

**fsp\_err\_t** [RM\\_TOUCH\\_DataGet](#) ([touch\\_ctrl\\_t](#) \*const p\_ctrl, [uint64\\_t](#) \*p\_button\_status, [uint16\\_t](#) \*p\_slider\_position, [uint16\\_t](#) \*p\_wheel\_position)

Gets the 64-bit mask indicating which buttons are pressed. Also, this function gets the current position of where slider or wheel is being pressed. If initial offset tuning is enabled, The first several calls are used to tuning for the sensors. Implements [touch\\_api\\_t::dataGet](#). [More...](#)

`fsp_err_t RM_TOUCH_PadDataGet (touch_ctrl_t *const p_ctrl, uint16_t *p_pad_rx_coordinate, uint16_t *p_pad_tx_coordinate, uint8_t *p_pad_num_touch)`

This function gets the current position of pad is being pressed. Implements `touch_api_t::padDataGet` , `g_touch_on_ctsu`. [More...](#)

`fsp_err_t RM_TOUCH_CallbackSet (touch_ctrl_t *const p_api_ctrl, void(*p_callback)(touch_callback_args_t *), void const *const p_context, touch_callback_args_t *const p_callback_memory)`

`fsp_err_t RM_TOUCH_Close (touch_ctrl_t *const p_ctrl)`

Disables specified TOUCH control block. Implements `touch_api_t::close`. [More...](#)

`fsp_err_t RM_TOUCH_VersionGet (fsp_version_t *const p_version)`

## Detailed Description

This module supports the Capacitive Touch Sensing Unit (CTSUs). It implements the [Touch Middleware Interface](#).

## Overview

The Touch Middleware uses the [Capacitive Touch Sensing Unit \(r\\_ctsu\)](#) API and provides application-level APIs for scanning touch buttons, sliders, and wheels. This module is configured via the [QE for Capacitive Touch](#).

## Features

- Supports touch buttons (Self and Mutual), sliders, and wheels
- Can retrieve the status of up to 64 buttons at once
- Software and external triggering
- Callback on scan end
- Collects and calculates usable scan results:
  - Slider position from 0 to 100 (percent)
  - Wheel position from 0 to 359 (degrees)
- Optional (build time) support for real-time monitoring functionality through the QE tool over UART

## Configuration

### Note

*This module is configured via the [QE for Capacitive Touch](#). For information on how to use the QE tool, once the tool is installed click [Help](#) -> [Help Contents in e2 studio](#) and search for "QE".*

*Multiple configurations can be defined within a single project allowing for different scan procedures or button layouts.*



## Build Time Configurations for rm\_touch

The following build time configurations are defined in fsp\_cfg/rm\_touch\_cfg.h:

Configuration	Options	Default	Description
Parameter Checking	<ul style="list-style-type: none"> <li>Default (BSP)</li> <li>Enabled</li> <li>Disabled</li> </ul>	Default (BSP)	If selected code for parameter checking is included in the build.
Support for QE monitoring using UART	<ul style="list-style-type: none"> <li>Enabled</li> <li>Disabled</li> </ul>	Disabled	Enable SCI_UART support for QE monitoring.

## Configurations for Middleware > CapTouch > TOUCH Driver on rm\_touch

This module can be added to the Stacks tab via New Stack > Middleware > CapTouch > TOUCH Driver on rm\_touch. Non-secure callable guard functions can be generated for this module by right clicking the module in the RA Configuration tool and checking the "Non-secure Callable" box.

Configuration	Options	Default	Description
---------------	---------	---------	-------------

### Interrupt Configuration

Refer to the [Capacitive Touch Sensing Unit \(r\\_ctsu\)](#) section for details.

### Clock Configuration

Refer to the [Capacitive Touch Sensing Unit \(r\\_ctsu\)](#) section for details.

### Pin Configuration

Refer to the [Capacitive Touch Sensing Unit \(r\\_ctsu\)](#) section for details.

## Usage Notes

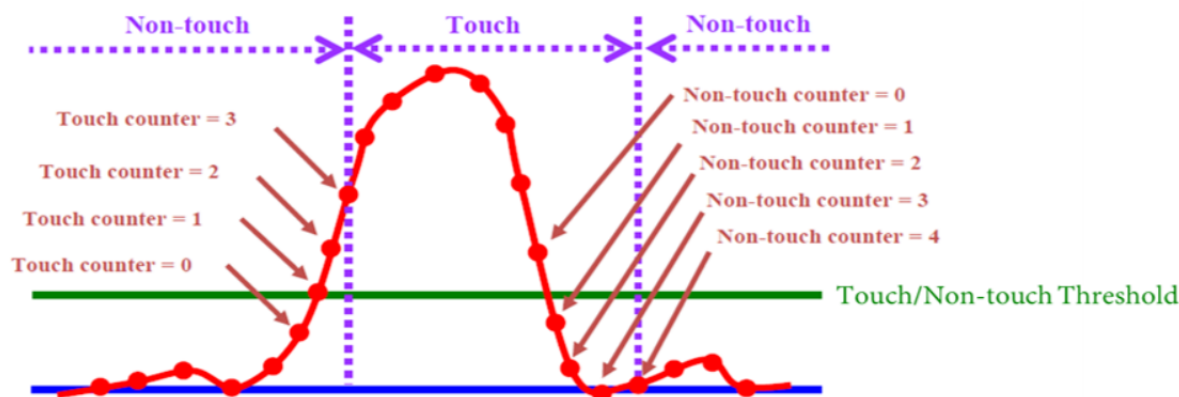
### Sliders and Wheels

Sliders and wheels are subject so some limitations:

	Slider	Wheel
Electrode type	Self capacitance only	Self capacitance only
Number of electrodes	4+	3-5
Touch position output range	0-100	0-359
Default value (no touch)	0xFFFF	0xFFFF

### Touch Judgement

Touch data is judged as touched or not-touched based on the threshold and hysteresis values determined during the QE tool tuning process. Refer to the QE for Capacitive Touch tool documentation in e2 studio Help for details on how these values are set.



Measurement Count	Initialization	n	n+1	n+2	n+3	n+4	n+5	n+6	n+7	n+8	n+9	n+10	n+11
User-set touch/non-touch	Non-touch			Touch						Non-touch			
Touch counter buffer	0	0	0	1	2	3	3	3	0	0	0	0	0
Non-touch counter buffer	0	1	2	0	0	0	0	0	1	2	3	4	4
Touch/Non-touch judgement buffer	0	0	0	0	0	1	1	1	1	1	1	0	0
Actual touch/Non-touch judgement	Non-touch					Touch						Non-touch	

Figure 190: Touch/Non-touch judgement Image

## TrustZone Support

In `r_ctsu` and `rm_touch` module, Non-Secure Callable Guard Functions are only generated from QE for Capacitive Touch. QE can be used for tuning in secure or flat project, but not in non-secure project. If you want to use in non-secure project, copy the output file from secure or flat project. Refer to QE Help for more information.

## Examples

### Basic Example

This is a basic example of minimal use of the TOUCH in an application.

```
void touch_basic_example (void)
{
    fsp_err_t err = FSP_SUCCESS;

    err = RM_TOUCH_Open(&g_touch_ctrl, &g_touch_cfg);

    /* Handle any errors. This function should be defined by the user. */
    handle_error(err);

    while (true)
    {
        RM_TOUCH_ScanStart(&g_touch_ctrl);

        while (0 == g_flag)
```

```
    {  
/* Wait scan end callback */  
    }  
    g_flag = 0;  
    err = RM_TOUCH_DataGet(&g_touch_ctrl, &button, slider, wheel);  
if (FSP_SUCCESS == err)  
    {  
/* Application specific data processing. */  
    }  
    }  
}
```

## Multi Mode Example

This is an optional example of using both Self-capacitance and Mutual-capacitance. Refer to the Multi Mode Example in CTSU usage notes.

```
void touch_optional_example (void)  
{  
    fsp_err_t err = FSP_SUCCESS;  
    err = RM_TOUCH_Open(&g_touch_ctrl, &g_touch_cfg);  
    handle_error(err);  
    err = RM_TOUCH_Open(&g_touch_ctrl_mutual, &g_touch_cfg_mutual);  
    handle_error(err);  
    while (true)  
    {  
RM_TOUCH_ScanStart(&g_touch_ctrl);  
        while (0 == g_flag)  
        {  
/* Wait scan end callback */  
        }  
        g_flag = 0;  
RM_TOUCH_ScanStart(&g_touch_ctrl_mutual);  
        while (0 == g_flag)  
        {
```

```

/* Wait scan end callback */
    }
    g_flag = 0;
    err = RM_TOUCH_DataGet(&g_touch_ctrl, &button, slider, wheel);
if (FSP_SUCCESS == err)
    {
/* Application specific data processing. */
    }
    err = RM_TOUCH_DataGet(&g_touch_ctrl_mutual, &button, slider, wheel);
if (FSP_SUCCESS == err)
    {
/* Application specific data processing. */
    }
    }
}

```

## Data Structures

struct [touch\\_button\\_info\\_t](#)

struct [touch\\_slider\\_info\\_t](#)

struct [touch\\_wheel\\_info\\_t](#)

struct [touch\\_pad\\_info\\_t](#)

struct [touch\\_instance\\_ctrl\\_t](#)

## Data Structure Documentation

### ◆ touch\_button\_info\_t

struct touch_button_info_t		
Information of button		
Data Fields		
uint64_t	status	Touch result bitmap.
uint16_t*	p_threshold	Pointer to Threshold value array. g_touch_button_threshold[] is set by Open API.
uint16_t*	p_hysteresis	Pointer to Hysteresis value

		array. g_touch_button_hysteresis[] is set by Open API.
uint16_t *	p_reference	Pointer to Reference value array. g_touch_button_reference[] is set by Open API.
uint16_t *	p_on_count	Continuous touch counter. g_touch_button_on_count[] is set by Open API.
uint16_t *	p_off_count	Continuous non-touch counter. g_touch_button_off_count[] is set by Open API.
uint32_t *	p_drift_buf	Drift reference value. g_touch_button_drift_buf[] is set by Open API.
uint16_t *	p_drift_count	Drift counter. g_touch_button_drift_count[] is set by Open API.
uint8_t	on_freq	Copy from config by Open API.
uint8_t	off_freq	Copy from config by Open API.
uint16_t	drift_freq	Copy from config by Open API.
uint16_t	cancel_freq	Copy from config by Open API.

#### ◆ touch\_slider\_info\_t

struct touch_slider_info_t		
Information of slider		
Data Fields		
uint16_t *	p_position	Calculated Position data. g_touch_slider_position[] is set by Open API.
uint16_t *	p_threshold	Copy from config by Open API. g_touch_slider_threshold[] is set by Open API.

#### ◆ touch\_wheel\_info\_t

struct touch_wheel_info_t		
Information of wheel		
Data Fields		
uint16_t *	p_position	Calculated Position data. g_touch_wheel_position[] is set by Open API.
uint16_t *	p_threshold	Copy from config by Open API.

		<code>g_touch_wheel_threshold[]</code> is set by Open API.
--	--	------------------------------------------------------------

◆ **touch\_pad\_info\_t**

struct touch_pad_info_t		
Information of pad		
Data Fields		
<code>uint16_t *</code>	<code>p_rx_coordinate</code>	RX coordinate.
<code>uint16_t *</code>	<code>p_tx_coordinate</code>	TX coordinate.
<code>uint16_t *</code>	<code>p_num_touch</code>	number of touch
<code>uint16_t *</code>	<code>p_threshold</code>	Coordinate calculation threshold value.
<code>uint16_t *</code>	<code>p_base_buf</code>	ScanData Base Value Buffer.
<code>uint16_t *</code>	<code>p_rx_pixel</code>	X coordinate resolution.
<code>uint16_t *</code>	<code>p_tx_pixel</code>	Y coordinate resolution.
<code>uint8_t *</code>	<code>p_max_touch</code>	Maximum number of touch judgments used by the pad.
<code>int32_t *</code>	<code>p_drift_buf</code>	Drift reference value. <code>g_touch_button_drift_buf[]</code> is set by Open API.
<code>uint16_t *</code>	<code>p_drift_count</code>	Drift counter. <code>g_touch_button_drift_count[]</code> is set by Open API.
<code>uint8_t</code>	<code>num_drift</code>	Copy from config by Open API.

◆ **touch\_instance\_ctrl\_t**

struct touch_instance_ctrl_t		
TOUCH private control block. DO NOT MODIFY. Initialization occurs when <code>RM_TOUCH_Open()</code> is called.		
Data Fields		
<code>uint32_t</code>	<code>open</code>	Whether or not driver is open.
<code>touch_button_info_t</code>	<code>binfo</code>	Information of button.
<code>touch_slider_info_t</code>	<code>sinfo</code>	Information of slider.
<code>touch_wheel_info_t</code>	<code>winfo</code>	Information of wheel.
<code>touch_pad_info_t</code>	<code>pinfo</code>	Information of pad.
<code>touch_cfg_t const *</code>	<code>p_touch_cfg</code>	Pointer to initial configurations.
<code>ctsu_instance_t const *</code>	<code>p_ctsu_instance</code>	Pointer to CTSU instance.

**Function Documentation**

◆ **RM\_TOUCH\_Open()**

```
fsp_err_t RM_TOUCH_Open ( touch_ctrl_t *const p_ctrl, touch_cfg_t const *const p_cfg )
```

Opens and configures the TOUCH Middle module. Implements `touch_api_t::open`.

Example:

```
err = RM_TOUCH_Open(&g_touch_ctrl, &g_touch_cfg);
```

**Return values**

FSP_SUCCESS	TOUCH successfully configured.
FSP_ERR_ASSERTION	Null pointer, or one or more configuration options is invalid.
FSP_ERR_ALREADY_OPEN	Module is already open. This module can only be opened once.
FSP_ERR_INVALID_ARGUMENT	Configuration parameter error.

◆ **RM\_TOUCH\_ScanStart()**

```
fsp_err_t RM_TOUCH_ScanStart ( touch_ctrl_t *const p_ctrl)
```

This function should be called each time a periodic timer expires. If initial offset tuning is enabled, The first several calls are used to tuning for the sensors. Before starting the next scan, first get the data with `RM_TOUCH_DataGet()`. If a different control block scan should be run, check the scan is complete before executing. Implements `touch_api_t::scanStart`.

**Return values**

FSP_SUCCESS	Successfully started.
FSP_ERR_ASSERTION	Null pointer passed as a parameter.
FSP_ERR_NOT_OPEN	Module is not open.
FSP_ERR_CTSU_SCANNING	Scanning this instance or other.
FSP_ERR_CTSU_NOT_GET_DATA	The previous data has not been retrieved by DataGet.

◆ **RM\_TOUCH\_DataGet()**

```
fsp_err_t RM_TOUCH_DataGet ( touch_ctrl_t *const p_ctrl, uint64_t * p_button_status, uint16_t *
p_slider_position, uint16_t * p_wheel_position )
```

Gets the 64-bit mask indicating which buttons are pressed. Also, this function gets the current position of where slider or wheel is being pressed. If initial offset tuning is enabled, The first several calls are used to tuning for the sensors. Implements [touch\\_api\\_t::dataGet](#).

**Return values**

FSP_SUCCESS	Successfully data decoded.
FSP_ERR_ASSERTION	Null pointer passed as a parameter.
FSP_ERR_NOT_OPEN	Module is not open.
FSP_ERR_CTSU_SCANNING	Scanning this instance.
FSP_ERR_CTSU_INCOMPLETE_TUNING	Incomplete initial offset tuning.

◆ **RM\_TOUCH\_PadDataGet()**

```
fsp_err_t RM_TOUCH_PadDataGet ( touch_ctrl_t *const p_ctrl, uint16_t * p_pad_rx_coordinate,
uint16_t * p_pad_tx_coordinate, uint8_t * p_pad_num_touch )
```

This function gets the current position of pad is being pressed. Implements [touch\\_api\\_t::padDataGet](#) , [g\\_touch\\_on\\_ctsu](#).

**Return values**

FSP_SUCCESS	Successfully data decoded.
FSP_ERR_ASSERTION	Null pointer.
FSP_ERR_NOT_OPEN	Module is not open.
FSP_ERR_CTSU_SCANNING	Scanning this instance.



◆ **RM\_TOUCH\_CallbackSet()**

```
fsp_err_t RM_TOUCH_CallbackSet ( touch_ctrl_t *const p_api_ctrl, void (*)(touch_callback_args_t *)
p_callback, void const *const p_context, touch_callback_args_t *const p_callback_memory )
```

Updates the user callback and has option of providing memory for callback structure. Implements [touch\\_api\\_t::callbackSet](#)

**Return values**

FSP_SUCCESS	Callback updated successfully.
FSP_ERR_ASSERTION	A required pointer is NULL.
FSP_ERR_NOT_OPEN	The control block has not been opened.

◆ **RM\_TOUCH\_Close()**

```
fsp_err_t RM_TOUCH_Close ( touch_ctrl_t *const p_ctrl)
```

Disables specified TOUCH control block. Implements [touch\\_api\\_t::close](#).

**Return values**

FSP_SUCCESS	Successfully closed.
FSP_ERR_ASSERTION	Null pointer passed as a parameter.
FSP_ERR_NOT_OPEN	Module is not open.

◆ **RM\_TOUCH\_VersionGet()**

```
fsp_err_t RM_TOUCH_VersionGet ( fsp_version_t *const p_version)
```

Return TOUCH Middle module version. Implements [touch\\_api\\_t::versionGet](#).

**Return values**

FSP_SUCCESS	Version information successfully read.
FSP_ERR_ASSERTION	Null pointer passed as a parameter

**4.2.73 Virtual EEPROM (rm\_vee\_flash)**

Modules

**Functions**

fsp_err_t	RM_VEE_FLASH_Open (rm_vee_ctrl_t *const p_api_ctrl, rm_vee_cfg_t const *const p_cfg)
fsp_err_t	RM_VEE_FLASH_RecordWrite (rm_vee_ctrl_t *const p_api_ctrl, uint32_t const rec_id, uint8_t const *const p_rec_data, uint32_t const num_bytes)
fsp_err_t	RM_VEE_FLASH_RecordPtrGet (rm_vee_ctrl_t *const p_api_ctrl, uint32_t const rec_id, uint8_t **const pp_rec_data, uint32_t *const p_num_bytes)
fsp_err_t	RM_VEE_FLASH_RefDataWrite (rm_vee_ctrl_t *const p_api_ctrl, uint8_t const *const p_ref_data)
fsp_err_t	RM_VEE_FLASH_RefDataPtrGet (rm_vee_ctrl_t *const p_api_ctrl, uint8_t **const pp_ref_data)
fsp_err_t	RM_VEE_FLASH_StatusGet (rm_vee_ctrl_t *const p_api_ctrl, rm_vee_status_t *const p_status)
fsp_err_t	RM_VEE_FLASH_Refresh (rm_vee_ctrl_t *const p_api_ctrl)
fsp_err_t	RM_VEE_FLASH_Format (rm_vee_ctrl_t *const p_api_ctrl, uint8_t const *const p_ref_data)
fsp_err_t	RM_VEE_FLASH_CallbackSet (rm_vee_ctrl_t *const p_api_ctrl, void(*p_callback)(rm_vee_callback_args_t *), void const *const p_context, rm_vee_callback_args_t *const p_callback_memory)
fsp_err_t	RM_VEE_FLASH_Close (rm_vee_ctrl_t *const p_api_ctrl)
fsp_err_t	RM_VEE_FLASH_VersionGet (fsp_version_t *const p_version)

## Detailed Description

Virtual EEPROM on RA MCUs. This module implements the [Virtual EEPROM Interface](#).

## Overview

This VEE module emulates basic EEPROM capabilities. Support is provided for reading and writing both common records and reference data (originally programmed during product assembly or test). A count of the number of segments erased throughout the lifetime of the application is maintained and can be accessed at any time. Wear leveling is handled automatically by the driver.

## Features

- Writing and reading user defined records of any length to data flash.
- Wear leveling is handled automatically.
- Reference data such as calibration data programmed at assembly or test time is preserved.
- Reference data can be updated at run time.

- Fault resilient design.

## Data Flash Segmentation

Wear leveling is handled by changing the location in the data flash where a record is stored every time that it is updated. This change in physical location of the record is transparent to the user. Any time an update for a specific record ID is written, it is written to the next unused location in data flash and its location is stored in RAM for quick look-up later. When required, only the most recent version of these records is automatically copied to the next blank segment in data flash. The data flash area is divided into a number of equal-size segments. There is only one segment active at a time. A segment contains two areas- the record area (which is the vast majority of the segment) and the reference data area which contains optional data typically programmed during assembly or final test. Records and updated reference data are written to this segment until one of the two areas becomes full. The record area must be able to hold at least one of every record ID possible and still have space left over for record updates.

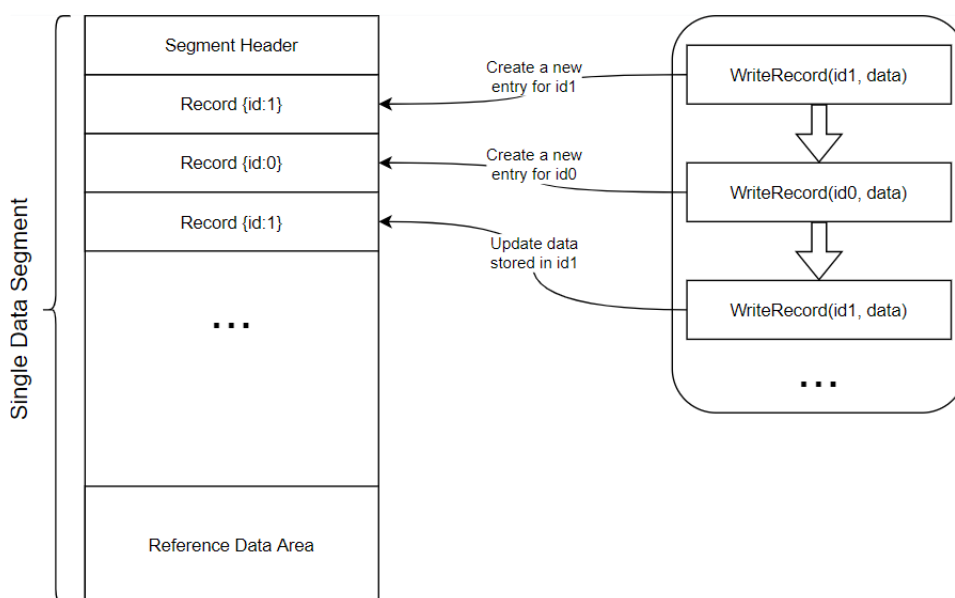


Figure 191: Segment Data Format

When a segment does not have sufficient space for additional records or updated reference data, a Refresh occurs. This process copies the most recent record for each ID as well as the latest version of reference data (if any) to the next segment. The very first time VEE runs on an MCU, it marks the last segment as active whether there is reference data configured or not. The end of VEE data flash area is used to provide an easily identified physical flash address that can be used while programming reference data without requiring Virtual EEPROM middleware.

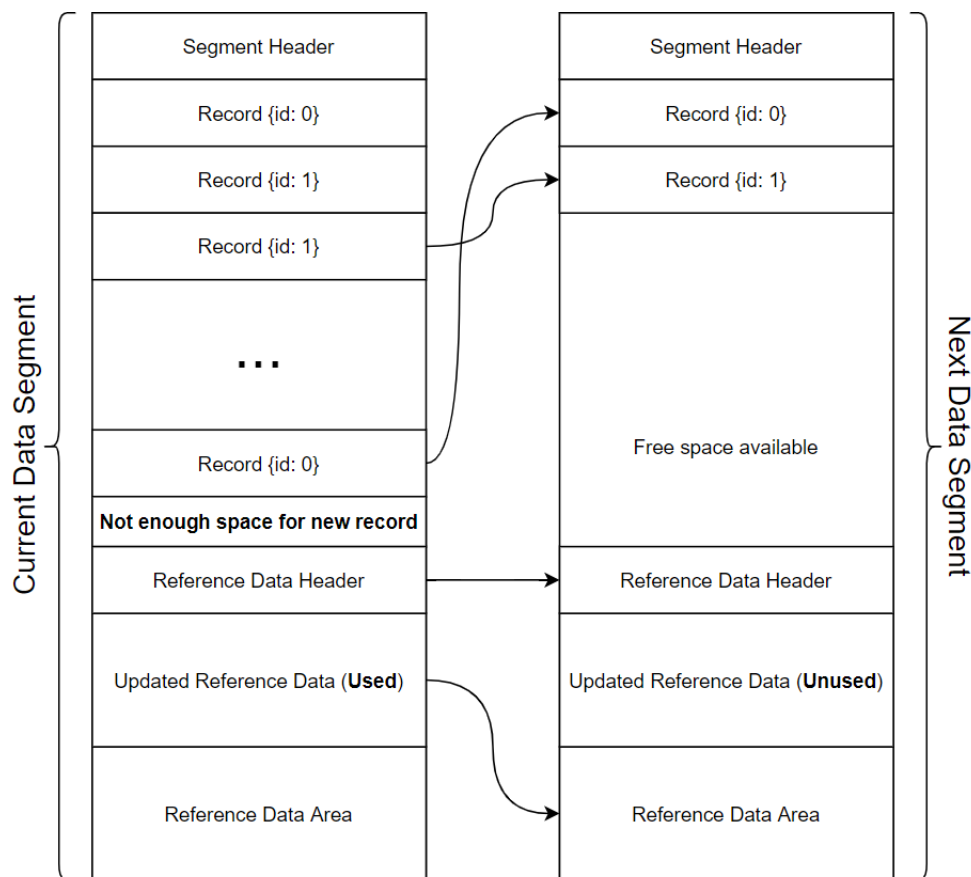


Figure 192: Refresh Operation

### Record Format

Each record begins with a header that contains the record size, followed by the data, and the trailer. The trailer contains a validation code which is used for internal purposes only and is not a 16-bit CRC or ECC value. If that level of error checking is desired, the user should include that in the record data passed to the driver.

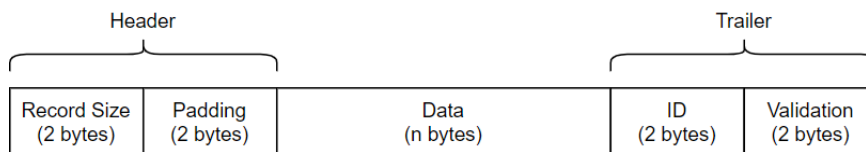


Figure 193: Record Format

### Reference Data Area

VEE can be configured for the presence of reference data. The original programmed reference data must be located at the end of the VEE data flash area. An area of equal size is reserved below this in case updated reference data becomes available later. Below that is a header which indicates whether the update area has been written to.

Padding (2 bytes)	Validation (2 bytes)	Update Area (n bytes)	Reference Data (n bytes)
----------------------	-------------------------	--------------------------	-----------------------------

Figure 194: Reference Data Area Format

Just as with records, the validation code is used for internal purposes only and is not a 16-bit CRC or ECC value. If that level of error checking is desired, the user should include that in the updated reference data passed to the driver.

## Fault Tolerance

The Virtual EEPROM has a fault tolerant design. If for any reason an operation fails before it is completed the next time the module is opened a refresh will occur. Any corrupted data will be discarded.

## Configuration

### Build Time Configurations for rm\_vee\_flash

The following build time configurations are defined in fsp\_cfg/rm\_vee\_flash\_cfg.h:

Configuration	Options	Default	Description
Parameter Checking	<ul style="list-style-type: none"> <li>Default (BSP)</li> <li>Enabled</li> <li>Disabled</li> </ul>	Default (BSP)	If selected code for parameter checking is included in the build.
Reference Data Support	<ul style="list-style-type: none"> <li>Enabled</li> <li>Disabled</li> </ul>	Disabled	Support writing reference data to the end of the segment.
Refresh Buffer Size	Value must be an integer greater than 0 and a multiple of 4 bytes.	32	The size of the internal buffer used to copying data from one flash segment to another during a refresh operation. This is required because data flash to data flash transfers are not supported by the hardware.

### Configurations for Middleware > Storage > Virtual EEPROM on Flash

This module can be added to the Stacks tab via New Stack > Middleware > Storage > Virtual EEPROM on Flash. Non-secure callable guard functions can be generated for this module by right clicking the module in the RA Configuration tool and checking the "Non-secure Callable" box.

Configuration	Options	Default	Description
Name	Name must be a valid C symbol	g_vee0	Module name.

Record Max ID	Value must be an integer.	16	Set this value to the highest record ID in use.
Number of Segments	Value must be an integer.	2	Set value to number of segments desired in data flash (minimum 2). The fewer the segments, the fewer refreshes occur, but the longer refreshes take to complete (erase time).
Total Size	Manual Entry	BSP_DATA_FLASH_SIZE_BYTES	The total size (In bytes) of the flash area used by Virtual EEPROM.
Reference Data Size	Value must be an integer.	0	The size of the reference area (In bytes) used by Virtual EEPROM.
Callback	Name must be a valid C symbol	vee_callback	A user callback function can be provided. If this callback function is provided, it will be called from the flash interrupt service routine (ISR).

## Clock Configuration

There is no clock configuration for the RM\_VEE\_FLASH module.

## Pin Configuration

This module does not use I/O pins.

## Usage Notes

A refresh buffer is required to copy data between segments. Data flash cannot be simultaneously read from and written to. Data will be temporarily copied into RAM during refresh operations.

## Examples

### Basic Example

This is a basic example of minimal use of the RM\_VEE\_FLASH module in an application.

```
volatile bool callback_called = false;
/* Record ID to use for storing pressure data. */
#define ID_PRESSURE (0U)
```

```
/* Example data structure. */
typedef struct st_pressure
{
    uint32_t timestamp;
    uint16_t low;
    uint16_t average;
    uint16_t high;
} pressure_t;

void rm_vee_example ()
{
    /* Open the Virtual EEPROM Module. */
    fsp_err_t err = RM_VEE_FLASH_Open(&g_vee_ctrl, &g_vee_cfg);
    if (FSP_SUCCESS != err)
    {
        error_handler();
    }

    /* Read pressure data from external sensor. */
    pressure_t pressure_data;
    get_pressure_data(&pressure_data);

    /* Write the pressure data to a Virtual EEPROM Record. */
    err = RM_VEE_FLASH_RecordWrite(&g_vee_ctrl, ID_PRESSURE, (uint8_t *)
&pressure_data, sizeof(pressure_t));
    if (FSP_SUCCESS != err)
    {
        error_handler();
    }

    /* Wait for the Virtual EEPROM callback to indicate it finished writing data. */
    while (false == callback_called)
    {
        ;
    }

    /* Get a pointer to the record that is stored in data flash. */
    uint32_t length;
    pressure_t * p_pressure_data;
```

```

    err = RM_VEE_FLASH_RecordPtrGet(&g_vee_ctrl, ID_PRESSURE, (uint8_t **)
&p_pressure_data, &length);
    if (FSP_SUCCESS != err)
    {
        error_handler();
    }
    /* Close the Virtual EEPROM Module. */
    err = RM_VEE_FLASH_Close(&g_vee_ctrl);
    if (FSP_SUCCESS != err)
    {
        error_handler();
    }
}
void rm_vee_tests_callback (rm_vee_callback_args_t * p_args)
{
    callback_called = true;
    FSP_PARAMETER_NOT_USED(p_args);
}

```

## Data Structures

struct [rm\\_vee\\_flash\\_cfg\\_t](#)

struct [rm\\_vee\\_flash\\_instance\\_ctrl\\_t](#)

## Data Structure Documentation

### ◆ [rm\\_vee\\_flash\\_cfg\\_t](#)

struct <a href="#">rm_vee_flash_cfg_t</a>		
User configuration structure, used in open function		
Data Fields		
<a href="#">flash_instance_t</a> const *	p_flash	Pointer to a flash instance.

### ◆ [rm\\_vee\\_flash\\_instance\\_ctrl\\_t](#)

struct <a href="#">rm_vee_flash_instance_ctrl_t</a>
Instance control block. This is private to the FSP and should not be used or modified by the application.



## Function Documentation

### ◆ RM\_VEE\_FLASH\_Open()

```
fsp_err_t RM_VEE_FLASH_Open ( rm_vee_ctrl_t *const p_api_ctrl, rm_vee_cfg_t const *const p_cfg )
```

Open the RM\_VEE\_FLASH driver module

Implements [rm\\_vee\\_api\\_t::open](#)

Initializes the driver's internal structures and opens the Flash driver. The Flash driver must be closed prior to opening VEE. The error code FSP\_SUCCESS\_RECOVERY indicates that VEE detected corrupted data; most likely due to a power loss during a data flash write or erase. In these cases, an automatic internal Refresh is performed and the partially written data is lost.

#### Return values

FSP_SUCCESS	Successful. FSP_SUCCESS_RECOVERY changed to FSP_SUCCESS
FSP_ERR_ASSERTION	An input parameter is NULL.
FSP_ERR_ALREADY_OPEN	This function has already been called.
FSP_ERR_PE_FAILURE	This error indicates that a flash programming, erase, or blankcheck operation has failed in hardware.
FSP_ERR_TIMEOUT	Interrupts disabled outside of VEE
FSP_ERR_NOT_INITIALIZED	Corruption found. A refresh is required.
FSP_ERR_INVALID_ARGUMENT	The supplied configuration is invalid.

### ◆ RM\_VEE\_FLASH\_RecordWrite()

```
fsp_err_t RM_VEE_FLASH_RecordWrite ( rm_vee_ctrl_t *const p_api_ctrl, uint32_t const rec_id,
uint8_t const *const p_rec_data, uint32_t const num_bytes )
```

Writes a record to data flash.

Implements `rm_vee_api_t::recordWrite`

This function writes `num_bytes` of data pointed to by `p_rec_data` to data flash. This function returns immediately after starting the flash write. BE SURE NOT TO MODIFY the data buffer contents until after the write completes. This includes exiting the calling function when the data buffer is a local variable (stack may be used by another function and corrupt the data buffer contents).

#### Return values

FSP_SUCCESS	Write started successfully.
FSP_ERR_NOT_OPEN	The module has not been opened.
FSP_ERR_ASSERTION	An input parameter is NULL.
FSP_ERR_INVALID_ARGUMENT	An argument contains an illegal value.
FSP_ERR_INVALID_MODE	The operation cannot be started in the current mode.
FSP_ERR_IN_USE	Last API call still executing.
FSP_ERR_PE_FAILURE	This error indicates that a flash programming, erase, or blankcheck operation has failed in hardware.
FSP_ERR_TIMEOUT	Flash write timed out (Should not be possible when flash bgo is used).
FSP_ERR_NOT_INITIALIZED	Corruption found. A refresh is required.

◆ **RM\_VEE\_FLASH\_RecordPtrGet()**

```
fsp_err_t RM_VEE_FLASH_RecordPtrGet ( rm_vee_ctrl_t *const p_api_ctrl, uint32_t const rec_id,
uint8_t **const pp_rec_data, uint32_t *const p_num_bytes )
```

Gets a pointer to the most recent reference data.

Implements `rm_vee_api_t::recordPtrGet`

This function sets the argument pointer to the most recent version of the reference data in flash. Flash cannot be accessed for reading and writing at the same time. Therefore, reading the data at `p_ref_data` must be completed prior to initiating any type of Flash write.

**Return values**

FSP_SUCCESS	Successful.
FSP_ERR_NOT_OPEN	The module has not been opened.
FSP_ERR_IN_USE	Last API call still executing.
FSP_ERR_ASSERTION	<code>p_ref_data</code> is NULL.
FSP_ERR_INVALID_ARGUMENT	Reference data not configured.
FSP_ERR_NOT_FOUND	The record associated with the requested ID could not be found.

### ◆ RM\_VEE\_FLASH\_RefDataWrite()

```
fsp_err_t RM_VEE_FLASH_RefDataWrite ( rm_vee_ctrl_t *const p_api_ctrl, uint8_t const *const p_ref_data )
```

Writes new Reference data to the reference update area.

Implements `rm_vee_api_t::refDataWrite`

This function writes VEE\_CFG\_REF\_DATA\_SIZE bytes pointed to by p\_ref\_data to data flash. This function returns immediately after starting the flash write. BE SURE NOT TO MODIFY the data buffer contents until after the write completes.

#### Return values

FSP_SUCCESS	Write started successfully.
FSP_ERR_NOT_OPEN	The module has not been opened.
FSP_ERR_IN_USE	Last API call still executing.
FSP_ERR_ASSERTION	An input parameter is NULL.
FSP_ERR_INVALID_MODE	The operation cannot be started in the current mode.
FSP_ERR_PE_FAILURE	This error indicates that a flash programming, erase, or blankcheck operation has failed in hardware.
FSP_ERR_TIMEOUT	Flash write timed out (Should not be possible when flash bgo is used).
FSP_ERR_UNSUPPORTED	Reference data is not supported in the current configuration.
FSP_ERR_NOT_INITIALIZED	Corruption found. A refresh is required.

◆ **RM\_VEE\_FLASH\_RefDataPtrGet()**

```
fsp_err_t RM_VEE_FLASH_RefDataPtrGet ( rm_vee_ctrl_t *const p_api_ctrl, uint8_t **const pp_ref_data )
```

Gets a pointer to the most recent reference data.

Implements `rm_vee_api_t::recordPtrGet`

This function sets the argument pointer to the most recent version of the reference data in flash. Flash cannot be accessed for reading and writing at the same time.

**Return values**

FSP_SUCCESS	Successful.
FSP_ERR_NOT_OPEN	The module has not been opened.
FSP_ERR_IN_USE	Last API call still executing.
FSP_ERR_ASSERTION	An input parameter is NULL.
FSP_ERR_UNSUPPORTED	Reference data is not supported in the current configuration.
FSP_ERR_NOT_FOUND	No reference data was found.

◆ **RM\_VEE\_FLASH\_StatusGet()**

```
fsp_err_t RM_VEE_FLASH_StatusGet ( rm_vee_ctrl_t *const p_api_ctrl, rm_vee_status_t *const p_status )
```

Get the current status of the driver.

Implements `rm_vee_api_t::statusGet`

This command is typically used to verify that the last Write or Refresh command has completed before attempting to perform another API call.

**Return values**

FSP_SUCCESS	Successful.
FSP_ERR_NOT_OPEN	The module has not been opened.
FSP_ERR_ASSERTION	An input parameter is NULL.

### ◆ RM\_VEE\_FLASH\_Refresh()

`fsp_err_t RM_VEE_FLASH_Refresh ( rm_vee_ctrl_t *const p_api_ctrl)`

Manually start a refresh operation

Implements `rm_vee_api_t::refresh`

This function is used to start a segment Refresh at any time. The Refresh process by default occurs automatically when no more record or reference data space is available and a Write is requested. However, the app may desire to force a refresh when it knows it is running low on space and large amounts of data are about to be recorded.

#### Return values

FSP_SUCCESS	Successful.
FSP_ERR_NOT_OPEN	The module has not been opened.
FSP_ERR_ASSERTION	An input parameter is NULL.
FSP_ERR_IN_USE	Last API call still executing.
FSP_ERR_PE_FAILURE	This error indicates that a flash programming, erase, or blankcheck operation has failed in hardware.
FSP_ERR_INVALID_MODE	The operation cannot be started in the current mode.
FSP_ERR_TIMEOUT	Flash write timed out (Should not be possible when flash bgo is used).
FSP_ERR_NOT_INITIALIZED	Corruption found. A refresh is required.

◆ **RM\_VEE\_FLASH\_Format()**

```
fsp_err_t RM_VEE_FLASH_Format ( rm_vee_ctrl_t *const p_api_ctrl, uint8_t const *const p_ref_data )
```

Start a manual format operation.

Implements `rm_vee_api_t::format`

**Return values**

FSP_SUCCESS	Successful.
FSP_ERR_NOT_OPEN	The module has not been opened.
FSP_ERR_IN_USE	Last API call still executing.
FSP_ERR_PE_FAILURE	This error indicates that a flash programming, erase, or blankcheck operation has failed
FSP_ERR_ASSERTION	An input parameter is NULL.
FSP_ERR_TIMEOUT	Flash write timed out (Should not be possible when flash bgo is used).
FSP_ERR_NOT_INITIALIZED	Corruption found. A refresh is required.

◆ **RM\_VEE\_FLASH\_CallbackSet()**

```
fsp_err_t RM_VEE_FLASH_CallbackSet ( rm_vee_ctrl_t *const p_api_ctrl, void(*) (rm_vee_callback_args_t *) p_callback, void const *const p_context, rm_vee_callback_args_t *const p_callback_memory )
```

Updates the user callback with the option to provide memory for the callback argument structure.

Implements `rm_vee_api_t::callbackSet`.

**Return values**

FSP_SUCCESS	Callback updated successfully.
FSP_ERR_ASSERTION	A required pointer is NULL.
FSP_ERR_NOT_OPEN	The control block has not been opened.
FSP_ERR_NO_CALLBACK_MEMORY	<code>p_callback</code> is non-secure and <code>p_callback_memory</code> is either secure or NULL.

### ◆ RM\_VEE\_FLASH\_Close()

```
fsp_err_t RM_VEE_FLASH_Close ( rm_vee_ctrl_t *const p_api_ctrl)
```

Closes the Flash driver and VEE driver.

Implements `rm_vee_api_t::close`

#### Return values

FSP_SUCCESS	Successful.
FSP_ERR_NOT_OPEN	The module has not been opened.
FSP_ERR_ASSERTION	An input parameter is NULL.

### ◆ RM\_VEE\_FLASH\_VersionGet()

```
fsp_err_t RM_VEE_FLASH_VersionGet ( fsp_version_t *const p_version)
```

Get the driver version based on compile time macros.

Implements `rm_vee_api_t::versionGet`

#### Return values

FSP_SUCCESS	Successful.
FSP_ERR_ASSERTION	p_version is NULL.

## 4.2.74 AWS Device Provisioning

### Modules

AWS Device Provisioning example software.

## Overview

### Terminology

The terminology defined below will be used in the following sections.

Term	Description
Service Provider	Entity that provides the cloud infrastructure and associated services, for example, AWS/Azure.
Device Manufacturer	Entity that provides the MCU, for example,



	Renesas.
OEM	Entity that uses the MCU to create a product.
Customer	End user of OEM product.

## Device ID

For systems that intend to use Public Key Certificate (PKC), the Device ID is in the form of a key pair (RSA or ECC). A PKC comprises of a **public key**, metadata, and finally a signature over all that. This signature is generated by the entity that issues the certificate and is known as a CA (Certificate Authority). The most common format for a public certificate is the [X.509 format](#) which is typically PEM (base 64) encoded such that the certificate is human-readable. It can also be DER encoded which is binary encoding and thus not human readable. The **public key** portion of the Device ID is used for the Device Certificate.

## Provisioning

Device Provisioning refers to the process by which a service provider links a certificate to a Device ID and thus a device. Depending on the provisioning model, an existing certificate from the device may be used or a new one will be issued at this stage. Provisioning (also referred to as Registration) occurs with respect to a particular service provider, for example, AWS or Azure. It is necessary that the certificate is issued by the service provider or a CA known to those providers. When a device is provisioned with AWS for example, the AWS IoT service associates the Device ID (and thus the device) with a specific certificate. The certificate will be programmed into the device and for all future transactions with AWS, the certificate will be used as the means of identifying the device. The public and private key are also stored on the MCU.

## Provisioning Models

Provisioning services vary between [service providers](#). There are essentially three general provisioning models.

1. Provisioning happens on the production line. This requires the provisioning Infrastructure to be present on the production line. This is the most secure model, but is expensive.
2. Devices are programmed with a shared credential that is linked into the code at build time and the provisioning occurs when a customer uses the device for the first time. The shared credential and a unique device serial number are used to uniquely identify the device during the provisioning process. So long as the product only has the shared credential, it will only operate with limited (as defined by certificate policy) functionality. Once the provisioning is done, then the device will be fully functional. This is the most common use case for consumer products where no sensitive information is being transmitted. AWS provides an [example](#) of this model.
3. Devices have no identity programmed in the factory; provisioning occurs through some other device like a smartphone which is already trusted by the service provider.

In all these cases, the Device Identity

1. Is unique to the device
2. Must have restricted access within the device
3. Can be used to issue more than one certificate and the certificates themselves have to be updatable in the field.

AWS uses the PKCS11 API to erase, store and retrieve certificates. These PKCS11 functions (Write, Read and Erase) are separated out into a Physical Abstraction Layer (PAL) which the OEM/Device Manufacturer is expected to implement for the type of memory that they intend to use. The internal

rm\_aws\_pkcs11\_pal module implements these requirements on RA MCU data flash.

## AWS Provisioning Example

AWS provides an **example** implementation to support device provisioning. This implementation uses the PKCS11 API to store device credentials into the PKCS11 defined memory. The implementation (aws\_dev\_mode\_key\_provisioning.c) exposes two functions:

1. vDevModeKeyProvisioning()
2. vAlternateKeyProvisioning()

Both of these functions require that the device credentials be provided in PEM format. Using either of these example functions as is in production is not recommended; but vAlternateKeyProvisioning() provides more flexibility because of the ability to provide credentials as arguments.

Credentials can be created as follows:

- [Create your own CA](#) and use that to generate the device certificate. This CA will have to be registered with the service provider with which the product will be used, for example [Register your CA with AWS](#).
- [Use AWS](#) to generate the device certificate.

## Examples

### Basic Example

This is a basic example of provisioning a device using the AWS demo implementation.

```
#define keyCLIENT_CERTIFICATE_PEM \
"-----BEGIN CERTIFICATE-----\n" \
"MIIDETCCAfkCFHwd2yn8zn5qB2ChYUT9Mvbi9Xp1MA0GCSqGS Ib3DQEBCwUAMEUx\n" \
"CzAJBgNVBAYTAkFVMRMwEQYDVQQIDApTb211LVN0YXR1MSEwHwYDVQQKDBhJbnRl\n" \
"cm5ldCBXaWRnaXRzIFB0eSBMdGQwHhcNMkxwOTExMjU0WhcNMjAwOTExMjU0\n" \
"MjU0WjBFMQswCQYDVQQGEwJBVTEETMBEGA1UECAwKU29tZS1TdGF0ZTEhMB8GA1UE\n" \
"CgwYSW50ZXJuZXQgV2lkZ210cyBQdHkgTHRkMIIBIjANBgkqhkiG9w0BAQEFAAO\n" \
"AQ8AMIIBCgKCAQEAo8oThJXSMDo41oL7HTpC4TX8Na1BvnkFw30Av67dl/oZDjVA\n" \
"iXPnZkhVppLnj++0/Oed0M7UwNUO2nurQt6yTYrvW7E8ZPjAlC7ueJcGYZhOaVv2\n" \
"bhSmigjFQru21w5odSuYy5+22CCgxf58nrRCo5Bk+GwWgZmcrxe/BzutRHQ7X4x\n" \
"dYJhyhBOi2R1Kt8XsbuWilfgfkVhkhVklFeKqiypdQM6cnPW0/G4DyW34jOXzzEM\n" \
"FLWvQOQLCKUZogjJBnFdbx8o0OwMkYcChbV7gqPE6cw0Zy26Cv1LQiINyonLPbNT\n" \
"64sS/ZBGPZFOPJmb4tG2nipYgZ1h0/r++jCbWIDAQABMA0GCSqGS Ib3DQEBCwUA\n" \
"A4IBAQCdqg59ubdRY9EiV3bleKXeqG7+8HgBHdm0X9dgq10nD37p00YLyZLE9NM\n" \
"066G/VcflGrx/Nzw+/UuI7/UuBbBS/3ppHRnsZqBI18nnr/ULrFQy8z3vKtL1q3C\n" \
"DxabjPONlP02keJeTTA71N/RCeMwJoa8i0XKXGdu/hQo6x4n+Gq73fEiGCl99xsc\n" \
```

```
"4tIO4yPS4lv+uXBzEUzoEy0CLlIkiDesnT5lLeCyPmUNoU89HU95IusZT7kygCHHD\n" \  
"72amlic3X8PKc268KT3ilr3VMhK67C+iIikfrM5AiU+oOIRrIHSC/p0RigJg3rXA\n" \  
"GBIRHvt+OYF9fDeG7U4QDJNCfGW+\n" \  
"-----END CERTIFICATE-----"  
#define keyCLIENT_PRIVATE_KEY_PEM \  
"-----BEGIN RSA PRIVATE KEY-----\n" \  
"MIIEowIBAAKCAQEAo8oThJXSMDo4loL7HTpC4TX8NalBvnkFw30Av67dl/oZDjVA\n" \  
"iXpNzkhVppLnj++0/Oed0M7UwNUO2nurQt6yTYrvW7E8ZPjAlC7ueJcGYZhOaVv2\n" \  
"bhSmigjFQru2lw5odSuYy5+22CCgxf58nrRCo5Bk+GwWgZmcrxe/BzutRHQ7X4x\n" \  
"dYJhyhBOi2R1Kt8XsbuWilfgfkVhkhVklFeKqiypdQM6cnPWo/G4DyW34jOXzzEM\n" \  
"FLWvQOQLCKUZogjJBnFdbx8o0OwMkYCChbV7gqPE6cw0Zy26CvLLQiINyonLPbNT\n" \  
"c64sS/ZBGPZFOPJmb4tG2nipYgZ1hO/r++jCbWIDAQABAoIBAQCGR2hC/ZVJhqiM\n" \  
"c2uuJZKpElpIIBBPOobZwwS3IYR4UUjzVgMn7Ubbmxf1LXD8lzfZU4YVp0vTH5lC\n" \  
"07qvYuXpHqtnj+GEok837VYctUY9AuHeDM/2paV3awNV15E1PFGLJd3pqnH7tJw6\n" \  
"VBZBDiGNnt1agN/UnoSlmfvpU0r8VGPXCBNxe3JY5QyBJPIlwF4LcxRI+eYmr7Ja\n" \  
"/cjn97DZotgz4B7gUNu8XIEkUOTwPabZINY1zcLWiXTMA+8qTniPVk653h14Xqt4\n" \  
"4o4D4YCTpwJcmxSV1m21/6+uyuXr9SIKAE+Ys2cYLA46x+rwLaW5fUoQ5hHa0Ytb\n" \  
"RYJ4SrtBAoGBANwtwle69N0hq5xDpckSbNGubIeG8P4mBhGkJxIqYoqugGLMDiGX\n" \  
"4bltrjr2TPWaxTo3pPavLJiBMIsENA5KU+c/r0jLkxgEp9MIVJrtNgkCiDQqogBG\n" \  
"j4IjL2iQwXoLCqk2tx/dh9Mww+7SETE7EPNrv4UrYaGN5AEvpf5W+NHPAoGBAMQ6\n" \  
"wVa0Mx1PlA4enY2rfe3WXP8bzjleSOWr75JXqG2WbPC0/cszwbyPWOEqRpBZfvD\n" \  
"QFkKx06xp1C09XwiQanr2gDucYXHeEKg/9iuJV1UkMQp95ojlhtSXdrZV7/14pmN\n" \  
"fpB2vcAptX/4gY4tDrWMO08JNnrje7duC+rmmk1hAoGAS4L0QLCNB/h2JOq+Uuhn\n" \  
"/FGfmOVfFPFrA6D3DbxcxpWUWVwzSLvb0SophrzxbfEKyau7V5KbDp7ZSU/IC20\n" \  
"KOyggjSEkAkDi7fjrrTRW/Cgg6g6G4YIOBO4qCtHdDbwJMHNdk6096qw5EzS67qLp\n" \  
"Apz5OZ5zChySjri/+HnTxJECgYBysGSP6IJ3fytplTtAshnU5JU2Bwpi3ViBoXe\n" \  
"bndilajWhvJO8dEqBB5OfAcCF0y6TnWt1T8oH2lLHnjcNKlsRw0Dvllbdloylybx\n" \  
"3da41dRG0sCEetoflMB7nHdDLt/DZDnoKtVvyFG6gfp47utn+Ahgn+Zp6K+46J3eP\n" \  
"s3g8AQKBgE/PJiaF8pbBXaZOuwRRA9GOMsbDIF6+jBYTYp4L9wk4+LZArKtyI+4k\n" \  
"Md2DUvHwMC+ddOtKqjYnLm+V5cSbvU7aPvBZtwxghzTUDcf7EvnA3V/bQBh3R0z7\n" \  
"pVsxTyGRmBSeLdbUWACUbX9LXdpuarPAJ59daWmP3mBEVmWdzUw\n" \  
"-----END RSA PRIVATE KEY-----"  
void device_provisioning_example (void)  
{
```

```
/* Initialize the crypto hardware acceleration. */
mbedtls_platform_setup(NULL);
    ProvisioningParams_t params;
/* Provision device with provided credentials. The provided credentials are written
to data flash.
* In production, the credentials can be provided over a comms channel instead of
being linked into the image.
* The same example provisioning function, vAlternateKeyProvisioning, can be used in
that case. */
    params.pucClientPrivateKey      = (uint8_t *) keyCLIENT_PRIVATE_KEY_PEM;
    params.pucClientCertificate     = (uint8_t *) keyCLIENT_CERTIFICATE_PEM;
    params.ulClientPrivateKeyLength = 1 + strlen((const char *)
params.pucClientPrivateKey);
    params.ulClientCertificateLength = 1 + strlen((const char *)
params.pucClientCertificate);
    params.pucJITPCertificate       = NULL;
    params.ulJITPCertificateLength  = 0;
    vAlternateKeyProvisioning(&params);
}
```

## Limitations

The provisioning code is an example provided by AWS. It must be modified to meet product requirements.

### 4.2.75 AWS MQTT

#### Modules

This module provides the AWS MQTT integration documentation.

## Overview

The AWS MQTT library can connect to either AWS or a third party MQTT broker such as [Mosquitto](#). The documentation for the library can be found on the [AWS IoT Device SDK C: MQTT](#) website.

## Features

- MQTT connections over TLS to an AWS IoT Endpoint or Mosquitto server
- Unsecure MQTT connections to Mosquitto servers. This is not recommended for production and should only be done to a local server for testing.

# Configuration

## Memory Usage

The AWS MQTT library relies heavily on dynamic memory allocation for thread/task creation as well as other uses. Depending on the configuration it may be required to provide as much as 110k heap. To decrease this it is recommended to tweak the thread stack configuration values based on usage. Notable values are:

## AWS IoT Common

- IoT Thread Default Stack Size
- IoT Network Receive Task Stack Size

## FreeRTOS Thread

- General|Minimal Stack Size

## FreeRTOS Plus TCP

- Stack size in words (not bytes)

# Usage Notes

The AWS MQTT library utilizes a system taskpool to queue up messages. This system task pool must be created before calling into the MQTT library. `iot_init.c` has been provided for easy initialization of this taskpool via `lotSdk_Init()`.

The AWS MQTT Demo has been provided to easily demonstrate MQTT functionality. An example of initializing the system taskpool and running the MQTT demo has been provided below.

## Limitations

- `aws_clientcredential.h` and `aws_clientcredential_keys.h` need to be added manually.
- The IoT Thread must have a higher priority than the Network Receive Thread.
- MbedTLS must be initialized and key provisioning must be done before starting a secure connection. Refer to [AWS Secure Sockets](#).

## Examples

### Non-secure connection to a Mosquitto server

```
#define IOT_LOG_STACK_SIZE (256)

const uint8_t g_ip_address[4] = {169, 254, 57, 49};
const uint8_t g_net_mask[4] = {255, 255, 0, 0};
const uint8_t g_gateway_address[4] = {169, 254, 57, 49};
```

```
const uint8_t g_dns_address[4] = {8, 8, 8, 8};
const uint8_t g_mac_address[6] = {0x66, 0x66, 0x66, 0x66, 0x66, 0x66};
void mqtt_non_secure_example ()
{
    bool connect_to_aws = false;
    /* Initialize the crypto hardware acceleration. */
    mbedtls_platform_setup(NULL);
    xLoggingTaskInitialize(IOT_LOG_STACK_SIZE, 1, 10);
    /* Start up the network stack. */
    FreeRTOS_IPInit(g_ip_address, g_net_mask, g_gateway_address, g_dns_address,
g_mac_address);
    while (pdFALSE == FreeRTOS_IsNetworkUp())
    {
        vTaskDelay(1);
    }
    Socket_t socket = SOCKETS_Socket(SOCKETS_AF_INET, SOCKETS_SOCK_STREAM,
SOCKET_IPPROTO_TCP);
    if (SOCKET_INVALID_SOCKET == socket)
    {
        /* Could not create socket. */
        __BKPT(0);
    }
    const IotNetworkServerInfo_t serverInfo =
    {
        .pHostName = "192.168.0.100",
        .port      = 1883
    };
    IotSdk_Init();
    RunMqttDemo(connect_to_aws, "renesas-iot-demo", (void *) &serverInfo, NULL,
&IotNetworkAfr);
}
```

## Secure connection to a Mosquitto server

*Note*

*MbedTLS must be initialized and key provisioning must be done before starting a secure connection. Refer to [AWS Secure Sockets](#).*

```
#define keyCLIENT_CERTIFICATE_PEM \
    "-----BEGIN CERTIFICATE-----\n" \
    "MIIDETCCAfKCFHwd2yn8zn5qB2ChYUT9Mvbi9Xp1MA0GCSqGS Ib3DQEBCwUAMEUx\n" \
    "CzAJBgNVBAYTAKFVMRMwEQYDVQQIDApTb211LVN0YXR1MSEwHwYDVQQKBhJbnRl\n" \
    "cm5ldCBXaWRnaXRzIFB0eSBMdGQwHhcNMjkwOTExMjE0WhcNMjAwOTExMjE0\n" \
    "MjU0WjBFMQswCQYDVQQGEwJBVTEtMBEGA1UECAwKU29tZS1TdGF0ZTEhMB8GA1UE\n" \
    "CgwYSW50ZXJuZXQgV2lkZ2l0cyBQdHkgTHRkMIIBIjANBgkqhkiG9w0BAQEFAAO\n" \
    "C\n" \
    "AQ8AMIIBCgKCAQEAo8oThJXSMDo41oL7HTpC4TX8NalBvnkFw30Av67dl/oZDjVA\n" \
    "iXpNzkhVppLnj++/Oed0M7UwNUO2nurQt6yTYrvW7E8ZPjAlC7ueJcGYZhOaVv2\n" \
    "bhSmigjFQru2lw5odSuYy5+22CCgxf58nrRCo5Bk+GwWgZmcrxe/BzutRHQ7X4x\n" \
    "dYJhyhBOi2R1Kt8XsbuWilfgfkVhkhVklFeKqiypdQM6cnPwo/G4DyW34jOXzzEM\n" \
    "FLWvQOQLCKUZOGjJBnFdbx8o0OwMkYcChbV7gqPE6cw0Zy26Cv1LQiINyonLPbNT\n" \
    "c64sS/ZBGPZFOPJmb4tG2nipYgZlh0/r++jCbWIDAQABMA0GCSqGS Ib3DQEBCwUA\n" \
    "A4IBAQCdq59ubdRY9EiV3bleKXeqG7+8HgBHdm0X9dgq10nD37p00YLyuZLE9NM\n" \
    "066G/VcflGrx/Nzw+/UuI7/UuBbBS/3ppHRnsZqBI18nnr/ULrFQy8z3vKtLlq3C\n" \
    "DxabjPONlPO2keJeTTA71N/RCEMwJoa8i0XKXGdu/hQo6x4n+Gq73fEiGCl99xsc\n" \
    "4tIO4yPS4lv+uXBzEUzoEy0CLikiDesnT5lLeCyPmUNoU89HU95IusZT7kygCHHd\n" \
    "72amlic3X8PKc268KT3ilr3VMhK67C+iIikfrM5AiU+oOIRrIHSC/p0RigJg3rXA\n" \
    "GBIRHvt+OYF9fDeG7U4QDJNcfGW+\n" \
    "-----END CERTIFICATE-----"

#define keyCLIENT_PRIVATE_KEY_PEM \
    "-----BEGIN RSA PRIVATE KEY-----\n" \
    "MIIEowIBAAKCAQEAo8oThJXSMDo41oL7HTpC4TX8NalBvnkFw30Av67dl/oZDjVA\n" \
    "iXpNzkhVppLnj++/Oed0M7UwNUO2nurQt6yTYrvW7E8ZPjAlC7ueJcGYZhOaVv2\n" \
    "bhSmigjFQru2lw5odSuYy5+22CCgxf58nrRCo5Bk+GwWgZmcrxe/BzutRHQ7X4x\n" \
    "dYJhyhBOi2R1Kt8XsbuWilfgfkVhkhVklFeKqiypdQM6cnPwo/G4DyW34jOXzzEM\n" \
    "FLWvQOQLCKUZOGjJBnFdbx8o0OwMkYcChbV7gqPE6cw0Zy26Cv1LQiINyonLPbNT\n" \
    "c64sS/ZBGPZFOPJmb4tG2nipYgZlh0/r++jCbWIDAQABAoIBAQCGR2hC/ZVJhqIM\n" \
    "c2uuZJKpElpIIBBPOObZwwS3IYR4UUjzVgMn7Ubbmxf1LXD8lzfZU4YVp0vTH5lC\n" \
    "07qvYuXpHqtnj+GEok837VYctUY9AuHeDM/2paV3awNV15E1PFG1Jd3pqnH7tJw6\n" \
    "VBZBDiGNnt1agN/UnoSlMfvpU0r8VGPXCbnxe3JY5QyBJPI1wF4LcxRI+eYmr7Ja\n" \
    "/cJn97DZotgz4B7gUNu8XIEkUOTwPabZINylzCLWiXTMA+8qTniPVk653h14Xqt4\n"
```

```

"4o4D4YCTpwJcmxSVlm2l/6+uyuXr9SIKAE+Ys2cYLA46x+rwLaW5fUoQ5hHa0Ytb\n" \
"RYJ4SrtBAoGBANWtwlE69N0hq5xDpckSbnGubIeG8P4mBhGkJxIqYoqUGLMDiGX\n" \
"4bltrjr2TPWaxTo3pPavLJiBmIsENA5KU+c/r0jLkxgEp9MIVJrtNgkCiDQqogBG\n" \
"j4IjL2iQwXoLCqk2tx/dh9Mww+7SETE7EPNrv4UrYaGN5AEvpf5W+NHPAoGBAMQ6\n" \
"wVa0Mx1PlA4enY2rfe3WXP8bzjleSOWr75JXqG2WbPC0/cszwbyPWOEqRpBZfvD/\n" \
"QFkKx06xp1C09XwiQanr2gDucYXHeEKg/9iuJV1UkMQp95ojlhtSXdRZV7/14pmN\n" \
"fpB2vcAptX/4gY4tDrWMO08JNnRjE7duC+rmmk1hAoGAS4L0QLCNB/h2JOq+Uuhn\n" \
"/FGfmOVfFPFrA6D3DbxcxpWUWVwzSLvb0SOpHryzxbfEKyau7V5KbDp7ZSU/IC20\n" \
"KOyggjSekAkDi7fjrrTRW/Cgg6g6G4YIOBO4qCtHdDbwJMHndk6096qw5EzS67qLp\n" \
"Apz5OZ5zChySjri/+HnTxJECgYBysGSP6IJ3fytplTtAshnU5JU2BWpi3ViBoXoE\n" \
"bndilajWhvJO8dEqBB5OfAcCF0y6TnWt1T8oH21LHnjcNKlsRw0Dv1lbdloylybx\n" \
"3da41dRG0sCEtoflMB7nHdDLt/DZDnoKtVvyFG6gfp47utn+Ahgn+Zp6K+46J3eP\n" \
"s3g8AQKBgE/PJiaF8pbBXaZOUwRRA9GOMSbDIF6+jBYTYp4L9wk4+LZArKtyI+4k\n" \
Md2DUvHwMC+ddOtKqjYnLm+V5cSbvU7aPvBZtwxghzTUDcf7EvnA3V/bQBh3R0z7\n" \
pVsxTyGRmBSeLdbUWACUbx9LXdpuDarPAJ59daWmP3mBEVmwDzUw\n" \
"-----END RSA PRIVATE KEY-----"

static char SERVER_CERTIFICATE_PEM[] = "-----BEGIN CERTIFICATE-----\n"
"example_certificate_formatting\n"
"-----END CERTIFICATE-----";

static char CLIENT_CERTIFICATE_PEM[] = "-----BEGIN CERTIFICATE-----\n"
"example_certificate_formatting\n"
"-----END CERTIFICATE-----";

static char CLIENT_KEY_PEM[] = "-----BEGIN RSA PRIVATE KEY-----\n"
"example_certificate_formatting\n"
"-----END RSA PRIVATE KEY-----";

void mqtt_secure_example ()
{
    bool connect_to_aws = false;

    /* Initialize the crypto hardware acceleration. */
    mbedtls_platform_setup(NULL);

    xLoggingTaskInitialize(IOT_LOG_STACK_SIZE, 1, 10);

    ProvisioningParams_t params;

    /* Write the keys into a secure region in data flash. */
    params.pucClientPrivateKey = (uint8_t *) keyCLIENT_PRIVATE_KEY_PEM;

```



```
params.pucClientCertificate      = (uint8_t *) keyCLIENT_CERTIFICATE_PEM;
params.ulClientPrivateKeyLength = 1 + strlen((const char *)
params.pucClientPrivateKey);
params.ulClientCertificateLength = 1 + strlen((const char *)
params.pucClientCertificate);
params.pucJITPCertificate       = NULL;
params.ulJITPCertificateLength  = 0;
vAlternateKeyProvisioning(&params);
/* Start up the network stack. */
FreeRTOS_IPInit(g_ip_address, g_net_mask, g_gateway_address, g_dns_address,
g_mac_address);
while (pdFALSE == FreeRTOS_IsNetworkUp())
{
    vTaskDelay(1);
}
Socket_t socket = SOCKETS_Socket(SOCKETS_AF_INET, SOCKETS SOCK_STREAM,
SOCKET_IPPROTO_TCP);
if (SOCKET_INVALID_SOCKET == socket)
{
    /* Could not create socket. */
    __BKPT(0);
}
const IotNetworkServerInfo_t serverInfo =
{
    .pHostName = "192.168.0.100",
    .port      = 8883
};
const IotNetworkCredentials_t afrCredentials =
{
    .pAlpnProtos      = NULL,
    .maxFragmentLength = 1400,
    .disableSni       = true,
    .pRootCa          = SERVER_CERTIFICATE_PEM,
    .rootCaSize       = sizeof(SERVER_CERTIFICATE_PEM),
```

```

    .pClientCert      = CLIENT_CERTIFICATE_PEM,
    .clientCertSize  = sizeof(CLIENT_CERTIFICATE_PEM),
    .pPrivateKey     = CLIENT_KEY_PEM,
    .privateKeySize  = sizeof(CLIENT_KEY_PEM),
};

IotSdk_Init();

RunMqttDemo(connect_to_aws, "renesas-iot-demo", (void *) &serverInfo, (void *)
&afrCredentials, &IotNetworkAfr);
}

```

## 4.2.76 Wifi Middleware (rm\_wifi\_onchip\_silex)

### Modules

#### Functions

fsp\_err\_t rm\_wifi\_onchip\_silex\_open (wifi\_onchip\_silex\_cfg\_t const \*const p\_cfg)

fsp\_err\_t rm\_wifi\_onchip\_silex\_version\_get (fsp\_version\_t \*const p\_version)

fsp\_err\_t rm\_wifi\_onchip\_silex\_close ()

fsp\_err\_t rm\_wifi\_onchip\_silex\_connect (const char \*p\_ssid, uint32\_t security, const char \*p\_passphrase)

fsp\_err\_t rm\_wifi\_onchip\_silex\_mac\_addr\_get (uint8\_t \*p\_macaddr)

fsp\_err\_t rm\_wifi\_onchip\_silex\_scan (WIFIScanResult\_t \*p\_results, uint32\_t maxNetworks)

fsp\_err\_t rm\_wifi\_onchip\_silex\_ping (uint8\_t \*p\_ip\_addr, uint32\_t count, uint32\_t interval\_ms)

fsp\_err\_t rm\_wifi\_onchip\_silex\_ip\_addr\_get (uint8\_t \*p\_ip\_addr)

fsp\_err\_t rm\_wifi\_onchip\_silex\_avail\_socket\_get (uint32\_t \*p\_socket\_id)

fsp\_err\_t rm\_wifi\_onchip\_silex\_socket\_status\_get (uint32\_t socket\_no, uint32\_t \*p\_socket\_status)

fsp\_err\_t rm\_wifi\_onchip\_silex\_socket\_create (uint32\_t socket\_no, uint32\_t type, uint32\_t ipversion)

fsp_err_t	<a href="#">rm_wifi_onchip_silex_tcp_connect</a> (uint32_t socket_no, uint32_t ipaddr, uint32_t port)
int32_t	<a href="#">rm_wifi_onchip_silex_tcp_send</a> (uint32_t socket_no, const uint8_t *p_data, uint32_t length, uint32_t timeout_ms)
int32_t	<a href="#">rm_wifi_onchip_silex_tcp_recv</a> (uint32_t socket_no, uint8_t *p_data, uint32_t length, uint32_t timeout_ms)
int32_t	<a href="#">rm_wifi_onchip_silex_tcp_shutdown</a> (uint32_t socket_no, uint32_t shutdown_channels)
fsp_err_t	<a href="#">rm_wifi_onchip_silex_socket_disconnect</a> (uint32_t socket_no)
fsp_err_t	<a href="#">rm_wifi_onchip_silex_disconnect</a> ()
fsp_err_t	<a href="#">rm_wifi_onchip_silex_dns_query</a> (const char *p_textstring, uint8_t *p_ip_addr)
fsp_err_t	<a href="#">rm_wifi_onchip_silex_socket_connected</a> (fsp_err_t *p_status)
void	<a href="#">rm_wifi_onchip_silex_uart_callback</a> (uart_callback_args_t *p_args)
Socket_t	<a href="#">SOCKETS_Socket</a> (int32_t IDomain, int32_t IType, int32_t IProtocol)
int32_t	<a href="#">SOCKETS_Connect</a> (Socket_t xSocket, SocketsSockaddr_t *pxAddress, Socklen_t xAddressLength)
int32_t	<a href="#">SOCKETS_Recv</a> (Socket_t xSocket, void *pvBuffer, size_t xBufferLength, uint32_t ulFlags)
int32_t	<a href="#">SOCKETS_Send</a> (Socket_t xSocket, const void *pvBuffer, size_t xDataLength, uint32_t ulFlags)
int32_t	<a href="#">SOCKETS_Shutdown</a> (Socket_t xSocket, uint32_t ulHow)
int32_t	<a href="#">SOCKETS_Close</a> (Socket_t xSocket)
int32_t	<a href="#">SOCKETS_SetSockOpt</a> (Socket_t xSocket, int32_t ILevel, int32_t IOptionName, const void *pvOptionValue, size_t xOptionLength)
uint32_t	<a href="#">SOCKETS_GetHostByName</a> (const char *pcHostName)
BaseType_t	<a href="#">SOCKETS_Init</a> (void)
WIFIReturnCode_t	<a href="#">WIFI_On</a> (void)
WIFIReturnCode_t	<a href="#">WIFI_Off</a> (void)

WIFIReturnCode_t	<a href="#">WIFI_ConnectAP</a> (const WIFINetworkParams_t *const pxNetworkParams)
WIFIReturnCode_t	<a href="#">WIFI_Disconnect</a> (void)
WIFIReturnCode_t	<a href="#">WIFI_Reset</a> (void)
WIFIReturnCode_t	<a href="#">WIFI_Scan</a> (WIFIScanResult_t *pxBuffer, uint8_t ucNumNetworks)
WIFIReturnCode_t	<a href="#">WIFI_Ping</a> (uint8_t *puclPAddr, uint16_t usCount, uint32_t ullIntervalMS)
WIFIReturnCode_t	<a href="#">WIFI_GetIP</a> (uint8_t *puclPAddr)
WIFIReturnCode_t	<a href="#">WIFI_GetMAC</a> (uint8_t *pucMac)
WIFIReturnCode_t	<a href="#">WIFI_GetHostIP</a> (char *pcHost, uint8_t *puclPAddr)
BaseType_t	<a href="#">WIFI_IsConnected</a> (void)

## Detailed Description

Wifi and Socket implementation using the Silex SX-ULPGN WiFi module on RA MCUs.

## Overview

This Middleware module supplies an implementation for the [FreeRTOS Secure Sockets and WiFi interfaces](#) using the Silex SX-ULPGN module.

The SX-ULPGN is a low-power, compact IEEE 802.11b/g/n 2.4GHz 1x1 Wireless LAN module equipped with the Qualcomm® QCA4010 Wireless SOC. The module comes readily equipped with radio certification for Japan, North America and Europe. More information about this module can be found at the [Silex Web Site](#)

## Features

The WiFi Onchip Silex Middleware driver supplies these features:

- Supports connect/disconnect to a b/g/n (2.4GHz) WiFi Access Point using Open, WPA, and WPA2 security. Encryption types can be either TKIP, or CCMP(AES).
- Supports retrieval of the module device MAC address.
- Once connected you can acquire the assigned module device IP.
- Supports a WiFi network scan capability to get a list of local Access Points.
- Supports a Ping function to test network connectivity.
- Supports a DNS Query call to retrieve the IPv4 address of a supplied URL.
- Supports a BSD style Secure Socket interface.
- Drive supports 1 or 2 UARTs for interfacing with the SX-ULPGN module. The second UART is considered optional.

## Configuration

## Build Time Configurations for rm\_wifi\_onchip\_silex

The following build time configurations are defined in fsp\_cfg/rm\_wifi\_onchip\_silex\_cfg.h:

Configuration	Options	Default	Description
Parameter Checking	<ul style="list-style-type: none"> <li>• Default (BSP)</li> <li>• Enabled</li> <li>• Disabled</li> </ul>	Default (BSP)	If selected code for parameter checking is included in the build.
Number of supported socket instances	Refer to the RA Configuration tool for available options.	1	Enable number of socket instances
Size of RX buffer for socket	Manual Entry	4096	
Size of TX buffer for CMD Port	Manual Entry	1500	
Size of RX buffer for CMD Port	Manual Entry	3000	
Semaphore maximum timeout	Manual Entry	10000	
Number of retries for AT commands	Manual Entry	10	
Module Reset Port	Refer to the RA Configuration tool for available options.	06	Specify the module reset pin port for the MCU.
Module Reset Pin	Refer to the RA Configuration tool for available options.	03	Specify the module reset pin for the MCU.

## Configurations for Middleware > WiFi > WiFi Onchip Silex Driver using r\_sci\_uart

Configuration	Options	Default	Description
---------------	---------	---------	-------------

Note: When configuring the two UART components you will need to make sure that DTC and FIFO are both enabled in the UART configuration. Also, you must create both TX/RX DTC components per UART.

Note: If you wish to use flow control then you must enable flow control in the RA Configuration editor. This can be found in the UART setting. It is advantageous to use flow control all the time since it allows the hardware to gate the flow of data across the serial bus. Without hardware flow control for faster data rate you will most likely see an overflow condition between MCU and the module device.

Note: Higher baud rates are supported in the RA Configuration editor and should be changed in the first UART configuration. There is no need to change the second UART baud rate since it is only used as an AT command channel.

Note: It is a good idea to also enable the FIFO in the UART configuration settings if you plan to use higher baud rates.

## Interrupt Configuration

Refer to [Serial Communications Interface \(SCI\) UART \(r\\_sci\\_uart\)](#). [R\\_SCI\\_UART\\_Open\(\)](#) is called by [Wifi Middleware \(rm\\_wifi\\_onchip\\_silex\)](#).

## Clock Configuration

Refer to [Serial Communications Interface \(SCI\) UART \(r\\_sci\\_uart\)](#).

## Pin Configuration

Refer to [Serial Communications Interface \(SCI\) UART \(r\\_sci\\_uart\)](#). [R\\_SCI\\_UART\\_Open\(\)](#) is called by [Wifi Middleware \(rm\\_wifi\\_onchip\\_silex\)](#)

# Usage Notes

## Limitations

- WiFi AP connections do not currently support WEP security.
- When operating with a single UART only single socket connections are possible. To support multiple sockets two UART channels must be connected to the module. When using the Renesas-provided SX-ULPGN PMOD board the second UART channel is on pins 9 and 10 of the PMOD header.
- Network connection parameters SSID and Passphrase for the Access Point can not contain any commas. This is a current limitation of the Silex module firmware. The [rm\\_wifi\\_onchip\\_silex\\_connect\(\)](#) function will return an error if a comma is detected.

# Examples

## Basic Example

This is a basic example of minimal use of WiFi Middleware in an application.

```
void wifi_onchip_basic_example (void)
{
    WIFIReturnCode_t    wifi_err;
    WIFINetworkParams_t net_params;
    SocketsSockaddr_t  addr          = {0};
    int32_t             number_bytes_rx = 0;
    int32_t             number_bytes_tx = 0;
    memset(scan_data, 0, sizeof(WIFIScanResult_t) * MAX_WIFI_SCAN_RESULTS);
    memset(g_socket_recv_buffer, 0, sizeof(uint8_t) * SX_WIFI_SOCKET_RX_BUFFER_SIZE);
    /* Open connection to the Wifi Module */
    wifi_err = WIFI_On();
    if (wifi_err)
    {
```

```
    handle_error((fsp_err_t) wifi_err);
}

/* Setup Access Point connection parameters */
net_params.cChannel      = 0;
net_params.pcPassword    = "password";
net_params.pcSSID        = "access_point_ssid";
net_params.ucPasswordLength = 8;
net_params.ucSSIDLength  = 17;
net_params.xSecurity     = eWiFiSecurityWPA2;

/* Connect to the Access Point */
wifi_err = WIFI_ConnectAP(&net_params);
if (wifi_err)
{
    handle_error((fsp_err_t) wifi_err);
}

/* Get address assigned by AP */
uint8_t ip_address_device[4] = {0};
wifi_err = WIFI_GetIP(&ip_address_device[0]);
if (wifi_err)
{
    handle_error((fsp_err_t) wifi_err);
}

/* Ping an address accessible on the network */
uint8_t ip_address[4] = {216, 58, 194, 174}; // NOLINT
const uint16_t ping_count = 3;
const uint32_t intervalMS = 100;

wifi_err = WIFI_Ping(&ip_address[0], ping_count, intervalMS);
if (wifi_err)
{
    handle_error((fsp_err_t) wifi_err);
}

/* Scan the local Wifi network for other APs */
wifi_err = WIFI_Scan(&scan_data[0], MAX_WIFI_SCAN_RESULTS);
if (wifi_err)
```

```
{
    handle_error((fsp_err_t) wifi_err);
}

/* Do a DNS Query for IP address of server */
addr.ulAddress = SOCKETS_GetHostByName("www.renesas.com");
addr.usPort     = SOCKETS_htons(80);

/* Initialize the Socket Interface */
BaseType_t sock_err = SOCKETS_Init();
if (sock_err != pdPASS)
{
    handle_error((fsp_err_t) sock_err);
}

/* Create a socket instance */
Socket_t socket1 = SOCKETS_Socket(SOCKETS_AF_INET, SOCKETS SOCK_STREAM,
SOCKET_IPPROTO_TCP);
if (socket1 == NULL)
{
    handle_error((fsp_err_t) !socket1);
}

/* Connect to an server using address */
sock_err = SOCKETS_Connect(socket1, &addr, sizeof(SocketsSockaddr_t));
if (sock_err)
{
    handle_error((fsp_err_t) sock_err);
}

/* Send a HTTP Get call to server */
number_bytes_tx = SOCKETS_Send(socket1, HTTP_GET_string, strlen(HTTP_GET_string),
0);
if (0 >= number_bytes_tx)
{
    handle_error((fsp_err_t) ERROR_OCCURED);
}

/* Receive the HTTP GET call reply */
number_bytes_rx = SOCKETS_Recv(socket1, g_socket_recv_buffer,
```



```

SX_WIFI_SOCKET_RX_BUFFER_SIZE, 0);

if (0 >= number_bytes_rx)
{
    handle_error((fsp_err_t) ERROR_OCCURED);
}

/* Close the socket connection */
SOCKETS_Close(socket1);

/* Shutdown the WIFI and Socket Interfaces */
WIFI_Off();
}

```

## Data Structures

struct [wifi\\_onchip\\_silex\\_cfg\\_t](#)

struct [ulpgn\\_socket\\_t](#)

struct [uart\\_state\\_t](#)

struct [wifi\\_onchip\\_silex\\_instance\\_ctrl\\_t](#)

## Enumerations

enum [sx\\_ulpgn\\_security\\_t](#)

enum [sx\\_ulpgn\\_socket\\_status\\_t](#)

enum [sx\\_ulpgn\\_socket\\_rw](#)

## Data Structure Documentation

### ◆ [wifi\\_onchip\\_silex\\_cfg\\_t](#)

Data Fields		
const uint32_t	num_uarts	Number of UART interfaces to use.
const uint32_t	num_sockets	Number of sockets to initialize.
const <a href="#">bsp_io_port_pin_t</a>	reset_pin	Reset pin used for module.
const <a href="#">uart_instance_t</a> *	uart_instances[WIFI_ONCHIP_SILEX_CFG_MAX_NUMBER_UART_PORTS]	SCI UART instances.

void const *	p_context	User defined context passed into callback function.
void const *	p_extend	Pointer to extended configuration by instance of interface.

#### ◆ ulpgn\_socket\_t

struct ulpgn_socket_t		
Silex ULPGN Wifi internal socket instance structure		
Data Fields		
StreamBufferHandle_t	socket_byteq_hdl	Socket stream buffer handle.
StaticStreamBuffer_t	socket_byteq_struct	Structure to hold stream buffer info.
uint8_t	socket_rcv_buff[WIFI_ONCHIP_SILEX_CFG_MAX_SOCKET_RX_SIZE]	Socket receive buffer used by byte queue.
uint32_t	socket_status	Current socket status.
uint32_t	socket_rcv_error_count	Socket receive error count.
uint32_t	socket_create_flag	Flag to determine in socket has been created.
uint32_t	socket_read_write_flag	flag to determine if read and/or write channels are active.

#### ◆ uart\_state\_t

struct uart_state_t		
Silex ULPGN Wifi SCI UART state information		
Data Fields		
SemaphoreHandle_t	uart_tei_sem	UART transmission end binary semaphore.

#### ◆ wifi\_onchip\_silex\_instance\_ctrl\_t

struct wifi_onchip_silex_instance_ctrl_t		
WIFI_ONCHIP_SILEX private control block. DO NOT MODIFY.		
Data Fields		
uint32_t	open	Flag to indicate if wifi instance has been initialized.
wifi_onchip_silex_cfg_t const *	p_wifi_onchip_silex_cfg	Pointer to initial configurations.
bsp_io_port_pin_t	reset_pin	Wifi module reset pin.
uint32_t	num_uarts	number of UARTS currently used for communication with

		module
uint32_t	tx_data_size	Size of the data to send.
uint32_t	num_creatable_sockets	Number of simultaneous sockets supported.
uint32_t	curr_cmd_port	Current UART instance index for AT commands.
uint32_t	curr_data_port	Current UART instance index for data.
uint8_t	cmd_rx_queue_buf[WIFI_ONCHIP_SILEX_CFG_CMD_RX_BUF_SIZE]	Command port receive buffer used by byte queue.
StreamBufferHandle_t	socket_byteq_hdl	Socket stream buffer handle.
StaticStreamBuffer_t	socket_byteq_struct	Structure to hold stream buffer info.
volatile uint32_t	curr_socket_index	Currently active socket instance.
uint8_t	cmd_tx_buff[WIFI_ONCHIP_SILEX_CFG_CMD_TX_BUF_SIZE]	Command send buffer.
uint8_t	cmd_rx_buff[WIFI_ONCHIP_SILEX_CFG_CMD_RX_BUF_SIZE]	Command receive buffer.
uint32_t	at_cmd_mode	Current command mode.
uint8_t	curr_ipaddr[4]	Current IP address of module.
uint8_t	curr_subnetmask[4]	Current Subnet Mask of module.
uint8_t	curr_gateway[4]	Current GATeway of module.
SemaphoreHandle_t	tx_sem	Transmit binary semaphore handle.
SemaphoreHandle_t	rx_sem	Receive binary semaphore handle.
uint8_t	last_data[WIFI_ONCHIP_SILEX_RETURN_TEXT_LENGTH]	Tailing buffer used for command parser.
uart_instance_t *	uart_instance_objects[WIFI_ONCHIP_SILEX_CFG_MAX_NUMBER_UART_PORTS]	UART instance objects.
uart_state_t	uart_state_info[WIFI_ONCHIP_SILEX_CFG_MAX_NUMBER_UART_PORTS]	UART instance state information.
ulpgn_socket_t	sockets[WIFI_ONCHIP_SILEX_CFG_NUM_CREATEABLE_SOCKETS]	Internal socket instances.

## Enumeration Type Documentation

◆ **sx\_ulpgn\_security\_t**enum `sx_ulpgn_security_t`

Silex ULPGN Wifi security types

◆ **sx\_ulpgn\_socket\_status\_t**enum `sx_ulpgn_socket_status_t`

Silex ULPGN Wifi socket status types

◆ **sx\_ulpgn\_socket\_rw**enum `sx_ulpgn_socket_rw`

Silex socket shutdown channels

**Function Documentation**◆ **rm\_wifi\_onchip\_silex\_open()**`fsp_err_t rm_wifi_onchip_silex_open ( wifi_onchip_silex_cfg_t const *const p_cfg)`

Opens and configures the WIFI\_ONCHIP\_SILEX Middleware module.

**Parameters**

[in]	p_cfg	Pointer to pin configuration structure.
------	-------	-----------------------------------------

**Return values**

FSP_SUCCESS	WIFI_ONCHIP_SILEX successfully configured.
FSP_ERR_ASSERTION	Assertion error occurred.
FSP_ERR_OUT_OF_MEMORY	There is no more heap memory available.
FSP_ERR_WIFI_FAILED	Error occurred with command to Wifi module.
FSP_ERR_ALREADY_OPEN	Module is already open. This module can only be opened once.

◆ **rm\_wifi\_onchip\_silex\_version\_get()**

```
fsp_err_t rm_wifi_onchip_silex_version_get ( fsp_version_t *const p_version)
```

Returns the WIFI\_ONCHIP\_SILEX Middleware module versions.

**Parameters**

[out]	p_version	Memory address to return version information to.
-------	-----------	--------------------------------------------------

**Return values**

FSP_SUCCESS	Function completed successfully.
FSP_ERR_ASSERTION	Assertion error occurred.

◆ **rm\_wifi\_onchip\_silex\_close()**

```
fsp_err_t rm_wifi_onchip_silex_close ( )
```

Disables WIFI\_ONCHIP\_SILEX.

**Return values**

FSP_SUCCESS	WIFI_ONCHIP_SILEX closed successfully.
FSP_ERR_ASSERTION	Assertion error occurred.
FSP_ERR_WIFI_FAILED	Error occurred with command to Wifi module.
FSP_ERR_NOT_OPEN	Module is not open.

◆ **rm\_wifi\_onchip\_silex\_connect()**

```
fsp_err_t rm_wifi_onchip_silex_connect ( const char * p_ssid, uint32_t security, const char * p_passphrase )
```

Connects to the specified Wifi Access Point.

**Parameters**

[in]	p_ssid	Pointer to SSID of Wifi Access Point.
[in]	security	Security type to use for connection.
[in]	p_passphrase	Pointer to the passphrase to use for connection.

**Return values**

FSP_SUCCESS	Function completed successfully.
FSP_ERR_WIFI_FAILED	Error occurred with command to Wifi module.
FSP_ERR_ASSERTION	Assertion error occurred.
FSP_ERR_NOT_OPEN	The instance has not been opened.
FSP_ERR_INVALID_ARGUMENT	No commas are accepted in the SSID or Passphrase.

◆ **rm\_wifi\_onchip\_silex\_mac\_addr\_get()**

```
fsp_err_t rm_wifi_onchip_silex_mac_addr_get ( uint8_t * p_macaddr)
```

Get MAC address.

**Parameters**

[out]	p_macaddr	Pointer array to hold mac address.
-------	-----------	------------------------------------

**Return values**

FSP_SUCCESS	Function completed successfully.
FSP_ERR_WIFI_FAILED	Error occurred with command to Wifi module.
FSP_ERR_ASSERTION	Assertion error occurred.
FSP_ERR_NOT_OPEN	The instance has not been opened.

◆ **rm\_wifi\_onchip\_silex\_scan()**

```
fsp_err_t rm_wifi_onchip_silex_scan ( WIFIScanResult_t* p_results, uint32_t maxNetworks )
```

Get the information about local Wifi Access Points.

**Parameters**

[out]	p_results	Pointer to a structure array holding scanned Access Points.
[in]	maxNetworks	Size of the structure array for holding APs.

**Return values**

FSP_SUCCESS	Function completed successfully.
FSP_ERR_WIFI_FAILED	Error occurred with command to Wifi module.
FSP_ERR_ASSERTION	Assertion error occurred.
FSP_ERR_NOT_OPEN	The instance has not been opened.

◆ **rm\_wifi\_onchip\_silex\_ping()**

```
fsp_err_t rm_wifi_onchip_silex_ping ( uint8_t* p_ip_addr, uint32_t count, uint32_t interval_ms )
```

Ping an IP address on the network.

**Parameters**

[in]	p_ip_addr	Pointer to IP address array.
[in]	count	Number of pings to attempt.
[in]	interval_ms	Interval between ping attempts.

**Return values**

FSP_SUCCESS	Function completed successfully.
FSP_ERR_WIFI_FAILED	Error occurred with command to Wifi module.
FSP_ERR_ASSERTION	Assertion error occurred.
FSP_ERR_NOT_OPEN	The instance has not been opened.

◆ **rm\_wifi\_onchip\_silex\_ip\_addr\_get()**

```
fsp_err_t rm_wifi_onchip_silex_ip_addr_get ( uint8_t* p_ip_addr)
```

Get the assigned module IP address.

**Parameters**

[out]	p_ip_addr	Pointer an array to hold the IP address.
-------	-----------	------------------------------------------

**Return values**

FSP_SUCCESS	Function completed successfully.
FSP_ERR_WIFI_FAILED	Error occurred with command to Wifi module.
FSP_ERR_ASSERTION	Assertion error occurred.
FSP_ERR_NOT_OPEN	The instance has not been opened.

◆ **rm\_wifi\_onchip\_silex\_avail\_socket\_get()**

```
fsp_err_t rm_wifi_onchip_silex_avail_socket_get ( uint32_t* p_socket_id)
```

Get the next available socket ID.

**Parameters**

[out]	p_socket_id	Pointer to an integer to hold the socket ID.
-------	-------------	----------------------------------------------

**Return values**

FSP_SUCCESS	Function completed successfully.
FSP_ERR_ASSERTION	Assertion error occurred.
FSP_ERR_NOT_OPEN	The instance has not been opened.
FSP_ERR_WIFI_FAILED	Error occurred in the execution of this function



◆ **rm\_wifi\_onchip\_silex\_socket\_status\_get()**

```
fsp_err_t rm_wifi_onchip_silex_socket_status_get ( uint32_t socket_no, uint32_t* p_socket_status )
```

Get the socket status.

**Parameters**

[in]	socket_no	Socket ID number.
[out]	p_socket_status	Pointer to an integer to hold the socket status

**Return values**

FSP_SUCCESS	Function completed successfully.
FSP_ERR_ASSERTION	Assertion error occurred.
FSP_ERR_NOT_OPEN	The instance has not been opened.

◆ **rm\_wifi\_onchip\_silex\_socket\_create()**

```
fsp_err_t rm_wifi_onchip_silex_socket_create ( uint32_t socket_no, uint32_t type, uint32_t ipversion )
```

Create a new socket instance.

**Parameters**

[in]	socket_no	Socket ID number.
[in]	type	Socket type.
[in]	ipversion	Socket IP type.

**Return values**

FSP_SUCCESS	Function completed successfully.
FSP_ERR_WIFI_FAILED	Error occurred with command to Wifi module.
FSP_ERR_ASSERTION	Assertion error occurred.
FSP_ERR_NOT_OPEN	The instance has not been opened.

◆ **rm\_wifi\_onchip\_silex\_tcp\_connect()**

```
fsp_err_t rm_wifi_onchip_silex_tcp_connect ( uint32_t socket_no, uint32_t ipaddr, uint32_t port )
```

Connect to a specific IP and Port using socket.

**Parameters**

[in]	socket_no	Socket ID number.
[in]	ipaddr	IP address for socket connection.
[in]	port	Port number for socket connection.

**Return values**

FSP_SUCCESS	Function completed successfully.
FSP_ERR_WIFI_FAILED	Error occurred with command to Wifi module.
FSP_ERR_ASSERTION	Assertion error occurred.
FSP_ERR_NOT_OPEN	The instance has not been opened.

◆ **rm\_wifi\_onchip\_silex\_tcp\_send()**

```
int32_t rm_wifi_onchip_silex_tcp_send ( uint32_t socket_no, const uint8_t* p_data, uint32_t length, uint32_t timeout_ms )
```

Send data over TCP to a server.

**Parameters**

[in]	socket_no	Socket ID number.
[in]	p_data	Pointer to data to send.
[in]	length	Length of data to send.
[in]	timeout_ms	Timeout to wait for transmit end event

**Return values**

FSP_ERR_WIFI_FAILED	Error occurred with command to Wifi module.
FSP_ERR_ASSERTION	Assertion error occurred.
FSP_ERR_NOT_OPEN	The instance has not been opened.

◆ **rm\_wifi\_onchip\_silex\_tcp\_recv()**

```
int32_t rm_wifi_onchip_silex_tcp_recv ( uint32_t socket_no, uint8_t * p_data, uint32_t length,
uint32_t timeout_ms )
```

Receive data over TCP from a server.

**Parameters**

[in]	socket_no	Socket ID number.
[out]	p_data	Pointer to data received from socket.
[in]	length	Length of data array used for receive.
[in]	timeout_ms	Timeout to wait for data to be received from socket.

**Return values**

FSP_SUCCESS	Function completed successfully.
FSP_ERR_WIFI_FAILED	Error occurred with command to Wifi module.
FSP_ERR_NOT_OPEN	The instance has not been opened.

◆ **rm\_wifi\_onchip\_silex\_tcp\_shutdown()**

```
int32_t rm_wifi_onchip_silex_tcp_shutdown ( uint32_t socket_no, uint32_t shutdown_channels )
```

Shutdown portion of a socket

**Parameters**

[in]	socket_no	Socket ID number.
[in]	shutdown_channels	Specify if read or write channel is shutdown for socket

**Return values**

FSP_SUCCESS	Function completed successfully.
FSP_ERR_ASSERTION	Assertion error occurred.
FSP_ERR_NOT_OPEN	The instance has not been opened.

◆ **rm\_wifi\_onchip\_silex\_socket\_disconnect()**

```
fsp_err_t rm_wifi_onchip_silex_socket_disconnect ( uint32_t socket_no)
```

Disconnect a specific socket connection.

**Parameters**

[in]	socket_no	Socket ID to disconnect
------	-----------	-------------------------

**Return values**

FSP_SUCCESS	Function completed successfully.
FSP_ERR_WIFI_FAILED	Error occurred with command to Wifi module.
FSP_ERR_ASSERTION	Assertion error occurred.
FSP_ERR_NOT_OPEN	The instance has not been opened.
FSP_ERR_INVALID_ARGUMENT	Bad parameter value was passed into function.

◆ **rm\_wifi\_onchip\_silex\_disconnect()**

```
fsp_err_t rm_wifi_onchip_silex_disconnect ( )
```

Disconnects from connected AP.

**Return values**

FSP_SUCCESS	WIFI_ONCHIP_SILEX disconnected successfully.
FSP_ERR_ASSERTION	Assertion error occurred.
FSP_ERR_WIFI_FAILED	Error occurred with command to Wifi module.
FSP_ERR_NOT_OPEN	Module is not open.

◆ **rm\_wifi\_onchip\_silex\_dns\_query()**

```
fsp_err_t rm_wifi_onchip_silex_dns_query ( const char * p_textstring, uint8_t * p_ip_addr )
```

Initiate a DNS lookup for a given URL.

**Parameters**

[in]	p_textstring	Pointer to array holding URL to query from DNS.
[out]	p_ip_addr	Pointer to IP address returned from look up.

**Return values**

FSP_SUCCESS	Function completed successfully.
FSP_ERR_WIFI_FAILED	Error occurred with command to Wifi module.
FSP_ERR_ASSERTION	Assertion error occurred.
FSP_ERR_NOT_OPEN	The instance has not been opened.
FSP_ERR_INVALID_ARGUMENT	The URL passed in is too long.

◆ **rm\_wifi\_onchip\_silex\_socket\_connected()**

```
fsp_err_t rm_wifi_onchip_silex_socket_connected ( fsp_err_t * p_status)
```

Check if a specific socket instance is connected.

**Parameters**

[out]	p_status	Pointer to integer holding the socket connection status.
-------	----------	----------------------------------------------------------

**Return values**

FSP_SUCCESS	Function completed successfully.
FSP_ERR_ASSERTION	Assertion error occurred.
FSP_ERR_NOT_OPEN	The instance has not been opened.
FSP_ERR_WIFI_FAILED	Error occurred with command to Wifi module.

◆ **rm\_wifi\_onchip\_silex\_uart\_callback()**

```
void rm_wifi_onchip_silex_uart_callback ( uart\_callback\_args\_t * p_args)
```

Callback function for first UART port in command mode. Used specifically for the SCI UART driver.

**Parameters**

[in]	p_args	Pointer to callback arguments structure.
------	--------	------------------------------------------

◆ **SOCKETS\_Socket()**

```
Socket_t SOCKETS_Socket ( int32_t IDomain, int32_t IType, int32_t IProtocol )
```

Creates a TCP socket.

This call allocates memory and claims a socket resource.

**See also**

[SOCKETS\\_Close\(\)](#)

**Parameters**

[in]	IDomain	Must be set to SOCKETS_AF_INET. See SocketDomains.
[in]	IType	Set to SOCKETS_SOCK_STREAM to create a TCP socket. No other value is valid. See SocketTypes.
[in]	IProtocol	Set to SOCKETS_IPPROTO_TCP to create a TCP socket. No other value is valid. See Protocols.

**Returns**

- If a socket is created successfully, then the socket handle is returned
- SOCKETS\_INVALID\_SOCKET is returned if an error occurred.

### ◆ SOCKETS\_Connect()

```
int32_t SOCKETS_Connect ( Socket_t xSocket, SocketsSockaddr_t * pXAddress, Socklen_t
xAddressLength )
```

Connects the socket to the specified IP address and port.

The socket must first have been successfully created by a call to [SOCKETS\\_Socket\(\)](#).

#### Parameters

[in]	xSocket	The handle of the socket to be connected.
[in]	pXAddress	A pointer to a SocketsSockaddr_t structure that contains the the address to connect the socket to.
[in]	xAddressLength	Should be set to sizeof( SocketsSockaddr_t ).

#### Returns

- SOCKETS\_ERROR\_NONE if a connection is established.
- If an error occurred, a negative value is returned.

◆ **SOCKETS\_Recv()**

```
int32_t SOCKETS_Recv ( Socket_t xSocket, void * pvBuffer, size_t xBufferLength, uint32_t ulFlags )
```

Receive data from a TCP socket.

The socket must have already been created using a call to [SOCKETS\\_Socket\(\)](#) and connected to a remote socket using [SOCKETS\\_Connect\(\)](#).

**Parameters**

[in]	xSocket	The handle of the socket from which data is being received.
[out]	pvBuffer	The buffer into which the received data will be placed.
[in]	xBufferLength	The maximum number of bytes which can be received. pvBuffer must be at least xBufferLength bytes long.
[in]	ulFlags	Not currently used. Should be set to 0.

**Returns**

- If the receive was successful then the number of bytes received (placed in the buffer pointed to by pvBuffer) is returned.
- If a timeout occurred before data could be received then 0 is returned (timeout is set using [SOCKETS\\_SO\\_RCVTIMEO](#)).
- If an error occurred, a negative value is returned.



◆ **SOCKETS\_Send()**

```
int32_t SOCKETS_Send ( Socket_t xSocket, const void * pvBuffer, size_t xDataLength, uint32_t ulFlags )
```

Transmit data to the remote socket.

The socket must have already been created using a call to [SOCKETS\\_Socket\(\)](#) and connected to a remote socket using [SOCKETS\\_Connect\(\)](#).

**Parameters**

[in]	xSocket	The handle of the sending socket.
[in]	pvBuffer	The buffer containing the data to be sent.
[in]	xDataLength	The length of the data to be sent.
[in]	ulFlags	Not currently used. Should be set to 0.

**Returns**

- On success, the number of bytes actually sent is returned.
- If an error occurred, a negative value is returned.

◆ **SOCKETS\_Shutdown()**

```
int32_t SOCKETS_Shutdown ( Socket_t xSocket, uint32_t ulHow )
```

Closes all or part of a full-duplex connection on the socket.

**Parameters**

[in]	xSocket	The handle of the socket to shutdown.
[in]	ulHow	SOCKETS_SHUT_RD, SOCKETS_SHUT_WR or SOCKETS_SHUT_RDWR. ShutdownFlags

**Returns**

- If the operation was successful, 0 is returned.
- If an error occurred, a negative value is returned.

◆ **SOCKETS\_Close()**

```
int32_t SOCKETS_Close ( Socket_t xSocket)
```

Closes the socket and frees the related resources.

**Parameters**

[in]	xSocket	The handle of the socket to close.
------	---------	------------------------------------

**Returns**

- On success, 0 is returned.
- If an error occurred, a negative value is returned.

◆ **SOCKETS\_SetSockOpt()**

```
int32_t SOCKETS_SetSockOpt ( Socket_t xSocket, int32_t lLevel, int32_t lOptionName, const void * pvOptionValue, size_t xOptionLength )
```

Manipulates the options for the socket.

**Parameters**

[in]	xSocket	The handle of the socket to set the option for.
[in]	lLevel	Not currently used. Should be set to 0.
[in]	lOptionName	See SetSockOptOptions.
[in]	pvOptionValue	A buffer containing the value of the option to set.
[in]	xOptionLength	The length of the buffer pointed to by pvOptionValue.

**Note**

Socket option support and possible values vary by port. Please see *PORT\_SPECIFIC\_LINK* to check the valid options and limitations of your device.

- Berkeley Socket Options
  - SOCKETS\_SO\_RCVTIMEO
    - Sets the receive timeout
    - pvOptionValue (TickType\_t) is the number of milliseconds that the receive function should wait before timing out.
    - Setting pvOptionValue = 0 causes receive to wait forever.
    - See PORT\_SPECIFIC\_LINK for device limitations.
  - SOCKETS\_SO\_SNDTIMEO
    - Sets the send timeout
    - pvOptionValue (TickType\_t) is the number of milliseconds that the send function should wait before timing out.
    - Setting pvOptionValue = 0 causes send to wait forever.

- See PORT\_SPECIFIC\_LINK for device limitations.
- Non-Standard Options
  - SOCKETS\_SO\_NONBLOCK
    - Makes a socket non-blocking.
    - pvOptionValue is ignored for this option.
- Security Sockets Options
  - SOCKETS\_SO\_REQUIRE\_TLS
    - Use TLS for all connect, send, and receive on this socket.
    - This socket options MUST be set for TLS to be used, even if other secure socket options are set.
    - pvOptionValue is ignored for this option.
  - SOCKETS\_SO\_TRUSTED\_SERVER\_CERTIFICATE
    - Set the root of trust server certificate for the socket.
    - This socket option only takes effect if SOCKETS\_SO\_REQUIRE\_TLS is also set. If SOCKETS\_SO\_REQUIRE\_TLS is not set, this option will be ignored.
    - pvOptionValue is a pointer to the formatted server certificate. TODO: Link to description of how to format certificates with
      - xOptionLength (BaseType\_t) is the length of the certificate in bytes.
  - SOCKETS\_SO\_SERVER\_NAME\_INDICATION
    - Use Server Name Indication (SNI)
    - This socket option only takes effect if SOCKETS\_SO\_REQUIRE\_TLS is also set. If SOCKETS\_SO\_REQUIRE\_TLS is not set, this option will be ignored.
    - pvOptionValue is a pointer to a string containing the hostname
    - xOptionLength is the length of the hostname string in bytes.

**Returns**

- On success, 0 is returned.
- If an error occurred, a negative value is returned.

**◆ SOCKETS\_GetHostByName()**

```
uint32_t SOCKETS_GetHostByName ( const char * pcHostName)
```

Resolve a host name using Domain Name Service.

**Parameters**

[in]	pcHostName	The host name to resolve.
------	------------	---------------------------

**Returns**

- The IPv4 address of the specified host.
- If an error has occurred, 0 is returned.

### ◆ SOCKETS\_Init()

BaseType\_t SOCKETS\_Init ( void )

Secure Sockets library initialization function.

This function does general initialization and setup. It must be called once and only once before calling any other function.

#### Returns

- pdPASS if everything succeeds
- pdFAIL otherwise.

### ◆ WIFI\_On()

WiFiReturnCode\_t WIFI\_On ( void )

Turns on Wi-Fi.

This function turns on Wi-Fi module, initializes the drivers and must be called before calling any other Wi-Fi API

#### Returns

eWiFiSuccess if Wi-Fi module was successfully turned on, failure code otherwise.

### ◆ WIFI\_Off()

WiFiReturnCode\_t WIFI\_Off ( void )

Turns off Wi-Fi.

This function turns off the Wi-Fi module. The Wi-Fi peripheral should be put in a low power or off state in this routine.

#### Returns

eWiFiSuccess if Wi-Fi module was successfully turned off, failure code otherwise.

◆ **WIFI\_ConnectAP()**

WIFIReturnCode\_t WIFI\_ConnectAP ( const WIFINetworkParams\_t \*const *pxNetworkParams* )

Connects to the Wi-Fi Access Point (AP) specified in the input.

The Wi-Fi should stay connected when the same Access Point it is currently connected to is specified. Otherwise, the Wi-Fi should disconnect and connect to the new Access Point specified. If the new Access Point specified has invalid parameters, then the Wi-Fi should be disconnected.

**Parameters**

[in]	pxNetworkParams	Configuration to join AP.
------	-----------------	---------------------------

**Returns**

eWiFiSuccess if connection is successful, failure code otherwise.

```
WIFINetworkParams_t xNetworkParams;
WIFIReturnCode_t xWifiStatus;
xNetworkParams.pcSSID = "SSID String";
xNetworkParams.ucSSIDLength = SSIDLen;
xNetworkParams.pcPassword = "Password String";
xNetworkParams.ucPasswordLength = PassLength;
xNetworkParams.xSecurity = eWiFiSecurityWPA2;
xWifiStatus = WIFI_ConnectAP( &( xNetworkParams ) );
if(xWifiStatus == eWiFiSuccess)
{
    //Connected to AP.
}
```

**See also**

WIFINetworkParams\_t

◆ **WIFI\_Disconnect()**

WIFIReturnCode\_t WIFI\_Disconnect ( void )

Disconnects from the currently connected Access Point.

**Returns**

eWiFiSuccess if disconnection was successful or if the device is already disconnected, failure code otherwise.

◆ **WIFI\_Reset()**

```
WIFIReturnCode_t WIFI_Reset ( void )
```

Resets the Wi-Fi Module.

**Returns**

eWiFiSuccess if Wi-Fi module was successfully reset, failure code otherwise.

◆ **WIFI\_Scan()**

```
WIFIReturnCode_t WIFI_Scan ( WIFIScanResult_t* pBuffer, uint8_t ucNumNetworks )
```

Perform a Wi-Fi network Scan.

**Parameters**

[in]	pBuffer	- Buffer for scan results.
[in]	ucNumNetworks	- Number of networks to retrieve in scan result.

**Returns**

eWiFiSuccess if the Wi-Fi network scan was successful, failure code otherwise.

*Note*

*The input buffer will have the results of the scan.*

```
const uint8_t ucNumNetworks = 10; //Get 10 scan results
WIFIScanResult_t xScanResults[ ucNumNetworks ];
WIFI_Scan( xScanResults, ucNumNetworks );
```

◆ **WIFI\_Ping()**

```
WIFIReturnCode_t WIFI_Ping ( uint8_t* pucIPAddr, uint16_t usCount, uint32_t ullIntervalMS )
```

Ping an IP address in the network.

**Parameters**

[in]	pucIPAddr	IP Address array to ping.
[in]	usCount	Number of times to ping
[in]	ullIntervalMS	Interval in milliseconds for ping operation

**Returns**

eWiFiSuccess if ping was successful, other failure code otherwise.

◆ **WIFI\_GetIP()**

WIFIReturnCode\_t WIFI\_GetIP ( uint8\_t\* *pucIPAddr* )

Retrieves the Wi-Fi interface's IP address.

**Parameters**

[out]	<i>pucIPAddr</i>	IP Address buffer.
-------	------------------	--------------------

**Returns**

eWiFiSuccess if successful and IP Address buffer has the interface's IP address, failure code otherwise.

```
uint8_t ucIPAddr[ 4 ];
WIFI_GetIP( &ucIPAddr[0] );
```

◆ **WIFI\_GetMAC()**

WIFIReturnCode\_t WIFI\_GetMAC ( uint8\_t\* *pucMac* )

Retrieves the Wi-Fi interface's MAC address.

**Parameters**

[out]	<i>pucMac</i>	MAC Address buffer sized 6 bytes.
-------	---------------	-----------------------------------

```
uint8_t ucMacAddressVal[ wificonfigMAX_BSSID_LEN ];
WIFI_GetMAC( &ucMacAddressVal[0] );
```

**Returns**

eWiFiSuccess if the MAC address was successfully retrieved, failure code otherwise. The returned MAC address must be 6 consecutive bytes with no delimiters.

◆ **WIFI\_GetHostIP()**

```
WiFiReturnCode_t WIFI_GetHostIP ( char * pCHost, uint8_t* puCIPAddr )
```

Retrieves the host IP address from a host name using DNS.

**Parameters**

[in]	pCHost	- Host (node) name.
[in]	puCIPAddr	- IP Address buffer.

**Returns**

eWiFiSuccess if the host IP address was successfully retrieved, failure code otherwise.

```
uint8_t ucIPAddr[ 4 ];
```

```
WIFI_GetHostIP( "amazon.com", &ucIPAddr[0] );
```

◆ **WIFI\_IsConnected()**

```
BaseType_t WIFI_IsConnected ( void )
```

Check if the Wi-Fi is connected.

**Returns**

pdTRUE if the link is up, pdFalse otherwise.

## 4.2.77 AWS Secure Sockets

### Modules

This module provides the AWS Secure Sockets implementation.

## Overview

### Features

Information about the features provided by the AWS Secure Sockets Library is available in the [FreeRTOS Libraries User Guide](#).

The FSP implementation supports using Secure Sockets with either Ethernet or WiFi. These stacks can be added in FSP via the RA Configuration editor under FreeRTOS | Secure Sockets.

### Dependencies

The Secure Sockets library has two dependencies:

1. A TCP/IP implementation



## 2. A TLS implementation

For TCP/IP, AWS have provided the FreeRTOS TCP/IP implementation. For TLS, AWS have chosen mbedTLS, but use PKCS11 for storage and invoking the crypto portion of mbedTLS. For more information about AWS Secure Sockets, refer to the [AWS documentation](#). An example of Secure Sockets usage is on the same page.

### mbedTLS

mbedTLS is ARM's implementation of the TLS and SSL protocols as well as the cryptographic primitives required by those implementations. mbedTLS is also solely used for its cryptographic features even if the TLS/SSL portions are not used. With PSA, ARM have created a separate API for cryptography. Starting with mbedTLS3, crypto implementation has been moved out to a new module called mbedCrypto (PSA Crypto API) and a build time configuration can direct the mbedTLS3 implementation to use either the old mbedtls cryptography functions or use the new PSA Crypto API. Since the current version of mbedCrypto (PSA Crypto API) implements both the old mbedtls crypto API as well as the new PSA Crypto API, either option is functional for now.

### CipherSuites

During the TLS connection setup stage, the client has to indicate to the server the type of cryptographic operations that it supports. This is referred to as the ciphersuite. The entire list of ciphersuites supported by mbedTLS can be found in mbedtls/ssl\_ciphersuites.h.

### Configuration

In FSP, Secure Sockets can be added as a new stack via FreeRTOS | Secure Sockets | Secure Sockets on WiFi or Secure Sockets on FreeRTOS Plus TCP. All required dependant modules, except heap, are automatically added. To complete the configuration,

- Add a heap instance and use the same one for all dependencies.
- Resolve the module configuration requirements.

## Usage Notes

For detailed documentation on Secure Sockets consult the [AWS documentation](#).

## Examples

### Basic Example

This is a basic example of using the Secure Sockets API with Ethernet. The message "hello, world!" is sent to a remote socket.

```
#define SECURE_SOCKETS_EXAMPLE_BUFFER_SIZE (64)
static const char SERVER_CERTIFICATE_PEM[] =
"-----BEGIN CERTIFICATE-----\n"
"MIIDazCCA1OgAwIBAgIURabL79ayIywQv0y8SPnbZ1FYDRIwDQYJKoZIhvcNAQEL\n"
"BQAwRTELMAkGA1UEBhMCQVUxEzARBgNVBAgMC1NvbWUtU3RhdGUxITAfBgNVBAoM\n"
"GE1udGVybWV0IFdpZGdpdHMgUHR5IEEx0ZDAeFw0xOTA5MTEyMTIyMjZaFw0yMDA5\n"
```

```

"MTAyMTIyMjZaMEUxCzAJBgNVBAYTAkFVMRMwEQYDVQQIDApTb211LVN0YXRlMSEw\n"
"HwYDVQQKBHJbnRlcm5ldCBXaWRnaXRzIFB0eSBMdGQwggEiMA0GCSqGSIb3DQEB\n"
"AQUAA4IBDwAwggEKAoIBAQDSA3h+5sT58FHgnovnQzsVHQ0H/3TsnEKwVzyBwTQl\n"
"s4PbG6VXCWyyJWjdJ4XMH1oU8gAlxauFbw0098Aquei4K3Pi/ynKNBeX4VJcLyE5\n"
"Azq7nRIIwt4+OoZ5kV7v8JIoLY5i+Ktn3zq1t0y1ZmK6Uk/rRPonb+Kx7wQPX7jq\n"
"ZIZGda+CgF6ZedidPcABuggqDly3U2gLiRPoBhe9nN2hg60rRp7vhhbWMF0pzTDXu\n"
"BKF7XSTbhYz3pl6NeOCLh5E3t8x908Ui5W1zDN3iOysrcwQFtCiGTvzNtxSfli1+\n"
"PugIt9Q2vlymuz5qi+juxHftJSX086M5SV7exqUOXP9RAGMBAAGjUzBRMB0GA1Ud\n"
"DgQWBQ8VNJEJUjptKMjmrOY3XApNp5lDAfBgNVHSMEGDAwBQ8VNJEJUjptKM\n"
"jmrOY3XApNp5lDAPBgNVHRMBAf8EBTADAQH/MA0GCSqGSIb3DQEBcWUAA4IBAQA\n"
"CabfjsYUnG8tt3/GDdhjsuG+SfeQe1lS73pzi3+L616bPH5MNUv+LkgR/1AFEqt5\n"
"WadKVTgzW5Ork1t7CfkYwrOHbyhyaaDPzERjMcfCcl8lQluBy6vE/1Eb0hWq6XlO\n"
"f6+8i+vKxWkSIXs2ZQqqYSOTTzAjHSSiiuE5WsC00ErvCvnc7uD6+3Y7W1uQRkFZ\n"
"uSd9ANlixPvAFi69FF/ymlJv6vII5GXOvDrIwdr50bMNuezMEx6qMNDADRH8iEaL\n"
"JaSgfk1czGiI1i7MPD4JTtsXOgKwxcBDAA0zQDVA5uBGEIOhva3m5X70N4iO7W0V\n"
"eEhZekKeg3F13t/CXi8l\n"
"-----END CERTIFICATE-----";
#define keyCLIENT_CERTIFICATE_PEM \
"-----BEGIN CERTIFICATE-----\n" \
"MIIDETCCAfKCFHwd2yn8zn5qB2ChYUT9Mvbi9Xp1MA0GCSqGSIb3DQEBcWUAMEUx\n" \
"CzAJBgNVBAYTAkFVMRMwEQYDVQQIDApTb211LVN0YXRlMSEwHwYDVQQKBHJbnRl\n" \
"cm5ldCBXaWRnaXRzIFB0eSBMdGQwHhcNMkU0OTUwWhcNMjAwOTUwMjE5MjE5\n" \
"MjU0WjBFMQswCQYDVQQGEwJBVTETMBEGA1UECAwKU29tZS1TdGF0ZTEhMB8GA1UE\n" \
"CgwYSW50ZXJuZXQvZ2l0cyBQdHkgTHRkMIIBIjANBgkqhkiG9w0BAQEFAAOCC\n" \
"AQ8AMIIBCgKCAQEAO8oThJXSMD04l0L7HTpC4TX8NalBvnkFw30Av67dl/oZDjVA\n" \
"iXpNzkhVppLnj++0/Oed0M7UwNUO2nurQt6yTYrvW7E8ZPjAlC7ueJcGYZhOaVv2\n" \
"bhSmigjFQru21w5odSuYy5+22CCgxf58nrRC05Bk+GwWgZmcrxe/BzutRHQ7X4x\n" \
"dYJhyhBOi2R1Kt8XsbuWilfgfkVhkhVklFeKqiypdQM6cnPWo/G4DyW34jOXzzEM\n" \
"FLWvQOQLCKUZogjJBnFdbx8o0OwMkYcChbV7gqPE6cw0Zy26Cv1LQiINyonLPbNT\n" \
"c64sS/ZBGPZFOPJmb4tG2nipYgZ1h0/r++jCbWIDAQABMA0GCSqGSIb3DQEBcWUA\n" \
"A4IBAQCdq59ubdRY9EiV3bleKXeqG7+8HgBHdm0X9dgq10nD37p00YLyuZLE9NM\n" \
"066G/VcflGrx/Nzw+/UuI7/UuBbBS/3ppHRnsZqBI18nnr/ULrFQy8z3vKtL1q3C\n" \
"DxabjPONlP02keJeTTA71N/RCeMwJoa8i0XKXGdu/hQo6x4n+Gq73fEiGCl99xsc\n" \
"4tIO4yPS4lv+uXBzEUzoEy0CLiKiDesnT5lLeCyPmUNoU89HU95IusZT7kygCHHD\n"

```

```

"72amlic3X8PKc268KT3ilr3VMhK67C+iIIkfrM5AiU+oOIRrIHSC/p0RigJg3rXA\n" \
"GBIRHvt+OYF9fDeG7U4QDJNCfGW+\n" \
"-----END CERTIFICATE-----"
#define keyCLIENT_PRIVATE_KEY_PEM \
"-----BEGIN RSA PRIVATE KEY-----\n" \
"MIIEowIBAAKCAQEAo8oThJXSMDo41oL7HTpC4TX8NalBvnkFw30Av67dl/oZDjVA\n" \
"iXpNzkhVppLnj++0/Oed0M7UwNUO2nurQt6yTYrvW7E8ZPjAlC7ueJcGYZhOaVv2\n" \
"bhSmigjFQru2lw5odSuYy5+22CCgxfT58nrRCo5Bk+GwWgZmcrxe/BzutRHQ7X4x\n" \
"dYJhyhBOi2R1Kt8XsbuWilfgfkVhkhVklFeKqiypdQM6cnPWo/G4DyW34jOXzZEM\n" \
"FLWvQOQLCKUZogjJBnFdbx8o0OwMkYCChbV7gqPE6cw0Zy26Cv1LQiINyonLPbNT\n" \
"c64sS/ZBGPZFOPJmb4tG2nipYgZ1h0/r++jCbWIDAQABAoIBAQCGR2hC/ZVJhQIM\n" \
"c2uuJZKpElpIIBBPOObzwwS3IYR4UUjzVgMn7Ubbmxf1LXD8lzfZU4YVp0vTH5lC\n" \
"07qvYuXpHqtnj+GEok837VYctUY9AuHeDM/2paV3awNV15E1PFG1Jd3pqnH7tJw6\n" \
"VBZBDiGNntlagN/UnoSlmfvpU0r8VGPXCBNxe3JY5QyBJPI1wF4LcxRI+eYmr7Ja\n" \
"/cjn97DZotgz4B7gUNu8XIEkUOTwPabZINY1zclWiXTMA+8qTniPVk653h14Xqt4\n" \
"4o4D4YCTpwJcmxSV1m21/6+uyuXr9SIKAE+Ys2cYLA46x+rwLaW5fUoQ5hHa0Ytb\n" \
"RYJ4SrtBAoGBANwtw1E69N0hq5xDPckSbNGubIeG8P4mBhGkJxIqYoqugGLMDiGX\n" \
"4bltrjr2TPWaxTo3pPavLJiBMIsENA5KU+c/r0jLkxgEp9MIVJrtNgkCiDQqogBG\n" \
"j4IJL2iQwXoLCqk2tx/dh9Mww+7SETE7EPNrv4UrYaGN5AEvpf5W+NHPAoGBAMQ6\n" \
"wVa0Mx1PLA4enY2rfe3WXP8bzjleSOWR75JXqG2WbPC0/cszwbyPWOEqRpBZfvD\n" \
"QFkKx06xp1C09XwiQanr2gDucYXHHeEKg/9iuJV1UkMQp95ojlhtSXdRZV7/14pmN\n" \
"fpB2vcAptX/4gY4tDrWMO08JNnRje7duC+rmmk1hAoGAS4L0QLCNB/h2JOq+Uuhn\n" \
"/FGfmOVfFPFrA6D3DbxcxpWUWVzSLvb0SophryzxbfEKyau7V5KbDp7ZSU/IC20\n" \
"KOyggjSekAkDi7fjrrTRW/Cgg6g6G4YIOBO4qCtHdDbwJMHndk6096qw5EzS67qLp\n" \
"Apz5OZ5zChySjri/+HnTxJECgYBysGSP6IJ3fytplTtAshnU5JU2BWpi3ViBoXoE\n" \
"bndilajWhvJO8dEqBB5OfAcCF0y6TnWt1T8oH21LHnjcNK1sRw0Dv11bd1oylybx\n" \
"3da41dRG0sCEtof1MB7nHdDLt/DZDnoKtVvyFG6gfP47utn+Ahgn+Zp6K+46J3eP\n" \
"s3g8AQKBgE/PJiaF8pbBXaZOuwRRA9GOMSbDIF6+jBYTYp4L9wk4+LZArKtyI+4k\n" \
Md2DUvHwMC+ddOtKqjYnLm+V5cSbvU7aPvBZtwxghzTUDcf7EvnA3V/bQBh3R0z7\n" \
pVsxTyGRmBSeLdbUWACUbx9LXdpuDarPAJ59daWmP3mBEVmwDzUw\n" \
"-----END RSA PRIVATE KEY-----"
const uint8_t g_ip_address[4] = {169, 254, 57, 49};
const uint8_t g_net_mask[4] = {255, 255, 0, 0};
const uint8_t g_gateway_address[4] = {169, 254, 57, 49};

```

```
const uint8_t g_dns_address[4] = {8, 8, 8, 8};
const uint8_t g_mac_address[6] = {0x66, 0x66, 0x66, 0x66, 0x66, 0x66};
static uint8_t g_buffer[SECURE_SOCKETS_EXAMPLE_BUFFER_SIZE];
/*****
*****
* Refer to the following link for detailed API information:
* https://docs.aws.amazon.com/freertos/latest/lib-
ref/html2/secure_sockets/secure_sockets_function_primary.html
*****
*****/
void secure_sockets_ethernet_example (void)
{
    /* Initialize the crypto hardware acceleration. */
    mbedtls_platform_setup(NULL);
    xLoggingTaskInitialize(256, 1, 10); // NOLINT(readability-magic-numbers)
    ProvisioningParams_t params;
    /* Write the keys into a secure region in data flash. */
    params.pucClientPrivateKey      = (uint8_t *) keyCLIENT_PRIVATE_KEY_PEM;
    params.pucClientCertificate     = (uint8_t *) keyCLIENT_CERTIFICATE_PEM;
    params.ulClientPrivateKeyLength = 1 + strlen((const char *)
params.pucClientPrivateKey);
    params.ulClientCertificateLength = 1 + strlen((const char *)
params.pucClientCertificate);
    params.pucJITPCertificate       = NULL;
    params.ulJITPCertificateLength  = 0;
    vAlternateKeyProvisioning(&params);
    /* Start up the network stack. */
    FreeRTOS_IPInit(g_ip_address, g_net_mask, g_gateway_address, g_dns_address,
g_mac_address);
    while (pdFALSE == FreeRTOS_IsNetworkUp())
    {
        vTaskDelay(1);
    }
    Socket_t socket = SOCKETS_Socket(SOCKETS_AF_INET, SOCKETS SOCK_STREAM,
```

```
SOCKETS_IPPROTO_TCP);

if (SOCKETS_INVALID_SOCKET == socket)
{
/* Could not create socket. */
    __BKPT(0);
}

/* Enable TLS and configure the server certificate. */
SOCKETS_SetSockOpt(socket, 0, SOCKETS_SO_REQUIRE_TLS, NULL, (size_t) 0);
SOCKETS_SetSockOpt(socket, 0, SOCKETS_SO_TRUSTED_SERVER_CERTIFICATE,
SERVER_CERTIFICATE_PEM,
sizeof(SERVER_CERTIFICATE_PEM));
/* Connect to a remote server */
SocketsSockaddr_t server_addr;
server_addr.usPort    = SOCKETS_htons(9001);
server_addr.ulAddress = SOCKETS_inet_addr_quick(192, 168, 0, 3);
if (0 != SOCKETS_Connect(socket, &server_addr, sizeof(server_addr)))
{
/* Could not connect to server. */
    __BKPT(0);
}

/* Send a message and check that the correct number of bytes were transferred */
const char msg[] = "hello, world!\n";
if (sizeof(msg) != SOCKETS_Send(socket, msg, sizeof(msg), 0))
{
/* Failed to send data. */
    __BKPT(0);
}

if (0 != SOCKETS_Shutdown(socket, SOCKETS_SHUT_RDWR))
{
    __BKPT(0);
}

/* Follow socket shutdown example:
 * https://freertos.org/FreRTOS-Plus/FreRTOS\_Plus\_TCP/API/close.html
 */
```

```
while (0 <= SOCKETS_Recv(socket, g_buffer, sizeof(g_buffer), 0))
{
    vTaskDelay(10);
}

SOCKETS_Close(socket);
}

const char * pcApplicationHostnameHook (void)
{
    /* Assign the name "FreeRTOS" to this network node. This function will
    * be called during the DHCP: the machine will be registered with an IP
    * address plus this name. */
    return "FreeRTOS";
}

void vApplicationIPNetworkEventHook (eIPCallbackEvent_t eNetworkEvent)
{
    FSP_PARAMETER_NOT_USED(eNetworkEvent);
}
```

## 4.3 Interfaces

### Detailed Description

The FSP interfaces provide APIs for common functionality. They can be implemented by one or more modules. Modules can use other modules as dependencies using this interface layer.

### Modules

#### ADC Interface

Interface for A/D Converters.

#### BLE Interface

Interface for Bluetooth Low Energy functions.

#### CAC Interface

Interface for clock frequency accuracy measurements.

### CAN Interface

Interface for CAN peripheral.

### CGC Interface

Interface for clock generation.

### Comparator Interface

Interface for comparators.

### CRC Interface

Interface for cyclic redundancy checking.

### CTSU Interface

Interface for Capacitive Touch Sensing Unit (CTSU) functions.

### DAC Interface

Interface for D/A converters.

### Display Interface

Interface for LCD panel displays.

### DOC Interface

Interface for the Data Operation Circuit.

### ELC Interface

Interface for the Event Link Controller.

### Ethernet Interface

Interface for Ethernet functions.

### Ethernet PHY Interface

Interface for Ethernet PHY functions.

**External IRQ Interface**

Interface for detecting external interrupts.

**Flash Interface**

Interface for the Flash Memory.

**I2C Master Interface**

Interface for I2C master communication.

**I2C Slave Interface**

Interface for I2C slave communication.

**I2S Interface**

Interface for I2S audio communication.

**I/O Port Interface**

Interface for accessing I/O ports and configuring I/O functionality.

**JPEG Codec Interface**

Interface for JPEG functions.

**Key Matrix Interface**

Interface for key matrix functions.

**Low Power Modes Interface**

Interface for accessing low power modes.

**Low Voltage Detection Interface**

Interface for Low Voltage Detection.

**OPAMP Interface**

Interface for Operational Amplifiers.

**PDC Interface**



Interface for PDC functions.

#### POEG Interface

Interface for the Port Output Enable for GPT.

#### RTC Interface

Interface for accessing the Realtime Clock.

#### SD/MMC Interface

Interface for accessing SD, eMMC, and SDIO devices.

#### SLCDC Interface

Interface for Segment LCD controllers.

#### SPI Interface

Interface for SPI communications.

#### SPI Flash Interface

Interface for accessing external SPI flash devices.

#### Three-Phase Interface

Interface for three-phase timer functions.

#### Timer Interface

Interface for timer functions.

#### Transfer Interface

Interface for data transfer functions.

#### UART Interface

Interface for UART communications.

#### USB Interface

Interface for USB functions.

### USB HCDC Interface

Interface for USB HCDC functions.

### USB HHID Interface

Interface for USB HHID functions.

### USB HMSC Interface

Interface for USB HMSC functions.

### USB PCDC Interface

Interface for USB PCDC functions.

### USB PHID Interface

Interface for USB PHID functions.

### USB PMSC Interface

Interface for USB PMSC functions.

### WDT Interface

Interface for watch dog timer functions.

### BLE ABS Interface

Interface for Bluetooth Low Energy Abstraction functions.

### Block Media Interface

Interface for block media memory access.

### FreeRTOS+FAT Port Interface

Interface for FreeRTOS+FAT port.

### LittleFS Interface

Interface for LittleFS access.

**MOTOR\_ANGLE Interface**

Interface for motor angle and speed calculation functions.

**Interface**

Interface for motor current functions.

**MOTOR\_DRIVER Interface**

Interface for motor driver functions.

**MOTOR\_SPEED Interface**

Interface for motor speed functions.

**Touch Middleware Interface**

Interface for Touch Middleware functions.

**Virtual EEPROM Interface**

Interface for Virtual EEPROM access.

## 4.3.1 ADC Interface

### Interfaces

#### Detailed Description

Interface for A/D Converters.

## Summary

The ADC interface provides standard ADC functionality including one-shot mode (single scan), continuous scan and group scan. It also allows configuration of hardware and software triggers for starting scans. After each conversion an interrupt can be triggered, and if a callback function is provided, the call back is invoked with the appropriate event information.

Implemented by: [Analog to Digital Converter \(r\\_adc\)](#)

#### Data Structures

```
struct adc\_status\_t
```

```
struct adc_callback_args_t
```

```
struct adc_info_t
```

```
struct adc_cfg_t
```

```
struct adc_api_t
```

```
struct adc_instance_t
```

## Typedefs

```
typedef void adc_ctrl_t
```

## Enumerations

```
enum adc_mode_t
```

```
enum adc_resolution_t
```

```
enum adc_alignment_t
```

```
enum adc_trigger_t
```

```
enum adc_event_t
```

```
enum adc_channel_t
```

```
enum adc_state_t
```

## Data Structure Documentation

### ◆ adc\_status\_t

struct adc_status_t		
ADC status.		
Data Fields		
<a href="#">adc_state_t</a>	state	Current state.

### ◆ adc\_callback\_args\_t

struct adc_callback_args_t		
ADC callback arguments definitions		
Data Fields		
uint16_t	unit	ADC device in use.
<a href="#">adc_event_t</a>	event	ADC callback event.
void const *	p_context	Placeholder for user data.

<a href="#">adc_channel_t</a>	channel	Channel of conversion result. Only valid for ADC_EVENT_CONVERSION_COMPLETE.
-------------------------------	---------	-----------------------------------------------------------------------------

◆ **adc\_info\_t**

struct adc_info_t		
ADC Information Structure for Transfer Interface		
Data Fields		
<a href="#">_l uint16_t *</a>	p_address	The address to start reading the data from.
uint32_t	length	The total number of transfers to read.
<a href="#">transfer_size_t</a>	transfer_size	The size of each transfer.
<a href="#">elc_peripheral_t</a>	elc_peripheral	Name of the peripheral in the ELC list.
<a href="#">elc_event_t</a>	elc_event	Name of the ELC event for the peripheral.
uint32_t	calibration_data	Temperature sensor calibration data (0xFFFFFFFF if unsupported) for reference voltage.
int16_t	slope_microvolts	Temperature sensor slope in microvolts/degrees C.
bool	calibration_ongoing	Calibration is in progress.

◆ **adc\_cfg\_t**

struct adc_cfg_t		
ADC general configuration		
<b>Data Fields</b>		
<a href="#">uint16_t</a>	<a href="#">unit</a>	ADC unit to be used.
<a href="#">adc_mode_t</a>	<a href="#">mode</a>	ADC operation mode.
<a href="#">adc_resolution_t</a>	<a href="#">resolution</a>	ADC resolution.

<code>adc_alignment_t</code>	<code>alignment</code>
	Specify left or right alignment; ignored if addition used.
<code>adc_trigger_t</code>	<code>trigger</code>
	Default and Group A trigger source.
<code>IRQn_Type</code>	<code>scan_end_irq</code>
	Scan end IRQ number.
<code>IRQn_Type</code>	<code>scan_end_b_irq</code>
	Scan end group B IRQ number.
<code>uint8_t</code>	<code>scan_end_ipl</code>
	Scan end interrupt priority.
<code>uint8_t</code>	<code>scan_end_b_ipl</code>
	Scan end group B interrupt priority.
<code>void(*</code>	<code>p_callback</code> )( <code>adc_callback_args_t *p_args</code> )
	Callback function; set to NULL for none.
<code>void const *</code>	<code>p_context</code>
	Placeholder for user data. Passed to the user callback in <code>adc_callback_args_t</code> .
<code>void const *</code>	<code>p_extend</code>
	Extension parameter for hardware specific settings.

◆ **adc\_api\_t**struct `adc_api_t`

ADC functions implemented at the HAL layer will follow this API.

**Data Fields**

<code>fsp_err_t</code> (*	<code>open</code> )( <code>adc_ctrl_t</code> *const p_ctrl, <code>adc_cfg_t</code> const *const p_cfg)
<code>fsp_err_t</code> (*	<code>scanCfg</code> )( <code>adc_ctrl_t</code> *const p_ctrl, void const *const p_extend)
<code>fsp_err_t</code> (*	<code>scanStart</code> )( <code>adc_ctrl_t</code> *const p_ctrl)
<code>fsp_err_t</code> (*	<code>scanStop</code> )( <code>adc_ctrl_t</code> *const p_ctrl)
<code>fsp_err_t</code> (*	<code>scanStatusGet</code> )( <code>adc_ctrl_t</code> *const p_ctrl, <code>adc_status_t</code> *p_status)
<code>fsp_err_t</code> (*	<code>read</code> )( <code>adc_ctrl_t</code> *const p_ctrl, <code>adc_channel_t</code> const reg_id, <code>uint16_t</code> *const p_data)
<code>fsp_err_t</code> (*	<code>read32</code> )( <code>adc_ctrl_t</code> *const p_ctrl, <code>adc_channel_t</code> const reg_id, <code>uint32_t</code> *const p_data)
<code>fsp_err_t</code> (*	<code>calibrate</code> )( <code>adc_ctrl_t</code> *const p_ctrl, void *const p_extend)
<code>fsp_err_t</code> (*	<code>offsetSet</code> )( <code>adc_ctrl_t</code> *const p_ctrl, <code>adc_channel_t</code> const reg_id, <code>int32_t</code> const offset)
<code>fsp_err_t</code> (*	<code>callbackSet</code> )( <code>adc_ctrl_t</code> *const p_api_ctrl, void(*p_callback)( <code>adc_callback_args_t</code> *), void const *const p_context, <code>adc_callback_args_t</code> *const p_callback_memory)
<code>fsp_err_t</code> (*	<code>close</code> )( <code>adc_ctrl_t</code> *const p_ctrl)
<code>fsp_err_t</code> (*	<code>infoGet</code> )( <code>adc_ctrl_t</code> *const p_ctrl, <code>adc_info_t</code> *const p_adc_info)
<code>fsp_err_t</code> (*	<code>versionGet</code> )( <code>fsp_version_t</code> *const p_version)

## Field Documentation

### ◆ open

`fsp_err_t(* adc_api_t::open) (adc_ctrl_t *const p_ctrl, adc_cfg_t const *const p_cfg)`

Initialize ADC Unit; apply power, set the operational mode, trigger sources, interrupt priority, and configurations common to all channels and sensors.

#### Implemented as

- [R\\_ADC\\_Open\(\)](#)
- [R\\_SDADC\\_Open\(\)](#)

#### Precondition

Configure peripheral clocks, ADC pins and IRQs prior to calling this function.

#### Parameters

[in]	p_ctrl	Pointer to control handle structure
[in]	p_cfg	Pointer to configuration structure

### ◆ scanCfg

`fsp_err_t(* adc_api_t::scanCfg) (adc_ctrl_t *const p_ctrl, void const *const p_extend)`

Configure the scan including the channels, groups, and scan triggers to be used for the unit that was initialized in the open call. Some configurations are not supported for all implementations. See implementation for details.

#### Implemented as

- [R\\_ADC\\_ScanCfg\(\)](#)
- [R\\_SDADC\\_ScanCfg\(\)](#)

#### Parameters

[in]	p_ctrl	Pointer to control handle structure
[in]	p_extend	See implementation for details



◆ **scanStart**

```
fsp_err_t(* adc_api_t::scanStart) (adc_ctrl_t *const p_ctrl)
```

Start the scan (in case of a software trigger), or enable the hardware trigger.

**Implemented as**

- R\_ADC\_ScanStart()
- R\_SDADC\_ScanStart()

**Parameters**

[in]	p_ctrl	Pointer to control handle structure
------	--------	-------------------------------------

◆ **scanStop**

```
fsp_err_t(* adc_api_t::scanStop) (adc_ctrl_t *const p_ctrl)
```

Stop the ADC scan (in case of a software trigger), or disable the hardware trigger.

**Implemented as**

- R\_ADC\_ScanStop()
- R\_SDADC\_ScanStop()

**Parameters**

[in]	p_ctrl	Pointer to control handle structure
------	--------	-------------------------------------

◆ **scanStatusGet**

```
fsp_err_t(* adc_api_t::scanStatusGet) (adc_ctrl_t *const p_ctrl, adc_status_t *p_status)
```

Check scan status.

**Implemented as**

- R\_ADC\_StatusGet()
- R\_SDADC\_StatusGet()

**Parameters**

[in]	p_ctrl	Pointer to control handle structure
[out]	p_status	Pointer to store current status in

## ◆ read

```
fsp_err_t(* adc_api_t::read) (adc_ctrl_t *const p_ctrl, adc_channel_t const reg_id, uint16_t *const p_data)
```

Read ADC conversion result.

**Implemented as**

- R\_ADC\_Read()
- R\_SDADC\_Read()

**Parameters**

[in]	p_ctrl	Pointer to control handle structure
[in]	reg_id	ADC channel to read (see enumeration adc_channel_t)
[in]	p_data	Pointer to variable to load value into.

## ◆ read32

```
fsp_err_t(* adc_api_t::read32) (adc_ctrl_t *const p_ctrl, adc_channel_t const reg_id, uint32_t *const p_data)
```

Read ADC conversion result into a 32-bit word.

**Implemented as**

- R\_SDADC\_Read32()

**Parameters**

[in]	p_ctrl	Pointer to control handle structure
[in]	reg_id	ADC channel to read (see enumeration adc_channel_t)
[in]	p_data	Pointer to variable to load value into.

◆ **calibrate**

```
fsp_err_t(* adc_api_t::calibrate) (adc_ctrl_t *const p_ctrl, void *const p_extend)
```

Calibrate ADC or associated PGA (programmable gain amplifier). The driver may require implementation specific arguments to the p\_extend input. Not supported for all implementations. See implementation for details.

**Implemented as**

- [R\\_SDADC\\_Calibrate\(\)](#)

**Parameters**

[in]	p_ctrl	Pointer to control handle structure
[in]	p_extend	Pointer to implementation specific arguments

◆ **offsetSet**

```
fsp_err_t(* adc_api_t::offsetSet) (adc_ctrl_t *const p_ctrl, adc_channel_t const reg_id, int32_t const offset)
```

Set offset for input PGA configured for differential input. Not supported for all implementations. See implementation for details.

**Implemented as**

- [R\\_SDADC\\_OffsetSet\(\)](#)

**Parameters**

[in]	p_ctrl	Pointer to control handle structure
[in]	reg_id	ADC channel to read (see enumeration adc_channel_t)
[in]	offset	See implementation for details.

◆ **callbackSet**

```
fsp_err_t(* adc_api_t::callbackSet) (adc_ctrl_t *const p_api_ctrl,
void(*p_callback)(adc_callback_args_t *), void const *const p_context, adc_callback_args_t *const
p_callback_memory)
```

Specify callback function and optional context pointer and working memory pointer.

**Implemented as**

- R\_ADC\_CallbackSet()

**Parameters**

[in]	p_ctrl	Pointer to the ADC control block.
[in]	p_callback	Callback function
[in]	p_context	Pointer to send to callback function
[in]	p_working_memory	Pointer to volatile memory where callback structure can be allocated. Callback arguments allocated here are only valid during the callback.

◆ **close**

```
fsp_err_t(* adc_api_t::close) (adc_ctrl_t *const p_ctrl)
```

Close the specified ADC unit by ending any scan in progress, disabling interrupts, and removing power to the specified A/D unit.

**Implemented as**

- R\_ADC\_Close()
- R\_SDADC\_Close()

**Parameters**

[in]	p_ctrl	Pointer to control handle structure
------	--------	-------------------------------------

## ◆ infoGet

```
fsp_err_t(* adc_api_t::infoGet) (adc_ctrl_t *const p_ctrl, adc_info_t *const p_adc_info)
```

Return the ADC data register address of the first (lowest number) channel and the total number of bytes to be read in order for the DTC/DMAC to read the conversion results of all configured channels. Return the temperature sensor calibration and slope data.

**Implemented as**

- R\_ADC\_InfoGet()
- R\_SDADC\_InfoGet()

**Parameters**

[in]	p_ctrl	Pointer to control handle structure
[out]	p_adc_info	Pointer to ADC information structure

## ◆ versionGet

```
fsp_err_t(* adc_api_t::versionGet) (fsp_version_t *const p_version)
```

Retrieve the API version.

**Implemented as**

- R\_ADC\_VersionGet()
- R\_SDADC\_VersionGet()

**Precondition**

This function retrieves the API version.

**Parameters**

[in]	p_version	Pointer to version structure
------	-----------	------------------------------

## ◆ adc\_instance\_t

```
struct adc_instance_t
```

This structure encompasses everything that is needed to use an instance of this interface.

## Data Fields

adc_ctrl_t *	p_ctrl	Pointer to the control structure for this instance.
adc_cfg_t const *	p_cfg	Pointer to the configuration structure for this instance.
void const *	p_channel_cfg	Pointer to the channel configuration structure for this instance.
adc_api_t const *	p_api	Pointer to the API structure for this instance.

## Typedef Documentation

### ◆ `adc_ctrl_t`

```
typedef void adc_ctrl_t
```

ADC control block. Allocate using driver instance control structure from driver instance header file.

## Enumeration Type Documentation

### ◆ `adc_mode_t`

```
enum adc_mode_t
```

ADC operation mode definitions

Enumerator

<code>ADC_MODE_SINGLE_SCAN</code>	Single scan - one or more channels.
<code>ADC_MODE_GROUP_SCAN</code>	Two trigger sources to trigger scan for two groups which contain one or more channels.
<code>ADC_MODE_CONTINUOUS_SCAN</code>	Continuous scan - one or more channels.

### ◆ `adc_resolution_t`

```
enum adc_resolution_t
```

ADC data resolution definitions

Enumerator

<code>ADC_RESOLUTION_12_BIT</code>	12 bit resolution
<code>ADC_RESOLUTION_10_BIT</code>	10 bit resolution
<code>ADC_RESOLUTION_8_BIT</code>	8 bit resolution
<code>ADC_RESOLUTION_14_BIT</code>	14 bit resolution
<code>ADC_RESOLUTION_16_BIT</code>	16 bit resolution
<code>ADC_RESOLUTION_24_BIT</code>	24 bit resolution

◆ **adc\_alignment\_t**

enum <a href="#">adc_alignment_t</a>	
ADC data alignment definitions	
Enumerator	
ADC_ALIGNMENT_RIGHT	Data alignment right.
ADC_ALIGNMENT_LEFT	Data alignment left.

◆ **adc\_trigger\_t**

enum <a href="#">adc_trigger_t</a>	
ADC trigger mode definitions	
Enumerator	
ADC_TRIGGER_SOFTWARE	Software trigger; not for group modes.
ADC_TRIGGER_SYNC_ELC	Synchronous trigger via ELC.
ADC_TRIGGER_ASYNC_EXTERNAL	External asynchronous trigger; not for group modes.

◆ **adc\_event\_t**

enum <a href="#">adc_event_t</a>	
ADC callback event definitions	
Enumerator	
ADC_EVENT_SCAN_COMPLETE	Normal/Group A scan complete.
ADC_EVENT_SCAN_COMPLETE_GROUP_B	Group B scan complete.
ADC_EVENT_CALIBRATION_COMPLETE	Calibration complete.
ADC_EVENT_CONVERSION_COMPLETE	Conversion complete.

◆ **adc\_channel\_t**

enum <code>adc_channel_t</code>	
ADC channels	
Enumerator	
<code>ADC_CHANNEL_0</code>	ADC channel 0.
<code>ADC_CHANNEL_1</code>	ADC channel 1.
<code>ADC_CHANNEL_2</code>	ADC channel 2.
<code>ADC_CHANNEL_3</code>	ADC channel 3.
<code>ADC_CHANNEL_4</code>	ADC channel 4.
<code>ADC_CHANNEL_5</code>	ADC channel 5.
<code>ADC_CHANNEL_6</code>	ADC channel 6.
<code>ADC_CHANNEL_7</code>	ADC channel 7.
<code>ADC_CHANNEL_8</code>	ADC channel 8.
<code>ADC_CHANNEL_9</code>	ADC channel 9.
<code>ADC_CHANNEL_10</code>	ADC channel 10.
<code>ADC_CHANNEL_11</code>	ADC channel 11.
<code>ADC_CHANNEL_12</code>	ADC channel 12.
<code>ADC_CHANNEL_13</code>	ADC channel 13.
<code>ADC_CHANNEL_14</code>	ADC channel 14.
<code>ADC_CHANNEL_15</code>	ADC channel 15.
<code>ADC_CHANNEL_16</code>	ADC channel 16.
<code>ADC_CHANNEL_17</code>	ADC channel 17.
<code>ADC_CHANNEL_18</code>	ADC channel 18.
<code>ADC_CHANNEL_19</code>	ADC channel 19.
<code>ADC_CHANNEL_20</code>	ADC channel 20.



ADC_CHANNEL_21	ADC channel 21.
ADC_CHANNEL_22	ADC channel 22.
ADC_CHANNEL_23	ADC channel 23.
ADC_CHANNEL_24	ADC channel 24.
ADC_CHANNEL_25	ADC channel 25.
ADC_CHANNEL_26	ADC channel 26.
ADC_CHANNEL_27	ADC channel 27.
ADC_CHANNEL_DUPLEX_A	Data duplexing register A.
ADC_CHANNEL_DUPLEX_B	Data duplexing register B.
ADC_CHANNEL_DUPLEX	Data duplexing register.
ADC_CHANNEL_TEMPERATURE	Temperature sensor output.
ADC_CHANNEL_VOLT	Internal reference voltage.

#### ◆ adc\_state\_t

enum <code>adc_state_t</code>	
ADC states.	
Enumerator	
ADC_STATE_IDLE	ADC is idle.
ADC_STATE_SCAN_IN_PROGRESS	ADC scan in progress.

## 4.3.2 BLE Interface

### Interfaces

#### Detailed Description

Interface for Bluetooth Low Energy functions.

## Summary

The BLE interface for the Bluetooth Low Energy (BLE) peripheral provides Bluetooth Low Energy functionality.

The Bluetooth Low Energy interface can be implemented by:

- [Bluetooth Low Energy Library \(r\\_ble\)](#)

### Macros

```
#define BLE_VERSION_MAJOR
```

```
#define BLE_VERSION_MINOR
```

```
#define BLE_LIB_ALL_FEATS
```

```
#define BLE_LIB_BALANCE
```

```
#define BLE_LIB_COMPACT
```

### Macro Definition Documentation

#### ◆ BLE\_VERSION\_MAJOR

```
#define BLE_VERSION_MAJOR
```

BLE Module Major Version.

#### ◆ BLE\_VERSION\_MINOR

```
#define BLE_VERSION_MINOR
```

BLE Module Minor Version.

#### ◆ BLE\_LIB\_ALL\_FEATS

```
#define BLE_LIB_ALL_FEATS
```

BLE Protocol Stack Library All Features type.

#### ◆ BLE\_LIB\_BALANCE

```
#define BLE_LIB_BALANCE
```

BLE Protocol Stack Library Balance type.

## ◆ BLE\_LIB\_COMPACT

```
#define BLE_LIB_COMPACT
```

BLE Protocol Stack Library Compacity type.

### 4.3.3 CAC Interface

#### Interfaces

#### Detailed Description

Interface for clock frequency accuracy measurements.

## Summary

The interface for the clock frequency accuracy measurement circuit (CAC) peripheral is used to check a system clock frequency with a reference clock signal by counting the number of pulses of the clock to be measured.

Implemented by: [Clock Frequency Accuracy Measurement Circuit \(r\\_cac\)](#)

#### Data Structures

struct [cac\\_ref\\_clock\\_config\\_t](#)

struct [cac\\_meas\\_clock\\_config\\_t](#)

struct [cac\\_callback\\_args\\_t](#)

struct [cac\\_cfg\\_t](#)

struct [cac\\_api\\_t](#)

struct [cac\\_instance\\_t](#)

#### Typedefs

typedef void [cac\\_ctrl\\_t](#)

#### Enumerations

enum [cac\\_event\\_t](#)

enum [cac\\_clock\\_type\\_t](#)

enum [cac\\_clock\\_source\\_t](#)

enum [cac\\_ref\\_divider\\_t](#)enum [cac\\_ref\\_digfilter\\_t](#)enum [cac\\_ref\\_edge\\_t](#)enum [cac\\_meas\\_divider\\_t](#)

## Data Structure Documentation

### ◆ [cac\\_ref\\_clock\\_config\\_t](#)

struct [cac\\_ref\\_clock\\_config\\_t](#)

Structure defining the settings that apply to reference clock configuration.

#### Data Fields

<a href="#">cac_ref_divider_t</a>	divider	Divider specification for the Reference clock.
<a href="#">cac_clock_source_t</a>	clock	Clock source for the Reference clock.
<a href="#">cac_ref_digfilter_t</a>	digfilter	Digital filter selection for the CACREF ext clock.
<a href="#">cac_ref_edge_t</a>	edge	Edge detection for the Reference clock.

### ◆ [cac\\_meas\\_clock\\_config\\_t](#)

struct [cac\\_meas\\_clock\\_config\\_t](#)

Structure defining the settings that apply to measurement clock configuration.

#### Data Fields

<a href="#">cac_meas_divider_t</a>	divider	Divider specification for the Measurement clock.
<a href="#">cac_clock_source_t</a>	clock	Clock source for the Measurement clock.

### ◆ [cac\\_callback\\_args\\_t](#)

struct [cac\\_callback\\_args\\_t](#)

Callback function parameter data

#### Data Fields

<a href="#">cac_event_t</a>	event	The event can be used to identify what caused the callback.
void const *	p_context	Value provided in configuration structure.

◆ **cac\_cfg\_t**

struct cac_cfg_t	
CAC Configuration	
<b>Data Fields</b>	
<a href="#">cac_ref_clock_config_t</a>	<a href="#">cac_ref_clock</a>
	Reference clock specific settings.
<a href="#">cac_meas_clock_config_t</a>	<a href="#">cac_meas_clock</a>
	Measurement clock specific settings.
<a href="#">uint16_t</a>	<a href="#">cac_upper_limit</a>
	The upper limit counter threshold.
<a href="#">uint16_t</a>	<a href="#">cac_lower_limit</a>
	The lower limit counter threshold.
<a href="#">IRQn_Type</a>	<a href="#">mendi_irq</a>
	Measurement End IRQ number.
<a href="#">IRQn_Type</a>	<a href="#">ovfi_irq</a>
	Measurement Overflow IRQ number.
<a href="#">IRQn_Type</a>	<a href="#">ferri_irq</a>
	Frequency Error IRQ number.
<a href="#">uint8_t</a>	<a href="#">mendi_ipl</a>
	Measurement end interrupt priority.
<a href="#">uint8_t</a>	<a href="#">ovfi_ipl</a>

	Overflow interrupt priority.
uint8_t	<a href="#">ferri_ipl</a>
	Frequency error interrupt priority.
void(*	<a href="#">p_callback</a> )(cac_callback_args_t *p_args)
	Callback provided when a CAC interrupt ISR occurs.
void const *	<a href="#">p_context</a>
	Passed to user callback in <a href="#">cac_callback_args_t</a> .
void const *	<a href="#">p_extend</a>
	CAC hardware dependent configuration */.

#### ◆ cac\_api\_t

struct cac_api_t	
CAC functions implemented at the HAL layer API	
<b>Data Fields</b>	
<a href="#">fsp_err_t</a> (*	<a href="#">open</a> )(cac_ctrl_t *const p_ctrl, <a href="#">cac_cfg_t</a> const *const p_cfg)
<a href="#">fsp_err_t</a> (*	<a href="#">startMeasurement</a> )(cac_ctrl_t *const p_ctrl)
<a href="#">fsp_err_t</a> (*	<a href="#">stopMeasurement</a> )(cac_ctrl_t *const p_ctrl)
<a href="#">fsp_err_t</a> (*	<a href="#">read</a> )(cac_ctrl_t *const p_ctrl, uint16_t *const p_counter)
<a href="#">fsp_err_t</a> (*	<a href="#">callbackSet</a> )(cac_ctrl_t *const p_api_ctrl, void(*p_callback)(cac_callback_args_t *), void const *const p_context, <a href="#">cac_callback_args_t</a> *const p_callback_memory)
<a href="#">fsp_err_t</a> (*	<a href="#">close</a> )(cac_ctrl_t *const p_ctrl)

```
fsp_err_t(* versionGet )(fsp_version_t *p_version)
```

## Field Documentation

### ◆ open

```
fsp_err_t(* cac_api_t::open) (cac_ctrl_t *const p_ctrl, cac_cfg_t const *const p_cfg)
```

Open function for CAC device.

#### Parameters

[out]	p_ctrl	Pointer to CAC device control. Must be declared by user.
[in]	cac_cfg_t	Pointer to CAC configuration structure.

### ◆ startMeasurement

```
fsp_err_t(* cac_api_t::startMeasurement) (cac_ctrl_t *const p_ctrl)
```

Begin a measurement for the CAC peripheral.

#### Parameters

[in]	p_ctrl	Pointer to CAC device control.
------	--------	--------------------------------

### ◆ stopMeasurement

```
fsp_err_t(* cac_api_t::stopMeasurement) (cac_ctrl_t *const p_ctrl)
```

End a measurement for the CAC peripheral.

#### Parameters

[in]	p_ctrl	Pointer to CAC device control.
------	--------	--------------------------------

## ◆ read

```
fsp_err_t(* cac_api_t::read) (cac_ctrl_t *const p_ctrl, uint16_t *const p_counter)
```

Read function for CAC peripheral.

**Parameters**

[in]	p_ctrl	Control for the CAC device context.
[in]	p_counter	Pointer to variable in which to store the current CACNTBR register contents.

## ◆ callbackSet

```
fsp_err_t(* cac_api_t::callbackSet) (cac_ctrl_t *const p_api_ctrl,
void(*p_callback)(cac_callback_args_t *), void const *const p_context, cac_callback_args_t *const
p_callback_memory)
```

Specify callback function and optional context pointer and working memory pointer.

**Implemented as**

- R\_CAC\_CallbackSet()

**Parameters**

[in]	p_ctrl	Control block set in <a href="#">cac_api_t::open</a> call
[in]	p_callback	Callback function to register
[in]	p_context	Pointer to send to callback function
[in]	p_working_memory	Pointer to volatile memory where callback structure can be allocated. Callback arguments allocated here are only valid during the callback.

## ◆ close

```
fsp_err_t(* cac_api_t::close) (cac_ctrl_t *const p_ctrl)
```

Close function for CAC device.

**Parameters**

[in]	p_ctrl	Pointer to CAC device control.
------	--------	--------------------------------



◆ **versionGet**

```
fsp_err_t(* cac_api_t::versionGet) (fsp_version_t *p_version)
```

Get the CAC API and code version information.

**Parameters**

[out]	p_version	is value returned.
-------	-----------	--------------------

◆ **cac\_instance\_t**

```
struct cac_instance_t
```

This structure encompasses everything that is needed to use an instance of this interface.

## Data Fields

<code>cac_ctrl_t *</code>	p_ctrl	Pointer to the control structure for this instance.
<code>cac_cfg_t const *</code>	p_cfg	Pointer to the configuration structure for this instance.
<code>cac_api_t const *</code>	p_api	Pointer to the API structure for this instance.

**Typedef Documentation**◆ **cac\_ctrl\_t**

```
typedef void cac_ctrl_t
```

CAC control block. Allocate an instance specific control block to pass into the CAC API calls.

**Implemented as**

- [cac\\_instance\\_ctrl\\_t](#)

**Enumeration Type Documentation**◆ **cac\_event\_t**

```
enum cac_event_t
```

Event types returned by the ISR callback when used in CAC interrupt mode

## Enumerator

CAC_EVENT_FREQUENCY_ERROR	Frequency error.
CAC_EVENT_MEASUREMENT_COMPLETE	Measurement complete.
CAC_EVENT_COUNTER_OVERFLOW	Counter overflow.

◆ **cac\_clock\_type\_t**

enum <code>cac_clock_type_t</code>	
Enumeration of the two possible clocks.	
Enumerator	
<code>CAC_CLOCK_MEASURED</code>	Measurement clock.
<code>CAC_CLOCK_REFERENCE</code>	Reference clock.

◆ **cac\_clock\_source\_t**

enum <code>cac_clock_source_t</code>	
Enumeration of the possible clock sources for both the reference and measurement clocks.	
Enumerator	
<code>CAC_CLOCK_SOURCE_MAIN_OSC</code>	Main clock oscillator.
<code>CAC_CLOCK_SOURCE_SUBCLOCK</code>	Sub-clock.
<code>CAC_CLOCK_SOURCE_HOCO</code>	HOCO (High speed on chip oscillator)
<code>CAC_CLOCK_SOURCE_MOCO</code>	MOCO (Middle speed on chip oscillator)
<code>CAC_CLOCK_SOURCE_LOCO</code>	LOCO (Low speed on chip oscillator)
<code>CAC_CLOCK_SOURCE_PCLKB</code>	PCLKB (Peripheral Clock B)
<code>CAC_CLOCK_SOURCE_IWDT</code>	IWDT-dedicated on-chip oscillator.
<code>CAC_CLOCK_SOURCE_EXTERNAL</code>	Externally supplied measurement clock on CACREF pin.

◆ **cac\_ref\_divider\_t**

enum <code>cac_ref_divider_t</code>	
Enumeration of available dividers for the reference clock.	
Enumerator	
<code>CAC_REF_DIV_32</code>	Reference clock divided by 32.
<code>CAC_REF_DIV_128</code>	Reference clock divided by 128.
<code>CAC_REF_DIV_1024</code>	Reference clock divided by 1024.
<code>CAC_REF_DIV_8192</code>	Reference clock divided by 8192.

◆ **cac\_ref\_digfilter\_t**

enum <code>cac_ref_digfilter_t</code>	
Enumeration of available digital filter settings for an external reference clock.	
Enumerator	
<code>CAC_REF_DIGITAL_FILTER_OFF</code>	No digital filter on the CACREF pin for reference clock.
<code>CAC_REF_DIGITAL_FILTER_1</code>	Sampling clock for digital filter = measuring frequency.
<code>CAC_REF_DIGITAL_FILTER_4</code>	Sampling clock for digital filter = measuring frequency/4.
<code>CAC_REF_DIGITAL_FILTER_16</code>	Sampling clock for digital filter = measuring frequency/16.

◆ **cac\_ref\_edge\_t**

enum <code>cac_ref_edge_t</code>	
Enumeration of available edge detect settings for the reference clock.	
Enumerator	
<code>CAC_REF_EDGE_RISE</code>	Rising edge detect for the Reference clock.
<code>CAC_REF_EDGE_FALL</code>	Falling edge detect for the Reference clock.
<code>CAC_REF_EDGE_BOTH</code>	Both Rising and Falling edges detect for the Reference clock.

◆ **cac\_meas\_divider\_t**

enum <code>cac_meas_divider_t</code>	
Enumeration of available dividers for the measurement clock	
Enumerator	
<code>CAC_MEAS_DIV_1</code>	Measurement clock divided by 1.
<code>CAC_MEAS_DIV_4</code>	Measurement clock divided by 4.
<code>CAC_MEAS_DIV_8</code>	Measurement clock divided by 8.
<code>CAC_MEAS_DIV_32</code>	Measurement clock divided by 32.

## 4.3.4 CAN Interface

### Interfaces

#### Detailed Description

Interface for CAN peripheral.

## Summary

The CAN interface provides common APIs for CAN HAL drivers. CAN interface supports following features.

- Full-duplex CAN communication
- Generic CAN parameter setting

- Interrupt driven transmit/receive processing
- Callback function support with returning event code
- Hardware resource locking during a transaction

Implemented by: [Controller Area Network \(r\\_can\)](#)

## Data Structures

struct [can\\_bit\\_timing\\_cfg\\_t](#)

struct [can\\_frame\\_t](#)

struct [can\\_mailbox\\_t](#)

struct [can\\_callback\\_args\\_t](#)

struct [can\\_cfg\\_t](#)

struct [can\\_api\\_t](#)

struct [can\\_instance\\_t](#)

## Typedefs

typedef uint32\_t [can\\_id\\_t](#)

typedef void [can\\_ctrl\\_t](#)

## Enumerations

enum [can\\_event\\_t](#)

enum [can\\_status\\_t](#)

enum [can\\_error\\_t](#)

enum [can\\_operation\\_mode\\_t](#)

enum [can\\_test\\_mode\\_t](#)

enum [can\\_id\\_mode\\_t](#)

enum [can\\_frame\\_type\\_t](#)

enum [can\\_message\\_mode\\_t](#)

enum [can\\_clock\\_source\\_t](#)

enum [can\\_time\\_segment1\\_t](#)

enum [can\\_time\\_segment2\\_t](#)

enum [can\\_sync\\_jump\\_width\\_t](#)enum [can\\_mailbox\\_send\\_receive\\_t](#)**Data Structure Documentation****◆ can\_bit\_timing\_cfg\_t**

struct <a href="#">can_bit_timing_cfg_t</a>		
CAN bit rate configuration.		
Data Fields		
<a href="#">uint32_t</a>	baud_rate_prescaler	Baud rate prescaler. Valid values: 1 - 1024.
<a href="#">can_time_segment1_t</a>	time_segment_1	Time segment 1 control.
<a href="#">can_time_segment2_t</a>	time_segment_2	Time segment 2 control.
<a href="#">can_sync_jump_width_t</a>	synchronization_jump_width	Synchronization jump width.

**◆ can\_frame\_t**

struct <a href="#">can_frame_t</a>		
CAN data Frame		
Data Fields		
<a href="#">can_id_t</a>	id	CAN id.
<a href="#">uint8_t</a>	data_length_code	CAN Data Length code, number of bytes in the message.
<a href="#">uint8_t</a>	data[8]	CAN data, up to 8 bytes.
<a href="#">can_frame_type_t</a>	type	Frame type, data or remote frame.

**◆ can\_mailbox\_t**

struct <a href="#">can_mailbox_t</a>		
CAN Mailbox		
Data Fields		
<a href="#">can_id_t</a>	mailbox_id	Mailbox ID.
<a href="#">can_mailbox_send_receive_t</a>	mailbox_type	Receive or Transmit mailbox type.
<a href="#">can_frame_type_t</a>	frame_type	Frame type for receive mailbox.

**◆ can\_callback\_args\_t**

struct <a href="#">can_callback_args_t</a>		
CAN callback parameter definition		

Data Fields		
uint32_t	channel	Device channel number.
can_event_t	event	Event code.
uint32_t	mailbox	Mailbox number of interrupt source.
can_frame_t *	p_frame	Pointer to the received frame.
void const *	p_context	Context provided to user during callback.

## ◆ can\_cfg\_t

struct can_cfg_t		
CAN Configuration		
<b>Data Fields</b>		
uint32_t	channel	
		CAN channel.
can_bit_timing_cfg_t *	p_bit_timing	
		CAN bit timing.
can_id_mode_t	id_mode	
		Standard or Extended ID mode.
uint32_t	mailbox_count	
		Number of mailboxes.
can_mailbox_t *	p_mailbox	
		Pointer to mailboxes.
can_message_mode_t	message_mode	
		Overwrite message or overrun.

<code>can_operation_mode_t</code>	<code>operation_mode</code>
	CAN operation mode.
<code>can_test_mode_t</code>	<code>test_mode</code>
	CAN operation mode.
<code>void(*</code>	<code>p_callback )(can_callback_args_t *p_args)</code>
	Pointer to callback function.
<code>void const *</code>	<code>p_context</code>
	User defined callback context.
<code>void const *</code>	<code>p_extend</code>
	CAN hardware dependent configuration.
<code>uint8_t</code>	<code>ipl</code>
	Error/Transmit/Receive interrupt priority.
<code>IRQn_Type</code>	<code>error_irq</code>
	Error IRQ number.
<code>IRQn_Type</code>	<code>mailbox_rx_irq</code>
	Receive mailbox IRQ number.
<code>IRQn_Type</code>	<code>mailbox_tx_irq</code>
	Transmit mailbox IRQ number.

#### ◆ `can_api_t`



struct can_api_t		
Shared Interface definition for CAN		
<b>Data Fields</b>		
fsp_err_t(*)	open	(can_ctrl_t *const p_ctrl, can_cfg_t const *const p_cfg)
fsp_err_t(*)	write	(can_ctrl_t *const p_ctrl, uint32_t mailbox, can_frame_t *const p_frame)
fsp_err_t(*)	close	(can_ctrl_t *const p_ctrl)
fsp_err_t(*)	modeTransition	(can_ctrl_t *const p_api_ctrl, can_operation_mode_t operation_mode, can_test_mode_t test_mode)
fsp_err_t(*)	infoGet	(can_ctrl_t *const p_ctrl, can_info_t *const p_info)
fsp_err_t(*)	callbackSet	(can_ctrl_t *const p_api_ctrl, void(*p_callback)(can_callback_args_t *), void const *const p_context, can_callback_args_t *const p_callback_memory)
fsp_err_t(*)	versionGet	(fsp_version_t *const p_version)
<b>Field Documentation</b>		
◆ <b>open</b>		
fsp_err_t(*) can_api_t::open (can_ctrl_t *const p_ctrl, can_cfg_t const *const p_cfg)		
Open function for CAN device		
<b>Implemented as</b>		
◦ R_CAN_Open()		
<b>Parameters</b>		
[in,out]	p_ctrl	Pointer to the CAN control block. Must be declared by user. Value set here.
[in]	can_cfg_t	Pointer to CAN configuration structure. All elements of this structure must be set by user.

## ◆ write

```
fsp_err_t(* can_api_t::write) (can_ctrl_t *const p_ctrl, uint32_t mailbox, can_frame_t *const p_frame)
```

Write function for CAN device

**Implemented as**

- R\_CAN\_Write()

**Parameters**

[in]	p_ctrl	Pointer to the CAN control block.
[in]	mailbox	Mailbox (number) to write to.
[in]	p_frame	Pointer for frame of CAN ID, DLC, data and frame type to write.

## ◆ close

```
fsp_err_t(* can_api_t::close) (can_ctrl_t *const p_ctrl)
```

Close function for CAN device

**Implemented as**

- R\_CAN\_Close()

**Parameters**

[in]	p_ctrl	Pointer to the CAN control block.
------	--------	-----------------------------------

## ◆ modeTransition

```
fsp_err_t(* can_api_t::modeTransition) (can_ctrl_t *const p_api_ctrl, can_operation_mode_t operation_mode, can_test_mode_t test_mode)
```

Mode Transition function for CAN device

**Implemented as**

- R\_CAN\_ModeTransition()

**Parameters**

[in]	p_ctrl	Pointer to the CAN control block.
[in]	operation_mode	Destination CAN operation state.
[in]	test_mode	Destination CAN test state.

## ◆ infoGet

```
fsp_err_t(* can_api_t::infoGet) (can_ctrl_t *const p_ctrl, can_info_t *const p_info)
```

Get CAN channel info.

**Implemented as**

- R\_CAN\_InfoGet()

**Parameters**

[in]	p_ctrl	Handle for channel (pointer to channel control block)
[out]	p_info	Memory address to return channel specific data to.

## ◆ callbackSet

```
fsp_err_t(* can_api_t::callbackSet) (can_ctrl_t *const p_api_ctrl,
void(*p_callback)(can_callback_args_t *), void const *const p_context, can_callback_args_t *const
p_callback_memory)
```

Specify callback function and optional context pointer and working memory pointer.

**Implemented as**

- R\_CAN\_CallbackSet()

**Parameters**

[in]	p_ctrl	Control block set in <a href="#">can_api_t::open</a> call.
[in]	p_callback	Callback function to register
[in]	p_context	Pointer to send to callback function
[in]	p_working_memory	Pointer to volatile memory where callback structure can be allocated. Callback arguments allocated here are only valid during the callback.

◆ **versionGet**

```
fsp_err_t(* can_api_t::versionGet) (fsp_version_t *const p_version)
```

Version get function for CAN device

**Implemented as**

- R\_CAN\_VersionGet()

**Parameters**

[in]	p_version	Pointer to the memory to store the version information
------	-----------	--------------------------------------------------------

◆ **can\_instance\_t**

```
struct can_instance_t
```

This structure encompasses everything that is needed to use an instance of this interface.

## Data Fields

<code>can_ctrl_t *</code>	p_ctrl	Pointer to the control structure for this instance.
<code>can_cfg_t const *</code>	p_cfg	Pointer to the configuration structure for this instance.
<code>can_api_t const *</code>	p_api	Pointer to the API structure for this instance.

**Typedef Documentation**◆ **can\_id\_t**

```
typedef uint32_t can_id_t
```

CAN Id

◆ **can\_ctrl\_t**

```
typedef void can_ctrl_t
```

CAN control block. Allocate an instance specific control block to pass into the CAN API calls.

**Implemented as**

- can\_instance\_ctrl\_t

**Enumeration Type Documentation**

◆ **can\_event\_t**

enum <code>can_event_t</code>	
CAN event codes	
Enumerator	
<code>CAN_EVENT_ERR_WARNING</code>	Error Warning event.
<code>CAN_EVENT_ERR_PASSIVE</code>	Error Passive event.
<code>CAN_EVENT_ERR_BUS_OFF</code>	Bus Off event.
<code>CAN_EVENT_BUS_RECOVERY</code>	Bus Off Recovery event.
<code>CAN_EVENT_MAILBOX_MESSAGE_LOST</code>	Mailbox has been overrun.
<code>CAN_EVENT_RX_COMPLETE</code>	Receive complete event.
<code>CAN_EVENT_TX_COMPLETE</code>	Transmit complete event.

◆ **can\_status\_t**

enum <code>can_status_t</code>	
CAN Status	
Enumerator	
<code>CAN_STATUS_NEW_DATA</code>	New Data status flag.
<code>CAN_STATUS_SENT_DATA</code>	Sent Data status flag.
<code>CAN_STATUS_RECEIVE_FIFO</code>	Receive FIFO status flag (Not supported)
<code>CAN_STATUS_TRANSMIT_FIFO</code>	Transmit FIFO status flag (Not supported)
<code>CAN_STATUS_NORMAL_MBOX_MESSAGE_LOST</code>	Normal mailbox message lost status flag.
<code>CAN_STATUS_FIFO_MBOX_MESSAGE_LOST</code>	FIFO mailbox message lost status flag (Not Supported)
<code>CAN_STATUS_TRANSMISSION_ABORT</code>	Transmission abort status flag.
<code>CAN_STATUS_ERROR</code>	Error status flag.
<code>CAN_STATUS_RESET_MODE</code>	Reset mode status flag.
<code>CAN_STATUS_HALT_MODE</code>	Halt mode status flag.
<code>CAN_STATUS_SLEEP_MODE</code>	Sleep mode status flag.
<code>CAN_STATUS_ERROR_PASSIVE</code>	Error-passive status flag.
<code>CAN_STATUS_BUS_OFF</code>	Bus-off status flag.

◆ **can\_error\_t**

enum <code>can_error_t</code>	
CAN Error Code	
Enumerator	
<code>CAN_ERROR_STUFF</code>	Stuff Error.
<code>CAN_ERROR_FORM</code>	Form Error.
<code>CAN_ERROR_ACK</code>	ACK Error.
<code>CAN_ERROR_CRC</code>	CRC Error.
<code>CAN_ERROR_BIT_RECESSIVE</code>	Bit Error (recessive) Error.
<code>CAN_ERROR_BIT_DOMINANT</code>	Bit Error (dominant) Error.
<code>CAN_ERROR_ACK_DELIMITER</code>	ACK Delimiter Error.
<code>CAN_ERROR_ERROR_DISPLAY_MODE</code>	Error Display mode.

◆ **can\_operation\_mode\_t**

enum <code>can_operation_mode_t</code>	
CAN Operation modes	
Enumerator	
<code>CAN_OPERATION_MODE_NORMAL</code>	CAN Normal Operation Mode.
<code>CAN_OPERATION_MODE_RESET</code>	CAN Reset Operation Mode.
<code>CAN_OPERATION_MODE_HALT</code>	CAN Halt Operation Mode.
<code>CAN_OPERATION_MODE_SLEEP</code>	CAN SLEEP Operation Mode.

◆ **can\_test\_mode\_t**

enum <code>can_test_mode_t</code>	
CAN Test modes	
Enumerator	
<code>CAN_TEST_MODE_DISABLED</code>	CAN Test Mode Disabled.
<code>CAN_TEST_MODE_LISTEN</code>	CAN Test Listen Mode.
<code>CAN_TEST_MODE_LOOPBACK_EXTERNAL</code>	CAN Test External Loopback Mode.
<code>CAN_TEST_MODE_LOOPBACK_INTERNAL</code>	CAN Test Internal Loopback Mode.

◆ **can\_id\_mode\_t**

enum <code>can_id_mode_t</code>	
CAN ID modes	
Enumerator	
<code>CAN_ID_MODE_STANDARD</code>	Standard IDs of 11 bits used.
<code>CAN_ID_MODE_EXTENDED</code>	Extended IDs of 29 bits used.

◆ **can\_frame\_type\_t**

enum <code>can_frame_type_t</code>	
CAN frame types	
Enumerator	
<code>CAN_FRAME_TYPE_DATA</code>	Data frame type.
<code>CAN_FRAME_TYPE_REMOTE</code>	Remote frame type.



◆ **can\_message\_mode\_t**

enum <code>can_message_mode_t</code>	
CAN Message Modes	
Enumerator	
<code>CAN_MESSAGE_MODE_OVERWRITE</code>	Receive data will be overwritten if not read before the next frame.
<code>CAN_MESSAGE_MODE_OVERRUN</code>	Receive data will be retained until it is read.

◆ **can\_clock\_source\_t**

enum <code>can_clock_source_t</code>	
CAN Source Clock	
Enumerator	
<code>CAN_CLOCK_SOURCE_PCLKB</code>	PCLKB is the source of the CAN Clock.
<code>CAN_CLOCK_SOURCE_CANMCLK</code>	CANMCLK is the source of the CAN Clock.

◆ **can\_time\_segment1\_t**

enum <code>can_time_segment1_t</code>	
CAN Time Segment 1 Time Quanta	
Enumerator	
<code>CAN_TIME_SEGMENT1_TQ4</code>	Time Segment 1 setting for 4 Time Quanta.
<code>CAN_TIME_SEGMENT1_TQ5</code>	Time Segment 1 setting for 5 Time Quanta.
<code>CAN_TIME_SEGMENT1_TQ6</code>	Time Segment 1 setting for 6 Time Quanta.
<code>CAN_TIME_SEGMENT1_TQ7</code>	Time Segment 1 setting for 7 Time Quanta.
<code>CAN_TIME_SEGMENT1_TQ8</code>	Time Segment 1 setting for 8 Time Quanta.
<code>CAN_TIME_SEGMENT1_TQ9</code>	Time Segment 1 setting for 9 Time Quanta.
<code>CAN_TIME_SEGMENT1_TQ10</code>	Time Segment 1 setting for 10 Time Quanta.
<code>CAN_TIME_SEGMENT1_TQ11</code>	Time Segment 1 setting for 11 Time Quanta.
<code>CAN_TIME_SEGMENT1_TQ12</code>	Time Segment 1 setting for 12 Time Quanta.
<code>CAN_TIME_SEGMENT1_TQ13</code>	Time Segment 1 setting for 13 Time Quanta.
<code>CAN_TIME_SEGMENT1_TQ14</code>	Time Segment 1 setting for 14 Time Quanta.
<code>CAN_TIME_SEGMENT1_TQ15</code>	Time Segment 1 setting for 15 Time Quanta.
<code>CAN_TIME_SEGMENT1_TQ16</code>	Time Segment 1 setting for 16 Time Quanta.

◆ **can\_time\_segment2\_t**

enum <code>can_time_segment2_t</code>	
CAN Time Segment 2 Time Quanta	
Enumerator	
<code>CAN_TIME_SEGMENT2_TQ2</code>	Time Segment 2 setting for 2 Time Quanta.
<code>CAN_TIME_SEGMENT2_TQ3</code>	Time Segment 2 setting for 3 Time Quanta.
<code>CAN_TIME_SEGMENT2_TQ4</code>	Time Segment 2 setting for 4 Time Quanta.
<code>CAN_TIME_SEGMENT2_TQ5</code>	Time Segment 2 setting for 5 Time Quanta.
<code>CAN_TIME_SEGMENT2_TQ6</code>	Time Segment 2 setting for 6 Time Quanta.
<code>CAN_TIME_SEGMENT2_TQ7</code>	Time Segment 2 setting for 7 Time Quanta.
<code>CAN_TIME_SEGMENT2_TQ8</code>	Time Segment 2 setting for 8 Time Quanta.

◆ **can\_sync\_jump\_width\_t**

enum <code>can_sync_jump_width_t</code>	
CAN Synchronization Jump Width Time Quanta	
Enumerator	
<code>CAN_SYNC_JUMP_WIDTH_TQ1</code>	Synchronization Jump Width setting for 1 Time Quanta.
<code>CAN_SYNC_JUMP_WIDTH_TQ2</code>	Synchronization Jump Width setting for 2 Time Quanta.
<code>CAN_SYNC_JUMP_WIDTH_TQ3</code>	Synchronization Jump Width setting for 3 Time Quanta.
<code>CAN_SYNC_JUMP_WIDTH_TQ4</code>	Synchronization Jump Width setting for 4 Time Quanta.

### ◆ can\_mailbox\_send\_receive\_t

enum can_mailbox_send_receive_t	
CAN Mailbox type	
Enumerator	
CAN_MAILBOX_RECEIVE	Mailbox is for receiving.
CAN_MAILBOX_TRANSMIT	Mailbox is for sending.

## 4.3.5 CGC Interface

### Interfaces

#### Detailed Description

Interface for clock generation.

### Summary

The CGC interface provides the ability to configure and use all of the CGC module's capabilities. Among the capabilities is the selection of several clock sources to use as the system clock source. Additionally, the system clocks can be divided down to provide a wide range of frequencies for various system and peripheral needs.

Clock stability can be checked and clocks may also be stopped to save power when not needed. The API has a function to return the frequency of the system and system peripheral clocks at run time. There is also a feature to detect when the main oscillator has stopped, with the option of calling a user provided callback function.

The CGC interface is implemented by:

- [Clock Generation Circuit \(r\\_cgc\)](#)

#### Data Structures

struct [cgc\\_callback\\_args\\_t](#)

struct [cgc\\_pll\\_cfg\\_t](#)

union [cgc\\_divider\\_cfg\\_t](#)

struct [cgc\\_cfg\\_t](#)

struct [cgc\\_clocks\\_cfg\\_t](#)

```
struct cgc\_api\_t
```

```
struct cgc\_instance\_t
```

## Typedefs

```
typedef void cgc\_ctrl\_t
```

## Enumerations

```
enum cgc\_event\_t
```

```
enum cgc\_clock\_t
```

```
enum cgc\_pll\_div\_t
```

```
enum cgc\_pll\_mul\_t
```

```
enum cgc\_sys\_clock\_div\_t
```

```
enum cgc\_usb\_clock\_div\_t
```

```
enum cgc\_clock\_change\_t
```

## Data Structure Documentation

### ◆ [cgc\\_callback\\_args\\_t](#)

struct <a href="#">cgc_callback_args_t</a>		
Callback function parameter data		
Data Fields		
<a href="#">cgc_event_t</a>	event	The event can be used to identify what caused the callback.
void const *	p_context	Placeholder for user data.

### ◆ [cgc\\_pll\\_cfg\\_t](#)

struct <a href="#">cgc_pll_cfg_t</a>		
Clock configuration structure - Used as an input parameter to the <a href="#">cgc_api_t::clockStart</a> function for the PLL clock.		
Data Fields		
<a href="#">cgc_clock_t</a>	source_clock	PLL source clock (main oscillator or HOCO)
<a href="#">cgc_pll_div_t</a>	divider	PLL divider.
<a href="#">cgc_pll_mul_t</a>	multiplier	PLL multiplier.

◆ **cgc\_divider\_cfg\_t**

union cgc_divider_cfg_t		
Clock configuration structure - Used as an input parameter to the <a href="#">cgc_api_t::systemClockSet</a> and <a href="#">cgc_api_t::systemClockGet</a> functions.		
Data Fields		
uint32_t	sckdivcr_w	(@ 0x4001E020) System clock Division control register
struct cgc_divider_cfg_t	__unnamed__	

◆ **cgc\_cfg\_t**

struct cgc_cfg_t
Configuration options.

◆ **cgc\_clocks\_cfg\_t**

struct cgc_clocks_cfg_t		
Clock configuration		
Data Fields		
<a href="#">cgc_clock_t</a>	system_clock	System clock source enumeration.
<a href="#">cgc_pll_cfg_t</a>	pll_cfg	PLL configuration structure.
<a href="#">cgc_pll_cfg_t</a>	pll2_cfg	PLL2 configuration structure.
<a href="#">cgc_divider_cfg_t</a>	divider_cfg	Clock dividers structure.
<a href="#">cgc_clock_change_t</a>	loco_state	State of LOCO.
<a href="#">cgc_clock_change_t</a>	moco_state	State of MOCO.
<a href="#">cgc_clock_change_t</a>	hoco_state	State of HOCO.
<a href="#">cgc_clock_change_t</a>	mainosc_state	State of Main oscillator.
<a href="#">cgc_clock_change_t</a>	pll_state	State of PLL.
<a href="#">cgc_clock_change_t</a>	pll2_state	State of PLL2.

◆ **cgc\_api\_t**

struct cgc_api_t		
CGC functions implemented at the HAL layer follow this API.		
<b>Data Fields</b>		
<a href="#">fsp_err_t</a> (*	<a href="#">open</a> )( <a href="#">cgc_ctrl_t</a> *const p_ctrl, <a href="#">cgc_cfg_t</a> const *const p_cfg)	
<a href="#">fsp_err_t</a> (*	<a href="#">clocksCfg</a> )( <a href="#">cgc_ctrl_t</a> *const p_ctrl, <a href="#">cgc_clocks_cfg_t</a> const *const p_clock_cfg)	

<code>fsp_err_t(*</code>	<code>clockStart )(cgc_ctrl_t *const p_ctrl, cgc_clock_t clock_source, cgc_pll_cfg_t const *const p_pll_cfg)</code>
<code>fsp_err_t(*</code>	<code>clockStop )(cgc_ctrl_t *const p_ctrl, cgc_clock_t clock_source)</code>
<code>fsp_err_t(*</code>	<code>clockCheck )(cgc_ctrl_t *const p_ctrl, cgc_clock_t clock_source)</code>
<code>fsp_err_t(*</code>	<code>systemClockSet )(cgc_ctrl_t *const p_ctrl, cgc_clock_t clock_source, cgc_divider_cfg_t const *const p_divider_cfg)</code>
<code>fsp_err_t(*</code>	<code>systemClockGet )(cgc_ctrl_t *const p_ctrl, cgc_clock_t *const p_clock_source, cgc_divider_cfg_t *const p_divider_cfg)</code>
<code>fsp_err_t(*</code>	<code>oscStopDetectEnable )(cgc_ctrl_t *const p_ctrl)</code>
<code>fsp_err_t(*</code>	<code>oscStopDetectDisable )(cgc_ctrl_t *const p_ctrl)</code>
<code>fsp_err_t(*</code>	<code>oscStopStatusClear )(cgc_ctrl_t *const p_ctrl)</code>
<code>fsp_err_t(*</code>	<code>callbackSet )(cgc_ctrl_t *const p_api_ctrl, void(*p_callback)(cgc_callback_args_t *), void const *const p_context, cgc_callback_args_t *const p_callback_memory)</code>
<code>fsp_err_t(*</code>	<code>close )(cgc_ctrl_t *const p_ctrl)</code>
<code>fsp_err_t(*</code>	<code>versionGet )(fsp_version_t *p_version)</code>

## Field Documentation

◆ **open**

```
fsp_err_t(* cgc_api_t::open) (cgc_ctrl_t *const p_ctrl, cgc_cfg_t const *const p_cfg)
```

Initial configuration

**Implemented as**

- R\_CGC\_Open()

**Parameters**

[in]	p_ctrl	Pointer to instance control block
[in]	p_cfg	Pointer to configuration

◆ **clocksCfg**

```
fsp_err_t(* cgc_api_t::clocksCfg) (cgc_ctrl_t *const p_ctrl, cgc_clocks_cfg_t const *const p_clock_cfg)
```

Configure all system clocks.

**Implemented as**

- R\_CGC\_ClocksCfg()

**Parameters**

[in]	p_ctrl	Pointer to instance control block
[in]	p_clock_cfg	Pointer to desired configuration of system clocks

◆ **clockStart**

```
fsp_err_t(* cgc_api_t::clockStart) (cgc_ctrl_t *const p_ctrl, cgc_clock_t clock_source, cgc_pll_cfg_t const *const p_pll_cfg)
```

Start a clock.

**Implemented as**

- R\_CGC\_ClockStart()

**Parameters**

[in]	p_ctrl	Pointer to instance control block
[in]	clock_source	Clock source to start
[in]	p_pll_cfg	Pointer to PLL configuration, can be NULL if clock_source is not CGC_CLOCK_PLL or CGC_CLOCK_PLL2



◆ **clockStop**

```
fsp_err_t(* cgc_api_t::clockStop) (cgc_ctrl_t *const p_ctrl, cgc_clock_t clock_source)
```

Stop a clock.

**Implemented as**

- R\_CGC\_ClockStop()

**Parameters**

[in]	p_ctrl	Pointer to instance control block
[in]	clock_source	The clock source to stop

◆ **clockCheck**

```
fsp_err_t(* cgc_api_t::clockCheck) (cgc_ctrl_t *const p_ctrl, cgc_clock_t clock_source)
```

Check the stability of the selected clock.

**Implemented as**

- R\_CGC\_ClockCheck()

**Parameters**

[in]	p_ctrl	Pointer to instance control block
[in]	clock_source	Which clock source to check for stability

◆ **systemClockSet**

```
fsp_err_t(* cgc_api_t::systemClockSet) (cgc_ctrl_t *const p_ctrl, cgc_clock_t clock_source, cgc_divider_cfg_t const *const p_divider_cfg)
```

Set the system clock.

**Implemented as**

- R\_CGC\_SystemClockSet()

**Parameters**

[in]	p_ctrl	Pointer to instance control block
[in]	clock_source	Clock source to set as system clock
[in]	p_divider_cfg	Pointer to the clock divider configuration

◆ **systemClockGet**

```
fsp_err_t(* cgc_api_t::systemClockGet) (cgc_ctrl_t *const p_ctrl, cgc_clock_t *const p_clock_source,
cgc_divider_cfg_t *const p_divider_cfg)
```

Get the system clock information.

**Implemented as**

- R\_CGC\_SystemClockGet()

**Parameters**

[in]	p_ctrl	Pointer to instance control block
[out]	p_clock_source	Returns the current system clock
[out]	p_divider_cfg	Returns the current system clock dividers

◆ **oscStopDetectEnable**

```
fsp_err_t(* cgc_api_t::oscStopDetectEnable) (cgc_ctrl_t *const p_ctrl)
```

Enable and optionally register a callback for Main Oscillator stop detection.

**Implemented as**

- R\_CGC\_OscStopDetectEnable()

**Parameters**

[in]	p_ctrl	Pointer to instance control block
[in]	p_callback	Callback function that will be called by the NMI interrupt when an oscillation stop is detected. If the second argument is "false", then this argument can be NULL.
[in]	enable	Enable/disable Oscillation Stop Detection

◆ **oscStopDetectDisable**

```
fsp_err_t(* cgc_api_t::oscStopDetectDisable) (cgc_ctrl_t *const p_ctrl)
```

Disable Main Oscillator stop detection.

**Implemented as**

- [R\\_CGC\\_OscStopDetectDisable\(\)](#)

**Parameters**

[in]	p_ctrl	Pointer to instance control block
------	--------	-----------------------------------

◆ **oscStopStatusClear**

```
fsp_err_t(* cgc_api_t::oscStopStatusClear) (cgc_ctrl_t *const p_ctrl)
```

Clear the oscillator stop detection flag.

**Implemented as**

- [R\\_CGC\\_OscStopStatusClear\(\)](#)

**Parameters**

[in]	p_ctrl	Pointer to instance control block
------	--------	-----------------------------------

◆ **callbackSet**

```
fsp_err_t(* cgc_api_t::callbackSet) (cgc_ctrl_t *const p_api_ctrl, void(*p_callback)(cgc_callback_args_t *), void const *const p_context, cgc_callback_args_t *const p_callback_memory)
```

Specify callback function and optional context pointer and working memory pointer.

**Implemented as**

- [R\\_CGC\\_CallbackSet\(\)](#)

**Parameters**

[in]	p_ctrl	Pointer to the CGC control block.
[in]	p_callback	Callback function
[in]	p_context	Pointer to send to callback function
[in]	p_working_memory	Pointer to volatile memory where callback structure can be allocated. Callback arguments allocated here are only valid during the callback.

◆ **close**

```
fsp_err_t(* cgc_api_t::close) (cgc_ctrl_t *const p_ctrl)
```

Close the CGC driver.

**Implemented as**

- R\_CGC\_Close()

**Parameters**

[in]	p_ctrl	Pointer to instance control block
------	--------	-----------------------------------

◆ **versionGet**

```
fsp_err_t(* cgc_api_t::versionGet) (fsp_version_t *p_version)
```

Gets the CGC driver version.

**Implemented as**

- R\_CGC\_VersionGet()

**Parameters**

[out]	p_version	Code and API version used
-------	-----------	---------------------------

◆ **cgc\_instance\_t**

```
struct cgc_instance_t
```

This structure encompasses everything that is needed to use an instance of this interface.

## Data Fields

cgc_ctrl_t *	p_ctrl	Pointer to the control structure for this instance.
cgc_cfg_t const *	p_cfg	Pointer to the configuration structure for this instance.
cgc_api_t const *	p_api	Pointer to the API structure for this instance.

**Typedef Documentation**◆ **cgc\_ctrl\_t**

```
typedef void cgc_ctrl_t
```

CGC control block. Allocate an instance specific control block to pass into the CGC API calls.

**Implemented as**

- cgc\_instance\_ctrl\_t

## Enumeration Type Documentation

### ◆ `cgc_event_t`

enum <code>cgc_event_t</code>	
Events that can trigger a callback function	
Enumerator	
<code>CGC_EVENT_OSC_STOP_DETECT</code>	Oscillator stop detection has caused the event.

### ◆ `cgc_clock_t`

enum <code>cgc_clock_t</code>	
System clock source identifiers - The source of ICLK, BCLK, FCLK, PCLKS A-D and UCLK prior to the system clock divider	
Enumerator	
<code>CGC_CLOCK_HOCO</code>	The high speed on chip oscillator.
<code>CGC_CLOCK_MOCO</code>	The middle speed on chip oscillator.
<code>CGC_CLOCK_LOCO</code>	The low speed on chip oscillator.
<code>CGC_CLOCK_MAIN_OSC</code>	The main oscillator.
<code>CGC_CLOCK_SUBCLOCK</code>	The subclock oscillator.
<code>CGC_CLOCK_PLL</code>	The PLL oscillator.
<code>CGC_CLOCK_PLL2</code>	The PLL2 oscillator.

◆ **cgc\_pll\_div\_t**

enum <a href="#">cgc_pll_div_t</a>	
PLL divider values	
Enumerator	
CGC_PLL_DIV_1	PLL divider of 1.
CGC_PLL_DIV_2	PLL divider of 2.
CGC_PLL_DIV_3	PLL divider of 3 (S7, S5 only)
CGC_PLL_DIV_4	PLL divider of 4 (S3 only)

◆ **cgc\_pll\_mul\_t**

enum <code>cgc_pll_mul_t</code>	
PLL multiplier values	
Enumerator	
<code>CGC_PLL_MUL_8_0</code>	PLL multiplier of 8.0.
<code>CGC_PLL_MUL_9_0</code>	PLL multiplier of 9.0.
<code>CGC_PLL_MUL_10_0</code>	PLL multiplier of 10.0.
<code>CGC_PLL_MUL_10_5</code>	PLL multiplier of 10.5.
<code>CGC_PLL_MUL_11_0</code>	PLL multiplier of 11.0.
<code>CGC_PLL_MUL_11_5</code>	PLL multiplier of 11.5.
<code>CGC_PLL_MUL_12_0</code>	PLL multiplier of 12.0.
<code>CGC_PLL_MUL_12_5</code>	PLL multiplier of 12.5.
<code>CGC_PLL_MUL_13_0</code>	PLL multiplier of 13.0.
<code>CGC_PLL_MUL_13_5</code>	PLL multiplier of 13.5.
<code>CGC_PLL_MUL_14_0</code>	PLL multiplier of 14.0.
<code>CGC_PLL_MUL_14_5</code>	PLL multiplier of 14.5.
<code>CGC_PLL_MUL_15_0</code>	PLL multiplier of 15.0.
<code>CGC_PLL_MUL_15_5</code>	PLL multiplier of 15.5.
<code>CGC_PLL_MUL_16_0</code>	PLL multiplier of 16.0.
<code>CGC_PLL_MUL_16_5</code>	PLL multiplier of 16.5.
<code>CGC_PLL_MUL_17_0</code>	PLL multiplier of 17.0.
<code>CGC_PLL_MUL_17_5</code>	PLL multiplier of 17.5.
<code>CGC_PLL_MUL_18_0</code>	PLL multiplier of 18.0.
<code>CGC_PLL_MUL_18_5</code>	PLL multiplier of 18.5.
<code>CGC_PLL_MUL_19_0</code>	PLL multiplier of 19.0.

CGC_PLL_MUL_19_5	PLL multiplier of 19.5.
CGC_PLL_MUL_20_0	PLL multiplier of 20.0.
CGC_PLL_MUL_20_5	PLL multiplier of 20.5.
CGC_PLL_MUL_21_0	PLL multiplier of 21.0.
CGC_PLL_MUL_21_5	PLL multiplier of 21.5.
CGC_PLL_MUL_22_0	PLL multiplier of 22.0.
CGC_PLL_MUL_22_5	PLL multiplier of 22.5.
CGC_PLL_MUL_23_0	PLL multiplier of 23.0.
CGC_PLL_MUL_23_5	PLL multiplier of 23.5.
CGC_PLL_MUL_24_0	PLL multiplier of 24.0.
CGC_PLL_MUL_24_5	PLL multiplier of 24.5.
CGC_PLL_MUL_25_0	PLL multiplier of 25.0.
CGC_PLL_MUL_25_5	PLL multiplier of 25.5.
CGC_PLL_MUL_26_0	PLL multiplier of 26.0.
CGC_PLL_MUL_26_5	PLL multiplier of 26.5.
CGC_PLL_MUL_27_0	PLL multiplier of 27.0.
CGC_PLL_MUL_27_5	PLL multiplier of 27.5.
CGC_PLL_MUL_28_0	PLL multiplier of 28.0.
CGC_PLL_MUL_28_5	PLL multiplier of 28.5.
CGC_PLL_MUL_29_0	PLL multiplier of 29.0.
CGC_PLL_MUL_29_5	PLL multiplier of 29.5.
CGC_PLL_MUL_30_0	PLL multiplier of 30.0.
CGC_PLL_MUL_31_0	PLL multiplier of 31.0.



◆ **cgc\_sys\_clock\_div\_t**

enum <code>cgc_sys_clock_div_t</code>	
System clock divider values - The individually selectable divider of each of the system clocks, ICLK, BCLK, FCLK, PCLKS A-D.	
Enumerator	
<code>CGC_SYS_CLOCK_DIV_1</code>	System clock divided by 1.
<code>CGC_SYS_CLOCK_DIV_2</code>	System clock divided by 2.
<code>CGC_SYS_CLOCK_DIV_4</code>	System clock divided by 4.
<code>CGC_SYS_CLOCK_DIV_8</code>	System clock divided by 8.
<code>CGC_SYS_CLOCK_DIV_16</code>	System clock divided by 16.
<code>CGC_SYS_CLOCK_DIV_32</code>	System clock divided by 32.
<code>CGC_SYS_CLOCK_DIV_64</code>	System clock divided by 64.

◆ **cgc\_usb\_clock\_div\_t**

enum <code>cgc_usb_clock_div_t</code>	
USB clock divider values	
Enumerator	
<code>CGC_USB_CLOCK_DIV_3</code>	Divide USB source clock by 3.
<code>CGC_USB_CLOCK_DIV_4</code>	Divide USB source clock by 4.
<code>CGC_USB_CLOCK_DIV_5</code>	Divide USB source clock by 5.

◆ **cgc\_clock\_change\_t**

enum <code>cgc_clock_change_t</code>	
Clock options	
Enumerator	
<code>CGC_CLOCK_CHANGE_START</code>	Start the clock.
<code>CGC_CLOCK_CHANGE_STOP</code>	Stop the clock.
<code>CGC_CLOCK_CHANGE_NONE</code>	No change to the clock.

## 4.3.6 Comparator Interface

### Interfaces

#### Detailed Description

Interface for comparators.

## Summary

The comparator interface provides standard comparator functionality, including generating an event when the comparator result changes.

Implemented by:

- [High-Speed Analog Comparator \(r\\_acmphs\)](#)
- [Low-Power Analog Comparator \(r\\_acmplp\)](#)

#### Data Structures

struct `comparator_info_t`

struct `comparator_status_t`

struct `comparator_callback_args_t`

struct `comparator_cfg_t`

struct `comparator_api_t`

struct `comparator_instance_t`

#### Macros

```
#define COMPARATOR_API_VERSION_MAJOR
```

## Typedefs

```
typedef void comparator_ctrl_t
```

## Enumerations

```
enum comparator_mode_t
```

```
enum comparator_trigger_t
```

```
enum comparator_polarity_invert_t
```

```
enum comparator_pin_output_t
```

```
enum comparator_filter_t
```

```
enum comparator_state_t
```

## Data Structure Documentation

### ◆ comparator\_info\_t

struct comparator_info_t		
Comparator information.		
Data Fields		
uint32_t	min_stabilization_wait_us	Minimum stabilization wait time in microseconds.

### ◆ comparator\_status\_t

struct comparator_status_t		
Comparator status.		
Data Fields		
comparator_state_t	state	Current comparator state.

### ◆ comparator\_callback\_args\_t

struct comparator_callback_args_t		
Callback function parameter data		
Data Fields		
void const *	p_context	Placeholder for user data. Set in <a href="#">comparator_api_t::open</a> function in <a href="#">comparator_cfg_t</a> .
uint32_t	channel	The physical hardware channel that caused the interrupt.

◆ **comparator\_cfg\_t**

struct comparator_cfg_t	
User configuration structure, used in open function	
<b>Data Fields</b>	
uint8_t	channel
	Hardware channel used.
comparator_mode_t	mode
	Normal or window mode.
comparator_trigger_t	trigger
	Trigger setting.
comparator_filter_t	filter
	Digital filter clock divisor setting.
comparator_polarity_invert_t	invert
	Whether to invert output.
comparator_pin_output_t	pin_output
	Whether to include output on output pin.
uint8_t	vref_select
	Internal Vref Select.
uint8_t	ipl
	Interrupt priority.

IRQn_Type	irq
	NVIC interrupt number.
void(*	p_callback )(comparator_callback_args_t *p_args)
void const *	p_context
void const *	p_extend
	Comparator hardware dependent configuration.

## Field Documentation

### ◆ p\_callback

void(\* comparator\_cfg\_t::p\_callback) (comparator\_callback\_args\_t \*p\_args)

Callback called when comparator event occurs.

### ◆ p\_context

void const\* comparator\_cfg\_t::p\_context

Placeholder for user data. Passed to the user callback in `comparator_callback_args_t`.

### ◆ comparator\_api\_t

struct comparator\_api\_t

Comparator functions implemented at the HAL layer will follow this API.

#### Data Fields

fsp_err_t(*	open )(comparator_ctrl_t *const p_ctrl, comparator_cfg_t const *const p_cfg)
fsp_err_t(*	outputEnable )(comparator_ctrl_t *const p_ctrl)
fsp_err_t(*	infoGet )(comparator_ctrl_t *const p_ctrl, comparator_info_t *const p_info)
fsp_err_t(*	statusGet )(comparator_ctrl_t *const p_ctrl, comparator_status_t *const p_status)

<code>fsp_err_t(*</code>	<code>close )(comparator_ctrl_t *const p_ctrl)</code>
--------------------------	-------------------------------------------------------

<code>fsp_err_t(*</code>	<code>versionGet )(fsp_version_t *const p_version)</code>
--------------------------	-----------------------------------------------------------

## Field Documentation

### ◆ open

`fsp_err_t(* comparator_api_t::open) (comparator_ctrl_t *const p_ctrl, comparator_cfg_t const *const p_cfg)`

Initialize the comparator.

#### Implemented as

- `R_ACMPHS_Open()`
- `R_ACMPPLP_Open()`

#### Parameters

[in]	p_ctrl	Pointer to instance control block
[in]	p_cfg	Pointer to configuration

### ◆ outputEnable

`fsp_err_t(* comparator_api_t::outputEnable) (comparator_ctrl_t *const p_ctrl)`

Start the comparator.

#### Implemented as

- `R_ACMPHS_OutputEnable()`
- `R_ACMPPLP_OutputEnable()`

#### Parameters

[in]	p_ctrl	Pointer to instance control block
------	--------	-----------------------------------

## ◆ infoGet

```
fsp_err_t(* comparator_api_t::infoGet) (comparator_ctrl_t *const p_ctrl, comparator_info_t *const p_info)
```

Provide information such as the recommended minimum stabilization wait time.

**Implemented as**

- R\_ACMPHS\_InfoGet()
- R\_ACMPPLP\_InfoGet()

**Parameters**

[in]	p_ctrl	Pointer to instance control block
[out]	p_info	Comparator information stored here

## ◆ statusGet

```
fsp_err_t(* comparator_api_t::statusGet) (comparator_ctrl_t *const p_ctrl, comparator_status_t *const p_status)
```

Provide current comparator status.

**Implemented as**

- R\_ACMPHS\_StatusGet()
- R\_ACMPPLP\_StatusGet()

**Parameters**

[in]	p_ctrl	Pointer to instance control block
[out]	p_status	Status stored here

## ◆ close

```
fsp_err_t(* comparator_api_t::close) (comparator_ctrl_t *const p_ctrl)
```

Stop the comparator.

**Implemented as**

- R\_ACMPHS\_Close()
- R\_ACMPPLP\_Close()

**Parameters**

[in]	p_ctrl	Pointer to instance control block
------	--------	-----------------------------------

◆ **versionGet**

```
fsp_err_t(* comparator_api_t::versionGet) (fsp_version_t *const p_version)
```

Retrieve the API version.

**Implemented as**

- R\_ACMPHS\_VersionGet()
- R\_ACMLP\_VersionGet()

**Precondition**

This function retrieves the API version.

**Parameters**

[in]	p_version	Pointer to version structure
------	-----------	------------------------------

◆ **comparator\_instance\_t**

```
struct comparator_instance_t
```

This structure encompasses everything that is needed to use an instance of this interface.

## Data Fields

comparator_ctrl_t *	p_ctrl	Pointer to the control structure for this instance.
comparator_cfg_t const *	p_cfg	Pointer to the configuration structure for this instance.
comparator_api_t const *	p_api	Pointer to the API structure for this instance.

**Macro Definition Documentation**◆ **COMPARATOR\_API\_VERSION\_MAJOR**

```
#define COMPARATOR_API_VERSION_MAJOR
```

Includes board and MCU related header files. Version Number of API.

**Typedef Documentation**◆ **comparator\_ctrl\_t**

```
typedef void comparator_ctrl_t
```

Comparator control block. Allocate an instance specific control block to pass into the comparator API calls.

**Implemented as**

- acmphs\_instance\_ctrl\_t
- acmplp\_instance\_ctrl\_t



## Enumeration Type Documentation

### ◆ comparator\_mode\_t

enum <code>comparator_mode_t</code>	
Select whether to invert the polarity of the comparator output.	
Enumerator	
COMPARATOR_MODE_NORMAL	Normal mode.
COMPARATOR_MODE_WINDOW	Window mode, not supported by all implementations.

### ◆ comparator\_trigger\_t

enum <code>comparator_trigger_t</code>	
Trigger type: rising edge, falling edge, both edges, low level.	
Enumerator	
COMPARATOR_TRIGGER_RISING	Rising edge trigger.
COMPARATOR_TRIGGER_FALLING	Falling edge trigger.
COMPARATOR_TRIGGER_BOTH_EDGE	Both edges trigger.

### ◆ comparator\_polarity\_invert\_t

enum <code>comparator_polarity_invert_t</code>	
Select whether to invert the polarity of the comparator output.	
Enumerator	
COMPARATOR_POLARITY_INVERT_OFF	Do not invert polarity.
COMPARATOR_POLARITY_INVERT_ON	Invert polarity.

◆ **comparator\_pin\_output\_t**

enum <a href="#">comparator_pin_output_t</a>	
Select whether to include the comparator output on the output pin.	
Enumerator	
COMPARATOR_PIN_OUTPUT_OFF	Do not include comparator output on output pin.
COMPARATOR_PIN_OUTPUT_ON	Include comparator output on output pin.

◆ **comparator\_filter\_t**

enum <a href="#">comparator_filter_t</a>	
Comparator digital filtering sample clock divisor settings.	
Enumerator	
COMPARATOR_FILTER_OFF	Disable debounce filter.
COMPARATOR_FILTER_1	Filter using PCLK divided by 1, not supported by all implementations.
COMPARATOR_FILTER_8	Filter using PCLK divided by 8.
COMPARATOR_FILTER_16	Filter using PCLK divided by 16, not supported by all implementations.
COMPARATOR_FILTER_32	Filter using PCLK divided by 32.

◆ **comparator\_state\_t**

enum <a href="#">comparator_state_t</a>	
Current comparator state.	
Enumerator	
COMPARATOR_STATE_OUTPUT_LOW	$VCMP < VREF$ if polarity is not inverted, $VCMP > VREF$ if inverted.
COMPARATOR_STATE_OUTPUT_HIGH	$VCMP > VREF$ if polarity is not inverted, $VCMP < VREF$ if inverted.
COMPARATOR_STATE_OUTPUT_DISABLED	<a href="#">comparator_api_t::outputEnable()</a> has not been called

## 4.3.7 CRC Interface

### Interfaces

#### Detailed Description

Interface for cyclic redundancy checking.

## Summary

The CRC (Cyclic Redundancy Check) calculator generates CRC codes using five different polynomials including 8 bit, 16 bit, and 32 bit variations. Calculation can be performed by sending data to the block using the CPU or by snooping on read or write activity on one of 10 SCI channels.

Implemented by:

- Cyclic Redundancy Check (CRC) Calculator (`r_crc`)

#### Data Structures

struct `crc_input_t`

struct `crc_cfg_t`

struct `crc_api_t`

struct `crc_instance_t`

#### Typedefs

typedef void `crc_ctrl_t`

#### Enumerations

enum `crc_polynomial_t`

enum `crc_bit_order_t`

enum `crc_snoop_direction_t`

enum `crc_snoop_address_t`

#### Data Structure Documentation

##### ◆ `crc_input_t`

struct `crc_input_t`

Structure for CRC inputs

◆ **crc\_cfg\_t**

struct <code>crc_cfg_t</code>		
User configuration structure, used in <code>open</code> function		
Data Fields		
<code>crc_polynomial_t</code>	<code>polynomial</code>	CRC Generating Polynomial Switching (GPS)
<code>crc_bit_order_t</code>	<code>bit_order</code>	CRC Calculation Switching (LMS)
<code>crc_snoop_address_t</code>	<code>snoop_address</code>	Register Snoop Address (CRCSA)
<code>void const *</code>	<code>p_extend</code>	CRC Hardware Dependent Configuration.

◆ **crc\_api\_t**

struct <code>crc_api_t</code>	
CRC driver structure. General CRC functions implemented at the HAL layer will follow this API.	
<b>Data Fields</b>	
<code>fsp_err_t(*)</code>	<code>open</code> <code>((crc_ctrl_t *const p_ctrl, crc_cfg_t const *const p_cfg)</code>
<code>fsp_err_t(*)</code>	<code>close</code> <code>((crc_ctrl_t *const p_ctrl)</code>
<code>fsp_err_t(*)</code>	<code>crcResultGet</code> <code>((crc_ctrl_t *const p_ctrl, uint32_t *crc_result)</code>
<code>fsp_err_t(*)</code>	<code>snoopEnable</code> <code>((crc_ctrl_t *const p_ctrl, uint32_t crc_seed)</code>
<code>fsp_err_t(*)</code>	<code>snoopDisable</code> <code>((crc_ctrl_t *const p_ctrl)</code>
<code>fsp_err_t(*)</code>	<code>calculate</code> <code>((crc_ctrl_t *const p_ctrl, crc_input_t *const p_crc_input, uint32_t *p_crc_result)</code>
<code>fsp_err_t(*)</code>	<code>versionGet</code> <code>((fsp_version_t *version)</code>
<b>Field Documentation</b>	

## ◆ open

```
fsp_err_t(* crc_api_t::open) (crc_ctrl_t *const p_ctrl, crc_cfg_t const *const p_cfg)
```

Open the CRC driver module.

**Implemented as**

- R\_CRC\_Open()

**Parameters**

[in]	p_ctrl	Pointer to CRC device handle.
[in]	p_cfg	Pointer to a configuration structure.

## ◆ close

```
fsp_err_t(* crc_api_t::close) (crc_ctrl_t *const p_ctrl)
```

Close the CRC module driver

**Implemented as**

- R\_CRC\_Close()

**Parameters**

[in]	p_ctrl	Pointer to crc device handle
------	--------	------------------------------

**Return values**

FSP_SUCCESS	Configuration was successful.
-------------	-------------------------------

## ◆ crcResultGet

```
fsp_err_t(* crc_api_t::crcResultGet) (crc_ctrl_t *const p_ctrl, uint32_t *crc_result)
```

Return the current calculated value.

**Implemented as**

- R\_CRC\_CalculatedValueGet()

**Parameters**

[in]	p_ctrl	Pointer to CRC device handle.
[out]	crc_result	The calculated value from the last CRC calculation.

◆ **snoopEnable**

```
fsp_err_t(* crc_api_t::snoopEnable) (crc_ctrl_t *const p_ctrl, uint32_t crc_seed)
```

Configure and Enable snooping.

**Implemented as**

- R\_CRC\_SnoopEnable()

**Parameters**

[in]	p_ctrl	Pointer to CRC device handle.
[in]	crc_seed	CRC seed.

◆ **snoopDisable**

```
fsp_err_t(* crc_api_t::snoopDisable) (crc_ctrl_t *const p_ctrl)
```

Disable snooping.

**Implemented as**

- R\_CRC\_SnoopDisable()

**Parameters**

[in]	p_ctrl	Pointer to CRC device handle.
------	--------	-------------------------------

◆ **calculate**

```
fsp_err_t(* crc_api_t::calculate) (crc_ctrl_t *const p_ctrl, crc_input_t *const p_crc_input, uint32_t *p_crc_result)
```

Perform a CRC calculation on a block of data.

**Implemented as**

- R\_CRC\_Calculate()

**Parameters**

[in]	p_ctrl	Pointer to crc device handle.
[in]	p_crc_input	A pointer to structure for CRC inputs
[out]	crc_result	The calculated value of the CRC calculation.

◆ **versionGet**

```
fsp_err_t(* crc_api_t::versionGet) (fsp_version_t *version)
```

Get the driver version based on compile time macros.

**Implemented as**

- [R\\_CRC\\_VersionGet\(\)](#)

◆ **crc\_instance\_t**

```
struct crc_instance_t
```

This structure encompasses everything that is needed to use an instance of this interface.

## Data Fields

<a href="#">crc_ctrl_t</a> *	p_ctrl	Pointer to the control structure for this instance.
<a href="#">crc_cfg_t</a> const *	p_cfg	Pointer to the configuration structure for this instance.
<a href="#">crc_api_t</a> const *	p_api	Pointer to the API structure for this instance.

**Typedef Documentation**◆ **crc\_ctrl\_t**

```
typedef void crc\_ctrl\_t
```

CRC control block. Allocate an instance specific control block to pass into the CRC API calls.

**Implemented as**

- [crc\\_instance\\_ctrl\\_t](#)

**Enumeration Type Documentation**

◆ **crc\_polynomial\_t**

enum <code>crc_polynomial_t</code>	
CRC Generating Polynomial Switching (GPS).	
Enumerator	
<code>CRC_POLYNOMIAL_CRC_8</code>	8-bit CRC-8 ( $X^8 + X^2 + X + 1$ )
<code>CRC_POLYNOMIAL_CRC_16</code>	16-bit CRC-16 ( $X^{16} + X^{15} + X^2 + 1$ )
<code>CRC_POLYNOMIAL_CRC_CCITT</code>	16-bit CRC-CCITT ( $X^{16} + X^{12} + X^5 + 1$ )
<code>CRC_POLYNOMIAL_CRC_32</code>	32-bit CRC-32 ( $X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$ )
<code>CRC_POLYNOMIAL_CRC_32C</code>	32-bit CRC-32C ( $X^{32} + X^{28} + X^{27} + X^{26} + X^{25} + X^{23} + X^{22} + X^{20} + X^{19} + X^{18} + X^{14} + X^{13} + X^{11} + X^{10} + X^9 + X^8 + X^6 + 1$ )

◆ **crc\_bit\_order\_t**

enum <code>crc_bit_order_t</code>	
CRC Calculation Switching (LMS)	
Enumerator	
<code>CRC_BIT_ORDER_LMS_LSB</code>	Generates CRC for LSB first communication.
<code>CRC_BIT_ORDER_LMS_MSB</code>	Generates CRC for MSB first communication.

◆ **crc\_snoop\_direction\_t**

enum <code>crc_snoop_direction_t</code>	
Snoop-On-Write/Read Switch (CRCSWR)	
Enumerator	
<code>CRC_SNOOP_DIRECTION_RECEIVE</code>	Snoop-on-read.
<code>CRC_SNOOP_DIRECTION_TRANSMIT</code>	Snoop-on-write.



◆ **enum crc\_snoop\_address\_t**

enum <code>enum crc_snoop_address_t</code>	
Snoop SCI register Address (lower 14 bits)	
Enumerator	
<code>CRC_SNOOP_ADDRESS_NONE</code>	Snoop mode disabled.
<code>CRC_SNOOP_ADDRESS_SCI0_TDR</code>	Snoop SCI0 transmit data register.
<code>CRC_SNOOP_ADDRESS_SCI1_TDR</code>	Snoop SCI1 transmit data register.
<code>CRC_SNOOP_ADDRESS_SCI2_TDR</code>	Snoop SCI2 transmit data register.
<code>CRC_SNOOP_ADDRESS_SCI3_TDR</code>	Snoop SCI3 transmit data register.
<code>CRC_SNOOP_ADDRESS_SCI4_TDR</code>	Snoop SCI4 transmit data register.
<code>CRC_SNOOP_ADDRESS_SCI5_TDR</code>	Snoop SCI5 transmit data register.
<code>CRC_SNOOP_ADDRESS_SCI6_TDR</code>	Snoop SCI6 transmit data register.
<code>CRC_SNOOP_ADDRESS_SCI7_TDR</code>	Snoop SCI7 transmit data register.
<code>CRC_SNOOP_ADDRESS_SCI8_TDR</code>	Snoop SCI8 transmit data register.
<code>CRC_SNOOP_ADDRESS_SCI9_TDR</code>	Snoop SCI9 transmit data register.
<code>CRC_SNOOP_ADDRESS_SCI0_FTDRL</code>	Snoop SCI0 transmit FIFO data register.
<code>CRC_SNOOP_ADDRESS_SCI1_FTDRL</code>	Snoop SCI1 transmit FIFO data register.
<code>CRC_SNOOP_ADDRESS_SCI2_FTDRL</code>	Snoop SCI2 transmit FIFO data register.
<code>CRC_SNOOP_ADDRESS_SCI3_FTDRL</code>	Snoop SCI3 transmit FIFO data register.
<code>CRC_SNOOP_ADDRESS_SCI4_FTDRL</code>	Snoop SCI4 transmit FIFO data register.
<code>CRC_SNOOP_ADDRESS_SCI5_FTDRL</code>	Snoop SCI5 transmit FIFO data register.
<code>CRC_SNOOP_ADDRESS_SCI6_FTDRL</code>	Snoop SCI6 transmit FIFO data register.
<code>CRC_SNOOP_ADDRESS_SCI7_FTDRL</code>	Snoop SCI7 transmit FIFO data register.
<code>CRC_SNOOP_ADDRESS_SCI8_FTDRL</code>	Snoop SCI8 transmit FIFO data register.
<code>CRC_SNOOP_ADDRESS_SCI9_FTDRL</code>	Snoop SCI9 transmit FIFO data register.

CRC_SNOOP_ADDRESS_SCI0_RDR	Snoop SCI0 receive data register.
CRC_SNOOP_ADDRESS_SCI1_RDR	Snoop SCI1 receive data register.
CRC_SNOOP_ADDRESS_SCI2_RDR	Snoop SCI2 receive data register.
CRC_SNOOP_ADDRESS_SCI3_RDR	Snoop SCI3 receive data register.
CRC_SNOOP_ADDRESS_SCI4_RDR	Snoop SCI4 receive data register.
CRC_SNOOP_ADDRESS_SCI5_RDR	Snoop SCI5 receive data register.
CRC_SNOOP_ADDRESS_SCI6_RDR	Snoop SCI6 receive data register.
CRC_SNOOP_ADDRESS_SCI7_RDR	Snoop SCI7 receive data register.
CRC_SNOOP_ADDRESS_SCI8_RDR	Snoop SCI8 receive data register.
CRC_SNOOP_ADDRESS_SCI9_RDR	Snoop SCI9 receive data register.
CRC_SNOOP_ADDRESS_SCI0_FRDRL	Snoop SCI0 receive FIFO data register.
CRC_SNOOP_ADDRESS_SCI1_FRDRL	Snoop SCI1 receive FIFO data register.
CRC_SNOOP_ADDRESS_SCI2_FRDRL	Snoop SCI2 receive FIFO data register.
CRC_SNOOP_ADDRESS_SCI3_FRDRL	Snoop SCI3 receive FIFO data register.
CRC_SNOOP_ADDRESS_SCI4_FRDRL	Snoop SCI4 receive FIFO data register.
CRC_SNOOP_ADDRESS_SCI5_FRDRL	Snoop SCI5 receive FIFO data register.
CRC_SNOOP_ADDRESS_SCI6_FRDRL	Snoop SCI6 receive FIFO data register.
CRC_SNOOP_ADDRESS_SCI7_FRDRL	Snoop SCI7 receive FIFO data register.
CRC_SNOOP_ADDRESS_SCI8_FRDRL	Snoop SCI8 receive FIFO data register.
CRC_SNOOP_ADDRESS_SCI9_FRDRL	Snoop SCI9 receive FIFO data register.

### 4.3.8 CTSU Interface

#### [Interfaces](#)

## Detailed Description

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Interface for Capacitive Touch Sensing Unit (CTSU) functions.

## Summary

The CTSU interface provides CTSU functionality.

The CTSU interface can be implemented by:

- [Capacitive Touch Sensing Unit \(r\\_ctsu\)](#)

## Data Structures

---

struct [ctsu\\_callback\\_args\\_t](#)

struct [ctsu\\_element\\_cfg\\_t](#)

struct [ctsu\\_cfg\\_t](#)

struct [ctsu\\_api\\_t](#)

struct [ctsu\\_instance\\_t](#)

## Typedefs

---

typedef void [ctsu\\_ctrl\\_t](#)

## Enumerations

---

enum [ctsu\\_event\\_t](#)

enum [ctsu\\_cap\\_t](#)

enum [ctsu\\_txvsel\\_t](#)

enum [ctsu\\_txvsel2\\_t](#)

enum [ctsu\\_atune1\\_t](#)

enum [ctsu\\_atune12\\_t](#)

enum [ctsu\\_md\\_t](#)

enum [ctsu\\_posel\\_t](#)

enum [ctsu\\_ssdiv\\_t](#)

---

## Data Structure Documentation

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### ◆ [ctsu\\_callback\\_args\\_t](#)

struct ctsu_callback_args_t		
Callback function parameter data		
Data Fields		
<a href="#">ctsu_event_t</a>	event	The event can be used to identify what caused the callback.
void const *	p_context	Placeholder for user data. Set in <a href="#">ctsu_api_t::open</a> function in <a href="#">ctsu_cfg_t</a> .

◆ **ctsu\_element\_cfg\_t**

struct ctsu_element_cfg_t		
CTSU Configuration parameters. Element Configuration		
Data Fields		
<a href="#">ctsu_sdiv_t</a>	ssdiv	CTSU Spectrum Diffusion Frequency Division Setting (CTSU Only)
uint16_t	so	CTSU Sensor Offset Adjustment.
uint8_t	snum	CTSU Measurement Count Setting.
uint8_t	sdpa	CTSU Base Clock Setting.

◆ **ctsu\_cfg\_t**

struct ctsu_cfg_t	
User configuration structure, used in open function	
Data Fields	
<a href="#">ctsu_cap_t</a>	cap
	CTSU Scan Start Trigger Select.
<a href="#">ctsu_txvsel_t</a>	txvsel
	CTSU Transmission Power Supply Select.
<a href="#">ctsu_txvsel2_t</a>	txvsel2
	CTSU Transmission Power Supply Select 2 (CTSU2 Only)
<a href="#">ctsu_atune1_t</a>	atune1

	CTSU Power Supply Capacity Adjustment (CTSU Only)
<code>ctsu_atune12_t</code>	<code>atune12</code>
	CTSU Power Supply Capacity Adjustment (CTSU2 Only)
<code>ctsu_md_t</code>	<code>md</code>
	CTSU Measurement Mode Select.
<code>ctsu_posel_t</code>	<code>posel</code>
	CTSU Non-Measured Channel Output Select (CTSU2 Only)
<code>uint8_t</code>	<code>ctsuchac0</code>
	TS00-TS07 enable mask.
<code>uint8_t</code>	<code>ctsuchac1</code>
	TS08-TS15 enable mask.
<code>uint8_t</code>	<code>ctsuchac2</code>
	TS16-TS23 enable mask.
<code>uint8_t</code>	<code>ctsuchac3</code>
	TS24-TS31 enable mask.
<code>uint8_t</code>	<code>ctsuchac4</code>
	TS32-TS39 enable mask.
<code>uint8_t</code>	<code>ctsuchtrc0</code>
	TS00-TS07 mutual-tx mask.

uint8_t	<a href="#">ctsuchtrc1</a>
	TS08-TS15 mutual-tx mask.
uint8_t	<a href="#">ctsuchtrc2</a>
	TS16-TS23 mutual-tx mask.
uint8_t	<a href="#">ctsuchtrc3</a>
	TS24-TS31 mutual-tx mask.
uint8_t	<a href="#">ctsuchtrc4</a>
	TS32-TS39 mutual-tx mask.
<a href="#">ctsu_element_cfg_t</a> const *	<a href="#">p_elements</a>
	Pointer to elements configuration array.
uint8_t	<a href="#">num_rx</a>
	Number of receive terminals.
uint8_t	<a href="#">num_tx</a>
	Number of transmit terminals.
uint16_t	<a href="#">num_moving_average</a>
	Number of moving average for measurement data.
bool	<a href="#">tunning_enable</a>
	Initial offset tuning flag.

void(*	<a href="#">p_callback</a> )(ctsu_callback_args_t *p_args)
	Callback provided when CTSUFN ISR occurs.
<a href="#">transfer_instance_t</a> const *	<a href="#">p_transfer_tx</a>
	DTC instance for transmit at CTSUWR. Set to NULL if unused.
<a href="#">transfer_instance_t</a> const *	<a href="#">p_transfer_rx</a>
	DTC instance for receive at CTSURD. Set to NULL if unused.
<a href="#">adc_instance_t</a> const *	<a href="#">p_adc_instance</a>
	ADC instance for temperature correction.
IRQn_Type	<a href="#">write_irq</a>
	CTSU_CTSUWR interrupt vector.
IRQn_Type	<a href="#">read_irq</a>
	CTSU_CTSURD interrupt vector.
IRQn_Type	<a href="#">end_irq</a>
	CTSU_CTSUFN interrupt vector.
void const *	<a href="#">p_context</a>
	User defined context passed into callback function.
void const *	<a href="#">p_extend</a>
	Pointer to extended configuration by instance of interface.

#### ◆ [ctsu\\_api\\_t](#)

struct ctsu\_api\_t

Functions implemented at the HAL layer will follow this API.

### Data Fields

fsp\_err\_t(\* open )(ctsu\_ctrl\_t \*const p\_ctrl, ctsu\_cfg\_t const \*const p\_cfg)

fsp\_err\_t(\* scanStart )(ctsu\_ctrl\_t \*const p\_ctrl)

fsp\_err\_t(\* dataGet )(ctsu\_ctrl\_t \*const p\_ctrl, uint16\_t \*p\_data)

fsp\_err\_t(\* callbackSet )(ctsu\_ctrl\_t \*const p\_api\_ctrl,  
void(\*p\_callback)(ctsu\_callback\_args\_t \*), void const \*const  
p\_context, ctsu\_callback\_args\_t \*const p\_callback\_memory)

fsp\_err\_t(\* close )(ctsu\_ctrl\_t \*const p\_ctrl)

fsp\_err\_t(\* versionGet )(fsp\_version\_t \*const p\_data)

### Field Documentation

#### ◆ open

fsp\_err\_t(\* ctsu\_api\_t::open) (ctsu\_ctrl\_t \*const p\_ctrl, ctsu\_cfg\_t const \*const p\_cfg)

Open driver.

#### Implemented as

- R\_CTSU\_Open()

#### Parameters

[in]	p_ctrl	Pointer to control structure.
[in]	p_cfg	Pointer to pin configuration structure.



## ◆ scanStart

```
fsp_err_t(* ctsu_api_t::scanStart) (ctsu_ctrl_t *const p_ctrl)
```

Scan start.

**Implemented as**

- R\_CTSU\_ScanStart()

**Parameters**

[in]	p_ctrl	Pointer to control structure.
------	--------	-------------------------------

## ◆ dataGet

```
fsp_err_t(* ctsu_api_t::dataGet) (ctsu_ctrl_t *const p_ctrl, uint16_t *p_data)
```

Data get.

**Implemented as**

- R\_CTSU\_DataGet()

**Parameters**

[in]	p_ctrl	Pointer to control structure.
[out]	p_data	Pointer to get data array.

## ◆ callbackSet

```
fsp_err_t(* ctsu_api_t::callbackSet) (ctsu_ctrl_t *const p_api_ctrl,
void(*p_callback)(ctsu_callback_args_t *), void const *const p_context,
ctsu_callback_args_t *const p_callback_memory)
```

Specify callback function and optional context pointer and working memory pointer.

**Implemented as**

- R\_CTSU\_CallbackSet()

**Parameters**

[in]	p_ctrl	Pointer to the CTSU control block.
[in]	p_callback	Callback function
[in]	p_context	Pointer to send to callback function
[in]	p_working_memory	Pointer to volatile memory where callback structure can be allocated. Callback arguments allocated here are only valid during the callback.

◆ **close**

```
fsp_err_t(* ctsu_api_t::close) (ctsu_ctrl_t *const p_ctrl)
```

Close driver.

**Implemented as**

- R\_CTSU\_Close()

**Parameters**

[in]	p_ctrl	Pointer to control structure.
------	--------	-------------------------------

◆ **versionGet**

```
fsp_err_t(* ctsu_api_t::versionGet) (fsp_version_t *const p_data)
```

Return the version of the driver.

**Implemented as**

- R\_CTSU\_VersionGet()

**Parameters**

[in]	p_ctrl	Pointer to control structure.
[out]	p_data	Memory address to return version information to.

◆ **ctsu\_instance\_t**

```
struct ctsu_instance_t
```

This structure encompasses everything that is needed to use an instance of this interface.

## Data Fields

ctsu_ctrl_t *	p_ctrl	Pointer to the control structure for this instance.
ctsu_cfg_t const *	p_cfg	Pointer to the configuration structure for this instance.
ctsu_api_t const *	p_api	Pointer to the API structure for this instance.

**Typedef Documentation**

◆ **ctsu\_ctrl\_t**typedef void [ctsu\\_ctrl\\_t](#)

CTSU Control block. Allocate an instance specific control block to pass into the API calls.

**Implemented as**

- [ctsu\\_instance\\_ctrl\\_t](#)

**Enumeration Type Documentation**◆ **ctsu\_event\_t**enum [ctsu\\_event\\_t](#)

CTSU Events for callback function

## Enumerator

CTSU_EVENT_SCAN_COMPLETE	Normal end.
CTSU_EVENT_OVERFLOW	Sensor counter overflow (CTSUST.CTSUSOVF set)
CTSU_EVENT_ICOMP	Abnormal TSCAP voltage (CTSUERRS.CTSUICOMP set)
CTSU_EVENT_ICOMP1	Abnormal sensor current (CTSUSR.ICOMP1 set)

◆ **ctsu\_cap\_t**enum [ctsu\\_cap\\_t](#)

CTSU Scan Start Trigger Select

## Enumerator

CTSU_CAP_SOFTWARE	Scan start by software trigger.
CTSU_CAP_EXTERNAL	Scan start by external trigger.

◆ **ctsu\_txvsel\_t**

enum <a href="#">ctsu_txvsel_t</a>	
CTSU Transmission Power Supply Select	
Enumerator	
CTSU_TXVSEL_VCC	VCC selected.
CTSU_TXVSEL_INTERNAL_POWER	Internal logic power supply selected.

◆ **ctsu\_txvsel2\_t**

enum <a href="#">ctsu_txvsel2_t</a>	
CTSU Transmission Power Supply Select 2 (CTSU2 Only)	
Enumerator	
CTSU_TXVSEL_MODE	Follow TXVSEL setting.
CTSU_TXVSEL_VCC_PRIVATE	VCC private selected.

◆ **ctsu\_atune1\_t**

enum <a href="#">ctsu_atune1_t</a>	
CTSU Power Supply Capacity Adjustment (CTSU Only)	
Enumerator	
CTSU_ATUNE1_NORMAL	Normal output (40uA)
CTSU_ATUNE1_HIGH	High-current output (80uA)

◆ **ctsu\_atune12\_t**

enum <code>ctsu_atune12_t</code>	
CTSU Power Supply Capacity Adjustment (CTSUS2 Only)	
Enumerator	
<code>CTSU_ATUNE12_80UA</code>	High-current output (80uA)
<code>CTSU_ATUNE12_40UA</code>	Normal output (40uA)
<code>CTSU_ATUNE12_20UA</code>	Low-current output (20uA)
<code>CTSU_ATUNE12_160UA</code>	Very high-current output (160uA)

◆ **ctsu\_md\_t**

enum <code>ctsu_md_t</code>	
CTSU Measurement Mode Select	
Enumerator	
<code>CTSU_MODE_SELF_MULTI_SCAN</code>	Self-capacitance multi scan mode.
<code>CTSU_MODE_MUTUAL_FULL_SCAN</code>	Mutual capacitance full scan mode.
<code>CTSU_MODE_MUTUAL_CFC_SCAN</code>	Mutual capacitance cfc scan mode (CTSUS2 Only)
<code>CTSU_MODE_CURRENT_SCAN</code>	Current scan mode (CTSUS2 Only)
<code>CTSU_MODE_CORRECTION_SCAN</code>	Correction scan mode (CTSUS2 Only)

◆ **ctsu\_posel\_t**

enum <code>ctsu_posel_t</code>	
CTSU Non-Measured Channel Output Select (CTS2 Only)	
Enumerator	
<code>CTSU_POSEL_LOW_GPIO</code>	Output low through GPIO.
<code>CTSU_POSEL_HI_Z</code>	Hi-Z.
<code>CTSU_POSEL_LOW</code>	Output low through the power setting by the TXVSEL[1:0] bits.
<code>CTSU_POSEL_SAME_PULSE</code>	Same phase pulse output as transmission channel through the power setting by the TXVSEL[1:0] bits.

◆ **ctsu\_ssddiv\_t**

enum <code>ctsu_ssddiv_t</code>	
CTSU Spectrum Diffusion Frequency Division Setting (CTSU Only)	
Enumerator	
<code>CTSU_SSDIV_4000</code>	4.00 <= Base clock frequency (MHz)
<code>CTSU_SSDIV_2000</code>	2.00 <= Base clock frequency (MHz) < 4.00
<code>CTSU_SSDIV_1330</code>	1.33 <= Base clock frequency (MHz) < 2.00
<code>CTSU_SSDIV_1000</code>	1.00 <= Base clock frequency (MHz) < 1.33
<code>CTSU_SSDIV_0800</code>	0.80 <= Base clock frequency (MHz) < 1.00
<code>CTSU_SSDIV_0670</code>	0.67 <= Base clock frequency (MHz) < 0.80
<code>CTSU_SSDIV_0570</code>	0.57 <= Base clock frequency (MHz) < 0.67
<code>CTSU_SSDIV_0500</code>	0.50 <= Base clock frequency (MHz) < 0.57
<code>CTSU_SSDIV_0440</code>	0.44 <= Base clock frequency (MHz) < 0.50
<code>CTSU_SSDIV_0400</code>	0.40 <= Base clock frequency (MHz) < 0.44
<code>CTSU_SSDIV_0360</code>	0.36 <= Base clock frequency (MHz) < 0.40
<code>CTSU_SSDIV_0330</code>	0.33 <= Base clock frequency (MHz) < 0.36
<code>CTSU_SSDIV_0310</code>	0.31 <= Base clock frequency (MHz) < 0.33
<code>CTSU_SSDIV_0290</code>	0.29 <= Base clock frequency (MHz) < 0.31
<code>CTSU_SSDIV_0270</code>	0.27 <= Base clock frequency (MHz) < 0.29
<code>CTSU_SSDIV_0000</code>	0.00 <= Base clock frequency (MHz) < 0.27

## 4.3.9 DAC Interface

### Interfaces

#### Detailed Description

Interface for D/A converters.

## Summary

The DAC interface provides standard Digital/Analog Converter functionality. A DAC application writes digital sample data to the device and generates analog output on the DAC output pin.

Implemented by:

- [Digital to Analog Converter \(r\\_dac\)](#)
- [Digital to Analog Converter \(r\\_dac8\)](#)

### Data Structures

struct [dac\\_info\\_t](#)

struct [dac\\_cfg\\_t](#)

struct [dac\\_api\\_t](#)

struct [dac\\_instance\\_t](#)

### Typedefs

typedef void [dac\\_ctrl\\_t](#)

### Enumerations

enum [dac\\_data\\_format\\_t](#)

### Data Structure Documentation

#### ◆ [dac\\_info\\_t](#)

struct <a href="#">dac_info_t</a>		
DAC information structure to store various information for a DAC		
Data Fields		
uint8_t	bit_width	Resolution of the DAC.

#### ◆ [dac\\_cfg\\_t](#)

struct <a href="#">dac_cfg_t</a>		
DAC Open API configuration parameter		
Data Fields		
uint8_t	channel	ID associated with this DAC channel.
bool	ad_da_synchronized	AD/DA synchronization.
void const *	p_extend	



◆ **dac\_api\_t**

struct dac\_api\_t

DAC driver structure. General DAC functions implemented at the HAL layer follow this API.

**Data Fields**fsp\_err\_t(\* **open** )(dac\_ctrl\_t \*const p\_ctrl, dac\_cfg\_t const \*const p\_cfg)fsp\_err\_t(\* **close** )(dac\_ctrl\_t \*const p\_ctrl)fsp\_err\_t(\* **write** )(dac\_ctrl\_t \*const p\_ctrl, uint16\_t value)fsp\_err\_t(\* **start** )(dac\_ctrl\_t \*const p\_ctrl)fsp\_err\_t(\* **stop** )(dac\_ctrl\_t \*const p\_ctrl)fsp\_err\_t(\* **versionGet** )(fsp\_version\_t \*p\_version)**Field Documentation**◆ **open**

fsp\_err\_t(\* dac\_api\_t::open) (dac\_ctrl\_t \*const p\_ctrl, dac\_cfg\_t const \*const p\_cfg)

Initial configuration.

**Implemented as**

- R\_DAC\_Open()
- R\_DAC8\_Open()

**Parameters**

[in]	p_ctrl	Pointer to control block. Must be declared by user. Elements set here.
[in]	p_cfg	Pointer to configuration structure. All elements of this structure must be set by user.

◆ **close**

```
fsp_err_t(* dac_api_t::close) (dac_ctrl_t *const p_ctrl)
```

Close the D/A Converter.

**Implemented as**

- [R\\_DAC\\_Close\(\)](#)
- [R\\_DAC8\\_Close\(\)](#)

**Parameters**

[in]	p_ctrl	Control block set in <a href="#">dac_api_t::open</a> call for this timer.
------	--------	---------------------------------------------------------------------------

◆ **write**

```
fsp_err_t(* dac_api_t::write) (dac_ctrl_t *const p_ctrl, uint16_t value)
```

Write sample value to the D/A Converter.

**Implemented as**

- [R\\_DAC\\_Write\(\)](#)
- [R\\_DAC8\\_Write\(\)](#)

**Parameters**

[in]	p_ctrl	Control block set in <a href="#">dac_api_t::open</a> call for this timer.
[in]	value	Sample value to be written to the D/A Converter.

◆ **start**

```
fsp_err_t(* dac_api_t::start) (dac_ctrl_t *const p_ctrl)
```

Start the D/A Converter if it has not been started yet.

**Implemented as**

- [R\\_DAC\\_Start\(\)](#)
- [R\\_DAC8\\_Start\(\)](#)

**Parameters**

[in]	p_ctrl	Control block set in <a href="#">dac_api_t::open</a> call for this timer.
------	--------	---------------------------------------------------------------------------

◆ **stop**

```
fsp_err_t(* dac_api_t::stop) (dac_ctrl_t *const p_ctrl)
```

Stop the D/A Converter if the converter is running.

**Implemented as**

- R\_DAC\_Stop()
- R\_DAC8\_Stop()

**Parameters**

[in]	p_ctrl	Control block set in <a href="#">dac_api_t::open</a> call for this timer.
------	--------	---------------------------------------------------------------------------

◆ **versionGet**

```
fsp_err_t(* dac_api_t::versionGet) (fsp_version_t *p_version)
```

Get version and store it in provided pointer p\_version.

**Implemented as**

- R\_DAC\_VersionGet()
- R\_DAC8\_VersionGet()

**Parameters**

[out]	p_version	Code and API version used.
-------	-----------	----------------------------

◆ **dac\_instance\_t**

```
struct dac_instance_t
```

This structure encompasses everything that is needed to use an instance of this interface.

## Data Fields

<a href="#">dac_ctrl_t</a> *	p_ctrl	Pointer to the control structure for this instance.
<a href="#">dac_cfg_t</a> const *	p_cfg	Pointer to the configuration structure for this instance.
<a href="#">dac_api_t</a> const *	p_api	Pointer to the API structure for this instance.

**Typedef Documentation**

◆ **dac\_ctrl\_t**typedef void [dac\\_ctrl\\_t](#)

DAC control block. Allocate an instance specific control block to pass into the DAC API calls.

**Implemented as**

- [dac\\_instance\\_ctrl\\_t](#)
- [dac8\\_instance\\_ctrl\\_t](#)

**Enumeration Type Documentation**◆ **dac\_data\_format\_t**enum [dac\\_data\\_format\\_t](#)

DAC Open API data format settings.

## Enumerator

DAC\_DATA\_FORMAT\_FLUSH\_RIGHT

LSB of data is flush to the right leaving the top 4 bits unused.

DAC\_DATA\_FORMAT\_FLUSH\_LEFT

MSB of data is flush to the left leaving the bottom 4 bits unused.

**4.3.10 Display Interface**[Interfaces](#)**Detailed Description**

Interface for LCD panel displays.

**Summary**

The display interface provides standard display functionality:

- Signal timing configuration for LCD panels with RGB interface.
- Dot clock source selection (internal or external) and frequency divider.
- Blending of multiple graphics layers on the background screen.
- Color correction (brightness/configuration/gamma correction).
- Interrupts and callback function.

Implemented by: [Graphics LCD Controller \(r\\_glcdc\)](#)**Data Structures**

struct	<a href="#">display_timing_t</a>
struct	<a href="#">display_color_t</a>
struct	<a href="#">display_coordinate_t</a>
struct	<a href="#">display_brightness_t</a>
struct	<a href="#">display_contrast_t</a>
struct	<a href="#">display_correction_t</a>
struct	<a href="#">gamma_correction_t</a>
struct	<a href="#">display_gamma_correction_t</a>
struct	<a href="#">display_clut_t</a>
struct	<a href="#">display_input_cfg_t</a>
struct	<a href="#">display_output_cfg_t</a>
struct	<a href="#">display_layer_t</a>
struct	<a href="#">display_callback_args_t</a>
struct	<a href="#">display_cfg_t</a>
struct	<a href="#">display_runtime_cfg_t</a>
struct	<a href="#">display_clut_cfg_t</a>
struct	<a href="#">display_status_t</a>
struct	<a href="#">display_api_t</a>
struct	<a href="#">display_instance_t</a>

### Typedefs

---

typedef void	<a href="#">display_ctrl_t</a>
--------------	--------------------------------

### Enumerations

---

enum	<a href="#">display_frame_layer_t</a>
enum	<a href="#">display_state_t</a>
enum	<a href="#">display_event_t</a>

enum [display\\_in\\_format\\_t](#)enum [display\\_out\\_format\\_t](#)enum [display\\_endian\\_t](#)enum [display\\_color\\_order\\_t](#)enum [display\\_signal\\_polarity\\_t](#)enum [display\\_sync\\_edge\\_t](#)enum [display\\_fade\\_control\\_t](#)enum [display\\_fade\\_status\\_t](#)

## Data Structure Documentation

### ◆ [display\\_timing\\_t](#)

struct <a href="#">display_timing_t</a>		
Display signal timing setting		
Data Fields		
<a href="#">uint16_t</a>	<a href="#">total_cyc</a>	Total cycles in one line or total lines in one frame.
<a href="#">uint16_t</a>	<a href="#">display_cyc</a>	Active video cycles or lines.
<a href="#">uint16_t</a>	<a href="#">back_porch</a>	Back porch cycles or lines.
<a href="#">uint16_t</a>	<a href="#">sync_width</a>	Sync signal asserting width.
<a href="#">display_signal_polarity_t</a>	<a href="#">sync_polarity</a>	Sync signal polarity.

### ◆ [display\\_color\\_t](#)

struct <a href="#">display_color_t</a>	
RGB Color setting	

### ◆ [display\\_coordinate\\_t](#)

struct <a href="#">display_coordinate_t</a>		
Contrast (gain) correction setting		
Data Fields		
<a href="#">int16_t</a>	<a href="#">x</a>	Coordinate X, this allows to set signed value.
<a href="#">int16_t</a>	<a href="#">y</a>	Coordinate Y, this allows to set signed value.

◆ **display\_brightness\_t**

struct display_brightness_t		
Brightness (DC) correction setting		
Data Fields		
bool	enable	Brightness Correction On/Off.
uint16_t	r	Brightness (DC) adjustment for R channel.
uint16_t	g	Brightness (DC) adjustment for G channel.
uint16_t	b	Brightness (DC) adjustment for B channel.

◆ **display\_contrast\_t**

struct display_contrast_t		
Contrast (gain) correction setting		
Data Fields		
bool	enable	Contrast Correction On/Off.
uint8_t	r	Contrast (gain) adjustment for R channel.
uint8_t	g	Contrast (gain) adjustment for G channel.
uint8_t	b	Contrast (gain) adjustment for B channel.

◆ **display\_correction\_t**

struct display_correction_t		
Color correction setting		
Data Fields		
<a href="#">display_brightness_t</a>	brightness	Brightness.
<a href="#">display_contrast_t</a>	contrast	Contrast.

◆ **gamma\_correction\_t**

struct gamma_correction_t		
Gamma correction setting for each color		
Data Fields		
bool	enable	Gamma Correction On/Off.
uint16_t *	gain	Gain adjustment.
uint16_t *	threshold	Start threshold.

◆ **display\_gamma\_correction\_t**

struct display_gamma_correction_t		
Gamma correction setting		
Data Fields		
gamma_correction_t	r	Gamma correction for R channel.
gamma_correction_t	g	Gamma correction for G channel.
gamma_correction_t	b	Gamma correction for B channel.

◆ **display\_clut\_t**

struct display_clut_t		
CLUT setting		
Data Fields		
uint32_t	color_num	The number of colors in CLUT.
const uint32_t *	p_clut	Address of the area storing the CLUT data (in ARGB8888 format)

◆ **display\_input\_cfg\_t**

struct display_input_cfg_t		
Graphics plane input configuration structure		
Data Fields		
uint32_t *	p_base	Base address to the frame buffer.
uint16_t	hsize	Horizontal pixel size in a line.
uint16_t	vsize	Vertical pixel size in a frame.
uint32_t	hstride	Memory stride (bytes) in a line.
display_in_format_t	format	Input format setting.
bool	line_descending_enable	Line descending enable.
bool	lines_repeat_enable	Line repeat enable.
uint16_t	lines_repeat_times	Expected number of line repeating.

◆ **display\_output\_cfg\_t**

struct display_output_cfg_t		
Display output configuration structure		
Data Fields		



<a href="#">display_timing_t</a>	htiming	Horizontal display cycle setting.
<a href="#">display_timing_t</a>	vtiming	Vertical display cycle setting.
<a href="#">display_out_format_t</a>	format	Output format setting.
<a href="#">display_endian_t</a>	endian	Bit order of output data.
<a href="#">display_color_order_t</a>	color_order	Color order in pixel.
<a href="#">display_signal_polarity_t</a>	data_enable_polarity	Data Enable signal polarity.
<a href="#">display_sync_edge_t</a>	sync_edge	Signal sync edge selection.
<a href="#">display_color_t</a>	bg_color	Background color.
<a href="#">display_brightness_t</a>	brightness	Brightness setting.
<a href="#">display_contrast_t</a>	contrast	Contrast setting.
<a href="#">display_gamma_correction_t</a> *	p_gamma_correction	Pointer to gamma correction setting.
bool	dithering_on	Dithering on/off.

◆ **display\_layer\_t**

struct display_layer_t		
Graphics layer blend setup parameter structure		
Data Fields		
<a href="#">display_coordinate_t</a>	coordinate	Blending location (starting point of image)
<a href="#">display_color_t</a>	bg_color	Color outside region.
<a href="#">display_fade_control_t</a>	fade_control	Layer fade-in/out control on/off.
uint8_t	fade_speed	Layer fade-in/out frame rate.

◆ **display\_callback\_args\_t**

struct display_callback_args_t		
Display callback parameter definition		
Data Fields		
<a href="#">display_event_t</a>	event	Event code.
void const *	p_context	Context provided to user during callback.

◆ **display\_cfg\_t**

struct display_cfg_t		
Display main configuration structure		
<b>Data Fields</b>		
<a href="#">display_input_cfg_t</a>	input [2]	

	Graphics input frame setting. <a href="#">More...</a>
<a href="#">display_output_cfg_t</a>	<a href="#">output</a>
	Graphics output frame setting.
<a href="#">display_layer_t</a>	<a href="#">layer [2]</a>
	Graphics layer blend setting.
<a href="#">uint8_t</a>	<a href="#">line_detect_ipl</a>
	Line detect interrupt priority.
<a href="#">uint8_t</a>	<a href="#">underflow_1_ipl</a>
	Underflow 1 interrupt priority.
<a href="#">uint8_t</a>	<a href="#">underflow_2_ipl</a>
	Underflow 2 interrupt priority.
<a href="#">IRQn_Type</a>	<a href="#">line_detect_irq</a>
	Line detect interrupt vector.
<a href="#">IRQn_Type</a>	<a href="#">underflow_1_irq</a>
	Underflow 1 interrupt vector.
<a href="#">IRQn_Type</a>	<a href="#">underflow_2_irq</a>
	Underflow 2 interrupt vector.
<a href="#">void(*)</a>	<a href="#">p_callback</a> ( <a href="#">display_callback_args_t</a> *p_args)
	Pointer to callback function. <a href="#">More...</a>

void const *	<a href="#">p_context</a>
	User defined context passed into callback function.
void const *	<a href="#">p_extend</a>
	Display hardware dependent configuration. <a href="#">More...</a>

## Field Documentation

### ◆ input

[display\\_input\\_cfg\\_t](#) [display\\_cfg\\_t::input\[2\]](#)

Graphics input frame setting.

Generic configuration for display devices

### ◆ p\_callback

void(\* [display\\_cfg\\_t::p\\_callback](#)) ([display\\_callback\\_args\\_t](#) \*p\_args)

Pointer to callback function.

Configuration for display event processing

### ◆ p\_extend

void const\* [display\\_cfg\\_t::p\\_extend](#)

Display hardware dependent configuration.

Pointer to display peripheral specific configuration

### ◆ display\_runtime\_cfg\_t

struct [display\\_runtime\\_cfg\\_t](#)

Display main configuration structure

#### Data Fields

<a href="#">display_input_cfg_t</a>	input	Graphics input frame setting. Generic configuration for display devices
<a href="#">display_layer_t</a>	layer	Graphics layer alpha blending setting.

### ◆ display\_clut\_cfg\_t

struct [display\\_clut\\_cfg\\_t](#)

Display CLUT configuration structure		
Data Fields		
uint32_t *	p_base	Pointer to CLUT source data.
uint16_t	start	Beginning of CLUT entry to be updated.
uint16_t	size	Size of CLUT entry to be updated.

◆ **display\_status\_t**

struct display_status_t		
Display Status		
Data Fields		
display_state_t	state	Status of GLCDC module.
display_fade_status_t	fade_status[ DISPLAY_FRAME_LAYER_2+1]	Status of fade-in/fade-out status.

◆ **display\_api\_t**

struct display_api_t	
Shared Interface definition for display peripheral	
Data Fields	
fsp_err_t(*)	open )(display_ctrl_t *const p_ctrl, display_cfg_t const *const p_cfg)
fsp_err_t(*)	close )(display_ctrl_t *const p_ctrl)
fsp_err_t(*)	start )(display_ctrl_t *const p_ctrl)
fsp_err_t(*)	stop )(display_ctrl_t *const p_ctrl)
fsp_err_t(*)	layerChange )(display_ctrl_t const *const p_ctrl, display_runtime_cfg_t const *const p_cfg, display_frame_layer_t frame)
fsp_err_t(*)	bufferChange )(display_ctrl_t const *const p_ctrl, uint8_t *const framebuffer, display_frame_layer_t frame)
fsp_err_t(*)	correction )(display_ctrl_t const *const p_ctrl, display_correction_t const *const p_param)

<code>fsp_err_t(*</code>	<code>clut )(display_ctrl_t const *const p_ctrl, display_clut_cfg_t const *const p_clut_cfg, display_frame_layer_t layer)</code>
<code>fsp_err_t(*</code>	<code>clutEdit )(display_ctrl_t const *const p_ctrl, display_frame_layer_t layer, uint8_t index, uint32_t color)</code>
<code>fsp_err_t(*</code>	<code>statusGet )(display_ctrl_t const *const p_ctrl, display_status_t *const p_status)</code>
<code>fsp_err_t(*</code>	<code>versionGet )(fsp_version_t *p_version)</code>

## Field Documentation

### ◆ open

`fsp_err_t(* display_api_t::open) (display_ctrl_t *const p_ctrl, display_cfg_t const *const p_cfg)`

Open display device.

#### Implemented as

- `R_GLCDC_Open()`

#### Parameters

[in,out]	<code>p_ctrl</code>	Pointer to display interface control block. Must be declared by user. Value set here.
[in]	<code>p_cfg</code>	Pointer to display configuration structure. All elements of this structure must be set by user.

### ◆ close

`fsp_err_t(* display_api_t::close) (display_ctrl_t *const p_ctrl)`

Close display device.

#### Implemented as

- `R_GLCDC_Close()`

#### Parameters

[in]	<code>p_ctrl</code>	Pointer to display interface control block.
------	---------------------	---------------------------------------------

◆ **start**

```
fsp_err_t(* display_api_t::start) (display_ctrl_t *const p_ctrl)
```

Display start.

**Implemented as**

- R\_GLCDC\_Start()

**Parameters**

[in]	p_ctrl	Pointer to display interface control block.
------	--------	---------------------------------------------

◆ **stop**

```
fsp_err_t(* display_api_t::stop) (display_ctrl_t *const p_ctrl)
```

Display stop.

**Implemented as**

- R\_GLCDC\_Stop()

**Parameters**

[in]	p_ctrl	Pointer to display interface control block.
------	--------	---------------------------------------------

◆ **layerChange**

```
fsp_err_t(* display_api_t::layerChange) (display_ctrl_t const *const p_ctrl, display_runtime_cfg_t const *const p_cfg, display_frame_layer_t frame)
```

Change layer parameters at runtime.

**Implemented as**

- R\_GLCDC\_LayerChange()

**Parameters**

[in]	p_ctrl	Pointer to display interface control block.
[in]	p_cfg	Pointer to run-time layer configuration structure.
[in]	frame	Number of graphic frames.

◆ **bufferChange**

```
fsp_err_t(* display_api_t::bufferChange) (display_ctrl_t const *const p_ctrl, uint8_t *const framebuffer, display_frame_layer_t frame)
```

Change layer framebuffer pointer.

**Implemented as**

- R\_GLCDC\_BufferChange()

**Parameters**

[in]	p_ctrl	Pointer to display interface control block.
[in]	framebuffer	Pointer to desired framebuffer.
[in]	frame	Number of graphic frames.

◆ **correction**

```
fsp_err_t(* display_api_t::correction) (display_ctrl_t const *const p_ctrl, display_correction_t const *const p_param)
```

Color correction.

**Implemented as**

- R\_GLCDC\_ColorCorrection()

**Parameters**

[in]	p_ctrl	Pointer to display interface control block.
[in]	param	Pointer to color correction configuration structure.

◆ **clut**

```
fsp_err_t(* display_api_t::clut) (display_ctrl_t const *const p_ctrl, display_clut_cfg_t const *const p_clut_cfg, display_frame_layer_t layer)
```

Set CLUT for display device.

**Implemented as**

- R\_GLCDC\_ClutUpdate()

**Parameters**

[in]	p_ctrl	Pointer to display interface control block.
[in]	p_clut_cfg	Pointer to CLUT configuration structure.
[in]	layer	Layer number corresponding to the CLUT.

◆ **clutEdit**

```
fsp_err_t(* display_api_t::clutEdit) (display_ctrl_t const *const p_ctrl, display_frame_layer_t layer, uint8_t index, uint32_t color)
```

Set CLUT element for display device.

**Implemented as**

- R\_GLCDC\_ClutEdit()

**Parameters**

[in]	p_ctrl	Pointer to display interface control block.
[in]	layer	Layer number corresponding to the CLUT.
[in]	index	CLUT element index.
[in]	color	Desired CLUT index color.



◆ **statusGet**

```
fsp_err_t(* display_api_t::statusGet) (display_ctrl_t const *const p_ctrl, display_status_t *const p_status)
```

Get status for display device.

**Implemented as**

- [R\\_GLCDC\\_StatusGet\(\)](#)

**Parameters**

[in]	p_ctrl	Pointer to display interface control block.
[in]	status	Pointer to display interface status structure.

◆ **versionGet**

```
fsp_err_t(* display_api_t::versionGet) (fsp_version_t *p_version)
```

Get version.

**Implemented as**

- [R\\_GLCDC\\_VersionGet\(\)](#)

**Parameters**

[in]	p_version	Pointer to the memory to store the version information.
------	-----------	---------------------------------------------------------

◆ **display\_instance\_t**

```
struct display_instance_t
```

This structure encompasses everything that is needed to use an instance of this interface.

## Data Fields

<a href="#">display_ctrl_t</a> *	p_ctrl	Pointer to the control structure for this instance.
<a href="#">display_cfg_t</a> const *	p_cfg	Pointer to the configuration structure for this instance.
<a href="#">display_api_t</a> const *	p_api	Pointer to the API structure for this instance.

**Typedef Documentation**

◆ **display\_ctrl\_t**typedef void `display_ctrl_t`

Display control block. Allocate an instance specific control block to pass into the display API calls.

**Implemented as**

- `glcdc_instance_ctrl_t` Display control block

**Enumeration Type Documentation**◆ **display\_frame\_layer\_t**enum `display_frame_layer_t`

Display frame number

Enumerator

DISPLAY\_FRAME\_LAYER\_1

Frame layer 1.

DISPLAY\_FRAME\_LAYER\_2

Frame layer 2.

◆ **display\_state\_t**enum `display_state_t`

Display interface operation state

Enumerator

DISPLAY\_STATE\_CLOSED

Display closed.

DISPLAY\_STATE\_OPENED

Display opened.

DISPLAY\_STATE\_DISPLAYING

Displaying.

◆ **display\_event\_t**

enum <code>display_event_t</code>	
Display event codes	
Enumerator	
<code>DISPLAY_EVENT_GR1_UNDERFLOW</code>	Graphics frame1 underflow occurs.
<code>DISPLAY_EVENT_GR2_UNDERFLOW</code>	Graphics frame2 underflow occurs.
<code>DISPLAY_EVENT_LINE_DETECTION</code>	Designated line is processed.

◆ **display\_in\_format\_t**

enum <code>display_in_format_t</code>	
Input format setting	
Enumerator	
<code>DISPLAY_IN_FORMAT_32BITS_ARGB8888</code>	ARGB8888, 32 bits.
<code>DISPLAY_IN_FORMAT_32BITS_RGB888</code>	RGB888, 32 bits.
<code>DISPLAY_IN_FORMAT_16BITS_RGB565</code>	RGB565, 16 bits.
<code>DISPLAY_IN_FORMAT_16BITS_ARGB1555</code>	ARGB1555, 16 bits.
<code>DISPLAY_IN_FORMAT_16BITS_ARGB4444</code>	ARGB4444, 16 bits.
<code>DISPLAY_IN_FORMAT_CLUT8</code>	CLUT8.
<code>DISPLAY_IN_FORMAT_CLUT4</code>	CLUT4.
<code>DISPLAY_IN_FORMAT_CLUT1</code>	CLUT1.

◆ **display\_out\_format\_t**

enum <code>display_out_format_t</code>	
Output format setting	
Enumerator	
<code>DISPLAY_OUT_FORMAT_24BITS_RGB888</code>	RGB888, 24 bits.
<code>DISPLAY_OUT_FORMAT_18BITS_RGB666</code>	RGB666, 18 bits.
<code>DISPLAY_OUT_FORMAT_16BITS_RGB565</code>	RGB565, 16 bits.
<code>DISPLAY_OUT_FORMAT_8BITS_SERIAL</code>	SERIAL, 8 bits.

◆ **display\_endian\_t**

enum <code>display_endian_t</code>	
Data endian select	
Enumerator	
<code>DISPLAY_ENDIAN_LITTLE</code>	Little-endian.
<code>DISPLAY_ENDIAN_BIG</code>	Big-endian.

◆ **display\_color\_order\_t**

enum <code>display_color_order_t</code>	
RGB color order select	
Enumerator	
<code>DISPLAY_COLOR_ORDER_RGB</code>	Color order RGB.
<code>DISPLAY_COLOR_ORDER_BGR</code>	Color order BGR.

◆ **display\_signal\_polarity\_t**

enum <code>display_signal_polarity_t</code>	
Polarity of a signal select	
Enumerator	
<code>DISPLAY_SIGNAL_POLARITY_LOACTIVE</code>	Low active signal.
<code>DISPLAY_SIGNAL_POLARITY_HIACTIVE</code>	High active signal.

◆ **display\_sync\_edge\_t**

enum <code>display_sync_edge_t</code>	
Signal synchronization edge select	
Enumerator	
<code>DISPLAY_SIGNAL_SYNC_EDGE_RISING</code>	Signal is synchronized to rising edge.
<code>DISPLAY_SIGNAL_SYNC_EDGE_FALLING</code>	Signal is synchronized to falling edge.

◆ **display\_fade\_control\_t**

enum <code>display_fade_control_t</code>	
Fading control	
Enumerator	
<code>DISPLAY_FADE_CONTROL_NONE</code>	Applying no fading control.
<code>DISPLAY_FADE_CONTROL_FADEIN</code>	Applying fade-in control.
<code>DISPLAY_FADE_CONTROL_FADEOUT</code>	Applying fade-out control.

◆ **display\_fade\_status\_t**

enum <code>display_fade_status_t</code>	
Fading status	
Enumerator	
<code>DISPLAY_FADE_STATUS_NOT_UNDERWAY</code>	Fade-in/fade-out is not in progress.
<code>DISPLAY_FADE_STATUS_FADING_UNDERWAY</code>	Fade-in or fade-out is in progress.
<code>DISPLAY_FADE_STATUS_PENDING</code>	Fade-in/fade-out is configured but not yet started.

**4.3.11 DOC Interface**[Interfaces](#)**Detailed Description**

Interface for the Data Operation Circuit.

Defines the API and data structures for the DOC implementation of the Data Operation Circuit (DOC) interface.

**Summary**

This module implements the `DOC_API` using the Data Operation Circuit (DOC).

Implemented by: [Data Operation Circuit \(r\\_doc\)](#)

**Data Structures**

```
struct doc\_status\_t
```

```
struct doc\_callback\_args\_t
```

```
struct doc\_cfg\_t
```

```
struct doc\_api\_t
```

```
struct doc\_instance\_t
```

**Typedefs**

```
typedef void doc\_ctrl\_t
```

## Enumerations

enum [doc\\_event\\_t](#)

## Data Structure Documentation

### ◆ [doc\\_status\\_t](#)

struct <a href="#">doc_status_t</a>
DOC status

### ◆ [doc\\_callback\\_args\\_t](#)

struct <a href="#">doc_callback_args_t</a>		
Callback function parameter data.		
Data Fields		
void const *	<a href="#">p_context</a>	Set in <a href="#">doc_api_t::open</a> function in <a href="#">doc_cfg_t</a> .  Placeholder for user data.

### ◆ [doc\\_cfg\\_t](#)

struct <a href="#">doc_cfg_t</a>		
User configuration structure, used in the open function.		
<b>Data Fields</b>		
<a href="#">doc_event_t</a>	<a href="#">event</a>	Select enumerated value from <a href="#">doc_event_t</a> .
<a href="#">uint16_t</a>	<a href="#">doc_data</a>	Initial/reference value for DODSR register.
<a href="#">uint8_t</a>	<a href="#">ipl</a>	DOC interrupt priority.
<a href="#">IRQn_Type</a>	<a href="#">irq</a>	NVIC interrupt number assigned to this instance.

void(*	<a href="#">p_callback</a> )(doc_callback_args_t *p_args)
void const *	<a href="#">p_context</a>

## Field Documentation

### ◆ [p\\_callback](#)

void(\* doc\_cfg\_t::p\_callback) (doc\_callback\_args\_t \*p\_args)

Callback provided when a DOC ISR occurs.

### ◆ [p\\_context](#)

void const\* doc\_cfg\_t::p\_context

Placeholder for user data. Passed to the user callback in [doc\\_callback\\_args\\_t](#).

### ◆ [doc\\_api\\_t](#)

struct doc\_api\_t

Data Operation Circuit (DOC) API structure. DOC functions implemented at the HAL layer will follow this API.

#### Data Fields

fsp_err_t(*	<a href="#">open</a> )(doc_ctrl_t *const p_ctrl, doc_cfg_t const *const p_cfg)
fsp_err_t(*	<a href="#">close</a> )(doc_ctrl_t *const p_ctrl)
fsp_err_t(*	<a href="#">statusGet</a> )(doc_ctrl_t *const p_ctrl, doc_status_t *p_status)
fsp_err_t(*	<a href="#">write</a> )(doc_ctrl_t *const p_ctrl, uint16_t data)
fsp_err_t(*	<a href="#">versionGet</a> )(fsp_version_t *const p_version)
fsp_err_t(*	<a href="#">callbackSet</a> )(doc_ctrl_t *const p_api_ctrl, void(*p_callback)(doc_callback_args_t *), void const *const p_context, doc_callback_args_t *const p_callback_memory)

## Field Documentation



◆ **open**

```
fsp_err_t(* doc_api_t::open) (doc_ctrl_t *const p_ctrl, doc_cfg_t const *const p_cfg)
```

Initial configuration.

**Implemented as**

- R\_DOC\_Open()

**Parameters**

[in]	p_ctrl	Pointer to control block. Must be declared by user. Elements set here.
[in]	p_cfg	Pointer to configuration structure. All elements of this structure must be set by user.

◆ **close**

```
fsp_err_t(* doc_api_t::close) (doc_ctrl_t *const p_ctrl)
```

Allow the driver to be reconfigured. Will reduce power consumption.

**Implemented as**

- R\_DOC\_Close()

**Parameters**

[in]	p_ctrl	Control block set in <code>doc_api_t::open</code> call.
------	--------	---------------------------------------------------------

◆ **statusGet**

```
fsp_err_t(* doc_api_t::statusGet) (doc_ctrl_t *const p_ctrl, doc_status_t *p_status)
```

Gets the result of addition/subtraction and stores it in the provided pointer p\_data.

**Implemented as**

- R\_DOC\_StatusGet()

**Parameters**

[in]	p_ctrl	Control block set in <code>doc_api_t::open</code> call.
[out]	p_data	Provides the 16 bit result of the addition/subtraction operation at the user defined location.

**◆ write**`fsp_err_t(* doc_api_t::write) (doc_ctrl_t *const p_ctrl, uint16_t data)`

Write to the DODIR register.

**Implemented as**

- [R\\_DOC\\_Write\(\)](#)

**Parameters**

[in]	p_ctrl	Control block set in <a href="#">doc_api_t::open</a> call.
[in]	data	data to be written to DOC DODIR register.

**◆ versionGet**`fsp_err_t(* doc_api_t::versionGet) (fsp_version_t *const p_version)`

Get version and stores it in provided pointer p\_version.

**Implemented as**

- [R\\_DOC\\_VersionGet\(\)](#)

**Parameters**

[out]	p_version	Code and API version used.
-------	-----------	----------------------------

◆ **callbackSet**

```
fsp_err_t(* doc_api_t::callbackSet) (doc_ctrl_t*const p_api_ctrl,
void(*p_callback)(doc_callback_args_t*), void const*const p_context, doc_callback_args_t*const
p_callback_memory)
```

Specify callback function and optional context pointer and working memory pointer.

**Implemented as**

- [R\\_DOC\\_CallbackSet\(\)](#)

**Parameters**

[in]	p_ctrl	Pointer to the DOC control block.
[in]	p_callback	Callback function
[in]	p_context	Pointer to send to callback function
[in]	p_working_memory	Pointer to volatile memory where callback structure can be allocated. Callback arguments allocated here are only valid during the callback.

◆ **doc\_instance\_t**

```
struct doc_instance_t
```

This structure encompasses everything that is needed to use an instance of this interface.

## Data Fields

<a href="#">doc_ctrl_t</a> *	p_ctrl	Pointer to the control structure for this instance.
<a href="#">doc_cfg_t</a> const *	p_cfg	Pointer to the configuration structure for this instance.
<a href="#">doc_api_t</a> const *	p_api	Pointer to the API structure for this instance.

**Typedef Documentation**◆ **doc\_ctrl\_t**

```
typedef void doc_ctrl_t
```

DOC control block. Allocate an instance specific control block to pass into the DOC API calls.

**Implemented as**

- [doc\\_instance\\_ctrl\\_t](#)

## Enumeration Type Documentation

### ◆ doc\_event\_t

enum <a href="#">doc_event_t</a>	
Event that can trigger a callback function.	
Enumerator	
DOC_EVENT_COMPARISON_MISMATCH	Comparison of data has resulted in a mismatch.
DOC_EVENT_ADDITION	Addition of data has resulted in a value greater than H'FFFF.
DOC_EVENT_SUBTRACTION	Subtraction of data has resulted in a value less than H'0000.
DOC_EVENT_COMPARISON_MATCH	Comparison of data has resulted in a match.

## 4.3.12 ELC Interface

### Interfaces

#### Detailed Description

Interface for the Event Link Controller.

#### Data Structures

struct [elc\\_cfg\\_t](#)

struct [elc\\_api\\_t](#)

struct [elc\\_instance\\_t](#)

#### Typedefs

typedef void [elc\\_ctrl\\_t](#)

#### Enumerations

enum [elc\\_peripheral\\_t](#)

enum [elc\\_software\\_event\\_t](#)

## Data Structure Documentation

### ◆ elc\_cfg\_t

struct elc_cfg_t		
Main configuration structure for the Event Link Controller		
Data Fields		
elc_event_t const	link[ELC_PERIPHERAL_NUM]	Event link register (ELSR) settings.

### ◆ elc\_api\_t

struct elc_api_t	
ELC driver structure. General ELC functions implemented at the HAL layer follow this API.	
<b>Data Fields</b>	
fsp_err_t(*)	open )(elc_ctrl_t *const p_ctrl, elc_cfg_t const *const p_cfg)
fsp_err_t(*)	close )(elc_ctrl_t *const p_ctrl)
fsp_err_t(*)	softwareEventGenerate )(elc_ctrl_t *const p_ctrl, elc_software_event_t event_num)
fsp_err_t(*)	linkSet )(elc_ctrl_t *const p_ctrl, elc_peripheral_t peripheral, elc_event_t signal)
fsp_err_t(*)	linkBreak )(elc_ctrl_t *const p_ctrl, elc_peripheral_t peripheral)
fsp_err_t(*)	enable )(elc_ctrl_t *const p_ctrl)
fsp_err_t(*)	disable )(elc_ctrl_t *const p_ctrl)
fsp_err_t(*)	versionGet )(fsp_version_t *const p_version)

## Field Documentation

◆ **open**

```
fsp_err_t(* elc_api_t::open) (elc_ctrl_t *const p_ctrl, elc_cfg_t const *const p_cfg)
```

Initialize all links in the Event Link Controller.

**Implemented as**

- R\_ELC\_Open()

**Parameters**

[in]	p_ctrl	Pointer to control structure.
[in]	p_cfg	Pointer to configuration structure.

◆ **close**

```
fsp_err_t(* elc_api_t::close) (elc_ctrl_t *const p_ctrl)
```

Disable all links in the Event Link Controller and close the API.

**Implemented as**

- R\_ELC\_Close()

**Parameters**

[in]	p_ctrl	Pointer to control structure.
------	--------	-------------------------------

◆ **softwareEventGenerate**

```
fsp_err_t(* elc_api_t::softwareEventGenerate) (elc_ctrl_t *const p_ctrl, elc_software_event_t event_num)
```

Generate a software event in the Event Link Controller.

**Implemented as**

- R\_ELC\_SoftwareEventGenerate()

**Parameters**

[in]	p_ctrl	Pointer to control structure.
[in]	eventNum	Software event number to be generated.

**◆ linkSet**

```
fsp_err_t(* elc_api_t::linkSet) (elc_ctrl_t *const p_ctrl, elc_peripheral_t peripheral, elc_event_t signal)
```

Create a single event link.

**Implemented as**

- R\_ELC\_LinkSet()

**Parameters**

[in]	p_ctrl	Pointer to control structure.
[in]	peripheral	The peripheral block that will receive the event signal.
[in]	signal	The event signal.

**◆ linkBreak**

```
fsp_err_t(* elc_api_t::linkBreak) (elc_ctrl_t *const p_ctrl, elc_peripheral_t peripheral)
```

Break an event link.

**Implemented as**

- R\_ELC\_LinkBreak()

**Parameters**

[in]	p_ctrl	Pointer to control structure.
[in]	peripheral	The peripheral that should no longer be linked.

**◆ enable**

```
fsp_err_t(* elc_api_t::enable) (elc_ctrl_t *const p_ctrl)
```

Enable the operation of the Event Link Controller.

**Implemented as**

- R\_ELC\_Enable()

**Parameters**

[in]	p_ctrl	Pointer to control structure.
------	--------	-------------------------------

◆ **disable**

```
fsp_err_t(* elc_api_t::disable) (elc_ctrl_t *const p_ctrl)
```

Disable the operation of the Event Link Controller.

**Implemented as**

- [R\\_ELC\\_Disable\(\)](#)

**Parameters**

[in]	p_ctrl	Pointer to control structure.
------	--------	-------------------------------

◆ **versionGet**

```
fsp_err_t(* elc_api_t::versionGet) (fsp_version_t *const p_version)
```

Get the driver version based on compile time macros.

**Implemented as**

- [R\\_ELC\\_VersionGet\(\)](#)

**Parameters**

[in]	p_ctrl	Pointer to control structure.
[out]	p_version	is value returned.

◆ **elc\_instance\_t**

```
struct elc_instance_t
```

This structure encompasses everything that is needed to use an instance of this interface.

## Data Fields

elc_ctrl_t *	p_ctrl	Pointer to the control structure for this instance.
elc_cfg_t const *	p_cfg	Pointer to the configuration structure for this instance.
elc_api_t const *	p_api	Pointer to the API structure for this instance.

**Typedef Documentation**◆ **elc\_ctrl\_t**

```
typedef void elc_ctrl_t
```

ELC control block. Allocate an instance specific control block to pass into the ELC API calls.

**Implemented as**

- [elc\\_instance\\_ctrl\\_t](#)



## Enumeration Type Documentation

### ◆ `elc_peripheral_t`

enum `elc_peripheral_t`

Possible peripherals to be linked to event signals (not all available on all MCUs)

### ◆ `elc_software_event_t`

enum `elc_software_event_t`

Software event number

Enumerator

`ELC_SOFTWARE_EVENT_0`

Software event 0.

`ELC_SOFTWARE_EVENT_1`

Software event 1.

## 4.3.13 Ethernet Interface

### Interfaces

#### Detailed Description

Interface for Ethernet functions.

## Summary

The Ethernet interface provides Ethernet functionality. The Ethernet interface supports the following features:

- Transmit/receive processing (Blocking and Non-Blocking)
- Callback function with returned event code
- Magic packet detection mode support
- Auto negotiation support
- Flow control support
- Multicast filtering support

Implemented by:

- [Ethernet \(`r\_ether`\)](#)

#### Data Structures

struct `ether_instance_descriptor_t`

```
struct ether_callback_args_t
```

```
struct ether_cfg_t
```

```
struct ether_api_t
```

```
struct ether_instance_t
```

## Typedefs

```
typedef void ether_ctrl_t
```

## Enumerations

```
enum ether_wake_on_lan_t
```

```
enum ether_flow_control_t
```

```
enum ether_multicast_t
```

```
enum ether_promiscuous_t
```

```
enum ether_zerocopy_t
```

```
enum ether_event_t
```

## Data Structure Documentation

### ◆ ether\_instance\_descriptor\_t

```
struct ether_instance_descriptor_t
```

EDMAC descriptor as defined in the hardware manual. Structure must be packed at 1 byte.

### ◆ ether\_callback\_args\_t

```
struct ether_callback_args_t
```

Callback function parameter data

Data Fields		
uint32_t	channel	Device channel number.
<a href="#">ether_event_t</a>	event	Event code.
uint32_t	status_ecsr	ETHERC status register for interrupt handler.
uint32_t	status_eesr	ETHERC/EDMAC status register for interrupt handler.
void const *	p_context	Placeholder for user data. Set in <a href="#">ether_api_t::open</a> function in

ether\_cfg\_t.

## ◆ ether\_cfg\_t

struct ether\_cfg\_t

Configuration parameters.

**Data Fields**

uint8_t	<a href="#">channel</a>
	Channel.
<a href="#">ether_zerocopy_t</a>	<a href="#">zerocopy</a>
	Zero copy enable or disable in Read/Write function.
<a href="#">ether_multicast_t</a>	<a href="#">multicast</a>
	Multicast enable or disable.
<a href="#">ether_promiscuous_t</a>	<a href="#">promiscuous</a>
	Promiscuous mode enable or disable.
<a href="#">ether_flow_control_t</a>	<a href="#">flow_control</a>
	Flow control functionally enable or disable.
uint32_t	<a href="#">broadcast_filter</a>
	Limit of the number of broadcast frames received continuously.
uint8_t *	<a href="#">p_mac_address</a>
	Pointer of MAC address.
<a href="#">ether_instance_descriptor_t</a> *	<a href="#">p_rx_descriptors</a>
	Receive descriptor buffer pool.

<code>ether_instance_descriptor_t *</code>	<code>p_tx_descriptors</code>
	Transmit descriptor buffer pool.
<code>uint8_t</code>	<code>num_tx_descriptors</code>
	Number of transmission descriptor.
<code>uint8_t</code>	<code>num_rx_descriptors</code>
	Number of receive descriptor.
<code>uint8_t **</code>	<code>pp_ether_buffers</code>
	Transmit and receive buffer.
<code>uint32_t</code>	<code>ether_buffer_size</code>
	Size of transmit and receive buffer.
<code>IRQn_Type</code>	<code>irq</code>
	NVIC interrupt number.
<code>uint32_t</code>	<code>interrupt_priority</code>
	NVIC interrupt priority.
<code>void(*</code>	<code>p_callback</code> <code>)(ether_callback_args_t *p_args)</code>
	Callback provided when an ISR occurs.
<code>ether_phy_instance_t const *</code>	<code>p_ether_phy_instance</code>
	Pointer to ETHER_PHY instance.

void const *	<a href="#">p_context</a>
	Placeholder for user data. <a href="#">More...</a>
void const *	<a href="#">p_extend</a>
	Placeholder for user extension.

## Field Documentation

### ◆ [p\\_context](#)

void const\* ether\_cfg\_t::p\_context

Placeholder for user data.

Placeholder for user data. Passed to the user callback in [ether\\_callback\\_args\\_t](#).

### ◆ [ether\\_api\\_t](#)

struct ether\_api\_t

Functions implemented at the HAL layer will follow this API.

#### Data Fields

<a href="#">fsp_err_t</a> (*	<a href="#">open</a> )(ether_ctrl_t *const p_api_ctrl, <a href="#">ether_cfg_t</a> const *const p_cfg)
<a href="#">fsp_err_t</a> (*	<a href="#">close</a> )(ether_ctrl_t *const p_api_ctrl)
<a href="#">fsp_err_t</a> (*	<a href="#">read</a> )(ether_ctrl_t *const p_api_ctrl, void *const p_buffer, uint32_t *const length_bytes)
<a href="#">fsp_err_t</a> (*	<a href="#">bufferRelease</a> )(ether_ctrl_t *const p_api_ctrl)
<a href="#">fsp_err_t</a> (*	<a href="#">write</a> )(ether_ctrl_t *const p_api_ctrl, void *const p_buffer, uint32_t const frame_length)
<a href="#">fsp_err_t</a> (*	<a href="#">linkProcess</a> )(ether_ctrl_t *const p_api_ctrl)
<a href="#">fsp_err_t</a> (*	<a href="#">wakeOnLANEnable</a> )(ether_ctrl_t *const p_api_ctrl)

<code>fsp_err_t(*</code>	<code>versionGet )(fsp_version_t *const p_data)</code>
--------------------------	--------------------------------------------------------

## Field Documentation

### ◆ open

<code>fsp_err_t(* ether_api_t::open) (ether_ctrl_t *const p_api_ctrl, ether_cfg_t const *const p_cfg)</code>
--------------------------------------------------------------------------------------------------------------

Open driver.

#### Implemented as

- [R\\_ETHER\\_Open\(\)](#)

#### Parameters

[in]	p_api_ctrl	Pointer to control structure.
[in]	p_cfg	Pointer to pin configuration structure.

### ◆ close

<code>fsp_err_t(* ether_api_t::close) (ether_ctrl_t *const p_api_ctrl)</code>
-------------------------------------------------------------------------------

Close driver.

#### Implemented as

- [R\\_ETHER\\_Close\(\)](#)

#### Parameters

[in]	p_api_ctrl	Pointer to control structure.
------	------------	-------------------------------

### ◆ read

<code>fsp_err_t(* ether_api_t::read) (ether_ctrl_t *const p_api_ctrl, void *const p_buffer, uint32_t *const length_bytes)</code>
----------------------------------------------------------------------------------------------------------------------------------

Read packet if data is available.

#### Implemented as

- [R\\_ETHER\\_Read\(\)](#)

#### Parameters

[in]	p_api_ctrl	Pointer to control structure.
[in]	p_buffer	Pointer to where to store read data.
[in]	length_bytes	Number of bytes in buffer

◆ **bufferRelease**

```
fsp_err_t(* ether_api_t::bufferRelease) (ether_ctrl_t *const p_api_ctrl)
```

Release rx buffer from buffer pool process in zero-copy read operation.

**Implemented as**

- [R\\_ETHER\\_BufferRelease\(\)](#)

**Parameters**

[in]	p_api_ctrl	Pointer to control structure.
------	------------	-------------------------------

◆ **write**

```
fsp_err_t(* ether_api_t::write) (ether_ctrl_t *const p_api_ctrl, void *const p_buffer, uint32_t const frame_length)
```

Write packet.

**Implemented as**

- [R\\_ETHER\\_Write\(\)](#)

**Parameters**

[in]	p_api_ctrl	Pointer to control structure.
[in]	p_buffer	Pointer to data to write.
[in]	frame_length	Send ethernet frame size (without 4 bytes of CRC data size).

◆ **linkProcess**

```
fsp_err_t(* ether_api_t::linkProcess) (ether_ctrl_t *const p_api_ctrl)
```

Process link.

**Implemented as**

- [R\\_ETHER\\_LinkProcess\(\)](#)

**Parameters**

[in]	p_api_ctrl	Pointer to control structure.
------	------------	-------------------------------

◆ **wakeOnLANEnable**

```
fsp_err_t(* ether_api_t::wakeOnLANEnable) (ether_ctrl_t *const p_api_ctrl)
```

Enable magic packet detection.

**Implemented as**

- [R\\_ETHER\\_WakeOnLANEnable\(\)](#)

**Parameters**

[in]	p_api_ctrl	Pointer to control structure.
------	------------	-------------------------------

◆ **versionGet**

```
fsp_err_t(* ether_api_t::versionGet) (fsp_version_t *const p_data)
```

Return the version of the driver.

**Implemented as**

- [R\\_ETHER\\_VersionGet\(\)](#)

**Parameters**

[out]	p_data	Memory address to return version information to.
-------	--------	--------------------------------------------------

◆ **ether\_instance\_t**

```
struct ether_instance_t
```

This structure encompasses everything that is needed to use an instance of this interface.

## Data Fields

<a href="#">ether_ctrl_t</a> *	p_ctrl	Pointer to the control structure for this instance.
<a href="#">ether_cfg_t</a> const *	p_cfg	Pointer to the configuration structure for this instance.
<a href="#">ether_api_t</a> const *	p_api	Pointer to the API structure for this instance.

**Typedef Documentation**◆ **ether\_ctrl\_t**

```
typedef void ether_ctrl_t
```

Control block. Allocate an instance specific control block to pass into the API calls.

**Implemented as**

- [ether\\_instance\\_ctrl\\_t](#)



## Enumeration Type Documentation

### ◆ ether\_wake\_on\_lan\_t

enum ether_wake_on_lan_t	
Wake on LAN	
Enumerator	
ETHER_WAKE_ON_LAN_DISABLE	Disable Wake on LAN.
ETHER_WAKE_ON_LAN_ENABLE	Enable Wake on LAN.

### ◆ ether\_flow\_control\_t

enum ether_flow_control_t	
Flow control functionality	
Enumerator	
ETHER_FLOW_CONTROL_DISABLE	Disable flow control functionality.
ETHER_FLOW_CONTROL_ENABLE	Enable flow control functionality with pause frames.

### ◆ ether\_multicast\_t

enum ether_multicast_t	
Multicast Filter	
Enumerator	
ETHER_MULTICAST_DISABLE	Disable reception of multicast frames.
ETHER_MULTICAST_ENABLE	Enable reception of multicast frames.

## ◆ ether\_promiscuous\_t

enum ether_promiscuous_t	
Promiscuous Mode	
Enumerator	
ETHER_PROMISCUOUS_DISABLE	Only receive packets with current MAC address, multicast, and broadcast.
ETHER_PROMISCUOUS_ENABLE	Receive all packets.

## ◆ ether\_zerocopy\_t

enum ether_zerocopy_t	
Zero copy	
Enumerator	
ETHER_ZEROCOPY_DISABLE	Disable zero copy in Read/Write function.
ETHER_ZEROCOPY_ENABLE	Enable zero copy in Read/Write function.

## ◆ ether\_event\_t

enum ether_event_t	
Event code of callback function	
Enumerator	
ETHER_EVENT_WAKEON_LAN	Magic packet detection event.
ETHER_EVENT_LINK_ON	Link up detection event.
ETHER_EVENT_LINK_OFF	Link down detection event.
ETHER_EVENT_INTERRUPT	Interrupt event.

## 4.3.14 Ethernet PHY Interface

### Interfaces

#### Detailed Description

Interface for Ethernet PHY functions.

## Summary

The Ethernet PHY module (`r_ether_phy`) provides an API for standard Ethernet PHY communications applications that use the ETHERC peripheral.

The Ethernet PHY interface supports the following features:

- Auto negotiation support
- Flow control support
- Link status check support

Implemented by:

- [Ethernet PHY \(`r\_ether\_phy`\)](#)

### Data Structures

struct [ether\\_phy\\_cfg\\_t](#)

struct [ether\\_phy\\_api\\_t](#)

struct [ether\\_phy\\_instance\\_t](#)

### Typedefs

typedef void [ether\\_phy\\_ctrl\\_t](#)

### Enumerations

enum [ether\\_phy\\_flow\\_control\\_t](#)

enum [ether\\_phy\\_link\\_speed\\_t](#)

enum [ether\\_phy\\_mii\\_type\\_t](#)

### Data Structure Documentation

#### ◆ ether\_phy\_cfg\_t

struct ether_phy_cfg_t		
Configuration parameters.		
Data Fields		
uint8_t	channel	Channel.
uint8_t	phy_lsi_address	Address of PHY-LSI.
uint32_t	phy_reset_wait_time	Wait time for PHY-LSI reboot.
int32_t	mii_bit_access_wait_time	Wait time for MII/RMII access.

<a href="#">ether_phy_flow_control_t</a>	flow_control	Flow control functionally enable or disable.
<a href="#">ether_phy_mii_type_t</a>	mii_type	Interface type is MII or RMII.
void const *	p_context	Placeholder for user data. Passed to the user callback in ether_phy_callback_args_t.
void const *	p_extend	Placeholder for user extension.

### ◆ ether\_phy\_api\_t

struct ether_phy_api_t	
Functions implemented at the HAL layer will follow this API.	
<b>Data Fields</b>	
<a href="#">fsp_err_t</a> (*	<a href="#">open</a> )(ether_phy_ctrl_t *const p_api_ctrl, ether_phy_cfg_t const *const p_cfg)
<a href="#">fsp_err_t</a> (*	<a href="#">close</a> )(ether_phy_ctrl_t *const p_api_ctrl)
<a href="#">fsp_err_t</a> (*	<a href="#">startAutoNegotiate</a> )(ether_phy_ctrl_t *const p_api_ctrl)
<a href="#">fsp_err_t</a> (*	<a href="#">linkPartnerAbilityGet</a> )(ether_phy_ctrl_t *const p_api_ctrl, uint32_t *const p_line_speed_duplex, uint32_t *const p_local_pause, uint32_t *const p_partner_pause)
<a href="#">fsp_err_t</a> (*	<a href="#">linkStatusGet</a> )(ether_phy_ctrl_t *const p_api_ctrl)
<a href="#">fsp_err_t</a> (*	<a href="#">versionGet</a> )(fsp_version_t *const p_data)
<b>Field Documentation</b>	

◆ **open**

```
fsp_err_t(* ether_phy_api_t::open) (ether_phy_ctrl_t *const p_api_ctrl, ether_phy_cfg_t const *const p_cfg)
```

Open driver.

**Implemented as**

- R\_ETHER\_PHY\_Open()

**Parameters**

[in]	p_api_ctrl	Pointer to control structure.
[in]	p_cfg	Pointer to pin configuration structure.

◆ **close**

```
fsp_err_t(* ether_phy_api_t::close) (ether_phy_ctrl_t *const p_api_ctrl)
```

Close driver.

**Implemented as**

- R\_ETHER\_PHY\_Close()

**Parameters**

[in]	p_api_ctrl	Pointer to control structure.
------	------------	-------------------------------

◆ **startAutoNegotiate**

```
fsp_err_t(* ether_phy_api_t::startAutoNegotiate) (ether_phy_ctrl_t *const p_api_ctrl)
```

Start auto negotiation.

**Implemented as**

- R\_ETHER\_PHY\_StartAutoNegotiate()

**Parameters**

[in]	p_api_ctrl	Pointer to control structure.
------	------------	-------------------------------

◆ **linkPartnerAbilityGet**

```
fsp_err_t(* ether_phy_api_t::linkPartnerAbilityGet) (ether_phy_ctrl_t *const p_api_ctrl, uint32_t *const p_line_speed_duplex, uint32_t *const p_local_pause, uint32_t *const p_partner_pause)
```

Get the partner ability.

**Implemented as**

- [R\\_ETHER\\_PHY\\_LinkPartnerAbilityGet\(\)](#)

**Parameters**

[in]	p_api_ctrl	Pointer to control structure.
[out]	p_line_speed_duplex	Pointer to the location of both the line speed and the duplex.
[out]	p_local_pause	Pointer to the location to store the local pause bits.
[out]	p_partner_pause	Pointer to the location to store the partner pause bits.

◆ **linkStatusGet**

```
fsp_err_t(* ether_phy_api_t::linkStatusGet) (ether_phy_ctrl_t *const p_api_ctrl)
```

Get Link status from PHY-LSI interface.

**Implemented as**

- [R\\_ETHER\\_PHY\\_LinkStatusGet\(\)](#)

**Parameters**

[in]	p_api_ctrl	Pointer to control structure.
------	------------	-------------------------------

◆ **versionGet**

```
fsp_err_t(* ether_phy_api_t::versionGet) (fsp_version_t *const p_data)
```

Return the version of the driver.

**Implemented as**

- [R\\_ETHER\\_PHY\\_VersionGet\(\)](#)

**Parameters**

[out]	p_data	Memory address to return version information to.
-------	--------	--------------------------------------------------

◆ **ether\_phy\_instance\_t**

```
struct ether_phy_instance_t
```

This structure encompasses everything that is needed to use an instance of this interface.

Data Fields		
<code>ether_phy_ctrl_t *</code>	<code>p_ctrl</code>	Pointer to the control structure for this instance.
<code>ether_phy_cfg_t const *</code>	<code>p_cfg</code>	Pointer to the configuration structure for this instance.
<code>ether_phy_api_t const *</code>	<code>p_api</code>	Pointer to the API structure for this instance.

## Typedef Documentation

### ◆ `ether_phy_ctrl_t`

```
typedef void ether_phy_ctrl_t
```

Control block. Allocate an instance specific control block to pass into the API calls.

#### Implemented as

- `ether_phy_instance_ctrl_t`

## Enumeration Type Documentation

### ◆ `ether_phy_flow_control_t`

```
enum ether_phy_flow_control_t
```

Flow control functionality

#### Enumerator

<code>ETHER_PHY_FLOW_CONTROL_DISABLE</code>	Disable flow control functionality.
<code>ETHER_PHY_FLOW_CONTROL_ENABLE</code>	Enable flow control functionality with pause frames.

## ◆ ether\_phy\_link\_speed\_t

enum ether_phy_link_speed_t	
Link speed	
Enumerator	
ETHER_PHY_LINK_SPEED_NO_LINK	Link is not established.
ETHER_PHY_LINK_SPEED_10H	Link status is 10Mbit/s and half duplex.
ETHER_PHY_LINK_SPEED_10F	Link status is 10Mbit/s and full duplex.
ETHER_PHY_LINK_SPEED_100H	Link status is 100Mbit/s and half duplex.
ETHER_PHY_LINK_SPEED_100F	Link status is 100Mbit/s and full duplex.

## ◆ ether\_phy\_mii\_type\_t

enum ether_phy_mii_type_t	
Media-independent interface	
Enumerator	
ETHER_PHY_MII_TYPE_MII	MII.
ETHER_PHY_MII_TYPE_RMII	RMII.

### 4.3.15 External IRQ Interface

#### Interfaces

#### Detailed Description

Interface for detecting external interrupts.

## Summary

The External IRQ Interface is for configuring interrupts to fire when a trigger condition is detected on an external IRQ pin.

The External IRQ Interface can be implemented by:

- [Interrupt Controller Unit \(r\\_icu\)](#)



## Data Structures

struct [external\\_irq\\_callback\\_args\\_t](#)

struct [external\\_irq\\_cfg\\_t](#)

struct [external\\_irq\\_api\\_t](#)

struct [external\\_irq\\_instance\\_t](#)

## Macros

#define [EXTERNAL\\_IRQ\\_API\\_VERSION\\_MAJOR](#)  
EXTERNAL IRQ API version number (Major)

#define [EXTERNAL\\_IRQ\\_API\\_VERSION\\_MINOR](#)  
EXTERNAL IRQ API version number (Minor)

## Typedefs

typedef void [external\\_irq\\_ctrl\\_t](#)

## Enumerations

enum [external\\_irq\\_trigger\\_t](#)

enum [external\\_irq\\_pclk\\_div\\_t](#)

## Data Structure Documentation

### ◆ external\_irq\_callback\_args\_t

struct <a href="#">external_irq_callback_args_t</a>		
Callback function parameter data		
Data Fields		
void const *	p_context	Placeholder for user data. Set in <a href="#">external_irq_api_t::open</a> function in <a href="#">external_irq_cfg_t</a> .
uint32_t	channel	The physical hardware channel that caused the interrupt.

### ◆ external\_irq\_cfg\_t

struct <a href="#">external_irq_cfg_t</a>		
User configuration structure, used in open function		
<b>Data Fields</b>		

uint8_t	<a href="#">channel</a>
	Hardware channel used.
uint8_t	<a href="#">ipl</a>
	Interrupt priority.
IRQn_Type	<a href="#">irq</a>
	NVIC interrupt number assigned to this instance.
<a href="#">external_irq_trigger_t</a>	<a href="#">trigger</a>
	Trigger setting.
<a href="#">external_irq_pclk_div_t</a>	<a href="#">pclk_div</a>
	Digital filter clock divisor setting.
bool	<a href="#">filter_enable</a>
	Digital filter enable/disable setting.
void(*	<a href="#">p_callback</a> )(external_irq_callback_args_t *p_args)
void const *	<a href="#">p_context</a>
void const *	<a href="#">p_extend</a>
	External IRQ hardware dependent configuration.

## Field Documentation

◆ **p\_callback**

```
void(* external_irq_cfg_t::p_callback) (external_irq_callback_args_t *p_args)
```

Callback provided external input trigger occurs.

◆ **p\_context**

```
void const* external_irq_cfg_t::p_context
```

Placeholder for user data. Passed to the user callback in [external\\_irq\\_callback\\_args\\_t](#).

◆ **external\_irq\_api\_t**

```
struct external_irq_api_t
```

External interrupt driver structure. External interrupt functions implemented at the HAL layer will follow this API.

**Data Fields**

fsp_err_t(*	<a href="#">open</a> )(external_irq_ctrl_t *const p_ctrl, external_irq_cfg_t const *const p_cfg)
-------------	--------------------------------------------------------------------------------------------------

fsp_err_t(*	<a href="#">enable</a> )(external_irq_ctrl_t *const p_ctrl)
-------------	-------------------------------------------------------------

fsp_err_t(*	<a href="#">disable</a> )(external_irq_ctrl_t *const p_ctrl)
-------------	--------------------------------------------------------------

fsp_err_t(*	<a href="#">callbackSet</a> )(external_irq_ctrl_t *const p_api_ctrl, void(*p_callback)(external_irq_callback_args_t *), void const *const p_context, external_irq_callback_args_t *const p_callback_memory)
-------------	-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------

fsp_err_t(*	<a href="#">close</a> )(external_irq_ctrl_t *const p_ctrl)
-------------	------------------------------------------------------------

fsp_err_t(*	<a href="#">versionGet</a> )(fsp_version_t *const p_version)
-------------	--------------------------------------------------------------

**Field Documentation**

◆ **open**

```
fsp_err_t(* external_irq_api_t::open) (external_irq_ctrl_t *const p_ctrl, external_irq_cfg_t const *const p_cfg)
```

Initial configuration.

**Implemented as**

- R\_ICU\_ExtrenalIrqOpen()

**Parameters**

[out]	p_ctrl	Pointer to control block. Must be declared by user. Value set here.
[in]	p_cfg	Pointer to configuration structure. All elements of the structure must be set by user.

◆ **enable**

```
fsp_err_t(* external_irq_api_t::enable) (external_irq_ctrl_t *const p_ctrl)
```

Enable callback when an external trigger condition occurs.

**Implemented as**

- R\_ICU\_ExtrenalIrqEnable()

**Parameters**

[in]	p_ctrl	Control block set in Open call for this external interrupt.
------	--------	-------------------------------------------------------------

◆ **disable**

```
fsp_err_t(* external_irq_api_t::disable) (external_irq_ctrl_t *const p_ctrl)
```

Disable callback when external trigger condition occurs.

**Implemented as**

- R\_ICU\_ExtrenalIrqDisable()

**Parameters**

[in]	p_ctrl	Control block set in Open call for this external interrupt.
------	--------	-------------------------------------------------------------

◆ **callbackSet**

```
fsp_err_t(* external_irq_api_t::callbackSet) (external_irq_ctrl_t *const p_api_ctrl, void(
*p_callback)(external_irq_callback_args_t *), void const *const p_context,
external_irq_callback_args_t *const p_callback_memory)
```

Specify callback function and optional context pointer and working memory pointer.

**Implemented as**

- R\_ICU\_ExtrenalIrqCallbackSet()

**Parameters**

[in]	p_ctrl	Pointer to the External IRQ control block.
[in]	p_callback	Callback function
[in]	p_context	Pointer to send to callback function
[in]	p_working_memory	Pointer to volatile memory where callback structure can be allocated. Callback arguments allocated here are only valid during the callback.

◆ **close**

```
fsp_err_t(* external_irq_api_t::close) (external_irq_ctrl_t *const p_ctrl)
```

Allow driver to be reconfigured. May reduce power consumption.

**Implemented as**

- R\_ICU\_ExtrenalIrqClose()

**Parameters**

[in]	p_ctrl	Control block set in Open call for this external interrupt.
------	--------	-------------------------------------------------------------

◆ **versionGet**

```
fsp_err_t(* external_irq_api_t::versionGet) (fsp_version_t *const p_version)
```

Get version and store it in provided pointer p\_version.

**Implemented as**

- R\_ICU\_ExtrenalIrqVersionGet()

**Parameters**

[out]	p_version	Code and API version used.
-------	-----------	----------------------------

◆ **external\_irq\_instance\_t**

struct external_irq_instance_t		
This structure encompasses everything that is needed to use an instance of this interface.		
Data Fields		
external_irq_ctrl_t *	p_ctrl	Pointer to the control structure for this instance.
external_irq_cfg_t const *	p_cfg	Pointer to the configuration structure for this instance.
external_irq_api_t const *	p_api	Pointer to the API structure for this instance.

**Typedef Documentation**◆ **external\_irq\_ctrl\_t**

typedef void external_irq_ctrl_t
External IRQ control block. Allocate an instance specific control block to pass into the external IRQ API calls.
<b>Implemented as</b>
◦ <a href="#">icu_instance_ctrl_t</a>

**Enumeration Type Documentation**◆ **external\_irq\_trigger\_t**

enum external_irq_trigger_t	
Condition that will trigger an interrupt when detected.	
Enumerator	
EXTERNAL_IRQ_TRIG_FALLING	Falling edge trigger.
EXTERNAL_IRQ_TRIG_RISING	Rising edge trigger.
EXTERNAL_IRQ_TRIG_BOTH_EDGE	Both edges trigger.
EXTERNAL_IRQ_TRIG_LEVEL_LOW	Low level trigger.

◆ **external\_irq\_pclk\_div\_t**

enum <a href="#">external_irq_pclk_div_t</a>	
External IRQ input pin digital filtering sample clock divisor settings. The digital filter rejects trigger conditions that are shorter than 3 periods of the filter clock.	
Enumerator	
EXTERNAL_IRQ_PCLK_DIV_BY_1	Filter using PCLK divided by 1.
EXTERNAL_IRQ_PCLK_DIV_BY_8	Filter using PCLK divided by 8.
EXTERNAL_IRQ_PCLK_DIV_BY_32	Filter using PCLK divided by 32.
EXTERNAL_IRQ_PCLK_DIV_BY_64	Filter using PCLK divided by 64.

**4.3.16 Flash Interface**[Interfaces](#)**Detailed Description**

Interface for the Flash Memory.

**Summary**

The Flash interface provides the ability to read, write, erase, and blank check the code flash and data flash regions.

The Flash interface is implemented by:

- [Low-Power Flash Driver \(r\\_flash\\_lp\)](#)

**Data Structures**

struct [flash\\_block\\_info\\_t](#)

struct [flash\\_regions\\_t](#)

struct [flash\\_info\\_t](#)

struct [flash\\_callback\\_args\\_t](#)

struct [flash\\_cfg\\_t](#)

struct [flash\\_api\\_t](#)

```
struct flash_instance_t
```

## Typedefs

```
typedef void flash_ctrl_t
```

## Enumerations

```
enum flash_result_t
```

```
enum flash_startup_area_swap_t
```

```
enum flash_event_t
```

```
enum flash_id_code_mode_t
```

```
enum flash_status_t
```

## Data Structure Documentation

### ◆ flash\_block\_info\_t

struct flash_block_info_t		
Flash block details stored in factory flash.		
Data Fields		
uint32_t	block_section_st_addr	Starting address for this block section (blocks of this size)
uint32_t	block_section_end_addr	Ending address for this block section (blocks of this size)
uint32_t	block_size	Flash erase block size.
uint32_t	block_size_write	Flash write block size.

### ◆ flash\_regions\_t

struct flash_regions_t		
Flash block details		
Data Fields		
uint32_t	num_regions	Length of block info array.
flash_block_info_t const *	p_block_array	Block info array base address.

### ◆ flash\_info\_t

struct flash_info_t		
Information about the flash blocks		
Data Fields		



<a href="#">flash_regions_t</a>	code_flash	Information about the code flash regions.
<a href="#">flash_regions_t</a>	data_flash	Information about the code flash regions.

◆ **flash\_callback\_args\_t**

struct flash_callback_args_t		
Callback function parameter data		
Data Fields		
<a href="#">flash_event_t</a>	event	Event can be used to identify what caused the callback (flash ready or error).
void const *	p_context	Placeholder for user data. Set in <a href="#">flash_api_t::open</a> function in <a href="#">in::flash_cfg_t</a> .

◆ **flash\_cfg\_t**

struct flash_cfg_t	
FLASH Configuration	
<b>Data Fields</b>	
bool	<a href="#">data_flash_bgo</a>
	True if BGO (Background Operation) is enabled for Data Flash.
void(*)	<a href="#">p_callback</a> ( <a href="#">flash_callback_args_t</a> *p_args)
	Callback provided when a Flash interrupt ISR occurs.
void const *	<a href="#">p_extend</a>
	FLASH hardware dependent configuration.
void const *	<a href="#">p_context</a>
	Placeholder for user data. Passed to user callback in <a href="#">flash_callback_args_t</a> .
uint8_t	<a href="#">ipl</a>
	Flash ready interrupt priority.

IRQn_Type	<a href="#">irq</a>
	Flash ready interrupt number.
uint8_t	<a href="#">err_ip</a>
	Flash error interrupt priority (unused in r_flash_lp)
IRQn_Type	<a href="#">err_irq</a>
	Flash error interrupt number (unused in r_flash_lp)

◆ **flash\_api\_t**

struct flash_api_t	
Shared Interface definition for FLASH	
<b>Data Fields</b>	
<a href="#">fsp_err_t</a> (*	<a href="#">open</a> )(flash_ctrl_t *const p_ctrl, flash_cfg_t const *const p_cfg)
<a href="#">fsp_err_t</a> (*	<a href="#">write</a> )(flash_ctrl_t *const p_ctrl, uint32_t const src_address, uint32_t const flash_address, uint32_t const num_bytes)
<a href="#">fsp_err_t</a> (*	<a href="#">erase</a> )(flash_ctrl_t *const p_ctrl, uint32_t const address, uint32_t const num_blocks)
<a href="#">fsp_err_t</a> (*	<a href="#">blankCheck</a> )(flash_ctrl_t *const p_ctrl, uint32_t const address, uint32_t const num_bytes, flash_result_t *const p_blank_check_result)
<a href="#">fsp_err_t</a> (*	<a href="#">infoGet</a> )(flash_ctrl_t *const p_ctrl, flash_info_t *const p_info)
<a href="#">fsp_err_t</a> (*	<a href="#">close</a> )(flash_ctrl_t *const p_ctrl)
<a href="#">fsp_err_t</a> (*	<a href="#">statusGet</a> )(flash_ctrl_t *const p_ctrl, flash_status_t *const p_status)
<a href="#">fsp_err_t</a> (*	<a href="#">accessWindowSet</a> )(flash_ctrl_t *const p_ctrl, uint32_t const

	start_addr, uint32_t const end_addr)
fsp_err_t(*	accessWindowClear )(flash_ctrl_t *const p_ctrl)
fsp_err_t(*	idCodeSet )(flash_ctrl_t *const p_ctrl, uint8_t const *const p_id_bytes, flash_id_code_mode_t mode)
fsp_err_t(*	reset )(flash_ctrl_t *const p_ctrl)
fsp_err_t(*	updateFlashClockFreq )(flash_ctrl_t *const p_ctrl)
fsp_err_t(*	startupAreaSelect )(flash_ctrl_t *const p_ctrl, flash_startup_area_swap_t swap_type, bool is_temporary)
fsp_err_t(*	callbackSet )(flash_ctrl_t *const p_api_ctrl, void(*p_callback)(flash_callback_args_t *), void const *const p_context, flash_callback_args_t *const p_callback_memory)
fsp_err_t(*	versionGet )(fsp_version_t *p_version)

## Field Documentation

### ◆ open

fsp\_err\_t(\* flash\_api\_t::open) (flash\_ctrl\_t \*const p\_ctrl, flash\_cfg\_t const \*const p\_cfg)

Open FLASH device.

### Implemented as

- R\_FLASH\_LP\_Open()
- R\_FLASH\_HP\_Open()

### Parameters

[out]	p_ctrl	Pointer to FLASH device control. Must be declared by user. Value set here.
[in]	flash_cfg_t	Pointer to FLASH configuration structure. All elements of this structure must be set by the user.

## ◆ write

```
fsp_err_t(* flash_api_t::write) (flash_ctrl_t *const p_ctrl, uint32_t const src_address, uint32_t const flash_address, uint32_t const num_bytes)
```

Write FLASH device.

**Implemented as**

- R\_FLASH\_LP\_Write()
- R\_FLASH\_HP\_Write()

**Parameters**

[in]	p_ctrl	Control for the FLASH device context.
[in]	src_address	Address of the buffer containing the data to write to Flash.
[in]	flash_address	Code Flash or Data Flash address to write. The address must be on a programming line boundary.
[in]	num_bytes	The number of bytes to write. This number must be a multiple of the programming size. For Code Flash this is FLASH_MIN_PGM_SIZE_CF. For Data Flash this is FLASH_MIN_PGM_SIZE_DF.

**Warning**

Specifying a number that is not a multiple of the programming size will result in SF\_FLASH\_ERR\_BYTES being returned and no data written.

◆ **erase**

```
fsp_err_t(* flash_api_t::erase) (flash_ctrl_t *const p_ctrl, uint32_t const address, uint32_t const num_blocks)
```

Erase FLASH device.

**Implemented as**

- R\_FLASH\_LP\_Erase()
- R\_FLASH\_HP\_Erase()

**Parameters**

[in]	p_ctrl	Control for the FLASH device.
[in]	address	The block containing this address is the first block erased.
[in]	num_blocks	Specifies the number of blocks to be erased, the starting block determined by the block_erase_address.

## ◆ blankCheck

```
fsp_err_t(* flash_api_t::blankCheck) (flash_ctrl_t *const p_ctrl, uint32_t const address, uint32_t const num_bytes, flash_result_t *const p_blank_check_result)
```

Blank check FLASH device.

### Implemented as

- R\_FLASH\_LP\_BlankCheck()
- R\_FLASH\_HP\_BlankCheck()

### Parameters

[in]	p_ctrl	Control for the FLASH device context.
[in]	address	The starting address of the Flash area to blank check.
[in]	num_bytes	Specifies the number of bytes that need to be checked. See the specific handler for details.
[out]	p_blank_check_result	Pointer that will be populated by the API with the results of the blank check operation in non-BGO (blocking) mode. In this case the blank check operation completes here and the result is returned. In Data Flash BGO mode the blank check operation is only started here and the result obtained later when the supplied callback routine is called. In this case FLASH_RESULT_BGO_ACTIVE will be returned in p_blank_check_result.

## ◆ infoGet

```
fsp_err_t(* flash_api_t::infoGet) (flash_ctrl_t *const p_ctrl, flash_info_t *const p_info)
```

Close FLASH device.

**Implemented as**

- R\_FLASH\_LP\_InfoGet()
- R\_FLASH\_HP\_InfoGet()

**Parameters**

[in]	p_ctrl	Pointer to FLASH device control.
[out]	p_info	Pointer to FLASH info structure.

## ◆ close

```
fsp_err_t(* flash_api_t::close) (flash_ctrl_t *const p_ctrl)
```

Close FLASH device.

**Implemented as**

- R\_FLASH\_LP\_Close()
- R\_FLASH\_HP\_Close()

**Parameters**

[in]	p_ctrl	Pointer to FLASH device control.
------	--------	----------------------------------

## ◆ statusGet

```
fsp_err_t(* flash_api_t::statusGet) (flash_ctrl_t *const p_ctrl, flash_status_t *const p_status)
```

Get Status for FLASH device.

**Implemented as**

- R\_FLASH\_LP\_StatusGet()
- R\_FLASH\_HP\_StatusGet()

**Parameters**

[in]	p_ctrl	Pointer to FLASH device control.
[out]	p_status	Pointer to the current flash status.

### ◆ accessWindowSet

`fsp_err_t(* flash_api_t::accessWindowSet) (flash_ctrl_t *const p_ctrl, uint32_t const start_addr, uint32_t const end_addr)`

Set Access Window for FLASH device.

#### Implemented as

- `R_FLASH_LP_AccessWindowSet()`
- `R_FLASH_HP_AccessWindowSet()`

#### Parameters

[in]	p_ctrl	Pointer to FLASH device control.
[in]	start_addr	Determines the Starting block for the Code Flash access window.
[in]	end_addr	Determines the Ending block for the Code Flash access window. This address will not be within the access window.

### ◆ accessWindowClear

`fsp_err_t(* flash_api_t::accessWindowClear) (flash_ctrl_t *const p_ctrl)`

Clear any existing Code Flash access window for FLASH device.

#### Implemented as

- `R_FLASH_LP_AccessWindowClear()`
- `R_FLASH_HP_AccessWindowClear()`

#### Parameters

[in]	p_ctrl	Pointer to FLASH device control.
[in]	start_addr	Determines the Starting block for the Code Flash access window.
[in]	end_addr	Determines the Ending block for the Code Flash access window.



◆ **idCodeSet**

```
fsp_err_t(* flash_api_t::idCodeSet) (flash_ctrl_t *const p_ctrl, uint8_t const *const p_id_bytes,
flash_id_code_mode_t mode)
```

Set ID Code for FLASH device. Setting the ID code can restrict access to the device. The ID code will be required to connect to the device. Bits 126 and 127 are set based on the mode.

For example, `uint8_t id_bytes[] = {0x00, 0x11, 0x22, 0x33, 0x44, 0x55, 0x66, 0x77, 0x88, 0x99, 0xaa, 0xbb, 0xcc, 0xdd, 0xee, 0x00};` with mode `FLASH_ID_CODE_MODE_LOCKED_WITH_ALL_ERASE_SUPPORT` will result in an ID code of `00112233445566778899aabbccddeec0`

With mode `FLASH_ID_CODE_MODE_LOCKED`, it will result in an ID code of `00112233445566778899aabbccdee80`

**Implemented as**

- `R_FLASH_LP_IdCodeSet()`
- `R_FLASH_HP_IdCodeSet()`

**Parameters**

[in]	<code>p_ctrl</code>	Pointer to FLASH device control.
[in]	<code>p_id_bytes</code>	Ponter to the ID Code to be written.
[in]	<code>mode</code>	Mode used for checking the ID code.

◆ **reset**

```
fsp_err_t(* flash_api_t::reset) (flash_ctrl_t *const p_ctrl)
```

Reset function for FLASH device.

**Implemented as**

- `R_FLASH_LP_Reset()`
- `R_FLASH_HP_Reset()`

**Parameters**

[in]	<code>p_ctrl</code>	Pointer to FLASH device control.
------	---------------------	----------------------------------

◆ **updateFlashClockFreq**

```
fsp_err_t(* flash_api_t::updateFlashClockFreq) (flash_ctrl_t *const p_ctrl)
```

Update Flash clock frequency (FCLK) and recalculate timeout values

**Implemented as**

- R\_FLASH\_LP\_UpdateFlashClockFreq()
- R\_FLASH\_HP\_UpdateFlashClockFreq()

**Parameters**

[in]	p_ctrl	Pointer to FLASH device control.
------	--------	----------------------------------

◆ **startupAreaSelect**

```
fsp_err_t(* flash_api_t::startupAreaSelect) (flash_ctrl_t *const p_ctrl, flash_startup_area_swap_t swap_type, bool is_temporary)
```

Select which block - Default (Block 0) or Alternate (Block 1) is used as the start-up area block.

**Implemented as**

- R\_FLASH\_LP\_StartUpAreaSelect()
- R\_FLASH\_HP\_StartUpAreaSelect()

**Parameters**

[in]	p_ctrl	Pointer to FLASH device control.
[in]	swap_type	FLASH_STARTUP_AREA_BLOCK0, FLASH_STARTUP_AREA_BLOCK1 or FLASH_STARTUP_AREA_BTFLG.
[in]	is_temporary	True or false. See table below.

swap_type	is_temporary	Operation
FLASH_STARTUP_AREA_BLOCK0	false	On next reset Startup area will be Block 0.
FLASH_STARTUP_AREA_BLOCK1	true	Startup area is immediately, but temporarily switched to Block 1.
FLASH_STARTUP_AREA_BTFLG	true	Startup area is immediately, but temporarily switched to the Block determined by the Configuration BTFLG.

◆ **callbackSet**

```
fsp_err_t(* flash_api_t::callbackSet) (flash_ctrl_t*const p_api_ctrl,
void(*p_callback)(flash_callback_args_t*), void const *const p_context, flash_callback_args_t*const
p_callback_memory)
```

Specify callback function and optional context pointer and working memory pointer.

**Implemented as**

- R\_FLASH\_HP\_CallbackSet()

**Parameters**

[in]	p_ctrl	Control block set in <a href="#">flash_api_t::open</a> call for this timer.
[in]	p_callback	Callback function to register
[in]	p_context	Pointer to send to callback function
[in]	p_working_memory	Pointer to volatile memory where callback structure can be allocated. Callback arguments allocated here are only valid during the callback.

◆ **versionGet**

```
fsp_err_t(* flash_api_t::versionGet) (fsp_version_t *p_version)
```

Get Flash driver version.

**Implemented as**

- R\_FLASH\_LP\_VersionGet()
- R\_FLASH\_HP\_VersionGet()

**Parameters**

[out]	p_version	Returns version.
-------	-----------	------------------

◆ **flash\_instance\_t**

```
struct flash_instance_t
```

This structure encompasses everything that is needed to use an instance of this interface.

## Data Fields

flash_ctrl_t *	p_ctrl	Pointer to the control structure for this instance.
flash_cfg_t const *	p_cfg	Pointer to the configuration structure for this instance.

<code>flash_api_t</code> const *	<code>p_api</code>	Pointer to the API structure for this instance.
----------------------------------	--------------------	-------------------------------------------------

## Typedef Documentation

### ◆ `flash_ctrl_t`

typedef void `flash_ctrl_t`

Flash control block. Allocate an instance specific control block to pass into the flash API calls.

#### Implemented as

- `flash_lp_instance_ctrl_t`
- `flash_hp_instance_ctrl_t`

## Enumeration Type Documentation

### ◆ `flash_result_t`

enum `flash_result_t`

Result type for certain operations

Enumerator

<code>FLASH_RESULT_BLANK</code>	Return status for Blank Check Function.
<code>FLASH_RESULT_NOT_BLANK</code>	Return status for Blank Check Function.
<code>FLASH_RESULT_BGO_ACTIVE</code>	Flash is configured for BGO mode. Result is returned in callback.

### ◆ `flash_startup_area_swap_t`

enum `flash_startup_area_swap_t`

Parameter for specifying the startup area swap being requested by `startupAreaSelect()`

Enumerator

<code>FLASH_STARTUP_AREA_BTFLG</code>	Startup area will be set based on the value of the BTFLG.
<code>FLASH_STARTUP_AREA_BLOCK0</code>	Startup area will be set to Block 0.
<code>FLASH_STARTUP_AREA_BLOCK1</code>	Startup area will be set to Block 1.

◆ **flash\_event\_t**

enum flash_event_t	
Event types returned by the ISR callback when used in Data Flash BGO mode	
Enumerator	
FLASH_EVENT_ERASE_COMPLETE	Erase operation successfully completed.
FLASH_EVENT_WRITE_COMPLETE	Write operation successfully completed.
FLASH_EVENT_BLANK	Blank check operation successfully completed. Specified area is blank.
FLASH_EVENT_NOT_BLANK	Blank check operation successfully completed. Specified area is NOT blank.
FLASH_EVENT_ERR_DF_ACCESS	Data Flash operation failed. Can occur when writing an unerased section.
FLASH_EVENT_ERR_CF_ACCESS	Code Flash operation failed. Can occur when writing an unerased section.
FLASH_EVENT_ERR_CMD_LOCKED	Operation failed, FCU is in Locked state (often result of an illegal command)
FLASH_EVENT_ERR_FAILURE	Erase or Program Operation failed.
FLASH_EVENT_ERR_ONE_BIT	A 1-bit error has been corrected when reading the flash memory area by the sequencer.

◆ **flash\_id\_code\_mode\_t**

enum flash_id_code_mode_t	
ID Code Modes for writing to ID code registers	
Enumerator	
FLASH_ID_CODE_MODE_UNLOCKED	ID code is ignored.
FLASH_ID_CODE_MODE_LOCKED_WITH_ALL_ERASE_SUPPORT	ID code is checked. All erase is available.
FLASH_ID_CODE_MODE_LOCKED	ID code is checked.

### ◆ flash\_status\_t

enum flash_status_t	
Flash status	
Enumerator	
FLASH_STATUS_IDLE	The flash is idle.
FLASH_STATUS_BUSY	The flash is currently processing a command.

## 4.3.17 I2C Master Interface

### Interfaces

#### Detailed Description

Interface for I2C master communication.

## Summary

The I2C master interface provides a common API for I2C HAL drivers. The I2C master interface supports:

- Interrupt driven transmit/receive processing
- Callback function support which can return an event code

Implemented by:

- [I2C Master on IIC \(r\\_iic\\_master\)](#)

#### Data Structures

struct [i2c\\_master\\_callback\\_args\\_t](#)

struct [i2c\\_master\\_cfg\\_t](#)

struct [i2c\\_master\\_api\\_t](#)

struct [i2c\\_master\\_instance\\_t](#)

#### Typedefs

typedef void [i2c\\_master\\_ctrl\\_t](#)

#### Enumerations

enum [i2c\\_master\\_rate\\_t](#)enum [i2c\\_master\\_addr\\_mode\\_t](#)enum [i2c\\_master\\_event\\_t](#)

## Data Structure Documentation

### ◆ [i2c\\_master\\_callback\\_args\\_t](#)

struct <a href="#">i2c_master_callback_args_t</a>		
I2C callback parameter definition		
Data Fields		
void const *	<a href="#">p_context</a>	Pointer to user-provided context.
<a href="#">i2c_master_event_t</a>	<a href="#">event</a>	Event code.

### ◆ [i2c\\_master\\_cfg\\_t](#)

struct <a href="#">i2c_master_cfg_t</a>		
I2C configuration block		
<b>Data Fields</b>		
<a href="#">uint8_t</a>	<a href="#">channel</a>	
		Identifier recognizable by implementation. <a href="#">More...</a>
<a href="#">i2c_master_rate_t</a>	<a href="#">rate</a>	
		Device's maximum clock rate from enum <a href="#">i2c_rate_t</a> .
<a href="#">uint32_t</a>	<a href="#">slave</a>	
		The address of the slave device.
<a href="#">i2c_master_addr_mode_t</a>	<a href="#">addr_mode</a>	
		Indicates how slave fields should be interpreted.
<a href="#">uint8_t</a>	<a href="#">ipl</a>	
		Interrupt priority level. Same for RXI, TXI, TEI and ERI.

IRQn_Type	<a href="#">rx_irq</a>
	Receive IRQ number.
IRQn_Type	<a href="#">tx_irq</a>
	Transmit IRQ number.
IRQn_Type	<a href="#">tei_irq</a>
	Transmit end IRQ number.
IRQn_Type	<a href="#">eri_irq</a>
	Error IRQ number.
<a href="#">transfer_instance_t</a> const *	<a href="#">p_transfer_tx</a>
	DTC instance for I2C transmit. Set to NULL if unused. <a href="#">More...</a>
<a href="#">transfer_instance_t</a> const *	<a href="#">p_transfer_rx</a>
	DTC instance for I2C receive. Set to NULL if unused.
void(*)	<a href="#">p_callback</a> (i2c_master_callback_args_t *p_args)
	Pointer to callback function. <a href="#">More...</a>
void const *	<a href="#">p_context</a>
	Pointer to the user-provided context.
void const *	<a href="#">p_extend</a>
	Any configuration data needed by the hardware. <a href="#">More...</a>



## Field Documentation

### ◆ channel

uint8\_t i2c\_master\_cfg\_t::channel

Identifier recognizable by implementation.

Generic configuration

### ◆ p\_transfer\_tx

transfer\_instance\_t const\* i2c\_master\_cfg\_t::p\_transfer\_tx

DTC instance for I2C transmit. Set to NULL if unused.

DTC support

### ◆ p\_callback

void(\* i2c\_master\_cfg\_t::p\_callback) (i2c\_master\_callback\_args\_t \*p\_args)

Pointer to callback function.

Parameters to control software behavior

### ◆ p\_extend

void const\* i2c\_master\_cfg\_t::p\_extend

Any configuration data needed by the hardware.

Implementation-specific configuration

### ◆ i2c\_master\_api\_t

struct i2c\_master\_api\_t

Interface definition for I2C access as master

#### Data Fields

fsp_err_t(*)	open )(i2c_master_ctrl_t *const p_ctrl, i2c_master_cfg_t const *const p_cfg)
--------------	------------------------------------------------------------------------------

fsp_err_t(*)	read )(i2c_master_ctrl_t *const p_ctrl, uint8_t *const p_dest, uint32_t const bytes, bool const restart)
--------------	----------------------------------------------------------------------------------------------------------

fsp_err_t(*)	write )(i2c_master_ctrl_t *const p_ctrl, uint8_t *const p_src, uint32_t const bytes, bool const restart)
--------------	----------------------------------------------------------------------------------------------------------

fsp_err_t(*)	abort )(i2c_master_ctrl_t *const p_ctrl)
--------------	------------------------------------------

fsp_err_t(*)	slaveAddressSet )(i2c_master_ctrl_t *const p_ctrl, uint32_t const
--------------	-------------------------------------------------------------------

	slave, i2c_master_addr_mode_t const addr_mode)
fsp_err_t(*	callbackSet )(i2c_master_ctrl_t *const p_api_ctrl, void(*p_callback)(i2c_master_callback_args_t *), void const *const p_context, i2c_master_callback_args_t *const p_callback_memory)
fsp_err_t(*	close )(i2c_master_ctrl_t *const p_ctrl)
fsp_err_t(*	versionGet )(fsp_version_t *const p_version)

## Field Documentation

### ◆ open

fsp\_err\_t(\* i2c\_master\_api\_t::open) (i2c\_master\_ctrl\_t \*const p\_ctrl, i2c\_master\_cfg\_t const \*const p\_cfg)

Opens the I2C Master driver and initializes the hardware.

### Implemented as

- R\_IIC\_MASTER\_Open()

### Parameters

[in]	p_ctrl	Pointer to control block. Must be declared by user. Elements are set here.
[in]	p_cfg	Pointer to configuration structure.

## ◆ read

```
fsp_err_t(* i2c_master_api_t::read) (i2c_master_ctrl_t *const p_ctrl, uint8_t *const p_dest, uint32_t
const bytes, bool const restart)
```

Performs a read operation on an I2C Master device.

**Implemented as**

- R\_IIC\_MASTER\_Read()

**Parameters**

[in]	p_ctrl	Pointer to control block set in i2c_api_master_t::open call.
[in]	p_dest	Pointer to the location to store read data.
[in]	bytes	Number of bytes to read.
[in]	restart	Specify if the restart condition should be issued after reading.

## ◆ write

```
fsp_err_t(* i2c_master_api_t::write) (i2c_master_ctrl_t *const p_ctrl, uint8_t *const p_src, uint32_t
const bytes, bool const restart)
```

Performs a write operation on an I2C Master device.

**Implemented as**

- R\_IIC\_MASTER\_Write()

**Parameters**

[in]	p_ctrl	Pointer to control block set in i2c_api_master_t::open call.
[in]	p_src	Pointer to the location to get write data from.
[in]	bytes	Number of bytes to write.
[in]	restart	Specify if the restart condition should be issued after writing.

◆ **abort**

```
fsp_err_t(* i2c_master_api_t::abort) (i2c_master_ctrl_t *const p_ctrl)
```

Performs a reset of the peripheral.

**Implemented as**

- [R\\_IIC\\_MASTER\\_Abort\(\)](#)

**Parameters**

[in]	p_ctrl	Pointer to control block set in i2c_api_master_t::open call.
------	--------	--------------------------------------------------------------

◆ **slaveAddressSet**

```
fsp_err_t(* i2c_master_api_t::slaveAddressSet) (i2c_master_ctrl_t *const p_ctrl, uint32_t const slave, i2c_master_addr_mode_t const addr_mode)
```

Sets address of the slave device without reconfiguring the bus.

**Implemented as**

- [R\\_IIC\\_MASTER\\_SlaveAddressSet\(\)](#)

**Parameters**

[in]	p_ctrl	Pointer to control block set in i2c_api_master_t::open call.
[in]	slave_address	Address of the slave device.
[in]	address_mode	Addressing mode.

◆ **callbackSet**

```
fsp_err_t(* i2c_master_api_t::callbackSet) (i2c_master_ctrl_t *const p_api_ctrl,
void(*p_callback)(i2c_master_callback_args_t*), void const *const p_context,
i2c_master_callback_args_t *const p_callback_memory)
```

Specify callback function and optional context pointer and working memory pointer.

**Implemented as**

- R\_IIC\_MASTER\_CallbackSet()

**Parameters**

[in]	p_ctrl	Pointer to the IIC Master control block.
[in]	p_callback	Callback function
[in]	p_context	Pointer to send to callback function
[in]	p_working_memory	Pointer to volatile memory where callback structure can be allocated. Callback arguments allocated here are only valid during the callback.

◆ **close**

```
fsp_err_t(* i2c_master_api_t::close) (i2c_master_ctrl_t *const p_ctrl)
```

Closes the driver and releases the I2C Master device.

**Implemented as**

- R\_IIC\_MASTER\_Close()

**Parameters**

[in]	p_ctrl	Pointer to control block set in i2c_api_master_t::open call.
------	--------	--------------------------------------------------------------

◆ **versionGet**

```
fsp_err_t(* i2c_master_api_t::versionGet) (fsp_version_t *const p_version)
```

Gets version information and stores it in the provided version struct.

**Implemented as**

- R\_IIC\_MASTER\_VersionGet()

**Parameters**

[out]	p_version	Code and API version used.
-------	-----------	----------------------------

◆ **i2c\_master\_instance\_t**

struct i2c_master_instance_t		
This structure encompasses everything that is needed to use an instance of this interface.		
Data Fields		
i2c_master_ctrl_t *	p_ctrl	Pointer to the control structure for this instance.
i2c_master_cfg_t const *	p_cfg	Pointer to the configuration structure for this instance.
i2c_master_api_t const *	p_api	Pointer to the API structure for this instance.

**Typedef Documentation**◆ **i2c\_master\_ctrl\_t**

typedef void i2c_master_ctrl_t
I2C control block. Allocate an instance specific control block to pass into the I2C API calls.
<b>Implemented as</b>
◦ <a href="#">iic_master_instance_ctrl_t</a>

**Enumeration Type Documentation**◆ **i2c\_master\_rate\_t**

enum i2c_master_rate_t	
Communication speed options	
Enumerator	
I2C_MASTER_RATE_STANDARD	100 kHz
I2C_MASTER_RATE_FAST	400 kHz
I2C_MASTER_RATE_FASTPLUS	1 MHz

◆ **i2c\_master\_addr\_mode\_t**

enum i2c_master_addr_mode_t	
Addressing mode options	
Enumerator	
I2C_MASTER_ADDR_MODE_7BIT	Use 7-bit addressing mode.
I2C_MASTER_ADDR_MODE_10BIT	Use 10-bit addressing mode.

◆ **i2c\_master\_event\_t**

enum i2c_master_event_t	
Callback events	
Enumerator	
I2C_MASTER_EVENT_ABORTED	A transfer was aborted.
I2C_MASTER_EVENT_RX_COMPLETE	A receive operation was completed successfully.
I2C_MASTER_EVENT_TX_COMPLETE	A transmit operation was completed successfully.

### 4.3.18 I2C Slave Interface

#### Interfaces

#### Detailed Description

Interface for I2C slave communication.

## Summary

The I2C slave interface provides a common API for I2C HAL drivers. The I2C slave interface supports:

- Interrupt driven transmit/receive processing
- Callback function support which returns a event codes

Implemented by:

- [I2C Slave on IIC \(r\\_iic\\_slave\)](#)

## Data Structures

struct [i2c\\_slave\\_callback\\_args\\_t](#)

struct [i2c\\_slave\\_cfg\\_t](#)

struct [i2c\\_slave\\_api\\_t](#)

struct [i2c\\_slave\\_instance\\_t](#)

## Typedefs

typedef void [i2c\\_slave\\_ctrl\\_t](#)

## Enumerations

enum [i2c\\_slave\\_rate\\_t](#)

enum [i2c\\_slave\\_addr\\_mode\\_t](#)

enum [i2c\\_slave\\_event\\_t](#)

## Data Structure Documentation

### ◆ [i2c\\_slave\\_callback\\_args\\_t](#)

struct <a href="#">i2c_slave_callback_args_t</a>		
I2C callback parameter definition		
Data Fields		
void const *	<a href="#">p_context</a>	Pointer to user-provided context.
uint32_t	bytes	Number of received/transmitted bytes in buffer.
<a href="#">i2c_slave_event_t</a>	event	Event code.

### ◆ [i2c\\_slave\\_cfg\\_t](#)

struct <a href="#">i2c_slave_cfg_t</a>		
I2C configuration block		
<b>Data Fields</b>		
uint8_t	<a href="#">channel</a>	Identifier recognizable by implementation. <a href="#">More...</a>
<a href="#">i2c_slave_rate_t</a>	<a href="#">rate</a>	Device's maximum clock rate from enum <a href="#">i2c_rate_t</a> .



uint16_t	<a href="#">slave</a>
	The address of the slave device.
<a href="#">i2c_slave_addr_mode_t</a>	<a href="#">addr_mode</a>
	Indicates how slave fields should be interpreted.
bool	<a href="#">general_call_enable</a>
	Allow a General call from master.
IRQn_Type	<a href="#">rx_irq</a>
	Receive IRQ number.
IRQn_Type	<a href="#">tx_irq</a>
	Transmit IRQ number.
IRQn_Type	<a href="#">tei_irq</a>
	Transmit end IRQ number.
IRQn_Type	<a href="#">eri_irq</a>
	Error IRQ number.
uint8_t	<a href="#">ipl</a>
	Interrupt priority level.
void(*	<a href="#">p_callback</a> )(i2c_slave_callback_args_t *p_args)
	Pointer to callback function. <a href="#">More...</a>

void const *	<a href="#">p_context</a>
	Pointer to the user-provided context.
void const *	<a href="#">p_extend</a>
	Any configuration data needed by the hardware. <a href="#">More...</a>

## Field Documentation

### ◆ channel

uint8\_t i2c\_slave\_cfg\_t::channel

Identifier recognizable by implementation.

Generic configuration

### ◆ p\_callback

void(\* i2c\_slave\_cfg\_t::p\_callback) (i2c\_slave\_callback\_args\_t \*p\_args)

Pointer to callback function.

Parameters to control software behavior

### ◆ p\_extend

void const\* i2c\_slave\_cfg\_t::p\_extend

Any configuration data needed by the hardware.

Implementation-specific configuration

### ◆ i2c\_slave\_api\_t

struct i2c\_slave\_api\_t

Interface definition for I2C access as slave

#### Data Fields

fsp_err_t(*	<a href="#">open</a> )(i2c_slave_ctrl_t *const p_ctrl, i2c_slave_cfg_t const *const p_cfg)
-------------	--------------------------------------------------------------------------------------------

fsp_err_t(*	<a href="#">read</a> )(i2c_slave_ctrl_t *const p_ctrl, uint8_t *const p_dest, uint32_t const bytes)
-------------	-----------------------------------------------------------------------------------------------------

fsp_err_t(*	<a href="#">write</a> )(i2c_slave_ctrl_t *const p_ctrl, uint8_t *const p_src, uint32_t const bytes)
-------------	-----------------------------------------------------------------------------------------------------

<code>fsp_err_t(*</code>	<code>callbackSet )(i2c_slave_ctrl_t *const p_api_ctrl, void(*p_callback)(i2c_slave_callback_args_t *), void const *const p_context, i2c_slave_callback_args_t *const p_callback_memory)</code>
<code>fsp_err_t(*</code>	<code>close )(i2c_slave_ctrl_t *const p_ctrl)</code>
<code>fsp_err_t(*</code>	<code>versionGet )(fsp_version_t *const p_version)</code>

## Field Documentation

### ◆ open

`fsp_err_t(* i2c_slave_api_t::open) (i2c_slave_ctrl_t *const p_ctrl, i2c_slave_cfg_t const *const p_cfg)`

Opens the I2C Slave driver and initializes the hardware.

#### Implemented as

- `R_IIC_SLAVE_Open()`

#### Parameters

[in]	<code>p_ctrl</code>	Pointer to control block. Must be declared by user. Elements are set here.
[in]	<code>p_cfg</code>	Pointer to configuration structure.

### ◆ read

`fsp_err_t(* i2c_slave_api_t::read) (i2c_slave_ctrl_t *const p_ctrl, uint8_t *const p_dest, uint32_t const bytes)`

Performs a read operation on an I2C Slave device.

#### Implemented as

- `R_IIC_SLAVE_Read()`

#### Parameters

[in]	<code>p_ctrl</code>	Pointer to control block set in <code>i2c_slave_api_t::open</code> call.
[in]	<code>p_dest</code>	Pointer to the location to store read data.
[in]	<code>bytes</code>	Number of bytes to read.

◆ **write**

```
fsp_err_t(* i2c_slave_api_t::write) (i2c_slave_ctrl_t *const p_ctrl, uint8_t *const p_src, uint32_t const bytes)
```

Performs a write operation on an I2C Slave device.

**Implemented as**

- [R\\_IIC\\_SLAVE\\_Write\(\)](#)

**Parameters**

[in]	p_ctrl	Pointer to control block set in <a href="#">i2c_slave_api_t::open</a> call.
[in]	p_src	Pointer to the location to get write data from.
[in]	bytes	Number of bytes to write.

◆ **callbackSet**

```
fsp_err_t(* i2c_slave_api_t::callbackSet) (i2c_slave_ctrl_t *const p_api_ctrl, void(*p_callback)(i2c_slave_callback_args_t *), void const *const p_context, i2c_slave_callback_args_t *const p_callback_memory)
```

Specify callback function and optional context pointer and working memory pointer.

**Implemented as**

- [R\\_IIC\\_SLAVE\\_CallbackSet\(\)](#)

**Parameters**

[in]	p_ctrl	Pointer to the IIC Slave control block.
[in]	p_callback	Callback function
[in]	p_context	Pointer to send to callback function
[in]	p_working_memory	Pointer to volatile memory where callback structure can be allocated. Callback arguments allocated here are only valid during the callback.

◆ **close**

```
fsp_err_t(* i2c_slave_api_t::close) (i2c_slave_ctrl_t *const p_ctrl)
```

Closes the driver and releases the I2C Slave device.

**Implemented as**

- [R\\_IIC\\_SLAVE\\_Close\(\)](#)

**Parameters**

[in]	p_ctrl	Pointer to control block set in <a href="#">i2c_slave_api_t::open</a> call.
------	--------	-----------------------------------------------------------------------------

◆ **versionGet**

```
fsp_err_t(* i2c_slave_api_t::versionGet) (fsp_version_t *const p_version)
```

Gets version information and stores it in the provided version struct.

**Implemented as**

- [R\\_IIC\\_SLAVE\\_VersionGet\(\)](#)

**Parameters**

[out]	p_version	Code and API version used.
-------	-----------	----------------------------

◆ **i2c\_slave\_instance\_t**

```
struct i2c_slave_instance_t
```

This structure encompasses everything that is needed to use an instance of this interface.

## Data Fields

<a href="#">i2c_slave_ctrl_t</a> *	p_ctrl	Pointer to the control structure for this instance.
<a href="#">i2c_slave_cfg_t</a> const *	p_cfg	Pointer to the configuration structure for this instance.
<a href="#">i2c_slave_api_t</a> const *	p_api	Pointer to the API structure for this instance.

**Typedef Documentation**◆ **i2c\_slave\_ctrl\_t**

```
typedef void i2c_slave_ctrl_t
```

I2C control block. Allocate an instance specific control block to pass into the I2C API calls.

**Implemented as**

- [iic\\_slave\\_instance\\_ctrl\\_t](#)

## Enumeration Type Documentation

### ◆ i2c\_slave\_rate\_t

enum i2c_slave_rate_t	
Communication speed options	
Enumerator	
I2C_SLAVE_RATE_STANDARD	100 kHz
I2C_SLAVE_RATE_FAST	400 kHz
I2C_SLAVE_RATE_FASTPLUS	1 MHz

### ◆ i2c\_slave\_addr\_mode\_t

enum i2c_slave_addr_mode_t	
Addressing mode options	
Enumerator	
I2C_SLAVE_ADDR_MODE_7BIT	Use 7-bit addressing mode.
I2C_SLAVE_ADDR_MODE_10BIT	Use 10-bit addressing mode.

◆ **i2c\_slave\_event\_t**

enum i2c_slave_event_t	
Callback events	
Enumerator	
I2C_SLAVE_EVENT_ABORTED	A transfer was aborted.
I2C_SLAVE_EVENT_RX_COMPLETE	A receive operation was completed successfully.
I2C_SLAVE_EVENT_TX_COMPLETE	A transmit operation was completed successfully.
I2C_SLAVE_EVENT_RX_REQUEST	A read operation expected from slave. Detected a write from master.
I2C_SLAVE_EVENT_TX_REQUEST	A write operation expected from slave. Detected a read from master.
I2C_SLAVE_EVENT_RX_MORE_REQUEST	A read operation expected from slave. Master sends out more data than configured to be read in slave.
I2C_SLAVE_EVENT_TX_MORE_REQUEST	A write operation expected from slave. Master requests more data than configured to be written by slave.
I2C_SLAVE_EVENT_GENERAL_CALL	General Call address received from Master. Detected a write from master.

**4.3.19 I2S Interface**[Interfaces](#)**Detailed Description**

Interface for I2S audio communication.

**Summary**

The I2S (Inter-IC Sound) interface provides APIs and definitions for I2S audio communication.

**Known Implementations**

## Serial Sound Interface (r\_ssi)

**Data Structures**struct [i2s\\_callback\\_args\\_t](#)struct [i2s\\_status\\_t](#)struct [i2s\\_cfg\\_t](#)struct [i2s\\_api\\_t](#)struct [i2s\\_instance\\_t](#)**Typedefs**typedef void [i2s\\_ctrl\\_t](#)**Enumerations**enum [i2s\\_pcm\\_width\\_t](#)enum [i2s\\_word\\_length\\_t](#)enum [i2s\\_event\\_t](#)enum [i2s\\_mode\\_t](#)enum [i2s\\_mute\\_t](#)enum [i2s\\_ws\\_continue\\_t](#)enum [i2s\\_state\\_t](#)**Data Structure Documentation**◆ **[i2s\\_callback\\_args\\_t](#)**

struct <a href="#">i2s_callback_args_t</a>		
Callback function parameter data		
Data Fields		
void const *	<a href="#">p_context</a>	Placeholder for user data. Set in <a href="#">i2s_api_t::open</a> function in <a href="#">i2s_cfg_t</a> .
<a href="#">i2s_event_t</a>	<a href="#">event</a>	The event can be used to identify what caused the callback (overflow or error).

◆ **[i2s\\_status\\_t](#)**



struct i2s_status_t		
I2S status.		
Data Fields		
i2s_state_t	state	Current I2S state.

## ◆ i2s\_cfg\_t

struct i2s_cfg_t		
User configuration structure, used in open function		
<b>Data Fields</b>		
uint32_t	channel	
i2s_pcm_width_t	pcm_width	Audio PCM data width.
i2s_word_length_t	word_length	Audio word length, bits must be $\geq$ i2s_cfg_t::pcm_width bits.
i2s_ws_continue_t	ws_continue	Whether to continue WS transmission during idle state.
i2s_mode_t	operating_mode	Master or slave mode.
transfer_instance_t const *	p_transfer_tx	
transfer_instance_t const *	p_transfer_rx	
void(*	p_callback	(i2s_callback_args_t *p_args)
void const *	p_context	
void const *	p_extend	

	Extension parameter for hardware specific settings.
uint8_t	<a href="#">rx_ipl</a>
	Receive interrupt priority.
uint8_t	<a href="#">tx_ipl</a>
	Transmit interrupt priority.
uint8_t	<a href="#">idle_err_ipl</a>
	Idle/Error interrupt priority.
IRQn_Type	<a href="#">tx_irq</a>
	Transmit IRQ number.
IRQn_Type	<a href="#">rx_irq</a>
	Receive IRQ number.
IRQn_Type	<a href="#">int_irq</a>
	Idle/Error IRQ number.

## Field Documentation

### ◆ channel

uint32\_t i2s\_cfg\_t::channel

Select a channel corresponding to the channel number of the hardware.

### ◆ p\_transfer\_tx

transfer\_instance\_t const\* i2s\_cfg\_t::p\_transfer\_tx

To use DTC during write, link a DTC instance here. Set to NULL if unused.

◆ **p\_transfer\_rx**

<code>transfer_instance_t</code> const* <code>i2s_cfg_t::p_transfer_rx</code>
-------------------------------------------------------------------------------

To use DTC during read, link a DTC instance here. Set to NULL if unused.

◆ **p\_callback**

<code>void(* i2s_cfg_t::p_callback) (i2s_callback_args_t *p_args)</code>
--------------------------------------------------------------------------

Callback provided when an I2S ISR occurs. Set to NULL for no CPU interrupt.

◆ **p\_context**

<code>void</code> const* <code>i2s_cfg_t::p_context</code>
------------------------------------------------------------

Placeholder for user data. Passed to the user callback in `i2s_callback_args_t`.

◆ **i2s\_api\_t**

<code>struct i2s_api_t</code>
-------------------------------

I2S functions implemented at the HAL layer will follow this API.

**Data Fields**

<code>fsp_err_t(*</code>	<code>open)(i2s_ctrl_t *const p_ctrl, i2s_cfg_t const *const p_cfg)</code>
--------------------------	----------------------------------------------------------------------------

<code>fsp_err_t(*</code>	<code>stop)(i2s_ctrl_t *const p_ctrl)</code>
--------------------------	----------------------------------------------

<code>fsp_err_t(*</code>	<code>mute)(i2s_ctrl_t *const p_ctrl, i2s_mute_t const mute_enable)</code>
--------------------------	----------------------------------------------------------------------------

<code>fsp_err_t(*</code>	<code>write)(i2s_ctrl_t *const p_ctrl, void const *const p_src, uint32_t const bytes)</code>
--------------------------	----------------------------------------------------------------------------------------------

<code>fsp_err_t(*</code>	<code>read)(i2s_ctrl_t *const p_ctrl, void *const p_dest, uint32_t const bytes)</code>
--------------------------	----------------------------------------------------------------------------------------

<code>fsp_err_t(*</code>	<code>writeRead)(i2s_ctrl_t *const p_ctrl, void const *const p_src, void *const p_dest, uint32_t const bytes)</code>
--------------------------	----------------------------------------------------------------------------------------------------------------------

<code>fsp_err_t(*</code>	<code>statusGet)(i2s_ctrl_t *const p_ctrl, i2s_status_t *const p_status)</code>
--------------------------	---------------------------------------------------------------------------------

<code>fsp_err_t(*</code>	<code>close)(i2s_ctrl_t *const p_ctrl)</code>
--------------------------	-----------------------------------------------

<code>fsp_err_t(*</code>	<code>versionGet)(fsp_version_t *const p_version)</code>
--------------------------	----------------------------------------------------------

<code>fsp_err_t</code> (*	<code>callbackSet )(i2s_ctrl_t *const p_api_ctrl, void(*p_callback)(i2s_callback_args_t *), void const *const p_context, i2s_callback_args_t *const p_callback_memory)</code>
---------------------------	-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------

## Field Documentation

### ◆ open

`fsp_err_t`(\* i2s\_api\_t::open) (i2s\_ctrl\_t \*const p\_ctrl, i2s\_cfg\_t const \*const p\_cfg)

Initial configuration.

#### Implemented as

- [R\\_SSI\\_Open\(\)](#)

#### Precondition

Peripheral clocks and any required output pins should be configured prior to calling this function.

#### Note

To reconfigure after calling this function, call [i2s\\_api\\_t::close](#) first.

#### Parameters

[in]	p_ctrl	Pointer to control block. Must be declared by user. Elements set here.
[in]	p_cfg	Pointer to configuration structure. All elements of this structure must be set by user.

### ◆ stop

`fsp_err_t`(\* i2s\_api\_t::stop) (i2s\_ctrl\_t \*const p\_ctrl)

Stop communication. Communication is stopped when callback is called with I2S\_EVENT\_IDLE.

#### Implemented as

- [R\\_SSI\\_Stop\(\)](#)

#### Parameters

[in]	p_ctrl	Control block set in <a href="#">i2s_api_t::open</a> call for this instance.
------	--------	------------------------------------------------------------------------------

◆ **mute**

```
fsp_err_t(* i2s_api_t::mute) (i2s_ctrl_t *const p_ctrl, i2s_mute_t const mute_enable)
```

Enable or disable mute.

**Implemented as**

- R\_SSI\_Mute()

**Parameters**

[in]	p_ctrl	Control block set in <a href="#">i2s_api_t::open</a> call for this instance.
[in]	mute_enable	Whether to enable or disable mute.

◆ **write**

```
fsp_err_t(* i2s_api_t::write) (i2s_ctrl_t *const p_ctrl, void const *const p_src, uint32_t const bytes)
```

Write I2S data. All transmit data is queued when callback is called with I2S\_EVENT\_TX\_EMPTY. Transmission is complete when callback is called with I2S\_EVENT\_IDLE.

**Implemented as**

- R\_SSI\_Write()

**Parameters**

[in]	p_ctrl	Control block set in <a href="#">i2s_api_t::open</a> call for this instance.
[in]	p_src	Buffer of PCM samples. Must be 4 byte aligned.
[in]	bytes	Number of bytes in the buffer. Recommended requesting a multiple of 8 bytes. If not a multiple of 8, padding 0s will be added to transmission to make it a multiple of 8.

## ◆ read

```
fsp_err_t(* i2s_api_t::read) (i2s_ctrl_t *const p_ctrl, void *const p_dest, uint32_t const bytes)
```

Read I2S data. Reception is complete when callback is called with I2S\_EVENT\_RX\_EMPTY.

**Implemented as**

- R\_SSI\_Read()

**Parameters**

[in]	p_ctrl	Control block set in <a href="#">i2s_api_t::open</a> call for this instance.
[in]	p_dest	Buffer to store PCM samples. Must be 4 byte aligned.
[in]	bytes	Number of bytes in the buffer. Recommended requesting a multiple of 8 bytes. If not a multiple of 8, receive will stop at the multiple of 8 below requested bytes.

◆ **writeRead**

```
fsp_err_t(* i2s_api_t::writeRead) (i2s_ctrl_t *const p_ctrl, void const *const p_src, void *const p_dest, uint32_t const bytes)
```

Simultaneously write and read I2S data. Transmission and reception are complete when callback is called with I2S\_EVENT\_IDLE.

**Implemented as**

- [R\\_SSI\\_WriteRead\(\)](#)

**Parameters**

[in]	p_ctrl	Control block set in <a href="#">i2s_api_t::open</a> call for this instance.
[in]	p_src	Buffer of PCM samples. Must be 4 byte aligned.
[in]	p_dest	Buffer to store PCM samples. Must be 4 byte aligned.
[in]	bytes	Number of bytes in the buffers. Recommended requesting a multiple of 8 bytes. If not a multiple of 8, padding 0s will be added to transmission to make it a multiple of 8, and receive will stop at the multiple of 8 below requested bytes.

◆ **statusGet**

```
fsp_err_t(* i2s_api_t::statusGet) (i2s_ctrl_t *const p_ctrl, i2s_status_t *const p_status)
```

Get current status and store it in provided pointer p\_status.

**Implemented as**

- [R\\_SSI\\_StatusGet\(\)](#)

**Parameters**

[in]	p_ctrl	Control block set in <a href="#">i2s_api_t::open</a> call for this instance.
[out]	p_status	Current status of the driver.

◆ **close**

```
fsp_err_t(* i2s_api_t::close) (i2s_ctrl_t *const p_ctrl)
```

Allows driver to be reconfigured and may reduce power consumption.

**Implemented as**

- [R\\_SSI\\_Close\(\)](#)

**Parameters**

[in]	p_ctrl	Control block set in <a href="#">i2s_api_t::open</a> call for this instance.
------	--------	------------------------------------------------------------------------------

◆ **versionGet**

```
fsp_err_t(* i2s_api_t::versionGet) (fsp_version_t *const p_version)
```

Get version and store it in provided pointer p\_version.

**Implemented as**

- [R\\_SSI\\_VersionGet\(\)](#)

**Parameters**

[out]	p_version	Code and API version used.
-------	-----------	----------------------------

◆ **callbackSet**

```
fsp_err_t(* i2s_api_t::callbackSet) (i2s_ctrl_t *const p_api_ctrl, void(*p_callback)(i2s_callback_args_t *), void const *const p_context, i2s_callback_args_t *const p_callback_memory)
```

Specify callback function and optional context pointer and working memory pointer.

**Implemented as**

- [R\\_SSI\\_CallbackSet\(\)](#)

**Parameters**

[in]	p_ctrl	Pointer to the I2S control block.
[in]	p_callback	Callback function
[in]	p_context	Pointer to send to callback function
[in]	p_working_memory	Pointer to volatile memory where callback structure can be allocated. Callback arguments allocated here are only valid during the callback.



◆ **i2s\_instance\_t**

struct i2s_instance_t		
This structure encompasses everything that is needed to use an instance of this interface.		
Data Fields		
i2s_ctrl_t *	p_ctrl	Pointer to the control structure for this instance.
i2s_cfg_t const *	p_cfg	Pointer to the configuration structure for this instance.
i2s_api_t const *	p_api	Pointer to the API structure for this instance.

**Typedef Documentation**◆ **i2s\_ctrl\_t**

typedef void i2s_ctrl_t
I2S control block. Allocate an instance specific control block to pass into the I2S API calls.
<b>Implemented as</b>
◦ <a href="#">ssi_instance_ctrl_t</a>

**Enumeration Type Documentation**◆ **i2s\_pcm\_width\_t**

enum i2s_pcm_width_t	
Audio PCM width	
Enumerator	
I2S_PCM_WIDTH_8_BITS	Using 8-bit PCM.
I2S_PCM_WIDTH_16_BITS	Using 16-bit PCM.
I2S_PCM_WIDTH_18_BITS	Using 18-bit PCM.
I2S_PCM_WIDTH_20_BITS	Using 20-bit PCM.
I2S_PCM_WIDTH_22_BITS	Using 22-bit PCM.
I2S_PCM_WIDTH_24_BITS	Using 24-bit PCM.
I2S_PCM_WIDTH_32_BITS	Using 24-bit PCM.

◆ **i2s\_word\_length\_t**

enum i2s_word_length_t	
Audio system word length.	
Enumerator	
I2S_WORD_LENGTH_8_BITS	Using 8-bit system word length.
I2S_WORD_LENGTH_16_BITS	Using 16-bit system word length.
I2S_WORD_LENGTH_24_BITS	Using 24-bit system word length.
I2S_WORD_LENGTH_32_BITS	Using 32-bit system word length.
I2S_WORD_LENGTH_48_BITS	Using 48-bit system word length.
I2S_WORD_LENGTH_64_BITS	Using 64-bit system word length.
I2S_WORD_LENGTH_128_BITS	Using 128-bit system word length.
I2S_WORD_LENGTH_256_BITS	Using 256-bit system word length.

◆ **i2s\_event\_t**

enum i2s_event_t	
Events that can trigger a callback function	
Enumerator	
I2S_EVENT_IDLE	Communication is idle.
I2S_EVENT_TX_EMPTY	Transmit buffer is below FIFO trigger level.
I2S_EVENT_RX_FULL	Receive buffer is above FIFO trigger level.

◆ **i2s\_mode\_t**

enum <a href="#">i2s_mode_t</a>	
I2S communication mode	
Enumerator	
I2S_MODE_SLAVE	Slave mode.
I2S_MODE_MASTER	Master mode.

◆ **i2s\_mute\_t**

enum <a href="#">i2s_mute_t</a>	
Mute audio samples.	
Enumerator	
I2S_MUTE_OFF	Disable mute.
I2S_MUTE_ON	Enable mute.

◆ **i2s\_ws\_continue\_t**

enum <a href="#">i2s_ws_continue_t</a>	
Whether to continue WS (word select line) transmission during idle state.	
Enumerator	
I2S_WS_CONTINUE_ON	Enable WS continue mode.
I2S_WS_CONTINUE_OFF	Disable WS continue mode.

◆ **i2s\_state\_t**

enum <a href="#">i2s_state_t</a>	
Possible status values returned by <a href="#">i2s_api_t::statusGet</a> .	
Enumerator	
I2S_STATE_IN_USE	I2S is in use.
I2S_STATE_STOPPED	I2S is stopped.

## 4.3.20 I/O Port Interface

### Interfaces

#### Detailed Description

Interface for accessing I/O ports and configuring I/O functionality.

## Summary

The IOPort shared interface provides the ability to access the IOPorts of a device at both bit and port level. Port and pin direction can be changed.

IOPORT Interface description: [I/O Ports \(r\\_ioport\)](#)

#### Data Structures

struct [ioport\\_pin\\_cfg\\_t](#)

struct [ioport\\_cfg\\_t](#)

struct [ioport\\_api\\_t](#)

struct [ioport\\_instance\\_t](#)

#### Typedefs

typedef uint16\_t [ioport\\_size\\_t](#)  
IO port size on this device. [More...](#)

typedef void [ioport\\_ctrl\\_t](#)

#### Enumerations

enum [ioport\\_peripheral\\_t](#)

enum [ioport\\_ethernet\\_channel\\_t](#)

enum [ioport\\_ethernet\\_mode\\_t](#)

enum [ioport\\_cfg\\_options\\_t](#)

enum [ioport\\_pwpr\\_t](#)

#### Data Structure Documentation

##### ◆ [ioport\\_pin\\_cfg\\_t](#)

struct ioport_pin_cfg_t		
Pin identifier and pin PFS pin configuration value		
Data Fields		
uint32_t	pin_cfg	Pin PFS configuration - Use ioport_cfg_options_t parameters to configure.
bsp_io_port_pin_t	pin	Pin identifier.

## ◆ ioport\_cfg\_t

struct ioport_cfg_t		
Multiple pin configuration data for loading into PFS registers by R_IOPORT_Init()		
Data Fields		
uint16_t	number_of_pins	Number of pins for which there is configuration data.
ioport_pin_cfg_t const *	p_pin_cfg_data	Pin configuration data.

## ◆ ioport\_api\_t

struct ioport_api_t	
IOPort driver structure. IOPort functions implemented at the HAL layer will follow this API.	
<b>Data Fields</b>	
fsp_err_t(*)	open )(ioport_ctrl_t *const p_ctrl, const ioport_cfg_t *p_cfg)
fsp_err_t(*)	close )(ioport_ctrl_t *const p_ctrl)
fsp_err_t(*)	pinsCfg )(ioport_ctrl_t *const p_ctrl, const ioport_cfg_t *p_cfg)
fsp_err_t(*)	pinCfg )(ioport_ctrl_t *const p_ctrl, bsp_io_port_pin_t pin, uint32_t cfg)
fsp_err_t(*)	pinEventInputRead )(ioport_ctrl_t *const p_ctrl, bsp_io_port_pin_t pin, bsp_io_level_t *p_pin_event)
fsp_err_t(*)	pinEventOutputWrite )(ioport_ctrl_t *const p_ctrl, bsp_io_port_pin_t pin, bsp_io_level_t pin_value)
fsp_err_t(*)	pinEthernetModeCfg )(ioport_ctrl_t *const p_ctrl, ioport_ethernet_channel_t channel, ioport_ethernet_mode_t mode)

<code>fsp_err_t(*</code>	<code>pinRead )(ioport_ctrl_t *const p_ctrl, bsp_io_port_pin_t pin, bsp_io_level_t *p_pin_value)</code>
<code>fsp_err_t(*</code>	<code>pinWrite )(ioport_ctrl_t *const p_ctrl, bsp_io_port_pin_t pin, bsp_io_level_t level)</code>
<code>fsp_err_t(*</code>	<code>portDirectionSet )(ioport_ctrl_t *const p_ctrl, bsp_io_port_t port, ioport_size_t direction_values, ioport_size_t mask)</code>
<code>fsp_err_t(*</code>	<code>portEventInputRead )(ioport_ctrl_t *const p_ctrl, bsp_io_port_t port, ioport_size_t *p_event_data)</code>
<code>fsp_err_t(*</code>	<code>portEventOutputWrite )(ioport_ctrl_t *const p_ctrl, bsp_io_port_t port, ioport_size_t event_data, ioport_size_t mask_value)</code>
<code>fsp_err_t(*</code>	<code>portRead )(ioport_ctrl_t *const p_ctrl, bsp_io_port_t port, ioport_size_t *p_port_value)</code>
<code>fsp_err_t(*</code>	<code>portWrite )(ioport_ctrl_t *const p_ctrl, bsp_io_port_t port, ioport_size_t value, ioport_size_t mask)</code>
<code>fsp_err_t(*</code>	<code>versionGet )(fsp_version_t *p_data)</code>

## Field Documentation

### ◆ open

`fsp_err_t(* ioport_api_t::open) (ioport_ctrl_t *const p_ctrl, const ioport_cfg_t *p_cfg)`

Initialize internal driver data and initial pin configurations. Called during startup. Do not call this API during runtime. Use `ioport_api_t::pinsCfg` for runtime reconfiguration of multiple pins.

### Implemented as

- `R_IOPORT_Open()`

### Parameters

[in]	<code>p_cfg</code>	Pointer to pin configuration data array.
------	--------------------	------------------------------------------

◆ **close**

```
fsp_err_t(* ioport_api_t::close) (ioport_ctrl_t *const p_ctrl)
```

Close the API.

**Implemented as**

- R\_IOPORT\_Close()

**Parameters**

[in]	p_ctrl	Pointer to control structure.
------	--------	-------------------------------

◆ **pinsCfg**

```
fsp_err_t(* ioport_api_t::pinsCfg) (ioport_ctrl_t *const p_ctrl, const ioport_cfg_t *p_cfg)
```

Configure multiple pins.

**Implemented as**

- R\_IOPORT\_PinsCfg()

**Parameters**

[in]	p_cfg	Pointer to pin configuration data array.
------	-------	------------------------------------------

◆ **pinCfg**

```
fsp_err_t(* ioport_api_t::pinCfg) (ioport_ctrl_t *const p_ctrl, bsp_io_port_pin_t pin, uint32_t cfg)
```

Configure settings for an individual pin.

**Implemented as**

- R\_IOPORT\_PinCfg()

**Parameters**

[in]	pin	Pin to be read.
[in]	cfg	Configuration options for the pin.

◆ **pinEventInputRead**

```
fsp_err_t(* ioport_api_t::pinEventInputRead) (ioport_ctrl_t *const p_ctrl, bsp_io_port_pin_t pin,
bsp_io_level_t *p_pin_event)
```

Read the event input data of the specified pin and return the level.

**Implemented as**

- R\_IOPORT\_PinEventInputRead()

**Parameters**

[in]	pin	Pin to be read.
[in]	p_pin_event	Pointer to return the event data.

◆ **pinEventOutputWrite**

```
fsp_err_t(* ioport_api_t::pinEventOutputWrite) (ioport_ctrl_t *const p_ctrl, bsp_io_port_pin_t pin,
bsp_io_level_t pin_value)
```

Write pin event data.

**Implemented as**

- R\_IOPORT\_PinEventOutputWrite()

**Parameters**

[in]	pin	Pin event data is to be written to.
[in]	pin_value	Level to be written to pin output event.

◆ **pinEthernetModeCfg**

```
fsp_err_t(* ioport_api_t::pinEthernetModeCfg) (ioport_ctrl_t *const p_ctrl, ioport_ethernet_channel_t
channel, ioport_ethernet_mode_t mode)
```

Configure the PHY mode of the Ethernet channels.

**Implemented as**

- R\_IOPORT\_EthernetModeCfg()

**Parameters**

[in]	channel	Channel configuration will be set for.
[in]	mode	PHY mode to set the channel to.



◆ **pinRead**

```
fsp_err_t(* ioport_api_t::pinRead) (ioport_ctrl_t *const p_ctrl, bsp_io_port_pin_t pin, bsp_io_level_t *p_pin_value)
```

Read level of a pin.

**Implemented as**

- [R\\_IOPORT\\_PinRead\(\)](#)

**Parameters**

[in]	pin	Pin to be read.
[in]	p_pin_value	Pointer to return the pin level.

◆ **pinWrite**

```
fsp_err_t(* ioport_api_t::pinWrite) (ioport_ctrl_t *const p_ctrl, bsp_io_port_pin_t pin, bsp_io_level_t level)
```

Write specified level to a pin.

**Implemented as**

- [R\\_IOPORT\\_PinWrite\(\)](#)

**Parameters**

[in]	pin	Pin to be written to.
[in]	level	State to be written to the pin.

◆ **portDirectionSet**

```
fsp_err_t(* ioport_api_t::portDirectionSet) (ioport_ctrl_t *const p_ctrl, bsp_io_port_t port, ioport_size_t direction_values, ioport_size_t mask)
```

Set the direction of one or more pins on a port.

**Implemented as**

- [R\\_IOPORT\\_PortDirectionSet\(\)](#)

**Parameters**

[in]	port	Port being configured.
[in]	direction_values	Value controlling direction of pins on port (1 - output, 0 - input).
[in]	mask	Mask controlling which pins on the port are to be configured.

### ◆ portEventInputRead

```
fsp_err_t(* ioport_api_t::portEventInputRead) (ioport_ctrl_t *const p_ctrl, bsp_io_port_t port,
ioport_size_t *p_event_data)
```

Read captured event data for a port.

#### Implemented as

- R\_IOPORT\_PortEventInputRead()

#### Parameters

[in]	port	Port to be read.
[in]	p_event_data	Pointer to return the event data.

### ◆ portEventOutputWrite

```
fsp_err_t(* ioport_api_t::portEventOutputWrite) (ioport_ctrl_t *const p_ctrl, bsp_io_port_t port,
ioport_size_t event_data, ioport_size_t mask_value)
```

Write event output data for a port.

#### Implemented as

- R\_IOPORT\_PortEventOutputWrite()

#### Parameters

[in]	port	Port event data will be written to.
[in]	event_data	Data to be written as event data to specified port.
[in]	mask_value	Each bit set to 1 in the mask corresponds to that bit's value in event data. being written to port.

◆ **portRead**

```
fsp_err_t(* ioport_api_t::portRead) (ioport_ctrl_t *const p_ctrl, bsp_io_port_t port, ioport_size_t *p_port_value)
```

Read states of pins on the specified port.

**Implemented as**

- R\_IOPORT\_PortRead()

**Parameters**

[in]	port	Port to be read.
[in]	p_port_value	Pointer to return the port value.

◆ **portWrite**

```
fsp_err_t(* ioport_api_t::portWrite) (ioport_ctrl_t *const p_ctrl, bsp_io_port_t port, ioport_size_t value, ioport_size_t mask)
```

Write to multiple pins on a port.

**Implemented as**

- R\_IOPORT\_PortWrite()

**Parameters**

[in]	port	Port to be written to.
[in]	value	Value to be written to the port.
[in]	mask	Mask controlling which pins on the port are written to.

◆ **versionGet**

```
fsp_err_t(* ioport_api_t::versionGet) (fsp_version_t *p_data)
```

Return the version of the IOPort driver.

**Implemented as**

- R\_IOPORT\_VersionGet()

**Parameters**

[out]	p_data	Memory address to return version information to.
-------	--------	--------------------------------------------------

◆ **ioport\_instance\_t**

```
struct ioport_instance_t
```

This structure encompasses everything that is needed to use an instance of this interface.

Data Fields		
<a href="#">ioport_ctrl_t</a> *	p_ctrl	Pointer to the control structure for this instance.
<a href="#">ioport_cfg_t</a> const *	p_cfg	Pointer to the configuration structure for this instance.
<a href="#">ioport_api_t</a> const *	p_api	Pointer to the API structure for this instance.

## Typedef Documentation

### ◆ [ioport\\_size\\_t](#)

typedef uint16_t <a href="#">ioport_size_t</a>
IO port size on this device.
IO port type used with ports

### ◆ [ioport\\_ctrl\\_t](#)

typedef void <a href="#">ioport_ctrl_t</a>
IOPORT control block. Allocate an instance specific control block to pass into the IOPORT API calls.
<b>Implemented as</b>
<ul style="list-style-type: none"> <li>◦ <a href="#">ioport_instance_ctrl_t</a></li> </ul>

## Enumeration Type Documentation

◆ **ioport\_peripheral\_t**

enum ioport_peripheral_t	
Superset of all peripheral functions.	
Enumerator	
IOPORT_PERIPHERAL_IO	Pin will functions as an IO pin
IOPORT_PERIPHERAL_DEBUG	Pin will function as a DEBUG pin
IOPORT_PERIPHERAL_AGT	Pin will function as an AGT peripheral pin
IOPORT_PERIPHERAL_GPT0	Pin will function as a GPT peripheral pin
IOPORT_PERIPHERAL_GPT1	Pin will function as a GPT peripheral pin
IOPORT_PERIPHERAL_SCI0_2_4_6_8	Pin will function as an SCI peripheral pin
IOPORT_PERIPHERAL_SCI1_3_5_7_9	Pin will function as an SCI peripheral pin
IOPORT_PERIPHERAL_SPI	Pin will function as a SPI peripheral pin
IOPORT_PERIPHERAL_IIC	Pin will function as a IIC peripheral pin
IOPORT_PERIPHERAL_KEY	Pin will function as a KEY peripheral pin
IOPORT_PERIPHERAL_CLKOUT_COMP_RTC	Pin will function as a clock/comparator/RTC peripheral pin
IOPORT_PERIPHERAL_CAC_AD	Pin will function as a CAC/ADC peripheral pin
IOPORT_PERIPHERAL_BUS	Pin will function as a BUS peripheral pin
IOPORT_PERIPHERAL_CTSU	Pin will function as a CTSU peripheral pin
IOPORT_PERIPHERAL_LCDC	Pin will function as a segment LCD peripheral pin
IOPORT_PERIPHERAL_DALI	Pin will function as a DALI peripheral pin
IOPORT_PERIPHERAL_CAN	Pin will function as a CAN peripheral pin
IOPORT_PERIPHERAL_QSPI	Pin will function as a QSPI peripheral pin
IOPORT_PERIPHERAL_SSI	Pin will function as an SSI peripheral pin
IOPORT_PERIPHERAL_USB_FS	Pin will function as a USB full speed peripheral pin

IOPORT_PERIPHERAL_USB_HS	Pin will function as a USB high speed peripheral pin
IOPORT_PERIPHERAL_SDHI_MMC	Pin will function as an SD/MMC peripheral pin
IOPORT_PERIPHERAL_ETHER_MII	Pin will function as an Ethernet MII peripheral pin
IOPORT_PERIPHERAL_ETHER_RMII	Pin will function as an Ethernet RMMI peripheral pin
IOPORT_PERIPHERAL_PDC	Pin will function as a PDC peripheral pin
IOPORT_PERIPHERAL_LCD_GRAPHICS	Pin will function as a graphics LCD peripheral pin
IOPORT_PERIPHERAL_TRACE	Pin will function as a debug trace peripheral pin
IOPORT_PERIPHERAL_OSPI	Pin will function as a OSPI peripheral pin
IOPORT_PERIPHERAL_END	Marks end of enum - used by parameter checking

#### ◆ ioport\_ethernet\_channel\_t

enum ioport_ethernet_channel_t	
Superset of Ethernet channels.	
Enumerator	
IOPORT_ETHERNET_CHANNEL_0	Used to select Ethernet channel 0.
IOPORT_ETHERNET_CHANNEL_1	Used to select Ethernet channel 1.
IOPORT_ETHERNET_CHANNEL_END	Marks end of enum - used by parameter checking.

◆ **ioport\_ethernet\_mode\_t**

enum <code>ioport_ethernet_mode_t</code>	
Superset of Ethernet PHY modes.	
Enumerator	
<code>IOPORT_ETHERNET_MODE_RMII</code>	Ethernet PHY mode set to MII.
<code>IOPORT_ETHERNET_MODE_MII</code>	Ethernet PHY mode set to RMII.
<code>IOPORT_ETHERNET_MODE_END</code>	Marks end of enum - used by parameter checking.

◆ **ioport\_cfg\_options\_t**

enum <code>ioport_cfg_options_t</code>	
Options to configure pin functions	
Enumerator	
<code>IOPORT_CFG_PORT_DIRECTION_INPUT</code>	Sets the pin direction to input (default)
<code>IOPORT_CFG_PORT_DIRECTION_OUTPUT</code>	Sets the pin direction to output.
<code>IOPORT_CFG_PORT_OUTPUT_LOW</code>	Sets the pin level to low.
<code>IOPORT_CFG_PORT_OUTPUT_HIGH</code>	Sets the pin level to high.
<code>IOPORT_CFG_PULLUP_ENABLE</code>	Enables the pin's internal pull-up.
<code>IOPORT_CFG_PIM_TTL</code>	Enables the pin's input mode.
<code>IOPORT_CFG_NMOS_ENABLE</code>	Enables the pin's NMOS open-drain output.
<code>IOPORT_CFG_PMOS_ENABLE</code>	Enables the pin's PMOS open-drain output.
<code>IOPORT_CFG_DRIVE_MID</code>	Sets pin drive output to medium.
<code>IOPORT_CFG_DRIVE_HS_HIGH</code>	Sets pin drive output to high along with supporting high speed.
<code>IOPORT_CFG_DRIVE_MID_IIC</code>	Sets pin to drive output needed for IIC on a 20mA port.
<code>IOPORT_CFG_DRIVE_HIGH</code>	Sets pin drive output to high.
<code>IOPORT_CFG_EVENT_RISING_EDGE</code>	Sets pin event trigger to rising edge.
<code>IOPORT_CFG_EVENT_FALLING_EDGE</code>	Sets pin event trigger to falling edge.
<code>IOPORT_CFG_EVENT_BOTH_EDGES</code>	Sets pin event trigger to both edges.
<code>IOPORT_CFG_IRQ_ENABLE</code>	Sets pin as an IRQ pin.
<code>IOPORT_CFG_ANALOG_ENABLE</code>	Enables pin to operate as an analog pin.
<code>IOPORT_CFG_PERIPHERAL_PIN</code>	Enables pin to operate as a peripheral pin.



◆ **ioport\_pwpr\_t**

enum ioport_pwpr_t	
Enumerator	
IOPORT_PFS_WRITE_DISABLE	Disable PFS write access.
IOPORT_PFS_WRITE_ENABLE	Enable PFS write access.

**4.3.21 JPEG Codec Interface**[Interfaces](#)**Detailed Description**

Interface for JPEG functions.

**Data Structures**

struct [jpeg\\_encode\\_image\\_size\\_t](#)

struct [jpeg\\_callback\\_args\\_t](#)

struct [jpeg\\_cfg\\_t](#)

struct [jpeg\\_api\\_t](#)

struct [jpeg\\_instance\\_t](#)

**Macros**

#define [JPEG\\_API\\_VERSION\\_MAJOR](#)

**Typedefs**

typedef void [jpeg\\_ctrl\\_t](#)

**Enumerations**

enum [jpeg\\_color\\_space\\_t](#)

enum [jpeg\\_data\\_order\\_t](#)

enum [jpeg\\_status\\_t](#)

enum [jpeg\\_decode\\_pixel\\_format\\_t](#)

enum [jpeg\\_decode\\_subsample\\_t](#)

## Data Structure Documentation

### ◆ jpeg\_encode\_image\_size\_t

struct jpeg_encode_image_size_t		
Image parameter structure		
Data Fields		
uint16_t	horizontal_stride_pixels	Horizontal stride.
uint16_t	horizontal_resolution	Horizontal Resolution in pixels.
uint16_t	vertical_resolution	Vertical Resolution in pixels.

### ◆ jpeg\_callback\_args\_t

struct jpeg_callback_args_t		
Callback status structure		
Data Fields		
<a href="#">jpeg_status_t</a>	status	JPEG status.
uint32_t	image_size	JPEG image size.
void const *	p_context	Pointer to user-provided context.

### ◆ jpeg\_cfg\_t

struct jpeg_cfg_t		
User configuration structure, used in open function.		
<b>Data Fields</b>		
IRQn_Type	<a href="#">jedi_irq</a>	
		Data transfer interrupt IRQ number.
IRQn_Type	<a href="#">jdti_irq</a>	
		Decompression interrupt IRQ number.
uint8_t	<a href="#">jdti_ipl</a>	
		Data transfer interrupt priority.

uint8_t	<a href="#">jedi_ipl</a>
	Decompression interrupt priority.
jpeg_mode_t	<a href="#">default_mode</a>
	Mode to use at startup.
jpeg_data_order_t	<a href="#">decode_input_data_order</a>
	Input data stream byte order.
jpeg_data_order_t	<a href="#">decode_output_data_order</a>
	Output data stream byte order.
jpeg_decode_pixel_format_t	<a href="#">pixel_format</a>
	Pixel format.
uint8_t	<a href="#">alpha_value</a>
	Alpha value to be applied to decoded pixel data. Only valid for ARGB8888 format.
void(*	<a href="#">p_decode_callback</a> )(jpeg_callback_args_t *p_args)
	User-supplied callback functions.
void const *	<a href="#">p_decode_context</a>
	Placeholder for user data. Passed to user callback in <a href="#">jpeg_callback_args_t</a> .
jpeg_data_order_t	<a href="#">encode_input_data_order</a>
	Input data stream byte order.

<a href="#">jpeg_data_order_t</a>	<a href="#">encode_output_data_order</a>
	Output data stream byte order.
<a href="#">uint16_t</a>	<a href="#">dri_marker</a>
	DRI Marker setting (0 = No DRI or RST marker)
<a href="#">uint16_t</a>	<a href="#">horizontal_resolution</a>
	Horizontal resolution of input image.
<a href="#">uint16_t</a>	<a href="#">vertical_resolution</a>
	Vertical resolution of input image.
<a href="#">uint16_t</a>	<a href="#">horizontal_stride_pixels</a>
	Horizontal stride of input image.
<a href="#">uint8_t const *</a>	<a href="#">p_quant_luma_table</a>
	Luma quantization table.
<a href="#">uint8_t const *</a>	<a href="#">p_quant_chroma_table</a>
	Chroma quantization table.
<a href="#">uint8_t const *</a>	<a href="#">p_huffman_luma_ac_table</a>
	Huffman AC table for luma.
<a href="#">uint8_t const *</a>	<a href="#">p_huffman_luma_dc_table</a>
	Huffman DC table for luma.
<a href="#">uint8_t const *</a>	<a href="#">p_huffman_chroma_ac_table</a>

	Huffman AC table for chroma.
uint8_t const *	<a href="#">p_huffman_chroma_dc_table</a>
	Huffman DC table for chroma.
void(*	<a href="#">p_encode_callback</a> )(jpeg_callback_args_t *p_args)
	User-supplied callback functions.
void const *	<a href="#">p_encode_context</a>
	Placeholder for user data. Passed to user callback in <a href="#">jpeg_callback_args_t</a> .

#### ◆ jpeg\_api\_t

struct jpeg_api_t	
JPEG functions implemented at the HAL layer will follow this API.	
<b>Data Fields</b>	
fsp_err_t(*	<a href="#">open</a> )(jpeg_ctrl_t *const p_ctrl, jpeg_cfg_t const *const p_cfg)
fsp_err_t(*	<a href="#">inputBufferSet</a> )(jpeg_ctrl_t *const p_ctrl, void *p_buffer, uint32_t buffer_size)
fsp_err_t(*	<a href="#">outputBufferSet</a> )(jpeg_ctrl_t *const p_ctrl, void *p_buffer, uint32_t buffer_size)
fsp_err_t(*	<a href="#">statusGet</a> )(jpeg_ctrl_t *const p_ctrl, jpeg_status_t *const p_status)
fsp_err_t(*	<a href="#">close</a> )(jpeg_ctrl_t *const p_ctrl)
fsp_err_t(*	<a href="#">versionGet</a> )(fsp_version_t *p_version)
fsp_err_t(*	<a href="#">horizontalStrideSet</a> )(jpeg_ctrl_t *const p_ctrl, uint32_t horizontal_stride)

<code>fsp_err_t(*</code>	<code>pixelFormatGet )(jpeg_ctrl_t *const p_ctrl, jpeg_color_space_t *const p_color_space)</code>
<code>fsp_err_t(*</code>	<code>imageSubsampleSet )(jpeg_ctrl_t *const p_ctrl, jpeg_decode_subsample_t horizontal_subsample, jpeg_decode_subsample_t vertical_subsample)</code>
<code>fsp_err_t(*</code>	<code>linesDecodedGet )(jpeg_ctrl_t *const p_ctrl, uint32_t *const p_lines)</code>
<code>fsp_err_t(*</code>	<code>imageSizeGet )(jpeg_ctrl_t *const p_ctrl, uint16_t *p_horizontal_size, uint16_t *p_vertical_size)</code>
<code>fsp_err_t(*</code>	<code>imageSizeSet )(jpeg_ctrl_t *const p_ctrl, jpeg_encode_image_size_t *p_image_size)</code>
<code>fsp_err_t(*</code>	<code>modeSet )(jpeg_ctrl_t *const p_ctrl, jpeg_mode_t mode)</code>

## Field Documentation

### ◆ open

`fsp_err_t(* jpeg_api_t::open) (jpeg_ctrl_t *const p_ctrl, jpeg_cfg_t const *const p_cfg)`

Initial configuration

#### Implemented as

- `R_JPEG_Open()`

#### Precondition

none

#### Parameters

[in,out]	<code>p_ctrl</code>	Pointer to control block. Must be declared by user. Elements set here.
[in]	<code>p_cfg</code>	Pointer to configuration structure. All elements of this structure must be set by user.

### ◆ inputBufferSet

```
fsp_err_t(* jpeg_api_t::inputBufferSet) (jpeg_ctrl_t *const p_ctrl, void *p_buffer, uint32_t buffer_size)
```

Assign input data buffer to JPEG codec.

#### Implemented as

- R\_JPEG\_InputBufferSet()

#### Precondition

the JPEG codec module must have been opened properly.

#### Note

*The buffer starting address must be 8-byte aligned.*

#### Parameters

[in]	p_ctrl	Control block set in <a href="#">jpeg_api_t::open</a> call.
[in]	p_buffer	Pointer to the input buffer space
[in]	buffer_size	Size of the input buffer

### ◆ outputBufferSet

```
fsp_err_t(* jpeg_api_t::outputBufferSet) (jpeg_ctrl_t *const p_ctrl, void *p_buffer, uint32_t buffer_size)
```

Assign output buffer to JPEG codec for storing output data.

#### Implemented as

- R\_JPEG\_OutputBufferSet()

#### Precondition

The JPEG codec module must have been opened properly.

#### Note

*The buffer starting address must be 8-byte aligned. For the decoding process, the HLD driver automatically computes the number of lines of the image to decoded so the output data fits into the given space. If the supplied output buffer is not able to hold the entire frame, the application should call the Output Full Callback function so it can be notified when additional buffer space is needed.*

#### Parameters

[in]	p_ctrl	Control block set in <a href="#">jpeg_api_t::open</a> call.
[in]	p_buffer	Pointer to the output buffer space
[in]	buffer_size	Size of the output buffer

◆ **statusGet**

```
fsp_err_t(* jpeg_api_t::statusGet) (jpeg_ctrl_t *const p_ctrl, jpeg_status_t *const p_status)
```

Retrieve current status of the JPEG codec module.

**Implemented as**

- [R\\_JPEG\\_StatusGet\(\)](#)

**Precondition**

the JPEG codec module must have been opened properly.

**Parameters**

[in]	p_ctrl	Control block set in <a href="#">jpeg_api_t::open</a> call.
[out]	p_status	JPEG module status

◆ **close**

```
fsp_err_t(* jpeg_api_t::close) (jpeg_ctrl_t *const p_ctrl)
```

Cancel an outstanding operation.

**Implemented as**

- [R\\_JPEG\\_Close\(\)](#)

**Precondition**

the JPEG codec module must have been opened properly.

*Note*

*If the encoding or the decoding operation is finished without errors, the HLD driver automatically closes the device. In this case, application does not need to explicitly close the JPEG device.*

**Parameters**

[in]	p_ctrl	Control block set in <a href="#">jpeg_api_t::open</a> call.
------	--------	-------------------------------------------------------------

◆ **versionGet**

```
fsp_err_t(* jpeg_api_t::versionGet) (fsp_version_t *p_version)
```

Get version and store it in provided pointer p\_version.

**Implemented as**

- [R\\_JPEG\\_VersionGet\(\)](#)

**Parameters**

[out]	p_version	Code and API version used.
-------	-----------	----------------------------



◆ **horizontalStrideSet**

```
fsp_err_t(* jpeg_api_t::horizontalStrideSet) (jpeg_ctrl_t *const p_ctrl, uint32_t horizontal_stride)
```

Configure the horizontal stride value.

**Implemented as**

- [R\\_JPEG\\_DecodeHorizontalStrideSet\(\)](#)

**Precondition**

The JPEG codec module must have been opened properly.

**Parameters**

[in]	p_ctrl	Control block set in <a href="#">jpeg_api_t::open</a> call.
[in]	horizontal_stride	Horizontal stride value to be used for the decoded image data.
[in]	buffer_size	Size of the output buffer

◆ **pixelFormatGet**

```
fsp_err_t(* jpeg_api_t::pixelFormatGet) (jpeg_ctrl_t *const p_ctrl, jpeg_color_space_t *const p_color_space)
```

Get the input pixel format.

**Implemented as**

- [R\\_JPEG\\_DecodePixelFormatGet\(\)](#)

**Precondition**

the JPEG codec module must have been opened properly.

**Parameters**

[in]	p_ctrl	Control block set in <a href="#">jpeg_api_t::open</a> call.
[out]	p_color_space	JPEG input format.

### ◆ imageSubsampleSet

```
fsp_err_t(* jpeg_api_t::imageSubsampleSet) (jpeg_ctrl_t *const p_ctrl, jpeg_decode_subsample_t
horizontal_subsample, jpeg_decode_subsample_t vertical_subsample)
```

Configure the horizontal and vertical subsample settings.

#### Implemented as

- R\_JPEG\_DecodeImageSubsampleSet()

#### Precondition

The JPEG codec module must have been opened properly.

#### Parameters

[in]	p_ctrl	Control block set in <a href="#">jpeg_api_t::open</a> call.
[in]	horizontal_subsample	Horizontal subsample value
[in]	vertical_subsample	Vertical subsample value

### ◆ linesDecodedGet

```
fsp_err_t(* jpeg_api_t::linesDecodedGet) (jpeg_ctrl_t *const p_ctrl, uint32_t *const p_lines)
```

Return the number of lines decoded into the output buffer.

#### Implemented as

- R\_JPEG\_DecodeLinesDecodedGet()

#### Precondition

the JPEG codec module must have been opened properly.

#### Parameters

[in]	p_ctrl	Control block set in <a href="#">jpeg_api_t::open</a> call.
[out]	p_lines	Number of lines decoded

◆ **imageSizeGet**

```
fsp_err_t(* jpeg_api_t::imageSizeGet) (jpeg_ctrl_t *const p_ctrl, uint16_t *p_horizontal_size, uint16_t *p_vertical_size)
```

Retrieve image size during decoding operation.

**Implemented as**

- [R\\_JPEG\\_DecodeImageSizeGet\(\)](#)

**Precondition**

the JPEG codec module must have been opened properly.

**Note**

*If the encoding or the decoding operation is finished without errors, the HLD driver automatically closes the device. In this case, application does not need to explicitly close the JPEG device.*

**Parameters**

[in]	p_ctrl	Control block set in <a href="#">jpeg_api_t::open</a> call.
[out]	p_horizontal_size	Image horizontal size, in number of pixels.
[out]	p_vertical_size	Image vertical size, in number of pixels.

◆ **imageSizeSet**

```
fsp_err_t(* jpeg_api_t::imageSizeSet) (jpeg_ctrl_t *const p_ctrl, jpeg_encode_image_size_t *p_image_size)
```

Set image parameters to JPEG Codec

**Implemented as**

- [R\\_JPEG\\_EncodeImageSizeSet\(\)](#)

**Precondition**

The JPEG codec module must have been opened properly.

**Parameters**

[in,out]	p_ctrl	Pointer to control block. Must be declared by user. Elements set here.
[in]	p_image_size	Pointer to the RAW image parameters

◆ **modeSet**

```
fsp_err_t(* jpeg_api_t::modeSet) (jpeg_ctrl_t *const p_ctrl, jpeg_mode_t mode)
```

Switch between encode and decode mode or vice-versa.

**Implemented as**

- R\_JPEG\_ModeSet()

**Precondition**

The JPEG codec module must have been opened properly. The JPEG Codec can only perform one operation at a time and requires different configuration for encode and decode. This function facilitates easy switching between the two modes in case both are needed in an application.

**Parameters**

[in]	p_ctrl	Control block set in <a href="#">jpeg_api_t::open</a> call.
[in]	mode	Mode to switch to

◆ **jpeg\_instance\_t**

```
struct jpeg_instance_t
```

This structure encompasses everything that is needed to use an instance of this interface.

## Data Fields

<a href="#">jpeg_ctrl_t</a> *	p_ctrl	Pointer to the control structure for this instance.
<a href="#">jpeg_cfg_t</a> const *	p_cfg	Pointer to the configuration structure for this instance.
<a href="#">jpeg_api_t</a> const *	p_api	Pointer to the API structure for this instance.

**Macro Definition Documentation**◆ **JPEG\_API\_VERSION\_MAJOR**

```
#define JPEG_API_VERSION_MAJOR
```

Configuration for this module

**Typedef Documentation**

## ◆ jpeg\_ctrl\_t

typedef void jpeg\_ctrl\_t

JPEG decode control block. Allocate an instance specific control block to pass into the JPEG decode API calls.

**Implemented as**

- jpeg\_instance\_ctrl\_t

**Enumeration Type Documentation**

## ◆ jpeg\_color\_space\_t

enum jpeg\_color\_space\_t

Image color space definitions

## Enumerator

JPEG_COLOR_SPACE_YCBCR444	Color Space YCbCr 444.
JPEG_COLOR_SPACE_YCBCR422	Color Space YCbCr 422.
JPEG_COLOR_SPACE_YCBCR420	Color Space YCbCr 420.
JPEG_COLOR_SPACE_YCBCR411	Color Space YCbCr 411.

## ◆ jpeg\_data\_order\_t

enum jpeg_data_order_t	
Multi-byte Data Format	
Enumerator	
JPEG_DATA_ORDER_NORMAL	(1)(2)(3)(4)(5)(6)(7)(8) Normal byte order
JPEG_DATA_ORDER_BYTE_SWAP	(2)(1)(4)(3)(6)(5)(8)(7) Byte Swap
JPEG_DATA_ORDER_WORD_SWAP	(3)(4)(1)(2)(7)(8)(5)(6) Word Swap
JPEG_DATA_ORDER_WORD_BYTE_SWAP	(4)(3)(2)(1)(8)(7)(6)(5) Word-Byte Swap
JPEG_DATA_ORDER_LONGWORD_SWAP	(5)(6)(7)(8)(1)(2)(3)(4) Longword Swap
JPEG_DATA_ORDER_LONGWORD_BYTE_SWAP	(6)(5)(8)(7)(2)(1)(4)(3) Longword Byte Swap
JPEG_DATA_ORDER_LONGWORD_WORD_SWAP	(7)(8)(5)(6)(3)(4)(1)(2) Longword Word Swap
JPEG_DATA_ORDER_LONGWORD_WORD_BYTE_SWAP	(8)(7)(6)(5)(4)(3)(2)(1) Longword Word Byte Swap

## ◆ jpeg\_status\_t

enum jpeg_status_t	
JPEG HLD driver internal status information. The driver can simultaneously be in more than any one status at the same time. Parse the status bit-fields using the definitions in this enum to determine driver status	
Enumerator	
JPEG_STATUS_NONE	JPEG codec module is not initialized.
JPEG_STATUS_IDLE	JPEG Codec module is open but not running.
JPEG_STATUS_RUNNING	JPEG Codec is running.
JPEG_STATUS_HEADER_PROCESSING	JPEG Codec module is reading the JPEG header information.
JPEG_STATUS_INPUT_PAUSE	JPEG Codec paused waiting for more input data.
JPEG_STATUS_OUTPUT_PAUSE	JPEG Codec paused after it decoded the number of lines specified by user.
JPEG_STATUS_IMAGE_SIZE_READY	JPEG decoding operation obtained image size, and paused.
JPEG_STATUS_ERROR	JPEG Codec module encountered an error.
JPEG_STATUS_OPERATION_COMPLETE	JPEG Codec has completed the operation.

## ◆ jpeg\_decode\_pixel\_format\_t

enum jpeg_decode_pixel_format_t	
Pixel Data Format	
Enumerator	
JPEG_DECODE_PIXEL_FORMAT_ARGB8888	Pixel Data ARGB8888 format.
JPEG_DECODE_PIXEL_FORMAT_RGB565	Pixel Data RGB565 format.

### ◆ jpeg\_decode\_subsample\_t

enum jpeg_decode_subsample_t	
Data type for horizontal and vertical subsample settings. This setting applies only to the decoding operation.	
Enumerator	
JPEG_DECODE_OUTPUT_NO_SUBSAMPLE	No subsample. The image is decoded with no reduction in size.
JPEG_DECODE_OUTPUT_SUBSAMPLE_HALF	The output image size is reduced by half.
JPEG_DECODE_OUTPUT_SUBSAMPLE_ONE_QUARTER	The output image size is reduced to one-quarter.
JPEG_DECODE_OUTPUT_SUBSAMPLE_ONE_EIGHTH	The output image size is reduced to one-eighth.

## 4.3.22 Key Matrix Interface

### Interfaces

#### Detailed Description

Interface for key matrix functions.

## Summary

The KEYMATRIX interface provides standard Key Matrix functionality including event generation on a rising or falling edge for one or more channels at the same time. The generated event indicates all channels that are active in that instant via a bit mask. This allows the interface to be used with a matrix configuration or a one-to-one hardware implementation that is triggered on either a rising or a falling edge.

Implemented by:

- [Key Interrupt \(r\\_kint\)](#)

#### Data Structures

struct [keymatrix\\_callback\\_args\\_t](#)

struct [keymatrix\\_cfg\\_t](#)

struct [keymatrix\\_api\\_t](#)



```
struct keymatrix_instance_t
```

## Macros

```
#define KEYMATRIX_API_VERSION_MAJOR
KEY MATRIX API version number (Major)
```

```
#define KEYMATRIX_API_VERSION_MINOR
KEY MATRIX API version number (Minor)
```

## Typedefs

```
typedef void keymatrix_ctrl_t
```

## Enumerations

```
enum keymatrix_trigger_t
```

## Data Structure Documentation

### ◆ keymatrix\_callback\_args\_t

struct keymatrix_callback_args_t		
Callback function parameter data		
Data Fields		
void const *	p_context	Holder for user data. Set in <a href="#">keymatrix_api_t::open</a> function in <a href="#">keymatrix_cfg_t</a> .
uint32_t	channel_mask	Bit vector representing the physical hardware channel(s) that caused the interrupt.

### ◆ keymatrix\_cfg\_t

struct keymatrix_cfg_t		
User configuration structure, used in open function		
Data Fields		
uint32_t	<a href="#">channel_mask</a>	Key Input channel(s). Bit mask of channels to open.
<a href="#">keymatrix_trigger_t</a>	<a href="#">trigger</a>	Key Input trigger setting.

uint8_t	<a href="#">ipl</a>
	Interrupt priority level.
IRQn_Type	<a href="#">irq</a>
	NVIC IRQ number.
void(*	<a href="#">p_callback</a> )(keymatrix_callback_args_t *p_args)
	Callback for key interrupt ISR.
void const *	<a href="#">p_context</a>
	Holder for user data. Passed to callback in keymatrix_user_cb_data_t.
void const *	<a href="#">p_extend</a>
	Extension parameter for hardware specific settings.

◆ **keymatrix\_api\_t**

struct keymatrix_api_t	
Key Matrix driver structure. Key Matrix functions implemented at the HAL layer will use this API.	
<b>Data Fields</b>	
<a href="#">fsp_err_t</a> (*	<a href="#">open</a> )(keymatrix_ctrl_t *const p_ctrl, keymatrix_cfg_t const *const p_cfg)
<a href="#">fsp_err_t</a> (*	<a href="#">enable</a> )(keymatrix_ctrl_t *const p_ctrl)
<a href="#">fsp_err_t</a> (*	<a href="#">disable</a> )(keymatrix_ctrl_t *const p_ctrl)
<a href="#">fsp_err_t</a> (*	<a href="#">close</a> )(keymatrix_ctrl_t *const p_ctrl)
<a href="#">fsp_err_t</a> (*	<a href="#">versionGet</a> )(fsp_version_t *const p_version)

## Field Documentation

### ◆ open

`fsp_err_t(* keymatrix_api_t::open) (keymatrix_ctrl_t *const p_ctrl, keymatrix_cfg_t const *const p_cfg)`

Initial configuration.

#### Implemented as

- [R\\_KINT\\_Open\(\)](#)

#### Parameters

[out]	p_ctrl	Pointer to control block. Must be declared by user. Value set in this function.
[in]	p_cfg	Pointer to configuration structure. All elements of the structure must be set by user.

### ◆ enable

`fsp_err_t(* keymatrix_api_t::enable) (keymatrix_ctrl_t *const p_ctrl)`

Enable Key interrupt

#### Implemented as

- [R\\_KINT\\_Enable\(\)](#)

#### Parameters

[in]	p_ctrl	Control block pointer set in Open call for this Key interrupt.
------	--------	----------------------------------------------------------------

### ◆ disable

`fsp_err_t(* keymatrix_api_t::disable) (keymatrix_ctrl_t *const p_ctrl)`

Disable Key interrupt.

#### Implemented as

- [R\\_KINT\\_Disable\(\)](#)

#### Parameters

[in]	p_ctrl	Control block pointer set in Open call for this Key interrupt.
------	--------	----------------------------------------------------------------

◆ **close**

```
fsp_err_t(* keymatrix_api_t::close) (keymatrix_ctrl_t *const p_ctrl)
```

Allow driver to be reconfigured. May reduce power consumption.

**Implemented as**

- R\_KINT\_Close()

**Parameters**

[in]	p_ctrl	Control block pointer set in Open call for this Key interrupt.
------	--------	----------------------------------------------------------------

◆ **versionGet**

```
fsp_err_t(* keymatrix_api_t::versionGet) (fsp_version_t *const p_version)
```

Get version and store it in provided pointer p\_version.

**Implemented as**

- R\_KINT\_VersionGet()

**Parameters**

[out]	p_version	Code and API version used.
-------	-----------	----------------------------

◆ **keymatrix\_instance\_t**

```
struct keymatrix_instance_t
```

This structure encompasses everything that is needed to use an instance of this interface.

## Data Fields

keymatrix_ctrl_t *	p_ctrl	Pointer to the control structure for this instance.
keymatrix_cfg_t const *	p_cfg	Pointer to the configuration structure for this instance.
keymatrix_api_t const *	p_api	Pointer to the API structure for this instance.

**Typedef Documentation**

◆ **keymatrix\_ctrl\_t**typedef void [keymatrix\\_ctrl\\_t](#)

Key matrix control block. Allocate an instance specific control block to pass into the key matrix API calls.

**Implemented as**

- [kint\\_instance\\_ctrl\\_t](#)

**Enumeration Type Documentation**◆ **keymatrix\_trigger\_t**enum [keymatrix\\_trigger\\_t](#)

Trigger type: rising edge, falling edge

## Enumerator

KEYMATRIX\_TRIG\_FALLING

Falling edge trigger.

KEYMATRIX\_TRIG\_RISING

Rising edge trigger.

**4.3.23 Low Power Modes Interface**[Interfaces](#)**Detailed Description**

Interface for accessing low power modes.

**Summary**

This section defines the API for the LPM (Low Power Mode) Driver. The LPM Driver provides functions for controlling power consumption by configuring and transitioning to a low power mode. The LPM driver supports configuration of MCU low power modes using the LPM hardware peripheral. The LPM driver supports low power modes deep standby, standby, sleep, and snooze.

*Note*

*Not all low power modes are available on all MCUs.*

The LPM interface is implemented by:

- [Low Power Modes \(r\\_lpm\)](#)

**Data Structures**

struct [lpm\\_cfg\\_t](#)

struct [lpm\\_api\\_t](#)

struct [lpm\\_instance\\_t](#)

## Typedefs

typedef void [lpm\\_ctrl\\_t](#)

## Enumerations

enum [lpm\\_mode\\_t](#)

enum [lpm\\_snooze\\_request\\_t](#)

enum [lpm\\_snooze\\_end\\_t](#)

enum [lpm\\_snooze\\_cancel\\_t](#)

enum [lpm\\_snooze\\_dtc\\_t](#)

enum [lpm\\_standby\\_wake\\_source\\_t](#)

enum [lpm\\_io\\_port\\_t](#)

enum [lpm\\_power\\_supply\\_t](#)

enum [lpm\\_deep\\_standby\\_cancel\\_edge\\_t](#)

enum [lpm\\_deep\\_standby\\_cancel\\_source\\_t](#)

enum [lpm\\_output\\_port\\_enable\\_t](#)

## Data Structure Documentation

### ◆ [lpm\\_cfg\\_t](#)

struct <a href="#">lpm_cfg_t</a>		
User configuration structure, used in open function		
Data Fields		
<a href="#">lpm_mode_t</a>	low_power_mode	Low Power Mode
<a href="#">lpm_standby_wake_source_bits_t</a>	standby_wake_sources	Bitwise list of sources to wake from standby
<a href="#">lpm_snooze_request_t</a>	snooze_request_source	Snooze request source
<a href="#">lpm_snooze_end_bits_t</a>	snooze_end_sources	Bitwise list of snooze end sources

<a href="#">lpm_snooze_cancel_t</a>	snooze_cancel_sources	List of snooze cancel sources
<a href="#">lpm_snooze_dtc_t</a>	dtc_state_in_snooze	State of DTC in snooze mode, enabled or disabled
void const *	p_extend	Placeholder for extension.

### ◆ lpm\_api\_t

struct lpm_api_t	
LPM driver structure. General LPM functions implemented at the HAL layer will follow this API.	
<b>Data Fields</b>	
<a href="#">fsp_err_t</a> (*	<a href="#">open</a> )(lpm_ctrl_t *const p_api_ctrl, lpm_cfg_t const *const p_cfg)
<a href="#">fsp_err_t</a> (*	<a href="#">close</a> )(lpm_ctrl_t *const p_api_ctrl)
<a href="#">fsp_err_t</a> (*	<a href="#">lowPowerReconfigure</a> )(lpm_ctrl_t *const p_api_ctrl, lpm_cfg_t const *const p_cfg)
<a href="#">fsp_err_t</a> (*	<a href="#">lowPowerModeEnter</a> )(lpm_ctrl_t *const p_api_ctrl)
<a href="#">fsp_err_t</a> (*	<a href="#">ioKeepClear</a> )(lpm_ctrl_t *const p_api_ctrl)
<a href="#">fsp_err_t</a> (*	<a href="#">versionGet</a> )(fsp_version_t *const p_version)
<b>Field Documentation</b>	
◆ <b>open</b>	
<a href="#">fsp_err_t</a> (* lpm_api_t::open) (lpm_ctrl_t *const p_api_ctrl, lpm_cfg_t const *const p_cfg)	
Initialization function	
<b>Implemented as</b>	
<ul style="list-style-type: none"> <li>◦ R_LPM_Open()</li> </ul>	
◆ <b>close</b>	
<a href="#">fsp_err_t</a> (* lpm_api_t::close) (lpm_ctrl_t *const p_api_ctrl)	
Initialization function	
<b>Implemented as</b>	
<ul style="list-style-type: none"> <li>◦ R_LPM_Close()</li> </ul>	

◆ **lowPowerReconfigure**

```
fsp_err_t(* lpm_api_t::lowPowerReconfigure) (lpm_ctrl_t *const p_api_ctrl, lpm_cfg_t const *const p_cfg)
```

Configure a low power mode.

**Implemented as**

- [R\\_LPM\\_LowPowerReconfigure\(\)](#)

**Parameters**

[in]	p_cfg	Pointer to configuration structure. All elements of this structure must be set by user.
------	-------	-----------------------------------------------------------------------------------------

◆ **lowPowerModeEnter**

```
fsp_err_t(* lpm_api_t::lowPowerModeEnter) (lpm_ctrl_t *const p_api_ctrl)
```

Enter low power mode (sleep/standby/deep standby) using WFI macro. Function will return after waking from low power mode.

**Implemented as**

- [R\\_LPM\\_LowPowerModeEnter\(\)](#)

◆ **ioKeepClear**

```
fsp_err_t(* lpm_api_t::ioKeepClear) (lpm_ctrl_t *const p_api_ctrl)
```

Clear the IOKEEP bit after deep software standby.

- **Implemented as**
- [R\\_LPM\\_IoKeepClear\(\)](#)

◆ **versionGet**

```
fsp_err_t(* lpm_api_t::versionGet) (fsp_version_t *const p_version)
```

Get the driver version based on compile time macros.

**Implemented as**

- [R\\_LPM\\_VersionGet\(\)](#)

**Parameters**

[out]	p_version	Code and API version used.
-------	-----------	----------------------------

◆ **lpm\_instance\_t**

```
struct lpm_instance_t
```

This structure encompasses everything that is needed to use an instance of this interface.



Data Fields		
<code>lpm_ctrl_t *</code>	<code>p_ctrl</code>	Pointer to the control structure for this instance.
<code>lpm_cfg_t const *const</code>	<code>p_cfg</code>	Pointer to the configuration structure for this instance.
<code>lpm_api_t const *const</code>	<code>p_api</code>	Pointer to the API structure for this instance.

## Typedef Documentation

### ◆ `lpm_ctrl_t`

```
typedef void lpm_ctrl_t
```

LPM control block. Allocate an instance specific control block to pass into the LPM API calls.

#### Implemented as

- `lpm_instance_ctrl_t`

## Enumeration Type Documentation

### ◆ `lpm_mode_t`

```
enum lpm_mode_t
```

Low power modes

#### Enumerator

<code>LPM_MODE_SLEEP</code>	Sleep mode.
<code>LPM_MODE_STANDBY</code>	Software Standby mode.
<code>LPM_MODE_STANDBY_SNOOZE</code>	Software Standby mode with Snooze mode enabled.
<code>LPM_MODE_DEEP</code>	Deep Software Standby mode.

◆ **lpm\_snooze\_request\_t**

enum <code>lpm_snooze_request_t</code>	
Snooze request sources	
Enumerator	
<code>LPM_SNOOZE_REQUEST_RXD0_FALLING</code>	Enable RXD0 falling edge snooze request.
<code>LPM_SNOOZE_REQUEST_IRQ0</code>	Enable IRQ0 pin snooze request.
<code>LPM_SNOOZE_REQUEST_IRQ1</code>	Enable IRQ1 pin snooze request.
<code>LPM_SNOOZE_REQUEST_IRQ2</code>	Enable IRQ2 pin snooze request.
<code>LPM_SNOOZE_REQUEST_IRQ3</code>	Enable IRQ3 pin snooze request.
<code>LPM_SNOOZE_REQUEST_IRQ4</code>	Enable IRQ4 pin snooze request.
<code>LPM_SNOOZE_REQUEST_IRQ5</code>	Enable IRQ5 pin snooze request.
<code>LPM_SNOOZE_REQUEST_IRQ6</code>	Enable IRQ6 pin snooze request.
<code>LPM_SNOOZE_REQUEST_IRQ7</code>	Enable IRQ7 pin snooze request.
<code>LPM_SNOOZE_REQUEST_IRQ8</code>	Enable IRQ8 pin snooze request.
<code>LPM_SNOOZE_REQUEST_IRQ9</code>	Enable IRQ9 pin snooze request.
<code>LPM_SNOOZE_REQUEST_IRQ10</code>	Enable IRQ10 pin snooze request.
<code>LPM_SNOOZE_REQUEST_IRQ11</code>	Enable IRQ11 pin snooze request.
<code>LPM_SNOOZE_REQUEST_IRQ12</code>	Enable IRQ12 pin snooze request.
<code>LPM_SNOOZE_REQUEST_IRQ13</code>	Enable IRQ13 pin snooze request.
<code>LPM_SNOOZE_REQUEST_IRQ14</code>	Enable IRQ14 pin snooze request.
<code>LPM_SNOOZE_REQUEST_IRQ15</code>	Enable IRQ15 pin snooze request.
<code>LPM_SNOOZE_REQUEST_KEY</code>	Enable KR snooze request.
<code>LPM_SNOOZE_REQUEST_ACMPS0</code>	Enable High-speed analog comparator 0 snooze request.
<code>LPM_SNOOZE_REQUEST_RTC_ALARM</code>	Enable RTC alarm snooze request.

LPM_SNOOZE_REQUEST_RTC_PERIOD	Enable RTC period snooze request.
LPM_SNOOZE_REQUEST_AGT1_UNDERFLOW	Enable AGT1 underflow snooze request.
LPM_SNOOZE_REQUEST_AGT1_COMPARE_A	Enable AGT1 compare match A snooze request.
LPM_SNOOZE_REQUEST_AGT1_COMPARE_B	Enable AGT1 compare match B snooze request.
LPM_SNOOZE_REQUEST_AGT3_UNDERFLOW	Enable AGT3 underflow snooze request.
LPM_SNOOZE_REQUEST_AGT3_COMPARE_A	Enable AGT3 compare match A snooze request.
LPM_SNOOZE_REQUEST_AGT3_COMPARE_B	Enable AGT3 compare match B snooze request.

#### ◆ lpm\_snooze\_end\_t

enum lpm_snooze_end_t	
Snooze end control	
Enumerator	
LPM_SNOOZE_END_STANDBY_WAKE_SOURCES	Transition from Snooze to Normal mode directly.
LPM_SNOOZE_END_AGT1_UNDERFLOW	AGT1 underflow.
LPM_SNOOZE_END_DTC_TRANS_COMPLETE	Last DTC transmission completion.
LPM_SNOOZE_END_DTC_TRANS_COMPLETE_NEGATED	Not Last DTC transmission completion.
LPM_SNOOZE_END_ADC0_COMPARE_MATCH	ADC Channel 0 compare match.
LPM_SNOOZE_END_ADC0_COMPARE_MISMATCH	ADC Channel 0 compare mismatch.
LPM_SNOOZE_END_ADC1_COMPARE_MATCH	ADC 1 compare match.
LPM_SNOOZE_END_ADC1_COMPARE_MISMATCH	ADC 1 compare mismatch.
LPM_SNOOZE_END_SCI0_ADDRESS_MATCH	SCI0 address mismatch.
LPM_SNOOZE_END_AGT3_UNDERFLOW	AGT3 underflow.

◆ **lpm\_snooze\_cancel\_t**

enum <code>lpm_snooze_cancel_t</code>	
Snooze cancel control	
Enumerator	
<code>LPM_SNOOZE_CANCEL_SOURCE_NONE</code>	No snooze cancel source.
<code>LPM_SNOOZE_CANCEL_SOURCE_ADC0_WCMPPM</code>	ADC Channel 0 window compare match.
<code>LPM_SNOOZE_CANCEL_SOURCE_ADC0_WCMPUM</code>	ADC Channel 0 window compare mismatch.
<code>LPM_SNOOZE_CANCEL_SOURCE_SCI0_AM</code>	SCI0 address match event.
<code>LPM_SNOOZE_CANCEL_SOURCE_SCI0_RXI_OR_ERI</code>	SCI0 receive error.
<code>LPM_SNOOZE_CANCEL_SOURCE_DTC_COMPLETE</code>	DTC transfer completion.
<code>LPM_SNOOZE_CANCEL_SOURCE_DOC_DOPCI</code>	Data operation circuit interrupt.

◆ **lpm\_snooze\_dtc\_t**

enum <code>lpm_snooze_dtc_t</code>	
DTC Enable in Snooze Mode	
Enumerator	
<code>LPM_SNOOZE_DTC_DISABLE</code>	Disable DTC operation.
<code>LPM_SNOOZE_DTC_ENABLE</code>	Enable DTC operation.

◆ **lpm\_standby\_wake\_source\_t**

enum <code>lpm_standby_wake_source_t</code>	
Wake from standby mode sources, does not apply to sleep or deep standby modes	
Enumerator	
<code>LPM_STANDBY_WAKE_SOURCE_IRQ0</code>	IRQ0.
<code>LPM_STANDBY_WAKE_SOURCE_IRQ1</code>	IRQ1.
<code>LPM_STANDBY_WAKE_SOURCE_IRQ2</code>	IRQ2.
<code>LPM_STANDBY_WAKE_SOURCE_IRQ3</code>	IRQ3.
<code>LPM_STANDBY_WAKE_SOURCE_IRQ4</code>	IRQ4.
<code>LPM_STANDBY_WAKE_SOURCE_IRQ5</code>	IRQ5.
<code>LPM_STANDBY_WAKE_SOURCE_IRQ6</code>	IRQ6.
<code>LPM_STANDBY_WAKE_SOURCE_IRQ7</code>	IRQ7.
<code>LPM_STANDBY_WAKE_SOURCE_IRQ8</code>	IRQ8.
<code>LPM_STANDBY_WAKE_SOURCE_IRQ9</code>	IRQ9.
<code>LPM_STANDBY_WAKE_SOURCE_IRQ10</code>	IRQ10.
<code>LPM_STANDBY_WAKE_SOURCE_IRQ11</code>	IRQ11.
<code>LPM_STANDBY_WAKE_SOURCE_IRQ12</code>	IRQ12.
<code>LPM_STANDBY_WAKE_SOURCE_IRQ13</code>	IRQ13.
<code>LPM_STANDBY_WAKE_SOURCE_IRQ14</code>	IRQ14.
<code>LPM_STANDBY_WAKE_SOURCE_IRQ15</code>	IRQ15.
<code>LPM_STANDBY_WAKE_SOURCE_IWDT</code>	Independent watchdog interrupt.
<code>LPM_STANDBY_WAKE_SOURCE_KEY</code>	Key interrupt.
<code>LPM_STANDBY_WAKE_SOURCE_LVD1</code>	Low Voltage Detection 1 interrupt.
<code>LPM_STANDBY_WAKE_SOURCE_LVD2</code>	Low Voltage Detection 2 interrupt.
<code>LPM_STANDBY_WAKE_SOURCE_VBATT</code>	VBATT Monitor interrupt.

LPM_STANDBY_WAKE_SOURCE_ACMPS0	Analog Comparator High-speed 0 interrupt.
LPM_STANDBY_WAKE_SOURCE_ACMPLP0	Analog Comparator Low-speed 0 interrupt.
LPM_STANDBY_WAKE_SOURCE_RTCALM	RTC Alarm interrupt.
LPM_STANDBY_WAKE_SOURCE_RTCPRD	RTC Period interrupt.
LPM_STANDBY_WAKE_SOURCE_USBHS	USB High-speed interrupt.
LPM_STANDBY_WAKE_SOURCE_USBFS	USB Full-speed interrupt.
LPM_STANDBY_WAKE_SOURCE_AGT1UD	AGT1 underflow interrupt.
LPM_STANDBY_WAKE_SOURCE_AGT1CA	AGT1 compare match A interrupt.
LPM_STANDBY_WAKE_SOURCE_AGT1CB	AGT1 compare match B interrupt.
LPM_STANDBY_WAKE_SOURCE_IIC0	I2C 0 interrupt.
LPM_STANDBY_WAKE_SOURCE_AGT3UD	AGT3 underflow interrupt.
LPM_STANDBY_WAKE_SOURCE_AGT3CA	AGT3 compare match A interrupt.
LPM_STANDBY_WAKE_SOURCE_AGT3CB	AGT3 compare match B interrupt.

#### ◆ lpm\_io\_port\_t

enum lpm_io_port_t	
I/O port state after Deep Software Standby mode	
Enumerator	
LPM_IO_PORT_RESET	When the Deep Software Standby mode is canceled, the I/O ports are in the reset state
LPM_IO_PORT_NO_CHANGE	When the Deep Software Standby mode is canceled, the I/O ports are in the same state as in the Deep Software Standby mode

◆ **lpm\_power\_supply\_t**

enum <code>lpm_power_supply_t</code>	
Power supply control	
Enumerator	
<code>LPM_POWER_SUPPLY_DEEPCUT0</code>	Power to the standby RAM, Low-speed on-chip oscillator, AGTn, and USBFS/HS resume detecting unit is supplied in deep software standby mode
<code>LPM_POWER_SUPPLY_DEEPCUT1</code>	Power to the standby RAM, Low-speed on-chip oscillator, AGTn, and USBFS/HS resume detecting unit is not supplied in deep software standby mode
<code>LPM_POWER_SUPPLY_DEEPCUT3</code>	Power to the standby RAM, Low-speed on-chip oscillator, AGTn, and USBFS/HS resume detecting unit is not supplied in deep software standby mode. In addition, LVD is disabled and the low power function in a poweron reset circuit is enabled

◆ **lpm\_deep\_standby\_cancel\_edge\_t**

enum <code>lpm_deep_standby_cancel_edge_t</code>	
Deep Standby Interrupt Edge	
Enumerator	
<code>LPM_DEEP_STANDBY_CANCEL_SOURCE_EDGE_NONE</code>	No options for a deep standby cancel source.
<code>LPM_DEEP_STANDBY_CANCEL_SOURCE_IRQ0_RISING</code>	IRQ0-DS Pin Rising Edge.
<code>LPM_DEEP_STANDBY_CANCEL_SOURCE_IRQ0_FALLING</code>	IRQ0-DS Pin Falling Edge.
<code>LPM_DEEP_STANDBY_CANCEL_SOURCE_IRQ1_RISING</code>	IRQ1-DS Pin Rising Edge.
<code>LPM_DEEP_STANDBY_CANCEL_SOURCE_IRQ1_FALLING</code>	IRQ1-DS Pin Falling Edge.
<code>LPM_DEEP_STANDBY_CANCEL_SOURCE_IRQ2_RISING</code>	IRQ2-DS Pin Rising Edge.
<code>LPM_DEEP_STANDBY_CANCEL_SOURCE_IRQ2_FALLING</code>	IRQ2-DS Pin Falling Edge.
<code>LPM_DEEP_STANDBY_CANCEL_SOURCE_IRQ3_RISING</code>	IRQ3-DS Pin Rising Edge.

ING	
LPM_DEEP_STANDBY_CANCEL_SOURCE_IRQ3_FALLING	IRQ3-DS Pin Falling Edge.
LPM_DEEP_STANDBY_CANCEL_SOURCE_IRQ4_RISING	IRQ4-DS Pin Rising Edge.
LPM_DEEP_STANDBY_CANCEL_SOURCE_IRQ4_FALLING	IRQ4-DS Pin Falling Edge.
LPM_DEEP_STANDBY_CANCEL_SOURCE_IRQ5_RISING	IRQ5-DS Pin Rising Edge.
LPM_DEEP_STANDBY_CANCEL_SOURCE_IRQ5_FALLING	IRQ5-DS Pin Falling Edge.
LPM_DEEP_STANDBY_CANCEL_SOURCE_IRQ6_RISING	IRQ6-DS Pin Rising Edge.
LPM_DEEP_STANDBY_CANCEL_SOURCE_IRQ6_FALLING	IRQ6-DS Pin Falling Edge.
LPM_DEEP_STANDBY_CANCEL_SOURCE_IRQ7_RISING	IRQ7-DS Pin Rising Edge.
LPM_DEEP_STANDBY_CANCEL_SOURCE_IRQ7_FALLING	IRQ7-DS Pin Falling Edge.
LPM_DEEP_STANDBY_CANCEL_SOURCE_IRQ8_RISING	IRQ8-DS Pin Rising Edge.
LPM_DEEP_STANDBY_CANCEL_SOURCE_IRQ8_FALLING	IRQ8-DS Pin Falling Edge.
LPM_DEEP_STANDBY_CANCEL_SOURCE_IRQ9_RISING	IRQ9-DS Pin Rising Edge.
LPM_DEEP_STANDBY_CANCEL_SOURCE_IRQ9_FALLING	IRQ9-DS Pin Falling Edge.
LPM_DEEP_STANDBY_CANCEL_SOURCE_IRQ10_RISING	IRQ10-DS Pin Rising Edge.
LPM_DEEP_STANDBY_CANCEL_SOURCE_IRQ10_FALLING	IRQ10-DS Pin Falling Edge.
LPM_DEEP_STANDBY_CANCEL_SOURCE_IRQ11_RISING	IRQ11-DS Pin Rising Edge.
LPM_DEEP_STANDBY_CANCEL_SOURCE_IRQ11_FALLING	IRQ11-DS Pin Falling Edge.
LPM_DEEP_STANDBY_CANCEL_SOURCE_IRQ12_RISING	IRQ12-DS Pin Rising Edge.
LPM_DEEP_STANDBY_CANCEL_SOURCE_IRQ12_FALLING	IRQ12-DS Pin Falling Edge.
LPM_DEEP_STANDBY_CANCEL_SOURCE_IRQ13_RISING	IRQ13-DS Pin Rising Edge.
LPM_DEEP_STANDBY_CANCEL_SOURCE_IRQ13_FALLING	



ALLING	IRQ13-DS Pin Falling Edge.
LPM_DEEP_STANDBY_CANCEL_SOURCE_IRQ14_RISING	IRQ14-DS Pin Rising Edge.
LPM_DEEP_STANDBY_CANCEL_SOURCE_IRQ14_FALLING	IRQ14-DS Pin Falling Edge.
LPM_DEEP_STANDBY_CANCEL_SOURCE_IRQ15_RISING	IRQ14-DS Pin Rising Edge.
LPM_DEEP_STANDBY_CANCEL_SOURCE_IRQ15_FALLING	IRQ14-DS Pin Falling Edge.
LPM_DEEP_STANDBY_CANCEL_SOURCE_LVD1_RISING	LVD1 Rising Slope.
LPM_DEEP_STANDBY_CANCEL_SOURCE_LVD1_FALLING	LVD1 Falling Slope.
LPM_DEEP_STANDBY_CANCEL_SOURCE_LVD2_RISING	LVD2 Rising Slope.
LPM_DEEP_STANDBY_CANCEL_SOURCE_LVD2_FALLING	LVD2 Falling Slope.
LPM_DEEP_STANDBY_CANCEL_SOURCE_NMI_RISING	NMI Pin Rising Edge.
LPM_DEEP_STANDBY_CANCEL_SOURCE_NMI_FALLING	NMI Pin Falling Edge.

#### ◆ lpm\_deep\_standby\_cancel\_source\_t

enum lpm_deep_standby_cancel_source_t	
Deep Standby cancel sources	
Enumerator	
LPM_DEEP_STANDBY_CANCEL_SOURCE_RESET_ONLY	Cancel deep standby only by reset.
LPM_DEEP_STANDBY_CANCEL_SOURCE_IRQ0	IRQ0.
LPM_DEEP_STANDBY_CANCEL_SOURCE_IRQ1	IRQ1.
LPM_DEEP_STANDBY_CANCEL_SOURCE_IRQ2	IRQ2.
LPM_DEEP_STANDBY_CANCEL_SOURCE_IRQ3	IRQ3.
LPM_DEEP_STANDBY_CANCEL_SOURCE_IRQ4	IRQ4.
LPM_DEEP_STANDBY_CANCEL_SOURCE_IRQ5	IRQ5.
LPM_DEEP_STANDBY_CANCEL_SOURCE_IRQ6	IRQ6.

LPM_DEEP_STANDBY_CANCEL_SOURCE_IRQ7	IRQ7.
LPM_DEEP_STANDBY_CANCEL_SOURCE_IRQ8	IRQ8.
LPM_DEEP_STANDBY_CANCEL_SOURCE_IRQ9	IRQ9.
LPM_DEEP_STANDBY_CANCEL_SOURCE_IRQ10	IRQ10.
LPM_DEEP_STANDBY_CANCEL_SOURCE_IRQ11	IRQ11.
LPM_DEEP_STANDBY_CANCEL_SOURCE_IRQ12	IRQ12.
LPM_DEEP_STANDBY_CANCEL_SOURCE_IRQ13	IRQ13.
LPM_DEEP_STANDBY_CANCEL_SOURCE_IRQ14	IRQ14.
LPM_DEEP_STANDBY_CANCEL_SOURCE_IRQ15	IRQ15.
LPM_DEEP_STANDBY_CANCEL_SOURCE_LVD1	LVD1.
LPM_DEEP_STANDBY_CANCEL_SOURCE_LVD2	LVD2.
LPM_DEEP_STANDBY_CANCEL_SOURCE_RTC_INTERVAL	RTC Interval Interrupt.
LPM_DEEP_STANDBY_CANCEL_SOURCE_RTC_ALARM	RTC Alarm Interrupt.
LPM_DEEP_STANDBY_CANCEL_SOURCE_NMI	NMI.
LPM_DEEP_STANDBY_CANCEL_SOURCE_USBFS	USBFS Suspend/Resume.
LPM_DEEP_STANDBY_CANCEL_SOURCE_USBHS	USBHS Suspend/Resume.
LPM_DEEP_STANDBY_CANCEL_SOURCE_AGT1	AGT1 Underflow.

◆ **lpm\_output\_port\_enable\_t**

enum <code>lpm_output_port_enable_t</code>	
Output port enable	
Enumerator	
<code>LPM_OUTPUT_PORT_ENABLE_HIGH_IMPEDANCE</code>	0: In Software Standby Mode or Deep Software Standby Mode, the address output pins, data output pins, and other bus control signal output pins are set to the high-impedance state. In Snooze, the status of the address bus and bus control signals are same as before entering Software Standby Mode.
<code>LPM_OUTPUT_PORT_ENABLE_RETAIN</code>	1: In Software Standby Mode, the address output pins, data output pins, and other bus control signal output pins retain the output state.

**4.3.24 Low Voltage Detection Interface**[Interfaces](#)**Detailed Description**

Interface for Low Voltage Detection.

**Summary**

The LVD driver provides functions for configuring the LVD voltage monitors and detectors.

Implemented by:

- [Low Voltage Detection \(r\\_lvd\)](#)

**Data Structures**

struct [lvd\\_status\\_t](#)

struct [lvd\\_callback\\_args\\_t](#)

struct [lvd\\_cfg\\_t](#)

struct [lvd\\_api\\_t](#)

struct [lvd\\_instance\\_t](#)

## Macros

```
#define LVD_API_VERSION_MAJOR
```

## Typedefs

```
typedef void lvd_ctrl_t
```

## Enumerations

```
enum lvd_threshold_t
```

```
enum lvd_response_t
```

```
enum lvd_voltage_slope_t
```

```
enum lvd_sample_clock_t
```

```
enum lvd_negation_delay_t
```

```
enum lvd_threshold_crossing_t
```

```
enum lvd_current_state_t
```

## Data Structure Documentation

### ◆ lvd\_status\_t

struct lvd_status_t		
Current state of a voltage monitor.		
Data Fields		
<a href="#">lvd_threshold_crossing_t</a>	crossing_detected	Threshold crossing detection (latched)
<a href="#">lvd_current_state_t</a>	current_state	Instantaneous status of monitored voltage (above or below threshold)

### ◆ lvd\_callback\_args\_t

struct lvd_callback_args_t		
LVD callback parameter definition		
Data Fields		
uint32_t	monitor_number	Monitor number.
<a href="#">lvd_current_state_t</a>	current_state	Current state of the voltage monitor.
void const *	p_context	Placeholder for user data.

◆ **lvd\_cfg\_t**

struct lvd_cfg_t	
LVD configuration structure	
<b>Data Fields</b>	
uint32_t	monitor_number
lvd_threshold_t	voltage_threshold
lvd_response_t	detection_response
lvd_voltage_slope_t	voltage_slope
lvd_negation_delay_t	negation_delay
lvd_sample_clock_t	sample_clock_divisor
IRQn_Type	irq
uint8_t	monitor_ipl
void(*)	p_callback )(lvd_callback_args_t *p_args)
void const *	p_context
void const *	p_extend
<b>Field Documentation</b>	
◆ <b>monitor_number</b>	
uint32_t lvd_cfg_t::monitor_number	
Monitor number, 1, 2, ...	
◆ <b>voltage_threshold</b>	
lvd_threshold_t lvd_cfg_t::voltage_threshold	
Threshold for out of range voltage detection	

◆ **detection\_response**

```
lvd_response_t lvd_cfg_t::detection_response
```

Response on detecting a threshold crossing

◆ **voltage\_slope**

```
lvd_voltage_slope_t lvd_cfg_t::voltage_slope
```

Direction of voltage crossing that will trigger a detection (Rising Edge, Falling Edge, Both).

◆ **negation\_delay**

```
lvd_negation_delay_t lvd_cfg_t::negation_delay
```

Negation of LVD signal follows reset or voltage in range

◆ **sample\_clock\_divisor**

```
lvd_sample_clock_t lvd_cfg_t::sample_clock_divisor
```

Sample clock divider, use LVD\_SAMPLE\_CLOCK\_DISABLED to disable digital filtering

◆ **irq**

```
IRQn_Type lvd_cfg_t::irq
```

Interrupt number.

◆ **monitor\_ipl**

```
uint8_t lvd_cfg_t::monitor_ipl
```

Interrupt priority level.

◆ **p\_callback**

```
void(* lvd_cfg_t::p_callback) (lvd_callback_args_t *p_args)
```

User function to be called from interrupt

◆ **p\_context**

```
void const* lvd_cfg_t::p_context
```

Placeholder for user data. Passed to the user callback in

◆ **p\_extend**

```
void const* lvd_cfg_t::p_extend
```

Extension parameter for hardware specific settings

◆ **lvd\_api\_t**

```
struct lvd_api_t
```

LVD driver API structure. LVD driver functions implemented at the HAL layer will adhere to this API.

Data Fields	
fsp_err_t(*)	open )(lvd_ctrl_t *const p_ctrl, lvd_cfg_t const *const p_cfg)
fsp_err_t(*)	statusGet )(lvd_ctrl_t *const p_ctrl, lvd_status_t *p_lvd_status)
fsp_err_t(*)	statusClear )(lvd_ctrl_t *const p_ctrl)
fsp_err_t(*)	callbackSet )(lvd_ctrl_t *const p_api_ctrl, void(*p_callback)(lvd_callback_args_t *), void const *const p_context, lvd_callback_args_t *const p_callback_memory)
fsp_err_t(*)	close )(lvd_ctrl_t *const p_ctrl)
fsp_err_t(*)	versionGet )(fsp_version_t *const p_version)

## Field Documentation

### ◆ open

fsp\_err\_t(\* lvd\_api\_t::open) (lvd\_ctrl\_t \*const p\_ctrl, lvd\_cfg\_t const \*const p\_cfg)

Initializes a low voltage detection driver according to the passed-in configuration structure.

### Implemented as

- R\_LVD\_Open()

### Parameters

[in]	p_ctrl	Pointer to control structure for the driver instance
[in]	p_cfg	Pointer to the configuration structure for the driver instance

◆ **statusGet**

```
fsp_err_t(* lvd_api_t::statusGet) (lvd_ctrl_t *const p_ctrl, lvd_status_t *p_lvd_status)
```

Get the current state of the monitor, (threshold crossing detected, voltage currently above or below threshold). Must be used if the peripheral was initialized with `lvd_response_t` set to `LVD_RESPONSE_NONE`.

**Implemented as**

- `R_LVD_StatusGet()`

**Parameters**

[in]	p_ctrl	Pointer to the control structure for the driver instance
[in,out]	p_lvd_status	Pointer to a <code>lvd_status_t</code> structure

◆ **statusClear**

```
fsp_err_t(* lvd_api_t::statusClear) (lvd_ctrl_t *const p_ctrl)
```

Clears the latched status of the monitor. Must be used if the peripheral was initialized with `lvd_response_t` set to `LVD_RESPONSE_NONE`.

**Implemented as**

- `R_LVD_StatusClear()`

**Parameters**

[in]	p_ctrl	Pointer to the control structure for the driver instance
------	--------	----------------------------------------------------------



◆ **callbackSet**

```
fsp_err_t(* lvd_api_t::callbackSet) (lvd_ctrl_t *const p_api_ctrl, void(*p_callback)(lvd_callback_args_t *), void const *const p_context, lvd_callback_args_t *const p_callback_memory)
```

Specify callback function and optional context pointer and working memory pointer.

**Implemented as**

- R\_LVD\_CallbackSet()

**Parameters**

[in]	p_ctrl	Pointer to the LVD control block.
[in]	p_callback	Callback function
[in]	p_context	Pointer to send to callback function
[in]	p_working_memory	Pointer to volatile memory where callback structure can be allocated. Callback arguments allocated here are only valid during the callback.

◆ **close**

```
fsp_err_t(* lvd_api_t::close) (lvd_ctrl_t *const p_ctrl)
```

Disables the LVD peripheral. Closes the driver instance.

**Implemented as**

- R\_LVD\_Close()

**Parameters**

[in]	p_ctrl	Pointer to the control structure for the driver instance
------	--------	----------------------------------------------------------

◆ **versionGet**

```
fsp_err_t(* lvd_api_t::versionGet) (fsp_version_t *const p_version)
```

Returns the LVD driver version based on compile time macros.

**Implemented as**

- R\_LVD\_VersionGet()

**Parameters**

[in,out]	p_version	Pointer to version structure
----------	-----------	------------------------------

◆ **lvd\_instance\_t**

struct lvd_instance_t		
This structure encompasses everything that is needed to use an instance of this interface.		
Data Fields		
<a href="#">lvd_ctrl_t</a> *	p_ctrl	Pointer to the control structure for this instance.
<a href="#">lvd_cfg_t</a> const *	p_cfg	Pointer to the configuration structure for this interface instance.
<a href="#">lvd_api_t</a> const *	p_api	Pointer to the API structure for this interface instance.

**Macro Definition Documentation**◆ **LVD\_API\_VERSION\_MAJOR**

#define LVD_API_VERSION_MAJOR
Register definitions, common services, and error codes.

**Typedef Documentation**◆ **lvd\_ctrl\_t**

typedef void <a href="#">lvd_ctrl_t</a>
LVD control block. Allocate an instance specific control block to pass into the LVD API calls.
<b>Implemented as</b>
<ul style="list-style-type: none"> <li>◦ <a href="#">lvd_instance_ctrl_t</a></li> </ul>

**Enumeration Type Documentation**◆ **lvd\_threshold\_t**

enum <a href="#">lvd_threshold_t</a>	
Voltage detection level The thresholds supported by each MCU are in the MCU User's Manual as well as in the r_lvd module description on the stack tab of the RA project.	
Enumerator	
LVD_THRESHOLD_MONITOR_1_LEVEL_4_29V	4.29V
LVD_THRESHOLD_MONITOR_1_LEVEL_4_14V	4.14V
LVD_THRESHOLD_MONITOR_1_LEVEL_4_02V	4.02V

LVD_THRESHOLD_MONITOR_1_LEVEL_3_84V	3.84V
LVD_THRESHOLD_MONITOR_1_LEVEL_3_10V	3.10V
LVD_THRESHOLD_MONITOR_1_LEVEL_3_00V	3.00V
LVD_THRESHOLD_MONITOR_1_LEVEL_2_90V	2.90V
LVD_THRESHOLD_MONITOR_1_LEVEL_2_79V	2.79V
LVD_THRESHOLD_MONITOR_1_LEVEL_2_68V	2.68V
LVD_THRESHOLD_MONITOR_1_LEVEL_2_58V	2.58V
LVD_THRESHOLD_MONITOR_1_LEVEL_2_48V	2.48V
LVD_THRESHOLD_MONITOR_1_LEVEL_2_20V	2.20V
LVD_THRESHOLD_MONITOR_1_LEVEL_1_96V	1.96V
LVD_THRESHOLD_MONITOR_1_LEVEL_1_86V	1.86V
LVD_THRESHOLD_MONITOR_1_LEVEL_1_75V	1.75V
LVD_THRESHOLD_MONITOR_1_LEVEL_1_65V	1.65V
LVD_THRESHOLD_MONITOR_1_LEVEL_2_99V	2.99V
LVD_THRESHOLD_MONITOR_1_LEVEL_2_92V	2.92V
LVD_THRESHOLD_MONITOR_1_LEVEL_2_85V	2.85V
LVD_THRESHOLD_MONITOR_2_LEVEL_4_29V	4.29V
LVD_THRESHOLD_MONITOR_2_LEVEL_4_14V	4.14V
LVD_THRESHOLD_MONITOR_2_LEVEL_4_02V	4.02V
LVD_THRESHOLD_MONITOR_2_LEVEL_3_84V	3.84V
LVD_THRESHOLD_MONITOR_2_LEVEL_2_99V	2.99V
LVD_THRESHOLD_MONITOR_2_LEVEL_2_92V	2.92V
LVD_THRESHOLD_MONITOR_2_LEVEL_2_85V	2.85V

◆ **lvd\_response\_t**

enum <code>lvd_response_t</code>	
Response types for handling threshold crossing event.	
Enumerator	
<code>LVD_RESPONSE_NMI</code>	Non-maskable interrupt.
<code>LVD_RESPONSE_INTERRUPT</code>	Maskable interrupt.
<code>LVD_RESPONSE_RESET</code>	Reset.
<code>LVD_RESPONSE_NONE</code>	No response, status must be requested via <code>statusGet</code> function.

◆ **lvd\_voltage\_slope\_t**

enum <code>lvd_voltage_slope_t</code>	
The direction from which Vcc must cross the threshold to trigger a detection (rising, falling, or both).	
Enumerator	
<code>LVD_VOLTAGE_SLOPE_RISING</code>	When $VCC \geq V_{det2}$ (rise) is detected.
<code>LVD_VOLTAGE_SLOPE_FALLING</code>	When $VCC < V_{det2}$ (drop) is detected.
<code>LVD_VOLTAGE_SLOPE_BOTH</code>	When drop and rise are detected.

◆ **lvd\_sample\_clock\_t**

enum <code>lvd_sample_clock_t</code>	
Sample clock divider, use <code>LVD_SAMPLE_CLOCK_DISABLED</code> to disable digital filtering	
Enumerator	
<code>LVD_SAMPLE_CLOCK_LOCO_DIV_2</code>	Digital filter sample clock is LOCO divided by 2.
<code>LVD_SAMPLE_CLOCK_LOCO_DIV_4</code>	Digital filter sample clock is LOCO divided by 4.
<code>LVD_SAMPLE_CLOCK_LOCO_DIV_8</code>	Digital filter sample clock is LOCO divided by 8.
<code>LVD_SAMPLE_CLOCK_LOCO_DIV_16</code>	Digital filter sample clock is LOCO divided by 16.
<code>LVD_SAMPLE_CLOCK_DISABLED</code>	Digital filter is disabled.

◆ **lvd\_negation\_delay\_t**

enum <code>lvd_negation_delay_t</code>	
Negation delay of LVD reset signal follows reset or voltage in range	
Enumerator	
<code>LVD_NEGATION_DELAY_FROM_VOLTAGE</code>	Negation follows a stabilization time ( $t_{LVDn}$ ) after $VCC > V_{det1}$ is detected. If a transition to software standby or deep software standby is to be made, the only possible value for the RN bit is <code>LVD_NEGATION_DELAY_FROM_VOLTAGE</code>
<code>LVD_NEGATION_DELAY_FROM_RESET</code>	Negation follows a stabilization time ( $t_{LVDn}$ ) after assertion of the LVDn reset. If a transition to software standby or deep software standby is to be made, the only possible value for the RN bit is <code>LVD_NEGATION_DELAY_FROM_VOLTAGE</code>

◆ **lvd\_threshold\_crossing\_t**

enum <code>lvd_threshold_crossing_t</code>	
Threshold crossing detection (latched)	
Enumerator	
<code>LVD_THRESHOLD_CROSSING_NOT_DETECTED</code>	Threshold crossing has not been detected.
<code>LVD_THRESHOLD_CROSSING_DETECTED</code>	Threshold crossing has been detected.

◆ **lvd\_current\_state\_t**

enum <code>lvd_current_state_t</code>	
Instantaneous status of VCC (above or below threshold)	
Enumerator	
<code>LVD_CURRENT_STATE_BELOW_THRESHOLD</code>	$VCC < \text{threshold}$ .
<code>LVD_CURRENT_STATE_ABOVE_THRESHOLD</code>	$VCC \geq \text{threshold}$ or monitor is disabled.

**4.3.25 OPAMP Interface**

## Interfaces

## Detailed Description

Interface for Operational Amplifiers.

## Summary

The OPAMP interface provides standard operational amplifier functionality, including starting and stopping the amplifier.

Implemented by: [Operational Amplifier \(r\\_opamp\)](#)

### Data Structures

struct [opamp\\_trim\\_args\\_t](#)

struct [opamp\\_info\\_t](#)

struct [opamp\\_status\\_t](#)

struct [opamp\\_cfg\\_t](#)

struct [opamp\\_api\\_t](#)

struct [opamp\\_instance\\_t](#)

### Macros

#define [OPAMP\\_API\\_VERSION\\_MAJOR](#)

### Typedefs

typedef void [opamp\\_ctrl\\_t](#)

### Enumerations

enum [opamp\\_trim\\_cmd\\_t](#)

enum [opamp\\_trim\\_input\\_t](#)

## Data Structure Documentation

### ◆ [opamp\\_trim\\_args\\_t](#)

struct <a href="#">opamp_trim_args_t</a>		
OPAMP trim arguments.		
Data Fields		
<a href="#">uint8_t</a>	channel	Channel.
<a href="#">opamp_trim_input_t</a>	input	Which input of the channel

above.

◆ **opamp\_info\_t**

struct opamp_info_t		
OPAMP information.		
Data Fields		
uint32_t	min_stabilization_wait_us	Minimum stabilization wait time in microseconds.

◆ **opamp\_status\_t**

struct opamp_status_t		
OPAMP status.		
Data Fields		
uint32_t	operating_channel_mask	Bitmask of channels currently operating.

◆ **opamp\_cfg\_t**

struct opamp_cfg_t		
OPAMP general configuration.		
Data Fields		
void const *	p_extend	Extension parameter for hardware specific settings.

◆ **opamp\_api\_t**

struct opamp_api_t		
OPAMP functions implemented at the HAL layer will follow this API.		
<b>Data Fields</b>		
fsp_err_t(*)	open )(opamp_ctrl_t *const p_ctrl, opamp_cfg_t const *const p_cfg)	
fsp_err_t(*)	start )(opamp_ctrl_t *const p_ctrl, uint32_t const channel_mask)	
fsp_err_t(*)	stop )(opamp_ctrl_t *const p_ctrl, uint32_t const channel_mask)	
fsp_err_t(*)	trim )(opamp_ctrl_t *const p_ctrl, opamp_trim_cmd_t const cmd, opamp_trim_args_t const *const p_args)	
fsp_err_t(*)	infoGet )(opamp_ctrl_t *const p_ctrl, opamp_info_t *const p_info)	

fsp_err_t(*	statusGet )(opamp_ctrl_t *const p_ctrl, opamp_status_t *const p_status)
-------------	-------------------------------------------------------------------------

fsp_err_t(*	close )(opamp_ctrl_t *const p_ctrl)
-------------	-------------------------------------

fsp_err_t(*	versionGet )(fsp_version_t *const p_version)
-------------	----------------------------------------------

## Field Documentation

### ◆ open

fsp_err_t(* opamp_api_t::open) (opamp_ctrl_t *const p_ctrl, opamp_cfg_t const *const p_cfg)
---------------------------------------------------------------------------------------------

Initialize the operational amplifier.

#### Implemented as

- R\_OPAMP\_Open()

#### Parameters

[in]	p_ctrl	Pointer to instance control block
[in]	p_cfg	Pointer to configuration

### ◆ start

fsp_err_t(* opamp_api_t::start) (opamp_ctrl_t *const p_ctrl, uint32_t const channel_mask)
-------------------------------------------------------------------------------------------

Start the op-amp(s).

#### Implemented as

- R\_OPAMP\_Start()

#### Parameters

[in]	p_ctrl	Pointer to instance control block
[in]	channel_mask	Bitmask of channels to start



## ◆ stop

```
fsp_err_t(* opamp_api_t::stop) (opamp_ctrl_t *const p_ctrl, uint32_t const channel_mask)
```

Stop the op-amp(s).

**Implemented as**

- R\_OPAMP\_Stop()

**Parameters**

[in]	p_ctrl	Pointer to instance control block
[in]	channel_mask	Bitmask of channels to stop

## ◆ trim

```
fsp_err_t(* opamp_api_t::trim) (opamp_ctrl_t *const p_ctrl, opamp_trim_cmd_t const cmd, opamp_trim_args_t const *const p_args)
```

Trim the op-amp(s). Not supported on all MCUs. See implementation for procedure details.

**Implemented as**

- R\_OPAMP\_Trim()

**Parameters**

[in]	p_ctrl	Pointer to instance control block
[in]	cmd	Trim command
[in]	p_args	Pointer to arguments for the command

## ◆ infoGet

```
fsp_err_t(* opamp_api_t::infoGet) (opamp_ctrl_t *const p_ctrl, opamp_info_t *const p_info)
```

Provide information such as the recommended minimum stabilization wait time.

**Implemented as**

- R\_OPAMP\_InfoGet()

**Parameters**

[in]	p_ctrl	Pointer to instance control block
[out]	p_info	OPAMP information stored here

◆ **statusGet**

```
fsp_err_t(* opamp_api_t::statusGet) (opamp_ctrl_t *const p_ctrl, opamp_status_t *const p_status)
```

Provide status of each op-amp channel.

**Implemented as**

- [R\\_OPAMP\\_StatusGet\(\)](#)

**Parameters**

[in]	p_ctrl	Pointer to instance control block
[out]	p_status	Status stored here

◆ **close**

```
fsp_err_t(* opamp_api_t::close) (opamp_ctrl_t *const p_ctrl)
```

Close the specified OPAMP unit by ending any scan in progress, disabling interrupts, and removing power to the specified A/D unit.

**Implemented as**

- [R\\_OPAMP\\_Close\(\)](#)

**Parameters**

[in]	p_ctrl	Pointer to instance control block
------	--------	-----------------------------------

◆ **versionGet**

```
fsp_err_t(* opamp_api_t::versionGet) (fsp_version_t *const p_version)
```

Retrieve the API version.

**Implemented as**

- [R\\_OPAMP\\_VersionGet\(\)](#)

**Precondition**

This function retrieves the API version.

**Parameters**

[in]	p_version	Pointer to version structure
------	-----------	------------------------------

◆ **opamp\_instance\_t**

```
struct opamp_instance_t
```

This structure encompasses everything that is needed to use an instance of this interface.

## Data Fields

opamp_ctrl_t *	p_ctrl	Pointer to the control structure for this instance.
----------------	--------	-----------------------------------------------------

<code>opamp_cfg_t</code> const *	<code>p_cfg</code>	Pointer to the configuration structure for this instance.
<code>opamp_api_t</code> const *	<code>p_api</code>	Pointer to the API structure for this instance.

## Macro Definition Documentation

### ◆ OPAMP\_API\_VERSION\_MAJOR

<code>#define OPAMP_API_VERSION_MAJOR</code>
Includes board and MCU related header files. Version Number of API.

## Typedef Documentation

### ◆ opamp\_ctrl\_t

<code>typedef void opamp_ctrl_t</code>
OPAMP control block. Allocate using driver instance control structure from driver instance header file.

## Enumeration Type Documentation

### ◆ opamp\_trim\_cmd\_t

<code>enum opamp_trim_cmd_t</code>	
Trim command.	
Enumerator	
<code>OPAMP_TRIM_CMD_START</code>	Initialize trim state machine.
<code>OPAMP_TRIM_CMD_NEXT_STEP</code>	Move to next step in state machine.
<code>OPAMP_TRIM_CMD_CLEAR_BIT</code>	Clear trim bit.

◆ **opamp\_trim\_input\_t**

enum <code>opamp_trim_input_t</code>	
Trim input.	
Enumerator	
<code>OPAMP_TRIM_INPUT_PCH</code>	Trim non-inverting (+) input.
<code>OPAMP_TRIM_INPUT_NCH</code>	Trim inverting (-) input.

**4.3.26 PDC Interface**[Interfaces](#)**Detailed Description**

Interface for PDC functions.

**Summary**

The PDC interface provides the functionality for capturing an image from an image sensor/camera. When a capture is complete a transfer complete interrupt is triggered.

Implemented by:

- [Parallel Data Capture \(r\\_pdc\)](#)

**Data Structures**

struct [pdc\\_callback\\_args\\_t](#)

struct [pdc\\_cfg\\_t](#)

struct [pdc\\_api\\_t](#)

struct [pdc\\_instance\\_t](#)

**Typedefs**

typedef void [pdc\\_ctrl\\_t](#)

**Enumerations**

enum [pdc\\_clock\\_division\\_t](#)

enum [pdc\\_endian\\_t](#)

enum [pdc\\_hsync\\_polarity\\_t](#)enum [pdc\\_vsync\\_polarity\\_t](#)enum [pdc\\_event\\_t](#)

## Data Structure Documentation

### ◆ pdc\_callback\_args\_t

struct pdc_callback_args_t		
Callback function parameter data		
Data Fields		
<a href="#">pdc_event_t</a>	event	Event causing the callback.
uint8_t *	p_buffer	Pointer to buffer containing the captured data.
void const *	p_context	Placeholder for user data. Set in <a href="#">pdc_api_t::open</a> function in <a href="#">pdc_cfg_t</a> .

### ◆ pdc\_cfg\_t

struct pdc_cfg_t		
PDC configuration parameters.		
Data Fields		
uint16_t	<a href="#">x_capture_start_pixel</a>	Horizontal position to start capture.
uint16_t	<a href="#">x_capture_pixels</a>	Number of horizontal pixels to capture.
uint16_t	<a href="#">y_capture_start_pixel</a>	Vertical position to start capture.
uint16_t	<a href="#">y_capture_pixels</a>	Number of vertical lines/pixels to capture.

<a href="#">pdc_clock_division_t</a>	<a href="#">clock_division</a>
	Clock divider.
<a href="#">pdc_endian_t</a>	<a href="#">endian</a>
	Endian of capture data.
<a href="#">pdc_hsync_polarity_t</a>	<a href="#">hsync_polarity</a>
	Polarity of HSYNC input.
<a href="#">pdc_vsync_polarity_t</a>	<a href="#">vsync_polarity</a>
	Polarity of VSYNC input.
<a href="#">uint8_t *</a>	<a href="#">p_buffer</a>
	Pointer to buffer to write image into.
<a href="#">uint8_t</a>	<a href="#">bytes_per_pixel</a>
	Number of bytes per pixel.
<a href="#">uint8_t</a>	<a href="#">pdc_ipl</a>
	PDC interrupt priority.
<a href="#">uint8_t</a>	<a href="#">transfer_req_ipl</a>
	Transfer interrupt priority.
<a href="#">IRQn_Type</a>	<a href="#">pdc_irq</a>
	PDC IRQ number.
<a href="#">IRQn_Type</a>	<a href="#">transfer_req_irq</a>

	Transfer request IRQ number.
<code>transfer_instance_t</code> const *	<code>p_lower_lvl_transfer</code>
	Pointer to the transfer instance the PDC should use.
<code>void</code> (* <code>p_callback</code> )( <code>pdc_callback_args_t</code> * <code>p_args</code> )	
	Callback provided when a PDC transfer ISR occurs.
<code>void</code> const *	<code>p_context</code>
	User defined context passed to callback function.
<code>void</code> const *	<code>p_extend</code>
	Placeholder for user data.

#### ◆ pdc\_api\_t

struct pdc_api_t	
PDC functions implemented at the HAL layer will follow this API.	
<b>Data Fields</b>	
<code>fsp_err_t</code> (* <code>open</code> )( <code>pdc_ctrl_t</code> *const <code>p_ctrl</code> , <code>pdc_cfg_t</code> const *const <code>p_cfg</code> )	
<code>fsp_err_t</code> (* <code>close</code> )( <code>pdc_ctrl_t</code> *const <code>p_ctrl</code> )	
<code>fsp_err_t</code> (* <code>captureStart</code> )( <code>pdc_ctrl_t</code> *const <code>p_ctrl</code> , <code>uint8_t</code> *const <code>p_buffer</code> )	
<code>fsp_err_t</code> (* <code>versionGet</code> )( <code>fsp_version_t</code> *const <code>p_data</code> )	
<b>Field Documentation</b>	

◆ **open**

```
fsp_err_t(* pdc_api_t::open) (pdc_ctrl_t *const p_ctrl, pdc_cfg_t const *const p_cfg)
```

Initial configuration.

**Implemented as**

- R\_PDC\_Open()

*Note*

To reconfigure after calling this function, call `pdc_api_t::close` first.

**Parameters**

[in]	p_ctrl	Pointer to control structure.
[in]	p_cfg	Pointer to pin configuration structure.

◆ **close**

```
fsp_err_t(* pdc_api_t::close) (pdc_ctrl_t *const p_ctrl)
```

Closes the driver and allows reconfiguration. May reduce power consumption.

**Implemented as**

- R\_PDC\_Close()

**Parameters**

[in]	p_ctrl	Pointer to control structure.
------	--------	-------------------------------

◆ **captureStart**

```
fsp_err_t(* pdc_api_t::captureStart) (pdc_ctrl_t *const p_ctrl, uint8_t *const p_buffer)
```

Start a capture.

**Implemented as**

- R\_PDC\_CaptureStart()

**Parameters**

[in]	p_ctrl	Pointer to control structure.
[in]	p_buffer	Pointer to store captured image data.



◆ **versionGet**

```
fsp_err_t(* pdc_api_t::versionGet) (fsp_version_t *const p_data)
```

Return the version of the driver.

**Implemented as**

- R\_PDC\_VersionGet()

**Parameters**

[in]	p_ctrl	Pointer to control structure.
[out]	p_data	Memory address to return version information to.

◆ **pd\_c\_instance\_t**

```
struct pd_c_instance_t
```

This structure encompasses everything that is needed to use an instance of this interface.

## Data Fields

pd_c_ctrl_t *	p_ctrl	Pointer to the control structure for this instance.
pd_c_cfg_t const *	p_cfg	Pointer to the configuration structure for this instance.
pd_c_api_t const *	p_api	Pointer to the API structure for this instance.

**Typedef Documentation**◆ **pd\_c\_ctrl\_t**

```
typedef void pd_c_ctrl_t
```

PDC control block. Allocate an instance specific control block to pass into the PDC API calls.

**Implemented as**

- pd\_c\_instance\_ctrl\_t

**Enumeration Type Documentation**

◆ **pdc\_clock\_division\_t**

enum <code>pdc_clock_division_t</code>	
Clock divider applied to PDC clock to provide PCKO output frequency	
Enumerator	
<code>PDC_CLOCK_DIVISION_2</code>	CLK / 2.
<code>PDC_CLOCK_DIVISION_4</code>	CLK / 4.
<code>PDC_CLOCK_DIVISION_6</code>	CLK / 6.
<code>PDC_CLOCK_DIVISION_8</code>	CLK / 8.
<code>PDC_CLOCK_DIVISION_10</code>	CLK / 10.
<code>PDC_CLOCK_DIVISION_12</code>	CLK / 12.
<code>PDC_CLOCK_DIVISION_14</code>	CLK / 14.
<code>PDC_CLOCK_DIVISION_16</code>	CLK / 16.

◆ **pdc\_endian\_t**

enum <code>pdc_endian_t</code>	
Endian of captured data	
Enumerator	
<code>PDC_ENDIAN_LITTLE</code>	Data is in little endian format.
<code>PDC_ENDIAN_BIG</code>	Data is in big endian format.

◆ **pdc\_hsync\_polarity\_t**

enum <code>pdc_hsync_polarity_t</code>	
Polarity of input HSYNC signal	
Enumerator	
<code>PDC_HSYNC_POLARITY_HIGH</code>	HSYNC signal is active high.
<code>PDC_HSYNC_POLARITY_LOW</code>	HSYNC signal is active low.

◆ **pdc\_vsync\_polarity\_t**

enum <code>pdc_vsync_polarity_t</code>	
Polarity of input VSYNC signal	
Enumerator	
<code>PDC_VSYNC_POLARITY_HIGH</code>	VSYNC signal is active high.
<code>PDC_VSYNC_POLARITY_LOW</code>	VSYNC signal is active low.

◆ **pdc\_event\_t**

enum <code>pdc_event_t</code>	
PDC events	
Enumerator	
<code>PDC_EVENT_TRANSFER_COMPLETE</code>	Complete frame transferred by DMAC/DTC.
<code>PDC_EVENT_RX_DATA_READY</code>	Receive data ready interrupt.
<code>PDC_EVENT_FRAME_END</code>	Frame end interrupt.
<code>PDC_EVENT_ERR_OVERRUN</code>	Overrun interrupt.
<code>PDC_EVENT_ERR_UNDERRUN</code>	Underrun interrupt.
<code>PDC_EVENT_ERR_V_SET</code>	Vertical line setting error interrupt.
<code>PDC_EVENT_ERR_H_SET</code>	Horizontal byte number setting error interrupt.

## 4.3.27 POEG Interface

### Interfaces

#### Detailed Description

Interface for the Port Output Enable for GPT.

Defines the API and data structures for the Port Output Enable for GPT (POEG) interface.

## Summary

The POEG disables GPT output pins based on configurable events.

Implemented by: [Port Output Enable for GPT \(r\\_poeg\)](#)

## Data Structures

struct [poeg\\_status\\_t](#)

struct [poeg\\_callback\\_args\\_t](#)

struct [poeg\\_cfg\\_t](#)

struct [poeg\\_api\\_t](#)

struct [poeg\\_instance\\_t](#)

## Typedefs

typedef void [poeg\\_ctrl\\_t](#)

## Enumerations

enum [poeg\\_state\\_t](#)

enum [poeg\\_trigger\\_t](#)

enum [poeg\\_gtetrg\\_polarity\\_t](#)

enum [poeg\\_gtetrg\\_noise\\_filter\\_t](#)

## Data Structure Documentation

### ◆ [poeg\\_status\\_t](#)

struct <a href="#">poeg_status_t</a>		
POEG status		
Data Fields		
<a href="#">poeg_state_t</a>	state	Current state of POEG.

### ◆ [poeg\\_callback\\_args\\_t](#)

struct <a href="#">poeg_callback_args_t</a>		
Callback function parameter data.		
Data Fields		
void const *	p_context	Placeholder for user data, set in <a href="#">poeg_cfg_t</a> .

### ◆ [poeg\\_cfg\\_t](#)

struct <a href="#">poeg_cfg_t</a>
-----------------------------------

User configuration structure, used in the open function.	
<b>Data Fields</b>	
<code>poeg_trigger_t</code>	<code>trigger</code>
	Select one or more triggers for the POEG.
<code>poeg_gtetrg_polarity_t</code>	<code>polarity</code>
	Select the polarity for the GTETRG pin.
<code>poeg_gtetrg_noise_filter_t</code>	<code>noise_filter</code>
	Configure the GTETRG noise filter.
<code>void(*</code>	<code>p_callback</code> <code>)(poeg_callback_args_t *p_args)</code>
<code>void const *</code>	<code>p_context</code>
<code>uint32_t</code>	<code>channel</code>
	Channel 0 corresponds to GTETRGA, 1 to GTETRGB, etc.
<code>IRQn_Type</code>	<code>irq</code>
	NVIC interrupt number assigned to this instance.
<code>uint8_t</code>	<code>ipl</code>
	POEG interrupt priority.
<b>Field Documentation</b>	
◆ <b>p_callback</b>	
<code>void(* poeg_cfg_t::p_callback) (poeg_callback_args_t *p_args)</code>	
Callback called when a POEG interrupt occurs.	

◆ **p\_context**

```
void const* poeg_cfg_t::p_context
```

Placeholder for user data. Passed to the user callback in [poeg\\_callback\\_args\\_t](#).

◆ **poeg\_api\_t**

```
struct poeg_api_t
```

Port Output Enable for GPT (POEG) API structure. POEG functions implemented at the HAL layer will follow this API.

**Data Fields**

<a href="#">fsp_err_t</a> (*	<a href="#">open</a> )(poeg_ctrl_t *const p_ctrl, poeg_cfg_t const *const p_cfg)
------------------------------	----------------------------------------------------------------------------------

<a href="#">fsp_err_t</a> (*	<a href="#">statusGet</a> )(poeg_ctrl_t *const p_ctrl, poeg_status_t *p_status)
------------------------------	---------------------------------------------------------------------------------

<a href="#">fsp_err_t</a> (*	<a href="#">callbackSet</a> )(poeg_ctrl_t *const p_api_ctrl, void(*p_callback)(poeg_callback_args_t *), void const *const p_context, poeg_callback_args_t *const p_callback_memory)
------------------------------	-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------

<a href="#">fsp_err_t</a> (*	<a href="#">outputDisable</a> )(poeg_ctrl_t *const p_ctrl)
------------------------------	------------------------------------------------------------

<a href="#">fsp_err_t</a> (*	<a href="#">reset</a> )(poeg_ctrl_t *const p_ctrl)
------------------------------	----------------------------------------------------

<a href="#">fsp_err_t</a> (*	<a href="#">close</a> )(poeg_ctrl_t *const p_ctrl)
------------------------------	----------------------------------------------------

<a href="#">fsp_err_t</a> (*	<a href="#">versionGet</a> )(fsp_version_t *const p_version)
------------------------------	--------------------------------------------------------------

**Field Documentation**

◆ **open**

```
fsp_err_t(* poeg_api_t::open) (poeg_ctrl_t *const p_ctrl, poeg_cfg_t const *const p_cfg)
```

Initial configuration.

**Implemented as**

- R\_POEG\_Open()

**Parameters**

[in]	p_ctrl	Pointer to control block. Must be declared by user. Elements set here.
[in]	p_cfg	Pointer to configuration structure. All elements of this structure must be set by user.

◆ **statusGet**

```
fsp_err_t(* poeg_api_t::statusGet) (poeg_ctrl_t *const p_ctrl, poeg_status_t *p_status)
```

Gets the current driver state.

**Implemented as**

- R\_POEG\_StatusGet()

**Parameters**

[in]	p_ctrl	Control block set in <a href="#">poeg_api_t::open</a> call.
[out]	p_status	Provides the current state of the POEG.

### ◆ callbackSet

```
fsp_err_t(* poeg_api_t::callbackSet) (poeg_ctrl_t *const p_api_ctrl,
void(*p_callback)(poeg_callback_args_t *), void const *const p_context, poeg_callback_args_t
*const p_callback_memory)
```

Specify callback function and optional context pointer and working memory pointer.

#### Implemented as

- R\_POEG\_CallbackSet()

#### Parameters

[in]	p_ctrl	Control block set in <a href="#">poeg_api_t::open</a> call for this timer.
[in]	p_callback	Callback function to register
[in]	p_context	Pointer to send to callback function
[in]	p_working_memory	Pointer to volatile memory where callback structure can be allocated. Callback arguments allocated here are only valid during the callback.

### ◆ outputDisable

```
fsp_err_t(* poeg_api_t::outputDisable) (poeg_ctrl_t *const p_ctrl)
```

Disables GPT output pins by software request.

#### Implemented as

- R\_POEG\_OutputDisable()

#### Parameters

[in]	p_ctrl	Control block set in <a href="#">poeg_api_t::open</a> call.
------	--------	-------------------------------------------------------------



◆ **reset**

`fsp_err_t(* poeg_api_t::reset) (poeg_ctrl_t *const p_ctrl)`

Attempts to clear status flags to reenable GPT output pins. Confirm all status flags are cleared after calling this function by calling `poeg_api_t::statusGet()`.

**Implemented as**

- `R_POEG_Reset()`

**Parameters**

[in]	p_ctrl	Control block set in <code>poeg_api_t::open</code> call.
------	--------	----------------------------------------------------------

◆ **close**

`fsp_err_t(* poeg_api_t::close) (poeg_ctrl_t *const p_ctrl)`

Disables POEG interrupt.

**Implemented as**

- `R_POEG_Close()`

**Parameters**

[in]	p_ctrl	Control block set in <code>poeg_api_t::open</code> call.
------	--------	----------------------------------------------------------

◆ **versionGet**

`fsp_err_t(* poeg_api_t::versionGet) (fsp_version_t *const p_version)`

Get version and stores it in provided pointer p\_version.

**Implemented as**

- `R_POEG_VersionGet()`

**Parameters**

[out]	p_version	Code and API version used.
-------	-----------	----------------------------

◆ **poeg\_instance\_t**

`struct poeg_instance_t`

This structure encompasses everything that is needed to use an instance of this interface.

## Data Fields

<code>poeg_ctrl_t *</code>	p_ctrl	Pointer to the control structure for this instance.
<code>poeg_cfg_t const *</code>	p_cfg	Pointer to the configuration structure for this instance.

<code>poeg_api_t</code> const *	<code>p_api</code>	Pointer to the API structure for this instance.
---------------------------------	--------------------	-------------------------------------------------

## Typedef Documentation

### ◆ `poeg_ctrl_t`

typedef void <code>poeg_ctrl_t</code>
DOC control block. Allocate an instance specific control block to pass into the DOC API calls.
<b>Implemented as</b>
<ul style="list-style-type: none"> <li>◦ <code>poeg_instance_ctrl_t</code></li> </ul>

## Enumeration Type Documentation

### ◆ `poeg_state_t`

enum <code>poeg_state_t</code>	
POEG states.	
Enumerator	
<code>POEG_STATE_NO_DISABLE_REQUEST</code>	GPT output is not disabled by POEG.
<code>POEG_STATE_PIN_DISABLE_REQUEST</code>	GPT output disabled due to GTETRGM pin level.
<code>POEG_STATE_GPT_OR_COMPARATOR_DISABLE_REQUEST</code>	GPT output disabled due to high speed analog comparator or GPT.
<code>POEG_STATE_OSCILLATION_STOP_DISABLE_REQUEST</code>	GPT output disabled due to main oscillator stop.
<code>POEG_STATE_SOFTWARE_STOP_DISABLE_REQUEST</code>	GPT output disabled due to <code>poeg_api_t::outputDisable()</code>
<code>POEG_STATE_PIN_DISABLE_REQUEST_ACTIVE</code>	GPT output disable request active from the GTETRGM pin. If a filter is used, this flag represents the state of the filtered input.

## ◆ poeg\_trigger\_t

enum poeg_trigger_t	
Triggers that will disable GPT output pins.	
Enumerator	
POEG_TRIGGER_SOFTWARE	Software disable is always supported with POEG. Select this option if no other triggers are used.
POEG_TRIGGER_PIN	Disable GPT output based on GTETRGM input level.
POEG_TRIGGER_GPT_OUTPUT_LEVEL	Disable GPT output based on GPT output pin levels.
POEG_TRIGGER_OSCILLATION_STOP	Disable GPT output based on main oscillator stop.
POEG_TRIGGER_ACMPHS0	Disable GPT output based on ACMPHS0 comparator result.
POEG_TRIGGER_ACMPHS1	Disable GPT output based on ACMPHS1 comparator result.
POEG_TRIGGER_ACMPHS2	Disable GPT output based on ACMPHS2 comparator result.
POEG_TRIGGER_ACMPHS3	Disable GPT output based on ACMPHS3 comparator result.
POEG_TRIGGER_ACMPHS4	Disable GPT output based on ACMPHS4 comparator result.
POEG_TRIGGER_ACMPHS5	Disable GPT output based on ACMPHS5 comparator result.

◆ **poeg\_gtetrg\_polarity\_t**

enum <a href="#">poeg_gtetrg_polarity_t</a>	
GTETRG polarity.	
Enumerator	
POEG_GTETRG_POLARITY_ACTIVE_HIGH	Disable GPT output based when GTETRG input level is high.
POEG_GTETRG_POLARITY_ACTIVE_LOW	Disable GPT output based when GTETRG input level is low.

◆ **poeg\_gtetrg\_noise\_filter\_t**

enum <a href="#">poeg_gtetrg_noise_filter_t</a>	
GTETRG noise filter. For the input signal to pass through the noise filter, the active level set in <a href="#">poeg_gtetrg_polarity_t</a> must be read 3 consecutive times at the sampling clock selected.	
Enumerator	
POEG_GTETRG_NOISE_FILTER_DISABLED	No noise filter applied to GTETRG input.
POEG_GTETRG_NOISE_FILTER_PCLKB_DIV_1	Apply noise filter with sample clock PCLKB.
POEG_GTETRG_NOISE_FILTER_PCLKB_DIV_8	Apply noise filter with sample clock PCLKB/8.
POEG_GTETRG_NOISE_FILTER_PCLKB_DIV_32	Apply noise filter with sample clock PCLKB/32.
POEG_GTETRG_NOISE_FILTER_PCLKB_DIV_128	Apply noise filter with sample clock PCLKB/128.

## 4.3.28 RTC Interface

### Interfaces

#### Detailed Description

Interface for accessing the Realtime Clock.

## Summary

The RTC Interface is for configuring Real Time Clock (RTC) functionality including alarm, periodic notification and error adjustment.

The Real Time Clock Interface can be implemented by:

- [Realtime Clock \(r\\_rtc\)](#)

## Data Structures

struct [rtc\\_callback\\_args\\_t](#)

struct [rtc\\_error\\_adjustment\\_cfg\\_t](#)

struct [rtc\\_alarm\\_time\\_t](#)

struct [rtc\\_info\\_t](#)

struct [rtc\\_cfg\\_t](#)

struct [rtc\\_api\\_t](#)

struct [rtc\\_instance\\_t](#)

## Typedefs

typedef struct tm [rtc\\_time\\_t](#)

typedef void [rtc\\_ctrl\\_t](#)

## Enumerations

enum [rtc\\_event\\_t](#)

enum [rtc\\_clock\\_source\\_t](#)

enum [rtc\\_status\\_t](#)

enum [rtc\\_error\\_adjustment\\_t](#)

enum [rtc\\_error\\_adjustment\\_mode\\_t](#)

enum [rtc\\_error\\_adjustment\\_period\\_t](#)

enum [rtc\\_periodic\\_irq\\_select\\_t](#)

## Data Structure Documentation

### ◆ [rtc\\_callback\\_args\\_t](#)

struct [rtc\\_callback\\_args\\_t](#)

Callback function parameter data

Data Fields

<a href="#">rtc_event_t</a>	event	The event can be used to identify what caused the callback (compare match or error).
void const *	p_context	Placeholder for user data.

#### ◆ [rtc\\_error\\_adjustment\\_cfg\\_t](#)

struct rtc_error_adjustment_cfg_t		
Time error adjustment value configuration		
Data Fields		
<a href="#">rtc_error_adjustment_mode_t</a>	adjustment_mode	Automatic Adjustment Enable/Disable.
<a href="#">rtc_error_adjustment_period_t</a>	adjustment_period	Error Adjustment period.
<a href="#">rtc_error_adjustment_t</a>	adjustment_type	Time error adjustment setting.
uint32_t	adjustment_value	Value of the prescaler for error adjustment.

#### ◆ [rtc\\_alarm\\_time\\_t](#)

struct rtc_alarm_time_t		
Alarm time setting structure		
Data Fields		
<a href="#">rtc_time_t</a>	time	Time structure.
bool	sec_match	Enable the alarm based on a match of the seconds field.
bool	min_match	Enable the alarm based on a match of the minutes field.
bool	hour_match	Enable the alarm based on a match of the hours field.
bool	mday_match	Enable the alarm based on a match of the days field.
bool	mon_match	Enable the alarm based on a match of the months field.
bool	year_match	Enable the alarm based on a match of the years field.
bool	dayofweek_match	Enable the alarm based on a match of the dayofweek field.

#### ◆ [rtc\\_info\\_t](#)

struct rtc_info_t		
RTC Information Structure for information returned by infoGet()		
Data Fields		

<a href="#">rtc_clock_source_t</a>	<a href="#">clock_source</a>	Clock source for the RTC block.
<a href="#">rtc_status_t</a>	<a href="#">status</a>	RTC run status.

◆ [rtc\\_cfg\\_t](#)

struct <a href="#">rtc_cfg_t</a>		
User configuration structure, used in <code>open</code> function		
<b>Data Fields</b>		
<a href="#">rtc_clock_source_t</a>	<a href="#">clock_source</a>	Clock source for the RTC block.
<a href="#">uint32_t</a>	<a href="#">freq_compare_value_loco</a>	The frequency comparison value for LOCO.
<a href="#">rtc_error_adjustment_cfg_t</a> const *const	<a href="#">p_err_cfg</a>	Pointer to Error Adjustment configuration.
<a href="#">uint8_t</a>	<a href="#">alarm_ipl</a>	Alarm interrupt priority.
<a href="#">IRQn_Type</a>	<a href="#">alarm_irq</a>	Alarm interrupt vector.
<a href="#">uint8_t</a>	<a href="#">periodic_ipl</a>	Periodic interrupt priority.
<a href="#">IRQn_Type</a>	<a href="#">periodic_irq</a>	Periodic interrupt vector.
<a href="#">uint8_t</a>	<a href="#">carry_ipl</a>	

	Carry interrupt priority.
IRQn_Type	<a href="#">carry_irq</a>
	Carry interrupt vector.
void(*	<a href="#">p_callback</a> )(rtc_callback_args_t *p_args)
	Called from the ISR.
void const *	<a href="#">p_context</a>
	User defined context passed into callback function.
void const *	<a href="#">p_extend</a>
	RTC hardware dependant configuration.

#### ◆ rtc\_api\_t

struct rtc_api_t	
RTC driver structure. General RTC functions implemented at the HAL layer follow this API.	
<b>Data Fields</b>	
fsp_err_t(*	<a href="#">open</a> )(rtc_ctrl_t *const p_ctrl, <a href="#">rtc_cfg_t</a> const *const p_cfg)
fsp_err_t(*	<a href="#">close</a> )(rtc_ctrl_t *const p_ctrl)
fsp_err_t(*	<a href="#">calendarTimeSet</a> )(rtc_ctrl_t *const p_ctrl, <a href="#">rtc_time_t</a> *const p_time)
fsp_err_t(*	<a href="#">calendarTimeGet</a> )(rtc_ctrl_t *const p_ctrl, <a href="#">rtc_time_t</a> *const p_time)
fsp_err_t(*	<a href="#">calendarAlarmSet</a> )(rtc_ctrl_t *const p_ctrl, <a href="#">rtc_alarm_time_t</a> *const p_alarm)
fsp_err_t(*	<a href="#">calendarAlarmGet</a> )(rtc_ctrl_t *const p_ctrl, <a href="#">rtc_alarm_time_t</a> *const p_alarm)



<code>fsp_err_t(*</code>	<code>periodicIrqRateSet )(rtc_ctrl_t *const p_ctrl, rtc_periodic_irq_select_t const rate)</code>
<code>fsp_err_t(*</code>	<code>errorAdjustmentSet )(rtc_ctrl_t *const p_ctrl, rtc_error_adjustment_cfg_t const *const err_adj_cfg)</code>
<code>fsp_err_t(*</code>	<code>callbackSet )(rtc_ctrl_t *const p_ctrl, void(*p_callback)(rtc_callback_args_t *), void const *const p_context, rtc_callback_args_t *const p_callback_memory)</code>
<code>fsp_err_t(*</code>	<code>infoGet )(rtc_ctrl_t *const p_ctrl, rtc_info_t *const p_rtc_info)</code>
<code>fsp_err_t(*</code>	<code>versionGet )(fsp_version_t *const version)</code>

## Field Documentation

### ◆ open

`fsp_err_t(* rtc_api_t::open) (rtc_ctrl_t *const p_ctrl, rtc_cfg_t const *const p_cfg)`

Open the RTC driver.

#### Implemented as

- `R_RTC_Open()`

#### Parameters

[in]	<code>p_ctrl</code>	Pointer to RTC device handle
[in]	<code>p_cfg</code>	Pointer to the configuration structure

### ◆ close

`fsp_err_t(* rtc_api_t::close) (rtc_ctrl_t *const p_ctrl)`

Close the RTC driver.

#### Implemented as

- `R_RTC_Close()`

#### Parameters

[in]	<code>p_ctrl</code>	Pointer to RTC device handle.
------	---------------------	-------------------------------

◆ **calendarTimeSet**

```
fsp_err_t(* rtc_api_t::calendarTimeSet) (rtc_ctrl_t *const p_ctrl, rtc_time_t *const p_time)
```

Set the calendar time and start the calendar counter

**Implemented as**

- [R\\_RTC\\_CalendarTimeSet\(\)](#)

**Parameters**

[in]	p_ctrl	Pointer to RTC device handle
[in]	p_time	Pointer to a time structure that contains the time to set
[in]	clock_start	Flag that starts the clock right after it is set

◆ **calendarTimeGet**

```
fsp_err_t(* rtc_api_t::calendarTimeGet) (rtc_ctrl_t *const p_ctrl, rtc_time_t *const p_time)
```

Get the calendar time.

**Implemented as**

- [R\\_RTC\\_CalendarTimeGet\(\)](#)

**Parameters**

[in]	p_ctrl	Pointer to RTC device handle
[out]	p_time	Pointer to a time structure that contains the time to get

◆ **calendarAlarmSet**

```
fsp_err_t(* rtc_api_t::calendarAlarmSet) (rtc_ctrl_t *const p_ctrl, rtc_alarm_time_t *const p_alarm)
```

Set the calendar alarm time and enable the alarm interrupt.

**Implemented as**

- [R\\_RTC\\_CalendarAlarmSet\(\)](#)

**Parameters**

[in]	p_ctrl	Pointer to RTC device handle
[in]	p_alarm	Pointer to an alarm structure that contains the alarm time to set
[in]	irq_enable_flag	Enable the ALARM irq if set

◆ **calendarAlarmGet**

```
fsp_err_t(* rtc_api_t::calendarAlarmGet) (rtc_ctrl_t *const p_ctrl, rtc_alarm_time_t *const p_alarm)
```

Get the calendar alarm time.

**Implemented as**

- [R\\_RTC\\_CalendarAlarmGet\(\)](#)

**Parameters**

[in]	p_ctrl	Pointer to RTC device handle
[out]	p_alarm	Pointer to an alarm structure to fill up with the alarm time

◆ **periodicIrqRateSet**

```
fsp_err_t(* rtc_api_t::periodicIrqRateSet) (rtc_ctrl_t *const p_ctrl, rtc_periodic_irq_select_t const rate)
```

Set the periodic irq rate

**Implemented as**

- [R\\_RTC\\_PeriodicIrqRateSet\(\)](#)

**Parameters**

[in]	p_ctrl	Pointer to RTC device handle
[in]	rate	Rate of periodic interrupts

◆ **errorAdjustmentSet**

```
fsp_err_t(* rtc_api_t::errorAdjustmentSet) (rtc_ctrl_t *const p_ctrl, rtc_error_adjustment_cfg_t const *const err_adj_cfg)
```

Set time error adjustment.

**Implemented as**

- [R\\_RTC\\_ErrorAdjustmentSet\(\)](#)

**Parameters**

[in]	p_ctrl	Pointer to control handle structure
[in]	err_adj_cfg	Pointer to the Error Adjustment Config

◆ **callbackSet**

```
fsp_err_t(* rtc_api_t::callbackSet) (rtc_ctrl_t *const p_ctrl, void(*p_callback)(rtc_callback_args_t *),
void const *const p_context, rtc_callback_args_t *const p_callback_memory)
```

Specify callback function and optional context pointer and working memory pointer.

**Implemented as**

- [R\\_RTC\\_CallbackSet\(\)](#)

**Parameters**

[in]	p_ctrl	Pointer to the RTC control block.
[in]	p_callback	Callback function
[in]	p_context	Pointer to send to callback function
[in]	p_working_memory	Pointer to volatile memory where callback structure can be allocated

◆ **infoGet**

```
fsp_err_t(* rtc_api_t::infoGet) (rtc_ctrl_t *const p_ctrl, rtc_info_t *const p_rtc_info)
```

Return the currently configure clock source for the RTC

**Implemented as**

- [R\\_RTC\\_InfoGet\(\)](#)

**Parameters**

[in]	p_ctrl	Pointer to control handle structure
[out]	p_rtc_info	Pointer to RTC information structure

◆ **versionGet**

```
fsp_err_t(* rtc_api_t::versionGet) (fsp_version_t *const version)
```

Gets version and stores it in provided pointer p\_version.

**Implemented as**

- [R\\_RTC\\_VersionGet\(\)](#)

**Parameters**

[out]	p_version	Code and API version used
-------	-----------	---------------------------

◆ **rtc\_instance\_t**

struct rtc_instance_t		
This structure encompasses everything that is needed to use an instance of this interface.		
Data Fields		
<code>rtc_ctrl_t *</code>	<code>p_ctrl</code>	Pointer to the control structure for this instance.
<code>rtc_cfg_t const *</code>	<code>p_cfg</code>	Pointer to the configuration structure for this instance.
<code>rtc_api_t const *</code>	<code>p_api</code>	Pointer to the API structure for this instance.

## Typedef Documentation

### ◆ `rtc_time_t`

typedef struct tm <code>rtc_time_t</code>
Date and time structure defined in C standard library <time.h>

### ◆ `rtc_ctrl_t`

typedef void <code>rtc_ctrl_t</code>
RTC control block. Allocate an instance specific control block to pass into the RTC API calls.
<b>Implemented as</b>
◦ <code>rtc_instance_ctrl_t</code>

## Enumeration Type Documentation

### ◆ `rtc_event_t`

enum <code>rtc_event_t</code>	
Events that can trigger a callback function	
Enumerator	
<code>RTC_EVENT_ALARM_IRQ</code>	Real Time Clock ALARM IRQ.
<code>RTC_EVENT_PERIODIC_IRQ</code>	Real Time Clock PERIODIC IRQ.

◆ **rtc\_clock\_source\_t**

enum <code>rtc_clock_source_t</code>	
Clock source for the RTC block	
Enumerator	
<code>RTC_CLOCK_SOURCE_SUBCLK</code>	Sub-clock oscillator.
<code>RTC_CLOCK_SOURCE_LOCO</code>	Low power On Chip Oscillator.

◆ **rtc\_status\_t**

enum <code>rtc_status_t</code>	
RTC run state	
Enumerator	
<code>RTC_STATUS_STOPPED</code>	RTC counter is stopped.
<code>RTC_STATUS_RUNNING</code>	RTC counter is running.

◆ **rtc\_error\_adjustment\_t**

enum <code>rtc_error_adjustment_t</code>	
Time error adjustment settings	
Enumerator	
<code>RTC_ERROR_ADJUSTMENT_NONE</code>	Adjustment is not performed.
<code>RTC_ERROR_ADJUSTMENT_ADD_PRESCALER</code>	Adjustment is performed by the addition to the prescaler.
<code>RTC_ERROR_ADJUSTMENT_SUBTRACT_PRESCALER</code>	Adjustment is performed by the subtraction from the prescaler.

**◆ rtc\_error\_adjustment\_mode\_t**

enum <code>rtc_error_adjustment_mode_t</code>	
Time error adjustment mode settings	
Enumerator	
<code>RTC_ERROR_ADJUSTMENT_MODE_MANUAL</code>	Adjustment mode is set to manual.
<code>RTC_ERROR_ADJUSTMENT_MODE_AUTOMATIC</code>	Adjustment mode is set to automatic.

**◆ rtc\_error\_adjustment\_period\_t**

enum <code>rtc_error_adjustment_period_t</code>	
Time error adjustment period settings	
Enumerator	
<code>RTC_ERROR_ADJUSTMENT_PERIOD_1_MINUTE</code>	Adjustment period is set to every one minute.
<code>RTC_ERROR_ADJUSTMENT_PERIOD_10_SECOND</code>	Adjustment period is set to every ten second.
<code>RTC_ERROR_ADJUSTMENT_PERIOD_NONE</code>	Adjustment period not supported in manual mode.

◆ **rtc\_periodic\_irq\_select\_t**

enum <code>rtc_periodic_irq_select_t</code>	
Periodic Interrupt select	
Enumerator	
<code>RTC_PERIODIC_IRQ_SELECT_1_DIV_BY_256_SECONDS</code>	A periodic irq is generated every 1/256 second.
<code>RTC_PERIODIC_IRQ_SELECT_1_DIV_BY_128_SECONDS</code>	A periodic irq is generated every 1/128 second.
<code>RTC_PERIODIC_IRQ_SELECT_1_DIV_BY_64_SECONDS</code>	A periodic irq is generated every 1/64 second.
<code>RTC_PERIODIC_IRQ_SELECT_1_DIV_BY_32_SECONDS</code>	A periodic irq is generated every 1/32 second.
<code>RTC_PERIODIC_IRQ_SELECT_1_DIV_BY_16_SECONDS</code>	A periodic irq is generated every 1/16 second.
<code>RTC_PERIODIC_IRQ_SELECT_1_DIV_BY_8_SECONDS</code>	A periodic irq is generated every 1/8 second.
<code>RTC_PERIODIC_IRQ_SELECT_1_DIV_BY_4_SECONDS</code>	A periodic irq is generated every 1/4 second.
<code>RTC_PERIODIC_IRQ_SELECT_1_DIV_BY_2_SECONDS</code>	A periodic irq is generated every 1/2 second.
<code>RTC_PERIODIC_IRQ_SELECT_1_SECOND</code>	A periodic irq is generated every 1 second.
<code>RTC_PERIODIC_IRQ_SELECT_2_SECONDS</code>	A periodic irq is generated every 2 seconds.

**4.3.29 SD/MMC Interface**[Interfaces](#)**Detailed Description**

Interface for accessing SD, eMMC, and SDIO devices.

**Summary**

The `r_sdhi` interface provides standard SD and eMMC media functionality. This interface also supports SDIO.

The SD/MMC interface is implemented by:



- SD/MMC Host Interface (r\_sdhi)

## Data Structures

struct [sdmmc\\_status\\_t](#)

struct [sdmmc\\_device\\_t](#)

struct [sdmmc\\_callback\\_args\\_t](#)

struct [sdmmc\\_cfg\\_t](#)

struct [sdmmc\\_api\\_t](#)

struct [sdmmc\\_instance\\_t](#)

## Typedefs

typedef void [sdmmc\\_ctrl\\_t](#)

## Enumerations

enum [sdmmc\\_card\\_type\\_t](#)

enum [sdmmc\\_bus\\_width\\_t](#)

enum [sdmmc\\_io\\_transfer\\_mode\\_t](#)

enum [sdmmc\\_io\\_address\\_mode\\_t](#)

enum [sdmmc\\_io\\_write\\_mode\\_t](#)

enum [sdmmc\\_event\\_t](#)

enum [sdmmc\\_card\\_detect\\_t](#)

enum [sdmmc\\_write\\_protect\\_t](#)

enum [sdmmc\\_r1\\_state\\_t](#)

## Data Structure Documentation

### ◆ [sdmmc\\_status\\_t](#)

struct [sdmmc\\_status\\_t](#)

Current status.

#### Data Fields

bool	initialized	False if card was removed (only applies if MCU supports card)
------	-------------	---------------------------------------------------------------

		detection and SDnCD pin is connected), true otherwise.  If ready is false, call <a href="#">sdmmc_api_t::medialnit</a> to reinitialize it
bool	transfer_in_progress	true = Card is busy
bool	card_inserted	Card detect status, true if card detect is not used.

◆ **sdmmc\_device\_t**

struct sdmmc_device_t		
Information obtained from the media device.		
Data Fields		
<a href="#">sdmmc_card_type_t</a>	card_type	SD, eMMC, or SDIO.
bool	write_protected	true = Card is write protected
uint32_t	clock_rate	Current clock rate.
uint32_t	sector_count	Sector count.
uint32_t	sector_size_bytes	Sector size.
uint32_t	erase_sector_count	Minimum erasable unit (in 512 byte sectors)

◆ **sdmmc\_callback\_args\_t**

struct sdmmc_callback_args_t		
Callback function parameter data		
Data Fields		
<a href="#">sdmmc_event_t</a>	event	The event can be used to identify what caused the callback.
sdmmc_response_t	response	Response from card, only valid if SDMMC_EVENT_RESPONSE is set in event.
void const *	p_context	Placeholder for user data.

◆ **sdmmc\_cfg\_t**

struct sdmmc_cfg_t		
SD/MMC Configuration		
<b>Data Fields</b>		
uint8_t	<a href="#">channel</a>	
		Channel of SD/MMC host interface.

<code>sdmmc_bus_width_t</code>	<code>bus_width</code>
	Device bus width is 1, 4 or 8 bits wide.
<code>transfer_instance_t const *</code>	<code>p_lower_lvl_transfer</code>
	Transfer instance used to move data with DMA or DTC.
<code>void(*</code>	<code>p_callback )(sdmmc_callback_args_t *p_args)</code>
	Pointer to callback function.
<code>void const *</code>	<code>p_context</code>
	User defined context passed into callback function.
<code>void const *</code>	<code>p_extend</code>
	SD/MMC hardware dependent configuration.
<code>uint32_t</code>	<code>block_size</code>
<code>sdmmc_card_detect_t</code>	<code>card_detect</code>
<code>sdmmc_write_protect_t</code>	<code>write_protect</code>
<code>IRQn_Type</code>	<code>access_irq</code>
	Access IRQ number.
<code>IRQn_Type</code>	<code>sdio_irq</code>
	SDIO IRQ number.
<code>IRQn_Type</code>	<code>card_irq</code>

	Card IRQ number.
IRQn_Type	<a href="#">dma_req_irq</a>
	DMA request IRQ number.
uint8_t	<a href="#">access_ipl</a>
	Access interrupt priority.
uint8_t	<a href="#">sdio_ipl</a>
	SDIO interrupt priority.
uint8_t	<a href="#">card_ipl</a>
	Card interrupt priority.
uint8_t	<a href="#">dma_req_ipl</a>
	DMA request interrupt priority.

## Field Documentation

### ◆ **block\_size**

[uint32\\_t sdmmc\\_cfg\\_t::block\\_size](#)

Block size in bytes. Block size must be 512 bytes for SD cards and eMMC devices. Block size can be 1-512 bytes for SDIO.

### ◆ **card\_detect**

[sdmmc\\_card\\_detect\\_t sdmmc\\_cfg\\_t::card\\_detect](#)

Whether or not card detection is used.

### ◆ **write\_protect**

[sdmmc\\_write\\_protect\\_t sdmmc\\_cfg\\_t::write\\_protect](#)

Select whether or not to use the write protect pin. Select Not Used if the MCU or device does not have a write protect pin.

◆ **sdmmc\_api\_t**

struct sdmmc_api_t	
SD/MMC functions implemented at the HAL layer API.	
Data Fields	
fsp_err_t(*)	<a href="#">open</a> )(sdmmc_ctrl_t *const p_ctrl, sdmmc_cfg_t const *const p_cfg)
fsp_err_t(*)	<a href="#">medialnit</a> )(sdmmc_ctrl_t *const p_ctrl, sdmmc_device_t *const p_device)
fsp_err_t(*)	<a href="#">read</a> )(sdmmc_ctrl_t *const p_ctrl, uint8_t *const p_dest, uint32_t const start_sector, uint32_t const sector_count)
fsp_err_t(*)	<a href="#">write</a> )(sdmmc_ctrl_t *const p_ctrl, uint8_t const *const p_source, uint32_t const start_sector, uint32_t const sector_count)
fsp_err_t(*)	<a href="#">readlo</a> )(sdmmc_ctrl_t *const p_ctrl, uint8_t *const p_data, uint32_t const function, uint32_t const address)
fsp_err_t(*)	<a href="#">writel</a> )(sdmmc_ctrl_t *const p_ctrl, uint8_t *const p_data, uint32_t const function, uint32_t const address, sdmmc_io_write_mode_t const read_after_write)
fsp_err_t(*)	<a href="#">readloExt</a> )(sdmmc_ctrl_t *const p_ctrl, uint8_t *const p_dest, uint32_t const function, uint32_t const address, uint32_t *const count, sdmmc_io_transfer_mode_t transfer_mode, sdmmc_io_address_mode_t address_mode)
fsp_err_t(*)	<a href="#">writelExt</a> )(sdmmc_ctrl_t *const p_ctrl, uint8_t const *const p_source, uint32_t const function, uint32_t const address, uint32_t const count, sdmmc_io_transfer_mode_t transfer_mode, sdmmc_io_address_mode_t address_mode)
fsp_err_t(*)	<a href="#">ioIntEnable</a> )(sdmmc_ctrl_t *const p_ctrl, bool enable)
fsp_err_t(*)	<a href="#">statusGet</a> )(sdmmc_ctrl_t *const p_ctrl, sdmmc_status_t *const p_status)
fsp_err_t(*)	<a href="#">erase</a> )(sdmmc_ctrl_t *const p_ctrl, uint32_t const start_sector, uint32_t const sector_count)

<code>fsp_err_t(*</code>	<code>callbackSet )(sdmmc_ctrl_t *const p_api_ctrl, void(*p_callback)(sdmmc_callback_args_t *), void const *const p_context, sdmmc_callback_args_t *const p_callback_memory)</code>
<code>fsp_err_t(*</code>	<code>close )(sdmmc_ctrl_t *const p_ctrl)</code>
<code>fsp_err_t(*</code>	<code>versionGet )(fsp_version_t *const p_version)</code>

## Field Documentation

### ◆ open

`fsp_err_t(* sdmmc_api_t::open) (sdmmc_ctrl_t *const p_ctrl, sdmmc_cfg_t const *const p_cfg)`

Open the SD/MMC driver.

#### Implemented as

- `R_SDHI_Open()`

#### Parameters

[in]	<code>p_ctrl</code>	Pointer to SD/MMC instance control block.
[in]	<code>p_cfg</code>	Pointer to SD/MMC instance configuration structure.

### ◆ medialnit

`fsp_err_t(* sdmmc_api_t::medialnit) (sdmmc_ctrl_t *const p_ctrl, sdmmc_device_t *const p_device)`

Initializes an SD/MMC device. If the device is a card, the card must be plugged in prior to calling this API. This API blocks until the device initialization procedure is complete.

#### Implemented as

- `R_SDHI_Medialnit()`

#### Parameters

[in]	<code>p_ctrl</code>	Pointer to SD/MMC instance control block.
[out]	<code>p_device</code>	Pointer to store device information.

## ◆ read

```
fsp_err_t(*sdmmc_api_t::read)(sdmmc_ctrl_t*const p_ctrl, uint8_t*const p_dest, uint32_t const start_sector, uint32_t const sector_count)
```

Read data from an SD/MMC channel. This API is not supported for SDIO devices.

**Implemented as**

- [R\\_SDHI\\_Read\(\)](#)

**Parameters**

[in]	p_ctrl	Pointer to an open SD/MMC instance control block.
[out]	p_dest	Pointer to data buffer to read data to.
[in]	start_sector	First sector address to read.
[in]	sector_count	Number of sectors to read. All sectors must be in the range of <a href="#">sdmmc_device_t::sector_count</a> .

## ◆ write

```
fsp_err_t(*sdmmc_api_t::write)(sdmmc_ctrl_t*const p_ctrl, uint8_t const*const p_source, uint32_t const start_sector, uint32_t const sector_count)
```

Write data to SD/MMC channel. This API is not supported for SDIO devices.

**Implemented as**

- [R\\_SDHI\\_Write\(\)](#)

**Parameters**

[in]	p_ctrl	Pointer to an open SD/MMC instance control block.
[in]	p_source	Pointer to data buffer to write data from.
[in]	start_sector	First sector address to write to.
[in]	sector_count	Number of sectors to write. All sectors must be in the range of <a href="#">sdmmc_device_t::sector_count</a> .

◆ **readlo**

```
fsp_err_t(* sdmmc_api_t::readlo) (sdmmc_ctrl_t *const p_ctrl, uint8_t *const p_data, uint32_t const
function, uint32_t const address)
```

Read one byte of I/O data from an SDIO device. This API is not supported for SD or eMMC memory devices.

**Implemented as**

- R\_SDHI\_Readlo()

**Parameters**

[in]	p_ctrl	Pointer to an open SD/MMC instance control block.
[out]	p_data	Pointer to location to store data byte.
[in]	function	SDIO Function Number.
[in]	address	SDIO register address.

◆ **writel0**

```
fsp_err_t(* sdmmc_api_t::writel0) (sdmmc_ctrl_t *const p_ctrl, uint8_t *const p_data, uint32_t const
function, uint32_t const address, sdmmc_io_write_mode_t const read_after_write)
```

Write one byte of I/O data to an SDIO device. This API is not supported for SD or eMMC memory devices.

**Implemented as**

- R\_SDHI\_Writel0()

**Parameters**

[in]	p_ctrl	Pointer to an open SD/MMC instance control block.
[in,out]	p_data	Pointer to data byte to write. Read data is also provided here if read_after_write is true.
[in]	function	SDIO Function Number.
[in]	address	SDIO register address.
[in]	read_after_write	Whether or not to read back the same register after writing



◆ **readloExt**

```
fsp_err_t(* sdmmc_api_t::readloExt) (sdmmc_ctrl_t *const p_ctrl, uint8_t *const p_dest, uint32_t
const function, uint32_t const address, uint32_t *const count, sdmmc_io_transfer_mode_t
transfer_mode, sdmmc_io_address_mode_t address_mode)
```

Read multiple bytes or blocks of I/O data from an SDIO device. This API is not supported for SD or eMMC memory devices.

**Implemented as**

- R\_SDHI\_ReadloExt()

**Parameters**

[in]	p_ctrl	Pointer to an open SD/MMC instance control block.
[out]	p_dest	Pointer to data buffer to read data to.
[in]	function	SDIO Function Number.
[in]	address	SDIO register address.
[in]	count	Number of bytes or blocks to read, maximum 512 bytes or 511 blocks.
[in]	transfer_mode	Byte or block mode
[in]	address_mode	Fixed or incrementing address mode

◆ **writeloExt**

```
fsp_err_t(* sdmmc_api_t::writeloExt) (sdmmc_ctrl_t *const p_ctrl, uint8_t const *const p_source,
uint32_t const function, uint32_t const address, uint32_t const count, sdmmc_io_transfer_mode_t
transfer_mode, sdmmc_io_address_mode_t address_mode)
```

Write multiple bytes or blocks of I/O data to an SDIO device. This API is not supported for SD or eMMC memory devices.

**Implemented as**

- R\_SDHI\_WriteloExt()

**Parameters**

[in]	p_ctrl	Pointer to an open SD/MMC instance control block.
[in]	p_source	Pointer to data buffer to write data from.
[in]	function_number	SDIO Function Number.
[in]	address	SDIO register address.
[in]	count	Number of bytes or blocks to write, maximum 512 bytes or 511 blocks.
[in]	transfer_mode	Byte or block mode
[in]	address_mode	Fixed or incrementing address mode

◆ **ioIntEnable**

```
fsp_err_t(* sdmmc_api_t::ioIntEnable) (sdmmc_ctrl_t *const p_ctrl, bool enable)
```

Enables SDIO interrupt for SD/MMC instance. This API is not supported for SD or eMMC memory devices.

**Implemented as**

- R\_SDHI\_IoIntEnable

**Parameters**

[in]	p_ctrl	Pointer to an open SD/MMC instance control block.
[in]	enable	Interrupt enable = true, interrupt disable = false.

◆ **statusGet**

```
fsp_err_t(* sdmmc_api_t::statusGet) (sdmmc_ctrl_t *const p_ctrl, sdmmc_status_t *const p_status)
```

Get SD/MMC device status.

**Implemented as**

- [R\\_SDHI\\_StatusGet\(\)](#)

**Parameters**

[in]	p_ctrl	Pointer to an open SD/MMC instance control block.
[out]	p_status	Pointer to current driver status.

◆ **erase**

```
fsp_err_t(* sdmmc_api_t::erase) (sdmmc_ctrl_t *const p_ctrl, uint32_t const start_sector, uint32_t const sector_count)
```

Erase SD/MMC sectors. The sector size for erase is fixed at 512 bytes. This API is not supported for SDIO devices.

**Implemented as**

- [R\\_SDHI\\_Erase](#)

**Parameters**

[in]	p_ctrl	Pointer to an open SD/MMC instance control block.
[in]	start_sector	First sector to erase. Must be a multiple of <a href="#">sdmmc_device_t::erase_sector_count</a> .
[in]	sector_count	Number of sectors to erase. Must be a multiple of <a href="#">sdmmc_device_t::erase_sector_count</a> . All sectors must be in the range of <a href="#">sdmmc_device_t::sector_count</a> .

◆ **callbackSet**

```
fsp_err_t(* sdmmc_api_t::callbackSet) (sdmmc_ctrl_t *const p_api_ctrl,
void(*p_callback)(sdmmc_callback_args_t *), void const *const p_context, sdmmc_callback_args_t
*const p_callback_memory)
```

Specify callback function and optional context pointer and working memory pointer.

**Implemented as**

- R\_SDHI\_CallbackSet()

**Parameters**

[in]	p_ctrl	Control block set in <a href="#">sdmmc_api_t::open</a> call.
[in]	p_callback	Callback function to register
[in]	p_context	Pointer to send to callback function
[in]	p_working_memory	Pointer to volatile memory where callback structure can be allocated. Callback arguments allocated here are only valid during the callback.

◆ **close**

```
fsp_err_t(* sdmmc_api_t::close) (sdmmc_ctrl_t *const p_ctrl)
```

Close open SD/MMC device.

**Implemented as**

- R\_SDHI\_Close()

**Parameters**

[in]	p_ctrl	Pointer to an open SD/MMC instance control block.
------	--------	---------------------------------------------------

◆ **versionGet**

```
fsp_err_t(* sdmmc_api_t::versionGet) (fsp_version_t *const p_version)
```

Returns the version of the SD/MMC driver.

**Implemented as**

- R\_SDHI\_VersionGet()

**Parameters**

[out]	p_version	Pointer to return version information to.
-------	-----------	-------------------------------------------

◆ **sdmmc\_instance\_t**

struct sdmmc_instance_t		
This structure encompasses everything that is needed to use an instance of this interface.		
Data Fields		
sdmmc_ctrl_t *	p_ctrl	Pointer to the control structure for this instance.
sdmmc_cfg_t const *	p_cfg	Pointer to the configuration structure for this instance.
sdmmc_api_t const *	p_api	Pointer to the API structure for this instance.

**Typedef Documentation**◆ **sdmmc\_ctrl\_t**

typedef void sdmmc_ctrl_t
SD/MMC control block. Allocate an instance specific control block to pass into the SD/MMC API calls.
<b>Implemented as</b>
◦ sdmmc_instance_ctrl_t

**Enumeration Type Documentation**◆ **sdmmc\_card\_type\_t**

enum sdmmc_card_type_t	
SD/MMC media uses SD protocol or MMC protocol.	
Enumerator	
SDMMC_CARD_TYPE_MMC	The media is an eMMC device.
SDMMC_CARD_TYPE_SD	The media is an SD card.
SDMMC_CARD_TYPE_SDIO	The media is an SDIO card.

◆ **sdmmc\_bus\_width\_t**

enum <a href="#">sdmmc_bus_width_t</a>	
SD/MMC data bus is 1, 4 or 8 bits wide.	
Enumerator	
SDMMC_BUS_WIDTH_1_BIT	Data bus is 1 bit wide.
SDMMC_BUS_WIDTH_4_BITS	Data bus is 4 bits wide.
SDMMC_BUS_WIDTH_8_BITS	Data bus is 8 bits wide.

◆ **sdmmc\_io\_transfer\_mode\_t**

enum <a href="#">sdmmc_io_transfer_mode_t</a>	
SDIO transfer mode, configurable in SDIO read/write extended commands.	
Enumerator	
SDMMC_IO_MODE_TRANSFER_BYTE	SDIO byte transfer mode.
SDMMC_IO_MODE_TRANSFER_BLOCK	SDIO block transfer mode.

◆ **sdmmc\_io\_address\_mode\_t**

enum <a href="#">sdmmc_io_address_mode_t</a>	
SDIO address mode, configurable in SDIO read/write extended commands.	
Enumerator	
SDMMC_IO_ADDRESS_MODE_FIXED	Write all data to the same address.
SDMMC_IO_ADDRESS_MODE_INCREMENT	Increment destination address after each write.

◆ **sdmmc\_io\_write\_mode\_t**

enum <a href="#">sdmmc_io_write_mode_t</a>	
Controls the RAW (read after write) flag of CMD52. Used to read back the status after writing a control register.	
Enumerator	
SDMMC_IO_WRITE_MODE_NO_READ	Write only (do not read back)
SDMMC_IO_WRITE_READ_AFTER_WRITE	Read back the register after write.

◆ **sdmmc\_event\_t**

enum <a href="#">sdmmc_event_t</a>	
Events that can trigger a callback function	
Enumerator	
SDMMC_EVENT_CARD_REMOVED	Card removed event.
SDMMC_EVENT_CARD_INSERTED	Card inserted event.
SDMMC_EVENT_RESPONSE	Response event.
SDMMC_EVENT_SDIO	IO event.
SDMMC_EVENT_TRANSFER_COMPLETE	Read or write complete.
SDMMC_EVENT_TRANSFER_ERROR	Read or write failed.
SDMMC_EVENT_ERASE_COMPLETE	Erase completed.
SDMMC_EVENT_ERASE_BUSY	Erase timeout, poll <a href="#">sdmmc_api_t::statusGet</a> .

◆ **sdmmc\_card\_detect\_t**

enum <a href="#">sdmmc_card_detect_t</a>	
Card detection configuration options.	
Enumerator	
SDMMC_CARD_DETECT_NONE	Card detection unused.
SDMMC_CARD_DETECT_CD	Card detection using the CD pin.

◆ **sdmmc\_write\_protect\_t**

enum <a href="#">sdmmc_write_protect_t</a>	
Write protection configuration options.	
Enumerator	
SDMMC_WRITE_PROTECT_NONE	Write protection unused.
SDMMC_WRITE_PROTECT_WP	Write protection using WP pin.

◆ **sdmmc\_r1\_state\_t**

enum <a href="#">sdmmc_r1_state_t</a>	
Card state when receiving the prior command.	
Enumerator	
SDMMC_R1_STATE_IDLE	Idle State.
SDMMC_R1_STATE_READY	Ready State.
SDMMC_R1_STATE_IDENT	Identification State.
SDMMC_R1_STATE_STBY	Stand-by State.
SDMMC_R1_STATE_TRAN	Transfer State.
SDMMC_R1_STATE_DATA	Sending-data State.
SDMMC_R1_STATE_RCV	Receive-data State.
SDMMC_R1_STATE_PRG	Programming State.
SDMMC_R1_STATE_DIS	Disconnect State (between programming and stand-by)
SDMMC_R1_STATE_IO	This is an I/O card and memory states do not apply.

**4.3.30 SLCDC Interface**[Interfaces](#)



## Detailed Description

Interface for Segment LCD controllers.

### Data Structures

struct [slcdc\\_cfg\\_t](#)

struct [slcdc\\_api\\_t](#)

struct [slcdc\\_instance\\_t](#)

### Typedefs

typedef void [slcdc\\_ctrl\\_t](#)

### Enumerations

enum [slcdc\\_bias\\_method\\_t](#)

enum [slcdc\\_time\\_slice\\_t](#)

enum [slcdc\\_waveform\\_t](#)

enum [slcdc\\_drive\\_volt\\_gen\\_t](#)

enum [slcdc\\_display\\_area\\_control\\_blink\\_t](#)

enum [slcdc\\_display\\_area\\_t](#)

enum [slcdc\\_contrast\\_t](#)

enum [slcdc\\_display\\_on\\_off\\_t](#)

enum [slcdc\\_display\\_enable\\_disable\\_t](#)

enum [slcdc\\_display\\_clock\\_t](#)

enum [slcdc\\_clk\\_div\\_t](#)

## Data Structure Documentation

### ◆ [slcdc\\_cfg\\_t](#)

struct <a href="#">slcdc_cfg_t</a>		
SLCDC configuration block		
Data Fields		
<a href="#">slcdc_display_clock_t</a>	<a href="#">slcdc_clock</a>	LCD clock source (LCDSCKSEL)
<a href="#">slcdc_clk_div_t</a>	<a href="#">slcdc_clock_setting</a>	LCD clock setting (LCDC0)

<a href="#">slcdc_bias_method_t</a>	bias_method	LCD display bias method select (LBAS bit)
<a href="#">slcdc_time_slice_t</a>	time_slice	Time slice of LCD display select (LDTY bit)
<a href="#">slcdc_waveform_t</a>	waveform	LCD display waveform select (LWAVE bit)
<a href="#">slcdc_drive_volt_gen_t</a>	drive_volt_gen	LCD Drive Voltage Generator Select (MDSET bit)
<a href="#">slcdc_contrast_t</a>	contrast	LCD Boost Level (contrast setting)

### ◆ [slcdc\\_api\\_t](#)

struct slcdc_api_t	
SLCDC functions implemented at the HAL layer will follow this API.	
<b>Data Fields</b>	
<a href="#">fsp_err_t</a> (*	<a href="#">open</a> )(slcdc_ctrl_t *const p_ctrl, slcdc_cfg_t const *const p_cfg)
<a href="#">fsp_err_t</a> (*	<a href="#">write</a> )(slcdc_ctrl_t *const p_ctrl, uint8_t const start_segment, uint8_t const *p_data, uint8_t const segment_count)
<a href="#">fsp_err_t</a> (*	<a href="#">modify</a> )(slcdc_ctrl_t *const p_ctrl, uint8_t const segment, uint8_t const data_mask, uint8_t const data)
<a href="#">fsp_err_t</a> (*	<a href="#">start</a> )(slcdc_ctrl_t *const p_ctrl)
<a href="#">fsp_err_t</a> (*	<a href="#">stop</a> )(slcdc_ctrl_t *const p_ctrl)
<a href="#">fsp_err_t</a> (*	<a href="#">setContrast</a> )(slcdc_ctrl_t *const p_ctrl, slcdc_contrast_t const contrast)
<a href="#">fsp_err_t</a> (*	<a href="#">setDisplayArea</a> )(slcdc_ctrl_t *const p_ctrl, slcdc_display_area_t const display_area)
<a href="#">fsp_err_t</a> (*	<a href="#">close</a> )(slcdc_ctrl_t *const p_ctrl)
<a href="#">fsp_err_t</a> (*	<a href="#">versionGet</a> )(fsp_version_t *p_version)
<b>Field Documentation</b>	

◆ **open**

```
fsp_err_t(* slcdc_api_t::open) (slcdc_ctrl_t *const p_ctrl, slcdc_cfg_t const *const p_cfg)
```

Open SLCDC.

**Implemented as**

- R\_SLCDC\_Open()

**Parameters**

[in,out]	p_ctrl	Pointer to display interface control block. Must be declared by user.
[in]	p_cfg	Pointer to display configuration structure. All elements of this structure must be set by the user.

◆ **write**

```
fsp_err_t(* slcdc_api_t::write) (slcdc_ctrl_t *const p_ctrl, uint8_t const start_segment, uint8_t const *p_data, uint8_t const segment_count)
```

Write data to the SLCDC segment data array. Specifies the initial display data. Except when using 8-time slice mode, store values in the lower 4 bits when writing to the A-pattern area and in the upper 4 bits when writing to the B-pattern area.

**Implemented as**

- R\_SLCDC\_Write()

**Parameters**

[in]	p_ctrl	Pointer to display interface control block.
[in]	start_segment	Specify the start segment number to be written.
[in]	p_data	Pointer to the display data to be written to the specified segments.
[in]	segment_count	Number of segments to be written.

◆ **modify**

```
fsp_err_t(* slcdc_api_t::modify) (slcdc_ctrl_t *const p_ctrl, uint8_t const segment, uint8_t const data_mask, uint8_t const data)
```

Rewrite data in the SLCDC segment data array. Rewrites the LCD display data in 1-bit units. If a bit is not specified for rewriting, the value stored in the bit is held as it is.

**Implemented as**

- [R\\_SLCDC\\_Modify\(\)](#)

**Parameters**

[in]	p_ctrl	Pointer to display interface control block.
[in]	segment	The segment to be written.
[in]	data_mask	Mask the data being displayed. Set 0 to the bit to be rewritten and set 1 to the other bits. Multiple bits can be rewritten.
[in]	data	Specify display data to rewrite to the specified segment.

◆ **start**

```
fsp_err_t(* slcdc_api_t::start) (slcdc_ctrl_t *const p_ctrl)
```

Enable display signal output. Displays the segment data on the LCD.

**Implemented as**

- [R\\_SLCDC\\_Start\(\)](#)

**Parameters**

[in]	p_ctrl	Pointer to display interface control block.
------	--------	---------------------------------------------

◆ **stop**

```
fsp_err_t(* slcdc_api_t::stop) (slcdc_ctrl_t *const p_ctrl)
```

Disable display signal output. Stops displaying data on the LCD.

**Implemented as**

- [R\\_SLCDC\\_Stop\(\)](#)

**Parameters**

[in]	p_ctrl	Pointer to display interface control block.
------	--------	---------------------------------------------

◆ **setContrast**

```
fsp_err_t(* slcdc_api_t::setContrast) (slcdc_ctrl_t *const p_ctrl, slcdc_contrast_t const contrast)
```

Set the display contrast. This function can be used only when the internal voltage boosting method is used for drive voltage generation.

**Implemented as**

- [R\\_SLCDC\\_SetContrast\(\)](#)

**Parameters**

[in]	p_ctrl	Pointer to display interface control block.
------	--------	---------------------------------------------

◆ **setDisplayArea**

```
fsp_err_t(* slcdc_api_t::setDisplayArea) (slcdc_ctrl_t *const p_ctrl, slcdc_display_area_t const display_area)
```

Set LCD display area. This function sets a specified display area, A-pattern or B-pattern. This function can be used to 'blink' the display between A-pattern and B-pattern area data.

When using blinking, the RTC is required to operate before this function is executed. To configure the RTC, follow the steps below. 1) Open RTC 2) Set Periodic IRQ 3) Start RTC counter 4) Enable IRQ, RTC\_EVENT\_PERIODIC\_IRQ Refer to the User's Manual for the detailed procedure.

**Implemented as**

- [R\\_SLCDC\\_SetDisplayArea\(\)](#)

**Parameters**

[in]	p_ctrl	Pointer to display interface control block.
[in]	display_area	Display area to be used, A-pattern or B-pattern area.

◆ **close**

```
fsp_err_t(* slcdc_api_t::close) (slcdc_ctrl_t *const p_ctrl)
```

Close SLCDC.

**Implemented as**

- [R\\_SLCDC\\_Close\(\)](#)

**Parameters**

[in]	p_ctrl	Pointer to display interface control block.
------	--------	---------------------------------------------

◆ **versionGet**

```
fsp_err_t(* slcdc_api_t::versionGet) (fsp_version_t *p_version)
```

Get version.

**Implemented as**

- R\_SLCDC\_VersionGet()

**Parameters**

[in]	p_version	Pointer to the memory to store the version information.
------	-----------	---------------------------------------------------------

◆ **slcdc\_instance\_t**

```
struct slcdc_instance_t
```

This structure encompasses everything that is needed to use an instance of this interface.

## Data Fields

slcdc_ctrl_t *	p_ctrl	Pointer to the control structure for this instance.
slcdc_cfg_t const *	p_cfg	Pointer to the configuration structure for this instance.
slcdc_api_t const *	p_api	Pointer to the API structure for this instance.

**Typedef Documentation**◆ **slcdc\_ctrl\_t**

```
typedef void slcdc_ctrl_t
```

SLCDC control block. Allocate an instance specific control block to pass into the SLCDC API calls.

**Implemented as**

- slcdc\_instance\_ctrl\_tSLCDC control block

**Enumeration Type Documentation**

◆ **slcdc\_bias\_method\_t**

enum <code>slcdc_bias_method_t</code>	
LCD display bias method.	
Enumerator	
SLCDC_BIAS_2	1/2 bias method
SLCDC_BIAS_3	1/3 bias method
SLCDC_BIAS_4	1/4 bias method

◆ **slcdc\_time\_slice\_t**

enum <code>slcdc_time_slice_t</code>	
Time slice of LCD display.	
Enumerator	
SLCDC_STATIC	Static.
SLCDC_SLICE_2	2-time slice
SLCDC_SLICE_3	3-time slice
SLCDC_SLICE_4	4-time slice
SLCDC_SLICE_8	8-time slice

◆ **slcdc\_waveform\_t**

enum <code>slcdc_waveform_t</code>	
LCD display waveform select.	
Enumerator	
SLCDC_WAVE_A	Waveform A.
SLCDC_WAVE_B	Waveform B.

◆ **slcdc\_drive\_volt\_gen\_t**

enum <code>slcdc_drive_volt_gen_t</code>	
LCD Drive Voltage Generator Select.	
Enumerator	
SLCDC_VOLT_EXTERNAL	External resistance division method.
SLCDC_VOLT_INTERNAL	Internal voltage boosting method.
SLCDC_VOLT_CAPACITOR	Capacitor split method.

◆ **slcdc\_display\_area\_control\_blink\_t**

enum <code>slcdc_display_area_control_blink_t</code>	
Display Data Area Control	
Enumerator	
SLCDC_NOT_BLINKING	Display either A-pattern or B-pattern data.
SLCDC_BLINKING	Alternately display A-pattern and B-pattern data.

◆ **slcdc\_display\_area\_t**

enum <code>slcdc_display_area_t</code>	
Display Area data	
Enumerator	
SLCDC_DISP_A	Display A-pattern data.
SLCDC_DISP_B	Display B-pattern data.
SLCDC_DISP_BLINK	Blink between A- and B-pattern.



◆ **slcdc\_contrast\_t**

enum <code>slcdc_contrast_t</code>	
LCD Boost Level (contrast) settings	
Enumerator	
<code>SLCDC_CONTRAST_0</code>	Contrast level 0.
<code>SLCDC_CONTRAST_1</code>	Contrast level 1.
<code>SLCDC_CONTRAST_2</code>	Contrast level 2.
<code>SLCDC_CONTRAST_3</code>	Contrast level 3.
<code>SLCDC_CONTRAST_4</code>	Contrast level 4.
<code>SLCDC_CONTRAST_5</code>	Contrast level 5.
<code>SLCDC_CONTRAST_6</code>	Contrast level 6.
<code>SLCDC_CONTRAST_7</code>	Contrast level 7.
<code>SLCDC_CONTRAST_8</code>	Contrast level 8.
<code>SLCDC_CONTRAST_9</code>	Contrast level 9.
<code>SLCDC_CONTRAST_10</code>	Contrast level 10.
<code>SLCDC_CONTRAST_11</code>	Contrast level 11.
<code>SLCDC_CONTRAST_12</code>	Contrast level 12.
<code>SLCDC_CONTRAST_13</code>	Contrast level 13.
<code>SLCDC_CONTRAST_14</code>	Contrast level 14.
<code>SLCDC_CONTRAST_15</code>	Contrast level 15.

◆ **slcdc\_display\_on\_off\_t**

enum <code>slcdc_display_on_off_t</code>	
LCD Display Enable/Disable	
Enumerator	
SLCDC_DISP_OFF	Display off.
SLCDC_DISP_ON	Display on.

◆ **slcdc\_display\_enable\_disable\_t**

enum <code>slcdc_display_enable_disable_t</code>	
LCD Display output enable	
Enumerator	
SLCDC_DISP_DISABLE	Output ground level to segment/common pins.
SLCDC_DISP_ENABLE	Output enable.

◆ **slcdc\_display\_clock\_t**

enum <code>slcdc_display_clock_t</code>	
LCD Display clock selection	
Enumerator	
SLCDC_CLOCK_LOCO	Display clock source LOCO.
SLCDC_CLOCK_SOSC	Display clock source SOSC.
SLCDC_CLOCK_MOSC	Display clock source MOSC.
SLCDC_CLOCK_HOCO	Display clock source HOCO.

◆ **slcdc\_clk\_div\_t**

enum <code>slcdc_clk_div_t</code>	
LCD clock settings	
Enumerator	
SLCDC_CLK_DIVISOR_LOCO_4	LOCO Clock/4.

SLCDC_CLK_DIVISOR_LOCO_8	LOCO Clock/8.
SLCDC_CLK_DIVISOR_LOCO_16	LOCO Clock/16.
SLCDC_CLK_DIVISOR_LOCO_32	LOCO Clock/32.
SLCDC_CLK_DIVISOR_LOCO_64	LOCO Clock/64.
SLCDC_CLK_DIVISOR_LOCO_128	LOCO Clock/128.
SLCDC_CLK_DIVISOR_LOCO_256	LOCO Clock/256.
SLCDC_CLK_DIVISOR_LOCO_512	LOCO Clock/512.
SLCDC_CLK_DIVISOR_LOCO_1024	LOCO Clock/1024.
SLCDC_CLK_DIVISOR_HOCO_256	HOCO Clock/256.
SLCDC_CLK_DIVISOR_HOCO_512	HOCO Clock/512.
SLCDC_CLK_DIVISOR_HOCO_1024	HOCO Clock/1024.
SLCDC_CLK_DIVISOR_HOCO_2048	HOCO Clock/2048.
SLCDC_CLK_DIVISOR_HOCO_4096	HOCO Clock/4096.
SLCDC_CLK_DIVISOR_HOCO_8192	HOCO Clock/8192.
SLCDC_CLK_DIVISOR_HOCO_16384	HOCO Clock/16384.
SLCDC_CLK_DIVISOR_HOCO_32768	HOCO Clock/32768.
SLCDC_CLK_DIVISOR_HOCO_65536	HOCO Clock/65536.
SLCDC_CLK_DIVISOR_HOCO_131072	HOCO Clock/131072.
SLCDC_CLK_DIVISOR_HOCO_262144	HOCO Clock/262144.
SLCDC_CLK_DIVISOR_HOCO_524288	HOCO Clock/524288.

### 4.3.31 SPI Interface

#### [Interfaces](#)

## Detailed Description

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Interface for SPI communications.

## Summary

Provides a common interface for communication using the SPI Protocol.

Implemented by:

- [Serial Peripheral Interface \(r\\_spi\)](#)
- [Serial Communications Interface \(SCI\) SPI \(r\\_sci\\_spi\)](#)

## Data Structures

---

struct [spi\\_callback\\_args\\_t](#)

struct [spi\\_write\\_read\\_guard\\_args\\_t](#)

struct [spi\\_cfg\\_t](#)

struct [spi\\_api\\_t](#)

struct [spi\\_instance\\_t](#)

## Typedefs

---

typedef void [spi\\_ctrl\\_t](#)

## Enumerations

---

enum [spi\\_bit\\_width\\_t](#)

enum [spi\\_mode\\_t](#)

enum [spi\\_clk\\_phase\\_t](#)

enum [spi\\_clk\\_polarity\\_t](#)

enum [spi\\_mode\\_fault\\_t](#)

enum [spi\\_bit\\_order\\_t](#)

enum [spi\\_event\\_t](#)

## Data Structure Documentation

---

### ◆ [spi\\_callback\\_args\\_t](#)

struct [spi\\_callback\\_args\\_t](#)

Common callback parameter definition

Data Fields		
uint32_t	channel	Device channel number.
<a href="#">spi_event_t</a>	event	Event code.
void const *	p_context	Context provided to user during callback.

#### ◆ [spi\\_write\\_read\\_guard\\_args\\_t](#)

struct <a href="#">spi_write_read_guard_args_t</a>
Non-secure arguments for write-read guard function

#### ◆ [spi\\_cfg\\_t](#)

struct <a href="#">spi_cfg_t</a>	
SPI interface configuration	
<b>Data Fields</b>	
uint8_t	<a href="#">channel</a>
	Channel number to be used.
IRQn_Type	<a href="#">rx_irq</a>
	Receive Buffer Full IRQ number.
IRQn_Type	<a href="#">tx_irq</a>
	Transmit Buffer Empty IRQ number.
IRQn_Type	<a href="#">tei_irq</a>
	Transfer Complete IRQ number.
IRQn_Type	<a href="#">eri_irq</a>
	Error IRQ number.
uint8_t	<a href="#">rx_ipl</a>
	Receive Interrupt priority.

uint8_t	<a href="#">txi_ipl</a>
	Transmit Interrupt priority.
uint8_t	<a href="#">tei_ipl</a>
	Transfer Complete Interrupt priority.
uint8_t	<a href="#">eri_ipl</a>
	Error Interrupt priority.
spi_mode_t	<a href="#">operating_mode</a>
	Select master or slave operating mode.
spi_clk_phase_t	<a href="#">clk_phase</a>
	Data sampling on odd or even clock edge.
spi_clk_polarity_t	<a href="#">clk_polarity</a>
	Clock level when idle.
spi_mode_fault_t	<a href="#">mode_fault</a>
	Mode fault error (master/slave conflict) flag.
spi_bit_order_t	<a href="#">bit_order</a>
	Select to transmit MSB/LSB first.
<a href="#">transfer_instance_t</a> const *	<a href="#">p_transfer_tx</a>
	To use SPI DTC/DMA write transfer, link a DTC/DMA instance here. Set to NULL if unused.

<code>transfer_instance_t</code> const *	<code>p_transfer_rx</code>
	To use SPI DTC/DMA read transfer, link a DTC/DMA instance here. Set to NULL if unused.
void(*	<code>p_callback</code> )(spi_callback_args_t *p_args)
	Pointer to user callback function.
void const *	<code>p_context</code>
	User defined context passed to callback function.
void const *	<code>p_extend</code>
	Extended SPI hardware dependent configuration.

◆ **spi\_api\_t**

struct spi_api_t	
Shared Interface definition for SPI	
<b>Data Fields</b>	
<code>fsp_err_t</code> (*	<code>open</code> )(spi_ctrl_t *p_ctrl, spi_cfg_t const *const p_cfg)
<code>fsp_err_t</code> (*	<code>read</code> )(spi_ctrl_t *const p_ctrl, void *p_dest, uint32_t const length, spi_bit_width_t const bit_width)
<code>fsp_err_t</code> (*	<code>write</code> )(spi_ctrl_t *const p_ctrl, void const *p_src, uint32_t const length, spi_bit_width_t const bit_width)
<code>fsp_err_t</code> (*	<code>writeRead</code> )(spi_ctrl_t *const p_ctrl, void const *p_src, void *p_dest, uint32_t const length, spi_bit_width_t const bit_width)
<code>fsp_err_t</code> (*	<code>callbackSet</code> )(spi_ctrl_t *const p_api_ctrl, void(*p_callback)(spi_callback_args_t *), void const *const p_context, spi_callback_args_t *const p_callback_memory)

<code>fsp_err_t(*</code>	<code>close )(spi_ctrl_t *const p_ctrl)</code>
--------------------------	------------------------------------------------

<code>fsp_err_t(*</code>	<code>versionGet )(fsp_version_t *p_version)</code>
--------------------------	-----------------------------------------------------

## Field Documentation

### ◆ open

<code>fsp_err_t(* spi_api_t::open) (spi_ctrl_t *p_ctrl, spi_cfg_t const *const p_cfg)</code>
----------------------------------------------------------------------------------------------

Initialize a channel for SPI communication mode.

### Implemented as

- [R\\_SPI\\_Open\(\)](#)
- [R\\_SCI\\_SPI\\_Open\(\)](#)

### Parameters

[in,out]	p_ctrl	Pointer to user-provided storage for the control block.
[in]	p_cfg	Pointer to SPI configuration structure.



## ◆ read

```
fsp_err_t(* spi_api_t::read) (spi_ctrl_t *const p_ctrl, void *p_dest, uint32_t const length,
spi_bit_width_t const bit_width)
```

Receive data from a SPI device.

**Implemented as**

- R\_SPI\_Read()
- R\_SCI\_SPI\_Read()

**Parameters**

[in]	p_ctrl	Pointer to the control block for the channel.
[in]	length	Number of units of data to be transferred (unit size specified by the bit_width).
[in]	bit_width	Data bit width to be transferred.
[out]	p_dest	Pointer to destination buffer into which data will be copied that is received from a SPI device. It is the responsibility of the caller to ensure that adequate space is available to hold the requested data count.

◆ **write**

```
fsp_err_t(* spi_api_t::write) (spi_ctrl_t *const p_ctrl, void const *p_src, uint32_t const length,
spi_bit_width_t const bit_width)
```

Transmit data to a SPI device.

**Implemented as**

- R\_SPI\_Write()
- R\_SCI\_SPI\_Write()

**Parameters**

[in]	p_ctrl	Pointer to the control block for the channel.
[in]	p_src	Pointer to a source data buffer from which data will be transmitted to a SPI device. The argument must not be NULL.
[in]	length	Number of units of data to be transferred (unit size specified by the bit_width).
[in]	bit_width	Data bit width to be transferred.

◆ **writeRead**

```
fsp_err_t(* spi_api_t::writeRead) (spi_ctrl_t *const p_ctrl, void const *p_src, void *p_dest, uint32_t
const length, spi_bit_width_t const bit_width)
```

Simultaneously transmit data to a SPI device while receiving data from a SPI device (full duplex).

**Implemented as**

- R\_SPI\_WriteRead()
- R\_SCI\_SPI\_WriteRead()

**Parameters**

[in]	p_ctrl	Pointer to the control block for the channel.
[in]	p_src	Pointer to a source data buffer from which data will be transmitted to a SPI device. The argument must not be NULL.
[out]	p_dest	Pointer to destination buffer into which data will be copied that is received from a SPI device. It is the responsibility of the caller to ensure that adequate space is available to hold the requested data count. The argument must not be NULL.
[in]	length	Number of units of data to be transferred (unit size specified by the bit_width).
[in]	bit_width	Data bit width to be transferred.

◆ **callbackSet**

```
fsp_err_t(* spi_api_t::callbackSet) (spi_ctrl_t *const p_api_ctrl, void(*p_callback)(spi_callback_args_t *), void const *const p_context, spi_callback_args_t *const p_callback_memory)
```

Specify callback function and optional context pointer and working memory pointer.

**Implemented as**

- R\_SCI\_SPI\_CallbackSet()

**Parameters**

[in]	p_ctrl	Pointer to the SPI control block.
[in]	p_callback	Callback function
[in]	p_context	Pointer to send to callback function
[in]	p_working_memory	Pointer to volatile memory where callback structure can be allocated. Callback arguments allocated here are only valid during the callback.

◆ **close**

```
fsp_err_t(* spi_api_t::close) (spi_ctrl_t *const p_ctrl)
```

Remove power to the SPI channel designated by the handle and disable the associated interrupts.

**Implemented as**

- R\_SPI\_Close()
- R\_SCI\_SPI\_Close()

**Parameters**

[in]	p_ctrl	Pointer to the control block for the channel.
------	--------	-----------------------------------------------

◆ **versionGet**

```
fsp_err_t(* spi_api_t::versionGet) (fsp_version_t *p_version)
```

Get the version information of the underlying driver.

**Implemented as**

- R\_SPI\_VersionGet()
- R\_SCI\_SPI\_VersionGet()

**Parameters**

[out]	p_version	pointer to memory location to return version number
-------	-----------	-----------------------------------------------------

◆ **spi\_instance\_t**

```
struct spi_instance_t
```

This structure encompasses everything that is needed to use an instance of this interface.

## Data Fields

<code>spi_ctrl_t *</code>	p_ctrl	Pointer to the control structure for this instance.
<code>spi_cfg_t const *</code>	p_cfg	Pointer to the configuration structure for this instance.
<code>spi_api_t const *</code>	p_api	Pointer to the API structure for this instance.

**Typedef Documentation**◆ **spi\_ctrl\_t**

```
typedef void spi_ctrl_t
```

SPI control block. Allocate an instance specific control block to pass into the SPI API calls.

**Implemented as**

- sci\_spi\_instance\_ctrl\_t
- spi\_instance\_ctrl\_t

**Enumeration Type Documentation**

◆ **spi\_bit\_width\_t**

enum <code>spi_bit_width_t</code>	
Data bit width	
Enumerator	
<code>SPI_BIT_WIDTH_8_BITS</code>	Data bit width is 8 bits byte.
<code>SPI_BIT_WIDTH_16_BITS</code>	Data bit width is 16 bits word.
<code>SPI_BIT_WIDTH_32_BITS</code>	Data bit width is 32 bits long word.

◆ **spi\_mode\_t**

enum <code>spi_mode_t</code>	
Master or slave operating mode	
Enumerator	
<code>SPI_MODE_MASTER</code>	Channel operates as SPI master.
<code>SPI_MODE_SLAVE</code>	Channel operates as SPI slave.

◆ **spi\_clk\_phase\_t**

enum <code>spi_clk_phase_t</code>	
Clock phase	
Enumerator	
<code>SPI_CLK_PHASE_EDGE_ODD</code>	0: Data sampling on odd edge, data variation on even edge
<code>SPI_CLK_PHASE_EDGE_EVEN</code>	1: Data variation on odd edge, data sampling on even edge

◆ **spi\_clk\_polarity\_t**

enum <code>spi_clk_polarity_t</code>	
Clock polarity	
Enumerator	
<code>SPI_CLK_POLARITY_LOW</code>	0: Clock polarity is low when idle
<code>SPI_CLK_POLARITY_HIGH</code>	1: Clock polarity is high when idle

◆ **spi\_mode\_fault\_t**

enum <code>spi_mode_fault_t</code>	
Mode fault error flag. This error occurs when the device is setup as a master, but the SS/SA line does not seem to be controlled by the master. This usually happens when the connecting device is also acting as master. A similar situation can also happen when configured as a slave.	
Enumerator	
<code>SPI_MODE_FAULT_ERROR_ENABLE</code>	Mode fault error flag on.
<code>SPI_MODE_FAULT_ERROR_DISABLE</code>	Mode fault error flag off.

◆ **spi\_bit\_order\_t**

enum <code>spi_bit_order_t</code>	
Bit order	
Enumerator	
<code>SPI_BIT_ORDER_MSB_FIRST</code>	Send MSB first in transmission.
<code>SPI_BIT_ORDER_LSB_FIRST</code>	Send LSB first in transmission.

◆ **spi\_event\_t**

enum <code>spi_event_t</code>	
SPI events	
Enumerator	
<code>SPI_EVENT_TRANSFER_COMPLETE</code>	The data transfer was completed.
<code>SPI_EVENT_TRANSFER_ABORTED</code>	The data transfer was aborted.
<code>SPI_EVENT_ERR_MODE_FAULT</code>	Mode fault error.
<code>SPI_EVENT_ERR_READ_OVERFLOW</code>	Read overflow error.
<code>SPI_EVENT_ERR_PARITY</code>	Parity error.
<code>SPI_EVENT_ERR_OVERRUN</code>	Overrun error.
<code>SPI_EVENT_ERR_FRAMING</code>	Framing error.
<code>SPI_EVENT_ERR_MODE_UNDERRUN</code>	Underrun error.

**4.3.32 SPI Flash Interface**[Interfaces](#)**Detailed Description**

Interface for accessing external SPI flash devices.

**Summary**

The SPI flash API provides an interface that configures, writes, and erases sectors in SPI flash devices.

Implemented by:

- [Octa Serial Peripheral Interface Flash \(r\\_osp\\_i\)](#)
- [Quad Serial Peripheral Interface Flash \(r\\_qs\\_p\\_i\)](#)

**Data Structures**

```
struct spi_flash_erase_command_t
```

```
struct spi_flash_cfg_t
```



struct [spi\\_flash\\_status\\_t](#)

struct [spi\\_flash\\_api\\_t](#)

struct [spi\\_flash\\_instance\\_t](#)

## Typedefs

typedef void [spi\\_flash\\_ctrl\\_t](#)

## Enumerations

enum [spi\\_flash\\_read\\_mode\\_t](#)

enum [spi\\_flash\\_protocol\\_t](#)

enum [spi\\_flash\\_address\\_bytes\\_t](#)

enum [spi\\_flash\\_data\\_lines\\_t](#)

enum [spi\\_flash\\_dummy\\_clocks\\_t](#)

enum [spi\\_flash\\_direct\\_transfer\\_dir\\_t](#)

## Data Structure Documentation

### ◆ [spi\\_flash\\_erase\\_command\\_t](#)

struct <a href="#">spi_flash_erase_command_t</a>		
Structure to define an erase command and associated erase size.		
Data Fields		
uint16_t	command	Erase command.
uint32_t	size	Size of erase for associated command, set to <code>SPI_FLASH_ERASE_SIZE_CHIP_ERASE</code> for chip erase.

### ◆ [spi\\_flash\\_cfg\\_t](#)

struct <a href="#">spi_flash_cfg_t</a>		
User configuration structure used by the open function		
Data Fields		
<a href="#">spi_flash_protocol_t</a>	spi_protocol	Initial SPI protocol. SPI protocol can be changed in <a href="#">spi_flash_api_t::spiProtocolSet</a> .
<a href="#">spi_flash_read_mode_t</a>	read_mode	Read mode.

<a href="#">spi_flash_address_bytes_t</a>	address_bytes	Number of bytes used to represent the address.
<a href="#">spi_flash_dummy_clocks_t</a>	dummy_clocks	Number of dummy clocks to use for fast read operations.
<a href="#">spi_flash_data_lines_t</a>	page_program_address_lines	Number of lines used to send address for page program command. This should either be 1 or match the number of lines used in the selected read mode.
uint8_t	write_status_bit	Which bit determines write status.
uint8_t	write_enable_bit	Which bit determines write status.
uint32_t	page_size_bytes	Page size in bytes (maximum number of bytes for page program)
uint8_t	page_program_command	Page program command.
uint8_t	write_enable_command	Command to enable write or erase, typically 0x06.
uint8_t	status_command	Command to read the write status.
uint8_t	read_command	Read command - OSPI SPI mode only.
uint8_t	xip_enter_command	Command to enter XIP mode.
uint8_t	xip_exit_command	Command to exit XIP mode.
uint8_t	erase_command_list_length	Length of erase command list.
<a href="#">spi_flash_erase_command_t</a> const *	p_erase_command_list	List of all erase commands and associated sizes.
void const *	p_extend	Pointer to implementation specific extended configurations.

#### ◆ spi\_flash\_status\_t

struct spi_flash_status_t		
Status.		
Data Fields		
bool	write_in_progress	Whether or not a write is in progress. This is determined by reading the <a href="#">spi_flash_cfg_t::write_status_bit</a> from the <a href="#">spi_flash_cfg_t::status_comman</a>

d.

## ◆ spi\_flash\_api\_t

struct spi\_flash\_api\_t

SPI flash implementations follow this API.

**Data Fields**

fsp_err_t(*)	open )(spi_flash_ctrl_t *p_ctrl, spi_flash_cfg_t const *const p_cfg)
fsp_err_t(*)	directWrite )(spi_flash_ctrl_t *p_ctrl, uint8_t const *const p_src, uint32_t const bytes, bool const read_after_write)
fsp_err_t(*)	directRead )(spi_flash_ctrl_t *p_ctrl, uint8_t *const p_dest, uint32_t const bytes)
fsp_err_t(*)	directTransfer )(spi_flash_ctrl_t *p_ctrl, spi_flash_direct_transfer_t *const p_transfer, spi_flash_direct_transfer_dir_t direction)
fsp_err_t(*)	spiProtocolSet )(spi_flash_ctrl_t *p_ctrl, spi_flash_protocol_t spi_protocol)
fsp_err_t(*)	write )(spi_flash_ctrl_t *p_ctrl, uint8_t const *const p_src, uint8_t *const p_dest, uint32_t byte_count)
fsp_err_t(*)	erase )(spi_flash_ctrl_t *p_ctrl, uint8_t *const p_device_address, uint32_t byte_count)
fsp_err_t(*)	statusGet )(spi_flash_ctrl_t *p_ctrl, spi_flash_status_t *const p_status)
fsp_err_t(*)	xipEnter )(spi_flash_ctrl_t *p_ctrl)
fsp_err_t(*)	xipExit )(spi_flash_ctrl_t *p_ctrl)
fsp_err_t(*)	bankSet )(spi_flash_ctrl_t *p_ctrl, uint32_t bank)
fsp_err_t(*)	close )(spi_flash_ctrl_t *p_ctrl)
fsp_err_t(*)	versionGet )(fsp_version_t *const p_version)

## Field Documentation

### ◆ open

`fsp_err_t(* spi_flash_api_t::open) (spi_flash_ctrl_t *p_ctrl, spi_flash_cfg_t const *const p_cfg)`

Open the SPI flash driver module.

#### Implemented as

- [R\\_QSPI\\_Open\(\)](#)

#### Parameters

[in]	p_ctrl	Pointer to a driver handle
[in]	p_cfg	Pointer to a configuration structure

### ◆ directWrite

`fsp_err_t(* spi_flash_api_t::directWrite) (spi_flash_ctrl_t *p_ctrl, uint8_t const *const p_src, uint32_t const bytes, bool const read_after_write)`

Write raw data to the SPI flash.

#### Implemented as

- [R\\_QSPI\\_DirectWrite\(\)](#)

#### Parameters

[in]	p_ctrl	Pointer to a driver handle
[in]	p_src	Pointer to raw data to write, must include any required command/address
[in]	bytes	Number of bytes to write
[in]	read_after_write	If true, the slave select remains asserted and the peripheral does not return to direct communications mode. If false, the slave select is deasserted and memory mapped access is possible after this function returns if the device is not busy.

◆ **directRead**

```
fsp_err_t(* spi_flash_api_t::directRead) (spi_flash_ctrl_t *p_ctrl, uint8_t *const p_dest, uint32_t const bytes)
```

Read raw data from the SPI flash. Must follow a call to [spi\\_flash\\_api\\_t::directWrite](#).

**Implemented as**

- [R\\_QSPI\\_DirectRead\(\)](#)

**Parameters**

[in]	p_ctrl	Pointer to a driver handle
[out]	p_dest	Pointer to read raw data into
[in]	bytes	Number of bytes to read

◆ **directTransfer**

```
fsp_err_t(* spi_flash_api_t::directTransfer) (spi_flash_ctrl_t *p_ctrl, spi_flash_direct_transfer_t *const p_transfer, spi_flash_direct_transfer_dir_t direction)
```

Direct Read/Write raw data to the SPI flash.

**Implemented as**

- [R\\_OSPI\\_DirectTransfer\(\)](#)

**Parameters**

[in]	p_ctrl	Pointer to a driver handle
[in]	p_data	Pointer to command, address and data values and lengths
[in]	direction	Direct Read/Write

◆ **spiProtocolSet**

```
fsp_err_t(* spi_flash_api_t::spiProtocolSet) (spi_flash_ctrl_t *p_ctrl, spi_flash_protocol_t spi_protocol)
```

Change the SPI protocol in the driver. The application must change the SPI protocol on the device.

**Implemented as**

- [R\\_QSPI\\_SpiProtocolSet\(\)](#)

**Parameters**

[in]	p_ctrl	Pointer to a driver handle
[in]	spi_protocol	Desired SPI protocol

◆ **write**

```
fsp_err_t(* spi_flash_api_t::write) (spi_flash_ctrl_t *p_ctrl, uint8_t const *const p_src, uint8_t *const p_dest, uint32_t byte_count)
```

Program a page of data to the flash.

**Implemented as**

- R\_QSPI\_Write()

**Parameters**

[in]	p_ctrl	Pointer to a driver handle
[in]	p_src	The memory address of the data to write to the flash device
[in]	p_dest	The location in the flash device address space to write the data to
[in]	byte_count	The number of bytes to write

◆ **erase**

```
fsp_err_t(* spi_flash_api_t::erase) (spi_flash_ctrl_t *p_ctrl, uint8_t *const p_device_address, uint32_t byte_count)
```

Erase a certain number of bytes of the flash.

**Implemented as**

- R\_QSPI\_Erase()

**Parameters**

[in]	p_ctrl	Pointer to a driver handle
[in]	p_device_address	The location in the flash device address space to start the erase from
[in]	byte_count	The number of bytes to erase. Set to SPI_FLASH_ERASE_SIZE_CHIP_ERASE to erase entire chip.

**◆ statusGet**

```
fsp_err_t(* spi_flash_api_t::statusGet) (spi_flash_ctrl_t *p_ctrl, spi_flash_status_t *const p_status)
```

Get the write or erase status of the flash.

**Implemented as**

- R\_QSPI\_StatusGet()

**Parameters**

[in]	p_ctrl	Pointer to a driver handle
[out]	p_status	Current status of the SPI flash device stored here.

**◆ xipEnter**

```
fsp_err_t(* spi_flash_api_t::xipEnter) (spi_flash_ctrl_t *p_ctrl)
```

Enter XIP mode.

**Implemented as**

- R\_QSPI\_XipEnter()

**Parameters**

[in]	p_ctrl	Pointer to a driver handle
------	--------	----------------------------

**◆ xipExit**

```
fsp_err_t(* spi_flash_api_t::xipExit) (spi_flash_ctrl_t *p_ctrl)
```

Exit XIP mode.

**Implemented as**

- R\_QSPI\_XipExit()

**Parameters**

[in]	p_ctrl	Pointer to a driver handle
------	--------	----------------------------

◆ **bankSet**

```
fsp_err_t(* spi_flash_api_t::bankSet) (spi_flash_ctrl_t *p_ctrl, uint32_t bank)
```

Select the bank to access. See implementation for details.

**Implemented as**

- [R\\_QSPI\\_BankSet\(\)](#)

**Parameters**

[in]	p_ctrl	Pointer to a driver handle
[in]	bank	The bank number

◆ **close**

```
fsp_err_t(* spi_flash_api_t::close) (spi_flash_ctrl_t *p_ctrl)
```

Close the SPI flash driver module.

**Implemented as**

- [R\\_QSPI\\_Close\(\)](#)

**Parameters**

[in]	p_ctrl	Pointer to a driver handle
------	--------	----------------------------

◆ **versionGet**

```
fsp_err_t(* spi_flash_api_t::versionGet) (fsp_version_t *const p_version)
```

Get the driver version based on compile time macros.

**Implemented as**

- [R\\_QSPI\\_VersionGet\(\)](#)

**Parameters**

[out]	p_version	Code and API version stored here.
-------	-----------	-----------------------------------

◆ **spi\_flash\_instance\_t**

```
struct spi_flash_instance_t
```

This structure encompasses everything that is needed to use an instance of this interface.

## Data Fields

<a href="#">spi_flash_ctrl_t</a> *	p_ctrl	Pointer to the control structure for this instance.
<a href="#">spi_flash_cfg_t</a> const *	p_cfg	Pointer to the configuration structure for this instance.



`spi_flash_api_t` const \*

p\_api

Pointer to the API structure for this instance.

## Typedef Documentation

### ◆ spi\_flash\_ctrl\_t

typedef void `spi_flash_ctrl_t`

SPI flash control block. Allocate an instance specific control block to pass into the SPI flash API calls.

#### Implemented as

- `qspi_instance_ctrl_t`

## Enumeration Type Documentation

### ◆ spi\_flash\_read\_mode\_t

enum `spi_flash_read_mode_t`

Read mode.

#### Enumerator

<code>SPI_FLASH_READ_MODE_STANDARD</code>	Standard Read Mode (no dummy cycles)
<code>SPI_FLASH_READ_MODE_FAST_READ</code>	Fast Read Mode (dummy cycles between address and data)
<code>SPI_FLASH_READ_MODE_FAST_READ_DUAL_OUTPUT</code>	Fast Read Dual Output Mode (data on 2 lines)
<code>SPI_FLASH_READ_MODE_FAST_READ_DUAL_IO</code>	Fast Read Dual I/O Mode (address and data on 2 lines)
<code>SPI_FLASH_READ_MODE_FAST_READ_QUAD_OUTPUT</code>	Fast Read Quad Output Mode (data on 4 lines)
<code>SPI_FLASH_READ_MODE_FAST_READ_QUAD_IO</code>	Fast Read Quad I/O Mode (address and data on 4 lines)

◆ **spi\_flash\_protocol\_t**

enum <code>spi_flash_protocol_t</code>	
SPI protocol.	
Enumerator	
<code>SPI_FLASH_PROTOCOL_EXTENDED_SPI</code>	Extended SPI mode (commands on 1 line)
<code>SPI_FLASH_PROTOCOL_QPI</code>	QPI mode (commands on 4 lines). Note that the application must ensure the device is in QPI mode.
<code>SPI_FLASH_PROTOCOL_SOPI</code>	SOPI mode (command and data on 8 lines). Note that the application must ensure the device is in SOPI mode.
<code>SPI_FLASH_PROTOCOL_DOPI</code>	DOPI mode (command and data on 8 lines, dual data rate). Note that the application must ensure the device is in DOPI mode.

◆ **spi\_flash\_address\_bytes\_t**

enum <code>spi_flash_address_bytes_t</code>	
Number of bytes in the address.	
Enumerator	
<code>SPI_FLASH_ADDRESS_BYTES_3</code>	3 address bytes
<code>SPI_FLASH_ADDRESS_BYTES_4</code>	4 address bytes with standard commands. If this option is selected, the application must issue the EN4B command using <code>spi_flash_api_t::directWrite()</code> if required by the device.
<code>SPI_FLASH_ADDRESS_BYTES_4_4BYTE_READ_CODE</code>	4 address bytes using standard 4-byte command set.

◆ **spi\_flash\_data\_lines\_t**

enum <code>spi_flash_data_lines_t</code>	
Number of data lines used.	
Enumerator	
<code>SPI_FLASH_DATA_LINES_1</code>	1 data line
<code>SPI_FLASH_DATA_LINES_2</code>	2 data lines
<code>SPI_FLASH_DATA_LINES_4</code>	4 data lines

## ◆ spi\_flash\_dummy\_clocks\_t

enum spi_flash_dummy_clocks_t	
Number of dummy cycles for fast read operations.	
Enumerator	
SPI_FLASH_DUMMY_CLOCKS_DEFAULT	Default is 6 clocks for Fast Read Quad I/O, 4 clocks for Fast Read Dual I/O, and 8 clocks for other fast read instructions including Fast Read Quad Output, Fast Read Dual Output, and Fast Read.
SPI_FLASH_DUMMY_CLOCKS_3	3 dummy clocks
SPI_FLASH_DUMMY_CLOCKS_4	4 dummy clocks
SPI_FLASH_DUMMY_CLOCKS_5	5 dummy clocks
SPI_FLASH_DUMMY_CLOCKS_6	6 dummy clocks
SPI_FLASH_DUMMY_CLOCKS_7	7 dummy clocks
SPI_FLASH_DUMMY_CLOCKS_8	8 dummy clocks
SPI_FLASH_DUMMY_CLOCKS_9	9 dummy clocks
SPI_FLASH_DUMMY_CLOCKS_10	10 dummy clocks
SPI_FLASH_DUMMY_CLOCKS_11	11 dummy clocks
SPI_FLASH_DUMMY_CLOCKS_12	12 dummy clocks
SPI_FLASH_DUMMY_CLOCKS_13	13 dummy clocks
SPI_FLASH_DUMMY_CLOCKS_14	14 dummy clocks
SPI_FLASH_DUMMY_CLOCKS_15	15 dummy clocks
SPI_FLASH_DUMMY_CLOCKS_16	16 dummy clocks
SPI_FLASH_DUMMY_CLOCKS_17	17 dummy clocks

### ◆ spi\_flash\_direct\_transfer\_dir\_t

enum spi_flash_direct_transfer_dir_t
--------------------------------------

Direct Read and Write direction
---------------------------------

## 4.3.33 Three-Phase Interface

### Interfaces

#### Detailed Description

Interface for three-phase timer functions.

## Summary

The Three-Phase interface provides functionality for synchronous start/stop/reset control of three timer channels for use in 3-phase motor control applications.

Implemented by:

- General PWM Timer Three-Phase Motor Control Driver (r\_gpt\_three\_phase)

#### Data Structures

struct	three_phase_duty_cycle_t
--------	--------------------------

struct	three_phase_cfg_t
--------	-------------------

struct	three_phase_api_t
--------	-------------------

struct	three_phase_instance_t
--------	------------------------

#### Typedefs

typedef void	three_phase_ctrl_t
--------------	--------------------

#### Enumerations

enum	three_phase_channel_t
------	-----------------------

enum	three_phase_buffer_mode_t
------	---------------------------

#### Data Structure Documentation

### ◆ three\_phase\_duty\_cycle\_t

struct three_phase_duty_cycle_t
---------------------------------

Struct for passing duty cycle values to <a href="#">three_phase_api_t::dutyCycleSet</a>		
Data Fields		
uint32_t	duty[3]	Duty cycle.
uint32_t	duty_buffer[3]	Double-buffer for duty cycle values.

◆ **three\_phase\_cfg\_t**

struct three_phase_cfg_t		
User configuration structure, used in open function		
Data Fields		
<a href="#">three_phase_buffer_mode_t</a>	buffer_mode	Single or double-buffer mode.
<a href="#">timer_instance_t</a> const *	p_timer_instance[3]	Pointer to the timer instance structs.
<a href="#">three_phase_channel_t</a>	callback_ch	Channel to enable callback when using <a href="#">three_phase_api_t::callbackSet</a> .
uint32_t	channel_mask	Bitmask of timer channels used by this module.
void const *	p_context	Placeholder for user data. Passed to the user callback in <a href="#">timer_callback_args_t</a> .
void const *	p_extend	Extension parameter for hardware specific settings.

◆ **three\_phase\_api\_t**

struct three_phase_api_t		
Three-Phase API structure.		
<b>Data Fields</b>		
<a href="#">fsp_err_t</a> (*	<a href="#">open</a> )( <a href="#">three_phase_ctrl_t</a> *const p_ctrl, <a href="#">three_phase_cfg_t</a> const *const p_cfg)	
<a href="#">fsp_err_t</a> (*	<a href="#">start</a> )( <a href="#">three_phase_ctrl_t</a> *const p_ctrl)	
<a href="#">fsp_err_t</a> (*	<a href="#">stop</a> )( <a href="#">three_phase_ctrl_t</a> *const p_ctrl)	
<a href="#">fsp_err_t</a> (*	<a href="#">reset</a> )( <a href="#">three_phase_ctrl_t</a> *const p_ctrl)	
<a href="#">fsp_err_t</a> (*	<a href="#">dutyCycleSet</a> )( <a href="#">three_phase_ctrl_t</a> *const p_ctrl, <a href="#">three_phase_duty_cycle_t</a> *const p_duty_cycle)	

<code>fsp_err_t(*</code>	<code>callbackSet )(three_phase_ctrl_t *const p_api_ctrl, void(*p_callback)(timer_callback_args_t *), void const *const p_context, timer_callback_args_t *const p_callback_memory)</code>
<code>fsp_err_t(*</code>	<code>close )(three_phase_ctrl_t *const p_ctrl)</code>
<code>fsp_err_t(*</code>	<code>versionGet )(fsp_version_t *const p_version)</code>

## Field Documentation

### ◆ open

`fsp_err_t(* three_phase_api_t::open) (three_phase_ctrl_t *const p_ctrl, three_phase_cfg_t const *const p_cfg)`

Initial configuration.

#### Implemented as

- `R_GPT_THREE_PHASE_Open()`

#### Parameters

[in]	<code>p_ctrl</code>	Pointer to control block. Must be declared by user. Elements set here.
[in]	<code>p_cfg</code>	Pointer to configuration structure. All elements of this structure must be set by user.

### ◆ start

`fsp_err_t(* three_phase_api_t::start) (three_phase_ctrl_t *const p_ctrl)`

Start all three timers synchronously.

#### Implemented as

- `R_GPT_THREE_PHASE_Start()`

#### Parameters

[in]	<code>p_ctrl</code>	Control block set in <code>three_phase_api_t::open</code> call for this timer.
------	---------------------	--------------------------------------------------------------------------------

## ◆ stop

```
fsp_err_t(* three_phase_api_t::stop) (three_phase_ctrl_t *const p_ctrl)
```

Stop all three timers synchronously.

**Implemented as**

- [R\\_GPT\\_THREE\\_PHASE\\_Stop\(\)](#)

**Parameters**

[in]	p_ctrl	Control block set in <a href="#">three_phase_api_t::open</a> call for this timer.
------	--------	-----------------------------------------------------------------------------------

## ◆ reset

```
fsp_err_t(* three_phase_api_t::reset) (three_phase_ctrl_t *const p_ctrl)
```

Reset all three timers synchronously.

**Implemented as**

- [R\\_GPT\\_THREE\\_PHASE\\_Reset\(\)](#)

**Parameters**

[in]	p_ctrl	Control block set in <a href="#">three_phase_api_t::open</a> call for this timer.
------	--------	-----------------------------------------------------------------------------------

## ◆ dutyCycleSet

```
fsp_err_t(* three_phase_api_t::dutyCycleSet) (three_phase_ctrl_t *const p_ctrl,  
three_phase_duty_cycle_t *const p_duty_cycle)
```

Sets the duty cycle match values. If the timer is counting, the updated duty cycle is reflected after the next timer expiration.

**Implemented as**

- [R\\_GPT\\_THREE\\_PHASE\\_DutyCycleSet\(\)](#)

**Parameters**

[in]	p_ctrl	Control block set in <a href="#">three_phase_api_t::open</a> call for this timer.
[in]	p_duty_cycle	Duty cycle values for all three timer channels.



### ◆ callbackSet

```
fsp_err_t(* three_phase_api_t::callbackSet) (three_phase_ctrl_t *const p_api_ctrl,
void(*p_callback)(timer_callback_args_t *), void const *const p_context, timer_callback_args_t
*const p_callback_memory)
```

Specify callback function and optional context pointer and working memory pointer.

#### Implemented as

- R\_GPT\_THREE\_PHASE\_CallbackSet()

#### Parameters

[in]	p_ctrl	Control block set in <a href="#">three_phase_api_t::open</a> call.
[in]	p_callback	Callback function to register with GPT U-channel
[in]	p_context	Pointer to send to callback function
[in]	p_working_memory	Pointer to volatile memory where callback structure can be allocated. Callback arguments allocated here are only valid during the callback.

### ◆ close

```
fsp_err_t(* three_phase_api_t::close) (three_phase_ctrl_t *const p_ctrl)
```

Allows driver to be reconfigured and may reduce power consumption.

#### Implemented as

- R\_GPT\_THREE\_PHASE\_Close()

#### Parameters

[in]	p_ctrl	Control block set in <a href="#">three_phase_api_t::open</a> call for this timer.
------	--------	-----------------------------------------------------------------------------------

◆ **versionGet**

```
fsp_err_t(* three_phase_api_t::versionGet) (fsp_version_t *const p_version)
```

Get version and store it in provided pointer p\_version.

**Implemented as**

- [R\\_GPT\\_THREE\\_PHASE\\_VersionGet\(\)](#)

**Parameters**

[out]	p_version	Code and API version used.
-------	-----------	----------------------------

◆ **three\_phase\_instance\_t**

```
struct three_phase_instance_t
```

This structure encompasses everything that is needed to use an instance of this interface.

## Data Fields

<a href="#">three_phase_ctrl_t</a> *	p_ctrl	Pointer to the control structure for this instance.
<a href="#">three_phase_cfg_t</a> const *	p_cfg	Pointer to the configuration structure for this instance.
<a href="#">three_phase_api_t</a> const *	p_api	Pointer to the API structure for this instance.

**Typedef Documentation**◆ **three\_phase\_ctrl\_t**

```
typedef void three_phase_ctrl_t
```

Three-Phase control block. Allocate an instance specific control block to pass into the timer API calls.

**Implemented as**

- [gpt\\_three\\_phase\\_instance\\_ctrl\\_t](#)

**Enumeration Type Documentation**

◆ **three\_phase\_channel\_t**

enum <code>three_phase_channel_t</code>	
Timer channel indices	
Enumerator	
<code>THREE_PHASE_CHANNEL_U</code>	U-channel index.
<code>THREE_PHASE_CHANNEL_V</code>	V-channel index.
<code>THREE_PHASE_CHANNEL_W</code>	W-channel index.

◆ **three\_phase\_buffer\_mode\_t**

enum <code>three_phase_buffer_mode_t</code>	
Buffering mode	
Enumerator	
<code>THREE_PHASE_BUFFER_MODE_SINGLE</code>	Single-buffer mode.
<code>THREE_PHASE_BUFFER_MODE_DOUBLE</code>	Double-buffer mode.

## 4.3.34 Timer Interface

### Interfaces

#### Detailed Description

Interface for timer functions.

## Summary

The general timer interface provides standard timer functionality including periodic mode, one-shot mode, PWM output, and free-running timer mode. After each timer cycle (overflow or underflow), an interrupt can be triggered.

If an instance supports output compare mode, it is provided in the extension configuration `timer_on_<instance>_cfg_t` defined in `r_<instance>.h`.

Implemented by:

- [General PWM Timer \(`r\_gpt`\)](#)
- [Asynchronous General Purpose Timer \(`r\_agt`\)](#)

## Data Structures

struct [timer\\_callback\\_args\\_t](#)

struct [timer\\_info\\_t](#)

struct [timer\\_status\\_t](#)

struct [timer\\_cfg\\_t](#)

struct [timer\\_api\\_t](#)

struct [timer\\_instance\\_t](#)

## Typedefs

typedef void [timer\\_ctrl\\_t](#)

## Enumerations

enum [timer\\_event\\_t](#)

enum [timer\\_variant\\_t](#)

enum [timer\\_state\\_t](#)

enum [timer\\_mode\\_t](#)

enum [timer\\_direction\\_t](#)

enum [timer\\_source\\_div\\_t](#)

## Data Structure Documentation

### ◆ timer\_callback\_args\_t

struct timer_callback_args_t		
Callback function parameter data		
Data Fields		
void const *	p_context	Placeholder for user data. Set in <a href="#">timer_api_t::open</a> function in <a href="#">timer_cfg_t</a> .
<a href="#">timer_event_t</a>	event	The event can be used to identify what caused the callback.
uint32_t	capture	Most recent capture, only valid if event is <a href="#">TIMER_EVENT_CAPTURE_A</a> or <a href="#">TIMER_EVENT_CAPTURE_B</a> .

◆ **timer\_info\_t**

struct timer_info_t		
Timer information structure to store various information for a timer resource		
Data Fields		
<a href="#">timer_direction_t</a>	count_direction	Clock counting direction of the timer.
uint32_t	clock_frequency	Clock frequency of the timer counter.
uint32_t	period_counts	Period in raw timer counts.  <i>Note</i> <i>For triangle wave PWM modes, the full period is double this value.</i>

◆ **timer\_status\_t**

struct timer_status_t		
Current timer status.		
Data Fields		
uint32_t	counter	Current counter value.
<a href="#">timer_state_t</a>	state	Current timer state (running or stopped)

◆ **timer\_cfg\_t**

struct timer_cfg_t		
User configuration structure, used in open function		
<b>Data Fields</b>		
<a href="#">timer_mode_t</a>	mode	
		Select enumerated value from <a href="#">timer_mode_t</a> .
uint32_t	<a href="#">period_counts</a>	
		Period in raw timer counts.
<a href="#">timer_source_div_t</a>	source_div	
		Source clock divider.
uint32_t	<a href="#">duty_cycle_counts</a>	

	Duty cycle in counts.
uint8_t	channel
uint8_t	cycle_end_ipr
	Cycle end interrupt priority.
IRQn_Type	cycle_end_irq
	Cycle end interrupt.
void(*	p_callback)(timer_callback_args_t *p_args)
void const *	p_context
void const *	p_extend
	Extension parameter for hardware specific settings.

## Field Documentation

### ◆ channel

uint8\_t timer\_cfg\_t::channel

Select a channel corresponding to the channel number of the hardware.

### ◆ p\_callback

void(\* timer\_cfg\_t::p\_callback)(timer\_callback\_args\_t \*p\_args)

Callback provided when a timer ISR occurs. Set to NULL for no CPU interrupt.

### ◆ p\_context

void const\* timer\_cfg\_t::p\_context

Placeholder for user data. Passed to the user callback in [timer\\_callback\\_args\\_t](#).

### ◆ timer\_api\_t

struct timer\_api\_t

Timer API structure. General timer functions implemented at the HAL layer follow this API.

### Data Fields

<code>fsp_err_t(*</code>	<code>open</code> )( <code>timer_ctrl_t *const p_ctrl, timer_cfg_t const *const p_cfg</code> )
<code>fsp_err_t(*</code>	<code>start</code> )( <code>timer_ctrl_t *const p_ctrl</code> )
<code>fsp_err_t(*</code>	<code>stop</code> )( <code>timer_ctrl_t *const p_ctrl</code> )
<code>fsp_err_t(*</code>	<code>reset</code> )( <code>timer_ctrl_t *const p_ctrl</code> )
<code>fsp_err_t(*</code>	<code>enable</code> )( <code>timer_ctrl_t *const p_ctrl</code> )
<code>fsp_err_t(*</code>	<code>disable</code> )( <code>timer_ctrl_t *const p_ctrl</code> )
<code>fsp_err_t(*</code>	<code>periodSet</code> )( <code>timer_ctrl_t *const p_ctrl, uint32_t const period</code> )
<code>fsp_err_t(*</code>	<code>dutyCycleSet</code> )( <code>timer_ctrl_t *const p_ctrl, uint32_t const duty_cycle_counts, uint32_t const pin</code> )
<code>fsp_err_t(*</code>	<code>infoGet</code> )( <code>timer_ctrl_t *const p_ctrl, timer_info_t *const p_info</code> )
<code>fsp_err_t(*</code>	<code>statusGet</code> )( <code>timer_ctrl_t *const p_ctrl, timer_status_t *const p_status</code> )
<code>fsp_err_t(*</code>	<code>callbackSet</code> )( <code>timer_ctrl_t *const p_api_ctrl, void(*p_callback)(timer_callback_args_t*), void const *const p_context, timer_callback_args_t *const p_callback_memory</code> )
<code>fsp_err_t(*</code>	<code>close</code> )( <code>timer_ctrl_t *const p_ctrl</code> )
<code>fsp_err_t(*</code>	<code>versionGet</code> )( <code>fsp_version_t *const p_version</code> )

### Field Documentation

◆ **open**

```
fsp_err_t(* timer_api_t::open) (timer_ctrl_t *const p_ctrl, timer_cfg_t const *const p_cfg)
```

Initial configuration.

**Implemented as**

- R\_GPT\_Open()
- R\_AGT\_Open()

**Parameters**

[in]	p_ctrl	Pointer to control block. Must be declared by user. Elements set here.
[in]	p_cfg	Pointer to configuration structure. All elements of this structure must be set by user.

◆ **start**

```
fsp_err_t(* timer_api_t::start) (timer_ctrl_t *const p_ctrl)
```

Start the counter.

**Implemented as**

- R\_GPT\_Start()
- R\_AGT\_Start()

**Parameters**

[in]	p_ctrl	Control block set in <a href="#">timer_api_t::open</a> call for this timer.
------	--------	-----------------------------------------------------------------------------

◆ **stop**

```
fsp_err_t(* timer_api_t::stop) (timer_ctrl_t *const p_ctrl)
```

Stop the counter.

**Implemented as**

- R\_GPT\_Stop()
- R\_AGT\_Stop()

**Parameters**

[in]	p_ctrl	Control block set in <a href="#">timer_api_t::open</a> call for this timer.
------	--------	-----------------------------------------------------------------------------



◆ **reset**

```
fsp_err_t(* timer_api_t::reset) (timer_ctrl_t *const p_ctrl)
```

Reset the counter to the initial value.

**Implemented as**

- [R\\_GPT\\_Reset\(\)](#)
- [R\\_AGT\\_Reset\(\)](#)

**Parameters**

[in]	p_ctrl	Control block set in <a href="#">timer_api_t::open</a> call for this timer.
------	--------	-----------------------------------------------------------------------------

◆ **enable**

```
fsp_err_t(* timer_api_t::enable) (timer_ctrl_t *const p_ctrl)
```

Enables input capture.

**Implemented as**

- [R\\_GPT\\_Enable\(\)](#)
- [R\\_AGT\\_Enable\(\)](#)

**Parameters**

[in]	p_ctrl	Control block set in <a href="#">timer_api_t::open</a> call for this timer.
------	--------	-----------------------------------------------------------------------------

◆ **disable**

```
fsp_err_t(* timer_api_t::disable) (timer_ctrl_t *const p_ctrl)
```

Disables input capture.

**Implemented as**

- [R\\_GPT\\_Disable\(\)](#)
- [R\\_AGT\\_Disable\(\)](#)

**Parameters**

[in]	p_ctrl	Control block set in <a href="#">timer_api_t::open</a> call for this timer.
------	--------	-----------------------------------------------------------------------------

◆ **periodSet**

```
fsp_err_t(* timer_api_t::periodSet) (timer_ctrl_t *const p_ctrl, uint32_t const period)
```

Set the time until the timer expires. See implementation for details of period update timing.

**Implemented as**

- R\_GPT\_PeriodSet()
- R\_AGT\_PeriodSet()

**Note**

*Timer expiration may or may not generate a CPU interrupt based on how the timer is configured in `timer_api_t::open`.*

**Parameters**

[in]	p_ctrl	Control block set in <a href="#">timer_api_t::open</a> call for this timer.
[in]	p_period	Time until timer should expire.

◆ **dutyCycleSet**

```
fsp_err_t(* timer_api_t::dutyCycleSet) (timer_ctrl_t *const p_ctrl, uint32_t const duty_cycle_counts, uint32_t const pin)
```

Sets the number of counts for the pin level to be high. If the timer is counting, the updated duty cycle is reflected after the next timer expiration.

**Implemented as**

- R\_GPT\_DutyCycleSet()
- R\_AGT\_DutyCycleSet()

**Parameters**

[in]	p_ctrl	Control block set in <a href="#">timer_api_t::open</a> call for this timer.
[in]	duty_cycle_counts	Time until duty cycle should expire.
[in]	pin	Which output pin to update. See implementation for details.

## ◆ infoGet

```
fsp_err_t(* timer_api_t::infoGet) (timer_ctrl_t *const p_ctrl, timer_info_t *const p_info)
```

Stores timer information in p\_info.

**Implemented as**

- R\_GPT\_InfoGet()
- R\_AGT\_InfoGet()

**Parameters**

[in]	p_ctrl	Control block set in <a href="#">timer_api_t::open</a> call for this timer.
[out]	p_info	Collection of information for this timer.

## ◆ statusGet

```
fsp_err_t(* timer_api_t::statusGet) (timer_ctrl_t *const p_ctrl, timer_status_t *const p_status)
```

Get the current counter value and timer state and store it in p\_status.

**Implemented as**

- R\_GPT\_StatusGet()
- R\_AGT\_StatusGet()

**Parameters**

[in]	p_ctrl	Control block set in <a href="#">timer_api_t::open</a> call for this timer.
[out]	p_status	Current status of this timer.

### ◆ callbackSet

```
fsp_err_t(* timer_api_t::callbackSet) (timer_ctrl_t *const p_api_ctrl,
void(*p_callback)(timer_callback_args_t *), void const *const p_context, timer_callback_args_t
*const p_callback_memory)
```

Specify callback function and optional context pointer and working memory pointer.

#### Implemented as

- R\_GPT\_CallbackSet()
- R\_AGT\_CallbackSet()

#### Parameters

[in]	p_ctrl	Control block set in <a href="#">timer_api_t::open</a> call for this timer.
[in]	p_callback	Callback function to register
[in]	p_context	Pointer to send to callback function
[in]	p_working_memory	Pointer to volatile memory where callback structure can be allocated. Callback arguments allocated here are only valid during the callback.

### ◆ close

```
fsp_err_t(* timer_api_t::close) (timer_ctrl_t *const p_ctrl)
```

Allows driver to be reconfigured and may reduce power consumption.

#### Implemented as

- R\_GPT\_Close()
- R\_AGT\_Close()

#### Parameters

[in]	p_ctrl	Control block set in <a href="#">timer_api_t::open</a> call for this timer.
------	--------	-----------------------------------------------------------------------------

◆ **versionGet**

```
fsp_err_t(* timer_api_t::versionGet) (fsp_version_t *const p_version)
```

Get version and store it in provided pointer p\_version.

**Implemented as**

- R\_GPT\_VersionGet()
- R\_AGT\_VersionGet()

**Parameters**

[out]	p_version	Code and API version used.
-------	-----------	----------------------------

◆ **timer\_instance\_t**

```
struct timer_instance_t
```

This structure encompasses everything that is needed to use an instance of this interface.

## Data Fields

timer_ctrl_t *	p_ctrl	Pointer to the control structure for this instance.
timer_cfg_t const *	p_cfg	Pointer to the configuration structure for this instance.
timer_api_t const *	p_api	Pointer to the API structure for this instance.

**Typedef Documentation**◆ **timer\_ctrl\_t**

```
typedef void timer_ctrl_t
```

Timer control block. Allocate an instance specific control block to pass into the timer API calls.

**Implemented as**

- gpt\_instance\_ctrl\_t
- agt\_instance\_ctrl\_t

**Enumeration Type Documentation**

◆ **timer\_event\_t**

enum <code>timer_event_t</code>	
Events that can trigger a callback function	
Enumerator	
TIMER_EVENT_CYCLE_END	Requested timer delay has expired or timer has wrapped around.
TIMER_EVENT_CREST	Timer crest event (counter is at a maximum, triangle-wave PWM only)
TIMER_EVENT_CAPTURE_A	A capture has occurred on signal A.
TIMER_EVENT_CAPTURE_B	A capture has occurred on signal B.
TIMER_EVENT_TROUGH	Timer trough event (counter is 0, triangle-wave PWM only).

◆ **timer\_variant\_t**

enum <code>timer_variant_t</code>	
Timer variant types.	
Enumerator	
TIMER_VARIANT_32_BIT	32-bit timer
TIMER_VARIANT_16_BIT	16-bit timer

◆ **timer\_state\_t**

enum <code>timer_state_t</code>	
Possible status values returned by <code>timer_api_t::statusGet</code> .	
Enumerator	
TIMER_STATE_STOPPED	Timer is stopped.
TIMER_STATE_COUNTING	Timer is running.

◆ **timer\_mode\_t**

enum <code>timer_mode_t</code>	
Timer operational modes	
Enumerator	
TIMER_MODE_PERIODIC	Timer restarts after period elapses.
TIMER_MODE_ONE_SHOT	Timer stops after period elapses.
TIMER_MODE_PWM	Timer generates saw-wave PWM output.
TIMER_MODE_TRIANGLE_WAVE_SYMMETRIC_PWM	Timer generates symmetric triangle-wave PWM output.
TIMER_MODE_TRIANGLE_WAVE_ASYMMETRIC_PWM	Timer generates asymmetric triangle-wave PWM output.

◆ **timer\_direction\_t**

enum <code>timer_direction_t</code>	
Direction of timer count	
Enumerator	
TIMER_DIRECTION_DOWN	Timer count goes up.
TIMER_DIRECTION_UP	Timer count goes down.

◆ **timer\_source\_div\_t**

enum timer_source_div_t	
PCLK divisors	
Enumerator	
TIMER_SOURCE_DIV_1	Timer clock source divided by 1.
TIMER_SOURCE_DIV_2	Timer clock source divided by 2.
TIMER_SOURCE_DIV_4	Timer clock source divided by 4.
TIMER_SOURCE_DIV_8	Timer clock source divided by 8.
TIMER_SOURCE_DIV_16	Timer clock source divided by 16.
TIMER_SOURCE_DIV_32	Timer clock source divided by 32.
TIMER_SOURCE_DIV_64	Timer clock source divided by 64.
TIMER_SOURCE_DIV_128	Timer clock source divided by 128.
TIMER_SOURCE_DIV_256	Timer clock source divided by 256.
TIMER_SOURCE_DIV_1024	Timer clock source divided by 1024.

### 4.3.35 Transfer Interface

#### Interfaces

#### Detailed Description

Interface for data transfer functions.

## Summary

The transfer interface supports background data transfer (no CPU intervention).

Implemented by:

- Data Transfer Controller (r\_dtc)
- Direct Memory Access Controller (r\_dmac)

#### Data Structures



struct [transfer\\_properties\\_t](#)

struct [transfer\\_info\\_t](#)

struct [transfer\\_cfg\\_t](#)

struct [transfer\\_api\\_t](#)

struct [transfer\\_instance\\_t](#)

## Typedefs

typedef void [transfer\\_ctrl\\_t](#)

## Enumerations

enum [transfer\\_mode\\_t](#)

enum [transfer\\_size\\_t](#)

enum [transfer\\_addr\\_mode\\_t](#)

enum [transfer\\_repeat\\_area\\_t](#)

enum [transfer\\_chain\\_mode\\_t](#)

enum [transfer\\_irq\\_t](#)

enum [transfer\\_start\\_mode\\_t](#)

## Data Structure Documentation

### ◆ [transfer\\_properties\\_t](#)

struct <a href="#">transfer_properties_t</a>		
Driver specific information.		
Data Fields		
uint32_t	block_count_max	Maximum number of blocks.
uint32_t	block_count_remaining	Number of blocks remaining.
uint32_t	transfer_length_max	Maximum number of transfers.
uint32_t	transfer_length_remaining	Number of transfers remaining.

### ◆ [transfer\\_info\\_t](#)

struct <a href="#">transfer_info_t</a>
This structure specifies the properties of the transfer.

**Warning**

When using DTC, this structure corresponds to the descriptor block registers required by the DTC. The following components may be modified by the driver: `p_src`, `p_dest`, `num_blocks`, and `length`.

When using DTC, do NOT reuse this structure to configure multiple transfers. Each transfer must have a unique [transfer\\_info\\_t](#).

When using DTC, this structure must not be allocated in a temporary location. Any instance of this structure must remain in scope until the transfer it is used for is closed.

**Note**

*When using DTC, consider placing instances of this structure in a protected section of memory.*

Data Fields		
union <a href="#">transfer_info_t</a>	<code>__unnamed__</code>	
void const *volatile	<code>p_src</code>	Source pointer.
void *volatile	<code>p_dest</code>	Destination pointer.
volatile uint16_t	<code>num_blocks</code>	Number of blocks to transfer when using <a href="#">TRANSFER_MODE_BLOCK</a> (both DTC and DMAC) and <a href="#">TRANSFER_MODE_REPEAT</a> (DMAC only), unused in other modes.
volatile uint16_t	<code>length</code>	Length of each transfer. Range limited for <a href="#">TRANSFER_MODE_BLOCK</a> and <a href="#">TRANSFER_MODE_REPEAT</a> , see HAL driver for details.

**◆ transfer\_cfg\_t**

Data Fields		
<a href="#">transfer_info_t</a> *	<code>p_info</code>	Pointer to transfer configuration options. If using chain transfer (DTC only), this can be a pointer to an array of chained transfers that will be completed in order.
void const *	<code>p_extend</code>	Extension parameter for hardware specific settings.

**◆ transfer\_api\_t**

Data Fields		
<a href="#">fsp_err_t</a> (* <code>open</code> )( <a href="#">transfer_ctrl_t</a> *const <code>p_ctrl</code> , <a href="#">transfer_cfg_t</a> const *const <code>p_cfg</code> )		

<code>fsp_err_t(*</code>	<code>reconfigure )(transfer_ctrl_t *const p_ctrl, transfer_info_t *p_info)</code>
<code>fsp_err_t(*</code>	<code>reset )(transfer_ctrl_t *const p_ctrl, void const *p_src, void *p_dest, uint16_t const num_transfers)</code>
<code>fsp_err_t(*</code>	<code>enable )(transfer_ctrl_t *const p_ctrl)</code>
<code>fsp_err_t(*</code>	<code>disable )(transfer_ctrl_t *const p_ctrl)</code>
<code>fsp_err_t(*</code>	<code>softwareStart )(transfer_ctrl_t *const p_ctrl, transfer_start_mode_t mode)</code>
<code>fsp_err_t(*</code>	<code>softwareStop )(transfer_ctrl_t *const p_ctrl)</code>
<code>fsp_err_t(*</code>	<code>infoGet )(transfer_ctrl_t *const p_ctrl, transfer_properties_t *const p_properties)</code>
<code>fsp_err_t(*</code>	<code>close )(transfer_ctrl_t *const p_ctrl)</code>
<code>fsp_err_t(*</code>	<code>versionGet )(fsp_version_t *const p_version)</code>

## Field Documentation

◆ **open**

```
fsp_err_t(* transfer_api_t::open) (transfer_ctrl_t *const p_ctrl, transfer_cfg_t const *const p_cfg)
```

Initial configuration.

**Implemented as**

- R\_DTC\_Open()
- R\_DMACE\_Open()

**Parameters**

[in,out]	p_ctrl	Pointer to control block. Must be declared by user. Elements set here.
[in]	p_cfg	Pointer to configuration structure. All elements of this structure must be set by user.

◆ **reconfigure**

```
fsp_err_t(* transfer_api_t::reconfigure) (transfer_ctrl_t *const p_ctrl, transfer_info_t *p_info)
```

Reconfigure the transfer. Enable the transfer if p\_info is valid.

**Implemented as**

- R\_DTC\_Reconfigure()
- R\_DMACE\_Reconfigure()

**Parameters**

[in,out]	p_ctrl	Pointer to control block. Must be declared by user. Elements set here.
[in]	p_info	Pointer to a new transfer info structure.

◆ **reset**

```
fsp_err_t(* transfer_api_t::reset) (transfer_ctrl_t *const p_ctrl, void const *p_src, void *p_dest,
uint16_t const num_transfers)
```

Reset source address pointer, destination address pointer, and/or length, keeping all other settings the same. Enable the transfer if p\_src, p\_dest, and length are valid.

**Implemented as**

- R\_DTC\_Reset()
- R\_DMACE\_Reset()

**Parameters**

[in]	p_ctrl	Control block set in <a href="#">transfer_api_t::open</a> call for this transfer.
[in]	p_src	Pointer to source. Set to NULL if source pointer should not change.
[in]	p_dest	Pointer to destination. Set to NULL if destination pointer should not change.
[in]	num_transfers	Transfer length in normal mode or number of blocks in block mode. In DMACE only, resets number of repeats (initially stored in <a href="#">transfer_info_t::num_blocks</a> ) in repeat mode. Not used in repeat mode for DTC.

◆ **enable**

```
fsp_err_t(* transfer_api_t::enable) (transfer_ctrl_t *const p_ctrl)
```

Enable transfer. Transfers occur after the activation source event (or when [transfer\\_api\\_t::softwareStart](#) is called if ELC\_EVENT\_ELC\_NONE is chosen as activation source).

**Implemented as**

- R\_DTC\_Enable()
- R\_DMACE\_Enable()

**Parameters**

[in]	p_ctrl	Control block set in <a href="#">transfer_api_t::open</a> call for this transfer.
------	--------	-----------------------------------------------------------------------------------

◆ **disable**

`fsp_err_t(* transfer_api_t::disable) (transfer_ctrl_t *const p_ctrl)`

Disable transfer. Transfers do not occur after the activation source event (or when `transfer_api_t::softwareStart` is called if `ELC_EVENT_ELC_NONE` is chosen as the DMAC activation source).

**Note**

*If a transfer is in progress, it will be completed. Subsequent transfer requests do not cause a transfer.*

**Implemented as**

- `R_DTC_Disable()`
- `R_DMACE_Disable()`

**Parameters**

[in]	p_ctrl	Control block set in <code>transfer_api_t::open</code> call for this transfer.
------	--------	--------------------------------------------------------------------------------

◆ **softwareStart**

`fsp_err_t(* transfer_api_t::softwareStart) (transfer_ctrl_t *const p_ctrl, transfer_start_mode_t mode)`

Start transfer in software.

**Warning**

Only works if `ELC_EVENT_ELC_NONE` is chosen as the DMAC activation source.

**Note**

*Not supported for DTC.*

**Implemented as**

- `R_DMACE_SoftwareStart()`

**Parameters**

[in]	p_ctrl	Control block set in <code>transfer_api_t::open</code> call for this transfer.
[in]	mode	Select mode from <code>transfer_start_mode_t</code> .

## ◆ softwareStop

```
fsp_err_t(* transfer_api_t::softwareStop) (transfer_ctrl_t *const p_ctrl)
```

Stop transfer in software. The transfer will stop after completion of the current transfer.

*Note*

*Not supported for DTC.*

*Only applies for transfers started with TRANSFER\_START\_MODE\_REPEAT.*

**Warning**

Only works if ELC\_EVENT\_ELC\_NONE is chosen as the DMAC activation source.

**Implemented as**

- R\_DMAMC\_SoftwareStop()

**Parameters**

[in]	p_ctrl	Control block set in <a href="#">transfer_api_t::open</a> call for this transfer.
------	--------	-----------------------------------------------------------------------------------

## ◆ infoGet

```
fsp_err_t(* transfer_api_t::infoGet) (transfer_ctrl_t *const p_ctrl, transfer_properties_t *const p_properties)
```

Provides information about this transfer.

**Implemented as**

- R\_DTC\_InfoGet()
- R\_DMAMC\_InfoGet()

**Parameters**

[in]	p_ctrl	Control block set in <a href="#">transfer_api_t::open</a> call for this transfer.
[out]	p_properties	Driver specific information.

## ◆ close

```
fsp_err_t(* transfer_api_t::close) (transfer_ctrl_t *const p_ctrl)
```

Releases hardware lock. This allows a transfer to be reconfigured using [transfer\\_api\\_t::open](#).

**Implemented as**

- R\_DTC\_Close()
- R\_DMAMC\_Close()

**Parameters**

[in]	p_ctrl	Control block set in <a href="#">transfer_api_t::open</a> call for this transfer.
------	--------	-----------------------------------------------------------------------------------

◆ **versionGet**

```
fsp_err_t(* transfer_api_t::versionGet) (fsp_version_t *const p_version)
```

Gets version and stores it in provided pointer p\_version.

**Implemented as**

- R\_DTC\_VersionGet()
- R\_DMxAC\_VersionGet()

**Parameters**

[out]	p_version	Code and API version used.
-------	-----------	----------------------------

◆ **transfer\_instance\_t**

```
struct transfer_instance_t
```

This structure encompasses everything that is needed to use an instance of this interface.

## Data Fields

<code>transfer_ctrl_t *</code>	p_ctrl	Pointer to the control structure for this instance.
<code>transfer_cfg_t const *</code>	p_cfg	Pointer to the configuration structure for this instance.
<code>transfer_api_t const *</code>	p_api	Pointer to the API structure for this instance.

**Typedef Documentation**◆ **transfer\_ctrl\_t**

```
typedef void transfer_ctrl_t
```

Transfer control block. Allocate an instance specific control block to pass into the transfer API calls.

**Implemented as**

- dtc\_instance\_ctrl\_t
- dmac\_instance\_ctrl\_t

**Enumeration Type Documentation**



◆ **transfer\_mode\_t**

enum <code>transfer_mode_t</code>	
Transfer mode describes what will happen when a transfer request occurs.	
Enumerator	
<code>TRANSFER_MODE_NORMAL</code>	In normal mode, each transfer request causes a transfer of <code>transfer_size_t</code> from the source pointer to the destination pointer. The transfer length is decremented and the source and address pointers are updated according to <code>transfer_addr_mode_t</code> . After the transfer length reaches 0, transfer requests will not cause any further transfers.
<code>TRANSFER_MODE_REPEAT</code>	Repeat mode is like normal mode, except that when the transfer length reaches 0, the pointer to the repeat area and the transfer length will be reset to their initial values. If DMAC is used, the transfer repeats only <code>transfer_info_t::num_blocks</code> times. After the transfer repeats <code>transfer_info_t::num_blocks</code> times, transfer requests will not cause any further transfers. If DTC is used, the transfer repeats continuously (no limit to the number of repeat transfers).
<code>TRANSFER_MODE_BLOCK</code>	In block mode, each transfer request causes <code>transfer_info_t::length</code> transfers of <code>transfer_size_t</code> . After each individual transfer, the source and destination pointers are updated according to <code>transfer_addr_mode_t</code> . After the block transfer is complete, <code>transfer_info_t::num_blocks</code> is decremented. After the <code>transfer_info_t::num_blocks</code> reaches 0, transfer requests will not cause any further transfers.

◆ **transfer\_size\_t**

enum <a href="#">transfer_size_t</a>	
Transfer size specifies the size of each individual transfer. Total transfer length = <code>transfer_size_t * transfer_length_t</code>	
Enumerator	
TRANSFER_SIZE_1_BYTE	Each transfer transfers a 8-bit value.
TRANSFER_SIZE_2_BYTE	Each transfer transfers a 16-bit value.
TRANSFER_SIZE_4_BYTE	Each transfer transfers a 32-bit value.

◆ **transfer\_addr\_mode\_t**

enum <a href="#">transfer_addr_mode_t</a>	
Address mode specifies whether to modify (increment or decrement) pointer after each transfer.	
Enumerator	
TRANSFER_ADDR_MODE_FIXED	Address pointer remains fixed after each transfer.
TRANSFER_ADDR_MODE_OFFSET	Offset is added to the address pointer after each transfer.
TRANSFER_ADDR_MODE_INCREMENTED	Address pointer is incremented by associated <a href="#">transfer_size_t</a> after each transfer.
TRANSFER_ADDR_MODE_DECREMENTED	Address pointer is decremented by associated <a href="#">transfer_size_t</a> after each transfer.

◆ **transfer\_repeat\_area\_t**

enum <code>transfer_repeat_area_t</code>	
Repeat area options (source or destination). In <code>TRANSFER_MODE_REPEAT</code> , the selected pointer returns to its original value after <code>transfer_info_t::length</code> transfers. In <code>TRANSFER_MODE_BLOCK</code> , the selected pointer returns to its original value after each transfer.	
Enumerator	
<code>TRANSFER_REPEAT_AREA_DESTINATION</code>	Destination area repeated in <code>TRANSFER_MODE_REPEAT</code> or <code>TRANSFER_MODE_BLOCK</code> .
<code>TRANSFER_REPEAT_AREA_SOURCE</code>	Source area repeated in <code>TRANSFER_MODE_REPEAT</code> or <code>TRANSFER_MODE_BLOCK</code> .

◆ **transfer\_chain\_mode\_t**

enum <code>transfer_chain_mode_t</code>	
Chain transfer mode options.	
<i>Note</i> <i>Only applies for DTC.</i>	
Enumerator	
<code>TRANSFER_CHAIN_MODE_DISABLED</code>	Chain mode not used.
<code>TRANSFER_CHAIN_MODE_EACH</code>	Switch to next transfer after a single transfer from this <code>transfer_info_t</code> .
<code>TRANSFER_CHAIN_MODE_END</code>	Complete the entire transfer defined in this <code>transfer_info_t</code> before chaining to next transfer.

◆ **transfer\_irq\_t**

enum <code>transfer_irq_t</code>	
Interrupt options.	
Enumerator	
TRANSFER_IRQ_END	<p>Interrupt occurs only after last transfer. If this transfer is chained to a subsequent transfer, the interrupt will occur only after subsequent chained transfer(s) are complete.</p> <p><b>Warning</b> DTC triggers the interrupt of the activation source. Choosing TRANSFER_IRQ_END with DTC will prevent activation source interrupts until the transfer is complete.</p>
TRANSFER_IRQ_EACH	<p>Interrupt occurs after each transfer.</p> <p><i>Note</i> <i>Not available in all HAL drivers. See HAL driver for details.</i></p>

◆ **transfer\_start\_mode\_t**

enum <code>transfer_start_mode_t</code>	
Select whether to start single or repeated transfer with software start.	
Enumerator	
TRANSFER_START_MODE_SINGLE	Software start triggers single transfer.
TRANSFER_START_MODE_REPEAT	Software start transfer continues until transfer is complete.

## 4.3.36 UART Interface

### Interfaces

#### Detailed Description

Interface for UART communications.

## Summary

The UART interface provides common APIs for UART HAL drivers. The UART interface supports the following features:

- Full-duplex UART communication
- Interrupt driven transmit/receive processing
- Callback function with returned event code
- Runtime baud-rate change
- Hardware resource locking during a transaction
- CTS/RTS hardware flow control support (with an associated IOPORT pin)

Implemented by:

- [Serial Communications Interface \(SCI\) UART \(r\\_sci\\_uart\)](#)

### Data Structures

struct [uart\\_info\\_t](#)

struct [uart\\_callback\\_args\\_t](#)

struct [uart\\_cfg\\_t](#)

struct [uart\\_api\\_t](#)

struct [uart\\_instance\\_t](#)

### Typedefs

typedef void [uart\\_ctrl\\_t](#)

### Enumerations

enum [uart\\_event\\_t](#)

enum [uart\\_data\\_bits\\_t](#)

enum [uart\\_parity\\_t](#)

enum [uart\\_stop\\_bits\\_t](#)

enum [uart\\_dir\\_t](#)

### Data Structure Documentation

#### ◆ [uart\\_info\\_t](#)

struct [uart\\_info\\_t](#)

UART driver specific information

Data Fields

uint32_t	write_bytes_max	Maximum bytes that can be written at this time. Only applies if <a href="#">uart_cfg_t::p_transfer_tx</a> is not NULL.
uint32_t	read_bytes_max	Maximum bytes that are available to read at one time. Only applies if <a href="#">uart_cfg_t::p_transfer_rx</a> is not NULL.

◆ **uart\_callback\_args\_t**

struct uart_callback_args_t		
UART Callback parameter definition		
Data Fields		
uint32_t	channel	Device channel number.
<a href="#">uart_event_t</a>	event	Event code.
uint32_t	data	Contains the next character received for the events UART_EVENT_RX_CHAR, UART_EVENT_ERR_PARITY, UART_EVENT_ERR_FRAMING, or UART_EVENT_ERR_OVERFLOW. Otherwise unused.
void const *	p_context	Context provided to user during callback.

◆ **uart\_cfg\_t**

struct uart_cfg_t	
UART Configuration	
<b>Data Fields</b>	
uint8_t	<a href="#">channel</a>
	Select a channel corresponding to the channel number of the hardware.
<a href="#">uart_data_bits_t</a>	<a href="#">data_bits</a>
	Data bit length (8 or 7 or 9)
<a href="#">uart_parity_t</a>	<a href="#">parity</a>
	Parity type (none or odd or even)

<code>uart_stop_bits_t</code>	<code>stop_bits</code>
	Stop bit length (1 or 2)
<code>uint8_t</code>	<code>rxi_ipl</code>
	Receive interrupt priority.
<code>IRQn_Type</code>	<code>rxi_irq</code>
	Receive interrupt IRQ number.
<code>uint8_t</code>	<code>txi_ipl</code>
	Transmit interrupt priority.
<code>IRQn_Type</code>	<code>txi_irq</code>
	Transmit interrupt IRQ number.
<code>uint8_t</code>	<code>tei_ipl</code>
	Transmit end interrupt priority.
<code>IRQn_Type</code>	<code>tei_irq</code>
	Transmit end interrupt IRQ number.
<code>uint8_t</code>	<code>eri_ipl</code>
	Error interrupt priority.
<code>IRQn_Type</code>	<code>eri_irq</code>
	Error interrupt IRQ number.

<code>transfer_instance_t const *</code>	<code>p_transfer_rx</code>
<code>transfer_instance_t const *</code>	<code>p_transfer_tx</code>
<code>void(*</code>	<code>p_callback )(uart_callback_args_t *p_args)</code>
	Pointer to callback function.
<code>void const *</code>	<code>p_context</code>
	User defined context passed into callback function.
<code>void const *</code>	<code>p_extend</code>
	UART hardware dependent configuration.

## Field Documentation

### ◆ `p_transfer_rx`

`transfer_instance_t const* uart_cfg_t::p_transfer_rx`

Optional transfer instance used to receive multiple bytes without interrupts. Set to NULL if unused. If NULL, the number of bytes allowed in the read API is limited to one byte at a time.

### ◆ `p_transfer_tx`

`transfer_instance_t const* uart_cfg_t::p_transfer_tx`

Optional transfer instance used to send multiple bytes without interrupts. Set to NULL if unused. If NULL, the number of bytes allowed in the write APIs is limited to one byte at a time.

### ◆ `uart_api_t`

`struct uart_api_t`

Shared Interface definition for UART

#### Data Fields

<code>fsp_err_t(*</code>	<code>open )(uart_ctrl_t *const p_ctrl, uart_cfg_t const *const p_cfg)</code>
<code>fsp_err_t(*</code>	<code>read )(uart_ctrl_t *const p_ctrl, uint8_t *const p_dest, uint32_t const bytes)</code>
<code>fsp_err_t(*</code>	<code>write )(uart_ctrl_t *const p_ctrl, uint8_t const *const p_src, uint32_t</code>



	const bytes)
<code>fsp_err_t(*</code>	<code>baudSet )(uart_ctrl_t *const p_ctrl, void const *const p_baudrate_info)</code>
<code>fsp_err_t(*</code>	<code>infoGet )(uart_ctrl_t *const p_ctrl, uart_info_t *const p_info)</code>
<code>fsp_err_t(*</code>	<code>communicationAbort )(uart_ctrl_t *const p_ctrl, uart_dir_t communication_to_abort)</code>
<code>fsp_err_t(*</code>	<code>callbackSet )(uart_ctrl_t *const p_api_ctrl, void(*p_callback)(uart_callback_args_t *), void const *const p_context, uart_callback_args_t *const p_callback_memory)</code>
<code>fsp_err_t(*</code>	<code>close )(uart_ctrl_t *const p_ctrl)</code>
<code>fsp_err_t(*</code>	<code>versionGet )(fsp_version_t *p_version)</code>

## Field Documentation

### ◆ open

`fsp_err_t(* uart_api_t::open) (uart_ctrl_t *const p_ctrl, uart_cfg_t const *const p_cfg)`

Open UART device.

#### Implemented as

- `R_SCI_UART_Open()`

#### Parameters

[in,out]	<code>p_ctrl</code>	Pointer to the UART control block. Must be declared by user. Value set here.
[in]	<code>uart_cfg_t</code>	Pointer to UART configuration structure. All elements of this structure must be set by user.

## ◆ read

`fsp_err_t(* uart_api_t::read) (uart_ctrl_t *const p_ctrl, uint8_t *const p_dest, uint32_t const bytes)`

Read from UART device. The read buffer is used until the read is complete. When a transfer is complete, the callback is called with event `UART_EVENT_RX_COMPLETE`. Bytes received outside an active transfer are received in the callback function with event `UART_EVENT_RX_CHAR`. The maximum transfer size is reported by `infoGet()`.

**Implemented as**

- `R_SCI_UART_Read()`

**Parameters**

[in]	<code>p_ctrl</code>	Pointer to the UART control block for the channel.
[in]	<code>p_dest</code>	Destination address to read data from.
[in]	<code>bytes</code>	Read data length.

## ◆ write

`fsp_err_t(* uart_api_t::write) (uart_ctrl_t *const p_ctrl, uint8_t const *const p_src, uint32_t const bytes)`

Write to UART device. The write buffer is used until write is complete. Do not overwrite write buffer contents until the write is finished. When the write is complete (all bytes are fully transmitted on the wire), the callback called with event `UART_EVENT_TX_COMPLETE`. The maximum transfer size is reported by `infoGet()`.

**Implemented as**

- `R_SCI_UART_Write()`

**Parameters**

[in]	<code>p_ctrl</code>	Pointer to the UART control block.
[in]	<code>p_src</code>	Source address to write data to.
[in]	<code>bytes</code>	Write data length.

◆ **baudSet**

```
fsp_err_t(* uart_api_t::baudSet) (uart_ctrl_t *const p_ctrl, void const *const p_baudrate_info)
```

Change baud rate.

**Warning**

Calling this API aborts any in-progress transmission and disables reception until the new baud settings have been applied.

**Implemented as**

- R\_SCI\_UART\_BaudSet()

**Parameters**

[in]	p_ctrl	Pointer to the UART control block.
[in]	p_baudrate_info	Pointer to module specific information for configuring baud rate.

◆ **infoGet**

```
fsp_err_t(* uart_api_t::infoGet) (uart_ctrl_t *const p_ctrl, uart_info_t *const p_info)
```

Get the driver specific information.

**Implemented as**

- R\_SCI\_UART\_InfoGet()

**Parameters**

[in]	p_ctrl	Pointer to the UART control block.
[in]	baudrate	Baud rate in bps.

◆ **communicationAbort**

```
fsp_err_t(* uart_api_t::communicationAbort) (uart_ctrl_t *const p_ctrl, uart_dir_t communication_to_abort)
```

Abort ongoing transfer.

**Implemented as**

- R\_SCI\_UART\_Abort()

**Parameters**

[in]	p_ctrl	Pointer to the UART control block.
[in]	communication_to_abort	Type of abort request.

◆ **callbackSet**

```
fsp_err_t(* uart_api_t::callbackSet) (uart_ctrl_t *const p_api_ctrl,
void(*p_callback)(uart_callback_args_t *), void const *const p_context, uart_callback_args_t *const
p_callback_memory)
```

Specify callback function and optional context pointer and working memory pointer.

**Implemented as**

- R\_SCI\_Uart\_CallbackSet()

**Parameters**

[in]	p_ctrl	Pointer to the UART control block.
[in]	p_callback	Callback function
[in]	p_context	Pointer to send to callback function
[in]	p_working_memory	Pointer to volatile memory where callback structure can be allocated. Callback arguments allocated here are only valid during the callback.

◆ **close**

```
fsp_err_t(* uart_api_t::close) (uart_ctrl_t *const p_ctrl)
```

Close UART device.

**Implemented as**

- R\_SCI\_UART\_Close()

**Parameters**

[in]	p_ctrl	Pointer to the UART control block.
------	--------	------------------------------------

◆ **versionGet**

```
fsp_err_t(* uart_api_t::versionGet) (fsp_version_t *p_version)
```

Get version.

**Implemented as**

- [R\\_SCI\\_UART\\_VersionGet\(\)](#)

**Parameters**

[in]	p_version	Pointer to the memory to store the version information.
------	-----------	---------------------------------------------------------

◆ **uart\_instance\_t**

```
struct uart_instance_t
```

This structure encompasses everything that is needed to use an instance of this interface.

## Data Fields

<a href="#">uart_ctrl_t</a> *	p_ctrl	Pointer to the control structure for this instance.
<a href="#">uart_cfg_t</a> const *	p_cfg	Pointer to the configuration structure for this instance.
<a href="#">uart_api_t</a> const *	p_api	Pointer to the API structure for this instance.

**Typedef Documentation**◆ **uart\_ctrl\_t**

```
typedef void uart_ctrl_t
```

UART control block. Allocate an instance specific control block to pass into the UART API calls.

**Implemented as**

- [sci\\_uart\\_instance\\_ctrl\\_t](#)

**Enumeration Type Documentation**

◆ **uart\_event\_t**

enum <code>uart_event_t</code>	
UART Event codes	
Enumerator	
<code>UART_EVENT_RX_COMPLETE</code>	Receive complete event.
<code>UART_EVENT_TX_COMPLETE</code>	Transmit complete event.
<code>UART_EVENT_RX_CHAR</code>	Character received.
<code>UART_EVENT_ERR_PARITY</code>	Parity error event.
<code>UART_EVENT_ERR_FRAMING</code>	Mode fault error event.
<code>UART_EVENT_ERR_OVERFLOW</code>	FIFO Overflow error event.
<code>UART_EVENT_BREAK_DETECT</code>	Break detect error event.
<code>UART_EVENT_TX_DATA_EMPTY</code>	Last byte is transmitting, ready for more data.

◆ **uart\_data\_bits\_t**

enum <code>uart_data_bits_t</code>	
UART Data bit length definition	
Enumerator	
<code>UART_DATA_BITS_8</code>	Data bits 8-bit.
<code>UART_DATA_BITS_7</code>	Data bits 7-bit.
<code>UART_DATA_BITS_9</code>	Data bits 9-bit.

◆ **uart\_parity\_t**

enum <a href="#">uart_parity_t</a>	
UART Parity definition	
Enumerator	
UART_PARITY_OFF	No parity.
UART_PARITY_EVEN	Even parity.
UART_PARITY_ODD	Odd parity.

◆ **uart\_stop\_bits\_t**

enum <a href="#">uart_stop_bits_t</a>	
UART Stop bits definition	
Enumerator	
UART_STOP_BITS_1	Stop bit 1-bit.
UART_STOP_BITS_2	Stop bits 2-bit.

◆ **uart\_dir\_t**

enum <a href="#">uart_dir_t</a>	
UART transaction definition	
Enumerator	
UART_DIR_RX_TX	Both RX and TX.
UART_DIR_RX	Only RX.
UART_DIR_TX	Only TX.

**4.3.37 USB Interface**[Interfaces](#)**Detailed Description**

Interface for USB functions.

## Summary

The USB interface provides USB functionality.

The USB interface can be implemented by:

- [USB \(r\\_usb\\_basic\)](#)

### Data Structures

```
struct usb\_api\_t
```

```
struct usb\_instance\_t
```

### Macros

```
#define USB\_API\_VERSION\_MINOR  
Minor version of the API.
```

```
#define USB\_API\_VERSION\_MAJOR  
Major version of the API.
```

```
#define USB\_BREQUEST  
b15-8
```

```
#define USB\_GET\_STATUS  
USB Standard request Get Status.
```

```
#define USB\_CLEAR\_FEATURE  
USB Standard request Clear Feature.
```

```
#define USB\_REQRESERVED  
USB Standard request Reqreserved.
```

```
#define USB\_SET\_FEATURE  
USB Standard request Set Feature.
```

```
#define USB\_REQRESERVED1
```



USB Standard request Reqreserved1.

```
#define USB_SET_ADDRESS
USB Standard request Set Address.
```

```
#define USB_GET_DESCRIPTOR
USB Standard request Get Descriptor.
```

```
#define USB_SET_DESCRIPTOR
USB Standard request Set Descriptor.
```

```
#define USB_GET_CONFIGURATION
USB Standard request Get Configuration.
```

```
#define USB_SET_CONFIGURATION
USB Standard request Set Configuration.
```

```
#define USB_GET_INTERFACE
USB Standard request Get Interface.
```

```
#define USB_SET_INTERFACE
USB Standard request Set Interface.
```

```
#define USB_SYNCH_FRAME
USB Standard request Synch Frame.
```

```
#define USB_HOST_TO_DEV
From host to device.
```

```
#define USB_DEV_TO_HOST
From device to host.
```

```
#define USB_STANDARD
Standard Request.
```

```
#define USB_CLASS  
Class Request.
```

```
#define USB_VENDOR  
Vendor Request.
```

```
#define USB_DEVICE  
Device.
```

```
#define USB_INTERFACE  
Interface.
```

```
#define USB_ENDPOINT  
End Point.
```

```
#define USB_OTHER  
Other.
```

```
#define USB_NULL  
NULL pointer.
```

```
#define USB_IP0  
USB0 module.
```

```
#define USB_IP1  
USB1 module.
```

```
#define USB_PIPE0  
Pipe Number0.
```

```
#define USB_PIPE1  
Pipe Number1.
```

```
#define USB_PIPE2  
    Pipe Number2.
```

```
#define USB_PIPE3  
    Pipe Number3.
```

```
#define USB_PIPE4  
    Pipe Number4.
```

```
#define USB_PIPE5  
    Pipe Number5.
```

```
#define USB_PIPE6  
    Pipe Number6.
```

```
#define USB_PIPE7  
    Pipe Number7.
```

```
#define USB_PIPE8  
    Pipe Number8.
```

```
#define USB_PIPE9  
    Pipe Number9.
```

```
#define USB_EP0  
    End Point Number0.
```

```
#define USB_EP1  
    End Point Number1.
```

```
#define USB_EP2  
    End Point Number2.
```

```
#define USB_EP3
```

End Point Number3.

```
#define USB_EP4  
End Point Number4.
```

```
#define USB_EP5  
End Point Number5.
```

```
#define USB_EP6  
End Point Number6.
```

```
#define USB_EP7  
End Point Number7.
```

```
#define USB_EP8  
End Point Number8.
```

```
#define USB_EP9  
End Point Number9.
```

```
#define USB_EP10  
End Point Number10.
```

```
#define USB_EP11  
End Point Number11.
```

```
#define USB_EP12  
End Point Number12.
```

```
#define USB_EP13  
End Point Number13.
```

```
#define USB_EP14  
End Point Number14.
```

```
#define USB_EP15  
    End Point Number15.
```

```
#define USB_DT_DEVICE  
    Device Descriptor.
```

```
#define USB_DT_CONFIGURATION  
    Configuration Descriptor.
```

```
#define USB_DT_STRING  
    String Descriptor.
```

```
#define USB_DT_INTERFACE  
    Interface Descriptor.
```

```
#define USB_DT_ENDPOINT  
    Endpoint Descriptor.
```

```
#define USB_DT_DEVICE_QUALIFIER  
    Device Qualifier Descriptor.
```

```
#define USB_DT_OTHER_SPEED_CONF  
    Other Speed Configuration Descriptor.
```

```
#define USB_DT_INTERFACE_POWER  
    Interface Power Descriptor.
```

```
#define USB_DT_OTGDESCRIPTOR  
    OTG Descriptor.
```

```
#define USB_DT_HUBDESCRIPTOR  
    HUB descriptor.
```

```
#define USB_IFCLS_NOT  
Un corresponding Class.
```

```
#define USB_IFCLS_AUD  
Audio Class.
```

```
#define USB_IFCLS_CDC  
CDC Class.
```

```
#define USB_IFCLS_CDCC  
CDC-Control Class.
```

```
#define USB_IFCLS_HID  
HID Class.
```

```
#define USB_IFCLS_PHY  
Physical Class.
```

```
#define USB_IFCLS_IMG  
Image Class.
```

```
#define USB_IFCLS_PRN  
Printer Class.
```

```
#define USB_IFCLS_MAS  
Mass Storage Class.
```

```
#define USB_IFCLS_HUB  
HUB Class.
```

```
#define USB_IFCLS_CDCCD  
CDC-Data Class.
```

```
#define USB_IFCLS_CHIP
```

Chip/Smart Card Class.

```
#define USB_IFCLS_CNT  
Content-Security Class.
```

```
#define USB_IFCLS_VID  
Video Class.
```

```
#define USB_IFCLS_DIAG  
Diagnostic Device.
```

```
#define USB_IFCLS_WIRE  
Wireless Controller.
```

```
#define USB_IFCLS_APL  
Application-Specific.
```

```
#define USB_IFCLS_VEN  
Vendor-Specific Class.
```

```
#define USB_EP_IN  
In Endpoint.
```

```
#define USB_EP_OUT  
Out Endpoint.
```

```
#define USB_EP_ISO  
Isochronous Transfer.
```

```
#define USB_EP_BULK  
Bulk Transfer.
```

```
#define USB_EP_INT  
Interrupt Transfer.
```

```
#define USB_CF_RESERVED  
Reserved(set to 1)
```

```
#define USB_CF_SELFP  
Self Powered.
```

```
#define USB_CF_BUSP  
Bus Powered.
```

```
#define USB_CF_RWUPON  
Remote Wake up ON.
```

```
#define USB_CF_RWUPOFF  
Remote Wake up OFF.
```

```
#define USB_DD_BLENGTH  
Device Descriptor Length.
```

```
#define USB_CD_BLENGTH  
Configuration Descriptor Length.
```

```
#define USB_ID_BLENGTH  
Interface Descriptor Length.
```

```
#define USB_ED_BLENGTH  
Endpoint Descriptor Length.
```

## Enumerations

```
enum usb_speed_t
```

```
enum usb_setup_status_t
```

```
enum usb_status_t
```

```
enum usb_class_t
```



enum [usb\\_bcport\\_t](#)enum [usb\\_onoff\\_t](#)enum [usb\\_transfer\\_t](#)enum [usb\\_transfer\\_type\\_t](#)enum [usb\\_mode\\_t](#)enum [usb\\_compliancetests\\_status\\_t](#)

## Data Structure Documentation

### ◆ [usb\\_api\\_t](#)

struct [usb\\_api\\_t](#)

Functions implemented at the HAL layer will follow this API.

#### Data Fields

<a href="#">fsp_err_t</a> (*	<a href="#">open</a> )( <a href="#">usb_ctrl_t</a> *const p_api_ctrl, <a href="#">usb_cfg_t</a> const *const p_cfg)
------------------------------	---------------------------------------------------------------------------------------------------------------------

<a href="#">fsp_err_t</a> (*	<a href="#">close</a> )( <a href="#">usb_ctrl_t</a> *const p_api_ctrl)
------------------------------	------------------------------------------------------------------------

<a href="#">fsp_err_t</a> (*	<a href="#">read</a> )( <a href="#">usb_ctrl_t</a> *const p_api_ctrl, <a href="#">uint8_t</a> *p_buf, <a href="#">uint32_t</a> size, <a href="#">uint8_t</a> destination)
------------------------------	---------------------------------------------------------------------------------------------------------------------------------------------------------------------------

<a href="#">fsp_err_t</a> (*	<a href="#">write</a> )( <a href="#">usb_ctrl_t</a> *const p_api_ctrl, <a href="#">uint8_t</a> const *const p_buf, <a href="#">uint32_t</a> size, <a href="#">uint8_t</a> destination)
------------------------------	----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------

<a href="#">fsp_err_t</a> (*	<a href="#">stop</a> )( <a href="#">usb_ctrl_t</a> *const p_api_ctrl, <a href="#">usb_transfer_t</a> direction, <a href="#">uint8_t</a> destination)
------------------------------	------------------------------------------------------------------------------------------------------------------------------------------------------

<a href="#">fsp_err_t</a> (*	<a href="#">suspend</a> )( <a href="#">usb_ctrl_t</a> *const p_api_ctrl)
------------------------------	--------------------------------------------------------------------------

<a href="#">fsp_err_t</a> (*	<a href="#">resume</a> )( <a href="#">usb_ctrl_t</a> *const p_api_ctrl)
------------------------------	-------------------------------------------------------------------------

<a href="#">fsp_err_t</a> (*	<a href="#">vbusSet</a> )( <a href="#">usb_ctrl_t</a> *const p_api_ctrl, <a href="#">uint16_t</a> state)
------------------------------	----------------------------------------------------------------------------------------------------------

<a href="#">fsp_err_t</a> (*	<a href="#">infoGet</a> )( <a href="#">usb_ctrl_t</a> *const p_api_ctrl, <a href="#">usb_info_t</a> *p_info, <a href="#">uint8_t</a> destination)
------------------------------	---------------------------------------------------------------------------------------------------------------------------------------------------

<code>fsp_err_t(*</code>	<code>pipeRead</code> )(usb_ctrl_t *const p_api_ctrl, uint8_t *p_buf, uint32_t size, uint8_t pipe_number)
<code>fsp_err_t(*</code>	<code>pipeWrite</code> )(usb_ctrl_t *const p_api_ctrl, uint8_t *p_buf, uint32_t size, uint8_t pipe_number)
<code>fsp_err_t(*</code>	<code>pipeStop</code> )(usb_ctrl_t *const p_api_ctrl, uint8_t pipe_number)
<code>fsp_err_t(*</code>	<code>usedPipesGet</code> )(usb_ctrl_t *const p_api_ctrl, uint16_t *p_pipe, uint8_t destination)
<code>fsp_err_t(*</code>	<code>pipeInfoGet</code> )(usb_ctrl_t *const p_api_ctrl, usb_pipe_t *p_info, uint8_t pipe_number)
<code>fsp_err_t(*</code>	<code>versionGet</code> )(fsp_version_t *const p_version)
<code>fsp_err_t(*</code>	<code>eventGet</code> )(usb_ctrl_t *const p_api_ctrl, usb_status_t *event)
<code>fsp_err_t(*</code>	<code>callback</code> )(usb_callback_t *p_callback)
<code>fsp_err_t(*</code>	<code>pullUp</code> )(usb_ctrl_t *const p_api_ctrl, uint8_t state)
<code>fsp_err_t(*</code>	<code>hostControlTransfer</code> )(usb_ctrl_t *const p_api_ctrl, usb_setup_t *p_setup, uint8_t *p_buf, uint8_t device_address)
<code>fsp_err_t(*</code>	<code>periControlDataGet</code> )(usb_ctrl_t *const p_api_ctrl, uint8_t *p_buf, uint32_t size)
<code>fsp_err_t(*</code>	<code>periControlDataSet</code> )(usb_ctrl_t *const p_api_ctrl, uint8_t *p_buf, uint32_t size)
<code>fsp_err_t(*</code>	<code>periControlStatusSet</code> )(usb_ctrl_t *const p_api_ctrl, usb_setup_status_t status)
<code>fsp_err_t(*</code>	<code>remoteWakeup</code> )(usb_ctrl_t *const p_api_ctrl)

<code>fsp_err_t(*</code>	<code>moduleNumberGet</code> )(usb_ctrl_t *const p_api_ctrl, uint8_t *module_number)
<code>fsp_err_t(*</code>	<code>classTypeGet</code> )(usb_ctrl_t *const p_api_ctrl, usb_class_t *class_type)
<code>fsp_err_t(*</code>	<code>deviceAddressGet</code> )(usb_ctrl_t *const p_api_ctrl, uint8_t *device_address)
<code>fsp_err_t(*</code>	<code>pipeNumberGet</code> )(usb_ctrl_t *const p_api_ctrl, uint8_t *pipe_number)
<code>fsp_err_t(*</code>	<code>deviceStateGet</code> )(usb_ctrl_t *const p_api_ctrl, uint16_t *state)
<code>fsp_err_t(*</code>	<code>dataSizeGet</code> )(usb_ctrl_t *const p_api_ctrl, uint32_t *data_size)
<code>fsp_err_t(*</code>	<code>setupGet</code> )(usb_ctrl_t *const p_api_ctrl, usb_setup_t *setup)

## Field Documentation

### ◆ open

`fsp_err_t(* usb_api_t::open)` (usb\_ctrl\_t \*const p\_api\_ctrl, usb\_cfg\_t const \*const p\_cfg)

Start the USB module

#### Implemented as

- R\_USB\_Open()

#### Parameters

[in]	p_api_ctrl	Pointer to control structure.
[in]	p_cfg	Pointer to configuration structure.

## ◆ close

```
fsp_err_t(* usb_api_t::close) (usb_ctrl_t *const p_api_ctrl)
```

Stop the USB module

**Implemented as**

- R\_USB\_Close()

**Parameters**

[in]	p_api_ctrl	Pointer to control structure.
------	------------	-------------------------------

## ◆ read

```
fsp_err_t(* usb_api_t::read) (usb_ctrl_t *const p_api_ctrl, uint8_t *p_buf, uint32_t size, uint8_t destination)
```

Request USB data read

**Implemented as**

- R\_USB\_Read()

**Parameters**

[in]	p_api_ctrl	Pointer to control structure.
[in]	p_buf	Pointer to area that stores read data.
[in]	size	Read request size.
[in]	destination	In Host mode, it represents the device address, and in Peripheral mode, it represents the device class.

◆ **write**

`fsp_err_t(* usb_api_t::write) (usb_ctrl_t *const p_api_ctrl, uint8_t const *const p_buf, uint32_t size, uint8_t destination)`

Request USB data write

**Implemented as**

- [R\\_USB\\_Write\(\)](#)

**Parameters**

[in]	p_api_ctrl	Pointer to control structure.
[in]	p_buf	Pointer to area that stores write data.
[in]	size	Read request size.
[in]	destination	In Host mode, it represents the device address, and in Peripheral mode, it represents the device class.

◆ **stop**

`fsp_err_t(* usb_api_t::stop) (usb_ctrl_t *const p_api_ctrl, usb_transfer_t direction, uint8_t destination)`

Stop USB data read/write processing

**Implemented as**

- [R\\_USB\\_Stop\(\)](#)

**Parameters**

[in]	p_api_ctrl	Pointer to control structure.
[in]	direction	Receive (USB_TRANSFER_READ) or send (USB_TRANSFER_WRITE).
[in]	destination	In Host mode, it represents the device address, and in Peripheral mode, it represents the device class.

◆ **suspend**

```
fsp_err_t(* usb_api_t::suspend) (usb_ctrl_t *const p_api_ctrl)
```

Request suspend

**Implemented as**

- R\_USB\_Suspend()

**Parameters**

[in]	p_api_ctrl	Pointer to control structure.
------	------------	-------------------------------

◆ **resume**

```
fsp_err_t(* usb_api_t::resume) (usb_ctrl_t *const p_api_ctrl)
```

Request resume

**Implemented as**

- R\_USB\_Resume()

**Parameters**

[in]	p_api_ctrl	Pointer to control structure.
------	------------	-------------------------------

◆ **vbusSet**

```
fsp_err_t(* usb_api_t::vbusSet) (usb_ctrl_t *const p_api_ctrl, uint16_t state)
```

Sets VBUS supply start/stop.

**Implemented as**

- R\_USB\_VbusSet()

**Parameters**

[in]	p_api_ctrl	Pointer to control structure.
[in]	state	VBUS supply start/stop specification

## ◆ infoGet

```
fsp_err_t(* usb_api_t::infoGet) (usb_ctrl_t *const p_api_ctrl, usb_info_t *p_info, uint8_t destination)
```

Get information on USB device.

**Implemented as**

- R\_USB\_InfoGet()

**Parameters**

[in]	p_api_ctrl	Pointer to control structure.
[in]	p_info	Pointer to usb_info_t structure area.
[in]	destination	Device address for Host.

## ◆ pipeRead

```
fsp_err_t(* usb_api_t::pipeRead) (usb_ctrl_t *const p_api_ctrl, uint8_t *p_buf, uint32_t size, uint8_t pipe_number)
```

Request data read from specified pipe

**Implemented as**

- R\_USB\_PipeRead()

**Parameters**

[in]	p_api_ctrl	Pointer to control structure.
[in]	p_buf	Pointer to area that stores read data.
[in]	size	Read request size.
[in]	pipe_number	Pipe Number.

## ◆ pipeWrite

```
fsp_err_t(* usb_api_t::pipeWrite) (usb_ctrl_t *const p_api_ctrl, uint8_t *p_buf, uint32_t size, uint8_t pipe_number)
```

Request data write to specified pipe

**Implemented as**

- R\_USB\_PipeWrite()

**Parameters**

[in]	p_api_ctrl	Pointer to control structure.
[in]	p_buf	Pointer to area that stores write data.
[in]	size	Read request size.
[in]	pipe_number	Pipe Number.

## ◆ pipeStop

```
fsp_err_t(* usb_api_t::pipeStop) (usb_ctrl_t *const p_api_ctrl, uint8_t pipe_number)
```

Stop USB data read/write processing to specified pipe

**Implemented as**

- R\_USB\_PipeStop()

**Parameters**

[in]	p_api_ctrl	Pointer to control structure.
[in]	pipe_number	Pipe Number.

## ◆ usedPipesGet

```
fsp_err_t(* usb_api_t::usedPipesGet) (usb_ctrl_t *const p_api_ctrl, uint16_t *p_pipe, uint8_t destination)
```

Get pipe number

**Implemented as**

- R\_USB\_UsedPipesGet()

**Parameters**

[in]	p_api_ctrl	Pointer to control structure.
[in]	p_pipe	Pointer to area that stores the selected pipe number (bit map information).
[in]	destination	Device address for Host.



◆ **pipeInfoGet**

```
fsp_err_t(* usb_api_t::pipeInfoGet) (usb_ctrl_t *const p_api_ctrl, usb_pipe_t *p_info, uint8_t pipe_number)
```

Get pipe information

**Implemented as**

- [R\\_USB\\_PipeInfoGet\(\)](#)

**Parameters**

[in]	p_api_ctrl	Pointer to control structure.
[in]	p_info	Pointer to usb_pipe_t structure area.
[in]	pipe_number	Pipe Number.

◆ **versionGet**

```
fsp_err_t(* usb_api_t::versionGet) (fsp_version_t *const p_version)
```

Get the driver version

**Implemented as**

- [R\\_USB\\_VersionGet\(\)](#)

**Parameters**

[out]	p_version	Version number.
-------	-----------	-----------------

◆ **eventGet**

```
fsp_err_t(* usb_api_t::eventGet) (usb_ctrl_t *const p_api_ctrl, usb_status_t *event)
```

Return USB-related completed events (OS less only)

**Implemented as**

- [R\\_USB\\_EventGet\(\)](#)

**Parameters**

[in]	p_api_ctrl	Pointer to control structure.
[out]	event	Pointer to event.

◆ **callback**

`fsp_err_t(* usb_api_t::callback) (usb_callback_t *p_callback)`

Register a callback function to be called upon completion of a USB related event. (RTOS only)

**Implemented as**

- [R\\_USB\\_Callback\(\)](#)

**Parameters**

[in]	p_callback	Pointer to Callback function.
------	------------	-------------------------------

◆ **pullUp**

`fsp_err_t(* usb_api_t::pullUp) (usb_ctrl_t *const p_api_ctrl, uint8_t state)`

Pull-up enable/disable setting of D+/D- line.

**Implemented as**

- [R\\_USB\\_PullUp\(\)](#)

**Parameters**

[in]	p_api_ctrl	Pointer to control structure.
[in]	state	Pull-up enable/disable setting.

◆ **hostControlTransfer**

`fsp_err_t(* usb_api_t::hostControlTransfer) (usb_ctrl_t *const p_api_ctrl, usb_setup_t *p_setup, uint8_t *p_buf, uint8_t device_address)`

Performs settings and transmission processing when transmitting a setup packet.

**Implemented as**

- [R\\_USB\\_HostControlTransfer\(\)](#)

**Parameters**

[in]	p_api_ctrl	USB control structure.
[in]	p_setup	Setup packet information.
[in]	p_buf	Transfer area information.
[in]	device_address	Device address information.

◆ **periControlDataGet**

`fsp_err_t(* usb_api_t::periControlDataGet) (usb_ctrl_t *const p_api_ctrl, uint8_t *p_buf, uint32_t size)`

Receives data sent by control transfer.

**Implemented as**

- [R\\_USB\\_PeriControlDataGet\(\)](#)

**Parameters**

[in]	p_api_ctrl	USB control structure.
[in]	p_buf	Data reception area information.
[in]	size	Data reception size information.

◆ **periControlDataSet**

`fsp_err_t(* usb_api_t::periControlDataSet) (usb_ctrl_t *const p_api_ctrl, uint8_t *p_buf, uint32_t size)`

Performs transfer processing for control transfer.

**Implemented as**

- [R\\_USB\\_PeriControlDataSet\(\)](#)

**Parameters**

[in]	p_api_ctrl	USB control structure.
[in]	p_buf	Area information for data transfer.
[in]	size	Transfer size information.

◆ **periControlStatusSet**

`fsp_err_t(* usb_api_t::periControlStatusSet) (usb_ctrl_t *const p_api_ctrl, usb_setup_status_t status)`

Set the response to the setup packet.

**Implemented as**

- [R\\_USB\\_PeriControlStatusSet\(\)](#)

**Parameters**

[in]	p_api_ctrl	USB control structure.
[in]	status	USB port startup information.

◆ **remoteWakeup**

```
fsp_err_t(* usb_api_t::remoteWakeup) (usb_ctrl_t *const p_api_ctrl)
```

Sends a remote wake-up signal to the connected Host.

**Implemented as**

- R\_USB\_RemoteWakeup()

**Parameters**

[in]	p_api_ctrl	USB control structure.
------	------------	------------------------

◆ **moduleNumberGet**

```
fsp_err_t(* usb_api_t::moduleNumberGet) (usb_ctrl_t *const p_api_ctrl, uint8_t *module_number)
```

This API gets the module number.

**Implemented as**

- R\_USB\_ModuleNumberGet()

**Parameters**

[in]	p_api_ctrl	USB control structure.
[out]	module_number	Module number to get.

◆ **classTypeGet**

```
fsp_err_t(* usb_api_t::classTypeGet) (usb_ctrl_t *const p_api_ctrl, usb_class_t *class_type)
```

This API gets the module number.

**Implemented as**

- R\_USB\_ClassTypeGet()

**Parameters**

[in]	p_api_ctrl	USB control structure.
[out]	class_type	Class type to get.

◆ **deviceAddressGet**

```
fsp_err_t(* usb_api_t::deviceAddressGet) (usb_ctrl_t *const p_api_ctrl, uint8_t *device_address)
```

This API gets the device address.

**Implemented as**

- [R\\_USB\\_DeviceAddressGet\(\)](#)

**Parameters**

[in]	p_api_ctrl	USB control structure.
[out]	device_address	Device address to get.

◆ **pipeNumberGet**

```
fsp_err_t(* usb_api_t::pipeNumberGet) (usb_ctrl_t *const p_api_ctrl, uint8_t *pipe_number)
```

This API gets the pipe number.

**Implemented as**

- [R\\_USB\\_PipeNumberGet\(\)](#)

**Parameters**

[in]	p_api_ctrl	USB control structure.
[out]	pipe_number	Pipe number to get.

◆ **deviceStateGet**

```
fsp_err_t(* usb_api_t::deviceStateGet) (usb_ctrl_t *const p_api_ctrl, uint16_t *state)
```

This API gets the state of the device.

**Implemented as**

- [R\\_USB\\_DeviceStateGet\(\)](#)

**Parameters**

[in]	p_api_ctrl	USB control structure.
[out]	state	Device state to get.

◆ **dataSizeGet**

```
fsp_err_t(* usb_api_t::dataSizeGet) (usb_ctrl_t *const p_api_ctrl, uint32_t *data_size)
```

This API gets the data size.

**Implemented as**

- R\_USB\_DataSizeGet()

**Parameters**

[in]	p_api_ctrl	USB control structure.
[out]	data_size	Data size to get.

◆ **setupGet**

```
fsp_err_t(* usb_api_t::setupGet) (usb_ctrl_t *const p_api_ctrl, usb_setup_t *setup)
```

This API gets the setup type.

**Implemented as**

- R\_USB\_SetupGet()

**Parameters**

[in]	p_api_ctrl	USB control structure.
[out]	setup	Setup type to get.

◆ **usb\_instance\_t**

```
struct usb_instance_t
```

This structure encompasses everything that is needed to use an instance of this interface.

## Data Fields

usb_ctrl_t *	p_ctrl	Pointer to the control structure for this instance.
usb_cfg_t const *	p_cfg	Pointer to the configuration structure for this instance.
usb_api_t const *	p_api	Pointer to the API structure for this instance.

**Enumeration Type Documentation**

◆ **usb\_speed\_t**

enum <code>usb_speed_t</code>	
USB speed type	
Enumerator	
<code>USB_SPEED_LS</code>	Low speed operation.
<code>USB_SPEED_FS</code>	Full speed operation.
<code>USB_SPEED_HS</code>	Hi speed operation.

◆ **usb\_setup\_status\_t**

enum <code>usb_setup_status_t</code>	
USB request result	
Enumerator	
<code>USB_SETUP_STATUS_ACK</code>	ACK response.
<code>USB_SETUP_STATUS_STALL</code>	STALL response.

◆ **usb\_status\_t**

enum <code>usb_status_t</code>	
USB driver status	
Enumerator	
<code>USB_STATUS_POWERED</code>	Powered State.
<code>USB_STATUS_DEFAULT</code>	Default State.
<code>USB_STATUS_ADDRESS</code>	Address State.
<code>USB_STATUS_CONFIGURED</code>	Configured State.
<code>USB_STATUS_SUSPEND</code>	Suspend State.
<code>USB_STATUS_RESUME</code>	Resume State.
<code>USB_STATUS_DETACH</code>	Detach State.
<code>USB_STATUS_REQUEST</code>	Request State.
<code>USB_STATUS_REQUEST_COMPLETE</code>	Request Complete State.
<code>USB_STATUS_READ_COMPLETE</code>	Read Complete State.
<code>USB_STATUS_WRITE_COMPLETE</code>	Write Complete State.
<code>USB_STATUS_BC</code>	battery Charge State
<code>USB_STATUS_OVERCURRENT</code>	Over Current state.
<code>USB_STATUS_NOT_SUPPORT</code>	Device Not Support.
<code>USB_STATUS_NONE</code>	None Status.
<code>USB_STATUS_MSC_CMD_COMPLETE</code>	MSC_CMD Complete.



◆ **usb\_class\_t**

enum <code>usb_class_t</code>	
USB class type	
Enumerator	
<code>USB_CLASS_PCDC</code>	PCDC Class.
<code>USB_CLASS_PCDCC</code>	PCDCC Class.
<code>USB_CLASS_PHID</code>	PHID Class.
<code>USB_CLASS_PVND</code>	PVND Class.
<code>USB_CLASS_HCDC</code>	HCDC Class.
<code>USB_CLASS_HCDCC</code>	HCDCC Class.
<code>USB_CLASS_HHID</code>	HHID Class.
<code>USB_CLASS_HVND</code>	HVND Class.
<code>USB_CLASS_HMSC</code>	HMSC Class.
<code>USB_CLASS_PMSC</code>	PMSC Class.
<code>USB_CLASS_REQUEST</code>	USB Class Request.
<code>USB_CLASS_END</code>	USB Class End Code.

◆ **usb\_bcport\_t**

enum <code>usb_bcport_t</code>	
USB battery charging type	
Enumerator	
<code>USB_BCPORT_SDP</code>	SDP port settings.
<code>USB_BCPORT_CDP</code>	CDP port settings.
<code>USB_BCPORT_DCP</code>	DCP port settings.

◆ **usb\_onoff\_t**

enum <code>usb_onoff_t</code>	
USB status	
Enumerator	
USB_OFF	USB Off State.
USB_ON	USB On State.

◆ **usb\_transfer\_t**

enum <code>usb_transfer_t</code>	
USB read/write type	
Enumerator	
USB_TRANSFER_READ	Data Receive communication.
USB_TRANSFER_WRITE	Data transmission communication.

◆ **usb\_transfer\_type\_t**

enum <code>usb_transfer_type_t</code>	
USB transfer type	
Enumerator	
USB_TRANSFER_TYPE_BULK	Bulk communication.
USB_TRANSFER_TYPE_INT	Interrupt communication.
USB_TRANSFER_TYPE_ISO	Isochronous communication.

◆ **usb\_mode\_t**

enum <code>usb_mode_t</code>	
Enumerator	
USB_MODE_HOST	Host mode.
USB_MODE_PERI	Peripheral mode.

◆ **usb\_compliancetest\_status\_t**

enum usb_compliancetest_status_t	
Enumerator	
USB_COMPLIANCETEST_ATTACH	Device Attach Detection.
USB_COMPLIANCETEST_DETACH	Device Detach Detection.
USB_COMPLIANCETEST_TPL	TPL device connect.
USB_COMPLIANCETEST_NOTTPL	Not TPL device connect.
USB_COMPLIANCETEST_HUB	USB Hub connect.
USB_COMPLIANCETEST_OVRC	Over current.
USB_COMPLIANCETEST_NORES	Response Time out for Control Read Transfer.
USB_COMPLIANCETEST_SETUP_ERR	Setup Transaction Error.

**4.3.38 USB HCDC Interface**[Interfaces](#)**Detailed Description**

Interface for USB HCDC functions.

**Summary**

The USB HCDC interface provides USB HCDC functionality.

The USB HCDC interface can be implemented by:

- [USB Host Communications Device Class Driver \(r\\_usb\\_hcdc\)](#)

**Data Structures**

struct [usb\\_hcdc\\_encapsulated\\_t](#)

struct [usb\\_hcdc\\_abstractstate\\_t](#)

struct [usb\\_hcdc\\_countrysetting\\_t](#)

union [usb\\_hcdc\\_commfeature\\_t](#)

struct [usb\\_hcdc\\_linecoding\\_t](#)

struct [usb\\_hcdc\\_controllinestate\\_t](#)

struct [usb\\_hcdc\\_serialstate\\_t](#)

struct [usb\\_hcdc\\_breakduration\\_t](#)

## Enumerations

enum [usb\\_hcdc\\_data\\_bit\\_t](#)

enum [usb\\_hcdc\\_stop\\_bit\\_t](#)

enum [usb\\_hcdc\\_parity\\_bit\\_t](#)

enum [usb\\_hcdc\\_line\\_speed\\_t](#)

enum [usb\\_hcdc\\_feature\\_selector\\_t](#)

## Data Structure Documentation

### ◆ [usb\\_hcdc\\_encapsulated\\_t](#)

struct <a href="#">usb_hcdc_encapsulated_t</a>		
Encapsulated data		
Data Fields		
uint8_t *	p_data	Protocol dependent data.
uint16_t	wlength	Data length in bytes.

### ◆ [usb\\_hcdc\\_abstractstate\\_t](#)

struct <a href="#">usb_hcdc_abstractstate_t</a>		
Abstract Control Model (ACM) settings bitmap		
Data Fields		
uint16_t	bis: 1	Idle enable.
uint16_t	bdms: 1	Data multiplexing enable.
uint16_t	rsv: 14	Reserved.

### ◆ [usb\\_hcdc\\_countrysetting\\_t](#)

struct <a href="#">usb_hcdc_countrysetting_t</a>		
Country code data		
Data Fields		

uint16_t	country_code	Country code.
----------	--------------	---------------

◆ **usb\_hcdc\_commfeature\_t**

union usb_hcdc_commfeature_t		
Feature setting data		
Data Fields		
usb_hcdc_abstractstate_t	abstract_state	ACM settings bitmap.
usb_hcdc_countrysetting_t	country_setting	Country code.

◆ **usb\_hcdc\_linecoding\_t**

struct usb_hcdc_linecoding_t		
Virtual UART configuration (line coding)		
Data Fields		
usb_hcdc_line_speed_t	dwote_rate	Data terminal rate in bits per second.
usb_hcdc_stop_bit_t	bchar_format	Stop bits.
usb_hcdc_parity_bit_t	bparity_type	Parity.
usb_hcdc_data_bit_t	bdata_bits	Data bits.
uint8_t	rsv	Reserved.

◆ **usb\_hcdc\_controllinestate\_t**

struct usb_hcdc_controllinestate_t		
Virtual UART control signal bitmap		
Data Fields		
uint16_t	bdtr: 1	DTR.
uint16_t	brts: 1	RTS.
uint16_t	rsv: 14	Reserved.

◆ **usb\_hcdc\_serialstate\_t**

struct usb_hcdc_serialstate_t		
Virtual UART state bitmap		
Data Fields		
uint16_t	brx_carrier: 1	DCD signal.
uint16_t	btx_carrier: 1	DSR signal.
uint16_t	bbreak: 1	Break detection status.
uint16_t	bring_signal: 1	Ring signal.
uint16_t	bframing: 1	Framing error.

uint16_t	bparity: 1	Parity error.
uint16_t	bover_run: 1	Over Run error.
uint16_t	rsv: 9	Reserved.

#### ◆ usb\_hcdc\_breakduration\_t

struct usb_hcdc_breakduration_t		
Break duration data		
Data Fields		
uint16_t	wtime_ms	Duration of Break.

### Enumeration Type Documentation

#### ◆ usb\_hcdc\_data\_bit\_t

enum usb_hcdc_data_bit_t	
Virtual UART data length	
Enumerator	
USB_HCDC_DATA_BIT_7	7 bits
USB_HCDC_DATA_BIT_8	8 bits

#### ◆ usb\_hcdc\_stop\_bit\_t

enum usb_hcdc_stop_bit_t	
Virtual UART stop bit length	
Enumerator	
USB_HCDC_STOP_BIT_1	1 bit
USB_HCDC_STOP_BIT_15	1.5 bits
USB_HCDC_STOP_BIT_2	2 bits

◆ **usb\_hcdc\_parity\_bit\_t**

enum <code>usb_hcdc_parity_bit_t</code>	
Virtual UART parity bit setting	
Enumerator	
USB_HCDC_PARITY_BIT_NONE	No parity bit.
USB_HCDC_PARITY_BIT_ODD	Odd parity.
USB_HCDC_PARITY_BIT_EVEN	Even parity.

◆ **usb\_hcdc\_line\_speed\_t**

enum <code>usb_hcdc_line_speed_t</code>
Virtual UART bitrate

◆ **usb\_hcdc\_feature\_selector\_t**

enum <code>usb_hcdc_feature_selector_t</code>
Feature Selector

## 4.3.39 USB HHID Interface

### Interfaces

#### Detailed Description

Interface for USB HHID functions.

## Summary

The USB HHID interface provides USB HHID functionality.

The USB HHID interface can be implemented by:

- [USB Host Human Interface Device Class Driver \(r\\_usb\\_hhid\)](#)

#### Data Structures

```
struct usb_hhid_api_t
```

```
struct usb_hhid_instance_t
```

## Macros

```
#define USB_HID_OTHER
```

Other.

```
#define USB_HID_KEYBOARD
```

Keyboard.

```
#define USB_HID_MOUSE
```

Mouse.

```
#define USB_HID_IN
```

In Transfer.

```
#define USB_HID_OUT
```

Out Transfer.

## Data Structure Documentation

### ◆ usb\_hhid\_api\_t

```
struct usb_hhid_api_t
```

USB HHID functions implemented at the HAL layer will follow this API.

#### Data Fields

<code>fsp_err_t(*)</code>	<code>typeGet</code> (usb_ctrl_t *const p_api_ctrl, uint8_t *p_type, uint8_t device_address)
---------------------------	----------------------------------------------------------------------------------------------

<code>fsp_err_t(*)</code>	<code>maxPacketSizeGet</code> (usb_ctrl_t *const p_api_ctrl, uint16_t *p_size, uint8_t direction, uint8_t device_address)
---------------------------	---------------------------------------------------------------------------------------------------------------------------

## Field Documentation



◆ **typeGet**

```
fsp_err_t(* usb_hhid_api_t::typeGet) (usb_ctrl_t *const p_api_ctrl, uint8_t *p_type, uint8_t device_address)
```

Get HID protocol.(USB Mouse/USB Keyboard/Other Type.)

**Implemented as**

- R\_USB\_HHID\_TypeGet()

**Parameters**

[in]	p_api_ctrl	Pointer to control structure.
[in]	p_type	Pointer to store HID protocol value.
[in]	device_address	Device Address.

◆ **maxPacketSizeGet**

```
fsp_err_t(* usb_hhid_api_t::maxPacketSizeGet) (usb_ctrl_t *const p_api_ctrl, uint16_t *p_size, uint8_t direction, uint8_t device_address)
```

Obtains max packet size for the connected HID device. The max packet size is set to the area. Set the direction (USB\_HID\_IN/USB\_HID\_OUT).

**Implemented as**

- R\_USB\_HHID\_MaxPacketSizeGet()

**Parameters**

[in]	p_api_ctrl	Pointer to control structure.
[in]	p_size	Pointer to the area to store the max package size.
[in]	direction	Transfer direction.
[in]	device_address	Device Address.

◆ **usb\_hhid\_instance\_t**

```
struct usb_hhid_instance_t
```

This structure encompasses everything that is needed to use an instance of this interface.

## Data Fields

usb_ctrl_t *	p_ctrl	Pointer to the control structure for this instance.
usb_cfg_t const *	p_cfg	Pointer to the configuration structure for this instance.
usb_hhid_api_t const *	p_api	Pointer to the API structure for this instance.

## 4.3.40 USB HMSC Interface

### Interfaces

#### Detailed Description

Interface for USB HMSC functions.

## Summary

The USB HMSC interface provides USB HMSC functionality.

The USB HMSC interface can be implemented by:

- [USB Host Mass Storage Class Driver \(r\\_usb\\_hmsc\)](#)

#### Data Structures

struct [usb\\_hmsc\\_api\\_t](#)

#### Enumerations

enum [usb\\_atapi\\_t](#)

enum [usb\\_csw\\_result\\_t](#)

#### Data Structure Documentation

##### ◆ [usb\\_hmsc\\_api\\_t](#)

struct [usb\\_hmsc\\_api\\_t](#)

USB HMSC functions implemented at the HAL layer will follow this API.

#### Data Fields

<a href="#">fsp_err_t</a> (*	<a href="#">storageCommand</a> )( <a href="#">usb_ctrl_t</a> *const p_api_ctrl, <a href="#">uint8_t</a> *buf, <a href="#">uint8_t</a> command, <a href="#">uint8_t</a> destination)
<a href="#">fsp_err_t</a> (*	<a href="#">driveNumberGet</a> )( <a href="#">usb_ctrl_t</a> *const p_api_ctrl, <a href="#">uint8_t</a> *p_drive, <a href="#">uint8_t</a> destination)
<a href="#">fsp_err_t</a> (*	<a href="#">storageReadSector</a> )( <a href="#">uint16_t</a> drive_number, <a href="#">uint8_t</a> *const buff, <a href="#">uint32_t</a> sector_number, <a href="#">uint16_t</a> sector_count)
<a href="#">fsp_err_t</a> (*	<a href="#">storageWriteSector</a> )( <a href="#">uint16_t</a> drive_number, <a href="#">uint8_t</a> const *const buff, <a href="#">uint32_t</a> sector_number, <a href="#">uint16_t</a> sector_count)

fsp_err_t(*)	semaphoreGet )(void)
--------------	----------------------

fsp_err_t(*)	semaphoreRelease )(void)
--------------	--------------------------

## Field Documentation

### ◆ storageCommand

fsp\_err\_t(\* usb\_hmsc\_api\_t::storageCommand) (usb\_ctrl\_t \*const p\_api\_ctrl, uint8\_t \*buf, uint8\_t command, uint8\_t destination)

Processing for MassStorage(ATAPI) command.

#### Implemented as

- R\_USB\_HMSC\_StorageCommand()

#### Parameters

[in]	p_api_ctrl	Pointer to control structure.
[in]	*buf	Pointer to the buffer area to store the transfer data.
[in]	command	ATAPI command.
[in]	destination	Represents a device address.

### ◆ driveNumberGet

fsp\_err\_t(\* usb\_hmsc\_api\_t::driveNumberGet) (usb\_ctrl\_t \*const p\_api\_ctrl, uint8\_t \*p\_drive, uint8\_t destination)

Get number of Storage drive.

#### Implemented as

- R\_USB\_HMSC\_DriveNumberGet()

#### Parameters

[in]	p_api_ctrl	Pointer to control structure.
[out]	p_drive	Store address for Drive No.
[in]	destination	Represents a device address.

### ◆ storageReadSector

`fsp_err_t(*usb_hmsc_api_t::storageReadSector)(uint16_t drive_number, uint8_t *const buff, uint32_t sector_number, uint16_t sector_count)`

Read sector information.

#### Implemented as

- [R\\_USB\\_HMSC\\_StorageReadSector\(\)](#)

#### Parameters

[in]	drive_number	Drive number.
[out]	*buff	Pointer to the buffer area to store the transfer data.
[in]	sector_number	The sector number to start with.
[in]	sector_count	Transmit with the sector size of the number of times.

### ◆ storageWriteSector

`fsp_err_t(*usb_hmsc_api_t::storageWriteSector)(uint16_t drive_number, uint8_t const *const buff, uint32_t sector_number, uint16_t sector_count)`

Write sector information.

#### Implemented as

- [R\\_USB\\_HMSC\\_StorageWriteSector\(\)](#)

#### Parameters

[in]	drive_number	Drive number.
[in]	*buff	Pointer to the buffer area to store the transfer data.
[in]	sector_number	The sector number to start with.
[in]	sector_count	Transmit with the sector size of the number of times.

### ◆ semaphoreGet

`fsp_err_t(*usb_hmsc_api_t::semaphoreGet)(void)`

Get Semaphore.

#### Implemented as

- [R\\_USB\\_HMSC\\_SemaphoreGet\(\)](#)

**◆ semaphoreRelease**`fsp_err_t(* usb_hmsc_api_t::semaphoreRelease) (void)`

Release Semaphore.

**Implemented as**

- `R_USB_HMSC_SemaphoreRelease()`

**Enumeration Type Documentation**

◆ **usb\_atapi\_t**

enum <code>usb_atapi_t</code>	
ATAPI commands	
Enumerator	
<code>USB_ATAPI_TEST_UNIT_READY</code>	Test Unit Ready.
<code>USB_ATAPI_REQUEST_SENSE</code>	Request Sense.
<code>USB_ATAPI_FORMAT_UNIT</code>	Format Unit.
<code>USB_ATAPI_INQUIRY</code>	Inquiry.
<code>USB_ATAPI_MODE_SELECT6</code>	Mode Select6.
<code>USB_ATAPI_MODE_SENSE6</code>	Mode Sense6.
<code>USB_ATAPI_START_STOP_UNIT</code>	Start Stop Unit.
<code>USB_ATAPI_PREVENT_ALLOW</code>	Prevent Allow.
<code>USB_ATAPI_READ_FORMAT_CAPACITY</code>	Read Format Capacity.
<code>USB_ATAPI_READ_CAPACITY</code>	Read Capacity.
<code>USB_ATAPI_READ10</code>	Read10.
<code>USB_ATAPI_WRITE10</code>	Write10.
<code>USB_ATAPI_SEEK</code>	Seek.
<code>USB_ATAPI_WRITE_AND_VERIFY</code>	Write and Verify.
<code>USB_ATAPI_VERIFY10</code>	Verify10.
<code>USB_ATAPI_MODE_SELECT10</code>	Mode Select10.
<code>USB_ATAPI_MODE_SENSE10</code>	Mode Sense10.

◆ **usb\_csw\_result\_t**

enum usb_csw_result_t	
Command Status Wrapper (CSW)	
Enumerator	
USB_CSW_RESULT_SUCCESS	CSW was successful.
USB_CSW_RESULT_FAIL	CSW failed.
USB_CSW_RESULT_PHASE	CSW has phase error.

**4.3.41 USB PCDC Interface**[Interfaces](#)**Detailed Description**

Interface for USB PCDC functions.

**Summary**

The USB PCDC interface provides USB PCDC functionality.

The USB PCDC interface can be implemented by:

- [USB Peripheral Communications Device Class \(r\\_usb\\_pcdc\)](#)

**Data Structures**

```
struct usb_serial_state_bitmap_t
```

```
union usb_sci_serialstate_t
```

```
struct usb_pcdc_linecoding_t
```

```
struct usb_pcdc_ctrllinestate_t
```

**Macros**

```
#define USB_PCDC_SET_LINE_CODING
Set Line Coding.
```

```
#define USB_PCDC_GET_LINE_CODING
```

Get Line Coding.

```
#define USB_PCDC_SET_CONTROL_LINE_STATE
```

Control Line State.

```
#define USB_PCDC_SERIAL_STATE
```

Serial State Code.

```
#define USB_PCDC_SETUP_TBL_BSIZE
```

Setup packet table size (uint16\_t \* 5)

## Data Structure Documentation

### ◆ usb\_serial\_state\_bitmap\_t

struct usb_serial_state_bitmap_t		
Virtual UART signal state		
Data Fields		
uint16_t	b_rx_carrier: 1	DCD signal.
uint16_t	b_tx_carrier: 1	DSR signal.
uint16_t	b_break: 1	Break signal.
uint16_t	b_ring_signal: 1	Ring signal.
uint16_t	b_framing: 1	Framing error.
uint16_t	b_parity: 1	Parity error.
uint16_t	b_over_run: 1	Overrun error.
uint16_t	rsv: 9	Reserved.

### ◆ usb\_sci\_serialstate\_t

union usb_sci_serialstate_t		
Class Notification Serial State		
Data Fields		
uint32_t	word	Word Access.
<a href="#">usb_serial_state_bitmap_t</a>	bit	Bit Access.

### ◆ usb\_pcdc\_linecoding\_t

struct usb_pcdc_linecoding_t



Virtual UART communication settings		
Data Fields		
uint32_t	dw_dte_rate	Bitrate.
uint8_t	b_char_format	Stop bits.
uint8_t	b_parity_type	Parity.
uint8_t	b_data_bits	Data bits.
uint8_t	rsv	Reserved.

#### ◆ usb\_pcdc\_ctrllinestate\_t

struct usb_pcdc_ctrllinestate_t		
Virtual UART control line state		
Data Fields		
uint16_t	bdtr: 1	DTR.
uint16_t	brts: 1	RTS.
uint16_t	rsv: 14	Reserved.

### 4.3.42 USB PHID Interface

#### Interfaces

#### Detailed Description

Interface for USB PHID functions.

### Summary

The USB interface provides USB functionality.

The USB PHID interface can be implemented by:

- [USB Peripheral Human Interface Device Class \(r\\_usb\\_phid\)](#)

### 4.3.43 USB PMSC Interface

#### Interfaces

#### Detailed Description

Interface for USB PMSC functions.

## Summary

The USB PMSC interface provides USB PMSC functionality.

The USB PMSC interface can be implemented by:

- [USB Peripheral Mass Storage Class \(r\\_usb\\_pmsc\)](#)

### Macros

```
#define USB_MASS_STORAGE_RESET
    Mass storage reset request code.
```

```
#define USB_GET_MAX_LUN
    Get max logical unit number request code.
```

## 4.3.44 WDT Interface

[Interfaces](#)

### Detailed Description

Interface for watch dog timer functions.

## Summary

The WDT interface for the Watchdog Timer (WDT) peripheral provides watchdog functionality including resetting the device or generating an interrupt.

The watchdog timer interface can be implemented by:

- [Watchdog Timer \(r\\_wdt\)](#)
- [Independent Watchdog Timer \(r\\_iwdt\)](#)

### Data Structures

```
struct wdt_callback_args_t
```

```
struct wdt_timeout_values_t
```

```
struct wdt_cfg_t
```

```
struct wdt_api_t
```

```
struct wdt_instance_t
```

## Typedefs

```
typedef void wdt_ctrl_t
```

## Enumerations

```
enum wdt_timeout_t
```

```
enum wdt_clock_division_t
```

```
enum wdt_window_start_t
```

```
enum wdt_window_end_t
```

```
enum wdt_reset_control_t
```

```
enum wdt_stop_control_t
```

```
enum wdt_status_t
```

## Data Structure Documentation

### ◆ wdt\_callback\_args\_t

struct wdt_callback_args_t		
Callback function parameter data		
Data Fields		
void const *	p_context	Placeholder for user data. Set in <a href="#">wdt_api_t::open</a> function in <a href="#">wdt_cfg_t</a> .

### ◆ wdt\_timeout\_values\_t

struct wdt_timeout_values_t		
WDT timeout data. Used to return frequency of WDT clock and timeout period		
Data Fields		
uint32_t	clock_frequency_hz	Frequency of watchdog clock after divider.
uint32_t	timeout_ticks	Timeout period in units of watchdog clock ticks.

### ◆ wdt\_cfg\_t

struct wdt_cfg_t		
WDT configuration parameters.		

Data Fields	
<code>wdt_timeout_t</code>	<code>timeout</code>
	Timeout period.
<code>wdt_clock_division_t</code>	<code>clock_division</code>
	Clock divider.
<code>wdt_window_start_t</code>	<code>window_start</code>
	Refresh permitted window start position.
<code>wdt_window_end_t</code>	<code>window_end</code>
	Refresh permitted window end position.
<code>wdt_reset_control_t</code>	<code>reset_control</code>
	Select NMI or reset generated on underflow.
<code>wdt_stop_control_t</code>	<code>stop_control</code>
	Select whether counter operates in sleep mode.
<code>void(*</code>	<code>p_callback</code> <code>)(wdt_callback_args_t *p_args)</code>
	Callback provided when a WDT NMI ISR occurs.
<code>void const *</code>	<code>p_context</code>
<code>void const *</code>	<code>p_extend</code>
	Placeholder for user extension.
Field Documentation	

◆ **p\_context**

```
void const* wdt_cfg_t::p_context
```

Placeholder for user data. Passed to the user callback in [wdt\\_callback\\_args\\_t](#).

◆ **wdt\_api\_t**

```
struct wdt_api_t
```

WDT functions implemented at the HAL layer will follow this API.

**Data Fields**

<a href="#">fsp_err_t</a> (*	<a href="#">open</a> )(wdt_ctrl_t *const p_ctrl, wdt_cfg_t const *const p_cfg)
------------------------------	--------------------------------------------------------------------------------

<a href="#">fsp_err_t</a> (*	<a href="#">refresh</a> )(wdt_ctrl_t *const p_ctrl)
------------------------------	-----------------------------------------------------

<a href="#">fsp_err_t</a> (*	<a href="#">statusGet</a> )(wdt_ctrl_t *const p_ctrl, wdt_status_t *const p_status)
------------------------------	-------------------------------------------------------------------------------------

<a href="#">fsp_err_t</a> (*	<a href="#">statusClear</a> )(wdt_ctrl_t *const p_ctrl, const wdt_status_t status)
------------------------------	------------------------------------------------------------------------------------

<a href="#">fsp_err_t</a> (*	<a href="#">counterGet</a> )(wdt_ctrl_t *const p_ctrl, uint32_t *const p_count)
------------------------------	---------------------------------------------------------------------------------

<a href="#">fsp_err_t</a> (*	<a href="#">timeoutGet</a> )(wdt_ctrl_t *const p_ctrl, wdt_timeout_values_t *const p_timeout)
------------------------------	-----------------------------------------------------------------------------------------------

<a href="#">fsp_err_t</a> (*	<a href="#">callbackSet</a> )(wdt_ctrl_t *const p_api_ctrl, void(*p_callback)(wdt_callback_args_t *), void const *const p_context, wdt_callback_args_t *const p_callback_memory)
------------------------------	----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------

<a href="#">fsp_err_t</a> (*	<a href="#">versionGet</a> )(fsp_version_t *const p_data)
------------------------------	-----------------------------------------------------------

**Field Documentation**

◆ **open**

```
fsp_err_t(* wdt_api_t::open) (wdt_ctrl_t *const p_ctrl, wdt_cfg_t const *const p_cfg)
```

Initialize the WDT in register start mode. In auto-start mode with NMI output it registers the NMI callback.

**Implemented as**

- R\_WDT\_Open()
- R\_IWDT\_Open()

**Parameters**

[in]	p_ctrl	Pointer to control structure.
[in]	p_cfg	Pointer to pin configuration structure.

◆ **refresh**

```
fsp_err_t(* wdt_api_t::refresh) (wdt_ctrl_t *const p_ctrl)
```

Refresh the watchdog timer.

**Implemented as**

- R\_WDT\_Refresh()
- R\_IWDT\_Refresh()

**Parameters**

[in]	p_ctrl	Pointer to control structure.
------	--------	-------------------------------

◆ **statusGet**

```
fsp_err_t(* wdt_api_t::statusGet) (wdt_ctrl_t *const p_ctrl, wdt_status_t *const p_status)
```

Read the status of the WDT.

**Implemented as**

- R\_WDT\_StatusGet()
- R\_IWDT\_StatusGet()

**Parameters**

[in]	p_ctrl	Pointer to control structure.
[out]	p_status	Pointer to variable to return status information through.

◆ **statusClear**

```
fsp_err_t(* wdt_api_t::statusClear) (wdt_ctrl_t *const p_ctrl, const wdt_status_t status)
```

Clear the status flags of the WDT.

**Implemented as**

- R\_WDT\_StatusClear()
- R\_IWDT\_StatusClear()

**Parameters**

[in]	p_ctrl	Pointer to control structure.
[in]	status	Status condition(s) to clear.

◆ **counterGet**

```
fsp_err_t(* wdt_api_t::counterGet) (wdt_ctrl_t *const p_ctrl, uint32_t *const p_count)
```

Read the current WDT counter value.

**Implemented as**

- R\_WDT\_CounterGet()
- R\_IWDT\_CounterGet()

**Parameters**

[in]	p_ctrl	Pointer to control structure.
[out]	p_count	Pointer to variable to return current WDT counter value.

◆ **timeoutGet**

```
fsp_err_t(* wdt_api_t::timeoutGet) (wdt_ctrl_t *const p_ctrl, wdt_timeout_values_t *const p_timeout)
```

Read the watchdog timeout values.

**Implemented as**

- R\_WDT\_TimeoutGet()
- R\_IWDT\_TimeoutGet()

**Parameters**

[in]	p_ctrl	Pointer to control structure.
[out]	p_timeout	Pointer to structure to return timeout values.

◆ **callbackSet**

```
fsp_err_t(* wdt_api_t::callbackSet) (wdt_ctrl_t *const p_api_ctrl,
void(*p_callback)(wdt_callback_args_t *), void const *const p_context, wdt_callback_args_t *const
p_callback_memory)
```

Specify callback function and optional context pointer and working memory pointer.

**Implemented as**

- R\_WDT\_CallbackSet()

**Parameters**

[in]	p_ctrl	Pointer to the WDT control block.
[in]	p_callback	Callback function
[in]	p_context	Pointer to send to callback function
[in]	p_working_memory	Pointer to volatile memory where callback structure can be allocated. Callback arguments allocated here are only valid during the callback.

◆ **versionGet**

```
fsp_err_t(* wdt_api_t::versionGet) (fsp_version_t *const p_data)
```

Return the version of the driver.

**Implemented as**

- R\_WDT\_VersionGet()
- R\_IWDT\_VersionGet()

**Parameters**

[in]	p_ctrl	Pointer to control structure.
[out]	p_data	Memory address to return version information to.

◆ **wdt\_instance\_t**

```
struct wdt_instance_t
```

This structure encompasses everything that is needed to use an instance of this interface.

## Data Fields

wdt_ctrl_t *	p_ctrl	Pointer to the control structure for this instance.
wdt_cfg_t const *	p_cfg	Pointer to the configuration



		structure for this instance.
<code>wdt_api_t</code> const *	<code>p_api</code>	Pointer to the API structure for this instance.

## Typedef Documentation

### ◆ `wdt_ctrl_t`

typedef void `wdt_ctrl_t`

WDT control block. Allocate an instance specific control block to pass into the WDT API calls.

#### Implemented as

- `wdt_instance_ctrl_t`
- `iwdt_instance_ctrl_t`

## Enumeration Type Documentation

### ◆ `wdt_timeout_t`

enum `wdt_timeout_t`

WDT time-out periods.

#### Enumerator

<code>WDT_TIMEOUT_128</code>	128 clock cycles
<code>WDT_TIMEOUT_512</code>	512 clock cycles
<code>WDT_TIMEOUT_1024</code>	1024 clock cycles
<code>WDT_TIMEOUT_2048</code>	2048 clock cycles
<code>WDT_TIMEOUT_4096</code>	4096 clock cycles
<code>WDT_TIMEOUT_8192</code>	8192 clock cycles
<code>WDT_TIMEOUT_16384</code>	16384 clock cycles

◆ **wdt\_clock\_division\_t**

enum <code>wdt_clock_division_t</code>	
WDT clock division ratio.	
Enumerator	
<code>WDT_CLOCK_DIVISION_1</code>	CLK/1.
<code>WDT_CLOCK_DIVISION_4</code>	CLK/4.
<code>WDT_CLOCK_DIVISION_16</code>	CLK/16.
<code>WDT_CLOCK_DIVISION_32</code>	CLK/32.
<code>WDT_CLOCK_DIVISION_64</code>	CLK/64.
<code>WDT_CLOCK_DIVISION_128</code>	CLK/128.
<code>WDT_CLOCK_DIVISION_256</code>	CLK/256.
<code>WDT_CLOCK_DIVISION_512</code>	CLK/512.
<code>WDT_CLOCK_DIVISION_2048</code>	CLK/2048.
<code>WDT_CLOCK_DIVISION_8192</code>	CLK/8192.

◆ **wdt\_window\_start\_t**

enum <code>wdt_window_start_t</code>	
WDT refresh permitted period window start position.	
Enumerator	
<code>WDT_WINDOW_START_25</code>	Start position = 25%.
<code>WDT_WINDOW_START_50</code>	Start position = 50%.
<code>WDT_WINDOW_START_75</code>	Start position = 75%.
<code>WDT_WINDOW_START_100</code>	Start position = 100%.

◆ **wdt\_window\_end\_t**

enum <a href="#">wdt_window_end_t</a>	
WDT refresh permitted period window end position.	
Enumerator	
WDT_WINDOW_END_75	End position = 75%.
WDT_WINDOW_END_50	End position = 50%.
WDT_WINDOW_END_25	End position = 25%.
WDT_WINDOW_END_0	End position = 0%.

◆ **wdt\_reset\_control\_t**

enum <a href="#">wdt_reset_control_t</a>	
WDT Counter underflow and refresh error control.	
Enumerator	
WDT_RESET_CONTROL_NMI	NMI request when counter underflows.
WDT_RESET_CONTROL_RESET	Reset request when counter underflows.

◆ **wdt\_stop\_control\_t**

enum <a href="#">wdt_stop_control_t</a>	
WDT Counter operation in sleep mode.	
Enumerator	
WDT_STOP_CONTROL_DISABLE	Count will not stop when device enters sleep mode.
WDT_STOP_CONTROL_ENABLE	Count will automatically stop when device enters sleep mode.

◆ **wdt\_status\_t**

enum <code>wdt_status_t</code>	
WDT status	
Enumerator	
<code>WDT_STATUS_NO_ERROR</code>	No status flags set.
<code>WDT_STATUS_UNDERFLOW_ERROR</code>	Underflow flag set.
<code>WDT_STATUS_REFRESH_ERROR</code>	Refresh error flag set. Refresh outside of permitted window.
<code>WDT_STATUS_UNDERFLOW_AND_REFRESH_ERROR</code>	Underflow and refresh error flags set.

**4.3.45 BLE ABS Interface**[Interfaces](#)**Detailed Description**

Interface for Bluetooth Low Energy Abstraction functions.

**Summary**

The BLE ABS interface for the Bluetooth Low Energy Abstraction (BLE ABS) peripheral provides Bluetooth Low Energy Abstraction functionality.

The Bluetooth Low Energy Abstraction interface can be implemented by:

- [Bluetooth Low Energy Abstraction \(rm\\_ble\\_abs\)](#)

**Data Structures**

struct [ble\\_device\\_address\\_t](#)

struct [ble\\_gap\\_connection\\_parameter\\_t](#)

struct [ble\\_gap\\_connection\\_phy\\_parameter\\_t](#)

struct [ble\\_gap\\_scan\\_phy\\_parameter\\_t](#)

struct [ble\\_gap\\_scan\\_on\\_t](#)

---

```

struct ble_abs_callback_args_t
struct ble_abs_pairing_parameter_t
struct ble_abs_gatt_server_callback_set_t
struct ble_abs_gatt_client_callback_set_t
struct ble_abs_legacy_advertising_parameter_t
struct ble_abs_extend_advertising_parameter_t
struct ble_abs_non_connectable_advertising_parameter_t
struct ble_abs_periodic_advertising_parameter_t
struct ble_abs_scan_phy_parameter_t
struct ble_abs_scan_parameter_t
struct ble_abs_connection_phy_parameter_t
struct ble_abs_connection_parameter_t
struct ble_abs_cfg_t
struct ble_abs_api_t
struct ble_abs_instance_t

```

## Macros

---

```

#define BLE_ABS_ADVERTISING_PHY_LEGACY
    Non-Connectable Legacy Advertising phy setting.

```

## Typedefs

---

```

typedef void(* ble_gap_application_callback_t) (uint16_t event_type, ble_status_t
event_result, st_ble_evt_data_t *p_event_data)
typedef void(* ble_vendor_specific_application_callback_t) (uint16_t event_type,
ble_status_t event_result, st_ble_vs_evt_data_t *p_event_data)
typedef void(* ble_gatt_server_application_callback_t) (uint16_t event_type,
ble_status_t event_result, st_ble_gatts_evt_data_t *p_event_data)
typedef void(* ble_gatt_client_application_callback_t) (uint16_t event_type,
ble_status_t event_result, st_ble_gattc_evt_data_t *p_event_data)

```

```
typedef void ble_abs_ctrl_t
```

## Enumerations

```
enum ble_abs_advertising_filter_t
```

## Data Structure Documentation

### ◆ ble\_device\_address\_t

struct ble_device_address_t		
st_ble_device_address is the type of bluetooth device address(BD_ADDR).		
Data Fields		
uint8_t	addr[BLE_BD_ADDR_LEN]	bluetooth device address.
uint8_t	type	the type of bluetooth device address.

### ◆ ble\_gap\_connection\_parameter\_t

struct ble_gap_connection_parameter_t		
ble_gap_connection_parameter_t is Connection parameters included in connection interval, slave latency, supervision timeout, ce length.		
Data Fields		
uint16_t	conn_intv_min	Minimum connection interval.
uint16_t	conn_intv_max	Maximum connection interval.
uint16_t	conn_latency	Slave latency.
uint16_t	sup_to	Supervision timeout.
uint16_t	min_ce_length	Minimum CE Length.
uint16_t	max_ce_length	Maximum CE Length.

### ◆ ble\_gap\_connection\_phy\_parameter\_t

struct ble_gap_connection_phy_parameter_t		
ble_gap_connection_phy_parameter_t is Connection parameters per PHY.		
Data Fields		
uint16_t	scan_intv	Scan interval.
uint16_t	scan_window	Scan window.
ble_gap_connection_parameter_t *	p_conn_param	Connection interval, slave latency, supervision timeout, and CE length.

### ◆ ble\_gap\_scan\_phy\_parameter\_t

struct ble_gap_scan_phy_parameter_t		
-------------------------------------	--	--

Scan parameters per scan PHY.

Data Fields		
uint8_t	scan_type	Scan type.
uint16_t	scan_intv	Scan interval.
uint16_t	scan_window	Scan window.

#### ◆ ble\_gap\_scan\_on\_t

Data Fields		
uint8_t	proc_type	Procedure type.
uint8_t	filter_dups	Filter duplicates.
uint16_t	duration	Scan duration.
uint16_t	period	Scan period.

#### ◆ ble\_abs\_callback\_args\_t

Data Fields		
uint32_t	channel	Select a channel corresponding to the channel number of the hardware.
<a href="#">ble_event_cb_t</a>	ble_abs_event	The event can be used to identify what caused the callback.
void const *	p_context	Placeholder for user data. Set in <a href="#">ble_abs_api_t::open</a> function in <a href="#">ble_abs_cfg_t</a> .

#### ◆ ble\_abs\_pairing\_parameter\_t

Data Fields		
uint8_t	io_capability_local_device	IO capabilities of local device.
uint8_t	mitm_protection_policy	MITM protection policy.
uint8_t	secure_connection_only	Determine whether to accept only Secure Connections or not.
uint8_t	local_key_distribute	Type of keys to be distributed from local device.

uint8_t	remote_key_distribute	Type of keys which local device requests a remote device to distribute.
uint8_t	maximum_key_size	Maximum LTK size.
uint8_t	padding[2]	padding

#### ◆ ble\_abs\_gatt\_server\_callback\_set\_t

struct ble_abs_gatt_server_callback_set_t		
GATT Server callback function and the priority.		
Data Fields		
ble_gatt_server_application_callback_t	gatt_server_callback_function	GATT Server callback function.
uint8_t	gatt_server_callback_priority	The priority number of GATT Server callback function.

#### ◆ ble\_abs\_gatt\_client\_callback\_set\_t

struct ble_abs_gatt_client_callback_set_t		
GATT Client callback function and the priority.		
Data Fields		
ble_gatt_client_application_callback_t	gatt_client_callback_function	GATT Client callback function.
uint8_t	gatt_client_callback_priority	The priority number of GATT Client callback function.

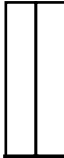
#### ◆ ble\_abs\_legacy\_advertising\_parameter\_t

struct ble_abs_legacy_advertising_parameter_t		
st_ble_abs_legacy_advertising_parameter_t is the parameters for legacy advertising.		
Data Fields		
ble_device_address_t *	p_peer_address	The remote device address. If the p_peer_address parameter is not NULL, Direct Connectable Advertising is performed to the remote address. If the p_peer_address parameter is NULL, Undirect Connectable Advertising is performed according to the advertising filter policy specified by the filter parameter.
uint8_t *	p_advertising_data	Advertising Data. If the p_advertising_data is specified as NULL, Advertising



		Data is not included in the advertising PDU.
uint8_t *	p_scan_response_data	Scan Response Data. If the p_scan_response_data is specified as NULL, Scan Response Data is not included in the advertising PDU.
uint32_t	fast_advertising_interval	Advertising with the fast_advertising_interval parameter continues for the period specified by the fast_period parameter. Time(ms) = fast_advertising_interval * 0.625. If the fast_period parameter is 0, this parameter is ignored. Valid range is 0x00000020 - 0x00FFFFFF.
uint32_t	slow_advertising_interval	After the elapse of the fast_period, advertising with the slow_advertising_interval parameter continues for the period specified by the slow_advertising_interval parameter. Time(ms) = slow_advertising_interval * 0.625. If the slow_advertising_interval parameter is 0, this parameter is ignored. Valid range is 0x00000020 - 0x00FFFFFF.
uint16_t	fast_advertising_period	The period which advertising with the fast_advertising_interval parameter continues for. Time = duration * 10ms. After the elapse of the fast_advertising_period, <a href="#">BLE_GAP_EVENT_ADV_OFF</a> event notifies that the advertising has stopped. Valid range is 0x0000 - 0xFFFF. If the fast_advertising_period parameter is 0x0000, advertising with the fast_advertising_interval parameter is not performed.
uint16_t	slow_advertising_period	The period which advertising with the

		<p>slow_advertising_interval parameter continues for. Time = duration * 10ms.</p> <p>After the elapse of the slow_advertising_period, <a href="#">BLE_GAP_EVENT_ADV_OFF</a> event notifies that the advertising has stopped.</p> <p>Valid range is 0x0000 - 0xFFFF.</p> <p>If the slow_advertising_period parameter is 0x0000, the advertising continues.</p>										
uint16_t	advertising_data_length	<p>Advertising data length(byte).</p> <p>Valid range is 0-31.</p> <p>If the advertising_data_length is 0, Advertising Data is not included in the advertising PDU.</p>										
uint16_t	scan_response_data_length	<p>Scan response data length (in bytes).</p> <p>Scan Response Data(byte).</p> <p>Valid range is 0-31.</p> <p>If the scan_response_data_length is 0, Scan Response Data is not included in the advertising PDU.</p>										
uint8_t	advertising_channel_map	<p>The channel map used for the advertising packet transmission.</p> <p>It is a bitwise OR of the following values.</p> <table border="1"> <thead> <tr> <th>macro</th> <th>description</th> </tr> </thead> <tbody> <tr> <td><a href="#">BLE_GAP_ADV_CH_37(0x01)</a></td> <td>Use 37 CH.</td> </tr> <tr> <td><a href="#">BLE_GAP_ADV_CH_38(0x02)</a></td> <td>Use 38 CH.</td> </tr> <tr> <td><a href="#">BLE_GAP_ADV_CH_39(0x04)</a></td> <td>Use 38 CH.</td> </tr> <tr> <td><a href="#">BLE_GAP_ADV_CH_ALL(0x07)</a></td> <td>Use 37 - 39 CH.</td> </tr> </tbody> </table>	macro	description	<a href="#">BLE_GAP_ADV_CH_37(0x01)</a>	Use 37 CH.	<a href="#">BLE_GAP_ADV_CH_38(0x02)</a>	Use 38 CH.	<a href="#">BLE_GAP_ADV_CH_39(0x04)</a>	Use 38 CH.	<a href="#">BLE_GAP_ADV_CH_ALL(0x07)</a>	Use 37 - 39 CH.
macro	description											
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<a href="#">BLE_GAP_ADV_CH_39(0x04)</a>	Use 38 CH.											
<a href="#">BLE_GAP_ADV_CH_ALL(0x07)</a>	Use 37 - 39 CH.											
uint8_t	advertising_filter_policy	<p>Advertising filter policy.</p> <p>If the p_peer_address parameter is NULL, the advertising is performed according to the advertising filter policy.</p> <p>If the p_peer_address parameter is not NULL, this parameter is ignored.</p>										

		macro	description
		BLE_ABS_ADV ERTISING_FILTER_ALLOW_ANY(0x00)	Process scan and connection requests from all devices.
		BLE_ABS_ADV ERTISING_FILTER_ALLOW_WHITE_LIST(0x01)	Process scan and connection requests from only devices in the White List.
uint8_t	own_bluetooth_address_type	Own Bluetooth address type. Select one of the following. 	
uint8_t	own_bluetooth_address[6]	Own Bluetooth address.	
uint8_t	padding[3]	padding	

◆ ble\_abs\_extend\_advertising\_parameter\_t

struct ble_abs_extend_advertising_parameter_t		
st_ble_abs_extend_advertising_parameter_t is the parameters for extended advertising.		
Data Fields		
ble_device_address_t *	p_peer_address	The remote device address. If the p_addr parameter is not NULL, Direct Connectable Advertising is performed to the remote address. If the p_addr parameter is NULL, Undirect Connectable Advertising is performed according to the advertising

		filter policy specified by the filter parameter.
uint8_t *	p_advertising_data	Advertising data. If p_adv_data is specified as NULL, advertising data is not set.
uint32_t	fast_advertising_interval	Advertising with the fast_advertising_interval parameter continues for the period specified by the fast_advertising_period parameter. Time(ms) = fast_advertising_interval * 0.625. If the fast_advertising_period parameter is 0, this parameter is ignored. Valid range is 0x00000020 - 0x00FFFFFF.
uint32_t	slow_advertising_interval	After the elapse of the fast_advertising_period, advertising with the slow_advertising_interval parameter continues for the period specified by the slow_advertising_period parameter. Time(ms) = fast_advertising_interval * 0.625. If the fast_advertising_period parameter is 0, this parameter is ignored. Valid range is 0x00000020 - 0x00FFFFFF.
uint16_t	fast_advertising_period	The period which advertising with the fast_advertising_interval parameter continues for. Time = duration * 10ms. After the elapse of the fast_advertising_period, <a href="#">BLE_GAP_EVENT_ADV_OFF</a> event notifies that the advertising has stopped. Valid range is 0x0000 - 0xFFFF. If the fast_advertising_period parameter is 0x0000, the fast_advertising_interval parameter is ignored.
uint16_t	slow_advertising_period	The period which advertising

		<p>with the <code>slow_advertising_interval</code> parameter continues for. <math>\text{Time} = \text{duration} * 10\text{ms}</math>. After the elapse of the <code>slow_advertising_period</code>, <code>BLE_GAP_EVENT_ADV_OFF</code> event notifies that the advertising has stopped. Valid range is 0x0000 - 0xFFFF. If the <code>slow_advertising_period</code> parameter is 0x0000, the advertising continues.</p>										
<code>uint16_t</code>	<code>advertising_data_length</code>	<p>Advertising data length (in bytes). Valid range is 0-229. If the <code>adv_data_length</code> is 0, Advertising Data is not included in the advertising PDU.</p>										
<code>uint8_t</code>	<code>advertising_channel_map</code>	<p>The channel map used for the advertising packet transmission. It is a bitwise OR of the following values.</p> <table border="1"> <thead> <tr> <th>macro</th> <th>description</th> </tr> </thead> <tbody> <tr> <td><code>BLE_GAP_ADV_CH3_7(0x01)</code></td> <td>Use 37 CH.</td> </tr> <tr> <td><code>BLE_GAP_ADV_CH3_8(0x02)</code></td> <td>Use 38 CH.</td> </tr> <tr> <td><code>BLE_GAP_ADV_CH3_9(0x04)</code></td> <td>Use 38 CH.</td> </tr> <tr> <td><code>BLE_GAP_ADV_CH_A_LL(0x07)</code></td> <td>Use 37 - 39 CH.</td> </tr> </tbody> </table>	macro	description	<code>BLE_GAP_ADV_CH3_7(0x01)</code>	Use 37 CH.	<code>BLE_GAP_ADV_CH3_8(0x02)</code>	Use 38 CH.	<code>BLE_GAP_ADV_CH3_9(0x04)</code>	Use 38 CH.	<code>BLE_GAP_ADV_CH_A_LL(0x07)</code>	Use 37 - 39 CH.
macro	description											
<code>BLE_GAP_ADV_CH3_7(0x01)</code>	Use 37 CH.											
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<code>BLE_GAP_ADV_CH_A_LL(0x07)</code>	Use 37 - 39 CH.											
<code>uint8_t</code>	<code>advertising_filter_policy</code>	Advertising filter policy.										

		<p>If the <code>p_peer_address</code> parameter is NULL, the advertising is performed according to the advertising filter policy.                  If the <code>p_peer_address</code> parameter is not NULL, this parameter is ignored.</p> <table border="1"> <thead> <tr> <th>macro</th> <th>description</th> </tr> </thead> <tbody> <tr> <td><code>BLE_ABS_ADV ERTISING_FILTER_ALLOW_ANY(0x00)</code></td> <td>Process scan and connection requests from all devices.</td> </tr> <tr> <td><code>BLE_ABS_ADV ERTISING_FILTER_ALLOW_WHITE_LIST(0x01)</code></td> <td>Process scan and connection requests from only devices in the White List.</td> </tr> </tbody> </table>	macro	description	<code>BLE_ABS_ADV ERTISING_FILTER_ALLOW_ANY(0x00)</code>	Process scan and connection requests from all devices.	<code>BLE_ABS_ADV ERTISING_FILTER_ALLOW_WHITE_LIST(0x01)</code>	Process scan and connection requests from only devices in the White List.
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uint8_t	own_bluetooth_address_type	<p>Own Bluetooth address type. Select one of the following.</p> <table border="1"> <thead> <tr> <th>macro</th> <th>description</th> </tr> </thead> <tbody> <tr> <td><code>BLE_GAP_ADD R_PUBLIC(0x00)</code></td> <td>Public Address</td> </tr> <tr> <td><code>BLE_GAP_ADD R_RPA_ID_PUBLIC(0x02)</code></td> <td>Resolvable Private Address. If the IRK of local device has not been registered in Resolving List, public address is used.</td> </tr> </tbody> </table>	macro	description	<code>BLE_GAP_ADD R_PUBLIC(0x00)</code>	Public Address	<code>BLE_GAP_ADD R_RPA_ID_PUBLIC(0x02)</code>	Resolvable Private Address. If the IRK of local device has not been registered in Resolving List, public address is used.
macro	description							
<code>BLE_GAP_ADD R_PUBLIC(0x00)</code>	Public Address							
<code>BLE_GAP_ADD R_RPA_ID_PUBLIC(0x02)</code>	Resolvable Private Address. If the IRK of local device has not been registered in Resolving List, public address is used.							
uint8_t	own_bluetooth_address[6]	Own Bluetooth address.						
uint8_t	primary_advertising_phy	<p>Primary advertising PHY. In this parameter, only 1M PHY and Coded PHY can be specified, and 2M PHY cannot be specified.</p> <table border="1"> <thead> <tr> <th>macro</th> <th>description</th> </tr> </thead> <tbody> <tr> <td><code>BLE_GAP_ADV _PHY_1M(0x01)</code></td> <td>Use 1M PHY as Primary Advertising PHY.</td> </tr> </tbody> </table>	macro	description	<code>BLE_GAP_ADV _PHY_1M(0x01)</code>	Use 1M PHY as Primary Advertising PHY.		
macro	description							
<code>BLE_GAP_ADV _PHY_1M(0x01)</code>	Use 1M PHY as Primary Advertising PHY.							

		<p>When the <code>adv_prop_type</code> field is Legacy Advertising PDU type, this field shall be set to <code>BLE_GAP_ADV_PHY_1M</code>.</p> <p><code>BLE_GAP_ADV_PHY_CD(0x03)</code> Use Coded PHY as Primary Advertising PHY. Coding scheme is configured by <code>R_BLE_VS_SetCodingScheme()</code>.</p>		
<code>uint8_t</code>	<code>secondary_advertising_phy</code>	<p>Secondary advertising Phy. Select one of the following.</p> <table border="1" style="float: right; margin-left: 20px;"> <tr> <td style="width: 20px; height: 20px;"></td> <td style="width: 20px; height: 20px;"></td> </tr> </table>		
<code>uint8_t</code>	<code>padding[3]</code>	<code>padding</code>		

◆ **ble\_abs\_non\_connectable\_advertising\_parameter\_t**

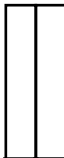
<code>struct ble_abs_non_connectable_advertising_parameter_t</code>
<code>st_ble_abs_non_connectable_advertising_parameter_t</code> is the parameters for non-connectable advertising.
Data Fields

<code>ble_device_address_t *</code>	<code>p_peer_address</code>	<p>The remote device address. If the <code>p_peer_address</code> parameter is not NULL, Direct Connectable Advertising is performed to the remote address.</p> <p>If the <code>p_peer_address</code> parameter is NULL, Undirect Connectable Advertising is performed according to the advertising filter policy specified by the filter parameter.</p>
<code>uint8_t *</code>	<code>p_advertising_data</code>	Advertising data. If <code>p_adv_data</code> is specified as NULL, advertising data is not set.
<code>uint32_t</code>	<code>advertising_interval</code>	<p>Advertising with the <code>advertising_interval</code> parameter continues for the period specified by the duration parameter.</p> <p><math>\text{Time(ms)} = \text{advertising\_interval} * 0.625.</math></p> <p>If the duration parameter is 0x0000, the advertising with the <code>advertising_interval</code> parameter continue.</p> <p>Valid range is 0x00000020 - 0x00FFFFFF.</p>
<code>uint16_t</code>	<code>advertising_duration</code>	<p>The period which advertising with the <code>advertising_interval</code> parameter continues for.</p> <p><math>\text{Time} = \text{advertising\_duration} * 10\text{ms}.</math></p> <p>After the elapse of the <code>advertising_duration</code>, <a href="#">BLE_GAP_EVENT_ADV_OFF</a> event notifies that the advertising has stopped.</p> <p>Valid range is 0x0000 - 0xFFFF.</p> <p>If the <code>advertising_duration</code> parameter is 0x0000, the advertising continues.</p>
<code>uint16_t</code>	<code>advertising_data_length</code>	<p>Advertising data length (in bytes).</p> <p>If the <code>primary_advertising_phy</code> parameter is <a href="#">BLE_ABS_ADVERTISING_PHY_LEGACY(0x00)</a>, the valid range is 0-31.</p> <p>If the <code>primary_advertising_phy</code> parameter is the other values,</p>



		<p>the valid range is 0-1650. If the advertising_data_length parameter is 0, Advertising Data is not included in the advertising PDU.</p>										
<p>uint8_t</p>	<p>advertising_channel_map</p>	<p>The channel map used for the advertising packet transmission. It is a bitwise OR of the following values.</p> <table border="1" data-bbox="1267 524 1473 1480"> <thead> <tr> <th>macro</th> <th>description</th> </tr> </thead> <tbody> <tr> <td>BLE_GAP_ADV_CH37(0x01)</td> <td>Use 37 CH.</td> </tr> <tr> <td>BLE_GAP_ADV_CH38(0x02)</td> <td>Use 38 CH.</td> </tr> <tr> <td>BLE_GAP_ADV_CH39(0x04)</td> <td>Use 38 - 39 CH.</td> </tr> <tr> <td>BLE_GAP_ADV_CHALL(0x07)</td> <td>Use 37 - 39 CH.</td> </tr> </tbody> </table>	macro	description	BLE_GAP_ADV_CH37(0x01)	Use 37 CH.	BLE_GAP_ADV_CH38(0x02)	Use 38 CH.	BLE_GAP_ADV_CH39(0x04)	Use 38 - 39 CH.	BLE_GAP_ADV_CHALL(0x07)	Use 37 - 39 CH.
macro	description											
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<p>uint8_t</p>	<p>own_bluetooth_address_type</p>	<p>Own Bluetooth address type. Select one of the following.</p> <table border="1" data-bbox="1034 1581 1473 2033"> <thead> <tr> <th>macro</th> <th>description</th> </tr> </thead> <tbody> <tr> <td>BLE_GAP_ADD_R_PUBLIC(0x00)</td> <td>Public Address</td> </tr> <tr> <td>BLE_GAP_ADD_R_RPA_ID_PUBLIC(0x02)</td> <td>Resolvable Private Address. If the IRK of local device has not been registered in Resolving List,</td> </tr> </tbody> </table>	macro	description	BLE_GAP_ADD_R_PUBLIC(0x00)	Public Address	BLE_GAP_ADD_R_RPA_ID_PUBLIC(0x02)	Resolvable Private Address. If the IRK of local device has not been registered in Resolving List,				
macro	description											
BLE_GAP_ADD_R_PUBLIC(0x00)	Public Address											
BLE_GAP_ADD_R_RPA_ID_PUBLIC(0x02)	Resolvable Private Address. If the IRK of local device has not been registered in Resolving List,											

		public address is used.								
uint8_t	own_bluetooth_address[6]	Own Bluetooth address.								
uint8_t	primary_advertising_phy	<p>Primary advertising PHY. In this parameter, only 1M PHY and Coded PHY can be specified, and 2M PHY cannot be specified.</p> <table border="1"> <thead> <tr> <th>macro</th> <th>description</th> </tr> </thead> <tbody> <tr> <td><a href="#">BLE_ABS_ADV_ADVERTISING_PHY_LEGACY(0x00)</a></td> <td>Use 1M PHY as Primary Advertising PHY for Non-Connectable Legacy Advertising. If Periodic Advertising is performed, this value shall not set to the adv_phy parameter.</td> </tr> <tr> <td><a href="#">BLE_GAP_ADV_PHY_1M(0x01)</a></td> <td>Use 1M PHY as Primary Advertising PHY. When the adv_prop_type field is Legacy Advertising PDU type, this field shall be set to BLE_GAP_ADV_PHY_1M.</td> </tr> <tr> <td><a href="#">BLE_GAP_ADV_PHY_CD(0x03)</a></td> <td>Use Coded PHY as Primary Advertising PHY. Coding scheme is configured by <a href="#">R_BLE_VS_SetCodingScheme()</a>.</td> </tr> </tbody> </table>	macro	description	<a href="#">BLE_ABS_ADV_ADVERTISING_PHY_LEGACY(0x00)</a>	Use 1M PHY as Primary Advertising PHY for Non-Connectable Legacy Advertising. If Periodic Advertising is performed, this value shall not set to the adv_phy parameter.	<a href="#">BLE_GAP_ADV_PHY_1M(0x01)</a>	Use 1M PHY as Primary Advertising PHY. When the adv_prop_type field is Legacy Advertising PDU type, this field shall be set to BLE_GAP_ADV_PHY_1M.	<a href="#">BLE_GAP_ADV_PHY_CD(0x03)</a>	Use Coded PHY as Primary Advertising PHY. Coding scheme is configured by <a href="#">R_BLE_VS_SetCodingScheme()</a> .
macro	description									
<a href="#">BLE_ABS_ADV_ADVERTISING_PHY_LEGACY(0x00)</a>	Use 1M PHY as Primary Advertising PHY for Non-Connectable Legacy Advertising. If Periodic Advertising is performed, this value shall not set to the adv_phy parameter.									
<a href="#">BLE_GAP_ADV_PHY_1M(0x01)</a>	Use 1M PHY as Primary Advertising PHY. When the adv_prop_type field is Legacy Advertising PDU type, this field shall be set to BLE_GAP_ADV_PHY_1M.									
<a href="#">BLE_GAP_ADV_PHY_CD(0x03)</a>	Use Coded PHY as Primary Advertising PHY. Coding scheme is configured by <a href="#">R_BLE_VS_SetCodingScheme()</a> .									
uint8_t	secondary_advertising_phy	Secondary advertising Phy.								

		Select one of the following. 
uint8_t	padding[2]	padding

#### ◆ ble\_abs\_periodic\_advertising\_parameter\_t

struct ble_abs_periodic_advertising_parameter_t		
st_ble_abs_periodic_advertising_parameter_t is the parameters for periodic advertising.		
Data Fields		
<a href="#">ble_abs_non_connectable_advertising_parameter_t</a>	advertising_parameter	Advertising parameters.
uint8_t *	p_periodic_advertising_data	Periodic advertising data. If p_perd_adv_data is specified as NULL, periodic advertising data is not set.
uint16_t	periodic_advertising_interval	Periodic advertising interval. Time(ms) = periodic_advertising_interval * 1.25. Valid range is 0x0006 - 0xFFFF.
uint16_t	periodic_advertising_data_length	Periodic advertising data length (in bytes). Valid range is 0 - 1650. If the periodic_advertising_data_length is 0, Periodic Advertising Data is not included in the advertising PDU.

#### ◆ ble\_abs\_scan\_phy\_parameter\_t

struct ble_abs_scan_phy_parameter_t
-------------------------------------

Data Fields								
st_ble_abs_scan_phy_parameter_t is the phy parameters for scan.								
Data Fields								
uint16_t	fast_scan_interval	Fast scan interval. Interval(ms) = fast_scan_interval * 0.625. Valid range is 0x0004 - 0xFFFF.						
uint16_t	slow_scan_interval	Slow Scan interval. Slow Scan interval(ms) = slow_scan_interval * 0.625. Valid range is 0x0004 - 0xFFFF.						
uint16_t	fast_scan_window	Fast Scan window. Fast Scan window(ms) = fast_scan_window * 0.625. Valid range is 0x0004 - 0xFFFF.						
uint16_t	slow_scan_window	Slow Scan window. Slow Scan window(ms) = slow_scan_window * 0.625. Valid range is 0x0004 - 0xFFFF.						
uint8_t	scan_type	Scan type. <table border="1" data-bbox="1182 936 1471 1025"> <thead> <tr> <th>macro</th> <th>description</th> </tr> </thead> <tbody> <tr> <td>BLE_GAP_SCAN_PASSIVE(0x00)</td> <td>Passive Scan.</td> </tr> <tr> <td>BLE_GAP_SCAN_ACTIVE(0x01)</td> <td>Active Scan.</td> </tr> </tbody> </table>	macro	description	BLE_GAP_SCAN_PASSIVE(0x00)	Passive Scan.	BLE_GAP_SCAN_ACTIVE(0x01)	Active Scan.
macro	description							
BLE_GAP_SCAN_PASSIVE(0x00)	Passive Scan.							
BLE_GAP_SCAN_ACTIVE(0x01)	Active Scan.							
uint8_t	padding[3]	padding.						

#### ◆ ble\_abs\_scan\_parameter\_t

Data Fields		
struct ble_abs_scan_parameter_t		
st_ble_abs_scan_parameter_t is the parameters for scan.		
Data Fields		
ble_abs_scan_phy_parameter_t *	p_phy_parameter_1M	Scan parameters for receiving the advertising packets in 1M PHY. In case of not receiving the advertising packets in 1M PHY, this field is specified as NULL. p_phy_parameter_1M or p_phy_parameter_coded field shall be set to scan parameters.
ble_abs_scan_phy_parameter_t *	p_phy_parameter_coded	Scan parameters for receiving the advertising packets in

		<p>Coded PHY.</p> <p>In case of not receiving the advertising packets in Coded PHY, this field is specified as NULL.</p> <p>p_phy_parameter_1M or p_phy_parameter_coded field shall be set to scan parameters.</p>
uint8_t *	p_filter_data	<p>Data for Advertising Data filtering.</p> <p>The p_filter_data parameter is used for the advertising data in single advertising report.</p> <p>The advertising data composed of multiple advertising reports is not filtered by this parameter.</p> <p>If the p_filter_data parameter is specified as NULL, the filtering is not done.</p>
uint16_t	fast_scan_period	<p>The period which scan with the fast scan interval/fast scan window continues for.</p> <p>Time(ms) = fast_scan_period * 10.</p> <p>Valid range is 0x0000 - 0xFFFF.</p> <p>If the fast_scan_period parameter is 0x0000, scan with the fast scan interval/fast scan window is not performed.</p> <p>After the elapse of the fast_scan_period, <a href="#">BLE_GAP_EVENT_SCAN_TO</a> event notifies that the scan has stopped.</p>
uint16_t	slow_scan_period	<p>The period which scan with the slow scan interval/slow scan window continues for.</p> <p>Time = slow_scan_period * 10ms.</p> <p>Valid range is 0x0000 - 0xFFFF.</p> <p>If the slow_scan_period parameter is 0x0000, the scan continues.</p> <p>After the elapse of the slow_scan_period, <a href="#">BLE_GAP_EVENT_SCAN_TO</a> event notifies that the scan has stopped.</p>
uint16_t	filter_data_length	<p>The length of the data specified by the p_filter_data parameter.</p> <p>Valid range is 0x0000-0x0010.</p>

		<p>If the filter_data_length parameter is 0, the filtering is not done.</p>						
<p>uint8_t</p>	<p>device_scan_filter_policy</p>	<p>Scan Filter Policy. Select one of the following.</p> <table border="1" data-bbox="1225 353 1473 443"> <thead> <tr> <th data-bbox="1225 353 1347 443">macro</th> <th data-bbox="1347 353 1473 443">description</th> </tr> </thead> <tbody> <tr> <td data-bbox="1225 454 1347 651"> <p>BLE_G AP_SC AN_ALL OW_AD V_ALL( 0x00)</p> </td> <td data-bbox="1347 454 1473 1014"> <p>Accept all advertising and scan response PDUs except directed advertising PDUs not addressed to local device.</p> </td> </tr> <tr> <td data-bbox="1225 1043 1347 1267"> <p>BLE_G AP_SC AN_ALL OW_AD V_WLS T(0x01 )</p> </td> <td data-bbox="1347 1043 1473 2045"> <p>Accept only advertising and scan response PDUs from remote devices whose address is registered in the White List. Directed advertising PDUs which are not addressed to local device is ignore</p> </td> </tr> </tbody> </table>	macro	description	<p>BLE_G AP_SC AN_ALL OW_AD V_ALL( 0x00)</p>	<p>Accept all advertising and scan response PDUs except directed advertising PDUs not addressed to local device.</p>	<p>BLE_G AP_SC AN_ALL OW_AD V_WLS T(0x01 )</p>	<p>Accept only advertising and scan response PDUs from remote devices whose address is registered in the White List. Directed advertising PDUs which are not addressed to local device is ignore</p>
macro	description							
<p>BLE_G AP_SC AN_ALL OW_AD V_ALL( 0x00)</p>	<p>Accept all advertising and scan response PDUs except directed advertising PDUs not addressed to local device.</p>							
<p>BLE_G AP_SC AN_ALL OW_AD V_WLS T(0x01 )</p>	<p>Accept only advertising and scan response PDUs from remote devices whose address is registered in the White List. Directed advertising PDUs which are not addressed to local device is ignore</p>							

		<p>d.</p> <p>BLE_G Accept  AP_SC all adv  AN_ALL ertisin  OW_AD g and  V_EXC scan re  EPT_DI sponse  RECTE PDUs  D(0x02 except  ) directe  d adve  rtising  PDUs  whose  the  target  addres  s is  identit  y  addres  s but  doesn't  addres  s local  device.  Howev  er  directe  d adve  rtising  PDUs  whose  the  target  addres  s is the  local re  solvabl  e  private  addres  s are a  ccepte  d.</p> <p>BLE_G Accept  AP_SC all adv  AN_ALL ertisin  OW_AD g and  V_EXC scan re  EPT_DI sponse  RECTE PDUs.  D_WLS The foll  T(0x03 owing</p>
--	--	------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------

		<p>) are excluded.</p> <ul style="list-style-type: none"> <li>Advertising and scan response PDUs where the advertiser's identity address is not in the White List.</li> <li>Directed advertising PDUs whose the target address is identity address but doesn't address local device. However directed advertising PDUs whose the target address is the local resolvable private address are accepted.  </li> </ul>								
uint8_t	filter_duplicate	<p>Filter duplicates. Maximum number of filtered devices is 8. The 9th and subsequent devices are not filtered by this parameter.</p> <table border="1"> <thead> <tr> <th>macro</th> <th>description</th> </tr> </thead> <tbody> <tr> <td>BLE_GAP_SCAN_FILTER_DUPLICATION_DISABLE(0x00)</td> <td>Duplicate filter disabled.</td> </tr> <tr> <td>BLE_GAP_SCAN_FILTER_DUPLICATION_ENABLE(0x01)</td> <td>Duplicate filter enabled.</td> </tr> <tr> <td>BLE_GAP_SCAN_FILTER_DUPLICATION_ENABLE_RESET(0x02)</td> <td>Duplicate filtering enabled, reset for each scan period.</td> </tr> </tbody> </table>	macro	description	BLE_GAP_SCAN_FILTER_DUPLICATION_DISABLE(0x00)	Duplicate filter disabled.	BLE_GAP_SCAN_FILTER_DUPLICATION_ENABLE(0x01)	Duplicate filter enabled.	BLE_GAP_SCAN_FILTER_DUPLICATION_ENABLE_RESET(0x02)	Duplicate filtering enabled, reset for each scan period.
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BLE_GAP_SCAN_FILTER_DUPLICATION_DISABLE(0x00)	Duplicate filter disabled.									
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BLE_GAP_SCAN_FILTER_DUPLICATION_ENABLE_RESET(0x02)	Duplicate filtering enabled, reset for each scan period.									
uint8_t	filter_ad_type	<p>The AD type of the data specified by the p_filter_data parameter. The AD type identifier values are defined in Bluetooth SIG Assigned Number (<a href="https://www.bluetooth.com/specifications/assigned-numbers">https://www.bluetooth.com/specifications/assigned-numbers</a>).</p>								
uint8_t	padding[3]	Padding.								



◆ **ble\_abs\_connection\_phy\_parameter\_t**

struct ble_abs_connection_phy_parameter_t		
st_ble_abs_connection_phy_parameter_t is the phy parameters for create connection.		
Data Fields		
uint16_t	connection_interval	Connection interval. Time(ms) = connection_interval * 1.25. Valid range is 0x0006 - 0x0C80.
uint16_t	connection_slave_latency	Slave latency. Valid range is 0x0000 - 0x01F3.
uint16_t	supervision_timeout	Supervision timeout. Time(ms) = supervision_timeout * 10. Valid range is 0x000A - 0x0C80.
uint8_t	padding[2]	Padding.

◆ **ble\_abs\_connection\_parameter\_t**

struct ble_abs_connection_parameter_t		
st_ble_abs_connection_parameter_t is the parameters for create connection.		
Data Fields		
ble_abs_connection_phy_parameter_t*	p_connection_phy_parameter_1M	Connection interval, slave latency, supervision timeout for 1M PHY. The p_connection_phy_parameter_1M is specified as NULL, a connection request is not sent with 1M PHY.
ble_abs_connection_phy_parameter_t*	p_connection_phy_parameter_2M	Connection interval, slave latency, supervision timeout for 2M PHY. The p_connection_phy_parameter_2M is specified as NULL, a connection request is not sent with 2M PHY.
ble_abs_connection_phy_parameter_t*	p_connection_phy_parameter_coded	Connection interval, slave latency, supervision timeout for Coded PHY. The p_connection_phy_parameter_coded is specified as NULL, a connection request is not sent with Coded PHY.
ble_device_address_t*	p_device_address	Address of the device to be connected. If the filter field is BLE_GAP_INIT_FILTER_USE_WLST(0x01), this parameter is

		ignored.						
uint8_t	filter_parameter	<p>The filter field specifies whether the White List is used or not, when connecting with a remote device.</p> <table border="1"> <thead> <tr> <th>macro</th> <th>description</th> </tr> </thead> <tbody> <tr> <td><a href="#">BLE_GAP_INIT_FILTER_USE_ADDR(0x00)</a></td> <td>White List is not used. The remote device to be connected is specified by the p_addr field is used.</td> </tr> <tr> <td><a href="#">BLE_GAP_INIT_FILTER_USE_WHITE_LIST(0x01)</a></td> <td>White List is used. The remote device registered in White List is connected with local device. The p_addr field is ignored.</td> </tr> </tbody> </table>	macro	description	<a href="#">BLE_GAP_INIT_FILTER_USE_ADDR(0x00)</a>	White List is not used. The remote device to be connected is specified by the p_addr field is used.	<a href="#">BLE_GAP_INIT_FILTER_USE_WHITE_LIST(0x01)</a>	White List is used. The remote device registered in White List is connected with local device. The p_addr field is ignored.
macro	description							
<a href="#">BLE_GAP_INIT_FILTER_USE_ADDR(0x00)</a>	White List is not used. The remote device to be connected is specified by the p_addr field is used.							
<a href="#">BLE_GAP_INIT_FILTER_USE_WHITE_LIST(0x01)</a>	White List is used. The remote device registered in White List is connected with local device. The p_addr field is ignored.							
uint8_t	connection_timeout	<p>The time(sec) to cancel the create connection request. Valid range is <math>0 \leq \text{connection\_timeout} \leq 10</math>. If the connection_timeout field is 0, the create connection request is not canceled.</p> <p>.</p>						
uint8_t	padding[2]	Padding.						

## ◆ ble\_abs\_cfg\_t

struct ble_abs_cfg_t	
BLE ABS configuration parameters.	
<b>Data Fields</b>	
uint32_t	<a href="#">channel</a>
	Select a channel corresponding to the channel number of the hardware. <a href="#">More...</a>
<a href="#">ble_gap_application_callback_t</a>	<a href="#">gap_callback</a>

	GAP callback function.
<code>ble_vendor_specific_application_callback_t</code>	<code>vendor_specific_callback</code>
	Vendor Specific callback function.
<code>ble_abs_gatt_server_callback_set_t *</code>	<code>p_gatt_server_callback_list</code>
	GATT Server callback set.
<code>uint8_t</code>	<code>gatt_server_callback_list_number</code>
	The number of GATT Server callback functions.
<code>ble_abs_gatt_client_callback_set_t *</code>	<code>p_gatt_client_callback_list</code>
	GATT Client callback set.
<code>uint8_t</code>	<code>gatt_client_callback_list_number</code>
	The number of GATT Client callback functions.
<code>ble_abs_pairing_parameter_t *</code>	<code>p_pairing_parameter</code>
	Pairing parameters.
<code>flash_instance_t const *</code>	<code>p_flash_instance</code>
	Pointer to flash instance.
<code>timer_instance_t const *</code>	<code>p_timer_instance</code>
	Pointer to timer instance.

void(*	<a href="#">p_callback</a> )(ble_abs_callback_args_t *p_args)
	Callback provided when a BLE ISR occurs.
void const *	<a href="#">p_context</a>
	Placeholder for user data. Passed to the user callback in <a href="#">ble_abs_callback_args_t</a> .
void const *	<a href="#">p_extend</a>
	Placeholder for user extension.

## Field Documentation

### ◆ channel

uint32\_t ble\_abs\_cfg\_t::channel

Select a channel corresponding to the channel number of the hardware.  
the parameters for initialization.

### ◆ ble\_abs\_api\_t

struct ble\_abs\_api\_t

BLE ABS functions implemented at the HAL layer will follow this API.

#### Data Fields

fsp_err_t(*	<a href="#">open</a> )(ble_abs_ctrl_t *const p_ctrl, <a href="#">ble_abs_cfg_t</a> const *const p_cfg)
fsp_err_t(*	<a href="#">close</a> )(ble_abs_ctrl_t *const p_ctrl)
fsp_err_t(*	<a href="#">reset</a> )(ble_abs_ctrl_t *const p_ctrl, <a href="#">ble_event_cb_t</a> init_callback)
fsp_err_t(*	<a href="#">versionGet</a> )(fsp_version_t *const p_data)
fsp_err_t(*	<a href="#">startLegacyAdvertising</a> )(ble_abs_ctrl_t *const p_ctrl, <a href="#">ble_abs_legacy_advertising_parameter_t</a> const *const p_advertising_parameter)
fsp_err_t(*	<a href="#">startExtendedAdvertising</a> )(ble_abs_ctrl_t *const p_ctrl,

	<code>ble_abs_extend_advertising_parameter_t</code> const *const <code>p_advertising_parameter</code> )
<code>fsp_err_t</code> (*	<code>startNonConnectableAdvertising</code> )(ble_abs_ctrl_t *const p_ctrl, ble_abs_non_connectable_advertising_parameter_t const *const p_advertising_parameter)
<code>fsp_err_t</code> (*	<code>startPeriodicAdvertising</code> )(ble_abs_ctrl_t *const p_ctrl, ble_abs_periodic_advertising_parameter_t const *const p_advertising_parameter)
<code>fsp_err_t</code> (*	<code>startScanning</code> )(ble_abs_ctrl_t *const p_ctrl, ble_abs_scan_parameter_t const *const p_scan_parameter)
<code>fsp_err_t</code> (*	<code>createConnection</code> )(ble_abs_ctrl_t *const p_ctrl, ble_abs_connection_parameter_t const *const p_connection_parameter)
<code>fsp_err_t</code> (*	<code>setLocalPrivacy</code> )(ble_abs_ctrl_t *const p_ctrl, uint8_t const *const p_lc_irk, uint8_t privacy_mode)
<code>fsp_err_t</code> (*	<code>startAuthentication</code> )(ble_abs_ctrl_t *const p_ctrl, uint16_t connection_handle)

## Field Documentation

### ◆ open

`fsp_err_t`(\* ble\_abs\_api\_t::open) (ble\_abs\_ctrl\_t \*const p\_ctrl, ble\_abs\_cfg\_t const \*const p\_cfg)

Initialize the BLE ABS in register start mode.

### Implemented as

- RM\_BLE\_ABS\_Open()

### Parameters

[in]	p_ctrl	Pointer to control structure.
[in]	p_cfg	Pointer to pin configuration structure.

◆ **close**

```
fsp_err_t(* ble_abs_api_t::close) (ble_abs_ctrl_t *const p_ctrl)
```

Close the BLE ABS.

**Implemented as**

- [RM\\_BLE\\_ABS\\_Close\(\)](#)

**Parameters**

[in]	p_ctrl	Pointer to control structure.
------	--------	-------------------------------

◆ **reset**

```
fsp_err_t(* ble_abs_api_t::reset) (ble_abs_ctrl_t *const p_ctrl, ble_event_cb_t init_callback)
```

Close the BLE ABS.

**Implemented as**

- [RM\\_BLE\\_ABS\\_Reset\(\)](#)

**Parameters**

[in]	p_ctrl	Pointer to control structure.
[in]	init_callback	callback function to initialize Host Stack.

◆ **versionGet**

```
fsp_err_t(* ble_abs_api_t::versionGet) (fsp_version_t *const p_data)
```

Return the version of the driver.

**Implemented as**

- [RM\\_BLE\\_ABS\\_VersionGet\(\)](#)

**Parameters**

[out]	p_data	Memory address to return version information to.
-------	--------	--------------------------------------------------

### ◆ startLegacyAdvertising

```
fsp_err_t(* ble_abs_api_t::startLegacyAdvertising) (ble_abs_ctrl_t *const p_ctrl,
ble_abs_legacy_advertising_parameter_t const *const p_advertising_parameter)
```

Start Legacy Connectable Advertising.

#### Implemented as

- RM\_BLE\_ABS\_StartLegacyAdvertising()

#### Parameters

[in]	p_ctrl	Pointer to control structure.
[in]	p_advertising_parameter	Pointer to Advertising parameters for Legacy Advertising.

### ◆ startExtendedAdvertising

```
fsp_err_t(* ble_abs_api_t::startExtendedAdvertising) (ble_abs_ctrl_t *const p_ctrl,
ble_abs_extend_advertising_parameter_t const *const p_advertising_parameter)
```

Start Extended Connectable Advertising.

#### Implemented as

- RM\_BLE\_ABS\_StartExtendedAdvertising()

#### Parameters

[in]	p_ctrl	Pointer to control structure.
[in]	p_advertising_parameter	Pointer to Advertising parameters for extend Advertising.

### ◆ startNonConnectableAdvertising

```
fsp_err_t(* ble_abs_api_t::startNonConnectableAdvertising) (ble_abs_ctrl_t *const p_ctrl,
ble_abs_non_connectable_advertising_parameter_t const *const p_advertising_parameter)
```

Start Non-Connectable Advertising.

#### Implemented as

- RM\_BLE\_ABS\_StartNonConnectableAdvertising()

#### Parameters

[in]	p_ctrl	Pointer to control structure.
[in]	p_advertising_parameter	Pointer to Advertising parameters for non-connectable Advertising.

### ◆ startPeriodicAdvertising

```
fsp_err_t(* ble_abs_api_t::startPeriodicAdvertising) (ble_abs_ctrl_t *const p_ctrl,
ble_abs_periodic_advertising_parameter_t const *const p_advertising_parameter)
```

Start Periodic Advertising.

#### Implemented as

- RM\_BLE\_ABS\_StartPeriodicAdvertising()

#### Parameters

[in]	p_ctrl	Pointer to control structure.
[in]	p_advertising_parameter	Pointer to Advertising parameters for periodic Advertising.

### ◆ startScanning

```
fsp_err_t(* ble_abs_api_t::startScanning) (ble_abs_ctrl_t *const p_ctrl, ble_abs_scan_parameter_t
const *const p_scan_parameter)
```

Start scanning.

#### Implemented as

- RM\_BLE\_ABS\_StartScanning()

#### Parameters

[in]	p_ctrl	Pointer to control structure.
[in]	p_scan_parameter	Pointer to scan parameter.

### ◆ createConnection

```
fsp_err_t(* ble_abs_api_t::createConnection) (ble_abs_ctrl_t *const p_ctrl,
ble_abs_connection_parameter_t const *const p_connection_parameter)
```

Request create connection.

#### Implemented as

- RM\_BLE\_ABS\_CreateConnection()

#### Parameters

[in]	p_ctrl	Pointer to control structure.
[in]	p_connection_parameter	Pointer to connection parameter.



◆ **setLocalPrivacy**

```
fsp_err_t(* ble_abs_api_t::setLocalPrivacy) (ble_abs_ctrl_t *const p_ctrl, uint8_t const *const p_lc_irk, uint8_t privacy_mode)
```

Configure local device privacy.

**Implemented as**

- [RM\\_BLE\\_ABS\\_SetLocalPrivacy\(\)](#)

**Parameters**

[in]	p_ctrl	Pointer to control structure.
[in]	p_lc_irk	Pointer to IRK to be registered in the resolving list.
[in]	privacy_mode	privacy_mode privacy mode.

◆ **startAuthentication**

```
fsp_err_t(* ble_abs_api_t::startAuthentication) (ble_abs_ctrl_t *const p_ctrl, uint16_t connection_handle)
```

Start pairing or encryption.

**Implemented as**

- [RM\\_BLE\\_ABS\\_StartAuthentication\(\)](#)

**Parameters**

[in]	p_ctrl	Pointer to control structure.
[in]	connection_handle	Connection handle identifying the remote device.

◆ **ble\_abs\_instance\_t**

```
struct ble_abs_instance_t
```

This structure encompasses everything that is needed to use an instance of this interface.

## Data Fields

<a href="#">ble_abs_ctrl_t</a> *	p_ctrl	Pointer to the control structure for this instance.
<a href="#">ble_abs_cfg_t</a> const *	p_cfg	Pointer to the configuration structure for this instance.
<a href="#">ble_abs_api_t</a> const *	p_api	Pointer to the API structure for this instance.

**Typedef Documentation**

### ◆ ble\_gap\_application\_callback\_t

```
typedef void(* ble_gap_application_callback_t) (uint16_t event_type, ble_status_t event_result,  
st_ble_evt_data_t *p_event_data)
```

ble\_gap\_application\_callback\_t is the GAP Event callback function type.

### ◆ ble\_vendor\_specific\_application\_callback\_t

```
typedef void(* ble_vendor_specific_application_callback_t) (uint16_t event_type, ble_status_t  
event_result, st_ble_vs_evt_data_t *p_event_data)
```

ble\_vendor\_specific\_application\_callback\_t is the Vendor Specific Event callback function type.

### ◆ ble\_gatt\_server\_application\_callback\_t

```
typedef void(* ble_gatt_server_application_callback_t) (uint16_t event_type, ble_status_t  
event_result, st_ble_gatts_evt_data_t *p_event_data)
```

ble\_gatt\_server\_application\_callback\_t is the GATT Server Event callback function type.

### ◆ ble\_gatt\_client\_application\_callback\_t

```
typedef void(* ble_gatt_client_application_callback_t) (uint16_t event_type, ble_status_t  
event_result, st_ble_gattc_evt_data_t *p_event_data)
```

ble\_gatt\_client\_application\_callback\_t is the GATT Server Event callback function type.

### ◆ ble\_abs\_ctrl\_t

```
typedef void ble_abs_ctrl_t
```

BLE ABS control block. Allocate an instance specific control block to pass into the BLE ABS API calls.

#### Implemented as

- ble\_abs\_instance\_ctrl\_t

## Enumeration Type Documentation

---

◆ **ble\_abs\_advertising\_filter\_t**

enum <code>ble_abs_advertising_filter_t</code>	
Advertising Filter Policy	
Enumerator	
<code>BLE_ABS_ADVERTISING_FILTER_ALLOW_ANY</code>	Receive a connect request from all devices.
<code>BLE_ABS_ADVERTISING_FILTER_ALLOW_WHITE_LIST</code>	Receive a connect request from only the devices registered in White List.

**4.3.46 Block Media Interface**[Interfaces](#)**Detailed Description**

Interface for block media memory access.

**Summary**

The block media interface supports reading, writing, and erasing media devices. All functions are non-blocking if possible. The callback is used to determine when an operation completes.

Implemented by:

- [SD/MMC Block Media Implementation \(`rm\_block\_media\_sdmmc`\)](#)
- [USB HMSC Block Media Implementation \(`rm\_block\_media\_usb`\)](#)

**Data Structures**

```
struct rm\_block\_media\_info\_t
```

```
struct rm\_block\_media\_callback\_args\_t
```

```
struct rm\_block\_media\_cfg\_t
```

```
struct rm\_block\_media\_status\_t
```

```
struct rm\_block\_media\_api\_t
```

```
struct rm\_block\_media\_instance\_t
```

**Typedefs**

```
typedef void rm\_block\_media\_ctrl\_t
```

## Enumerations

enum [rm\\_block\\_media\\_event\\_t](#)

## Data Structure Documentation

### ◆ [rm\\_block\\_media\\_info\\_t](#)

struct <a href="#">rm_block_media_info_t</a>		
Block media device information supported by the instance		
Data Fields		
uint32_t	<a href="#">sector_size_bytes</a>	Sector size in bytes.
uint32_t	<a href="#">num_sectors</a>	Total number of sectors.
bool	<a href="#">reentrant</a>	True if connected block media driver is reentrant.
bool	<a href="#">write_protected</a>	True if connected block media device is write protected.

### ◆ [rm\\_block\\_media\\_callback\\_args\\_t](#)

struct <a href="#">rm_block_media_callback_args_t</a>		
Callback function parameter data		
Data Fields		
<a href="#">rm_block_media_event_t</a>	<a href="#">event</a>	The event can be used to identify what caused the callback.
void const *	<a href="#">p_context</a>	Placeholder for user data.

### ◆ [rm\\_block\\_media\\_cfg\\_t](#)

struct <a href="#">rm_block_media_cfg_t</a>		
User configuration structure, used in open function		
<b>Data Fields</b>		
uint32_t	<a href="#">block_size</a>	
		Block size, must be a power of 2 multiple of <a href="#">sector_size_bytes</a> .
void(*	<a href="#">p_callback</a> )( <a href="#">rm_block_media_callback_args_t</a> *p_args)	
		Pointer to callback function.
void const *	<a href="#">p_context</a>	

	User defined context passed into callback function.
void const *	<a href="#">p_extend</a>
	Extension parameter for hardware specific settings.

◆ **rm\_block\_media\_status\_t**

struct <a href="#">rm_block_media_status_t</a>		
Current status		
Data Fields		
bool	<a href="#">initialized</a>	False if <a href="#">rm_block_media_api_t::medialnit</a> has not been called since media was inserted, true otherwise.
bool	<a href="#">busy</a>	True if media is busy with a previous write/erase operation.
bool	<a href="#">media_inserted</a>	Media insertion status, true if media is not removable.

◆ **rm\_block\_media\_api\_t**

struct <a href="#">rm_block_media_api_t</a>	
Block media interface API.	
<b>Data Fields</b>	
<a href="#">fsp_err_t</a> (*	<a href="#">open</a> )( <a href="#">rm_block_media_ctrl_t</a> *const p_ctrl, <a href="#">rm_block_media_cfg_t</a> const *const p_cfg)
<a href="#">fsp_err_t</a> (*	<a href="#">medialnit</a> )( <a href="#">rm_block_media_ctrl_t</a> *const p_ctrl)
<a href="#">fsp_err_t</a> (*	<a href="#">read</a> )( <a href="#">rm_block_media_ctrl_t</a> *const p_ctrl, <a href="#">uint8_t</a> *const p_dest_address, <a href="#">uint32_t</a> const block_address, <a href="#">uint32_t</a> const num_blocks)
<a href="#">fsp_err_t</a> (*	<a href="#">write</a> )( <a href="#">rm_block_media_ctrl_t</a> *const p_ctrl, <a href="#">uint8_t</a> const *const p_src_address, <a href="#">uint32_t</a> const block_address, <a href="#">uint32_t</a> const num_blocks)
<a href="#">fsp_err_t</a> (*	<a href="#">erase</a> )( <a href="#">rm_block_media_ctrl_t</a> *const p_ctrl, <a href="#">uint32_t</a> const block_address, <a href="#">uint32_t</a> const num_blocks)

<code>fsp_err_t(*</code>	<code>callbackSet )(rm_block_media_ctrl_t *const p_ctrl, void(*p_callback)(rm_block_media_callback_args_t *), void const *const p_context, rm_block_media_callback_args_t *const p_callback_memory)</code>
<code>fsp_err_t(*</code>	<code>statusGet )(rm_block_media_ctrl_t *const p_ctrl, rm_block_media_status_t *const p_status)</code>
<code>fsp_err_t(*</code>	<code>infoGet )(rm_block_media_ctrl_t *const p_ctrl, rm_block_media_info_t *const p_info)</code>
<code>fsp_err_t(*</code>	<code>close )(rm_block_media_ctrl_t *const p_ctrl)</code>
<code>fsp_err_t(*</code>	<code>versionGet )(fsp_version_t *const p_version)</code>

## Field Documentation

### ◆ open

`fsp_err_t(* rm_block_media_api_t::open) (rm_block_media_ctrl_t *const p_ctrl, rm_block_media_cfg_t const *const p_cfg)`

Initialize block media device. `rm_block_media_api_t::medialnit` must be called to complete the initialization procedure.

### Implemented as

- `RM_BLOCK_MEDIA_SDMMC_Open`
- `RM_BLOCK_MEDIA_USB_Open`

### Parameters

[in]	<code>p_ctrl</code>	Pointer to control block. Must be declared by user. Elements set here.
[in]	<code>p_cfg</code>	Pointer to configuration structure. All elements of this structure must be set by user.

◆ **medialnit**

```
fsp_err_t(* rm_block_media_api_t::medialnit) (rm_block_media_ctrl_t *const p_ctrl)
```

Initializes a media device. If the device is removable, it must be plugged in prior to calling this API. This function blocks until media initialization is complete.

**Implemented as**

- [RM\\_BLOCK\\_MEDIA\\_SDMMC\\_Medialnit](#)
- [RM\\_BLOCK\\_MEDIA\\_USB\\_Medialnit](#)

**Parameters**

[in]	p_ctrl	Control block set in <a href="#">rm_block_media_api_t::open</a> call.
------	--------	-----------------------------------------------------------------------

◆ **read**

```
fsp_err_t(* rm_block_media_api_t::read) (rm_block_media_ctrl_t *const p_ctrl, uint8_t *const p_dest_address, uint32_t const block_address, uint32_t const num_blocks)
```

Reads blocks of data from the specified memory device address to the location specified by the caller.

**Implemented as**

- [RM\\_BLOCK\\_MEDIA\\_SDMMC\\_Read](#)
- [RM\\_BLOCK\\_MEDIA\\_USB\\_Read](#)

**Parameters**

[in]	p_ctrl	Control block set in <a href="#">rm_block_media_api_t::open</a> call.
[out]	p_dest_address	Destination to read the data into.
[in]	block_address	Block address to read the data from.
[in]	num_blocks	Number of blocks of data to read.

## ◆ write

```
fsp_err_t(* rm_block_media_api_t::write) (rm_block_media_ctrl_t *const p_ctrl, uint8_t const *const p_src_address, uint32_t const block_address, uint32_t const num_blocks)
```

Writes blocks of data to the specified device memory address.

**Implemented as**

- RM\_BLOCK\_MEDIA\_SDMMC\_Write
- RM\_BLOCK\_MEDIA\_USB\_Write

**Parameters**

[in]	p_ctrl	Control block set in <a href="#">rm_block_media_api_t::open</a> call.
[in]	p_src_address	Address to read the data to be written.
[in]	block_address	Block address to write the data to.
[in]	num_blocks	Number of blocks of data to write.

## ◆ erase

```
fsp_err_t(* rm_block_media_api_t::erase) (rm_block_media_ctrl_t *const p_ctrl, uint32_t const block_address, uint32_t const num_blocks)
```

Erases blocks of data from the memory device.

**Implemented as**

- RM\_BLOCK\_MEDIA\_SDMMC\_Erase
- RM\_BLOCK\_MEDIA\_USB\_Erase

**Parameters**

[in]	p_ctrl	Control block set in <a href="#">rm_block_media_api_t::open</a> call.
[in]	block_address	Block address to start the erase process at.
[in]	num_blocks	Number of blocks of data to erase.



### ◆ callbackSet

```
fsp_err_t(* rm_block_media_api_t::callbackSet) (rm_block_media_ctrl_t *const p_ctrl, void(
*p_callback)(rm_block_media_callback_args_t *), void const *const p_context,
rm_block_media_callback_args_t *const p_callback_memory)
```

Specify callback function and optional context pointer and working memory pointer.

#### Implemented as

- RM\_BLOCK\_MEDIA\_SDMMC\_CallbackSet()

#### Parameters

[in]	p_ctrl	Control block set in <a href="#">rm_block_media_api_t::open</a> call.
[in]	p_callback	Callback function to register
[in]	p_context	Pointer to send to callback function
[in]	p_working_memory	Pointer to volatile memory where callback structure can be allocated. Callback arguments allocated here are only valid during the callback.

### ◆ statusGet

```
fsp_err_t(* rm_block_media_api_t::statusGet) (rm_block_media_ctrl_t *const p_ctrl,
rm_block_media_status_t *const p_status)
```

Get status of connected device.

#### Implemented as

- RM\_BLOCK\_MEDIA\_SDMMC\_StatusGet
- RM\_BLOCK\_MEDIA\_USB\_StatusGet

#### Parameters

[in]	p_ctrl	Control block set in <a href="#">rm_block_media_api_t::open</a> call.
[out]	p_status	Pointer to store current status.

## ◆ infoGet

```
fsp_err_t(* rm_block_media_api_t::infoGet) (rm_block_media_ctrl_t *const p_ctrl,
rm_block_media_info_t *const p_info)
```

Returns information about the block media device.

**Implemented as**

- [RM\\_BLOCK\\_MEDIA\\_SDMMC\\_InfoGet](#)
- [RM\\_BLOCK\\_MEDIA\\_USB\\_InfoGet](#)

**Parameters**

[in]	p_ctrl	Control block set in <a href="#">rm_block_media_api_t::open</a> call.
[out]	p_info	Pointer to information structure. All elements of this structure will be set by the function.

## ◆ close

```
fsp_err_t(* rm_block_media_api_t::close) (rm_block_media_ctrl_t *const p_ctrl)
```

Closes the module.

**Implemented as**

- [RM\\_BLOCK\\_MEDIA\\_SDMMC\\_Close](#)
- [RM\\_BLOCK\\_MEDIA\\_USB\\_Close](#)

**Parameters**

[in]	p_ctrl	Control block set in <a href="#">rm_block_media_api_t::open</a> call.
------	--------	-----------------------------------------------------------------------

## ◆ versionGet

```
fsp_err_t(* rm_block_media_api_t::versionGet) (fsp_version_t *const p_version)
```

Gets version and stores it in provided pointer p\_version.

**Implemented as**

- [RM\\_BLOCK\\_MEDIA\\_SDMMC\\_VersionGet](#)
- [RM\\_BLOCK\\_MEDIA\\_USB\\_VersionGet](#)

**Parameters**

[out]	p_version	Code and API version used.
-------	-----------	----------------------------

## ◆ rm\_block\_media\_instance\_t

```
struct rm_block_media_instance_t
```

This structure encompasses everything that is needed to use an instance of this interface.

#### Data Fields

<a href="#">rm_block_media_ctrl_t</a> *	p_ctrl	Pointer to the control structure for this instance.
<a href="#">rm_block_media_cfg_t</a> const *	p_cfg	Pointer to the configuration structure for this instance.
<a href="#">rm_block_media_api_t</a> const *	p_api	Pointer to the API structure for this instance.

## Typedef Documentation

### ◆ [rm\\_block\\_media\\_ctrl\\_t](#)

```
typedef void rm\_block\_media\_ctrl\_t
```

Block media API control block. Allocate an instance specific control block to pass into the block media API calls.

#### Implemented as

- [rm\\_block\\_media\\_sdmmc\\_instance\\_ctrl\\_t](#)
- [rm\\_block\\_media\\_usb\\_instance\\_ctrl\\_t](#)

## Enumeration Type Documentation

### ◆ [rm\\_block\\_media\\_event\\_t](#)

```
enum rm\_block\_media\_event\_t
```

Events that can trigger a callback function

#### Enumerator

RM_BLOCK_MEDIA_EVENT_MEDIA_REMOVED	Media removed event.
RM_BLOCK_MEDIA_EVENT_MEDIA_INSERTED	Media inserted event.
RM_BLOCK_MEDIA_EVENT_OPERATION_COMPLETE	Read, write, or erase completed.
RM_BLOCK_MEDIA_EVENT_ERROR	Media inserted event.
RM_BLOCK_MEDIA_EVENT_POLL_STATUS	Poll <a href="#">rm_block_media_api_t::statusGet</a> for write/erase completion.
RM_BLOCK_MEDIA_EVENT_MEDIA_SUSPEND	Media suspended event.
RM_BLOCK_MEDIA_EVENT_MEDIA_RESUME	Media resumed event.

## 4.3.47 FreeRTOS+FAT Port Interface

### Interfaces

#### Detailed Description

Interface for FreeRTOS+FAT port.

### Summary

The FreeRTOS+FAT port provides notifications for insertion and removal of removable media and provides initialization functions required by FreeRTOS+FAT.

The FreeRTOS+FAT interface can be implemented by: [FreeRTOS+FAT Port \(rm\\_freertos\\_plus\\_fat\)](#)

#### Data Structures

struct [rm\\_freertos\\_plus\\_fat\\_callback\\_args\\_t](#)

struct [rm\\_freertos\\_plus\\_fat\\_device\\_t](#)

struct [rm\\_freertos\\_plus\\_fat\\_api\\_t](#)

struct [rm\\_freertos\\_plus\\_fat\\_instance\\_t](#)

#### Enumerations

enum [rm\\_freertos\\_plus\\_fat\\_event\\_t](#)

enum [rm\\_freertos\\_plus\\_fat\\_type\\_t](#)

#### Data Structure Documentation

##### ◆ [rm\\_freertos\\_plus\\_fat\\_callback\\_args\\_t](#)

struct <a href="#">rm_freertos_plus_fat_callback_args_t</a>		
Callback function parameter data		
Data Fields		
<a href="#">rm_freertos_plus_fat_event_t</a>	event	The event can be used to identify what caused the callback.
void const *	p_context	Placeholder for user data.

##### ◆ [rm\\_freertos\\_plus\\_fat\\_device\\_t](#)

struct <a href="#">rm_freertos_plus_fat_device_t</a>
------------------------------------------------------

Information obtained from the media device.

#### Data Fields

uint32_t	sector_count	Sector count.
uint32_t	sector_size_bytes	Sector size in bytes.

#### ◆ rm\_freertos\_plus\_fat\_api\_t

struct rm\_freertos\_plus\_fat\_api\_t

FreeRTOS plus Fat functions implemented at the HAL layer will follow this API.

#### Data Fields

fsp_err_t(*)	<a href="#">open</a> )(rm_freertos_plus_fat_ctrl_t *const p_ctrl, rm_freertos_plus_fat_cfg_t const *const p_cfg)
fsp_err_t(*)	<a href="#">mediaInit</a> )(rm_freertos_plus_fat_ctrl_t *const p_ctrl, rm_freertos_plus_fat_device_t *const p_device)
fsp_err_t(*)	<a href="#">diskInit</a> )(rm_freertos_plus_fat_ctrl_t *const p_ctrl, rm_freertos_plus_fat_disk_cfg_t const *const p_disk_cfg, FF_Disk_t *const p_disk)
fsp_err_t(*)	<a href="#">diskDeinit</a> )(rm_freertos_plus_fat_ctrl_t *const p_ctrl, FF_Disk_t *const p_disk)
fsp_err_t(*)	<a href="#">infoGet</a> )(rm_freertos_plus_fat_ctrl_t *const p_ctrl, FF_Disk_t *const p_disk, rm_freertos_plus_fat_info_t *const p_info)
fsp_err_t(*)	<a href="#">close</a> )(rm_freertos_plus_fat_ctrl_t *const p_ctrl)
fsp_err_t(*)	<a href="#">versionGet</a> )(fsp_version_t *const p_version)

#### Field Documentation

◆ **open**

```
fsp_err_t(* rm_freertos_plus_fat_api_t::open) (rm_freertos_plus_fat_ctrl_t *const p_ctrl,
rm_freertos_plus_fat_cfg_t const *const p_cfg)
```

Open media device.

**Implemented as**

- [RM\\_FREERTOS\\_PLUS\\_FAT\\_Open\(\)](#)

**Parameters**

[in]	p_ctrl	Pointer to control structure.
[in]	p_cfg	Pointer to configuration structure.

◆ **medialnit**

```
fsp_err_t(* rm_freertos_plus_fat_api_t::medialnit) (rm_freertos_plus_fat_ctrl_t *const p_ctrl,
rm_freertos_plus_fat_device_t *const p_device)
```

Initializes a media device. If the device is removable, it must be plugged in prior to calling this API. This function blocks until media initialization is complete.

**Implemented as**

- [RM\\_FREERTOS\\_PLUS\\_FAT\\_Medialnit](#)

**Parameters**

[in]	p_ctrl	Pointer to control structure.
[in]	p_device	Pointer to store device information.

◆ **diskinit**

```
fsp_err_t(* rm_freertos_plus_fat_api_t::diskinit) (rm_freertos_plus_fat_ctrl_t *const p_ctrl,
rm_freertos_plus_fat_disk_cfg_t const *const p_disk_cfg, FF_Disk_t *const p_disk)
```

Initializes a FreeRTOS+FAT FF\_Disk\_t structure.

**Implemented as**

- [RM\\_FREERTOS\\_PLUS\\_FAT\\_Diskinit](#)

**Parameters**

[in]	p_ctrl	Pointer to control structure.
[in]	p_disk_cfg	Pointer to disk configurations
[out]	p_disk	Pointer to store FreeRTOS+FAT disk structure.

◆ **diskDeinit**

```
fsp_err_t(* rm_freertos_plus_fat_api_t::diskDeinit) (rm_freertos_plus_fat_ctrl_t *const p_ctrl,
FF_Disk_t *const p_disk)
```

Deinitializes a FreeRTOS+FAT FF\_Disk\_t structure.

**Implemented as**

- [RM\\_FREERTOS\\_PLUS\\_FAT\\_DiskDeinit](#)

**Parameters**

[in]	p_ctrl	Pointer to control structure.
[in]	p_disk_cfg	Pointer to disk configurations
[out]	p_disk	Pointer to store FreeRTOS+FAT disk structure.

◆ **infoGet**

```
fsp_err_t(* rm_freertos_plus_fat_api_t::infoGet) (rm_freertos_plus_fat_ctrl_t *const p_ctrl, FF_Disk_t
*const p_disk, rm_freertos_plus_fat_info_t *const p_info)
```

Returns information about the media device.

**Implemented as**

- [RM\\_FREERTOS\\_PLUS\\_FAT\\_InfoGet](#)

**Parameters**

[in]	p_ctrl	Pointer to control structure.
[out]	p_info	Pointer to information structure. All elements of this structure will be set by the function.

◆ **close**

```
fsp_err_t(* rm_freertos_plus_fat_api_t::close) (rm_freertos_plus_fat_ctrl_t *const p_ctrl)
```

Close media device.

**Implemented as**

- [RM\\_FREERTOS\\_PLUS\\_FAT\\_Close\(\)](#)

**Parameters**

[in]	p_ctrl	Pointer to control structure.
------	--------	-------------------------------

◆ **versionGet**

```
fsp_err_t(* rm_freertos_plus_fat_api_t::versionGet) (fsp_version_t *const p_version)
```

Get the driver version.

**Implemented as**

- RM\_FREERTOS\_PLUS\_FAT\_VersionGet()

**Parameters**

[in]	p_ctrl	Pointer to control structure.
------	--------	-------------------------------

◆ **rm\_freertos\_plus\_fat\_instance\_t**

```
struct rm_freertos_plus_fat_instance_t
```

This structure encompasses everything that is needed to use an instance of this interface.

## Data Fields

rm_freertos_plus_fat_ctrl_t *	p_ctrl	Pointer to the control structure for this instance.
rm_freertos_plus_fat_cfg_t const *const	p_cfg	Pointer to the configuration structure for this instance.
rm_freertos_plus_fat_api_t const *	p_api	Pointer to the API structure for this instance.

**Enumeration Type Documentation**◆ **rm\_freertos\_plus\_fat\_event\_t**

```
enum rm_freertos_plus_fat_event_t
```

Events that can trigger a callback function

## Enumerator

RM_FREERTOS_PLUS_FAT_EVENT_MEDIA_REMOVED	Media removed event.
RM_FREERTOS_PLUS_FAT_EVENT_MEDIA_INSERTED	Media inserted event.
RM_FREERTOS_PLUS_FAT_EVENT_MEDIA_SUSPENDED	Media suspended event.
RM_FREERTOS_PLUS_FAT_EVENT_MEDIA_RESUMED	Media resumed event.



◆ **rm\_freertos\_plus\_fat\_type\_t**

enum <code>rm_freertos_plus_fat_type_t</code>	
Enumerator	
<code>RM_FREERTOS_PLUS_FAT_TYPE_FAT32</code>	FAT32 disk.
<code>RM_FREERTOS_PLUS_FAT_TYPE_FAT16</code>	FAT16 disk.
<code>RM_FREERTOS_PLUS_FAT_TYPE_FAT12</code>	FAT12 disk.

**4.3.48 LittleFS Interface**[Interfaces](#)**Detailed Description**

Interface for LittleFS access.

**Summary**

The LittleFS Port configures a fail-safe filesystem designed for microcontrollers on top of a lower level storage device.

Implemented by: [LittleFS Flash Port \(rm\\_littlefs\\_flash\)](#)

**Data Structures**

struct [rm\\_littlefs\\_cfg\\_t](#)

struct [rm\\_littlefs\\_api\\_t](#)

struct [rm\\_littlefs\\_instance\\_t](#)

**Typedefs**

typedef void [rm\\_littlefs\\_ctrl\\_t](#)

**Data Structure Documentation**◆ **rm\_littlefs\_cfg\_t**

struct <code>rm_littlefs_cfg_t</code>
User configuration structure, used in open function
Data Fields

struct lfs_config const *	p_lfs_cfg	Pointer LittleFS configuration structure.
void const *	p_extend	Pointer to hardware dependent configuration.

### ◆ rm\_littlefs\_api\_t

struct rm_littlefs_api_t		
LittleFS Port interface API.		
<b>Data Fields</b>		
fsp_err_t(*	open )(rm_littlefs_ctrl_t *const p_ctrl, rm_littlefs_cfg_t const *const p_cfg)	
fsp_err_t(*	close )(rm_littlefs_ctrl_t *const p_ctrl)	
fsp_err_t(*	versionGet )(fsp_version_t *const p_version)	
<b>Field Documentation</b>		
◆ open		
fsp_err_t(* rm_littlefs_api_t::open) (rm_littlefs_ctrl_t *const p_ctrl, rm_littlefs_cfg_t const *const p_cfg)		
Initialize The lower level storage device.		
<b>Implemented as</b>		
◦ RM_LITTLEFS_FLASH_Open		
<b>Parameters</b>		
[in]	p_ctrl	Pointer to control block. Must be declared by user. Elements set here.
[in]	p_cfg	Pointer to configuration structure. All elements of this structure must be set by user.

◆ **close**

```
fsp_err_t(* rm_littlefs_api_t::close) (rm_littlefs_ctrl_t *const p_ctrl)
```

Closes the module and lower level storage device.

**Implemented as**

- [RM\\_LITTLEFS\\_FLASH\\_Close](#)

**Parameters**

[in]	p_ctrl	Control block set in <a href="#">rm_littlefs_api_t::open</a> call.
------	--------	--------------------------------------------------------------------

◆ **versionGet**

```
fsp_err_t(* rm_littlefs_api_t::versionGet) (fsp_version_t *const p_version)
```

Gets version and stores it in provided pointer p\_version.

**Implemented as**

- [RM\\_LITTLEFS\\_FLASH\\_VersionGet](#)

**Parameters**

[out]	p_version	Code and API version used.
-------	-----------	----------------------------

◆ **rm\_littlefs\_instance\_t**

```
struct rm_littlefs_instance_t
```

This structure encompasses everything that is needed to use an instance of this interface.

## Data Fields

<a href="#">rm_littlefs_ctrl_t</a> *	p_ctrl	Pointer to the control structure for this instance.
<a href="#">rm_littlefs_cfg_t</a> const *	p_cfg	Pointer to the configuration structure for this instance.
<a href="#">rm_littlefs_api_t</a> const *	p_api	Pointer to the API structure for this instance.

**Typedef Documentation**

◆ **rm\_littlefs\_ctrl\_t**

```
typedef void rm_littlefs_ctrl_t
```

LittleFS Port API control block. Allocate an instance specific control block to pass into the LittleFS Port API calls.

**Implemented as**

- [rm\\_littlefs\\_flash\\_instance\\_ctrl\\_t](#)

## 4.3.49 MOTOR ANGLE Interface

### Interfaces

#### Detailed Description

Interface for motor angle and speed calculation functions.

## Summary

The MOTOR\_ANGLE interface calculates the rotor angle and rotational speed from other data.

The motor angle interface can be implemented by:

- [Motor Angle and Speed Estimation \(rm\\_motor\\_estimate\)](#)

#### Data Structures

```
struct motor_angle_cfg_t
```

```
struct motor_angle_current_t
```

```
struct motor_angle_api_t
```

```
struct motor_angle_instance_t
```

#### Typedefs

```
typedef void motor_angle_ctrl_t
```

#### Data Structure Documentation

◆ **motor\_angle\_cfg\_t**

```
struct motor_angle_cfg_t
```

Configuration parameters.

◆ **motor\_angle\_current\_t**

struct motor_angle_current_t		
Interface structure		
Data Fields		
float	id	d-axis current
float	iq	q-axis current

◆ **motor\_angle\_api\_t**

struct motor_angle_api_t	
Functions implemented as application interface will follow these APIs.	
<b>Data Fields</b>	
fsp_err_t(*)	<code>open</code> )(motor_angle_ctrl_t *const p_ctrl, motor_angle_cfg_t const *const p_cfg)
fsp_err_t(*)	<code>close</code> )(motor_angle_ctrl_t *const p_ctrl)
fsp_err_t(*)	<code>reset</code> )(motor_angle_ctrl_t *const p_ctrl)
fsp_err_t(*)	<code>currentSet</code> )(motor_angle_ctrl_t *const p_ctrl, motor_angle_current_t *const p_st_current, motor_angle_voltage_reference_t *const p_st_voltage)
fsp_err_t(*)	<code>speedSet</code> )(motor_angle_ctrl_t *const p_ctrl, float const speed_ctrl, float const damp_speed)
fsp_err_t(*)	<code>flagPiCtrlSet</code> )(motor_angle_ctrl_t *const p_ctrl, uint32_t const flag_pi)
fsp_err_t(*)	<code>angleSpeedGet</code> )(motor_angle_ctrl_t *const p_ctrl, float *const p_angle, float *const p_speed, float *const p_phase_err)
fsp_err_t(*)	<code>estimatedComponentGet</code> )(motor_angle_ctrl_t *const p_ctrl, float *const p_ed, float *const p_eq)
fsp_err_t(*)	<code>parameterUpdate</code> )(motor_angle_ctrl_t *const p_ctrl, motor_angle_cfg_t const *p_cfg)

fsp_err_t(*	versionGet )(fsp_version_t *const p_version)
-------------	----------------------------------------------

## Field Documentation

### ◆ open

`fsp_err_t(* motor_angle_api_t::open) (motor_angle_ctrl_t *const p_ctrl, motor_angle_cfg_t const *const p_cfg)`

Initialize the Motor\_Angle.

#### Implemented as

- [RM\\_MOTOR\\_ESTIMATE\\_Open\(\)](#)

#### Parameters

[in]	p_ctrl	Pointer to control structure.
[in]	p_cfg	Pointer to configuration structure.

### ◆ close

`fsp_err_t(* motor_angle_api_t::close) (motor_angle_ctrl_t *const p_ctrl)`

Close (Finish) the Motor\_Angle.

#### Implemented as

- [RM\\_MOTOR\\_ESTIMATE\\_Close\(\)](#)

#### Parameters

[in]	p_ctrl	Pointer to control structure.
------	--------	-------------------------------

### ◆ reset

`fsp_err_t(* motor_angle_api_t::reset) (motor_angle_ctrl_t *const p_ctrl)`

Reset the Motor\_Angle.

#### Implemented as

- [RM\\_MOTOR\\_ESTIMATE\\_Reset\(\)](#)

#### Parameters

[in]	p_ctrl	Pointer to control structure.
------	--------	-------------------------------

◆ **currentSet**

```
fsp_err_t(* motor_angle_api_t::currentSet) (motor_angle_ctrl_t *const p_ctrl, motor_angle_current_t *const p_st_current, motor_angle_voltage_reference_t *const p_st_voltage)
```

Set (Input) Current & Voltage Reference data into the Motor\_Angle.

**Implemented as**

- RM\_MOTOR\_ESTIMATE\_CurrentSet()

**Parameters**

[in]	p_ctrl	Pointer to control structure.
[in]	p_st_current	Pointer to current structure
[in]	p_st_voltage	Pointer to voltage Reference structure

◆ **speedSet**

```
fsp_err_t(* motor_angle_api_t::speedSet) (motor_angle_ctrl_t *const p_ctrl, float const speed_ctrl, float const damp_speed)
```

Set (Input) Speed Information into the Motor\_Angle.

**Implemented as**

- RM\_MOTOR\_ESTIMATE\_SpeedSet()

**Parameters**

[in]	p_ctrl	Pointer to control structure.
[in]	speed_ctrl	Control reference of rotational speed [rad/s]
[in]	damp_speed	Damping rotational speed [rad/s]

◆ **flagPiCtrlSet**

```
fsp_err_t(* motor_angle_api_t::flagPiCtrlSet) (motor_angle_ctrl_t *const p_ctrl, uint32_t const flag_pi)
```

Set the flag of PI Control runs.

**Implemented as**

- RM\_MOTOR\_ESTIMATE\_FlagPiCtrlSet()

**Parameters**

[in]	p_ctrl	Pointer to control structure.
[in]	flag_pi	The flag of PI control runs

### ◆ angleSpeedGet

`fsp_err_t(* motor_angle_api_t::angleSpeedGet) (motor_angle_ctrl_t *const p_ctrl, float *const p_angle, float *const p_speed, float *const p_phase_err)`

Get rotor angle and rotational speed from the Motor\_Angle.

#### Implemented as

- `RM_MOTOR_ESTIMATE_AngleSpeedGet()`

#### Parameters

[in]	p_ctrl	Pointer to control structure.
[out]	p_angl	Memory address to get rotor angle data
[out]	p_speed	Memory address to get rotational speed data
[out]	p_phase_err	Memory address to get phase(angle) error data

### ◆ estimatedComponentGet

`fsp_err_t(* motor_angle_api_t::estimatedComponentGet) (motor_angle_ctrl_t *const p_ctrl, float *const p_ed, float *const p_eq)`

Get estimated d/q-axis component from the Motor\_Angle.

#### Implemented as

- `RM_MOTOR_ESTIMATE_EstimatedComponentGet()`

#### Parameters

[in]	p_ctrl	Pointer to control structure.
[out]	p_ed	Memory address to get estimated d-axis component
[out]	p_eq	Memory address to get estimated q-axis component



### ◆ parameterUpdate

```
fsp_err_t(* motor_angle_api_t::parameterUpdate) (motor_angle_ctrl_t *const p_ctrl,
motor_angle_cfg_t const *p_cfg)
```

Update Parameters for the calculation in the Motor\_Angle.

#### Implemented as

- RM\_MOTOR\_ESTIMATE\_ParameterUpdate()

#### Parameters

[in]	p_ctrl	Pointer to control structure.
[in]	p_cfg	Pointer to configuration structure include update parameters.

### ◆ versionGet

```
fsp_err_t(* motor_angle_api_t::versionGet) (fsp_version_t *const p_version)
```

Return the version of the driver.

#### Implemented as

- RM\_MOTOR\_ESTIMATE\_VersionGet()

#### Parameters

[out]	p_version	Memory address to return version information to.
-------	-----------	--------------------------------------------------

### ◆ motor\_angle\_instance\_t

```
struct motor_angle_instance_t
```

This structure encompasses everything that is needed to use an instance of this interface.

#### Data Fields

motor_angle_ctrl_t *	p_ctrl	Pointer to the control structure for this instance.
motor_angle_cfg_t const *	p_cfg	Pointer to the configuration structure for this instance.
motor_angle_api_t const *	p_api	Pointer to the API structure for this instance.

## Typedef Documentation

**◆ motor\_angle\_ctrl\_t**

```
typedef void motor_angle_ctrl_t
```

Motor Angle Control block. Allocate an instance specific control block to pass into the API calls.

**Implemented as**

- motor\_angle\_ctrl\_t

**4.3.50 Interface**[Interfaces](#)**Detailed Description**

Interface for motor current functions.

**Summary**

The MOTOR\_CURRENT interface for getting the PWM modulation duty from electric current and speed

The motor current control interface can be implemented by:

- [Motor Current \(rm\\_motor\\_current\)](#)

**Data Structures**

```
struct motor_current_cfg_t
```

```
struct motor_current_api_t
```

```
struct motor_current_instance_t
```

**Typedefs**

```
typedef void motor_current_ctrl_t
```

**Enumerations**

```
enum motor_current_event_t
```

**Data Structure Documentation****◆ motor\_current\_cfg\_t**

```
struct motor_current_cfg_t
```

Configuration parameters.

### ◆ motor\_current\_api\_t

struct motor\_current\_api\_t

Functions implemented at the Motor Current Module will follow these APIs.

#### Data Fields

fsp_err_t(*)	open )(motor_current_ctrl_t *const p_ctrl, motor_current_cfg_t const *const p_cfg)
fsp_err_t(*)	close )(motor_current_ctrl_t *const p_ctrl)
fsp_err_t(*)	reset )(motor_current_ctrl_t *const p_ctrl)
fsp_err_t(*)	run )(motor_current_ctrl_t *const p_ctrl)
fsp_err_t(*)	parameterSet )(motor_current_ctrl_t *const p_ctrl, motor_current_input_t const *const p_st_input)
fsp_err_t(*)	currentReferenceSet )(motor_current_ctrl_t *const p_ctrl, float const id_reference, float const iq_reference)
fsp_err_t(*)	speedPhaseSet )(motor_current_ctrl_t *const p_ctrl, float const speed_rad, float const phase_rad)
fsp_err_t(*)	currentSet )(motor_current_ctrl_t *const p_ctrl, motor_current_input_current_t const *const p_st_current, motor_current_input_voltage_t const *const p_st_voltage)
fsp_err_t(*)	parameterGet )(motor_current_ctrl_t *const p_ctrl, motor_current_output_t *const p_st_output)
fsp_err_t(*)	currentGet )(motor_current_ctrl_t *const p_ctrl, float *const p_id, float *const p_iq)
fsp_err_t(*)	phaseVoltageGet )(motor_current_ctrl_t *const p_ctrl, motor_current_get_voltage_t *const p_voltage)

<code>fsp_err_t(*</code>	<code>parameterUpdate )(motor_current_ctrl_t *const p_ctrl, motor_current_cfg_t const *const p_cfg)</code>
<code>fsp_err_t(*</code>	<code>versionGet )(fsp_version_t *const p_version)</code>
<b>Field Documentation</b>	
◆ <b>open</b>	
<code>fsp_err_t(* motor_current_api_t::open) (motor_current_ctrl_t *const p_ctrl, motor_current_cfg_t const *const p_cfg)</code>	
Initialize the Motor Current Module.	
<b>Implemented as</b>	
◦ <a href="#">RM_MOTOR_CURRENT_Open()</a>	
<b>Parameters</b>	
[in]	<code>p_ctrl</code> Pointer to control structure.
[in]	<code>p_cfg</code> Pointer to configuration structure.
◆ <b>close</b>	
<code>fsp_err_t(* motor_current_api_t::close) (motor_current_ctrl_t *const p_ctrl)</code>	
Close (Finish) the Motor Current Module.	
<b>Implemented as</b>	
◦ <a href="#">RM_MOTOR_CURRENT_Close()</a>	
<b>Parameters</b>	
[in]	<code>p_ctrl</code> Pointer to control structure.
◆ <b>reset</b>	
<code>fsp_err_t(* motor_current_api_t::reset) (motor_current_ctrl_t *const p_ctrl)</code>	
Reset variables for the Motor Current Module.	
<b>Implemented as</b>	
◦ <a href="#">RM_MOTOR_CURRENT_Reset()</a>	
<b>Parameters</b>	
[in]	<code>p_ctrl</code> Pointer to control structure.

◆ **run**

```
fsp_err_t(* motor_current_api_t::run) (motor_current_ctrl_t *const p_ctrl)
```

Activate the Motor Current Control.

**Implemented as**

- [RM\\_MOTOR\\_CURRENT\\_Run\(\)](#)

**Parameters**

[in]	p_ctrl	Pointer to control structure.
------	--------	-------------------------------

◆ **parameterSet**

```
fsp_err_t(* motor_current_api_t::parameterSet) (motor_current_ctrl_t *const p_ctrl,
motor_current_input_t const *const p_st_input)
```

Set (Input) parameters into the Motor Current Module.

**Implemented as**

- [RM\\_MOTOR\\_CURRENT\\_ParameterSet\(\)](#)

**Parameters**

[in]	p_ctrl	Pointer to control structure.
[in]	p_st_input	Pointer to input data structure(speed control output data)

◆ **currentReferenceSet**

```
fsp_err_t(* motor_current_api_t::currentReferenceSet) (motor_current_ctrl_t *const p_ctrl, float
const id_reference, float const iq_reference)
```

Set (Input) Current reference into the Motor Current Module.

**Implemented as**

- [RM\\_MOTOR\\_CURRENT\\_CurrentReferenceSet\(\)](#)

**Parameters**

[in]	p_ctrl	Pointer to control structure.
[in]	id_reference	D-axis current Reference [A]
[in]	iq_reference	Q-axis current Reference [A]

### ◆ speedPhaseSet

`fsp_err_t(* motor_current_api_t::speedPhaseSet) (motor_current_ctrl_t *const p_ctrl, float const speed_rad, float const phase_rad)`

Set (Input) Speed & Phase data into the Motor Current Module.

#### Implemented as

- `RM_MOTOR_CURRENT_SpeedPhaseSet()`

#### Parameters

[in]	p_ctrl	Pointer to control structure.
[in]	speed_rad	Rotational speed [rad/s]
[in]	phase_rad	Rotor phase [rad]

### ◆ currentSet

`fsp_err_t(* motor_current_api_t::currentSet) (motor_current_ctrl_t *const p_ctrl, motor_current_input_current_t const *const p_st_current, motor_current_input_voltage_t const *const p_st_voltage)`

Set (Input) Current data into the Motor Current Module.

#### Implemented as

- `RM_MOTOR_CURRENT_CurrentSet()`

#### Parameters

[in]	p_ctrl	Pointer to control structure.
[in]	p_st_current	Pointer to input current structure
[in]	p_st_voltage	Pointer to input voltage structure

◆ **parameterGet**

```
fsp_err_t(* motor_current_api_t::parameterGet) (motor_current_ctrl_t *const p_ctrl,
motor_current_output_t *const p_st_output)
```

Get (output) parameters from the Motor Current Module

**Implemented as**

- [RM\\_MOTOR\\_CURRENT\\_ParameterGet\(\)](#)

**Parameters**

[in]	p_ctrl	Pointer to control structure.
[out]	p_st_output	Pointer to output data structure(speed control input data)

◆ **currentGet**

```
fsp_err_t(* motor_current_api_t::currentGet) (motor_current_ctrl_t *const p_ctrl, float *const p_id,
float *const p_iq)
```

Get d/q-axis current

**Implemented as**

- [RM\\_MOTOR\\_CURRENT\\_CurrentGet\(\)](#)

**Parameters**

[in]	p_ctrl	Pointer to control structure.
[out]	p_id	Pointer to get d-axis current [A]
[out]	p_iq	Pointer to get q-axis current [A]

◆ **phaseVoltageGet**

```
fsp_err_t(* motor_current_api_t::phaseVoltageGet) (motor_current_ctrl_t *const p_ctrl,
motor_current_get_voltage_t *const p_voltage)
```

Get Phase Output Voltage

**Implemented as**

- [RM\\_MOTOR\\_CURRENT\\_PhaseVoltageGet\(\)](#)

**Parameters**

[in]	p_ctrl	Pointer to control structure.
[out]	p_voltage	Pointer to get Voltages

◆ **parameterUpdate**

```
fsp_err_t(* motor_current_api_t::parameterUpdate) (motor_current_ctrl_t *const p_ctrl,
motor_current_cfg_t const *const p_cfg)
```

Update Parameters for the calculation in the Motor Current Control.

**Implemented as**

- [RM\\_MOTOR\\_CURRENT\\_ParameterUpdate\(\)](#)

**Parameters**

[in]	p_ctrl	Pointer to control structure.
[in]	p_cfg	Pointer to configuration structure include update parameters.

◆ **versionGet**

```
fsp_err_t(* motor_current_api_t::versionGet) (fsp_version_t *const p_version)
```

Return the version of the driver.

**Implemented as**

- [RM\\_MOTOR\\_CURRENT\\_VersionGet\(\)](#)

**Parameters**

[out]	p_version	Memory address to return version information to.
-------	-----------	--------------------------------------------------

◆ **motor\_current\_instance\_t**

```
struct motor_current_instance_t
```

This structure encompasses everything that is needed to use an instance of this interface.

## Data Fields

motor_current_ctrl_t *	p_ctrl	Pointer to the control structure for this instance.
motor_current_cfg_t const *	p_cfg	Pointer to the configuration structure for this instance.
motor_current_api_t const *	p_api	Pointer to the API structure for this instance.

**Typedef Documentation**



◆ **motor\_current\_ctrl\_t**

```
typedef void motor_current_ctrl_t
```

Control block. Allocate an instance specific control block to pass into the API calls.

**Implemented as**

- motor\_current\_ctrl\_t

**Enumeration Type Documentation**◆ **motor\_current\_event\_t**

```
enum motor_current_event_t
```

Events that can trigger a callback function

## Enumerator

MOTOR_CURRENT_EVENT_FORWARD	Event forward Speed Control.
MOTOR_CURRENT_EVENT_DATA_SET	Event Set Speed Control Output Data.
MOTOR_CURRENT_EVENT_BACKWARD	Event backward Speed Control.

**4.3.51 MOTOR\_DRIVER Interface**[Interfaces](#)**Detailed Description**

Interface for motor driver functions.

**Summary**

The MOTOR\_DRIVER interface for setting the PWM modulation duty

The motor current control interface can be implemented by:

- [Motor Driver \(rm\\_motor\\_driver\)](#)

**Data Structures**

```
struct motor_driver_callback_args_t
```

```
struct motor_driver_current_get_t
```

```
struct motor_driver_cfg_t
```

```
struct motor_driver_api_t
```

```
struct motor_driver_instance_t
```

## Typedefs

```
typedef void motor_driver_ctrl_t
```

## Enumerations

```
enum motor_driver_event_t
```

## Data Structure Documentation

### ◆ motor\_driver\_callback\_args\_t

struct motor_driver_callback_args_t		
Callback function parameter data		
Data Fields		
motor_driver_event_t	event	Event trigger.
void const *	p_context	Placeholder for user data.

### ◆ motor\_driver\_current\_get\_t

struct motor_driver_current_get_t		
Current Data Get Structure		
Data Fields		
float	iu	U phase current [A].
float	iw	W phase current [A].
float	vdc	Main Line Voltage [V].
float	va_max	maximum magnitude of voltage vector

### ◆ motor\_driver\_cfg\_t

struct motor_driver_cfg_t		
Configuration parameters.		
<b>Data Fields</b>		
adc_channel_t	iu_ad_ch	A/D Channel for U Phase Current.

<code>adc_channel_t</code>	<code>iw_ad_ch</code>
	A/D Channel for W Phase Current.
<code>adc_channel_t</code>	<code>vdc_ad_ch</code>
	A/D Channel for Main Line Voltage.
<code>void const *</code>	<code>p_context</code>
	Placeholder for user data.

#### ◆ motor\_driver\_api\_t

struct motor_driver_api_t	
Functions implemented at the HAL layer will follow these APIs.	
<b>Data Fields</b>	
<code>fsp_err_t(*)</code>	<code>open</code> )(motor_driver_ctrl_t *const p_ctrl, motor_driver_cfg_t const *const p_cfg)
<code>fsp_err_t(*)</code>	<code>close</code> )(motor_driver_ctrl_t *const p_ctrl)
<code>fsp_err_t(*)</code>	<code>reset</code> )(motor_driver_ctrl_t *const p_ctrl)
<code>fsp_err_t(*)</code>	<code>phaseVoltageSet</code> )(motor_driver_ctrl_t *const p_ctrl, float const u_voltage, float const v_voltage, float const w_voltage)
<code>fsp_err_t(*)</code>	<code>currentGet</code> )(motor_driver_ctrl_t *const p_ctrl, motor_driver_current_get_t *const p_current_get)
<code>fsp_err_t(*)</code>	<code>flagCurrentOffsetGet</code> )(motor_driver_ctrl_t *const p_ctrl, uint8_t *const p_flag_offset)
<code>fsp_err_t(*)</code>	<code>currentOffsetRestart</code> )(motor_driver_ctrl_t *const p_ctrl)
<code>fsp_err_t(*)</code>	<code>parameterUpdate</code> )(motor_driver_ctrl_t *const p_ctrl, motor_driver_cfg_t const *const p_cfg)

<code>fsp_err_t(*</code>	<code>versionGet )(fsp_version_t *const p_version)</code>
--------------------------	-----------------------------------------------------------

## Field Documentation

### ◆ open

<code>fsp_err_t(* motor_driver_api_t::open) (motor_driver_ctrl_t *const p_ctrl, motor_driver_cfg_t const *const p_cfg)</code>
-------------------------------------------------------------------------------------------------------------------------------

Initialize the Motor Driver Module.

#### Implemented as

- [RM\\_MOTOR\\_DRIVER\\_Open\(\)](#)

#### Parameters

[in]	p_ctrl	Pointer to control structure.
[in]	p_cfg	Pointer to configuration structure.

### ◆ close

<code>fsp_err_t(* motor_driver_api_t::close) (motor_driver_ctrl_t *const p_ctrl)</code>
-----------------------------------------------------------------------------------------

Close the Motor Driver Module

#### Implemented as

- [RM\\_MOTOR\\_DRIVER\\_Close\(\)](#)

#### Parameters

[in]	p_ctrl	Pointer to control structure.
------	--------	-------------------------------

### ◆ reset

<code>fsp_err_t(* motor_driver_api_t::reset) (motor_driver_ctrl_t *const p_ctrl)</code>
-----------------------------------------------------------------------------------------

Reset variables of the Motor Driver Module

#### Implemented as

- [RM\\_MOTOR\\_DRIVER\\_Reset\(\)](#)

#### Parameters

[in]	p_ctrl	Pointer to control structure.
------	--------	-------------------------------

### ◆ phaseVoltageSet

`fsp_err_t(* motor_driver_api_t::phaseVoltageSet) (motor_driver_ctrl_t *const p_ctrl, float const u_voltage, float const v_voltage, float const w_voltage)`

Set (Input) Phase Voltage data into the Motor Driver Module

#### Implemented as

- `RM_MOTOR_DRIVER_PhaseVoltageSet()`

#### Parameters

[in]	p_ctrl	Pointer to control structure.
[in]	u_voltage	U phase voltage [V]
[in]	v_voltage	V phase voltage [V]
[in]	w_voltage	W phase voltage [V]

### ◆ currentGet

`fsp_err_t(* motor_driver_api_t::currentGet) (motor_driver_ctrl_t *const p_ctrl, motor_driver_current_get_t *const p_current_get)`

Get Phase current, Vdc and Va\_max data from the Motor Driver Module

#### Implemented as

- `RM_MOTOR_DRIVER_CurrentGet()`

#### Parameters

[in]	p_ctrl	Pointer to control structure.
[out]	p_current_get	Pointer to get data structure.

### ◆ flagCurrentOffsetGet

`fsp_err_t(* motor_driver_api_t::flagCurrentOffsetGet) (motor_driver_ctrl_t *const p_ctrl, uint8_t *const p_flag_offset)`

Get the flag of finish current offset detection from the Motor Driver Module

#### Implemented as

- `RM_MOTOR_DRIVER_FlagCurrentOffsetGet()`

#### Parameters

[in]	p_ctrl	Pointer to control structure.
[out]	p_flag_offset	Flag of finish current offset detection

◆ **currentOffsetRestart**

```
fsp_err_t(* motor_driver_api_t::currentOffsetRestart) (motor_driver_ctrl_t *const p_ctrl)
```

Restart current offset detection

**Implemented as**

- RM\_MOTOR\_DRIVER\_CurrentOffsetRestart()

**Parameters**

[in]	p_ctrl	Pointer to control structure.
------	--------	-------------------------------

◆ **parameterUpdate**

```
fsp_err_t(* motor_driver_api_t::parameterUpdate) (motor_driver_ctrl_t *const p_ctrl,  
motor_driver_cfg_t const *const p_cfg)
```

Update Configuration Parameters for the calculation in the Motor Driver Module

**Implemented as**

- RM\_MOTOR\_DRIVER\_ParameterUpdate()

**Parameters**

[in]	p_ctrl	Pointer to control structure.
[in]	p_cfg	Pointer to configuration structure include update parameters.

◆ **versionGet**

```
fsp_err_t(* motor_driver_api_t::versionGet) (fsp_version_t *const p_version)
```

Return the version of the driver.

**Implemented as**

- RM\_MOTOR\_DRIVER\_VersionGet()

**Parameters**

[out]	p_version	Memory address to return version information to.
-------	-----------	--------------------------------------------------

◆ **motor\_driver\_instance\_t**

```
struct motor_driver_instance_t
```

This structure encompasses everything that is needed to use an instance of this interface.

## Data Fields

motor_driver_ctrl_t*	p_ctrl	Pointer to the control structure for this instance.
----------------------	--------	-----------------------------------------------------

<code>motor_driver_cfg_t</code> const *	<code>p_cfg</code>	Pointer to the configuration structure for this instance.
<code>motor_driver_api_t</code> const *	<code>p_api</code>	Pointer to the API structure for this instance.

## Typedef Documentation

### ◆ `motor_driver_ctrl_t`

typedef void <code>motor_driver_ctrl_t</code>
Control block. Allocate an instance specific control block to pass into the API calls.
<b>Implemented as</b>
◦ <code>motor_driver_ctrl_t</code>

## Enumeration Type Documentation

### ◆ `motor_driver_event_t`

enum <code>motor_driver_event_t</code>	
Events that can trigger a callback function	
Enumerator	
<code>MOTOR_DRIVER_EVENT_FORWARD</code>	Event before Motor Driver Process (before Current Control timing)
<code>MOTOR_DRIVER_EVENT_CURRENT</code>	Event Current Control timing.
<code>MOTOR_DRIVER_EVENT_BACKWARD</code>	Event after Motor Driver Process (after PWM duty setting)

## 4.3.52 MOTOR SPEED Interface

### Interfaces

#### Detailed Description

Interface for motor speed functions.

## Summary

The `MOTOR_SPEED` interface for getting the current references from electric current and rotational speed

The motor speed interface can be implemented by:

- [Motor Speed \(rm\\_motor\\_speed\)](#)

## Data Structures

```
struct motor_speed_callback_args_t
```

```
struct motor_speed_cfg_t
```

```
struct motor_speed_api_t
```

```
struct motor_speed_instance_t
```

## Typedefs

```
typedef void motor_speed_ctrl_t
```

## Enumerations

```
enum motor_speed_event_t
```

## Data Structure Documentation

### ◆ motor\_speed\_callback\_args\_t

struct motor_speed_callback_args_t		
Callback function parameter data		
Data Fields		
void const *	p_context	Placeholder for user data.
<a href="#">motor_speed_event_t</a>	event	

### ◆ motor\_speed\_cfg\_t

struct motor_speed_cfg_t		
Configuration parameters.		
<b>Data Fields</b>		
motor_speed_input_t *	<a href="#">st_input</a>	
		Input data structure for automatic set.
motor_speed_output_t *	<a href="#">st_output</a>	
		Output data structure for automatic receive.
void const *	<a href="#">p_context</a>	



	Placeholder for user data.

### ◆ motor\_speed\_api\_t

struct motor_speed_api_t	
Functions implemented at the HAL layer will follow these APIs.	
<b>Data Fields</b>	
fsp_err_t(*)	open )(motor_speed_ctrl_t *const p_ctrl, motor_speed_cfg_t const *const p_cfg)
fsp_err_t(*)	close )(motor_speed_ctrl_t *const p_ctrl)
fsp_err_t(*)	reset )(motor_speed_ctrl_t *const p_ctrl)
fsp_err_t(*)	run )(motor_speed_ctrl_t *const p_ctrl)
fsp_err_t(*)	speedReferenceSet )(motor_speed_ctrl_t *const p_ctrl, float const speed_reference_rpm)
fsp_err_t(*)	parameterSet )(motor_speed_ctrl_t *const p_ctrl, motor_speed_input_t const *const p_st_input)
fsp_err_t(*)	speedControl )(motor_speed_ctrl_t *const p_ctrl)
fsp_err_t(*)	parameterGet )(motor_speed_ctrl_t *const p_ctrl, motor_speed_output_t *const p_st_output)
fsp_err_t(*)	parameterUpdate )(motor_speed_ctrl_t *const p_ctrl, motor_speed_cfg_t const *const p_cfg)
fsp_err_t(*)	versionGet )(fsp_version_t *const p_version)
<b>Field Documentation</b>	

◆ **open**

```
fsp_err_t(* motor_speed_api_t::open) (motor_speed_ctrl_t *const p_ctrl, motor_speed_cfg_t const *const p_cfg)
```

Initialize the Motor Speed Module.

**Implemented as**

- [RM\\_MOTOR\\_SPEED\\_Open\(\)](#)

**Parameters**

[in]	p_ctrl	Pointer to control structure.
[in]	p_cfg	Pointer to configuration structure.

◆ **close**

```
fsp_err_t(* motor_speed_api_t::close) (motor_speed_ctrl_t *const p_ctrl)
```

Close (Finish) the Motor Speed Module.

**Implemented as**

- [RM\\_MOTOR\\_SPEED\\_Close\(\)](#)

**Parameters**

[in]	p_ctrl	Pointer to control structure.
------	--------	-------------------------------

◆ **reset**

```
fsp_err_t(* motor_speed_api_t::reset) (motor_speed_ctrl_t *const p_ctrl)
```

Reset(Stop) the Motor Speed Module.

**Implemented as**

- [RM\\_MOTOR\\_SPEED\\_Reset\(\)](#)

**Parameters**

[in]	p_ctrl	Pointer to control structure.
------	--------	-------------------------------

◆ **run**

```
fsp_err_t(* motor_speed_api_t::run) (motor_speed_ctrl_t *const p_ctrl)
```

Activate the Motor Speed Control.

**Implemented as**

- RM\_MOTOR\_SPEED\_Run()

**Parameters**

[in]	p_ctrl	Pointer to control structure.
------	--------	-------------------------------

◆ **speedReferenceSet**

```
fsp_err_t(* motor_speed_api_t::speedReferenceSet) (motor_speed_ctrl_t *const p_ctrl, float const speed_reference_rpm)
```

Set (Input) Speed reference into the Motor Speed Module.

**Implemented as**

- RM\_MOTOR\_SPEED\_SpeedReferenceSet()

**Parameters**

[in]	p_ctrl	Pointer to control structure.
[in]	speed_refernce_rpm	Speed reference [rpm]

◆ **parameterSet**

```
fsp_err_t(* motor_speed_api_t::parameterSet) (motor_speed_ctrl_t *const p_ctrl, motor_speed_input_t const *const p_st_input)
```

Set (Input) Speed Parameters into the Motor Speed Module.

**Implemented as**

- RM\_MOTOR\_SPEED\_ParameterSet()

**Parameters**

[in]	p_ctrl	Pointer to control structure.
[in]	p_st_input	Pointer to structure to input parameters.

◆ **speedControl**

```
fsp_err_t(* motor_speed_api_t::speedControl) (motor_speed_ctrl_t *const p_ctrl)
```

Calculate Current Reference

**Implemented as**

- [RM\\_MOTOR\\_SPEED\\_SpeedControl\(\)](#)

**Parameters**

[in]	p_ctrl	Pointer to control structure.
------	--------	-------------------------------

◆ **parameterGet**

```
fsp_err_t(* motor_speed_api_t::parameterGet) (motor_speed_ctrl_t *const p_ctrl,  
motor_speed_output_t *const p_st_output)
```

Get Speed Control Output Parameters

**Implemented as**

- [RM\\_MOTOR\\_SPEED\\_ParameterGet\(\)](#)

**Parameters**

[in]	p_ctrl	Pointer to control structure.
[out]	p_st_output	Pointer to get speed control parameters

◆ **parameterUpdate**

```
fsp_err_t(* motor_speed_api_t::parameterUpdate) (motor_speed_ctrl_t *const p_ctrl,  
motor_speed_cfg_t const *const p_cfg)
```

Update Parameters for the calculation in the Motor Speed Module.

**Implemented as**

- [RM\\_MOTOR\\_SPEED\\_ParameterUpdate\(\)](#)

**Parameters**

[in]	p_ctrl	Pointer to control structure.
[in]	p_cfg	Pointer to configuration structure include update parameters.

◆ **versionGet**

```
fsp_err_t(* motor_speed_api_t::versionGet) (fsp_version_t *const p_version)
```

Return the version of the driver.

**Implemented as**

- RM\_MOTOR\_SPEED\_VersionGet()

**Parameters**

[out]	p_version	Memory address to return version information to.
-------	-----------	--------------------------------------------------

◆ **motor\_speed\_instance\_t**

```
struct motor_speed_instance_t
```

This structure encompasses everything that is needed to use an instance of this interface.

## Data Fields

<code>motor_speed_ctrl_t *</code>	p_ctrl	Pointer to the control structure for this instance.
<code>motor_speed_cfg_t const *</code>	p_cfg	Pointer to the configuration structure for this instance.
<code>motor_speed_api_t const *</code>	p_api	Pointer to the API structure for this instance.

**Typedef Documentation**◆ **motor\_speed\_ctrl\_t**

```
typedef void motor_speed_ctrl_t
```

Control block. Allocate an instance specific control block to pass into the API calls.

**Implemented as**

- motor\_speed\_ctrl\_t

**Enumeration Type Documentation**

◆ **motor\_speed\_event\_t**

enum <a href="#">motor_speed_event_t</a>	
Events that can trigger a callback function	
Enumerator	
MOTOR_SPEED_EVENT_FORWARD	Event forward Speed Control.
MOTOR_SPEED_EVENT_BACKWARD	Event backward Speed Control.

**4.3.53 Touch Middleware Interface**[Interfaces](#)**Detailed Description**

Interface for Touch Middleware functions.

**Summary**

The TOUCH interface provides TOUCH functionality.

The TOUCH interface can be implemented by:

- [Capacitive Touch Middleware \(rm\\_touch\)](#)

**Data Structures**

struct [touch\\_button\\_cfg\\_t](#)

struct [touch\\_slider\\_cfg\\_t](#)

struct [touch\\_wheel\\_cfg\\_t](#)

struct [touch\\_pad\\_cfg\\_t](#)

struct [touch\\_cfg\\_t](#)

struct [touch\\_api\\_t](#)

struct [touch\\_instance\\_t](#)

**Typedefs**

typedef void [touch\\_ctrl\\_t](#)

```
typedef struct touch_callback_args_t
st_ctsu_callback_args
```

## Data Structure Documentation

### ◆ touch\_button\_cfg\_t

struct touch_button_cfg_t		
Configuration of each button		
Data Fields		
uint8_t	elem_index	Element number used by this button.
uint16_t	threshold	Touch/non-touch judgment threshold.
uint16_t	hysteresis	Threshold hysteresis for chattering prevention.

### ◆ touch\_slider\_cfg\_t

struct touch_slider_cfg_t		
Configuration of each slider		
Data Fields		
uint8_t const *	p_elem_index	Element number array used by this slider.
uint8_t	num_elements	Number of elements used by this slider.
uint16_t	threshold	Position calculation start threshold value.

### ◆ touch\_wheel\_cfg\_t

struct touch_wheel_cfg_t		
Configuration of each wheel		
Data Fields		
uint8_t const *	p_elem_index	Element number array used by this wheel.
uint8_t	num_elements	Number of elements used by this wheel.
uint16_t	threshold	Position calculation start threshold value.

### ◆ touch\_pad\_cfg\_t

struct touch_pad_cfg_t		
Configuration of each pads		

Data Fields		
uint8_t const *	p_elem_index_rx	RX of element number arrays used by this pad.
uint8_t const *	p_elem_index_tx	TX of element number arrays used by this pad.
uint8_t	num_elements	Number of elements used by this pad.
uint16_t	threshold	Coordinate calculation threshold value.
uint16_t	rx_pixel	rx coordinate resolution
uint16_t	tx_pixel	tx coordinate resolution
uint8_t	max_touch	Maximum number of touch judgments used by the pad.
uint8_t	num_drift	Number of pad drift.

## ◆ touch\_cfg\_t

Data Fields		
struct touch_cfg_t		
User configuration structure, used in open function		
Data Fields		
touch_button_cfg_t const *	p_buttons	Pointer to array of button configuration.
touch_slider_cfg_t const *	p_sliders	Pointer to array of slider configuration.
touch_wheel_cfg_t const *	p_wheels	Pointer to array of wheel configuration.
touch_pad_cfg_t const *	p_pad	Pointer of pad configuration.
uint8_t	num_buttons	Number of buttons.
uint8_t	num_sliders	Number of sliders.
uint8_t	num_wheels	Number of wheels.
uint8_t	on_freq	The cumulative number of determinations of ON.
uint8_t	off_freq	The cumulative number of determinations of OFF.
uint16_t	drift_freq	Base value drift frequency. [0 : no use].
uint16_t	cancel_freq	Maximum continuous ON. [0 : no use].
uint8_t	number	Configuration number for QE monitor.



<code>cts_instance_t</code> const *	<code>p_ctsu_instance</code>	Pointer to CTSU instance.
<code>uart_instance_t</code> const *	<code>p_uart_instance</code>	Pointer to UART instance.
void const *	<code>p_context</code>	User defined context passed into callback function.
void const *	<code>p_extend</code>	Pointer to extended configuration by instance of interface.

### ◆ touch\_api\_t

struct touch_api_t	
Functions implemented at the HAL layer will follow this API.	
<b>Data Fields</b>	
<code>fsp_err_t</code> (*	<code>open</code> )( <code>touch_ctrl_t</code> *const p_ctrl, <code>touch_cfg_t</code> const *const p_cfg)
<code>fsp_err_t</code> (*	<code>scanStart</code> )( <code>touch_ctrl_t</code> *const p_ctrl)
<code>fsp_err_t</code> (*	<code>dataGet</code> )( <code>touch_ctrl_t</code> *const p_ctrl, <code>uint64_t</code> *p_button_status, <code>uint16_t</code> *p_slider_position, <code>uint16_t</code> *p_wheel_position)
<code>fsp_err_t</code> (*	<code>padDataGet</code> )( <code>touch_ctrl_t</code> *const p_ctrl, <code>uint16_t</code> *p_pad_rx_coordinate, <code>uint16_t</code> *p_pad_tx_coordinate, <code>uint8_t</code> *p_pad_num_touch)
<code>fsp_err_t</code> (*	<code>callbackSet</code> )( <code>touch_ctrl_t</code> *const p_api_ctrl, void(*p_callback)( <code>touch_callback_args_t</code> *), void const *const p_context, <code>touch_callback_args_t</code> *const p_callback_memory)
<code>fsp_err_t</code> (*	<code>close</code> )( <code>touch_ctrl_t</code> *const p_ctrl)
<code>fsp_err_t</code> (*	<code>versionGet</code> )( <code>fsp_version_t</code> *const p_data)
<b>Field Documentation</b>	

◆ **open**

```
fsp_err_t(* touch_api_t::open) (touch_ctrl_t *const p_ctrl, touch_cfg_t const *const p_cfg)
```

Open driver.

**Implemented as**

- RM\_TOUCH\_Open()

**Parameters**

[in]	p_ctrl	Pointer to control structure.
[in]	p_cfg	Pointer to pin configuration structure.

◆ **scanStart**

```
fsp_err_t(* touch_api_t::scanStart) (touch_ctrl_t *const p_ctrl)
```

Scan start.

**Implemented as**

- RM\_TOUCH\_ScanStart()

**Parameters**

[in]	p_ctrl	Pointer to control structure.
------	--------	-------------------------------

◆ **dataGet**

```
fsp_err_t(* touch_api_t::dataGet) (touch_ctrl_t *const p_ctrl, uint64_t *p_button_status, uint16_t *p_slider_position, uint16_t *p_wheel_position)
```

Data get.

**Implemented as**

- RM\_TOUCH\_DataGet()

**Parameters**

[in]	p_ctrl	Pointer to control structure.
[out]	p_button_status	Pointer to get data bitmap.
[out]	p_slider_position	Pointer to get data array.
[out]	p_wheel_position	Pointer to get data array.

### ◆ padDataGet

```
fsp_err_t(* touch_api_t::padDataGet) (touch_ctrl_t*const p_ctrl, uint16_t *p_pad_rx_coordinate,
uint16_t *p_pad_tx_coordinate, uint8_t *p_pad_num_touch)
```

pad data get.

#### Implemented as

- RM\_TOUCH\_PadDataGet()

#### Parameters

[in]	p_ctrl	Pointer to control structure.
[out]	p_pad_rx_coordinate	Pointer to get coordinate of receiver side.
[out]	p_pad_tx_coordinate	Pointer to get coordinate of transmitter side.
[out]	p_pad_num_touch	Pointer to get touch count.

### ◆ callbackSet

```
fsp_err_t(* touch_api_t::callbackSet) (touch_ctrl_t*const p_api_ctrl,
void(*p_callback)(touch_callback_args_t *), void const *const p_context, touch_callback_args_t
*const p_callback_memory)
```

Specify callback function and optional context pointer and working memory pointer.

#### Implemented as

- RM\_TOUCH\_CallbackSet()

#### Parameters

[in]	p_ctrl	Pointer to the CTSU control block.
[in]	p_callback	Callback function
[in]	p_context	Pointer to send to callback function
[in]	p_working_memory	Pointer to volatile memory where callback structure can be allocated. Callback arguments allocated here are only valid during the callback.

◆ **close**

```
fsp_err_t(* touch_api_t::close) (touch_ctrl_t *const p_ctrl)
```

Close driver.

**Implemented as**

- RM\_TOUCH\_Close()

**Parameters**

[in]	p_ctrl	Pointer to control structure.
------	--------	-------------------------------

◆ **versionGet**

```
fsp_err_t(* touch_api_t::versionGet) (fsp_version_t *const p_data)
```

Return the version of the driver.

**Implemented as**

- RM\_TOUCH\_VersionGet()

**Parameters**

[in]	p_ctrl	Pointer to control structure.
[out]	p_data	Memory address to return version information to.

◆ **touch\_instance\_t**

```
struct touch_instance_t
```

This structure encompasses everything that is needed to use an instance of this interface.

## Data Fields

touch_ctrl_t *	p_ctrl	Pointer to the control structure for this instance.
touch_cfg_t const *	p_cfg	Pointer to the configuration structure for this instance.
touch_api_t const *	p_api	Pointer to the API structure for this instance.

**Typedef Documentation**

◆ **touch\_ctrl\_t**

```
typedef void touch_ctrl_t
```

Control block. Allocate an instance specific control block to pass into the API calls.

**Implemented as**

- [touch\\_instance\\_ctrl\\_t](#)

◆ **touch\_callback\_args\_t**

```
typedef struct st_ctsu_callback_args touch_callback_args_t
```

Callback function parameter data

## 4.3.54 Virtual EEPROM Interface

### Interfaces

#### Detailed Description

Interface for Virtual EEPROM access.

## Summary

The Virtual EEPROM Port configures a fail-safe key value store designed for microcontrollers on top of a lower level storage device.

Implemented by: [Virtual EEPROM \(rm\\_vee\\_flash\)](#)

#### Data Structures

```
struct rm_vee_callback_args_t
```

```
struct rm_vee_cfg_t
```

```
struct rm_vee_api_t
```

```
struct rm_vee_instance_t
```

#### Typedefs

```
typedef void rm_vee_ctrl_t
```

#### Enumerations

```
enum rm_vee_state_t
```

## Data Structure Documentation

### ◆ `rm_vee_callback_args_t`

struct <code>rm_vee_callback_args_t</code>		
User configuration structure, used in <code>open</code> function		
Data Fields		
<code>rm_vee_state_t</code>	<code>state</code>	State of the Virtual EEPROM.
<code>void const *</code>	<code>p_context</code>	Placeholder for user data. Set in <code>rm_vee_api_t::open</code> function in <code>::rm_vee_cfg_t</code> .

### ◆ `rm_vee_cfg_t`

struct <code>rm_vee_cfg_t</code>		
User configuration structure, used in <code>open</code> function		
<b>Data Fields</b>		
<code>uint32_t</code>	<code>num_segments</code>	
		Number of segments to divide the volume into.
<code>uint32_t</code>	<code>total_size</code>	
		Total size of the volume.
<code>uint32_t</code>	<code>ref_data_size</code>	
		Size of the reference data stored at the end of the segment.
<code>uint32_t</code>	<code>record_max_id</code>	
		Maximum record ID that can be used.
<code>uint16_t *</code>	<code>rec_offset</code>	
		Pointer to buffer used for record offset caching.
<code>void(*</code>	<code>p_callback</code> <code>(rm_vee_callback_args_t *p_args)</code>	
		Callback provided when a Virtual EEPROM event occurs.

void const *	<a href="#">p_context</a>
	Placeholder for user data.
void const *	<a href="#">p_extend</a>
	Pointer to hardware dependent configuration.

### ◆ [rm\\_vee\\_api\\_t](#)

struct <a href="#">rm_vee_api_t</a>	
Virtual EEPROM interface API.	
<b>Data Fields</b>	
<a href="#">fsp_err_t</a> (*	<a href="#">open</a> )( <a href="#">rm_vee_ctrl_t</a> *const p_ctrl, <a href="#">rm_vee_cfg_t</a> const *const p_cfg)
<a href="#">fsp_err_t</a> (*	<a href="#">recordWrite</a> )( <a href="#">rm_vee_ctrl_t</a> *const p_ctrl, uint32_t const rec_id, uint8_t const *const p_rec_data, uint32_t num_bytes)
<a href="#">fsp_err_t</a> (*	<a href="#">recordPtrGet</a> )( <a href="#">rm_vee_ctrl_t</a> *const p_ctrl, uint32_t rec_id, uint8_t **const pp_rec_data, uint32_t *const p_num_bytes)
<a href="#">fsp_err_t</a> (*	<a href="#">refDataWrite</a> )( <a href="#">rm_vee_ctrl_t</a> *const p_ctrl, uint8_t const *const p_ref_data)
<a href="#">fsp_err_t</a> (*	<a href="#">refDataPtrGet</a> )( <a href="#">rm_vee_ctrl_t</a> *const p_ctrl, uint8_t **const pp_ref_data)
<a href="#">fsp_err_t</a> (*	<a href="#">statusGet</a> )( <a href="#">rm_vee_ctrl_t</a> *const p_ctrl, <a href="#">rm_vee_status_t</a> *const p_status)
<a href="#">fsp_err_t</a> (*	<a href="#">refresh</a> )( <a href="#">rm_vee_ctrl_t</a> *const p_ctrl)
<a href="#">fsp_err_t</a> (*	<a href="#">format</a> )( <a href="#">rm_vee_ctrl_t</a> *const p_ctrl, uint8_t const *const p_ref_data)
<a href="#">fsp_err_t</a> (*	<a href="#">callbackSet</a> )( <a href="#">rm_vee_ctrl_t</a> *const p_api_ctrl, void(*p_callback)( <a href="#">rm_vee_callback_args_t</a> *), void const *const p_context, <a href="#">rm_vee_callback_args_t</a> *const p_callback_memory)

<code>fsp_err_t(*</code>	<code>close )(rm_vee_ctrl_t *const p_ctrl)</code>
--------------------------	---------------------------------------------------

<code>fsp_err_t(*</code>	<code>versionGet )(fsp_version_t *const p_version)</code>
--------------------------	-----------------------------------------------------------

## Field Documentation

### ◆ open

`fsp_err_t(* rm_vee_api_t::open) (rm_vee_ctrl_t *const p_ctrl, rm_vee_cfg_t const *const p_cfg)`

Initializes the driver's internal structures and opens the Flash driver.

#### Implemented as

- [RM\\_VEE\\_FLASH\\_Open](#)

#### Parameters

[in]	p_ctrl	Pointer to control block. Must be declared by user. Elements set here.
[in]	p_cfg	Pointer to configuration structure. All elements of this structure must be set by user.

### ◆ recordWrite

`fsp_err_t(* rm_vee_api_t::recordWrite) (rm_vee_ctrl_t *const p_ctrl, uint32_t const rec_id, uint8_t const *const p_rec_data, uint32_t num_bytes)`

Writes a record to data flash.

#### Implemented as

- [RM\\_VEE\\_FLASH\\_RecordWrite](#)

#### Parameters

[in]	p_ctrl	Pointer to control block.
[in]	rec_id	ID of record to write.
[in]	p_rec_data	Pointer to record data to write.
[in]	num_bytes	Length of data to write.



## ◆ recordPtrGet

```
fsp_err_t(* rm_vee_api_t::recordPtrGet) (rm_vee_ctrl_t *const p_ctrl, uint32_t rec_id, uint8_t **const pp_rec_data, uint32_t *const p_num_bytes)
```

This function gets the pointer to the most recent version of a record specified by ID.

**Implemented as**

- [RM\\_VEE\\_FLASH\\_RecordPtrGet](#)

**Parameters**

[in]	p_ctrl	Pointer to control block.
[in]	rec_id	ID of record to locate.
[in]	pp_rec_data	Pointer to set to the most recent version of the record.
[in]	p_num_bytes	Variable to load with record length.

## ◆ refDataWrite

```
fsp_err_t(* rm_vee_api_t::refDataWrite) (rm_vee_ctrl_t *const p_ctrl, uint8_t const *const p_ref_data)
```

Writes new Reference data to the reference update area.

**Implemented as**

- [RM\\_VEE\\_FLASH\\_RefDataWrite](#)

**Parameters**

[in]	p_ctrl	Pointer to control block.
[in]	p_ref_data	Pointer to data to write to the reference data update area.

## ◆ refDataPtrGet

```
fsp_err_t(* rm_vee_api_t::refDataPtrGet) (rm_vee_ctrl_t *const p_ctrl, uint8_t **const pp_ref_data)
```

Gets a pointer to the most recent reference data.

**Implemented as**

- [RM\\_VEE\\_FLASH\\_RefDataPtrGet](#)

**Parameters**

[in]	p_ctrl	Pointer to control block.
[in]	pp_ref_data	Pointer to set to the most recent valid reference data.

◆ **statusGet**

```
fsp_err_t(* rm_vee_api_t::statusGet) (rm_vee_ctrl_t *const p_ctrl, rm_vee_status_t *const p_status)
```

Get the current status of the VEE driver.

**Implemented as**

- [RM\\_VEE\\_FLASH\\_StatusGet](#)

**Parameters**

[in]	p_ctrl	Pointer to control block.
[in]	p_status	Pointer to store the current status of the VEE driver.

◆ **refresh**

```
fsp_err_t(* rm_vee_api_t::refresh) (rm_vee_ctrl_t *const p_ctrl)
```

Manually start a refresh operation.

**Implemented as**

- [RM\\_VEE\\_FLASH\\_Refresh](#)

**Parameters**

[in]	p_ctrl	Pointer to control block.
------	--------	---------------------------

◆ **format**

```
fsp_err_t(* rm_vee_api_t::format) (rm_vee_ctrl_t *const p_ctrl, uint8_t const *const p_ref_data)
```

Format the Virtual EEPROM.

**Implemented as**

- [RM\\_VEE\\_FLASH\\_Format](#)

**Parameters**

[in]	p_ctrl	Pointer to control block.
[in]	p_ref_data	Optional pointer to reference data to write during format.

◆ **callbackSet**

```
fsp_err_t(* rm_vee_api_t::callbackSet) (rm_vee_ctrl_t *const p_api_ctrl,
void(*p_callback)(rm_vee_callback_args_t*), void const *const p_context, rm_vee_callback_args_t
*const p_callback_memory)
```

Specify callback function and optional context pointer and working memory pointer.

**Implemented as**

- RM\_VEE\_FLASH\_CallbackSet()

**Parameters**

[in]	p_ctrl	Control block set in <a href="#">rm_vee_api_t::open</a> call.
[in]	p_callback	Callback function to register
[in]	p_context	Pointer to send to callback function
[in]	p_working_memory	Pointer to volatile memory where callback structure can be allocated. Callback arguments allocated here are only valid during the callback.

◆ **close**

```
fsp_err_t(* rm_vee_api_t::close) (rm_vee_ctrl_t *const p_ctrl)
```

Closes the module and lower level storage device.

**Implemented as**

- RM\_VEE\_FLASH\_Close

**Parameters**

[in]	p_ctrl	Control block set in <a href="#">rm_vee_api_t::open</a> call.
------	--------	---------------------------------------------------------------

◆ **versionGet**

```
fsp_err_t(* rm_vee_api_t::versionGet) (fsp_version_t *const p_version)
```

Gets version and stores it in provided pointer p\_version.

**Implemented as**

- RM\_VEE\_FLASH\_VersionGet

**Parameters**

[out]	p_version	Code and API version used.
-------	-----------	----------------------------

◆ **rm\_vee\_instance\_t**

struct rm_vee_instance_t		
This structure encompasses everything that is needed to use an instance of this interface.		
Data Fields		
rm_vee_ctrl_t *	p_ctrl	Pointer to the control structure for this instance.
rm_vee_cfg_t const *	p_cfg	Pointer to the configuration structure for this instance.
rm_vee_api_t const *	p_api	Pointer to the API structure for this instance.

**Typedef Documentation**◆ **rm\_vee\_ctrl\_t**

typedef void rm_vee_ctrl_t
Virtual EEPROM API control block. Allocate an instance specific control block to pass into the VEE API calls.
<b>Implemented as</b>
◦ <a href="#">rm_vee_flash_instance_ctrl_t</a>

**Enumeration Type Documentation**◆ **rm\_vee\_state\_t**

enum rm_vee_state_t	
Enumerator	
RM_VEE_STATE_READY	Ready.
RM_VEE_STATE_BUSY	Operation in progress.
RM_VEE_STATE_REFRESH	Refresh operation in progress.
RM_VEE_STATE_OVERFLOW	The amount of data written exceeds the space available.
RM_VEE_STATE_HARDWARE_FAIL	Lower level hardware failure.

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