User's Manual

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RL78/H1D

User's Manual: Hardware

16-Bit Single-Chip Microcontrollers

Renesas Electronics
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General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products
   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

How to Use This Manual

Readers

This manual is intended for user engineers who wish to understand the functions of the RL78/H1D and design and develop application systems and programs for these devices.
The target products are as follows.

- 48-pin: R5F11NGx (x = F, G)
- 64-pin: R5F11NLx (x = F, G)
  R5F11PLx (x = F, G)
- 80-pin: R5F11NMx (x = E, F, G)
  R5F11RMG

Purpose

This manual is intended to give users an understanding of the functions described in the **Organization** below.

Organization

The RL78/H1D manual is separated into two parts: this manual and the software edition (common to the RL78 family).

RL78/H1D User's Manual Hardware (This Manual)	**RL78 Family User's Manual Software**
• Pin functions • Internal block functions • Interrupts • Other on-chip peripheral functions • Electrical specifications	• CPU functions • Instruction set • Explanation of each instruction

How to Read This Manual

It is assumed that the readers of this manual have general knowledge of electrical engineering, logic circuits, and microcontrollers.

- To gain a general understanding of functions:
  → Read this manual in the order of the **CONTENTS**. The mark "<R>" shows major revised points. The revised points can be easily searched by copying an "<R>" in the PDF file and specifying it in the "Find what:" field.
- How to interpret the register format:
  → For a bit number enclosed in angle brackets, the bit name is defined as a reserved word in the assembler, and is defined as an sfr variable using the #pragma sfr directive in the compiler.
- To know details of the RL78/H1D Microcontroller instructions:
  → Refer to the separate document **RL78 Family User's Manual Software (R01US0015E)**.

Conventions	Data significance:	Higher digits on the left and lower digits on the right
	Active low representations:	$\overline{\times\times\times}$ (overscore over pin and signal name)
	Note:	Footnote for item marked with Note in the text
	Caution:	Information requiring particular attention
	Remark:	Supplementary information
	Numerical representations:	Binary.....×××× or ××××B
		Decimal.....××××
		Hexadecimal.....××××H

Related Documents The related documents indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such.

Documents Related to Devices

Document Name	Document No.
RL78/H1D User's Manual Hardware	This manual
RL78 Family User's Manual Software	R01US0015E

Documents Related to Flash Memory Programming (User's Manual)

Document Name	Document No.
PG-FP6 Flash Memory Programmer User's Manual	R20UT4025E
E1, E20 Emulator User's Manual	R20UT0398E
E2 Emulator User's Manual	R20UT3538E
E2 Lite Emulator User's Manual	R20UT3240E
Renesas Flash Programmer Flash Memory Programming Software User's Manual	R20UT4066E
Renesas Flash Development Toolkit User's Manual	R20UT0508E

Caution The related documents listed above are subject to change without notice. Be sure to use the latest version of each document when designing.

Other Documents

Document Name	Document No.
Renesas Microcontrollers RL78 Family	R01CP0003E
Semiconductor Package Mount Manual	R50ZZ0003E
Semiconductor Reliability Handbook	R51ZZ0001E

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Caution: This product uses SuperFlash® technology licensed from Silicon Storage Technology, Inc.

CONTENTS

CHAPTER 1 OUTLINE

1.1 Features

○ Ultra-low power consumption technology
- V_{DD} = 2.4 to 5.5 V
  (10-bit SAR A/D converter: 2.4 to 5.5 V, operating voltage of the analog front-end (AFE): 2.7 to 5.5 V) Note 1,
  V_{DD} = 1.8 to 5.5 V Note 2
- HALT mode
- STOP mode
- SNOOZE mode

○ RL78 CPU core
- CISC architecture with 3-stage pipeline
- Minimum instruction execution time: Can be changed from high speed (0.04167 µs: @ 24 MHz operation with high-speed on-chip oscillator clock) to ultra-low speed (30.5 µs: @ 32.768 kHz operation with subsystem clock)
- Multiply/divide and multiply/accumulate instructions are supported.
- Address space: 1 MB
- General-purpose registers: (8-bit register × 8) × 4 banks
- On-chip RAM: 5.5 KB Note 1, 8 KB Note 2

○ Code flash memory
- Code flash memory: 64 to 128 KB
- Block size: 1 KB
- Prohibition of block erase and rewriting (security function)
- On-chip debug function
- Self-programming (with boot swap function/flash shield window function)

○ Data flash memory
- Data flash memory: 4 KB
- Background operation (BGO): Instructions can be executed from the program memory while rewriting the data flash memory.
- Number of rewrites: 1,000,000 times (TYP.)
- Voltage of rewrites: V_{DD} = 2.4 to 5.5 V Note 1, 1.8 to 5.5 V Note 2

○ High-speed on-chip oscillator
- Select from 24 MHz, 16 MHz, 12 MHz, 8 MHz, 6 MHz, 4 MHz, 3 MHz, 2 MHz, and 1 MHz
- High accuracy: ±1.0% (V_{DD} = 2.4 to 5.5 V, T_A = -20 to +85°C[Note 1], V_{DD} = 1.8 to 5.5 V, T_A = -20 to +85°C[Note 2])

○ Operating ambient temperature
- T_A = -40 to +85°C (A: Consumer applications[Note 1], D: Industrial applications[Note 2])

○ Power management and reset function
- On-chip power-on-reset (POR) circuit
- On-chip voltage detector (LVD) (Select interrupt and reset from 9[Note 1] or 12[Note 2] levels)

○ Data transfer controller (DTC)
- Transfer modes: Normal transfer mode, repeat transfer mode, block transfer mode
- Activation sources: Activated by interrupt sources (35 sources).
- Chain transfer function

○ Event link controller (ELC)
- Event signals of 18 to 26 types can be linked to the specified peripheral function.

○ Serial interfaces
- Simplified SPI (CSI [Note 3])/Simplified SPI (CSI): (SPI supported): 3 channels
- UART/UART (LIN-bus supported): 3 channels
- I^2C/simplified I^2C: 4 channels
- Serial interface UARTMG (9600 bps @ 38.4 kHz): 1 channel (R5F11R only)

○ Timers
- 16-bit timer: Timer array unit (TAU): 8 channels, Timer RJ: 2 channels (R5F11R only)
- 8-bit timer: 2 channels[Note 1], 6 channels[Note 2]
- 12-bit interval timer: 1 channel
- Real-time clock 2: 1 channel (calendar for 99 years, alarm function, and clock correction function)
- Watchdog timer: 1 channel (operable with the dedicated low-speed on-chip oscillator)
- External signal sampler: 1 channel (R5F11R only)
- Sampling output timer detector (SMOTD): 6 channels for input, 3 channels for output (R5F11R only)

○ LCD controller/driver
- Internal voltage boosting method, capacitor split method, and external resistance division method are switchable.
- Segment signal output: 27 (23) to 36 (32) Note 4
- Common signal output: 4 (8) Note 4

○ Analog front-end power supply circuit (R5F11N and R5F11P only)
- AFE reference power supply (ABGR)
- LDO for supplying power to internal circuits (REGA)
- LDO for supplying power to a sensor (SBIAS): 0.5 to 2.2 V

○ 24-bit ΔΣ A/D converter with programmable gain instrumentation amplifier (R5F11N and R5F11P only)
- 24-bit second-order ΔΣ A/D converter (AV_{DD} = 2.7 to 5.5 V)
  - SNDR: 85 dB (TYP.)
  - Output data rate: 488 sps to 15.625 ksps in normal mode
    61 sps to 1.953 ksps in low power mode
- Programmable gain instrumentation amplifier (PGA0)
  - Analog input: 1 to 5 channels (differential input mode or single-ended input mode)
  - D/A converter for offset adjustment
  - Variable gain: x1 to x64

○ Amplifier unit (R5F11N and R5F11P only)
- Programmable gain instrumentation amplifier (PGA1): 1 channel (R5F11NL, R5F11PL, and R5F11NG only)
  - Analog input: 1 or 2 channels
  - Variable gain: x12, x16, x20, x24
- Rail-to-rail operational amplifier (AMP0): 1 channel
- General-purpose operational amplifier (AMP1, AMP2): 2 channels (R5F11NL, R5F11PL, and R5F11NG only)

○ D/A converter (R5F11N and R5F11P only)
- 8-bit resolution R-2R resistor ladder D/A converter (DAC0) (AV_{DD} = 2.7 to 5.5 V): 1 channel
- 12-bit resolution R-2R resistor ladder D/A converter (DAC1) (AV_{DD} = 2.7 to 5.5 V): 1 channel (R5F11NL, R5F11PL, and R5F11NG only)

○ 10-bit SAR A/D converter
- 10-bit resolution A/D converter (V_{DD} = 2.4 to 5.5 V Note 1, V_{DD} = 1.8 to 5.5 V Note 2)
- Analog input: 3 channels
- Internal reference voltage (TYP. 1.45 V) Note 5 and temperature sensor Note 5

○ I/O ports
- I/O ports: 29 to 63 (N-ch open drain I/O [withstand voltage of 6 V]: 2)
- Can be set to N-ch open drain, TTL input buffer, and on-chip pull-up resistor
- On-chip clock output/buzzer output controller

○ Others

• On-chip BCD (binary-coded decimal) correction circuit

Note 1. In case of R5F11N and R5F11P.

Note 2. In case of R5F11R.

Note 3. Although the CSI function is generally called SPI, it is also called CSI in this product, so it is referred to as such in this manual.

Note 4. The number in parentheses indicates the number of signal outputs when 8 coms are used.

Note 5. Selectable only in HS (high-speed main) mode.

Remark The functions mounted depend on the product. See **1.6 Outline of Functions**.

○ ROM, RAM capacities

Flash ROM	Data Flash	RAM	RL78/H1D			
			80-pin LFQFP	64-pin LFQFP	64-pin TFBGA	48-pin LFQFP
128 KB	4 KB	5.5 KB	R5F11NMG	R5F11NLG	R5F11PLG	R5F11NGG
96 KB	4 KB	5.5 KB	R5F11NMF	R5F11NLF	R5F11PLF	R5F11NGF
64 KB	4 KB	5.5 KB	R5F11NME	—	—	—
128 KB	4 KB	8 KB	R5F11RMG	—	—	—

1.2 Ordering Information

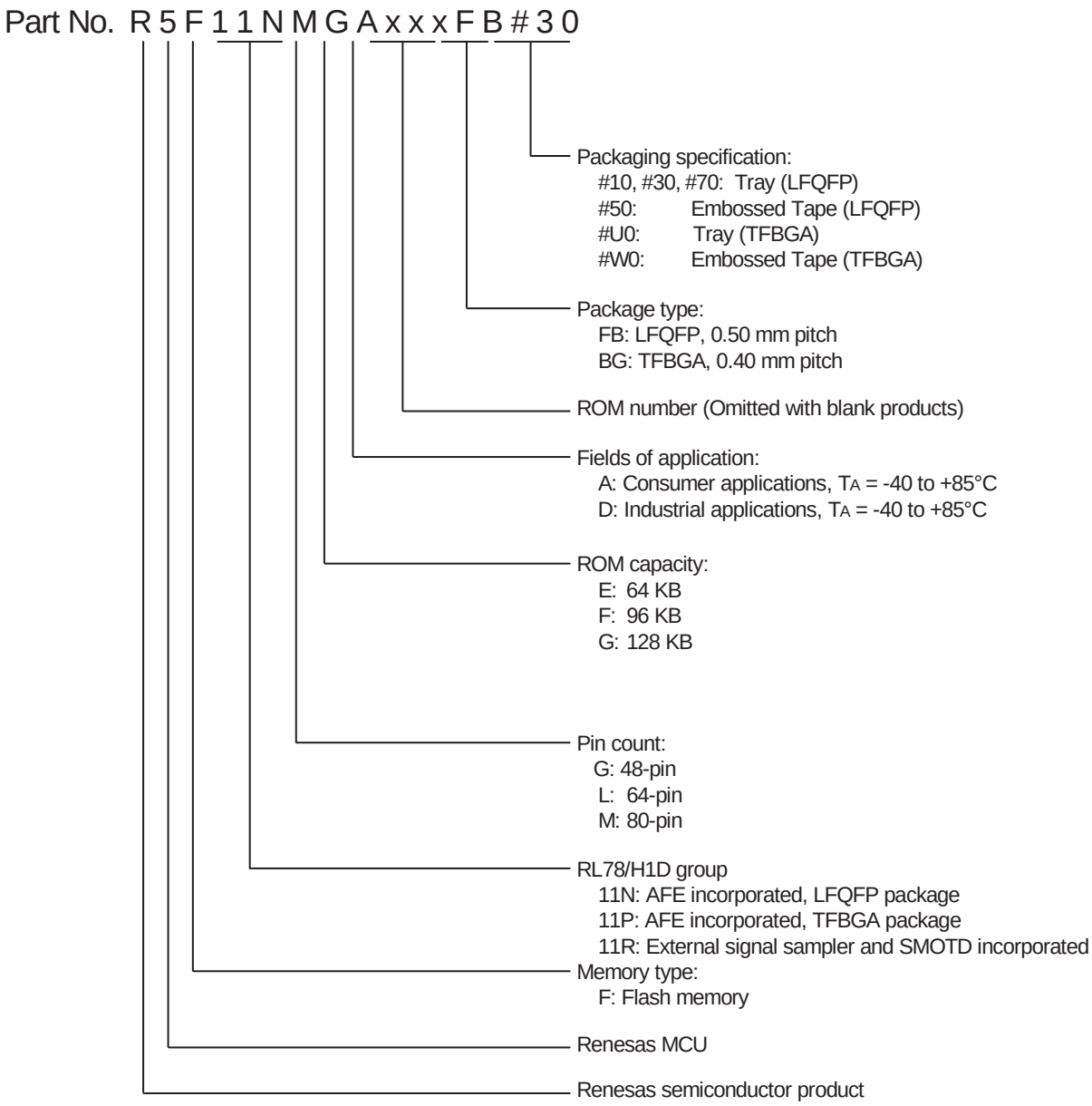
<R>

Pin Count	Package	Fields of Application	Orderable Part Number		RENESAS Code
			Product Name	Packaging Specifications	
80 pins	80-pin plastic LFQFP (12 × 12 mm, 0.5 mm pitch)	A	R5F11NMGAFB, R5F11NMFAFB, R5F11NMEAFB	#10, #30, #50, #70	PLQP0080KB-B
64 pins	64-pin plastic LFQFP (10 × 10 mm, 0.5 mm pitch)	A	R5F11NLGAFB, R5F11NLFAFB	#10, #30, #50, #70	PLQP0064KB-C
64 pins	64-pin plastic TFBGA (4 × 4 mm, 0.4 mm pitch)	A	R5F11PLGABG, R5F11PLFABG	#U0, #W0	PTBG0064LA-A
48 pins	48-pin plastic LFQFP (7 × 7 mm, 0.5 mm pitch)	A	R5F11NGGAFB, R5F11NGFAFB	#10, #30, #50, #70	PLQP0048KB-B
80 pins	80-pin plastic LFQFP (12 × 12 mm, 0.5 mm pitch)	D	R5F11RMGDFB	#10, #30, #50, #70	PLQP0080KB- B

Remark 1. Products (R5F11PL) in 64-pin TFBGA have the same functionality as those (R5F11NG) in 48-pin LFQFP. The only difference is the package.

Remark 2. For the fields of application, refer to Part Number, Memory Size, and Package.

<R> **Figure 1 - 1 Part Number, Memory Size, and Package of RL78/H1D**

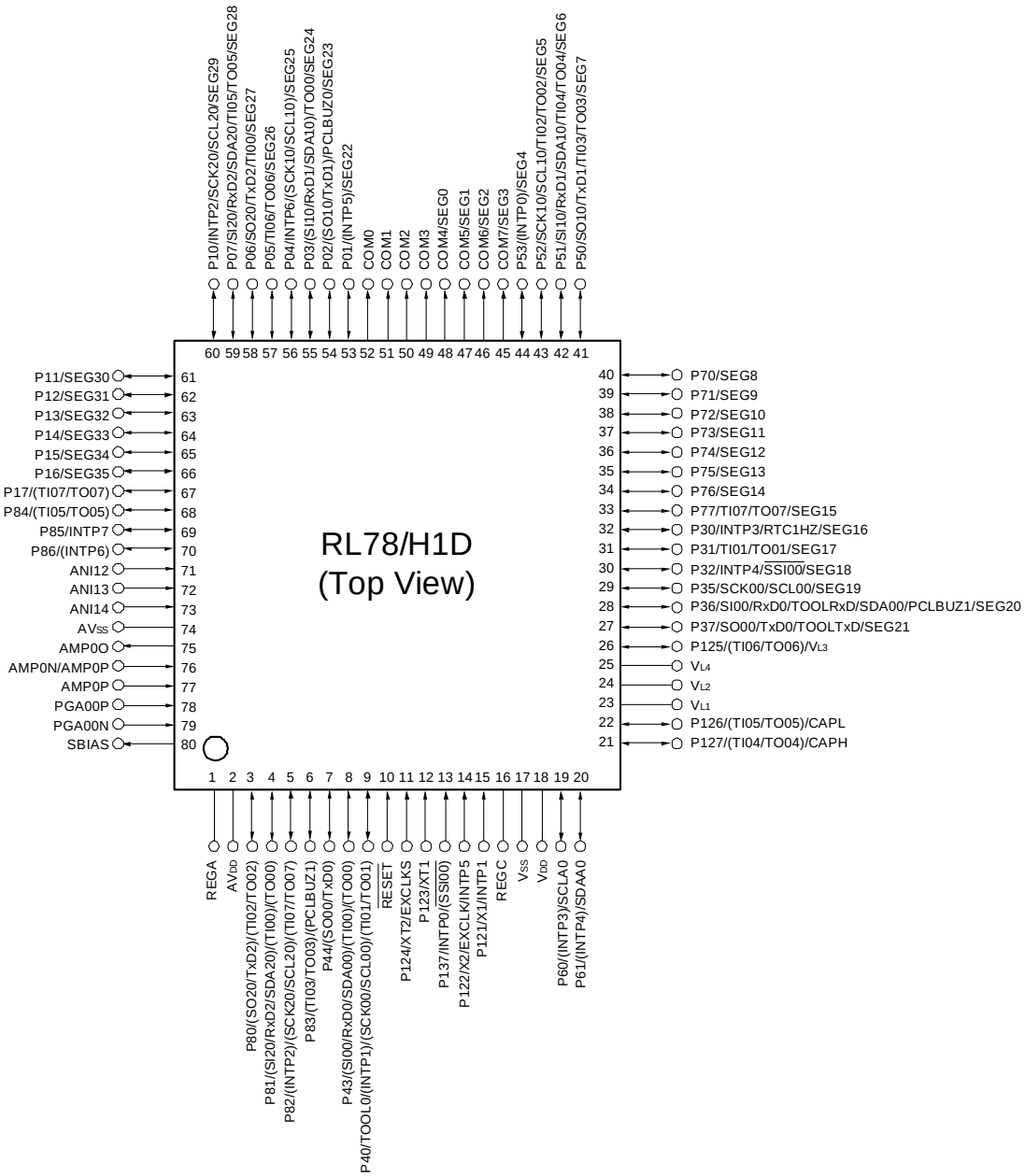


Caution Orderable part numbers are current as of when this manual was published.
Please make sure to refer to the relevant product page on the Renesas website for the latest part numbers.

1.3 Pin Configuration (Top View)

1.3.1 80-pin products (R5F11NM)

• 80-pin plastic LFQFP (12 × 12 mm, 0.5 mm pitch)

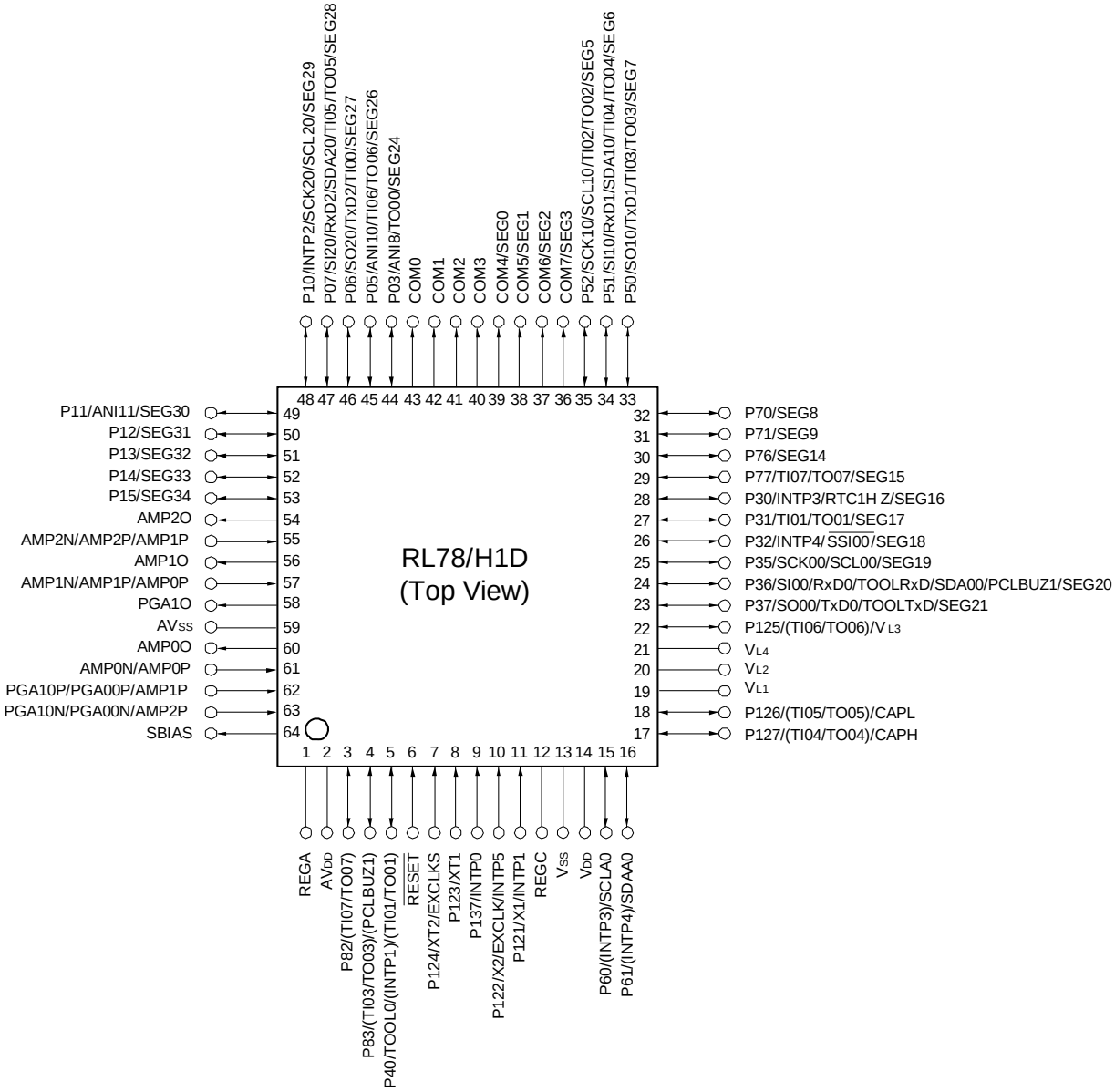


Caution 1. Connect the REGC pin to VSS pin via a capacitor (0.47 to 1 μF).
Caution 2. Connect the REGA pin to AVSS pin via a capacitor (0.22 μF).
Caution 3. Make the AVSS pin the same potential as the VSS pin.
Caution 4. Make the AVDD pin the same potential as the VDD pin.
Caution 5. Connect the SBIAS pin to AVSS pin via a capacitor (0.22 μF).

Remark 1. For pin identification, see **1.4 Pin Identification**.
Remark 2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection registers 0 to 3 (PIOR0 to PIOR3).
Remark 3. Set the AMP0P and AMP0N functions in the above figure by the amplifier unit 1 input select register (AMP0S).

1.3.2 64-pin products (R5F11NL)

• 64-pin plastic LFQFP (10 × 10 mm, 0.5 mm pitch)

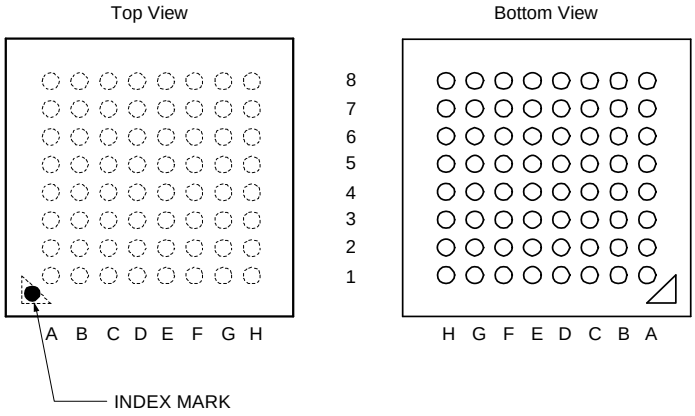


Caution 1. Connect the REGC pin to VSS pin via a capacitor (0.47 to 1 μF).
Caution 2. Connect the REGA pin to AVSS pin via a capacitor (0.22 μF).
Caution 3. Make the AVSS pin the same potential as the VSS pin.
Caution 4. Make the AVDD pin the same potential as the VDD pin.
Caution 5. Connect the SBIAS pin to AVSS pin via a capacitor (0.22 μF).

Remark 1. For pin identification, see **1.4 Pin Identification**.
Remark 2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection registers 0 to 3 (PIOR0 to PIOR3).
Remark 3. Set the AMP0P and AMP0N functions in the above figure by the amplifier unit 1 input select register (AMP0S).
Set the AMP1P and AMP1N functions in the above figure by the amplifier unit 2 input select register (AMP1S).
Set the AMP2P and AMP2N functions in the above figure by the amplifier unit 3 input select register (AMP2S).

1.3.3 64-pin products (R5F11PL)

• 64-pin plastic TFBGA (4 × 4 mm, 0.4 mm pitch)



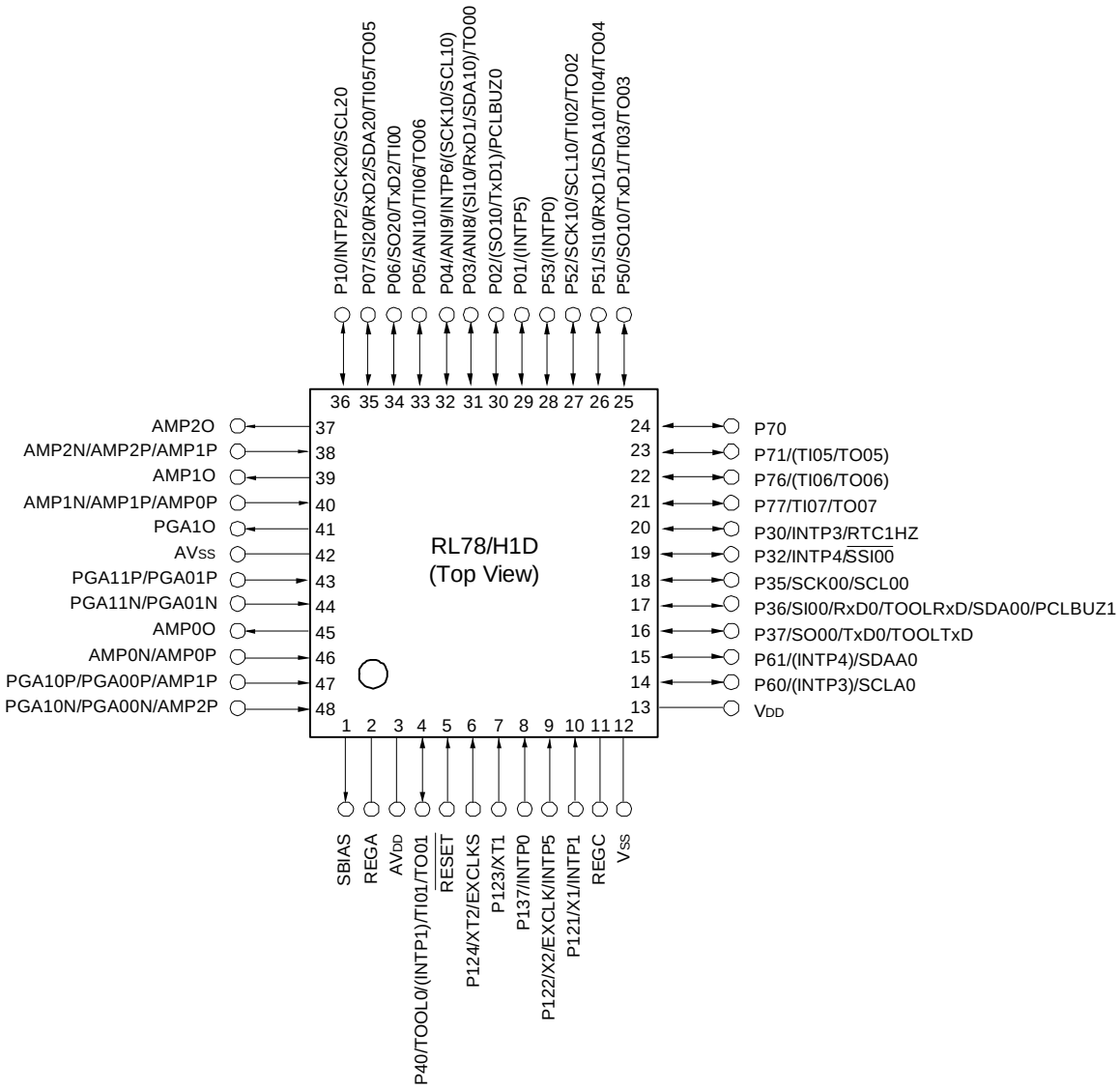
	A	B	C	D	E	F	G	H	
8	Vss	P71/(TI05/TO05)	P77/TI07/TO07	P35/SCK00/SCL00	P36/SI00/RxD0/TOOLRxD/SDA00/PCLBUZ1	P61/(INTP4)/SDAA0	VDD	Vss	8
7	P50/SO10/TxD1/TI03/TO03	P51/SI10/RxD1/SDA10/TI04/TO04	P76/(TI06/TO06)	P32/INTP4/$\overline{\text{SSI00}}$	P37/SO00/TxD0/TOOLTxD	P60/(INTP3)/SCLA0	Vss	P121/X1/INTP1	7
6	P53/(INTP0)	P52/SCK10/SCL10/TI02/TO02	P70	P30/INTP3/RTC1HZ	Vss	$\overline{\text{RESET}}$	REGC	P122/X2/EXCLK/INTP5	6
5	P02/(SO10/TxD1)/PCLBUZ0	P03/ANI8/(SI10/RxD1/SDA10)/TO00	P04/ANI9/INTP6/(SCK10/SCL10)	P01/(INTP5)	Vss	P40/TOOL0/(INTP1)/TI01/TO01	P137/INTP0	P123/XT1	5
4	P05/ANI10/TI06/TO06	P07/SI20/RxD2/SDA20/TI05/TO05	P06/SO20/TxD2/TI00	P10/INTP2/SCK20/SCL20	Vss	Vss	Vss	P124/XT2/EXCLKS	4
3	AMP1O	AVss	AVss	AVss	AVss	AVss	REGA	AVDD	3
2	AMP2O	AMP1N/AMP1P/AMP0P	PGA11P/PGA01P	PGA11N/PGA01N	AMP0N/AMP0P	AVss	AVss	SBIAS	2
1	AVss	AMP2N/AMP2P/AMP1P	PGA1O	AVss	AMP0O	PGA10P/PGA00P/AMP1P	PGA10N/PGA00N/AMP2P	SBIAS	1
	A	B	C	D	E	F	G	H	

Caution 1. Connect the REGC pin to Vss pin via a capacitor (0.47 to 1 μF).
Caution 2. Connect the REGA pin to AVss pin via a capacitor (0.22 μF).
Caution 3. Make the AVss pin the same potential as the Vss pin.
Caution 4. Make the AVDD pin the same potential as the VDD pin.
Caution 5. Connect an SBIAS pin (either of two) to the AVss pin via a capacitor (0.22 μF).

Remark 1. For pin identification, see **1.4 Pin Identification**.
Remark 2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection registers 0, 1, and 3 (PIOR0, PIOR1, and PIOR3).
Remark 3. Set the AMP0P and AMP0N functions in the above figure by the amplifier unit 1 input select register (AMP0S).
Set the AMP1P and AMP1N functions in the above figure by the amplifier unit 2 input select register (AMP1S).
Set the AMP2P and AMP2N functions in the above figure by the amplifier unit 3 input select register (AMP2S).

1.3.4 48-pin products (R5F11NG)

• 48-pin plastic LFQFP (7 × 7 mm, 0.5 mm pitch)

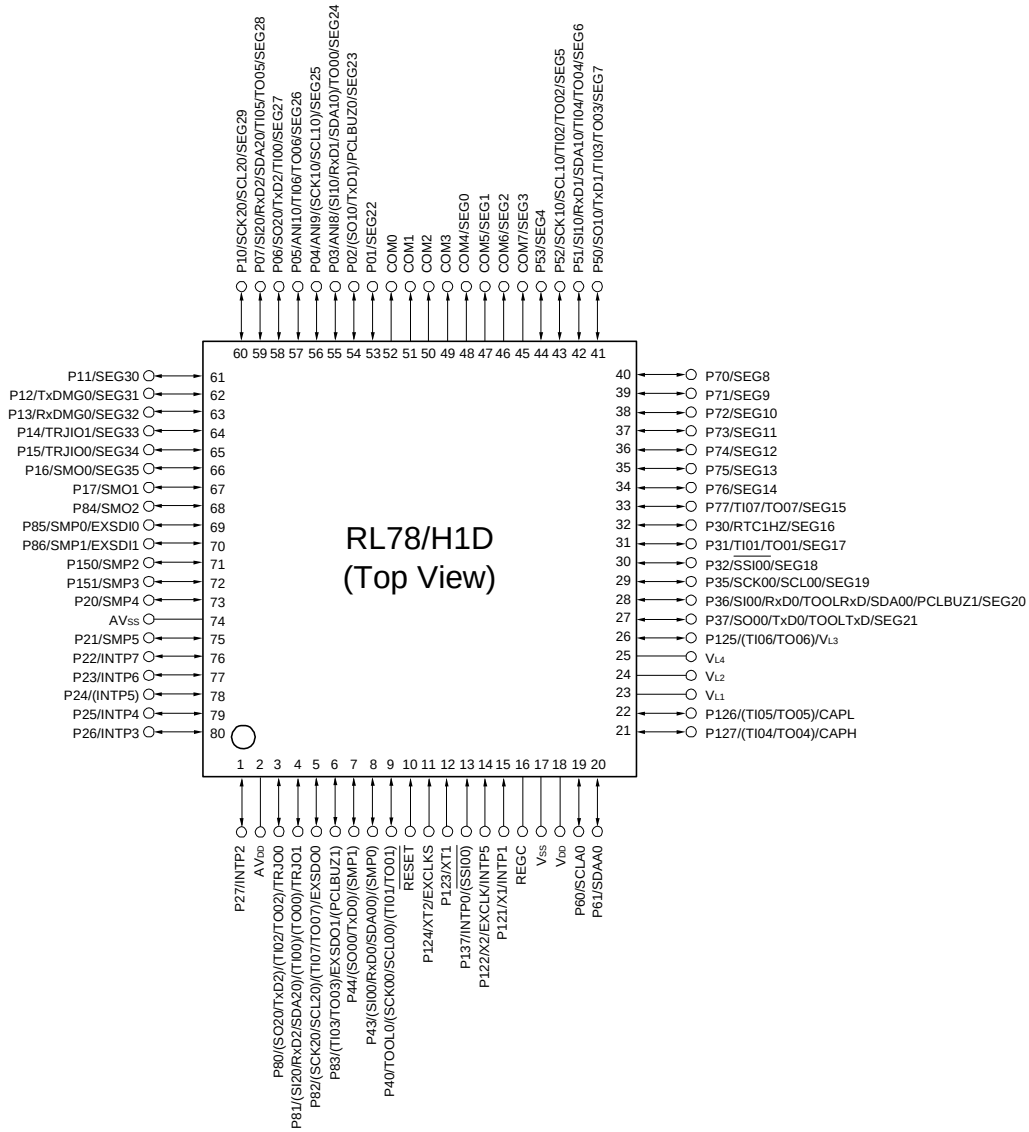


Caution 1. Connect the REGC pin to Vss pin via a capacitor (0.47 to 1 µF).
Caution 2. Connect the REGA pin to AVss pin via a capacitor (0.22 µF).
Caution 3. Make the AVss pin the same potential as the Vss pin.
Caution 4. Make the AVDD pin the same potential as the VDD pin.
Caution 5. Connect the SBIAS pin to AVss pin via a capacitor (0.22 µF).

Remark 1. For pin identification, see **1.4 Pin Identification**.
Remark 2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection registers 0, 1, and 3 (PIOR0, PIOR1, and PIOR3).
Remark 3. Set the AMP0P and AMP0N functions in the above figure by the amplifier unit 1 input select register (AMP0S).
Set the AMP1P and AMP1N functions in the above figure by the amplifier unit 2 input select register (AMP1S).
Set the AMP2P and AMP2N functions in the above figure by the amplifier unit 3 input select register (AMP2S).

1.3.5 80-pin products (R5F11RM)

• 80-pin plastic LFQFP (12 × 12 mm, 0.5 mm pitch)



Caution 1. Connect the REGC pin to Vss pin via a capacitor (0.47 to 1 μF).

Caution 2. Make the AVSS pin the same potential as the VSS pin.

Caution 3. Make the AVDD pin the same potential as the VDD pin.

Remark 1. For pin identification, see **1.4 Pin Identification**.

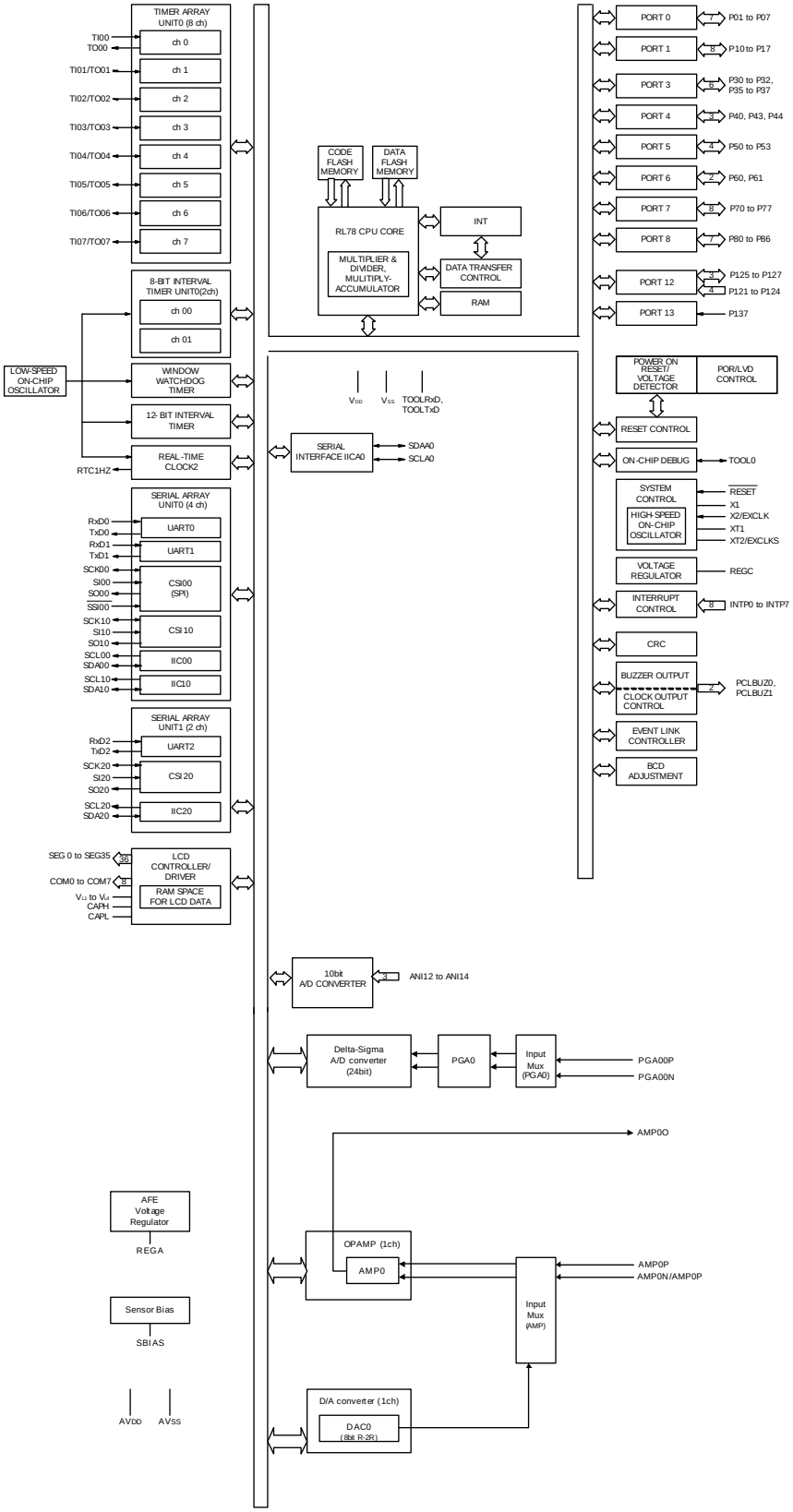
Remark 2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection registers 0 to 3 (PIOR0 to PIOR3).

1.4 Pin Identification

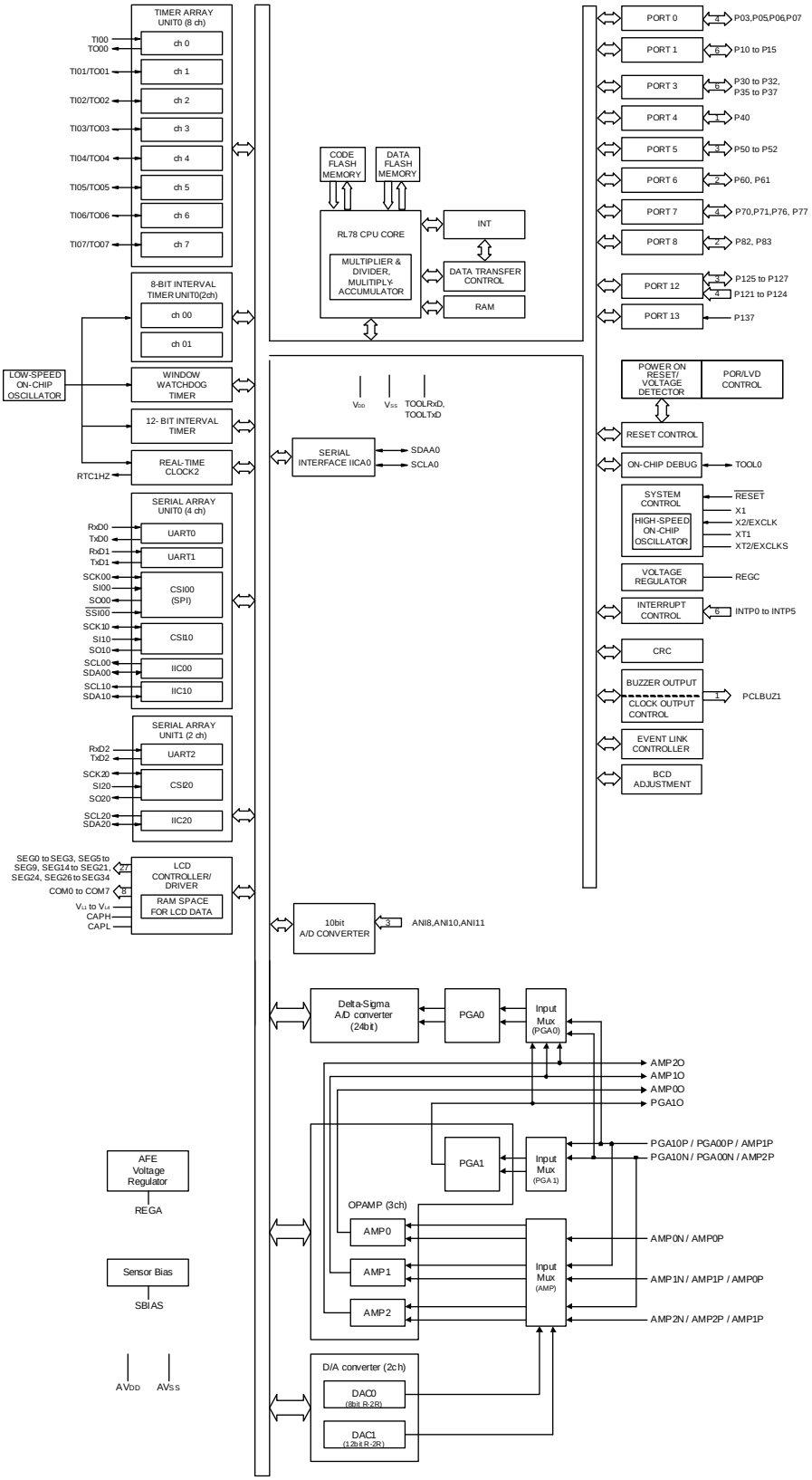
AMP0N to AMP2N :OP AMP Negative Input
AMP0P to AMP2P :OP AMP Positive Input
AMP0O to AMP2O :OP AMP Output
ANI8 to ANI14 :Analog Input
AV_{DD} :Analog Power Supply
AV_{SS} :Analog Ground
CAPH, CAPL :Capacitor for LCD
COM0 to COM7 :LCD Common Output
EXCLK :External Clock Input (Main System Clock)
EXCLKS :External Clock Input (Sub System Clock)
EXSDI0, EXSDI1 :External Sampling Input
EXSDO0, EXSDO1 :External Sampling Clock Output
INTP0 to INTP7 :External Interrupt Input
P01 to P07 :Port 0
P10 to P17 :Port 1
P20 to P27 :Port 2
P30 to P32, P35 to P37 :Port 3
P40, P43, P44 :Port 4
P50 to P53 :Port 5
P60 to P61 :Port 6
P70 to P77 :Port 7
P80 to P86 :Port 8
P121 to P127 :Port 12
P137 :Port 13
P150, P151 :Port 15
PCLBUZ0, PCLBUZ1 :Programmable Clock Output/ Buzzer Output
PGA00N, PGA01N PGA10N, PGA11N :PGA Negative Input
PGA00P, PGA01P PGA10P, PGA11P :PGA Positive Input
PGA1O :PGA Output
REGA :Regulator Capacitance for Analog
REGC :Regulator Capacitance
SBIAS :Reference Voltage Output
$\overline{RESET}$:Reset
RTC1HZ :Real-time Clock Correction
RxD0 to RxD2, RxDMG0 :Receive Data
SCK00, SCK10, SCK20, :Serial Clock Input/Output
SCLA0 :Serial Clock Input/Output
SCL00, SCL10, SCL20 :Serial Clock Output
SDAA0, SDA00, SDA10, SDA20 :Serial Data Input/Output
SEG0 to SEG35 :LCD Segment Output
SI00, SI10, SI20 :Serial Data Input
SO00, SO10, SO20 :Serial Data Output
SSI00 :Slave Select Input
SMP0 to SMP5 :Sampling Input
SMO0 to SMO2 :Sampling Clock Output
TI00 to TI07 :Timer Input
TO00 to TO07,TRJO0, TRJO1 :Timer Output
TOOL0 :Data Input/Output for Tool
TOOLRxD, TOOLTxD :Data Input/Output for External Device
TRJIO0, TRJIO1 :Timer Input/Output
TxD0 to TxD2, TxDMG0 :Transmit Data
V_{DD} :Power Supply
V_{L1} to V_{L4} :LCD Power Supply
V_{SS} :Ground
X1, X2 :Crystal Oscillator (Main System Clock)
XT1, XT2 :Crystal Oscillator (Subsystem Clock)

1.5 Block Diagram

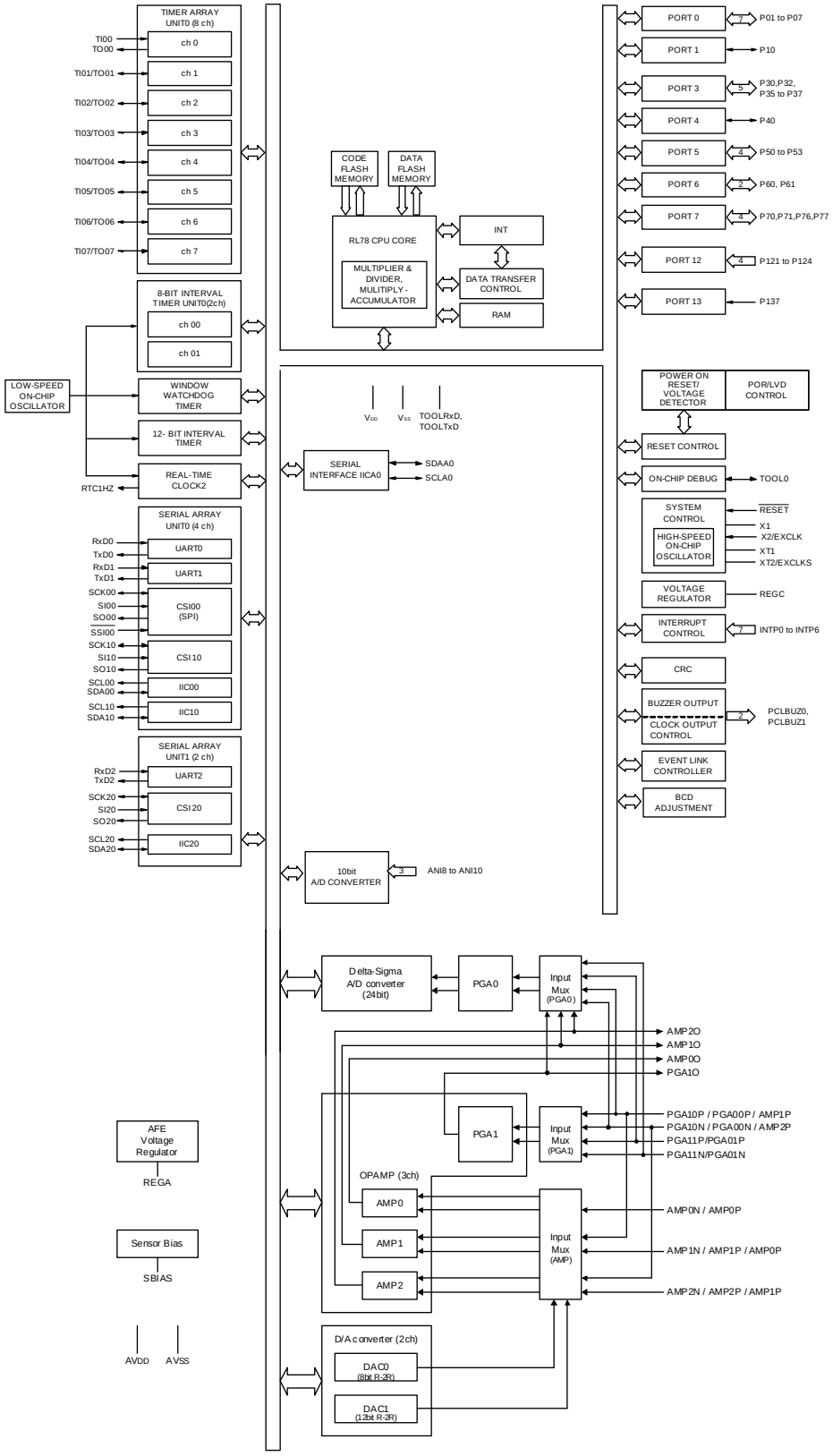
1.5.1 80-pin products (R5F11NM)



1.5.2 64-pin products (R5F11NL)

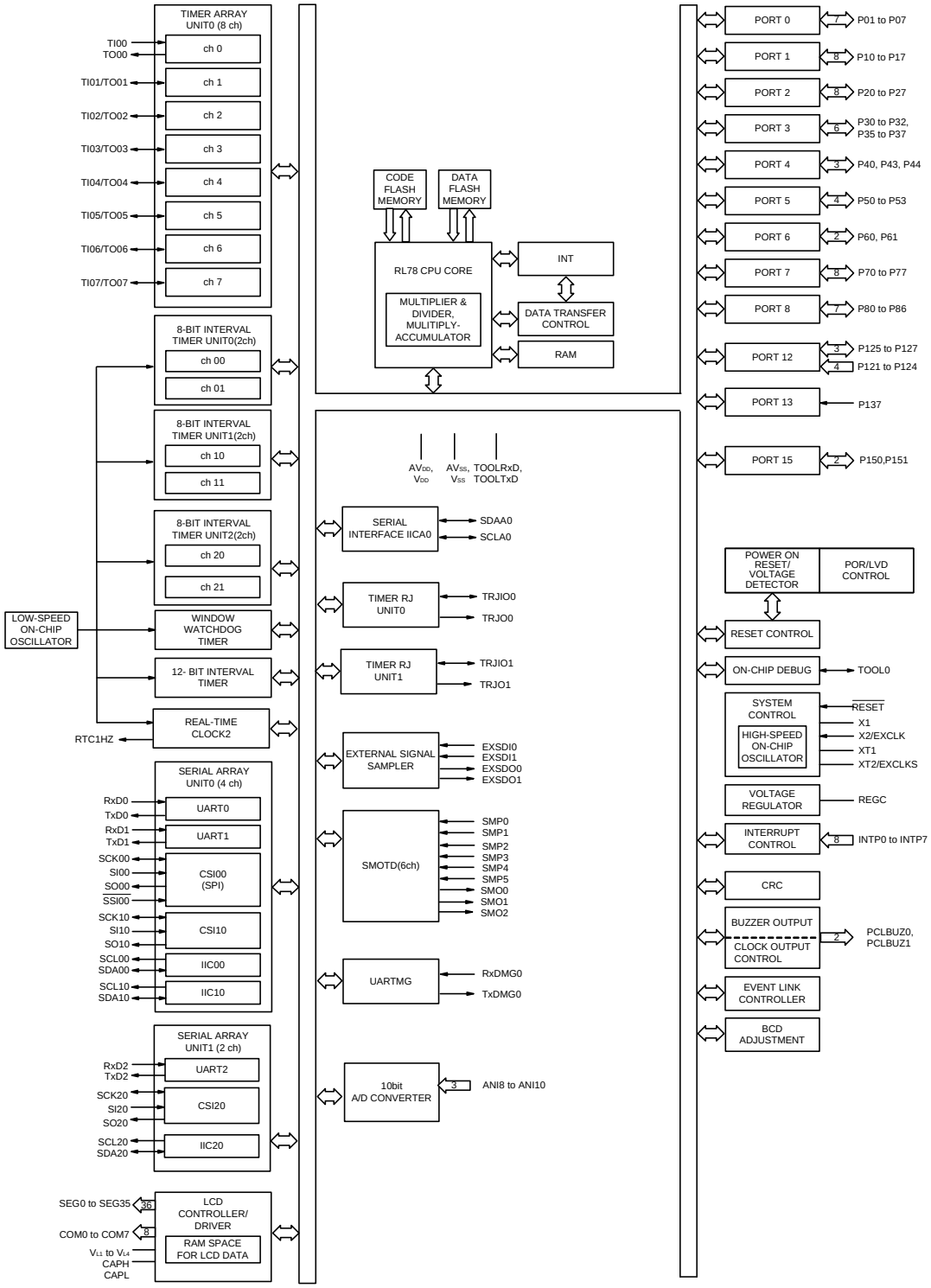


1.5.3 64-pin products (R5F11PL), 48-pin products (R5F11NG)



Remark 64-pin products (R5F11PL) have the same functionality as 48-pin products (R5F11NG). The only difference is the package.

1.5.4 80-pin products (R5F11RM)



1.6 Outline of Functions

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Item		80-pin LFQFP	64-pin LFQFP	64-pin TFBGA 48-pin LFQFP	80-pin LFQFP
		R5F11NMx (x = E to G)	R5F11NLx (x = F, G)	R5F11PLx, R5F11NGx (x = F, G)	R5F11RMG
Code flash memory (KB)		64 to 128	96 to 128	96 to 128	128
Data flash memory (KB)		4	4	4	4
RAM (KB)		5.5	5.5	5.5	8
Memory space		1 MB			
Main system clock	High-speed system clock	X1 (crystal/ceramic) oscillation, external main system clock input (EXCLK)			
		1 to 20 MHz: V_{DD} = 2.7 to 5.5 V, 1 to 8 MHz: V_{DD} = 2.4 to 2.7 V			1 to 20 MHz: V_{DD} = 2.7 to 5.5 V, 1 to 8 MHz: V_{DD} = 1.8 to 2.7 V
	High-speed on-chip oscillator clock	HS (high-speed main) operation mode: 1 to 24 MHz (V_{DD} = 2.7 to 5.5 V), HS (high-speed main) operation mode: 1 to 16 MHz (V_{DD} = 2.4 to 5.5 V)			HS (high-speed main) operation mode: 1 to 24 MHz (V_{DD} = 2.7 to 5.5 V), HS (high-speed main) operation mode: 1 to 16 MHz (V_{DD} = 2.4 to 5.5 V), LS (low-speed main) operation mode: 1 to 8 MHz (V_{DD} = 1.8 to 5.5 V)
Subsystem clock		XT1 (crystal) oscillation, external subsystem clock input (EXCLKS)			
		32.768 kHz (TYP.): V_{DD} = 2.4 to 5.5 V			32.768 kHz (TYP.): V_{DD} = 1.8 to 5.5 V 38.4 kHz (TYP.): V_{DD} = 1.8 to 5.5 V
Low-speed on-chip oscillator clock		15 kHz (TYP.): V_{DD} = 2.4 to 5.5 V			15 kHz (TYP.): V_{DD} = 1.8 to 5.5 V
General-purpose register		8 bits × 32 registers (8 bits × 8 registers × 4 banks)			
Minimum instruction execution time		0.04167 μs (High-speed on-chip oscillator clock: f_{IH} = 24 MHz operation)			
		0.05 μs (High-speed system clock: f_{MX} = 20 MHz operation)			
		30.5 μs (Subsystem clock: f_{SUB} = 32.768 kHz operation)			
Instruction set		• Data transfer (8/16 bits) • Adder and subtractor/logical operation (8/16 bits) • Multiplication (8 bits × 8 bits, 16 bits × 16 bits), Division (16 bits ÷ 16 bits, 32 bits ÷ 32 bits) • Multiplication and Accumulation (16 bits × 16 bits + 32 bits) • Rotate, barrel shift, and bit manipulation (Set, reset, test, and Boolean operation), etc.			
I/O port	Total	53	36	29	63
	CMOS I/O	46	29	22	56
	CMOS input	5	5	5	5
	CMOS output	—	—	—	—
	N-ch open-drain I/O (6 V tolerance)	2	2	2	2

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Item		80-pin LFQFP	64-pin LFQFP	64-pin TFBGA 48-pin LFQFP	80-pin LFQFP
		R5F11NMx (x = E to G)	R5F11NLx (x = F, G)	R5F11PLx, R5F11NGx (x = F, G)	R5F11RMG
Timer	16-bit timer TAU	8 channels (Timer outputs: 8, PWM outputs: 7 Note 1)			
	8-bit or 16-bit interval timer	2 channels (8 bits)/1 channel (16 bits)			6 channels (8 bits)/3 channels (16 bits)
	Watchdog timer	1 channel			
	12-bit interval timer	1 channel			
	Real-time clock 2	1 channel			
	RTC output	1 1 Hz (subsystem clock: f_{SUB} = 32.768 kHz)			
	16-bit timer RJ	—			2 channels, timer outputs: 2
	External signal sampler	—			1 channel
	Sampling output timer detector (SMOTD)	—			Input: 6 channels Output: 3 channels
Clock output/buzzer output		2	1	2	2
		• 2.44 kHz, 4.88 kHz, 9.77 kHz, 1.25 MHz, 2.5 MHz, 5 MHz, 10 MHz (Main system clock: f_{MAIN} = 20 MHz operation) • 256 Hz, 512 Hz, 1.024 kHz, 2.048 kHz, 4.096 kHz, 8.192 kHz, 16.384 kHz, 32.768 kHz (Subsystem clock: f_{SUB} = 32.768 kHz operation)			
8/10-bit resolution A/D converter	Internal	3 channels			
	External	2 channels: Internal reference voltage (1.45 V), temperature sensor output voltage (only selectable in HS (high-speed main) mode)			
24-bit ΔΣ A/D converter with programmable gain instrumentation amplifier 0 (PGA0)		Analog input: 1 channel (differential or single-ended)	Analog input: 1 channel (differential or single-ended), 3 channels (single-ended)	Analog input: 2 channels (differential or single-ended), 3 channels (single-ended)	—
D/A converter	12-bit	—	1 channel (with an output amplifier but no external output pin)	1 channel (with an output amplifier but no external output pin)	—
	8-bit	1 channel (without an output amplifier and no external output pin)	1 channel (without an output amplifier and no external output pin)	1 channel (without an output amplifier and no external output pin)	—
Programmable gain instrumentation amplifier 1 (PGA1)		—	1 channel	1 channel	—
Rail-to-rail operational amplifier		1 channel	1 channel	1 channel	—
General-purpose operational amplifier		—	2 channels	2 channels	—
Serial interface		• Simplified SPI(CSI)(SPI supported): 1 channel/UART (LIN-bus supported): 1 channel/simplified I^2C: 1 channel • Simplified SPI(CSI): 1 channel/UART: 1 channel/simplified I^2C: 1 channel • Simplified SPI(CSI): 1 channel/UART: 1 channel/simplified I^2C: 1 channel			
	I^2C bus	1 channel			1 channel
	Serial interface UARTMG	—			1 channel

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Item		80-pin LFQFP R5F11NMx (x = E to G)	64-pin LFQFP R5F11NLx (x = F, G)	64-pin TFBGA 48-pin LFQFP R5F11PLx, R5F11NGx (x = F, G)	80-pin LFQFP R5F11RMG
LCD controller/driver		Internal voltage boosting method, capacitor split method, and external resistance division method are switchable.			
	Segment signal output	36 (32) Note 2	27 (23) Note 2	—	36 (32) Note 2
	Common signal output	4 (8) Note 2	4 (8) Note 2	—	4 (8) Note 2
Data transfer controller (DTC)		26 sources	24 sources	25 sources	35 sources
Event link controller (ELC)		Event input: 20, Event trigger output: 7	Event input: 18, Event trigger output: 10	Event input: 19, Event trigger output: 10	Event input: 26, Event trigger output: 5
Vectored interrupt sources	Internal	29	29	29	43
	External	8	6	7	8
Reset		• Reset by $\overline{\text{RESET}}$ pin • Internal reset by watchdog timer • Internal reset by power-on-reset • Internal reset by voltage detector • Internal reset by illegal instruction execution Note 3 • Internal reset by RAM parity error • Internal reset by illegal-memory access			
Power-on-reset circuit		• Power-on-reset: 1.51 ±0.04 V • Power-down-reset: 1.50 ±0.04 V			
Voltage detector		• Rising edge: 2.50 V to 4.06 V (9 stages) • Falling edge: 2.45 V to 3.98 V (9 stages)			• Rising edge: 1.88 V to 4.06 V (12 stages) • Falling edge: 1.84 V to 3.98 V (12 stages)
On-chip debug function		Provided			
Power supply voltage		V_{DD} = 2.4 to 5.5 V (10-bit SAR A/D converter: 2.4 to 5.5 V, operating voltage of the analog front-end (AFE): 2.7 to 5.5 V)			V_{DD} = 1.8 to 5.5 V
Operating ambient temperature		T_A = -40 to +85°C (A: Consumer applications)			T_A = -40 to +85°C (D: Industrial applications)

Note 1. The number of outputs depends on the setting of channels in use and the number of the master.

Note 2. The number in parentheses indicates the number of signal outputs when 8 coms are used.

Note 3. The illegal instruction is generated when instruction code FFH is executed.
Reset by the illegal instruction execution not is issued by emulation with the in-circuit emulator or on-chip debug emulator.

CHAPTER 2 PIN FUNCTIONS

2.1 Port Function

Pin I/O buffer power supplies depend on the product. The relationship between these power supplies and the pins is shown below.

Table 2 - 1 Pin I/O Buffer Power Supplies

(1) R5F11NM

Power Supply	Corresponding Pins
V_{DD}	• Pins other than below
AV_{DD}	• REGA, SBIAS, PGA00N, PGA00P, AMP0P, AMP0N/AMP0P, AMP0O, ANI12 to ANI14

(2) R5F11NL

Power Supply	Corresponding Pins
V_{DD}	• Pins other than below
AV_{DD}	• REGA, SBIAS, PGA10N/PGA00N/AMP2P, PGA10P/PGA00P/AMP1P, AMP0N/AMP0P, AMP1N/AMP1P/AMP0P, AMP2N/AMP2P/AMP1P, PGA1O, AMP0O to AMP2O

(3) R5F11PL, R5F11NG

Power Supply	Corresponding Pins
V_{DD}	• Pins other than below
AV_{DD}	• REGA, SBIAS, PGA10N/PGA00N/AMP2P, PGA10P/PGA00P/AMP1P, AMP0N/AMP0P, AMP1N/AMP1P/AMP0P, AMP2N/AMP2P/AMP1P, PGA11N/PGA01N, PGA11P/PGA01P, PGA1O, AMP0O to AMP2O

(4) R5F11RM

Power Supply	Corresponding Pins
V_{DD}	• Pins other than below
AV_{DD}	• P20 to P27, P150, P151

Setting in each port I/O, buffer, pull-up resistor is also valid for alternate functions.

2.1.1 R5F11NM

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Function Name	Pin Type	I/O	After Reset	Alternate Function	Function
P01	7-5-4	I/O	Digital input invalid Note	(INTP5)/SEG22	Port 0. 7-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting at input port. Input of P03, P04, and P07 can be set to TTL input buffer. Output of P02 to P04, P06, and P07 can be set to N-ch open-drain output (VDD tolerance).
P02	7-5-10			(SO10/TxD1)/ PCLBUZ0/SEG23	
P03	8-5-10			(SI10/RxD1/SDA10)/ TO00/SEG24	
P04				INTP6/(SCK10/SCL10)/ SEG25	
P05	7-5-4			TI06/TO06/SEG26	
P06	7-5-10			SO20/TxD2/TI00/ SEG27	
P07	8-5-10			SI20/RxD2/SDA20/ TI05/TO05/SEG28	
P10	8-5-10	I/O	Digital input invalid Note	INTP2/SCK20/SCL20/ SEG29	Port 1. 8-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting at input port. Input of P10 can be set to TTL input buffer. Output of P10 can be set to N-ch open-drain output (VDD tolerance).
P11	7-5-4			SEG30	
P12				SEG31	
P13				SEG32	
P14				SEG33	
P15				SEG34	
P16				SEG35	
P17	7-1-3		Input port	(TI07/TO07)	
P30	7-5-4	I/O	Digital input invalid Note	INTP3/RTC1HZ/SEG16	Port 3. 6-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting at input port. Input of P35 and P36 can be set to TTL input buffer. Output of P35 to P37 can be set to N-ch open-drain output (VDD tolerance).
P31				TI01/TO01/SEG17	
P32				INTP4/$\overline{\text{SSI00}}$/SEG18	
P35	8-5-10			SCK00/SCL00/SEG19	
P36				SI00/RxD0/TOOLRxD/ SDA00/PCLBUZ1/ SEG20	
P37	7-5-10			SO00/TxD0/TOOLTxD/ SEG21	

Note “Digital input invalid” refers to the state in which all the digital outputs, digital inputs, and LCD outputs are disabled.

Remark Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection registers 0 to 3 (PIOR0 to PIOR3).
For details, see **Figure 4 - 7** to **Figure 4 - 10**.

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Function Name	Pin Type	I/O	After Reset	Alternate Function	Function
P40	8-1-4	I/O	Input port	TOOL0/(INTP1)/ (SCK00/SCL00)/ (TI01/TO01)	Port 4. 3-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting at input port. Input of P40 and P43 can be set to TTL input buffer. Output of P40, P43, and P44 can be set to N-ch open-drain (V_{DD} tolerance).
P43				(SI00/RxD0/SDA00)/ (TI00)/(TO00)	
P44	7-1-4			(SO00/TxD0)	
P50	7-5-10	I/O	Digital input invalid Note	SO10/TxD1/TI03/TO03/ SEG7	Port 5. 4-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting at input port. Input of P51 and P52 can be set to TTL input buffer. Output of P50 to P52 can be set to N-ch open-drain (V_{DD} tolerance).
P51	8-5-10			SI10/RxD1/SDA10/TI04 /TO04/SEG6	
P52				SCK10/SCL10/TI02/ TO02/SEG5	
P53	7-5-4			(INTP0)/SEG4	
P60	12-1-3	I/O	Input port	(INTP3)/SCLA0	Port 6. 2-bit I/O port. Input/output can be specified in 1-bit units. Output of P60 and P61 can be set to N-ch open-drain output (6 V tolerance).
P61				(INTP4)/SDAA0	
P70	7-5-4	I/O	Digital input invalid Note	SEG8	Port 7. 8-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting at input port.
P71				SEG9	
P72				SEG10	
P73				SEG11	
P74				SEG12	
P75				SEG13	
P76				SEG14	
P77				TI07/TO07/SEG15	
P80	7-1-4	I/O	Input port	(SO20/TxD2)/(TI02/ TO02)	Port 8. 7-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting at input port. Input of P81 and P82 can be set to TTL input buffer. Output of P80 to P82 can be set to N-ch open-drain output (V_{DD} tolerance).
P81	8-1-4			(SI20/RxD2/SDA20)/ (TI00)/(TO00)	
P82				(INTP2)/(SCK20/ SCL20)/(TI07/TO07)	
P83	7-1-3			(TI03/TO03)/ (PCLBUZ1)	
P84				(TI05/TO05)	
P85				INTP7	
P86				(INTP6)	

Note “Digital input invalid” refers to the state in which all the digital outputs, digital inputs, and LCD outputs are disabled.

Remark Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection registers 0 to 3 (PIOR0 to PIOR3).
For details, see **Figure 4 - 7** to **Figure 4 - 10**.

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Function Name	Pin Type	I/O	After Reset	Alternate Function	Function
P121	2-2-1	Input	Input port	X1/INTP1	Port 12. 3-bit I/O port and 4-bit input only port. For only P125 to P127, input/output can be specified. For only P125 to P127, use of an on-chip pull-up resistor can be specified by a software setting at input port.
P122				X2/EXCLK/INTP5	
P123				XT1	
P124				XT2/EXCLKS	
P125	7-5-6	I/O	Digital input invalid Note	(TI06/TO06)/VL3	
P126	7-5-5			(TI05/TO05)/CAPL	
P127				(TI04/TO04)/CAPH	
P137	2-1-2	Input	Input port	INTP0/($\overline{\text{SSI00}}$)	Port 13. 1-bit input only port.
$\overline{\text{RESET}}$	2-1-1	Input	—	—	Input-only pin for external reset. Connect to V_{DD} directly or via a resistor when external reset is not used.
COM0 to COM3	18-5-1	Output	Output	—	COM-only pin.
COM4				SEG0	
COM5				SEG1	
COM6				SEG2	
COM7				SEG3	

Note “Digital input invalid” refers to the state in which all the digital outputs, digital inputs, and LCD outputs are disabled.

Remark Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection registers 0 to 3 (PIOR0 to PIOR3).
For details, see **Figure 4 - 7** to **Figure 4 - 10**.

2.1.2 R5F11NL

(1/3)

Function Name	Pin Type	I/O	After Reset	Alternate Function	Function
P03	7-10-3	I/O	Analog input	ANI8/TO00/SEG24	Port 0. 4-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting at input port. Input of P07 can be set to TTL input buffer. Output of P06 and P07 can be set to N-ch open-drain output (V_{DD} tolerance). P03 and P05 can be set to analog input Note 2.
P05				ANI10/TI06/TO06/SEG26	
P06	7-5-10		Digital input invalid Note 1	SO20/TxD2/TI00/SEG27	
P07	8-5-10			SI20/RxD2/SDA20/TI05/TO05/SEG28	
P10	8-5-10	I/O	Digital input invalid Note 1	INTP2/SCK20/SCL20/SEG29	Port 1. 6-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting at input port. Input of P10 can be set to TTL input buffer. Output of P10 can be set to N-ch open-drain output (V_{DD} tolerance). P11 can be set to analog input Note 2.
P11	7-10-3		Analog input	ANI11/SEG30	
P12	7-5-4		Digital input invalid Note 1	SEG31	
P13				SEG32	
P14				SEG33	
P15				SEG34	
P30	7-5-4	I/O	Digital input invalid Note 1	INTP3/RTC1HZ/SEG16	Port 3. 6-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting at input port. Input of P35 and P36 can be set to TTL input buffer. Output of P35 to P37 can be set to N-ch open-drain output (V_{DD} tolerance).
P31				TI01/TO01/SEG17	
P32				INTP4/$\overline{\text{SSI00}}$/SEG18	
P35	8-5-10			SCK00/SCL00/SEG19	
P36				SI00/RxD0/TOOLRxD/SDA00/PCLBUZ1/SEG20	
P37	7-5-10			SO00/TxD0/TOOLTxD/SEG21	

Note 1. "Digital input invalid" refers to the state in which all the digital outputs, digital inputs, and LCD outputs are disabled.

Note 2. Each pin can be specified as either digital or analog by setting port mode control register x (PMCx) (can be specified in 1-bit units).

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Function Name	Pin Type	I/O	After Reset	Alternate Function	Function
P40	7-1-3	I/O	Input port	TOOL0/(INTP1)/ (TI01/TO01)	Port 4. 1-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting at input port.
P50	7-5-10	I/O	Digital input invalid Note	SO10/TxD1/TI03/TO03/ SEG7	Port 5. 3-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting at input port. Input of P51 and P52 can be set to TTL input buffer. Output of P50 to P52 can be set to N-ch open-drain output (V_{DD} tolerance).
P51	8-5-10			SI10/RxD1/SDA10/TI04 /TO04/SEG6	
P52				SCK10/SCL10/TI02/ TO02/SEG5	
P60	12-1-3	I/O	Input port	(INTP3)/SCLA0	Port 6. 2-bit I/O port. Input/output can be specified in 1-bit units. Output of P60 and P61 is N-ch open-drain output (6 V tolerance).
P61				(INTP4)/SDAA0	
P70	7-5-4	I/O	Digital input invalid Note	SEG8	Port 7. 4-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting at input port.
P71				SEG9	
P76				SEG14	
P77				TI07/TO07/SEG15	
P82	7-1-3	I/O	Input port	(TI07/TO07)	Port 8. 2-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting at input port.
P83				(TI03/TO03)/ (PCLBUZ1)	
P121	2-2-1	Input	Input port	X1/INTP1	Port 12. 3-bit I/O port and 4-bit input only port. For only P125 to P127, input/output can be specified. For only P125 to P127, use of an on-chip pull-up resistor can be specified by a software setting at input port.
P122				X2/EXCLK/INTP5	
P123				XT1	
P124				XT2/EXCLKS	
P125	7-5-6	I/O	Digital input invalid Note	(TI06/TO06)/VL3	
P126	7-5-5			(TI05/TO05)/CAPL	
P127				(TI04/TO04)/CAPH	
P137	2-1-2	Input	Input port	INTP0	Port 13. 1-bit input only port.
$\overline{\text{RESET}}$	2-1-1	Input	—	—	Input-only pin for external reset. Connect to V_{DD} directly or via a resistor when external reset is not used.

Note "Digital input invalid" refers to the state in which all the digital outputs, digital inputs, and LCD outputs are disabled.

Remark Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection registers 0 to 3 (PIOR0 to PIOR3).
For details, see **Figure 4 - 7** to **Figure 4 - 10**.

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Function Name	Pin Type	I/O	After Reset	Alternate Function	Function
COM0 to COM3	18-5-1	Output	Output	—	COM-only pin.
COM4				SEG0	
COM5				SEG1	
COM6				SEG2	
COM7				SEG3	

2.1.3 R5F11PL, R5F11NG

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Function Name	Pin Type	I/O	After Reset	Alternate Function	Function
P01	7-1-3	I/O	Input port	(INTP5)	Port 0. 7-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting at input port. Input of P03, P04, and P07 can be set to TTL input buffer. Output of P02 to P04, P06, and P07 can be set to N-ch open-drain output (V_{DD} tolerance). P03 to P05 can be set to analog input Note.
P02	7-1-4			(SO10/TxD1)/ PCLBUZ0	
P03	8-3-4		Analog input	ANI8/(SI10/RxD1/ SDA10)/TO00	
P04				ANI9/INTP6/(SCK10/ SCL10)	
P05	7-3-3			ANI10/TI06/TO06	
P06	7-1-4		Input port	SO20/TxD2/TI00	
P07	8-1-4			SI20/RxD2/SDA20/TI05 /TO05	
P10	8-1-4	I/O	Input port	INTP2/SCK20/SCL20	Port 1. 1-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting at input port. Input of P10 can be set to TTL input buffer. Output of P10 can be set to N-ch open-drain output (V_{DD} tolerance).
P30	7-1-3	I/O	Input port	INTP3/RTC1HZ	Port 3. 5-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting at input port. Input of P35 and P36 can be set to TTL input buffer. Output of P35 to P37 can be set to N-ch open-drain output (V_{DD} tolerance).
P32				INTP4/$\overline{SSI00}$	
P35	8-1-4			SCK00/SCL00	
P36				SI00/RxD0/TOOLRxD/ SDA00/PCLBUZ1	
P37	7-1-4			SO00/TxD0/TOOLTxD	
P40	7-1-3	I/O	Input port	TOOL0/(INTP1)/TI01/ TO01	Port 4. 1-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting at input port.
P50	7-1-4	I/O	Input port	SO10/TxD1/TI03/TO03	Port 5. 4-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting at input port. Input of P51 and P52 can be set to TTL input buffer. Output of P50 to P52 can be set to N-ch open-drain output (V_{DD} tolerance).
P51	8-1-4			SI10/RxD1/SDA10/TI04 /TO04	
P52				SCK10/SCL10/TI02/ TO02	
P53	7-1-3			P53/(INTP0)	

Note Each pin can be specified as either digital or analog by setting port mode control register x (PMCx) (can be specified in 1-bit units).

Remark Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection registers 0, 1, 3 (PIOR0, PIOR1, PIOR3).
For details, see **Figure 4 - 7**, **Figure 4 - 8**, and **Figure 4 - 10**.

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Function Name	Pin Type	I/O	After Reset	Alternate Function	Function
P60	12-1-3	I/O	Input port	(INTP3)/SCLA0	Port 6. 2-bit I/O port. Input/output can be specified in 1-bit units. Output of P60 and P61 is N-ch open-drain output (6 V tolerance).
P61				(INTP4)/SDAA0	
P70	7-1-3	I/O	Input port	—	Port 7. 4-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting at input port.
P71				(TI05/TO05)	
P76				(TI06/TO06)	
P77				TI07/TO07	
P121	2-2-1	Input	Input port	X1/INTP1	Port 12. 4-bit input only port.
P122				X2/EXCLK/INTP5	
P123				XT1	
P124				XT2/EXCLKS	
P137	2-1-2	Input	Input port	INTP0	Port 13. 1-bit input only port.
$\overline{\text{RESET}}$	2-1-1	Input	—	—	Input-only pin for external reset. Connect to V_{DD} directly or via a resistor when external reset is not used.

Remark Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection registers 0, 1, 3 (PIOR0, PIOR1, PIOR3).
For details, see **Figure 4 - 7**, **Figure 4 - 8**, and **Figure 4 - 10**.

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Function Name	Pin Type	I/O	After Reset	Alternate Function	Function
P01	7-5-4	I/O	Digital input invalid Note 1	SEG22	Port 0. 7-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting at input port. Input of P03, P04, and P07 can be set to TTL input buffer. Output of P02 to P04, P06, and P07 can be set to N-ch open-drain output (VDD tolerance). P03 to P05 can be set to analog input Note 2.
P02	7-5-10			(SO10/TxD1)/ PCLBUZ0/SEG23	
P03	8-5-13		Analog input	ANI8/(SI10/RxD1/ SDA10)/TO00/SEG24	
P04				ANI9/(SCK10/SCL10)/ SEG25	
P05	7-10-3			ANI10/TI06/TO06/ SEG26	
P06	7-5-10		Digital input invalid Note 1	SO20/TxD2/TI00/ SEG27	
P07	8-5-10			SI20/RxD2/SDA20/TI05 /TO05/SEG28	
P10	8-5-10	I/O	Digital input invalid Note 1	SCK20/SCL20/SEG29	Port 1. 8-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting at input port. Input of P10 and P13 can be set to TTL input buffer. Output of P10 and P12 can be set to N-ch open-drain output (VDD tolerance).
P11	7-5-4			SEG30	
P12	7-5-10			TxDMG0/SEG31	
P13	8-5-4			RxDMG0/SEG32	
P14	7-5-4			TRJIO1/SEG33	
P15				TRJIO0/SEG34	
P16				SMO0/SEG35	
P17	7-1-3		Input port	SMO1	
P20	7-1-3	I/O	Input port	SMP4	Port 2. 8-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting at input port.
P21				SMP5	
P22				INTP7	
P23				INTP6	
P24				(INTP5)	
P25				INTP4	
P26				INTP3	
P27				INTP2	

Note 1. "Digital input invalid" refers to the state in which all the digital outputs, digital inputs, and LCD outputs are disabled.

Note 2. Each pin can be specified as either digital or analog by setting port mode control register x (PMCx) (can be specified in 1-bit units).

Remark Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection registers 0 to 3 (PIOR0 to PIOR3).
For details, see **Figure 4 - 7** to **Figure 4 - 10**.

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Function Name	Pin Type	I/O	After Reset	Alternate Function	Function
P30	7-5-4	I/O	Digital input invalid Note	RTC1HZ/SEG16	Port 3. 6-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting at input port. Input of P35 and P36 can be set to TTL input buffer. Output of P35 to P37 can be set to N-ch open-drain output (V_{DD} tolerance).
P31				TI01/TO01/SEG17	
P32				$\overline{SSI00}$/SEG18	
P35	8-5-10			SCK00/SCL00/SEG19	
P36				SI00/RxD0/TOOLRxD/ SDA00/PCLBUZ1/ SEG20	
P37	7-5-10			SO00/TxD0/TOOLTxD/ SEG21	
P40	8-1-4	I/O	Input port	TOOL0/(SCK00/ SCL00)/(TI01/TO01)	Port 4. 3-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting at input port. Input of P40 and P43 can be set to TTL input buffer. Output of P40, P43, and P44 can be set to N-ch open-drain (V_{DD} tolerance).
P43				(SI00/RxD0/SDA00)/ (SMP0)	
P44	7-1-4			(SO00/TxD0)/(SMP1)	
P50	7-5-10	I/O	Digital input invalid Note	SO10/TxD1/TI03/TO03/ SEG7	Port 5. 4-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting at input port. Input of P51 and P52 can be set to TTL input buffer. Output of P50 to P52 can be set to N-ch open-drain output (V_{DD} tolerance).
P51	8-5-10			SI10/RxD1/SDA10/TI04 /TO04/SEG6	
P52				SCK10/SCL10/TI02/ TO02/SEG5	
P53	7-5-4			SEG4	
P60	12-1-3	I/O	Input port	SCLA0	Port 6. 2-bit I/O port. Input/output can be specified in 1-bit units. Output of P60 and P61 is N-ch open-drain output (6 V tolerance).
P61				SDAA0	
P70	7-5-4	I/O	Digital input invalid Note	SEG8	Port 7. 8-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting at input port.
P71				SEG9	
P72				SEG10	
P73				SEG11	
P74				SEG12	
P75				SEG13	
P76				SEG14	
P77				TI07/TO07/SEG15	

Note “Digital input invalid” refers to the state in which all the digital outputs, digital inputs, and LCD outputs are disabled.

Remark Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection registers 0 to 3 (PIOR0 to PIOR3).
For details, see **Figure 4 - 7** to **Figure 4 - 10**.

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Function Name	Pin Type	I/O	After Reset	Alternate Function	Function
P80	7-1-4	I/O	Input port	(SO20/TxD2)/ (TI02/TO02)/TRJO0	Port 8. 7-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting at input port. Input of P81 and P82 can be set to TTL input buffer. Output of P80 to P82 can be set to N-ch open-drain output (V_{DD} tolerance).
P81	8-1-4			(SI20/RxD2/SDA20)/ (TI00)/(TO00)/TRJO1	
P82				(SCK20/SCL20)/(TI07/ TO07)/EXSDO0	
P83	7-1-3			(TI03/TO03)/EXSDO1/ (PCLBUZ1)	
P84				SMO2	
P85				SMP0/EXSDI0	
P86				SMP1/EXSDI1	
P121	2-2-1	Input	Input port	X1/INTP1	Port 12. 3-bit I/O port and 4-bit input only port. For only P125 to P127, input/output can be specified. For only P125 to P127, use of an on-chip pull-up resistor can be specified by a software setting at input port.
P122				X2/EXCLK/INTP5	
P123				XT1	
P124				XT2/EXCLKS	
P125	7-5-6	I/O	Digital input invalid Note	(TI06/TO06)/VL3	
P126	7-5-5			(TI05/TO05)/CAPL	
P127				(TI04/TO04)/CAPH	
P137	2-1-2	Input	Input port	INTP0/($\overline{\text{SSI00}}$)	Port 13. 1-bit input only port.
P150	7-1-3	I/O	Input port	SMP2	Port 15. 2-bit I/O port port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting at input port.
P151				SMP3	
$\overline{\text{RESET}}$	2-1-1	Input	—	—	Input-only pin for external reset. Connect to V_{DD} directly or via a resistor when external reset is not used.
COM0 to COM3	18-5-1	Output	Output	—	COM-only pin.
COM4				SEG0	
COM5				SEG1	
COM6				SEG2	
COM7				SEG3	

Note “Digital input invalid” refers to the state in which all the digital outputs, digital inputs, and LCD outputs are disabled.

Remark Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection registers 0 to 3 (PIOR0 to PIOR3).
For details, see **Figure 4 - 7** to **Figure 4 - 10**.

2.2 Functions other than port pins

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Function Name	I/O	Function	R5F11NM	R5F11NL	R5F11PL, R5F11NG	R5F11RM
PGA00N	Input	PGA0 negative input	√	√	√	—
PGA01N	Input		—	—	√	—
PGA10N	Input	PGA1 negative input	—	√	√	—
PGA11N	Input		—	—	√	—
PGA00P	Input	PGA0 positive input	√	√	√	—
PGA01P	Input		—	—	√	—
PGA10P	Input	PGA1 positive input	—	√	√	—
PGA11P	Input		—	—	√	—
PGA1O	Output	PGA1 output	—	√	√	—
AMP0N	Input	Operational amplifier 0 negative input	√	√	√	—
AMP1N	Input	Operational amplifier 1 negative input	—	√	√	—
AMP2N	Input	Operational amplifier 2 negative input	—	√	√	—
AMP0P	Input	Operational amplifier 0 positive input	√	√	√	—
AMP1P	Input	Operational amplifier 1 positive input	—	√	√	—
AMP2P	Input	Operational amplifier 2 positive input	—	√	√	—
AMP0O	Output	Operational amplifier 0 output	√	√	√	—
AMP1O	Output	Operational amplifier 1 output	—	√	√	—
AMP2O	Output	Operational amplifier 2 output	—	√	√	—
SBIAS	Output	Reference voltage output	√	√	√	—
REGA	—	Pin for connecting regulator output stabilization capacitance for internal operation (analog power supply)	√	√	√	—
ANI8	Input	Analog input 8 of 10-bit A/D converter	—	√	√	√
ANI9	Input	Analog input 9 of 10-bit A/D converter	—	—	√	√
ANI10	Input	Analog input 10 of 10-bit A/D converter	—	√	√	√
ANI11	Input	Analog input 11 of 10-bit A/D converter	—	√	—	—
ANI12	Input	Analog input 12 of 10-bit A/D converter	√	—	—	—
ANI13	Input	Analog input 13 of 10-bit A/D converter	√	—	—	—
ANI14	Input	Analog input 14 of 10-bit A/D converter	√	—	—	—
INTP0	Input	External interrupt request input Specified the valid edge: Rising edge, falling edge, or both rising and falling edges	√	√	√	√
INTP1	Input		√	√	√	√
INTP2	Input		√	√	√	√
INTP3	Input		√	√	√	√
INTP4	Input		√	√	√	√
INTP5	Input		√	√	√	√
INTP6	Input		√	—	√	√
INTP7	Input		√	—	—	√
PCLBUZ0	Output	Clock output/buzzer output	√	—	√	√
PCLBUZ1	Output		√	√	√	√

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Function Name	I/O	Function	R5F11NM	R5F11NL	R5F11PL, R5F11NG	R5F11RM
RTC1HZ	Output	Real-time clock correction clock (1 Hz) output	√	√	√	√
RxD0	Input	Serial data input pin of serial interface UART0	√	√	√	√
RxD1	Input	Serial data input pin of serial interface UART1	√	√	√	√
RxD2	Input	Serial data input pin of serial interface UART2	√	√	√	√
RxDMG0	Input	Serial data input pin of serial interface UARTMG0	—	—	—	√
TxD0	Output	Serial data output pin of serial interface UART0	√	√	√	√
TxD1	Output	Serial data output pin of serial interface UART1	√	√	√	√
TxD2	Output	Serial data output pin of serial interface UART2	√	√	√	√
TxDMG0	Output	Serial data output pin of serial interface UARTMG0	—	—	—	√
SCK00	I/O	Clock I/O pin of serial interface CSI00	√	√	√	√
SCK10	I/O	Clock I/O pin of serial interface CSI10	√	√	√	√
SCK20	I/O	Clock I/O pin of serial interface CSI20	√	√	√	√
SI00	Input	Serial data input pin of serial interface CSI00	√	√	√	√
SI10	Input	Serial data input pin of serial interface CSI10	√	√	√	√
SI20	Input	Serial data input pin of serial interface CSI20	√	√	√	√
SO00	Output	Serial data output pin of serial interface CSI00	√	√	√	√
SO10	Output	Serial data output pin of serial interface CSI10	√	√	√	√
SO20	Output	Serial data output pin of serial interface CSI20	√	√	√	√
$\overline{\text{SSI00}}$	Input	Slave select input pin of serial interface CSI00	√	√	√	√
SCL00	Output	Clock output pin of serial interface IIC00	√	√	√	√
SCL10	Output	Clock output pin of serial interface IIC10	√	√	√	√
SCL20	Output	Clock output pin of serial interface IIC20	√	√	√	√
SDA00	I/O	Serial data I/O pin of serial interface IIC00	√	√	√	√
SDA10	I/O	Serial data I/O pin of serial interface IIC10	√	√	√	√
SDA20	I/O	Serial data I/O pin of serial interface IIC20	√	√	√	√
SCLA0	I/O	Clock I/O pin of serial interface IICA0	√	√	√	√
SDAA0	I/O	Serial data I/O pin of serial interface IICA0	√	√	√	√
EXSDI0	Input	External signal sampler phase detection input	—	—	—	√
EXSDI1	Input		—	—	—	√
EXSDO0	Output	External signal sampler clock output	—	—	—	√
EXSDO1	Output		—	—	—	√
SMP0	Input	Sampling input	—	—	—	√
SMP1	Input		—	—	—	√
SMP2	Input		—	—	—	√
SMP3	Input		—	—	—	√
SMP4	Input		—	—	—	√
SMP5	Input		—	—	—	√
SMO0	Output	Sampling clock output	—	—	—	√
SMO1	Output		—	—	—	√
SMO2	Output		—	—	—	√

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Function Name	I/O	Function	R5F11NM	R5F11NL	R5F11PL, R5F11NG	R5F11RM
TRJIO0	I/O	Timer RJ I/O	—	—	—	√
TRJIO1	I/O		—	—	—	√
TRJO0	Output	Timer RJ output	—	—	—	√
TRJO1	Output		—	—	—	√
TI00	Input	The pins for inputting an external count clock/capture trigger to 16-bit timers 00 to 07	√	√	√	√
TI01	Input		√	√	√	√
TI02	Input		√	√	√	√
TI03	Input		√	√	√	√
TI04	Input		√	√	√	√
TI05	Input		√	√	√	√
TI06	Input		√	√	√	√
TI07	Input		√	√	√	√
TO00	Output	Timer output pins of 16-bit timers 00 to 07	√	√	√	√
TO01	Output		√	√	√	√
TO02	Output		√	√	√	√
TO03	Output		√	√	√	√
TO04	Output		√	√	√	√
TO05	Output		√	√	√	√
TO06	Output		√	√	√	√
TO07	Output		√	√	√	√
V_{L1}	—	LCD drive voltage	√	√	—	√
V_{L2}	—		√	√	—	√
V_{L3}	—		√	√	—	√
V_{L4}	—		√	√	—	√
CAPH	—	Connecting a capacitor for LCD controller/driver	√	√	—	√
CAPL	—		√	√	—	√
COM0	Output	LCD controller/driver common signal output	√	√	—	√
COM1	Output		√	√	—	√
COM2	Output		√	√	—	√
COM3	Output		√	√	—	√
COM4	Output		√	√	—	√
COM5	Output		√	√	—	√
COM6	Output		√	√	—	√
COM7	Output		√	√	—	√

(4/5)

Function Name	I/O	Function	R5F11NM	R5F11NL	R5F11PL, R5F11NG	R5F11RM
SEG0	Output	LCD controller/driver segment signal output	√	√	—	√
SEG1	Output		√	√	—	√
SEG2	Output		√	√	—	√
SEG3	Output		√	√	—	√
SEG4	Output		√	—	—	√
SEG5	Output		√	√	—	√
SEG6	Output		√	√	—	√
SEG7	Output		√	√	—	√
SEG8	Output		√	√	—	√
SEG9	Output		√	√	—	√
SEG10	Output		√	—	—	√
SEG11	Output		√	—	—	√
SEG12	Output		√	—	—	√
SEG13	Output		√	—	—	√
SEG14	Output		√	√	—	√
SEG15	Output		√	√	—	√
SEG16	Output		√	√	—	√
SEG17	Output		√	√	—	√
SEG18	Output		√	√	—	√
SEG19	Output		√	√	—	√
SEG20	Output		√	√	—	√
SEG21	Output		√	√	—	√
SEG22	Output		√	—	—	√
SEG23	Output		√	—	—	√
SEG24	Output		√	√	—	√
SEG25	Output		√	—	—	√
SEG26	Output		√	√	—	√
SEG27	Output		√	√	—	√
SEG28	Output		√	√	—	√
SEG29	Output		√	√	—	√
SEG30	Output		√	√	—	√
SEG31	Output		√	√	—	√
SEG32	Output		√	√	—	√
SEG33	Output		√	√	—	√
SEG34	Output		√	√	—	√
SEG35	Output		√	—	—	√
X1	—	Resonator connection for main system clock	√	√	√	√
X2	—		√	√	√	√
EXCLK	Input	External clock input for main system clock	√	√	√	√
XT1	—	Resonator connection for subsystem clock	√	√	√	√
XT2	—		√	√	√	√
EXCLKS	Input	External clock input for subsystem clock	√	√	√	√

(5/5)

Function Name	I/O	Function	R5F11NM	R5F11NL	R5F11PL, R5F11NG	R5F11RM
REGC	—	Pin for connecting regulator output stabilization capacitance for internal operation. Connect this pin to Vss via a capacitor (0.47 to 1 µF). Also, use a capacitor with good characteristics, since it is used to stabilize internal voltage.	√	√	√	√
$\overline{\text{RESET}}$	Input	This is the active-low system reset input pin. When the external reset pin is not used, connect this pin directly or via a resistor to VDD.	√	√	√	√
VDD	—	Power supply voltage for port pins (other than P20 to P27, P150, and P151) Power supply voltage for the 10-bit SAR A/D converter	√	√	√	√
AVDD	—	Analog power supply voltage (other than for the 10-bit SAR A/D converter) and power supply voltage for port pins (P20 to P27, P150, and P151) Note	√	√	√	√
VSS	—	Ground potential for port pins (other than P20 to P27, P150, and P151) Ground potential for the 10-bit SAR A/D converter	√	√	√	√
AVSS	—	Analog ground potential (other than for the 10-bit SAR A/D converter) Ground potential for port pins (P20 to P27, P150, and P151)Note	√	√	√	√
TOOLRxD	Input	UART reception pin for the external device connection used during flash memory programming	√	√	√	√
TOOLTxD	Output	UART transmission pin for the external device connection used during flash memory programming	√	√	√	√
TOOL0	I/O	Data I/O for flash memory programmer/debugger	√	√	√	√

Note R5F11R only.

Caution After reset release, the relationship between P40/TOOL0 and the operating mode are as follows.

Table 2 - 2 Relationship Between P40/TOOL0 and Operating Mode After Reset Release

P40/TOOL0	Operating mode
VDD	Normal operation mode
0 V	Flash memory programming mode

For details, see **34.4 Serial Programming Method**.

Remark Use bypass capacitors (about 0.1 µF) as noise and latch up countermeasures with relatively thick wires at the shortest distance to VDD to VSS lines.

2.3 Connection of Unused Pins

2.3.1 R5F11N, R5F11P

Table 2 - 3 shows the connections of unused pins.

Remark The pins mounted depend on the product. Refer to **1.3 Pin Configuration (Top View)** and **2.1 Port Function**.

Table 2 - 3 Connection of Unused Pins

Pin Name	I/O	Recommended Connection of Unused Pins
P01 to P07	I/O	Digital input invalid: Leave open. Analog input mode: Leave open. Digital input: Independently connect to VDD or VSS via a resistor. Digital output: Leave open. Segment output: Leave open.
P10 to P16		
P17		Input: Independently connect to VDD or VSS via a resistor. Output: Leave open.
P30 to P32, P35 to P37		Digital input invalid: Leave open. Digital input: Independently connect to VDD or VSS via a resistor. Digital output: Leave open. Segment output: Leave open.
P40/TOOL0		Input: Independently connect to VDD via a resistor, or leave open. Output: Leave open.
P43, P44		Input: Independently connect to VDD or VSS via a resistor. Output: Leave open.
P50 to P53		Digital input invalid: Leave open. Digital input: Independently connect to VDD or VSS via a resistor. Digital output: Leave open. Segment output: Leave open.
P60, P61		Input: Independently connect to VDD or VSS via a resistor. Output: Set the port's output latch to 0 and leave the pins open, or set the port's output latch to 1 and independently connect the pins to VDD or VSS via a resistor.
P70 to P77		Digital input invalid: Leave open. Digital input: Independently connect to VDD or VSS via a resistor. Digital output: Leave open. Segment output: Leave open.
P80 to P86		Input: Independently connect to VDD or VSS via a resistor. Output: Leave open.
P121 to P124	Input	Independently connect to VDD or VSS via a resistor.
P125 to P127	I/O	Digital input invalid: Leave open. Input: Independently connect to VDD or VSS via a resistor. Output: Leave open. LCD function mode: Leave open.
P137	Input	Independently connect to VDD or VSS via a resistor.
$\overline{\text{RESET}}$	Input	Connect to VDD directly or via a resistor.
REGC	—	Connect to VSS via a capacitor (0.47 to 1 μF).
COM0 to COM7	Output	Leave open.
VL1, VL2, VL4	—	Leave open.
PGA00N, PGA00P, PGA01N, PGA01P, PGA10N, PGA10P, PGA11N, PGA11P, AMP0N to AMP2N, AMP0P to AMP2P	Input	Connect to AVSS directly.
AMP0O to AMP2O, PGA1O	Output	Leave open.
REGA	—	Connect to AVSS via a capacitor (0.22 μF).
SBIAS	Output	Connect to AVSS via a capacitor (0.22 μF).

2.3.2 R5F11R

Table 2 - 4 shows the connections of unused pins.

Remark The pins mounted depend on the product. Refer to **1.3 Pin Configuration (Top View)** and **2.1 Port Function**.

Table 2 - 4 Connection of Unused Pins

Pin Name	I/O	Recommended Connection of Unused Pins
P01 to P07 P10 to P16	I/O	Digital input invalid: Leave open. Analog input mode: Leave open. Digital input: Independently connect to VDD or VSS via a resistor. Digital output: Leave open. Segment output: Leave open.
P17		Input: Independently connect to VDD or VSS via a resistor. Output: Leave open.
P20 to P27		Input: Independently connect to AVDD or AVSS via a resistor. Output: Leave open.
P30 to P32, P35 to P37		Digital input invalid: Leave open. Digital input: Independently connect to VDD or VSS via a resistor. Digital output: Leave open. Segment output: Leave open.
P40/TOOL0		Input: Independently connect to VDD via a resistor, or leave open. Output: Leave open.
P43, P44		Input: Independently connect to VDD or VSS via a resistor. Output: Leave open.
P50 to P53		Digital input invalid: Leave open. Digital input: Independently connect to VDD or VSS via a resistor. Digital output: Leave open. Segment output: Leave open.
P60, P61		Input: Independently connect to VDD or VSS via a resistor. Output: Set the port's output latch to 0 and leave the pins open, or set the port's output latch to 1 and independently connect the pins to VDD or VSS via a resistor.
P70 to P77		Digital input invalid: Leave open. Digital input: Independently connect to VDD or VSS via a resistor. Digital output: Leave open. Segment output: Leave open.
P80 to P86		Input: Independently connect to VDD or VSS via a resistor. Output: Leave open.
P121 to P124	Input	Independently connect to VDD or VSS via a resistor.
P125 to P127	I/O	Digital input invalid: Leave open. Input: Independently connect to VDD or VSS via a resistor. Output: Leave open. LCD function mode: Leave open.
P137	Input	Independently connect to VDD or VSS via a resistor.
P150, P151	I/O	Input: Independently connect to AVDD or AVSS via a resistor. Output: Leave open.
$\overline{\text{RESET}}$	Input	Connect to VDD directly or via a resistor.
REGC	—	Connect to VSS via a capacitor (0.47 to 1 μF).
COM0 to COM7	Output	Leave open.
VL1, VL2, VL4	—	Leave open.

2.4 Pin Block Diagrams

For the pin types listed in **2.1.1** to **2.1.4**, pin block diagrams are shown in **Figure 2 - 1** to **Figure 2 - 18**.

Figure 2 - 1 Pin Block Diagram of Pin Type 2-1-1

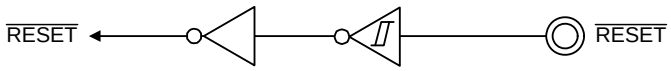


Figure 2 - 2 Pin Block Diagram of Pin Type 2-1-2

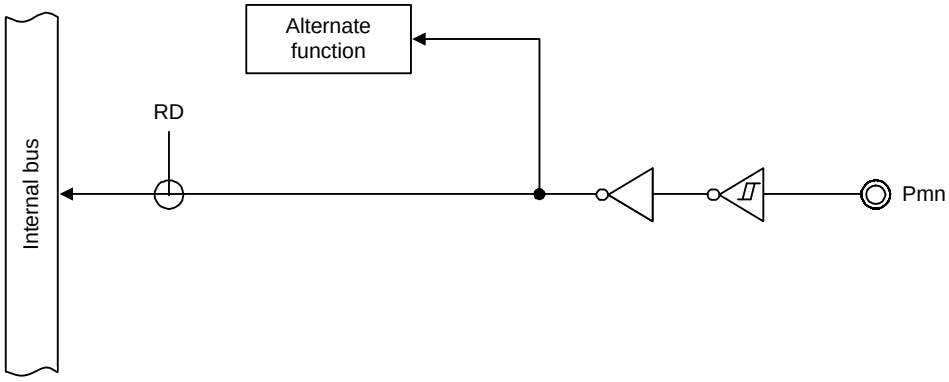
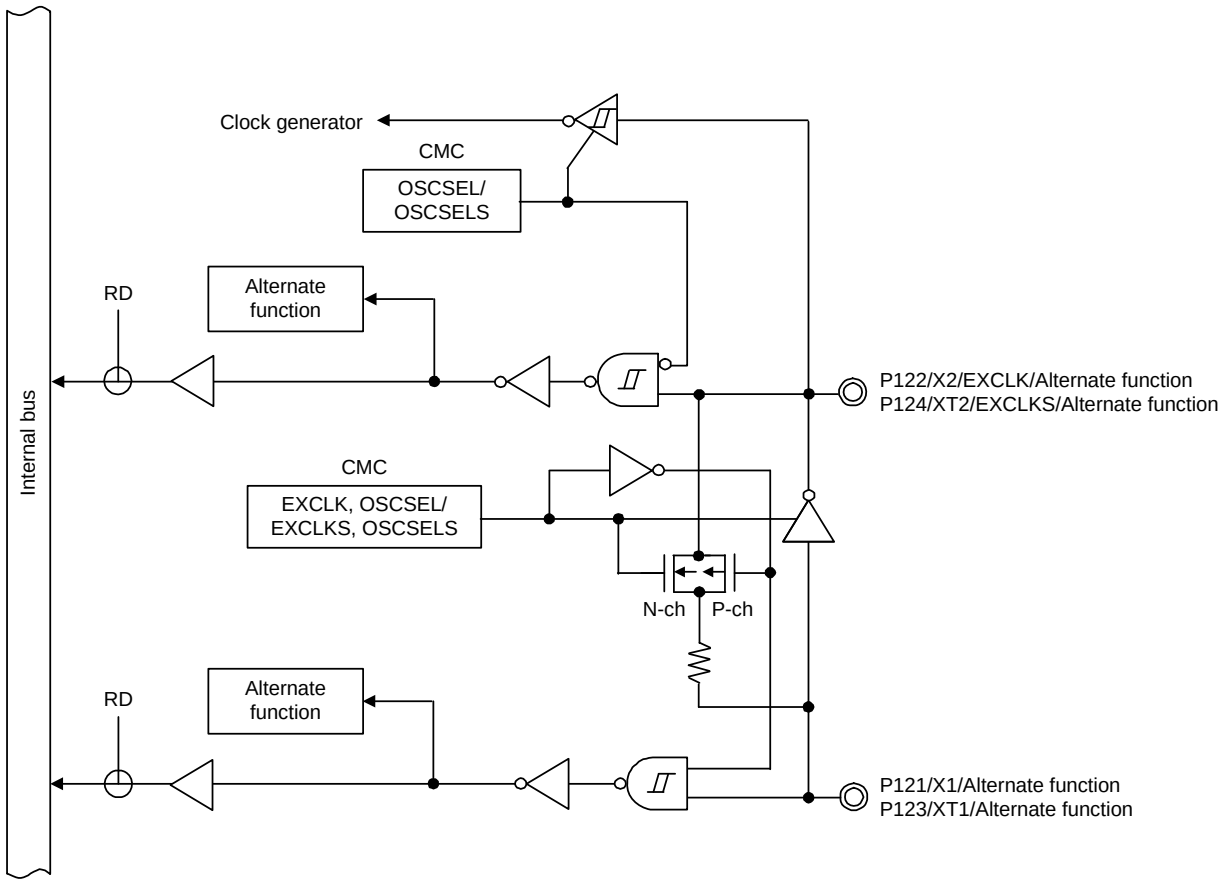
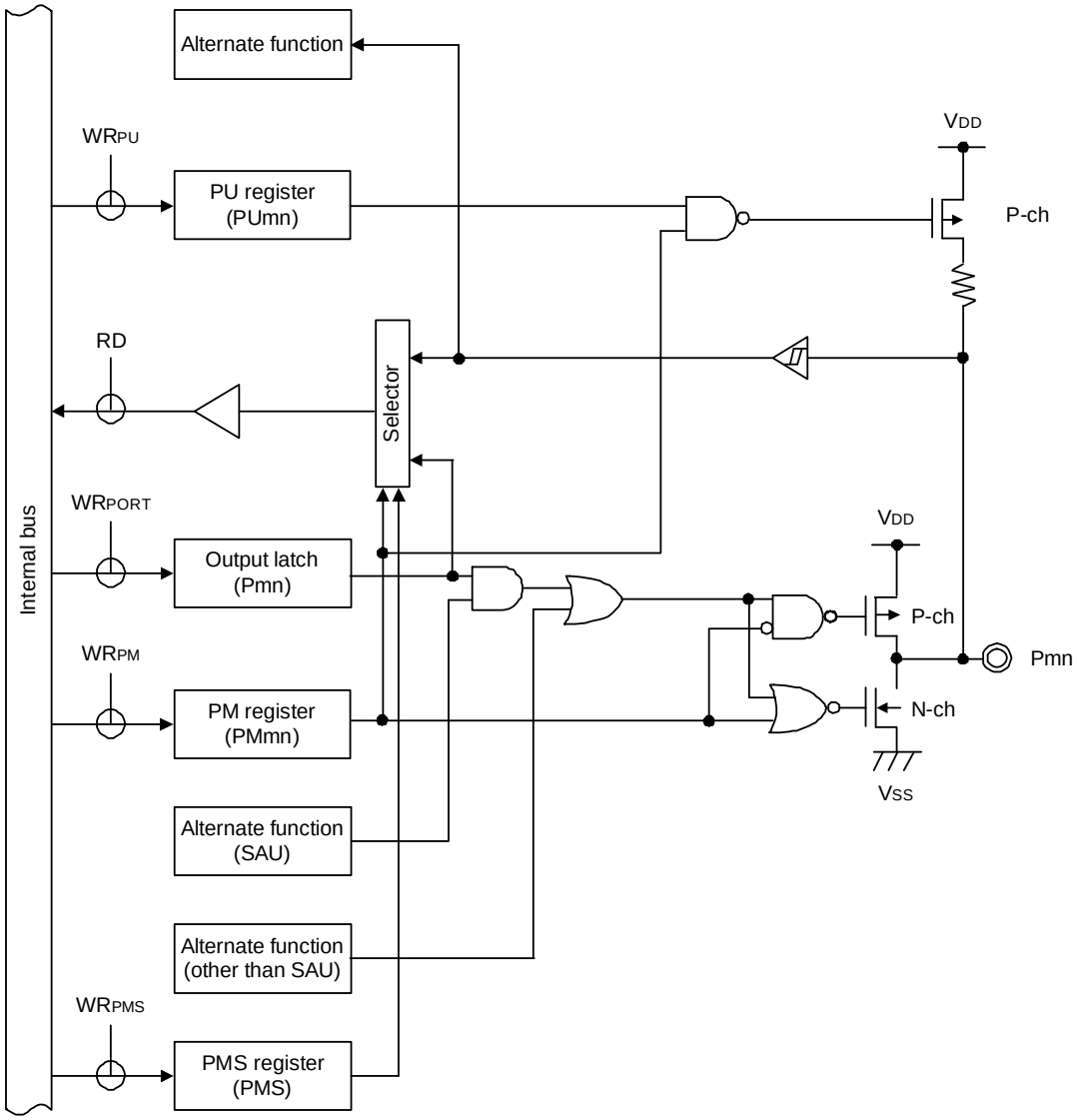


Figure 2 - 3 Pin Block Diagram of Pin Type 2-2-1



Remark Refer to **2.1 Port Function** for alternate functions.

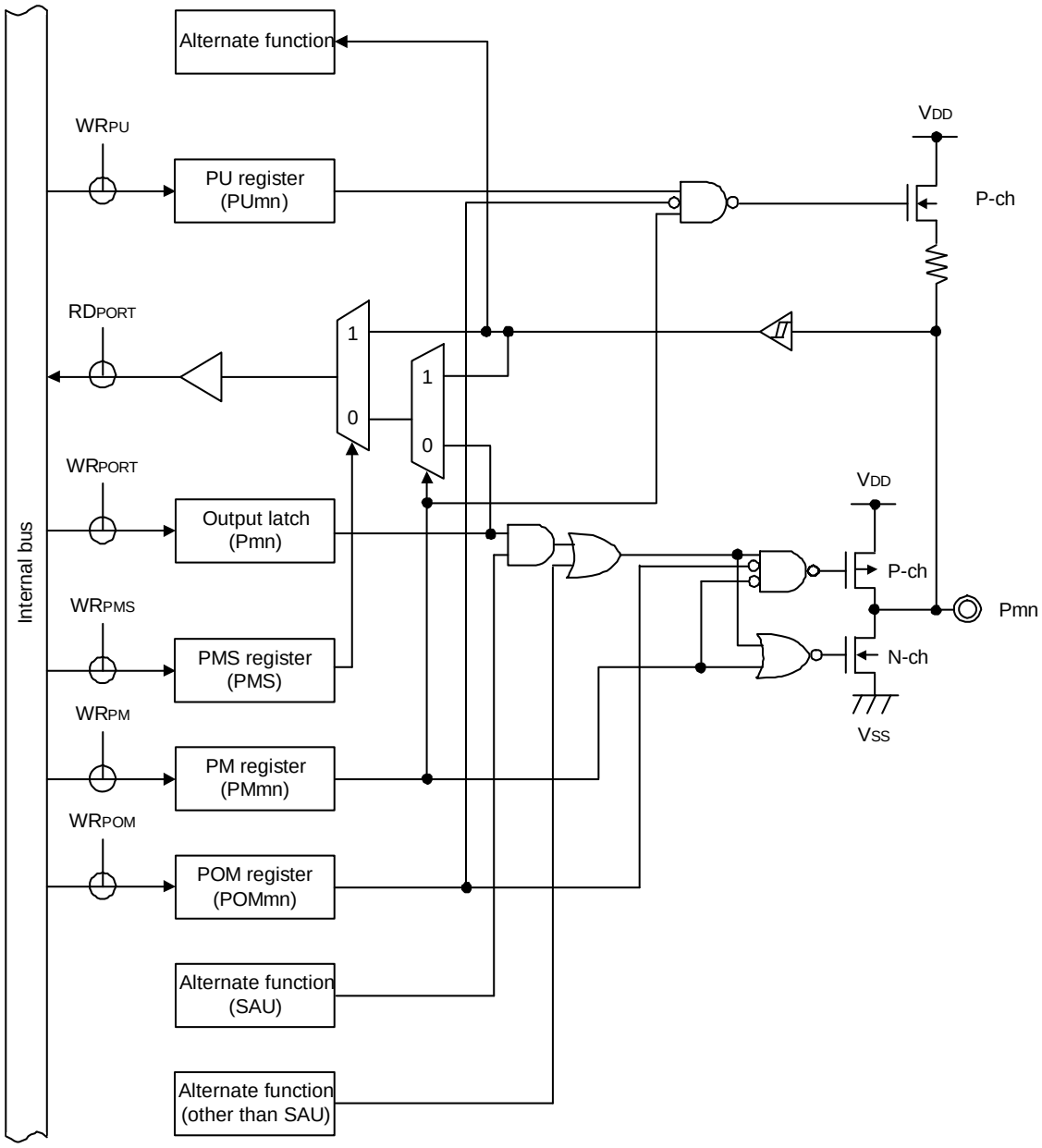
Figure 2 - 4 Pin Block Diagram of Pin Type 7-1-3



Caution In the case of the R5F11R, VDD and VSS in the above figure should be read as AVDD and AVSS, respectively, for P20 to P27, P150, and P151.

Remark 1. Refer to **2.1 Port Function** for alternate functions.
Remark 2. SAU: Serial array unit

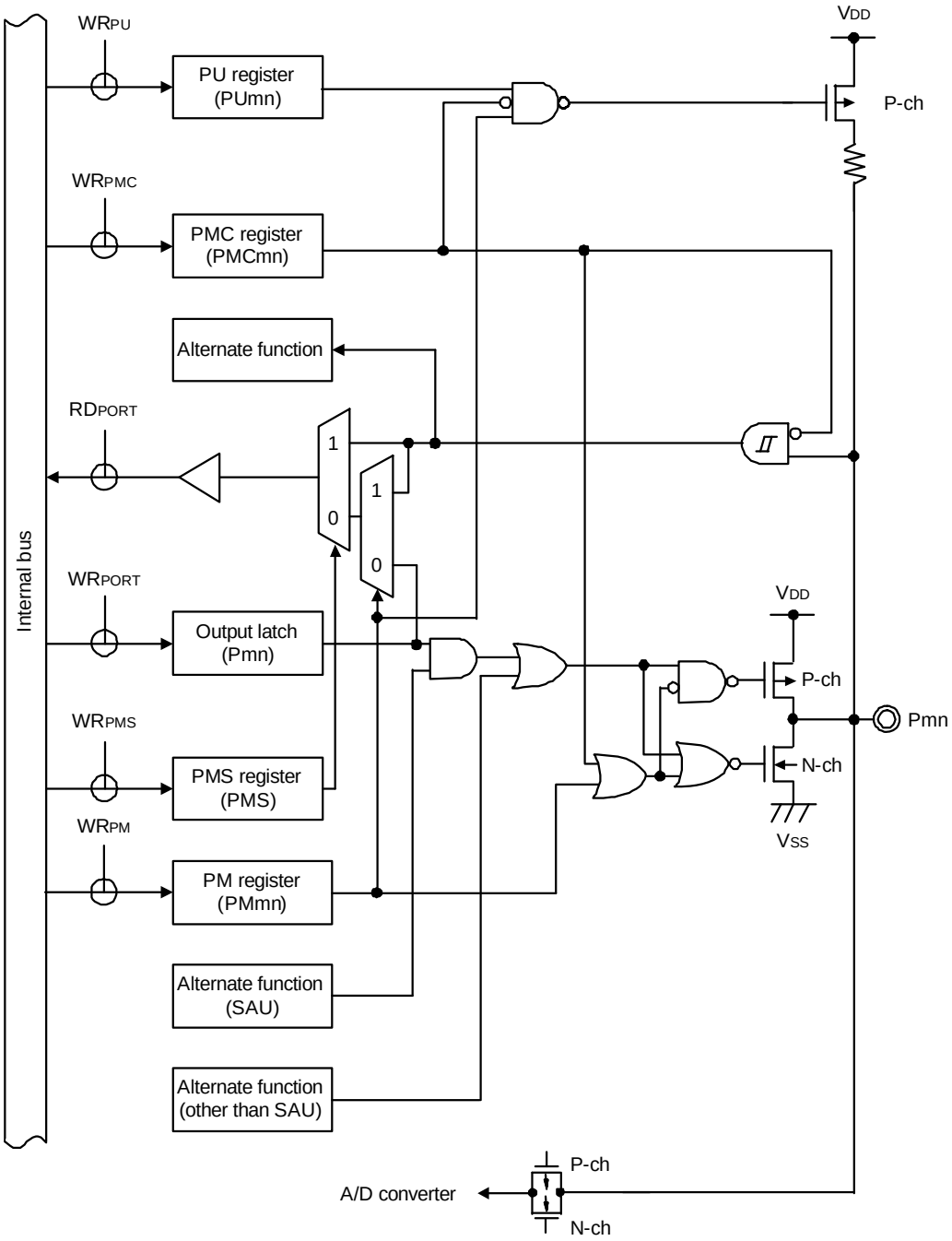
Figure 2 - 5 Pin Block Diagram of Pin Type 7-1-4



Caution The input buffer is enabled even if the type 7-1-4 pin is operating as an output when the N-ch open drain output mode is selected by the corresponding bit in the port output mode register (POMxx). This may lead to a through current flowing through the type 7-1-4 pin when the voltage level on this pin is intermediate.

Remark 1. Refer to **2.1 Port Function** for alternate functions.
Remark 2. SAU: Serial array unit

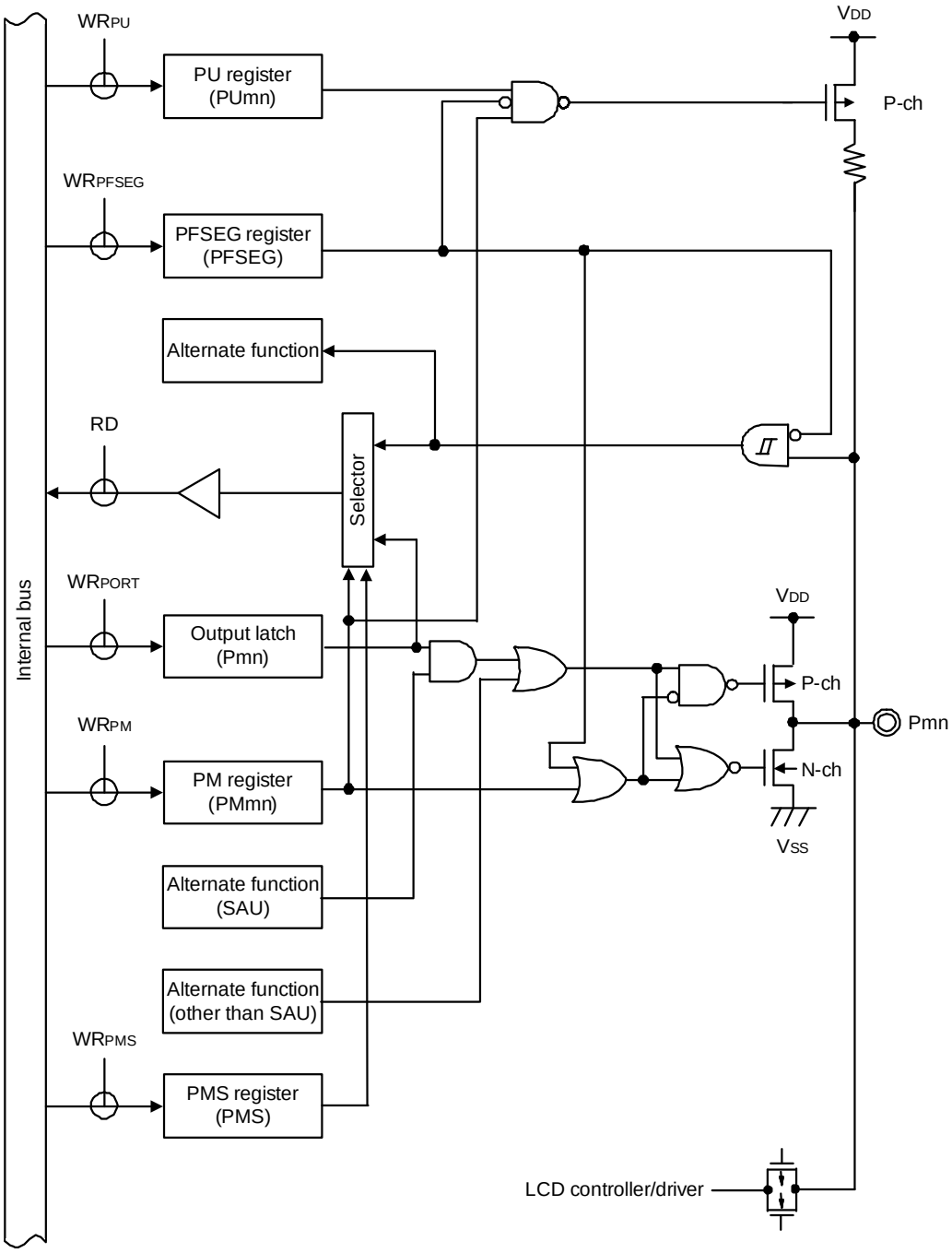
Figure 2 - 6 Pin Block Diagram of Pin Type 7-3-3



Remark 1. Refer to **2.1 Port Function** for alternate functions.

Remark 2. SAU: Serial array unit

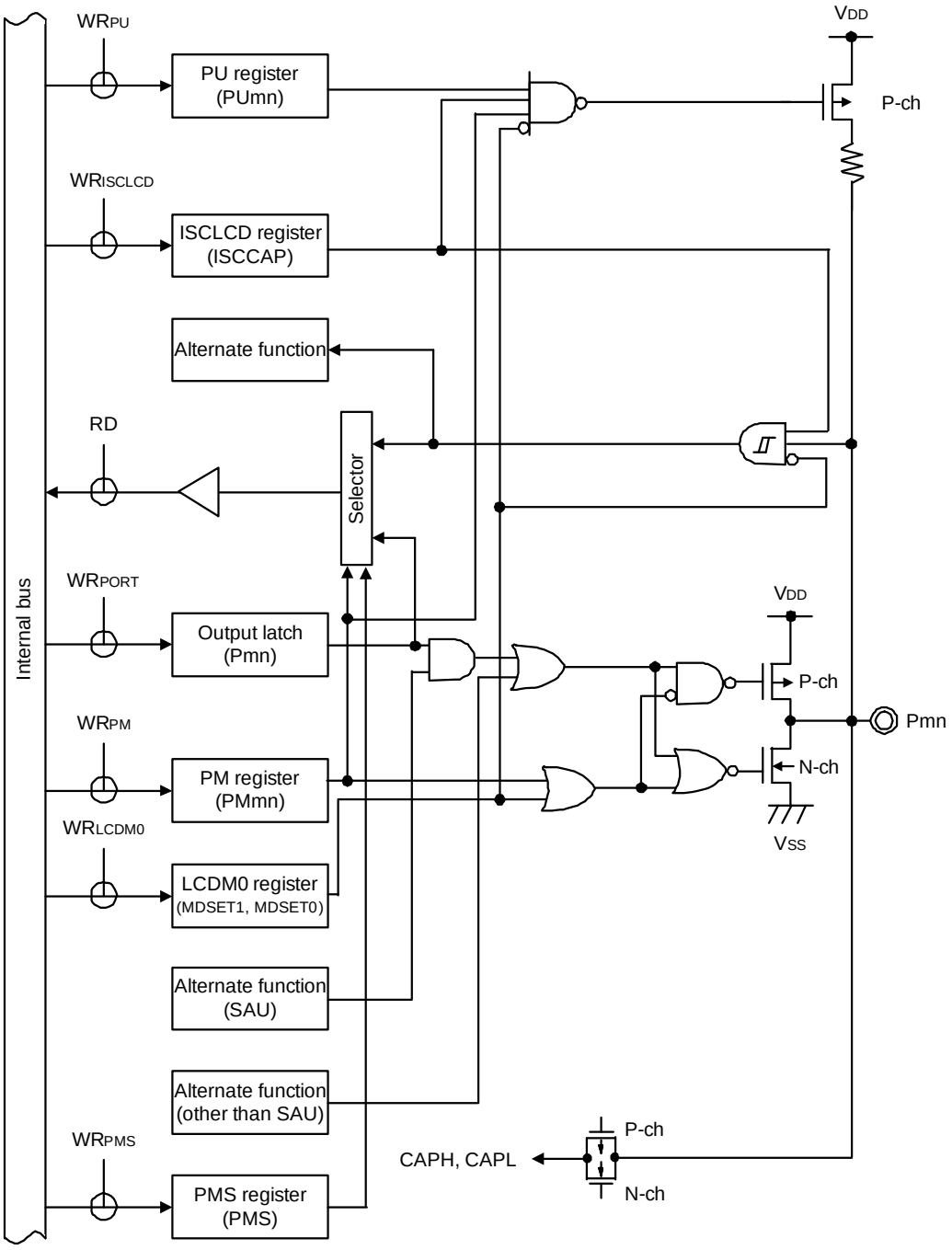
Figure 2 - 7 Pin Block Diagram of Pin Type 7-5-4



Remark 1. Refer to **2.1 Port Function** for alternate functions.

Remark 2. SAU: Serial array unit

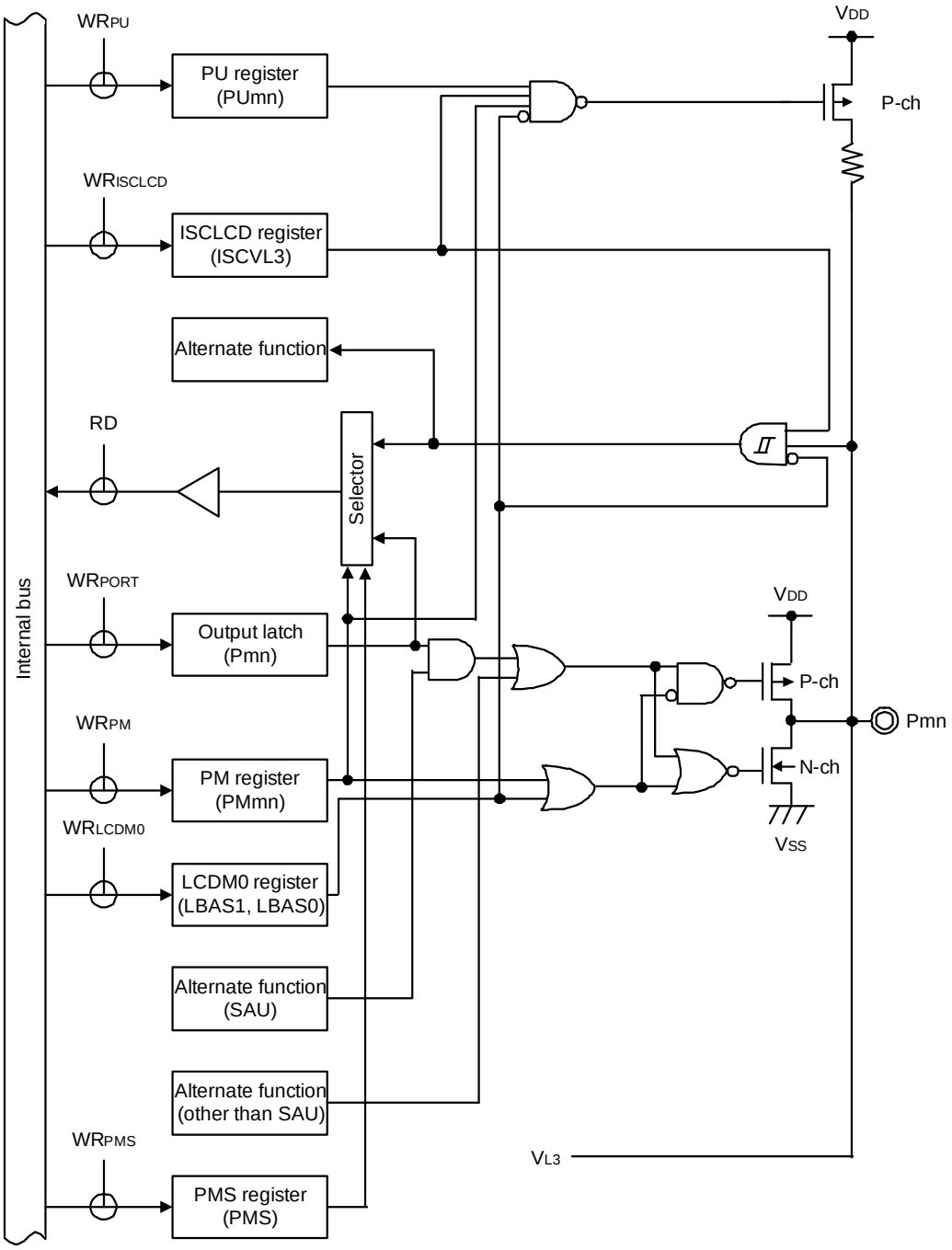
Figure 2 - 8 Pin Block Diagram of Pin Type 7-5-5



Remark 1. Refer to **2.1 Port Function** for alternate functions.

Remark 2. SAU: Serial array unit

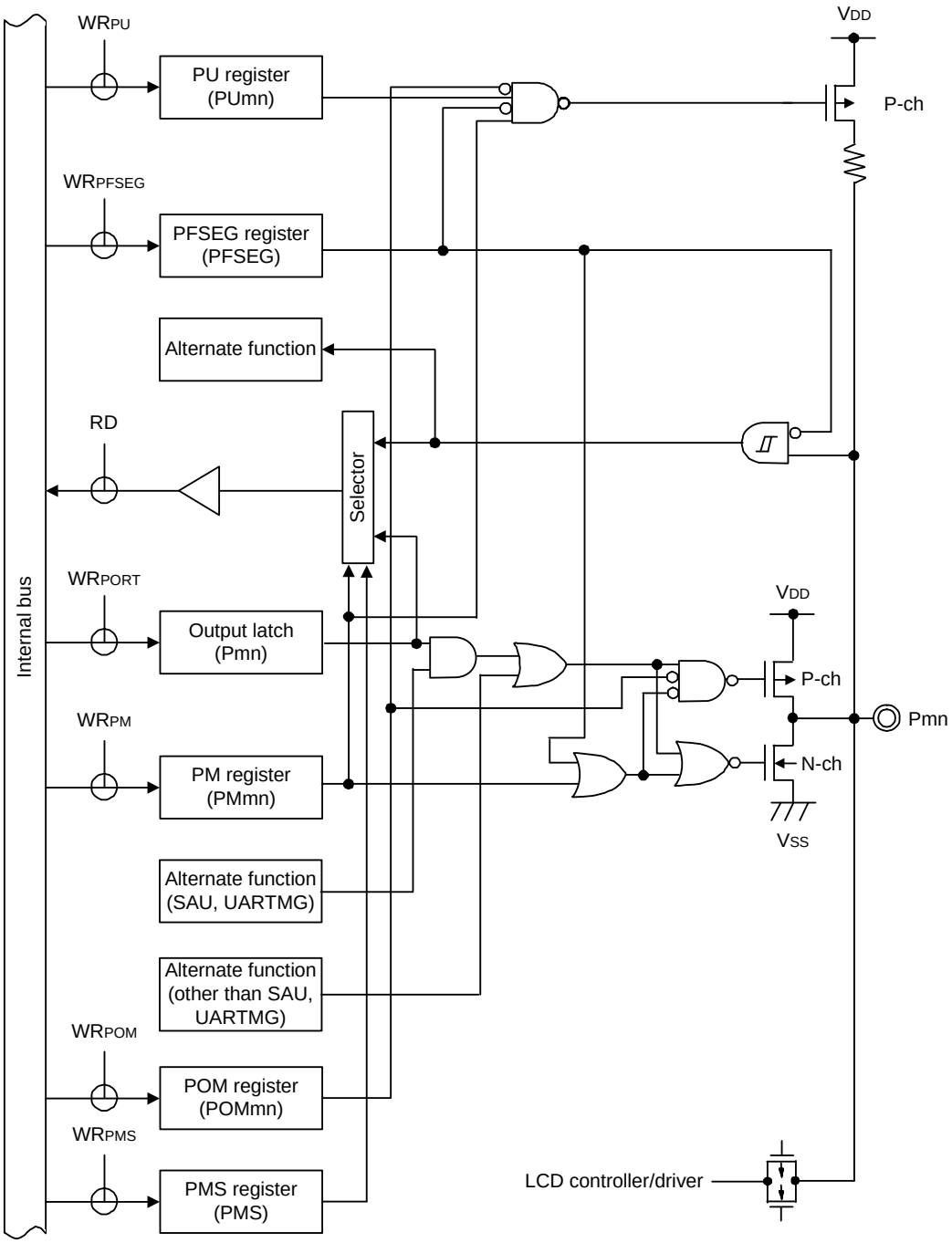
Figure 2 - 9 Pin Block Diagram of Pin Type 7-5-6



Remark 1. Refer to **2.1 Port Function** for alternate functions.

Remark 2. SAU: Serial array unit

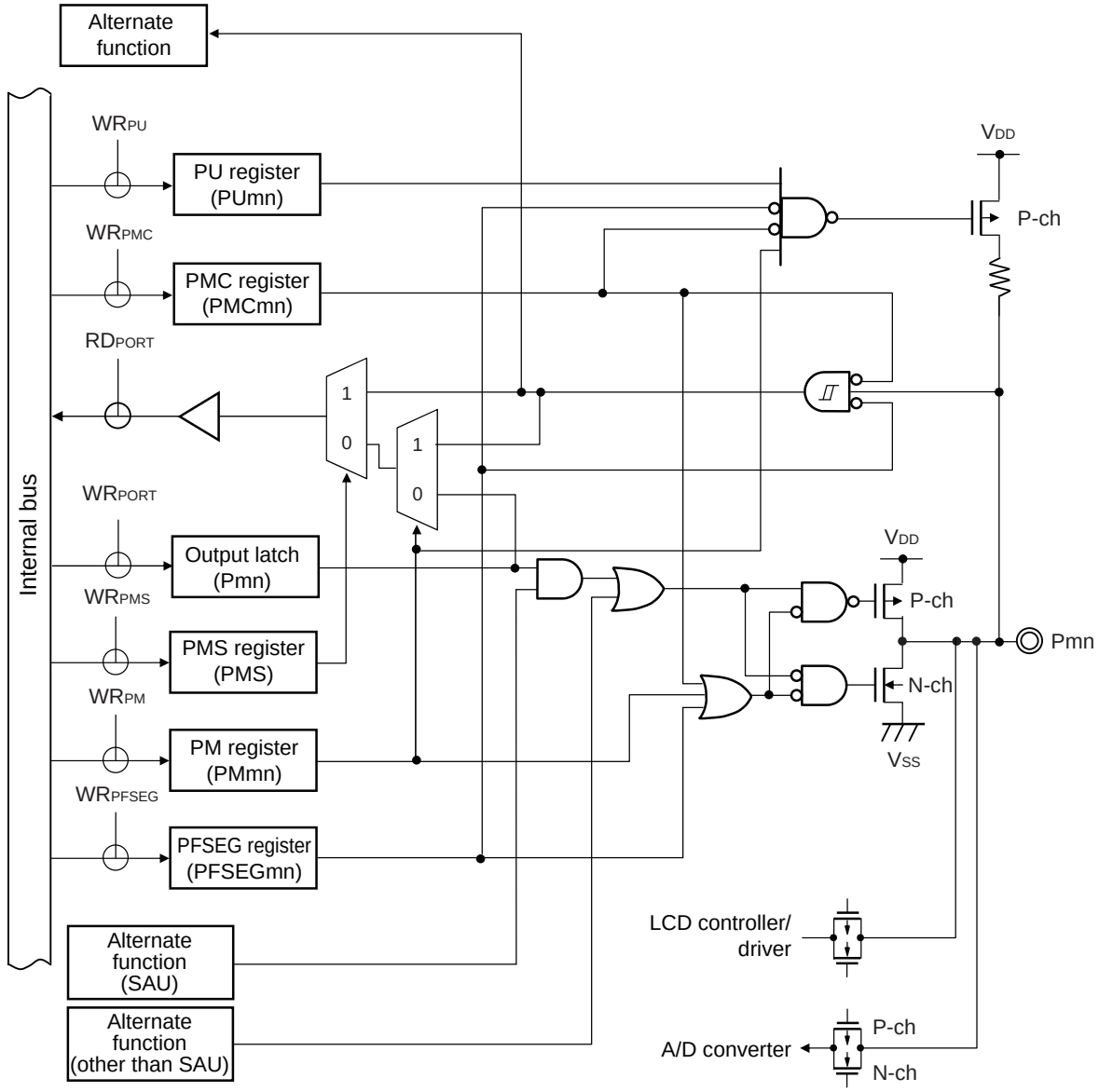
Figure 2 - 10 Pin Block Diagram of Pin Type 7-5-10



Caution The input buffer is enabled even if the type 7-5-10 pin is operating as an output when the N-ch open drain output mode is selected by the corresponding bit in the port output mode register (POMxx). This may lead to a through current flowing through the type 7-5-10 pin when the voltage level on this pin is intermediate.

Remark 1. Refer to **2.1 Port Function** for alternate functions.
Remark 2. SAU: Serial array unit
Remark 3. UARTMG: Serial interface UARTMG (R5F11R only)

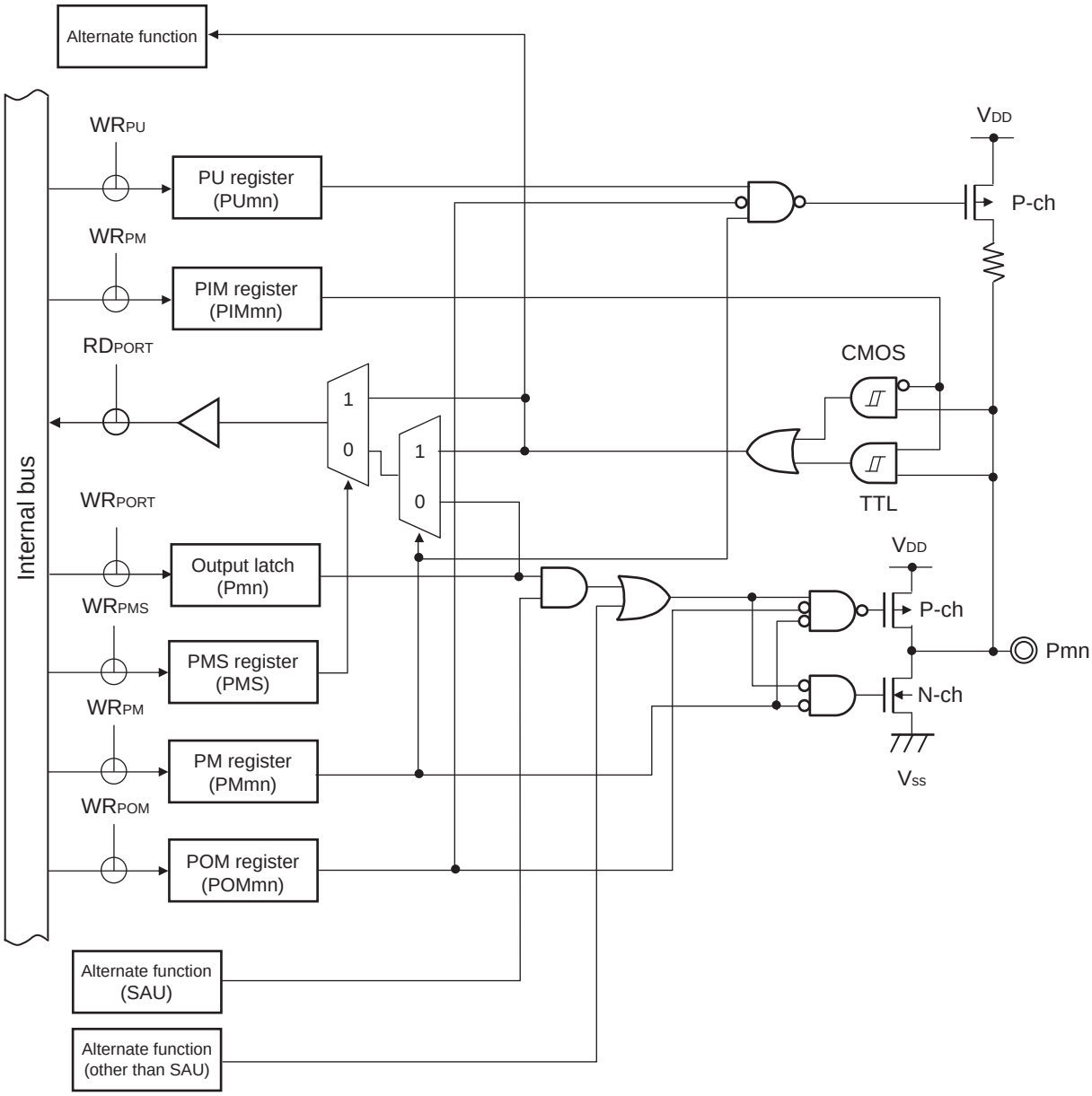
Figure 2 - 11 Pin Block Diagram of Pin Type 7-10-3



Remark 1. Refer to **2.1 Port Function** for alternate functions.

Remark 2. SAU: Serial array unit

Figure 2 - 12 Pin Block Diagram of Pin Type 8-1-4



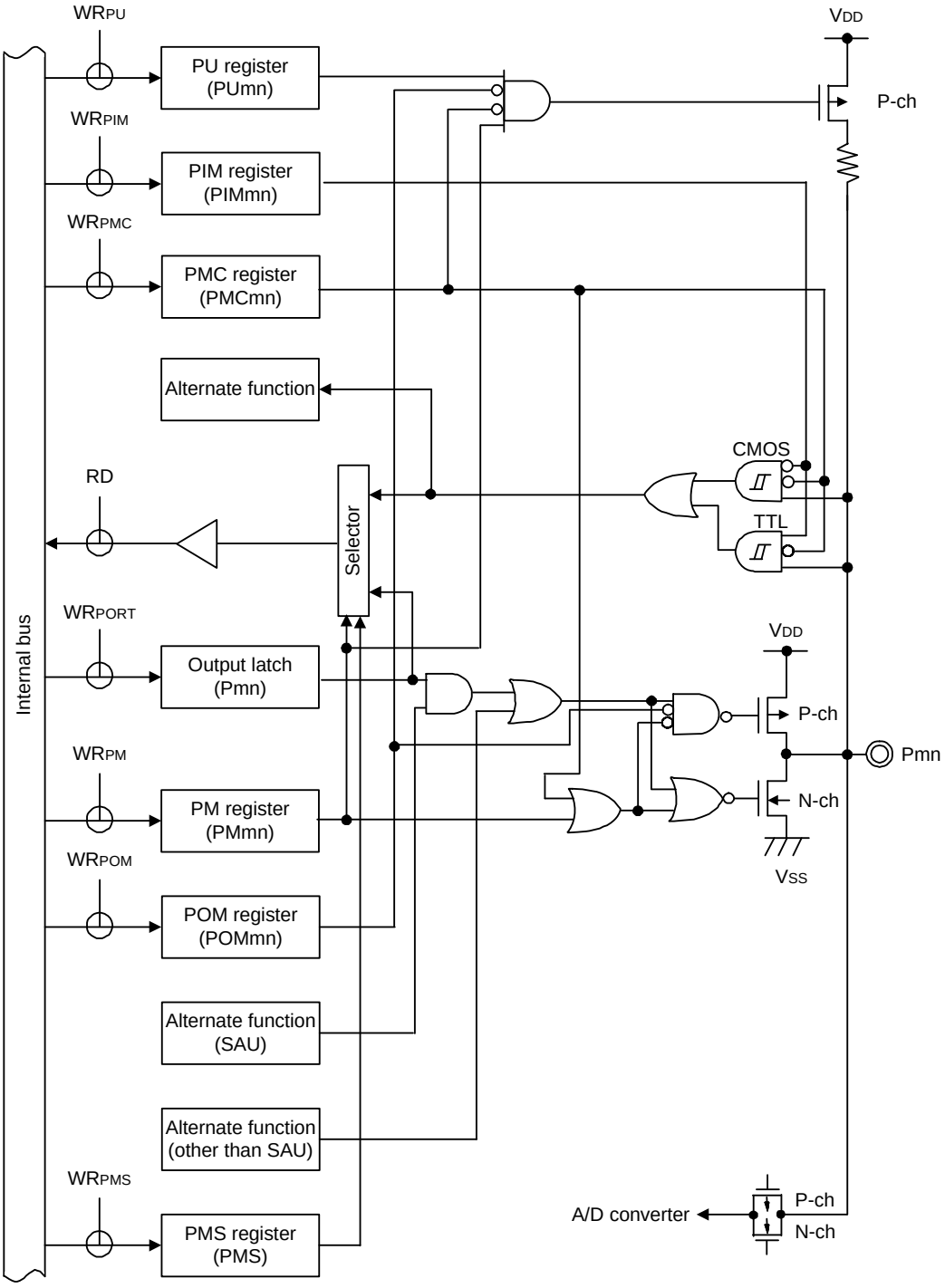
Caution 1. The input buffer is enabled even if the type 8-1-4 pin is operating as an output when the N-ch open drain output mode is selected by the corresponding bit in the port output mode register (POMxx). This may lead to a through current flowing through the type 8-1-4 pin when the voltage level on this pin is intermediate.

Caution 2. When the type 8-1-4 pin is set to TTL input buffer by the corresponding bit in the port input mode register (PIMxx) and is driven high, a through current may flow through the type 8-1-4 pin due to the configuration of the TTL input buffer. Drive the type 8-1-4 pin low to prevent the through current.

Remark 1. Refer to **2.1 Port Function** for alternate functions.

Remark 2. SAU: Serial array unit

Figure 2 - 13 Pin Block Diagram of Pin 8-3-4



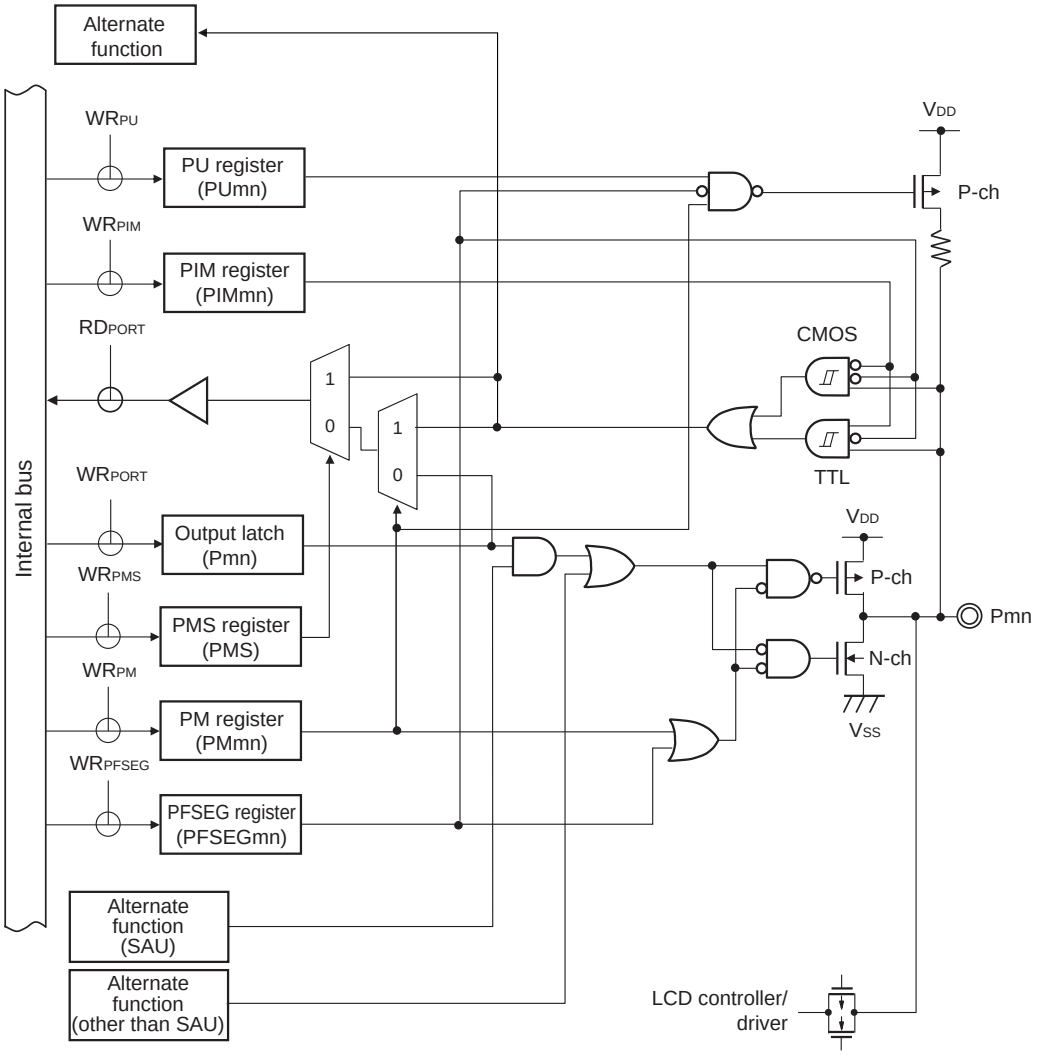
Caution 1. The input buffer is enabled even if the type 8-3-4 pin is operating as an output when the N-ch open drain output mode is selected by the corresponding bit in the port output mode register (POMxx). This may lead to a through current flowing through the type 8-3-4 pin when the voltage level on this pin is intermediate.

Caution 2. When the type 8-3-4 pin is set to TTL input buffer by the corresponding bit in the port input mode register (PIMxx) and is driven high, a through current may flow through the type 8-3-4 pin due to the configuration of the TTL input buffer. Drive the type 8-3-4 pin low to prevent the through current.

Remark 1. Refer to **2.1 Port Function** for alternate functions.

Remark 2. SAU: Serial array unit

Figure 2 - 14 Pin Block Diagram of Pin 8-5-4

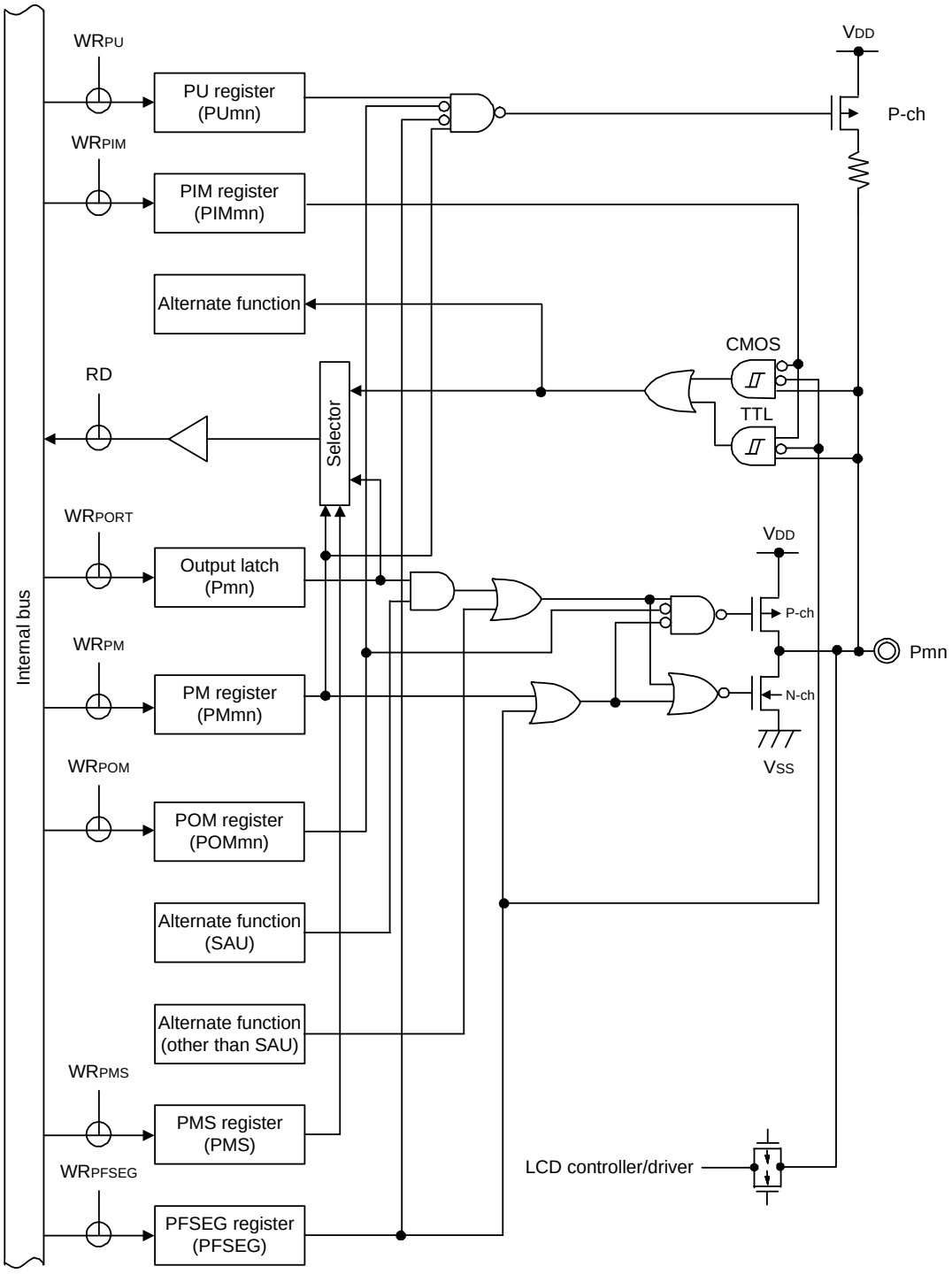


Caution When the type 8-5-4 pin is set to TTL input buffer by the corresponding bit in the port input mode register (PIMxx) and is driven high, a through current may flow through the type 8-5-4 pin due to the configuration of the TTL input buffer. Drive the type 8-5-4 pin low to prevent the through current.

Remark 1. Refer to **2.1 Port Function** for alternate functions.

Remark 2. SAU: Serial array unit

Figure 2 - 15 Pin Block Diagram of Pin Type 8-5-10



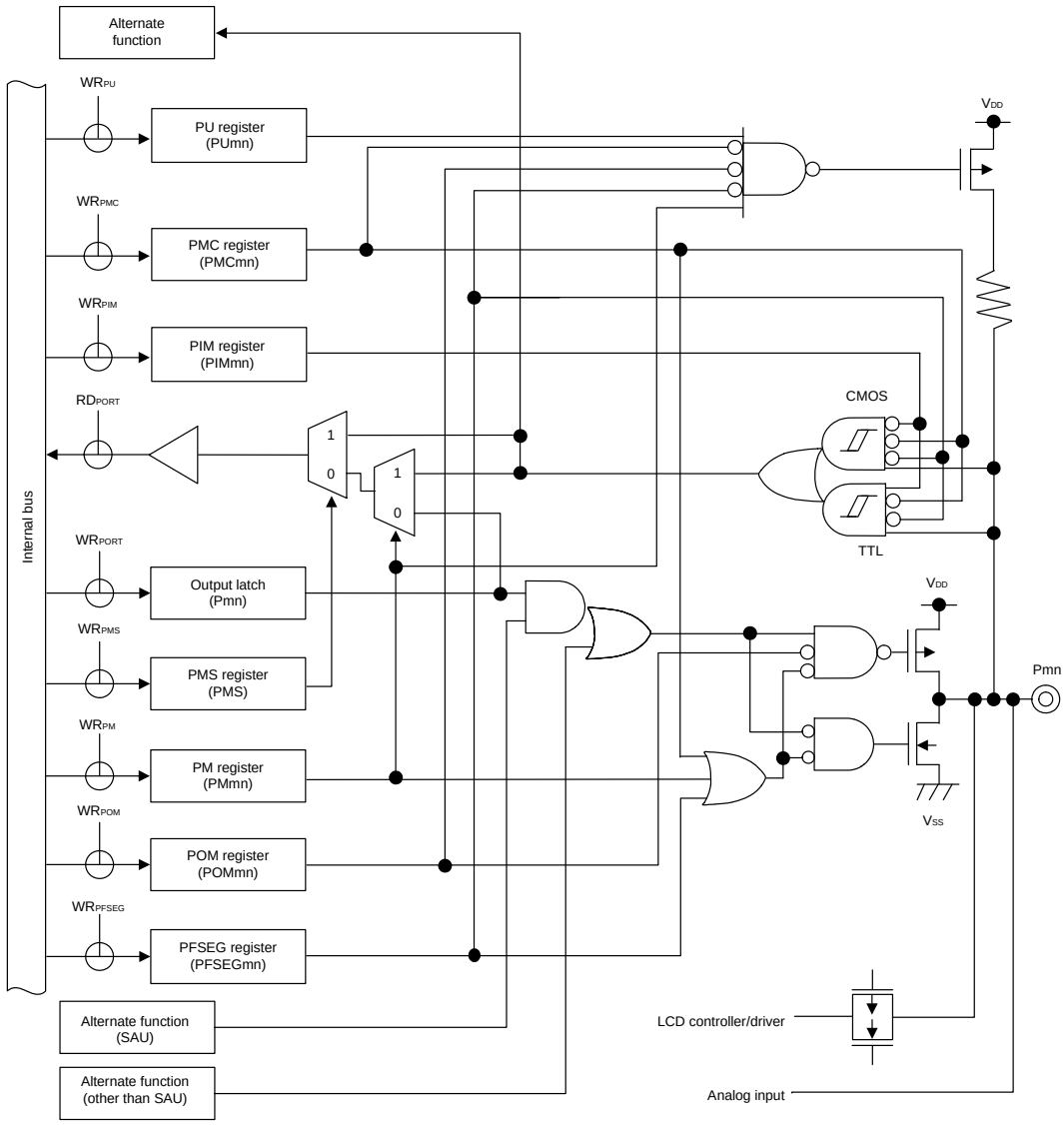
Caution 1. The input buffer is enabled even if the type 8-5-10 pin is operating as an output when the N-ch open drain output mode is selected by the corresponding bit in the port output mode register (POMxx). This may lead to a through current flowing through the type 8-5-10 pin when the voltage level on this pin is intermediate.

Caution 2. When the type 8-5-10 pin is set to TTL input buffer by the corresponding bit in the port input mode register (PIMxx) and is driven high, a through current may flow through the type 8-5-10 pin due to the configuration of the TTL input buffer. Drive the type 8-5-10 pin low to prevent the through current.

Remark 1. Refer to **2.1 Port Function** for alternate functions.

Remark 2. SAU: Serial array unit

Figure 2 - 16 Pin Block Diagram of Pin Type 8-5-13



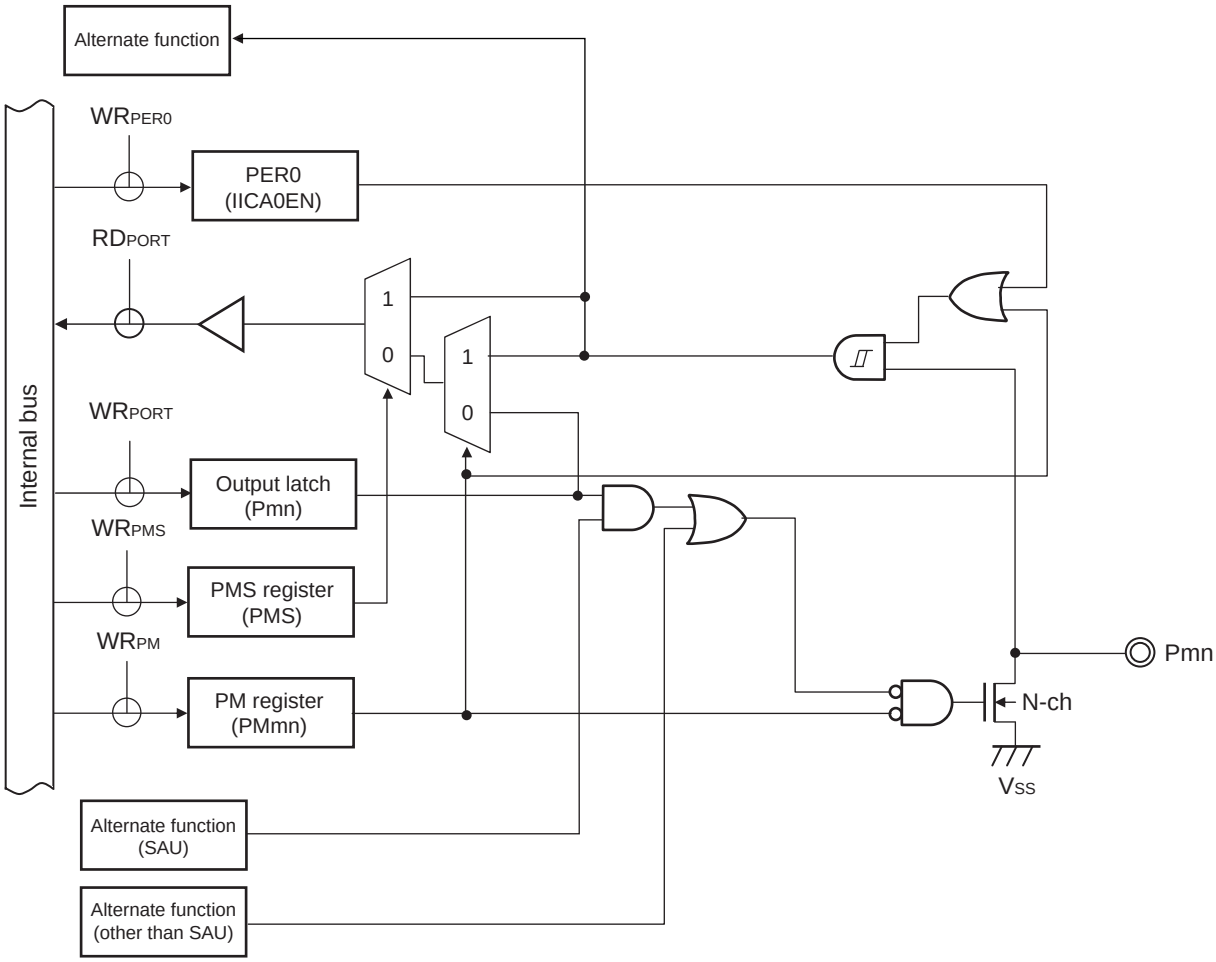
Caution 1. The input buffer is enabled even if the type 8-5-13 pin is operating as an output when the N-ch open drain output mode is selected by the corresponding bit in the port output mode register (POMxx). This may lead to a through current flowing through the type 8-5-13 pin when the voltage level on this pin is intermediate.

Caution 2. When the type 8-5-13 pin is set to TTL input buffer by the corresponding bit in the port input mode register (PIMxx) and is driven high, a through current may flow through the type 8-5-13 pin due to the configuration of the TTL input buffer. Drive the type 8-5-13 pin low to prevent the through current.

Remark 1. Refer to **2.1 Port Function** for alternate functions.

Remark 2. SAU: Serial array unit

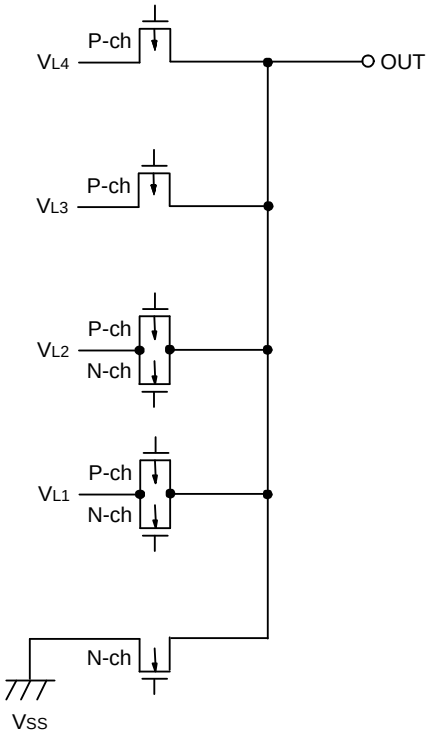
Figure 2 - 17 Pin Block Diagram of Pin 12-1-3



Remark 1. Refer to **2.1 Port Function** for alternate functions.

Remark 2. SAU: Serial array unit

Figure 2 - 18 Pin Block Diagram of Pin Type 18-5-1



CHAPTER 3 CPU ARCHITECTURE

3.1 Overview

The CPU core in the RL78 microcontroller employs the Harvard architecture which has independent instruction fetch bus, address bus and data bus. In addition, through the adoption of three-stage pipeline control of fetch, decode, and memory access, the operation efficiency is remarkably improved over the conventional CPU core. The CPU core features high performance and highly functional instruction processing, and can be suited for use in various applications that require high speed and highly functional processing.

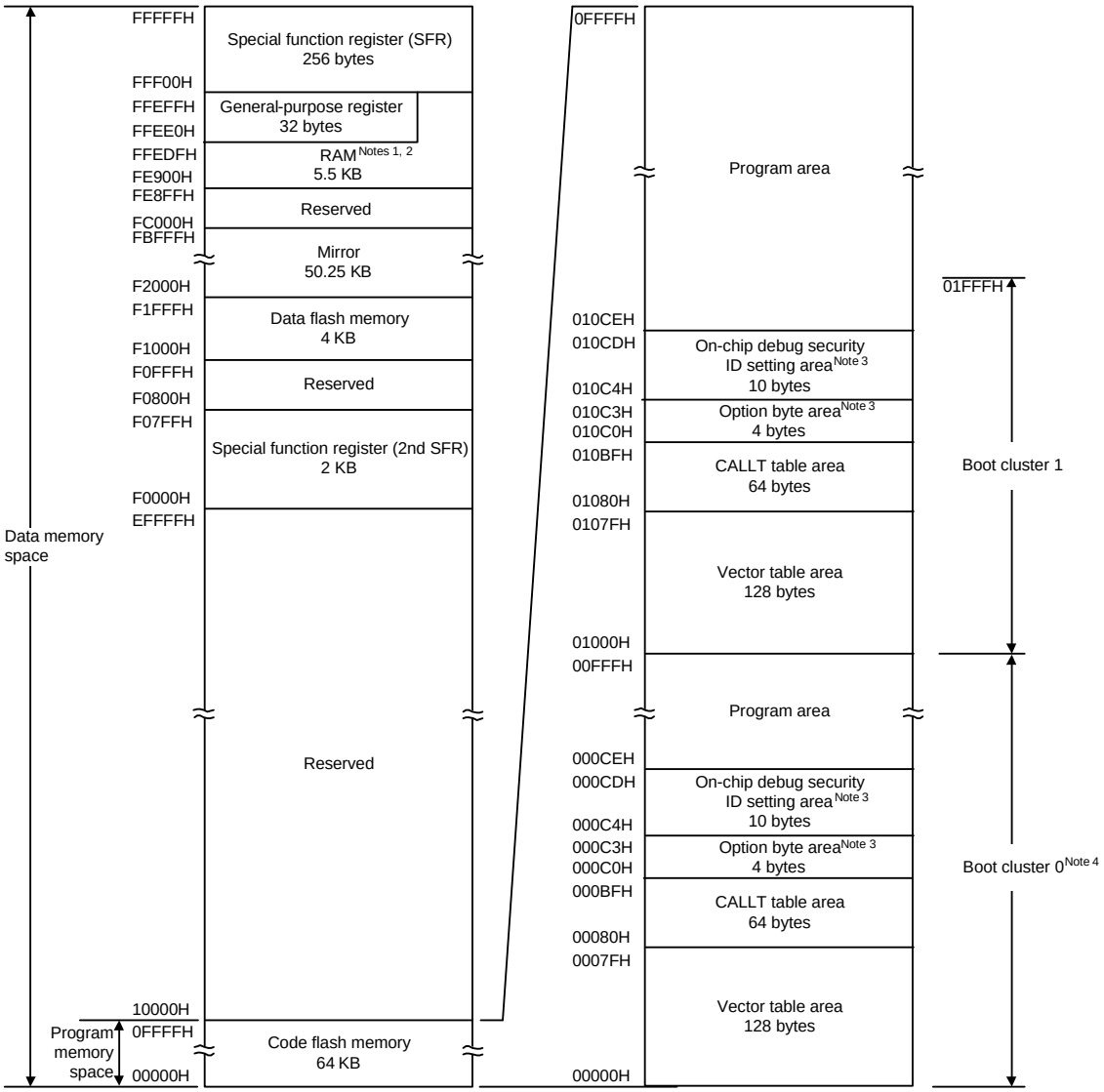
The RL78/H1D integrates the RL78-S3 core that has the following features.

- 3-stage pipeline CISC architecture
- Address space: 1 MB
- Minimum instruction execution time: One instruction per clock cycle
- General-purpose registers: Eight 8-bit registers
- Type of instruction: 81
- Data allocation: Little endian
- Multiply/divide and multiply/accumulate instructions: Supported

3.2 Memory Space

Products in the RL78/H1D can access a 1 MB memory space. Figures 3 - 1 to 3 - 4 show the memory maps.

Figure 3 - 1 Memory Map (R5F11NME)



Note 1. Do not allocate the stack area, data buffers for use by the flash library, arguments of library functions, branch destinations in the processing of vectored interrupts, or destinations or sources for DTC transfer to the area from FFE20H to FFEDFH when performing self-programming or rewriting of the data flash memory.

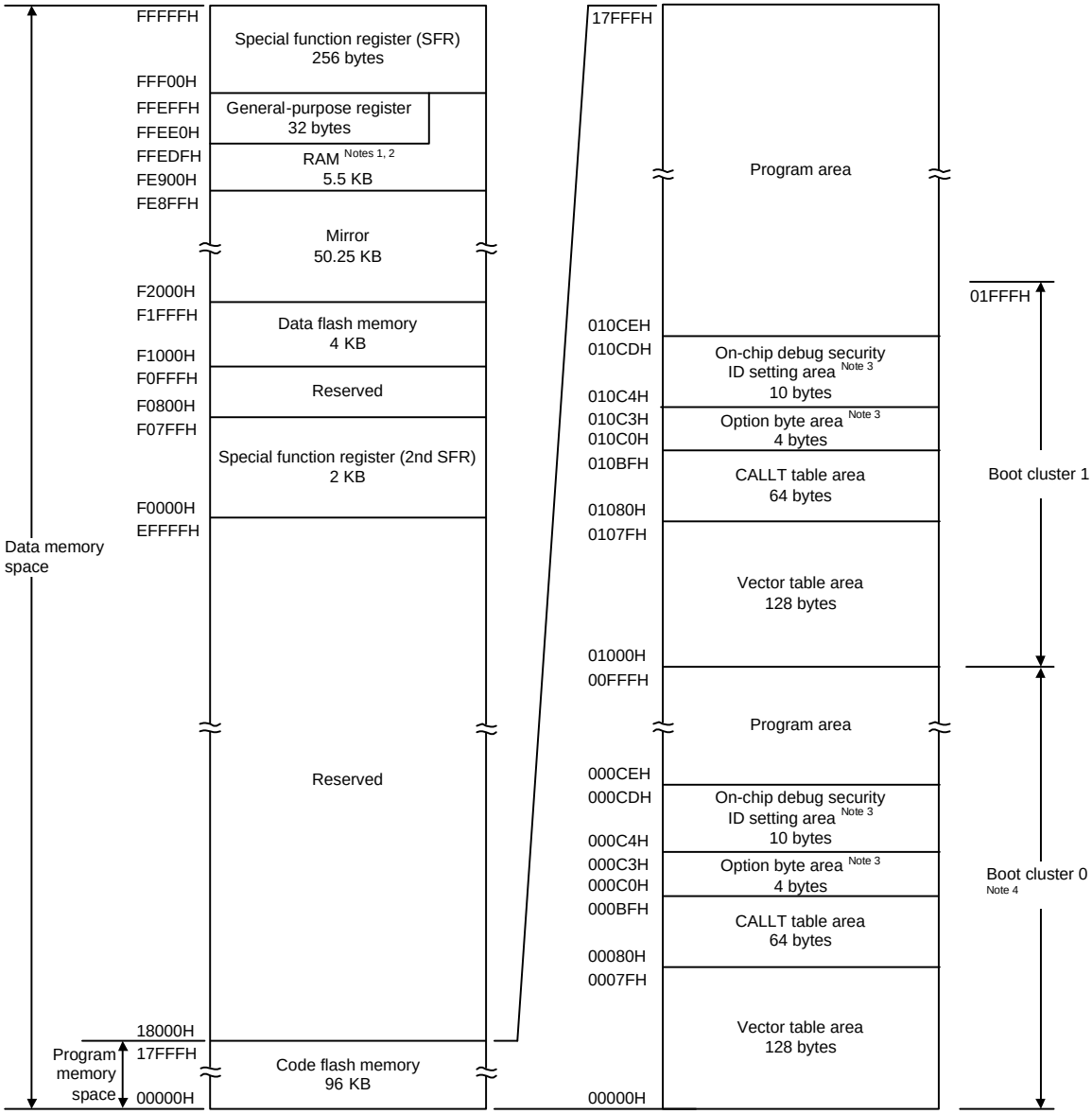
Note 2. Instructions can be executed from the RAM area excluding the general-purpose register area.

Note 3. When boot swap is not used: Set the option bytes to 000C0H to 000C3H, and the on-chip debug security IDs to 000C4H to 000CDH.
When boot swap is used: Set the option bytes to 000C0H to 000C3H and 010C0H to 010C3H, and the on-chip debug security IDs to 000C4H to 000CDH and 010C4H to 010CDH.

Note 4. Writing boot cluster 0 can be prohibited depending on the setting of security (see **34.7 Security Settings**).

Caution While RAM parity error resets are enabled (RPERDIS = 0), be sure to initialize RAM areas where data access is to proceed and the RAM area + 10 bytes when instructions are fetched from RAM areas, respectively.
Reset signal generation sets RAM parity error resets to enabled (RPERDIS = 0). For details, see 31.3.3 RAM parity error detection function.

Figure 3 - 2 Memory Map (R5F11xF (x = NG, NL, NM, PL))



Note 1. Do not allocate the stack area, data buffers for use by the flash library, arguments of library functions, branch destinations in the processing of vectored interrupts, or destinations or sources for DTC transfer to the area from FFE20H to FFEDFH when performing self-programming or rewriting of the data flash memory.

Note 2. Instructions can be executed from the RAM area excluding the general-purpose register area.

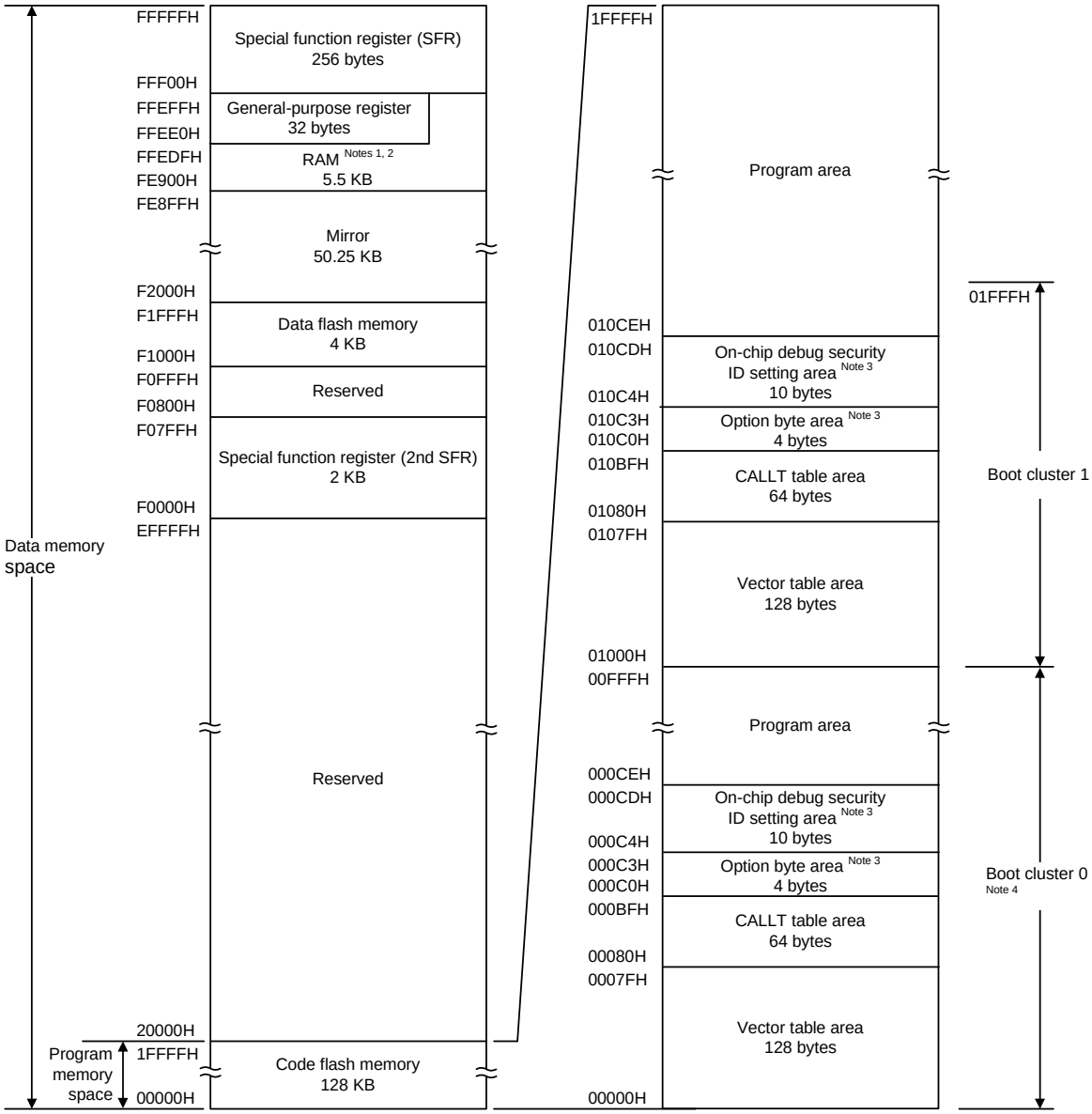
Note 3. When boot swap is not used: Set the option bytes to 000C0H to 000C3H, and the on-chip debug security IDs to 000C4H to 000CDH.

When boot swap is used: Set the option bytes to 000C0H to 000C3H and 010C0H to 010C3H, and the on-chip debug security IDs to 000C4H to 000CDH and 010C4H to 010CDH.

Note 4. Writing boot cluster 0 can be prohibited depending on the setting of security (see **34.7 Security Settings**).

Caution While RAM parity error resets are enabled (RPERDIS = 0), be sure to initialize RAM areas where data access is to proceed and the RAM area + 10 bytes when instructions are fetched from RAM areas, respectively.
Reset signal generation sets RAM parity error resets to enabled (RPERDIS = 0). For details, see 31.3.3 RAM parity error detection function.

Figure 3 - 3 Memory Map (R5F11xG (x = NG, NL, NM, PL))



Note 1. Do not allocate the stack area, data buffers for use by the flash library, arguments of library functions, branch destinations in the processing of vectored interrupts, or destinations or sources for DTC transfer to the area from FFE20H to FFEDFH when performing self-programming or rewriting of the data flash memory.

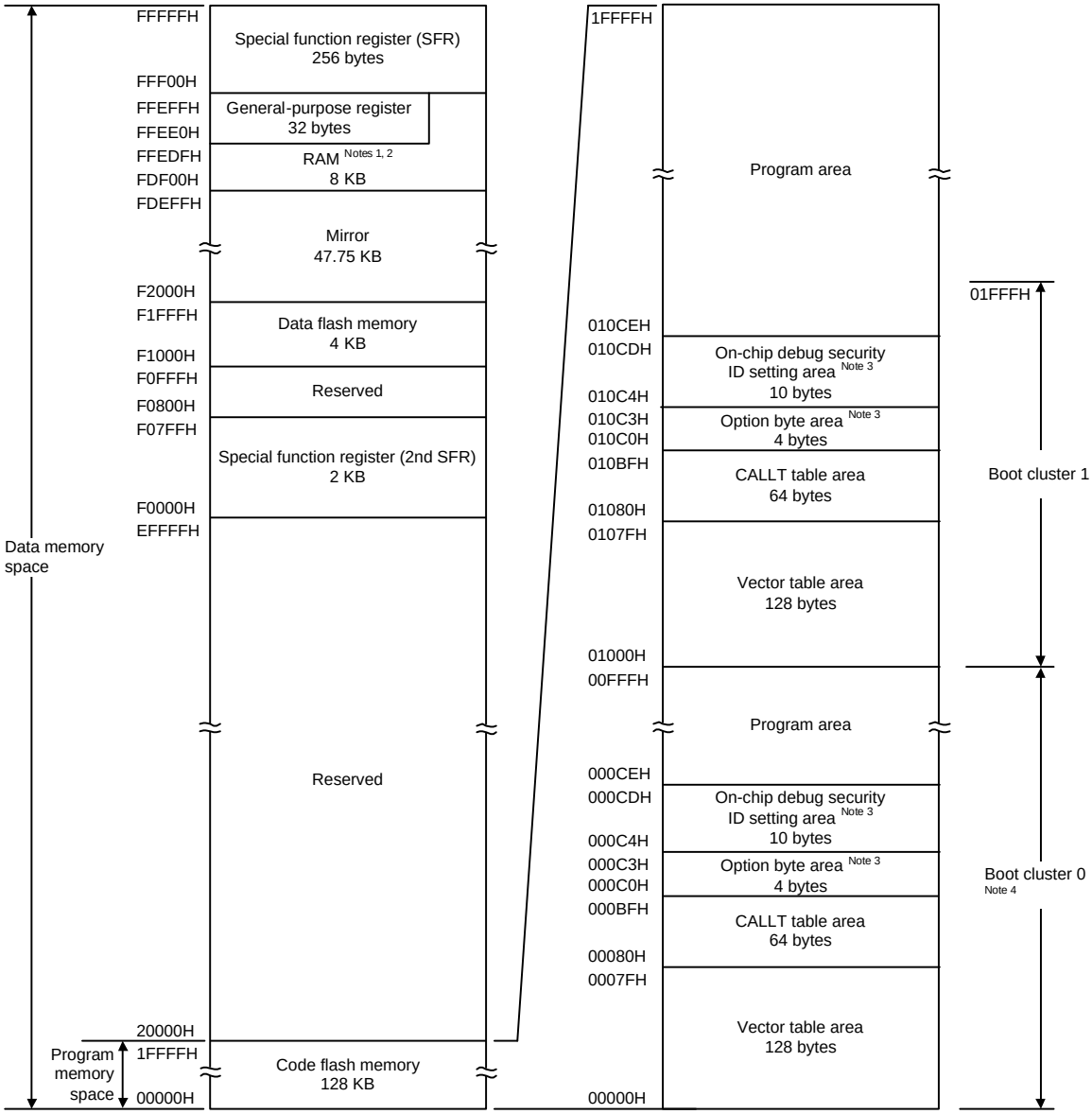
Note 2. Instructions can be executed from the RAM area excluding the general-purpose register area.

Note 3. When boot swap is not used: Set the option bytes to 000C0H to 000C3H, and the on-chip debug security IDs to 000C4H to 000CDH.
When boot swap is used: Set the option bytes to 000C0H to 000C3H and 010C0H to 010C3H, and the on-chip debug security IDs to 000C4H to 000CDH and 010C4H to 010CDH.

Note 4. Writing boot cluster 0 can be prohibited depending on the setting of security (see **34.7 Security Settings**).

Caution While RAM parity error resets are enabled (RPERDIS = 0), be sure to initialize RAM areas where data access is to proceed and the RAM area + 10 bytes when instructions are fetched from RAM areas, respectively.
Reset signal generation sets RAM parity error resets to enabled (RPERDIS = 0). For details, see 31.3.3 RAM parity error detection function.

Figure 3 - 4 Memory Map (R5F11RMG)



Note 1. Do not allocate the stack area, data buffers for use by the flash library, arguments of library functions, branch destinations in the processing of vectored interrupts, or destinations or sources for DTC transfer to the area from FFE20H to FFEDFH when performing self-programming or rewriting of the data flash memory. The RAM area used by the flash library starts at FDF00H. For the RAM areas used by the flash library, see **Self RAM list of Flash Self-Programming Library for RL78 Family (R20UT2944)**.

Note 2. Instructions can be executed from the RAM area excluding the general-purpose register area.

Note 3. When boot swap is not used: Set the option bytes to 000C0H to 000C3H, and the on-chip debug security IDs to 000C4H to 000CDH.

When boot swap is used: Set the option bytes to 000C0H to 000C3H and 010C0H to 010C3H, and the on-chip debug security IDs to 000C4H to 000CDH and 010C4H to 010CDH.

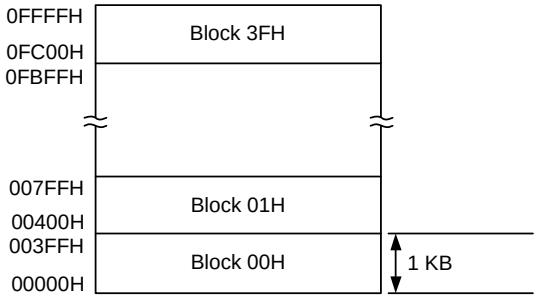
Note 4. Writing boot cluster 0 can be prohibited depending on the setting of security (see **34.7 Security Settings**).

(Cautions and Remark are given on the next page.)

Caution 1. While RAM parity error resets are enabled (RPERDIS = 0), be sure to initialize RAM areas where data access is to proceed and the RAM area + 10 bytes when instructions are fetched from RAM areas, respectively.
Reset signal generation sets RAM parity error resets to enabled (RPERDIS = 0). For details, see 31.3.3 RAM parity error detection function.

Caution 2. Use of the area from FE300H to FE6FFH is prohibited when using the on-chip debug trace function.

Remark The flash memory is divided into blocks (one block = 1 KB). For the address values and block numbers, see **Table 3 - 1 Correspondence Between Address Values and Block Numbers in Flash Memory**.



(R5F11NME)

Correspondence between the address values and block numbers in the flash memory are shown below.

Table 3 - 1 Correspondence Between Address Values and Block Numbers in Flash Memory

Address Value	Block Number	Address Value	Block Number	Address Value	Block Number	Address Value	Block Number
00000H to 003FFH	00H	08000H to 083FFH	20H	10000H to 103FFH	40H	18000H to 183FFH	60H
00400H to 007FFH	01H	08400H to 087FFH	21H	10400H to 107FFH	41H	18400H to 187FFH	61H
00800H to 00BFFH	02H	08800H to 08BFFH	22H	10800H to 10BFFH	42H	18800H to 18BFFH	62H
00C00H to 00FFFH	03H	08C00H to 08FFFH	23H	10C00H to 10FFFH	43H	18C00H to 18FFFH	63H
01000H to 013FFH	04H	09000H to 093FFH	24H	11000H to 113FFH	44H	19000H to 193FFH	64H
01400H to 017FFH	05H	09400H to 097FFH	25H	11400H to 117FFH	45H	19400H to 197FFH	65H
01800H to 01BFFH	06H	09800H to 09BFFH	26H	11800H to 11BFFH	46H	19800H to 19BFFH	66H
01C00H to 01FFFH	07H	09C00H to 09FFFH	27H	11C00H to 11FFFH	47H	19C00H to 19FFFH	67H
02000H to 023FFH	08H	0A000H to 0A3FFH	28H	12000H to 123FFH	48H	1A000H to 1A3FFH	68H
02400H to 027FFH	09H	0A400H to 0A7FFH	29H	12400H to 127FFH	49H	1A400H to 1A7FFH	69H
02800H to 02BFFH	0AH	0A800H to 0ABFFH	2AH	12800H to 12BFFH	4AH	1A800H to 1ABFFH	6AH
02C00H to 02FFFH	0BH	0AC00H to 0AFFFH	2BH	12C00H to 12FFFH	4BH	1AC00H to 1AFFFH	6BH
03000H to 033FFH	0CH	0B000H to 0B3FFH	2CH	13000H to 133FFH	4CH	1B000H to 1B3FFH	6CH
03400H to 037FFH	0DH	0B400H to 0B7FFH	2DH	13400H to 137FFH	4DH	1B400H to 1B7FFH	6DH
03800H to 03BFFH	0EH	0B800H to 0BBFFH	2EH	13800H to 13BFFH	4EH	1B800H to 1BBFFH	6EH
03C00H to 03FFFH	0FH	0BC00H to 0BFFFH	2FH	13C00H to 13FFFH	4FH	1BC00H to 1BFFFH	6FH
04000H to 043FFH	10H	0C000H to 0C3FFH	30H	14000H to 143FFH	50H	1C000H to 1C3FFH	70H
04400H to 047FFH	11H	0C400H to 0C7FFH	31H	14400H to 147FFH	51H	1C400H to 1C7FFH	71H
04800H to 04BFFH	12H	0C800H to 0CBFFH	32H	14800H to 14BFFH	52H	1C800H to 1CBFFH	72H
04C00H to 04FFFH	13H	0CC00H to 0CFFFH	33H	14C00H to 14FFFH	53H	1CC00H to 1CFFFH	73H
05000H to 053FFH	14H	0D000H to 0D3FFH	34H	15000H to 153FFH	54H	1D000H to 1D3FFH	74H
05400H to 057FFH	15H	0D400H to 0D7FFH	35H	15400H to 157FFH	55H	1D400H to 1D7FFH	75H
05800H to 05BFFH	16H	0D800H to 0DBFFH	36H	15800H to 15BFFH	56H	1D800H to 1DBFFH	76H
05C00H to 05FFFH	17H	0DC00H to 0DFFFH	37H	15C00H to 15FFFH	57H	1DC00H to 1DFFFH	77H
06000H to 063FFH	18H	0E000H to 0E3FFH	38H	16000H to 163FFH	58H	1E000H to 1E3FFH	78H
06400H to 067FFH	19H	0E400H to 0E7FFH	39H	16400H to 167FFH	59H	1E400H to 1E7FFH	79H
06800H to 06BFFH	1AH	0E800H to 0EBFFH	3AH	16800H to 16BFFH	5AH	1E800H to 1EBFFH	7AH
06C00H to 06FFFH	1BH	0EC00H to 0EFFFH	3BH	16C00H to 16FFFH	5BH	1EC00H to 1EFFFH	7BH
07000H to 073FFH	1CH	0F000H to 0F3FFH	3CH	17000H to 173FFH	5CH	1F000H to 1F3FFH	7CH
07400H to 077FFH	1DH	0F400H to 0F7FFH	3DH	17400H to 177FFH	5DH	1F400H to 1F7FFH	7DH
07800H to 07BFFH	1EH	0F800H to 0FBFFH	3EH	17800H to 17BFFH	5EH	1F800H to 1FBFFH	7EH
07C00H to 07FFFH	1FH	0FC00H to 0FFFFH	3FH	17C00H to 17FFFH	5FH	1FC00H to 1FFFFH	7FH

Remark R5F11NME: Block numbers 00H to 3FH
R5F11xF (x = NG, NL, NM, PL): Block numbers 00H to 5FH
R5F11xG (x = NG, NL, NM, PL), R5F11RMG: Block numbers 00H to 7FH

3.2.1 Internal program memory space

The internal program memory space stores the program and table data. The RL78/H1D products incorporate internal ROM (flash memory), as shown below.

Table 3 - 2 Internal ROM Capacity

Part Number	Internal ROM	
	Structure	Capacity
R5F11NME	Flash memory	65536 × 8 bits (00000H to 0FFFFH)
R5F11xF (x = NG, NL, NM, PL)		98304 × 8 bits (00000H to 17FFFH)
R5F11xG (x = NG, NL, NM, PL), R5F11RMG		131072 × 8 bits (00000H to 1FFFFH)

The internal program memory space is divided into the following areas.

(1) Vector table area

The 128-byte area 00000H to 0007FH is reserved as a vector table area. The program start addresses for branch upon reset or generation of each interrupt request are stored in the vector table area. Furthermore, the interrupt jump address is a 64 K address of 00000H to 0FFFFH, because the vector code is assumed to be 2 bytes.

Of the 16-bit address, the lower 8 bits are stored at even addresses and the higher 8 bits are stored at odd addresses.

To use the boot swap function, set a vector table also at 01000H to 0107FH.

Table 3 - 3 Vector Table (1/2)

Vector Table Address	Interrupt Source	R5F11NM	R5F11NL	R5F11PL, R5F11NG	R5F11RM
00000H	RESET, POR, LVD, WDT, TRAP, IAW, RPE	√	√	√	√
00004H	INTWDTI	√	√	√	√
00006H	INTLVI	√	√	√	√
00008H	INTP0	√	√	√	√
0000AH	INTP1	√	√	√	√
0000CH	INTP2	√	√	√	√
0000EH	INTP3	√	√	√	√
00010H	INTP4	√	√	√	√
00012H	INTP5	√	√	√	√
00014H	INTST2/INTCSI20/INTIIC20	√	√	√	√
00016H	INTSR2	√	√	√	√
00018H	INTSRE2	√	√	√	√
0001EH	INTST0/INTCSI00/INTIIC00	√	√	√	√
00020H	INTTM00	√	√	√	√
00022H	INTSR0	√	√	√	√
00024H	INTSRE0	√	√	√	√
	INTTM01H	√	√	√	√
00026H	INTST1/INTCSI10/INTIIC10	√	√	√	√
00028H	INTSR1	√	√	√	√
0002AH	INTSRE1	√	√	√	√
	INTTM03H	√	√	√	√
0002CH	INTIICA0	√	√	√	√
0002EH	INTRTIT	√	√	√	√
	INTSMP0	—	—	—	√
00032H	INTTM01	√	√	√	√
00034H	INTTM02	√	√	√	√
00036H	INTTM03	√	√	√	√
00038H	INTAD	√	√	√	√
0003AH	INTRTC	√	√	√	√
	INTSMP1	—	—	—	√
0003CH	INTIT	√	√	√	√
0003EH	INTTRJ0	—	—	—	√
00040H	INTTRJ1	—	—	—	√
00042H	INTTM04	√	√	√	√
00044H	INTTM05	√	√	√	√
00046H	INTP6	√	—	√	√
00048H	INTP7	√	—	—	√
0004CH	INTTM06	√	√	√	√
0004EH	INTTM07	√	√	√	√
00050H	INTIT00	√	√	√	√
00052H	INTIT01	√	√	√	√
00054H	INTIT10	—	—	—	√

Table 3 - 3 Vector Table (2/2)

Vector Table Address	Interrupt Source	R5F11NM	R5F11NL	R5F11PL, R5F11NG	R5F11RM
00056H	INTIT11	—	—	—	√
00058H	INTIT20	—	—	—	√
0005AH	INTIT21	—	—	—	√
0005CH	INTDSAD	√	√	√	—
	INTEXSD	—	—	—	√
00060H	INTDSADS	√	√	√	—
	INTSMP2	—	—	—	√
00062H	INTFL	√	√	√	√
00064H	INTSMP3	—	—	—	√
00066H	INTSMP4	—	—	—	√
00068H	INTSMP5	—	—	—	√
0006AH	INTSMOTA	—	—	—	√
0006CH	INTSMOTB	—	—	—	√
0006EH	INTSTMG0	—	—	—	√
00070H	INTSRMG0	—	—	—	√
00072H	INTSREMG0	—	—	—	√
0007EH	BRK	√	√	√	√

(2) CALLT instruction table area

The 64-byte area 00080H to 000BFH can store the subroutine entry address of a 2-byte call instruction (CALLT). Set the subroutine entry address to a value in a range of 00000H to 0FFFFH (because an address code is 2 bytes).

To use the boot swap function, set a CALLT instruction table also at 01080H to 010BFH.

(3) Option byte area

A 4-byte area of 000C0H to 000C3H can be used as an option byte area. Set the option byte at 010C0H to 010C3H when the boot swap is used. For details, see **CHAPTER 33 OPTION BYTE**.

(4) On-chip debug security ID setting area

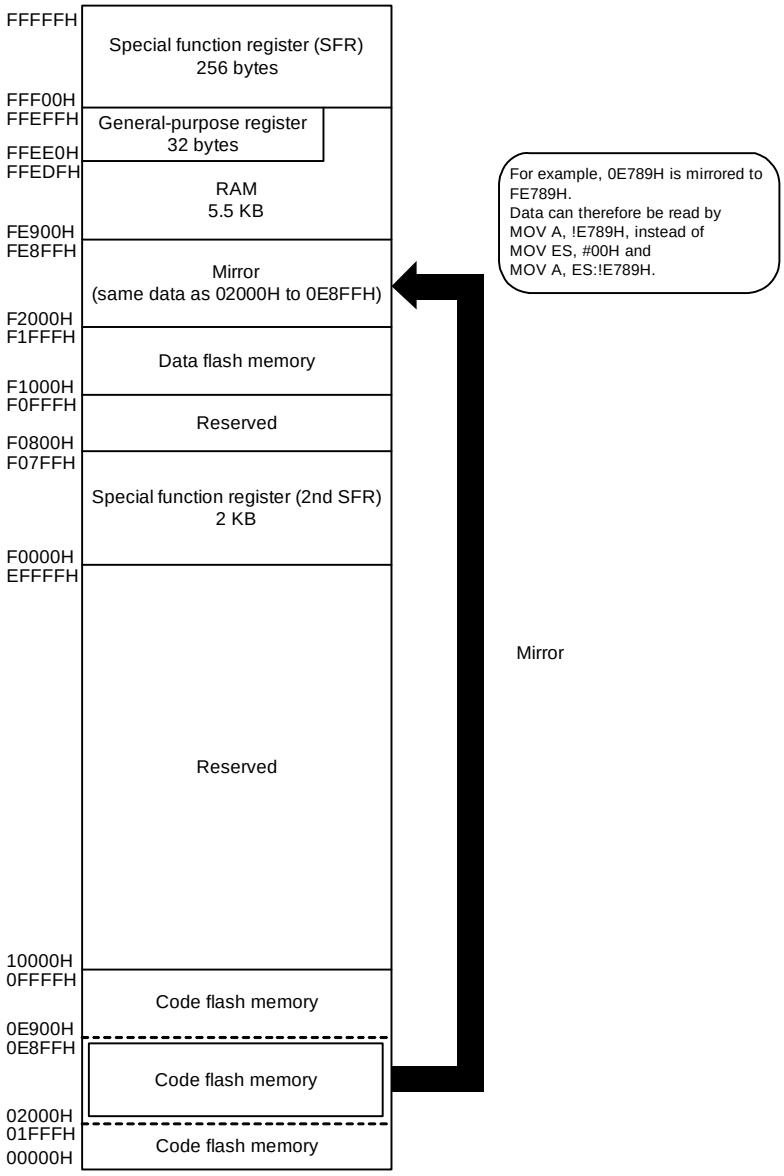
A 10-byte area of 000C4H to 000CDH and 010C4H to 010CDH can be used as an on-chip debug security ID setting area. Set the on-chip debug security ID of 10 bytes at 000C4H to 000CDH when the boot swap is not used and at 000C4H to 000CDH and at 010C4H to 010CDH when the boot swap is used. For details, see **CHAPTER 35 ON-CHIP DEBUG FUNCTION**.

3.2.2 Mirror area

The RL78/H1D mirrors the code flash area of 00000H to 0FFFFH, to F0000H to FFFFFH. The products with 96 KB or more flash memory mirror the code flash area of 00000H to 0FFFFH or 10000H to 1FFFFH, to F0000H to FFFFFH (the code flash area to be mirrored is set by the processor mode control register (PMC)).
By reading data from F0000H to FFFFFH, an instruction that does not have the ES register as an operand can be used, and thus the contents of the code flash can be read with the shorter code. However, the code flash area is not mirrored to the SFR, extended SFR, RAM, and use prohibited areas.

See **3.2 Memory Space** for the mirror area of each product.
The mirror area can only be read and no instruction can be fetched from this area.
The following show examples.

Example R5F11NME (Flash memory: 64 KB, RAM: 5.5 KB)



The PMC register is described below.

• Processor mode control register (PMC)
This register sets the flash memory space for mirroring to area from F0000H to FFFFFH.
The PMC register can be set by a 1-bit or 8-bit memory manipulation instruction.
Reset signal generation sets this register to 00H.

Figure 3 - 5 Format of Configuration of Processor mode control register (PMC)

Address: FFFFEH After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	<0>
PMC	0	0	0	0	0	0	0	MAA

MAA	Selection of flash memory space for mirroring to area from F0000H to FFFFFH
0	00000H to 0FFFFH is mirrored to F0000H to FFFFFH
1	10000H to 1FFFFH is mirrored to F0000H to FFFFFH

Caution 1. In products with 64 KB or less flash memory, be sure to set bit 0 (MAA) to 0 (initial value).
Caution 2. Set the PMC register only once during the initial settings prior to operating the DTC (data transfer controller).
Rewriting the PMC register other than during the initial settings is prohibited.
Caution 3. After setting the PMC register, wait for at least one instruction and access the mirror area.

3.2.3 Internal data memory space

The RL78/H1D products incorporate the following RAMs.

Table 3 - 4 Internal RAM Capacity

Part Number	Internal RAM
R5F11NME	5632 × 8 bits (FE900H to FFEFFH)
R5F11xF (x = NG, NL, NM, PL)	
R5F11xG (x = NG, NL, NM, PL)	
R5F11RMG	8192 × 8 bits (FDF00H to FFEFFH)

The internal RAM can be used as a data area and a program area where instructions are written and executed (it is prohibited to use the general-purpose register area for executing instructions). Four general-purpose register banks consisting of eight 8-bit registers per bank are assigned to the 32-byte area of FFEE0H to FFEFFH of the internal RAM area.
The internal RAM is used as a stack memory.

Caution 1. It is prohibited to use the general-purpose register (FFEE0H to FFEFFH) space for fetching instructions or as a stack area.

Caution 2. Do not allocate the stack area, data buffers, branch destinations in the processing of vectored interrupts, or destinations or sources for DTC transfer to the area from FFE20H to FFEDFH when performing self-programming or rewriting of the data flash memory.

Caution 3. Use of the RAM areas of the following products is prohibited when performing self-programming and rewriting the data flash memory, because these areas are used for each library.
R5F11RMG: FDF00H to FE309H

Caution 4. The internal RAM area in the following products cannot be used as the stack memory when using the on-chip debug trace function.
R5F11RMG: FE300H to FE6FFH

3.2.4 Special function register (SFR) area

On-chip peripheral hardware special function registers (SFRs) are allocated in the area FFF00H to FFFFFH (see **Table 3 - 5** in **3.3.4 Special function registers (SFRs)**).

Caution Do not access addresses to which SFRs are not assigned.

3.2.5 Extended special function register (2nd SFR: 2nd Special Function Register) area

On-chip peripheral hardware special function registers (2nd SFRs) are allocated in the area F0000H to F07FFH (see **Table 3 - 6** in **3.3.5 Extended special function registers (2nd SFRs: 2nd Special Function Registers)**). SFRs other than those in the SFR area (FFF00H to FFFFFH) are allocated to this area. An instruction that accesses the extended SFR area, however, is 1 byte longer than an instruction that accesses the SFR area.

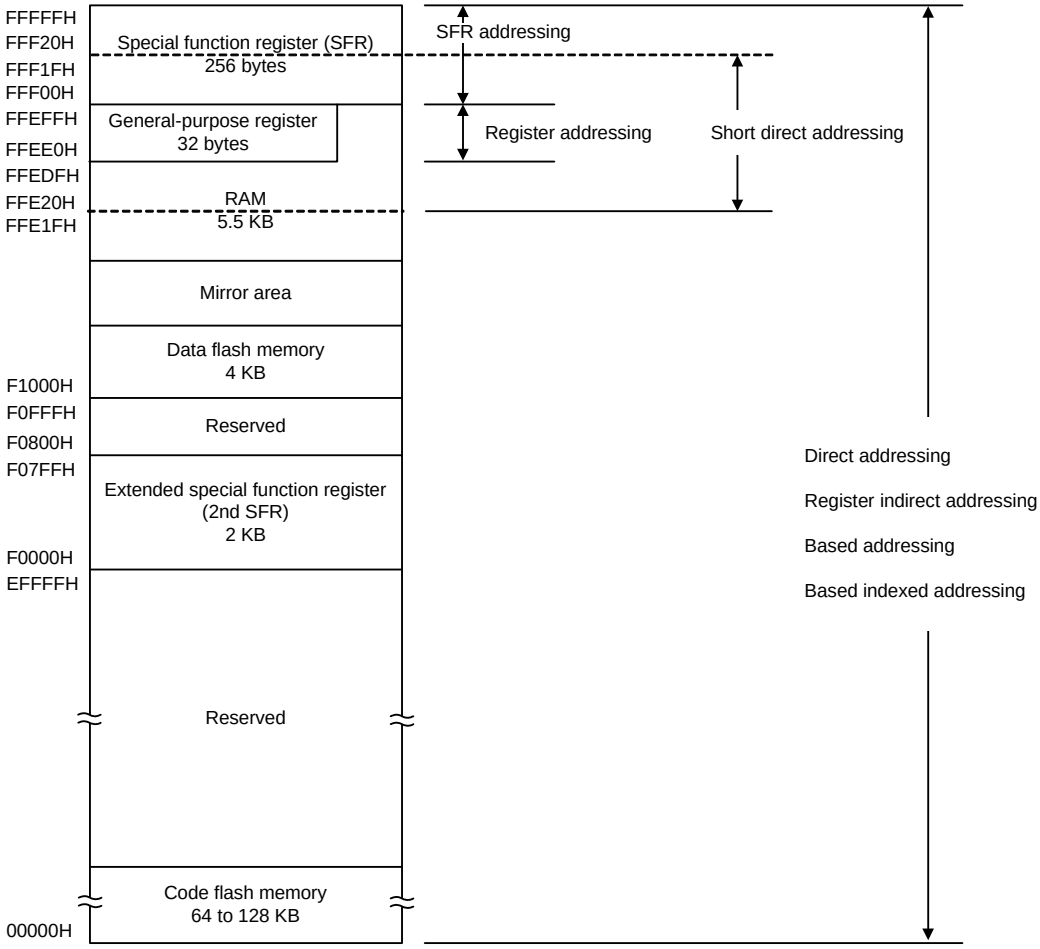
Caution Do not access addresses to which extended SFRs are not assigned.

3.2.6 Data memory addressing

Addressing refers to the method of specifying the address of the instruction to be executed next or the address of the register or memory relevant to the execution of instructions.
Several addressing modes are provided for addressing the memory relevant to the execution of instructions for the RL78/H1D, based on operability and other considerations. For areas containing data memory in particular, special addressing methods designed for the functions of the special function registers (SFR) and general-purpose registers are available for use. Figure 3 - 6 shows the correspondence between data memory and addressing.

For details of each addressing, see **3.5 Addressing for Processing Data Addresses**.

Figure 3 - 6 Correspondence Between Data Memory and Addressing



3.3 Processor Registers

The RL78/H1D products incorporate the following processor registers.

3.3.1 Control registers

The control registers control the program sequence, statuses and stack memory. The control registers consist of a program counter (PC), a program status word (PSW) and a stack pointer (SP).

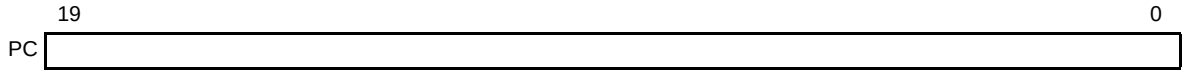
(1) Program counter (PC)

The program counter is a 20-bit register that holds the address information of the next program to be executed.

In normal operation, PC is automatically incremented according to the number of bytes of the instruction to be fetched. When a branch instruction is executed, immediate data and register contents are set.

Reset signal generation sets the reset vector table values at addresses 0000H and 0001H to the 16 lower-order bits of the program counter. The four higher-order bits of the program counter are cleared to 0000.

Figure 3 - 7 Format of Program Counter



(2) Program status word (PSW)

The program status word is an 8-bit register consisting of various flags set/reset by instruction execution.

Program status word contents are stored in the stack area upon vectored interrupt request is acknowledged or PUSH PSW instruction execution and are restored upon execution of the RETB, RETI and POP PSW instructions. Reset signal generation sets the PSW register to 06H.

Figure 3 - 8 Format of Program Status Word

	7							0
PSW	IE	Z	RBS1	AC	RBS0	ISP1	ISP0	CY

(a) Interrupt enable flag (IE)

This flag controls the interrupt request acknowledge operations of the CPU.

When 0, the IE flag is set to the interrupt disabled (DI) state, and all maskable interrupt requests are disabled.

When 1, the IE flag is set to the interrupt enabled (EI) state and interrupt request acknowledgment is controlled with an in-service priority flag (ISP1, ISP0), an interrupt mask flag for various interrupt sources, and a priority specification flag.

The IE flag is reset (0) upon DI instruction execution or interrupt acknowledgment and is set (1) upon EI instruction execution.

(b) Zero flag (Z)
When the operation result is zero, this flag is set (1). It is reset (0) in all other cases.

(c) Register bank select flags (RBS0, RBS1)
These are 2-bit flags to select one of the four register banks.
In these flags, the 2-bit information that indicates the register bank selected by SEL RBn instruction execution is stored.

(d) Auxiliary carry flag (AC)
If the operation result has a carry from bit 3 or a borrow at bit 3, this flag is set (1). It is reset (0) in all other cases.

(e) In-service priority flags (ISP1, ISP0)
This flag manages the priority of acknowledgeable maskable vectored interrupts. Vectored interrupt requests specified lower than the value of ISP0 and ISP1 flags by the priority specification flag registers (PRn0L, PRn0H, PRn1L, PRn1H, PRn2L, PRn2H) (see **26.3.3**) cannot be acknowledged. Actual request acknowledgment is controlled by the interrupt enable flag (IE).

Remark n = 0, 1

(f) Carry flag (CY)
This flag stores overflow and underflow upon add/subtract instruction execution. It stores the shift-out value upon rotate instruction execution and functions as a bit accumulator during bit operation instruction execution.

(3) Stack pointer (SP)

This is a 16-bit register to hold the start address of the memory stack area. Only the internal RAM area can be set as the stack area.

Figure 3 - 9 Format of Stack Pointer

	15															0
SP	SP15	SP14	SP13	SP12	SP11	SP10	SP9	SP8	SP7	SP6	SP5	SP4	SP3	SP2	SP1	0

In stack addressing through a stack pointer, the SP is decremented ahead of write (save) to the stack memory and is incremented after read (restore) from the stack memory.

Caution 1. Since reset signal generation makes the SP contents undefined, be sure to initialize the SP before using the stack.

Caution 2. It is prohibited to use the general-purpose register (FFEE0H to FFEFFH) space for fetching instructions or as a stack area.

Caution 3. Do not allocate the stack area, data buffers, branch destinations in the processing of vectored interrupts, or destinations or sources for DTC transfer to the area from FFE20H to FFEDFH when performing self-programming or rewriting of the data flash memory.

Caution 4. Use of the RAM areas of the following products is prohibited when performing self-programming and rewriting the data flash memory, because these areas are used for each library.

R5F11RMG: FDF00H to FE309H

Caution 5. The internal RAM area in the following products cannot be used as the stack memory when using the on-chip debug trace function.

R5F11RMG: FE300H to FE6FFH

3.3.2 General-purpose registers

General-purpose registers are mapped at particular addresses (FFEE0H to FFEFFH) of the data memory. The general-purpose registers consists of 4 banks, each bank consisting of eight 8-bit registers (X, A, C, B, E, D, L, and H).

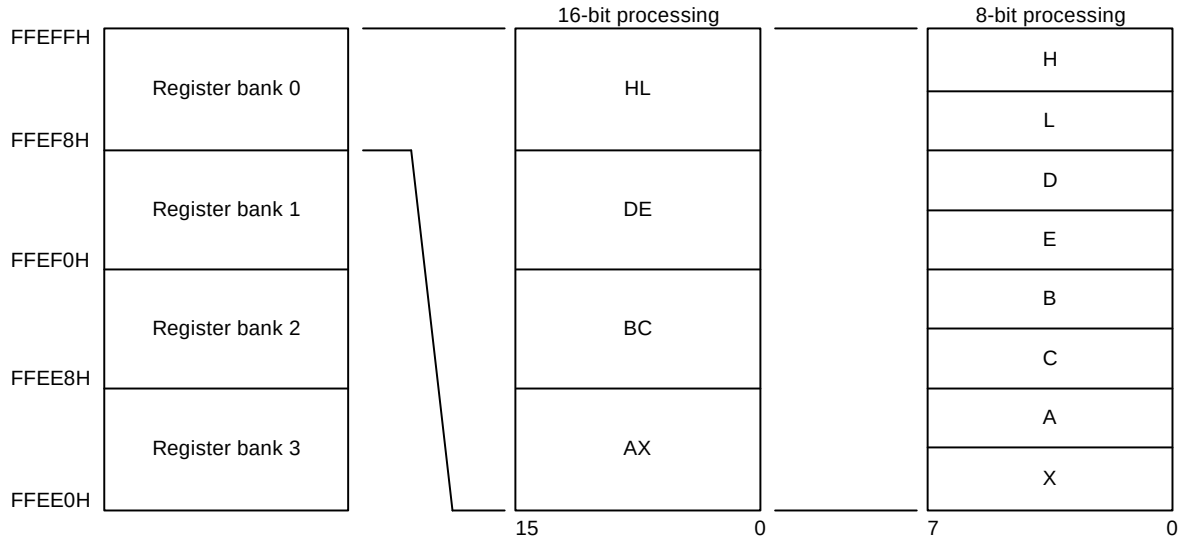
Each register can be used as an 8-bit register, and two 8-bit registers can also be used in a pair as a 16-bit register (AX, BC, DE, and HL).

Register banks to be used for instruction execution are set by the CPU control instruction (SEL RBn). Because of the 4-register bank configuration, an efficient program can be created by switching between a register for normal processing and a register for interrupts for each bank.

Caution It is prohibited to use the general-purpose register (FFEE0H to FFEFFH) space for fetching instructions or as a stack area.

Figure 3 - 10 Configuration of General-Purpose Registers

(a) Function name



3.3.3 ES and CS registers

The ES register and CS register are used to specify the higher address for data access and when a branch instruction is executed (register direct addressing), respectively.
The default value of the ES register after reset is 0FH, and that of the CS register is 00H.

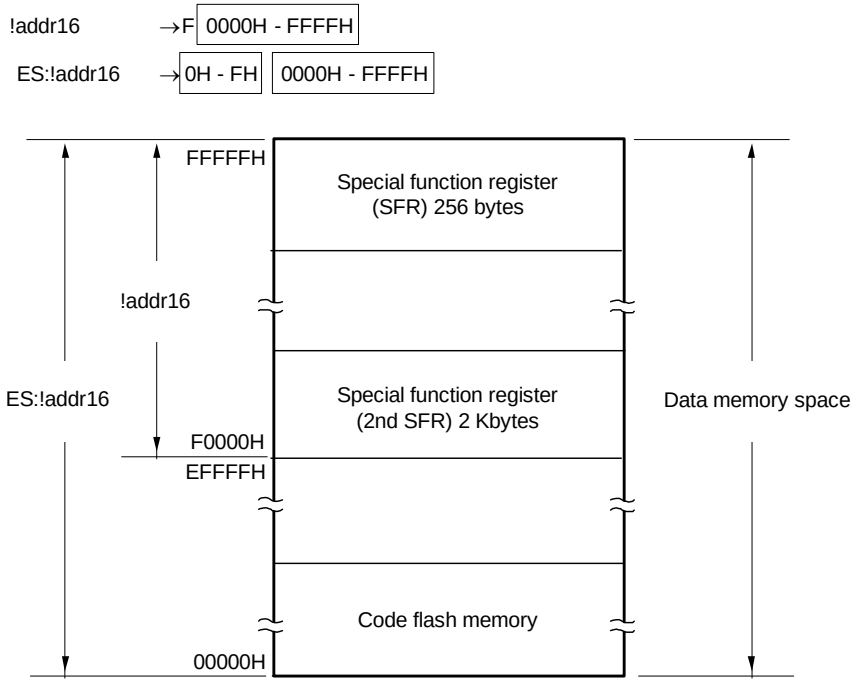
Figure 3 - 11 Configuration of ES and CS Registers

	7	6	5	4	3	2	1	0
ES	0	0	0	0	ES3	ES2	ES1	ES0

	7	6	5	4	3	2	1	0
CS	0	0	0	0	CS3	CS2	CS1	CS0

Though the data area which can be accessed with 16-bit addresses is the 64 Kbytes from F0000H to FFFFFH, using the ES register as well extends this to the 1 Mbyte from 00000H to FFFFFH.

Figure 3 - 12 Extension of Data Area Which Can Be Accessed



3.3.4 Special function registers (SFRs)

Unlike a general-purpose register, each SFR has a special function.

SFRs are allocated to the FFF00H to FFFFFH area.

SFRs can be manipulated like general-purpose registers, using operation, transfer, and bit manipulation instructions. The manipulable bit units, 1, 8, and 16, depend on the SFR type.

Each manipulation bit unit can be specified as follows.

- 1-bit manipulation
  Describe as follows for the 1-bit manipulation instruction operand (sfr.bit).
  When the bit name is defined: <Bit name>
  When the bit name is not defined: <Register name>.<Bit number> or <Address>.<Bit number>
- 8-bit manipulation
  Describe the symbol reserved by the assembler for the 8-bit manipulation instruction operand (sfr).
  This manipulation can also be specified with an address.
- 16-bit manipulation
  Describe the symbol reserved by the assembler for the 16-bit manipulation instruction operand (sfrp).
  When specifying an address, describe an even address.

Table 3 - 5 give lists of the SFRs. The meanings of items in the table are as follows.

- Symbol
  This item indicates the address of a special function register. It is a reserved word in the assembler, and is defined as an sfr variable using the #pragma sfr directive in the compiler. When using the assembler, debugger, and simulator, symbols can be written as an instruction operand.
- R/W
  This item indicates whether the corresponding SFR can be read or written.
  R/W: Read/write enable
  R: Read only
  W: Write only
- Manipulable bit units
  "√" indicates the manipulable bit unit (1, 8, or 16). "—" indicates a bit unit for which manipulation is not possible.
- After reset
  This item indicates each register status upon reset signal generation.

Caution **Do not access addresses to which SFRs are not assigned.**

Remark For extended SFRs (2nd SFRs), see **3.3.5 Extended special function registers (2nd SFRs: 2nd Special Function Registers)**.

Table 3 - 5 SFR List (1/4)

Address	Special Function Register (SFR) Name	Symbol		R/W	Manipulable Bit Range			After Reset
					1-bit	8-bit	16-bit	
FFF00H	Port register 0	P0		R/W	√	√	—	00H
FFF01H	Port register 1	P1		R/W	√	√	—	00H
FFF02H	Port register 2	P2		R/W	√	√	—	00H
FFF03H	Port register 3	P3		R/W	√	√	—	00H
FFF04H	Port register 4	P4		R/W	√	√	—	00H
FFF05H	Port register 5	P5		R/W	√	√	—	00H
FFF06H	Port register 6	P6		R/W	√	√	—	00H
FFF07H	Port register 7	P7		R/W	√	√	—	00H
FFF08H	Port register 8	P8		R/W	√	√	—	00H
FFF0CH	Port register 12	P12		R/W	√	√	—	Undefined
FFF0DH	Port register 13	P13		R/W	√	√	—	Undefined
FFF0FH	Port register 15	P15		R/W	√	√	—	00H
FFF10H	Serial data register 00	TXD0/ SIO00	SDR00	R/W	—	√	√	0000H
FFF11H		—			—	—		
FFF12H	Serial data register 01	RXD0	SDR01	R/W	—	√	√	0000H
FFF13H		—			—	—		
FFF18H	Timer data register 00	TDR00		R/W	—	—	√	0000H
FFF19H								
FFF1AH	Timer data register 01	TDR01L	TDR01	R/W	—	√	√	00H
FFF1BH		TDR01H			—	√		00H
FFF1EH	10-bit A/D conversion result register	ADCR		R	—	—	√	0000H
FFF1FH	8-bit A/D conversion result register	ADCRH		R	—	√	—	00H
FFF20H	Port mode register 0	PM0		R/W	√	√	—	FFH
FFF21H	Port mode register 1	PM1		R/W	√	√	—	FFH
FFF22H	Port mode register 2	PM2		R/W	√	√	—	FFH
FFF23H	Port mode register 3	PM3		R/W	√	√	—	FFH
FFF24H	Port mode register 4	PM4		R/W	√	√	—	FFH
FFF25H	Port mode register 5	PM5		R/W	√	√	—	FFH
FFF26H	Port mode register 6	PM6		R/W	√	√	—	FFH
FFF27H	Port mode register 7	PM7		R/W	√	√	—	FFH
FFF28H	Port mode register 8	PM8		R/W	√	√	—	FFH
FFF2CH	Port mode register 12	PM12		R/W	√	√	—	FFH
FFF2FH	Port mode register 15	PM15		R/W	√	√	—	FFH

Table 3 - 5 SFR List (2/4)

Address	Special Function Register (SFR) Name	Symbol		R/W	Manipulable Bit Range			After Reset
					1-bit	8-bit	16-bit	
FFF30H	A/D converter mode register 0	ADM0		R/W	√	√	—	00H
FFF31H	Analog input channel specification register	ADS		R/W	√	√	—	00H
FFF32H	A/D converter mode register 1	ADM1		R/W	√	√	—	00H
FFF38H	External interrupt rising edge enable register 0	EGP0		R/W	√	√	—	00H
FFF39H	External interrupt falling edge enable register 0	EGN0		R/W	√	√	—	00H
FFF40H	LCD mode register 0	LCDM0		R/W	—	√	—	00H
FFF41H	LCD mode register 1	LCDM1		R/W	√	√	—	00H
FFF42H	LCD clock control register 0	LCDC0		R/W	—	√	—	00H
FFF43H	LCD boost level control register	VLCD		R/W	—	√	—	04H
FFF44H	Serial data register 02	TXD1/ SIO10	SDR02	R/W	—	√	√	0000H
FFF45H		—			—	—		
FFF46H	Serial data register 03	RXD1	SDR03	R/W	—	√	√	0000H
FFF47H		—			—	—		
FFF48H	Serial data register 10	TXD2/ SIO20	SDR10	R/W	—	√	√	0000H
FFF49H					—	—		
FFF4AH	Serial data register 11	RXD2	SDR11	R/W	—	√	√	0000H
FFF4BH		—			—	—		
FFF50H	IICA shift register 0	IICA0		R/W	—	√	—	00H
FFF51H	IICA status register 0	IICS0		R	√	√	—	00H
FFF52H	IICA flag register 0	IICF0		R/W	√	√	—	00H
FFF64H	Timer data register 02	TDR02		R/W	—	—	√	0000H
FFF65H								
FFF66H	Timer data register 03	TDR03L	TDR03	R/W	—	√	√	00H
FFF67H		TDR03H			—	√		00H
FFF68H	Timer data register 04	TDR04		R/W	—	—	√	0000H
FFF69H								
FFF6AH	Timer data register 05	TDR05		R/W	—	—	√	0000H
FFF6BH								
FFF6CH	Timer data register 06	TDR06		R/W	—	—	√	0000H
FFF6DH								
FFF6EH	Timer data register 07	TDR07		R/W	—	—	√	0000H
FFF6FH								

Table 3 - 5 SFR List (3/4)

Address	Special Function Register (SFR) Name	Symbol	R/W	Manipulable Bit Range			After Reset
				1-bit	8-bit	16-bit	
FFF90H	12-bit interval timer control register	ITMC	R/W	—	—	√	0FFFH
FFF91H							
FFF92H	Second count register	SEC	R/W	—	√	—	Undefined
FFF93H	Minute count register	MIN	R/W	—	√	—	Undefined
FFF94H	Hour count register	HOUR	R/W	—	√	—	Undefined
FFF95H	Week count register	WEEK	R/W	—	√	—	Undefined
FFF96H	Day count register	DAY	R/W	—	√	—	Undefined
FFF97H	Month count register	MONTH	R/W	—	√	—	Undefined
FFF98H	Year count register	YEAR	R/W	—	√	—	Undefined
FFF9AH	Alarm minute register	ALARMWM	R/W	—	√	—	Undefined
FFF9BH	Alarm hour register	ALARMWH	R/W	—	√	—	Undefined
FFF9CH	Alarm week register	ALARMWW	R/W	—	√	—	Undefined
FFF9DH	Real-time clock control register 0	RTCC0	R/W	√	√	—	00H Note 1
FFF9EH	Real-time clock control register 1	RTCC1	R/W	√	√	—	00H Note 1
FFFA0H	Clock operation mode control register	CMC	R/W	—	√	—	00H Note 1
FFFA1H	Clock operation status control register	CSC	R/W	√	√	—	C0H Note 1
FFFA2H	Oscillation stabilization time counter status register	OSTC	R	√	√	—	00H
FFFA3H	Oscillation stabilization time select register	OSTS	R/W	—	√	—	07H
FFFA4H	System clock control register	CKC	R/W	√	√	—	00H
FFFA5H	Clock output select register 0	CKS0	R/W	√	√	—	00H
FFFA6H	Clock output select register 1	CKS1	R/W	√	√	—	00H
FFFA8H	Reset control flag register	RESF	R	—	√	—	Undefined Note 2
FFFA9H	Voltage detection register	LVIM	R/W	√	√	—	00H Note 2
FFFAAH	Voltage detection level register	LVIS	R/W	√	√	—	00H/01H/81H Note 2
FFFABH	Watchdog timer enable register	WDTE	R/W	—	√	—	9AH/1AH Note 3
FFFACH	CRC input register	CRCIN	R/W	—	√	—	00H

Note 1. This register is reset only by a power-on reset.

Note 2. The register states change depending on reset sources as shown below.

Register \ Reset Source		$\overline{\text{RESET}}$ Input	Reset by POR	Reset by Executing Illegal Instruction	Reset by WDT	Reset by RAM Parity Error	Reset by Illegal Memory Access	Reset by LVD
RESF	TRAP	Cleared (0)		Set (1)	Retained			Retained
	WDTRF			Retained	Set (1)	Retained		
	RPERF			Retained		Set (1)	Retained	
	IAWRF			Retained			Set (1)	
	LVIRF			Retained				Set (1)
LVIM	LVISEN	Cleared (0)						Retained
	LVIOMSK	Retained						
	LVIF							
LVIS		Cleared (00H/01H/81H)						

Note 3. The reset value of the WDTE register is determined by the setting of the option byte.

Table 3 - 5 SFR List (4/4)

Address	Special Function Register (SFR) Name	Symbol		R/W	Manipulable Bit Range			After Reset
					1-bit	8-bit	16-bit	
FFFD0H	Interrupt request flag register 2	IF2L	IF2	R/W	√	√	√	00H
FFFD1H		IF2H		R/W	√	√		00H
FFFD2H	Interrupt request flag register 3	IF3L		R/W	√	√	—	00H
FFFD4H	Interrupt mask flag register 2	MK2L	MK2	R/W	√	√	√	FFH
FFFD5H		MK2H		R/W	√	√		FFH
FFFD6H	Interrupt mask flag register 3	MK3L		R/W	√	√	—	FFH
FFFD8H	Priority specification flag register 02	PR02L	PR02	R/W	√	√	√	FFH
FFFD9H		PR02H		R/W	√	√		FFH
FFFDAH	Priority specification flag register 03	PR03L		R/W	√	√	—	FFH
FFFDCH	Priority specification flag register 12	PR12L	PR12	R/W	√	√	√	FFH
FFFDDH		PR12H		R/W	√	√		FFH
FFFDEH	Priority specification flag register 13	PR13L		R/W	√	√	—	FFH
FFFE0H	Interrupt request flag register 0	IF0L	IF0	R/W	√	√	√	00H
FFFE1H		IF0H		R/W	√	√		00H
FFFE2H	Interrupt request flag register 1	IF1L	IF1	R/W	√	√	√	00H
FFFE3H		IF1H		R/W	√	√		00H
FFFE4H	Interrupt mask flag register 0	MK0L	MK0	R/W	√	√	√	FFH
FFFE5H		MK0H		R/W	√	√		FFH
FFFE6H	Interrupt mask flag register 1	MK1L	MK1	R/W	√	√	√	FFH
FFFE7H		MK1H		R/W	√	√		FFH
FFFE8H	Priority specification flag register 00	PR00L	PR00	R/W	√	√	√	FFH
FFFE9H		PR00H		R/W	√	√		FFH
FFFEAH	Priority specification flag register 01	PR01L	PR01	R/W	√	√	√	FFH
FFFEBH		PR01H		R/W	√	√		FFH
FFFECH	Priority specification flag register 10	PR10L	PR10	R/W	√	√	√	FFH
FFFEDH		PR10H		R/W	√	√		FFH
FFFEEH	Priority specification flag register 11	PR11L	PR11	R/W	√	√	√	FFH
FFFEFH		PR11H		R/W	√	√		FFH
FFFF0H	Multiply and accumulation register (L)	MACRL		R/W	—	—	√	0000H
FFFF1H								
FFFF2H	Multiply and accumulation register (H)	MACRH		R/W	—	—	√	0000H
FFFF3H								
FFFFEH	Processor mode control register	PMC		R/W	√	√	—	00H

Remark For extended SFRs (2nd SFRs), see **Table 3 - 6 Extended SFR (2nd SFR) List**.

3.3.5 Extended special function registers (2nd SFRs: 2nd Special Function Registers)

Unlike a general-purpose register, each extended SFR (2nd SFR) has a special function.
Extended SFRs are allocated to the F0000H to F07FFH area. SFRs other than those in the SFR area (FFF00H to FFFFFH) are allocated to this area. An instruction that accesses the extended SFR area, however, is 1 byte longer than an instruction that accesses the SFR area.
Extended SFRs can be manipulated like general-purpose registers, using operation, transfer, and bit manipulation instructions. The manipulable bit units, 1, 8, and 16, depend on the SFR type.
Each manipulation bit unit can be specified as follows.

- 1-bit manipulation
  Describe as follows for the 1-bit manipulation instruction operand (!addr16.bit)
  When the bit name is defined: <Bit name>
  When the bit name is not defined: <Register name>.<Bit number> or <Address>.<Bit number>
- 8-bit manipulation
  Describe the symbol reserved by the assembler for the 8-bit manipulation instruction operand (!addr16). This manipulation can also be specified with an address.
- 16-bit manipulation
  Describe the symbol reserved by the assembler for the 16-bit manipulation instruction operand (!addr16). When specifying an address, describe an even address.

Table 3 - 6 give lists of the extended SFRs. The meanings of items in the table are as follows.

- Symbol
  This item indicates the address of an extended SFR. It is a reserved word in the assembler, and is defined as an sfr variable using the #pragma sfr directive in the compiler. When using the assembler, debugger, and simulator, symbols can be written as an instruction operand.
- R/W
  This item indicates whether the corresponding extended SFR can be read or written.
  R/W: Read/write enable
  R: Read only
  W: Write only
- Manipulable bit units
  "√" indicates the manipulable bit unit (1, 8, or 16). "—" indicates a bit unit for which manipulation is not possible.
- After reset
  This item indicates each register status upon reset signal generation.

Caution Do not access addresses to which extended SFRs are not assigned.

Remark For SFRs in the SFR area, see **3.3.4 Special function registers (SFRs)**.

Table 3 - 6 Extended SFR (2nd SFR) List (1/10)

Address	Special Function Register (SFR) Name	Symbol	R/W	Manipulable Bit Range			After Reset
				1-bit	8-bit	16-bit	
F0010H	A/D converter mode register 2	ADM2	R/W	√	√	—	00H
F0011H	Conversion result comparison upper limit setting register	ADUL	R/W	—	√	—	FFH
F0012H	Conversion result comparison lower limit setting register	ADLL	R/W	—	√	—	00H
F0013H	A/D test register	ADTES	R/W	—	√	—	00H
F0030H	Pull-up resistor option register 0	PU0	R/W	√	√	—	00H
F0031H	Pull-up resistor option register 1	PU1	R/W	√	√	—	00H
F0032H	Pull-up resistor option register 2	PU2	R/W	√	√	—	00H
F0033H	Pull-up resistor option register 3	PU3	R/W	√	√	—	00H
F0034H	Pull-up resistor option register 4	PU4	R/W	√	√	—	01H
F0035H	Pull-up resistor option register 5	PU5	R/W	√	√	—	00H
F0037H	Pull-up resistor option register 7	PU7	R/W	√	√	—	00H
F0038H	Pull-up resistor option register 8	PU8	R/W	√	√	—	00H
F003CH	Pull-up resistor option register 12	PU12	R/W	√	√	—	00H
F003FH	Pull-up resistor option register 15	PU15	R/W	√	√	—	00H
F0040H	Port input mode register 0	PIM0	R/W	√	√	—	00H
F0041H	Port input mode register 1	PIM1	R/W	√	√	—	00H
F0043H	Port input mode register 3	PIM3	R/W	√	√	—	00H
F0044H	Port input mode register 4	PIM4	R/W	√	√	—	00H
F0045H	Port input mode register 5	PIM5	R/W	√	√	—	00H
F0048H	Port input mode register 8	PIM8	R/W	√	√	—	00H
F0050H	Port output mode register 0	POM0	R/W	√	√	—	00H
F0051H	Port output mode register 1	POM1	R/W	√	√	—	00H
F0053H	Port output mode register 3	POM3	R/W	√	√	—	00H
F0054H	Port output mode register 4	POM4	R/W	√	√	—	00H
F0055H	Port output mode register 5	POM5	R/W	√	√	—	00H
F0058H	Port output mode register 8	POM8	R/W	√	√	—	00H
F0060H	Port mode control register 0	PMC0	R/W	√	√	—	FFH
F0061H	Port mode control register 1	PMC1	R/W	√	√	—	FFH
F0070H	Noise filter enable register 0	NFEN0	R/W	√	√	—	00H
F0071H	Noise filter enable register 1	NFEN1	R/W	√	√	—	00H
F0073H	Input switch control register	ISC	R/W	√	√	—	00H
F0074H	Timer input select register 0	TIS0	R/W	—	√	—	00H
F0075H	Peripheral I/O redirection register 2	PIOR2	R/W	—	√	—	00H
F0077H	Peripheral I/O redirection register 0	PIOR0	R/W	—	√	—	00H
F0078H	Invalid memory access detection control register	IAWCTL	R/W	—	√	—	00H
F0079H	Peripheral I/O redirection register 1	PIOR1	R/W	—	√	—	00H
F007AH	Peripheral enable register 1	PER1	R/W	√	√	—	00H
F007BH	Port mode select register	PMS	R/W	√	√	—	00H

Table 3 - 6 Extended SFR (2nd SFR) List (2/10)

Address	Special Function Register (SFR) Name	Symbol		R/W	Manipulable Bit Range			After Reset
					1-bit	8-bit	16-bit	
F007DH	Peripheral I/O redirection register 3	PIOR3		R/W	—	√	—	00H
F0090H	Data flash control register	DFLCTL		R/W	√	√	—	00H
F00A0H	High-speed on-chip oscillator trimming register	HIOTRM		R/W	—	√	—	Undefined Note 1
F00A8H	High-speed on-chip oscillator frequency select register	HOCODIV		R/W	—	√	—	The value set by FRQSEL2 to FRQSEL0 of the option byte (000C2H) Note 2
F00F0H	Peripheral enable register 0	PER0		R/W	√	√	—	00H
F00F3H	Subsystem clock supply mode control register	OSMC		R/W	—	√	—	00H
F00F5H	RAM parity error control register	RPECTL		R/W	√	√	—	00H
F00F9H	Power-on-reset status register	PORSR		R/W	—	√	—	00H Note 3
F00FDH	Peripheral enable register 2	PER2		R/W	√	√	—	00H
F00FEH	BCD correction result register	BCDADJ		R	—	√	—	Undefined
F0100H	Serial status register 00	SSR00L	SSR00	R	—	√	√	0000H
F0101H		—			—	—		
F0102H	Serial status register 01	SSR01L	SSR01	R	—	√	√	0000H
F0103H		—			—	—		
F0104H	Serial status register 02	SSR02L	SSR02	R	—	√	√	0000H
F0105H		—			—	—		
F0106H	Serial status register 03	SSR03L	SSR03	R	—	√	√	0000H
F0107H		—			—	—		
F0108H	Serial flag clear trigger register 00	SIR00L	SIR00	R/W	—	√	√	0000H
F0109H		—			—	—		
F010AH	Serial flag clear trigger register 01	SIR01L	SIR01	R/W	—	√	√	0000H
F010BH		—			—	—		
F010CH	Serial flag clear trigger register 02	SIR02L	SIR02	R/W	—	√	√	0000H
F010DH		—			—	—		
F010EH	Serial flag clear trigger register 03	SIR03L	SIR03	R/W	—	√	√	0000H
F010FH		—			—	—		
F0110H	Serial mode register 00	SMR00		R/W	—	—	√	0020H
F0111H								
F0112H	Serial mode register 01	SMR01		R/W	—	—	√	0020H
F0113H								
F0114H	Serial mode register 02	SMR02		R/W	—	—	√	0020H
F0115H								
F0116H	Serial mode register 03	SMR03		R/W	—	—	√	0020H
F0117H								
F0118H	Serial communication operation setting register 00	SCR00		R/W	—	—	√	0087H
F0119H								
F011AH	Serial communication operation setting register 01	SCR01		R/W	—	—	√	0087H
F011BH								
F011CH	Serial communication operation setting register 02	SCR02		R/W	—	—	√	0087H
F011DH								

Note 1. The value after a reset is adjusted at the time of shipment.

Note 2. The value after a reset is a value set in FRQSEL2 to FRQSEL0 of the option byte 000C2H.

Note 3. This register is reset only by a power-on reset.

Table 3 - 6 Extended SFR (2nd SFR) List (3/10)

Address	Special Function Register (SFR) Name	Symbol		R/W	Manipulable Bit Range			After Reset
					1-bit	8-bit	16-bit	
F011EH	Serial communication operation setting register 03	SCR03		R/W	—	—	√	0087H
F011FH								
F0120H	Serial channel enable status register 0	SE0L	SE0	R	√	√	√	0000H
F0121H		—			—	—		
F0122H	Serial channel start register 0	SS0L	SS0	R/W	√	√	√	0000H
F0123H		—			—	—		
F0124H	Serial channel stop register 0	ST0L	ST0	R/W	√	√	√	0000H
F0125H		—			—	—		
F0126H	Serial clock select register 0	SPS0L	SPS0	R/W	—	√	√	0000H
F0127H		—			—	—		
F0128H	Serial output register 0	SO0		R/W	—	—	√	0F0FH
F0129H								
F012AH	Serial output enable register 0	SOE0L	SOE0	R/W	√	√	√	0000H
F012BH		—			—	—		
F0134H	Serial output level register 0	SOL0L	SOL0	R/W	—	√	√	0000H
F0135H		—			—	—		
F0138H	Serial standby control register 0	SSC0L	SSC0	R/W	—	√	√	0000H
F0139H		—			—	—		
F0140H	Serial status register 10	SSR10L	SSR10	R	—	√	√	0000H
F0141H		—			—	—		
F0142H	Serial status register 11	SSR11L	SSR11	R	—	√	√	0000H
F0143H		—			—	—		
F0148H	Serial flag clear trigger register 10	SIR10L	SIR10	R/W	—	√	√	0000H
F0149H		—			—	—		
F014AH	Serial flag clear trigger register 11	SIR11L	SIR11	R/W	—	√	√	0000H
F014BH		—			—	—		
F0150H	Serial mode register 10	SMR10		R/W	—	—	√	0020H
F0151H								
F0152H	Serial mode register 11	SMR11		R/W	—	—	√	0020H
F0153H								

Table 3 - 6 Extended SFR (2nd SFR) List (4/10)

Address	Special Function Register (SFR) Name	Symbol		R/W	Manipulable Bit Range			After Reset
					1-bit	8-bit	16-bit	
F0158H	Serial communication operation setting register 10	SCR10		R/W	—	—	√	0087H
F0159H								
F015AH	Serial communication operation setting register 11	SCR11		R/W	—	—	√	0087H
F015BH								
F0160H	Serial channel enable status register 1	SE1L	SE1	R	√	√	√	0000H
F0161H		—			—	—		
F0162H	Serial channel start register 1	SS1L	SS1	R/W	√	√	√	0000H
F0163H		—			—	—		
F0164H	Serial channel stop register 1	ST1L	ST1	R/W	√	√	√	0000H
F0165H		—			—	—		
F0166H	Serial clock select register 1	SPS1L	SPS1	R/W	—	√	√	0000H
F0167H		—			—	—		
F0168H	Serial output register 1	SO1		R/W	—	—	√	0303H
F0169H								
F016AH	Serial output enable register 1	SOE1L	SOE1	R/W	√	√	√	0000H
F016BH		—			—	—		
F0174H	Serial output level register 1	SOL1L	SOL1	R/W	—	√	√	0000H
F0175H		—			—	—		
F0178H	Serial standby control register 1	SSC1L	SSC1	R/W	—	√	√	0000H
F0179H		—			—	—		
F0180H	Timer counter register 00	TCR00		R	—	—	√	FFFFH
F0181H								
F0182H	Timer counter register 01	TCR01		R	—	—	√	FFFFH
F0183H								
F0184H	Timer counter register 02	TCR02		R	—	—	√	FFFFH
F0185H								
F0186H	Timer counter register 03	TCR03		R	—	—	√	FFFFH
F0187H								
F0188H	Timer counter register 04	TCR04		R	—	—	√	FFFFH
F0189H								
F018AH	Timer counter register 05	TCR05		R	—	—	√	FFFFH
F018BH								
F018CH	Timer counter register 06	TCR06		R	—	—	√	FFFFH
F018DH								

Table 3 - 6 Extended SFR (2nd SFR) List (5/10)

Address	Special Function Register (SFR) Name	Symbol		R/W	Manipulable Bit Range			After Reset
					1-bit	8-bit	16-bit	
F018EH	Timer counter register 07	TCR07		R	—	—	√	FFFFH
F018FH								
F0190H	Timer mode register 00	TMR00		R/W	—	—	√	0000H
F0191H								
F0192H	Timer mode register 01	TMR01		R/W	—	—	√	0000H
F0193H								
F0194H	Timer mode register 02	TMR02		R/W	—	—	√	0000H
F0195H								
F0196H	Timer mode register 03	TMR03		R/W	—	—	√	0000H
F0197H								
F0198H	Timer mode register 04	TMR04		R/W	—	—	√	0000H
F0199H								
F019AH	Timer mode register 05	TMR05		R/W	—	—	√	0000H
F019BH								
F019CH	Timer mode register 06	TMR06		R/W	—	—	√	0000H
F019DH								
F019EH	Timer mode register 07	TMR07		R/W	—	—	√	0000H
F019FH								
F01A0H	Timer status register 00	TSR00L	TSR00	R	—	√	√	0000H
F01A1H		—			—	—		
F01A2H	Timer status register 01	TSR01L	TSR01	R	—	√	√	0000H
F01A3H		—			—	—		
F01A4H	Timer status register 02	TSR02L	TSR02	R	—	√	√	0000H
F01A5H		—			—	—		
F01A6H	Timer status register 03	TSR03L	TSR03	R	—	√	√	0000H
F01A7H		—			—	—		
F01A8H	Timer status register 04	TSR04L	TSR04	R	—	√	√	0000H
F01A9H		—			—	—		
F01AAH	Timer status register 05	TSR05L	TSR05	R	—	√	√	0000H
F01ABH		—			—	—		
F01ACH	Timer status register 06	TSR06L	TSR06	R	—	√	√	0000H
F01ADH		—			—	—		
F01AEH	Timer status register 07	TSR07L	TSR07	R	—	√	√	0000H
F01AFH		—			—	—		
F01B0H	Timer channel enable status register 0	TE0L	TE0	R	√	√	√	0000H
F01B1H		—			—	—		
F01B2H	Timer channel start register 0	TS0L	TS0	R/W	√	√	√	0000H
F01B3H		—			—	—		
F01B4H	Timer channel stop register 0	TT0L	TT0	R/W	√	√	√	0000H
F01B5H		—			—	—		

Table 3 - 6 Extended SFR (2nd SFR) List (6/10)

Address	Special Function Register (SFR) Name	Symbol		R/W	Manipulable Bit Range			After Reset
					1-bit	8-bit	16-bit	
F01B6H	Timer clock select register 0	TPS0		R/W	—	—	√	0000H
F01B7H								
F01B8H	Timer output register 0	TO0L	TO0	R/W	—	√	√	0000H
F01B9H		—			—	—		
F01BAH	Timer output enable register 0	TOE0L	TOE0	R/W	√	√	√	0000H
F01BBH		—			—	—		
F01BCH	Timer output level register 0	TOL0L	TOL0	R/W	—	√	√	0000H
F01BDH		—			—	—		
F01BEH	Timer output mode register 0	TOM0L	TOM0	R/W	—	√	√	0000H
F01BFH		—			—	—		
F01C0H	Event link setting register 00	ELSELR00		R/W	—	√	—	00H
F01C1H	Event link setting register 01	ELSELR01		R/W	—	√	—	00H
F01C2H	Event link setting register 02	ELSELR02		R/W	—	√	—	00H
F01C3H	Event link setting register 03	ELSELR03		R/W	—	√	—	00H
F01C4H	Event link setting register 04	ELSELR04		R/W	—	√	—	00H
F01C5H	Event link setting register 05	ELSELR05		R/W	—	√	—	00H
F01C6H	Event link setting register 06	ELSELR06		R/W	—	√	—	00H
F01C7H	Event link setting register 07	ELSELR07		R/W	—	√	—	00H
F01C8H	Event link setting register 08	ELSELR08		R/W	—	√	—	00H
F01C9H	Event link setting register 09	ELSELR09		R/W	—	√	—	00H
F01CAH	Event link setting register 10	ELSELR10		R/W	—	√	—	00H
F01CBH	Event link setting register 11	ELSELR11		R/W	—	√	—	00H
F01CCH	Event link setting register 12	ELSELR12		R/W	—	√	—	00H
F01CDH	Event link setting register 13	ELSELR13		R/W	—	√	—	00H
F01CEH	Event link setting register 14	ELSELR14		R/W	—	√	—	00H
F01CFH	Event link setting register 15	ELSELR15		R/W	—	√	—	00H
F01D0H	Event link setting register 16	ELSELR16		R/W	—	√	—	00H
F01D1H	Event link setting register 17	ELSELR17		R/W	—	√	—	00H
F01D2H	Event link setting register 18	ELSELR18		R/W	—	√	—	00H
F01D3H	Event link setting register 19	ELSELR19		R/W	—	√	—	00H
F01D4H	Event link setting register 20	ELSELR20		R/W	—	√	—	00H
F01D5H	Event link setting register 21	ELSELR21		R/W	—	√	—	00H
F01D6H	Event link setting register 22	ELSELR22		R/W	—	√	—	00H
F01D7H	Event link setting register 23	ELSELR23		R/W	—	√	—	00H
F01D8H	Event link setting register 24	ELSELR24		R/W	—	√	—	00H
F01D9H	Event link setting register 25	ELSELR25		R/W	—	√	—	00H
F0230H	IICA control register 00	IICCTL00		R/W	√	√	—	00H
F0231H	IICA control register 01	IICCTL01		R/W	√	√	—	00H
F0232H	IICA low-level width setting register 0	IICWL0		R/W	—	√	—	FFH
F0233H	IICA high-level width setting register 0	IICWH0		R/W	—	√	—	FFH
F0234H	Slave address register 0	SVA0		R/W	—	√	—	00H

Table 3 - 6 Extended SFR (2nd SFR) List (7/10)

Address	Special Function Register (SFR) Name	Symbol	R/W	Manipulable Bit Range			After Reset
				1-bit	8-bit	16-bit	
F0240H	Timer RJ control register 0	TRJCR0	R/W	—	√	—	00H
F0241H	Timer RJ I/O control register 0	TRJIOC0	R/W	√	√	—	00H
F0242H	Timer RJ mode register 0	TRJMR0	R/W	√	√	—	00H
F0243H	Timer RJ event pin select register 0	TRJISR0	R/W	√	√	—	00H
F0244H	Timer RJ control register 1	TRJCR1	R/W	—	√	—	00H
F0245H	Timer RJ I/O control register 1	TRJIOC1	R/W	√	√	—	00H
F0246H	Timer RJ mode register 1	TRJMR1	R/W	√	√	—	00H
F0247H	Timer RJ event pin select register 1	TRJISR1	R/W	√	√	—	00H
F026BH	External signal sampler control register 0	EXSDM0	R/W	√	√	—	00H
F0270H	SMOTD compare register A	SMOTDCRSA	R/W	—	√	—	00H
F0271H	SMOTD compare register B	SMOTDCRSB	R/W	—	√	—	00H
F0272H	SMOTD clock select register	SMOTDTCS	R/W	—	√	—	00H
F0273H	SMOTD control register	SMOTDCR	R/W	√	√	—	00H
F0274H	SMOTD sampling level setting register	SMOTDSMS	R/W	√	√	—	00H
F0275H	SMOTD sampling pin status register	SMOTDSMD	R	√	√	—	00H
F0276H	SMOTD output control register	SMOTDOE	R/W	√	√	—	00H
F0280H	Transmit buffer register 0	TXBMG0	R/W	—	√	—	FFH
F0281H	Receive buffer register 0	RXBMG0	R	—	√	—	FFH
F0282H	Operating mode setting register 00	ASIMMG00	R/W	√	√	—	01H
F0283H	Operating mode setting register 01	ASIMMG01	R/W	√	√	—	1AH
F0284H	Baud rate generator control register 0	BRGCMG0	R/W	—	√	—	FFH
F0285H	Status register 0	ASISMG0	R	—	√	—	00H
F0286H	Status clear trigger register 0	ASCTMG0	R/W	√	√	—	00H
F02CCH	UARTMG0 clock doubler control register	CLKDCTL	R/W	√	√	—	00H
F02E0H	DTC base address register	DTCBAR	R/W	—	√	—	FDH
F02E8H	DTC activation enable register 0	DTCEN0	R/W	√	√	—	00H
F02E9H	DTC activation enable register 1	DTCEN1	R/W	√	√	—	00H
F02EAH	DTC activation enable register 2	DTCEN2	R/W	√	√	—	00H
F02EBH	DTC activation enable register 3	DTCEN3	R/W	√	√	—	00H
F02ECH	DTC activation enable register 4	DTCEN4	R/W	√	√	—	00H
F02F0H	Flash memory CRC control register	CRC0CTL	R/W	√	√	—	00H
F02F2H	Flash memory CRC operation result register	PGCRCL	R/W	—	—	√	0000H
F02FAH	CRC data register	CRCD	R/W	—	—	√	0000H
F0300H	LCD port function register 0	PFSEG0	R/W	√	√	—	F0H
F0301H	LCD port function register 1	PFSEG1	R/W	√	√	—	FFH
F0302H	LCD port function register 2	PFSEG2	R/W	√	√	—	FFH
F0303H	LCD port function register 3	PFSEG3	R/W	√	√	—	FFH
F0304H	LCD port function register 4	PFSEG4	R/W	√	√	—	0FH
F0308H	LCD input switch control register	ISCLCD	R/W	√	√	—	00H
F0310H	Watch error correction register	SUBCUD	R/W	—	—	√	0020H Note
F0311H							

Note This register is reset only by a power-on reset.

Table 3 - 6 Extended SFR (2nd SFR) List (8/10)

Address	Special Function Register (SFR) Name	Symbol		R/W	Manipulable Bit Range			After Reset
					1-bit	8-bit	16-bit	
F0350H	8-bit interval timer compare register 00	TRTCMP00	TRTCMP0	R/W	—	√	√	FFH
F0351H	8-bit interval timer compare register 01	TRTCMP01		R/W	—	√		FFH
F0352H	8-bit interval timer control register 0	TRTCR0		R/W	√	√	—	00H
F0353H	8-bit interval timer division ratio register 0	TRTMD0		R/W	—	√	—	00H
F0354H	8-bit interval timer compare register 10	TRTCMP10	TRTCMP1	R/W	—	√	√	FFH
F0355H	8-bit interval timer compare register 11	TRTCMP11		R/W	—	√		FFH
F0356H	8-bit interval timer control register 1	TRTCR1		R/W	√	√	—	00H
F0357H	8-bit interval timer division ratio register 1	TRTMD1		R/W	—	√	—	00H
F0358H	8-bit interval timer compare register 20	TRTCMP20	TRTCMP2	R/W	—	√	√	FFH
F0359H	8-bit interval timer compare register 21	TRTCMP21		R/W	—	√		FFH
F035AH	8-bit interval timer control register 2	TRTCR2		R/W	√	√	—	00H
F035BH	8-bit interval timer division ratio register 2	TRTMD2		R/W	—	√	—	00H
F0400H	LCD display data memory 0	SEG0		R/W	—	√	—	00H
F0401H	LCD display data memory 1	SEG1		R/W	—	√	—	00H
F0402H	LCD display data memory 2	SEG2		R/W	—	√	—	00H
F0403H	LCD display data memory 3	SEG3		R/W	—	√	—	00H
F0404H	LCD display data memory 4	SEG4		R/W	—	√	—	00H
F0405H	LCD display data memory 5	SEG5		R/W	—	√	—	00H
F0406H	LCD display data memory 6	SEG6		R/W	—	√	—	00H
F0407H	LCD display data memory 7	SEG7		R/W	—	√	—	00H
F0408H	LCD display data memory 8	SEG8		R/W	—	√	—	00H
F0409H	LCD display data memory 9	SEG9		R/W	—	√	—	00H
F040AH	LCD display data memory 10	SEG10		R/W	—	√	—	00H
F040BH	LCD display data memory 11	SEG11		R/W	—	√	—	00H
F040CH	LCD display data memory 12	SEG12		R/W	—	√	—	00H
F040DH	LCD display data memory 13	SEG13		R/W	—	√	—	00H
F040EH	LCD display data memory 14	SEG14		R/W	—	√	—	00H
F040FH	LCD display data memory 15	SEG15		R/W	—	√	—	00H
F0410H	LCD display data memory 16	SEG16		R/W	—	√	—	00H
F0411H	LCD display data memory 17	SEG17		R/W	—	√	—	00H
F0412H	LCD display data memory 18	SEG18		R/W	—	√	—	00H
F0413H	LCD display data memory 19	SEG19		R/W	—	√	—	00H
F0414H	LCD display data memory 20	SEG20		R/W	—	√	—	00H
F0415H	LCD display data memory 21	SEG21		R/W	—	√	—	00H
F0416H	LCD display data memory 22	SEG22		R/W	—	√	—	00H
F0417H	LCD display data memory 23	SEG23		R/W	—	√	—	00H
F0418H	LCD display data memory 24	SEG24		R/W	—	√	—	00H

Table 3 - 6 Extended SFR (2nd SFR) List (9/10)

Address	Special Function Register (SFR) Name	Symbol		R/W	Manipulable Bit Range			After Reset
					1-bit	8-bit	16-bit	
F0419H	LCD display data memory 25	SEG25		R/W	—	√	—	00H
F041AH	LCD display data memory 26	SEG26		R/W	—	√	—	00H
F041BH	LCD display data memory 27	SEG27		R/W	—	√	—	00H
F041CH	LCD display data memory 28	SEG28		R/W	—	√	—	00H
F041DH	LCD display data memory 29	SEG29		R/W	—	√	—	00H
F041EH	LCD display data memory 30	SEG30		R/W	—	√	—	00H
F041FH	LCD display data memory 31	SEG31		R/W	—	√	—	00H
F0420H	LCD display data memory 32	SEG32		R/W	—	√	—	00H
F0421H	LCD display data memory 33	SEG33		R/W	—	√	—	00H
F0422H	LCD display data memory 34	SEG34		R/W	—	√	—	00H
F0423H	LCD display data memory 35	SEG35		R/W	—	√	—	00H
F0440H	Analog front-end power supply select register	AFEPWS		R/W	√	√	—	00H
F0441H	Analog front-end power supply detection register	AFEPWD		R	√	√	—	00H
F0442H	Analog front-end clock select register	AFECKS		R/W	—	√	—	00H
F0443H	Sensor reference voltage setting register	VSBIAS		R/W	—	√	—	19H
F0450H	ΔΣ A/D converter conversion result register C	DSAD CRC	DSADC R0	R	—	√	√	00H
F0451H	ΔΣ A/D converter conversion result register L	DSAD CRL		R	—	√		00H
F0452H	ΔΣ A/D converter conversion result register M	DSAD CRM	DSADC R1	R	—	√	√	00H
F0453H	ΔΣ A/D converter conversion result register H	DSAD CRH		R	—	√		00H
F0454H	ΔΣ A/D converter mean value register C	DSAD MVC	DSADM V0	R	—	√	√	00H
F0455H	ΔΣ A/D converter mean value register L	DSAD MVL		R	—	√		00H
F0456H	ΔΣ A/D converter mean value register M	DSAD MVM	DSADM V1	R	—	√	√	00H
F0457H	ΔΣ A/D converter mean value register H	DSAD MVH		R	—	√		00H
F0458H	ΔΣ A/D converter mode register	DSADMR		R/W	—	√	—	00H
F0459H	ΔΣ A/D converter control register	DSADCTL		R/W	√	√	—	00H
F045AH	Input multiplexer 0 setting register 0	PGA0CTL0		R/W	—	√	—	40H
F045BH	Input multiplexer 0 setting register 1	PGA0CTL1		R/W	—	√	—	10H
F045CH	Input multiplexer 0 setting register 2	PGA0CTL2		R/W	—	√	—	01H
F045DH	Input multiplexer 0 setting register 3	PGA0CTL3		R/W	—	√	—	00H
F045EH	Input multiplexer 1 setting register 0	PGA1CTL0		R/W	—	√	—	40H
F045FH	Input multiplexer 1 setting register 1	PGA1CTL1		R/W	—	√	—	10H
F0460H	Input multiplexer 1 setting register 2	PGA1CTL2		R/W	—	√	—	01H
F0461H	Input multiplexer 1 setting register 3	PGA1CTL3		R/W	—	√	—	00H
F0462H	Input multiplexer 2 setting register 0	PGA2CTL0		R/W	—	√	—	40H
F0463H	Input multiplexer 2 setting register 1	PGA2CTL1		R/W	—	√	—	10H
F0464H	Input multiplexer 2 setting register 2	PGA2CTL2		R/W	—	√	—	01H
F0465H	Input multiplexer 2 setting register 3	PGA2CTL3		R/W	—	√	—	00H
F0466H	Input multiplexer 3 setting register 0	PGA3CTL0		R/W	—	√	—	40H

Table 3 - 6 Extended SFR (2nd SFR) List (10/10)

Address	Special Function Register (SFR) Name	Symbol		R/W	Manipulable Bit Range			After Reset
					1-bit	8-bit	16-bit	
F0467H	Input multiplexer 3 setting register 1	PGA3CTL1		R/W	—	√	—	10H
F0468H	Input multiplexer 3 setting register 2	PGA3CTL2		R/W	—	√	—	01H
F0469H	Input multiplexer 3 setting register 3	PGA3CTL3		R/W	—	√	—	00H
F046EH	Disconnected line detection setting register	PGABOD		R/W	—	√	—	00H
F0470H	Amplifier mode control register	AMPMC		R/W	√	√	—	00H
F0471H	Amplifier trigger mode control register	AMPTRM		R/W	—	√	—	00H
F0472H	Amplifier ELC trigger select register	AMPTRS		R/W	—	√	—	00H
F0473H	Amplifier control register	AMPC		R/W	√	√	—	00H
F0474H	Amplifier control signal monitor register	AMPMON		R	—	√	—	00H
F0476H	Amplifier unit 0 gain setting register	PGA1GC		R/W	—	√	—	00H
F0477H	Amplifier unit 0 input select register	PGA1S		R/W	—	√	—	00H
F0478H	Amplifier unit 1 input select register	AMP0S		R/W	—	√	—	00H
F0479H	Amplifier unit 2 input select register	AMP1S		R/W	—	√	—	00H
F047AH	Amplifier unit 3 input select register	AMP2S		R/W	—	√	—	00H
F0480H	D/A conversion value setting register 0	DAC0DR		R/W	—	√	—	00H
F0482H	D/A conversion value setting register 1	DAC1DR		R/W	—	—	√	0000H
F0483H								
F0484H	D/A converter mode register 0	DACM0		R/W	—	√	—	00H
F0485H	D/A converter mode register 1	DACM1		R/W	—	√	—	00H
F0500H	8-bit interval timer counter register 00	TRT00	TRT0	R	—	√	√	00H
F0501H	8-bit interval timer counter register 01	TRT01		R	—	√		00H
F0502H	8-bit interval timer counter register 10	TRT10	TRT1	R	—	√	√	00H
F0503H	8-bit interval timer counter register 11	TRT11		R	—	√		00H
F0504H	8-bit interval timer counter register 20	TRT20	TRT2	R	—	√	√	00H
F0505H	8-bit interval timer counter register 21	TRT21		R	—	√		00H
F0508H	Timer RJ counter register 0	TRJ0		R/W	—	—	√	FFFFH
F0509H								
F050AH	Timer RJ counter register 1	TRJ1		R/W	—	—	√	FFFFH
F050BH								

Remark For SFRs in the SFR area, see **Table 3 - 5 SFR List**.

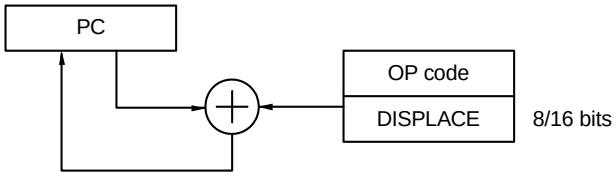
3.4 Instruction Address Addressing

3.4.1 Relative addressing

[Function]

Relative addressing stores in the program counter (PC) the result of adding a displacement value included in the instruction word (signed complement data: -128 to +127 or -32768 to +32767) to the program counter (PC)'s value (the start address of the next instruction), and specifies the program address to be used as the branch destination. Relative addressing is applied only to branch instructions.

Figure 3 - 13 Outline of Relative Addressing



3.4.2 Immediate addressing

[Function]

Immediate addressing stores immediate data of the instruction word in the program counter, and specifies the program address to be used as the branch destination.

For immediate addressing, CALL !!addr20 or BR !!addr20 is used to specify 20-bit addresses and CALL !addr16 or BR !addr16 is used to specify 16-bit addresses. 0000 is set to the higher 4 bits when specifying 16-bit addresses.

Figure 3 - 14 Example of CALL !!addr20/BR !!addr20

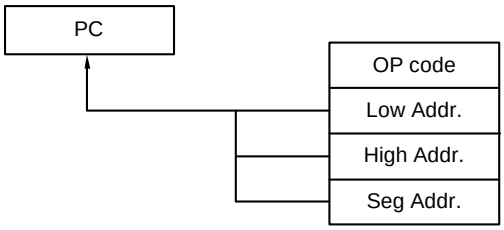
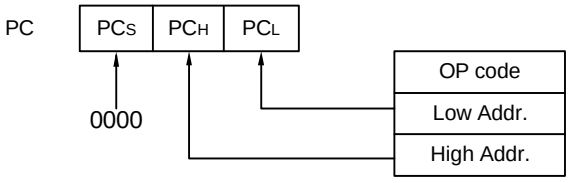


Figure 3 - 15 Example of CALL !addr16/BR !addr16



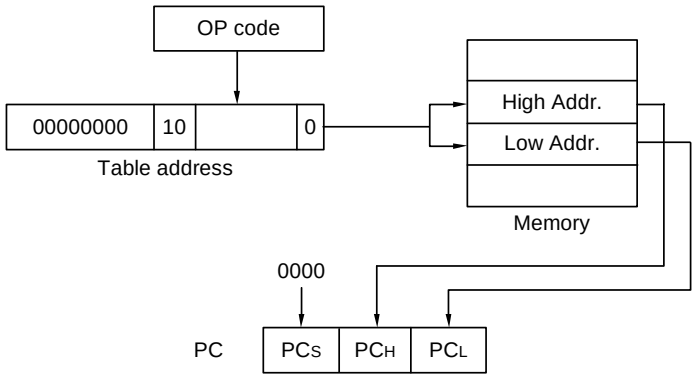
3.4.3 Table indirect addressing

[Function]

Table indirect addressing specifies a table address in the CALLT table area (0080H to 00BFH) with the 5-bit immediate data in the instruction word, stores the contents at that table address and the next address in the program counter (PC) as 16-bit data, and specifies the program address. Table indirect addressing is applied only for CALLT instructions.

In the RL78 microcontrollers, branching is enabled only to the 64 KB space from 00000H to 0FFFFH.

Figure 3 - 16 Outline of Table Indirect Addressing

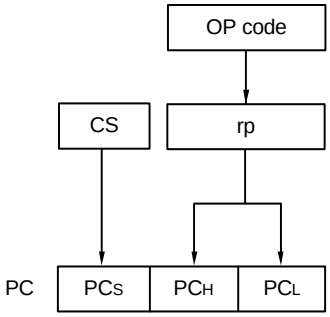


3.4.4 Register indirect addressing

[Function]

Register direct addressing stores in the program counter (PC) the contents of a general-purpose register pair (AX/BC/DE/HL) and CS register of the current register bank specified with the instruction word as 20-bit data, and specifies the program address. Register indirect addressing can be applied only to the CALL AX, BC, DE, HL, and BR AX instructions.

Figure 3 - 17 Outline of Register Indirect Addressing



3.5 Addressing for Processing Data Addresses

3.5.1 Implied addressing

[Function]

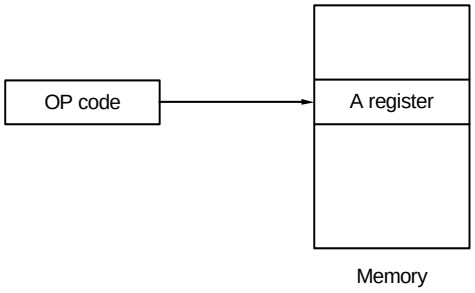
Instructions for accessing registers (such as accumulators) that have special functions are directly specified with the instruction word, without using any register specification field in the instruction word.

[Operand format]

Because implied addressing can be automatically employed with an instruction, no particular operand format is necessary.

Implied addressing can be applied only to MULU X.

Figure 3 - 18 Outline of Implied Addressing



3.5.2 Register addressing

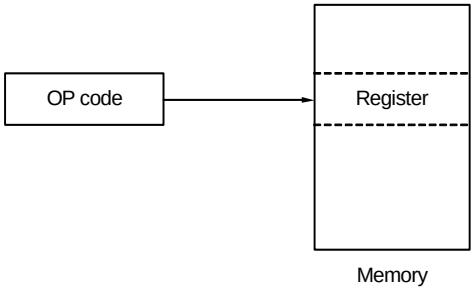
[Function]

Register addressing accesses a general-purpose register as an operand. The instruction word of 3-bit long is used to select an 8-bit register and the instruction word of 2-bit long is used to select a 16-bit register.

[Operand format]

Identifier	Description
r	X, A, C, B, E, D, L, H
rp	AX, BC, DE, HL

Figure 3 - 19 Outline of Register Addressing



3.5.3 Direct addressing

[Function]

Direct addressing uses immediate data in the instruction word as an operand address to directly specify the target address.

[Operand format]

Identifier	Description
!addr16	Label or 16-bit immediate data (only the space from F0000H to FFFFFH is specifiable)
ES:!addr16	Label or 16-bit immediate data (higher 4-bit addresses are specified by the ES register)

Figure 3 - 20 Example of !addr16

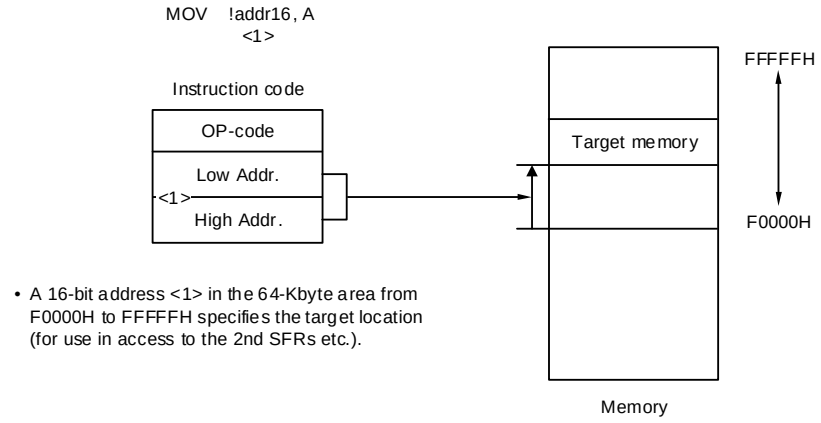
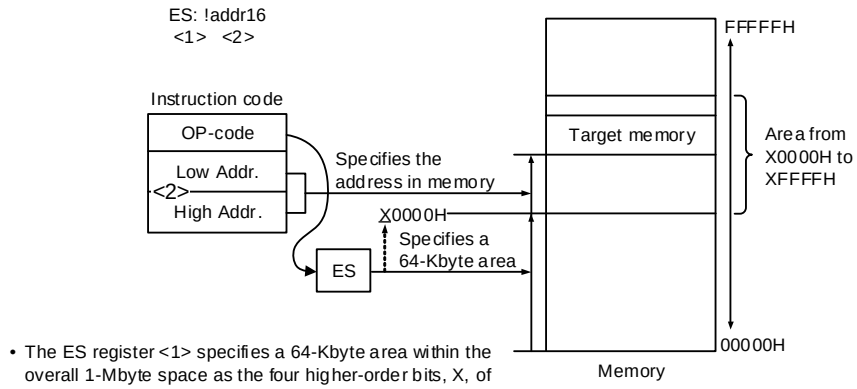


Figure 3 - 21 Example of ES:!addr16



3.5.4 Short direct addressing

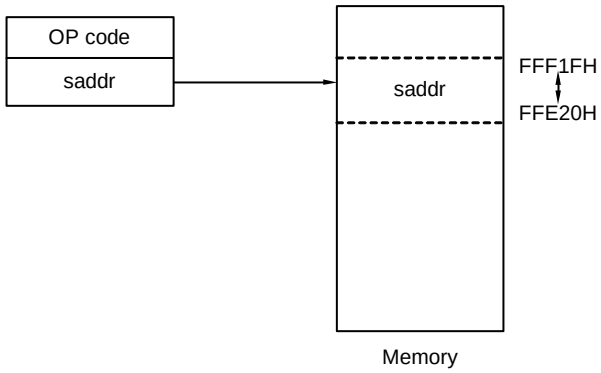
[Function]

Short direct addressing directly specifies the target addresses using 8-bit data in the instruction word. This type of addressing is applied only to the space from FFE20H to FFF1FH.

[Operand format]

Identifier	Description
SADDR	Label, FFE20H to FFF1FH immediate data, or 0FE20H to 0FF1FH immediate data (only the space from FFE20H to FFF1FH is specifiable)
SADDRP	Label, FFE20H to FFF1FH immediate data, or 0FE20H to 0FF1FH immediate data (even address only) (only the space from FFE20H to FFF1FH is specifiable)

Figure 3 - 22 Outline of Short Direct Addressing



Remark SADDR and SADDRP are used to describe the values of addresses FE20H to FF1FH with 16-bit immediate data (higher 4 bits of actual address are omitted), and the values of addresses FFE20H to FFF1FH with 20-bit immediate data.
Regardless of whether SADDR or SADDRP is used, addresses within the space from FFE20H to FFF1FH are specified for the memory.

3.5.5 SFR addressing

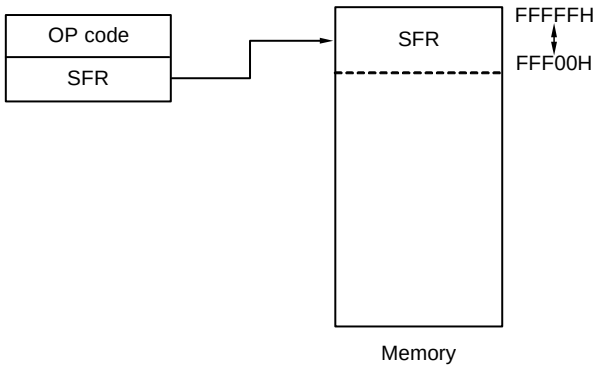
[Function]

SFR addressing directly specifies the target SFR addresses using 8-bit data in the instruction word. This type of addressing is applied only to the space from FFF00H to FFFFFH.

[Operand format]

Identifier	Description
SFR	SFR name
SFRP	16-bit-manipulatable SFR name (even address only)

Figure 3 - 23 Outline of SFR Addressing



3.5.6 Register indirect addressing

[Function]

Register indirect addressing directly specifies the target addresses using the contents of the register pair specified with the instruction word as an operand address.

[Operand format]

Identifier	Description
—	[DE], [HL] (only the space from F0000H to FFFFFH is specifiable)
—	ES:[DE], ES:[HL] (higher 4-bit addresses are specified by the ES register)

Figure 3 - 24 Example of [DE], [HL]

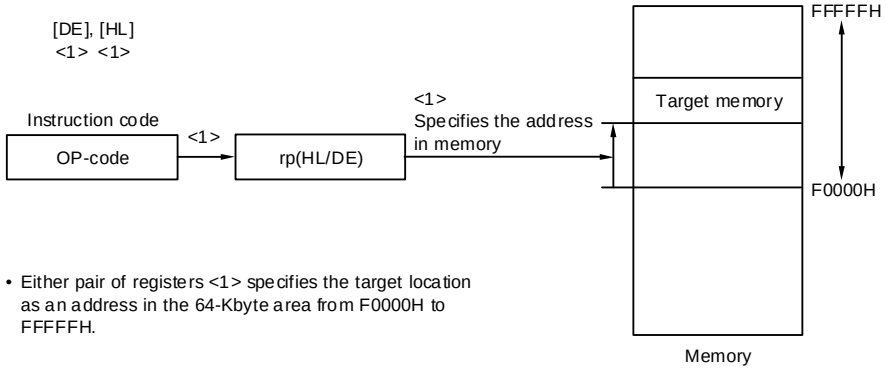
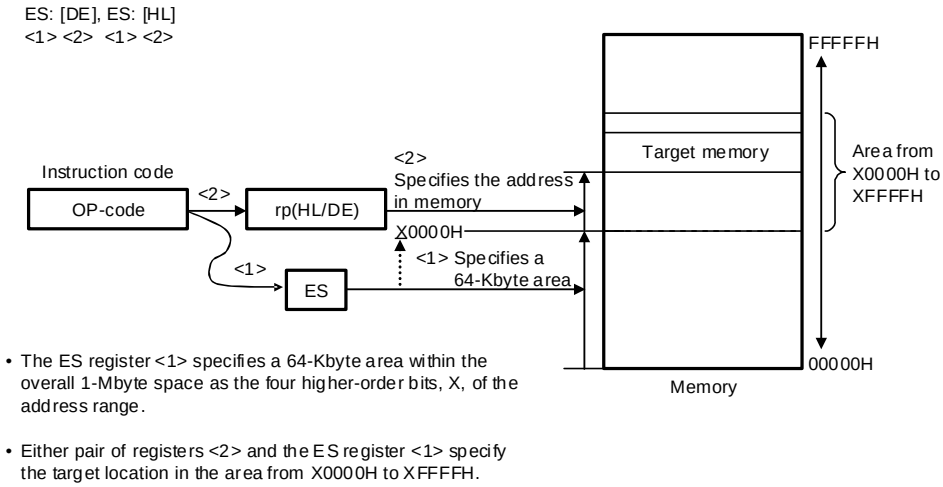


Figure 3 - 25 Example of ES:[DE], ES:[HL]



3.5.7 Based addressing

[Function]

Based addressing uses the contents of a register pair specified with the instruction word or 16-bit immediate data as a base address, and 8-bit immediate data or 16-bit immediate data as offset data. The sum of these values is used to specify the target address.

[Operand format]

Identifier	Description
—	[HL + byte], [DE + byte], [SP + byte] (only the space from F0000H to FFFFFH is specifiable)
—	word[B], word[C] (only the space from F0000H to FFFFFH is specifiable)
—	word[BC] (only the space from F0000H to FFFFFH is specifiable)
—	ES:[HL + byte], ES:[DE + byte] (higher 4-bit addresses are specified by the ES register)
—	ES:word[B], ES:word[C] (higher 4-bit addresses are specified by the ES register)
—	ES:word[BC] (higher 4-bit addresses are specified by the ES register)

Figure 3 - 26 Example of [SP+byte]

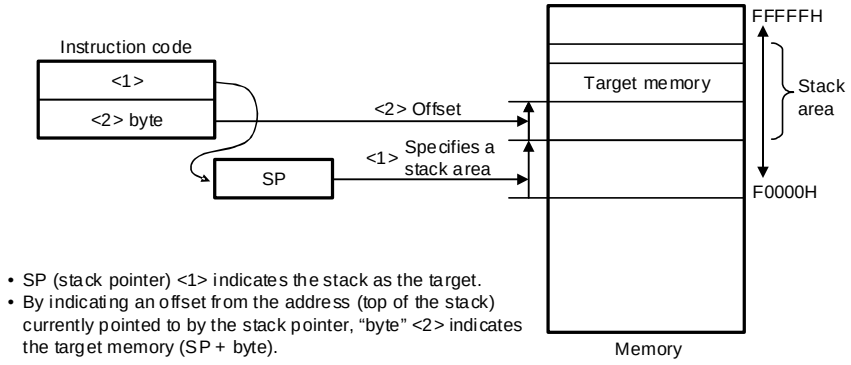
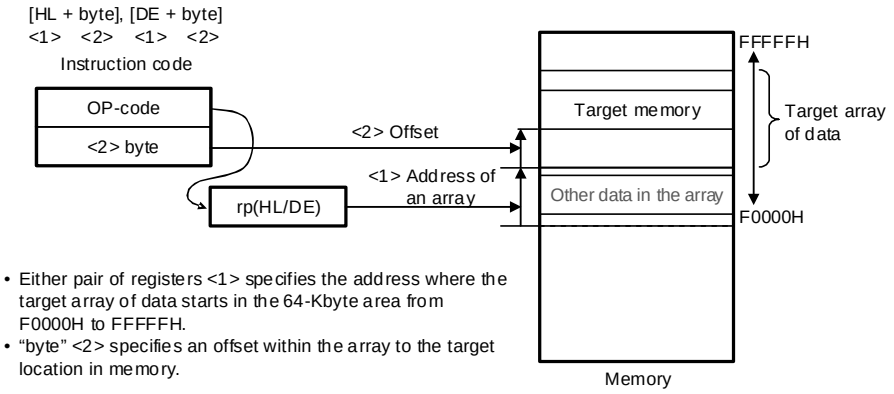
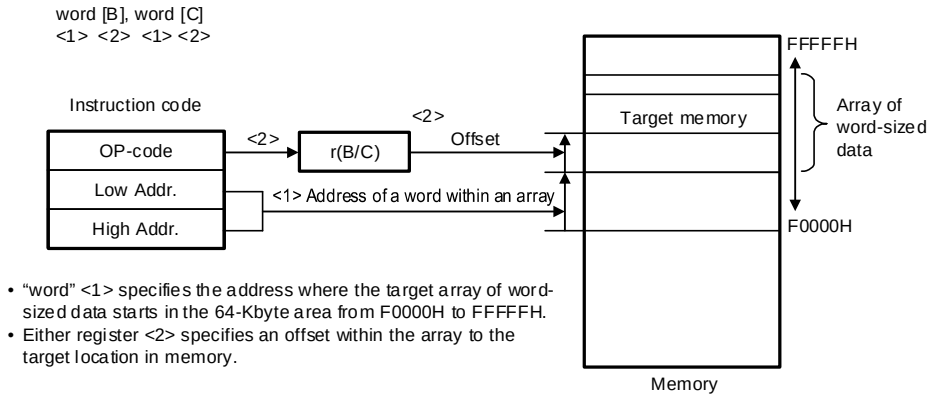


Figure 3 - 27 Example of [HL + byte], [DE + byte]]



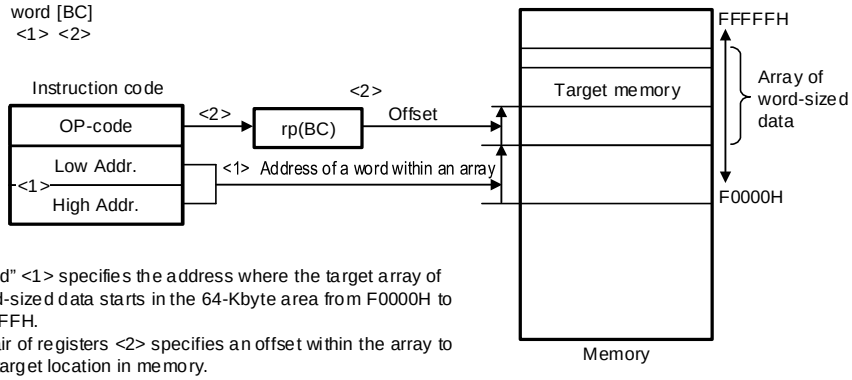
- Either pair of registers <1> specifies the address where the target array of data starts in the 64-Kbyte area from F0000H to FFFFFH.
- "byte" <2> specifies an offset within the array to the target location in memory.

Figure 3 - 28 Example of word[B], word[C]



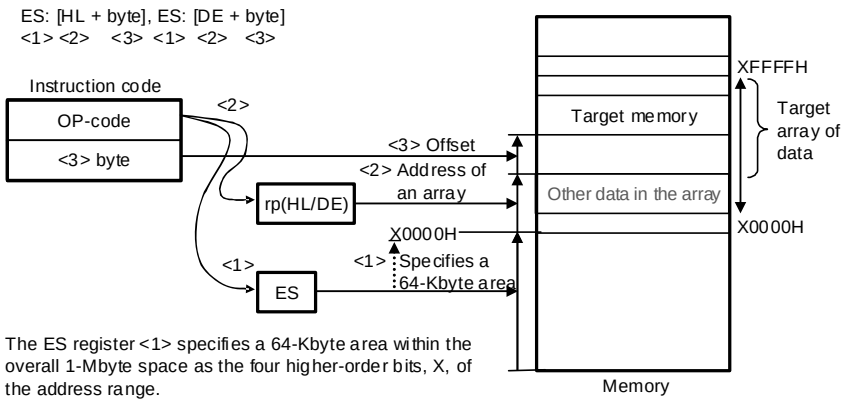
- "word" <1> specifies the address where the target array of word-sized data starts in the 64-Kbyte area from F0000H to FFFFFH.
- Either register <2> specifies an offset within the array to the target location in memory.

Figure 3 - 29 Example of word[BC]



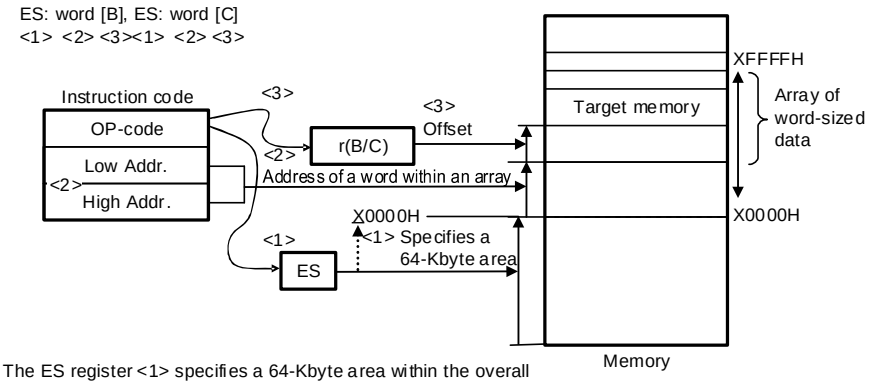
- "word" <1> specifies the address where the target array of word-sized data starts in the 64-Kbyte area from F0000H to FFFFFH.
- A pair of registers <2> specifies an offset within the array to the target location in memory.

Figure 3 - 30 Example of ES:[HL + byte], ES:[DE + byte]]



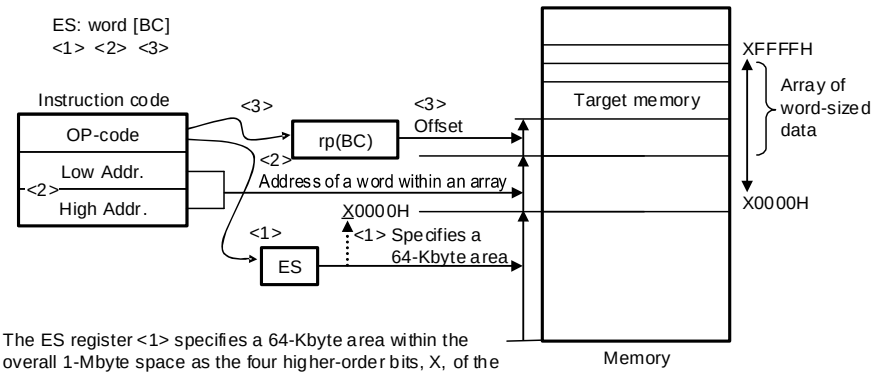
- The ES register <1> specifies a 64-Kbyte area within the overall 1-Mbyte space as the four higher-order bits, X, of the address range.
- Either pair of registers <2> specifies the address where the target array of data starts in the 64-Kbyte area specified in the ES register <1>.
- “byte” <3> specifies an offset within the array to the target location in memory.

Figure 3 - 31 Example of ES:word[B], ES:word[C]



- The ES register <1> specifies a 64-Kbyte area within the overall 1-Mbyte space as the four higher-order bits, X, of the address range.
- “word” <2> specifies the address where the target array of word-sized data starts in the 64-Kbyte area specified in the ES register <1>.
- Either register <3> specifies an offset within the array to the target location in memory.

Figure 3 - 32 Example of ES:word[BC]



- The ES register <1> specifies a 64-Kbyte area within the overall 1-Mbyte space as the four higher-order bits, X, of the address range.
- “word” <2> specifies the address where the target array of word-sized data starts in the 64-Kbyte area specified in the ES register <1>.
- A pair of registers <3> specifies an offset within the array to the target location in memory.

3.5.8 Based indexed addressing

[Function]

Based indexed addressing uses the contents of a register pair specified with the instruction word as the base address, and the content of the B register or C register similarly specified with the instruction word as offset address. The sum of these values is used to specify the target address.

[Operand format]

Identifier	Description
—	[HL+B], [HL+C] (only the space from F0000H to FFFFFH is specifiable)
—	ES:[HL+B], ES:[HL+C] (higher 4-bit addresses are specified by the ES register)

Figure 3 - 33 Example of [HL+B], [HL+C]

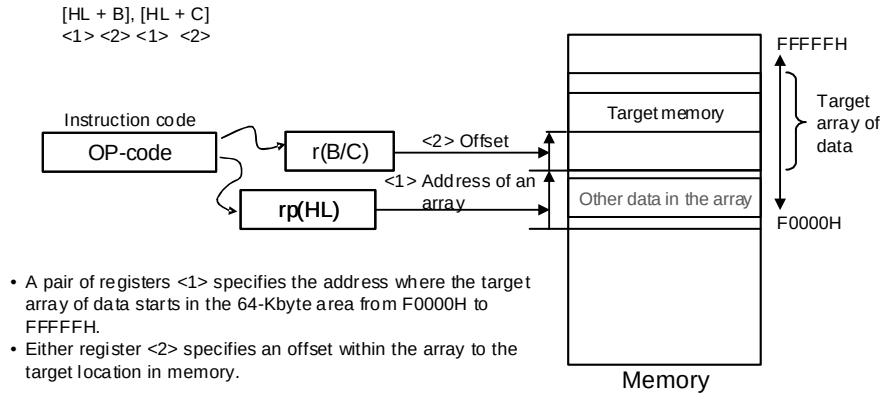
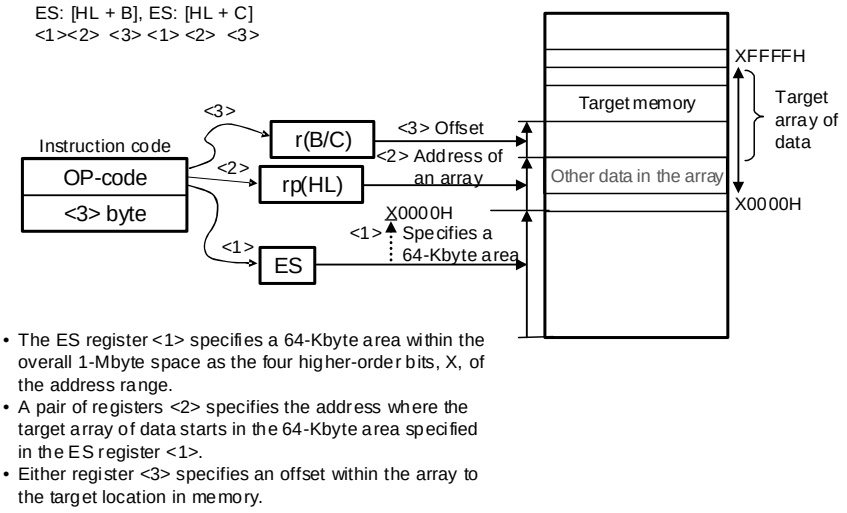


Figure 3 - 34 Example of ES:[HL+B], ES:[HL+C]



3.5.9 Stack addressing

[Function]

The stack area is indirectly addressed with the stack pointer (SP) values. This addressing is automatically employed when the PUSH, POP, subroutine call, and return instructions are executed or the register is saved/restored upon generation of an interrupt request.

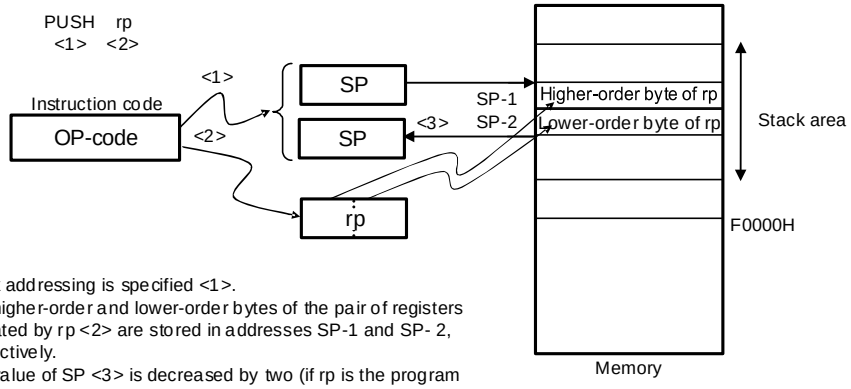
Only the internal RAM area can be set as the stack area.

[Description format]

Identifier	Description
—	PUSH PSW AX/BC/DE/HL POP PSW AX/BC/DE/HL CALL/CALLT RET BRK RETB (Interrupt request generated) RETI

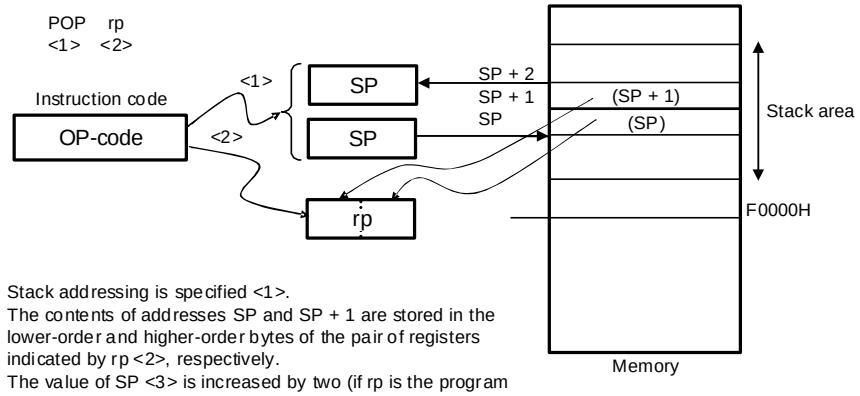
The data to be saved/restored by each stack operation is shown in Figures 3 - 35 to 3 - 40.

Figure 3 - 35 Example of PUSH rp



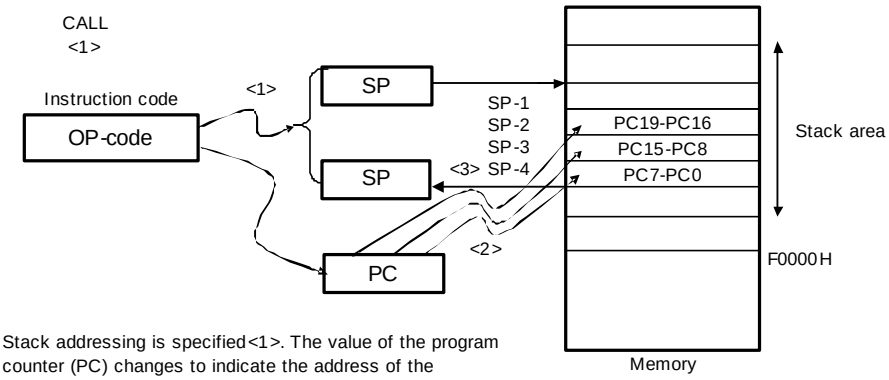
- Stack addressing is specified <1>.
- The higher-order and lower-order bytes of the pair of registers indicated by rp <2> are stored in addresses SP-1 and SP- 2, respectively.
- The value of SP <3> is decreased by two (if rp is the program status word (PSW), the value of the PSW is stored in SP-1 and 0 is stored in SP- 2).

Figure 3 - 36 Example of POP



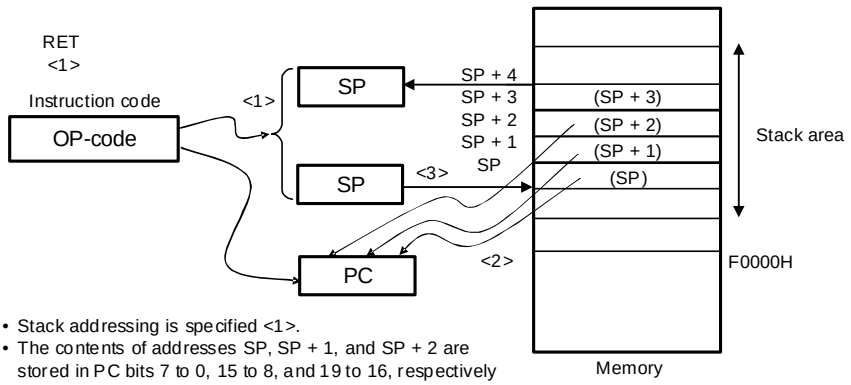
- Stack addressing is specified <1>.
- The contents of addresses SP and SP + 1 are stored in the lower-order and higher-order bytes of the pair of registers indicated by rp <2>, respectively.
- The value of SP <3> is increased by two (if rp is the program status word (PSW), the content of address SP + 1 is stored in the PSW).

Figure 3 - 37 Example of CALL, CALLT



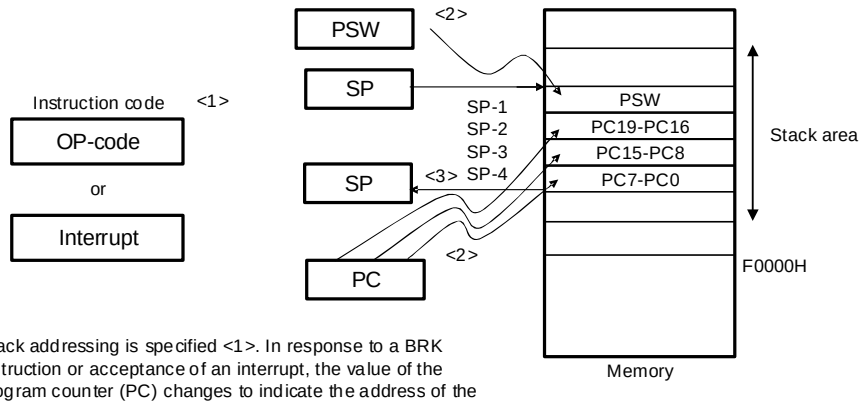
- Stack addressing is specified<1>. The value of the program counter (PC) changes to indicate the address of the instruction following the CALL instruction
- The values of PC bits19 to 16, 15 to 8, and 7 to 0 are stored in addresses SP - 2, SP - 3, and SP - 4, respectively <2>.
- The value of the SP <3> is decreased by 4.

Figure 3 - 38 Example of RET



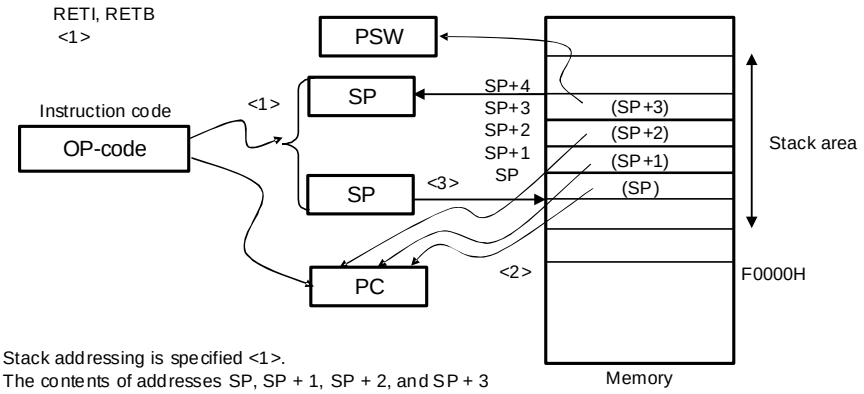
- Stack addressing is specified <1>.
- The contents of addresses SP, SP + 1, and SP + 2 are stored in PC bits 7 to 0, 15 to 8, and 19 to 16, respectively <2>.
- The value of SP <3> is increased by four.

Figure 3 - 39 Example of Interrupt, BRK



- Stack addressing is specified <1>. In response to a BRK instruction or acceptance of an interrupt, the value of the program counter (PC) changes to indicate the address of the next instruction.
- The values of the PSW, PC bits 19 to 16, 15 to 8, and 7 to 0 are stored in addresses SP-1, SP-2, SP-3, and SP-4, respectively <2>.
- The value of the SP <3> is decreased by 4.

Figure 3 - 40 Example of RETI, RETB



- Stack addressing is specified <1>.
- The contents of addresses SP, SP + 1, SP + 2, and SP + 3 are stored in PC bits 7 to 0, 15 to 8, 19 to 16, and the PSW, respectively <2>.
- The value of SP <3> is increased by four.

CHAPTER 4 PORT FUNCTIONS

4.1 Port Functions

The RL78/H1D microcontrollers are provided with digital I/O ports, which enable variety of control operations.
In addition to the function as digital I/O ports, these ports have several alternate functions. For details of the alternate functions, see **CHAPTER 2 PIN FUNCTIONS**.

4.2 Port Configuration (R5F11N, R5F11P)

Ports include the following hardware.

Table 4 - 1 Port Configuration

Item	Configuration
Control registers	Port mode registers (PM0, PM1, PM3 to PM8, PM12) Port registers (P0, P1, P3 to P8, P12, P13) Pull-up resistor option registers (PU0, PU1, PU3 to PU5, PU7, PU8, PU12) Port input mode registers (PIM0, PIM1, PIM3 to PIM5, PIM8) Port output mode registers (POM0, POM1, POM3 to POM5, POM8) Port mode control registers (PMC0, PMC1) Peripheral I/O redirection registers (PIOR0 to PIOR3) LCD port function registers (PFSEG0 to PFSEG4) LCD input switch control register (ISCLCD)
Port	• R5F11NM: Total: 53 (CMOS I/O: 46 (N-ch open drain I/O [V_{DD} tolerance]: 18), CMOS input: 5, N-ch open-drain I/O [6 V tolerance]: 2) • R5F11NL: Total: 36 (CMOS I/O: 29 (N-ch open drain I/O [V_{DD} tolerance]: 9), CMOS input: 5, N-ch open-drain I/O [6 V tolerance]: 2) • R5F11PL, R5F11NG: Total: 29 (CMOS I/O: 22 (N-ch open drain I/O [V_{DD} tolerance]: 12), CMOS input: 5, N-ch open-drain I/O [6 V tolerance]: 2)

4.2.1 Port 0

Port 0 is an I/O port with an output latch. Port 0 can be set to the input mode or output mode in 1-bit units using port mode register 0 (PM0). When the P01 to P07 pins are used as an input port, use of an on-chip pull-up resistor can be specified in 1-bit units by pull-up resistor option register 0 (PU0).

Input to the P03Note 2, P04, and P07 pins can be specified through a normal input buffer or a TTL input buffer in 1-bit units using port input mode register 0 (PIM0).

Output from the P02, P03Note 2, P04, P06, and P07 pins can be specified as N-ch open-drain output (V_{DD} tolerance) in 1-bit units using port output mode register 0 (POM0).

To use the P03Note 3, P04Note 4, P05Note 3, and P10Note 5 pins as digital input/output pins, set them in the digital I/O mode by using port mode control register 0 (PMC0) (can be specified in 1-bit units).

To use the P03Note 3, P04Note 4, P05 Note 3, and P10Note 5 pins as analog input pins, set them in the analog input mode by using port mode control register 0 (PMC0) (can be specified in 1-bit units).

This port can also be used for segment output of LCD controller/driver, serial interface data I/O, clock I/O, timer I/O, external interrupt request input, clock output/buzzer output, and 10-bit A/D converter analog input.

When reset signal is generated, the following configuration will be set.

• P01 to P07 pins of R5F11NM	Digital input invalid Note 1
• P06 and P07 pins of R5F11NL	Digital input invalid Note 1
• P03 and P05 pins of R5F11NL	Analog input
• P03 to P05 pins of R5F11NG and R5F11PL	Analog input
• P01, P02, P06, and P07 pins of R5F11NG and R5F11PL	Input port

Note 1. “Digital input invalid” refers to the state in which all the digital outputs, digital inputs, and LCD outputs are disabled.

Note 2. R5F11NM, R5F11NG, and R5F11PL only.

Note 3. R5F11NL, R5F11NG, and R5F11PL only.

Note 4. R5F11NG and R5F11PL only.

Note 5. R5F11NL only.

4.2.2 Port 1

Port 1 is an I/O port with an output latch. Port 1 can be set to the input mode or output mode in 1-bit units using port mode register 1 (PM1). When the P10 to P17 pins are used as an input port, use of an on-chip pull-up resistor can be specified in 1-bit units by pull-up resistor option register 1 (PU1).

Input to the P10 pin can be specified through a normal input buffer or a TTL input buffer in 1-bit units using port input mode register 1 (PIM1).

Output from the P10 pin can be specified as N-ch open-drain output (V_{DD} tolerance) in 1-bit units using port output mode register 1 (POM1).

To use the P11Note 2 pin as digital input/output pin, set the pin in the digital I/O mode by using port mode control register 1 (PMC1) (can be specified in 1-bit units).

To use the P11Note 2 pin as analog input pin, set the pin in the analog input mode by using port mode control register 1 (PMC1) (can be specified in 1-bit units).

This port can also be used for serial interface clock I/O, external interrupt request input, segment output of LCD controller/driver, 10-bit A/D converter analog input, and timer I/O.

When reset signal is generated, the following configuration will be set.

- P10 to P16 pins of R5F11NM — Digital input invalid Note 1
- P17 pin of R5F11NL — Input port
- P10 and P12 to P15 pins of R5F11NL — Digital input invalid Note 1
- P11 pin of R5F11NG and R5F11PL — Analog input
- P10 pin of R5F11NG and R5F11PL — Input port

Note 1. “Digital input invalid” refers to the state in which all the digital outputs, digital inputs, and LCD outputs are disabled.

Note 2. R5F11NL only.

4.2.3 Port 3

Port 3 is an I/O port with an output latch. Port 3 can be set to the input mode or output mode in 1-bit units using port mode register 3 (PM3). When the P30 to P32 and P35 to P37 pins are used as an input port, use of an on-chip pull-up resistor can be specified in 1-bit units by pull-up resistor option register 3 (PU3).

Input to the P35 and P36 pins can be specified through a normal input buffer or a TTL input buffer in 1-bit units using port input mode register 3 (PIM3).

Output from the P35 to P37 pins can be specified as N-ch open-drain output (V_{DD} tolerance) in 1-bit units using port output mode register 3 (POM3).

This port can also be used for external interrupt request input, real-time clock 2 correction clock output, serial interface clock I/O, data I/O, slave select input, timer I/O, clock output/buzzer output, segment output of LCD controller/driver, and programming UART transmission/reception.

When reset signal is generated, the following configuration will be set.

- P30 to P32 and P35 to P37 pins of R5F11NM and R5F11NL — Digital input invalid Note
- P30, P32, and P35 to P37 pins of R5F11NG and R5F11PL — Input port

Note “Digital input invalid” refers to the state in which all the digital outputs, digital inputs, and LCD outputs are disabled.

4.2.4 Port 4

Port 4 is an I/O port with an output latch. Port 4 can be set to the input mode or output mode in 1-bit units using port mode register 4 (PM4). To use the P40, P43, and P44 pins as input ports, use of an on-chip pull-up resistor can be specified by setting pull-up resistor option register 4 (PU4).

Input to the P40Note and P43 pins can be specified through a normal input buffer or a TTL input buffer in 1-bit units using port input mode register 4 (PIM4).

Output from the P40Note, P43, and P44 pins can be specified as N-ch open-drain output (V_{DD} tolerance) in 1-bit units using port output mode register 4 (POM4).

This port can also be used for external interrupt request input, timer I/O, serial interface clock I/O, data I/O, and data I/O for a flash memory programmer/debugger.

Reset signal generation sets port 4 to input mode.

Note R5F11NM only.

4.2.5 Port 5

Port 5 is an I/O port with an output latch. Port 5 can be set to the input mode or output mode in 1-bit units using port mode register 5 (PM5). When the P50 to P53 pins are used as an input port, use of an on-chip pull-up resistor can be specified in 1-bit units by pull-up resistor option register 5 (PU5).

Input to the P51 and P52 pins can be specified through a normal input buffer or a TTL input buffer in 1-bit units using port input mode register 5 (PIM5).

Output from the P50 to P52 pins can be specified as N-ch open-drain output (V_{DD} tolerance) in 1-bit units using port output mode register 5 (POM5).

This port can also be used for external interrupt request input, timer I/O, serial interface clock I/O, data I/O, and segment output of LCD controller/driver.

When reset signal is generated, the following configuration will be set.

- P50 to P53 pins of R5F11NM — Digital input invalid Note
- P50 to P52 pins of R5F11NL — Digital input invalid Note
- P50 to P53 pins of R5F11NG and R5F11PL — Input port

Note “Digital input invalid” refers to the state in which all the digital outputs, digital inputs, and LCD outputs are disabled.

4.2.6 Port 6

Port 6 is an I/O port with an output latch. Port 6 can be set to the input mode or output mode in 1-bit units using port mode register 6 (PM6).

The output of the P60 and P61 pins is N-ch open-drain output (6 V tolerance).

This port can also be used for serial interface data I/O, clock I/O, and external interrupt request input.

Reset signal generation sets port 6 to input mode.

4.2.7 Port 7

Port 7 is an I/O port with an output latch. Port 7 can be set to the input mode or output mode in 1-bit units using port mode register 7 (PM7). When the P70 to P77 pins are used as an input port, use of an on-chip pull-up resistor can be specified in 1-bit units by pull-up resistor option register 7 (PU7).
This port can also be used for timer I/O and segment output of LCD controller/driver.
When reset signal is generated, the following configuration will be set.

- P70 to P77 pins of R5F11NM — Digital input invalid Note
- P70, P71, P76, and P77 pins of R5F11NL — Digital input invalid Note
- P70, P71, P76, and P77 pins of R5F11NG and R5F11PL — Input port

Note “Digital input invalid” refers to the state in which all the digital outputs, digital inputs, and LCD outputs are disabled.

4.2.8 Port 8

Port 8 is an I/O port with an output latch. Port 8 can be set to the input mode or output mode in 1-bit units using port mode register 8 (PM8). When the P80 to P86 pins are used as an input port, use of an on-chip pull-up resistor can be specified in 1-bit units by pull-up resistor option register 8 (PU8).
Input to the P81 and P82Note pins can be specified through a normal input buffer or a TTL input buffer in 1-bit units using port input mode register 8 (PIM8).
Output from the P80, P81, and P82Note pins can be specified as N-ch open-drain output (V_{DD} tolerance) in 1-bit units using port output mode register 8 (POM8).
This port can also be used for serial interface clock I/O, data I/O, external interrupt request input, and timer I/O.
Reset signal generation sets P80 to P86 to the input mode.

Note R5F11NM only.

4.2.9 Port 12

P125 to P127 are I/O ports with output latches. P125 to P127 can be set to the input mode or output mode in 1-bit units using port mode register 12 (PM12). When the P125 to P127 pins are used as an input port, use of an on-chip pull-up resistor can be specified by pull-up resistor option register 12 (PU12).
P121 to P124 are 4-bit input ports.
This port can also be used for external interrupt request input, timer I/O, connecting resonator for main system clock, connecting resonator for subsystem clock, external clock input for main system clock, external clock input for subsystem clock, connecting a capacitor for LCD controller/driver, and power supply voltage pin for driving the LCD.
Reset signal generation sets P121 to P124 to input mode, and sets P125 to P127 to digital input invalid modeNote.

Note “Digital input invalid” refers to the state in which all the digital outputs, digital inputs, and LCD outputs are disabled.

4.2.10 Port 13

P137 is a 1-bit input-only port.
P137 is fixed an input ports.
This port can also be used for external interrupt request input and serial interface slave select input.

4.3 Port Configuration (R5F11R)

Ports include the following hardware.

Table 4 - 2 Port Configuration

Item	Configuration
Control registers	Port mode registers (PM0 to PM8, PM12, PM15) Port registers (P0 to P8, P12, P13, P15) Pull-up resistor option registers (PU0 to PU5, PU7, PU8, PU12, PU15) Port input mode registers (PIM0, PIM1, PIM3 to PIM5, PIM8) Port output mode registers (POM0, POM1, POM3 to POM5, POM8) Port mode control registers (PMC0) Peripheral I/O redirection registers (PIOR0 to PIOR3) LCD port function registers (PFSEG0 to PFSEG4) LCD input switch control register (ISCLCD)
Port	Total: 63 (CMOS I/O: 56 (N-ch open drain I/O [V_{DD} tolerance]: 19), CMOS input: 5, N-ch open-drain I/O [6 V tolerance]: 2)

4.3.1 Port 0

Port 0 is an I/O port with an output latch. Port 0 can be set to the input mode or output mode in 1-bit units using port mode register 0 (PM0). When the P01 to P07 pins are used as an input port, use of an on-chip pull-up resistor can be specified in 1-bit units by pull-up resistor option register 0 (PU0).

Input to the P03, P04, and P07 pins can be specified through a normal input buffer or a TTL input buffer in 1-bit units using port input mode register 0 (PIM0).

Output from the P02 to P04, P06, and P07 pins can be specified as N-ch open-drain output (V_{DD} tolerance) in 1-bit units using port output mode register 0 (POM0).

To use the P03 to P05 pins as digital input/output pins, set them in the digital I/O mode by using port mode control register 0 (PMC0) (can be specified in 1-bit units).

To use the P03 to P05 pins as analog input pins, set them in the analog input mode by using port mode control register 0 (PMC0) (can be specified in 1-bit units).

This port can also be used for segment output of LCD controller/driver, serial interface data I/O, clock I/O, clock output/buzzer output, 10-bit A/D converter analog input, and timer I/O.

Reset signal generation sets P01, P02, P06, and P07 to the digital input invalid mode[Note], and P03 to P05 to the analog input mode.

Note “Digital input invalid” refers to the state in which all the digital outputs, digital inputs, and LCD outputs are disabled.

4.3.2 Port 1

Port 1 is an I/O port with an output latch. Port 1 can be set to the input mode or output mode in 1-bit units using port mode register 1 (PM1). When the P10 to P17 pins are used as an input port, use of an on-chip pull-up resistor can be specified in 1-bit units by pull-up resistor option register 1 (PU1).

Input to the P10 and P13 pins can be specified through a normal input buffer or a TTL input buffer in 1-bit units using port input mode register 1 (PIM1).

Output from the P10 and P12 pins can be specified as N-ch open-drain output (V_{DD} tolerance) in 1-bit units using port output mode register 1 (POM1).

This port can also be used for serial interface data I/O, clock I/O, segment output of LCD controller/driver, timer I/O, and sampling output.

Reset signal generation sets P10 to P16 to the digital input invalid mode[Note], and P17 to the input mode.

Note "Digital input invalid" refers to the state in which all the digital outputs, digital inputs, and LCD outputs are disabled.

4.3.3 Port 2

Port 2 is an I/O port with an output latch. Port 2 can be set to the input mode or output mode in 1-bit units using port mode register 2 (PM2). When the P20 to P27 pins are used as an input port, use of an on-chip pull-up resistor can be specified in 1-bit units by pull-up resistor option register 2 (PU2).

This port can also be used for external interrupt request input and sampling input.

Reset signal generation sets port 2 to the input mode.

4.3.4 Port 3

Port 3 is an I/O port with an output latch. Port 3 can be set to the input mode or output mode in 1-bit units using port mode register 3 (PM3). When the P30 to P32 and P35 to P37 pins are used as an input port, use of an on-chip pull-up resistor can be specified in 1-bit units by pull-up resistor option register 3 (PU3).

Input to the P35 and P36 pins can be specified through a normal input buffer or a TTL input buffer in 1-bit units using port input mode register 3 (PIM3).

Output from the P35 to P37 pins can be specified as N-ch open-drain output (V_{DD} tolerance) in 1-bit units using port output mode register 3 (POM3).

This port can also be used for clock output/buzzer output, real-time clock 2 correction clock output, serial interface clock I/O, data I/O, slave select input, segment output of LCD controller/driver, timer I/O, and programming UART transmission/reception.

Reset signal generation sets port 3 to the digital input invalid mode[Note].

Note "Digital input invalid" refers to the state in which all the digital outputs, digital inputs, and LCD outputs are disabled.

4.3.5 Port 4

Port 4 is an I/O port with an output latch. Port 4 can be set to the input mode or output mode in 1-bit units using port mode register 4 (PM4). To use the P40, P43, and P44 pins as input ports, use of an on-chip pull-up resistor can be specified by setting pull-up resistor option register 4 (PU4).

Input to the P40 and P43 pins can be specified through a normal input buffer or a TTL input buffer in 1-bit units using port input mode register 4 (PIM4).

Output from the P40, P43, and P44 pins can be specified as N-ch open-drain output (V_{DD} tolerance) in 1-bit units using port output mode register 4 (POM4).

This port can also be used for serial interface clock I/O, data I/O, timer I/O, data I/O for a flash memory programmer/debugger, and sampling input.

Reset signal generation sets port 4 to input mode.

4.3.6 Port 5

Port 5 is an I/O port with an output latch. Port 5 can be set to the input mode or output mode in 1-bit units using port mode register 5 (PM5). When the P50 to P53 pins are used as an input port, use of an on-chip pull-up resistor can be specified in 1-bit units by pull-up resistor option register 5 (PU5).

Input to the P51 and P52 pins can be specified through a normal input buffer or a TTL input buffer in 1-bit units using port input mode register 5 (PIM5).

Output from the P50 to P52 pins can be specified as N-ch open-drain output (V_{DD} tolerance) in 1-bit units using port output mode register 5 (POM5).

This port can also be used for serial interface clock I/O, data I/O, segment output of LCD controller/driver, and timer I/O.

Reset signal generation sets port 5 to the digital input invalid mode[Note].

Note “Digital input invalid” refers to the state in which all the digital outputs, digital inputs, and LCD outputs are disabled.

4.3.7 Port 6

Port 6 is an I/O port with an output latch. Port 6 can be set to the input mode or output mode in 1-bit units using port mode register 6 (PM6).

The output from the P60 and P61 pins is N-ch open-drain output (6 V tolerance).

This port can also be used for serial interface data I/O and clock I/O.

Reset signal generation sets port 6 to the input mode.

4.3.8 Port 7

Port 7 is an I/O port with an output latch. Port 7 can be set to the input mode or output mode in 1-bit units using port mode register 7 (PM7). When the P70 to P77 pins are used as an input port, use of an on-chip pull-up resistor can be specified in 1-bit units by pull-up resistor option register 7 (PU7).

This port can also be used for timer I/O and segment output of LCD controller/driver.

Reset signal generation sets port 7 to the digital input invalid mode[Note].

Note “Digital input invalid” refers to the state in which all the digital outputs, digital inputs, and LCD outputs are disabled.

4.3.9 Port 8

Port 8 is an I/O port with an output latch. Port 8 can be set to the input mode or output mode in 1-bit units using port mode register 8 (PM8). When the P80 to P86 pins are used as an input port, use of an on-chip pull-up resistor can be specified in 1-bit units by pull-up resistor option register 8 (PU8).

Input to the P81 and P81 pins can be specified through a normal input buffer or a TTL input buffer in 1-bit units using port input mode register 8 (PIM8).

Output from the P80, P81, and P82 pins can be specified as N-ch open-drain output (V_{DD} tolerance) in 1-bit units using port output mode register 8 (POM8).

This port can also be used for serial interface clock I/O, data I/O, sampling input, sampling output, external signal sampler clock output, external signal sampler phase detection input, clock output/buzzer output, and timer I/O.

Reset signal generation sets port 8 to the input mode.

4.3.10 Port 12

P125 to P127 are I/O ports with output latches. P125 to P127 can be set to the input mode or output mode in 1-bit units using port mode register 12 (PM12). When the P125 to P127 pins are used as an input port, use of an on-chip pull-up resistor can be specified by pull-up resistor option register 12 (PU12).

P121 to P124 are 4-bit input ports.

This port can also be used for external interrupt request input, timer I/O, connecting resonator for main system clock, connecting resonator for subsystem clock, external clock input for main system clock, external clock input for subsystem clock, connecting a capacitor for LCD controller/driver, and power supply voltage pin for driving the LCD.

Reset signal generation sets P121 to P124 to input mode, and P125 to P127 to digital input invalid mode[Note].

Note “Digital input invalid” refers to the state in which all the digital outputs, digital inputs, and LCD outputs are disabled.

4.3.11 Port 13

P137 is a 1-bit input-only port.

P137 is fixed an input ports.

This port can also be used for external interrupt request input and serial interface slave select input.

4.3.12 Port 15

Port 15 is an I/O port with output latches. Port 15 can be set to the input mode or output mode in 1-bit units using port mode register 15 (PM15).

When the P150 and P151 pins are used as an input port, use of an on-chip pull-up resistor can be specified by pull-up resistor option register 15 (PU15).

This port can also be used for sampling input.

Reset signal generation sets port 15 to input mode.

4.4 Registers Controlling Port Function

Port functions are controlled by the following registers.

- Port mode registers (PMxx)
- Port registers (Pxx)
- Pull-up resistor option registers (PUxx)
- Port input mode registers (PIMxx)
- Port output mode registers (POMxx)
- Port mode control registers (PMCxx)
- Peripheral I/O redirection registers (PIOR0 to PIOR3)
- LCD port function registers (PFSEG0 to PFSEG4)
- LCD input switch control register (ISCLCD)

Caution Which registers and bits are included depends on the product. For registers and bits mounted on each product, see Table 4 - 3. Be sure to set bits that are not mounted to their initial values.

Table 4 - 3 PMxx, Pxx, PUxx, PIMxx, POMxx, PMCxx registers and the bits mounted on each product (1/4)

Port		Bit Name						R5F11NM	R5F11NL	R5F11PL, R5F11NG	R5F11RM
		PMxx register	Pxx register	PUxx register	PIMxx register	POMxx register	PMCxx register				
Port 0	0	—	—	—	—	—	—	—	—	—	—
	1	PM01	P01	PU01	—	—	—	√	—	√	√
	2	PM02	P02	PU02	—	POM02	—	√	—	√	√
	3	PM03	P03	PU03	PIM03 Note 1	POM03 Note 1	PMC03 Note 2	√	√	√	√
	4	PM04	P04	PU04	PIM04	POM04	PMC04 Note 3	√	—	√	√
	5	PM05	P05	PU05	—	—	PMC05 Note 2	√	√	√	√
	6	PM06	P06	PU06	—	POM06	—	√	√	√	√
	7	PM07	P07	PU07	PIM07	POM07	—	√	√	√	√
Port 1	0	PM10	P10	PU10	PIM10	POM10	—	√	√	√	√
	1	PM11	P11	PU11	—	—	PMC11 Note 4	√	√	—	√
	2	PM12	P12	PU12	—	POM12 Note 5	—	√	√	—	√
	3	PM13	P13	PU13	PIM13 Note 5	—	—	√	√	—	√
	4	PM14	P14	PU14	—	—	—	√	√	—	√
	5	PM15	P15	PU15	—	—	—	√	√	—	√
	6	PM16	P16	PU16	—	—	—	√	—	—	√
	7	PM17	P17	PU17	—	—	—	√	—	—	√
Port 2	0	PM20	P20	PU20	—	—	—	—	—	—	√
	1	PM21	P21	PU21	—	—	—	—	—	—	√
	2	PM22	P22	PU22	—	—	—	—	—	—	√
	3	PM23	P23	PU23	—	—	—	—	—	—	√
	4	PM24	P24	PU24	—	—	—	—	—	—	√
	5	PM25	P25	PU25	—	—	—	—	—	—	√
	6	PM26	P26	PU26	—	—	—	—	—	—	√
	7	PM27	P27	PU27	—	—	—	—	—	—	√

Note 1. R5F11NM, R5F11NG, R5F11PL, and R5F11RM only.
Note 2. R5F11NL, R5F11NG, R5F11PL, and R5F11RM only.
Note 3. R5F11NG, R5F11PL, and R5F11RM only.
Note 4. R5F11NL only.
Note 5. R5F11RM only.

Table 4 - 3 PMxx, Pxx, PUxx, PIMxx, POMxx, PMCxx registers and the bits mounted on each product (2/4)

Port		Bit Name						R5F11NM	R5F11NL	R5F11PL, R5F11NG	R5F11RM
		PMxx register	Pxx register	PUxx register	PIMxx register	POMxx register	PMCxx register				
Port 3	0	PM30	P30	PU30	—	—	—	√	√	√	√
	1	PM31	P31	PU31	—	—	—	√	√	—	√
	2	PM32	P32	PU32	—	—	—	√	√	√	√
	3	—	—	—	—	—	—	—	—	—	—
	4	—	—	—	—	—	—	—	—	—	—
	5	PM35	P35	PU35	PIM35	POM35	—	√	√	√	√
	6	PM36	P36	PU36	PIM36	POM36	—	√	√	√	√
	7	PM37	P37	PU37	—	POM37	—	√	√	√	√
Port 4	0	PM40	P40	PU40	PIM40 Note	POM40 Note	—	√	√	√	√
	1	—	—	—	—	—	—	—	—	—	—
	2	—	—	—	—	—	—	—	—	—	—
	3	PM43	P43	PU43	PIM43	POM43	—	√	—	—	√
	4	PM44	P44	PU44	—	POM44	—	√	—	—	√
	5	—	—	—	—	—	—	—	—	—	—
	6	—	—	—	—	—	—	—	—	—	—
	7	—	—	—	—	—	—	—	—	—	—
Port 5	0	PM50	P50	PU50	—	POM50	—	√	√	√	√
	1	PM51	P51	PU51	PIM51	POM51	—	√	√	√	√
	2	PM52	P52	PU52	PIM52	POM52	—	√	√	√	√
	3	PM53	P53	PU53	—	—	—	√	—	√	√
	4	—	—	—	—	—	—	—	—	—	—
	5	—	—	—	—	—	—	—	—	—	—
	6	—	—	—	—	—	—	—	—	—	—
	7	—	—	—	—	—	—	—	—	—	—

Note R5F11NM and R5F11RM only.

Table 4 - 3 PMxx, Pxx, PUxx, PIMxx, POMxx, PMCxx registers and the bits mounted on each product (3/4)

Port		Bit Name						R5F11NM	R5F11NL	R5F11PL, R5F11NG	R5F11RM
		PMxx register	Pxx register	PUxx register	PIMxx register	POMxx register	PMCxx register				
Port 6	0	PM60	P60	—	—	—	—	√	√	√	√
	1	PM61	P61	—	—	—	—	√	√	√	√
	2	—	—	—	—	—	—	—	—	—	—
	3	—	—	—	—	—	—	—	—	—	—
	4	—	—	—	—	—	—	—	—	—	—
	5	—	—	—	—	—	—	—	—	—	—
	6	—	—	—	—	—	—	—	—	—	—
	7	—	—	—	—	—	—	—	—	—	—
Port 7	0	PM70	P70	PU70	—	—	—	√	√	√	√
	1	PM71	P71	PU71	—	—	—	√	√	√	√
	2	PM72	P72	PU72	—	—	—	√	—	—	√
	3	PM73	P73	PU73	—	—	—	√	—	—	√
	4	PM74	P74	PU74	—	—	—	√	—	—	√
	5	PM75	P75	PU75	—	—	—	√	—	—	√
	6	PM76	P76	PU76	—	—	—	√	√	√	√
	7	PM77	P77	PU77	—	—	—	√	√	√	√
Port 8	0	PM80	P80	PU80	—	POM80	—	√	—	—	√
	1	PM81	P81	PU81	PIM81	POM81	—	√	—	—	√
	2	PM82	P82	PU82	PIM82 Note	POM82 Note	—	√	√	—	√
	3	PM83	P83	PU83	—	—	—	√	√	—	√
	4	PM84	P84	PU84	—	—	—	√	—	—	√
	5	PM85	P85	PU85	—	—	—	√	—	—	√
	6	PM86	P86	PU86	—	—	—	√	—	—	√
	7	—	—	—	—	—	—	—	—	—	—

Note R5F11NM and R5F11RM only.

Table 4 - 3 PMxx, Pxx, PUxx, PIMxx, POMxx, PMCxx registers and the bits mounted on each product (4/4)

Port		Bit Name						R5F11NM	R5F11NL	R5F11PL, R5F11NG	R5F11RM
		PMxx register	Pxx register	PUxx register	PIMxx register	POMxx register	PMCxx register				
Port 12	0	—	—	—	—	—	—	—	—	—	—
	1	—	P121	—	—	—	—	√	√	√	√
	2	—	P122	—	—	—	—	√	√	√	√
	3	—	P123	—	—	—	—	√	√	√	√
	4	—	P124	—	—	—	—	√	√	√	√
	5	PM125	P125	PU125	—	—	—	√	√	—	√
	6	PM126	P126	PU126	—	—	—	√	√	—	√
	7	PM127	P127	PU127	—	—	—	√	√	—	√
Port 13	0	—	—	—	—	—	—	—	—	—	—
	1	—	—	—	—	—	—	—	—	—	—
	2	—	—	—	—	—	—	—	—	—	—
	3	—	—	—	—	—	—	—	—	—	—
	4	—	—	—	—	—	—	—	—	—	—
	5	—	—	—	—	—	—	—	—	—	—
	6	—	—	—	—	—	—	—	—	—	—
	7	—	P137	—	—	—	—	√	√	√	√
Port 15	0	PM150	P150	PU150	—	—	—	—	—	—	√
	1	PM151	P151	PU151	—	—	—	—	—	—	√
	2	—	—	—	—	—	—	—	—	—	—
	3	—	—	—	—	—	—	—	—	—	—
	4	—	—	—	—	—	—	—	—	—	—
	5	—	—	—	—	—	—	—	—	—	—
	6	—	—	—	—	—	—	—	—	—	—
	7	—	—	—	—	—	—	—	—	—	—

4.4.1 Port mode registers (PMxx)

These registers specify input or output mode for the port in 1-bit units.

These registers can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets these registers to FFH.

When port pins are used as alternate-function pins, set the port mode register by referencing **4.6 Register Settings When Using Alternate Function**.

Figure 4 - 1 Format of Port mode register

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
PM0	PM07	PM06	PM05	PM04	PM03	PM02	PM01	1	FFF20H	FFH	R/W
PM1	PM17	PM16	PM15	PM14	PM13	PM12	PM11	PM10	FFF21H	FFH	R/W
PM2	PM27	PM26	PM25	PM24	PM23	PM22	PM21	PM20	FFF22H	FFH	R/W
PM3	PM37	PM36	PM35	1	1	PM32	PM31	PM30	FFF23H	FFH	R/W
PM4	1	1	1	PM44	PM43	1	1	PM40	FFF24H	FFH	R/W
PM5	1	1	1	1	PM53	PM52	PM51	PM50	FFF25H	FFH	R/W
PM6	1	1	1	1	1	1	PM61	PM60	FFF26H	FFH	R/W
PM7	PM77	PM76	PM75	PM74	PM73	PM72	PM71	PM70	FFF27H	FFH	R/W
PM8	1	PM86	PM85	PM84	PM83	PM82	PM81	PM80	FFF28H	FFH	R/W
PM12	PM127	PM126	PM125	1	1	1	1	1	FFF2CH	FFH	R/W
PM15	1	1	1	1	1	1	PM151	PM150	FFF2FH	FFH	R/W

PMmn	Pmn pin I/O mode selection (m = 0 to 8, 12, 15; n = 0 to 7)
0	Output mode (output buffer on)
1	Input mode (output buffer off)

Caution Be sure to set bits that are not mounted to their initial values.

4.4.2 Port registers (Pxx)

These registers set the output latch value of a port.

If the data is read in the input mode, the pin level is read. If it is read in the output mode, the output latch value is read Note.

These registers can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears these registers to 00H.

Note If P03 to P05 and P11 are set up as analog I/O function, or when a port is read while in the input mode, 0 is always returned, not the pin level.

Figure 4 - 2 Format of Port register

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
P0	P07	P06	P05	P04	P03	P02	P01	0	FFF00H	00H (output latch)	R/W
P1	P17	P16	P15	P14	P13	P12	P11	P10	FFF01H	00H (output latch)	R/W
P2	P27	P26	P25	P24	P23	P22	P21	P20	FFF02H	00H (output latch)	R/W
P3	P37	P36	P35	0	0	P32	P31	P30	FFF03H	00H (output latch)	R/W
P4	0	0	0	P44	P43	0	0	P40	FFF04H	00H (output latch)	R/W
P5	0	0	0	0	P53	P52	P51	P50	FFF05H	00H (output latch)	R/W
P6	0	0	0	0	0	0	P61	P60	FFF06H	00H (output latch)	R/W
P7	P77	P76	P75	P74	P73	P72	P71	P70	FFF07H	00H (output latch)	R/W
P8	0	P86	P85	P84	P83	P82	P81	P80	FFF08H	00H (output latch)	R/W
P12	P127	P126	P125	P124	P123	P122	P121	0	FFF0CH	Undefined	R/W Note
P13	P137	0	0	0	0	0	0	0	FFF0DH	Undefined	R/W Note
P15	0	0	0	0	0	0	P151	P150	FFF0FH	00H (output latch)	R/W

Pmn	m = 0 to 8, 12, 13, 15; n = 0 to 7	
	Output data control (in output mode)	Input data read (in input mode)
0	Output 0	Input low level
1	Output 1	Input high level

Note P121 to P124, and P137 are read-only.

Caution Be sure to set bits that are not mounted to their initial values.

4.4.3 Pull-up resistor option registers (PUxx)

These registers specify whether the on-chip pull-up resistors are to be used or not. On-chip pull-up resistors can be used in bit units only for the bits set to normal output mode (POMmn = 0) and input mode (PMmn = 1) for the pins to which the use of an on-chip pull-up resistor has been specified in these registers.

On-chip pull-up resistors cannot be connected to bits set to output mode and bits used as alternate-function output pins and analog setting (PMC = 1), regardless of the settings of these registers.

These registers can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears these registers to 00H (only PU4 is set to 01H).

Caution When a port with the PIMn register is input from a different potential device to the TTL buffer, pull up to the power supply of the different potential device via an external resistor by setting PUmn = 0.

Figure 4 - 3 Format of Pull-up resistor option register

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
PU0	PU07	PU06	PU05	PU04	PU03	PU02	PU01	0	F0030H	00H	R/W
PU1	PU17	PU16	PU15	PU14	PU13	PU12	PU11	PU10	F0031H	00H	R/W
PU2	PU27	PU26	PU25	PU24	PU23	PU22	PU21	PU20	F0032H	00H	R/W
PU3	PU37	PU36	PU35	0	0	PU32	PU31	PU30	F0033H	00H	R/W
PU4	0	0	0	PU44	PU43	0	0	PU40	F0034H	01H	R/W
PU5	0	0	0	0	PU53	PU52	PU51	PU50	F0035H	00H	R/W
PU7	PU77	PU76	PU75	PU74	PU73	PU72	PU71	PU70	F0037H	00H	R/W
PU8	0	PU86	PU85	PU84	PU83	PU82	PU81	PU80	F0038H	00H	R/W
PU12	PU127	PU126	PU125	0	0	0	0	0	F003CH	00H	R/W
PU15	0	0	0	0	0	0	PU151	PU150	F003FH	00H	R/W

PUmn	Pmn pin on-chip pull-up resistor selection (m = 0 to 5, 7, 8, 12, 15; n = 0 to 7)
0	On-chip pull-up resistor not connected
1	On-chip pull-up resistor connected

Caution Be sure to set bits that are not mounted to their initial values.

4.4.4 Port input mode registers (PIMxx)

These registers set the input buffer in 1-bit units.

TTL input buffer can be selected during serial communication with an external device of the different potential.

Port input mode registers can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears these registers to 00H.

Figure 4 - 4 Format of Port input mode register

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
PIM0	PIM07	0	0	PIM04	PIM03 Note 1	0	0	0	F0040H	00H	R/W
PIM1	0	0	0	0	PIM13 Note 2	0	0	PIM10	F0041H	00H	R/W
PIM3	0	PIM35	PIM36	0	0	0	0	0	F0043H	00H	R/W
PIM4	0	0	0	0	PIM43	0	0	PIM40 Note 3	F0044H	00H	R/W
PIM5	0	0	0	0	0	PIM52	PIM51	0	F0045H	00H	R/W
PIM8	0	0	0	0	0	PIM82 Note 3	PIM81	PIM80	F0048H	00H	R/W

PIMmn	Pmn pin input buffer selection (m = 0, 1, 3, 4, 5 and 8; n = 0 to 7)
0	Normal input buffer
1	TTL input buffer

Note 1. R5F11NM, R5F11NG, R5F11PL, and R5F11RM only.

Note 2. R5F11RM only.

Note 3. R5F11NM and R5F11RM only.

Caution Be sure to set bits that are not mounted to their initial values.

4.4.5 Port output mode registers (POMxx)

These registers set the output mode in 1-bit units.

N-ch open-drain output (V_{DD} tolerance) mode can be selected during serial communication with an external device of the different potential, and for the SDA00, SDA10, and SDA20 pins during simplified I^2C communication with an external device of the same potential.

In addition, POMxx register is set with PUxx register, whether or not to use the on-chip pull-up resistor.

Port output mode registers can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears these registers to 00H.

Caution An on-chip pull-up resistor is not connected to a bit for which N-ch open drain output (V_{DD} tolerance) mode (POMmn = 1) is set.

Figure 4 - 5 Format of Port output mode register

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
POM0	POM07	POM06	0	POM04	POM03 Note 1	POM02	0	0	F0050H	00H	R/W
POM1	0	0	0	0	0	POM12 Note 2	0	POM10	F0051H	00H	R/W
POM3	POM37	POM36	POM35	0	0	0	0	0	F0053H	00H	R/W
POM4	0	0	0	POM44	POM43	0	0	POM40 Note 3	F0054H	00H	R/W
POM5	0	0	0	0	0	POM52	POM51	POM50	F0055H	00H	R/W
POM8	0	0	0	0	0	POM82 Note 3	POM81	POM80	F0058H	00H	R/W

POMmn	Pmn pin output mode selection (m = 0, 1, 3, 4, 5 and 8; n = 0 to 7)
0	Normal output mode
1	N-ch open-drain output (V_{DD} tolerance) mode

Note 1. R5F11NM, R5F11NG, R5F11PL, and R5F11RM only.

Note 2. R5F11RM only.

Note 3. R5F11NM and R5F11RM only.

Caution Be sure to set bits that are not mounted to their initial values.

4.4.6 Port mode control registers (PMCxx) (R5F11NL, R5F11NG, R5F11PL, and R5F11RM only)

These registers set the digital I/O or analog input in 1-bit units.

Port mode control registers can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears these registers to FFH.

Figure 4 - 6 Format of Port mode control register

Address: F0060H After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
PMC0	1	1	PMC05 Note 1	PMC04 Note 2	PMC03 Note 1	1	1	1

Address: F0061H After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
PMC1	1	1	1	1	1	1	PMC11 Note 3	1

PMCmn	Selection of digital I/O or analog input for Pmn pin (m = 0, 1; n = 1, 3 to 5)
0	Digital I/O (alternate function other than analog input)
1	Analog input

Note 1. R5F11NL, R5F11NG, R5F11PL, and R5F11RM only.

Note 2. R5F11NG, R5F11PL, and R5F11RM only.

Note 3. R5F11NL only.

Caution Be sure to set bits that are not mounted to their initial values.

4.4.7 Peripheral I/O redirection register 0 (PIOR0)

This register is used to specify whether to enable or disable the peripheral I/O redirect function.
This function is used to switch ports to which alternate functions are assigned.
Use the PIOR0 register to assign a port to the function to redirect and enable the function.
In addition, can be changed the settings for redirection until its function enable operation.
The PIOR0 register can be set by an 8-bit memory manipulation instruction.
Reset signal generation sets this register to 00H.

Figure 4 - 7 Format of Peripheral I/O redirection register 0 (PIOR0)

Address: F0077H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
PIOR0	0	0	PIOR05	PIOR04	PIOR03	PIOR02	PIOR01	PIOR00

Bit	Alternate Function	R5F11NM		R5F11NL		R5F11PL, R5F11NG		R5F11RM	
		0	1	0	1	0	1	0	1
PIOR05	$\overline{SSI00}$	P32	P137	Note				P32	P137
PIOR04	SMP0	Note						P85	P43
	SMP1							P86	P44
PIOR03	PCLBUZ1	P36	P83	P36	P83	Note		P36	P83
PIOR02	TxD1	P50	P02	Note		P50	P02	P50	P02
	RxD1	P51	P03			P51	P03	P51	P03
	SCL10	P52	P04			P52	P04	P52	P04
	SDA10	P51	P03			P51	P03	P51	P03
	SI10	P51	P03			P51	P03	P51	P03
	SO10	P50	P02			P50	P02	P50	P02
	SCK10	P52	P04			P52	P04	P52	P04
PIOR01	TxD2	P06	P80	Note				P06	P80
	RxD2	P07	P81					P07	P81
	SCL20	P10	P82					P10	P82
	SDA20	P07	P81					P07	P81
	SI20	P07	P81					P07	P81
	SO20	P06	P80					P06	P80
	SCK20	P10	P82					P10	P82
PIOR00	TxD0	P37	P44	Note				P37	P44
	RxD0	P36	P43					P36	P43
	SCL00	P35	P40					P35	P40
	SDA00	P36	P43					P36	P43
	SI00	P36	P43					P36	P43
	SO00	P37	P44					P37	P44
	SCK00	P35	P40					P35	P40

Note These functions are not available for use. Set this bit to 0 (default value).

4.4.8 Peripheral I/O redirection register 1 (PIOR1)

This register is used to specify whether to enable or disable the peripheral I/O redirect function.
This function is used to switch ports to which alternate functions are assigned.
Use the PIOR1 register to assign a port to the function to redirect and enable the function.
In addition, can be changed the settings for redirection until its function enable operation.
The PIOR1 register can be set by an 8-bit memory manipulation instruction.
Reset signal generation sets this register to 00H.

Figure 4 - 8 Format of Peripheral I/O redirection register 1 (PIOR1)

Address: F0079H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
PIOR1	0	PIOR16	PIOR15	PIOR14	PIOR13	PIOR12	PIOR11	PIOR10

Bit	Alternate Function	R5F11NM		R5F11NL		R5F11PL, R5F11NG		R5F11RM	
		0	1	0	1	0	1	0	1
PIOR10	INTP0	P137	P53	Note		P137	P53	Note	
PIOR11	INTP1	P121	P40	P121	P40	P121	P40		
PIOR12	INTP2	P10	P82	Note					
PIOR13	INTP3	P30	P60	P30	P60	P30	P60		
PIOR14	INTP4	P32	P61	P32	P61	P32	P61		
PIOR15	INTP5	P122	P01	Note		P122	P01	P122	P24
PIOR16	INTP6	P04	P86	Note					

Note These functions are not available for use. Set this bit to 0 (default value).

4.4.9 Peripheral I/O redirection register 2 (PIOR2) (R5F11NM, R5F11NL, and R5F11RM only)

This register is used to specify whether to enable or disable the peripheral I/O redirect function.
This function is used to switch ports to which alternate functions are assigned.
Use the PIOR2 register to assign a port to the function to redirect and enable the function.
In addition, can be changed the settings for redirection until its function enable operation.
The PIOR2 register can be set by an 8-bit memory manipulation instruction.
Reset signal generation sets this register to 00H.

Figure 4 - 9 Format of Peripheral I/O redirection register 2 (PIOR2)

Address: F0075H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
PIOR2	PIOR27	PIOR26	PIOR25	PIOR24	PIOR23	PIOR22	PIOR21	PIOR20

PIOR21	PIOR20	Timer array unit TI00 pin select
0	0	Multiplexed with P06
0	1	Multiplexed with P81 Note 1
1	0	Multiplexed with P43 Note 2
1	1	Setting prohibited

PIOR23	PIOR22	Timer array unit TO00 pin select
0	0	Multiplexed with P03
0	1	Multiplexed with P81 Note 1
1	0	Multiplexed with P43 Note 2
1	1	Setting prohibited

PIOR24	Timer array unit TI01/TO01 pin select
0	Multiplexed with P31
1	Multiplexed with P40

PIOR25	Timer array unit TI02/TO02 pin select
0	Multiplexed with P52
1	Multiplexed with P80 Note 1

PIOR26	Timer array unit TI03/TO03 pin select
0	Multiplexed with P50
1	Multiplexed with P83

PIOR27	Timer array unit TI04/TO04 pin select
0	Multiplexed with P51
1	Multiplexed with P127

Note 1. R5F11NM and R5F11RM only. For R5F11NL, setting is prohibited.
Note 2. R5F11NM only. For R5F11NL and R5F11RM, setting is prohibited.

4.4.10 Peripheral I/O redirection register 3 (PIOR3)

This register is used to specify whether to enable or disable the peripheral I/O redirect function.
This function is used to switch ports to which alternate functions are assigned.
Use the PIOR3 register to assign a port to the function to redirect and enable the function.
In addition, can be changed the settings for redirection until its function enable operation.
The PIOR3 register can be set by an 8-bit memory manipulation instruction.
Reset signal generation sets this register to 00H.

Figure 4 - 10 Format of Peripheral I/O redirection register 3 (PIOR3)

Address: F007DH After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
PIOR3	0	0	PIOR35	PIOR34	PIOR33	PIOR32	PIOR31	PIOR30

PIOR31	PIOR30	Timer array unit TI05/TO05 pin select
0	0	Multiplexed with P07
0	1	Multiplexed with P126 Note 1
1	0	Multiplexed with P84 Note 2
1	1	Multiplexed with P71Note 3

PIOR33	PIOR32	Timer array unit TI06/TO06 pin select
0	0	Multiplexed with P05
0	1	Multiplexed with P125 Note 1
1	0	Multiplexed with P76 Note 3
1	1	Setting prohibited

PIOR35	PIOR34	Timer array unit TI07/TO07 pin select
0	0	Multiplexed with P77
0	1	Multiplexed with P82 Note 1
1	0	Multiplexed with P17 Note 2
1	1	Setting prohibited

Note 1. R5F11NM, R5F11NL, and R5F11RM only. For R5F11NG and R5F11PL, setting is prohibited.
Note 2. R5F11NM only. For R5F11NL, R5F11NG, R5F11PL, and R5F11RM, setting is prohibited.
Note 3. R5F11NG and R5F11PL only. For R5F11NM, R5F11NL, and R5F11RM, setting is prohibited.

4.4.11 LCD port function registers 0 to 4 (PFSEG0 to PFSEG4) (R5F11NM, R5F11NL, and R5F11RM only)

These registers specify whether to use pins P01 to P07, P10 to P16, P30 to P32, P35 to P37, P50 to P53, and P70 to P77 as port pins (other than segment output pins) or segment output pins.

These registers are set by using a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets these registers to FFH (PFSEG0 is F0H, and PFSEG4 is 0FH).

Remark The correspondence between the segment output pins (SEGxx) and the PFSEG register (PFSEGxx bits) and the existence of SEGxx pins in each product are shown in Table 4 - 4 Segment Output Pins in Each Product and Correspondence with PFSEG Register (PFSEG Bits).

Figure 4 - 11 Format of LCD Port Function Registers 0 to 4 (PFSEG0 to PFSEG4)

Address: F0300H After reset: F0H R/W

Symbol	7	6	5	4	3	2	1	0
PFSEG0	PFSEG07	PFSEG06	PFSEG05	PFSEG04	0	0	0	0

Address: F0301H After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
PFSEG1	PFSEG15	PFSEG14	PFSEG13	PFSEG12	PFSEG11	PFSEG10	PFSEG09	PFSEG08

Address: F0302H After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
PFSEG2	PFSEG23	PFSEG22	PFSEG21	PFSEG20	PFSEG19	PFSEG18	PFSEG17	PFSEG16

Address: F0303H After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
PFSEG3	PFSEG31	PFSEG30	PFSEG29	PFSEG28	PFSEG27	PFSEG26	PFSEG25	PFSEG24

Address: F0304H After reset: 0FH R/W

Symbol	7	6	5	4	3	2	1	0
PFSEG4	0	0	0	0	PFSEG35	PFSEG34	PFSEG33	PFSEG32

PFSEGxx (xx = 04 to 35)	Specification of port (other than segment output)/segment output for Pmn pins (mn = 01 to 07, 10 to 16, 30 to 32, 35 to 37, 50 to 53, 70 to 77)
0	Used as port (other than segment output)
1	Used as segment output

Caution To use the Pmn pins as segment output pins (PFSEGxx = 1), be sure to set the PUmn bit of the PUm register, POMmn bit of the POMm register, and PIMmn bit of the PIMm register to "0".

Table 4 - 4 Segment Output Pins in Each Product and Correspondence with PFSEG Register (PFSEG Bits)

Bit name of PFSEG register	Corresponding SEGxx pins	Alternate port	R5F11NM	R5F11NL	R5F11RM
PFSEG04	SEG4	P53	√	—	√
PFSEG05	SEG5	P52	√	√	√
PFSEG06	SEG6	P51	√	√	√
PFSEG07	SEG7	P50	√	√	√
PFSEG08	SEG8	P70	√	√	√
PFSEG09	SEG9	P71	√	√	√
PFSEG10	SEG10	P72	√	—	√
PFSEG11	SEG11	P73	√	—	√
PFSEG12	SEG12	P74	√	—	√
PFSEG13	SEG13	P75	√	—	√
PFSEG14	SEG14	P76	√	√	√
PFSEG15	SEG15	P77	√	√	√
PFSEG16	SEG16	P30	√	√	√
PFSEG17	SEG17	P31	√	√	√
PFSEG18	SEG18	P32	√	√	√
PFSEG19	SEG19	P35	√	√	√
PFSEG20	SEG20	P36	√	√	√
PFSEG21	SEG21	P37	√	√	√
PFSEG22	SEG22	P01	√	—	√
PFSEG23	SEG23	P02	√	—	√
PFSEG24	SEG24	P03	√	√	√
PFSEG25	SEG25	P04	√	—	√
PFSEG26	SEG26	P05	√	√	√
PFSEG27	SEG27	P06	√	√	√
PFSEG28	SEG28	P07	√	√	√
PFSEG29	SEG29	P10	√	√	√
PFSEG30	SEG30	P11	√	√	√
PFSEG31	SEG31	P12	√	√	√
PFSEG32	SEG32	P13	√	√	√
PFSEG33	SEG33	P14	√	√	√
PFSEG34	SEG34	P15	√	√	√
PFSEG35	SEG35	P16	√	—	√

Caution Be sure to set bits that are not mounted to their initial values.

4.4.12 LCD input switch control register (ISCLCD) (R5F11NM, R5F11NL, and R5F11RM only)

The CAPL/P126, CAPH/P127, and V_{L3}/P125 pins are internally connected with a Schmitt trigger buffer.
Input to the Schmitt trigger buffer must be disabled until the CAPL/P126, CAPH/P127, and V_{L3}/P125 pins are set to operate as LCD function pins in order to prevent through-current from entering.
This register is set by using a 1-bit or 8-bit memory manipulation instruction.
Reset signal generation sets ISCLCD to 00H.

Figure 4 - 12 Format of LCD input switch control register (ISCLCD)

Address: F0308H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
ISCLCD	0	0	0	0	0	0	ISCVL3	ISCCAP

ISCVL3	V_{L3}/P125 pin Schmitt trigger buffer control
0	Makes digital input ineffective
1	Makes digital input effective

ISCCAP	CAPL/P126, CAPH/P127 pins Schmitt trigger buffer control
0	Makes digital input ineffective
1	Makes digital input effective

Caution If ISCVL3 = 0 and ISCCAP = 0, set the corresponding port registers as follows:
PU127 bit of PU12 register = 0, P127 bit of P12 register = 0
PU126 bit of PU12 register = 0, P126 bit of P12 register = 0
PU125 bit of PU12 register = 0, P125 bit of P12 register = 0

4.5 Port Function Operations

Port operations differ depending on whether the input or output mode is set, as shown below.

4.5.1 Writing to I/O port

(1) Output mode

A value is written to the output latch by a transfer instruction, and the output latch contents are output from the pin.

Once data is written to the output latch, it is retained until data is written to the output latch again.

The data of the output latch is cleared when a reset signal is generated.

(2) Input mode

A value is written to the output latch by a transfer instruction, but since the output buffer is off, the pin status does not change.

Once data is written to the output latch, it is retained until data is written to the output latch again.

The data of the output latch is cleared when a reset signal is generated.

4.5.2 Reading from I/O port

(1) Output mode

The output latch contents are read by a transfer instruction. The output latch contents do not change.

(2) Input mode

The pin status is read by a transfer instruction. The output latch contents do not change.

4.5.3 Operations on I/O port

(1) Output mode

An operation is performed on the output latch contents, and the result is written to the output latch. The output latch contents are output from the pins.

Once data is written to the output latch, it is retained until data is written to the output latch again.

The data of the output latch is cleared when a reset signal is generated.

(2) Input mode

The pin level is read and an operation is performed on its contents. The result of the operation is written to the output latch, but since the output buffer is off, the pin status does not change. Therefore, byte data can be written to the ports used for both input and output.

The data of the output latch is cleared when a reset signal is generated.

4.5.4 Handling different potential (1.8 V Note, 2.5 V, 3 V) by using I/O buffers

It is possible to connect an external device operating on a different potential (1.8 V Note 1 , 2.5 V, or 3 V) by switching I/O buffers with the port input mode register (PIMxx) and port output mode register (POMxx). When receiving input from an external device with a different potential (1.8 V Note 1 , 2.5 V, or 3 V), set port input mode registers 0, 1, 3, 4, 5, 8 (PIM0, PIM1, PIM3, PIM4, PIM5, PIM8) on a bit-by-bit basis to enable normal input (CMOS)/TTL switching.

When outputting data to an external device with a different potential (1.8 V Note , 2.5 V, or 3 V), set port output mode registers 0, 1, 3, 4, 5, 8 (POM0, POM1, POM3, POM4, POM5, POM8) on a bit-by-bit basis to enable normal output (CMOS)/N-ch open drain (V_{DD} tolerance) switching.

Connection of a serial interface is described as follows.

(1) Setting procedure when using input ports of UART0 to UART2, CSI00, CSI10, and CSI20 functions for the TTL input buffer

In case of UART0:	P36 (P43)
In case of UART1:	P51 (P03)
In case of UART2:	P07 (P81)
In case of CSI00:	P35, P36 (P40, P43)
In case of CSI10:	P52, P51 (P04, P03)
In case of CSI20:	P10, P07 (P82, P81)

Remark Functions in parentheses can be assigned via settings in the peripheral I/O redirection register 0 (PIOR0).

<1> Using an external resistor, pull up externally the pin to be used to the power supply of the target device (on-chip pull-up resistor cannot be used).

<2> Set the corresponding bit of the PIM0, PIM1, PIM3, PIM4, PIM5, and PIM8 registers to 1 to switch to the TTL input buffer. For V_{IH} and V_{IL}, refer to the DC characteristics when the TTL input buffer is selected.

<3> Enable the operation of the serial array unit and set the mode to UART/Simplified SPI(CSI Note 2) mode.

Note 1. R5F11R only.

Note 2. Although the CSI function is generally called SPI, it is also called CSI in this product, so it is referred to as such in this manual.

(2) Setting procedure when using output ports of UART0 to UART2, CSI00, CSI10, and CSI20 functions in N-ch open-drain output mode

In case of UART0:	P37 (P44)
In case of UART1:	P50 (P02)
In case of UART2:	P06 (P80)
In case of CSI00:	P35, P37 (P40, P44)
In case of CSI10:	P52, P50 (P04, P02)
In case of CSI20:	P10, P06 (P82, P80)

Remark Functions in parentheses can be assigned via settings in the peripheral I/O redirection register 0 (PIOR0).

<1> Using an external resistor, pull up externally the pin to be used to the power supply of the target device (on-chip pull-up resistor cannot be used).
<2> After reset release, the port mode is the input mode (high-impedance).
<3> Set the output latch of the corresponding port to 1.
<4> Set the corresponding bit of the POM0, POM1, POM3, POM4, POM5, and POM8 registers to 1 to set the N-ch open-drain output (V_{DD} withstand voltage) mode.
<5> Enable the operation of the serial array unit and set the mode to UART/Simplified SPI(CSI) mode.
<6> Set the corresponding bit of the PM0, PM1, PM3, PM4, PM5, and PM8 registers to output mode. At this time, the output data is high level, so the pin is in the Hi-Z state.

(3) Setting procedure when using I/O ports of simplified IIC00, IIC10 and IIC20 functions with a different potential (1.8 V[Note], 2.5 V, 3 V)

In case of simplified IIC00: P35, P36 (P40, P43)
In case of simplified IIC10: P52, P51 (P04, P03)
In case of simplified IIC20: P10, P07 (P82, P81)

Remark Functions in parentheses can be assigned via settings in the peripheral I/O redirection register 0 (PIOR0).

<1> Using an external resistor, pull up externally the pin to be used to the power supply of the target device (on-chip pull-up resistor cannot be used).
<2> After reset release, the port mode is the input mode (Hi-Z).
<3> Set the output latch of the corresponding port to 1.
<4> Set the corresponding bit of the POM0, POM1, POM3, POM4, POM5, and POM8 registers to 1 to set N-ch open drain output (V_{DD} tolerance) mode.
<5> Set the corresponding bit of the PIM0, PIM1, PIM3, PIM4, PIM5, and PIM8 registers to 1 to switch to the TTL input buffer. For V_{IH} and V_{IL}, refer to the DC characteristics when the TTL input buffer is selected.
<6> Enable the operation of the serial array unit and set the mode to simplified I^2C mode.
<7> Set the corresponding bit of the PM0, PM1, PM3, PM4, PM5, and PM8 registers to output mode (data I/O is possible in output mode).
At this time, the output data is high level, so the pin is in the Hi-Z state.

Note R5F11R only.

4.6 Register Settings When Using Alternate Function

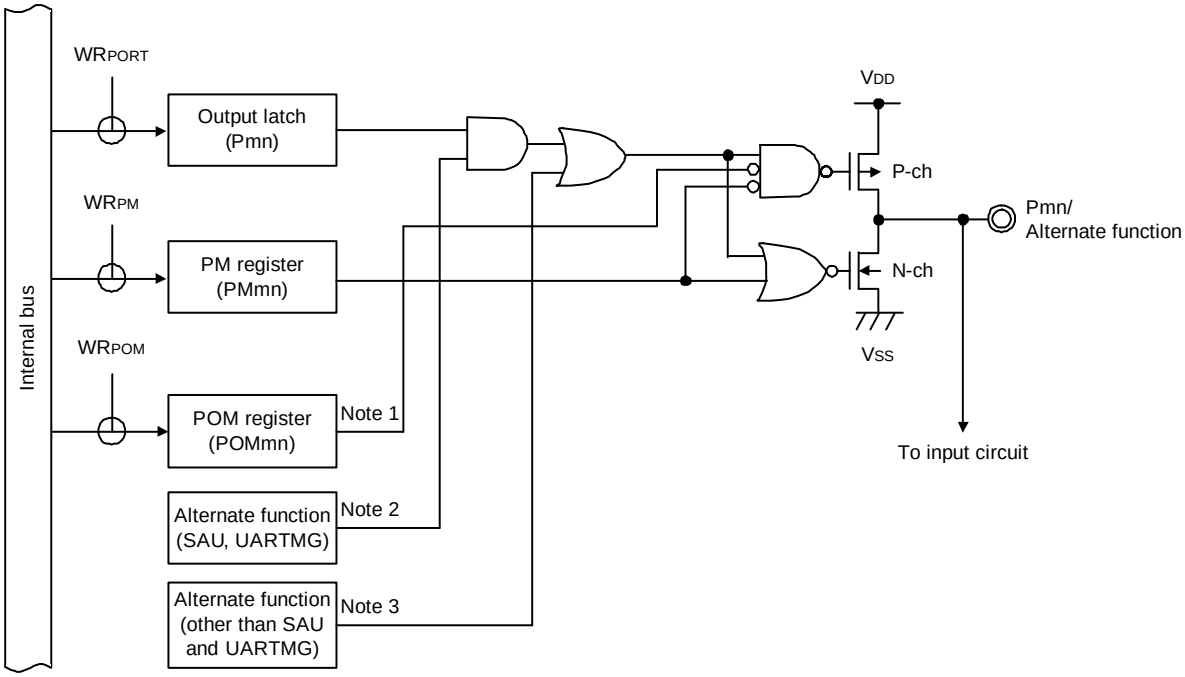
4.6.1 Basic concept when using alternate function

In the beginning, for a pin also assigned to be used for analog input, use the port mode control register (PMCxx) to specify whether to use the pin for analog input or digital input/output.

Figure 4 - 13 shows the basic configuration of an output circuit for pins used for digital input/output. The output of the output latch for the port and the output of the alternate SAU and UARTMG Note function are input to an AND gate. The output of the AND gate is input to an OR gate. The output of an alternate function other than SAU and UARTMG Note (TAU, RTC2, clock/buzzer output, IICA, etc.) is connected to the other input pin of the OR gate. When such kind of pins are used by the port function or an alternate function, the unused alternate function must not hinder the output of the function to be used. An idea of basic settings for this kind of case is shown in Table 4 - 5.

Note R5F11R only.

Figure 4 - 13 Basic Configuration of Output Circuit for Pins



Note 1. When there is no POM register, this signal should be considered to be low level (0).
Note 2. When there is no alternate function, this signal should be considered to be high level (1).
Note 3. When there is no alternate function, this signal should be considered to be low level (0).

Remark m: Port number (m = 0 to 8, 12, 13, 15); n: Bit number (n = 0 to 7)

Table 4 - 5 Concept of Basic Settings

Output Function of Used Pin	Output Settings of Unused Alternate Function		
	Output Function for Port	Output Function for SAU and UARTMG Note 2	Output Function for other than SAU and UARTMG Note 2
Output function for port	—	Output is high (1)	Output is low (0)
Output function for SAU and UARTMG Note 2	High (1)	—	Output is low (0)
Output function for other than SAU and UARTMG Note 2	Low (0)	Output is high (1)	Output is low (0) Note 1

Note 1. Since more than one output function other than SAU and UARTMG Note 2 may be assigned to a single pin, the output of an unused alternate function must be set to low level (0). For details on the setting method, see **4.6.2 Register settings for alternate function whose output function is not used**.

Note 2. R5F11R only.

4.6.2 Register settings for alternate function whose output function is not used

When the output of an alternate function of the pin is not used, the following settings should be made. Note that when the peripheral I/O redirection function is the target, the output can be switched to another pin by setting the peripheral I/O redirection registers 0, 1, 2, and 3 (PIOR0, PIOR1, PIOR2, and PIOR3). This allows usage of the port function or other alternate function assigned to the target pin.

(1) SOp = 1, TxDq = 1 (settings when the serial output (SOp/TxDq) of SAU is not used)
When the serial output (SOp/TxDq) is not used, such as, a case in which only the serial input of SAU is used, set the bit in serial output enable register m (SOEm) which corresponds to the unused output to 0 (output disabled) and set the SOmn bit in serial output register m (SOm) to 1 (high). These are the same settings as the initial state.

(2) SCKp = 1, SDAr = 1, SCLr = 1 (settings when channel n in SAU is not used)
When SAU is not used, set bit n (SEmn) in serial channel enable status register m (SEm) to 0 (operation stopped state), set the bit in serial output enable register m (SOEm) which corresponds to the unused output to 0 (output disabled), and set the SOmn and CKOmn bits in serial output register m (SOm) to 1 (high). These are the same settings as the initial state.

(3) TOmn = 0 (settings when the output of channel n in TAU is not used)
When the TOmn output of TAU is not used, set the bit in timer output enable register 0 (TOE0) which corresponds to the unused output to 0 (output disabled) and set the bit in timer output register 0 (TO0) to 0 (low). These are the same settings as the initial state.

(4) SDAAn = 0, SCLAn = 0 (setting when IICA is not used)
When IICA is not used, set the IICEn bit in IICA control register n0 (IICCTLn0) to 0 (operation stopped). This is the same setting as the initial state.

(5) PCLBUZn = 0 (setting when clock/buzzer output is not used)
When the clock/buzzer output is not used, set the PCLOEn bit in clock output select register n (CKSn) to 0 (output disabled). This is the same setting as the initial state.

(6) RTC1HZ = 0 (setting when real-time clock 2 output is not used)
When the real-time clock 2 output is not used, set the RCLOE1 bit in real-time clock control register 0 (RTCC0) to 0 (output disabled). This is the same setting as the initial state.

(7) TxDMG0 = 1 (setting when UARTMG output is not used)
When the UARTMG is not to be used, set bit 7 to 0 (disabling operation of the UART operation clock) and bit 6 (disabling transmission) to 0 in UARTMG0 operating mode setting register 0 (ASIMMG00), and bit 0 in UARTMG0 operating mode setting register 1 (ASIMMG01) to 0 (positive logic).

(8) TRJIOn = 0/TRJOn = 0 (setting when timer RJn output is not used)
When TRJO0 pin is not used for the pulse output function of timer RJ, set bit 2 (TOENA) in the timer RJ I/O control register n (TRJIOCn) to 0 (disabling TRJOn output). This is the same setting as the initial state.
When TRJIOn pin of timer RJ is not used for the output function, set bits 2 to 0 (TMOD2 to TMOD0) in the timer RJ mode register n (TRJMRn) to the value other than 001b (pulse output mode). The initial setting is 000b (timer mode).

(9) EXSDO0 = 0/EXSDO1 = 0 (setting when external signal sampler clock output is not used)
When external signal sampler clock output (EXSDOn) is not used, set bit n (EXSDOE0n) in the external signal sampler control register 0 (EXSDM0) to 0 (disabling EXSDOn output). This is the same setting as the initial state.

(10) SMO0 = 0/SMO1 = 0/SMO2 = 0 (setting when sampling output is not used)
When sampling clock output (SMOn) is not used, set bit n (SMOTDOEn) in the SMOTD output control register (SMOTDOE) to 0 (disabling SMOn output). This is the same setting as the initial state.

4.6.3 Register setting examples for used port and alternate functions

Register setting examples for used port and alternate functions are shown in tables 4 - 6 to 4 - 9. The registers used to control the port functions should be set as shown in tables 4 - 6 to 4 - 9. See the following remark for legends used in tables 4 - 6 to 4 - 9.

Remark -: Not supported
×: don’t care
PIORx: Peripheral I/O redirection register
PFSEGXX: LCD port function register
POMxx: Port output mode register
PMCxx: Port mode control register
PMxx: Port mode register
Pxx: Port output latch

Functions in parentheses can be assigned via settings in the peripheral I/O redirection registers 0 to 3 (PIOR0 to PIOR3).
For details about ports that also serve as segment output pins (SEGxx), see **4.6.4 Operation of ports that alternately function as SEGxx pins**.
For details about ports that also serve as V_{L3}, CAPL, and CAPH pins, see **4.6.5 Operation of ports that alternately function as V_{L3}, CAPL, and CAPH pins**.

Table 4 - 6 Setting Examples of Registers and Output Latches When Using Pin Function (R5F11NM) (1/8)

Port Name	Used Function		PIORXX	PFSEGXX	POMXX	PMCXX	PMXX	PXX	Alternate Function Output	
	Function Name	I/O							SAU Output Function	Other than SAU
P01	P01	Input	—	PFSEG22 = 0	—	—	1	×	—	—
		Output	—	PFSEG22 = 0	—	—	0	0/1	—	—
	(INTP5)	Input	PIOR15 = 1	PFSEG22 = 0	—	—	1	×	—	—
	SEG22	Output	—	PFSEG22 = 1	—	—	0	0	—	—
P02	P02	Input	—	PFSEG23 = 0	×	—	1	×	×	×
		Output	—	PFSEG23 = 0	0	—	0	0/1	(SO10)/(TxD1) = 1	PCLBUZ0 = 0
		N-ch OD output	—	PFSEG23 = 0	1	—	0	0/1		
	(SO10)	Output	PIOR02 = 1	PFSEG23 = 0	0/1	—	0	1	—	PCLBUZ0 = 0
	(TxD1)	Output	PIOR02 = 1	PFSEG23 = 0	0/1	—	0	1	—	PCLBUZ0 = 0
	PCLBUZ0	Output	—	PFSEG23 = 0	0	—	0	0	(SO10)/(TxD1) = 1	—
	SEG23	Output	—	PFSEG23 = 1	0	—	0	0	×	×
P03	P03	Input	—	PFSEG24 = 0	×	—	1	×	×	×
		Output	—	PFSEG24 = 0	0	—	0	0/1	(SDA10) = 1	TO00 = 0
		N-ch OD output	—	PFSEG24 = 0	1	—	0	0/1		
	(SI10)	Input	PIOR02 = 1	PFSEG24 = 0	×	—	1	×	×	×
	(RxD1)	Input	PIOR02 = 1	PFSEG24 = 0	×	—	1	×	×	×
	(SDA10)	I/O	PIOR02 = 1	PFSEG24 = 0	1	—	0	1	×	TO00 = 0
	TO00	Output	PIOR23 = 0 PIOR22 = 0	PFSEG24 = 0	0	—	0	0	(SDA10) = 1	—
	SEG24	Output	—	PFSEG24 = 1	0	—	0	0	×	×
P04	P04	Input	—	PFSEG25 = 0	×	—	1	×	×	—
		Output	—	PFSEG25 = 0	0	—	0	0/1	(SCK10)/(SCL10) = 1	—
		N-ch OD output	—	PFSEG25 = 0	1	—	0	0/1		—
	(SCK10)	Input	PIOR02 = 1	PFSEG25 = 0	×	—	1	×	×	—
		Output	PIOR02 = 1	PFSEG25 = 0	0/1	—	0	1	—	—
	(SCL10)	Output	PIOR02 = 1	PFSEG25 = 0	0/1	—	0	1	—	—
	INTP6	Input	PIOR16 = 0	PFSEG25 = 0	×	—	1	×	×	—
	SEG25	Output	—	PFSEG25 = 1	0	—	0	0	×	—
P05	P05	Input	—	PFSEG26 = 0	—	—	1	×	—	×
		Output	—	PFSEG26 = 0	—	—	0	0/1	—	TO06 = 0
	TI06	Input	PIOR32 = 0	PFSEG26 = 0	—	—	1	×	—	×
	TO06	Output	PIOR32 = 0	PFSEG26 = 0	—	—	0	0	—	—
	SEG26	Output	—	PFSEG26 = 1	—	—	0	0	—	×
P06	P06	Input	—	PFSEG27=0	×	—	1	×	×	—
		Output	—	PFSEG27 = 0	0	—	0	0/1	SO20/TxD2 = 1	—
		N-ch OD output	—	PFSEG27 = 0	1	—	0	0/1		—
	SO20	Output	PIOR01 = 0	PFSEG27 = 0	0/1	—	0	1	—	—
	TxD2	Output	PIOR01 = 0	PFSEG27 = 0	0/1	—	0	1	—	—
	TI00	Input	PIOR21 = 0 PIOR20 = 0	PFSEG27=0	×	—	1	×	×	—
	SEG27	Output	—	PFSEG27 = 1	0	—	0	0	×	—

Table 4 - 6 Setting Examples of Registers and Output Latches When Using Pin Function (R5F11NM) (2/8)

Port Name	Used Function		PIORXX	PFSEGXX	POMXX	PMCXX	PMXX	PXX	Alternate Function Output	
	Function Name	I/O							SAU Output Function	Other than SAU
P07	P07	Input	—	PFSEG28 = 0	×	—	1	×	×	×
		Output	—	PFSEG28 = 0	0	—	0	0/1	SDA20 = 1	TO05 = 0
		N-ch OD output	—	PFSEG28 = 0	1	—	0	0/1		
	SI20	Input	PIOR01 = 0	PFSEG28 = 0	×	—	1	×	×	×
	RxD2	Input	PIOR01 = 0	PFSEG28 = 0	×	—	1	×	×	×
	SDA20	I/O	PIOR01 = 0	PFSEG28 = 0	1	—	0	1	—	TO05 = 0
	TI05	Input	PIOR31 = 0 PIOR30 = 0	PFSEG28 = 0	×	—	1	×	×	×
	TO05	Output	PIOR31 = 0 PIOR30 = 0	PFSEG28 = 0	0	—	0	0	SDA20 = 1	—
	SEG28	Output	—	PFSEG28 = 1	0	—	0	0	×	×
P10	P10	Input	—	PFSEG29 = 0	×	—	1	×	×	—
		Output	—	PFSEG29 = 0	0	—	0	0/1	SCK20/SCL20 = 1	—
		N-ch OD output	—	PFSEG29 = 0	1	—	0	0/1		—
	SCK20	Input	PIOR01 = 0	PFSEG29 = 0	×	—	1	×	×	—
		Output	PIOR01 = 0	PFSEG29 = 0	0/1	—	0	1	—	—
	SCL20	Output	PIOR01 = 0	PFSEG29 = 0	0/1	—	0	1	—	—
	INTP2	Input	PIOR12 = 0	PFSEG29 = 0	×	—	1	×	×	—
	SEG29	Output	—	PFSEG29 = 1	0	—	0	0	×	—
P11	P11	Input	—	PFSEG30 = 0	—	—	1	×	—	—
		Output	—	PFSEG30 = 0	—	—	0	0/1	—	—
	SEG30	Output	—	PFSEG30 = 1	—	—	0	0	—	—
P12	P12	Input	—	PFSEG31=0	—	—	1	×	—	—
		Output	—	PFSEG31 = 0	—	—	0	0/1	—	—
	SEG31	Output	—	PFSEG31 = 1	—	—	0	0	—	—
P13	P13	Input	—	PFSEG32 = 0	—	—	1	×	—	—
		Output	—	PFSEG32 = 0	—	—	0	0/1	—	—
	SEG32	Output	—	PFSEG32 = 1	—	—	0	0	—	—
P14	P14	Input	—	PFSEG33 = 0	—	—	1	×	—	—
		Output	—	PFSEG33 = 0	—	—	0	0/1	—	—
	SEG33	Output	—	PFSEG33 = 1	—	—	0	0	—	—
P15	P15	Input	—	PFSEG34 = 0	—	—	1	×	—	—
		Output	—	PFSEG34 = 0	—	—	0	0/1	—	—
	SEG34	Output	—	PFSEG34 = 1	—	—	0	0	—	—
P16	P16	Input	—	PFSEG35 = 0	—	—	1	×	—	—
		Output	—	PFSEG35 = 0	—	—	0	0/1	—	—
	SEG35	Output	—	PFSEG35 = 1	—	—	0	0	—	—
P17	P17	Input	—	—	—	—	1	×	—	×
		Output	—	—	—	—	0	0/1	—	(TO07) = 0
	(TI07)	Input	PIOR35 = 1 PIOR34 = 0	—	—	—	1	×	—	×
	(TO07)	Output	PIOR35 = 1 PIOR34 = 0	—	—	—	0	0	—	—
P30	P30	Input	—	PFSEG16 = 0	—	—	1	×	—	×
		Output	—	PFSEG16 = 0	—	—	0	0/1	—	RTC1HZ = 0
	INTP3	Input	PIOR13 = 0	PFSEG16 = 0	—	—	1	×	—	×
	RTC1HZ	Output	—	PFSEG16 = 0	—	—	0	0	—	—
	SEG16	Output	—	PFSEG16 = 1	—	—	0	0	—	×

Table 4 - 6 Setting Examples of Registers and Output Latches When Using Pin Function (R5F11NM) (3/8)

Port Name	Used Function		PIORXX	PFSEGXX	POMXX	PMCXX	PMXX	PXX	Alternate Function Output	
	Function Name	I/O							SAU Output Function	Other than SAU
P31	P31	Input	—	PFSEG17 = 0	—	—	1	×	—	×
		Output	—	PFSEG17 = 0	—	—	0	0/1	—	TO01 = 0
	TI01	Input	PIOR24 = 0	PFSEG17 = 0	—	—	1	×	—	×
	TO01	Output	PIOR24 = 0	PFSEG17 = 0	—	—	0	0	—	—
	SEG17	Output	—	PFSEG17 = 1	—	—	0	0	—	×
P32	P32	Input	—	PFSEG18 = 0	—	—	1	×	—	—
		Output	—	PFSEG18 = 0	—	—	0	0/1	—	—
	INTP4	Input	PIOR14 = 0	PFSEG18 = 0	—	—	1	×	—	—
	$\overline{SSI00}$	Input	PIOR05 = 0	PFSEG18 = 0	—	—	1	×	—	—
	SEG18	Output	—	PFSEG18 = 1	—	—	0	0	—	—
P35	P35	Input	—	PFSEG19 = 0	×	—	1	×	×	—
		Output	—	PFSEG19 = 0	0	—	0	0/1	SCK00/SCL00 = 1	—
		N-ch OD output	—	PFSEG19 = 0	1	—	0	0/1		—
	SCK00	Input	PIOR00 = 0	PFSEG19 = 0	×	—	1	×	×	—
		Output	PIOR00 = 0	PFSEG19 = 0	0/1	—	0	1	—	—
	SCL00	Output	PIOR00 = 0	PFSEG19 = 0	0/1	—	0	1	—	—
	SEG19	Output	—	PFSEG19 = 1	0	—	0	0	×	—
P36	P36	Input	—	PFSEG20 = 0	×	—	1	×	×	×
		Output	—	PFSEG20 = 0	0	—	0	0/1	SDA00 = 1	PCLBUZ1 = 0
		N-ch OD output	—	PFSEG20 = 0	1	—	0	0/1		
	SI00	Input	PIOR00 = 0	PFSEG20 = 0	×	—	1	×	×	×
	RxD0	Input	PIOR00 = 0	PFSEG20 = 0	×	—	1	×	×	×
	SDA00	I/O	PIOR00 = 0	PFSEG20 = 0	1	—	0	1	—	PCLBUZ1 = 0
	PCLBUZ1	Output	PIOR03 = 0	PFSEG20 = 0	0	0	0	0	SDA00 = 1	—
	SEG20	Output	—	PFSEG20 = 1	0	—	0	0	×	×
P37	P37	Input	—	PFSEG21 = 0	×	—	1	×	×	—
		Output	—	PFSEG21 = 0	0	—	0	0/1	SO00/TxD0 = 1	—
		N-ch OD output	—	PFSEG21 = 0	1	—	0	0/1		—
	SO00	Output	PIOR00 = 0	PFSEG21 = 0	0/1	—	0	1	—	—
	TxD0	Output	PIOR00 = 0	PFSEG21 = 0	0/1	—	0	1	—	—
	SEG21	Output	—	PFSEG21 = 1	0	—	0	0	×	—
P40	P40	Input	—	—	×	—	1	×	×	×
		Output	—	—	0	—	0	0/1	(SCK00)/(SCL00) = 1	(TO01) = 0
		N-ch OD output	—	—	1	—	0	0/1		
	(SCK00)	Input	PIOR00 = 1	—	×	—	1	×	×	×
		Output	PIOR00 = 1	—	0/1	—	0	1	—	(TO01) = 0
	(SCL00)	Output	PIOR00 = 1	—	0/1	—	0	1	—	(TO01) = 0
	(INTP1)	Input	PIOR11 = 1	—	×	—	1	×	×	×
	(TI01)	Input	PIOR24 = 1	—	×	—	1	×	×	×
	(TO01)	Output	PIOR24 = 1	—	0	—	0	0	(SCK00)/(SCL00) = 1	—
P43	P43	Input	—	—	×	—	1	×	×	×
		Output	—	—	0	—	0	0/1	(SDA00) = 1	(TO00) = 0
		N-ch OD output	—	—	1	—	0	0/1		
	(SI00)	Input	PIOR00 = 1	—	×	—	1	×	×	×
	(RxD0)	Input	PIOR00 = 1	—	×	—	1	×	×	×
	(SDA00)	I/O	PIOR00 = 1	—	1	—	0	1	—	(TO00) = 0
	(TI00)	Input	PIOR21 = 1 PIOR20 = 0	—	×	—	1	×	×	×
	(TO00)	Output	PIOR23 = 1 PIOR22 = 0	—	0	—	0	0	(SDA00) = 1	—

Table 4 - 6 Setting Examples of Registers and Output Latches When Using Pin Function (R5F11NM) (4/8)

Port Name	Used Function		PIORXX	PFSEGXX	POMXX	PMCXX	PMXX	PXX	Alternate Function Output	
	Function Name	I/O							SAU Output Function	Other than SAU
P44	P44	Input	—	—	×	—	1	×	×	—
		Output	—	—	0	—	0	0/1	(SO00)/(TxD0) = 1	—
		N-ch OD output	—	—	1	—	0	0/1		—
	(SO00)	Output	PIOR00 = 1	—	0/1	—	0	1	—	—
	(TxD0)	Output	PIOR00 = 1	—	0/1	—	0	1	—	—
P50	P50	Input	—	PFSEG07 = 0	×	—	1	×	×	×
		Output	—	PFSEG07 = 0	0	—	0	0/1	SO10/TxD1 = 1	TO03 = 0
		N-ch OD output	—	PFSEG07 = 0	1	—	0	0/1		
	SO10	Output	PIOR02 = 0	PFSEG07 = 0	0/1	—	0	1	—	TO03 = 0
	TxD1	Output	PIOR02 = 0	PFSEG07 = 0	0/1	—	0	1	—	TO03 = 0
	TI03	Input	PIOR26 = 0	PFSEG07 = 0	×	—	1	×	×	×
	TO03	Output	PIOR26 = 0	PFSEG07 = 0	0	—	0	0	SO10/TxD1 = 1	—
	SEG7	Output	—	PFSEG07 = 1	0	—	0	0	×	×
P51	P51	Input	—	PFSEG06 = 0	×	—	1	×	×	×
		Output	—	PFSEG06 = 0	0	—	0	0/1	SDA10 = 1	TO04 = 0
		N-ch OD output	—	PFSEG06 = 0	1	—	0	0/1		
	SI10	Input	PIOR02 = 0	PFSEG06 = 0	×	—	1	×	×	×
	RxD1	Input	PIOR02 = 0	PFSEG06 = 0	×	—	1	×	×	×
	SDA10	I/O	PIOR02 = 0	PFSEG06 = 0	1	—	0	1	—	TO04 = 0
	TI04	Input	PIOR27 = 0	PFSEG06 = 0	×	—	1	×	×	×
	TO04	Output	PIOR27 = 0	PFSEG06 = 0	0	—	0	0	SDA10 = 1	—
	SEG6	Output	—	PFSEG06 = 1	0	—	0	0	×	×
P52	P52	Input	—	PFSEG05 = 0	×	—	1	×	×	×
		Output	—	PFSEG05 = 0	0	—	0	0/1	SCK10/SCL10 = 1	TO02 = 0
		N-ch OD output	—	PFSEG05 = 0	1	—	0	0/1		
	SCK10	Input	PIOR02 = 0	PFSEG05 = 0	×	—	1	×	×	×
		Output	PIOR02 = 0	PFSEG05 = 0	0/1	—	0	1	—	TO02 = 0
	SCL10	Output	PIOR02 = 0	PFSEG05 = 0	0/1	—	0	1	—	TO02 = 0
	TI02	Input	PIOR25 = 0	PFSEG05 = 0	×	—	1	×	×	×
	TO02	Output	PIOR25 = 0	PFSEG05 = 0	0	—	0	0	SCK10/SCL10 = 1	—
	SEG5	Output	—	PFSEG05 = 1	0	—	0	0	×	×
P53	P53	Input	—	PFSEG04 = 0	—	—	1	×	—	—
		Output	—	PFSEG04 = 0	—	—	0	0/1	—	—
	(INTP0)	Input	PIOR10 = 1	PFSEG04 = 0	—	—	1	×	—	—
	SEG4	Output	—	PFSEG04 = 1	—	—	0	0	—	—
P60	P60	Input	—	—	—	—	1	×	—	×
		N-ch OD output (6-V tolerance)	—	—	—	—	0	0/1	—	SCLA0 = 0
	SCLA0	I/O	—	—	—	—	0	0	—	—
	(INTP3)	Input	PIOR13 = 1	—	—	—	1	×	—	×
P61	P61	Input	—	—	—	—	1	×	—	×
		N-ch OD output (6-V tolerance)	—	—	—	—	0	0/1	—	SDAA0 = 0
	SDAA0	I/O	—	—	—	—	0	0	—	—
	(INTP4)	Input	PIOR14 = 1	—	—	—	1	×	—	×
P70	P70	Input	—	PFSEG08 = 0	—	—	1	×	—	—
		Output	—	PFSEG08 = 0	—	—	0	0/1	—	—
	SEG8	Output	—	PFSEG08 = 1	—	—	0	0	—	—

Table 4 - 6 Setting Examples of Registers and Output Latches When Using Pin Function (R5F11NM) (5/8)

Port Name	Used Function		PIORXX	PFSEGXX	POMXX	PMCXX	PMXX	PXX	Alternate Function Output	
	Function Name	I/O							SAU Output Function	Other than SAU
P71	P71	Input	—	PFSEG09 = 0	—	—	1	×	—	—
		Output	—	PFSEG09 = 0	—	—	0	0/1	—	—
	SEG9	Output	—	PFSEG09 = 1	—	—	0	0	—	—
P72	P72	Input	—	PFSEG10 = 0	—	—	1	×	—	—
		Output	—	PFSEG10 = 0	—	—	0	0/1	—	—
	SEG10	Output	—	PFSEG10 = 1	—	—	0	0	—	—
P73	P73	Input	—	PFSEG11 = 0	—	—	1	×	—	—
		Output	—	PFSEG11 = 0	—	—	0	0/1	—	—
	SEG11	Output	—	PFSEG11 = 1	—	—	0	0	—	—
P74	P74	Input	—	PFSEG12 = 0	—	—	1	×	—	—
		Output	—	PFSEG12 = 0	—	—	0	0/1	—	—
	SEG12	Output	—	PFSEG12 = 1	—	—	0	0	—	—
P75	P75	Input	—	PFSEG13 = 0	—	—	1	×	—	—
		Output	—	PFSEG13 = 0	—	—	0	0/1	—	—
	SEG13	Output	—	PFSEG13 = 1	—	—	0	0	—	—
P76	P76	Input	—	PFSEG14 = 0	—	—	1	×	—	—
		Output	—	PFSEG14 = 0	—	—	0	0/1	—	—
	SEG14	Output	—	PFSEG14 = 1	—	—	0	0	—	—
P77	P77	Input	—	PFSEG15 = 0	—	—	1	×	—	×
		Output	—	PFSEG15 = 0	—	—	0	0/1	—	TO07 = 0
	TI07	Input	PIOR35 = 0 PIOR34 = 0	PFSEG15 = 0	—	—	1	×	—	×
	TO07	Output	PIOR35 = 0 PIOR34 = 0	PFSEG15 = 0	—	—	0	0	—	—
	SEG15	Output	—	PFSEG15 = 1	—	—	0	0	—	×
P80	P80	Input	—	—	×	—	1	×	×	×
		Output	—	—	0	—	0	0/1	(SO20)/(TxD2) = 1	(TO02) = 0
		N-ch OD output	—	—	1	—	0	0/1		
	(SO20)	Output	PIOR01 = 1	—	0/1	—	0	1	—	(TO02) = 0
	(TxD2)	Output	PIOR01 = 1	—	0/1	—	0	1	—	(TO02) = 0
	(TI02)	Input	PIOR25 = 1	—	×	—	1	×	×	×
	(TO02)	Output	PIOR25 = 1	—	0	—	0	0	(SO20)/(TxD2) = 1	—
P81	P81	Input	—	—	×	—	1	×	×	×
		Output	—	—	0	—	0	0/1	(SDA20) = 1	(TO00) = 0
		N-ch OD output	—	—	1	—	0	0/1		
	(SI20)	Input	PIOR01 = 1	—	×	—	1	×	×	×
	(RxD2)	Input	PIOR01 = 1	—	×	—	1	×	×	×
	(SDA20)	I/O	PIOR01 = 1	—	1	—	0	1	—	(TO00) = 0
	(TI00)	Input	PIOR21 = 0 PIOR20 = 1	—	×	—	1	×	×	×
	(TO00)	Output	PIOR23 = 0 PIOR22 = 1	—	0	—	0	0	(SDA20) = 1	—

Table 4 - 6 Setting Examples of Registers and Output Latches When Using Pin Function (R5F11NM) (6/8)

Port Name	Used Function		PIORXX	PFSEGXX	POMXX	PMCXX	PMXX	PXX	Alternate Function Output	
	Function Name	I/O							SAU Output Function	Other than SAU
P82	P82	Input	—	—	×	—	1	×	×	×
		Output	—	—	0	—	0	0/1	(SCK20)/(SCL20) = 1	(TO07) = 0
		N-ch OD output	—	—	1	—	0	0/1		
	(SCK20)	Input	PIOR01 = 1	—	×	—	1	×	×	×
		Output	PIOR01 = 1	—	0/1	—	0	1	—	(TO07) = 0
	(SCL20)	Output	PIOR01 = 1	—	0/1	—	0	1	—	(TO07) = 0
	(INTP2)	Input	PIOR12 = 1	—	×	—	1	×	×	×
	(TI07)	Input	PIOR35 = 0 PIOR34 = 1	—	×	—	1	×	×	×
	(TO07)	Output	PIOR35 = 0 PIOR34 = 1	—	0	—	0	0	(SCK20)/(SCL20) = 1	—
P83	P83	Input	—	—	—	—	1	×	—	×
		Output	—	—	—	—	0	0/1	—	(PCLBUZ1) = 0 (TO03) = 0
	(PCLBUZ1)	Output	PIOR03 = 1	—	—	—	0	0	—	(TO03) = 0
	(TI03)	Input	PIOR26 = 1	—	—	—	1	×	—	×
	(TO03)	Output	PIOR26 = 1	—	—	—	0	0	—	(PCLBUZ1) = 0
P84	P84	Input	—	—	—	—	1	×	—	×
		Output	—	—	—	—	0	0/1	—	(TO05) = 0
	(TI05)	Input	PIOR31 = 1 PIOR30 = 0	—	—	—	1	×	—	×
	(TO05)	Output	PIOR31 = 1 PIOR30 = 0	—	—	—	0	0	—	—
P85	P85	Input	—	—	—	—	1	×	—	—
		Output	—	—	—	—	0	0/1	—	—
	INTP7	Input	—	—	—	—	1	×	—	—
P86	P86	Input	—	—	—	—	1	×	—	—
		Output	—	—	—	—	0	0/1	—	—
	(INTP6)	Input	PIOR16 = 1	—	—	—	1	×	—	—

Table 4 - 6 Setting Examples of Registers and Output Latches When Using Pin Function (R5F11NM) (7/8)

Port Name	Used Function		PIORXX	CMC (EXCLK, OSCSEL, EXCLKS, OSCSELS)	PXX
	Function Name	I/O			
P121	P121	Input	—	00xx/10xx/11xx	×
	X1	—	—	01xx	—
	INTP1	Input	PIOR11 = 0	00xx/10xx/11xx	×
P122	P122	Input	—	00xx/10xx	×
	X2	—	—	01xx	—
	EXCLK	—	—	11xx	—
	INTP5	Input	PIOR15 = 0	00xx/10xx	×
P123	P123	Input	—	xx00/xx10/xx11	×
	XT1	—	—	xx01	—
P124	P124	Input	—	xx00/xx10	×
	XT2	—	—	xx01	—
	EXCLKS	—	—	xx11	—

Table 4 - 6 Setting Examples of Registers and Output Latches When Using Pin Function (R5F11NM) (8/8)

Port Name	Used Function		PIORXX	POMXX	PMCXX	PMXX	PXX	ISCLCD	Alternate Function Output	
	Function Name	I/O							SAU Output Function	Other than SAU
P125	P125	Input	—	—	—	1	×	ISCVL3 = 1	—	×
		Output	—	—	—	0	0/1	ISCVL3 = 1	—	(TO06) = 0
	VL3	I/O	—	—	—	1	0	ISCVL3 = 0	—	×
	(TI06)	Input	PIOR32 = 1	—	—	1	x	ISCVL3 = 1	—	×
	(TO06)	Output	PIOR32 = 1	—	—	0	0	ISCVL3 = 1	—	—
P126	P126	Input	—	—	—	1	×	ISCCAP = 1	—	×
		Output	—	—	—	0	0/1	ISCCAP = 1	—	(TO05) = 0
	CAPL	Output	—	—	—	1	0	ISCCAP = 0	—	×
	(TI05)	Input	PIOR31 = 0 PIOR30 = 1	—	—	1	x	ISCCAP = 1	—	×
	(TO05)	Output	PIOR31 = 0 PIOR30 = 1	—	—	0	0	ISCCAP = 1	—	—
P127	P127	Input	—	—	—	1	×	ISCCAP = 1	—	×
		Output	—	—	—	0	0/1	ISCCAP = 1	—	(TO04) = 0
	CAPH	Output	—	—	—	1	0	ISCCAP = 0	—	×
	(TI04)	Input	PIOR27 = 1	—	—	1	x	ISCCAP = 1	—	×
	(TO04)	Output	PIOR27 = 1	—	—	0	0	ISCCAP = 1	—	—
P137	P137	Input	—	—	—	—	×	—	—	—
	INTP0	Input	PIOR10 = 0	—	—	—	×	—	—	—
	($\overline{SSI00}$)	Input	PIOR05 = 1	—	—	—	×	—	—	—

Table 4 - 7 Setting Examples of Registers and Output Latches When Using Pin Function (R5F11NL) (1/5)

Port Name	Used Function		PIORXX	PFSEGXX	POMXX	PMCXX	PMXX	PXX	Alternate Function Output	
	Function Name	I/O							SAU Output Function	Other than SAU
P03	P03	Input	—	PFSEG24 = 0	—	0	1	×	—	×
		Output	—	PFSEG24 = 0	—	0	0	0/1	—	TO00 = 0
	TO00	Output	—	PFSEG24 = 0	—	0	0	0	—	—
	ANI8	Analog input	—	PFSEG24 = 1	—	1	1	×	—	×
	SEG24	Output	—	PFSEG24 = 1	—	0	0	0	—	×
P05	P05	Input	—	PFSEG26 = 0	—	0	1	×	—	×
		Output	—	PFSEG26 = 0	—	0	0	0/1	—	TO06 = 0
	TI06	Input	PIOR32 = 0	PFSEG26 = 0	—	0	1	×	—	×
	TO06	Output	PIOR32 = 0	PFSEG26 = 0	—	0	0	0	—	—
	ANI10	Analog input	—	PFSEG26 = 1	—	1	1	×	—	×
	SEG26	Output	—	PFSEG26 = 1	—	0	0	0	—	×
P06	P06	Input	—	PFSEG27 = 0	×	—	1	×	×	—
		Output	—	PFSEG27 = 0	0	—	0	0/1	SO20/TxD2 = 1	—
		N-ch OD output	—	PFSEG27 = 0	1	—	0	0/1		—
	SO20	Output	—	PFSEG27 = 0	0/1	—	0	1	—	—
	TxD2	Output	—	PFSEG27 = 0	0/1	—	0	1	—	—
	TI00	Input	—	PFSEG27 = 0	×	—	1	×	×	—
	SEG27	Output	—	PFSEG27 = 1	0	—	0	0	×	—
P07	P07	Input	—	PFSEG28 = 0	×	—	1	×	×	×
		Output	—	PFSEG28 = 0	0	—	0	0/1	SDA20 = 1	TO05 = 0
		N-ch OD output	—	PFSEG28 = 0	`1	—	0	0/1		
	SI20	Input	—	PFSEG28 = 0	×	—	1	×	×	×
	RxD2	Input	—	PFSEG28 = 0	×	—	1	×	×	×
	SDA20	I/O	—	PFSEG28 = 0	1	—	0	1	—	TO05 = 0
	TI05	Input	PIOR30 = 0	PFSEG28 = 0	×	—	1	×	×	×
	TO05	Output	PIOR30 = 0	PFSEG28 = 0	0	—	0	0	SDA20 = 1	—
	SEG28	Output	—	PFSEG28 = 1	0	—	0	0	×	×
P10	P10	Input	—	PFSEG29 = 0	×	—	1	×	×	—
		Output	—	PFSEG29 = 0	0	—	0	0/1	SCK20/SCL20 = 1	—
		N-ch OD output	—	PFSEG29 = 0	1	—	0	0/1		—
	SCK20	Input	—	PFSEG29 = 0	×	—	1	×	×	—
		Output	—	PFSEG29 = 0	0/1	—	0	1	—	—
	SCL20	Output	—	PFSEG29 = 0	0/1	—	0	1	—	—
	INTP2	Input	—	PFSEG29 = 0	×	—	1	×	×	—
	SEG29	Output	—	PFSEG29 = 1	0	—	0	0	×	—
P11	P11	Input	—	PFSEG30 = 0	—	0	1	×	—	—
		Output	—	PFSEG30 = 0	—	0	0	0/1	—	—
	ANI11	Analog input	—	PFSEG30 = 1	—	1	1	×	—	—
	SEG30	Output	—	PFSEG30 = 1	—	0	0	0	—	—
P12	P12	Input	—	PFSEG31 = 0	—	—	1	×	—	—
		Output	—	PFSEG31 = 0	—	—	0	0/1	—	—
	SEG31	Output	—	PFSEG31 = 1	—	—	0	0	—	—
P13	P13	Input	—	PFSEG32 = 0	—	—	1	×	—	—
		Output	—	PFSEG32 = 0	—	—	0	0/1	—	—
	SEG32	Output	—	PFSEG32 = 1	—	—	0	0	—	—
P14	P14	Input	—	PFSEG33 = 0	—	—	1	×	—	—
		Output	—	PFSEG33 = 0	—	—	0	0/1	—	—
	SEG33	Output	—	PFSEG33 = 1	—	—	0	0	—	—
P15	P15	Input	—	PFSEG34 = 0	—	—	1	×	—	—
		Output	—	PFSEG34 = 0	—	—	0	0/1	—	—
	SEG34	Output	—	PFSEG34 = 1	—	—	0	0	—	—

Table 4 - 7 Setting Examples of Registers and Output Latches When Using Pin Function (R5F11NL) (2/5)

Port Name	Used Function		PIORXX	PFSEGXX	POMXX	PMCXX	PMXX	PXX	Alternate Function Output	
	Function Name	I/O							SAU Output Function	Other than SAU
P30	P30	Input	—	PFSEG16=0	—	—	1	×	—	×
		Output	—	PFSEG16 = 0	—	—	0	0/1	—	RTC1HZ = 0
	INTP3	Input	PIOR13 = 0	PFSEG16 = 0	—	—	1	×	—	×
	RTC1HZ	Output	—	PFSEG16 = 0	—	—	0	0	—	—
	SEG16	Output	—	PFSEG16 = 1	—	—	0	0	—	×
P31	P31	Input	—	PFSEG17 = 0	—	—	1	×	—	×
		Output	—	PFSEG17 = 0	—	—	0	0/1	—	TO01 = 0
	TI01	Input	PIOR24 = 0	PFSEG17 = 0	—	—	1	×	—	×
	TO01	Output	PIOR24 = 0	PFSEG17 = 0	—	—	0	0	—	—
	SEG17	Output	—	PFSEG17 = 1	—	—	0	0	—	×
P32	P32	Input	—	PFSEG18 = 0	—	—	1	×	—	—
		Output	—	PFSEG18 = 0	—	—	0	0/1	—	—
	INTP4	Input	PIOR14 = 0	PFSEG18 = 0	—	—	1	×	—	—
	$\overline{SSI00}$	Input	—	PFSEG18 = 0	—	—	1	×	—	—
	SEG18	Output	—	PFSEG18 = 1	—	—	0	0	—	—
P35	P35	Input	—	PFSEG19 = 0	×	—	1	×	×	—
		Output	—	PFSEG19 = 0	0	—	0	0/1	SCK00/SCL00 = 1	—
		N-ch OD output	—	PFSEG19 = 0	1	—	0	0/1		—
	SCK00	Input	—	PFSEG19 = 0	×	—	1	×	×	—
		Output	—	PFSEG19 = 0	0/1	—	0	1	—	—
	SCL00	Output	—	PFSEG19 = 0	0/1	—	0	1	—	—
	SEG19	Output	—	PFSEG19 = 1	0	—	0	0	×	—
P36	P36	Input	—	PFSEG20 = 0	×	—	1	×	×	×
		Output	—	PFSEG20 = 0	0	—	0	0/1	SDA00 = 1	PCLBUZ1 = 0
		N-ch OD output	—	PFSEG20 = 0	1	—	0	0/1		
	SI00	Input	—	PFSEG20 = 0	×	—	1	×	×	×
	RxD0	Input	—	PFSEG20 = 0	×	—	1	×	×	×
	SDA00	I/O	—	PFSEG20 = 0	1	—	0	1	—	PCLBUZ1 = 0
	PCLBUZ1	Output	PIOR03 = 0	PFSEG20 = 0	0	—	0	0	SDA00 = 1	—
	SEG20	Output	—	PFSEG20 = 1	0	—	0	0	×	×
P37	P37	Input	—	PFSEG21 = 0	×	—	1	×	×	—
		Output	—	PFSEG21 = 0	0	—	0	0/1	SO00/TxD0 = 1	—
		N-ch OD output	—	PFSEG21 = 0	1	—	0	0/1		—
	SO00	Output	—	PFSEG21 = 0	0/1	—	0	1	—	—
	TxD0	Output	—	PFSEG21 = 0	0/1	—	0	1	—	—
	SEG21	Output	—	PFSEG21 = 1	0	—	0	0	×	—
P40	P40	Input	—	—	—	—	1	×	—	×
		Output	—	—	—	—	0	0/1	—	(TO01) = 0
	(INTP1)	Input	PIOR11 = 1	—	—	—	1	×	—	×
	(TI01)	Input	PIOR24 = 1	—	—	—	1	×	—	×
	(TO01)	Output	PIOR24 = 1	—	—	—	0	0	—	—
P50	P50	Input	—	PFSEG07 = 0	×	—	1	×	×	×
		Output	—	PFSEG07 = 0	0	—	0	0/1	SO10/TxD1 = 1	TO03 = 0
		N-ch OD output	—	PFSEG07 = 0	1	—	0	0/1		
	SO10	Output	—	PFSEG07 = 0	0/1	—	0	1	—	TO03 = 0
	TxD1	Output	—	PFSEG07 = 0	0/1	—	0	1	—	TO03 = 0
	TI03	Input	PIOR26 = 0	PFSEG07 = 0	×	—	1	×	×	×
	TO03	Output	PIOR26 = 0	PFSEG07 = 0	0	—	0	0	SO10/TxD1 = 1	—
	SEG7	Output	—	PFSEG07 = 1	0	—	0	0	×	×

Table 4 - 7 Setting Examples of Registers and Output Latches When Using Pin Function (R5F11NL) (3/5)

Port Name	Used Function		PIORXX	PFSEGXX	POMXX	PMCXX	PMXX	PXX	Alternate Function Output	
	Function Name	I/O							SAU Output Function	Other than SAU
P51	P51	Input	—	PFSEG06 = 0	×	—	1	×	×	×
		Output	—	PFSEG06 = 0	0	—	0	0/1	SDA10 = 1	TO04 = 0
		N-ch OD output	—	PFSEG06 = 0	1	—	0	0/1		
	SI10	Input	—	PFSEG06 = 0	×	—	1	×	×	×
	RxD1	Input	—	PFSEG06 = 0	×	—	1	×	×	×
	SDA10	I/O	—	PFSEG06 = 0	1	—	0	1	—	TO04 = 0
	TI04	Input	PIOR27 = 0	PFSEG06 = 0	×	—	1	×	×	×
	TO04	Output	PIOR27 = 0	PFSEG06 = 0	0	—	0	0	SDA10 = 1	—
	SEG6	Output	—	PFSEG06 = 1	0	—	0	0	×	×
P52	P52	Input	—	PFSEG05 = 0	×	—	1	×	×	×
		Output	—	PFSEG05 = 0	0	—	0	0/1	SCK10/SCL10 = 1	TO02 = 0
		N-ch OD output	—	PFSEG05 = 0	1	—	0	0/1		
	SCK10	Input	—	PFSEG05 = 0	×	—	1	×	×	×
		Output	—	PFSEG05 = 0	0/1	—	0	1	—	TO02 = 0
	SCL10	Output	—	PFSEG05 = 0	0/1	—	0	1	—	TO02 = 0
	TI02	Input	—	PFSEG05 = 0	×	—	1	×	×	×
	TO02	Output	—	PFSEG05 = 0	0	—	0	0	SCK10/SCL10 = 1	—
	SEG5	Output	—	PFSEG05 = 1	0	—	0	0	×	×
P60	P60	Input	—	—	—	—	1	×	—	×
		N-ch OD output (6-V tolerance)	—	—	—	—	0	0/1	—	SCLA0 = 0
	SCLA0	I/O	—	—	—	—	0	0	—	—
	(INTP3)	Input	PIOR13 = 1	—	—	—	1	×	—	×
P61	P61	Input	×	—	—	—	1	×	—	×
		N-ch OD output (6-V tolerance)	×	—	—	—	0	0/1	—	SDAA0 = 0
	SDAA0	I/O	×	—	—	—	0	0	—	—
	(INTP4)	Input	PIOR14 = 1	—	—	—	1	×	—	×
P70	P70	Input	—	PFSEG08 = 0	—	—	1	×	—	—
		Output	—	PFSEG08 = 0	—	—	0	0/1	—	—
	SEG8	Output	—	PFSEG08 = 1	—	—	0	0	—	—
P71	P71	Input	—	PFSEG09 = 0	—	—	1	×	—	—
		Output	—	PFSEG09 = 0	—	—	0	0/1	—	—
	SEG9	Output	—	PFSEG09 = 1	—	—	0	0	—	—
P76	P76	Input	—	PFSEG14 = 0	—	—	1	×	—	—
		Output	—	PFSEG14 = 0	—	—	0	0/1	—	—
	SEG14	Output	—	PFSEG14 = 1	—	—	0	0	—	—
P77	P77	Input	—	PFSEG15 = 0	—	—	1	×	—	×
		Output	—	PFSEG15 = 0	—	—	0	0/1	—	TO07 = 0
	TI07	Input	PIOR34 = 0	PFSEG15 = 0	—	—	1	×	—	×
	TO07	Output	PIOR34 = 0	PFSEG15 = 0	—	—	0	0	—	—
	SEG15	Output	—	PFSEG15 = 1	—	—	0	0	—	×
P82	P82	Input	—	—	—	—	1	×	—	×
		Output	—	—	—	—	0	0/1	—	(TO07) = 0
	(TI07)	Input	PIOR34 = 1	—	—	—	1	×	—	×
	(TO07)	Output	PIOR34 = 1	—	—	—	0	0	—	—
P83	P83	Input	—	—	—	—	1	×	—	×
		Output	—	—	—	—	0	0/1	—	(PCLBUZ1) = 0 (TO03) = 0
	(PCLBUZ1)	Output	PIOR03 = 1	—	—	—	0	0	—	(TO03) = 0
	(TI03)	Input	PIOR26 = 1	—	—	—	1	×	—	×
	(TO03)	Output	PIOR26 = 1	—	—	—	0	0	—	(PCLBUZ1) = 0

Table 4 - 7 Setting Examples of Registers and Output Latches When Using Pin Function (R5F11NL) (4/5)

Port Name	Used Function		PIORXX	CMC (EXCLK, OSCSEL, EXCLKS, OSCSELS)	PXX
	Function Name	I/O			
P121	P121	Input	—	00xx/10xx/11xx	×
	X1	—	—	01xx	—
	INTP1	Input	PIOR11 = 0	00xx/10xx/11xx	×
P122	P122	Input	—	00xx/10xx	×
	X2	—	—	01xx	—
	EXCLK	—	—	11xx	—
	INTP5	Input	—	00xx/10xx	×
P123	P123	Input	—	xx00/xx10/xx11	×
	XT1	—	—	xx01	—
P124	P124	Input	—	xx00/xx10	×
	XT2	—	—	xx01	—
	EXCLKS	—	—	xx11	—

Table 4 - 7 Setting Examples of Registers and Output Latches When Using Pin Function (R5F11NL) (5/5)

Port Name	Used Function		PIORXX	POMXX	PMCXX	PMXX	PXX	ISCLCD	Alternate Function Output	
	Function Name	I/O							SAU Output Function	Other than SAU
P125	P125	Input	—	—	—	1	×	ISCVL3 = 1	—	×
		Output	—	—	—	0	0/1	ISCVL3 = 1	—	(TO06) = 0
	VL3	I/O	—	—	—	1	0	ISCVL3 = 0	—	×
	(TI06)	Input	PIOR32 = 1	—	—	1	x	ISCVL3 = 1	—	×
	(TO06)	Output	PIOR32 = 1	—	—	0	0	ISCVL3 = 1	—	—
P126	P126	Input	—	—	—	1	×	ISCCAP = 1	—	×
		Output	—	—	—	0	0/1	ISCCAP = 1	—	(TO05) = 0
	CAPL	Output	—	—	—	1	0	ISCCAP = 0	—	×
	(TI05)	Input	PIOR30 = 1	—	—	1	x	ISCCAP = 1	—	×
	(TO05)	Output	PIOR30 = 1	—	—	0	0	ISCCAP = 1	—	—
P127	P127	Input	—	—	—	1	×	ISCCAP = 1	—	×
		Output	—	—	—	0	0/1	ISCCAP = 1	—	(TO04) = 0
	CAPH	Output	—	—	—	1	0	ISCCAP = 0	—	×
	(TI04)	Input	PIOR27 = 1	—	—	1	x	ISCCAP = 1	—	×
	(TO04)	Output	PIOR27 = 1	—	—	0	0	ISCCAP = 1	—	—
P137	P137	Input	—	—	—	—	×	—	—	—
	INTP0	Input	—	—	—	—	×	—	—	—

Table 4 - 8 Setting Examples of Registers and Output Latches When Using Pin Function (R5F11NG, R5F11PL) (1/5)

Port Name	Used Function		PIORXX	PFSEGXX	POMXX	PMCXX	PMXX	PXX	Alternate Function Output	
	Function Name	I/O							SAU Output Function	Other than SAU
P01	P01	Input	—	—	—	—	1	×	—	—
		Output	—	—	—	—	0	0/1	—	—
	(INTP5)	Input	PIOR15 = 1	—	—	—	1	×	—	—
P02	P02	Input	—	—	×	—	1	×	×	×
		Output	—	—	0	—	0	0/1	(SO10)/(TxD1) = 1	PCLBUZ0 = 0
		N-ch OD output	—	—	1	—	0	0/1		
	(SO10)	Output	PIOR02 = 1	—	0/1	—	0	1	—	PCLBUZ0 = 0
	(TxD1)	Output	PIOR02 = 1	—	0/1	—	0	1	—	PCLBUZ0 = 0
	PCLBUZ0	Output	—	—	0	—	0	0	(SO10)/(TxD1) = 1	—
P03	P03	Input	—	—	×	0	1	×	×	×
		Output	—	—	0	0	0	0/1	(SDA10) = 1	TO00 = 0
		N-ch OD output	—	—	1	0	0	0/1		
	(SI10)	Input	PIOR02 = 1	—	×	0	1	×	×	×
	(RxD1)	Input	PIOR02 = 1	—	×	0	1	×	×	×
	(SDA10)	I/O	PIOR02 = 1	—	1	0	0	1	—	TO00 = 0
	TO00	Output	—	—	0	0	0	0	(SDA10) = 1	—
	ANI8	Analog input	—	—	×	1	1	×	×	×
P04	P04	Input	—	—	×	0	1	×	×	—
		Output	—	—	0	0	0	0/1	(SCK10)/(SCL10) = 1	—
		N-ch OD output	—	—	1	0	0	0/1		—
	(SCK10)	Input	PIOR02 = 1	—	×	0	1	×	×	—
		Output	PIOR02 = 1	—	0/1	0	0	1	—	—
	(SCL10)	Output	PIOR02 = 1	—	0/1	0	0	1	—	—
	INTP6	Input	—	—	×	0	1	×	×	—
	ANI9	Analog input	—	—	×	1	1	×	×	—
P05	P05	Input	—	—	—	0	1	×	—	×
		Output	—	—	—	0	0	0/1	—	TO06 = 0
	TI06	Input	PIOR33 = 0	—	—	0	1	×	—	×
	TO06	Output	PIOR33 = 0	—	—	0	0	0	—	—
	ANI10	Analog input	—	—	—	1	1	×	—	×
P06	P06	Input	—	—	×	—	1	×	×	—
		Output	—	—	0	—	0	0/1	SO20/TxD2 = 1	—
		N-ch OD output	—	—	1	—	0	0/1		—
	SO20	Output	—	—	0/1	—	0	1	—	—
	TxD2	Output	—	—	0/1	—	0	1	—	—
	TI00	Input	—	—	×	—	1	×	×	—
P07	P07	Input	—	—	×	—	1	×	×	×
		Output	—	—	0	—	0	0/1	SDA20 = 1	TO05 = 0
		N-ch OD output	—	—	1	—	0	0/1		
	SI20	Input	—	—	×	—	1	×	×	×
	RxD2	Input	—	—	×	—	1	×	×	×
	SDA20	I/O	—	—	1	—	0	1	—	TO05 = 0
	TI05	Input	PIOR31 = 0 PIOR30 = 0	—	×	—	1	×	×	×
	TO05	Output	PIOR31 = 0 PIOR30 = 0	—	0	—	0	0	SDA20 = 1	—

Table 4 - 8 Setting Examples of Registers and Output Latches When Using Pin Function (R5F11NG, R5F11PL) (2/5)

Port Name	Used Function		PIORXX	PFSEGXX	POMXX	PMCXX	PMXX	PXX	Alternate Function Output	
	Function Name	I/O							SAU Output Function	Other than SAU
P10	P10	Input	—	—	×	—	1	×	×	—
		Output	—	—	0	—	0	0/1	SCK20/SCL20 = 1	—
		N-ch OD output	—	—	1	—	0	0/1		—
	SCK20	Input	—	—	×	—	1	×	×	—
		Output	—	—	0/1	—	0	1	—	—
	SCL20	Output	—	—	0/1	—	0	1	—	—
	INTP2	Input	—	—	×	—	1	×	×	—
P30	P30	Input	—	—	—	—	1	×	—	×
		Output	—	—	—	—	0	0/1	—	RTC1HZ = 0
	INTP3	Input	PIOR13 = 0	—	—	—	1	×	—	×
	RTC1HZ	Output	—	—	—	—	0	0	—	—
P32	P32	Input	—	—	—	—	1	×	—	—
		Output	—	—	—	—	0	0/1	—	—
	INTP4	Input	PIOR14 = 0	—	—	—	1	×	—	—
	$\overline{SSI00}$	Input	—	—	—	—	1	×	—	—
P35	P35	Input	—	—	×	—	1	×	×	—
		Output	—	—	0	—	0	0/1	SCK00/SCL00 = 1	—
		N-ch OD output	—	—	1	—	0	0/1		—
	SCK00	Input	—	—	×	—	1	×	×	—
		Output	—	—	0/1	—	0	1	—	—
	SCL00	Output	—	—	0/1	—	0	1	—	—
P36	P36	Input	—	—	×	—	1	×	×	×
		Output	—	—	0	—	0	0/1	SDA00 = 1	PCLBUZ1 = 0
		N-ch OD output	—	—	1	—	0	0/1		
	SI00	Input	—	—	×	—	1	×	×	×
	RxD0	Input	—	—	×	—	1	×	×	×
	SDA00	I/O	—	—	1	—	0	1	—	PCLBUZ1 = 0
	PCLBUZ1	Output	—	—	0	—	0	0	SDA00 = 1	—
P37	P37	Input	—	—	×	—	1	×	×	—
		Output	—	—	0	—	0	0/1	SO00/TxD0 = 1	—
		N-ch OD output	—	—	1	—	0	0/1		—
	SO00	Output	—	—	0/1	—	0	1	—	—
	TxD0	Output	—	—	0/1	—	0	1	—	—
P40	P40	Input	—	—	—	—	1	×	—	×
		Output	—	—	—	—	0	0/1	—	TO01 = 0
	(INTP1)	Input	PIOR11 = 1	—	—	—	1	×	—	×
	TI01	Input	—	—	—	—	1	×	—	×
	TO01	Output	—	—	—	—	0	0	—	—
P50	P50	Input	—	—	×	—	1	×	×	×
		Output	—	—	0	—	0	0/1	SO10/TxD1 = 1	TO03 = 0
		N-ch OD output	—	—	1	—	0	0/1		
	SO10	Output	PIOR02 = 0	—	0/1	—	0	1	—	TO03 = 0
	TxD1	Output	PIOR02 = 0	—	0/1	—	0	1	—	TO03 = 0
	TI03	Input	—	—	×	—	1	×	×	×
	TO03	Output	—	—	0	—	0	0	SO10/TxD1 = 1	—

Table 4 - 8 Setting Examples of Registers and Output Latches When Using Pin Function (R5F11NG, R5F11PL) (3/5)

Port Name	Used Function		PIORXX	PFSEGXX	POMXX	PMCXX	PMXX	PXX	Alternate Function Output	
	Function Name	I/O							SAU Output Function	Other than SAU
P51	P51	Input	—	—	×	—	1	×	×	×
		Output	—	—	0	—	0	0/1	SDA10 = 1	TO04 = 0
		N-ch OD output	—	—	1	—	0	0/1		
	SI10	Input	PIOR02 = 0	—	×	—	1	×	×	×
	RxD1	Input	PIOR02 = 0	—	×	—	1	×	×	×
	SDA10	I/O	PIOR02 = 0	—	1	—	0	1	—	TO04 = 0
	TI04	Input	—	—	×	—	1	×	×	×
	TO04	Output	—	—	0	—	0	0	SDA10 = 1	—
P52	P52	Input	—	—	×	—	1	×	×	×
		Output	—	—	0	—	0	0/1	SCK10/SCL10 = 1	TO02 = 0
		N-ch OD output	—	—	1	—	0	0/1		
	SCK10	Input	PIOR02 = 0	—	×	—	1	×	×	×
		Output	PIOR02 = 0	—	0/1	—	0	1	—	TO02 = 0
	SCL10	Output	PIOR02 = 0	—	0/1	—	0	1	—	TO02 = 0
	TI02	Input	—	—	×	—	1	×	×	×
	TO02	Output	—	—	0	—	0	0	SCK10/SCL10 = 1	—
P53	P53	Input	—	—	—	—	1	×	—	—
		Output	—	—	—	—	0	0/1	—	—
	(INTP0)	Input	PIOR10 = 1	—	—	—	1	×	—	—
P60	P60	Input	—	—	—	—	1	×	—	×
		N-ch OD output (6-V tolerance)	—	—	—	—	0	0/1	—	SCLA0 = 0
	SCLA0	I/O	—	—	—	—	0	0	—	—
	(INTP3)	Input	PIOR13 = 1	—	—	—	1	×	—	×
P61	P61	Input	—	—	—	—	1	×	—	×
		N-ch OD output (6-V tolerance)	—	—	—	—	0	0/1	—	SDAA0 = 0
	SDAA0	I/O	—	—	—	—	0	0	—	—
	(INTP4)	Input	PIOR14 = 1	—	—	—	1	×	—	×
P70	P70	Input	—	—	—	—	1	×	—	—
		Output	—	—	—	—	0	0/1	—	—
P71	P71	Input	—	—	—	—	1	×	—	×
		Output	—	—	—	—	0	0/1	—	(TO05) = 0
	(TI05)	Input	PIOR31 = 1 PIOR30 = 1	—	—	—	1	×	—	×
	(TO05)	Output	PIOR31 = 1 PIOR30 = 1	—	—	—	0	0	—	—
P76	P76	Input	—	—	—	—	1	×	—	×
		Output	—	—	—	—	0	0/1	—	(TO06) = 0
	(TI06)	Input	PIOR33 = 1	—	—	—	1	×	—	×
	(TO06)	Output	PIOR33 = 1	—	—	—	0	0	—	—
P77	P77	Input	—	—	—	—	1	×	—	×
		Output	—	—	—	—	0	0/1	—	TO07 = 0
	TI07	Input	—	—	—	—	1	×	—	×
	TO07	Output	—	—	—	—	0	0	—	—

Table 4 - 8 Setting Examples of Registers and Output Latches When Using Pin Function (R5F11NG, R5F11PL) (4/5)

Port Name	Used Function		PIORXX	CMC (EXCLK, OSCSEL, EXCLKS, OSCSELS)	PXX
	Function Name	I/O			
P121	P121	Input	—	00xx/10xx/11xx	×
	X1	—	—	01xx	—
	INTP1	Input	PIOR11 = 0	00xx/10xx/11xx	×
P122	P122	Input	—	00xx/10xx	×
	X2	—	—	01xx	—
	EXCLK	—	—	11xx	—
	INTP5	Input	PIOR15 = 0	00xx/10xx	×
P123	P123	Input	—	xx00/xx10/xx11	×
	XT1	—	—	xx01	—
P124	P124	Input	—	xx00/xx10	×
	XT2	—	—	xx01	—
	EXCLKS	—	—	xx11	—

Table 4 - 8 Setting Examples of Registers and Output Latches When Using Pin Function (R5F11NG, R5F11PL) (5/5)

Port Name	Used Function		PIORXX	POMXX	PMCXX	PMXX	PXX	ISCLCD	Alternate Function Output	
	Function Name	I/O							SAU Output Function	Other than SAU
P137	P137	Input	—	—	—	—	×	—	—	—
	INTP0	Input	PIOR10 = 0	—	—	—	×	—	—	—

Table 4 - 9 Setting Examples of Registers and Output Latches When Using Pin Function (R5F11RM) (1/8)

Port Name	Used Function		PIORXX	PFSEGXX	POMXX	PMCXX	PMXX	PXX	Alternate Function Output	
	Function Name	I/O							Output Function of SAU and UARTMG	Other than SAU and UARTMG
P01	P01	Input	—	PFSEG22 = 0	—	—	1	×	—	—
		Output	—	PFSEG22 = 0	—	—	0	0/1	—	—
	SEG22	Output	—	PFSEG22 = 1	—	—	0	0	—	—
P02	P02	Input	—	PFSEG23 = 0	×	—	1	×	×	×
		Output	—	PFSEG23 = 0	0	—	0	0/1	(SO10)/(TxD1) = 1	PCLBUZ0 = 0
		N-ch OD output	—	PFSEG23 = 0	1	—	0	0/1		
	(SO10)	Output	PIOR02 = 1	PFSEG23 = 0	0/1	—	0	1	—	PCLBUZ0 = 0
	(TxD1)	Output	PIOR02 = 1	PFSEG23 = 0	0/1	—	0	1	—	PCLBUZ0 = 0
	PCLBUZ0	Output	—	PFSEG23 = 0	0	—	0	0	(SO10)/(TxD1) = 1	—
	SEG23	Output	—	PFSEG23 = 1	0	—	0	0	×	×
P03	P03	Input	—	PFSEG24 = 0	×	0	1	×	×	×
		Output	—	PFSEG24 = 0	0	0	0	0/1	(SDA10) = 1	TO00 = 0
		N-ch OD output	—	PFSEG24 = 0	1	0	0	0/1		
	(SI10)	Input	PIOR02 = 1	PFSEG24 = 0	×	0	1	×	×	×
	(RxD1)	Input	PIOR02 = 1	PFSEG24 = 0	×	0	1	×	×	×
	(SDA10)	I/O	PIOR02 = 1	PFSEG24 = 0	1	0	0	1	—	TO00 = 0
	TO00	Output	PIOR22 = 0	PFSEG24 = 0	0	0	0	0	(SDA10) = 1	—
	ANI8	Analog input	—	PFSEG24 = 1	×	1	1	×	×	×
	SEG24	Output	—	PFSEG24 = 1	0	0	0	0	×	×
P04	P04	Input	—	PFSEG25 = 0	×	0	1	×	×	—
		Output	—	PFSEG25 = 0	0	0	0	0/1	(SCK10)/(SCL10) = 1	—
		N-ch OD output	—	PFSEG25 = 0	1	0	0	0/1		—
	(SCK10)	Input	PIOR02 = 1	PFSEG25 = 0	×	0	1	×	×	—
		Output	PIOR02 = 1	PFSEG25 = 0	0/1	0	0	1	—	—
	(SCL10)	Output	PIOR02 = 1	PFSEG25 = 0	0/1	0	0	1	—	—
	ANI9	Analog input	—	PFSEG25 = 1	×	1	1	×	×	—
	SEG25	Output	—	PFSEG25 = 1	0	0	0	0	×	—
P05	P05	Input	—	PFSEG26 = 0	—	0	1	×	—	×
		Output	—	PFSEG26 = 0	—	0	0	0/1	—	TO06 = 0
	TI06	Input	PIOR32 = 0	PFSEG26 = 0	—	0	1	×	—	×
	TO06	Output	PIOR32 = 0	PFSEG26 = 0	—	0	0	0	—	—
	ANI10	Analog input	—	PFSEG26 = 1	—	1	1	×	—	×
	SEG26	Output	—	PFSEG26 = 1	—	0	0	0	—	×
P06	P06	Input	—	PFSEG27 = 0	×	—	1	×	×	—
		Output	—	PFSEG27 = 0	0	—	0	0/1	SO20/TxD2 = 1	—
		N-ch OD output	—	PFSEG27 = 0	1	—	0	0/1		—
	SO20	Output	PIOR01 = 0	PFSEG27 = 0	0/1	—	0	1	—	—
	TxD2	Output	PIOR01 = 0	PFSEG27 = 0	0/1	—	0	1	—	—
	TI00	Input	PIOR20 = 0	PFSEG27 = 0	×	—	1	×	×	—
	SEG27	Output	—	PFSEG27 = 1	0	—	0	0	×	—
P07	P07	Input	—	PFSEG28 = 0	×	—	1	×	×	×
		Output	—	PFSEG28 = 0	0	—	0	0/1	SDA20 = 1	TO05 = 0
		N-ch OD output	—	PFSEG28 = 0	1	—	0	0/1		
	SI20	Input	PIOR01 = 0	PFSEG28 = 0	×	—	1	×	×	×
	RxD2	Input	PIOR01 = 0	PFSEG28 = 0	×	—	1	×	×	×
	SDA20	I/O	PIOR01 = 0	PFSEG28 = 0	1	—	0	1	—	TO05 = 0
	TI05	Input	PIOR30 = 0	PFSEG28 = 0	×	—	1	×	×	×
	TO05	Output	PIOR30 = 0	PFSEG28 = 0	0	—	0	0	SDA20 = 1	—
	SEG28	Output	—	PFSEG28 = 1	0	—	0	0	×	×

Table 4 - 9 Setting Examples of Registers and Output Latches When Using Pin Function (R5F11RM) (2/8)

Port Name	Used Function		PIORXX	PFSEGXX	POMXX	PMCXX	PMXX	PXX	Alternate Function Output	
	Function Name	I/O							Output Function of SAU and UARTMG	Other than SAU and UARTMG
P10	P10	Input	—	PFSEG29 = 0	×	—	1	×	×	—
		Output	—	PFSEG29 = 0	0	—	0	0/1	SCK20/SCL20 = 1	—
		N-ch OD output	—	PFSEG29 = 0	1	—	0	0/1		—
	SCK20	Input	PIOR01 = 0	PFSEG29 = 0	×	—	1	×	×	—
		Output	PIOR01 = 0	PFSEG29 = 0	0/1	—	0	1	—	—
	SCL20	Output	PIOR01 = 0	PFSEG29 = 0	0/1	—	0	1	—	—
	SEG29	Output	—	PFSEG29 = 1	0	—	0	0	×	—
P11	P11	Input	—	PFSEG30 = 0	—	—	1	×	—	—
		Output	—	PFSEG30 = 0	—	—	0	0/1	—	—
	SEG30	Output	—	PFSEG30 = 1	—	—	0	0	—	—
P12	P12	Input	—	PFSEG31 = 0	×	—	1	×	×	—
		Output	—	PFSEG31 = 0	0	—	0	0/1	TxDMG0 = 1	—
		N-ch OD output	—	PFSEG31 = 0	1	—	0	0/1		—
	TxDMG0	Output	—	PFSEG31 = 0	0/1	—	0	1	—	—
	SEG31	Output	—	PFSEG31 = 1	0	—	0	0	×	—
P13	P13	Input	—	PFSEG32 = 0	—	—	1	×	—	—
		Output	—	PFSEG32 = 0	—	—	0	0/1	—	—
	RxDMG0	Input	—	PFSEG32 = 0	—	—	1	×	—	—
	SEG32	Output	—	PFSEG32 = 1	—	—	0	0	—	—
P14	P14	Input	—	PFSEG33 = 0	—	—	1	×	—	×
		Output	—	PFSEG33 = 0	—	—	0	0/1	—	TRJIO1 = 0
	TRJIO1	Input	—	PFSEG33 = 0	—	—	1	×	—	×
		Output	—	PFSEG33 = 0	—	—	0	0	—	—
	SEG33	Output	—	PFSEG33 = 1	—	—	0	0	—	×
P15	P15	Input	—	PFSEG34 = 0	—	—	1	×	—	×
		Output	—	PFSEG34 = 0	—	—	0	0/1	—	TRJIO0 = 0
	TRJIO0	Input	—	PFSEG34 = 0	—	—	1	×	—	×
		Output	—	PFSEG34 = 0	—	—	0	0	—	—
	SEG34	Output	—	PFSEG34 = 1	—	—	0	0	—	×
P16	P16	Input	—	PFSEG35 = 0	—	—	1	×	—	×
		Output	—	PFSEG35 = 0	—	—	0	0/1	—	SMO0 = 0
	SMO0	Output	—	PFSEG35 = 0	—	—	0	0	—	—
	SEG35	Output	—	PFSEG35 = 1	—	—	0	0	—	×
P17	P17	Input	—	—	—	—	1	×	—	×
		Output	—	—	—	—	0	0/1	—	SMO1 = 0
	SMO1	Output	—	—	—	—	0	0	—	—
P20	P20	Input	—	—	—	—	1	×	—	—
		Output	—	—	—	—	0	0/1	—	—
	SMP4	Input	—	—	—	—	1	×	—	—
P21	P21	Input	—	—	—	—	1	×	—	—
		Output	—	—	—	—	0	0/1	—	—
	SMP5	Input	—	—	—	—	1	×	—	—
P22	P22	Input	—	—	—	—	1	×	—	—
		Output	—	—	—	—	0	0/1	—	—
	INTP7	Input	—	—	—	—	1	×	—	—
P23	P23	Input	—	—	—	—	1	×	—	—
		Output	—	—	—	—	0	0/1	—	—
	INTP6	Input	—	—	—	—	1	×	—	—
P24	P24	Input	—	—	—	—	1	×	—	—
		Output	—	—	—	—	0	0/1	—	—
	(INTP5)	Input	PIOR15 = 1	—	—	—	1	×	—	—

Table 4 - 9 Setting Examples of Registers and Output Latches When Using Pin Function (R5F11RM) (3/8)

Port Name	Used Function		PIORXX	PFSEGXX	POMXX	PMCXX	PMXX	PXX	Alternate Function Output	
	Function Name	I/O							Output Function of SAU and UARTMG	Other than SAU and UARTMG
P25	P25	Input	—	—	—	—	1	×	—	—
		Output	—	—	—	—	0	0/1	—	—
	INTP4	Input	—	—	—	—	1	×	—	—
P26	P26	Input	—	—	—	—	1	×	—	—
		Output	—	—	—	—	0	0/1	—	—
	INTP3	Input	—	—	—	—	1	×	—	—
P27	P27	Input	—	—	—	—	1	×	—	—
		Output	—	—	—	—	0	0/1	—	—
	INTP2	Input	—	—	—	—	1	×	—	—
P30	P30	Input	—	PFSEG16 = 0	—	—	1	×	—	×
		Output	—	PFSEG16 = 0	—	—	0	0/1	—	RTC1HZ = 0
	RTC1HZ	Output	—	PFSEG16 = 0	—	—	0	0	—	—
	SEG16	Output	—	PFSEG16 = 1	—	—	0	0	—	×
P31	P31	Input	—	PFSEG17 = 0	—	—	1	×	—	×
		Output	—	PFSEG17 = 0	—	—	0	0/1	—	TO01 = 0
	TI01	Input	PIOR24 = 0	PFSEG17 = 0	—	—	1	×	—	×
	TO01	Output	PIOR24 = 0	PFSEG17 = 0	—	—	0	0	—	—
	SEG17	Output	—	PFSEG17 = 1	—	—	0	0	—	×
P32	P32	Input	—	PFSEG18 = 0	—	—	1	×	—	—
		Output	—	PFSEG18 = 0	—	—	0	0/1	—	—
	$\overline{SSI00}$	Input	PIOR05 = 0	PFSEG18 = 0	—	—	1	×	—	—
	SEG18	Output	—	PFSEG18 = 1	—	—	0	0	—	—
P35	P35	Input	—	PFSEG19 = 0	×	—	1	×	×	—
		Output	—	PFSEG19 = 0	0	—	0	0/1	SCK00/SCL00 = 1	—
		N-ch OD output	—	PFSEG19 = 0	1	—	0	0/1		—
	SCK00	Input	PIOR00 = 0	PFSEG19 = 0	×	—	1	×	×	—
		Output	PIOR00 = 0	PFSEG19 = 0	0/1	—	0	1	—	—
	SCL00	Output	PIOR00 = 0	PFSEG19 = 0	0/1	—	0	1	—	—
	SEG19	Output	—	PFSEG19 = 1	0	—	0	0	×	—
P36	P36	Input	—	PFSEG20 = 0	×	—	1	×	×	×
		Output	—	PFSEG20 = 0	0	—	0	0/1	SDA00 = 1	PCLBUZ1 = 0
		N-ch OD output	—	PFSEG20 = 0	1	—	0	0/1		
	SI00	Input	PIOR00 = 0	PFSEG20 = 0	×	—	1	×	×	×
	RxD0	Input	PIOR00 = 0	PFSEG20 = 0	×	—	1	×	×	×
	SDA00	I/O	PIOR00 = 0	PFSEG20 = 0	1	—	0	1	—	PCLBUZ1 = 0
	PCLBUZ1	Output	PIOR03 = 0	PFSEG20 = 0	0	—	0	0	SDA00 = 1	—
	SEG20	Output	—	PFSEG20 = 1	0	—	0	0	×	×
P37	P37	Input	—	PFSEG21 = 0	×	—	1	×	×	—
		Output	—	PFSEG21 = 0	0	—	0	0/1	SO00/TxD0 = 1	—
		N-ch OD output	—	PFSEG21 = 0	1	—	0	0/1		—
	SO00	Output	PIOR00 = 0	PFSEG21 = 0	0/1	—	0	1	—	—
	TxD0	Output	PIOR00 = 0	PFSEG21 = 0	0/1	—	0	1	—	—
	SEG21	Output	—	PFSEG21 = 1	0	—	0	0	×	—

Table 4 - 9 Setting Examples of Registers and Output Latches When Using Pin Function (R5F11RM) (4/8)

Port Name	Used Function		PIORXX	PFSEGXX	POMXX	PMCXX	PMXX	PXX	Alternate Function Output	
	Function Name	I/O							Output Function of SAU and UARTMG	Other than SAU and UARTMG
P40	P40	Input	—	—	×	—	1	×	×	×
		Output	—	—	0	—	0	0/1	(SCK00)/(SCL00) = 1	(TO01) = 0
		N-ch OD output	—	—	1	—	0	0/1		
	(SCK00)	Input	PIOR00 = 1	—	×	—	1	×	×	×
		Output	PIOR00 = 1	—	0/1	—	0	1	—	(TO01) = 0
	(SCL00)	Output	PIOR00 = 1	—	0/1	—	0	1	—	(TO01) = 0
	(TI01)	Input	PIOR24 = 1	—	×	—	1	×	×	×
	(TO01)	Output	PIOR24 = 1	—	0	—	0	0	(SCK00)/(SCL00) = 1	—
P43	P43	Input	—	—	×	—	1	×	×	—
		Output	—	—	0	—	0	0/1	(SDA00) = 1	—
		N-ch OD output	—	—	1	—	0	0/1		
	(SI00)	Input	PIOR00 = 1	—	×	—	1	×	×	—
	(RxD0)	Input	PIOR00 = 1	—	×	—	1	×	×	—
	(SDA00)	I/O	PIOR00 = 1	—	1	—	0	1	—	—
	(SMP0)	Input	PIOR04 = 1	—	×	—	1	×	×	—
P44	P44	Input	—	—	×	—	1	×	×	—
		Output	—	—	0	—	0	0/1	(SO00)/(TxD0) = 1	—
		N-ch OD output	—	—	1	—	0	0/1		—
	(SO00)	Output	PIOR00 = 1	—	0/1	—	0	1	—	—
	(TxD0)	Output	PIOR00 = 1	—	0/1	—	0	1	—	—
	(SMP1)	Input	PIOR04 = 1	—	×	—	1	×	×	—
P50	P50	Input	—	PFSEG07 = 0	×	—	1	×	×	×
		Output	—	PFSEG07 = 0	0	—	0	0/1	SO10/TxD1 = 1	TO03 = 0
		N-ch OD output	—	PFSEG07 = 0	1	—	0	0/1		
	SO10	Output	PIOR02 = 0	PFSEG07 = 0	0/1	—	0	1	—	TO03 = 0
	TxD1	Output	PIOR02 = 0	PFSEG07 = 0	0/1	—	0	1	—	TO03 = 0
	TI03	Input	PIOR26 = 0	PFSEG07 = 0	×	—	1	×	×	×
	TO03	Output	PIOR26 = 0	PFSEG07 = 0	0	—	0	0	SO10/TxD1 = 1	—
	SEG7	Output	—	PFSEG07 = 1	0	—	0	0	×	×
P51	P51	Input	—	PFSEG06 = 0	×	—	1	×	×	×
		Output	—	PFSEG06 = 0	0	—	0	0/1	SDA10 = 1	TO04 = 0
		N-ch OD output	—	PFSEG06 = 0	1	—	0	0/1		
	SI10	Input	PIOR02 = 0	PFSEG06 = 0	×	—	1	×	×	×
	RxD1	Input	PIOR02 = 0	PFSEG06 = 0	×	—	1	×	×	×
	SDA10	I/O	PIOR02 = 0	PFSEG06 = 0	1	—	0	1	—	TO04 = 0
	TI04	Input	PIOR27 = 0	PFSEG06 = 0	×	—	1	×	×	×
	TO04	Output	PIOR27 = 0	PFSEG06 = 0	0	—	0	0	SDA10 = 1	—
	SEG6	Output	—	PFSEG06 = 1	0	—	0	0	×	×
P52	P52	Input	—	PFSEG05 = 0	×	—	1	×	×	×
		Output	—	PFSEG05 = 0	0	—	0	0/1	SCK10/SCL10 = 1	TO02 = 0
		N-ch OD output	—	PFSEG05 = 0	1	—	0	0/1		
	SCK10	Input	PIOR02 = 0	PFSEG05 = 0	×	—	1	×	×	×
		Output	PIOR02 = 0	PFSEG05 = 0	0/1	—	0	1	—	TO02 = 0
	SCL10	Output	PIOR02 = 0	PFSEG05 = 0	0/1	—	0	1	—	TO02 = 0
	TI02	Input	PIOR25 = 0	PFSEG05 = 0	×	—	1	×	×	×
	TO02	Output	PIOR25 = 0	PFSEG05 = 0	0	—	0	0	SCK10/SCL10 = 1	—
	SEG5	Output	—	PFSEG05 = 1	0	—	0	0	×	×
P53	P53	Input	—	PFSEG04 = 0	—	—	1	×	—	—
		Output	—	PFSEG04 = 0	—	—	0	0/1	—	—
	SEG4	Output	—	PFSEG04 = 1	—	—	0	0	—	—

Table 4 - 9 Setting Examples of Registers and Output Latches When Using Pin Function (R5F11RM) (5/8)

Port Name	Used Function		PIORXX	PFSEGXX	POMXX	PMCXX	PMXX	PXX	Alternate Function Output	
	Function Name	I/O							Output Function of SAU and UARTMG	Other than SAU and UARTMG
P60	P60	Input	—	—	—	—	1	×	—	×
		N-ch OD output (6-V tolerance)	—	—	—	—	0	0/1	—	SCLA0 = 0
	SCLA0	I/O	—	—	—	—	0	0	—	—
P61	P61	Input	—	—	—	—	1	×	—	×
		N-ch OD output (6-V tolerance)	—	—	—	—	0	0/1	—	SDAA0 = 0
	SDAA0	I/O	—	—	—	—	0	0	—	—
P70	P70	Input	—	PFSEG08 = 0	—	—	1	×	—	—
		Output	—	PFSEG08 = 0	—	—	0	0/1	—	—
	SEG8	Output	—	PFSEG08 = 1	—	—	0	0	—	—
P71	P71	Input	—	PFSEG09 = 0	—	—	1	×	—	—
		Output	—	PFSEG09 = 0	—	—	0	0/1	—	—
	SEG9	Output	—	PFSEG09 = 1	—	—	0	0	—	—
P72	P72	Input	—	PFSEG10 = 0	—	—	1	×	—	—
		Output	—	PFSEG10 = 0	—	—	0	0/1	—	—
	SEG10	Output	—	PFSEG10 = 1	—	—	0	0	—	—
P73	P73	Input	—	PFSEG11 = 0	—	—	1	×	—	—
		Output	—	PFSEG11 = 0	—	—	0	0/1	—	—
	SEG11	Output	—	PFSEG11 = 1	—	—	0	0	—	—
P74	P74	Input	—	PFSEG12 = 0	—	—	1	×	—	—
		Output	—	PFSEG12 = 0	—	—	0	0/1	—	—
	SEG12	Output	—	PFSEG12 = 1	—	—	0	0	—	—
P75	P75	Input	—	PFSEG13 = 0	—	—	1	×	—	—
		Output	—	PFSEG13 = 0	—	—	0	0/1	—	—
	SEG13	Output	—	PFSEG13 = 1	—	—	0	0	—	—
P76	P76	Input	—	PFSEG14 = 0	—	—	1	×	—	—
		Output	—	PFSEG14 = 0	—	—	0	0/1	—	—
	SEG14	Output	—	PFSEG14 = 1	—	—	0	0	—	—
P77	P77	Input	—	PFSEG15 = 0	—	—	1	×	—	×
		Output	—	PFSEG15 = 0	—	—	0	0/1	—	TO07 = 0
	TI07	Input	PIOR34 = 0	PFSEG15 = 0	—	—	1	×	—	×
	TO07	Output	PIOR34 = 0	PFSEG15 = 0	—	—	0	0	—	—
	SEG15	Output	—	PFSEG15 = 1	—	—	0	0	—	×
P80	P80	Input	—	—	×	—	1	×	×	—
		Output	—	—	0	—	0	0/1	(SO20)/(TxD2) = 1	(TO02) = 0 TRJO0 = 0
		N-ch OD output	—	—	1	—	0	0/1		
	(SO20)	Output	PIOR01 = 1	—	0/1	—	0	1	—	(TO02) = 0 TRJO0 = 0
	(TxD2)	Output	PIOR01 = 1	—	0/1	—	0	1	—	(TO02) = 0 TRJO0 = 0
	(TI02)	Input	PIOR25 = 1	—	×	—	1	×	×	×
	(TO02)	Output	PIOR25 = 1	—	0	—	0	0	(SO20)/(TxD2) = 1	TRJO0 = 0
	TRJO0	Output	—	—	0	—	0	0	(SO20)/(TxD2) = 1	(TO02) = 0

Table 4 - 9 Setting Examples of Registers and Output Latches When Using Pin Function (R5F11RM) (6/8)

Port Name	Used Function		PIORXX	PFSEGXX	POMXX	PMCXX	PMXX	PXX	Alternate Function Output	
	Function Name	I/O							Output Function of SAU and UARTMG	Other than SAU and UARTMG
P81	P81	Input	—	—	×	—	1	×	×	×
		Output	—	—	0	—	0	0/1	(SDA20) = 1	(TO00) = 0 TRJO1 = 0
		N-ch OD output	—	—	1	—	0	0/1		
	(SI20)	Input	PIOR01 = 1	—	×	—	1	×	×	×
	(RxD2)	Input	PIOR01 = 1	—	×	—	1	×	×	×
	(SDA20)	I/O	PIOR01 = 1	—	1	—	0	1	—	(TO00) = 0 TRJO1 = 0
	(TI00)	Input	PIOR20 = 1	—	×	—	1	×	×	×
	(TO00)	Output	PIOR22 = 1	—	0	—	0	0	(SDA20) = 1	TRJO1 = 0
	TRJO1	Output	—	—	0	—	0	0	(SDA20) = 1	(TO00) = 0
P82	P82	Input	—	—	×	—	1	×	×	×
		Output	—	—	0	—	0	0/1	(SCK20)/(SCL20) = 1	(TO07) = 0 EXSDO0 = 0
		N-ch OD output	—	—	1	—	0	0/1		
	(SCK20)	Input	PIOR01 = 1	—	×	—	1	×	×	×
		Output	PIOR01 = 1	—	0/1	—	0	1	—	(TO07) = 0 EXSDO0 = 0
	(SCL20)	Output	PIOR01 = 1	—	0/1	—	0	1	—	(TO07) = 0 EXSDO0 = 0
	(TI07)	Input	PIOR34 = 1	—	×	—	1	×	×	×
	(TO07)	Output	PIOR34 = 1	—	0	—	0	0	(SCK20)/(SCL20) = 1	EXSDO0 = 0
	EXSDO0	Output	—	—	0	—	0	0	(SCK20)/(SCL20) = 1	(TO07) = 0
P83	P83	Input	—	—	—	—	1	×	—	×
		Output	—	—	—	—	0	0/1	—	(PCLBUZ1) = 0 (TO03) = 0 EXSDO1 = 0
	(PCLBUZ1)	Output	PIOR03 = 1	—	—	—	0	0	—	(TO03) = 0 EXSDO1 = 0
	(TI03)	Input	PIOR26 = 1	—	—	—	1	×	—	×
	(TO03)	Output	PIOR26 = 1	—	—	—	0	0	—	(PCLBUZ1) = 0 EXSDO1 = 0
	EXSDO1	Output	—	—	—	—	0	0	—	(PCLBUZ1) = 0 (TO03) = 0
P84	P84	Input	—	—	—	—	1	×	—	×
		Output	—	—	—	—	0	0/1	—	SMO2 = 0
	SMO2	Output	—	—	—	—	0	0	—	—
P85	P85	Input	—	—	—	—	1	×	—	—
		Output	—	—	—	—	0	0/1	—	—
	SMP0	Input	PIOR04 = 0	—	—	—	1	×	—	—
	EXSDI0	Input	—	—	—	—	1	×	—	—
P86	P86	Input	—	—	—	—	1	×	—	—
		Output	—	—	—	—	0	0/1	—	—
	SMP1	Input	PIOR04 = 0	—	—	—	1	×	—	—
	EXSDI1	Input	—	—	—	—	1	×	—	—

Table 4 - 9 Setting Examples of Registers and Output Latches When Using Pin Function (R5F11RM) (7/8)

Port Name	Used Function		PIORXX	CMC (EXCLK, OSCSEL, EXCLKS, OSCSELS)	PXX
	Function Name	I/O			
P121	P121	Input	—	00xx/10xx/11xx	×
	X1	—	—	01xx	—
	INTP1	Input	—	00xx/10xx/11xx	×
P122	P122	Input	—	00xx/10xx	×
	X2	—	—	01xx	—
	EXCLK	—	—	11xx	—
	INTP5	Input	PIOR15 = 0	00xx/10xx	×
P123	P123	Input	—	xx00/xx10/xx11	×
	XT1	—	—	xx01	—
P124	P124	Input	—	xx00/xx10	×
	XT2	—	—	xx01	—
	EXCLKS	—	—	xx11	—

Table 4 - 9 Setting Examples of Registers and Output Latches When Using Pin Function (R5F11RM) (8/8)

Port Name	Used Function		PIORXX	POMXX	PMCXX	PMXX	PXX	ISCLCD	Alternate Function Output	
	Function Name	I/O							Output Function of SAU and UARTMG	Other than SAU and UARTMG
P125	P125	Input	—	—	—	1	×	ISCVL3 = 1	—	×
		Output	—	—	—	0	0/1	ISCVL3 = 1	—	(TO06) = 0
	VL3	I/O	—	—	—	1	0	ISCVL3 = 0	—	×
	(TI06)	Input	PIOR32 = 1	—	—	1	x	ISCVL3 = 1	—	×
	(TO06)	Output	PIOR32 = 1	—	—	0	0	ISCVL3 = 1	—	—
P126	P126	Input	—	—	—	1	×	ISCCAP = 1	—	×
		Output	—	—	—	0	0/1	ISCCAP = 1	—	(TO05) = 0
	CAPL	Output	—	—	—	1	0	ISCCAP = 0	—	×
	(TI05)	Input	PIOR30 = 1	—	—	1	x	ISCCAP = 1	—	×
	(TO05)	Output	PIOR30 = 1	—	—	0	0	ISCCAP = 1	—	—
P127	P127	Input	—	—	—	1	×	ISCCAP = 1	—	×
		Output	—	—	—	0	0/1	ISCCAP = 1	—	(TO04) = 0
	CAPH	Output	—	—	—	1	0	ISCCAP = 0	—	×
	(TI04)	Input	PIOR27 = 1	—	—	1	x	ISCCAP = 1	—	×
	(TO04)	Output	PIOR27 = 1	—	—	0	0	ISCCAP = 1	—	—
P137	P137	Input	—	—	—	—	×	—	—	—
	INTP0	Input	—	—	—	—	×	—	—	—
	($\overline{SSI00}$)	Input	PIOR05 = 1	—	—	—	×	—	—	—
P150	P150	Input	—	—	—	1	×	—	—	—
		Output	—	—	—	0	0/1	—	—	—
	SMP2	Input	—	—	—	1	×	—	—	—
P151	P151	Input	—	—	—	1	×	—	—	—
		Output	—	—	—	0	0/1	—	—	—
	SMP3	Input	—	—	—	1	×	—	—	—

4.6.4 Operation of ports that alternately function as SEGxx pins

The functions of ports that also serve as segment output pins (SEGxx) can be selected by using the port mode control register (PMCxx), port mode register (PMxx), and LCD port function registers 0 to 4 (PFSEG0 to PFSEG4).

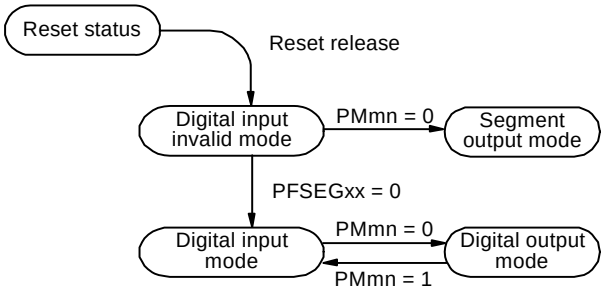
- P01 to P07, P10 to P16, P30 to P32, P35 to P37, P50 to P53, P70 to P77
  (ports that do not serve as analog input pins)

Table 4 - 10 Settings of SEGxx/Port Pin Function

PFSEGxx Bit of PFSEG0 to PFSEG4 Registers	PMxx Bit of PMxx Register	Pin Function	Initial Status
1	1	Digital input invalid mode	√
0	0	Digital output mode	—
0	1	Digital input mode	—
1	0	Segment output mode	—

The following shows the SEGxx/port pin function status transitions.

Figure 4 - 14 SEGxx/Port Pin Function Status Transitions



Caution Be sure to set the segment output mode before segment output starts (while SCOC bit of LCD mode register 1 (LCDM1) is 0).

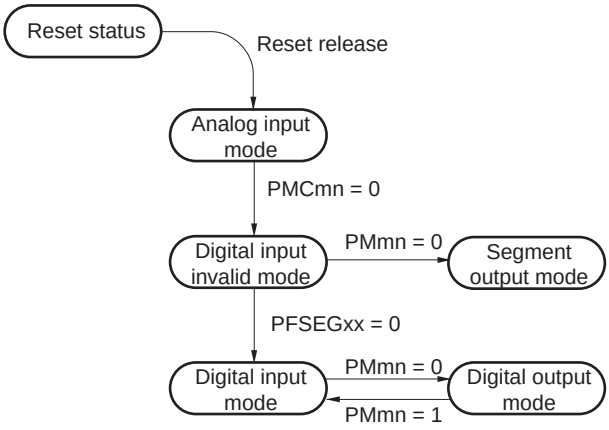
• P03 to P05 and P11 (ports that serve as analog input pins (ANIxx))

Table 4 - 11 Settings of ANIxx/SEGxx/Port Pin Function

PMCxx Bit of PMCxx Register	PFSEGxx Bit of PFSEG3 Register	PMxx Bit of PMxx Register	Pin Function	Initial Status
1	1	1	Analog input mode	√
0	0	0	Digital output mode	—
0	0	1	Digital input mode	—
0	1	0	Segment output mode	—
0	1	1	Digital input invalid mode	—
Other than above			Setting prohibited	

The following shows the ANIxx/SEGxx/port pin function status transitions.

Figure 4 - 15 ANIxx/SEGxx/Port Pin Function Status Transitions



Caution Be sure to set the segment output mode before segment output starts (while SCOC bit of LCD mode register 1 (LCDM1) is 0).

4.6.5 Operation of ports that alternately function as V_{L3}, CAPL, and CAPH pins

The functions of the V_{L3}/P125, CAPL/P126, and CAPH/P127 pins can be selected by using the LCD input switch control register (ISCLCD), LCD mode register 0 (LCDM0), and port mode register 12 (PM12).

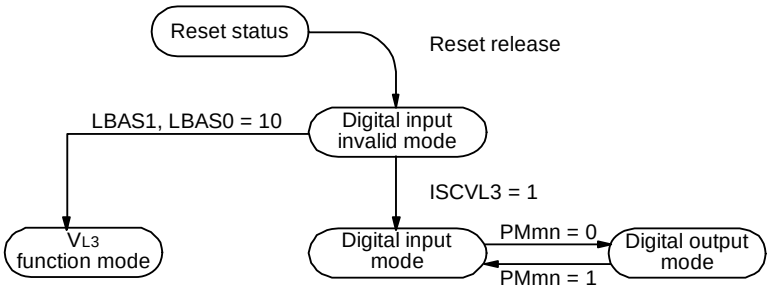
• V_{L3}/P125

Table 4 - 12 Settings of V_{L3}/P125 Pin Function

Bias Setting (LBAS1 and LBAS0 Bits of LCDM0 Register)	ISCVL3 Bit of ISCLCD Register	PM125 Bit of PM12 Register	Pin Function	Initial Status
Other than 1/4 bias method (LBAS1, LBAS0 = 00 or 01)	0	1	Digital input invalid mode	√
	1	0	Digital output mode	—
	1	1	Digital input mode	—
1/4 bias method (LBAS1, LBAS0 = 10)	0	1	V_{L3} function mode	—
Other than above			Setting prohibited	

The following shows the V_{L3}/P125 pin function status transitions.

Figure 4 - 16 V_{L3}/P125 Pin Function Status Transitions



Caution Be sure to set the V_{L3} function mode before segment output starts (while SCOC bit of LCD mode register 1 (LCDM1) is 0).

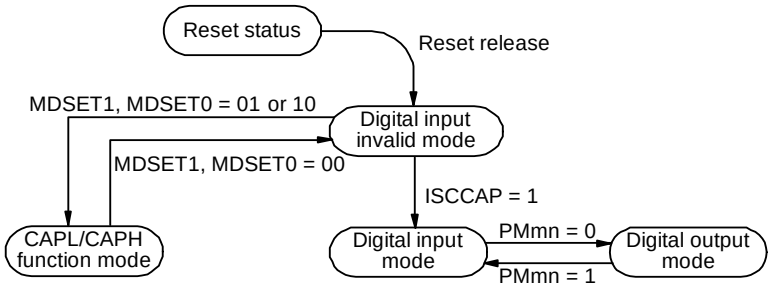
- **CAPL/P126, CAPH/P127**

Table 4 - 13 Settings of CAPL/P126 and CAPH/P127 Pin Functions

LCD Drive Voltage Generator (MDSET1 and MDSET0 Bits of LCDM0 Register)	ISCCAP Bit of ISCLCD Register	PM126 and PM127 Bits of PM12 Register	Pin Function	Initial Status
External resistance division (MDSET1, MDSET0 = 00)	0	1	Digital input invalid mode	√
	1	0	Digital output mode	—
	1	1	Digital input mode	—
Internal voltage boosting or capacitor split (MDSET1, MDSET0 = 01 or 10)	0	1	CAPL/CAPH function mode	—
Other than above			Setting prohibited	

The following shows the CAPL/P126 and CAPH/P127 pin function status transitions.

Figure 4 - 17 CAPL/P126 and CAPH/P127 Pin Function Status Transitions



Caution Be sure to set the CAPL/CAPH function mode before segment output starts (while SCOC bit of LCD mode register 1 (LCDM1) is 0).

4.7 Cautions When Using Port Function

4.7.1 Cautions on 1-Bit Manipulation Instruction for Port Register n (Pn)

When a 1-bit manipulation instruction is executed on a port that provides both input and output functions, the output latch value of an input port that is not subject to manipulation may be written in addition to the targeted bit.
Therefore, it is recommended to rewrite the output latch when switching a port from input mode to output mode.

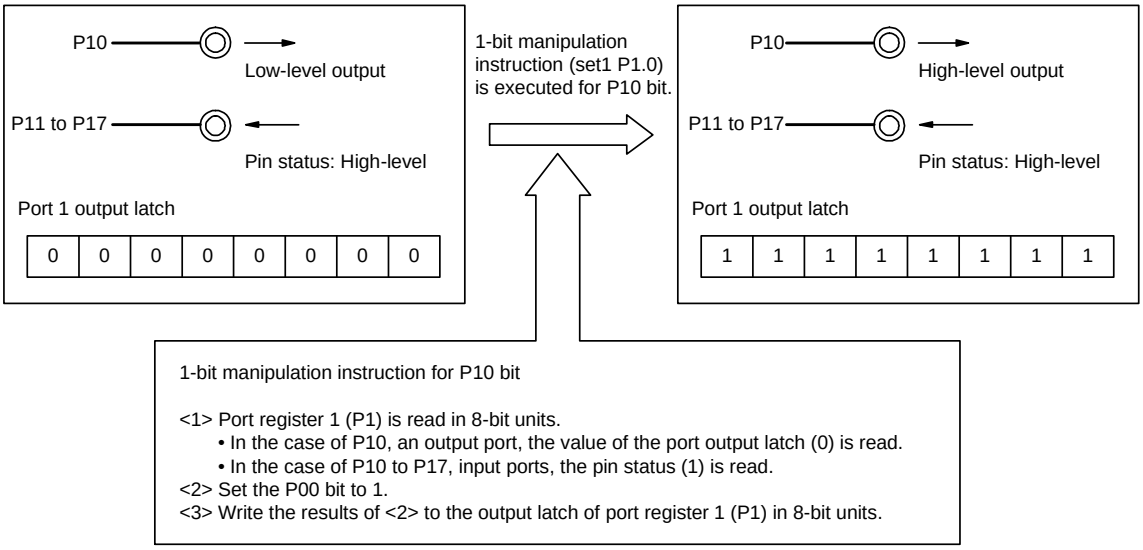
<Example> When P10 is an output port, P11 to P17 are input ports (all pin statuses are high level), and the port latch value of port 1 is 00H, if the output of output port P10 is changed from low level to high level via a 1-bit manipulation instruction, the output latch value of port 1 is FFH.

Explanation: The targets of writing to and reading from the Pn register of a port whose PMnm bit is 1 are the output latch and pin status, respectively.
A 1-bit manipulation instruction is executed in the following order in the RL78/H1D.

<1> The Pn register is read in 8-bit units.
<2> The targeted one bit is manipulated.
<3> The Pn register is written in 8-bit units.

In step <1>, the output latch value (0) of P10, which is an output port, is read, while the pin statuses of P11 to P17, which are input ports, are read. If the pin statuses of P11 to P17 are high level at this time, the read value is FEH.
The value is changed to FFH by the manipulation in <2>.
FFH is written to the output latch by the manipulation in <3>.

Figure 4 - 18 1-Bit Manipulation Instruction (P10)



4.7.2 Notes on specifying the pin settings

For an output pin to which multiple functions are assigned, the output of the unused alternate functions must be set to its initial state so as to prevent conflicting outputs. This also applies to the functions assigned by using the peripheral I/O redirection registers 0 to 3 (PIOR0 to PIOR3). For details about the alternate output function, see **4.6 Register Settings When Using Alternate Function**.

No specific setting is required for input pins because the output of their alternate functions is disabled (the buffer output is Hi-Z).

Disabling the unused functions, including blocks that are only used for input or do not have I/O, is recommended to lower power consumption.

CHAPTER 5 CLOCK GENERATOR

5.1 Functions of Clock Generator

The clock generator generates the clock to be supplied to the CPU and peripheral hardware.
The following three kinds of system clocks and clock oscillators are selectable.

(1) Main system clock

<1> X1 oscillator

This circuit oscillates a clock of f_X = 1 to 20 MHz by connecting a resonator to X1 pin and X2 pin. Oscillation can be stopped by executing the STOP instruction or setting of the MSTOP bit (bit 7 of the clock operation status control register (CSC)).

<2> High-speed on-chip oscillator

The frequency at which to oscillate can be selected from among f_{IH} = 24, 16, 12, 8, 6, 4, 3, 2, or 1 MHz (TYP.) by using the option byte (000C2H). After a reset release, the CPU always starts operating with this high-speed on-chip oscillator clock. Oscillation can be stopped by executing the STOP instruction or setting of the HIOSTOP bit (bit 0 of the CSC register).

The frequency specified by using the option byte can be changed by using the high-speed on-chip oscillator frequency select register (HOCODIV). For details about the frequency, see **Figure 5 - 12 Format of High-speed on-chip oscillator frequency select register (HOCODIV)**.

The frequencies that can be specified for the high-speed on-chip oscillator by using the option byte and the high-speed on-chip oscillator frequency select register (HOCODIV) are shown below.

Power Supply Voltage	Oscillation Frequency (MHz)								
	1	2	3	4	6	8	12	16	24
2.7 V ≤ V_{DD} ≤ 5.5 V	√	√	√	√	√	√	√	√	√
2.4 V ≤ V_{DD} ≤ 5.5 V	√	√	√	√	√	√	√	√	—
1.8 V ≤ V_{DD} ≤ 5.5 V Note	√	√	√	√	√	√	—	—	—

Note R5F11R only.

An external main system clock (f_{EX} = 1 to 20 MHz) can also be supplied from the EXCLK/X2/INTP5/P122 pin. An external main system clock input can be disabled by executing the STOP instruction or setting of the MSTOP bit. As the main system clock, a high-speed system clock (X1 clock or external main system clock) or high-speed on-chip oscillator clock can be selected by setting of the MCM0 bit (bit 4 of the system clock control register (CKC)).

(2) Subsystem clock

• XT1 clock oscillator

This circuit oscillates a clock of f_{XT} = 32.768 kHz or 38.4 kHz[Note] by connecting a 32.768 kHz or 38.4 kHz[Note] resonator to XT1 pin and XT2 pin. Oscillation can be stopped by setting the XTSTOP bit (bit 6 of the clock operation status control register (CSC)).

An external subsystem clock (f_{EXT} = 32.768 kHz or 38.4 kHz[Note]) can also be supplied from the EXCLKS/XT2/P124 pin. An external subsystem clock input can be disabled by the setting of the XTSTOP bit.

Note R5F11R only.

(3) Low-speed on-chip oscillator

This circuit oscillates a clock of f_{IL} = 15 kHz (TYP.).

The low-speed on-chip oscillator clock cannot be used as the CPU clock.

Only the following peripheral hardware runs on the low-speed on-chip oscillator clock.

- Watchdog timer
- Real-time clock 2
- 12-bit interval timer
- 8-bit interval timer
- LCD controller/driver
- Serial interface UARTMG0
- External signal sampler
- Sampling output timer detector
- Timers RJ0 and RJ1

This clock operates when bit 4 (WDTON) of the option byte (000C0H), bit 4 (WUTMMCK0) of the subsystem clock supply mode control register (OSMC), or both are set to 1.

However, when WDTON = 1, WUTMMCK0 = 0, and bit 0 (WDSTBYON) of the option byte (000C0H) is 0, oscillation of the low-speed on-chip oscillator stops if the HALT or STOP instruction is executed.

Caution The low-speed on-chip oscillator clock (f_{IL}) can only be selected as the real-time clock 2 count clock when the fixed-cycle interrupt function is used.

Remark f_X: X1 clock oscillation frequency
f_{IH}: High-speed on-chip oscillator clock frequency
f_{EX}: External main system clock frequency
f_{XT}: XT1 clock oscillation frequency
f_{EXT}: External subsystem clock frequency
f_{IL}: Low-speed on-chip oscillator frequency

5.2 Configuration of Clock Generator

The clock generator includes the following hardware.

Table 5 - 1 Configuration of Clock Generator

Item	Configuration
Control registers	Clock operation mode control register (CMC) System clock control register (CKC) Clock operation status control register (CSC) Oscillation stabilization time counter status register (OSTC) Oscillation stabilization time select register (OSTS) Peripheral enable registers 0, 1, 2 (PER0, PER1, PER2[Note]) Subsystem clock supply mode control register (OSMC) High-speed on-chip oscillator frequency select register (HOCODIV) High-speed on-chip oscillator trimming register (HIOTRM)
Oscillators	X1 oscillator XT1 oscillator High-speed on-chip oscillator Low-speed on-chip oscillator

Note R5F11R only.

Figure 5 - 1 Block Diagram of Clock Generator (R5F11N, R5F11P)

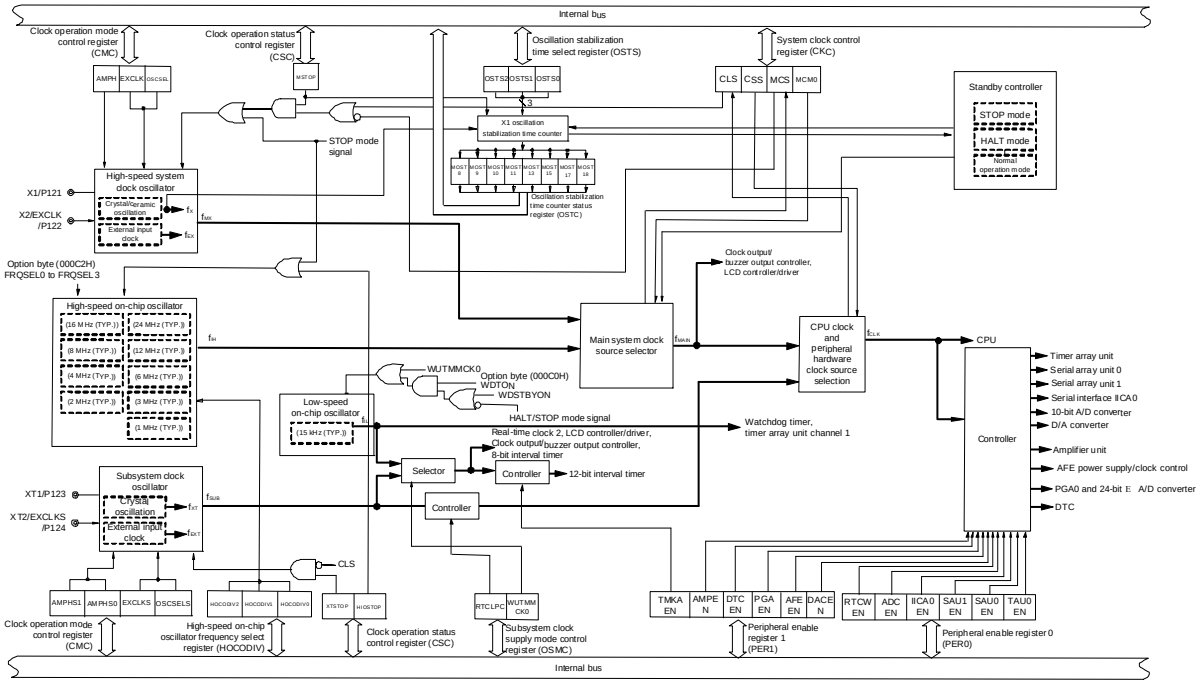
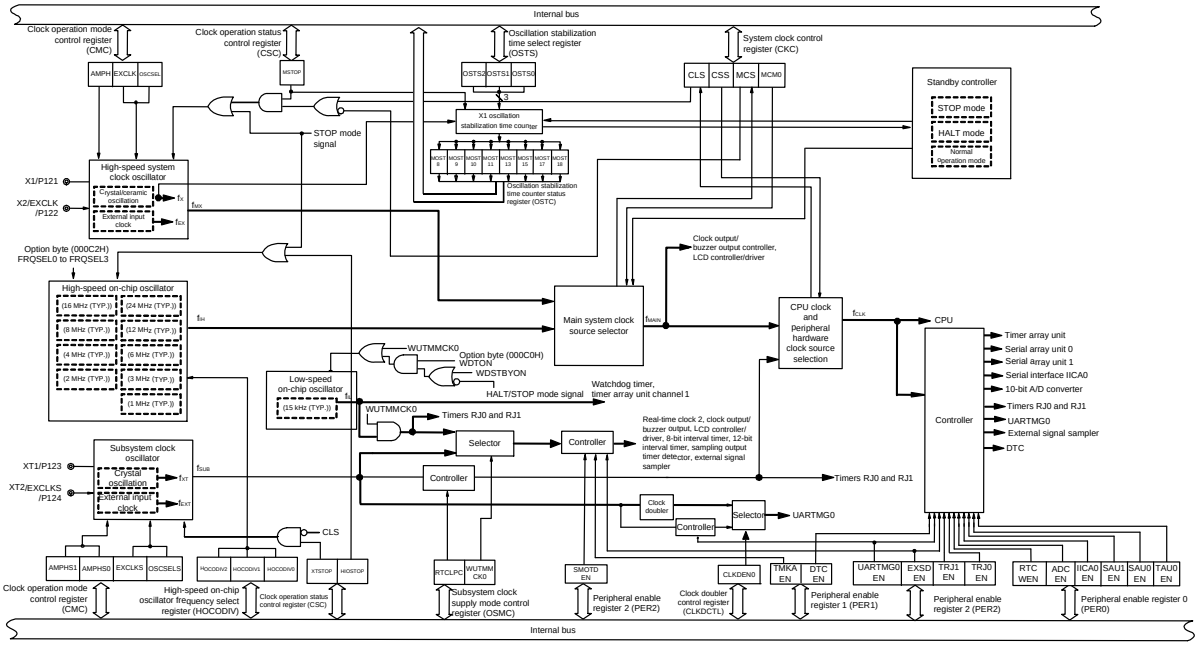


Figure 5 - 2 Block Diagram of Clock Generator (R5F11R)



Caution The low-speed on-chip oscillator clock cannot be selected as the operation clock for the serial interface UARTMG0, external signal sampler, and sampling output timer detector. When using the serial interface UARTMG0, external signal sampler, and sampling output timer detector, select the subsystem clock as the operation clock by setting the WUTMMCK0 to 0.

(**Remark** is listed on the next page.)

Remark f_X: X1 clock oscillation frequency
f_{IH}: High-speed on-chip oscillator clock frequency
f_{EX}: External main system clock frequency
f_{MX}: High-speed system clock frequency
f_{MAIN}: Main system clock frequency
f_{XT}: XT1 clock oscillation frequency
f_{EXT}: External subsystem clock frequency
f_{SUB}: Subsystem clock frequency
f_{CLK}: CPU/peripheral hardware clock frequency
f_{IL}: Low-speed on-chip oscillator clock frequency

5.3 Registers Controlling Clock Generator

The following registers are used to control the clock generator.

- Clock operation mode control register (CMC)
- System clock control register (CKC)
- Clock operation status control register (CSC)
- Oscillation stabilization time counter status register (OSTC)
- Oscillation stabilization time select register (OSTS)
- Peripheral enable registers 0, 1, 2 (PER0, PER1, PER2[Note])
- Subsystem clock supply mode control register (OSMC)
- High-speed on-chip oscillator frequency select register (HOCODIV)
- High-speed on-chip oscillator trimming register (HIOTRM)

Note R5F11R only.

Caution Which registers and bits are included depends on the product. Be sure to set registers and bits that are not mounted in a product to their initial values.

5.3.1 Clock operation mode control register (CMC)

This register is used to set the operation mode of the X1/INTP1/P121, X2/EXCLK/INTP5/P122, XT1/P123, and XT2/EXCLKS/P124 pins, and to select a gain of the oscillator.

The CMC register can be written only once by an 8-bit memory manipulation instruction after reset release. This register can be read by an 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Caution The EXCLKS, OSCSELS, AMPHS1, and AMPHS0 bits are reset only by a power-on reset; they retain the previous values when a reset caused by another factor occurs.

Figure 5 - 3 Format of clock operation mode control register (CMC)

Address: FFFA0H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
CMC	EXCLK	OSCSEL	EXCLKS Note	OSCSELS Note	0	AMPHS1 Note	AMPHS0 Note	AMPH

EXCLK	OSCSEL	High-speed system clock pin operation mode	X1/INTP1/P121 pin	X2/EXCLK//INTP5/P122 pin
0	0	Input port mode	Input port	
0	1	X1 oscillation mode	Crystal/ceramic resonator connection	
1	0	Input port mode	Input port	
1	1	External clock input mode	Input port	External clock input

EXCLKS Note	OSCSELS Note	Subsystem clock pin operation mode	XT1/P123 pin	XT2/EXCLKS/P124 pin
0	0	Input port mode	Input port	
0	1	XT1 oscillation mode	Crystal/ceramic resonator connection	
1	0	Input port mode	Input port	
1	1	External clock input mode	Input port	External clock input

AMPHS1 Note	AMPHS0 Note	XT1 oscillator oscillation mode selection
0	0	Low power consumption oscillation (default)
0	1	Normal oscillation
1	0	Ultra-low power consumption oscillation
1	1	Setting prohibited

AMPH	Control of X1 clock oscillation frequency
0	1 MHz ≤ fX ≤ 10 MHz
1	10 MHz < fX ≤ 20 MHz

Note The EXCLKS, OSCSELS, AMPHS1, and AMPHS0 bits are reset only by a power-on reset; they retain the values when a reset caused by another factor occurs.

(**Cautions** and **Remark** are given on the next page.)

Caution 1. The CMC register can be written only once after a reset ends, by an 8-bit memory manipulation instruction. When using the CMC register with its initial value (00H), be sure to set the register to 00H after a reset ends in order to prevent malfunction due to a program loop. A malfunction caused by mistakenly writing a value other than 00H is unrecoverable.

Caution 2. After reset release, set the CMC register before X1 or XT1 oscillation is started as set by the clock operation status control register (CSC).

Caution 3. Be sure to set the AMPH bit to 1 if the X1 clock oscillation frequency exceeds 10 MHz.

Caution 4. Specify the settings for the AMPH, AMPHS1, and AMPHS0 bits while f_{IH} is selected as f_{CLK} after a reset ends (before f_{CLK} is switched to f_{MX}).

Caution 5. Count the f_{XT} oscillation stabilization time by using software.

Caution 6. Although the maximum system clock frequency is 24 MHz, the maximum frequency of the X1 oscillator is 20 MHz.

Caution 7. If a reset other than a power-on reset occurs after the CMC register is written and then the reset ends, be sure to set the CMC register to the value specified before the reset occurred, to prevent a malfunction if a program loop occurs.

Caution 8. The XT1 oscillator is a circuit with low amplification in order to achieve low-power consumption. Note the following points when designing the circuit.

- **Pins and circuit boards include parasitic capacitance. Therefore, perform oscillation evaluation using a circuit board to be actually used and confirm that there are no problems.**
- **Make the wiring between the XT1 and XT2 pins and the resonators as short as possible, and minimize the parasitic capacitance and wiring resistance. Note this particularly when the ultra-low power consumption oscillation (AMPHS1, AMPHS0 = 1, 0) is selected.**
- **Configure the circuit of the circuit board, using material with little parasitic capacitance and wiring resistance.**
- **Place a ground pattern that has the same potential as V_{SS} as much as possible near the XT1 oscillator.**
- **Be sure that the signal lines between the XT1 and XT2 pins, and the resonators do not cross with the other signal lines. Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **The impedance between the XT1 and XT2 pins may drop and oscillation may be disturbed due to moisture absorption of the circuit board in a high-humidity environment or dew condensation on the board. When using the circuit board in such an environment, take measures to damp-proof the circuit board, such as by coating.**
- **When coating the circuit board, use material that does not cause capacitance or leakage between the XT1 and XT2 pins.**

Remark fx: X1 clock frequency

5.3.2 System clock control register (CKC)

This register is used to select a CPU/peripheral hardware clock and a main system clock.

The CKC register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets this register to 00H.

Figure 5 - 4 Format of System clock control register (CKC)

Address: FFFA4H After reset: 00H R/W Note 1

Symbol	<7>	<6>	<5>	<4>	3	2	1	0
CKC	CLS	CSS	MCS	MCM0	0	0	0	0

CLS	Status of CPU/peripheral hardware clock (f_{CLK})
0	Main system clock (f_{MAIN})
1	Subsystem clock (f_{SUB})

CSS	Selection of CPU/peripheral hardware clock (f_{CLK})
0	Main system clock (f_{MAIN})
1 Note 2	Subsystem clock (f_{SUB})

MCS	Status of Main system clock (f_{MAIN})
0	High-speed on-chip oscillator clock (f_{IH})
1	High-speed system clock (f_{MX})

MCM0 Note 2	Main system clock (f_{MAIN}) operation control
0	Selects the high-speed on-chip oscillator clock (f_{IH}) as the main system clock (f_{MAIN})
1	Selects the high-speed system clock (f_{MX}) as the main system clock (f_{MAIN})

Note 1. Bits 7 and 5 are read-only.

Note 2. Changing the value of the MCM0 bit is prohibited while the CSS bit is set to 1.

Caution 1. Be sure to set bits 0 to 3 to 0.

Caution 2. The clock set by the CSS bit is supplied to the CPU and peripheral hardware. If the CPU clock is changed, therefore, the clock supplied to peripheral hardware (except the real-time clock 2, 12-bit interval timer, 8-bit interval timer, clock output/buzzer output, LCD controller/driver, and watchdog timer) is also changed at the same time. Consequently, stop each peripheral function when changing the CPU/peripheral hardware clock.

Caution 3. If the subsystem clock is used as the peripheral hardware clock, the operations of the 10-bit A/D converter and IICA are not guaranteed. For the operating characteristics of the peripheral hardware, refer to the chapters describing the various peripheral hardware as well as CHAPTER 38 or CHAPTER 39 ELECTRICAL SPECIFICATIONS.

Remark f_{IH}: Main system clock source frequency when the high-speed on-chip oscillator clock is selected (24 MHz max.)

f_{MX}: High-speed system clock frequency

f_{MAIN}: Main system clock frequency

f_{SUB}: Subsystem clock frequency

5.3.3 Clock operation status control register (CSC)

This register is used to control the operations of the high-speed system clock, high-speed on-chip oscillator clock, and subsystem clock (except the low-speed on-chip oscillator clock).

The CSC register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets this register to C0H.

Caution The XTSTOP bit is reset only by a power-on reset; it retains the value when a reset caused by another factor occurs.

Figure 5 - 5 Format of Clock operation status control register (CSC)

Address: FFFA1H After reset: C0H R/W

Symbol	<7>	<6>	5	4	3	2	1	<0>
CSC	MSTOP	XTSTOP Note	0	0	0	0	0	HIOSTOP

MSTOP	High-speed system clock operation control		
	X1 oscillation mode	External clock input mode	Input port mode
0	X1 oscillator operating	External clock from EXCLK pin is valid	Input port
1	X1 oscillator stopped	External clock from EXCLK pin is invalid	

XTSTOP Note	Subsystem clock operation control		
	XT1 oscillation mode	External clock input mode	Input port mode
0	XT1 oscillator operating	External clock from EXCLKS pin is valid	Input port
1	XT1 oscillator stopped	External clock from EXCLKS pin is invalid	

HIOSTOP	High-speed on-chip oscillator clock operation control
0	High-speed on-chip oscillator operating
1	High-speed on-chip oscillator stopped

Note The XTSTOP bit is reset only by a power-on reset; it retains the value when a reset caused by another factor occurs.

Caution 1. After reset release, set the clock operation mode control register (CMC) before setting the CSC register.

Caution 2. Set the oscillation stabilization time select register (OSTS) before setting the MSTOP bit to 0 after releasing reset. Note that if the OSTS register is being used with its default settings, the OSTS register is not required to be set here.

Caution 3. To start X1 oscillation as set by the MSTOP bit, check the oscillation stabilization time of the X1 clock by using the oscillation stabilization time counter status register (OSTC).

Caution 4. When starting XT1 oscillation by setting the XSTOP bit, wait for oscillation of the subsystem clock to stabilize by setting a wait time using software.

Caution 5. Do not stop the clock selected for the CPU peripheral hardware clock (f_{CLK}) with the OSC register.

Caution 6. The setting of the flags of the register to stop clock oscillation (invalidate the external clock input) and the condition before clock oscillation is to be stopped are as Table 5 - 2.

Table 5 - 2 Stopping the Clock

Clock	Condition Before Stopping Clock (Invalidating External Clock Input)	Setting of CSC Register Flags
X1 clock External main system clock	CPU and peripheral hardware clocks operate with a clock other than the high-speed system clock. (CLS = 0 and MCS = 0, or CLS = 1)	MSTOP = 1
XT1 clock External subsystem clock	CPU and peripheral hardware clocks operate with a clock other than the subsystem clock. (CLS = 0)	XTSTOP = 1
High-speed on-chip oscillator clock	CPU and peripheral hardware clocks operate with a clock other than the high-speed on-chip oscillator clock. (CLS = 0 and MCS = 1, or CLS = 1)	HIOSTOP = 1

5.3.4 Oscillation stabilization time counter status register (OSTC)

This is the register that indicates the count status of the X1 clock oscillation stabilization time counter.
The X1 clock oscillation stabilization time can be checked in the following case,

- If the X1 clock starts oscillation while the high-speed on-chip oscillator clock or subsystem clock is being used as the CPU clock.
- If the STOP mode is entered and then released while the high-speed on-chip oscillator clock is being used as the CPU clock with the X1 clock oscillating.

The OSTC register can be read by a 1-bit or 8-bit memory manipulation instruction.
The generation of reset signal, the STOP instruction and MSTOP (bit 7 of clock operation status control register (CSC)) = 1 clear the OSTC register to 00H.

Remark The oscillation stabilization time counter starts counting in the following cases.
- When oscillation of the X1 clock starts (EXCLK, OSCSEL = 0, 1 → MSTOP = 0)
- When the STOP mode is released

Figure 5 - 6 Format of Oscillation stabilization time counter status register (OSTC)

Address: FFFA2H After reset: 00H R

Symbol	7	6	5	4	3	2	1	0
OSTC	MOST8	MOST9	MOST 10	MOST 11	MOST 13	MOST 15	MOST 17	MOST 18

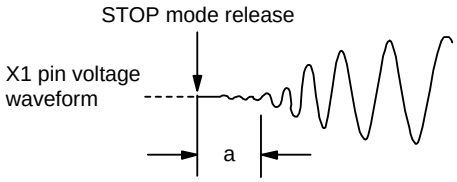
MOST 8	MOST 9	MOST 10	MOST 11	MOST 13	MOST 15	MOST 17	MOST 18	Oscillation stabilization time status		
									fx = 10 MHz	fx = 20 MHz
0	0	0	0	0	0	0	0	2^8/fx max.	25.6 μs max.	12.8 μs max.
1	0	0	0	0	0	0	0	2^8/fx min.	25.6 μs min.	12.8 μs min.
1	1	0	0	0	0	0	0	2^9/fx min.	51.2 μs min.	25.6 μs min.
1	1	1	0	0	0	0	0	2^{10}/fx min.	102 μs min.	51.2 μs min.
1	1	1	1	0	0	0	0	2^{11}/fx min.	204 μs min.	102 μs min.
1	1	1	1	1	0	0	0	2^{13}/fx min.	819 μs min.	409 μs min.
1	1	1	1	1	1	0	0	2^{15}/fx min.	3.27 ms min.	1.63 ms min.
1	1	1	1	1	1	1	0	2^{17}/fx min.	13.1 ms min.	6.55 ms min.
1	1	1	1	1	1	1	1	2^{18}/fx min.	26.2 ms min.	13.1 ms min.

Caution 1. After the above time has elapsed, the bits are set to 1 in order from the MOST8 bit and remain 1.

Caution 2. The oscillation stabilization time counter counts up to the oscillation stabilization time set by the oscillation stabilization time select register (OSTS).
In the following cases, set the oscillation stabilization time of the OSTS register to a value greater than the count value to be monitored by using the OSTC register after the oscillation starts.

- **If the X1 clock starts oscillation while the high-speed on-chip oscillator clock or subsystem clock is being used as the CPU clock.**
- **If the STOP mode is entered and then released while the high-speed on-chip oscillator clock is being used as the CPU clock with the X1 clock oscillating.**
  (Note, therefore, that only the status up to the oscillation stabilization time set by the OSTS register is set to the OSTC register after the STOP mode is released.)

Caution 3. The X1 clock oscillation stabilization wait time does not include the time until clock oscillation starts ("a" below).



Remark fx: X1 clock oscillation frequency

5.3.5 Oscillation stabilization time select register (OSTS)

This register is used to select the X1 clock oscillation stabilization wait time.

When the X1 clock is made to oscillate by clearing the MSTOP bit to start the X1 oscillation circuit operating, actual operation is automatically delayed for the time set in the OSTS register.

When switching the CPU clock from the high-speed on-chip oscillator clock or the subsystem clock to the X1 clock, and when using the high-speed on-chip oscillator clock for switching the X1 clock from the oscillating state to STOP mode, use the oscillation stabilization time counter status register (OSTC) to confirm that the desired oscillation stabilization time has elapsed after release from the STOP mode. The oscillation stabilization time can be checked up to the time set using the OSTC register.

The OSTS register can be set by an 8-bit memory manipulation instruction.

Reset signal generation sets the OSTS register to 07H.

Figure 5 - 7 Format of Oscillation stabilization time select register (OSTS)

Address: FFFA3H After reset: 07H R/W

Symbol	7	6	5	4	3	2	1	0
OSTS	0	0	0	0	0	OSTS2	OSTS1	OSTS0

OSTS2	OSTS1	OSTS0	Oscillation stabilization time selection		
				fx = 10 MHz	fx = 20 MHz
0	0	0	2^8/fx	25.6 μs	12.8 μs
0	0	1	2^9/fx	51.2 μs	25.6 μs
0	1	0	2^{10}/fx	102 μs	51 μs
0	1	1	2^{11}/fx	204 μs	102 μs
1	0	0	2^{13}/fx	819 μs	409 μs
1	0	1	2^{15}/fx	3.27 ms	1.63 ms
1	1	0	2^{17}/fx	13.1 ms	6.55 ms
1	1	1	2^{18}/fx	26.2 ms	13.1 ms

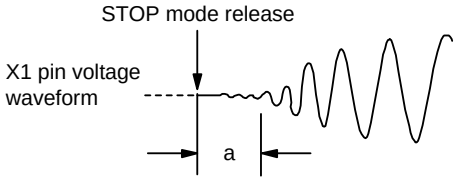
Caution 1. Change the setting of the OSTS register before setting the MSTOP bit of the clock operation status control register (CSC) to 0.

Caution 2. The oscillation stabilization time counter counts up to the oscillation stabilization time set by the OSTS register.

In the following cases, set the oscillation stabilization time of the OSTS register to the value greater than the count value which is to be checked by the OSTC register after the oscillation starts.

- **If the X1 clock starts oscillation while the high-speed on-chip oscillator clock or subsystem clock is being used as the CPU clock.**
- **If the STOP mode is entered and then released while the high-speed on-chip oscillator clock is being used as the CPU clock with the X1 clock oscillating. (Note, therefore, that only the status up to the oscillation stabilization time set by the OSTS register is set to the OSTC register after the STOP mode is released.)**

Caution 3. The X1 clock oscillation stabilization wait time does not include the time until clock oscillation starts ("a" below).



Remark fx: X1 clock oscillation frequency

5.3.6 Peripheral enable registers 0, 1, 2 (PER0, PER1, PER2)

These registers are used to enable or disable supplying the clock to the peripheral hardware. Clock supply to the hardware that is not used is also stopped so as to decrease the power consumption and noise.
To use the peripheral functions below, which are controlled by these registers, set (1) the bit corresponding to each function before specifying the initial settings of the peripheral functions.
The PER2 register is only provided in the R5F11R.

- Real-time clock 2
- 10-bit A/D converter
- Serial interface IICA0
- Serial array unit 1
- Serial array unit 0
- Timer array unit
- 12-bit interval timer
- D/A converter Note 1
- Amplifier unit Note 1
- Data transfer controller
- PGA0 and 24-bit ΔΣ A/D converter Note 1
- Clock control block in the AFE power supply Note 1
- Serial interface UARTMG0 Note 2
- Sampling output timer detector Note 2
- External signal sampler Note 2
- Timers RJ0 and RJ1 Note 2

The PER0, PER1, and PER2 registers can be set by a 1-bit or 8-bit memory manipulation instruction.
Reset signal generation clears these registers to 00H.

Note 1. R5F11N and R5F11P only.
Note 2. R5F11R only.

Figure 5 - 8 Format of Peripheral enable register 0 (PER0) (1/2)

Address: F00F0H After reset: 00H R/W

Symbol	<7>	6	<5>	<4>	<3>	<2>	1	<0>
PER0	RTCWEN	0	ADCEN	IICA0EN	SAU1EN	SAU0EN	0	TAU0EN

RTCWEN	Control of real-time clock 2 (RTC2) input clock supply
0	Stops input clock supply (stops f_{CLK} supply). • SFRs used by the real-time clock 2 (RTC2) cannot be written. • The real-time clock 2 (RTC2) is operable.
1	Enables input clock supply. • SFRs used by the real-time clock 2 (RTC2) can be read and written. • The real-time clock 2 (RTC2) is operable.

ADCEN	Control of 10-bit A/D converter input clock supply
0	Stops input clock supply. • SFRs used by the 10-bit A/D converter cannot be written. • The 10-bit A/D converter is in the reset status.
1	Enables input clock supply. • SFRs used by the 10-bit A/D converter can be read and written.

Caution Be sure to clear bits 1 and 6 to 0.

Figure 5 - 8 Format of Peripheral enable register 0 (PER0) (2/2)

Address: F00F0H After reset: 00H R/W

Symbol	<7>	6	<5>	<4>	<3>	<2>	1	<0>
PER0	RTCWEN	0	ADCEN	IICA0EN	SAU1EN	SAU0EN	0	TAU0EN

IICA0EN	Control of serial interface IICA0 input clock supply
0	Stops input clock supply. • SFRs used by the serial interface IICA0 cannot be written. • The serial interface IICA0 is in the reset status.
1	Enables input clock supply. • SFRs used by the serial interface IICA0 can be read and written.

SAU1EN	Control of serial array unit 1 input clock supply
0	Stops input clock supply. • SFRs used by serial array unit 1 cannot be written. • Serial array unit 1 is in the reset status.
1	Enables input clock supply. • SFRs used by serial array unit 1 can be read and written.

SAU0EN	Control of serial array unit 0 input clock supply
0	Stops input clock supply. • SFRs used by serial array unit 0 cannot be written. • Serial array unit 0 is in the reset status.
1	Enables input clock supply. • SFRs used by serial array unit 0 can be read and written.

TAU0EN	Control of timer array unit input clock supply
0	Stops input clock supply. • SFRs used by the timer array unit cannot be written. • The timer array unit is in the reset status.
1	Enables input clock supply. • SFRs used by the timer array unit can be read and written.

Caution Be sure to clear bits 1 and 6 to 0.

Figure 5 - 9 Format of Peripheral enable register 1 (PER1)

Address: F007AH After reset: 00H R/W

Symbol	<7>	6	5	<4>	<3>	<2>	<1>	<0>
PER1	TMKAEN	0	0	AMPEN Note	DTCEN	PGAEN Note	AFEEN Note	DACEN Note

TMKAEN	Control of 12-bit interval timer input clock supply
0	Stops input clock supply. • SFRs used by the 12-bit interval timer cannot be written. • The 12-bit interval timer is in the reset status.
1	Enables input clock supply. • SFRs used by the 12-bit interval timer can be read and written.

AMPEN Note	Control of amplifier unit input clock supply
0	Stops input clock supply. • SFRs used by the amplifier unit cannot be written. • The amplifier unit is in the reset status.
1	Enables input clock supply. • SFRs used by the amplifier unit can be read and written.

DTCEN	Control of DTC input clock supply
0	Stops input clock supply. • DTC cannot run.
1	Enables input clock supply. • DTC can run.

PGAEN Note	Control of input clock supply to PGA0 and 24-bit ΔΣ A/D converter
0	Stops input clock supply. • SFRs used by the PGA0 and 24-bit ΔΣ A/D converter cannot be written. • The PGA0 and 24-bit ΔΣ A/D converter are in the reset status.
1	Enables input clock supply. • SFRs used by the PGA0 and 24-bit ΔΣ A/D converter can be read and written.

AFEEN Note	Control of input clock supply to clock control block in AFE power supply
0	Stops input clock supply. • SFRs used by the clock control block in the AFE power supply cannot be written. • The clock control block in the AFE power supply is in the reset status.
1	Enables input clock supply. • SFRs used by the clock control block in the AFE power supply can be read and written.

DACEN Note	Control of D/A converter input clock supply
0	Stops input clock supply. • SFRs used by the D/A converter cannot be written. • The D/A converter is in the reset status.
1	Enables input clock supply. • SFRs used by the D/A converter can be read and written.

Note R5F11N and R5F11P only.

Caution Be sure to set the following bits to 0.
R5F11N, R5F11P: bits 5 and 6
R5F11R: bits 0 to 2, 4 to 6

Figure 5 - 10 Format of Peripheral enable register 2 (PER2)

Address: F007AH After reset: 00H R/W

Symbol	7	6	5	<4>	<3>	<2>	<1>	<0>
PER2 Note	0	0	0	UARTMG0EN	SMOTDEN	EXSDEN	TRJ1EN	TRJ0EN

UARTMG0EN	Control of serial interface UARTMG0 input clock supply
0	Stops input clock supply. • SFRs used by the serial interface UARTMG0 cannot be written. • The serial interface UARTMG0 is in the reset status.
1	Enables input clock supply. • SFRs used by the serial interface UARTMG0 can be read and written.

SMOTDEN	Control of sampling output timer detector input clock supply
0	Stops input clock supply. • SFRs used by the sampling output timer detector cannot be written. • The sampling output timer detector is in the reset status.
1	Enables input clock supply. • SFRs used by the sampling output timer detector can be read and written.

EXSDEN	Control of external signal sampler input clock supply
0	Stops input clock supply. • SFRs used by the external signal sampler cannot be written. • The external signal sampler is in the reset status.
1	Enables input clock supply. • SFRs used by the external signal sampler can be read and written.

TRJ1EN	Control of timer RJ1 input clock supply
0	Stops input clock supply. • SFRs used by the timer RJ1 cannot be written. • The timer RJ1 is in the reset status.
1	Enables input clock supply. • SFRs used by the timer RJ1 can be read and written.

TRJ0EN	Control of timer RJ0 input clock supply
0	Stops input clock supply. • SFRs used by the timer RJ0 cannot be written. • The timer RJ0 is in the reset status.
1	Enables input clock supply. • SFRs used by the timer RJ0 can be read and written.

Note R5F11R only.

Caution Be sure to set the bits 5 to 7 to 0.

5.3.7 Subsystem clock supply mode control register (OSMC)

This register is used to reduce power consumption by stopping unnecessary clock functions.

If the RTCLPC bit is set to 1, power consumption can be reduced, because clock supply to the peripheral functions other than the real-time clock 2, 12-bit interval timer, 8-bit interval timer, clock output/buzzer output controller, LCD controller/driver, serial interface UARTMG0, external signal sampler, and sampling output timer detector is stopped in STOP mode or in HALT mode while the subsystem clock is selected as the CPU clock.

The OSMC register can be used to select the count clock of the real-time clock 2, 12-bit interval timer, and 8-bit interval timer, and the operating clock of the clock output/buzzer output, LCD controller/driver, serial interface UARTMG0, external signal sampler, sampling output timer detector, and timers RJ0 and RJ1.

The low-speed on-chip oscillator clock cannot be selected as the operation clock for the serial interface UARTMG0, external signal sampler, and sampling output timer detector. When using the serial interface UARTMG0, external signal sampler, and sampling output timer detector, select the subsystem clock as the operation clock by setting the WUTMMCK0 to 0.

The OSMC register can be set by an 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 5 - 11 Format of Subsystem clock supply mode control register (OSMC)

Address: F00F3H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
OSMC	RTCLPC	0	0	WUTMMCK0	0	0	0	0

RTCLPC	Setting in STOP mode or in HALT mode while subsystem clock is selected as CPU clock
0	Enables supplying the subsystem clock to peripheral functions (See **Tables 27 - 1** and **27 - 2** for peripheral functions whose operations are enabled.)
1	Stops supplying the subsystem clock to peripheral functions other than the real-time clock 2, 12-bit interval timer, 8-bit interval timer, clock output/buzzer output controller, LCD controller/driver, serial interface UARTMG0, external signal sampler, and sampling output timer detector.

WUTMMCK0 Note	Selection of operation clock for real-time clock 2, 12-bit interval timer, 8-bit interval timer, LCD controller/driver, and timers RJ0 and RJ1	Selection of clock output from PCLBUZn pin of clock output/buzzer output controller
0	Subsystem clock (f_{SUB}) • The subsystem clock is selected as the operation clock for the real-time clock 2, 12-bit interval timer, 8-bit interval timer, and LCD controller/driver. • The low-speed on-chip oscillator cannot be selected as the count source for timers RJ0 and RJ1.	Selecting the subsystem clock (f_{SUB}) is enabled.
1	Low-speed on-chip oscillator clock (f_{IL}) • The low-speed on-chip oscillator clock is selected as the operation clock for the real-time clock 2, 12-bit interval timer, 8-bit interval timer, and LCD controller/driver. • The low-speed on-chip oscillator or subsystem clock can be selected as the count source for timers RJ0 an RJ1.	Selecting the subsystem clock (f_{SUB}) is disabled.

Note Be sure to select the subsystem clock (WUTMMCK0 bit = 0) while the subsystem clock is oscillating.

Caution 1. The subsystem clock and low-speed on-chip oscillator clock can only be switched by using the WUTMMCK0 bit if the real-time clock 2, 12-bit interval timer, 8-bit interval timer, and LCD controller/driver are all stopped.

Caution 2. Do not select f_{SUB} as the clock output or buzzer output clock when the WUTMMCK0 bit is 1.

5.3.8 High-speed on-chip oscillator frequency select register (HOCODIV)

The frequency of the high-speed on-chip oscillator which is set by an option byte (000C2H) can be changed by using high-speed on-chip oscillator frequency select register (HOCODIV). However, the selectable frequency depends on the FRQSEL3 bit of the option byte (000C2H).

The HOCODIV register can be set by an 8-bit memory manipulation instruction.

Reset signal generation clears this register to the value set by FRQSEL2 to FRQSEL0 of the option byte (000C2H).

Figure 5 - 12 Format of High-speed on-chip oscillator frequency select register (HOCODIV)

Address: F00A8H After reset: The value set by FRQSEL2 to FRQSEL0 of the option byte (000C2H) R/W

Symbol	7	6	5	4	3	2	1	0
HOCODIV	0	0	0	0	0	HOCODIV2	HOCODIV1	HOCODIV0

HOCODIV2	HOCODIV1	HOCODIV0	Selection of high-speed on-chip oscillator clock frequency	
			FRQSEL3 = 0	FRQSEL3 = 1
0	0	0	f_{IH} = 24 MHz	Setting prohibited
0	0	1	f_{IH} = 12 MHz	f_{IH} = 16 MHz
0	1	0	f_{IH} = 6 MHz	f_{IH} = 8 MHz
0	1	1	f_{IH} = 3 MHz	f_{IH} = 4 MHz
1	0	0	Setting prohibited	f_{IH} = 2 MHz
1	0	1	Setting prohibited	f_{IH} = 1 MHz
Other than above			Setting prohibited	

Caution Set the HOCODIV register within the operable voltage range of the flash operation mode set in the option byte (000C2H) before and after the frequency change.

Option Byte (000C2H) Value		Flash Operation Mode	Operating Frequency Range	Operating Voltage Range
CMODE1	CMODE0			
1	0	LS (low-speed main) mode Note	1 to 8 MHz	1.8 to 5.5 V
1	1	HS (high-speed main) mode	1 to 16 MHz	2.4 to 5.5 V
			1 to 24 MHz	2.7 to 5.5 V

Note R5F11R only.

Caution 1. Set the HOCODIV register with the high-speed on-chip oscillator clock (f_{IH}) selected as the CPU/peripheral hardware clock (f_{CLK}).

Caution 2. After the frequency is changed with the HOCODIV register, the frequency is switched after the following transition time has elapsed.

- **Operation for up to three clocks at the pre-change frequency**
- **CPU/peripheral hardware clock wait at the post-change frequency for up to three clocks**

Caution 3. To change the frequency of the high-speed on-chip oscillator when X1 oscillation, external oscillation input or sub clock is set for the system clock, stop the high-speed on-chip oscillator by setting bit 0 (HIOSTOP) of the CSC register to 1 and then change the frequency.

5.3.9 High-speed on-chip oscillator trimming register (HIOTRM)

This register is used to adjust the accuracy of the high-speed on-chip oscillator.

With self-measurement of the high-speed on-chip oscillator frequency via a timer using high-accuracy external clock input, and so on, the accuracy can be adjusted.

The HIOTRM register can be set by an 8-bit memory manipulation instruction.

Caution The frequency will vary if the temperature and V_{DD} pin voltage change after accuracy adjustment. When the temperature and V_{DD} voltage change, accuracy adjustment must be executed regularly or before the frequency accuracy is required.

Figure 5 - 13 Format of High-speed on-chip oscillator trimming register (HIOTRM)

Address: F00A0H After reset: Note R/W

Symbol	7	6	5	4	3	2	1	0
HIOTRM	0	0	HIOTRM5	HIOTRM4	HIOTRM3	HIOTRM2	HIOTRM1	HIOTRM0

HIOTRM5	HIOTRM4	HIOTRM3	HIOTRM2	HIOTRM1	HIOTRM0	High-speed on-chip oscillator
0	0	0	0	0	0	Minimum speed
0	0	0	0	0	1	
0	0	0	0	1	0	
0	0	0	0	1	1	
0	0	0	1	0	0	
• • •						
1	1	1	1	1	0	
1	1	1	1	1	1	Maximum speed

Note The value after reset is the value adjusted at shipment.

Remark 1. The HIOTRM register can be used to adjust the high-speed on-chip oscillator clock to an accuracy within about 0.05%.

Remark 2. For the usage example of the HIOTRM register, see the application note for RL78 MCU Series High-speed On-chip Oscillator (HOCO) Clock Frequency Correction (R01AN0464).

5.4 System Clock Oscillator

5.4.1 X1 oscillator

The X1 oscillator oscillates with a crystal resonator or ceramic resonator (1 to 20 MHz) connected to the X1 and X2 pins.

An external clock can also be input. In this case, input the clock signal to the EXCLK pin.

To use the X1 oscillator, set bits 7 and 6 (EXCLK, OSCSEL) of the clock operation mode control register (CMC) as follows.

- Crystal or ceramic oscillation: EXCLK, OSCSEL = 0, 1
- External clock input: EXCLK, OSCSEL = 1, 1

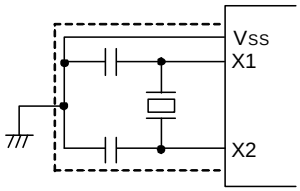
When the X1 oscillator is not used, set the input port mode (EXCLK, OSCSEL = 0, 0).

When the pins are not used as input port pins, either, see **Table 2 - 3 Connection of Unused Pins**.

Figure 5 - 14 shows an example of the external circuit of the X1 oscillator.

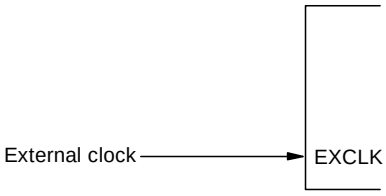
Figure 5 - 14 Example of External Circuit of X1 Oscillator

(a) Crystal or ceramic oscillation



Crystal resonator
or
ceramic resonator

(b) External clock



(**Cautions** are listed on the next page.)

5.4.2 XT1 oscillator

The XT1 oscillator oscillates with a crystal resonator (standard: 32.768 kHz or 38.4 kHz[Note]) connected to the XT1 and XT2 pins.

To use the XT1 oscillator, set bit 4 (OSCSELS) of the clock operation mode control register (CMC) to 1.

An external clock can also be input. In this case, input the clock signal to the EXCLKS pin.

To use the XT1 oscillator, set bits 5 and 4 (EXCLKS, OSCSELS) of the clock operation mode control register (CMC) as follows.

- Crystal oscillation: EXCLKS, OSCSELS = 0, 1
- External clock input: EXCLKS, OSCSELS = 1, 1

When the XT1 oscillator is not used, set the input port mode (EXCLKS, OSCSELS = 0, 0).

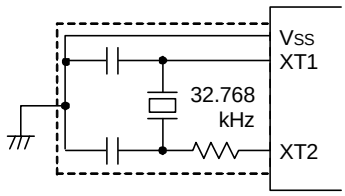
When the pins are not used as input port pins, either, see **Table 2 - 3 Connection of Unused Pins**.

Figure 5 - 15 shows an example of the external circuit of the XT1 oscillator.

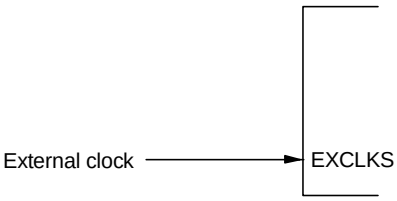
Note R5F11R only.

Figure 5 - 15 Example of External Circuit of XT1 Oscillator

(a) Crystal oscillation



(b) External clock



Caution When using the X1 oscillator and XT1 oscillator, wire as follows in the area enclosed by the broken lines in the Figures 5 - 14 and 5 - 15 to avoid an adverse effect from wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines. Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as Vss. Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

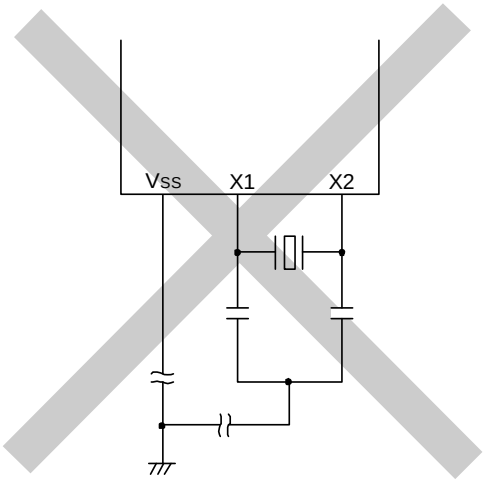
The XT1 oscillator is a circuit with low amplification in order to achieve low-power consumption. Note the following points when designing the circuit.

- **Pins and circuit boards include parasitic capacitance. Therefore, perform oscillation evaluation using a circuit board to be actually used and confirm that there are no problems.**
- **Make the wiring between the XT1 and XT2 pins and the resonators as short as possible, and minimize the parasitic capacitance and wiring resistance. Note this particularly when the ultra-low power consumption oscillation (AMPHS1, AMPHS0 = 1, 0) is selected.**
- **Configure the circuit of the circuit board, using material with little wiring resistance.**
- **Place a ground pattern that has the same potential as Vss as much as possible near the XT1 oscillator.**
- **Be sure that the signal lines between the XT1 and XT2 pins, and the resonators do not cross with the other signal lines. Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **The impedance between the XT1 and XT2 pins may drop and oscillation may be disturbed due to moisture absorption of the circuit board in a high-humidity environment or dew condensation on the board. When using the circuit board in such an environment, take measures to damp-proof the circuit board, such as by coating.**
- **When coating the circuit board, use material that does not cause capacitance or leakage between the XT1 and XT2 pins.**

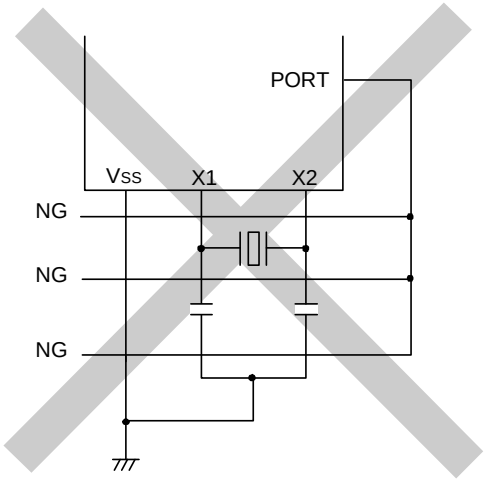
Figure 5 - 16 shows examples of incorrect resonator connection.

Figure 5 - 16 Examples of Incorrect Resonator Connection (1/2)

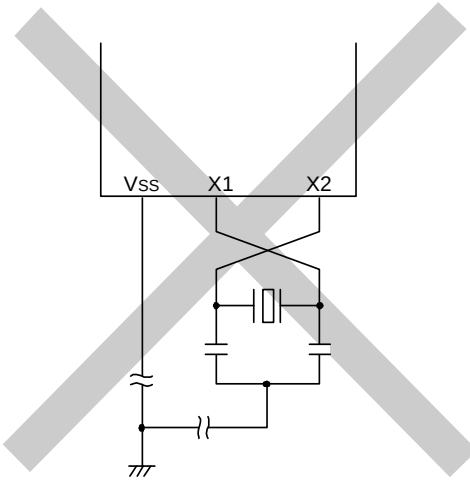
(a) Too long wiring



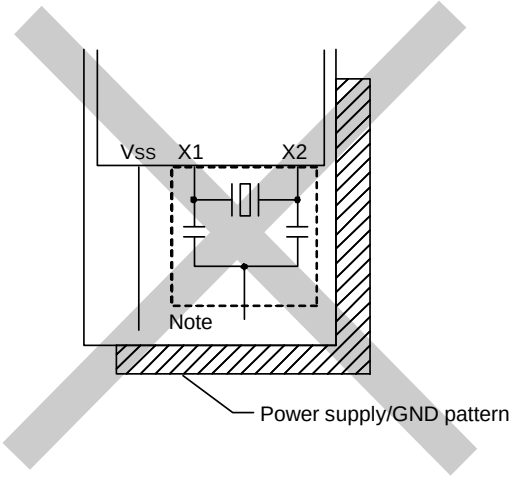
(b) Crossed signal line



(c) The X1 and X2 signal line wires cross.



(d) A power supply/GND pattern exists under the X1 and X2 wires.

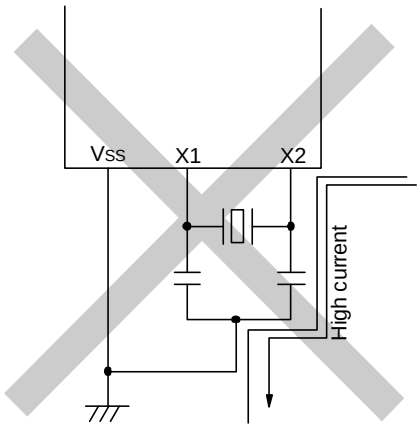


Note Do not place a power supply/GND pattern under the wiring section (section indicated by a broken line in the figure) of the X1 and X2 pins and the resonators in a multi-layer board or double-sided board.
Do not configure a layout that will cause capacitance elements and affect the oscillation characteristics.

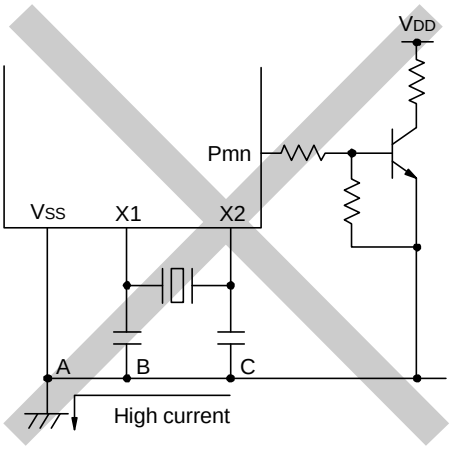
Remark When using the subsystem clock, replace X1 and X2 with XT1 and XT2, respectively. Also, insert resistors in series on the XT2 side.

Figure 5 - 16 Examples of Incorrect Resonator Connection (2/2)

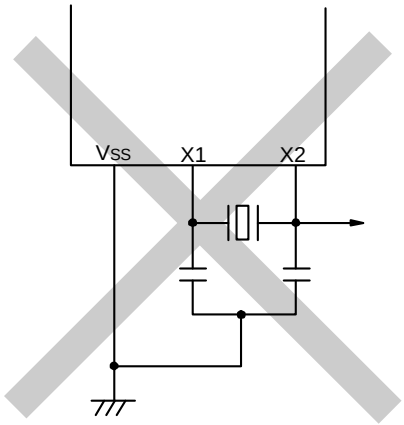
(e) Wiring near high alternating current



(f) Current flowing through ground line of oscillator
(potential at points A, B, and C fluctuates)



(g) Signals are fetched



Caution **When X2 and XT1 are wired in parallel, the crosstalk noise of X2 may increase with XT1, resulting in malfunctioning.**

Remark When using the subsystem clock, replace X1 and X2 with XT1 and XT2, respectively. Also, insert resistors in series on the XT2 side.

5.4.3 High-speed on-chip oscillator

The high-speed on-chip oscillator is incorporated in the RL78/H1D. The frequency can be selected from among 24, 16, 12, 8, 6, 4, 3, 2, or 1 MHz by using the option byte (000C2H). Oscillation can be controlled by bit 0 (HIOSTOP) of the clock operation status control register (CSC).

The high-speed on-chip oscillator automatically starts oscillating after reset release.

5.4.4 Low-speed on-chip oscillator

The low-speed on-chip oscillator is incorporated in the RL78/H1D.

The low-speed on-chip oscillator clock is used only as the clock for the watchdog timer, real-time clock 2, 12-bit interval timer, 8-bit interval timer, LCD controller/driver, and timers RJ0 and RJ1 Note. The low-speed on-chip oscillator clock cannot be used as the CPU clock.

The low-speed on-chip oscillator runs while the watchdog timer is operating or when the setting of bit 4 (WUTMMCK0) in the subsystem clock supply mode control register (OSMC) is 1.

The low-speed on-chip oscillator is stopped when the watchdog timer is stopped and WUTMMCK0 is set to 0.

Note R5F11R only.

5.5 Clock Generator Operation

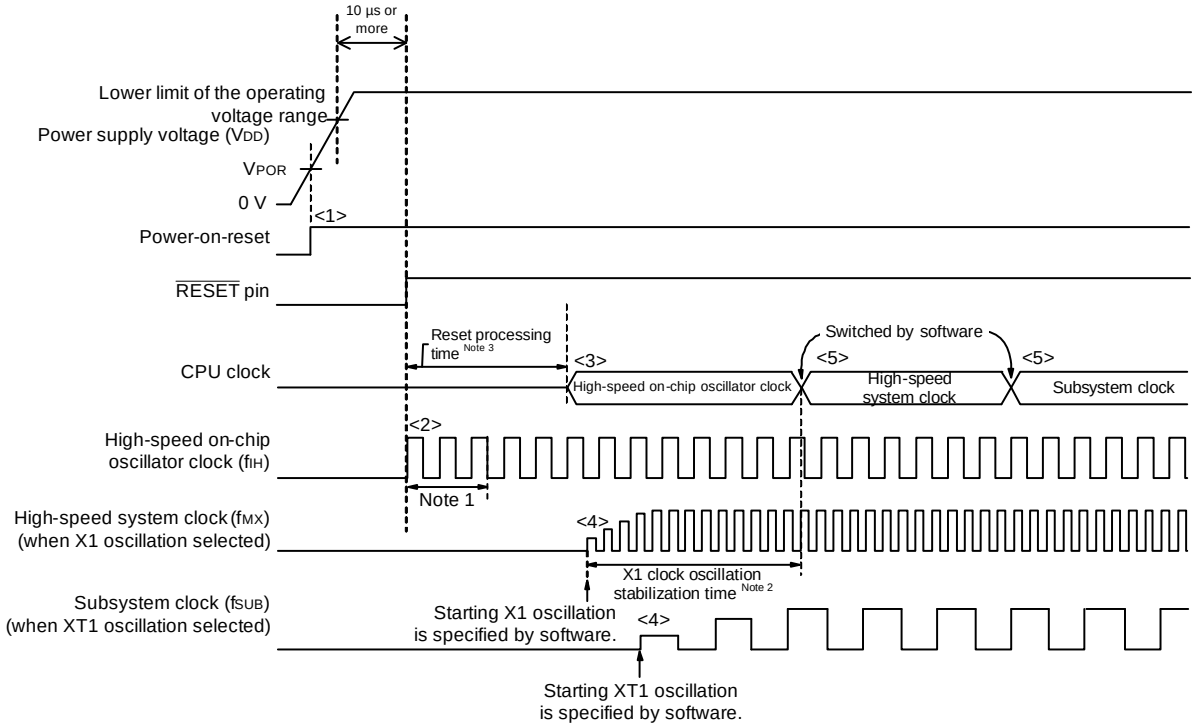
The clock generator generates the following clocks and controls the operation modes of the CPU, such as standby mode (see **Figure 5 - 1** or **Figure 5 - 2**).

- Main system clock f_{MAIN}
  - High-speed system clock f_{MX}
    X1 clock f_X
    External main system clock f_{EX}
  - High-speed on-chip oscillator clock f_{IH}

- Subsystem clock f_{SUB}
  - XT1 clock f_{XT}
  - External subsystem clock f_{EXT}
- Low-speed on-chip oscillator clock f_{IL}
- CPU/peripheral hardware clock f_{CLK}

The CPU starts operation when the high-speed on-chip oscillator starts outputting after a reset release in the RL78/H1D.
When the power supply voltage is turned on, the clock generator operation is shown in Figure 5 - 17.

Figure 5 - 17 Clock Generator Operation When Power Supply Voltage Is Turned On



<1> When the power is turned on, an internal reset signal is generated by the power-on-reset (POR) circuit.
Note that the reset state is maintained after a reset by the voltage detection circuit or an external reset until the voltage reaches the range of operating voltage described in **38.4** or **39.4 AC Characteristics** (the above figure is an example when the external reset is in use).

<2> When the reset is released, the high-speed on-chip oscillator automatically starts oscillation.

<3> The CPU starts operation on the high-speed on-chip oscillator clock after waiting for the voltage to stabilize and a reset processing have been performed after reset release.

<4> Set the start of oscillation of the X1 or XT1 clock via software (see **5.6.2 Example of setting X1 oscillation clock** and **5.6.3 Example of setting XT1 oscillation clock**).

<5> When switching the CPU clock to the X1 or XT1 clock, wait for the clock oscillation to stabilize, and then set switching via software (see **5.6.2 Example of setting X1 oscillation clock** and **5.6.3 Example of setting XT1 oscillation clock**).

Note 1. The reset processing time includes the oscillation accuracy stabilization time of the high-speed on-chip oscillator clock.

Note 2. When releasing a reset, confirm the oscillation stabilization time for the X1 clock using the oscillation stabilization time counter status register (OSTC).

Note 3. For details on the reset processing time, refer to **CHAPTER 29 POWER-ON-RESET CIRCUIT**.

Caution It is not necessary to wait for the oscillation stabilization time when an external clock input from the EXCLK pin is used.

5.6 Controlling Clock

5.6.1 Example of setting high-speed on-chip oscillator

After a reset release, the CPU/peripheral hardware clock (f_{CLK}) always starts operating with the high-speed on-chip oscillator clock. The frequency of the high-speed on-chip oscillator can be selected from 24, 16, 12, 8, 6, 4, 3, 2, and 1 MHz by using FRQSEL0 to FRQSEL3 of the option byte (000C2H). In addition, oscillation can be changed by the high-speed on-chip oscillator frequency select register (HOCODIV).

[Option byte setting]

Address: 000C2H

Option byte (000C2H)

7	6	5	4	3	2	1	0
CMODE1 1	CMODE0 0/1	1	0	FRQSEL3 0/1	FRQSEL2 0/1	FRQSEL1 0/1	FRQSEL0 0/1

CMODE1	CMODE0	Setting of flash operation mode	
1	0	LS (low speed main) mode Note	V_{DD} = 1.8 V to 5.5 V @ 1 MHz to 8 MHz
1	1	HS (high speed main) mode	V_{DD} = 2.4 V to 5.5 V @ 1 MHz to 16 MHz V_{DD} = 2.7 V to 5.5 V @ 1 MHz to 24 MHz
Other than above		Setting prohibited	

Note R5F11R only.

FRQSEL3	FRQSEL2	FRQSEL1	FRQSEL0	Frequency of the high-speed on-chip oscillator (f_{IH})
0	0	0	0	24 MHz
1	0	0	1	16 MHz
0	0	0	1	12 MHz
1	0	1	0	8 MHz
0	0	1	0	6 MHz
1	0	1	1	4 MHz
0	0	1	1	3 MHz
1	1	0	0	2 MHz
1	1	0	1	1 MHz
Other than above				Setting prohibited

[High-speed on-chip oscillator frequency select register (HOCODIV) setting]

Address: F00A8H

Symbol	7	6	5	4	3	2	1	0
HOCODIV	0	0	0	0	0	HOCODIV2	HOCODIV1	HOCODIV0

HOCODIV2	HOCODIV1	HOCODIV0	Selection of high-speed on-chip oscillator clock frequency	
			FRQSEL3 = 0	FRQSEL3 = 1
0	0	0	f_{IH} = 24 MHz	Setting prohibited
0	0	1	f_{IH} = 12 MHz	f_{IH} = 16 MHz
0	1	0	f_{IH} = 6 MHz	f_{IH} = 8 MHz
0	1	1	f_{IH} = 3 MHz	f_{IH} = 4 MHz
1	0	0	Setting prohibited	f_{IH} = 2 MHz
1	0	1	Setting prohibited	f_{IH} = 1 MHz
Other than above			Setting prohibited	

5.6.2 Example of setting X1 oscillation clock

After a reset release, the CPU/peripheral hardware clock (f_{CLK}) always starts operating with the high-speed on-chip oscillator clock. To subsequently change the clock to the X1 oscillation clock, set the oscillator and start oscillation by using the oscillation stabilization time select register (OSTS), clock operation mode control register (CMC), and clock operation status control register (CSC) and wait for oscillation to stabilize by using the oscillation stabilization time counter status register (OSTC). After the oscillation stabilizes, set the X1 oscillation clock to f_{CLK} by using the system clock control register (CKC).

[Register settings] Set the register in the order of <1> to <5> below.

<1> Set (1) the OSCSEL bit of the CMC register, except for the cases where the fx is equal to or more than 10 MHz, in such cases set (1) the AMPH bit, to operate the X1 oscillator.

	7	6	5	4	3	2	1	0
CMC	EXCLK 0	OSCSEL 1	EXCLKS 0	OSCSELS 0	 0	AMPHS1 0	AMPHS0 0	AMPH 0/1

AMPH bit: Set this bit to 0 if the X1 oscillation clock is 10 MHz or less.

<2> Using the OSTS register, select the oscillation stabilization time of the X1 oscillator at releasing of the STOP mode.

Example: Setting values when a wait of at least 102 µs is set based on a 10 MHz resonator.

	7	6	5	4	3	2	1	0
OSTS	 0	 0	 0	 0	 0	OSTS2 0	OSTS1 1	OSTS0 0

<3> Clear (0) the MSTOP bit of the CSC register to start oscillating the X1 oscillator.

	7	6	5	4	3	2	1	0
CSC	MSTOP 0	XTSTOP 1	 0	 0	 0	 0	 0	HIOSTOP 0

<4> Use the OSTC register to wait for oscillation of the X1 oscillator to stabilize.

Example: Wait until the bits reach the following values when a wait of at least 102 µs is set based on a 10 MHz resonator.

	7	6	5	4	3	2	1	0
OSTC	MOST8 1	MOST9 1	MOST10 1	MOST11 0	MOST13 0	MOST15 0	MOST17 0	MOST18 0

<5> Use the MCM0 bit of the CKC register to specify the X1 oscillation clock as the CPU/peripheral hardware clock.

	7	6	5	4	3	2	1	0
CKC	CLS 0	CSS 0	MCS 0	MCM0 1	 0	 0	 0	 0

Caution The EXCLKS, OSCSELS, AMPHS1, AMPHS0, and XTSTOP bits are reset only by a power on reset; they retain the previous values when a reset caused by another factor occurs.

5.6.3 Example of setting XT1 oscillation clock

After a reset release, the CPU/peripheral hardware clock (f_{CLK}) always starts operating with the high-speed on-chip oscillator clock. To subsequently change the clock to the XT1 oscillation clock, set the oscillator and start oscillation by using the subsystem clock supply mode control register (OSMC), clock operation mode control register (CMC), and clock operation status control register (CSC), set the XT1 oscillation clock to f_{CLK} by using the system clock control register (CKC).

[Register settings] Set the register in the order of <1> to <5> below.

<1> Set the RTCLPC bit to 1 to run only the real-time clock 2, 12-bit interval timer, 8-bit interval timer, LCD controller/driver, serial interface UARTMG0 Note, external signal sampler Note , and sampling output timer detector Note on the subsystem clock (for ultra-low current consumption) in the STOP mode or sub-HALT mode.

	7	6	5	4	3	2	1	0
OSMC	RTCLPC			WUTMMCK0				
	0/1	0	0	0	0	0	0	0

Note R5F11R only.

<2> Set (1) the OSCSELS bit of the CMC register to operate the XT1 oscillator.

	7	6	5	4	3	2	1	0
CMC	EXCLK	OSCSEL	EXCLKS	OSCSELS		AMPHS1	AMPHS0	AMPH
	0	0	0	1	0	0/1	0/1	0

AMPHS0 and AMPHS1 bits: These bits are used to specify the oscillation mode of the XT1 oscillator.

<3> Clear (0) the XTSTOP bit of the CSC register to start oscillating the XT1 oscillator.

	7	6	5	4	3	2	1	0
CSC	MSTOP	XTSTOP						HIOSTOP
	1	0	0	0	0	0	0	0

<4> Use the timer function or another function to wait for oscillation of the subsystem clock to stabilize by using software.

<5> Use the CSS bit of the CKC register to specify the XT1 oscillation clock as the CPU/peripheral hardware clock.

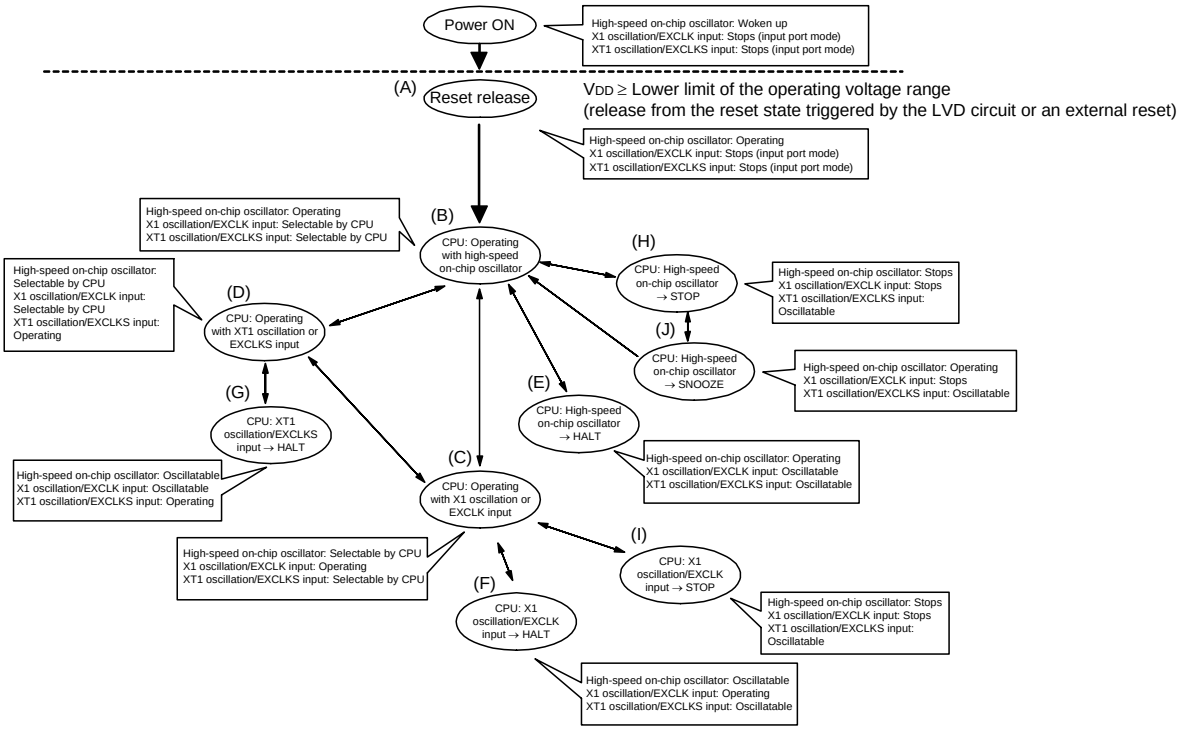
	7	6	5	4	3	2	1	0
CKC	CLS	CSS	MCS	MCM0				
	0	1	0	0	0	0	0	0

Caution The EXCLKS, OSCSELS, AMPHS1, AMPHS0, and XTSTOP bits are reset only by a power on reset; they retain the previous values when a reset caused by another factor occurs.

5.6.4 CPU clock status transition diagram

Figure 5 - 18 shows the CPU Clock Status Transition Diagram of this product.

Figure 5 - 18 CPU Clock Status Transition Diagram



Tables 5 - 3 to 5 - 7 show transition of the CPU clock and examples of setting the SFR registers.

Table 5 - 3 CPU Clock Transition and SFR Register Setting Examples (1/5)

(1) CPU operating with high-speed on-chip oscillator clock (B) after reset release (A)

Status Transition	SFR Register Setting
(A) → (B)	SFR registers do not have to be set (default status after reset release).

(2) CPU operating with high-speed system clock (C) after reset release (A)
(The CPU operates with the high-speed on-chip oscillator clock immediately after a reset release (B).)

(Setting sequence of SFR registers) →

Setting Flag of SFR Register / Status Transition	CMC Register Note 1			OSTS Register	CSC Register	OSTC Register	CKC Register
	EXCLK	OSCSEL	AMPH		MSTOP		MCM0
(A) → (B) → (C) (X1 clock: 1 MHz ≤ fx ≤ 10 MHz)	0	1	0	Note 2	0	Must be checked	1
(A) → (B) → (C) (X1 clock: 10 MHz < fx ≤ 20 MHz)	0	1	1	Note 2	0	Must be checked	1
(A) → (B) → (C) (external main clock)	1	1	×	Note 2	0	Need not be checked	1

Note 1. The clock operation mode control register (CMC) can be written only once by an 8-bit memory manipulation instruction after reset release.

Note 2. Set the oscillation stabilization time as follows.

- Desired the oscillation stabilization time counter status register (OSTC) oscillation stabilization time ≤ Oscillation stabilization time set by the oscillation stabilization time select register (OSTS)

Caution Set the clock after the supply voltage has reached the operable voltage of the clock to be set (see CHAPTER 38 or CHAPTER 39 ELECTRICAL SPECIFICATIONS).

(3) CPU operating with subsystem clock (D) after reset release (A)
(The CPU operates with the high-speed on-chip oscillator clock immediately after a reset release (B).)

(Setting sequence of SFR registers) →

Setting Flag of SFR Register / Status Transition	CMC Register Note				CSC Register	Waiting for Oscillation Stabilization	CKC Register
	EXCLKS	OSCSELS	AMPHS1	AMPHS0	XTSTOP		CSS
(A) → (B) → (D) (XT1 clock)	0	1	0/1	0/1	0	Necessary	1
(A) → (B) → (D) (external sub clock)	1	1	×	×	0	Necessary	1

Note The clock operation mode control register (CMC) can be written only once by an 8-bit memory manipulation instruction after reset release.

Remark 1. ×: don't care

Remark 2. (A) to (J) in Tables 5 - 3 to 5 - 7 correspond to (A) to (J) in Figure 5 - 18.

Table 5 - 4 CPU Clock Transition and SFR Register Setting Examples (2/5)

(4) CPU clock changing from high-speed on-chip oscillator clock (B) to high-speed system clock (C)

(Setting sequence of SFR registers) →

Setting Flag of SFR Register / Status Transition	CMC Register Note 1			OSTS Register	CSC Register	OSTC Register	CKC Register
	EXCLK	OSCSEL	AMPH		MSTOP		MCM0
(B) → (C) (X1 clock: 1 MHz ≤ fx ≤10 MHz)	0	1	0	Note 2	0	Must be checked	1
(B) → (C) (X1 clock: 10 MHz < fx ≤ 20 MHz)	0	1	1	Note 2	0	Must be checked	1
(B) → (C) (external main clock)	1	1	×	Note 2	0	Need not be checked	1

Unnecessary if these registers are already set

Unnecessary if the CPU is operating with the high-speed system clock

Note 1. The clock operation mode control register (CMC) can be written only once by an 8-bit memory manipulation instruction after reset release. This setting is not necessary if it has already been set.

Note 2. Set the oscillation stabilization time as follows.

- Desired the oscillation stabilization time counter status register (OSTC) oscillation stabilization time ≤ Oscillation stabilization time set by the oscillation stabilization time select register (OSTS)

Caution Set the clock after the supply voltage has reached the operable voltage of the clock to be set (see CHAPTER 38 or CHAPTER 39 ELECTRICAL SPECIFICATIONS).

(5) CPU clock changing from high-speed on-chip oscillator clock (B) to subsystem clock (D)

(Setting sequence of SFR registers) →

Setting Flag of SFR Register / Status Transition	CMC Register Note			CSC Register	Waiting for Oscillation Stabilization	CKC Register
	EXCLKS	OSCSELS	AMPHS1, 0	XTSTOP		CSS
(B) → (D) (XT1 clock)	0	1	00: Low power consumption oscillation 01: Normal oscillation 10: Ultra-low power consumption oscillation	0	Necessary	1
(B) → (D) (external sub clock)	1	1	×	0	Necessary	1

Unnecessary if these registers are already set

Unnecessary if the CPU is operating with the subsystem clock

Note The clock operation mode control register (CMC) can be written only once by an 8-bit memory manipulation instruction after reset release. This setting is not necessary if it has already been set.

Remark 1. ×: don't care

Remark 2. (A) to (J) in Tables 5 - 3 to 5 - 7 correspond to (A) to (J) in Figure 5 - 18.

Table 5 - 5 CPU Clock Transition and SFR Register Setting Examples (3/5)

(6) CPU clock changing from high-speed system clock (C) to high-speed on-chip oscillator clock (B)

(Setting sequence of SFR registers) →

Setting Flag of SFR Register / Status Transition	CSC Register	Oscillation accuracy stabilization time	CKC Register
	HIOSTOP		MCM0
(C) → (B)	0	18 μs to 65 μs	0

Unnecessary if the CPU is operating with the high-speed on-chip oscillator clock

Remark The oscillation accuracy stabilization time changes according to the temperature conditions and the STOP mode period.

(7) CPU clock changing from high-speed system clock (C) to subsystem clock (D)

(Setting sequence of SFR registers) →

Setting Flag of SFR Register / Status Transition	CSC Register	Waiting for Oscillation Stabilization	CKC Register
	XTSTOP		CSS
(C) → (D)	0	Necessary	1

Unnecessary if the CPU is operating with the subsystem clock

(8) CPU clock changing from subsystem clock (D) to high-speed on-chip oscillator clock (B)

(Setting sequence of SFR registers) →

Setting Flag of SFR Register / Status Transition	CSC Register	Oscillation accuracy stabilization time	CKC Register
	HIOSTOP		CSS
(D) → (B)	0	18 μs to 65 μs	0

Unnecessary if the CPU is operating with the high-speed on-chip oscillator clock

Remark 1. (A) to (J) in Tables 5 - 3 to 5 - 7 correspond to (A) to (J) in Figure 5 - 18.

Remark 2. The oscillation accuracy stabilization time changes according to the temperature conditions and the STOP mode period.

Table 5 - 6 CPU Clock Transition and SFR Register Setting Examples (4/5)

(9) CPU clock changing from subsystem clock (D) to high-speed system clock (C)

(Setting sequence of SFR registers) →

Setting Flag of SFR Register / Status Transition	OSTS Register	CSC Register	OSTC Register	CKC Register
		MSTOP		CSS
(D) → (C) (X1 clock: 1 MHz ≤ fx ≤ 10 MHz)	Note	0	Must be checked	0
(D) → (C) (X1 clock: 10 MHz < fx ≤ 20 MHz)	Note	0	Must be checked	0
(D) → (C) (external main clock)	Note	0	Need not be checked	0

Unnecessary if the CPU is operating with the high-speed system clock

Note Set the oscillation stabilization time as follows.
- Desired the oscillation stabilization time counter status register (OSTC) oscillation stabilization time ≤ Oscillation stabilization time set by the oscillation stabilization time select register (OSTS)

Caution Set the clock after the supply voltage has reached the operable voltage of the clock to be set (see CHAPTER 38 or CHAPTER 39 ELECTRICAL SPECIFICATIONS).

(10) • HALT mode (E) set while CPU is operating with high-speed on-chip oscillator clock (B)
- HALT mode (F) set while CPU is operating with high-speed system clock (C)
- HALT mode (G) set while CPU is operating with subsystem clock (D)

Status Transition	Setting
(B) → (E) (C) → (F) (D) → (G)	Executing HALT instruction

Remark (A) to (J) in Tables 5 - 3 to 5 - 7 correspond to (A) to (J) in Figure 5 - 18.

Table 5 - 7 CPU Clock Transition and SFR Register Setting Examples (5/5)

(11) • STOP mode (H) set while CPU is operating with high-speed on-chip oscillator clock (B)
• STOP mode (I) set while CPU is operating with high-speed system clock (C)

(Setting sequence) →

Status Transition		Setting		
(B) → (H)		Stopping peripheral functions that are disabled in STOP mode	—	Executing STOP instruction
(C) → (I)	In X1 oscillation		Sets the OSTS register	
	External main system clock		—	

(12) CPU changing from STOP mode (H) to SNOOZE mode (J)
For details about the setting for switching from the STOP mode to the SNOOZE mode, see **20.5.7 SNOOZE mode function**, and **20.7.3 SNOOZE mode function**.

Remark (A) to (J) in Tables 5 - 3 to 5 - 7 correspond to (A) to (J) in Figure 5 - 18.

5.6.5 Condition before changing CPU clock and processing after changing CPU clock

Condition before changing the CPU clock and processing after changing the CPU clock are shown below.

Table 5 - 8 Changing CPU Clock (1/3)

CPU Clock		Condition Before Change	Processing After Change
Before Change	After Change		
High-speed on-chip oscillator clock	X1 clock	Stabilization of X1 oscillation • OSCSEL = 1, EXCLK = 0, MSTOP = 0 • After elapse of oscillation stabilization time	Operating current can be reduced by stopping high-speed on-chip oscillator (HIOSTOP = 1) after checking that the CPU clock is changed.
	External main system clock	Enabling input of external clock from the EXCLK pin • OSCSEL = 1, EXCLK = 1, MSTOP = 0	
	XT1 clock	Stabilization of XT1 oscillation • OSCSELS = 1, EXCLKS = 0, XTSTOP = 0 • After elapse of oscillation stabilization time	
	External subsystem clock	Enabling input of external clock from the EXCLKS pin • OSCSELS = 1, EXCLKS = 1, XTSTOP = 0	
X1 clock	High-speed on-chip oscillator clock	Enabling oscillation of high-speed on-chip oscillator • HIOSTOP = 0 • The oscillation accuracy stabilization time has elapsed	X1 oscillation can be stopped (MSTOP = 1) after checking that the CPU clock is changed.
	External main system clock	Transition not possible	—
	XT1 clock	Stabilization of XT1 oscillation • OSCSELS = 1, EXCLKS = 0, XTSTOP = 0 • After elapse of oscillation stabilization time	X1 oscillation can be stopped (MSTOP = 1) after checking that the CPU clock is changed.
	External subsystem clock	Enabling input of external clock from the EXCLKS pin • OSCSELS = 1, EXCLKS = 1, XTSTOP = 0	X1 oscillation can be stopped (MSTOP = 1) after checking that the CPU clock is changed.

Table 5 - 9 Changing CPU Clock (2/3)

CPU Clock		Condition Before Change	Processing After Change
Before Change	After Change		
External main system clock	High-speed on-chip oscillator clock	Enabling oscillation of high-speed on-chip oscillator • HIOSTOP = 0 • The oscillation accuracy stabilization time has elapsed	External main system clock input can be disabled (MSTOP = 1) after checking that the CPU clock is changed.
	X1 clock	• Transition not possible	—
	XT1 clock	Stabilization of XT1 oscillation • OSCSELS = 1, EXCLKS = 0, XTSTOP = 0 • After elapse of oscillation stabilization time	External main system clock input can be disabled (MSTOP = 1) after checking that the CPU clock is changed.
	External subsystem clock	Enabling input of external clock from the EXCLKS pin • OSCSELS = 1, EXCLKS = 1, XTSTOP = 0	External main system clock input can be disabled (MSTOP = 1) after checking that the CPU clock is changed.
XT1 clock	High-speed on-chip oscillator clock	Oscillation of high-speed on-chip oscillator and selection of high-speed on-chip oscillator clock as main system clock • HIOSTOP = 0, MCS = 0	XT1 oscillation can be stopped (XTSTOP = 1) after checking that the CPU clock is changed.
	X1 clock	Stabilization of X1 oscillation and selection of high-speed system clock as main system clock • OSCSEL = 1, EXCLK = 0, MSTOP = 0 • After elapse of oscillation stabilization time • MCS = 1	
	External main system clock	Enabling input of external clock from the EXCLK pin and selection of high-speed system clock as main system clock • OSCSEL = 1, EXCLK = 1, MSTOP = 0 • MCS = 1	
	External subsystem clock	Transition not possible	—

Table 5 - 10 Changing CPU Clock (3/3)

CPU Clock		Condition Before Change	Processing After Change
Before Change	After Change		
External subsystem clock	High-speed on-chip oscillator clock	Oscillation of high-speed on-chip oscillator and selection of high-speed on-chip oscillator clock as main system clock • HIOSTOP = 0, MCS = 0	External subsystem clock input can be disabled (XTSTOP = 1) after checking that the CPU clock is changed.
	X1 clock	Stabilization of X1 oscillation and selection of high-speed system clock as main system clock • OSCSEL = 1, EXCLK = 0, MSTOP = 0 • After elapse of oscillation stabilization time • MCS = 1	
	External main system clock	Enabling input of external clock from the EXCLK pin and selection of high-speed system clock as main system clock • OSCSEL = 1, EXCLK = 1, MSTOP = 0 • MCS = 1	
	XT1 clock	Transition not possible	—

5.6.6 Time required for switchover of CPU clock and main system clock

By setting bits 4 and 6 (MCM0, CSS) of the system clock control register (CKC), the CPU clock can be switched (between the main system clock and the subsystem clock), and main system clock can be switched (between the high-speed on-chip oscillator clock and the high-speed system clock).

The actual switchover operation is not performed immediately after rewriting to the CKC register; operation continues on the pre-switchover clock for several clocks (see **Tables 5 - 11** to **5 - 13**).

Whether the CPU is operating on the main system clock or the subsystem clock can be ascertained using bit 7 (CLS) of the CKC register. Whether the main system clock is operating on the high-speed system clock or high-speed on-chip oscillator clock can be ascertained using bit 5 (MCS) of the CKC register.

When the CPU clock is switched, the peripheral hardware clock is also switched.

Table 5 - 11 Maximum Time Required for Main System Clock Switchover

Clock A	Switching directions	Clock B	Remark
f_{IH}	⟷	f_{MX}	See **Table 5 - 12**
f_{MAIN}	⟷	f_{SUB}	See **Table 5 - 13**

Table 5 - 12 Maximum Number of Clocks Required for f_{IH} ↔ f_{MX}

Set Value Before Switchover		Set Value After Switchover	
MCM0		MCM0	
		0 ($f_{MAIN} = f_{IH}$)	1 ($f_{MAIN} = f_{MX}$)
0 ($f_{MAIN} = f_{IH}$)	$f_{MX} \geq f_{IH}$		2 clock
	$f_{MX} < f_{IH}$		$2f_{IH}/f_{MX}$ clock
1 ($f_{MAIN} = f_{IH}$)	$f_{MX} \geq f_{IH}$	$2f_{MX}/f_{IH}$ clock	
	$f_{MX} < f_{IH}$	2 clock	

Table 5 - 13 Maximum Number of Clocks Required for f_{MAIN} ↔ f_{SUB}

Set Value Before Switchover	Set Value After Switchover	
CSS	CSS	
	0 ($f_{CLK} = f_{MAIN}$)	1 ($f_{CLK} = f_{SUB}$)
0 ($f_{CLK} = f_{MAIN}$)		$1 + 2f_{MAIN}/f_{SUB}$ clock
1 ($f_{CLK} = f_{SUB}$)	3 clock	

Remark 1. The number of clocks listed in Tables 5 - 12 and 5 - 13 is the number of CPU clocks before switchover.

Remark 2. Calculate the number of clocks in Tables 5 - 12 and 5 - 13 by rounding up the number after the decimal position.

Example When switching the main system clock from the high-speed system clock to the high-speed on-chip oscillator clock (when f_{IH} = 8 MHz, f_{MX} = 10 MHz)

$2f_{MX}/f_{IH}$ cycles = 2 (10/8) = 2.5 → 3 clock cycles

5.6.7 Conditions before clock oscillation is stopped

The following lists the register flag settings for stopping the clock oscillation (disabling external clock input) and conditions before the clock oscillation is stopped.

Table 5 - 14 Conditions Before the Clock Oscillation Is Stopped and Flag Settings

Clock	Conditions Before Clock Oscillation Is Stopped (External Clock Input Disabled)	Flag Settings of SFR Register
High-speed on-chip oscillator clock	MCS = 1 or CLS = 1 (The CPU is operating on a clock other than the high-speed on-chip oscillator clock.)	HIOSTOP = 1
X1 clock External main system clock	MCS = 0 or CLS = 1 (The CPU is operating on a clock other than the high-speed system clock.)	MSTOP = 1
XT1 clock External subsystem clock	CLS = 0 (The CPU is operating on a clock other than the subsystem clock.)	XTSTOP = 1

5.7 Resonator and Oscillator Constants

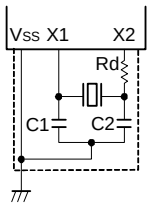
The resonators for which the operation is verified and their oscillator constants are available on the Renesas Electronics website. See the website page for the RL78/H1D.

Caution 1. The constants for these oscillator circuits are reference values based on specific environments set up for evaluation by the manufacturers. For actual applications, request evaluation by the manufacturer of the oscillator circuit mounted on a board. Furthermore, if you are switching from a different product to this microcontroller, and whenever you change the board, again request evaluation by the manufacturer of the oscillator circuit mounted on the new board.

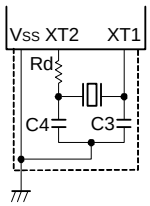
Caution 2. The oscillation voltage and oscillation frequency only indicate the oscillator characteristic. Use the RL78 microcontroller so that the internal operation conditions are within the specifications of the DC and AC characteristics.

Figure 5 - 19 Example of External Circuit

(a) X1 oscillation

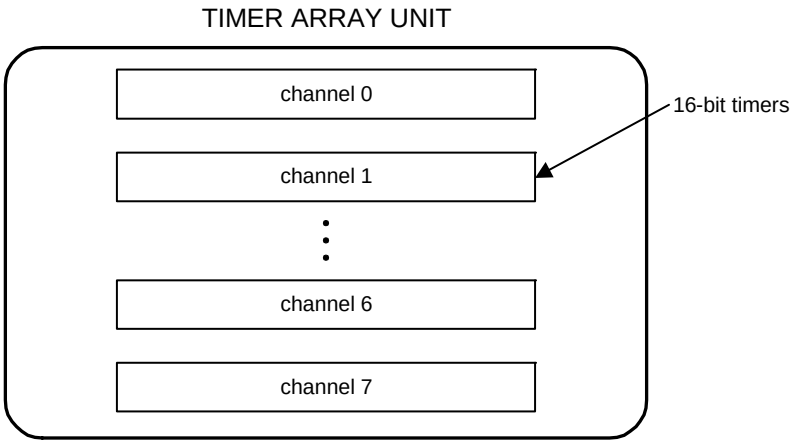


(b) XT1 oscillation



CHAPTER 6 TIMER ARRAY UNIT

The timer array unit has eight 16-bit timers.
Each 16-bit timer is called a channel and can be used as an independent timer. In addition, two or more “channels” can be used to create a high-accuracy timer.



For details about each function, see the table below.

Independent channel operation function	Simultaneous channel operation function
• Interval timer (→ refer to **6.8.1**) • Square wave output (→ refer to **6.8.1**) • External event counter (→ refer to **6.8.2**) • Input pulse interval measurement (→ refer to **6.8.3**) • Measurement of high-/low-level width of input signal (→ refer to **6.8.4**) • Delay counter (→ refer to **6.8.5**)	• One-shot pulse output (→ refer to **6.9.1**) • PWM output (→ refer to **6.9.2**) • Multiple PWM output (→ refer to **6.9.3**)

It is possible to use the 16-bit timer of channels 1 and 3 as two 8-bit timers (higher and lower). The functions that can use channels 1 and 3 as 8-bit timers are as follows:

- Interval timer (upper or lower 8-bit timer)/square wave output (lower 8-bit timer only)
- External event counter (lower 8-bit timer only)
- Delay counter (lower 8-bit timer only)

Channel 7 can be used to realize LIN-bus communication operating in combination with UART0 of the serial array unit.

6.1 Functions of Timer Array Unit

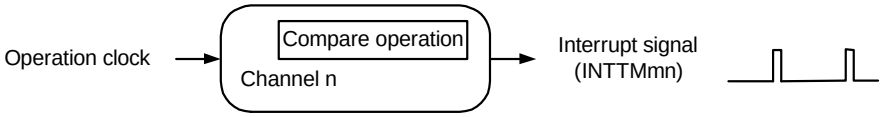
Timer array unit has the following functions.

6.1.1 Independent channel operation function

By operating a channel independently, it can be used for the following purposes without being affected by the operation mode of other channels.

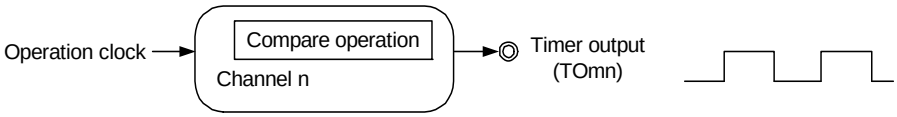
(1) Interval timer

Each timer of a unit can be used as a reference timer that generates an interrupt (INTTMmn) at fixed intervals.



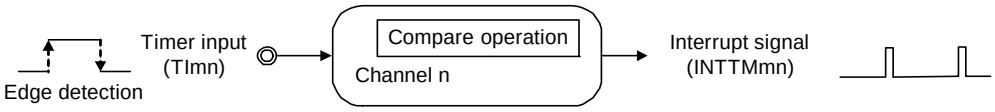
(2) Square wave output

A toggle operation is performed each time INTTMmn interrupt is generated and a square wave with a duty factor of 50% is output from a timer output pin (TOmn).



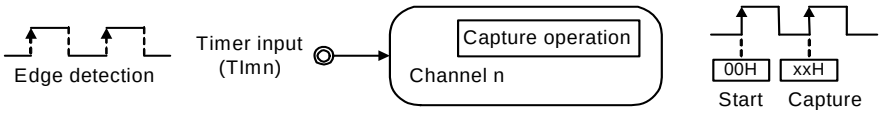
(3) External event counter

Each timer of a unit can be used as an event counter that generates an interrupt when the number of the valid edges of a signal input to the timer input pin (TImn) has reached a specific value.



(4) Input pulse interval measurement

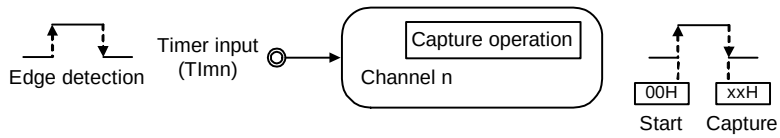
Counting is started by the valid edge of a pulse signal input to a timer input pin (TImn). The count value of the timer is captured at the valid edge of the next pulse. In this way, the interval of the input pulse can be measured.



(**Remark** is listed on the next page.)

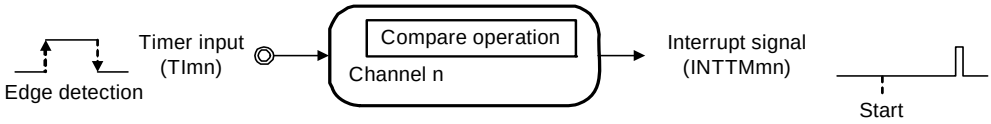
(5) Measurement of high-/low-level width of input signal

Counting is started by a single edge of the signal input to the timer input pin (TImn), and the count value is captured at the other edge. In this way, the high-level or low-level width of the input signal can be measured.



(6) Delay counter

Counting is started at the valid edge of the signal input to the timer input pin (TImn), and an interrupt is generated after any delay period.



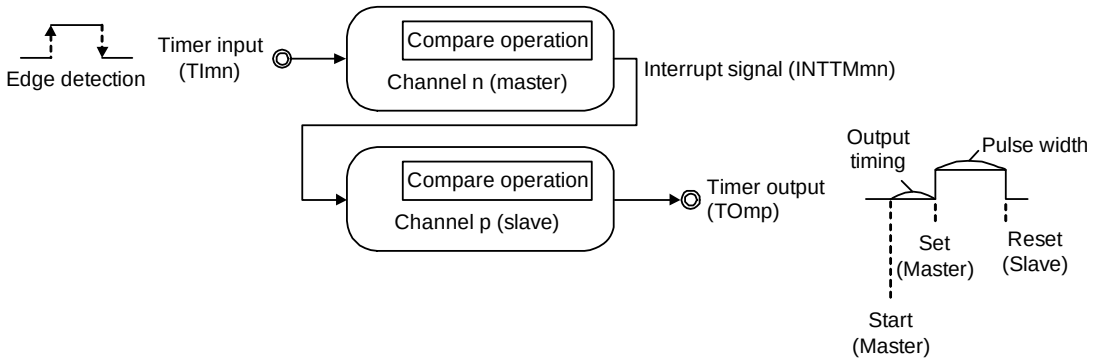
Remark m: Unit number (m = 0), n: Channel number (n = 0 to 7)

6.1.2 Simultaneous channel operation function

By using the combination of a master channel (a reference timer mainly controlling the cycle) and slave channels (timers operating according to the master channel), channels can be used for the following purposes.

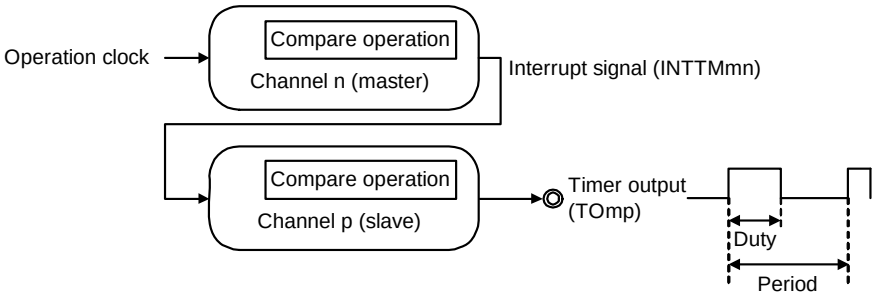
(1) One-shot pulse output

Two channels are used as a set to generate a one-shot pulse with a specified output timing and a specified pulse width.



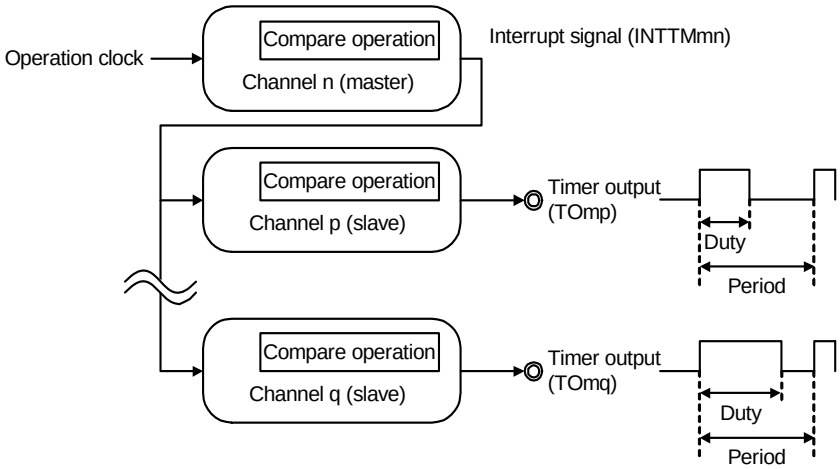
(2) PWM (Pulse Width Modulation) output

Two channels are used as a set to generate a pulse with a specified period and a specified duty factor.



(3) Multiple PWM (Pulse Width Modulation) output

By extending the PWM function and using one master channel and two or more slave channels, up to seven types of PWM signals that have a specific period and a specified duty factor can be generated.



Caution For details about the rules of simultaneous channel operation function, see 6.4.1 Basic rules of simultaneous channel operation function.

Remark m: Unit number (m = 0), n: Channel number (n = 0 to 7),
p, q: Slave channel number (n < p < q ≤ 7)

6.1.3 8-bit timer operation function (channels 1 and 3 only)

The 8-bit timer operation function makes it possible to use a 16-bit timer channel in a configuration consisting of two 8-bit timer channels. This function can only be used for channels 1 and 3.

Caution There are several rules for using 8-bit timer operation function.
For details, see 6.4.2 Basic rules of 8-bit timer operation function (channels 1 and 3 only).

6.1.4 LIN-bus supporting function (channel 7 only)

Timer array unit is used to check whether signals received in LIN-bus communication match the LIN-bus communication format.

(1) Detection of wakeup signal

The timer starts counting at the falling edge of a signal input to the serial data input pin (RxD0) of UART0 and the count value of the timer is captured at the rising edge. In this way, a low-level width can be measured. If the low-level width is greater than a specific value, it is recognized as a wakeup signal.

(2) Detection of sync break field

The timer starts counting at the falling edge of a signal input to the serial data input pin (RxD0) of UART0 after a wakeup signal is detected, and the count value of the timer is captured at the rising edge. In this way, a low-level width is measured. If the low-level width is greater than a specific value, it is recognized as a sync break field.

(3) Measurement of pulse width of sync field

After a sync break field is detected, the low-level width and high-level width of the signal input to the serial data input pin (RxD0) of UART0 are measured. From the bit interval of the sync field measured in this way, a baud rate is calculated.

Remark For details about setting up the operations used to implement the LIN-bus, see **6.3.13 Input switch control register (ISC)** and **6.8.4 Operation as input signal high-/low-level width measurement**.

6.2 Configuration of Timer Array Unit

Timer array unit includes the following hardware.

Table 6 - 1 Configuration of Timer Array Unit

Item	Configuration
Timer/counter	Timer count register mn (TCRmn)
Register	Timer data register mn (TDRmn)
Timer input	TI00 to TI07, RxD0 pin (for LIN-bus)
Timer output	TO00 to TO07, output controller
Control registers	<Registers of unit setting block> • Peripheral enable register 0 (PER0) • Timer clock select register m (TPSm) • Timer channel enable status register m (TEm) • Timer channel start register m (TSm) • Timer channel stop register m (TTm) • Timer input select register 0 (TIS0) • Timer output enable register m (TOEm) • Timer output register m (TOm) • Timer output level register m (TOLm) • Timer output mode register m (TOMm)
	<Registers of each channel> • Timer mode register mn (TMRmn) • Timer status register mn (TSRmn) • Input switch control register (ISC) • Noise filter enable register 1 (NFEN1) • Port mode control register (PMCxx) Note • Port mode register (PMxx) Note • Port register (Pxx) Note

Note The Port mode registers (PMxx) and port registers (Pxx) to be set differ depending on the product. For details, see **4.6.4 Operation of ports that alternately function as SEGxx pins**.

Remark m: Unit number (m = 0), n: Channel number (n = 0 to 7)

The port pins alternatively used as timer I/O pins in each timer array unit channel are shown below.

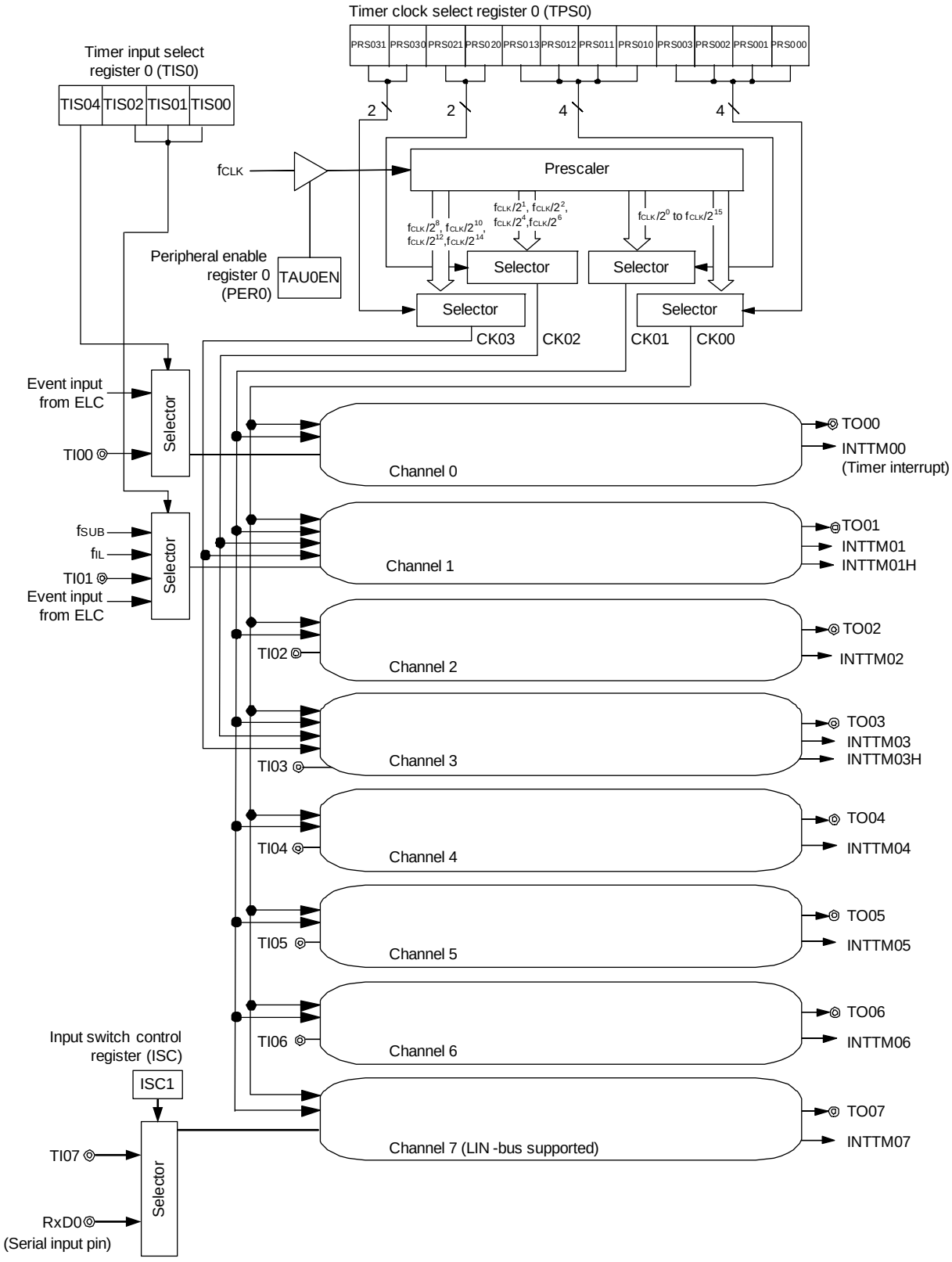
Table 6 - 2 Timer I/O Pins provided in Each Product

Timer array unit channels	R5F11NM	R5F11NL	R5F11PL, R5F11NG	R5F11RM
Channel 0	TI00, TO00			
Channel 1	TI01/TO01			
Channel 2	TI02/TO02			
Channel 3	TI03/TO03			
Channel 4	TI04/TO04			
Channel 5	TI05/TO05			
Channel 6	TI06/TO06			
Channel 7	TI07/TO07			

Remark When the timer input and timer output are multiplexed on the same pin, only one of them can be used.

Figure 6 - 1 shows the block diagram of the timer array unit.

Figure 6 - 1 Entire Configuration of Timer Array Unit



Remark fSUB: Subsystem clock frequency

fIL: Low-speed on-chip oscillator clock frequency

Figure 6 - 2 Internal Block Diagram of Channel 0 of Timer Array Unit

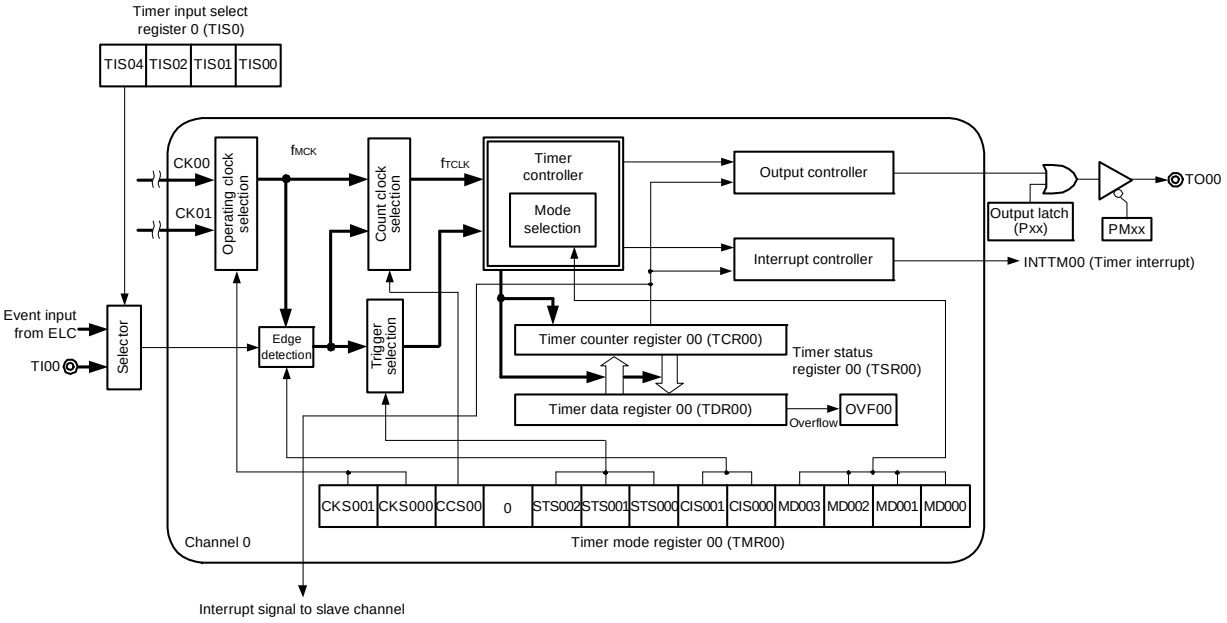


Figure 6 - 3 Internal Block Diagram of Channel 1 of Timer Array Unit

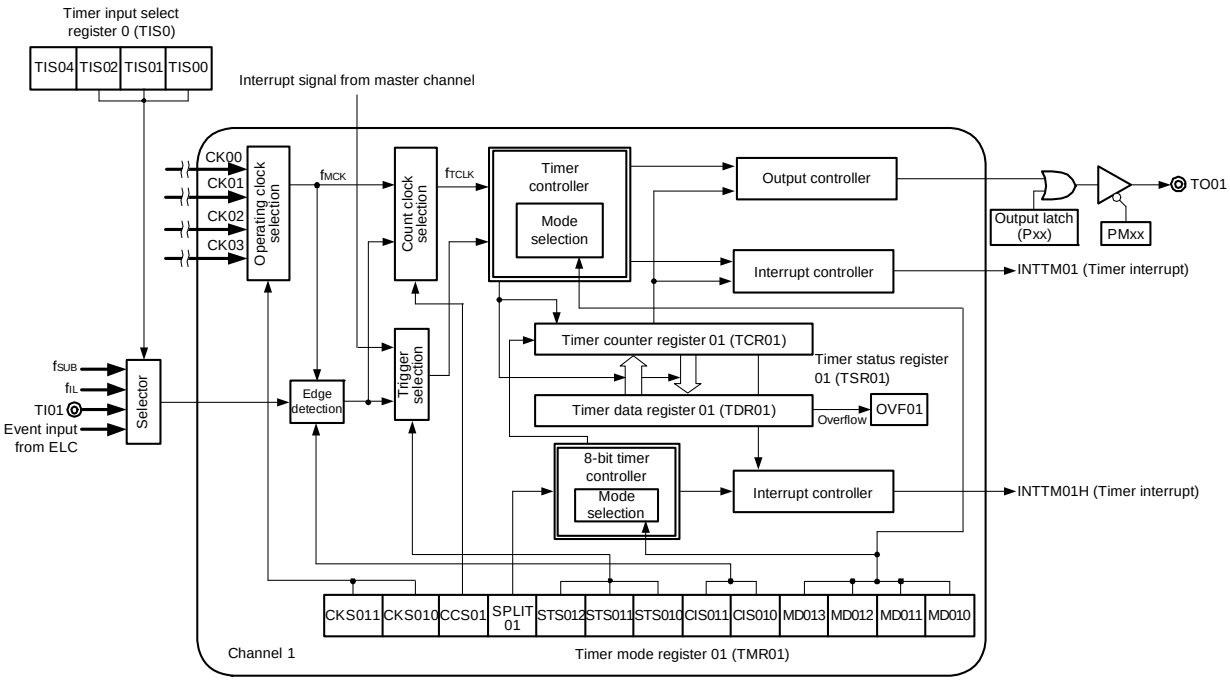
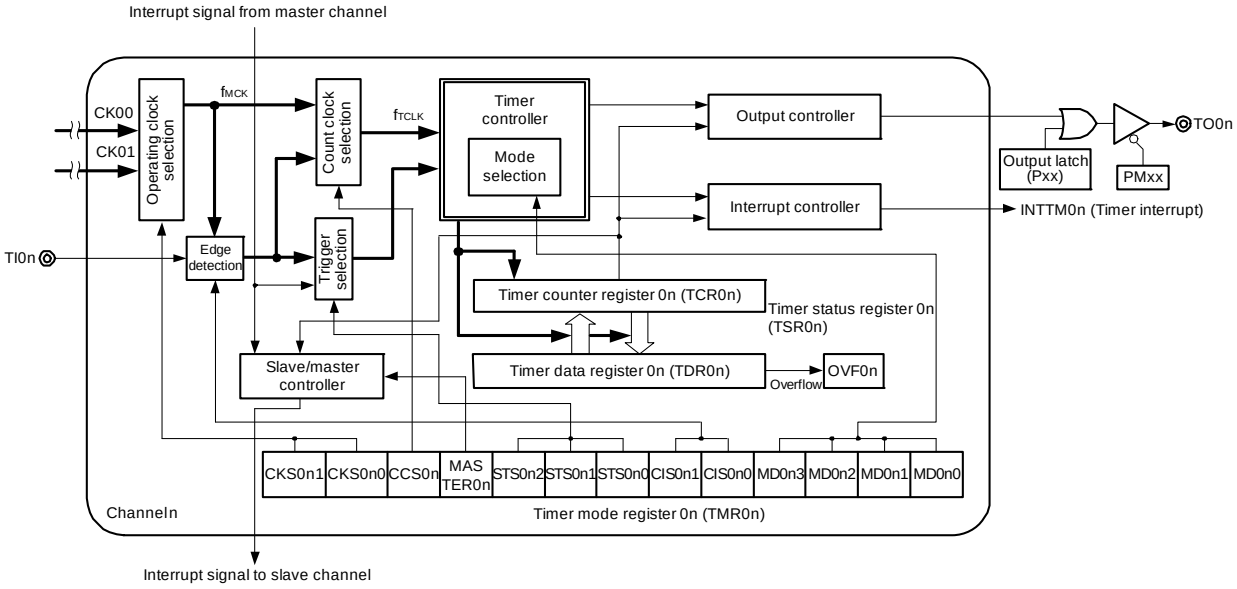


Figure 6 - 4 Internal Block Diagram of Channel n of Timer Array Unit



Remark n = 2, 4, 6

Figure 6 - 5 Internal Block Diagram of Channel 3 of Timer Array Unit

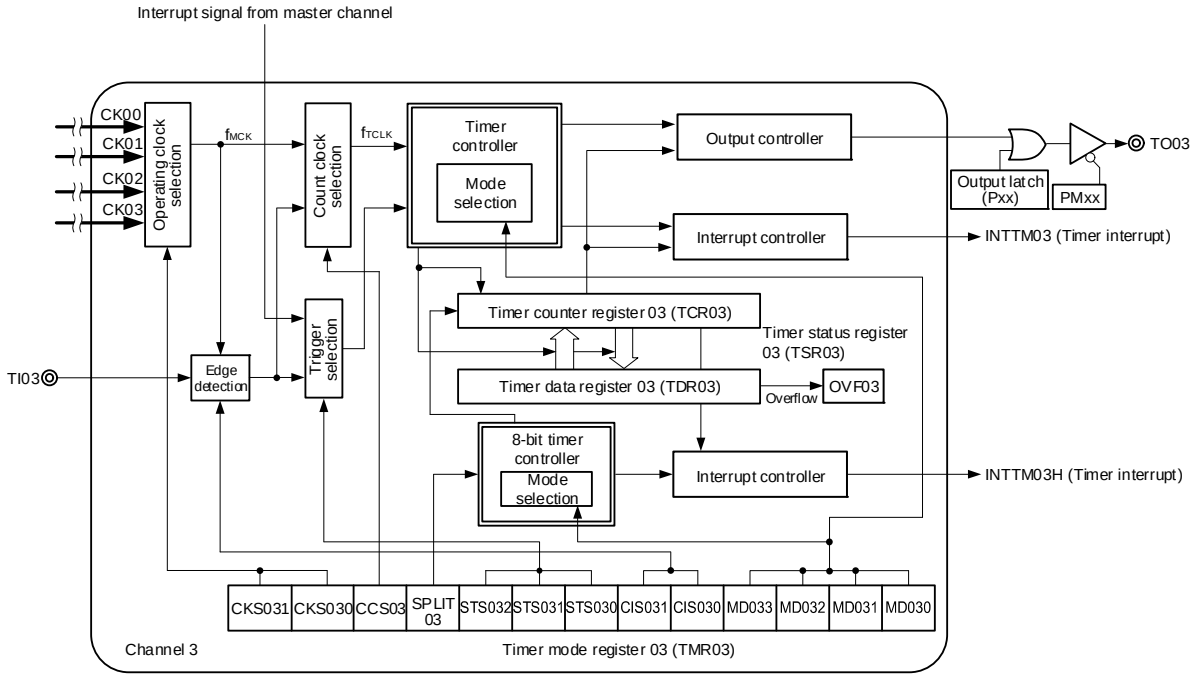


Figure 6 - 6 Internal Block Diagram of Channel 5 of Timer Array Unit

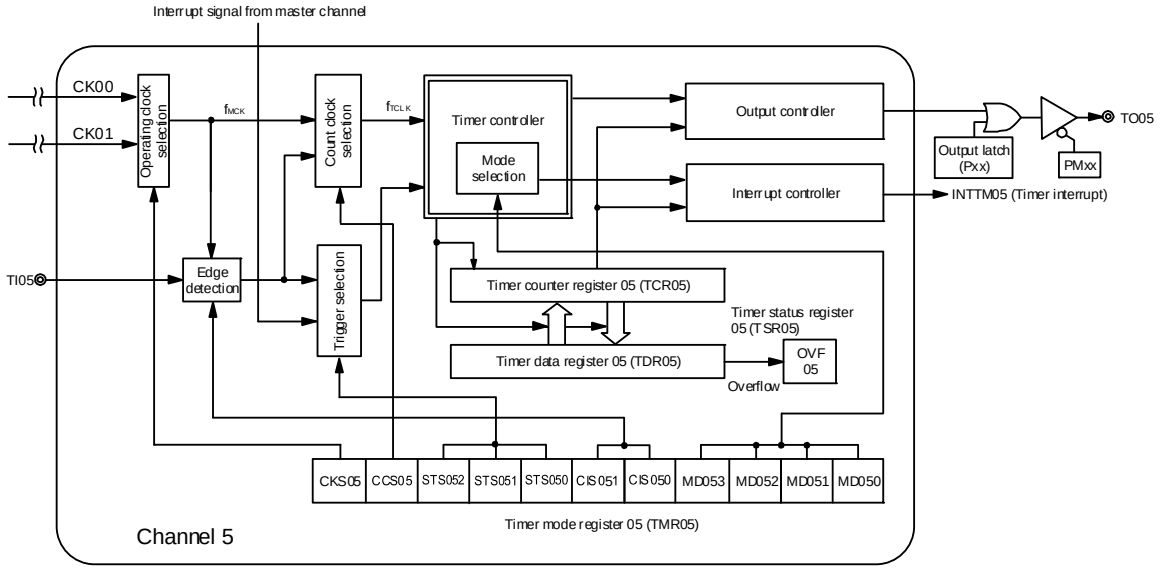
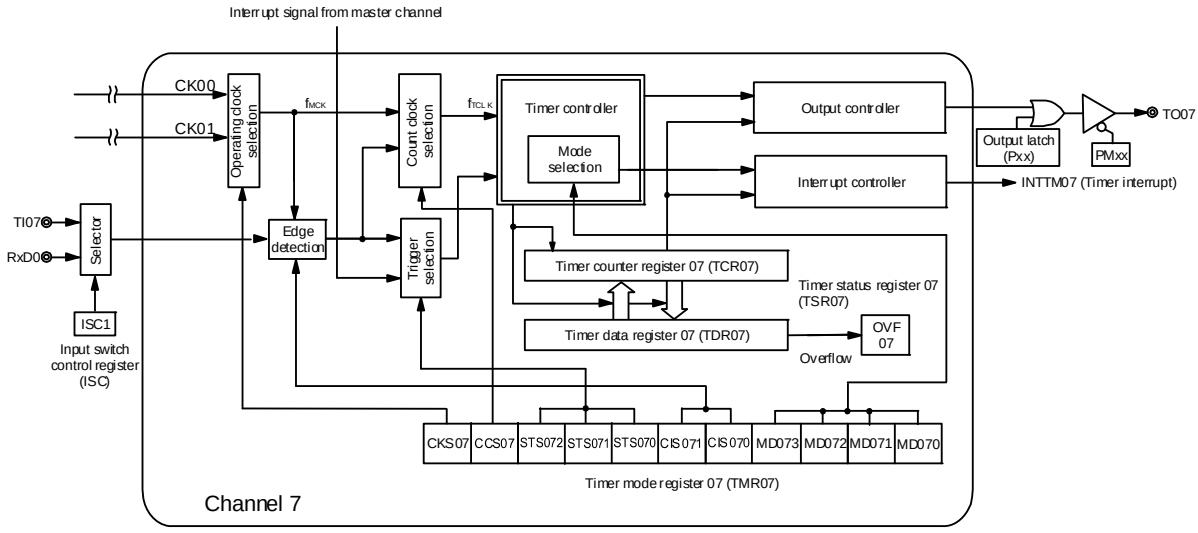


Figure 6 - 7 Internal Block Diagram of Channel 7 of Timer Array Unit



6.2.1 Timer count register mn (TCRmn)

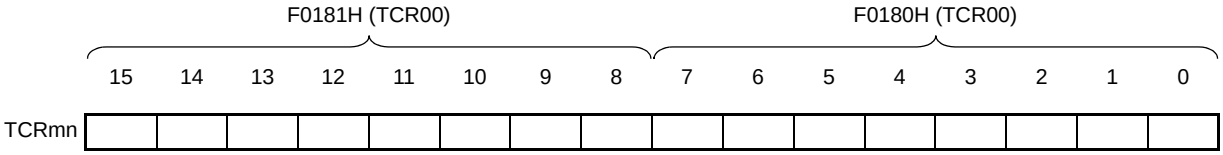
The TCRmn register is a 16-bit read-only register and is used to count clocks.

The value of this counter is incremented or decremented in synchronization with the rising edge of a count clock.

Whether the counter is incremented or decremented depends on the operation mode that is selected by the MDmn3 to MDmn0 bits of timer mode register mn (TMRmn) (refer to **6.3.3 Timer mode register mn (TMRmn)**).

Figure 6 - 8 Format of Timer count register mn (TCRmn)

Address: F0180H, F0181H (TCR00) to F018EH, F018FH (TCR07) After reset: FFFFH R



Remark m: Unit number (m = 0), n: Channel number (n = 0 to 7)

The count value can be read by reading timer count register mn (TCRmn).

The count value is set to FFFFH in the following cases.

- When the reset signal is generated
- When the TAUmEN bit of peripheral enable register 0 (PER0) is cleared
- When counting of the slave channel has been completed in the PWM output mode
- When counting of the slave channel has been completed in the delay count mode
- When counting of the master/slave channel has been completed in the one-shot pulse output mode
- When counting of the slave channel has been completed in the multiple PWM output mode

The count value is cleared to 0000H in the following cases.

- When the start trigger is input in the capture mode
- When capturing has been completed in the capture mode

Caution The count value is not captured to timer data register mn (TDRmn) even when the TCRmn register is read.

The TCRmn register read value differs as follows according to operation mode changes and the operating status.

Table 6 - 3 Timer Count Register mn (TCRmn) Read Value in Various Operation Modes

Operation Mode	Count Mode	Timer count register mn (TCRmn) Read Value Note			
		Value if the operation mode was changed after releasing reset	Value if the operation was restarted after count operation paused (TTmn = 1)	Value if the operation mode was changed after count operation paused (TTmn = 1)	Value when waiting for a start trigger after one count
Interval timer mode	Count down	FFFFH	Value if stop	Undefined	—
Capture mode	Count up	0000H	Value if stop	Undefined	—
Event counter mode	Count down	FFFFH	Value if stop	Undefined	—
One-count mode	Count down	FFFFH	Value if stop	Undefined	FFFFH
Capture & one-count mode	Count up	0000H	Value if stop	Undefined	Capture value of TDRmn register + 1

Note This indicates the value read from the TCRmn register when channel n has stopped operating as a timer (TEmn = 0) and has been enabled to operate as a counter (TSmn = 1). The read value is held in the TCRmn register until the count operation starts.

Remark m: Unit number (m = 0), n: Channel number (n = 0 to 7)

6.2.2 Timer data register mn (TDRmn)

This is a 16-bit register from which a capture function and a compare function can be selected.

The capture or compare function can be switched by selecting an operation mode by using the MDmn3 to MDmn0 bits of timer mode register mn (TMRmn).

The value of the TDRmn register can be changed at any time.

This register can be read or written in 16-bit units.

In addition, for the TDRm1 and TDRm3 registers, while in the 8-bit timer mode (when the SPLIT bits of timer mode registers 01 and 03 (TMRm1, TMRm3) are 1), it is possible to rewrite the data in 8-bit units, with TDRm1H and TDRm3H used as the higher 8 bits, and TDRm1L and TDRm3L used as the lower 8 bits. However, reading is only possible in 16-bit units.

Reset signal generation clears this register to 0000H.

Figure 6 - 9 Format of Timer data register mn (TDRmn) (n = 0, 2, 4 to 7)

Address: FFF18H, FFF19H (TDR00), FFF64H, FFF65H (TDR02) After reset: 0000H R/W
FFF68H, FFF69H (TDR04) to FFF6EH, FFF6FH (TDR07)

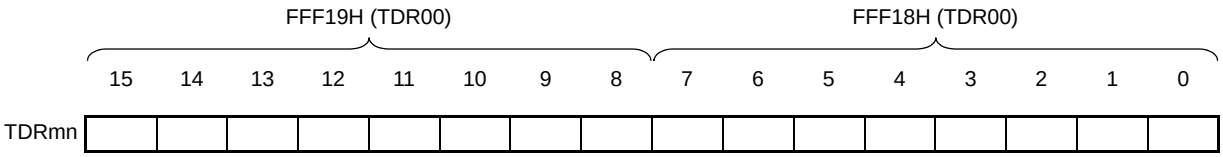
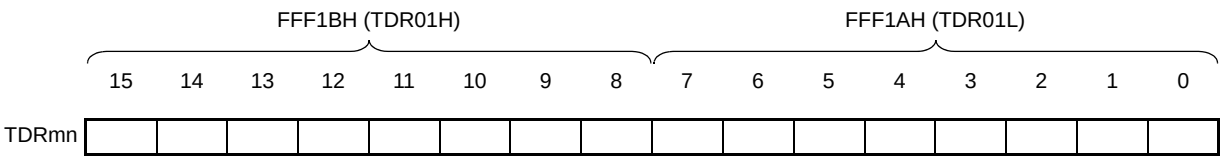


Figure 6 - 10 Format of Timer data register mn (TDRmn) (n = 1, 3)

Address: FFF1AH, FFF1BH (TDR01), FFF66H, FFF67H (TDR03) After reset: 00H R/W



(i) When timer data register mn (TDRmn) is used as compare register

Counting down is started from the value set to the TDRmn register. When the count value reaches 0000H, an interrupt signal (INTTMmn) is generated. The TDRmn register holds its value until it is rewritten.

Caution The TDRmn register does not perform a capture operation even if a capture trigger is input, when it is set to the compare function.

(ii) When timer data register mn (TDRmn) is used as capture register

The count value of timer count register mn (TCRmn) is captured to the TDRmn register when the capture trigger is input.

A valid edge of the TImn pin can be selected as the capture trigger. This selection is made by timer mode register mn (TMRmn).

Remark m: Unit number (m = 0), n: Channel number (n = 0 to 7)

6.3 Registers Controlling Timer Array Unit

Timer array unit is controlled by the following registers.

- Peripheral enable register 0 (PER0)
- Timer clock select register m (TPSm)
- Timer mode register mn (TMRmn)
- Timer status register mn (TSRmn)
- Timer channel enable status register m (TEm)
- Timer channel start register m (TSm)
- Timer channel stop register m (TTm)
- Timer input select register 0 (TIS0)
- Timer output enable register m (TOEm)
- Timer output register m (TOm)
- Timer output level register m (TOLm)
- Timer output mode register m (TOMm)
- Input switch control register (ISC)
- Noise filter enable register 1 (NFEN1)
- Port mode control register (PMCxx)
- Port mode register (PMxx)
- Port register (Pxx)

Caution **Which registers and bits are included depends on the product. Be sure to set bits that are not mounted to their initial values.**

Remark m: Unit number (m = 0), n: Channel number (n = 0 to 7)

6.3.1 Peripheral enable register 0 (PER0)

This register is used to enable or disable supplying the clock to the peripheral hardware. Clock supply to the hardware that is not used is also stopped so as to decrease the power consumption and noise.

When the timer array unit 0 is used, be sure to set bit 0 (TAU0EN) of this register to 1.

The PER0 register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 6 - 11 Format of Peripheral enable register 0 (PER0)

Address: F00F0H After reset: 00H R/W

Symbol	<7>	6	<5>	<4>	<3>	<2>	1	<0>
PER0	RTCWEN	0	ADCEN	IICA0EN	SAU1EN	SAU0EN	0	TAU0EN

TAU0EN	Control of timer array unit input clock
0	Stops supply of input clock. • SFR used by the timer array unit cannot be written. • The timer array unit is in the reset status.
1	Supplies input clock. • SFR used by the timer array unit can be read/written.

Caution 1. When setting the timer array unit, be sure to set the following registers first while the TAUmEN bit is set to 1. If TAUmEN = 0, the values of the registers which control the timer array unit are cleared to their initial values and writing to them is ignored (except for the timer input select register (TIS0), input switch control register (ISC), noise filter enable register 1 (NFEN1), port mode registers (PMxx), and port registers (Pxx)).

- **Timer clock select register m (TPSm)**
- **Timer mode register mn (TMRmn)**
- **Timer status register mn (TSRmn)**
- **Timer channel enable status register m (TEm)**
- **Timer channel start register m (TSm)**
- **Timer channel stop register m (TTm)**
- **Timer output enable register m (TOEm)**
- **Timer output register m (TOm)**
- **Timer output level register m (TOLm)**
- **Timer output mode register m (TOMm)**

Caution 2. Be sure to clear bits 1 and 6 to 0.

6.3.2 Timer clock select register m (TPSm)

The TPSm register is a 16-bit register that is used to select two types or four types of operation clocks (CKm0, CKm1, CKm2, CKm3) that are commonly supplied to each channel. CKm0 is selected by using bits 3 to 0 of the TPSm register, and CKm1 is selected by using bits 7 to 4 of the TPSm register. In addition, only for channels 1 and 3, CKm2 and CKm3 can be also selected. CKm2 is selected by using bits 9 and 8 of the TPSm register, and CKm3 is selected by using bits 13 and 12 of the TPSm register.
Rewriting of the TPSm register during timer operation is possible only in the following cases.

If the PRSm00 to PRSm03 bits can be rewritten (n = 0 to 7):
All channels for which CKm0 is selected as the operation clock (CKSmn1, CKSmn0 = 0, 0) are stopped (TEmn = 0).
If the PRSm10 to PRSm13 bits can be rewritten (n = 0 to 7):
All channels for which CKm2 is selected as the operation clock (CKSmn1, CKSmn0 = 0, 1) are stopped (TEmn = 0).
If the PRSm20 and PRSm21 bits can be rewritten (n = 1, 3):
All channels for which CKm1 is selected as the operation clock (CKSmn1, CKSmn0 = 1, 0) are stopped (TEmn = 0).
If the PRSm30 and PRSm31 bits can be rewritten (n = 1, 3):
All channels for which CKm3 is selected as the operation clock (CKSmn1, CKSmn0 = 1, 1) are stopped (TEmn = 0).

The TPSm register can be set by a 16-bit memory manipulation instruction.
Reset signal generation clears this register to 0000H.

Figure 6 - 12 Format of Timer clock select register m (TPSm) (1/2)

Address: F01B6H, F01B7H After reset: 0000H R/W

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TPSm	0	0	PRSm 31	PRSm 30	0	0	PRSm 21	PRSm 20	PRSm 13	PRSm 12	PRSm 11	PRSm 10	PRSm 03	PRSm 02	PRSm 01	PRSm 00

PRS mk3	PRS mk2	PRS mk1	PRS mk0	Selection of operation clock (CKmk) Note (k = 0, 1)					
					f_{CLK} = 2 MHz	f_{CLK} = 5 MHz	f_{CLK} = 10 MHz	f_{CLK} = 20 MHz	f_{CLK} = 24 MHz
0	0	0	0	f_{CLK}	2 MHz	5 MHz	10 MHz	20 MHz	24 MHz
0	0	0	1	$f_{CLK}/2$	1 MHz	2.5 MHz	5 MHz	10 MHz	12 MHz
0	0	1	0	$f_{CLK}/2^2$	500 kHz	1.25 MHz	2.5 MHz	5 MHz	6 MHz
0	0	1	1	$f_{CLK}/2^3$	250 kHz	625 kHz	1.25 MHz	2.5 MHz	3 MHz
0	1	0	0	$f_{CLK}/2^4$	125 kHz	313 kHz	625 kHz	1.25 MHz	1.5 MHz
0	1	0	1	$f_{CLK}/2^5$	62.5 kHz	156 kHz	313 kHz	625 kHz	750 kHz
0	1	1	0	$f_{CLK}/2^6$	31.3 kHz	78.1 kHz	156 kHz	313 kHz	375 kHz
0	1	1	1	$f_{CLK}/2^7$	15.6 kHz	39.1 kHz	78.1 kHz	156 kHz	187.5 kHz
1	0	0	0	$f_{CLK}/2^8$	7.81 kHz	19.5 kHz	39.1 kHz	78.1 kHz	93.8 kHz
1	0	0	1	$f_{CLK}/2^9$	3.91 kHz	9.77 kHz	19.5 kHz	39.1 kHz	46.9 kHz
1	0	1	0	$f_{CLK}/2^{10}$	1.95 kHz	4.88 kHz	9.77 kHz	19.5 kHz	23.4 kHz
1	0	1	1	$f_{CLK}/2^{11}$	977 Hz	2.44 kHz	4.88 kHz	9.77 kHz	11.7 kHz
1	1	0	0	$f_{CLK}/2^{12}$	488 Hz	1.22 kHz	2.44 kHz	4.88 kHz	5.86 kHz
1	1	0	1	$f_{CLK}/2^{13}$	244 Hz	610 Hz	1.22 kHz	2.44 kHz	2.93 kHz
1	1	1	0	$f_{CLK}/2^{14}$	122 Hz	305 Hz	610 Hz	1.22 kHz	1.46 kHz
1	1	1	1	$f_{CLK}/2^{15}$	61.0 Hz	153 Hz	305 Hz	610 Hz	732 Hz

Note When changing the clock selected for f_{CLK} (by changing the system clock control register (CKC) value), stop timer array unit (TTm = 00FFH).

Caution 1. Be sure to clear bits 15, 14, 11, and 10 to "0".

Caution 2. If f_{CLK} (undivided) is selected as the operation clock (CKmk) and TDRnm is set to 0000H (n = 0, m = 0 to 7), interrupt requests output from timer array units cannot be used.

Remark 1. f_{CLK}: CPU/peripheral hardware clock frequency

Remark 2. The above $f_{CLK}/2^r$ is not a signal which is simply divided f_{CLK} by 2r, but a signal which becomes high level for one period of f_{CLK} from its rising edge (r = 1 to 15). For details, see **6.5.1 Count clock (f_{TCLK})**.

Figure 6 - 12 Format of Timer clock select register m (TPSm) (2/2)

Address: F01B6H, F01B7H After reset: 0000H R/W

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TPSm	0	0	PRSm31	PRSm30	0	0	PRSm21	PRSm20	PRSm13	PRSm12	PRSm11	PRSm10	PRSm03	PRSm02	PRSm01	PRSm00

PRS m21	PRS m20	Selection of operation clock (CKm2) Note					
			f_{CLK} = 2 MHz	f_{CLK} = 5 MHz	f_{CLK} = 10 MHz	f_{CLK} = 20 MHz	f_{CLK} = 24 MHz
0	0	$f_{CLK}/2$	1 MHz	2.5 MHz	5 MHz	10 MHz	12 MHz
0	1	$f_{CLK}/2^2$	500 kHz	1.25 MHz	2.5 MHz	5 MHz	6 MHz
1	0	$f_{CLK}/2^4$	125 kHz	313 kHz	625 kHz	1.25 MHz	1.5 MHz
1	1	$f_{CLK}/2^6$	31.3 kHz	78.1 kHz	156.2 kHz	313 kHz	375 kHz

PRS m31	PRS m30	Selection of operation clock (CKm3) Note					
			f_{CLK} = 2 MHz	f_{CLK} = 5 MHz	f_{CLK} = 10 MHz	f_{CLK} = 20 MHz	f_{CLK} = 24 MHz
0	0	$f_{CLK}/2^8$	7.81 kHz	19.5 kHz	39.1 kHz	78.1 kHz	93.8 kHz
0	1	$f_{CLK}/2^{10}$	1.95 kHz	4.88 kHz	9.77 kHz	19.5 kHz	23.4 kHz
1	0	$f_{CLK}/2^{12}$	488 Hz	1.22 kHz	2.44 kHz	4.88 kHz	5.86 kHz
1	1	$f_{CLK}/2^{14}$	122 Hz	305 Hz	610 Hz	1.22 kHz	1.46 kHz

Note When changing the clock selected for f_{CLK} (by changing the system clock control register (CKC) value), stop the timer array unit (TTm = 00FFH).
The timer array unit must also be stopped if the operating clock (f_{MCK}) or the valid edge of the signal input from the TImn pin is selected.

Caution Be sure to clear bits 15, 14, 11, and 10 to "0".

By using channels 1 and 3 in the 8-bit timer mode and specifying CKm2 or CKm3 as the operation clock, the interval times shown in Table 6 - 4 can be achieved by using the interval timer function.

Table 6 - 4 Interval Times Available for Operation Clock CKSm2 or CKSm3

Clock		Interval time Note (f_{CLK} = 20 MHz)			
		16 µs	160 µs	1.6 ms	16 ms
CKm2	$f_{CLK}/2$	√	—	—	—
	$f_{CLK}/2^2$	√	—	—	—
	$f_{CLK}/2^4$	√	√	—	—
	$f_{CLK}/2^6$	√	√	—	—
CKm3	$f_{CLK}/2^8$	—	√	√	—
	$f_{CLK}/2^{10}$	—	√	√	—
	$f_{CLK}/2^{12}$	—	—	√	√
	$f_{CLK}/2^{14}$	—	—	√	√

Note The margin is within 5%.

Remark 1. f_{CLK}: CPU/peripheral hardware clock frequency

Remark 2. For details of a signal of $f_{CLK}/2^i$ selected with the TPSm register, see **6.5.1 Count clock (f_{TCLK})**.

6.3.3 Timer mode register mn (TMRmn)

The TMRmn register sets an operation mode of channel n. This register is used to select the operation clock (f_{MCK}), select the count clock, select the master/slave, select the 16 or 8-bit timer (only for channels 1 and 3), specify the start trigger and capture trigger, select the valid edge of the timer input, and specify the operation mode (interval, capture, event counter, one-count, or capture and one-count).

Rewriting the TMRmn register is prohibited when the register is in operation (when TEmn = 1). However, bits 7 and 6 (CISmn1, CISmn0) can be rewritten even while the register is operating with some functions (when TEmn = 1) (for details, see **6.8 Independent Channel Operation Function of Timer Array Unit** and **6.9 Simultaneous Channel Operation Function of Timer Array Unit**).

The TMRmn register can be set by a 16-bit memory manipulation instruction.

Reset signal generation clears this register to 0000H.

Caution The bits mounted depend on the channels in bit 11 of TMRmn register.
TMRm2, TMRm4, TMRm6: MASTERmn bit (n = 2, 4, 6)
TMRm1, TMRm3: SPLITmn bit (n = 1, 3)
TMRm0, TMRm5, TMRm7: Fixed to 0

Figure 6 - 13 Format of Timer mode register mn (TMRmn) (1/4)

Address: F0190H, F0191H (TMR00) to F019EH, F019FH (TMR07) After reset: 0000H R/W

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TMRmn (n = 2, 4, 6)	CKSmn1	CKSmn0	0	CCSmn	MASTERmn	STSmn2	STSmn1	STSmn0	CISmn1	CISmn0	0	0	MDmn3	MDmn2	MDmn1	MDmn0

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TMRmn (n = 1, 3)	CKSmn1	CKSmn0	0	CCSmn	SPLITmn	STSmn2	STSmn1	STSmn0	CISmn1	CISmn0	0	0	MDmn3	MDmn2	MDmn1	MDmn0

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TMRmn (n = 0, 5, 7)	CKSmn1	CKSmn0	0	CCSmn	0 Note	STSmn2	STSmn1	STSmn0	CISmn1	CISmn0	0	0	MDmn3	MDmn2	MDmn1	MDmn0

CKSmn1	CKSmn0	Selection of operation clock (f_{MCK}) of channel n
0	0	Operation clock CKm0 set by timer clock select register m (TPSm)
0	1	Operation clock CKm2 set by timer clock select register m (TPSm)
1	0	Operation clock CKm1 set by timer clock select register m (TPSm)
1	1	Operation clock CKm3 set by timer clock select register m (TPSm)
Operation clock (f_{MCK}) is used by the edge detector. A count clock (f_{TCLK}) and a sampling clock are generated depending on the setting of the CCSmn bit. The operation clocks CKm2 and CKm3 can only be selected for channels 1 and 3.		

CCSmn	Selection of count clock (f_{TCLK}) of channel n
0	Operation clock (f_{MCK}) specified by the CKSmn0 and CKSmn1 bits
1	Valid edge of input signal input from the TImn pin In channel 1, Valid edge of input signal selected by TIS0
Count clock (f_{TCLK}) is used for the timer/counter, output controller, and interrupt controller.	

Note Bit 11 is read-only and fixed to 0, so writing to this bit is ignored.

Caution 1. Be sure to clear bits 13, 5, and 4 to "0".

Caution 2. The timer array unit must be stopped (TTm = 00FFH) if the clock selected for f_{CLK} is changed (by changing the value of the system clock control register (CKC)), even if the operating clock specified by using the CKSmn0 and CKSmn1 bits (f_{MCK}) or the valid edge of the signal input from the TImn pin is selected as the count clock (f_{TCLK}).

Remark m: Unit number (m = 0), n: Channel number (n = 0 to 7)

Figure 6 - 14 Format of Timer mode register mn (TMRmn) (2/4)

Address: F0190H, F0191H (TMR00) to F019EH, F019FH (TMR07) After reset: 0000H R/W

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TMRmn (n = 2, 4, 6)	CKSmn1	CKSmn0	0	CCSmn	MASTERmn	STSmn2	STSmn1	STSmn0	CISmn1	CISmn0	0	0	MDmn3	MDmn2	MDmn1	MDmn0

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TMRmn (n = 1, 3)	CKSmn1	CKSmn0	0	CCSmn	SPLITmn	STSmn2	STSmn1	STSmn0	CISmn1	CISmn0	0	0	MDmn3	MDmn2	MDmn1	MDmn0

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TMRmn (n = 0, 5, 7)	CKSmn1	CKSmn0	0	CCSmn	0 Note	STSmn2	STSmn1	STSmn0	CISmn1	CISmn0	0	0	MDmn3	MDmn2	MDmn1	MDmn0

(Bit 11 of TMRmn (n = 2, 4, 6))

MASTERmn	Selection between using channel n independently or simultaneously with another channel (as a slave or master)
0	Operates in independent channel operation function or as slave channel in simultaneous channel operation function.
1	Operates as master channel in simultaneous channel operation function.
Only channel 2, 4, 6 can be set as a master channel (MASTERmn = 1). Be sure to use channel 0, 5, 7 are fixed to 0 (Regardless of the bit setting, channel 0 operates as master, because it is the highest channel). Clear the MASTERmn bit to 0 for a channel that is used with the independent channel operation function.	

(Bit 11 of TMRmn (n = 1, 3))

SPLITmn	Selection of 8 or 16-bit timer operation for channels 1 and 3
0	Operates as 16-bit timer. (Operates in independent channel operation function or as slave channel in simultaneous channel operation function.)
1	Operates as 8-bit timer.

STSmn2	STSmn1	STSmn0	Setting of start trigger or capture trigger of channel n
0	0	0	Only software trigger start is valid (other trigger sources are unselected).
0	0	1	Valid edge of the TImn pin input is used as both the start trigger and capture trigger.
0	1	0	Both the edges of the TImn pin input are used as a start trigger and a capture trigger.
1	0	0	Interrupt signal of the master channel is used (when the channel is used as a slave channel with the simultaneous channel operation function).
Other than above			Setting prohibited

Note Bit 11 is read-only and fixed to 0, so writing to this bit is ignored.

Remark m: Unit number (m = 0), n: Channel number (n = 0 to 7)

Figure 6 - 15 Format of Timer mode register mn (TMRmn) (3/4)

Address: F0190H, F0191H (TMR00) to F019EH, F019FH (TMR07) After reset: 0000H R/W

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TMRmn (n = 2, 4, 6)	CKSmn1	CKSmn0	0	CCSmn	MASTERmn	STSmn2	STSmn1	STSmn0	CISmn1	CISmn0	0	0	MDmn3	MDmn2	MDmn1	MDmn0

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TMRmn (n = 1, 3)	CKSmn1	CKSmn0	0	CCSmn	SPLITmn	STSmn2	STSmn1	STSmn0	CISmn1	CISmn0	0	0	MDmn3	MDmn2	MDmn1	MDmn0

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TMRmn (n = 0, 5, 7)	CKSmn1	CKSmn0	0	CCSmn	0 Note	STSmn2	STSmn1	STSmn0	CISmn1	CISmn0	0	0	MDmn3	MDmn2	MDmn1	MDmn0

(When the input source is other than an event input signal from the ELC by setting the TIS0 register)

CISmn1	CISmn0	Selection of TImn pin input valid edge (n = 0, 1)
0	0	Falling edge
0	1	Rising edge
1	0	Both edges (when low-level width is measured) Start trigger: Falling edge, Capture trigger: Rising edge
1	1	Both edges (when high-level width is measured) Start trigger: Rising edge, Capture trigger: Falling edge
If both the edges are specified when the value of the STSmn2 to STSmn0 bits is other than 010B, set the CISmn1 to CISmn0 bits to 10B.		

When the input source is an event input signal from the ELC by setting the TIS0 register.

CISmn1	CISmn0	Selection of TImn pin input valid edge (n = 0, 1)
0	0	Set to 00 (event input signal from the ELC).
Other than above		Setting prohibited

Note Bit 11 is read-only and fixed to 0, so writing to this bit is ignored.

Remark m: Unit number (m = 0), n: Channel number (n = 0 to 7)

Figure 6 - 16 Format of Timer mode register mn (TMRmn) (4/4)

Address: F0190H, F0191H (TMR00) to F019EH, F019FH (TMR07) After reset: 0000H R/W

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TMRmn (n = 2, 4, 6)	CKSmn1	CKSmn0	0	CCSmn	MASTERmn	STSmn2	STSmn1	STSmn0	CISmn1	CISmn0	0	0	MDmn3	MDmn2	MDmn1	MDmn0

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TMRmn (n = 1, 3)	CKSmn1	CKSmn0	0	CCSmn	SPLITmn	STSmn2	STSmn1	STSmn0	CISmn1	CISmn0	0	0	MDmn3	MDmn2	MDmn1	MDmn0

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TMRmn (n = 0, 5, 7)	CKSmn1	CKSmn0	0	CCSmn	0 Note 1	STSmn2	STSmn1	STSmn0	CISmn1	CISmn0	0	0	MDmn3	MDmn2	MDmn1	MDmn0

MD mn3	MD mn2	MD mn1	Operation mode of channel n	Corresponding function	Count operation of TCR
0	0	0	Interval timer mode	Interval timer / Square wave output / PWM output (master)	Counting down
0	1	0	Capture mode	Input pulse interval measurement	Counting up
0	1	1	Event counter mode	External event counter	Counting down
1	0	0	One-count mode	Delay counter / One-shot pulse output / PWM output (slave)	Counting down
1	1	0	Capture & one-count mode	Measurement of high-/low-level width of input signal	Counting up
Other than above			Setting prohibited		
The operation of each mode varies depending on MDmn0 bit (see the table below).					

Operation mode (Value set by the MDmn3 to MDmn1 bits (see the table above))	MDmn0	Setting of starting counting and interrupt
• Interval timer mode (0, 0, 0) • Capture mode (0, 1, 0)	0	Timer interrupt is not generated when counting is started (timer output does not change, either).
	1	Timer interrupt is generated when counting is started (timer output also changes).
• Event counter mode (0, 1, 1)	0	Timer interrupt is not generated when counting is started (timer output does not change, either).
• One-count mode Note 2 (1, 0, 0)	0	Start trigger is invalid during counting operation. At that time, interrupt is not generated, either.
	1	Start trigger is valid during counting operation Note 3. At that time, interrupt is not generated, either.
• Capture & one-count mode (1, 1, 0)	0	Timer interrupt is not generated when counting is started (timer output does not change, either). Start trigger is invalid during counting operation. At that time interrupt is not generated, either.

Note 1. Bit 11 is read-only and fixed to 0, so writing to this bit is ignored.

Note 2. In one-count mode, interrupt output (INTTMmn) when starting a count operation and TOmn output are not controlled.

Note 3. If the start trigger (TSmn = 1) is issued during operation, the counter is initialized, an interrupt is generated, and recounting is started (does not occur the interrupt request).

Remark m: Unit number (m = 0), n: Channel number (n = 0 to 7)

6.3.4 Timer status register mn (TSRmn)

The TSRmn register indicates the overflow status of the counter of channel n.

The TSRmn register is valid only in the capture mode (MDmn3 to MDmn1 = 010B) and capture & one-count mode (MDmn3 to MDmn1 = 110B). See **Table 6 - 5** for the operation of the OVF bit in each operation mode and set/clear conditions.

The TSRmn register can be read by a 16-bit memory manipulation instruction.

The lower 8 bits of the TSRmn register can be set with an 8-bit memory manipulation instruction with TSRmnL.

Reset signal generation clears this register to 0000H.

Figure 6 - 17 Format of Timer status register mn (TSRmn)

Address: F01A0H, F01A1H (TSR00) to F01AEH, F01AFH (TSR07) After reset: 0000H R

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TSRmn	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	OVF

OVF	Counter overflow status of channel n
0	Overflow does not occur.
1	Overflow occurs.
When OVF = 1, this flag is cleared (OVF = 0) when the next value is captured without overflow.	

Remark m: Unit number (m = 0), n: Channel number (n = 0 to 7)

Table 6 - 5 OVF Bit Operation and Set/Clear Conditions in Each Operation Mode

Timer operation mode	OVF bit	Set/clear conditions
• Capture mode • Capture & one-count mode	clear	When no overflow has occurred upon capturing
	set	When an overflow has occurred upon capturing
• Interval timer mode • Event counter mode • One-count mode	clear	—
	set	(Use prohibited)

Remark The OVF bit does not change immediately after the counter has overflowed, but changes upon the subsequent capture.

6.3.5 Timer channel enable status register m (TEm)

The TEm register is used to enable or stop the timer operation of each channel.

Each bit of the TEm register corresponds to each bit of the timer channel start register m (TSm) and the timer channel stop register m (TTm). When a bit of the TSm register is set to 1, the corresponding bit of this register is set to 1. When a bit of the TTm register is set to 1, the corresponding bit of this register is cleared to 0.

The TEm register can be read by a 16-bit memory manipulation instruction.

The lower 8 bits of the TEm register can be set with a 1-bit or 8-bit memory manipulation instruction with TEmL.

Reset signal generation clears this register to 0000H.

Figure 6 - 18 Format of Timer channel enable status register m (TEm)

Address: F01B0H, F01B1H After reset: 0000H R

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TEm	0	0	0	0	TEHm3	0	TEHm1	0	TEm7	TEm6	TEm5	TEm4	TEm3	TEm2	TEm1	TEm0

TEHm3	Indication of whether operation of the higher 8-bit timer is enabled or stopped when channel 3 is in the 8-bit timer mode
0	Operation is stopped.
1	Operation is enabled.

TEHm1	Indication of whether operation of the higher 8-bit timer is enabled or stopped when channel 1 is in the 8-bit timer mode
0	Operation is stopped.
1	Operation is enabled.

TEmn	Indication of operation enable/stop status of channel n
0	Operation is stopped.
1	Operation is enabled.
This bit displays whether operation of the lower 8-bit timer for TEm1 and TEm3 is enabled or stopped when channel 1 or 3 is in the 8-bit timer mode.	

Remark m: Unit number (m = 0), n: Channel number (n = 0 to 7)

6.3.6 Timer channel start register m (TSm)

The TSm register is a trigger register that is used to initialize timer count register mn (TCRmn) and start the counting operation of each channel.

When a bit of this register is set to 1, the corresponding bit of timer channel enable status register m (TEm) is set to 1. The TSmn, TSHm1, TSHm3 bits are immediately cleared when operation is enabled (TEmn, TEHm1, TEHm3 = 1), because they are trigger bits.

The TSm register can be set by a 16-bit memory manipulation instruction.

The lower 8 bits of the TSm register can be set with a 1-bit or 8-bit memory manipulation instruction with TSmL.

Reset signal generation clears this register to 0000H.

Figure 6 - 19 Format of Timer channel start register m (TSm)

Address: F01B2H, F01B3H After reset: 0000H R/W

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TSm	0	0	0	0	TSHm3	0	TSHm1	0	TSm7	TSm6	TSm5	TSm4	TSm3	TSm2	TSm1	TSm0

TSHm3	Trigger to enable operation (start operation) of the higher 8-bit timer when channel 3 is in the 8-bit timer mode
0	No trigger operation
1	The TEHm3 bit is set to 1 and the count operation becomes enabled. The TCRm3 register count operation start in the interval timer mode in the count operation enabled state (see **Table 6 - 6** in **6.5.2 Start timing of counter**).

TSHm1	Trigger to enable operation (start operation) of the higher 8-bit timer when channel 1 is in the 8-bit timer mode
0	No trigger operation
1	The TEHm1 bit is set to 1 and the count operation becomes enabled. The TCRm1 register count operation start in the interval timer mode in the count operation enabled state (see **Table 6 - 6** in **6.5.2 Start timing of counter**).

TSmn	Operation enable (start) trigger of channel n
0	No trigger operation
1	The TEmn bit is set to 1 and the count operation becomes enabled. The TCRmn register count operation start in the count operation enabled state varies depending on each operation mode (see **Table 6 - 6** in **6.5.2 Start timing of counter**). This bit is the trigger to enable operation (start operation) of the lower 8-bit timer for TSm1 and TSm3 when channel 1 or 3 is in the 8-bit timer mode.

(**Caution** and **Remark** are listed on the next page.)

Caution 1. Be sure to clear bits 15 to 12, 10, and 8 to “0”.

Caution 2. When switching from a function that does not use TImn pin input to one that does, the following wait period is required from when timer mode register mn (TMRmn) is set until the TSmn (TSHm1, TSHm3) bit is set to 1.
When the TImn pin noise filter is enabled (TNFENmn = 1): Four cycles of the operation clock (f_{MCK})
When the TImn pin noise filter is disabled (TNFENmn = 0): Two cycles of the operation clock (f_{MCK})

Remark 1. When the TSm register is read, 0 is always read.

Remark 2. m: Unit number (m = 0), n: Channel number (n = 0 to 7)

6.3.7 Timer channel stop register m (TTm)

The TTm register is a trigger register that is used to stop the counting operation of each channel.

When a bit of this register is set to 1, the corresponding bit of timer channel enable status register m (TEm) is cleared to 0. The TTmn, TTHm1, TTHm3 bits are immediately cleared when operation is stopped (TEmn, TEHm1, TEHm3 = 0), because they are trigger bits.

The TTm register can be set by a 16-bit memory manipulation instruction.

The lower 8 bits of the TTm register can be set with a 1-bit or 8-bit memory manipulation instruction with TTmL.

Reset signal generation clears this register to 0000H.

Figure 6 - 20 Format of Timer channel stop register m (TTm)

Address: F01B4H, F01B5H After reset: 0000H R/W

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TTm	0	0	0	0	TTHm3	0	TTHm1	0	TTm7	TTm6	TTm5	TTm4	TTm3	TTm2	TTm1	TTm0

TTHm3	Trigger to stop operation of the higher 8-bit timer when channel 3 is in the 8-bit timer mode
0	No trigger operation
1	TEHm3 bit is cleared to 0 and the count operation is stopped.

TTHm1	Trigger to stop operation of the higher 8-bit timer when channel 1 is in the 8-bit timer mode
0	No trigger operation
1	TEHm1 bit is cleared to 0 and the count operation is stopped.

TTmn	Operation stop trigger of channel n
0	No trigger operation
1	TEmn bit is cleared to 0 and the count operation is stopped. This bit is the trigger to stop operation of the lower 8-bit timer for TTm1 and TTm3 when channel 1 or 3 is in the 8-bit timer mode.

Caution Be sure to clear bits 15 to 12, 10, and 8 of the TTm register to “0”.

Remark 1. When the TTm register is read, 0 is always read.

Remark 2. m: Unit number (m = 0), n: Channel number (n = 0 to 7)

6.3.8 Timer input select register 0 (TIS0)

The TIS0 register is used to select the channel 0 and 1 timer input.

The TIS0 register can be set by an 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 6 - 21 Format of Timer input select register 0 (TIS0)

Address: F0074H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
TIS0	0	0	0	TIS04	0	TIS02	TIS01	TIS00

TIS04	Selection of timer input used with channel 0
0	Input signal of timer input pin (TI00)
1	Event input signal from ELC

TIS02	TIS01	TIS00	Selection of timer input used with channel 1
0	0	0	Input signal of timer input pin (TI01)
0	1	0	
0	1	1	
0	0	1	Event input signal from ELC
1	0	0	Low-speed on-chip oscillator clock (f_{IL})
1	0	1	Subsystem clock (f_{SUB})
Other than above			Setting prohibited

Caution 1. High-level width, low-level width of timer input is selected, will require more than 1/f_{MCK} + 10 ns. Therefore, when selecting f_{SUB} to f_{CLK} (CSS bit of CKS register = 1), the TIS02 bit cannot be set to 1.

Caution 2. When selecting an event input signal from the ELC using timer input select register 0 (TIS0), select f_{CLK} using timer clock select register 0 (TPS0).

6.3.9 Timer output enable register m (TOEm)

The TOEm register is used to enable or disable timer output of each channel.

Channel n for which timer output has been enabled becomes unable to rewrite the value of the TOmn bit of timer output register m (TOm) described later by software, and the value reflecting the setting of the timer output function through the count operation is output from the timer output pin (TOmn).

The TOEm register can be set by a 16-bit memory manipulation instruction.

The lower 8 bits of the TOEm register can be set with a 1-bit or 8-bit memory manipulation instruction with TOEmL.

Reset signal generation clears this register to 0000H.

Figure 6 - 22 Format of Timer output enable register m (TOEm)

Address: F01BAH, F01BBH After reset: 0000H R/W

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TOEm	0	0	0	0	0	0	0	0	TOEm7	TOEm6	TOEm5	TOEm4	TOEm3	TOEm2	TOEm1	TOEm0

TOEmn	Timer output enable/disable of channel n
0	Timer output is disabled. Timer operation is not applied to the TOmn bit and the output is fixed. Writing to the TOmn bit is enabled and the level set in the TOmn bit is output from the TOmn pin.
1	Timer output is enabled. Timer operation is applied to the TOmn bit and an output waveform is generated. Writing to the TOmn bit is ignored.

Caution Be sure to clear bits 15 to 8 to “0”.

Remark m: Unit number (m = 0), n: Channel number (n = 0 to 7)

6.3.10 Timer output register m (TOm)

The TOm register is a buffer register of timer output of each channel.

The value of each bit in this register is output from the timer output pin (TOmn) of each channel.

The TOmn bit of this register can be rewritten by software only when timer output is disabled (TOEmn = 0). When timer output is enabled (TOEmn = 1), rewriting this register by software is ignored, and the value is changed only by the timer operation.

To use the TI00/TO00 to TI07/TO07 pins as a port function pin, set the corresponding TOmn bit to “0”.

The TOm register can be set by a 16-bit memory manipulation instruction.

The lower 8 bits of the TOm register can be set with an 8-bit memory manipulation instruction with TOmL.

Reset signal generation clears this register to 0000H.

Figure 6 - 23 Format of Timer output register m (TOm)

Address: F01B8H, F01B9H After reset: 0000H R/W

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TOm	0	0	0	0	0	0	0	0	TOm7	TOm6	TOm5	TOm4	TOm3	TOm2	TOm1	TOm0

TOmn	Timer output of channel n
0	Timer output value is “0”.
1	Timer output value is “1”.

Caution Be sure to clear bits 15 to 8 to “0”.

Remark m: Unit number (m = 0), n: Channel number (n = 0 to 7)

6.3.11 Timer output level register m (TOLm)

The TOLm register is a register that controls the timer output level of each channel.

The setting of the inverted output of channel n by this register is reflected at the timing of set or reset of the timer output signal while the timer output is enabled (TOEmn = 1) in the Slave channel output mode (TOMmn = 1). In the master channel output mode (TOMmn = 0), this register setting is invalid.

The TOLm register can be set by a 16-bit memory manipulation instruction.

The lower 8 bits of the TOLm register can be set with an 8-bit memory manipulation instruction with TOLmL.

Reset signal generation clears this register to 0000H.

Figure 6 - 24 Format of Timer output level register m (TOLm)

Address: F01BCH, F01BDH After reset: 0000H R/W

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TOLm	0	0	0	0	0	0	0	0	TOLm7	TOLm6	TOLm5	TOLm4	TOLm3	TOLm2	TOLm1	0

TOLmn	Control of timer output level of channel n
0	Positive logic output (active-high)
1	Negative logic output (active-low)

Caution Be sure to clear bits 15 to 8, and 0 to “0”.

Remark 1. If the value of this register is rewritten during timer operation, the timer output logic is inverted when the timer output signal changes next, instead of immediately after the register value is rewritten.

Remark 2. m: Unit number (m = 0), n: Channel number (n = 0 to 7)

6.3.12 Timer output mode register m (TOMm)

The TOMm register is used to control the timer output mode of each channel.

When a channel is used for the independent channel operation function, set the corresponding bit of the channel to be used to 0.

When a channel is used for the simultaneous channel operation function (PWM output, one-shot pulse output, or multiple PWM output), set the corresponding bit of the master channel to 0 and the corresponding bit of the slave channel to 1.

The setting of each channel n by this register is reflected at the timing when the timer output signal is set or reset while the timer output is enabled (TOEmn = 1).

The TOMm register can be set by a 16-bit memory manipulation instruction.

The lower 8 bits of the TOMm register can be set with an 8-bit memory manipulation instruction with TOMmL.

Reset signal generation clears this register to 0000H.

Figure 6 - 25 Format of Timer output mode register m (TOMm)

Address: F01BEH, F01BFH After reset: 0000H R/W

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TOMm	0	0	0	0	0	0	0	0	TOMm 7	TOMm 6	TOMm 5	TOMm 4	TOMm 3	TOMm 2	TOMm 1	0

TOM mn	Control of timer output mode of channel n
0	Master channel output mode (to produce toggle output by timer interrupt request signal (INTTMmn)
1	Slave channel output mode (output is set by the timer interrupt request signal (INTTMmn) of the master channel, and reset by the timer interrupt request signal (INTTM0p) of the slave channel)

Caution **Be sure to clear bits 15 to 8, and 0 to “0”.**

Remark m: Unit number (m = 0)
n: Channel number
n = 0 to 7 (n = 0, 2, 4, 6 for master channel)
p: Slave channel number
n < p ≤ 7
(For details of the relation between the master channel and slave channel, refer to **6.4.1 Basic rules of simultaneous channel operation function**.)

6.3.13 Input switch control register (ISC)

The ISC1 and ISC0 bits of the ISC register are used to implement LIN-bus communication operation by using channel 7 in association with the serial array unit. When the ISC1 bit is set to 1, the input signal of the serial data input pin (RxD0) is selected as a timer input signal.

For details about setting the SSIE00 bit, see **20.3.15 Input switch control register (ISC)**.

The ISC register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 6 - 26 Format of Input switch control register (ISC)

Address: F0073H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
ISC	SSIE00	0	0	0	0	0	ISC1	ISC0

SSIE00	Channel 0 $\overline{\text{SSI00}}$ input setting in CSI00 communication and slave mode
0	Disables $\overline{\text{SSI00}}$ pin input.
1	Enables $\overline{\text{SSI00}}$ pin input.

ISC1	Switching channel 7 input of timer array unit 0
0	Uses the input signal of the TI07 pin as a timer input (normal operation).
1	Input signal of the RXD0 pin is used as timer input (detects the wakeup signal and measures the low width of the break field and the pulse width of the sync field).

ISC0	Switching external interrupt (INTP0) input
0	Uses the input signal of the INTP0 pin as an external interrupt (normal operation).
1	Uses the input signal of the RXD0 pin as an external interrupt (wakeup signal detection).

Caution Be sure to clear bits 6 to 2 to “0”.

Remark When the LIN-bus communication function is used, select the input signal of the RxD0 pin by setting ISC1 to 1.

6.3.14 Noise filter enable register 1 (NFEN1)

The NFEN1 register is used to set whether the noise filter can be used for the timer input signal to each channel.
Enable the noise filter by setting the corresponding bits to 1 on the pins in need of noise removal.
When the noise filter is enabled, after synchronization with the operating clock (f_{MCK}) for the target channel, whether the signal keeps the same value for two clock cycles is detected. When the noise filter is disabled, the input signal is only synchronized with the operating clock (f_{MCK}) for the target channel Note.
The NFEN1 register can be set by a 1-bit or 8-bit memory manipulation instruction.
Reset signal generation clears this register to 00H.

Note For details, see **6.5.1 (2) When valid edge of input signal via the TImn pin is selected (CCSmn = 1)**, **6.5.2 Start timing of counter**, and **6.7 Timer Input (TImn) Control**.

Figure 6 - 27 Format of Noise filter enable register 1 (NFEN1)

Address: F0071H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
NFEN1	TNFEN07	TNFEN06	TNFEN05	TNFEN04	TNFEN03	TNFEN02	TNFEN01	TNFEN00

TNFEN07	Enable/disable using noise filter of TI07 pin or RxD0 pin input signal Note
0	Noise filter OFF
1	Noise filter ON

TNFEN06	Enable/disable using noise filter of TI06 pin input signal
0	Noise filter OFF
1	Noise filter ON

TNFEN05	Enable/disable using noise filter of TI05 pin input signal
0	Noise filter OFF
1	Noise filter ON

TNFEN04	Enable/disable using noise filter of TI04 pin input signal
0	Noise filter OFF
1	Noise filter ON

TNFEN03	Enable/disable using noise filter of TI03 pin input signal
0	Noise filter OFF
1	Noise filter ON

TNFEN02	Enable/disable using noise filter of TI02 pin input signal
0	Noise filter OFF
1	Noise filter ON

TNFEN01	Enable/disable using noise filter of TI01 pin input signal
0	Noise filter OFF
1	Noise filter ON

TNFEN00	Enable/disable using noise filter of TI00 pin input signal
0	Noise filter OFF
1	Noise filter ON

Note The applicable pin can be switched by setting the ISC1 bit of the ISC register.
ISC1 = 0: Whether or not to use the noise filter of the TI07 pin can be selected.
ISC1 = 1: Whether or not to use the noise filter of the RxD0 pin can be selected.

6.3.15 Registers that control port functions of timer input/output pins

Using the timer array unit requires setting of the registers that control the port functions for the port pins with which the timer array unit pin functions for the target channel are multiplexed (port mode register (PMxx), port register (Pxx), and port mode control register (PMCxx)). For details, see **4.4.1 Port mode registers (PMxx)**, **4.4.2 Port registers (Pxx)**, and **4.4.6 Port mode control registers (PMCxx)**.
The port mode register (PMxx), port register (Pxx), and port mode control register (PMCxx) to be set depend on the product. For details, see **4.6.4 Operation of ports that alternately function as SEGxx pins**.

Using a port pin which is multiplexed with a timer output pin function (e.g. P52/TI02/TO02, P05/TI06/TO06) for timer output requires setting the corresponding bits in the port mode register (PMxx) and port register (Pxx) to 0.

Example When P05/TO06/TI06 is to be used for timer output
Set the PM05 bit of port mode register 0 to 0.
Set the P05 bit of port register 0 to 0.

Using a port pin which is multiplexed with a timer input pin function (e.g. P52/TI02/TO02, P05/TI06/TO06) for timer input requires setting the corresponding bit in the port mode register (PMxx) to 1. At this time, the value of the corresponding bit in the port register (Pxx) may be 0 or 1.

Example When P05/TO06/TI06 is to be used for timer input
Set the PM05 bit of port mode register 0 to 1.
Set the P05 bit of port register 0 to 0 or 1.

Remark 1. When using a port pin which is multiplexed with an analog input pin function for timer I/O, be sure to set the corresponding bit of the port mode control register (PMCxx) which switches between digital I/O and analog input to “0”.
Remark 2. When using a port pin which is multiplexed with a segment output pin function for timer I/O, be sure to clear the corresponding bit of LCD port function registers 0 to 4 (PFSEG0 to PFSEG4) to “0”.
Remark 3. When using the P125/(TI06)/(TO06)/V_{L3} pin for timer I/O, be sure to set the ISCVL3 bit of the LCD Input switch control register (ISCLCD) to “1”.
Remark 4. When using the P126/(TI05)/(TO05)/CAPL and P127/(TI04)/(TO04)/CAPH pins for timer I/O, be sure to set the ISCCAP bit of the LCD Input switch control register (ISCLCD) to “1”.

6.4 Basic Rules of Timer Array Unit

6.4.1 Basic rules of simultaneous channel operation function

When simultaneously using multiple channels, namely, a combination of a master channel (a reference timer mainly counting the cycle) and slave channels (timers operating according to the master channel), the following rules apply.

(1) Only an even channel (channel 0, 2, 4, etc.) can be set as a master channel.
(2) Any channel, except channel 0, can be set as a slave channel.
(3) The slave channel must be lower than the master channel.
Example If channel 2 is set as a master channel, channel 3 or those that follow (channels 3, 4, 5, etc.) can be set as a slave channel.

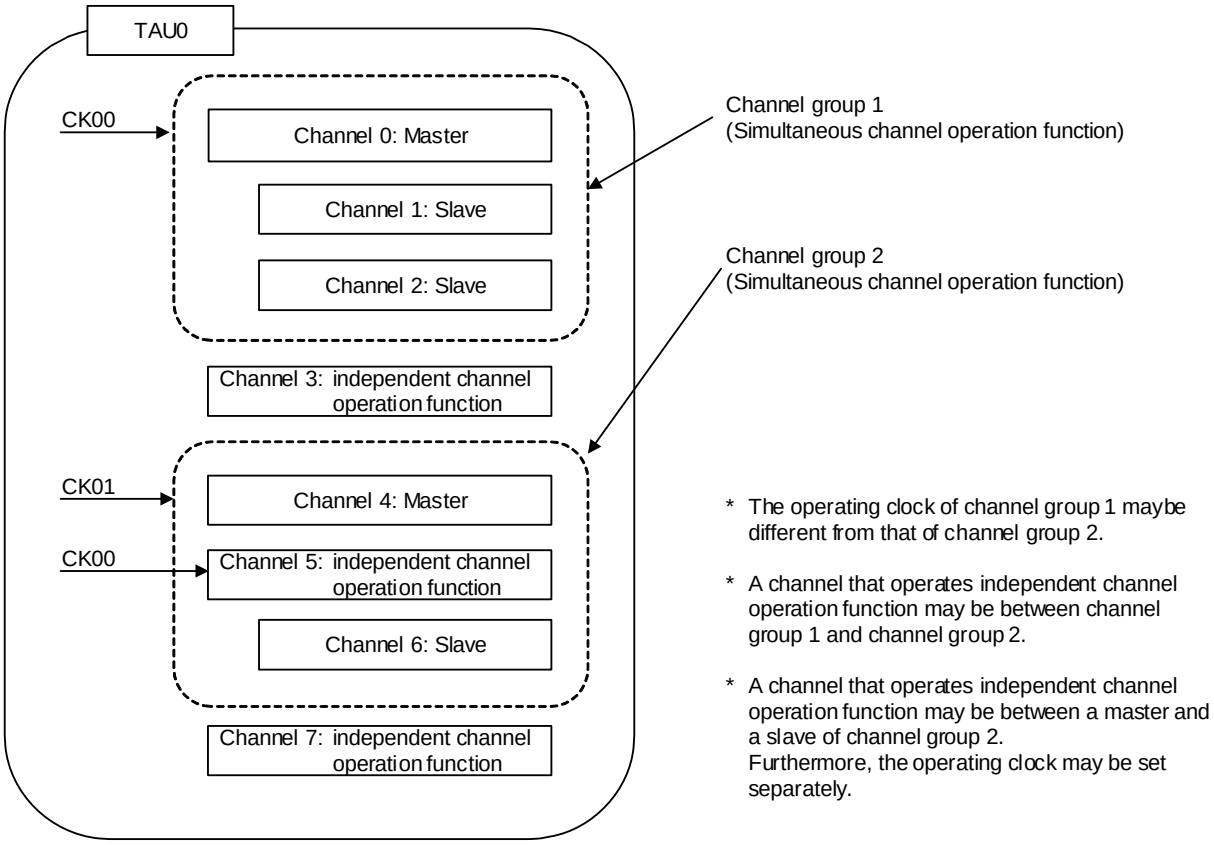
(4) Two or more slave channels can be set for one master channel.
(5) When two or more master channels are to be used, slave channels with a master channel between them may not be set.
Example If channels 0 and 4 are set as master channels, channels 1 to 3 can be set as the slave channels of master channel 0. Channels 5 to 7 cannot be set as the slave channels of master channel 0.

(6) The operating clock for a slave channel in combination with a master channel must be the same as that of the master channel. The CKSmn0, CKSmn1 bits (bit 15, 14 of timer mode register mn (TMRmn)) of the slave channel that operates in combination with the master channel must be the same value as that of the master channel.
(7) A master channel can transmit INTTMmn (interrupt), start software trigger, and count clock to the lower channels.
(8) A slave channel can use INTTMmn (interrupt), a start software trigger, or the count clock of the master channel as a source clock, but cannot transmit its own INTTMmn (interrupt), start software trigger, or count clock to channels with lower channel numbers.
(9) A master channel cannot use INTTMmn (interrupt), a start software trigger, or the count clock from the other higher master channel as a source clock.
(10) To simultaneously start channels that operate in combination, the channel start trigger bit (TSmn) of the channels in combination must be set at the same time.
(11) During the counting operation, a TSmn bit of a master channel or TSmn bits of all channels which are operating simultaneously can be set. It cannot be applied to TSmn bits of slave channels alone.
(12) To stop the channels in combination simultaneously, the channel stop trigger bit (TTmn) of the channels in combination must be set at the same time.
(13) CKm2/CKm3 cannot be selected while channels are operating simultaneously, because the operating clocks of master channels and slave channels have to be synchronized.
(14) Timer mode register m0 (TMRm0) has no master bit (it is fixed as “0”). However, as channel 0 is the highest channel, it can be used as a master channel during simultaneous operation.

The rules of the simultaneous channel operation function are applied in a channel group (a master channel and slave channels forming one simultaneous channel operation function).
If two or more channel groups that do not operate in combination are specified, the basic rules of the simultaneous channel operation function in **6.4.1 Basic rules of simultaneous channel operation function** do not apply to the channel groups.

Remark m: Unit number (m = 0), n: Channel number (n = 0 to 7)

Example



6.4.2 Basic rules of 8-bit timer operation function (channels 1 and 3 only)

The 8-bit timer operation function makes it possible to use a 16-bit timer channel in a configuration consisting of two 8-bit timer channels.
This function can only be used for channels 1 and 3, and there are several rules for using it.
The basic rules for this function are as follows:

(1) The 8-bit timer operation function applies only to channels 1 and 3.
(2) When using 8-bit timers, set the SPLIT bit of timer mode register mn (TMRmn) to 1.
(3) The higher 8 bits can be operated as the interval timer function.
(4) At the start of operation, the higher 8 bits output INTTMm1H/INTTMm3H (an interrupt) (which is the same operation performed when MDmn0 is set to 1).
(5) The operation clock of the higher 8 bits is selected according to the CKSmn1 and CKSmn0 bits of the lower-bit TMRmn register.
(6) For the higher 8 bits, the TSHm1/TSHm3 bit is manipulated to start channel operation and the TTHm1/TTHm3 bit is manipulated to stop channel operation. The channel status can be checked using the TEHm1/TEHm3 bit.
(7) The lower 8 bits operate according to the TMRmn register settings. The following three functions support operation of the lower 8 bits:
  • Interval timer function
  • External event counter function
  • Delay count function

(8) For the lower 8 bits, the TSm1/TSm3 bit is manipulated to start channel operation and the TTm1/TTm3 bit is manipulated to stop channel operation. The channel status can be checked using the TEm1/TEm3 bit.
(9) During 16-bit operation, manipulating the TSHm1, TSHm3, TTHm1, and TTHm3 bits is invalid. The TSm1, TSm3, TTm1, and TTm3 bits are manipulated to operate channels 1 and 3. The TEHm3 and TEHm1 bits are not changed.
(10) For the 8-bit timer function, the simultaneous operation functions (one-shot pulse, PWM, and multiple PWM) cannot be used.

Remark m: Unit number (m = 0), n: Channel number (n = 1, 3)

6.5 Operation of Counter

6.5.1 Count clock (f_{TCLK})

The count clock (f_{TCLK}) of the timer array unit can be selected between following by CCSmn bit of timer mode register mn (TMRmn).

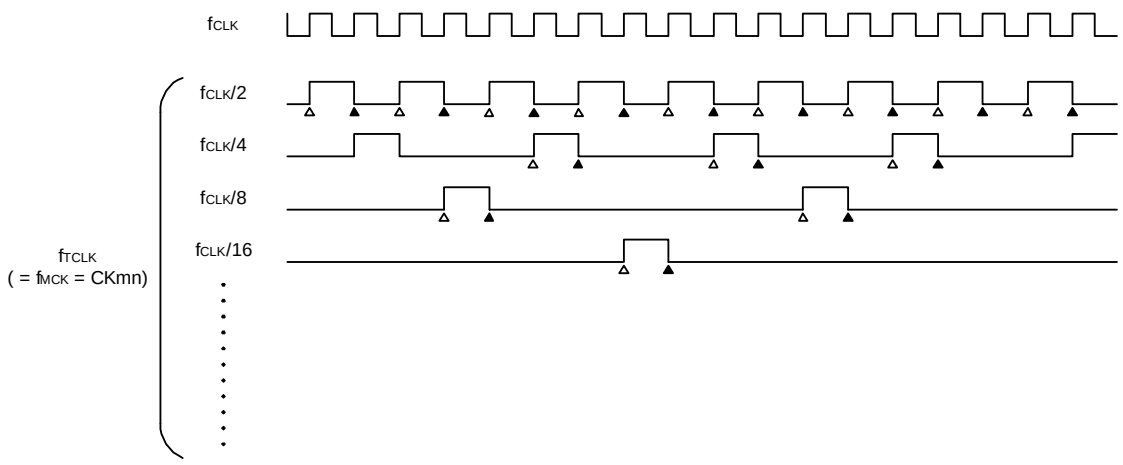
- Operation clock (f_{MCK}) specified by the CKSmn0 and CKSmn1 bits
- Valid edge of input signal input from the TImn pin

Because the timer array unit is designed to operate in synchronization with f_{CLK}, the timings of the count clock (f_{TCLK}) are shown below.

(1) When operation clock (f_{MCK}) specified by the CKSmn0 and CKSmn1 bits is selected (CCSmn = 0)

The count clock (f_{TCLK}) is between f_{CLK} to f_{CLK} /2^{15} by setting of timer clock select register m (TPSm). When a divided f_{CLK} is selected, however, the clock selected in TPSmn register, but a signal which becomes high level for one period of f_{CLK} from its rising edge. When a f_{CLK} is selected, fixed to high level. Counting of timer count register mn (TCRmn) delayed by one period of f_{CLK} from rising edge of the count clock, because of synchronization with f_{CLK}. But, this is described as “counting at rising edge of the count clock”, as a matter of convenience.

Figure 6 - 28 Timing of f_{CLK} and count clock (f_{TCLK}) (When CCSmn = 0)



Remark 1. △ : Rising edge of the count clock
▲ : Synchronization, increment/decrement of counter

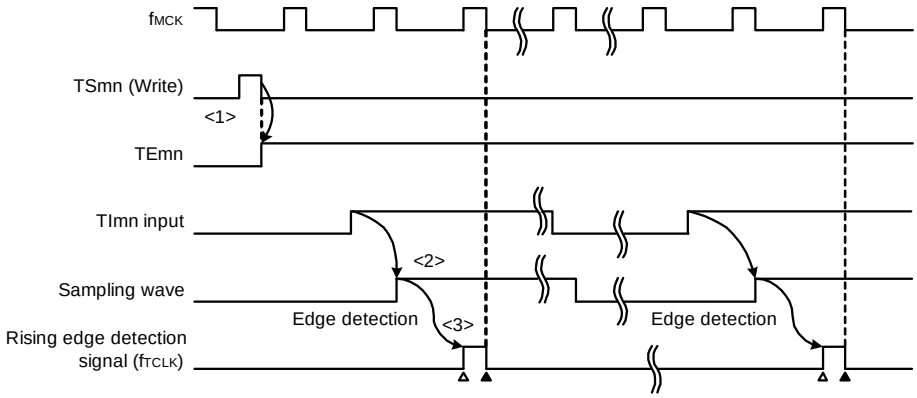
Remark 2. f_{CLK}: CPU/peripheral hardware clock

(2) When valid edge of input signal via the TImn pin is selected (CCSmn = 1)

The count clock (f_{TCLK}) becomes the signal that detects valid edge of input signal via the TImn pin and synchronizes next rising f_{MCK}. The count clock (f_{TCLK}) is delayed for 1 to 2 periods of f_{MCK} from the input signal via the TImn pin (when a noise filter is used, the delay becomes 3 to 4 clocks).

Counting of timer count register mn (TCRmn) delayed by one period of f_{CLK} from rising edge of the count clock, because of synchronization with f_{CLK}. But, this is described as “counting at valid edge of input signal via the TImn pin”, as a matter of convenience.

Figure 6 - 29 Timing of f_{CLK} and count clock (f_{TCLK}) (When CCSmn = 1, noise filter unused)



<1> Setting TSmn bit to 1 enables the timer to be started and to become wait state for valid edge of input signal via the TImn pin.
<2> The rise of input signal via the TImn pin is sampled by f_{MCK}.
<3> The edge is detected by the rising of the sampled signal and the detection signal (count clock) is output.

Remark 1. △ : Rising edge of the count clock
▲ : Synchronization, increment/decrement of counter

Remark 2. f_{CLK}: CPU/peripheral hardware clock
f_{MCK}: Operation clock of channel n

Remark 3. The waveform of the input signal via TImn pin of the input pulse interval measurement, the measurement of high/low width of input signal, and the delay counter, and the one-shot pulse output are the same as that shown in Figure 6 - 29.

6.5.2 Start timing of counter

Timer count register mn (TCRmn) becomes enabled to operation by setting of TSmn bit of timer channel start register m (TSm).

Operations from count operation enabled state to timer count Register mn (TCRmn) count start is shown in Table 6 - 6.

Table 6 - 6 Operations from Count Operation Enabled State to Timer count Register mn (TCRmn) Count Start

Timer operation mode	Operation when TSmn = 1 is set
• Interval timer mode	No operation is carried out from start trigger detection (TSmn = 1) until count clock generation. The first count clock loads the value of the TDRmn register to the TCRmn register and the subsequent count clock performs count down operation (see **6.5.3 (1) Operation of interval timer mode**).
• Event counter mode	Writing 1 to the TSmn bit loads the value of the TDRmn register to the TCRmn register. If detect edge of TImn input. The subsequent count clock performs count down operation. (see **6.5.3 (2) Operation of event counter mode**).
• Capture mode	No operation is carried out from start trigger detection (TSmn = 1) until count clock generation. The first count clock loads 0000H to the TCRmn register and the subsequent count clock performs count up operation (see **6.5.3 (3) Operation of capture mode (input pulse interval measurement)**).
• One-count mode	The waiting-for-start-trigger state is entered by writing 1 to the TSmn bit while the timer is stopped (TEmn = 0). No operation is carried out from start trigger detection until count clock generation. The first count clock loads the value of the TDRmn register to the TCRmn register and the subsequent count clock performs count down operation (see **6.5.3 (4) Operation of one-count mode**).
• Capture & one-count mode	The waiting-for-start-trigger state is entered by writing 1 to the TSmn bit while the timer is stopped (TEmn = 0). No operation is carried out from start trigger detection until count clock generation. The first count clock loads 0000H to the TCRmn register and the subsequent count clock performs count up operation (see **6.5.3 (5) Start timing in capture & one-count mode (when high-level width is measured)**).

6.5.3 Operation of counter

Here, the counter operation in each mode is explained.

(1) Operation of interval timer mode

<1> Operation is enabled (TEmn = 1) by writing 1 to the TSmn bit. Timer count register mn (TCRmn) holds the initial value until count clock generation.

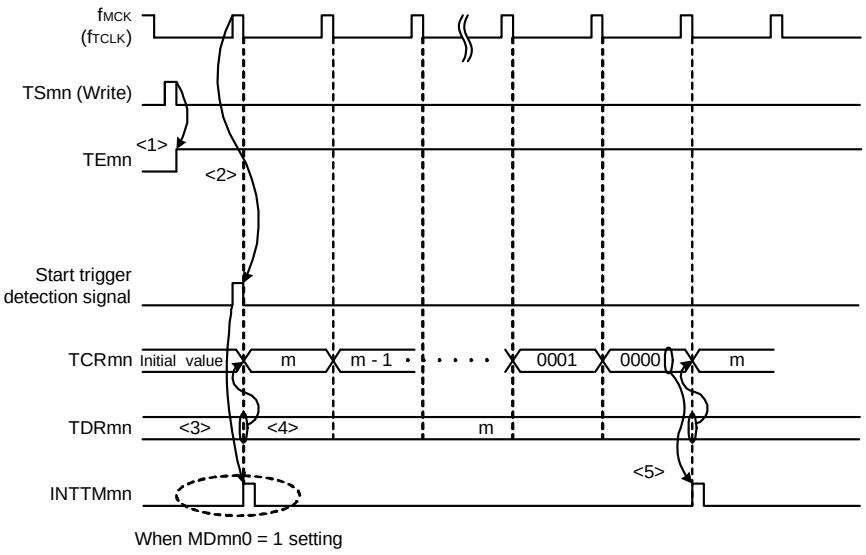
<2> A start trigger is generated at the first count clock after operation is enabled.

<3> When the MDmn0 bit is set to 1, INTTMmn is generated by the start trigger.

<4> By the first count clock after the operation enable, the value of timer data register mn (TDRmn) is loaded to the TCRmn register and counting starts in the interval timer mode.

<5> When the TCRmn register counts down and its count value is 0000H, INTTMmn is generated and the value of timer data register mn (TDRmn) is loaded to the TCRmn register and counting keeps on.

Figure 6 - 30 Operation Timing (In Interval Timer Mode)



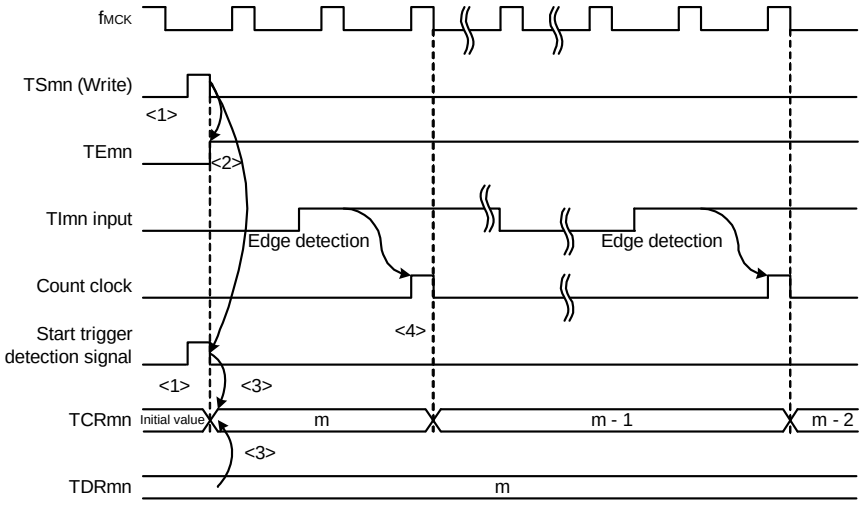
Caution **In the first cycle operation of count clock after writing the TSmn bit, an error at a maximum of one clock is generated since count start delays until count clock has been generated. When the information on count start timing is necessary, an interrupt can be generated at count start by setting MDmn0 = 1.**

Remark fMCK, the start trigger detection signal, and INTTMmn become active between one clock in synchronization with fCLK.

(2) Operation of event counter mode

<1> Timer count register mn (TCRmn) holds its initial value while operation is stopped (TEmn = 0).
<2> Operation is enabled (TEmn = 1) by writing 1 to the TSmn bit.
<3> As soon as 1 has been written to the TSmn bit and 1 has been set to the TEmn bit, the value of timer data register mn (TDRmn) is loaded to the TCRmn register to start counting.
<4> After that, the TCRmn register value is counted down according to the count clock of the valid edge of the TImn input.

Figure 6 - 31 Operation Timing (In Event Counter Mode)

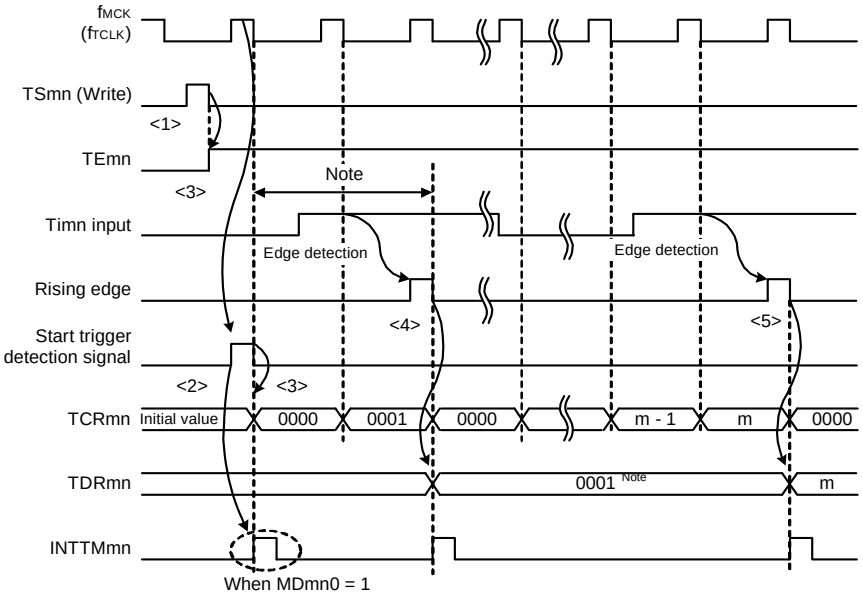


Remark The above figure shows the timing when the noise filter is not used. By making the noise filter on-state, the edge detection becomes 2 fMCK cycles (it sums up to 3 to 4 cycles) later than the normal cycle of TImn input. The error per one period occurs be the asynchronous between the period of the TImn input and that of the count clock (fMCK).

(3) Operation of capture mode (input pulse interval measurement)

<1> Operation is enabled (TEmn = 1) by writing 1 to the TSmn bit.
<2> Timer count register mn (TCRmn) holds the initial value until count clock generation.
<3> A start trigger is generated at the first count clock after operation is enabled. And the value of 0000H is loaded to the TCRmn register and counting starts in the capture mode. (When the MDmn0 bit is set to 1, INTTMmn is generated by the start trigger.)
<4> On detection of the valid edge of the TImn input, the value of the TCRmn register is captured to timer data register mn (TDRmn) and INTTMmn is generated. However, this capture value is no meaning. The TCRmn register keeps on counting from 0000H.
<5> On next detection of the valid edge of the TImn input, the value of the TCRmn register is captured to timer data register mn (TDRmn) and INTTMmn is generated.

Figure 6 - 32 Operation Timing (In Capture Mode: Input Pulse Interval Measurement)



Note If a clock has been input to TImn (the trigger exists) when capturing starts, counting starts when a trigger is detected, even if no edge is detected. Therefore, the first captured value (<4>) does not determine a pulse interval (in the above figure, 0001 just indicates two clock cycles but does not determine the pulse interval) and so the user can ignore it.

Caution In the first cycle operation of count clock after writing the TSmn bit, an error at a maximum of one clock is generated since count start delays until count clock has been generated. When the information on count start timing is necessary, an interrupt can be generated at count start by setting MDmn0 = 1.

Remark The above figure shows the timing when the noise filter is not used. By making the noise filter on-state, the edge detection becomes 2 fMCK cycles (it sums up to 3 to 4 cycles) later than the normal cycle of TImn input. The error per one period occurs be the asynchronous between the period of the TImn input and that of the count clock (fMCK).

(4) Operation of one-count mode

<1> Operation is enabled (TEmn = 1) by writing 1 to the TSmn bit.

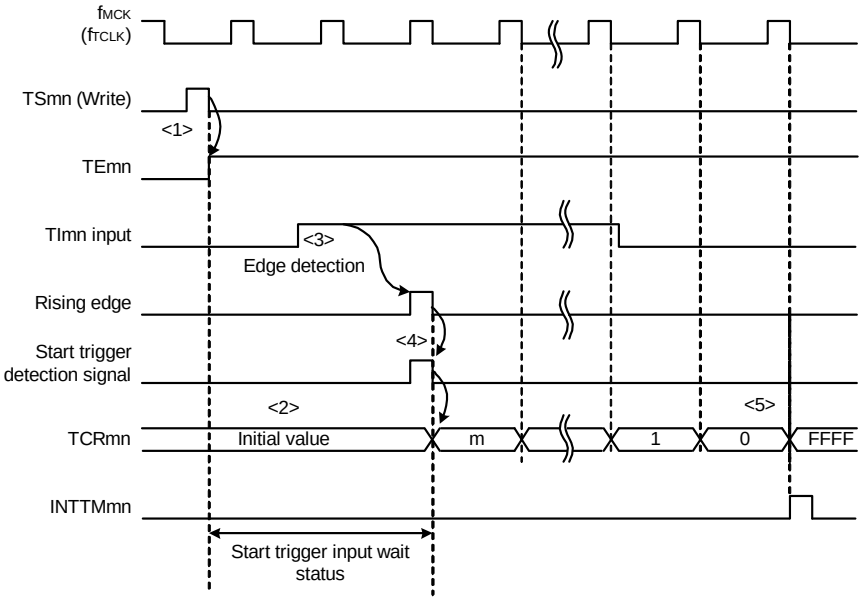
<2> Timer count register mn (TCRmn) holds the initial value until start trigger generation.

<3> Rising edge of the TImn input is detected.

<4> On start trigger detection, the value of timer data register mn (TDRmn) is loaded to the TCRmn register and count starts.

<5> When the TCRmn register counts down and its count value is 0000H, INTTMmn is generated and the value of the TCRmn register becomes FFFFH and counting stops.

Figure 6 - 33 Operation Timing (In One-count Mode)



Remark The above figure shows the timing when the noise filter is not used. By making the noise filter on-state, the edge detection becomes 2 fMCK cycles (it sums up to 3 to 4 cycles) later than the normal cycle of TImn input. The error per one period occurs be the asynchronous between the period of the TImn input and that of the count clock (fMCK).

(5) Start timing in capture & one-count mode (when high-level width is measured)

<1> Operation is enabled (TEmn = 1) by writing 1 to the TSmn bit of timer channel start register m (TSm).

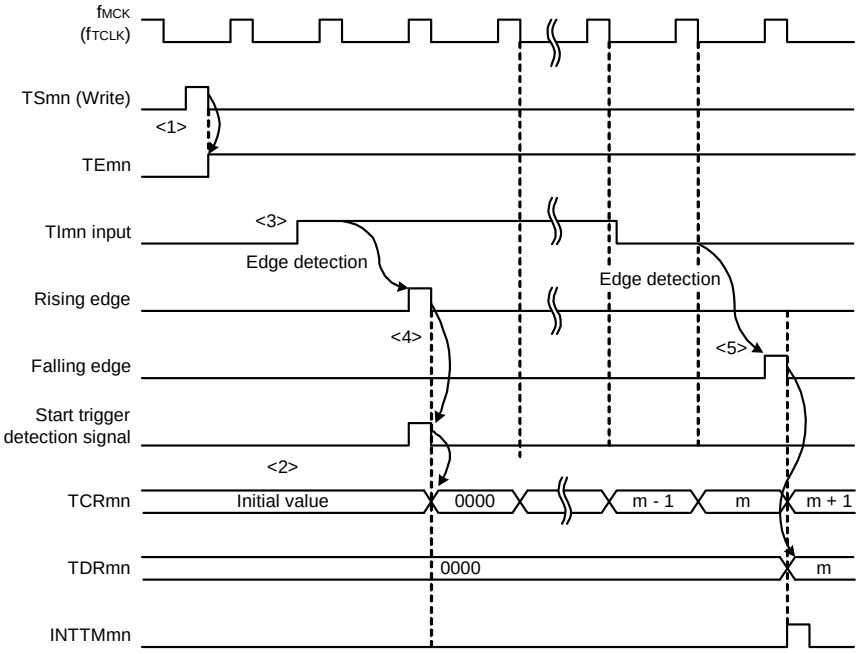
<2> Timer count register mn (TCRmn) holds the initial value until start trigger generation.

<3> Rising edge of the TImn input is detected.

<4> On start trigger detection, the value of 0000H is loaded to the TCRmn register and count starts.

<5> On detection of the falling edge of the TImn input, the value of the TCRmn register is captured to timer data register mn (TDRmn) and INTTMmn is generated.

Figure 6 - 34 Operation Timing (In Capture & One-count Mode: High-level Width Measurement)

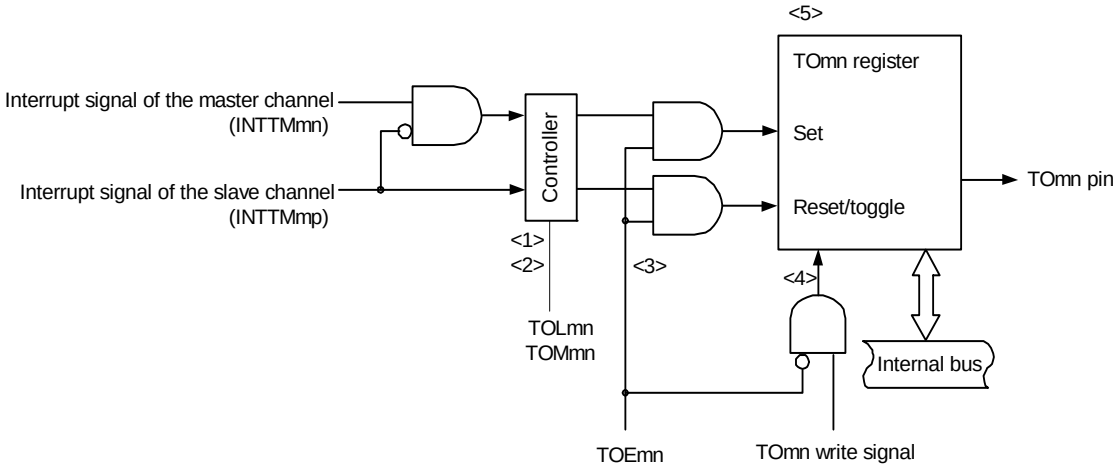


Remark The above figure shows the timing when the noise filter is not used. By making the noise filter on-state, the edge detection becomes 2 fMCK cycles (it sums up to 3 to 4 cycles) later than the normal cycle of TImn input. The error per one period occurs be the asynchronous between the period of the TImn input and that of the count clock (fMCK).

6.6 Channel Output (TOmn pin) Control

6.6.1 TOmn pin output circuit configuration

Figure 6 - 35 Output Circuit Configuration



The following describes the TOmn pin output circuit.

<1> When TOMmn = 0 (master channel output mode), the set value of timer output level register m (TOLm) is ignored and only INTTM0p (slave channel timer interrupt) is transmitted to timer output register m (TOm).

<2> When TOMmn = 1 (slave channel output mode), both INTTMmn (master channel timer interrupt) and INTTM0p (slave channel timer interrupt) are transmitted to the TOm register.
At this time, the TOLm register becomes valid and the signals are controlled as follows:

When TOLmn = 0: Positive logic output (INTTMmn → set, INTTM0p → reset)
When TOLmn = 1: Negative logic output (INTTMmn → reset, INTTM0p → set)

When INTTMmn and INTTM0p are simultaneously generated, (0% output of PWM), INTTM0p (reset signal) takes priority, and INTTMmn (set signal) is masked.

<3> While timer output is enabled (TOEmn = 1), INTTMmn (master channel timer interrupt) and INTTM0p (slave channel timer interrupt) are transmitted to the TOm register. Writing to the TOm register (TOmn write signal) becomes invalid.
When TOEmn = 1, the TOmn pin output never changes with signals other than interrupt signals.
To initialize the TOmn pin output level, it is necessary to set timer operation is stopped (TOEmn = 0) and to write a value to the TOm register.

<4> While timer output is disabled (TOEmn = 0), writing to the TOmn bit to the target channel (TOmn write signal) becomes valid. When timer output is disabled (TOEmn = 0), neither INTTMmn (master channel timer interrupt) nor INTTM0p (slave channel timer interrupt) is transmitted to the TOm register.

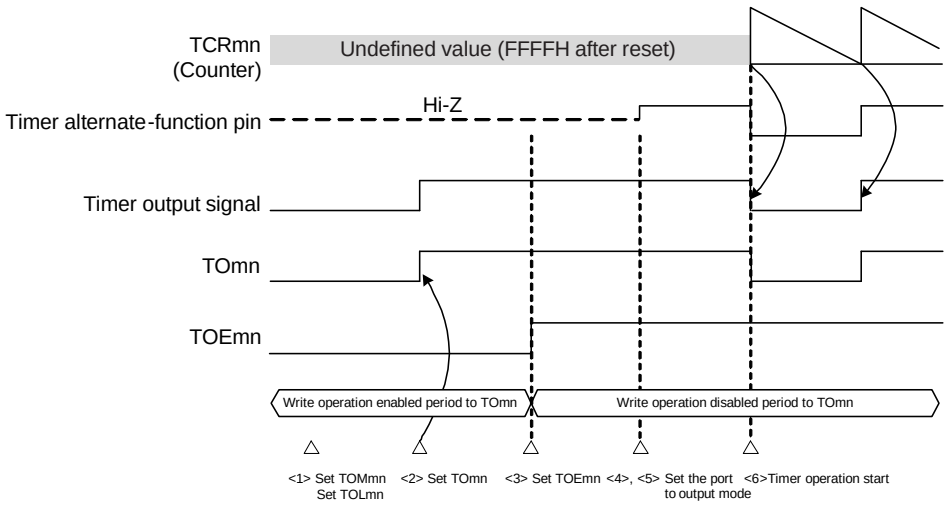
<5> The TOm register can always be read, and the TOmn pin output level can be checked.

Remark m: Unit number (m = 0)
n: Channel number
n = 0 to 7 (n = 0, 2, 4, 6 for master channel)
p: Slave channel number
$n < p \leq 7$

6.6.2 TOmn Pin Output Setting

The following figure shows the procedure and status transition of the TOmn output pin from initial setting to timer operation start.

Figure 6 - 36 Status Transition from Timer Output Setting to Operation Start



<1> The operation mode of timer output is set.

- TOMmn bit (0: Master channel output mode, 1: Slave channel output mode)
- TOLmn bit (0: Positive logic output, 1: Negative logic output)

<2> The timer output signal is set to the initial status by setting timer output register m (TOm).

<3> The timer output operation is enabled by writing 1 to the TOEmn bit (writing to the TOm register is disabled).

<4> The port is set to digital I/O by port mode control register (PMCxx).

<5> The port I/O setting is set to output (see **6.3.15 Registers that control port functions of timer input/output pins**).

<6> The timer operation is enabled (TSmn = 1).

Remark m: Unit number (m = 0), n: Channel number (n = 0 to 7)

6.6.3 Cautions on Channel Output Operation

(1) Changing values set in the registers TOm, TOEm, and TOLm during timer operation

Since the timer operations (operations of timer count register mn (TCRmn) and timer data register mn (TDRmn)) are independent of the TOmn output circuit and changing the values set in timer output register m (TOm), timer output enable register m (TOEm), and timer output level register m (TOLm) does not affect the timer operation, the values can be changed during timer operation. To output an expected waveform from the TOmn pin by timer operation, however, set the TOm, TOEm, TOLm, and TOMm registers to the values stated in the register setting example of each operation shown by 6.8 and 6.9

When the values set to the TOEm, and TOMm registers (but not the TOm register) are changed close to the occurrence of the timer interrupt (INTTMmn) of each channel, the waveform output to the TOmn pin might differ, depending on whether the values are changed immediately before or immediately after the timer interrupt (INTTMmn) occurs.

Remark m: Unit number (m = 0), n: Channel number (n = 0 to 7)

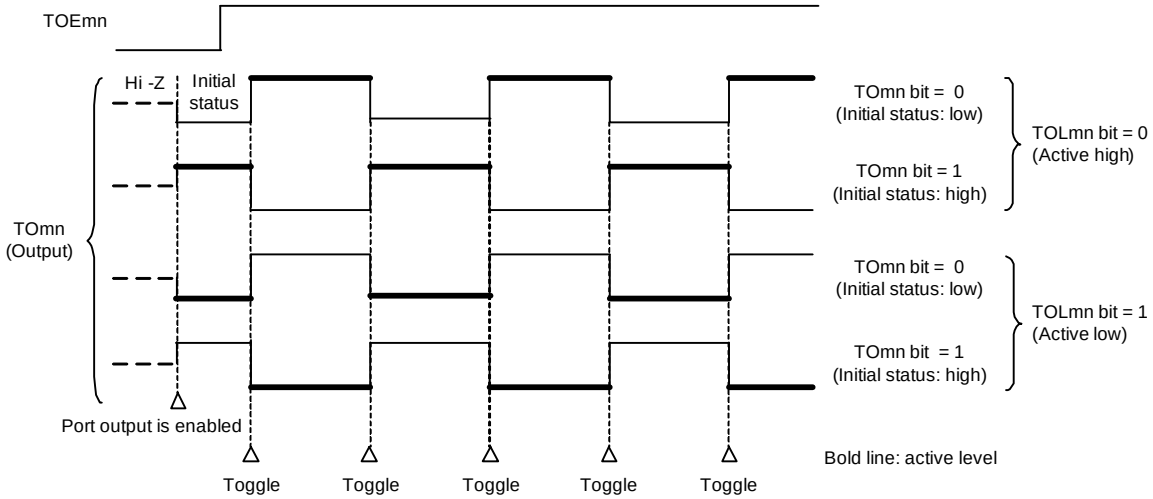
(2) Default level of TOmn pin and output level after timer operation start

The change in the output level of the TOmn pin when timer output register m (TOm) is written while timer output is disabled (TOEmn = 0), the initial level is changed, and then timer output is enabled (TOEmn = 1) before port output is enabled, is shown below.

(a) When operation starts with master channel output mode (TOMmn = 0) setting

The setting of timer output level register m (TOLm) is invalid when master channel output mode (TOMmn = 0). When the timer operation starts after setting the default level, the toggle signal is generated and the output level of the TOmn pin is reversed.

Figure 6 - 37 TOmn Pin Output Status at Toggle Output (TOMmn = 0)

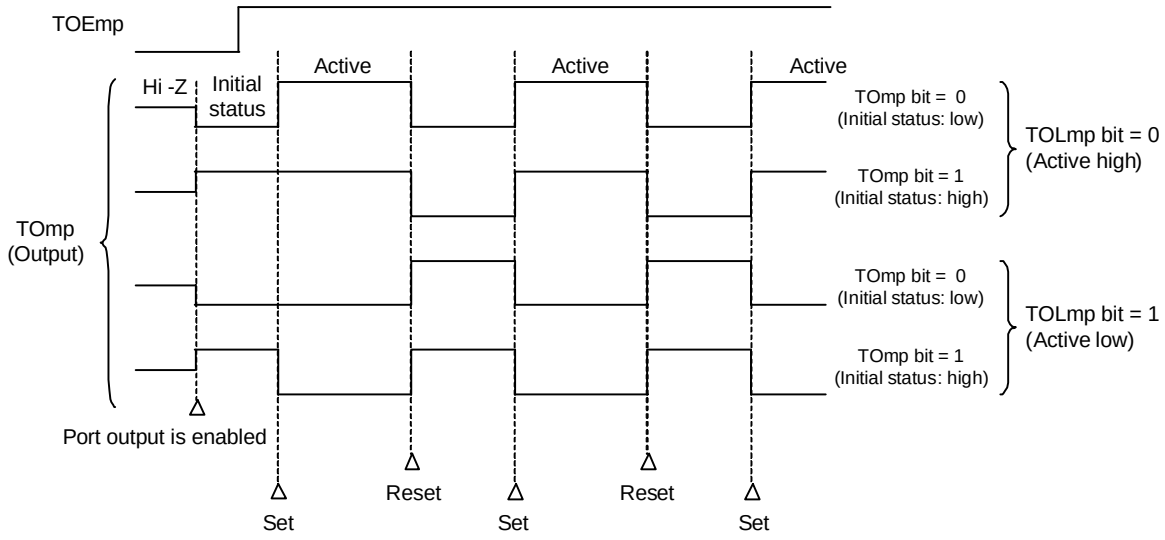


Remark 1. Toggle: Reverse TOmn pin output status

Remark 2. m: Unit number (m = 0), n: Channel number (n = 0 to 7)

(b) When operation starts with slave channel output mode (TOMmp = 1) setting (PWM output))
When slave channel output mode (TOMmp = 1), the active level is determined by timer output level register m (TOLm) setting.

Figure 6 - 38 TOmp Pin Output Status at PWM Output (TOMmp = 1)



Remark 1. Set: The output signal of the TOmp pin changes from inactive level to active level.
Reset: The output signal of the TOmp pin changes from active level to inactive level.

Remark 2. m: Unit number (m = 0), p: Channel number (p = 1 to 7)

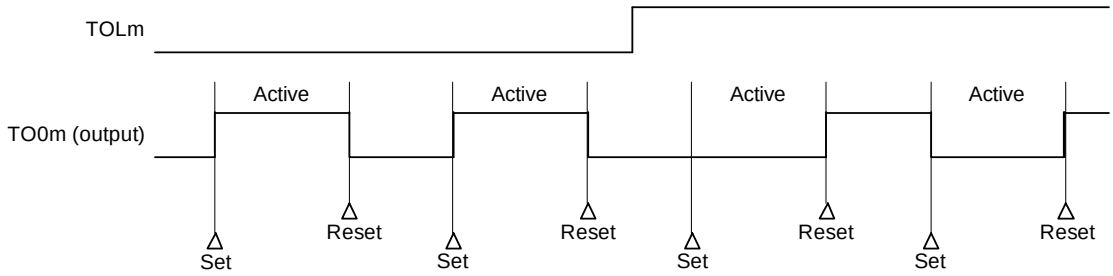
(3) Operation of TOmn pin in slave channel output mode (TOMmn = 1)

(a) When timer output level register m (TOLm) setting has been changed during timer operation

When the TOLm register setting has been changed during timer operation, the setting becomes valid at the generation timing of the TOmn pin change condition. Rewriting the TOLm register does not change the output level of the TOmn pin.

The operation when TOMmn is set to 1 and the value of the TOLm register is changed while the timer is operating (TEmn = 1) is shown below.

Figure 6 - 39 Operation when TOLm Register Has Been Changed Contents during Timer Operation



Remark 1. Set: The output signal of the TOmn pin changes from inactive level to active level.
Reset: The output signal of the TOmn pin changes from active level to inactive level.

Remark 2. m: Unit number (m = 0), n: Channel number (n = 0 to 7)

(b) Set/reset timing

To realize 0%/100% output at PWM output, the TOmn pin/TOmn bit set timing at master channel timer interrupt (INTTMmn) generation is delayed by 1 count clock by the slave channel.

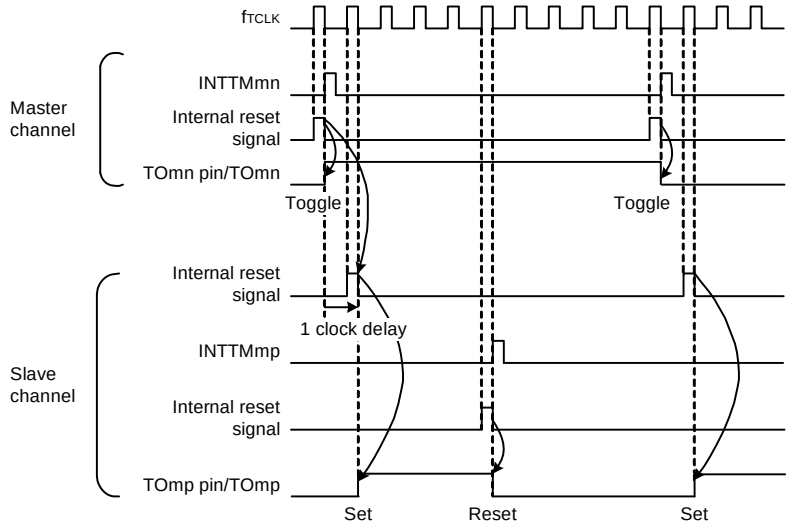
If the set condition and reset condition are generated at the same time, a higher priority is given to the latter.

Figure 6 - 40 shows the set/reset operating statuses where the master/slave channels are set as follows.

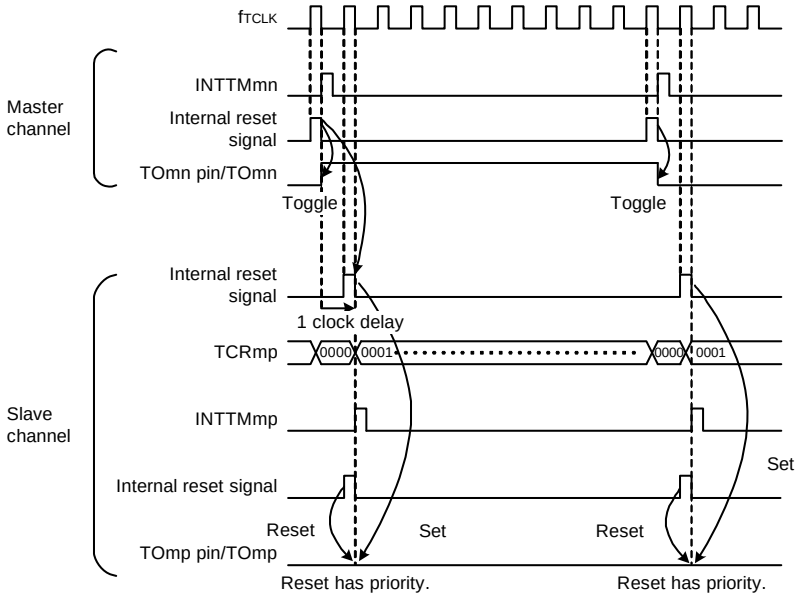
Master channel: TOEmn = 1, TOMmn = 0, TOLmn = 0
Slave channel: TOEmp = 1, TOMmp = 1, TOLmp = 0

Figure 6 - 40 Set/Reset Timing Operating Statuses

(1) Basic operation timing



(2) Operation timing when 0% duty



Remark 1. Internal reset signal: TOmn pin reset/toggle signal
Internal set signal: TOmn pin set signal

Remark 2. m: Unit number (m = 0)
n: Channel number
n = 0 to 7 (n = 0, 2, 4, 6 for master channel)
p: Slave channel number
n < p ≤ 7

6.6.4 Collective manipulation of TOmn bit

In timer output register m (TOm), the setting bits for all the channels are located in one register in the same way as timer channel start register m (TSm). Therefore, the TOmn bit of all the channels can be manipulated collectively.

Only the desired bits can also be manipulated by enabling writing only to the TOmn bits (TOEmn = 0) that correspond to the relevant bits of the channel used to perform output (TOmn).

Figure 6 - 41 Example of TO0n Bit Collective Manipulation

Before writing

									TO07	TO06	TO05	TO04	TO03	TO02	TO01	TO00
TO0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0
TOE0	0	0	0	0	0	0	0	0	TOE07	TOE06	TOE05	TOE04	TOE03	TOE02	TOE01	TOE00
									0	0	1	0	1	1	1	1

Data to be written

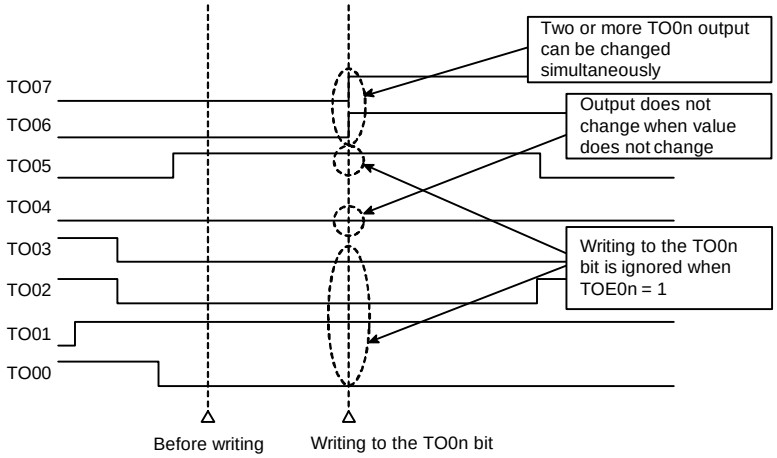
0	0	0	0	0	0	0	0	1	1	0	0	0	0	1	1

After writing

									TO07	TO06	TO05	TO04	TO03	TO02	TO01	TO00
TO0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	1	0

Writing is done only to the TOmn bit with TOEmn = 0, and writing to the TOmn bit with TOEmn = 1 is ignored. TOmn (channel output) to which TOEmn = 1 is set is not affected by the write operation. Even if the write operation is done to the TOmn bit, it is ignored and the output change by timer operation is normally done.

Figure 6 - 42 TO0n Pin Statuses by Collective Manipulation of TO0n Bit



Caution While timer output is enabled (TOEmn = 1), even if the output by timer interrupt of each timer (INTTMmn) contends with writing to the TOmn bit, output is normally done to the TOmn pin.

Remark m: Unit number (m = 0), n: Channel number (n = 0 to 7)

6.6.5 Timer Interrupt and TOmn Pin Output at Operation Start

In the interval timer mode or capture mode, the MDmn0 bit in timer mode register mn (TMRmn) sets whether or not to generate a timer interrupt at count start.

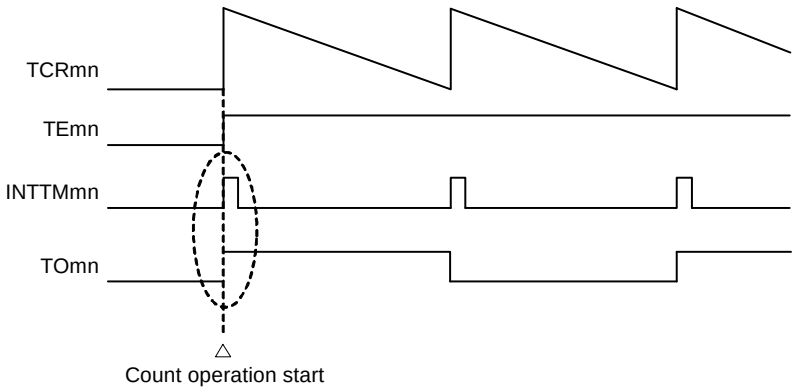
When MDmn0 is set to 1, the count operation start timing can be known by the timer interrupt (INTTMmn) generation.

In the other modes, neither timer interrupt at count operation start nor TOmn output is controlled.

Figure 6 - 43 shows operation examples when the interval timer mode (TOEmn = 1, TOMmn = 0) is set.

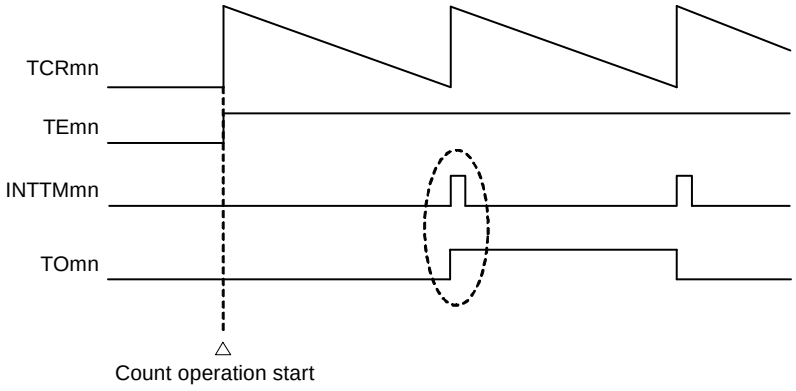
Figure 6 - 43 Operation examples of timer interrupt at count operation start and TOmn output

(a) When MDmn0 is set to 1



When MDmn0 is set to 1, a timer interrupt (INTTMmn) is output at count operation start, and TOmn performs a toggle operation.

(b) When MDmn0 is set to 0



When MDmn0 is set to 0, a timer interrupt (INTTMmn) is not output at count operation start, and TOmn does not change either. After counting one cycle, INTTMmn is output and TOmn performs a toggle operation.

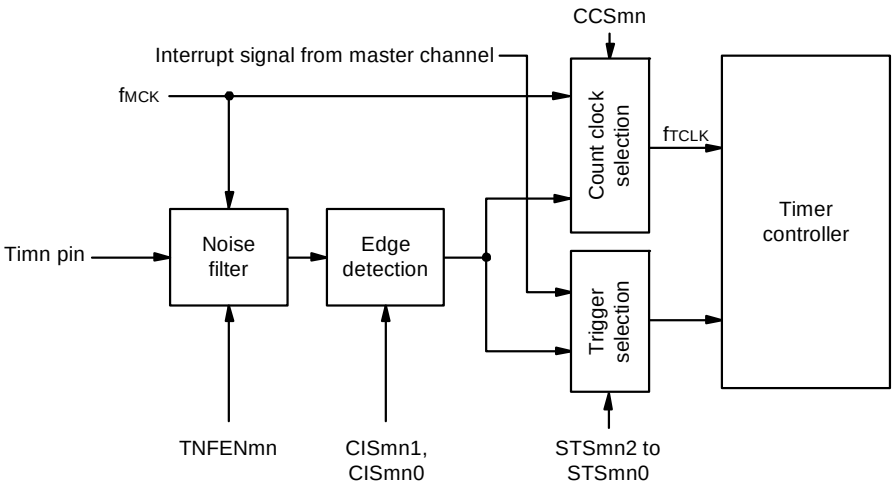
Remark m: Unit number (m = 0), n: Channel number (n = 0 to 7)

6.7 Timer Input (TImn) Control

6.7.1 TImn input circuit configuration

A signal is input from a timer input pin, goes through a noise filter and an edge detector, and is sent to a timer controller. Enable the noise filter for the pin in need of noise removal. The following shows the configuration of the input circuit.

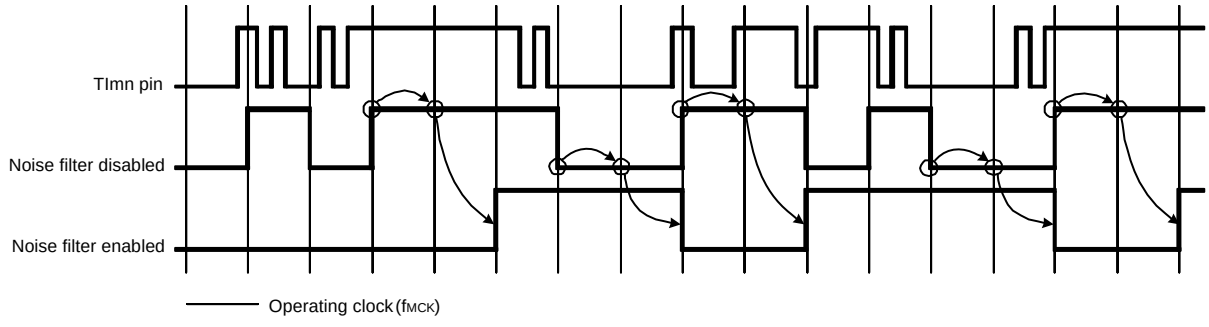
Figure 6 - 44 Input Circuit Configuration



6.7.2 Noise filter

When the noise filter is disabled, the input signal is only synchronized with the operating clock (fMCK) for channel n. When the noise filter is enabled, after synchronization with the operating clock (fMCK) for channel n, whether the signal keeps the same value for two clock cycles is detected. The following shows differences in waveforms output from the noise filter between when the noise filter is enabled and disabled.

Figure 6 - 45 Sampling Waveforms through TImn Input Pin with Noise Filter Enabled and Disabled



Caution The input waveforms to the TImn pin are shown to explain the operation when the noise filter is enabled or disabled. When actually inputting waveforms, input them according to the TImn input high-level and low-level widths listed in 38.4 or 39.4 AC Characteristics.

6.7.3 Cautions on channel input operation

When a timer input pin is set as unused, the operating clock is not supplied to the noise filter. Therefore, after settings are made to use the timer input pin, the following wait time is necessary before a trigger is specified to enable operation of the channel corresponding to the timer input pin.

(1) Noise filter is disabled

When bits 12 (CCSmn), 9 (STSmn1), and 8 (STSmn0) in the timer mode register mn (TMRmn) are 0 and then one of them is set to 1, wait for at least two cycles of the operating clock (f_{MCK}), and then set the operation enable trigger bit in the timer channel start register (TSm).

(2) Noise filter is enabled

When bits 12 (CCSmn), 9 (STSmn1), and 8 (STSmn0) in the timer mode register mn (TMRmn) are all 0 and then one of them is set to 1, wait for at least four cycles of the operating clock (f_{MCK}), and then set the operation enable trigger bit in the timer channel start register (TSm).

6.8 Independent Channel Operation Function of Timer Array Unit

6.8.1 Operation as interval timer/square wave output

(1) Interval timer

The timer array unit can be used as a reference timer that generates INTTMmn (timer interrupt) at fixed intervals.

The interrupt generation period can be calculated by the following expression.

Generation period of INTTMmn (timer interrupt) = Period of count clock × (Set value of TDRmn + 1)

(2) Operation as square wave output

TOmn performs a toggle operation as soon as INTTMmn has been generated, and outputs a square wave with a duty factor of 50%.

The period and frequency for outputting a square wave from TOmn can be calculated by the following expressions.

- Period of square wave output from TOmn = Period of count clock × (Set value of TDRmn + 1) × 2
- Frequency of square wave output from TOmn = Frequency of count clock/{(Set value of TDRmn + 1) × 2}

Timer count register mn (TCRmn) operates as a down counter in the interval timer mode.

The TCRmn register loads the value of timer data register mn (TDRmn) at the first count clock after the channel start trigger bit (TSmn, TSHm1, TSHm3) of timer channel start register m (TSm) is set to 1. If the MDmn0 bit of timer mode register mn (TMRmn) is 0 at this time, INTTMmn is not output and TOmn is not toggled. If the MDmn0 bit of the TMRmn register is 1, INTTMmn is output and TOmn is toggled.

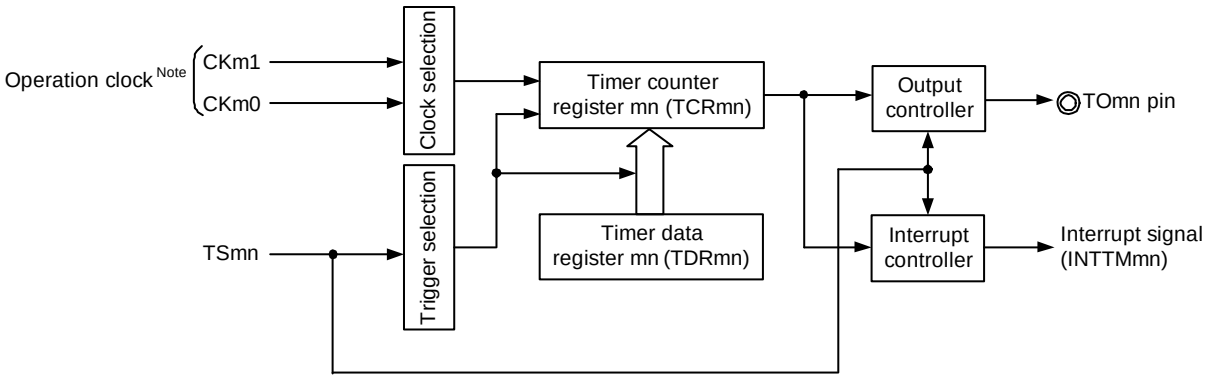
After that, the TCRmn register count down in synchronization with the count clock.

When TCRmn = 0000H, INTTMmn is output and TOmn is toggled at the next count clock. At the same time, the TCRmn register loads the value of the TDRmn register again. After that, the same operation is repeated.

The TDRmn register can be rewritten at any time. The new value of the TDRmn register becomes valid from the next period.

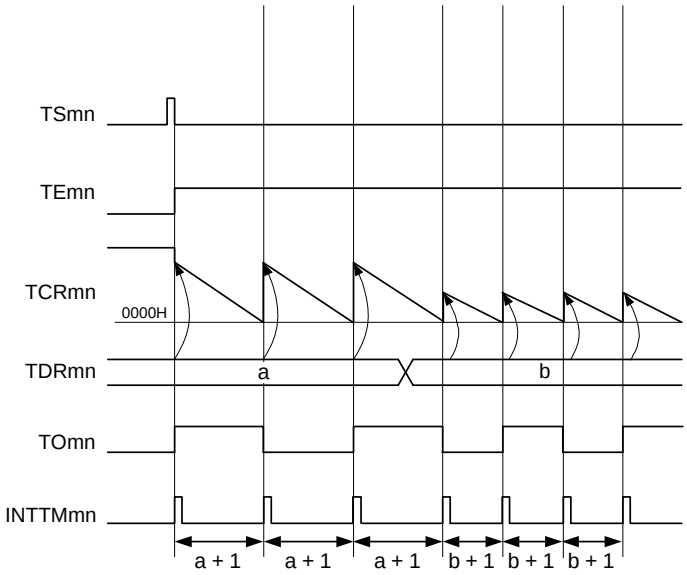
Remark m: Unit number (m = 0), n: Channel number (n = 0 to 7)

Figure 6 - 46 Block Diagram of Operation as Interval Timer/Square Wave Output



Note When channels 1 and 3, the clock can be selected from CKm0, CKm1, CKm2 and CKm3.

Figure 6 - 47 Example of Basic Timing of Operation as Interval Timer/Square Wave Output (MDmn0 = 1)

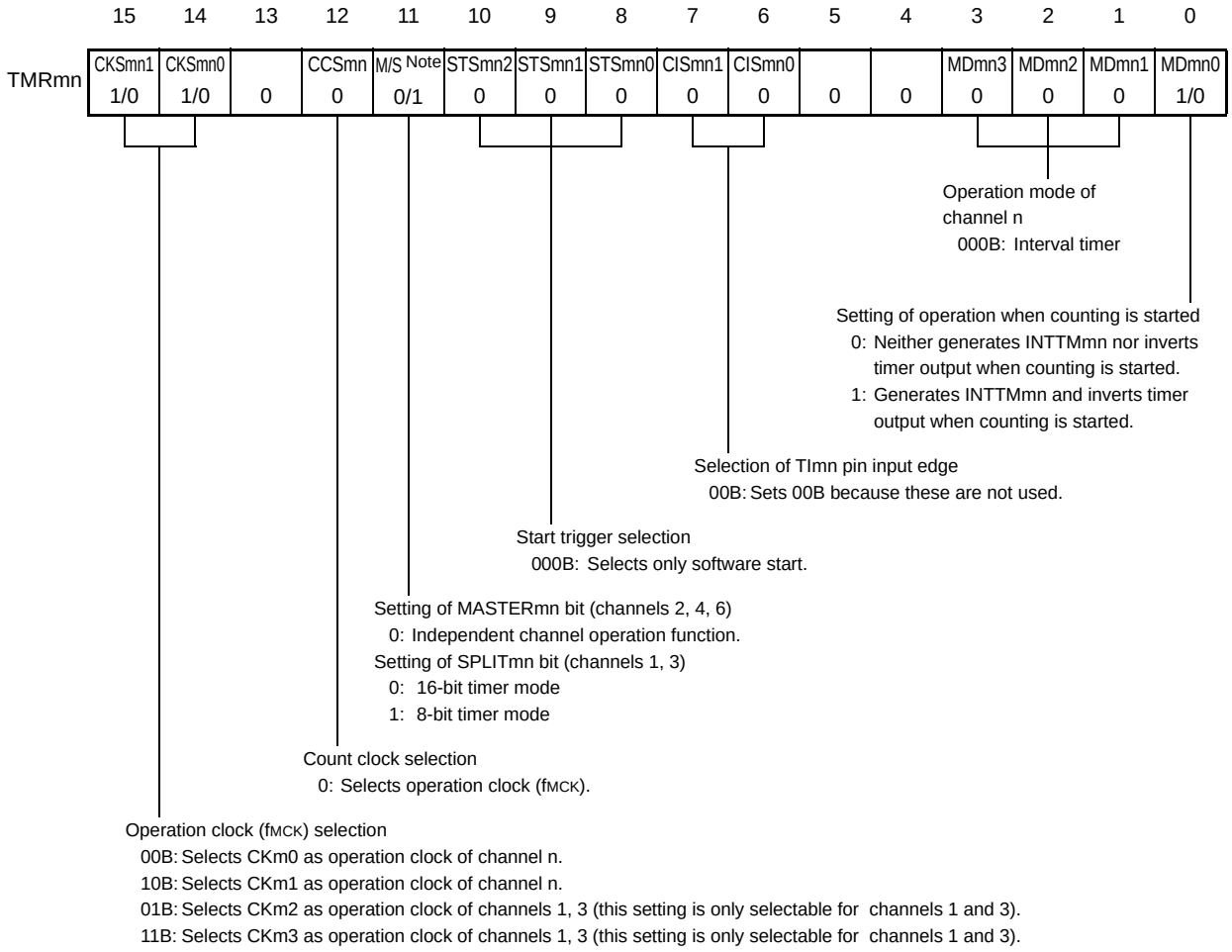


Remark 1. m: Unit number (m = 0), n: Channel number (n = 0 to 7)

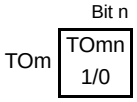
Remark 2. TSmn: Bit n of timer channel start register m (TSm)
TEmn: Bit n of timer channel enable status register m (TEm)
TCRmn: Timer count register mn (TCRmn)
TDRmn: Timer data register mn (TDRmn)
TOmn: TOmn pin output signal

Figure 6 - 48 Example of Set Contents of Registers During Operation as Interval Timer/Square Wave Output

(a) Timer mode register mn (TMRmn)

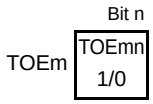


(b) Timer output register m (TOm)



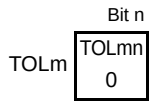
0: Outputs 0 from TOmn.
1: Outputs 1 from TOmn.

(c) Timer output enable register m (TOEm)



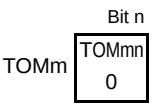
0: Stops the TOmn output operation by counting operation.
1: Enables the TOmn output operation by counting operation.

(d) Timer output level register m (TOLm)



0: Cleared to 0 when TOMmn = 0 (master channel output mode)

(e) Timer output mode register m (TOMm)



0: Sets master channel output mode.

Note TMRm2, TMRm4, TMRm6: MASTERmn bit
TMRm1, TMRm3: SPLITmn bit
TMRm0, TMRm5, TMRm7: Fixed to 0

Remark m: Unit number (m = 0), n: Channel number (n = 0 to 7)

Figure 6 - 49 Operation Procedure of Interval Timer/Square Wave Output Function (1/2)

	Software Operation	Hardware Status
TAU default setting		Power-off status (Clock supply is stopped and writing to each register is disabled.)
	Sets the TAUmEN bit of peripheral enable register 0 (PER0) to 1. →	Power-on status. Each channel stops operating. (Clock supply is started and writing to each register is enabled.)
	Sets timer clock select register m (TPSm). Determines clock frequencies of CKm0 to CKm3.	
Channel default setting	Sets timer mode register mn (TMRmn) (determines operation mode of channel). Sets interval (period) value to timer data register mn (TDRmn).	Channel stops operating. (Clock is supplied and some power is consumed.)
	To use the TOmn output Clears the TOMmn bit of timer output mode register m (TOMm) to 0 (master channel output mode). Clears the TOLmn bit to 0. Sets the TOmn bit and determines default level of the TOmn output. →	The TOmn pin goes into Hi-Z output state. The TOmn default setting level is output when the port mode register is in the output mode and the port register is 0.
	Sets the TOEmn bit to 1 and enables operation of TOmn. →	TOmn does not change because channel stops operating.
	Clears the port register and port mode register to 0. →	The TOmn pin outputs the TOmn set level.
Operation start	(Sets the TOEmn bit to 1 only if using TOmn output and resuming operation.). Sets the TSmn (TSHm1, TSHm3) bit to 1. → The TSmn (TSHm1, TSHm3) bit automatically returns to 0 because it is a trigger bit.	TEmn (TEHm1, TEHm3) = 1, and count operation starts. Value of the TDRmn register is loaded to timer count register mn (TCRmn). INTTMmn is generated and TOmn performs toggle operation if the MDmn0 bit of the TMRmn register is 1.
During operation	Set value of the TDRmn register can be changed. The TCRmn register can always be read. The TSRmn register is not used. Set values of the TOm and TOEm registers can be changed. Set values of the TMRmn register, TOMmn, and TOLmn bits cannot be changed.	Counter (TCRmn) counts down. When count value reaches 0000H, the value of the TDRmn register is loaded to the TCRmn register again and the count operation is continued. By detecting TCRmn = 0000H, INTTMmn is generated and TOmn performs toggle operation. After that, the above operation is repeated.
Operation stop	The TTmn (TTHm1, TTHm3) bit is set to 1. → The TTmn (TTHm1, TTHm3) bit automatically returns to 0 because it is a trigger bit.	TEmn (TEHm1, TEHm3), and count operation stops. The TCRmn register holds count value and stops. The TOmn output is not initialized but holds current status.
	The TOEmn bit is cleared to 0 and value is set to the TOmn bit. →	The TOmn pin outputs the TOmn bit set level.

Operation is resumed.

(**Remark** is listed on the next page.)

Figure 6 - 49 Operation Procedure of Interval Timer/Square Wave Output Function (2/2)

	Software Operation	Hardware Status
TAU stop	To hold the TOmn pin output level Clears the TOmn bit to 0 after the value to be held is set to the port register. →	The TOmn pin output level is held by port function.
	When holding the TOmn pin output level is not necessary Setting not required.	
	The TAUmEN bit of the PER0 register is cleared to 0. →	Power-off status All circuits are initialized and SFR of each channel is also initialized. (The TOmn bit is cleared to 0 and the TOmn pin is set to port mode.)

Remark m: Unit number (m = 0), n: Channel number (n = 0 to 7)

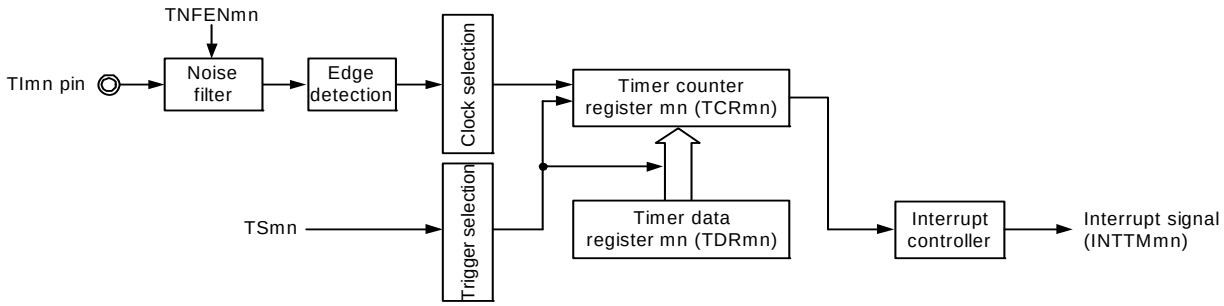
6.8.2 Operation as external event counter

The timer array unit can be used as an external event counter that counts the number of times the valid input edge (external event) is detected in the TImn pin. When a specified count value is reached, the event counter generates an interrupt. The specified number of counts can be calculated by the following expression.

Specified number of counts = Set value of TDRmn + 1

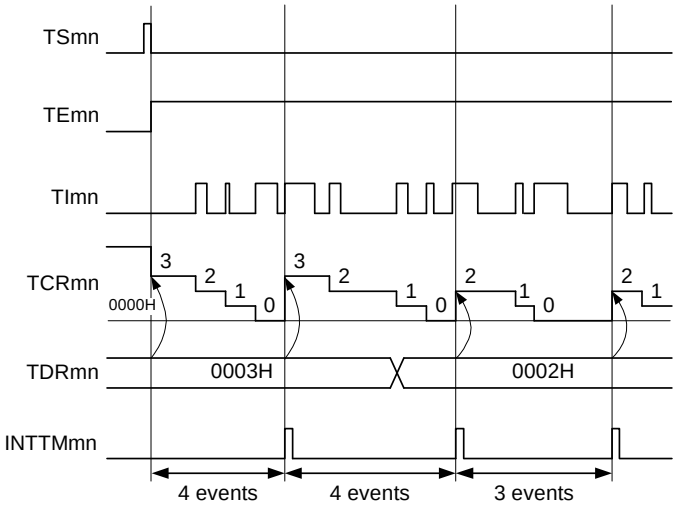
Timer count register mn (TCRmn) operates as a down counter in the event counter mode.
The TCRmn register loads the value of timer data register mn (TDRmn) by setting any channel start trigger bit (TSmn, TSHm1, TSHm3) of timer channel start register m (TSm) to 1.
The TCRmn register counts down each time the valid input edge of the TImn pin has been detected. When TCRmn = 0000H, the TCRmn register loads the value of the TDRmn register again, and outputs INTTMmn.
After that, the above operation is repeated.
An irregular waveform that depends on external events is output from the TOmn pin. Stop the output by setting the TOEmn bit of timer output enable register m (TOEm) to 0.
The TDRmn register can be rewritten at any time. The new value of the TDRmn register becomes valid during the next count period.

Figure 6 - 50 Block Diagram of Operation as External Event Counter



Remark m: Unit number (m = 0), n: Channel number (n = 0 to 7)

Figure 6 - 51 Example of Basic Timing of Operation as External Event Counter

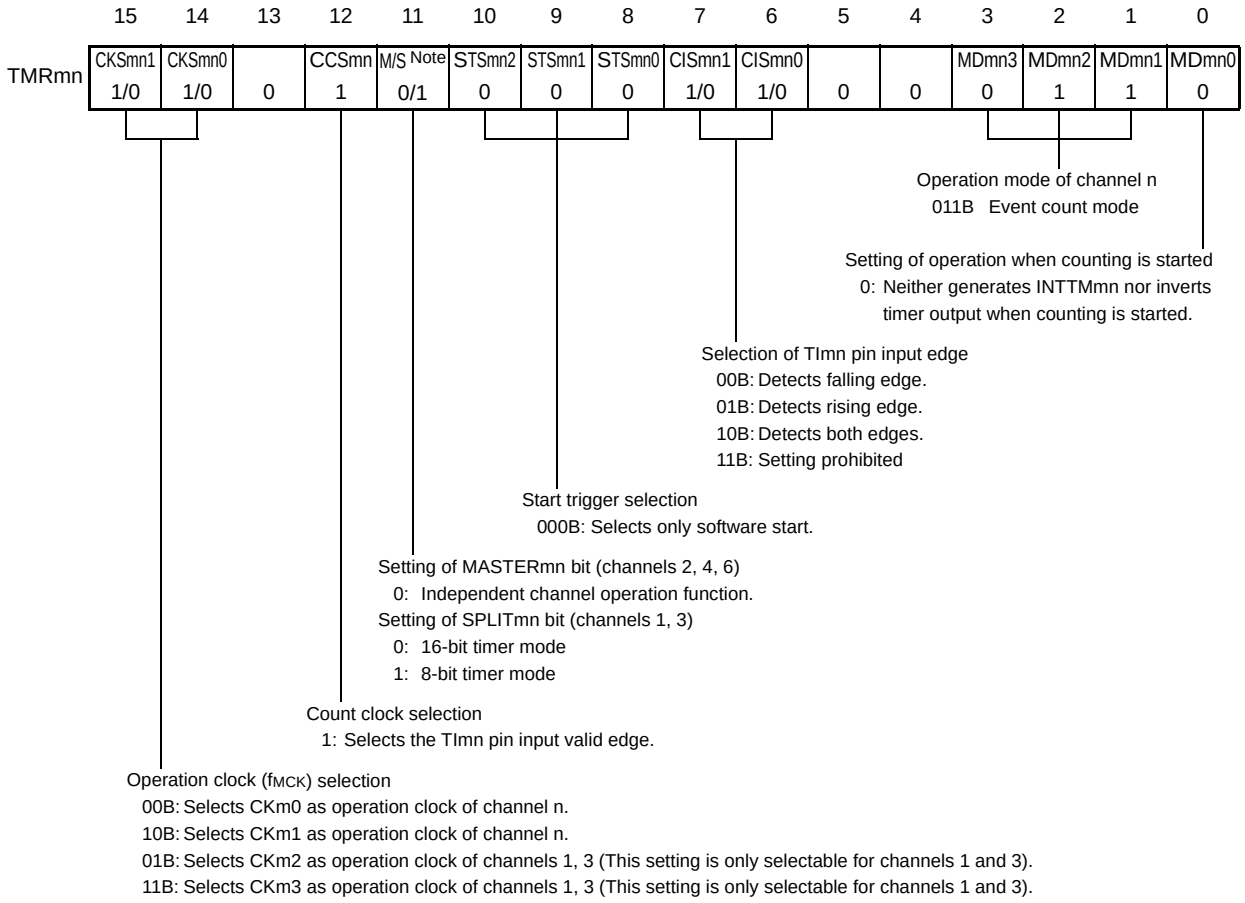


Remark 1. m: Unit number (m = 0), n: Channel number (n = 0 to 7)

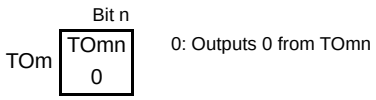
Remark 2. TSmn: Bit n of timer channel start register m (TSm)
TEmn: Bit n of timer channel enable status register m (TEm)
TImn: TImn pin input signal
TCRmn: Timer count register mn (TCRmn)
TDRmn: Timer data register mn (TDRmn)

Figure 6 - 52 Example of Set Contents of Registers in External Event Counter Mode

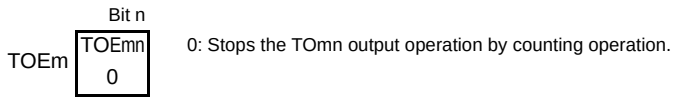
(a) Timer mode register mn (TMRmn)



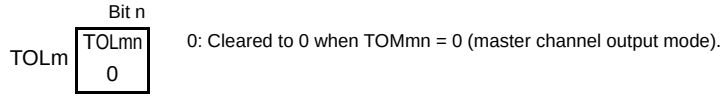
(b) Timer output register m (TOm)



(c) Timer output enable register m (TOEm)



(d) Timer output level register m (TOLm)



(e) Timer output mode register m (TOMm)

Note TMRm2, TMRm4, TMRm6: MASTERmn bit
TMRm1, TMRm3: SPLITmn bit
TMRm0, TMRm5, TMRm7: Fixed to 0

Remark m: Unit number (m = 0), n: Channel number (n = 0 to 7)

Figure 6 - 53 Operation Procedure When External Event Counter Function Is Used

	Software Operation	Hardware Status
TAU default setting		Power-off status (Clock supply is stopped and writing to each register is disabled.)
	Sets the TAUmEN bit of peripheral enable register 0 (PER0) to 1. →	Power-on status. Each channel stops operating. (Clock supply is started and writing to each register is enabled.)
	Sets timer clock select register m (TPSm). Determines clock frequencies of CKm0 to CKm3.	
Channel default setting	Sets the corresponding bit of the noise filter enable register 1 (NFEN1) to 0 (off) or 1 (on). Sets timer mode register mn (TMRmn) (determines operation mode of channel). Sets number of counts to timer data register mn (TDRmn). Clears the TOEmn bit of timer output enable register m (TOEm) to 0.	Channel stops operating. (Clock is supplied and some power is consumed.)
Operation start	Sets the TSmn bit to 1. → The TSmn bit automatically returns to 0 because it is a trigger bit.	TEmn = 1, and count operation starts. Value of the TDRmn register is loaded to timer count register mn (TCRmn) and detection of the TImn pin input edge is awaited.
During operation	Set value of the TDRmn register can be changed. The TCRmn register can always be read. The TSRmn register is not used. Set values of the TMRmn register, TOMmn, TOLmn, TOmn, and TOEmn bits cannot be changed.	Counter (TCRmn) counts down each time input edge of the TImn pin has been detected. When count value reaches 0000H, the value of the TDRmn register is loaded to the TCRmn register again, and the count operation is continued. By detecting TCRmn = 0000H, the INTTMmn output is generated. After that, the above operation is repeated.
Operation stop	The TTmn bit is set to 1. → The TTmn bit automatically returns to 0 because it is a trigger bit.	TEmn = 0, and count operation stops. The TCRmn register holds count value and stops.
TAU stop	The TAUmEN bit of the PER0 register is cleared to 0. →	Power-off status All circuits are initialized and SFR of each channel is also initialized.

Operation is resumed.

Remark m: Unit number (m = 0), n: Channel number (n = 0 to 7)

6.8.3 Operation as input pulse interval measurement

The count value can be captured at the TImn valid edge and the interval of the pulse input to TImn can be measured. In addition, the count value can be captured by using software operation (TSmn = 1) as a capture trigger while the TEmn bit is set to 1.

The pulse interval can be calculated by the following expression.

TImn input pulse interval = Period of count clock × ((10000H × TSRmn: OVF) + (Capture value of TDRmn + 1))

Caution The TImn pin input is sampled using the operating clock selected with the CKSmn bit of timer mode register mn (TMRmn), so an error of up to one operating clock cycle occurs.

Timer count register mn (TCRmn) operates as an up counter in the capture mode.

When the channel start trigger bit (TSmn) of timer channel start register m (TSm) is set to 1, the TCRmn register counts up from 0000H in synchronization with the count clock.

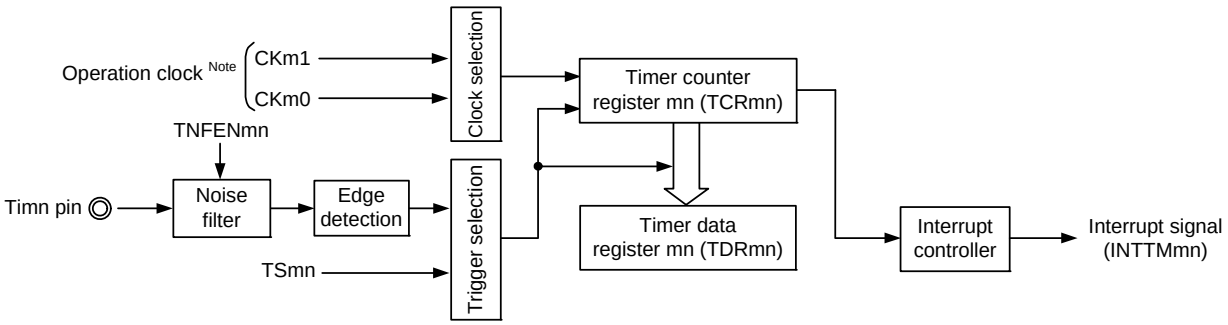
When the TImn pin input valid edge is detected, the count value of the TCRmn register is transferred (captured) to timer data register mn (TDRmn) and, at the same time, the TCRmn register is cleared to 0000H, and the INTTMmn is output. If the counter overflows at this time, the OVF bit of timer status register mn (TSRmn) is set to 1. If the counter does not overflow, the OVF bit is cleared. After that, the above operation is repeated.

As soon as the count value has been captured to the TDRmn register, the OVF bit of the TSRmn register is updated depending on whether the counter overflows during the measurement period. Therefore, the overflow status of the captured value can be checked.

If the counter reaches a full count for two or more periods, it is judged to be an overflow occurrence, and the OVF bit of the TSRmn register is set to 1. However, a normal interval value cannot be measured for the OVF bit, if two or more overflows occur.

Set the STSmn2 to STSmn0 bits of the TMRmn register to 001B to use the valid edges of TImn as a start trigger and a capture trigger.

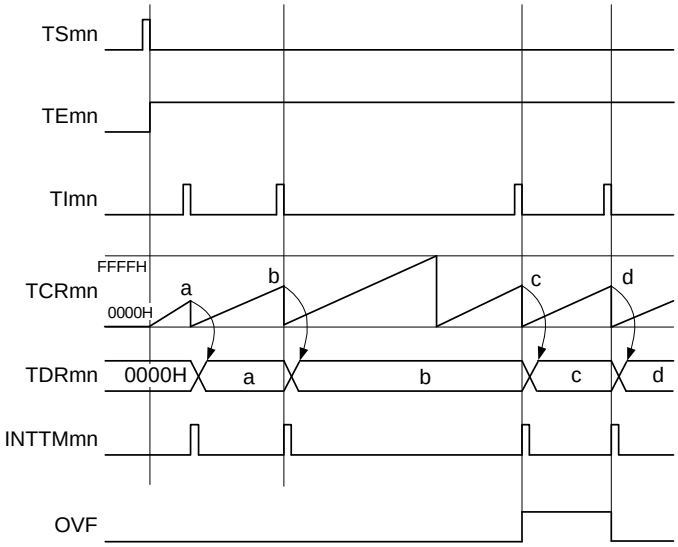
Figure 6 - 54 Block Diagram of Operation as Input Pulse Interval Measurement



Note When channels 1 and 3, the clock can be selected from CKm0, CKm1, CKm2 and CKm3.

Remark m: Unit number (m = 0), n: Channel number (n = 0 to 7)

Figure 6 - 55 Example of Basic Timing of Operation as Input Pulse Interval Measurement (MDmn0 = 0)

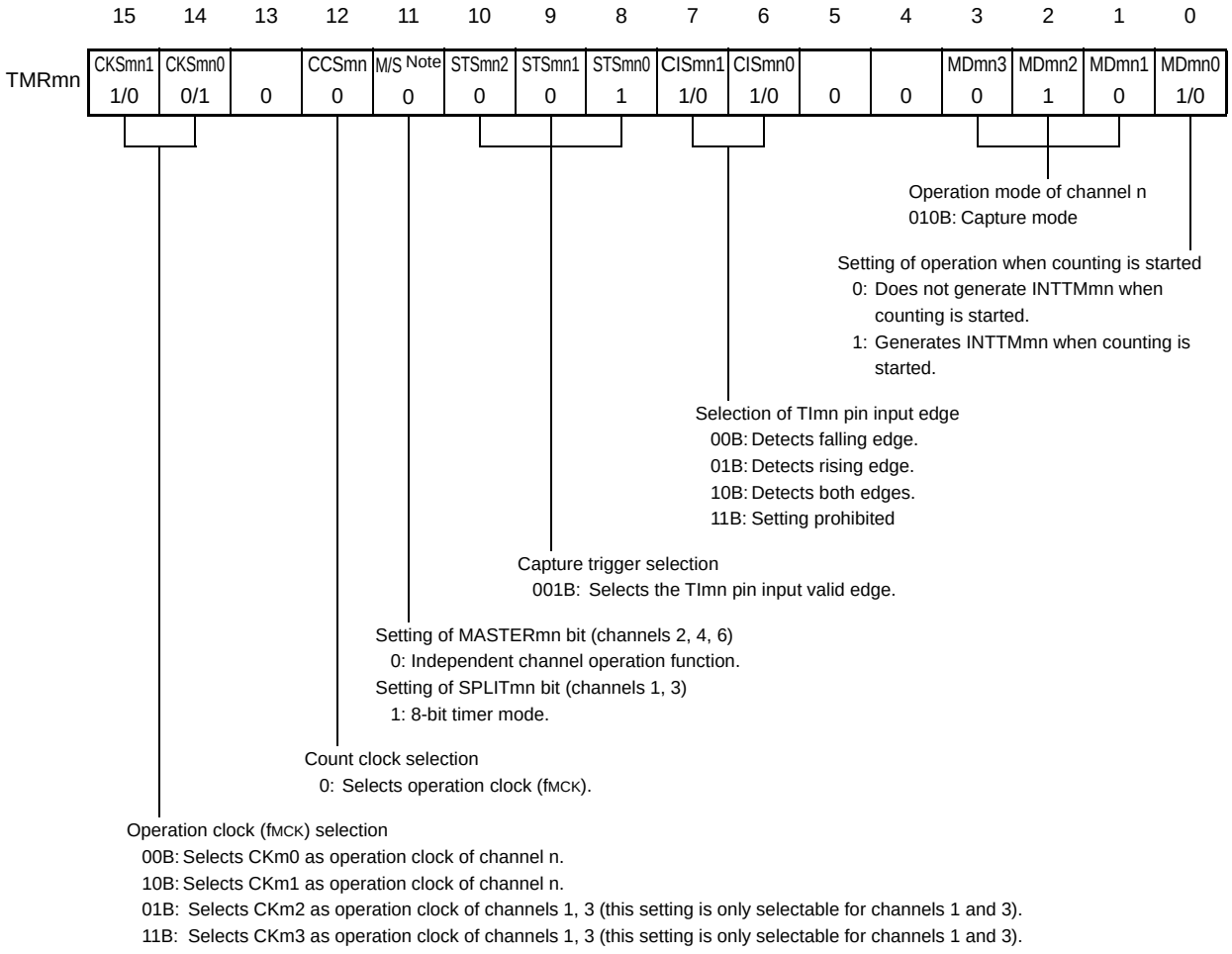


Remark 1. m: Unit number (m = 0), n: Channel number (n = 0 to 7)

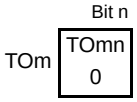
Remark 2. TSmn: Bit n of timer channel start register m (TSm)
TEmn: Bit n of timer channel enable status register m (TEm)
TImn: TImn pin input signal
TCRmn: Timer count register mn (TCRmn)
TDRmn: Timer data register mn (TDRmn)
OVF: Bit 0 of timer status register mn (TSRmn)

Figure 6 - 56 Example of Set Contents of Registers to Measure Input Pulse Interval

(a) Timer mode register mn (TMRmn)

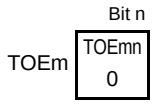


(b) Timer output register m (TOm)



0: Outputs 0 from TOmn.

(c) Timer output enable register m (TOEm)

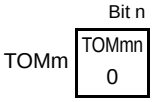


0: Stops TOmn output operation by counting operation.

(d) Timer output level register m (TOLm)

0: Cleared to 0 when TOMmn = 0 (master channel output mode).

(e) Timer output mode register m (TOMm)



0: Sets master channel output mode.

Note TMRm2, TMRm4, TMRm6: MASTERmn bit
TMRm1, TMRm3: SPLITmn bit
TMRm0, TMRm5, TMRm7: Fixed to 0

Remark m: Unit number (m = 0), n: Channel number (n = 0 to 7)

Figure 6 - 57 Operation Procedure When Input Pulse Interval Measurement Function Is Used

	Software Operation	Hardware Status
TAU default setting		Power-off status (Clock supply is stopped and writing to each register is disabled.)
	Sets the TAUmEN bit of peripheral enable register 0 (PER0) to 1. →	Power-on status. Each channel stops operating. (Clock supply is started and writing to each register is enabled.)
	Sets timer clock select register m (TPSm). Determines clock frequencies of CKm0 to CKm3.	
Channel default setting	Sets the corresponding bit of the noise filter enable register 1 (NFEN1) to 0 (off) or 1 (on). Sets timer mode register mn (TMRmn) (determines operation mode of channel).	Channel stops operating. (Clock is supplied and some power is consumed.)
Operation start	Sets TSmn bit to 1. → The TSmn bit automatically returns to 0 because it is a trigger bit.	TEmn = 1, and count operation starts. Timer count register mn (TCRmn) is cleared to 0000H at the count clock input. When the MDmn0 bit of the TMRmn register is 1, INTTMmn is generated.
During operation	Set values of only the CISmn1 and CISmn0 bits of the TMRmn register can be changed. The TDRmn register can always be read. The TCRmn register can always be read. The TSRmn register can always be read. Set values of the TOMmn, TOLmn, TOmn, and TOEmn bits cannot be changed.	Counter (TCRmn) counts up from 0000H. When the valid edge of the TImn pin input is detected or the TSmn bit is set to 1, the count value is transferred (captured) to timer data register mn (TDRmn). At the same time, the TCRmn register is cleared to 0000H, and the INTTMmn signal is generated. If an overflow occurs at this time, the OVF bit of timer status register mn (TSRmn) is set; if an overflow does not occur, the OVF bit is cleared. After that, the above operation is repeated.
Operation stop	The TTmn bit is set to 1. → The TTmn bit automatically returns to 0 because it is a trigger bit.	TEmn = 0, and count operation stops. The TCRmn register holds count value and stops. The OVF bit of the TSRmn register is also held.
TAU stop	The TAUmEN bit of the PER0 register is cleared to 0. →	Power-off status All circuits are initialized and SFR of each channel is also initialized.

Operation is resumed.

Remark m: Unit number (m = 0), n: Channel number (n = 0 to 7)

6.8.4 Operation as input signal high-/low-level width measurement

Caution When using a channel to implement the LIN-bus, set bit 1 (ISC1) of the input switch control register (ISC) to 1. In the following descriptions, read TImn as RxD0.

By starting counting at one edge of the TImn pin input and capturing the number of counts at another edge, the signal width (high-level width/low-level width) of TImn can be measured. The signal width of TImn can be calculated by the following expression.

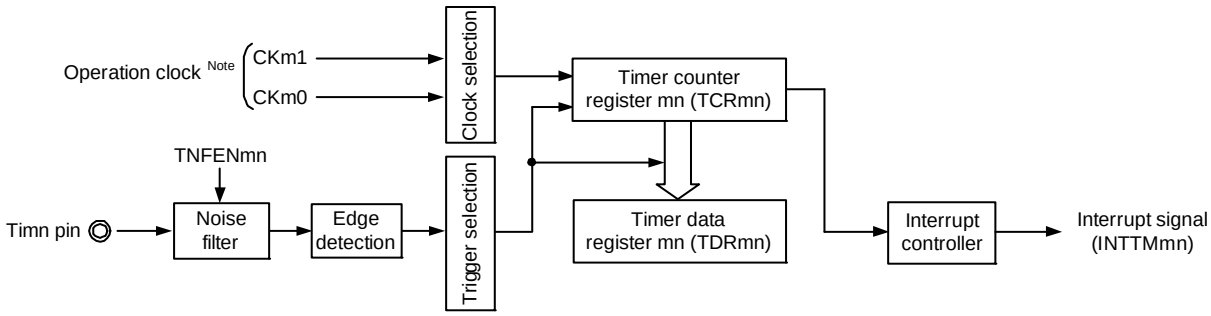
Signal width of TImn input = Period of count clock × ((10000H × TSRmn: OVF) + (Capture value of TDRmn + 1))

Caution The TImn pin input is sampled using the operating clock selected with the CKSmn bit of timer mode register mn (TMRmn), so an error equivalent to one operation clock occurs.

Timer count register mn (TCRmn) operates as an up counter in the capture & one-count mode.
When the channel start trigger bit (TSmn) of timer channel start register m (TSm) is set to 1, the TEmn bit is set to 1 and the TImn pin start edge detection wait status is set.
When the TImn pin input start edge (rising edge of the TImn pin input when the high-level width is to be measured) is detected, the counter counts up from 0000H in synchronization with the count clock. When the valid capture edge (falling edge of the TImn pin input when the high-level width is to be measured) is detected later, the count value is transferred to timer data register mn (TDRmn) and, at the same time, INTTMmn is output. If the counter overflows at this time, the OVF bit of timer status register mn (TSRmn) is set to 1. If the counter does not overflow, the OVF bit is cleared. The TCRmn register stops at the value “value transferred to the TDRmn register + 1”, and the TImn pin start edge detection wait status is set. After that, the above operation is repeated.
As soon as the count value has been captured to the TDRmn register, the OVF bit of the TSRmn register is updated depending on whether the counter overflows during the measurement period. Therefore, the overflow status of the captured value can be checked.
If the counter reaches a full count for two or more periods, it is judged to be an overflow occurrence, and the OVF bit of the TSRmn register is set to 1. However, a normal interval value cannot be measured for the OVF bit, if two or more overflows occur.
Whether the high-level width or low-level width of the TImn pin is to be measured can be selected by using the CISmn1 and CISmn0 bits of the TMRmn register.
Because this function is used to measure the signal width of the TImn pin input, the TSmn bit cannot be set to 1 while the TEmn bit is 1.

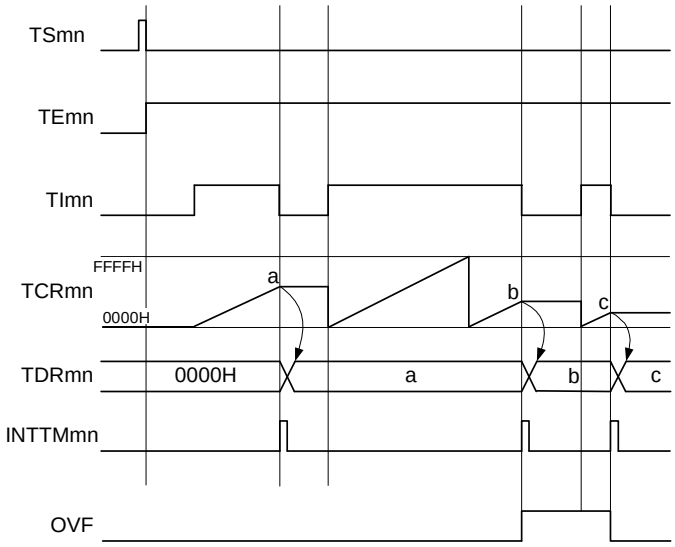
CISmn1, CISmn0 of TMRmn register = 10B: Low-level width is measured.
CISmn1, CISmn0 of TMRmn register = 11B: High-level width is measured.

Figure 6 - 58 Block Diagram of Operation as Input Signal High-/Low-Level Width Measurement



Note For channels 1 and 3, the clock can be selected from CKm0, CKm1, CKm2 and CKm3.

Figure 6 - 59 Example of Basic Timing of Operation as Input Signal High-/Low-Level Width Measurement

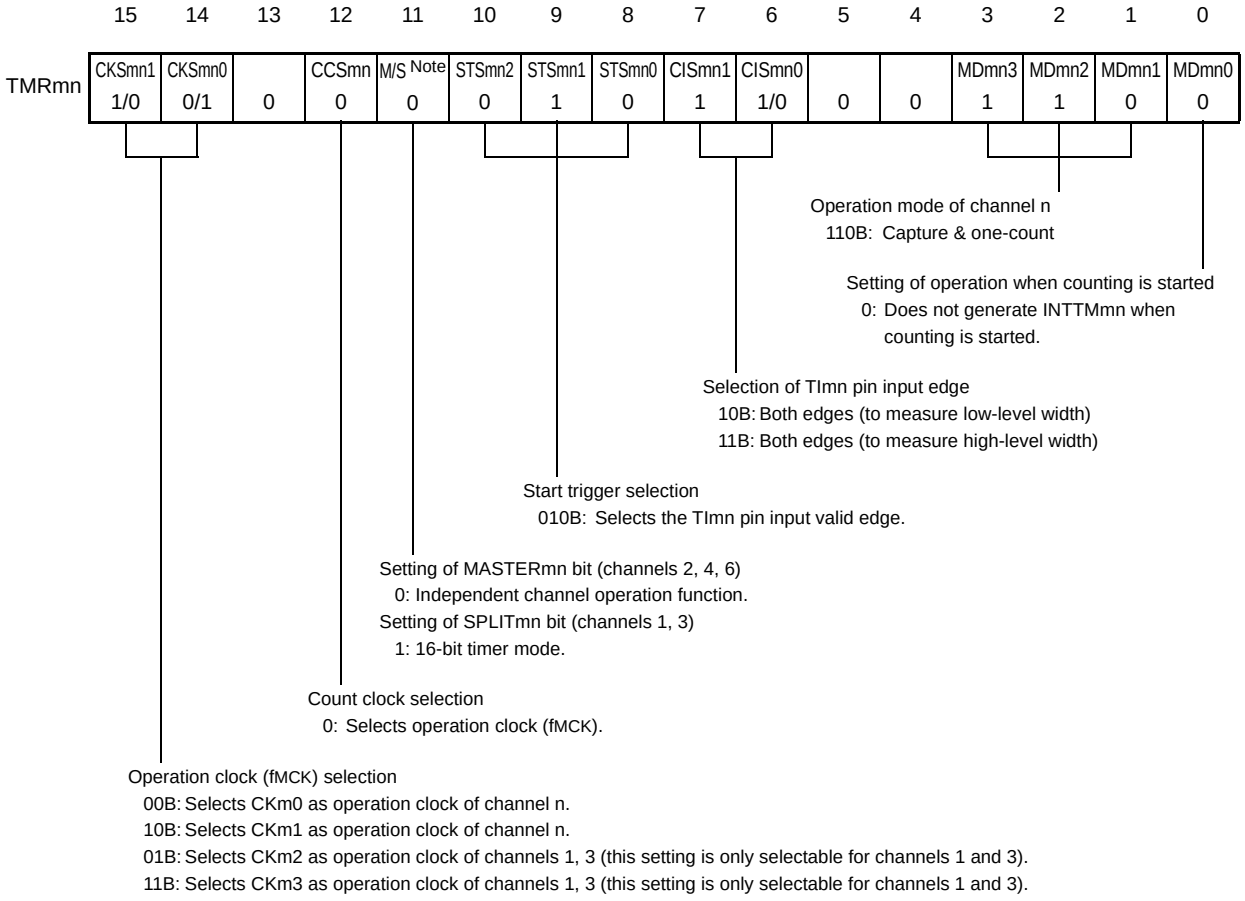


Remark 1. m: Unit number (m = 0), n: Channel number (n = 0 to 7)

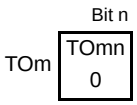
Remark 2. TSmn: Bit n of timer channel start register m (TSm)
TEmn: Bit n of timer channel enable status register m (TEm)
TImn: TImn pin input signal
TCRmn: Timer count register mn (TCRmn)
TDRmn: Timer data register mn (TDRmn)
OVF: Bit 0 of timer status register mn (TSRmn)

Figure 6 - 60 Example of Set Contents of Registers to Measure Input Signal High-/Low-Level Width

(a) Timer mode register mn (TMRmn)

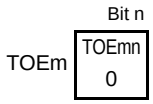


(b) Timer output register m (TOm)



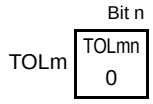
0: Outputs 0 from TOmn.

(c) Timer output enable register m (TOEm)



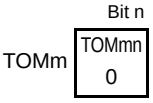
0: Stops the TOmn output operation by counting operation.

(d) Timer output level register m (TOLm)



0: Cleared to 0 when TOMmn = 0 (master channel output mode).

(e) Timer output mode register m (TOMm)



0: Sets master channel output mode.

Note TMRm2, TMRm4, TMRm6: MASTERmn bit
TMRm1, TMRm3: SPLITmn bit
TMRm0, TMRm5, TMRm7: Fixed to 0

Remark m: Unit number (m = 0), n: Channel number (n = 0 to 7)

Figure 6 - 61 Operation Procedure When Input Signal High-/Low-Level Width Measurement Function Is Used

	Software Operation	Hardware Status
TAU default setting		Power-off status (Clock supply is stopped and writing to each register is disabled.)
	Sets the TAUmEN bit of peripheral enable register 0 (PER0) to 1. →	Power-on status. Each channel stops operating. (Clock supply is started and writing to each register is enabled.)
	Sets timer clock select register m (TPSm). Determines clock frequencies of CKm0 to CKm3.	
Channel default setting	Sets the corresponding bit of the noise filter enable register 1 (NFEN1) to 0 (off) or 1 (on). Sets timer mode register mn (TMRmn) (determines operation mode of channel). Clears the TOEmn bit to 0 and stops operation of TOmn.	Channel stops operating. (Clock is supplied and some power is consumed.)
Operation start	Sets the TSmn bit to 1. → The TSmn bit automatically returns to 0 because it is a trigger bit.	TEmn = 1, and the TImn pin start edge detection wait status is set.
	Detects the TImn pin input count start valid edge. →	Clears timer count register mn (TCRmn) to 0000H and starts counting up.
During operation	Set value of the TDRmn register can be changed. The TCRmn register can always be read. The TSRmn register is not used. Set values of the TMRmn register, TOMmn, TOLmn, TOmn, and TOEmn bits cannot be changed.	When the TImn pin start edge is detected, the counter (TCRmn) counts up from 0000H. If a capture edge of the TImn pin is detected, the count value is transferred to timer data register mn (TDRmn) and INTTMmn is generated. If an overflow occurs at this time, the OVF bit of timer status register mn (TSRmn) is set; if an overflow does not occur, the OVF bit is cleared. The TCRmn register stops the count operation until the next TImn pin start edge is detected.
Operation stop	The TTmn bit is set to 1. → The TTmn bit automatically returns to 0 because it is a trigger bit.	TEmn = 0, and count operation stops. The TCRmn register holds count value and stops. The OVF bit of the TSRmn register is also held.
TAU stop	The TAUmEN bit of the PER0 register is cleared to 0. →	Power-off status All circuits are initialized and SFR of each channel is also initialized.

Operation is resumed.

Remark m: Unit number (m = 0), n: Channel number (n = 0 to 7)

6.8.5 Operation as delay counter

It is possible to start counting down when the valid edge of the TImn pin input is detected (an external event), and then generate INTTMmn (a timer interrupt) after any specified interval.

It is also possible to start counting down and generate INTTMmn (timer interrupt) at any interval by setting TSmn to 1 by software while TEmn = 1.

The interrupt generation period can be calculated by the following expression.

Generation period of INTTMmn (timer interrupt) = Period of count clock × (Set value of TDRmn + 1)

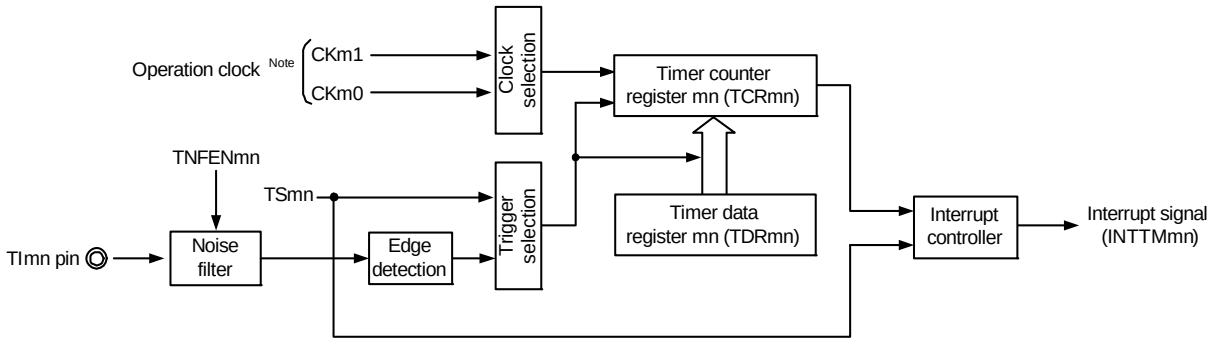
Timer count register mn (TCRmn) operates as a down counter in the one-count mode.

When the channel start trigger bit (TSmn, TSHm1, TSHm3) of timer channel start register m (TSm) is set to 1, the TEmn, TEHm1, TEHm3 bits are set to 1 and the TImn pin input valid edge detection wait status is set.

Timer count register mn (TCRmn) starts operating upon TImn pin input valid edge detection and loads the value of timer data register mn (TDRmn). The TCRmn register counts down from the value of the TDRmn register it has loaded, in synchronization with the count clock. When TCRmn = 0000H, it outputs INTTMmn and stops counting until the next TImn pin input valid edge is detected.

The TDRmn register can be rewritten at any time. The new value of the TDRmn register becomes valid from the next period.

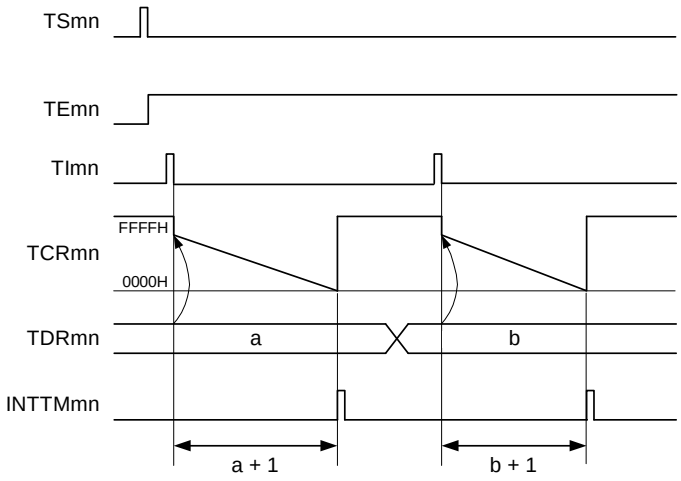
Figure 6 - 62 Block Diagram of Operation as Delay Counter



Note For using channels 1 and 3, the clock can be selected from CKm0, CKm1, CKm2 and CKm3.

Remark m: Unit number (m = 0), n: Channel number (n = 0 to 7)

Figure 6 - 63 Example of Basic Timing of Operation as Delay Counter

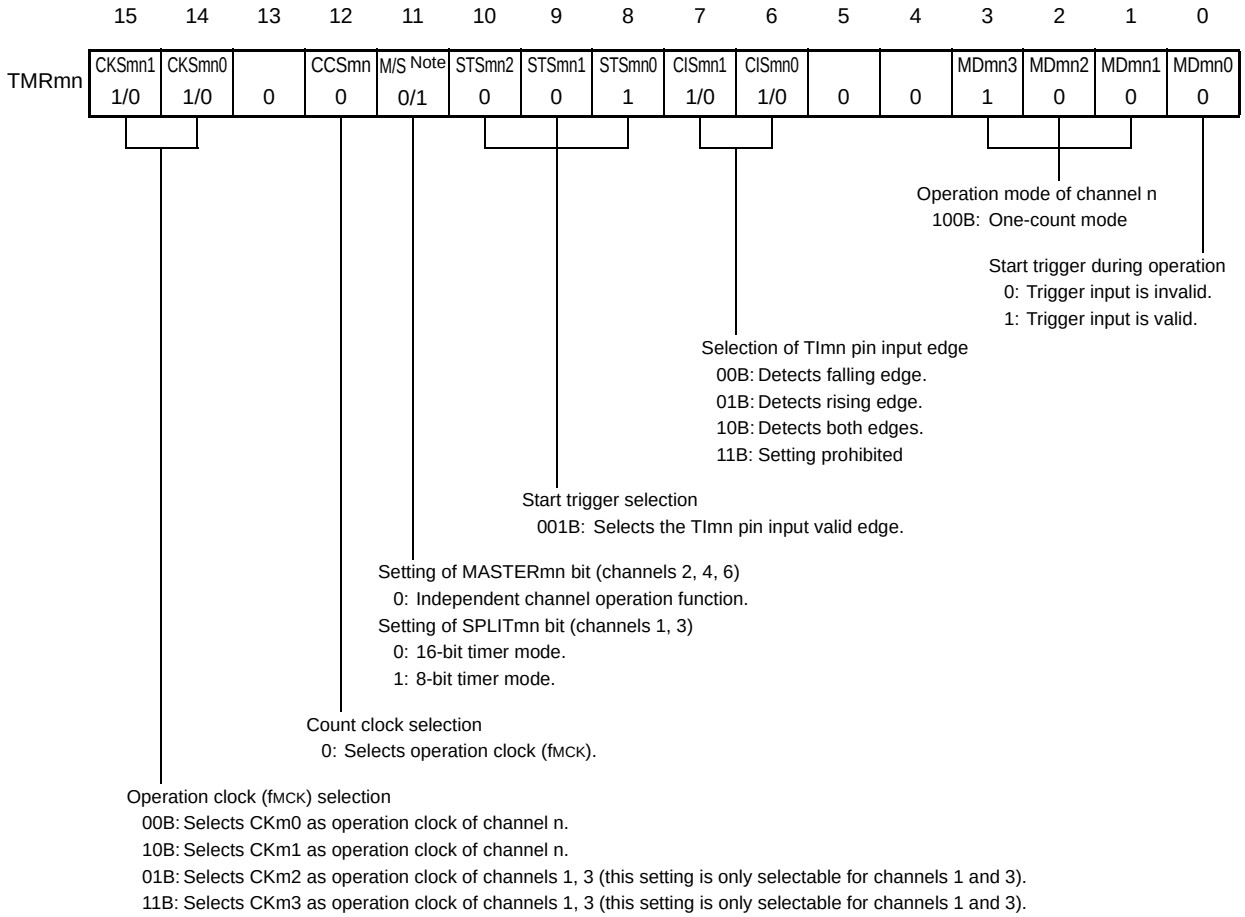


Remark 1. m: Unit number (m = 0), n: Channel number (n = 0 to 7)

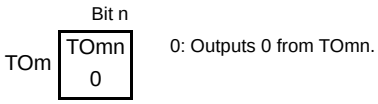
Remark 2. TSmn: Bit n of timer channel start register m (TSm)
TEmn: Bit n of timer channel enable status register m (TEm)
TImn: TImn pin input signal
TCRmn: Timer count register mn (TCRmn)
TDRmn: Timer data register mn (TDRmn)

Figure 6 - 64 Example of Set Contents of Registers to Delay Counter

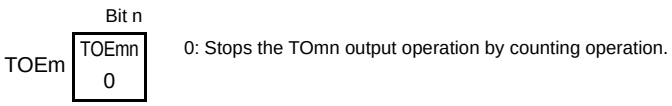
(a) Timer mode register mn (TMRmn)



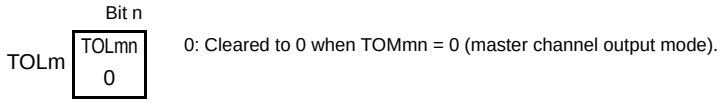
(b) Timer output register m (TOm)



(c) Timer output enable register m (TOEm)



(d) Timer output level register m (TOLm)



(e) Timer output mode register m (TOMm)

Note TMRm2, TMRm4, TMRm6: MASTERmn bit
TMRm1, TMRm3: SPLITmn bit
TMRm0, TMRm5, TMRm7: Fixed to 0

Remark m: Unit number (m = 0), n: Channel number (n = 0 to 7)

Figure 6 - 65 Operation Procedure When Delay Counter Function Is Used

	Software Operation	Hardware Status
TAU default setting		Power-off status (Clock supply is stopped and writing to each register is disabled.)
	Sets the TAUmEN bit of peripheral enable register 0 (PER0) to 1. →	Power-on status. Each channel stops operating. (Clock supply is started and writing to each register is enabled.)
	Sets timer clock select register m (TPSm). Determines clock frequencies of CKm0 to CKm3.	
Channel default setting	Sets the corresponding bit of the noise filter enable register 1 (NFEN1) to 0 (off) or 1 (on). Sets timer mode register mn (TMRmn) (determines operation mode of channel). INTTMmn output delay is set to timer data register mn (TDRmn). Clears the TOEmn bit to 0 and stops operation of TOmn.	Channel stops operating. (Clock is supplied and some power is consumed.)
Operation start	Sets the TSmn bit to 1. → The TSmn bit automatically returns to 0 because it is a trigger bit.	TEmn = 1, and the start trigger detection (the valid edge of the TImn pin input is detected or the TSmn bit is set to 1) wait status is set.
	Detects the TImn pin input valid edge. →	Value of the TDRmn register is loaded to the timer count register mn (TCRmn).
During operation	Set value of the TDRmn register can be changed. The TCRmn register can always be read. The TSRmn register is not used.	The counter (TCRmn) counts down. When the count value of TCRmn reaches 0000H, the INTTMmn output is generated, and the count operation stops until the next start trigger detection (the valid edge of the TImn pin input is detected or the TSmn bit is set to 1).
Operation stop	The TTmn bit is set to 1. → The TTmn bit automatically returns to 0 because it is a trigger bit.	TEmn = 0, and count operation stops. The TCRmn register holds count value and stops.
TAU stop	The TAUmEN bit of the PER0 register is cleared to 0. →	Power-off status All circuits are initialized and SFR of each channel is also initialized.

Operation is resumed.

Remark m: Unit number (m = 0), n: Channel number (n = 0 to 7)

6.9 Simultaneous Channel Operation Function of Timer Array Unit

6.9.1 Operation as one-shot pulse output function

By using two channels as a set, a one-shot pulse having any delay pulse width can be generated from the signal input to the TImn pin.

The delay time and pulse width can be calculated by the following expressions.

Delay time = {Set value of TDRmn (master) + 2} × Count clock period
Pulse width = {Set value of TDRmp (slave)} × Count clock period

The master channel operates in the one-count mode and counts the delays. Timer count register mn (TCRmn) of the master channel starts operating upon start trigger detection and loads the value of timer data register mn (TDRmn).

The TCRmn register counts down from the value of the TDRmn register it has loaded, in synchronization with the count clock. When TCRmn = 0000H, it outputs INTTMmn and stops counting until the next start trigger is detected.

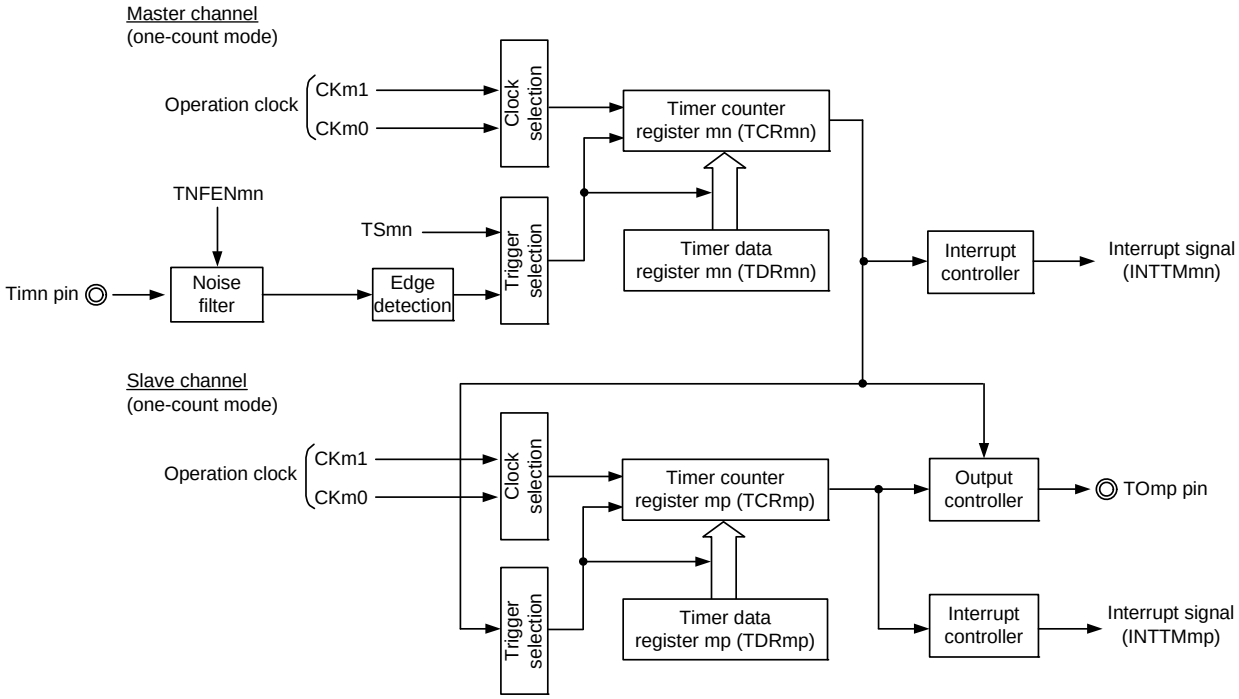
The slave channel operates in the one-count mode and counts the pulse width. The TCRmp register of the slave channel starts operation using INTTMmn of the master channel as a start trigger, and loads the value of the TDRmp register. The TCRmp register counts down from the value of The TDRmp register it has loaded, in synchronization with the count value. When count value = 0000H, it outputs INTTMmp and stops counting until the next start trigger (INTTMmn of the master channel) is detected. The output level of TOmp becomes active one count clock after generation of INTTMmn from the master channel, and inactive when TCRmp = 0000H.

Instead of using the TImn pin input, a one-shot pulse can also be output using the software operation (TSmn = 1) as a start trigger.

Caution **The timing of loading of the TDRmn register of the master channel is different from that of the TDRmp register of the slave channel. If the TDRmn and TDRmp registers are rewritten during counting, therefore, an illegal waveform is output in conflict with the timing of loading. Rewrite the TDRmn register after INTTMmn is generated and the TDRmp register after INTTMmp is generated.**

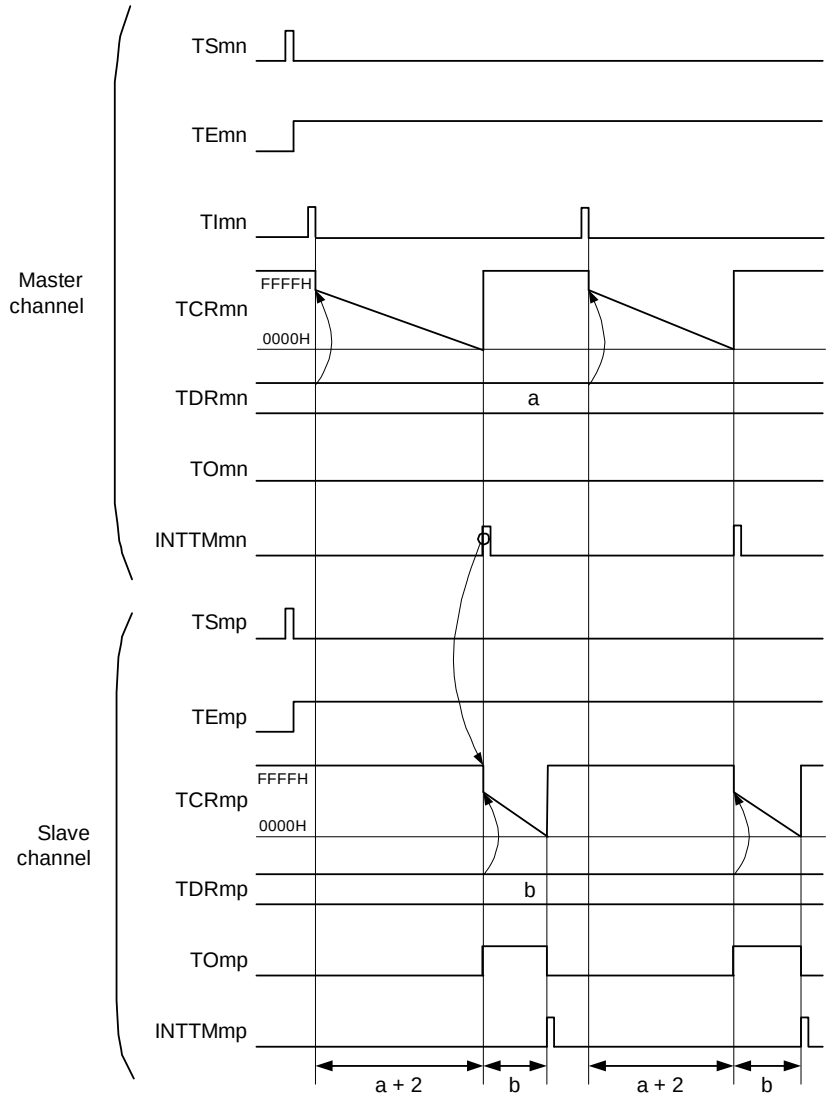
Remark m: Unit number (m = 0), n: Channel number (n = 0, 2, 4, 6)
p: Slave channel number (n < p ≤ 7)

Figure 6 - 66 Block Diagram of Operation as One-Shot Pulse Output Function



Remark m: Unit number (m = 0), n: Channel number (n = 0, 2, 4, 6))
p: Slave channel number (n < p ≤ 7)

Figure 6 - 67 Example of Basic Timing of Operation as One-Shot Pulse Output Function

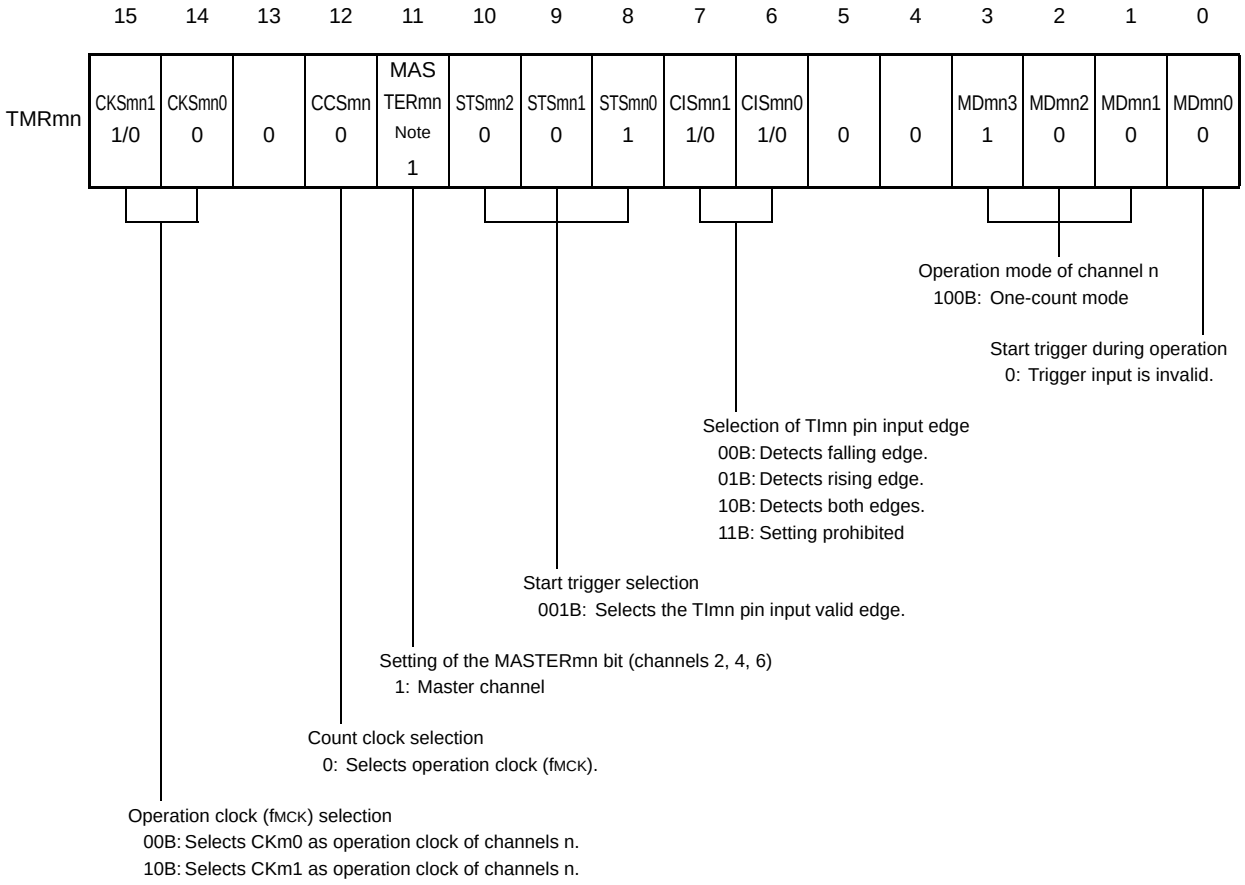


Remark 1. m: Unit number (m = 0), n: Channel number (n = 0, 2, 4, 6)
p: Slave channel number (n < p ≤ 7)

Remark 2. TSmn, TSmp: Bit n, p of timer channel start register m (TSm)
TEmn, TEmp: Bit n, p of timer channel enable status register m (TEm)
TImn, TImp: TImn and TImp pins input signal
TCRmn, TCRmp: Timer count registers mn, mp (TCRmn, TCRmp)
TDRmn, TDRmp: Timer data registers mn, mp (TDRmn, TDRmp)
TOmn, TOmp: TOmn and TOmp pins output signal

Figure 6 - 68 Example of Set Contents of Registers
When One-Shot Pulse Output Function Is Used (Master Channel)

(a) Timer mode register mn (TMRmn)



(b) Timer output register m (TOm)

	Bit n	
TOm	TOmn 0	0: Outputs 0 from TOmn.

(c) Timer output enable register m (TOEm)

	Bit n	
TOEm	TOEmn 0	0: Stops the TOmn output operation by counting operation.

(d) Timer output level register m (TOLm)

	Bit n	
TOLm	TOLmn 0	0: Cleared to 0 when TOMmn = 0 (master channel output mode).

(e) Timer output mode register m (TOMm)

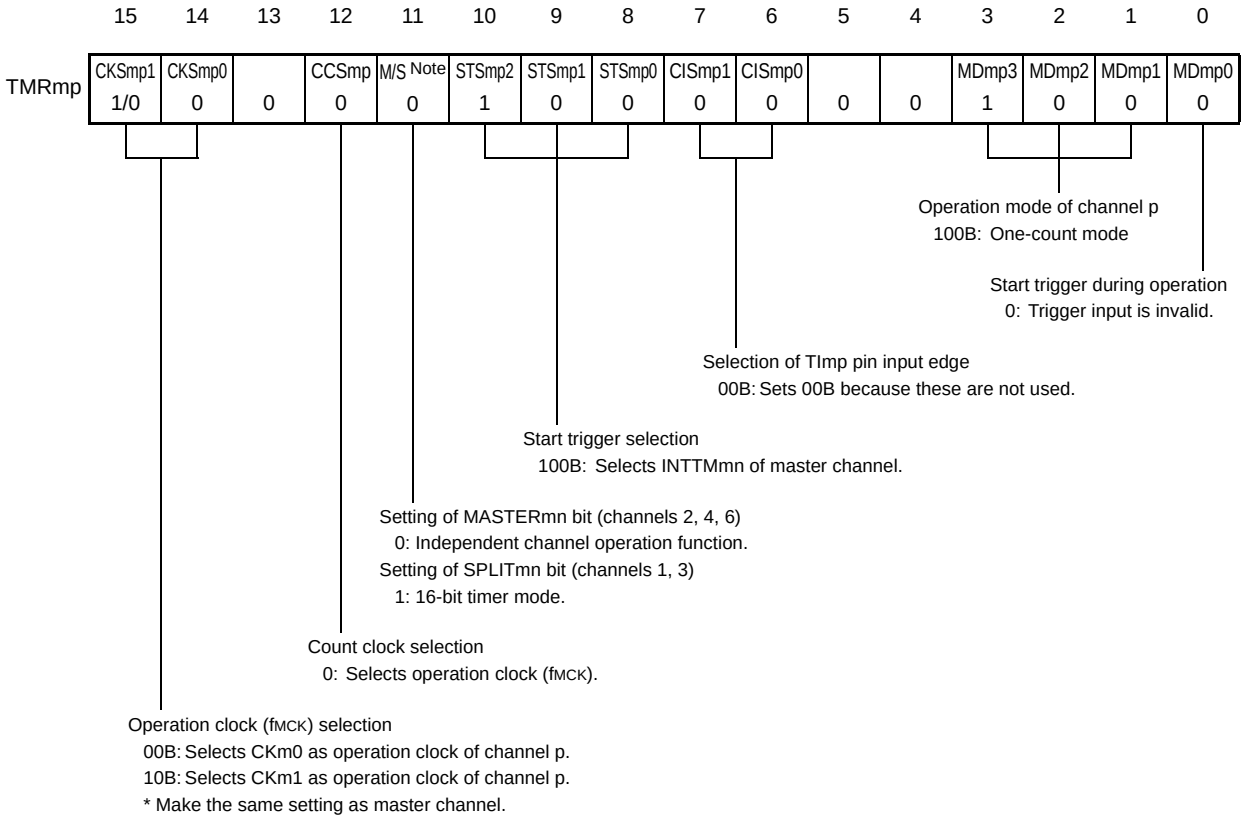
	Bit n	
TOMm	TOMmn 0	0: Sets master channel output mode.

Note TMRm2, TMRm4, TMRm6: MASTERmn = 1
TMRm0: Fixed to 0

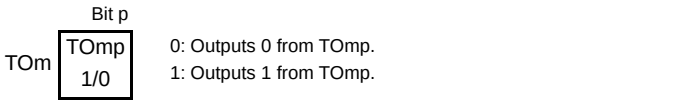
Remark m: Unit number (m = 0), n: Channel number (n = 0, 2, 4, 6)

Figure 6 - 69 Example of Set Contents of Registers
When One-Shot Pulse Output Function Is Used (Slave Channel)

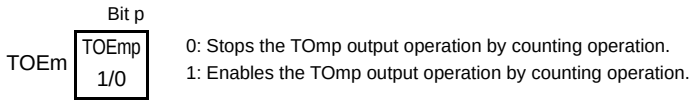
(a) Timer mode register mp (TMRmp)



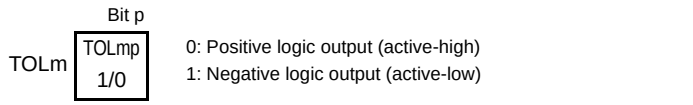
(b) Timer output register m (TOm)



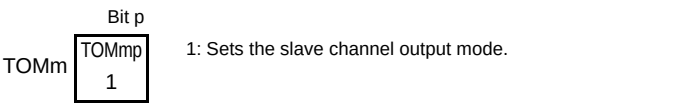
(c) Timer output enable register m (TOEm)



(d) Timer output level register m (TOLm)



(e) Timer output mode register m (TOMm)



Note TMRm2, TMRm4, TMRm6: MASTERmn bit
TMRm1, TMRm3: SPLITmp bit
TMRm5, TMRm7: Fixed to 0

Remark m: Unit number (m = 0), n: Channel number (n = 0, 2, 4, 6)
p: Slave channel number (n < p ≤ 7)

Figure 6 - 70 Operation Procedure of One-Shot Pulse Output Function (1/2)

	Software Operation	Hardware Status
TAU default setting		Power-off status (Clock supply is stopped and writing to each register is disabled.)
	Sets the TAUmEN bit of peripheral enable registers 0 (PER0) to 1. →	Power-on status. Each channel stops operating. (Clock supply is started and writing to each register is enabled.)
	Sets timer clock select register m (TPSm). Determines clock frequencies of CKm0 and CKm1.	
Channel default setting	Sets the corresponding bit of the noise filter enable registers 1 (NFEN1) to 1. Sets timer mode register mn, mp (TMRmn, TMRmp) of two channels to be used (determines operation mode of channels). An output delay is set to timer data register mn (TDRmn) of the master channel, and a pulse width is set to the TDRmp register of the slave channel.	Channel stops operating. (Clock is supplied and some power is consumed.)
	Sets slave channel. The TOMmp bit of timer output mode register m (TOMm) is set to 1 (slave channel output mode). Sets the TOLmp bit. Sets the TOmp bit and determines default level of the TOmp output. →	The TOmp pin goes into Hi-Z output state. The TOmp default setting level is output when the port mode register is in output mode and the port register is 0.
	Sets the TOEmp bit to 1 and enables operation of TOmp. →	TOmp does not change because channel stops operating.
	Clears the port register and port mode register to 0. →	The TOmp pin outputs the TOmp set level.

(**Remark** is listed on the next page.)

Figure 6 - 70 Operation Procedure of One-Shot Pulse Output Function (2/2)

	Software Operation	Hardware Status
Operation start	Sets the TOEmp bit (slave) to 1 (only when operation is resumed). →	The TEmn and TEmp bits are set to 1 and the master channel enters the start trigger detection (the valid edge of the TImn pin input is detected or the TSmn bit of the master channel is set to 1) wait status. Counter stops operating.
	The TSmn (master) and TSmp (slave) bits of timer channel start register m (TSm) are set to 1 at the same time. The TSmn and TSmp bits automatically return to 0 because they are trigger bits.	
	Count operation of the master channel is started by start trigger detection of the master channel. • Detects the TImn pin input valid edge. • Sets the TSmn bit of the master channel to 1 by software Note. Note Do not set the TSmn bit of the slave channel to 1. →	Master channel starts counting.
During operation	Set values of only the CISmn1 and CISmn0 bits of the TMRmn register can be changed. Set values of the TMRmp, TDRmn, TDRmp registers, TOMmn, TOMmp, TOLmn, and TOLmp bits cannot be changed. The TCRmn and TCRmp registers can always be read. The TSRmn and TSRmp registers are not used. Set values of the TOm and TOEm registers by slave channel can be changed.	Master channel loads the value of the TDRmn register to timer count register mn (TCRmn) by the start trigger detection (the valid edge of the TImn pin input is detected or the TSmn bit of the master channel is set to 1), and the counter starts counting down. When the count value reaches TCRmn = 0000H, the INTTMmn output is generated, and the counter stops until the next start trigger detection. The slave channel, triggered by INTTMmn of the master channel, loads the value of the TDRmp register to the TCRmp register, and the counter starts counting down. The output level of TOmp becomes active one count clock after generation of INTTMmn from the master channel. It becomes inactive when TCRmp = 0000H, and the counting operation is stopped. After that, the above operation is repeated.
Operation stop	The TTmn (master) and TTmp (slave) bits are set to 1 at the same time. → The TTmn (master) and TTmp (slave) bits are set to 1 at the same time.	TEmn, TEmp = 0, and count operation stops. The TCRmn and TCRmp registers hold count value and stop. The TOmp output is not initialized but holds current status.
	The TOEmp bit of slave channel is cleared to 0 and value is set to the TOmp bit. →	The TOmp pin outputs the TOmp set level.
TAU stop	To hold the TOmp pin output level Clears the TOmp bit to 0 after the value to be held is set to the port register. → When holding the TOmp pin output level is not necessary Setting not required.	The TOmp pin output level is held by port function.
	The TAUmEN bit of the PER0 register is cleared to 0. →	Power-off status All circuits are initialized and SFR of each channel is also initialized. (The TOmp bit is cleared to 0 and the TOmp pin is set to port mode.)

Operation is resumed.

Remark m: Unit number (m = 0), n: Channel number (n = 0, 2, 4, 6)
p: Slave channel number (n < p ≤ 7)

6.9.2 Operation as PWM function

Two channels can be used as a set to generate a pulse of any period and duty factor.
The period and duty factor of the output pulse can be calculated by the following expressions.

Pulse period = {Set value of TDRmn (master) + 1} × Count clock period
Duty factor [%] = {Set value of TDRmp (slave)}/{Set value of TDRmn (master) + 1} × 100
0% output: Set value of TDRmp (slave) = 0000H
100% output: Set value of TDRmp (slave) ≥ {Set value of TDRmn (master) + 1}

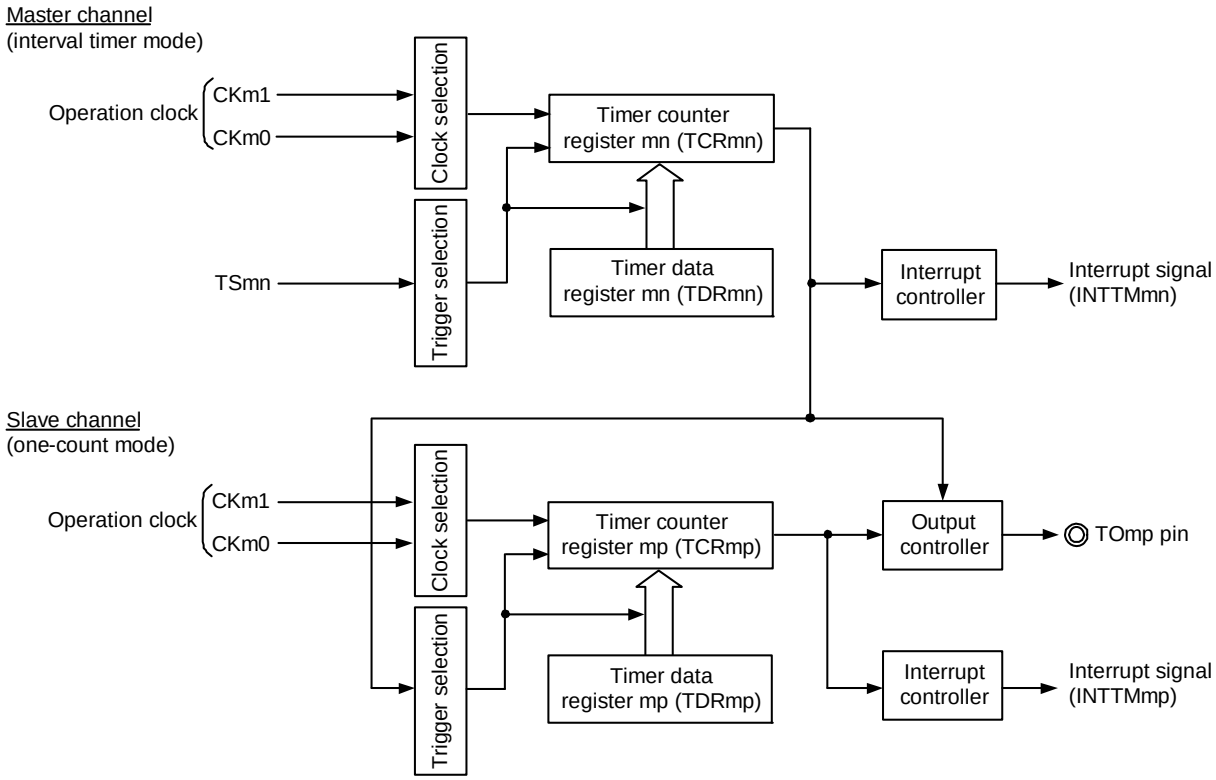
Remark The duty factor exceeds 100% if the set value of TDRmp (slave) > (set value of TDRmn (master) + 1), it summarizes to 100% output.

The master channel operates in the interval timer mode. If the channel start trigger bit (TSmn) of timer channel start register m (TSm) is set to 1, an interrupt (INTTMmn) is output, the value set to timer data register mn (TDRmn) is loaded to timer count register mn (TCRmn), and the counter counts down in synchronization with the count clock. When the counter reaches 0000H, INTTMmn is output, the value of the TDRmn register is loaded again to the TCRmn register, and the counter counts down. This operation is repeated until the channel stop trigger bit (TTmn) of timer channel stop register m (TTm) is set to 1.
If two channels are used to output a PWM waveform, the period until the master channel counts down to 0000H is the PWM output (TOmp) cycle.
The slave channel operates in one-count mode. By using INTTMmn from the master channel as a start trigger, the TCRmp register loads the value of the TDRmp register and the counter counts down to 0000H. When the counter reaches 0000H, it outputs INTTMmp and waits until the next start trigger (INTTMmn from the master channel) is generated.
If two channels are used to output a PWM waveform, the period until the slave channel counts down to 0000H is the PWM output (TOmp) duty.
PWM output (TOmp) goes to the active level one clock after the master channel generates INTTMmn and goes to the inactive level when the TCRmp register of the slave channel becomes 0000H.

Caution **To rewrite both timer data register mn (TDRmn) of the master channel and the TDRmp register of the slave channel, a write access is necessary two times. The timing at which the values of the TDRmn and TDRmp registers are loaded to the TCRmn and TCRmp registers is upon occurrence of INTTMmn of the master channel. Thus, when rewriting is performed split before and after occurrence of INTTMmn of the master channel, the TOmp pin cannot output the expected waveform. To rewrite both the TDRmn register of the master and the TDRmp register of the slave, therefore, be sure to rewrite both the registers immediately after INTTMmn is generated from the master channel.**

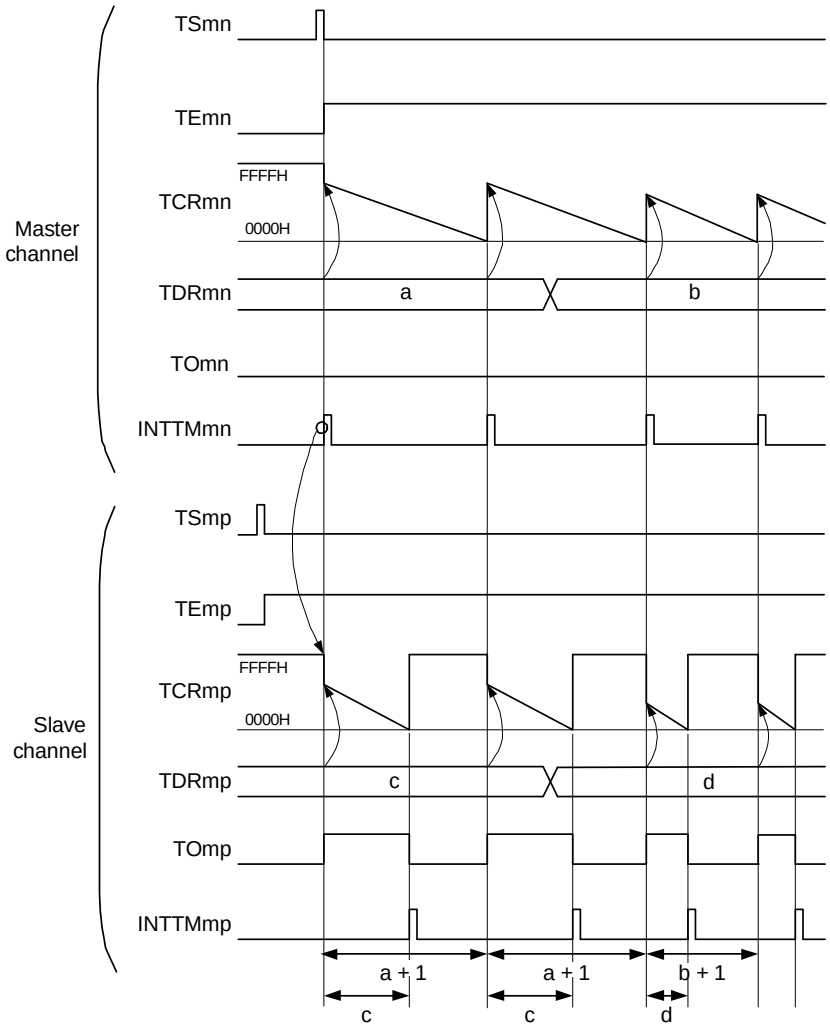
Remark m: Unit number (m = 0), n: Channel number (n = 0, 2, 4, 6)
p: Slave channel number (n < p ≤ 7)

Figure 6 - 71 Block Diagram of Operation as PWM Function



Remark m: Unit number (m = 0), n: Channel number (n = 0, 2, 4, 6)
p: Slave channel number (n < p ≤ 7)

Figure 6 - 72 Example of Basic Timing of Operation as PWM Function

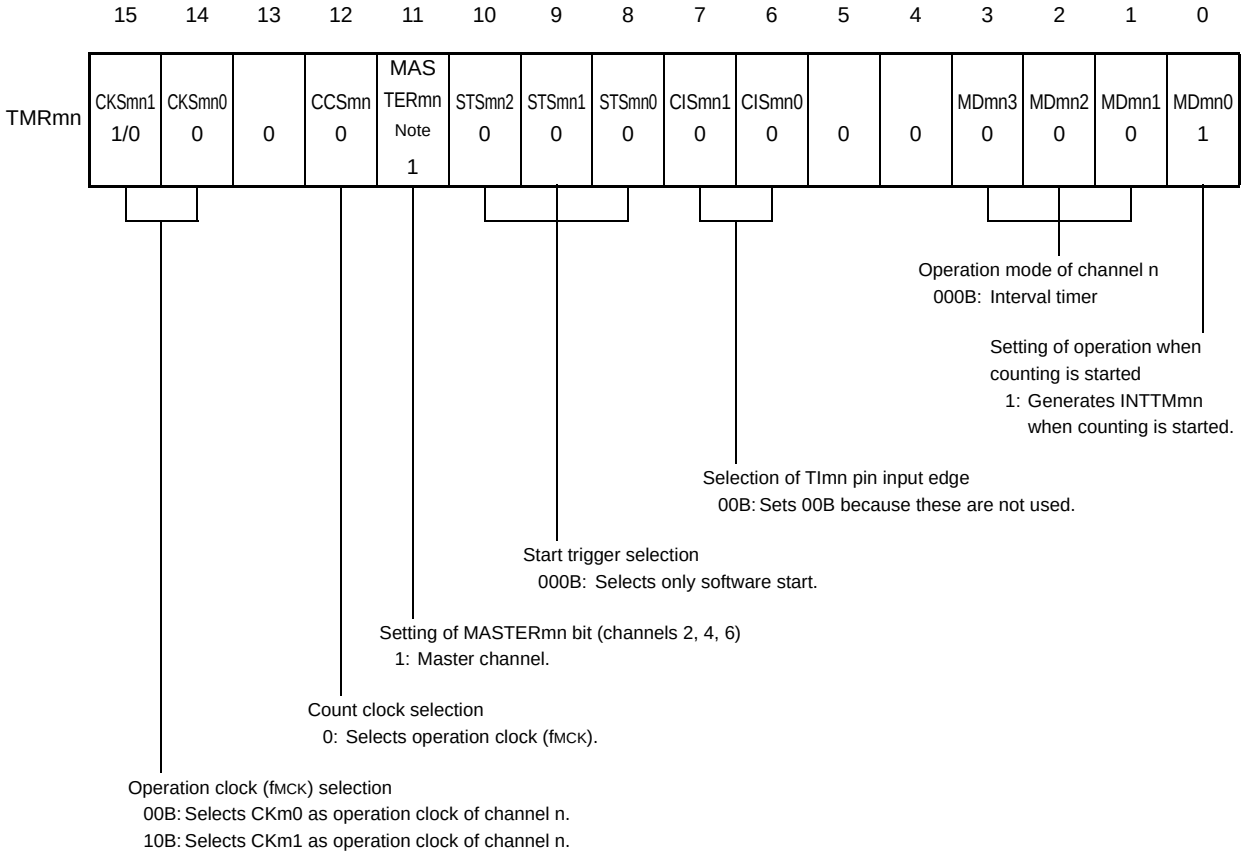


Remark 1. m: Unit number (m = 0), n: Channel number (n = 0, 2, 4, 6)
p: Slave channel number (n < p ≤ 7)

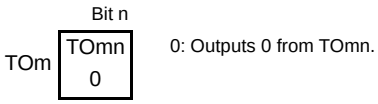
Remark 2. TSmn, TSmp: Bit n, p of timer channel start register m (TSm)
TEmn, TEmp: Bit n, p of timer channel enable status register m (TEm)
TCRmn, TCRmp: Timer count registers mn, mp (TCRmn, TCRmp)
TDRmn, TDRmp: Timer data registers mn, mp (TDRmn, TDRmp)
TOmn, TOmp: TOmn and TOmp pins output signal

Figure 6 - 73 Example of Set Contents of Registers When PWM Function (Master Channel) Is Used

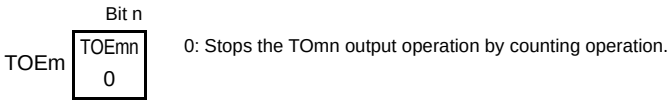
(a) Timer mode register mn (TMRmn)



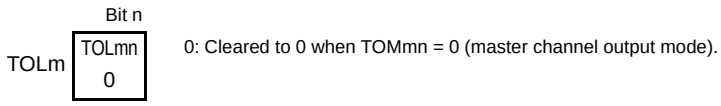
(b) Timer output register m (TOm)



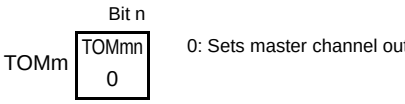
(c) Timer output enable register m (TOEm)



(d) Timer output level register m (TOLm)



(e) Timer output mode register m (TOMm)

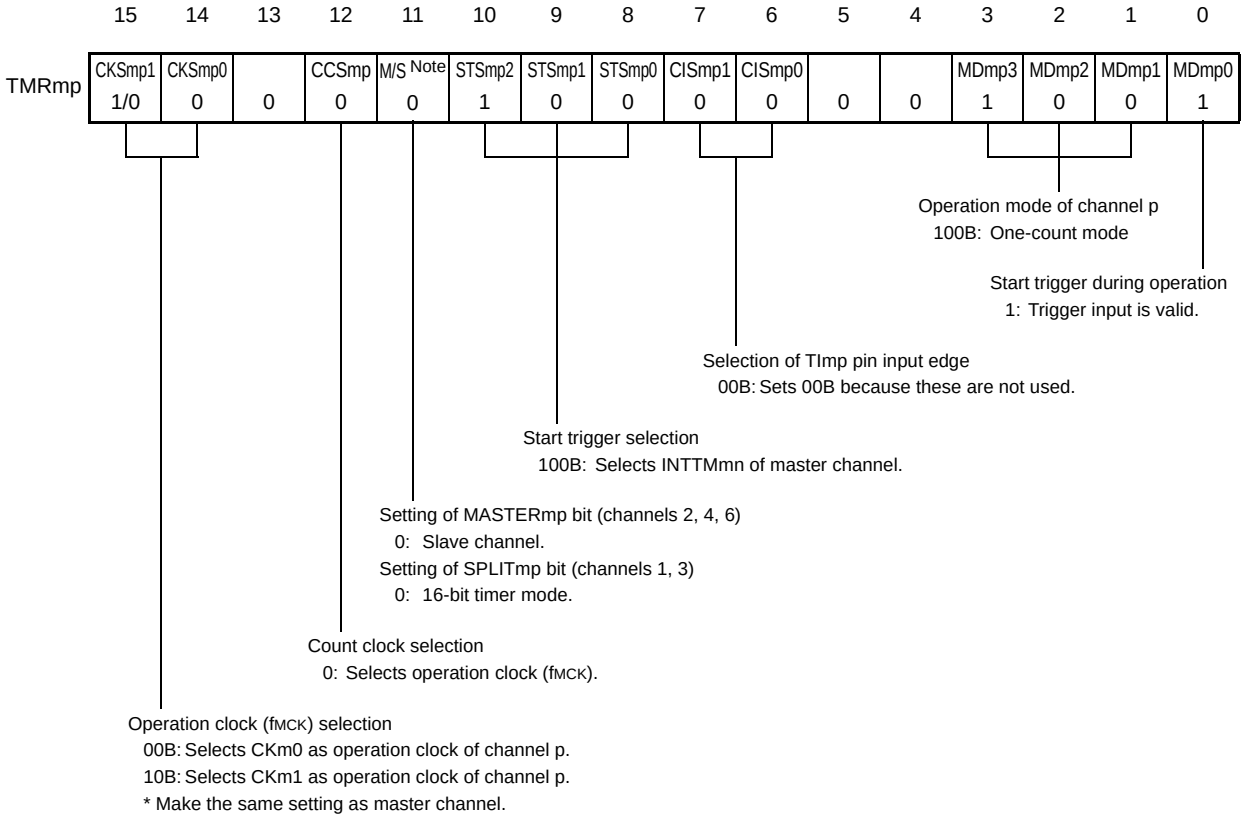


Note TMRm2, TMRm4, TMRm6: MASTERmn = 1
TMRm0: Fixed to 0

Remark m: Unit number (m = 0), n: Channel number (n = 0, 2, 4, 6)

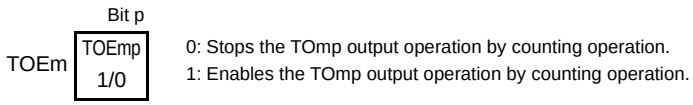
Figure 6 - 74 Example of Set Contents of Registers When PWM Function (Slave Channel) Is Used

(a) Timer mode register mp (TMRmp)

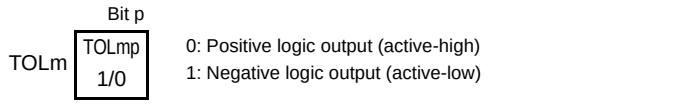


(b) Timer output register m (TOm)

(c) Timer output enable register m (TOEm)



(d) Timer output level register m (TOLm)



(e) Timer output mode register m (TOMm)

Note TMRm2, TMRm4 TMRm6: MASTERmn bit
TMRm1, TMRm3: SPLITmp bit
TMRm5, TMRm7: Fixed to 0

Remark m: Unit number (m = 0), n: Channel number (n = 0, 2, 4, 6)
p: Slave channel number (n < p ≤ 7)

Figure 6 - 75 Operation Procedure When PWM Function Is Used (1/2)

	Software Operation	Hardware Status
TAU default setting		Power-off status (Clock supply is stopped and writing to each register is disabled.)
	Sets the TAUmEN bit of peripheral enable register 0 (PER0) to 1. →	Power-on status. Each channel stops operating. (Clock supply is started and writing to each register is enabled.)
	Sets timer clock select register m (TPSm). Determines clock frequencies of CKm0 and CKm1.	
Channel default setting	Sets timer mode registers mn, mp (TMRmn, TMRmp) of two channels to be used (determines operation mode of channels). An interval (period) value is set to timer data register mn (TDRmn) of the master channel, and a duty factor is set to the TDRmp register of the slave channel.	Channel stops operating. (Clock is supplied and some power is consumed.)
	Sets slave channel. The TOMmp bit of timer output mode register m (TOMm) is set to 1 (slave channel output mode). Sets the TOLmp bit. Sets the TOmp bit and determines default level of the TOmp output. →	The TOmp pin goes into Hi-Z output state. The TOmp default setting level is output when the port mode register is in output mode and the port register is 0.
	Sets the TOEmp bit to 1 and enables operation of TOmp. →	TOmp does not change because channel stops operating.
	Clears the port register and port mode register to 0. →	The TOmp pin outputs the TOmp set level.

(**Remark** is listed on the next page.)

Figure 6 - 75 Operation Procedure When PWM Function Is Used (2/2)

Operation is resumed.

	Software Operation	Hardware Status
Operation start	Sets the TOEmp bit (slave) to 1 (only when operation is resumed). The TSmn (master) and TSmp (slave) bits of timer channel start register m (TSm) are set to 1 at the same time. → The TSmn and TSmp bits automatically return to 0 because they are trigger bits.	TEmn = 1, TEmp = 1 → When the master channel starts counting, INTTMmn is generated. Triggered by this interrupt, the slave channel also starts counting.
During operation	Set values of the TMRmn and TMRmp registers, TOMmn, TOMmp, TOLmn, and TOLmp bits cannot be changed. Set values of the TDRmn and TDRmp registers can be changed after INTTMmn of the master channel is generated. The TCRmn and TCRmp registers can always be read. The TSRmn and TSRmp registers are not used.	The counter of the master channel loads the TDRmn register value to timer count register mn (TCRmn), and counts down. When the count value reaches TCRmn = 0000H, INTTMmn output is generated. At the same time, the value of the TDRmn register is loaded to the TCRmn register, and the counter starts counting down again. At the slave channel, the value of the TDRmp register is loaded to the TCRmp register, triggered by INTTMmn of the master channel, and the counter starts counting down. The output level of TOmp becomes active one count clock after generation of the INTTMmn output from the master channel. It becomes inactive when TCRmp = 0000H, and the counting operation is stopped. After that, the above operation is repeated.
Operation stop	The TTmn (master) and TTmp (slave) bits are set to 1 at the same time. → The TTmn and TTmp bits automatically return to 0 because they are trigger bits.	TEmn, TEmp = 0, and count operation stops. The TCRmn and TCRmp registers hold count value and stop. The TOmp output is not initialized but holds current status.
	The TOEmp bit of slave channel is cleared to 0 and value is set to the TOmp bit. →	The TOmp pin outputs the TOmp set level.
TAU stop	To hold the TOmp pin output level Clears the TOmp bit to 0 after the value to be held is set to the port register. →	The TOmp pin output level is held by port function.
	When holding the TOmp pin output level is not necessary Setting not required.	
	The TAUmEN bit of the PER0 register is cleared to 0. →	Power-off status All circuits are initialized and SFR of each channel is also initialized. (The TOmp bit is cleared to 0 and the TOmp pin is set to port mode.)

Remark m: Unit number (m = 0), n: Channel number (n = 0, 2, 4, 6)
p: Slave channel number (n < p ≤ 7)

6.9.3 Operation as multiple PWM output function

By extending the PWM function and using multiple slave channels, many PWM waveforms with different duty values can be output.

For example, when using two slave channels, the period and duty factor of an output pulse can be calculated by the following expressions.

Pulse period = {Set value of TDRmn (master) + 1} × Count clock period
Duty factor 1 [%] = {Set value of TDRmp (slave 1)}/{Set value of TDRmn (master) + 1} × 100
Duty factor 2 [%] = {Set value of TDRmq (slave 2)}/{Set value of TDRmn (master) + 1} × 100

Remark Although the duty factor exceeds 100% if the set value of TDRmp (slave 1) > {set value of TDRmn (master) + 1} or if the {set value of TDRmq (slave 2)} > {set value of TDRmn (master) + 1}, it is summarized into 100% output.

Timer count register mn (TCRmn) of the master channel operates in the interval timer mode and counts the periods.

The TCRmp register of the slave channel 1 operates in one-count mode, counts the duty factor, and outputs a PWM waveform from the TOmp pin. The TCRmp register loads the value of timer data register mp (TDRmp), using INTTMmn of the master channel as a start trigger, and starts counting down. When TCRmp = 0000H, TCRmp outputs INTTMmp and stops counting until the next start trigger (INTTMmn of the master channel) has been input. The output level of TOmp becomes active one count clock after generation of INTTMmn from the master channel, and inactive when TCRmp = 0000H.

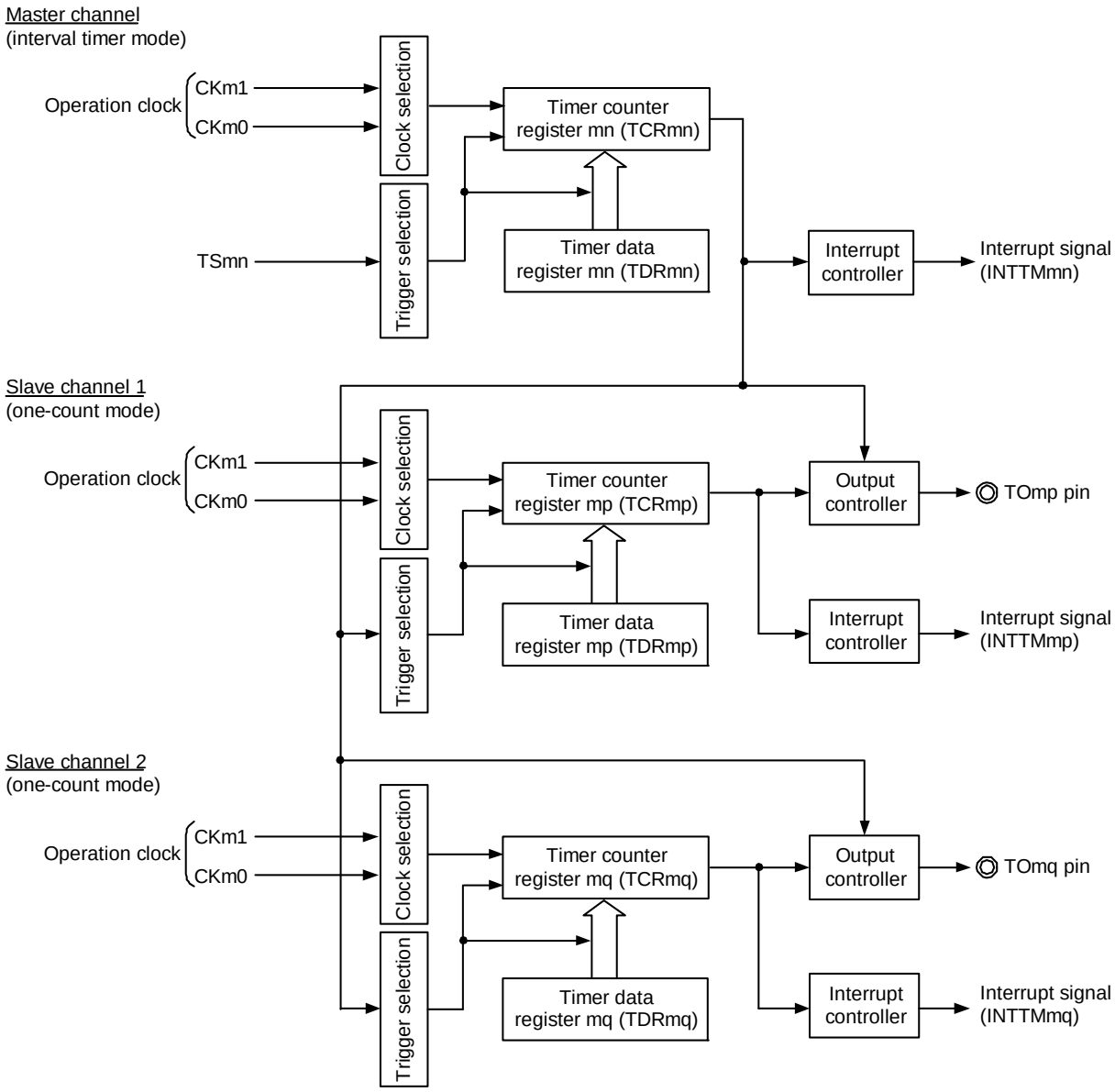
In the same way as the TCRmp register of the slave channel 1, the TCRmq register of the slave channel 2 operates in one-count mode, counts the duty factor, and outputs a PWM waveform from the TOmq pin. The TCRmq register loads the value of the TDRmq register, using INTTMmn of the master channel as a start trigger, and starts counting down. When TCRmq = 0000H, the TCRmq register outputs INTTMmq and stops counting until the next start trigger (INTTMmn of the master channel) has been input. The output level of TOmq becomes active one count clock after generation of INTTMmn from the master channel, and inactive when TCRmq = 0000H.

When channel 0 is used as the master channel as above, up to seven types of PWM signals can be output at the same time.

Caution **To rewrite both timer data register mn (TDRmn) of the master channel and the TDRmp register of the slave channel 1, write access is necessary at least twice. Since the values of the TDRmn and TDRmp registers are loaded to the TCRmn and TCRmp registers after INTTMmn is generated from the master channel, if rewriting is performed separately before and after generation of INTTMmn from the master channel, the TOmp pin cannot output the expected waveform. To rewrite both the TDRmn register of the master and the TDRmp register of the slave, be sure to rewrite both the registers immediately after INTTMmn is generated from the master channel (This applies also to the TDRmq register of the slave channel 2).**

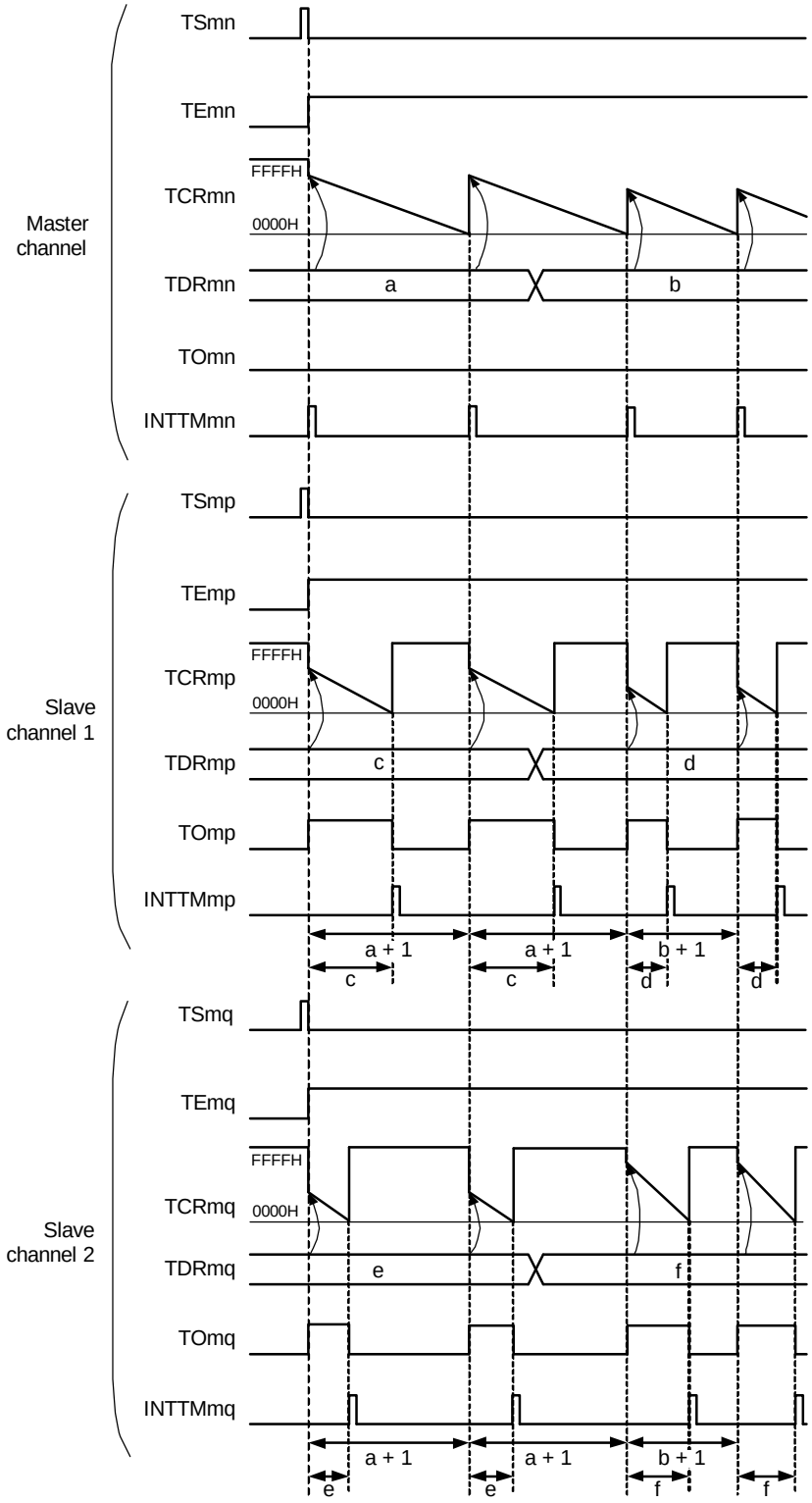
Remark m: Unit number (m = 0), n: Channel number (n = 0, 2, 4)
p: Slave channel number 1, q: Slave channel number 2
n < p < q ≤ 7 (Where p and q are integers greater than n)

Figure 6 - 76 Block Diagram of Operation as Multiple PWM Output Function (output two types of PWMs)



Remark m: Unit number (m = 0), n: Channel number (n = 0, 2, 4)
p: Slave channel number 1, q: Slave channel number 2
n < p < q ≤ 7 (Where p and q are integers greater than n)

Figure 6 - 77 Example of Basic Timing of Operation as Multiple PWM Output Function (Output two types of PWMs)



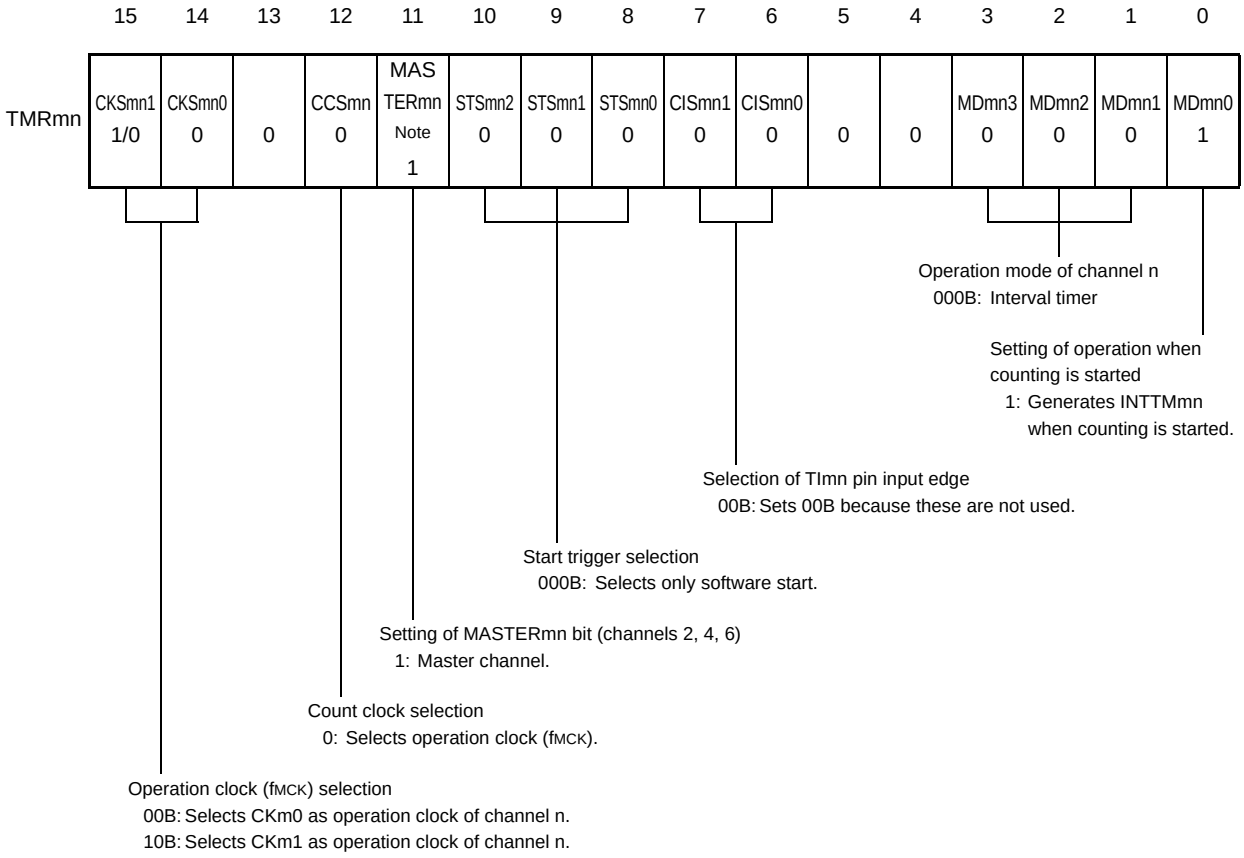
(**Remark** is listed on the next page.)

Remark 1. m: Unit number (m = 0), n: Channel number (n = 0, 2, 4)
p: Slave channel number 1, q: Slave channel number 2
n < p < q ≤ 7 (Where p and q are integers greater than n)

Remark 2. TSmn, TSmp, TSmq: Bit n, p, q of timer channel start register m (TSm)
TEmn, TEmp, TEmq: Bit n, p, q of timer channel enable status register m (TEm)
TCRmn, TCRmp, TCRmq: Timer count registers mn, mp, mq (TCRmn, TCRmp, TCRmq)
TDRmn, TDRmp, TDRmq: Timer data registers mn, mp, mq (TDRmn, TDRmp, TDRmq)
TOmn, TOmp, TOmq: TOmn, TOmp, and TOmq pins output signal

Figure 6 - 78 Example of Set Contents of Registers
When Multiple PWM Output Function (Master Channel) Is Used

(a) Timer mode register mn (TMRmn)



(b) Timer output register m (TOm)

	Bit n	
TOm	TOmn 0	0: Outputs 0 from TOmn.

(c) Timer output enable register m (TOEm)

	Bit n	
TOEm	TOEmn 0	0: Stops the TOmn output operation by counting operation.

(d) Timer output level register m (TOLm)

	Bit n	
TOLm	TOLmn 0	0: Cleared to 0 when TOMmn = 0 (master channel output mode).

(e) Timer output mode register m (TOMm)

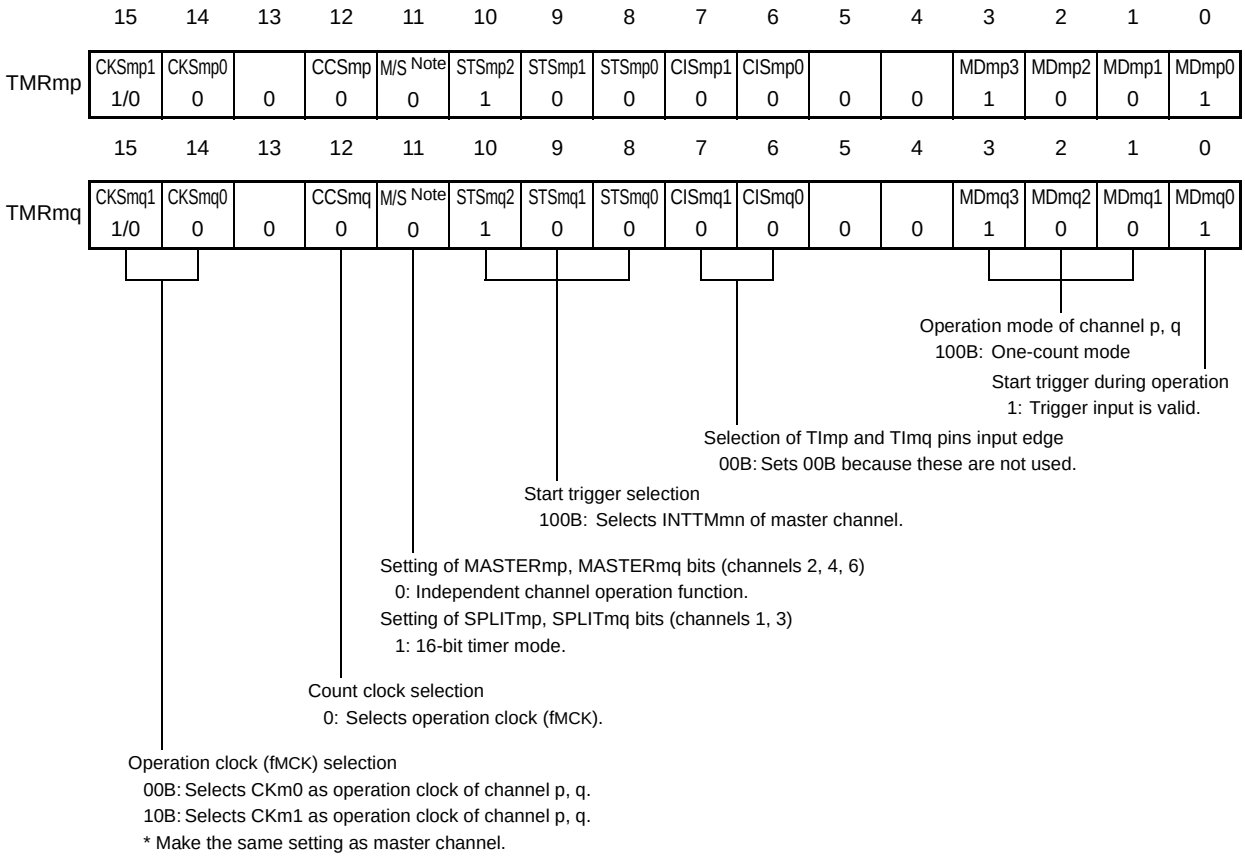
	Bit n	
TOMm	TOMmn 0	0: Sets master channel output mode.

Note TMRm2, TMRm4, TMRm6: MASTERmn = 1
TMRm0: Fixed to 0

Remark m: Unit number (m = 0), n: Channel number (n = 0, 2, 4)

Figure 6 - 79 Example of Set Contents of Registers
When Multiple PWM Output Function (Slave Channel) Is Used (output two types of PWMs)

(a) Timer mode register mp, mq (TMRmp, TMRmq)



(b) Timer output register m (TOm)

Bit q Bit p

TOm	TOmq	TOmp
	1/0	1/0

0: Outputs 0 from TOmp or TOmq.
1: Outputs 1 from TOmp or TOmq.

(c) Timer output enable register m (TOEm)

Bit q Bit p

TOEm	TOEmq	TOEmp
	1/0	1/0

0: Stops the TOmp or TOmq output operation by counting operation.
1: Enables the TOmp or TOmq output operation by counting operation.

(d) Timer output level register m (TOLm)

Bit q Bit p

TOLm	TOLmq	TOLmp
	1/0	1/0

0: Positive logic output (active-high)
1: Negative logic output (active-low)

(e) Timer output mode register m (TOMm)

Bit q Bit p

TOMm	TOMmq	TOMmp
	1	1

1: Sets the slave channel output mode.

Note TMRm2, TMRm4, TMRm6: MASTERmp, MASTERmq bit
TMRm1, TMRm3: SPLITmp, SPLIT0q bit
TMRm5, TMRm7: Fixed to 0

Remark m: Unit number (m = 0), n: Channel number (n = 0, 2, 4)
p: Slave channel number 1, q: Slave channel number 2
n < p < q ≤ 7 (Where p and q are integers greater than n)

Figure 6 - 80 Operation Procedure When Multiple PWM Output Function Is Used (output two types of PWMs) (1/2)

	Software Operation	Hardware Status
TAU default setting		Power-off status (Clock supply is stopped and writing to each register is disabled.)
	Sets the TAUmEN bit of peripheral enable register 0 (PER0) to 1. →	Power-on status. Each channel stops operating. (Clock supply is started and writing to each register is enabled.)
	Sets timer clock select register m (TPSm). Determines clock frequencies of CKm0 and CKm1.	
Channel default setting	Sets timer mode registers mn, mp, mq (TMRmn, TMRmp, TMRmq) of each channel to be used (determines operation mode of channels). An interval (period) value is set to timer data register mn (TDRmn) of the master channel, and a duty factor is set to the TDRmp and TDRmq registers of the slave channels.	Channel stops operating. (Clock is supplied and some power is consumed.)
	Sets slave channels. The TOMmp and TOMmq bits of timer output mode register m (TOMm) are set to 1 (slave channel output mode). Clears the TOLmp and TOLmq bits to 0. Sets the TOmp and TOmq bits and determines default level of the TOmp and TOmq outputs. →	The TOmp and TOmq pins go into Hi-Z output state. The TOmp and TOmq default setting levels are output when the port mode register is in output mode and the port register is 0.
	Sets the TOEmp and TOEmq bits to 1 and enables operation of TOmp and TOmq. →	TOmp and TOmq do not change because channels stop operating.
	Clears the port register and port mode register to 0. →	The TOmp and TOmq pins output the TOmp and TOmq set levels.

(**Remark** is listed on the next page.)

Figure 6 - 80 Operation Procedure When Multiple PWM Output Function Is Used (output two types of PWMs) (2/2)

	Software Operation	Hardware Status
Operation start	(Sets the TOEmp and TOEmq (slave) bits to 1 only when resuming operation.) The TSmn bit (master), and TSmp and TSmq (slave) bits of timer channel start register m (TSm) are set to 1 at the same time. →	TEmn = 1, TEmp, TEmq = 1 When the master channel starts counting, INTTMmn is generated. Triggered by this interrupt, the slave channel also starts counting.
	The TSmn, TSmp, and TSmq bits automatically return to 0 because they are trigger bits.	
During operation	Set values of the TMRmn, TMRmp, TMRmq registers, TOMmn, TOMmp, TOMmq, TOLmn, TOLmp, and TOLmq bits cannot be changed. Set values of the TDRmn, TDRmp, and TDRmq registers can be changed after INTTMmn of the master channel is generated. The TCRmn, TCRmp, and TCRmq registers can always be read. The TSRmn, TSRmp, and TSRmq registers are not used.	The counter of the master channel loads the TDRmn register value to timer count register mn (TCRmn) and counts down. When the count value reaches TCRmn = 0000H, INTTMmn output is generated. At the same time, the value of the TDRmn register is loaded to the TCRmn register, and the counter starts counting down again. At the slave channel 1, the values of the TDRmp register are transferred to the TCRmp register, triggered by INTTMmn of the master channel, and the counter starts counting down. The output levels of TOmp become active one count clock after generation of the INTTMmn output from the master channel. It becomes inactive when TCRmp = 0000H, and the counting operation is stopped. At the slave channel 2, the values of the TDRmq register are transferred to TCRmq register, triggered by INTTMmn of the master channel, and the counter starts counting down. The output levels of TOmq become active one count clock after generation of the INTTMmn output from the master channel. It becomes inactive when TCRmq = 0000H, and the counting operation is stopped. After that, the above operation is repeated.
Operation stop	The TTmn bit (master), TTmp, and TTmq (slave) bits are set to 1 at the same time. →	TEmn, TEmp, TEmq = 0, and count operation stops. The TCRmn, TCRmp, and TCRmq registers hold count value and stop. The TOmp and TOmq output are not initialized but hold current status.
	The TTmn, TTmp, and TTmq bits automatically return to 0 because they are trigger bits.	
	The TOEmp and TOEmq bits of slave channels are cleared to 0 and value is set to the TOmp and TOmq bits. →	The TOmp and TOmq pins output the TOmp and TOmq set levels.
TAU stop	To hold the TOmp and TOmq pin output levels Clears the TOmp and TOmq bits to 0 after the value to be held is set to the port register. →	The TOmp and TOmq pin output levels are held by port function.
	When holding the TOmp and TOmq pin output levels are not necessary Setting not required	
	The TAUmEN bit of the PER0 register is cleared to 0. →	Power-off status All circuits are initialized and SFR of each channel is also initialized. (The TOmp and TOmq bits are cleared to 0 and the TOmp and TOmq pins are set to port mode.)

Operation is resumed.

Remark m: Unit number (m = 0), n: Channel number (n = 0, 2, 4)
p: Slave channel number, q: Slave channel number
n < p < q ≤ 7 (Where p and q are integer greater than n)

6.10 Cautions When Using Timer Array Unit

6.10.1 Cautions When Using Timer output

Depends on products, a pin is assigned a timer output and other alternate functions. In this case, outputs of the other alternate functions must be set in initial status.

For details, see **4.6 Register Settings When Using Alternate Function**.

When the non-divided clock is selected for the timer array unit and TDR0n (n = 0 to 7) is set to 0000H, the interrupt signal output is fixed to the high level, so interrupt requests cannot be detected.

CHAPTER 7 8-BIT INTERVAL TIMER

The 8-bit interval timer has two 8-bit timers (channel 0 and channel 1) which operate independently. These timers can be connected to operate as a 16-bit timer.
The number of units and channels supported by the RL78/H1D depends on the product.

Unit	Channel	R5F11N, R5F11P	R5F11R
Unit 0	Channel 0	√	√
	Channel 1	√	√
Unit 1	Channel 0	—	√
	Channel 1	—	√
Unit 2	Channel 0	—	√
	Channel 1	—	√

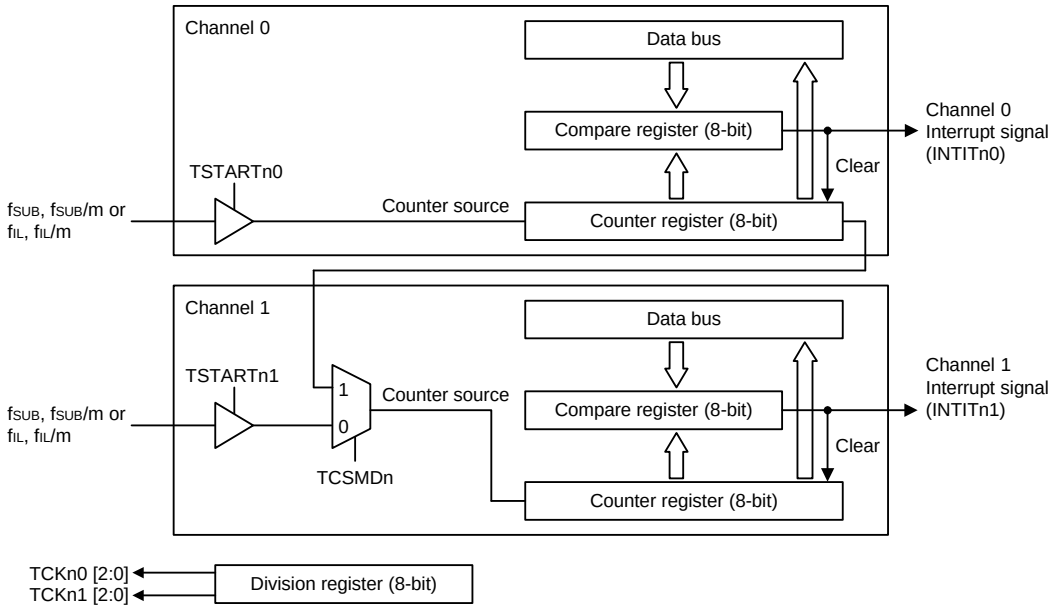
7.1 Overview

The 8-bit interval timer is an 8-bit timer that operates using the f_{SUB} or f_{IL} clock that is asynchronous with the CPU.
Table 7 - 1 lists the 8-Bit Interval Timer Specifications and Figure 7 - 1 shows the 8-Bit Interval Timer Block Diagram.

Table 7 - 1 8-Bit Interval Timer Specifications

Item	Description
Count source (operating clock)	• f_{SUB}, $f_{SUB}/2$, $f_{SUB}/4$, $f_{SUB}/8$, $f_{SUB}/16$, $f_{SUB}/32$, $f_{SUB}/64$, $f_{SUB}/128$ • f_{IL}, $f_{IL}/2$, $f_{IL}/4$, $f_{IL}/8$, $f_{IL}/16$, $f_{IL}/32$, $f_{IL}/64$, $f_{IL}/128$
Operating mode	• 8-bit counter mode Channel 0 and channel 1 operate independently as an 8-bit counter • 16-bit counter mode Channel 0 and channel 1 are connected to operate as a 16-bit counter
Interrupt	• Output when the counter matches the compare value

Figure 7 - 1 8-Bit Interval Timer Block Diagram



TSTARTni (i = 0, 1), TCSMDn, TCLKENn: Bits in TRTCRn register
TCKni [2:0]: Bit in TRTMDn register

Remark m = 2, 4, 8, 16, 32, 64, 128
n: Unit number (n = 0 to 2)

7.2 I/O Pins

The 8-bit interval timer does not have an I/O pin.

7.3 Registers

Table 7 - 2 lists the 8-bit interval timer register configuration.

Table 7 - 2 Registers

Register Name	Symbol
8-bit interval timer counter register n0	TRTn0 Note 1
8-bit interval timer counter register n1	TRTn1 Note 1
8-bit interval timer counter register n	TRTn Note 2
8-bit interval timer compare register n0	TRTCMPn0 Note 1
8-bit interval timer compare register n1	TRTCMPn1 Note 1
8-bit interval timer compare register n	TRTCMPn Note 2
8-bit interval timer control register n	TRTCRn
8-bit interval timer division register n	TRTMDn

Note 1. Can be accessed only when the TCSMDn bit in the TRTCRn register = 0.

Note 2. Can be accessed only when the TCSMDn bit in the TRTCRn register = 1.

Remark n: Unit number (n = 0 to 2)

7.3.1 8-bit interval timer counter register ni (TRTni)

This is the 8-bit interval timer counter register. It is used as a counter that counts up based on the count clock.

The TRTni register can be set by an 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 7 - 2 Format of 8-bit interval timer counter register ni (TRTni)

Address: F0500H (TRT00), F0501H (TRT01), F0502H (TRT10), F0503H (TRT11), F0504H (TRT20), F0505H (TRT21) — After reset: 00H — R Notes 1, 2

Symbol	7	6	5	4	3	2	1	0
TRTni								

Note 1. The TRTni register is set to 00H two cycles of the count clock after the compare register TRTCMPni is write-accessed. Refer to **7.4.4 Timing for updating compare register values**.

Note 2. Can be accessed only when the mode select bit (TCSMDn) in the 8-bit interval timer control register n (TRTCRn) is 0.

Remark n: Unit number (n = 0 to 2), i: Channel number (n = 0, 1)

7.3.2 8-bit interval timer counter register n (TRTn)

This is a 16-bit counter register when the 8-bit interval timer is used in 16-bit interval timer mode.

The TRTn register can be set by a 16-bit memory manipulation instruction.

Reset signal generation sets this register to 0000H.

Figure 7 - 3 Format of 8-bit interval timer counter register n (TRTn)

Address: F0500H (TRT0), F0502H (TRT1), F0504H (TRT2) — After reset: 0000H — R Notes 1, 2

	F0501H (TRT01), F0503H (TRT11), F0505H (TRT21)								F0500H (TRT00), F0502H (TRT10), F0504H (TRT20)							
Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TRTn																

Note 1. The TRTn register is set to 0000H two cycles of the count clock after the compare register TRTCMPn is write-accessed. Refer to **7.4.4 Timing for updating compare register values**.

Note 2. Can be accessed only when the mode select bit (TCSMDn) in the 8-bit interval timer control register n (TRTCRn) is 0.

Remark n: Unit number (n = 0 to 2)

7.3.3 8-bit interval timer compare register ni (TRTCMPni)

This is the 8-bit interval timer compare value register.

The TRTCMPni register can be set by an 8-bit memory manipulation instruction.

Reset signal generation sets this register to FFH.

The setting range is 01H to FFH Note 1.

This register is used to store the compare value of registers TRTn0 and TRTn1 (counters).

Write-access clears the count value (TRTn0, TRTn1) to 00H.

Refer to **7.4.4 Timing for updating compare register values** for the timing of rewriting the compare value.

Figure 7 - 4 Format of 8-bit interval timer compare register ni (TRTCMPni)

Address: F0350H (TRTCMP00), F0351H (TRTCMP01), F0354H (TRTCMP10), F0355H (TRTCMP11), F0358H (TRTCMP20), F0359H (TRTCMP21) After reset: FFH R/W Notes 1, 2

Symbol	7	6	5	4	3	2	1	0
TRTCMPni								

Note 1. The TRTCMPni register must not be set to 00H.

Note 2. Can be accessed only when the mode select bit (TCSMDn) in the 8-bit interval timer control register n (TRTCRn) is 0.

Remark n: Unit number (n = 0 to 2), i: Channel number (n = 0, 1)

7.3.4 8-bit interval timer compare register n (TRTCMPn)

This is a compare value register when the 8-bit interval timer is used in 16-bit interval timer mode.

The TRTCMPn register can be set by a 16-bit memory manipulation instruction.

Reset signal generation sets this register to FFFFH.

The setting is 0001H to FFFFH Note 1.

This register is used to store the compare value of the TRTn register (counter).

Write-access clears the count value (TRTn) to 0000H.

Refer to **7.4.4 Timing for updating compare register values** for the timing of rewriting the compare value.

Figure 7 - 5 Format of 8-bit interval timer compare register n (TRTCMPn)

Address: F0350H (TRTCMP0), F0354H (TRTCMP1), F0358H (TRTCMP2) After reset: FFFFH R/W Note 2

	F0351H (TRTCMP01), F0355H (TRTCMP11), F0359H (TRTCMP21)								F0350H (TRTCMP00), F0354H (TRTCMP10), F0358H (TRTCMP20)							
Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TRTCMPn																

Note 1. The TRTCMPn register must not be set to 0000H.

Note 2. Can be accessed only when the mode select bit (TCSMDn) in the 8-bit interval timer control register n (TRTCRn) is 1.

Remark n: Unit number (n = 0 to 2)

7.3.5 8-bit interval timer control register n (TRTCRn)

This register is used to start and stop counting by the 8-bit interval timer and to switch between using the 8-bit interval timer as an 8-bit counter or a 16-bit counter.

The TRTCRn register can be set by a 1-bit or 8-bit manipulation instruction.

Reset signal generation resets this register to 00H.

Figure 7 - 6 Format of 8-bit interval timer control register n (TRTCRn)

Address: F0352H (TRTCR0), F0356H (TRTCR1), F035AH (TRTCR2) After reset: 00H R/W Note 3

Symbol	7	6	5	4	3	<2>	1	<0>
TRTCRn	TCSMDn	0	0	TCLKENn	0	TSTARTn1	0	TSTARTn0

TCSMDn	Mode select
0	Operates as 8-bit counter
1	Operates as 16-bit counter (channel 0 and channel 1 are connected)
Refer to **7.4 Operation** for details.	

TCLKENn	8-bit interval timer clock enable Note 1
0	Clock is stopped
1	Clock is supplied

TSTARTn1	8-bit interval timer 1 count start Notes 1, 2
0	Count stops
1	Count starts
In 8-bit interval timer mode, writing 1 to the TSTARTn1 bit starts the TRTn1 count and writing 0 stops the count. In 16-bit interval timer mode, this bit is invalid because it is not used. Refer to **7.4 Operation** for details.	

TSTARTn0	8-bit interval timer 0 count start Notes 1, 2
0	Count stops
1	Count starts
In 8-bit interval timer mode, writing 1 to the TSTARTn0 bit starts the TRTn0 count and writing 0 stops the count. In 16-bit interval timer mode, writing 1 to the TSTARTn0 bit starts the TRTn count and writing 0 stops the count. Refer to **7.4 Operation** for details.	

Note 1. Be sure to set the TCLKENn bit to 1 before setting the 8-bit interval timer. To stop the clock, set TSTARTn0 and TSTARTn1 to 0 and then set the TCLKENn bit to 0 after one or more cycles of the operating clock (f_{SUB} or f_{IL}) have elapsed. Refer to **7.5.3 8-bit interval timer setting procedure** for details.

Note 2. Refer to **7.5.1 Changing settings of operating mode** for the notes on using bits TSTARTn0, TSTARTn1, and TCSMDn.

Note 3. Bits 6, 5, 3, and 1 are read-only. When writing, write 0. When reading, 0 is read.

Remark n: Unit number (n = 0 to 2)

7.3.6 8-bit interval timer division register n (TRTMDn)

This register is used to select the division ratio of the count source used by the 8-bit interval timer.

The TRTMDn register can be set by an 8-bit memory manipulation instruction.

Reset signal generation sets this register to 00H.

Figure 7 - 7 Format of 8-bit interval timer division register n (TRTMDn)

Address: F0353H (TRTMD0), F0357H (TRTMD1), F035BH (TRTMD2) After reset: 00H R/W Note 4

Symbol	7	6	5	4	3	2	1	0
TRTMDn	—	TCKn1			—	TCKn0		

TCKn1			8-bit interval timer 1 division select Notes 1, 2, 3
Bit 6	Bit 5	Bit 4	
0	0	0	f_{SUB} or f_{IL}
0	0	1	$f_{SUB}/2$ or $f_{IL}/2$
0	1	0	$f_{SUB}/4$ or $f_{IL}/4$
0	1	1	$f_{SUB}/8$ or $f_{IL}/8$
1	0	0	$f_{SUB}/16$ or $f_{IL}/16$
1	0	1	$f_{SUB}/32$ or $f_{IL}/32$
1	1	0	$f_{SUB}/64$ or $f_{IL}/64$
1	1	1	$f_{SUB}/128$ or $f_{IL}/128$
In 8-bit interval timer mode, TRTn1 counts using the count source set in TCKn1. In 16-bit interval timer mode, set these bits to 000 because they are not used. Refer to **7.4 Operation** for details.			

TCKn0			8-bit interval timer 0 division select Notes 1, 2, 3
Bit 2	Bit 1	Bit 0	
0	0	0	f_{SUB} or f_{IL}
0	0	1	$f_{SUB}/2$ or $f_{IL}/2$
0	1	0	$f_{SUB}/4$ or $f_{IL}/4$
0	1	1	$f_{SUB}/8$ or $f_{IL}/8$
1	0	0	$f_{SUB}/16$ or $f_{IL}/16$
1	0	1	$f_{SUB}/32$ or $f_{IL}/32$
1	1	0	$f_{SUB}/64$ or $f_{IL}/64$
1	1	1	$f_{SUB}/128$ or $f_{IL}/128$
In 8-bit interval timer mode, TRTn0 counts using the count source set in TCKn0. In 16-bit interval timer mode, TRTn counts using the count source set in TCKn0. Refer to **7.4 Operation** for details.			

Note 1. Do not switch the count source during count operation. When switching the count source, set these bits while the TSTARTni bit in the TRTCRn register is 0 (count stops).

Note 2. Set TCKni of the unused channel to 000B.

Note 3. Be sure to set the TCKni (i = 0, 1) bit before setting the TRTCMPni register.

Note 4. Bits 7 and 3 are read-only. When writing, write 0. When reading, 0 is read.

Remark n: Unit number (n = 0 to 2)

7.4 Operation

7.4.1 Count mode

The following two modes are supported: 8-bit counter mode and 16-bit counter mode. Table 7 - 3 lists the Registers and Settings Used in 8-Bit Counter Mode and Table 7 - 4 lists the Registers and Settings Used in 16-Bit Counter Mode.

Table 7 - 3 Registers and Settings Used in 8-Bit Counter Mode

Register Name (Symbol)	Bit	Function
8-bit interval timer counter register n0 (TRTn0)	b7 to b0	8-bit counter of channel 0. The count value can be read.
8-bit interval timer counter register n1 (TRTn1)	b7 to b0	8-bit counter of channel 1. The count value can be read.
8-bit interval timer compare register n0 (TRTCMPn0)	b7 to b0	8-bit compare value of channel 0. Set the compare value.
8-bit interval timer compare register n1 (TRTCMPn1)	b7 to b0	8-bit compare value of channel 1. Set the compare value.
8-bit interval timer control register n (TRTCRn)	TSTARTn0	Select whether to start/stop the count of channel 0.
	TSTARTn1	Select whether to start/stop the count of channel 1.
	TCLKENn	Set to 1.
	TCSMDn	Set to 0.
8-bit interval timer division register n (TRTMDn)	TCKn0	Select the count clock of channel 0.
	TCKn1	Select the count clock of channel 1.

Remark n: Unit number (n = 0 to 2)

Table 7 - 4 Registers and Settings Used in 16-Bit Counter Mode

Register Name (Symbol)	Bit	Function
8-bit interval timer counter register n (TRTn)	b15 to b0	16-bit counter. The count value can be read.
8-bit interval timer compare register n (TRTCMPn)	b15 to b0	16-bit compare value. Set the compare value.
8-bit interval timer control register n (TRTCRn)	TSTARTn0	Select whether to control starting/stopping the count.
	TSTARTn1	Set to 0.
	TCLKENn	Set to 1.
	TCSMDn	Set to 1.
8-bit interval timer division register n (TRTMDn)	TCKn0	Select the count clock.
	TCKn1	Set to 000B.

Remark n: Unit number (n = 0 to 2)

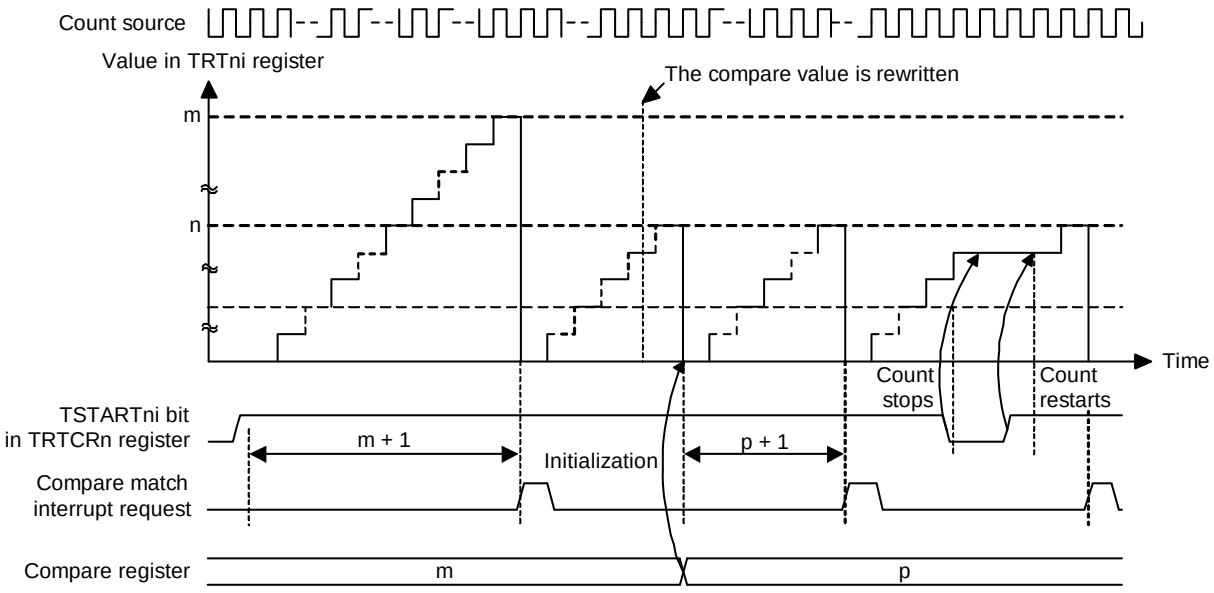
7.4.2 Timer operation

The counter is incremented by cycles of the source selected by the TCKni (n = 0 to 2, i = 0, 1) bits in the division register (TRTMDn). The counter value is incremented by one each time a cycle from the source is input. After the counter value reaches the value for comparison, matching of the values is detected on the input of the next cycle from the source, after which an interrupt is generated. The interrupt request takes the form of a single pulse synchronized with the source for counting.

Note that, when the TSTARTni bit in the TRTCRn register is set to 0 and counting is stopped at 00h, the interrupt signal (INTITnm) will be fixed to the high level. If the interrupt signal (INTITnm) is in use as an activating source for the data transfer controller or a source of events for the ELC in such cases, the activating source or event signal is continually generated.

When operation is stopped, the counter retains the value counted immediately before it stopped. To clear the value, set a value for comparison in the TRTCMPni register again. After writing to the TRTCMPni register, the counter value is cleared after two cycles of the source for counting.

Figure 7 - 8 Example of Timer Operation



Remark n: Unit number (n = 0 to 2), i: Channel number (i = 0, 1), m, p: Values set in TRTCMPni register

However, the initial 00H count interval when starting count varies as follows according to the timing 1 is written in the TSTARTni (i = 0, 1) bit of the TRTCR register.

- When the count source (f_{SUB} or f_{IL}) is selected
  Maximum: Two cycles of the count source
  Minimum: One cycle of the count source
- When the count source ($f_{SUB}/2^m$ or $f_{IL}/2^m$) is selected
  Maximum: One cycle of the count source
  Minimum: One cycle of the selected clock (f_{SUB} or f_{IL})

When the count value matches the compare value, the count value is cleared by the next count source. When the compare value in the TRTCMPni register is rewritten, the count value is also cleared two cycles of the count source after writing.

Table 7 - 5 lists the Interrupt Sources in 8-Bit/16-Bit Count Mode.

Table 7 - 5 Interrupt Sources in 8-Bit/16-Bit Count Mode

Interrupt Name	8-Bit Count Mode Source	16-Bit Count Mode Source
INTITn0	Rising edge of the next count source after compare match of channel 0	Rising edge of the next count source after compare match
INTITn1	Rising edge of the next count source after compare match of channel 1	Not generated

Remark n: Unit number (n = 0 to 2)

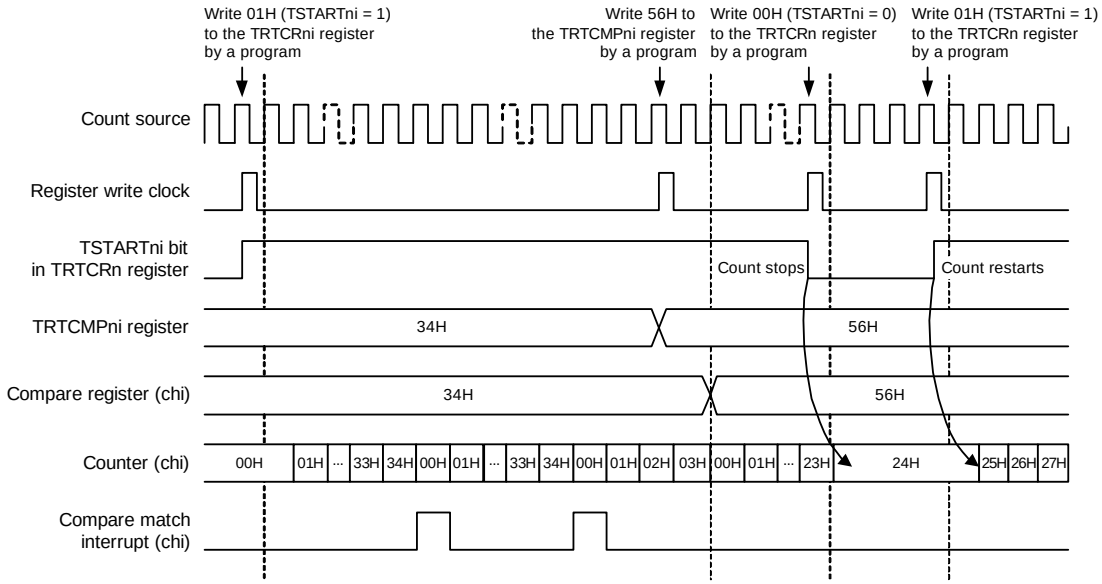
7.4.3 Start/stop timing

7.4.3.1 When count source (f_{SUB}) is selected

After 1 is written to the TSTARTni (n = 0, i = 0, 1) bit in the TRTCRn register, the count is started by the next subsystem clock (f_{SUB}), and then the counter is incremented from 00H to 01H by the next count source (f_{SUB}). Likewise, after 0 is written to the TSTARTni bit, the count is stopped after the counter is incremented by the subsystem clock (f_{SUB}).

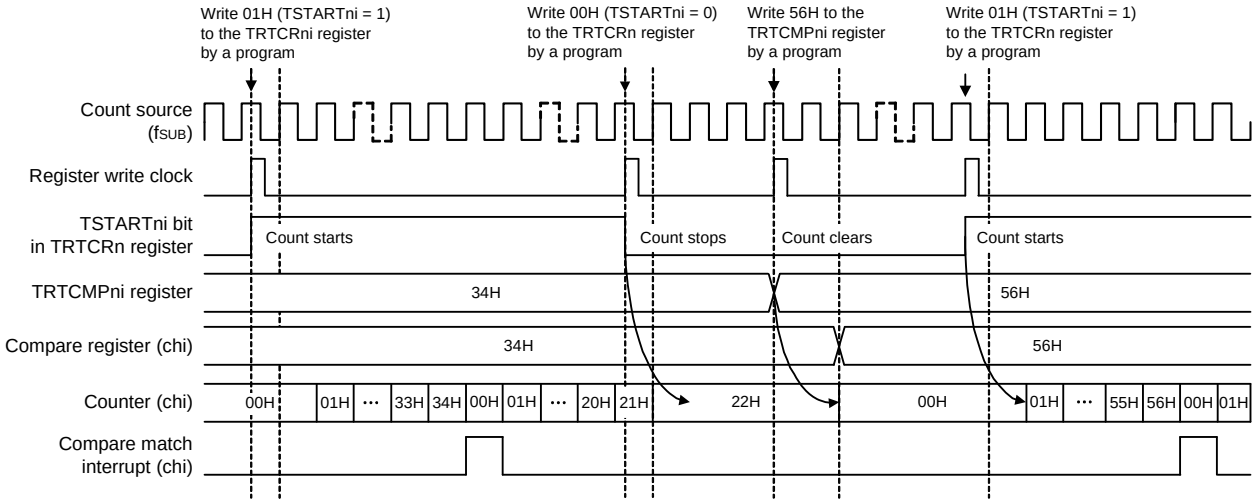
Figure 7 - 9 shows the timing for starting/stopping count operation, and Figure 7 - 10 shows the timing of count stop → compare setting (count clearing) → count start. Figure 7 - 9 and Figure 7 - 10 show the update timing in 8-bit counter mode, but operation is performed at the same timing even in 16-bit counter mode.

Figure 7 - 9 Example of Count Start/Stop Operation (f_{SUB} Selected)



Remark n: Unit number (n = 0 to 2), i: Channel number (n = 0, 1)

Figure 7 - 10 Example of Count Stop → Count Clearing → Count Start Operation (f_{SUB} Selected)



The TCSMDn bit in the TRTCRn register is set to 0 (8-bit counter operation)

Remark n: Unit number (n = 0 to 2), i: Channel number (n = 0, 1)

7.4.3.2 When count source ($f_{SUB}/2^m$) is selected

After 1 is written to the TSTARTni (n = 0 to 2, i = 0, 1) bit in the TRTCRn register, the count is started with the next subsystem clock (f_{SUB}), and then the counter is incremented from 00H to 01H by the next count source ($f_{SUB}/2^m$). Likewise, after 0 is written to the TSTARTni bit, the count is stopped with the subsystem clock (f_{SUB}).

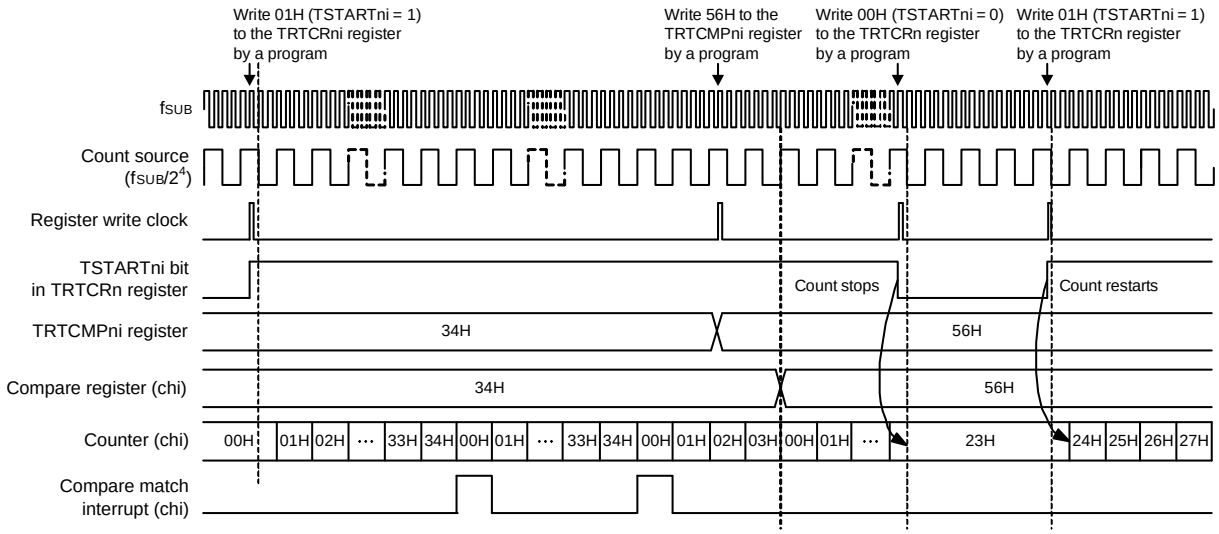
However, the first period to count 00H when the timer starts counting is shorter than one cycle of the count source as below, depending on the timing for writing to the TSTARTni bit and the timing of the next count source.

Minimum: One cycle of the subsystem clock (f_{SUB})

Maximum: One cycle of the count source

Figure 7 - 11 shows the timing for starting/stopping count operation, and Figure 7 - 12 shows the timing of count stop → compare setting (count clearing) → count start. Figure 7 - 11 and Figure 7 - 12 show the update timing in 8-bit counter mode, but operation is performed at the same timing even in 16-bit counter mode.

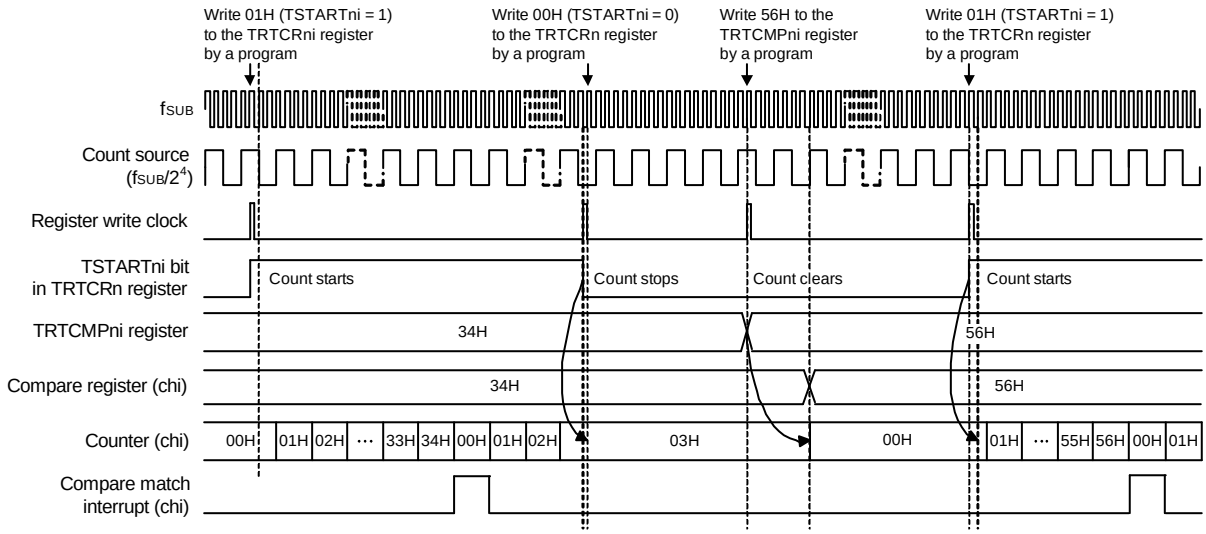
Figure 7 - 11 Example of Count Start/Stop Operation ($f_{SUB}/2^m$ Selected)



The TCSMDn bit in the TRTCRn register is set to 0 (8-bit counter operation)

Remark n: Unit number (n = 0 to 2), i: Channel number (n = 0, 1)

Figure 7 - 12 Example of Count Stop → Count Clearing → Count Start Operation ($f_{SUB}/2^m$ Selected)



The TCSMDn bit in the TRTCRn register is set to 0 (8-bit counter operation)

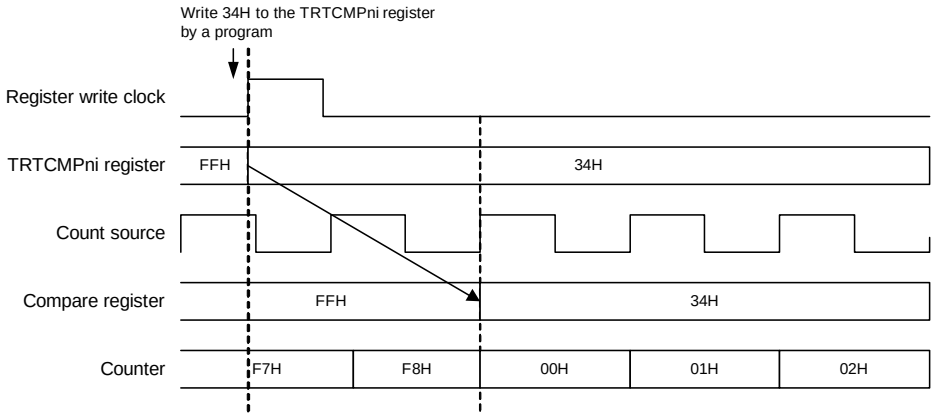
Remark n: Unit number (n = 0 to 2), i: Channel number (n = 0, 1)

7.4.4 Timing for updating compare register values

The timing for updating the value of the TRTCMPni (n = 0 to 2, i = 0, 1) register is the same, regardless of the value of the TSTARTni bit in the TRTCRn register. After TRTCMPni is write-accessed, the value is stored in the compare register after two cycles of the count source. When stored in the compare register, the count value is cleared and set (8-bit count mode: 00H, 16-bit count mode: 0000H).

Figure 7 - 13 shows the timing of rewrite operation. This figure shows the update timing in 8-bit count mode, but operation is performed at the same timing in 16-bit count mode.

Figure 7 - 13 Timing of Compare Value Rewrite Operation

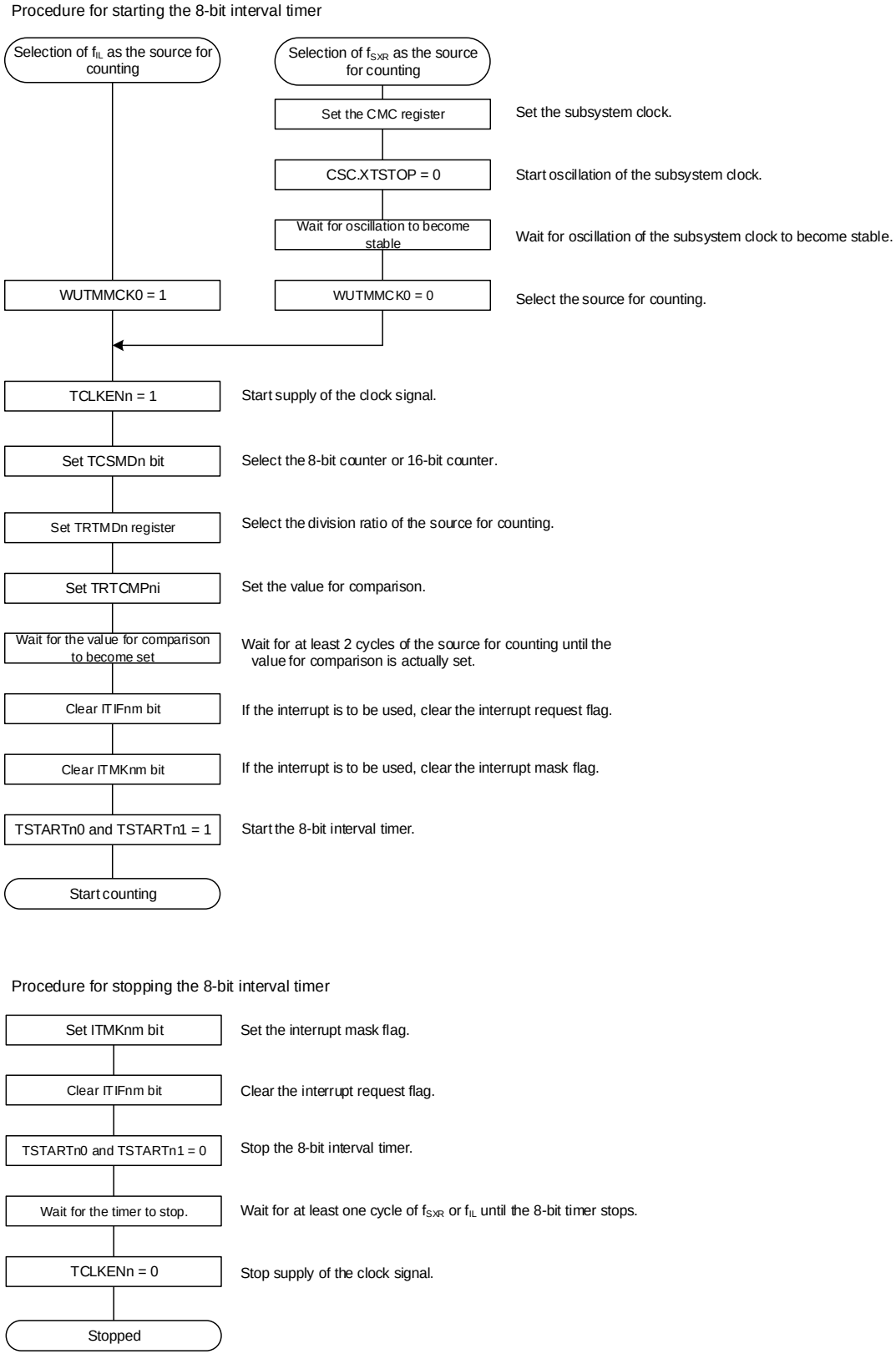


Remark n: Unit number (n = 0 to 2), i: Channel number (n = 0, 1)

7.4.5 Procedure for Setting the 8-bit Interval Timer

The procedure for starting and stopping the 8-bit interval timer is shown below.

Figure 7 - 14 Procedure for Starting and Stopping the 8-bit Interval Timer



7.5 Notes on 8-Bit Interval Timer

7.5.1 Changing settings of operating mode

The settings of bits TCSMDn and TCKni (n = 0 to 2, i = 0, 1) must be changed while the TSTARTni bit in the TRTCRn register is 0 (count stops). After the value of the TSTARTni bit is rewritten from 1 to 0 (count stops), allow at least one cycle of f_{SUB} or f_{IL} to elapse before accessing the registers (TRTCRn and TRTMDn) associated with the 8-bit interval timer.

7.5.2 Accessing compare registers

Do not write to the same compare registers (TRTCMPn0, TRTCMPn1, and TRTCMPn) successively. When writing successively, allow at least two cycles of the count source between writes.
Writing to the compare register (TRTCMPn0, TRTCMPn1, TRTCMPn) must proceed while the source to drive counting is made to oscillate by setting the 8-bit interval timer clock enable bit (TCLKENn) to 1.

7.5.3 8-bit interval timer setting procedure

To supply the clock, set the 8-bit interval timer clock enable bit (TCLKENn) in the 8-bit interval timer control register (TRTCRn) to 1 and then set the TSTARTni bit. Do not set bits TCLKENn and TSTARTni at the same time.
To stop the clock, set TSTARTni to 0 and then allow at least one cycle of f_{SUB} or f_{IL} to elapse before setting the TCLKENn bit to 0.

Remark n: Unit number (n = 0 to 2), i: Channel number (n = 0, 1)

CHAPTER 8 REAL-TIME CLOCK 2

8.1 Functions of Real-time Clock 2

The real-time clock 2 (RTC2) has the following functions.

- Counters of year, month, day of the week, date, hour, minute, and second, that can count up to 99 years (with leap year correction function)
- Constant-period interrupt function (period: 0.5 seconds, 1 second, 1 minute, 1 hour, 1 day, 1 month)
- Alarm interrupt function (alarm: day of the week, hour, and minute)
- Pin output function of 1 Hz

Caution The year, month, week, day, hour, minute and second can only be counted when a subsystem clock (f_{SUB} = 32.768 kHz) is selected as the operation clock of the real-time clock 2. When the low-speed oscillation clock (f_{IL} = 15 kHz) is selected, only the constant-period interrupt function is available.
However, the constant-period interrupt interval when f_{IL} is selected will be calculated with the constant-period (the value selected with RTCC0 register) × f_{SUB}/f_{IL}.

8.2 Configuration of Real-time Clock 2

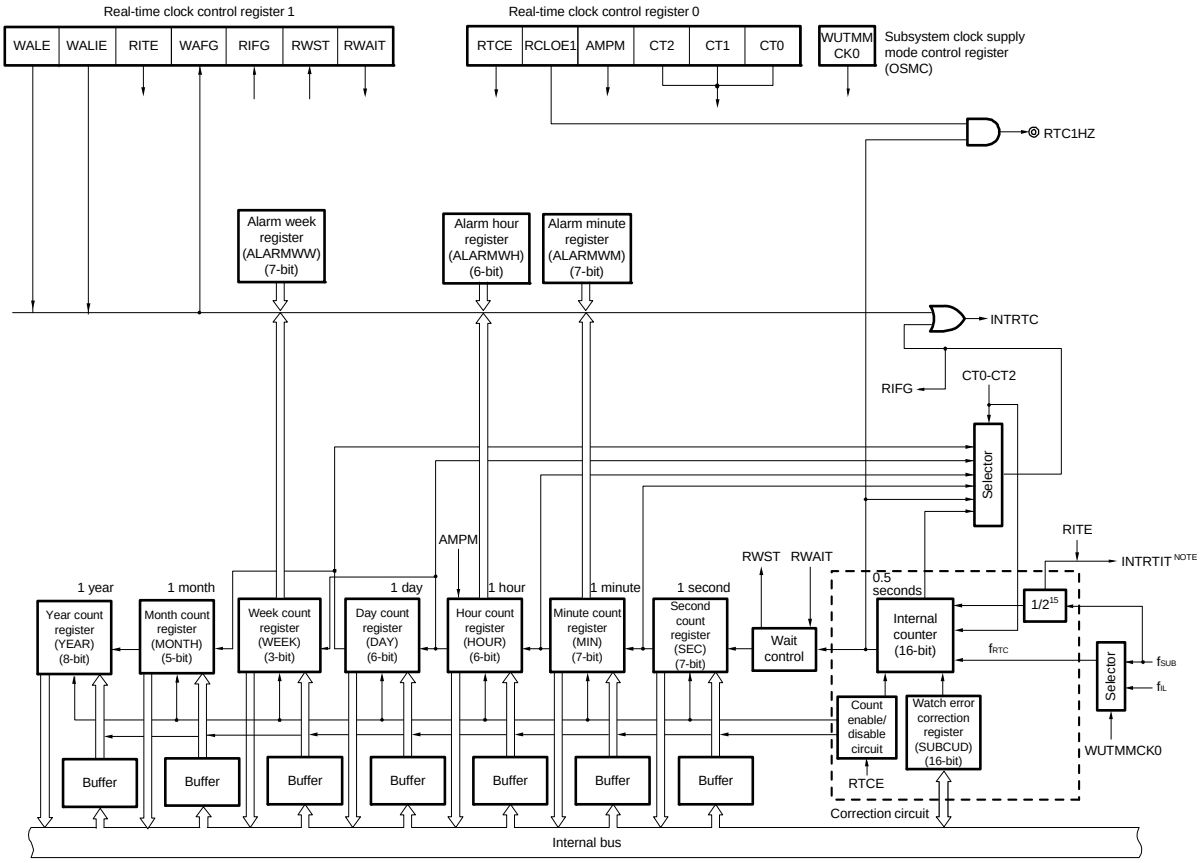
The real-time clock 2 includes the following hardware.

Table 8 - 1 Configuration of Real-time Clock 2

Item	Configuration
Counter	Counter (16-bit)
Control registers	Peripheral enable register 0 (PER0)
	Subsystem clock supply mode control register (OSMC)
	Real-time clock control register 0 (RTCC0)
	Real-time clock control register 1 (RTCC1)
	Second count register (SEC)
	Minute count register (MIN)
	Hour count register (HOUR)
	Day count register (DAY)
	Week count register (WEEK)
	Month count register (MONTH)
	Year count register (YEAR)
	Watch error correction register (SUBCUD)
	Alarm minute register (ALARMWM)
	Alarm hour register (ALARMWH)
	Alarm week register (ALARMWW)

Figure 8 - 1 shows the Block Diagram of Real-time Clock 2.

Figure 8 - 1 Block Diagram of Real-time Clock 2



Note An interrupt that indicates the timing to get the correction value from the clock error correction register (SUBCUD). The fetch timing is 1 second (f_{SUB} base) interval.

Caution The year, month, week, day, hour, minute and second can only be counted when a subsystem clock (f_{SUB} = 32.768 kHz) is selected as the operation clock of the real-time clock 2. When the low-speed oscillation clock (f_{IL} = 15 kHz) is selected, only the constant-period interrupt function is available.
However, the constant-period interrupt interval when f_{IL} is selected will be calculated with the constant-period (the value selected with RTCC0 register) × f_{SUB}/f_{IL}.

8.3 Registers Controlling Real-time Clock 2

The real-time clock 2 is controlled by the following registers.

- Peripheral enable register 0 (PER0)
- Subsystem clock supply mode control register (OSMC)
- Real-time clock control register 0 (RTCC0)
- Real-time clock control register 1 (RTCC1)
- Second count register (SEC)
- Minute count register (MIN)
- Hour count register (HOUR)
- Day count register (DAY)
- Week count register (WEEK)
- Month count register (MONTH)
- Year count register (YEAR)
- Watch error correction register (SUBCUD)
- Alarm minute register (ALARMWM)
- Alarm hour register (ALARMWH)
- Alarm week register (ALARMWW)

The following shows the register states depending on reset sources.

Reset Source	System-related Register Note 1	Calendar-related Register Note 2
POR	Reset	Not reset
External reset	Retained	Retained
WDT	Retained	Retained
TRAP	Retained	Retained
LVD	Retained	Retained
Other internal reset	Retained	Retained

Note 1. RTCC0, RTCC1, SUBCUD

Note 2. SEC, MIN, HOUR, DAY, WEEK, MONTH, YEAR, ALARMWM, ALARMWH, ALARMWW, (counter)

Reset generation does not reset the SEC, MIN, HOUR, DAY, WEEK, MONTH, YEAR, ALARMWM, ALARMWH, or ALARMWW register. Initialize all the registers after power on.

8.3.1 Peripheral enable register 0 (PER0)

This register is used to enable or disable supplying the clock to the peripheral hardware. Clock supply to the hardware that is not used is also stopped so as to decrease the power consumption and noise.

When the real-time clock 2 registers are manipulated, be sure to set bit 7 (RTCWEN) of this register to 1.

The PER0 register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 8 - 2 Format of Peripheral enable register 0 (PER0)

Address: F00F0H After reset: 00H R/W

Symbol	<7>	6	<5>	<4>	<3>	<2>	1	<0>
PER0	RTCWEN	0	ADCEN	IICA0EN	SAU1EN	SAU0EN	0	TAU0EN

RTCWEN	Control of internal clock supply to real-time clock 2
0	Stops input clock supply (stops f_{CLK} supply). • SFR used by the real-time clock 2 cannot be written. • The real-time clock 2 can operate.
1	Enables input clock supply. • SFR used by the real-time clock 2 can be read/written. • The real-time clock 2 can operate.

Caution 1. When using the real-time clock 2, first set the RTCWEN bit to 1, while oscillation of the input clock (f_{RTC}) is stable. If RTCWEN = 0, writing to a control register of the real-time clock 2 is ignored.

Caution 2. Be sure to set bits 1 and 6 to 0.

8.3.2 Subsystem clock supply mode control register (OSMC)

This register is used to reduce power consumption by stopping unnecessary clock functions.

If the RTCLPC bit is set to 1, power consumption can be reduced, because clock supply to the peripheral functions other than the real-time clock 2, 12-bit interval timer, 8-bit interval timer, clock output/buzzer output, LCD controller/driver, serial interface UARTMG0, external signal sampler, and sampling output timer detector is stopped in STOP mode or in HALT mode while the subsystem clock is selected as the CPU clock.

In addition, the OSMC register is used to select the count clock of the real-time clock 2, 12-bit interval timer, and 8-bit timer, and the operation clock of the clock output/buzzer output, LCD controller/driver, timers RJ0 and RJ1, serial interface UARTMG0, external signal sampler, and sampling output timer detector. The low-speed on-chip oscillator clock cannot be selected as the operation clock for the serial interface UARTMG0, external signal sampler, and sampling output timer detector. When using the serial interface UARTMG0, external signal sampler, and sampling output timer detector, select the subsystem clock as the operation clock by setting the WUTMMCK0 to 0.

The OSMC register can be set by an 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 8 - 3 Format of Subsystem clock supply mode control register (OSMC)

Address: F00F3H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
OSMC	RTCLPC	0	0	WUTMMCK0	0	0	0	0

RTCLPC	In STOP mode and in HALT mode while the CPU operates using the subsystem clock
0	Enables subsystem clock supply to peripheral functions. For peripheral functions for which operation is enabled, refer to **Table 27 - 1** to **Table 27 - 3**.
1	Stops subsystem clock supply to peripheral functions other than the real-time clock 2, 12-bit interval timer, 8-bit interval timer, clock output/buzzer output, LCD controller/driver, serial interface UARTMG0, external signal sampler, and sampling output timer detector.

WUTMMCK0 Notes 1, 2, 3	Selection of operation clock of the real-time clock 2, 12-bit interval timer, 8-bit interval timer, LCD controller/driver, and timers RJ0 and RJ1	Selection of clock output from PCLBUZn pin of clock output/buzzer output controller
0	Subsystem clock (f_{SUB}) • The subsystem clock is selected as the operation clock for the real-time clock 2, 12-bit interval timer, 8-bit interval timer, and LCD controller/driver. • The low-speed on-chip oscillator cannot be selected as the count source for timers RJ0 and RJ1.	Selecting the subsystem clock (f_{SUB}) is enabled.
1	Low-speed on-chip oscillator clock (f_{IL}) • The low-speed on-chip oscillator clock is selected as the operation clock for the real-time clock 2, 12-bit interval timer, 8-bit interval timer, and LCD controller/driver. • The low-speed on-chip oscillator or subsystem clock can be selected as the count source for timers RJ0 an RJ1.	Selecting the subsystem clock (f_{SUB}) is disabled.

(**Notes** and **Caution** are listed on the next page.)

Note 1. Be sure to select the subsystem clock (WUTMMCK0 bit = 0) while the subsystem clock is oscillating. The f_{IL} clock can be selected (WUTMMCK0 = 1) only when oscillation of the subsystem clock is stopped (the XTSTOP bit in the CSC register = 1).

Note 2. When WUTMMCK0 is set to 1, the low-speed on-chip oscillator clock oscillates.

Note 3. When WUTMMCK0 is set to 1, the 1 Hz output function of the real-time clock 2 cannot be used.

Caution The count of year, month, week, day, hour, minutes and second can only be performed when a subsystem clock (f_{SUB} = 32.768 kHz) is selected as the operation clock of the real-time clock 2
When the low-speed oscillation clock (f_{IL} = 15 kHz) is selected, only the constant-period interrupt function is available.
However, the constant-period interrupt interval when f_{IL} is selected will be calculated with the constant-period (the value selected with RTCC0 register) × f_{SUB}/f_{IL}.

8.3.3 Real-time clock control register 0 (RTCC0)

The RTCC0 register is an 8-bit register that is used to start or stop the real-time clock 2 operation, control the RTC1HZ pin, and set a 12- or 24-hour system and the constant-period interrupt function.

The RTCC0 register can be set by a 1-bit or 8-bit memory manipulation instruction.

Internal reset generated by the power-on-reset circuit clears this register to 00H.

Figure 8 - 4 Format of Real-time clock control register 0 (RTCC0) (1/2)

Address: FFF9DH After reset: 00H R/W

Symbol	<7>	6	<5>	4	3	2	1	0
RTCC0	RTCE	0	RCLOE1	0	AMPM	CT2	CT1	CT0

RTCE Note 1	Real-time clock 2 operation control
0	Stops counter operation.
1	Starts counter operation.

RCLOE1 Note 2	RTC1HZ pin output control
0	Disables output of the RTC1HZ pin (1 Hz).
1	Enables output of the RTC1HZ pin (1 Hz).
Output of 1 Hz is not output because the clock counter does not operate when RTCE = 0.	

Relation between RTCE and RCLOE1 Settings and Status

Register Settings		Status	
RTCE	RCLOE1	Real-time clock 2	RTC1HZ pin output
0	×	Counting stopped	No output
1	0	Count operation	No output
	1	Count operation	1 Hz output

Note 1. When shifting to STOP mode immediately after setting RTCE to 1, use the procedure shown in Figure 8 - 20 Procedure for Shifting to HALT/STOP Mode After Setting RTCE bit to 1.

Note 2. When the RCLOE1 bit is set while the clock counter operates (RTCE = 1), a glitch may be output to the 1 Hz output pin (RTC1HZ).

Caution Be sure to clear bits 4 and 6 to “0”.

Figure 8 - 4 Format of Real-time clock control register 0 (RTCC0) (2/2)

Address: FFF9DH After reset: 00H R/W

Symbol	<7>	6	<5>	4	3	2	1	0
RTCC0	RTCE	0	RCLOE1	0	AMPM	CT2	CT1	CT0

AMPM	12-/24-hour system select
0	12-hour system (a.m. and p.m. are displayed.)
1	24-hour system
• When changing the value of the AMPM bit while the clock counter operates (RTCE = 1), set RWAIT (bit 0 of RTCC1) and then set the hour counter (HOUR) again. When the AMPM value is 0, the 12-hour system is displayed. When the value is 1, the 24-hour system is displayed. • Table 8 - 2 shows the displayed time digits.	

CT2	CT1	CT0	Constant-period interrupt (INTRTC) selection
0	0	0	Does not use fixed-cycle interrupt function.
0	0	1	Once per 0.5 s (synchronized with second count up)
0	1	0	Once per 1 s (same time as second count up)
0	1	1	Once per 1 m (second 00 of every minute)
1	0	0	Once per 1 hour (minute 00 and second 00 of every hour)
1	0	1	Once per 1 day (hour 00, minute 00, and second 00 of every day)
1	1	×	Once per 1 month (Day 1, hour 00 a.m., minute 00, and second 00 of every month)
When changing the values of the CT2 to CT0 bits while the counter operates (RTCE = 1), rewrite the values of the CT2 to CT0 bits after disabling interrupt servicing INTRTC by using the interrupt mask flag register. Furthermore, after rewriting the values of the CT2 to CT0 bits, enable interrupt servicing after clearing the RIFG and RTCIF flags.			

Caution Be sure to clear bits 4 and 6 to “0”.

Remark ×: don’t care

8.3.4 Real-time clock control register 1 (RTCC1)

The RTCC1 register is an 8-bit register that is used to control the alarm interrupt function and the wait time of the counter.

The RTCC1 register can be set by a 1-bit or 8-bit memory manipulation instruction.

Internal reset generated by the power-on-reset circuit clears this register to 00H.

Figure 8 - 5 Format of Real-time clock control register 1 (RTCC1) (1/3)

Address: FFF9EH After reset: 00H R/W

Symbol	<7>	<6>	<5>	<4>	<3>	2	<1>	<0>
RTCC1	WALE	WALIE	RITE	WAFG	RIFG	0	RWST	RWAIT

WALE	Alarm operation control
0	Match operation is invalid.
1	Match operation is valid.
When setting a value to the WALE bit while the counter operates (RTCE = 1) and WALIE = 1, rewrite the WALE bit after disabling interrupt servicing INTRTC by using the interrupt mask flag register. Furthermore, clear the WAFG and RTCIF flags after rewriting the WALE bit. When setting each alarm register (WALIE flag of real-time clock control register 1 (RTCC1), the alarm minute register (ALARMWM), the alarm hour register (ALARMWH), and the alarm week register (ALARMWW)), set match operation to be invalid (“0”) for the WALE bit.	

WALIE	Control of alarm interrupt (INTRTC) function operation
0	Does not generate interrupt on matching of alarm.
1	Generates interrupt on matching of alarm.

Caution If writing is performed to RTCC1 with a 1-bit manipulation instruction, the RIFG and WAFG flags may be cleared. Therefore, to perform writing to RTCC1, be sure to use an 8- bit manipulation instruction. To prevent the RIFG and WAFG flags from being cleared during writing, set 1 (writing disabled) to the corresponding bit. If the RIFG and WAFG flags are not used and the value may be changed, RTCC1 may be written by using a 1-bit manipulation instruction.

Figure 8 - 6 Format of Real-time clock control register 1 (RTCC1) (2/3)

Address: FFF9EH After reset: 00H R/W

Symbol	<7>	<6>	<5>	<4>	<3>	2	<1>	<0>
RTCC1	WALE	WALIE	RITE	WAFG	RIFG	0	RWST	RWAIT

RITE	Control of correction timing signal interrupt (INTRTIT) function operation
0	Does not generate interrupt of correction timing signal.
1	Generates interrupt of correction timing signal.

WAFG	Alarm detection status flag
0	Alarm mismatch
1	Detection of matching of alarm
This is a status flag that indicates detection of matching with the alarm. It is valid only when WALE = 1 and is set to “1” one clock (32.768 kHz) after matching of the alarm is detected. This flag is cleared when “0” is written to it. Writing “1” to it is invalid. (Writing 1 does not change the value of WAFG.)	

RIFG	Constant-period interrupt status flag
0	Constant-period interrupt is not generated.
1	Constant-period interrupt is generated.
This flag indicates the status of generation of the constant-period interrupt. When the constant-period interrupt is generated, it is set to “1”. This flag is cleared when “0” is written to it. Writing 1 to it is invalid. (Writing 1 does not change the value of RIFG.)	

Caution If writing is performed to RTCC1 with a 1-bit manipulation instruction, the RIFG and WAFG flags may be cleared. Therefore, to perform writing to RTCC1, be sure to use an 8- bit manipulation instruction. To prevent the RIFG and WAFG flags from being cleared during writing, set 1 (writing disabled) to the corresponding bit. If the RIFG and WAFG flags are not used and the value may be changed, RTCC1 may be written by using a 1-bit manipulation instruction.

Figure 8 - 7 Format of Real-time clock control register 1 (RTCC1) (3/3)

Address: FFF9EH After reset: 00H R/W

Symbol	<7>	<6>	<5>	<4>	<3>	2	<1>	<0>
RTCC1	WALE	WALIE	RITE	WAFG	RIFG	0	RWST	RWAIT

RWST	Wait status flag of real-time clock 2
0	Counter is operating.
1	Mode to read or write counter value.
This status flag indicates whether the setting of the RWAIT bit is valid. Before reading or writing the counter value, confirm that the value of this flag is 1. Even if the RWAIT bit is set to 0, the RWST bit is not set to 0 while writing to the counter. After writing is completed, the RWST bit is set to 0.	

RWAIT	Wait control of real-time clock 2
0	Sets counter operation.
1	Stops SEC to YEAR counters. Mode to read or write counter value.
This bit controls the operation of the counter. Be sure to write “1” to it to read or write the counter value. As the counter (16-bit) is continuing to run, complete reading or writing within one second and turn back to 0. When reading or writing to the counter is required while generation of the alarm interrupt is enabled, first set the CT2 to CT0 bits to 010B (generating the constant-period interrupt once per 1 second). Then, complete the processing from setting the RWAIT bit to 1 to setting it to 0 before generation of the next constant-period interrupt. When RWAIT = 1, it takes up to 1 clock (f_{RTC}) until the counter value can be read or written (RWST = 1) Notes 1, 2. When the counter (16-bit) overflowed while RWAIT = 1, it keeps the event of overflow until RWAIT = 0, then counts up. However, when it wrote a value to second count register, it will not keep the overflow event.	

Note 1. When the RWAIT bit is set to 1 within one cycle of f_{RTC} clock after setting the RTCE bit to 1, the RWST bit being set to 1 may take up to two cycles of the operating clock (f_{RTC}).

Note 2. When the RWAIT bit is set to 1 within one cycle of f_{RTC} clock after release from the standby mode (HALT mode, STOP mode, or SNOOZE mode), the RWST bit being set to 1 may take up to two cycles of the operating clock (f_{RTC}).

Caution If writing is performed to RTCC1 with a 1-bit manipulation instruction, the RIFG and WAFG flags may be cleared. Therefore, to perform writing to RTCC1, be sure to use an 8- bit manipulation instruction. To prevent the RIFG and WAFG flags from being cleared during writing, set 1 (writing disabled) to the corresponding bit. If the RIFG and WAFG flags are not used and the value may be changed, RTCC1 may be written by using a 1-bit manipulation instruction.

Remark 1. Constant-period interrupts and alarm match interrupts use the same interrupt source (INTRTC).
When using these two types of interrupts at the same time, which interrupt occurred can be judged by checking the constant-period interrupt status flag (RIFG) and the alarm detection status flag (WAFG) upon INTRTC occurrence.

Remark 2. The internal counter (16 bits) is cleared when the second count register (SEC) is written.

8.3.5 Second count register (SEC)

The SEC register is an 8-bit register that takes a value of 0 to 59 (decimal) and indicates the count value of seconds.

It is a decimal counter that counts up when the counter (16-bit) overflows.

When data is written to this register, it is written to a buffer and then to the counter up to 2 clocks (f_{RTC}) later. Set a decimal value of 00 to 59 to this register in BCD code.

The SEC register can be set by an 8-bit memory manipulation instruction.

Reset signal generation not clears this register to default value.

Figure 8 - 8 Format of Second count register (SEC)

Address: FFF92H After reset: Undefined R/W

Symbol	7	6	5	4	3	2	1	0
SEC	0	SEC40	SEC20	SEC10	SEC8	SEC4	SEC2	SEC1

Caution When reading or writing to SEC while the clock counter operates (RTCE = 1), be sure to use the flows shown in 8.4.3 Reading real-time clock 2 and 8.4.4 Writing to real-time clock 2 counter.

Remark The internal counter (16 bits) is cleared when the second count register (SEC) is written.

8.3.6 Minute count register (MIN)

The MIN register is an 8-bit register that takes a value of 0 to 59 (decimal) and indicates the count value of minutes.

It is a decimal counter that counts up when the second counter overflows.

When data is written to this register, it is written to a buffer and then to the counter up to 2 clocks (f_{RTC}) later. Even if the second count register overflows while this register is being written, this register ignores the overflow and is set to the value written. Set a decimal value of 00 to 59 to this register in BCD code.

The MIN register can be set by an 8-bit memory manipulation instruction.

Reset signal generation not clears this register to default value.

Figure 8 - 9 Format of Minute count register (MIN)

Address: FFF93H After reset: Undefined R/W

Symbol	7	6	5	4	3	2	1	0
MIN	0	MIN40	MIN20	MIN10	MIN8	MIN4	MIN2	MIN1

Caution When reading or writing to MIN while the clock counter operates (RTCE = 1), be sure to use the flows shown in 8.4.3 Reading real-time clock 2 and 8.4.4 Writing to real-time clock 2 counter.

8.3.7 Hour count register (HOUR)

The HOUR register is an 8-bit register that takes a value of 00 to 23 or 01 to 12 and 21 to 32 (decimal) and indicates the count value of hours.

It is a decimal counter that counts up when the minute counter overflows.

When data is written to this register, it is written to a buffer and then to the counter up to 2 clocks (f_{RTC}) later. Even if the minute count register overflows while this register is being written, this register ignores the overflow and is set to the value written. Specify a decimal value of 00 to 23, 01 to 12, or 21 to 32 by using BCD code according to the time system specified using bit 3 (AMPM) of real-time clock control register 0 (RTCC0).

If the AMPM bit value is changed, the values of the HOUR register change according to the specified time system.

The HOUR register can be set by an 8-bit memory manipulation instruction.

Reset signal generation not clears this register to default value.

Figure 8 - 10 Format of Hour count register (HOUR)

Address: FFF94H After reset: Undefined R/W

Symbol	7	6	5	4	3	2	1	0
HOUR	0	0	HOUR20	HOUR10	HOUR8	HOUR4	HOUR2	HOUR1

Caution 1. Bit 5 (HOUR20) of the HOUR register indicates AM(0)/PM(1) if AMPM = 0 (if the 12-hour system is selected).

Caution 2. When reading or writing to HOUR while the clock counter operates (RTCE = 1), be sure to use the flows shown in 8.4.3 Reading real-time clock 2 and 8.4.4 Writing to real-time clock 2 counter.

Table 8 - 2 shows the relationship between the setting value of the AMPM bit, the hour count register (HOUR) value, and time.

Table 8 - 2 Displayed Time Digits

24-Hour Display (AMPM = 1)		12-Hour Display (AMPM = 0)	
Time	HOUR Register	Time	HOUR Register
0	00 H	12 a.m.	12 H
1	01 H	1 a.m.	01 H
2	02 H	2 a.m.	02 H
3	03 H	3 a.m.	03 H
4	04 H	4 a.m.	04 H
5	05 H	5 a.m.	05 H
6	06 H	6 a.m.	06 H
7	07 H	7 a.m.	07 H
8	08 H	8 a.m.	08 H
9	09 H	9 a.m.	09 H
10	10 H	10 a.m.	10 H
11	11 H	11 a.m.	11 H
12	12 H	12 p.m.	32 H
13	13 H	1 p.m.	21 H
14	14 H	2 p.m.	22 H
15	15 H	3 p.m.	23 H
16	16 H	4 p.m.	24 H
17	17 H	5 p.m.	25 H
18	18 H	6 p.m.	26 H
19	19 H	7 p.m.	27 H
20	20 H	8 p.m.	28 H
21	21 H	9 p.m.	29 H
22	22 H	10 p.m.	30 H
23	23 H	11 p.m.	31 H

The HOUR register value is set to 12-hour display when the AMPM bit is “0” and to 24-hour display when the AMPM bit is “1”.
In 12-hour display, the fifth bit of the HOUR register displays 0 for AM and 1 for PM.

8.3.8 Day count register (DAY)

The DAY register is an 8-bit register that takes a value of 1 to 31 (decimal) and indicates the count value of days.
It is a decimal counter that count ups when the hour counter overflows.
This counter counts as follows.

[DAY count values]
- 01 to 31 (January, March, May, July, August, October, December)
- 01 to 30 (April, June, September, November)
- 01 to 29 (February, leap year)
- 01 to 28 (February, normal year)

When data is written to this register, it is written to a buffer and then to the counter up to 2 clocks (f_{RTC}) later.
Even if the hour count register overflows while this register is being written, this register ignores the overflow and is set to the value written. Set a decimal value of 01 to 31 to this register in BCD code.
The DAY register can be set by an 8-bit memory manipulation instruction.
Reset signal generation not clears this register to default value.

Figure 8 - 11 Format of Day count register (DAY)

Address: FFF96H After reset: Undefined R/W

Symbol	7	6	5	4	3	2	1	0
DAY	0	0	DAY20	DAY10	DAY8	DAY4	DAY2	DAY1

Caution When reading or writing to DAY while the clock counter operates (RTCE = 1), be sure to use the flows shown in 8.4.3 Reading real-time clock 2 and 8.4.4 Writing to real-time clock 2 counter.

8.3.9 Week count register (WEEK)

The WEEK register is an 8-bit register that takes a value of 0 to 6 (decimal) and indicates the count value of weekdays.

It is a decimal counter that counts up when a carry to the date counter occurs.

When data is written to this register, it is written to a buffer and then to the counter up to 2 clocks (f_{RTC}) later. Set a decimal value of 00 to 06 to this register in BCD code.

The WEEK register can be set by an 8-bit memory manipulation instruction.

Reset signal generation not clears this register to default value.

Figure 8 - 12 Format of Week count register (WEEK)

Address: FFF95H After reset: Undefined R/W

Symbol	7	6	5	4	3	2	1	0
WEEK	0	0	0	0	0	WEEK4	WEEK2	WEEK1

Caution 1. The value corresponding to the month count register (MONTH) or the day count register (DAY) is not stored in the week count register (WEEK) automatically. After reset release, set the week count register as follow.

Day	WEEK
Sunday	00 H
Monday	01 H
Tuesday	02 H
Wednesday	03 H
Thursday	04 H
Friday	05 H
Saturday	06 H

Caution 2. When reading or writing to WEEK while the clock counter operates (RTCE = 1), be sure to use the flows shown in 8.4.3 Reading real-time clock 2 and 8.4.4 Writing to real-time clock 2 counter.

8.3.10 Month count register (MONTH)

The MONTH register is an 8-bit register that takes a value of 1 to 12 (decimal) and indicates the count value of months.

It is a decimal counter that count ups when the date counter overflows.

When data is written to this register, it is written to a buffer and then to the counter up to 2 clocks (f_{RTC}) later. Even if the day count register overflows while this register is being written, this register ignores the overflow and is set to the value written. Set a decimal value of 01 to 12 to this register in BCD code.

The MONTH register can be set by an 8-bit memory manipulation instruction.

Reset signal generation not clears this register to default value.

Figure 8 - 13 Format of Month count register (MONTH)

Address: FFF97H After reset: Undefined R/W

Symbol	7	6	5	4	3	2	1	0
MONTH	0	0	0	MONTH10	MONTH8	MONTH4	MONTH2	MONTH1

Caution When reading or writing to MONTH while the clock counter operates (RTCE = 1), be sure to use the flows shown in 8.4.3 Reading real-time clock 2 and 8.4.4 Writing to real-time clock 2 counter.

8.3.11 Year count register (YEAR)

The YEAR register is an 8-bit register that takes a value of 0 to 99 (decimal) and indicates the count value of years.

It is a decimal counter that counts up when the month count register (MONTH) overflows.

Values 00, 04, 08, …, 92, and 96 indicate a leap year.

When data is written to this register, it is written to a buffer and then to the counter up to 2 clocks (f_{RTC}) later. Even if the MONTH register overflows while this register is being written, this register ignores the overflow and is set to the value written. Set a decimal value of 00 to 99 to this register in BCD code.

The YEAR register can be set by an 8-bit memory manipulation instruction.

Reset signal generation not clears this register to default value.

Figure 8 - 14 Format of Year count register (YEAR)

Address: FFF98H After reset: Undefined R/W

Symbol	7	6	5	4	3	2	1	0
YEAR	YEAR80	YEAR40	YEAR20	YEAR10	YEAR8	YEAR4	YEAR2	YEAR1

Caution When reading or writing to YEAR while the clock counter operates (RTCE = 1), be sure to use the flows shown in 8.4.3 Reading real-time clock 2 and 8.4.4 Writing to real-time clock 2 counter.

8.3.12 Watch error correction register (SUBCUD)

This register is used to correct the clock with a minimum resolution and accuracy of 0.96 ppm when it is slow or fast by changing the counter value every second.

The SUBCUD register can be set by an 16-bit memory manipulation instruction.

Internal reset generated by the power-on-reset circuit clears this register to 0020H.

Figure 8 - 15 Format of Watch error correction register (SUBCUD)

Address: F0310H After reset: 0020H R/W

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SUBCUD	F15	0	0	0	0	0	0	F8	F7	F6	F5	F4	F3	F2	F1	F0

F15	Clock error correction enable
0	Stops clock error correction.
1	Enables clock error correction.

The range of value that can be corrected by using the clock error correction register (SUBCUD) is shown in Table 8 - 3.

Table 8 - 3 Correctable Range of Crystal Resonator Oscillation Frequency Deviation

Item	Value
Correctable range	-274.6 ppm to +212.6 ppm
Maximum quantization error	±0.48 ppm
Minimum resolution	0.96 ppm

Table 8 - 4 Clock Error Correction Values

SUBCUD										Target Correction Values
F15	F8	F7	F6	F5	F4	F3	F2	F1	F0	
1	1	0	0	0	0	0	0	0	0	-274.6 ppm
	1	0	0	0	0	0	0	0	1	-273.7 ppm
	1	0	0	0	0	0	0	1	0	-272.7 ppm
	• • •	• • •	• • •	• • •	• • •	• • •	• • •	• • •	• • •	• • •
	1	1	1	1	1	1	1	0	1	-33.3 ppm
	1	1	1	1	1	1	1	1	0	-32.4 ppm
	1	1	1	1	1	1	1	1	1	-31.4 ppm
	0	0	0	0	0	0	0	0	0	-30.5 ppm
	0	0	0	0	0	0	0	0	1	-29.6 ppm
	0	0	0	0	0	0	0	1	0	-28.6 ppm
	• • •	• • •	• • •	• • •	• • •	• • •	• • •	• • •	• • •	• • •
	0	0	0	0	1	1	1	1	1	-0.95 ppm
	0	0	0	1	0	0	0	0	0	0 ppm
	0	0	0	1	0	0	0	0	1	0.95 ppm
	• • •	• • •	• • •	• • •	• • •	• • •	• • •	• • •	• • •	• • •
	0	1	1	1	1	1	1	0	1	210.7 ppm
	0	1	1	1	1	1	1	1	0	211.7 ppm
	0	1	1	1	1	1	1	1	1	212.6 ppm
0	×	×	×	×	×	×	×	×	×	Clock error correction stopped

The F8 to F0 value of the SUBCUD register is calculated from the target correction value by using the following expression.

$$SUBCUD[8:0] = \left[\frac{\text{Target correction value [ppm]} \times 2^{20}}{10^6}\right]_{\text{Binary (9 digits)}} + 0\ 0010\ 0000\ B$$

Caution The target correction value is the oscillation frequency deviation (unit: [ppm]) of the crystal resonator. For calculating the correction value, see 8.4.8 Example of watch error correction of real-time clock 2.

Examples 1. When target correction value = 18.3 [ppm]

SUBCUD[8:0] = $(18.3 \times 2^{20} / 10^6)_{\text{Binary (9 digits)}}$ + 000100000B
= $(19.1889408)_{\text{Binary (9 digits)}}$ + 000100000B
= 000010011B + 000100000B
= 000110011B

Examples 2. When target correction value = -18.3 [ppm]

SUBCUD[8:0] = $(-18.3 \times 2^{20} / 10^{6})$ Binary (9 digits) + 000100000B
= (-19.1889408) Binary (9 digits) + 000100000B
= (000010011B) two's complement + 000100000B
= 111101101B + 000100000B
= 000001101B

8.3.13 Alarm minute register (ALARMWM)

This register is used to set minutes of alarm.

The ALARMWM register can be set by an 8-bit memory manipulation instruction.

Reset signal generation not clears this register to default value.

Figure 8 - 16 Format of Alarm minute register (ALARMWM)

Address: FFF9AH After reset: Undefined R/W

Symbol	7	6	5	4	3	2	1	0
ALARMWM	0	WM40	WM20	WM10	WM8	WM4	WM2	WM1

Caution Set a decimal value of 00 to 59 to this register in BCD code. If a value outside the range is set, the alarm is not detected.

8.3.14 Alarm hour register (ALARMWH)

This register is used to set hours of alarm.

The ALARMWH register can be set by an 8-bit memory manipulation instruction.

Reset signal generation not clears this register to default value.

Figure 8 - 17 Format of Alarm hour register (ALARMWH)

Address: FFF9BH After reset: Undefined R/W

Symbol	7	6	5	4	3	2	1	0
ALARMWH	0	0	WH20	WH10	WH8	WH4	WH2	WH1

Caution 1. Set a decimal value of 00 to 23 or 01 to 12 and 21 to 32 to this register in BCD code. If a value outside the range is set, the alarm is not detected.

Caution 2. Bit 5 (WH20) of the ALARMWH register indicates AM(0)/PM(1) if AMPM = 0 (if the 12-hour system is selected).

8.3.15 Alarm week register (ALARMWW)

This register is used to set date of alarm.

The ALARMWW register can be set by an 8-bit memory manipulation instruction.

Reset signal generation not clears this register to default value.

Figure 8 - 18 Format of Alarm week register (ALARMWW)

Address: FFF9CH After reset: Undefined R/W

Symbol	7	6	5	4	3	2	1	0
ALARMWW	0	WW6	WW5	WW4	WW3	WW2	WW1	WW0

Table 8 - 5 shows an example of setting the alarm.

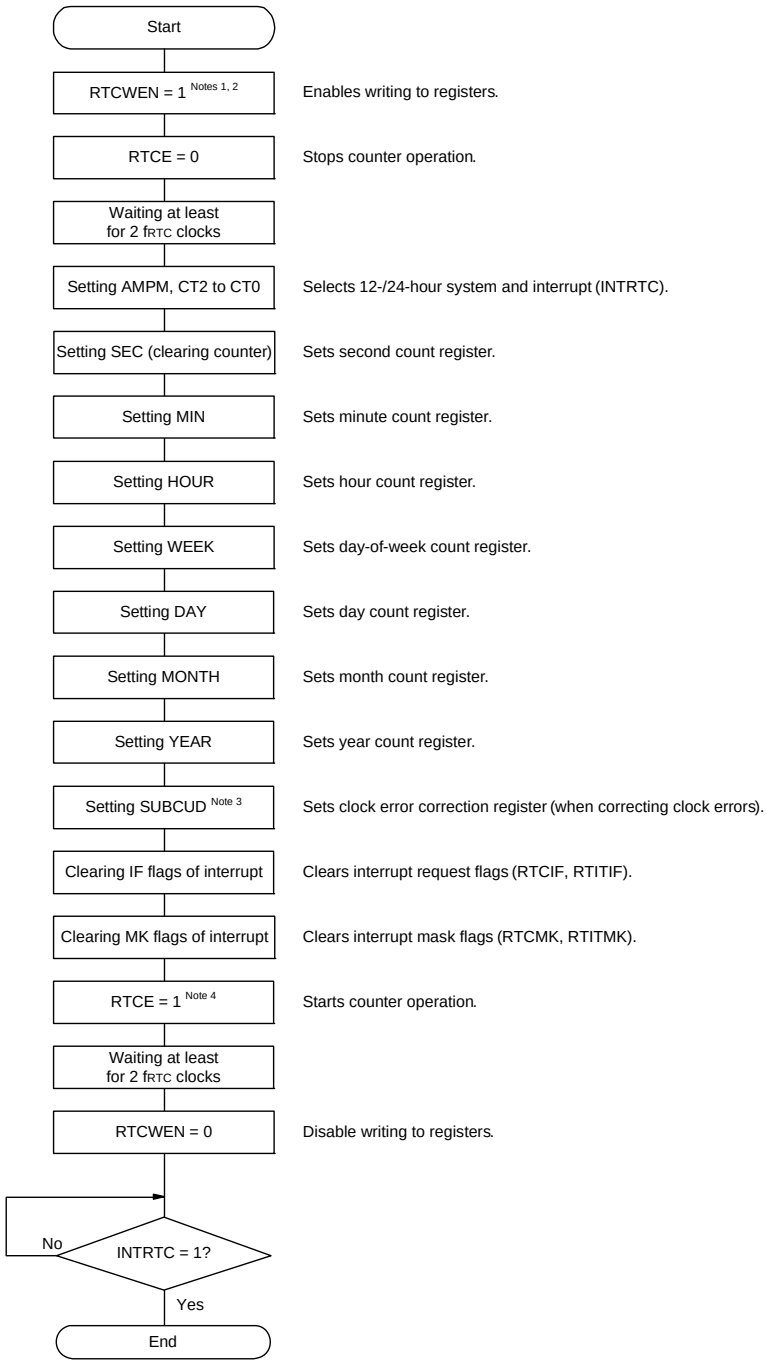
Table 8 - 5 Setting Alarm

Time of Alarm	Day							12-Hour Display				24-Hour Display			
	Sunday	Monday	Tuesday	Wednesday	Thursday	Friday	Saturday	Hour 10	Hour 1	Minute 10	Minute 1	Hour 10	Hour 1	Minute 10	Minute 1
	WW0	WW1	WW2	WW3	WW4	WW5	WW6								
Every day, 0:00 a.m.	1	1	1	1	1	1	1	1	2	0	0	0	0	0	0
Every day, 1:30 a.m.	1	1	1	1	1	1	1	0	1	3	0	0	1	3	0
Every day, 11:59 a.m.	1	1	1	1	1	1	1	1	1	5	9	1	1	5	9
Monday through Friday, 0:00 p.m.	0	1	1	1	1	1	0	3	2	0	0	1	2	0	0
Sunday, 1:30 p.m.	1	0	0	0	0	0	0	2	1	3	0	1	3	3	0
Monday, Wednesday, Friday, 11:59 p.m.	0	1	0	1	0	1	0	3	1	5	9	2	3	5	9

8.4 Real-time Clock 2 Operation

8.4.1 Starting operation of real-time clock 2

Figure 8 - 19 Procedure for Starting Operation of Real-time Clock 2



Note 1. Set RTCWEN to 0 except when accessing the RTC register.

Note 2. First set the RTCWEN bit to 1, while oscillation of the input clock (f_{RTC}) is stable.

Note 3. Set up the SUBCUD register only if the watch error must be corrected. For details about how to calculate the correction value, see **8.4.8 Example of watch error correction of real-time clock 2**.

Note 4. Confirm the procedure described in **8.4.2 Shifting to HALT/STOP mode after starting operation** when shifting to HALT/STOP mode without waiting for INTRTC = 1 after RTCE = 1.

8.4.2 Shifting to HALT/STOP mode after starting operation

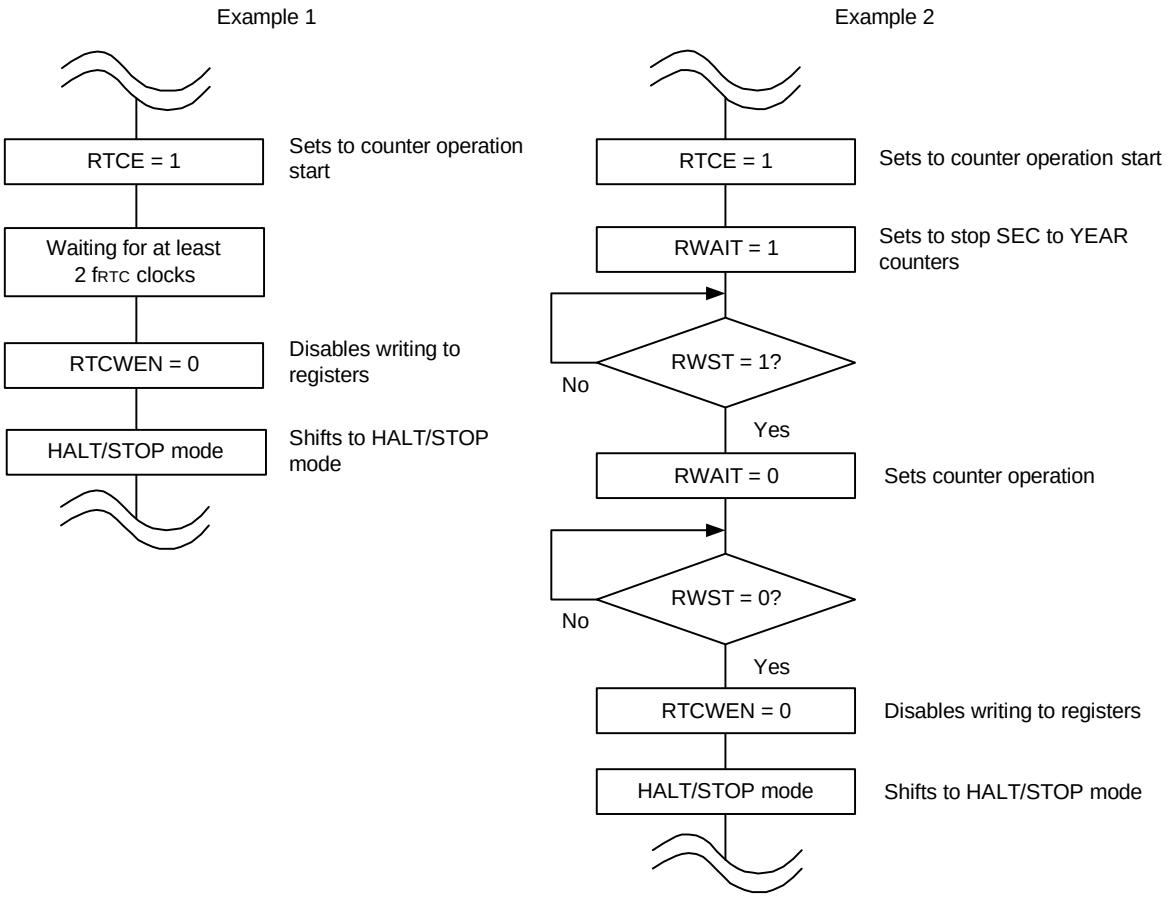
Perform one of the following processing when shifting to HALT/STOP mode immediately after setting the RTCE bit to 1.

However, after setting the RTCE bit to 1, this processing is not required when shifting to STOP mode after the first INTRTC interrupt has occurred.

(1) Shifting to HALT/STOP mode when at least two input clocks (f_{RTC}) have elapsed after setting the RTCE bit to 1 (see **Figure 8 - 20**, **Example 1**).

(2) Checking by polling the RWST bit to become 1, after setting the RTCE bit to 1 and then setting the RWAIT bit to 1. Afterward, setting the RWAIT bit to 0 and shifting to HALT/STOP mode after checking again by polling that the RWST bit has become 0 (see **Figure 8 - 20**, **Example 2**).

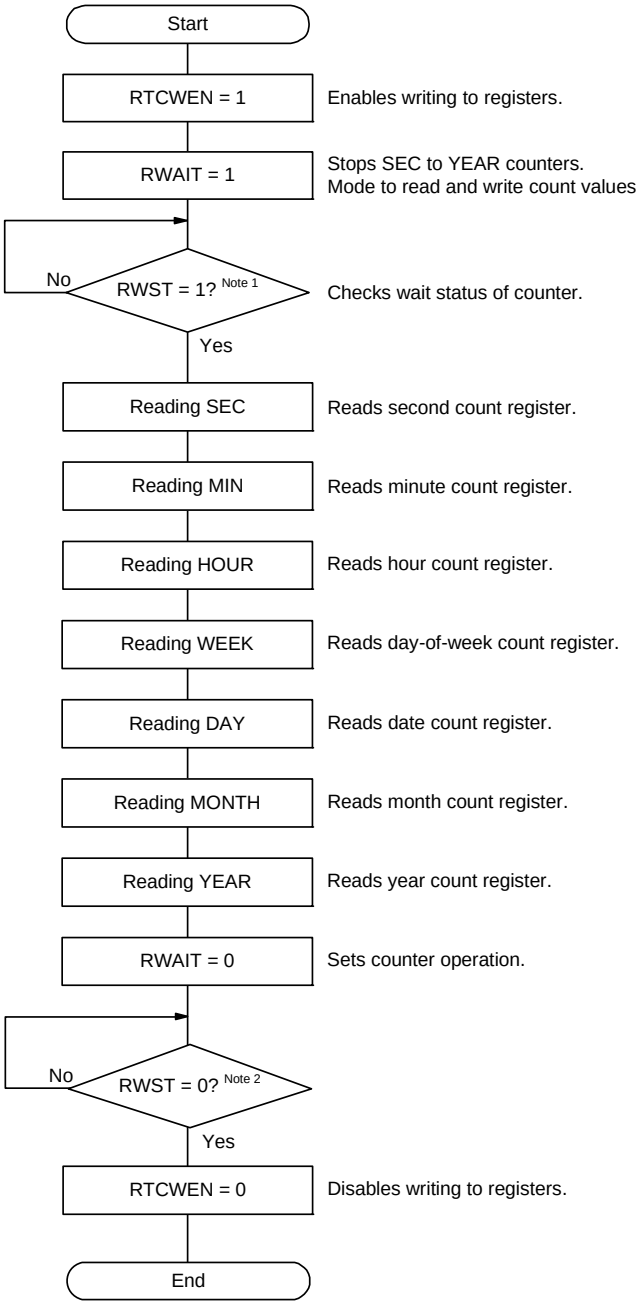
Figure 8 - 20 Procedure for Shifting to HALT/STOP Mode After Setting RTCE bit to 1



8.4.3 Reading real-time clock 2

Read the counter during counter operation (RTCE = 1) after setting RWAIT to 1 first.
Set RWAIT to 0 after completion of reading the counter.

Figure 8 - 21 Procedure for Reading Real-time Clock 2



Note 1. When the counter is stopped (RTCE = 0), RWST is not set to 1.

Note 2. Be sure to confirm that RWST = 0 before setting HALT/STOP mode.

Caution **Complete the series of operations of setting the RWAIT bit to 1 to clearing the RWAIT bit to 0 within 1 second. When reading to the counter is required while generation of the alarm interrupt is enabled, first set the CT2 to CT0 bits to 010B (generating the constant-period interrupt once per 1 second). Then, complete the processing from setting the RWAIT bit to 1 to setting it to 0 before generation of the next constant-period interrupt.**

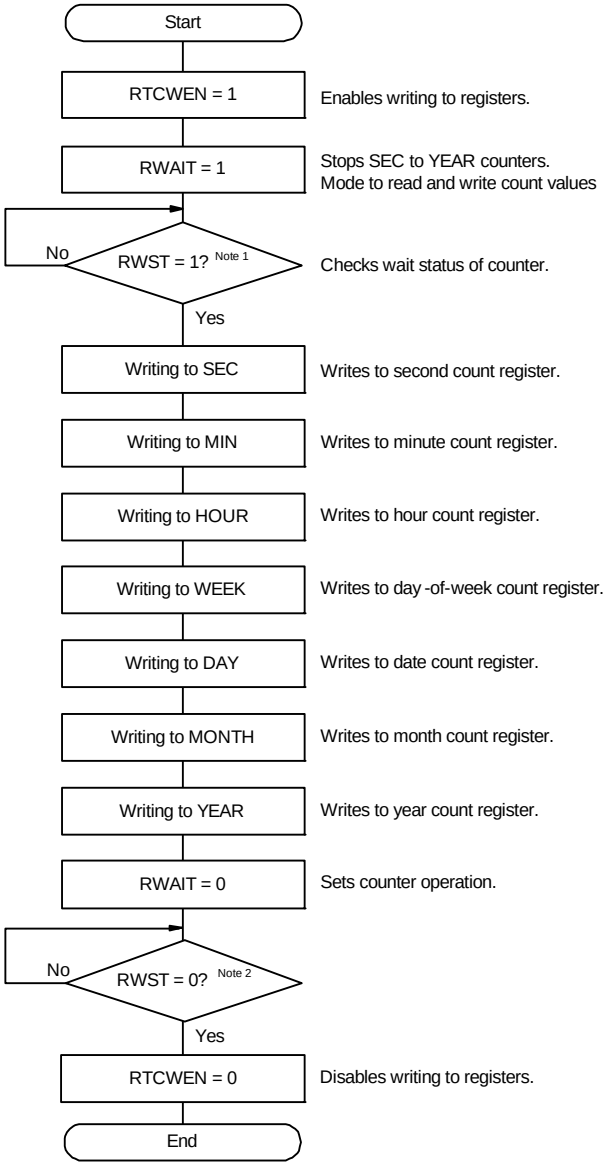
Remark SEC, MIN, HOUR, WEEK, DAY, MONTH, and YEAR may be read in any sequence. All the registers do not have to be set and only some registers may be read.

8.4.4 Writing to real-time clock 2 counter

Write the counter during counter operation (RTCE = 1) after setting RWAIT to 1 first.

Set RWAIT to 0 after completion of writing the counter.

Figure 8 - 22 Procedure for Writing Real-time Clock 2



Note 1. When the counter is stopped (RTCE = 0), RWST is not set to 1.

Note 2. Be sure to confirm that RWST = 0 before setting HALT/STOP mode.

Caution 1. Complete the series of operations of setting the RWAIT bit to 1 to clearing the RWAIT bit to 0 within 1 second. When writing to the counter is required while generation of the alarm interrupt is enabled, first set the CT2 to CT0 bits to 010B (generating the constant-period interrupt once per 1 second). Then, complete the processing from setting the RWAIT bit to 1 to setting it to 0 before generation of the next constant-period interrupt.

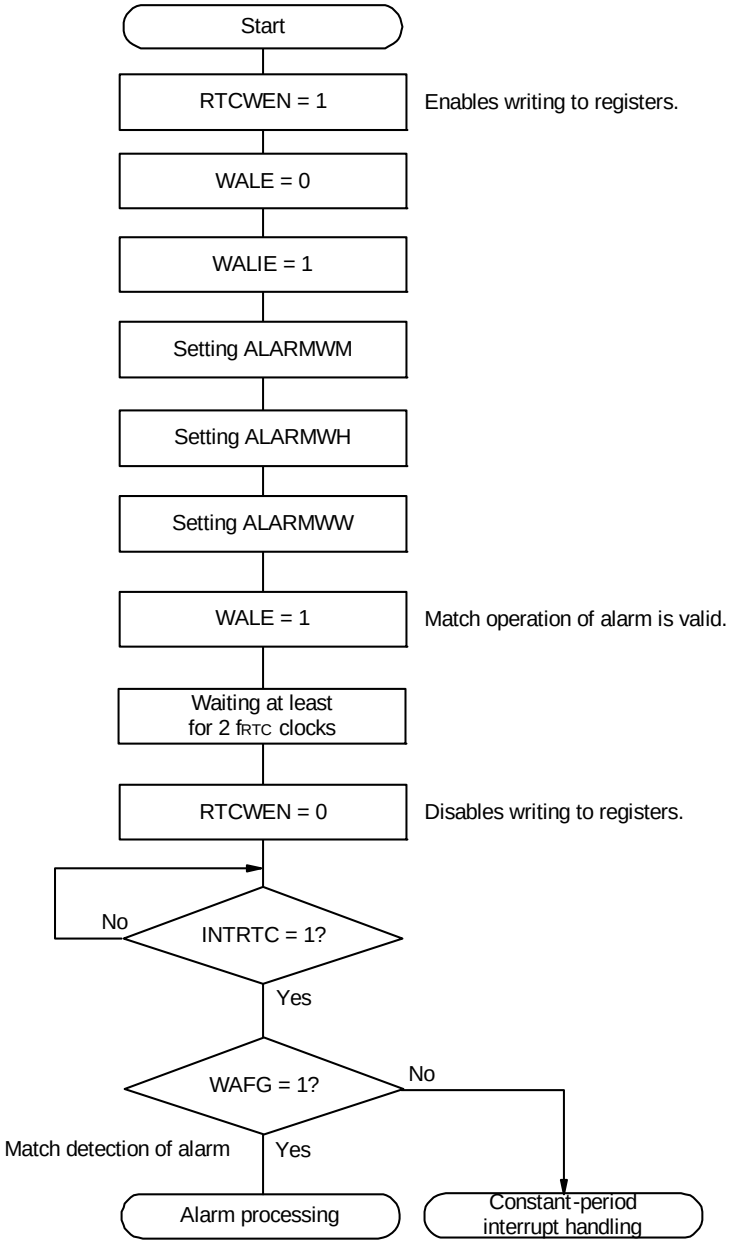
Caution 2. When changing the values of the SEC, MIN, HOUR, WEEK, DAY, MONTH, and YEAR register while the counter operates (RTCE = 1), rewrite the values of the MIN register after disabling interrupt servicing INTRTC by using the interrupt mask flag register. Furthermore, clear the WAFG, RIFG and RTCIF flags after rewriting the MIN register.

Remark SEC, MIN, HOUR, WEEK, DAY, MONTH, and YEAR may be read in any sequence. All the registers do not have to be set and only some registers may be written.

8.4.5 Setting alarm of real-time clock 2

Set the alarm time after setting 0 to WALE (alarm operation invalid) first.

Figure 8 - 23 Alarm Setting Procedure

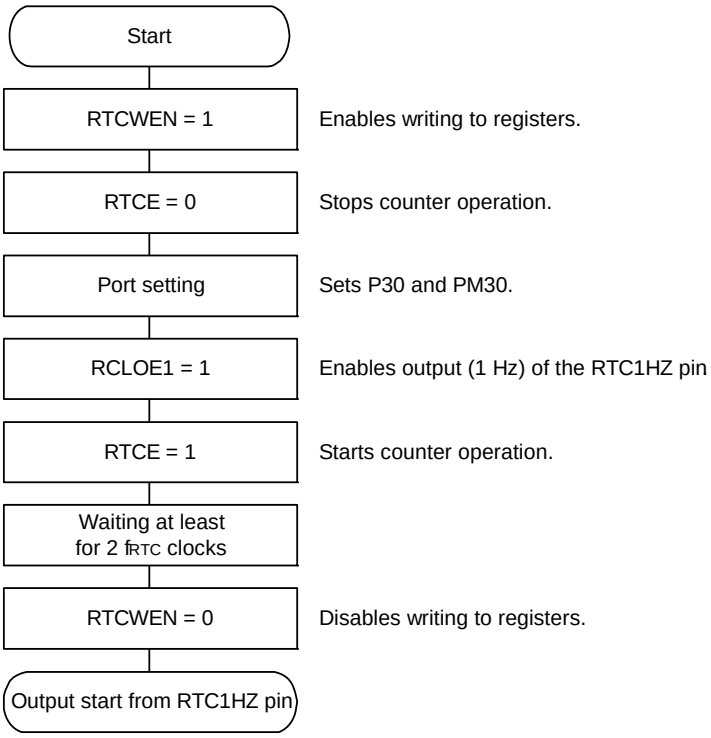


Remark 1. ALARMWM, ALARMWH, and ALARMWW may be written in any sequence.

Remark 2. Fixed-cycle interrupts and alarm match interrupts use the same interrupt source (INTRTC). When using these two types of interrupts at the same time, which interrupt occurred can be judged by checking the fixed-cycle interrupt status flag (RIFG) and the alarm detection status flag (WAFG) upon INTRTC occurrence.

8.4.6 1 Hz output of real-time clock 2

Figure 8 - 24 1 Hz Output Setting Procedure

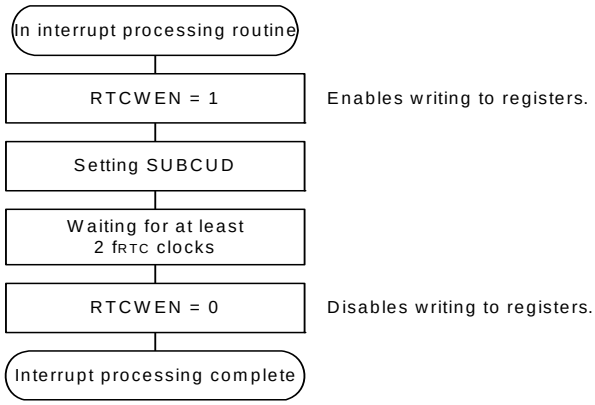


8.4.7 Clock error correction register setting procedure

To set the clock error correction register (SUBCUD), perform the following procedure in the interrupt handling routine of the correction timing signal interrupt (INTRTIT).

Caution The process from generation of a correction timing signal interrupt (INTRTIT) to the interrupt response and SUBCUD setting should be completed within 1 second (before the next timing of correction every second).

Set the clock error correction register after setting RTCWEN to 1 first. Then set RTCWEN to 0 .



8.4.8 Example of watch error correction of real-time clock 2

The clock can be corrected every second with a minimum resolution and accuracy of 0.96 ppm when it is slow or fast, by setting a value to the clock error correction register.
The following shows how to calculate the target correction value, and how to calculate the F8 to F0 values of the clock error correction register from the target correction value.

Calculating the target correction value 1

(When using output frequency of the RTC1HZ pin)

[Measuring the oscillation frequency]
The oscillation frequency Note of each product is measured by outputting about 1 Hz from the RTC1HZ pin when the F15 of the watch error correction register (SUBCUD) is set to 1 (stops the watch error correction).

Note See **8.4.6 1 Hz output of real-time clock 2** for the setting procedure of outputting about 1 Hz from the RTC1HZ pin.

[Measuring the oscillation frequency]
(When the output frequency from the RTCCL pin is 0.9999817 Hz)
Oscillation frequency = 32768 × 0.9999817 ≈ 32767.4 Hz
Assume the target frequency to be 32768 Hz. Then the target correction value is calculated as follows.

Target correction value = Oscillation frequency ÷ Target frequency - 1
= 32767.4 ÷ 32768 - 1
≈ -18.3 ppm

Remark 1. The oscillation frequency is the input clock (f_{RTC}). It can be calculated from the output frequency of the RTC1HZ pin × 32768 when stops the watch error correction.
Remark 2. The target correction value is the oscillation frequency deviation (unit: [ppm]) of the crystal resonator.
Remark 3. The target frequency is the frequency resulting after watch error correction performed.

Calculating the F8 to F0 value of the watch error correction register

The F8 to F0 value of the SUBCUD register is calculated from the target correction value by using the following expression.

$$SUBCUD[8:0] = \left[\frac{\text{Target correction value [ppm]} \times 2^{20}}{10^6}\right]_{\text{Binary (9 digits)}} + 0\ 0010\ 0000\ B$$

Examples 1. When target correction value = -18.3 [ppm]

SUBCUD[8:0] = $(-18.3 \times 2^{20} / 10^6)$ Binary (9 digits) + 000100000B
= (-19.1889408) Binary (9 digits) + 000100000B
= (000010011B) 2's complement + 000100000B
= 111101101B + 000100000B
= 000001101B

Examples 2. When target correction value = 94.0 [ppm]

SUBCUD[8:0] = $(94.0 \times 2^{20} / 10^6)$ Binary (9 digits) + 000100000B
= (98.566144) Binary (9 digits) + 000100000B
= 001100011B + 000100000B
= 010000011B

CHAPTER 9 12-BIT INTERVAL TIMER

9.1 Functions of 12-bit Interval Timer

An interrupt (INTIT) is generated at any previously specified time interval. It can be utilized for wakeup from STOP mode.

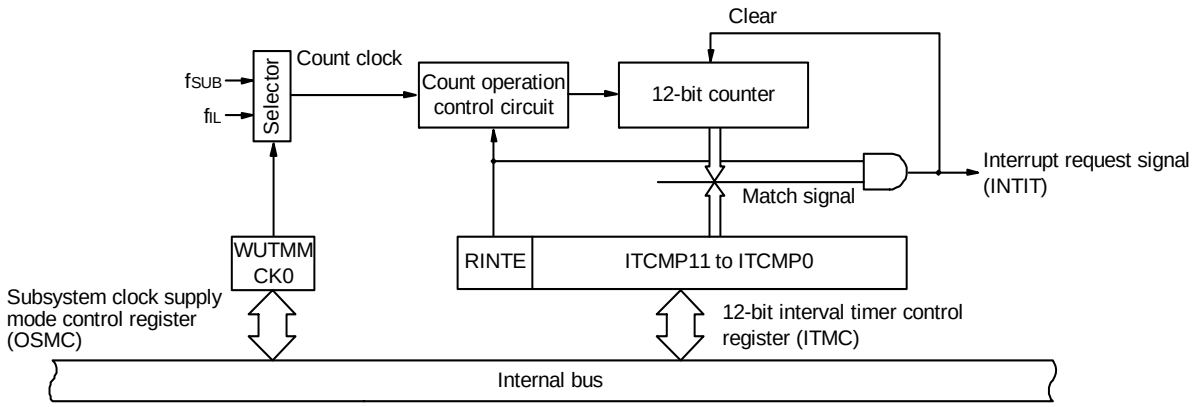
9.2 Configuration of 12-bit Interval Timer

The 12-bit interval timer includes the following hardware.

Table 9 - 1 Configuration of 12-bit Interval Timer

Item	Configuration
Counter	12-bit counter
Control registers	Peripheral enable register 1 (PER1)
	Subsystem clock supply mode control register (OSMC)
	12-bit interval timer control register (ITMC)

Figure 9 - 1 Block Diagram of 12-bit Interval Timer



9.3 Registers Controlling 12-bit Interval Timer

The 12-bit interval timer is controlled by the following registers.

- Peripheral enable register 1 (PER1)
- Subsystem clock supply mode control register (OSMC)
- 12-bit interval timer control register (ITMC)

9.3.1 Peripheral enable register 1 (PER1)

This register is used to enable or disable supplying the clock to the peripheral hardware. Clock supply to the hardware that is not used is also stopped so as to decrease the power consumption and noise.

The PER1 register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 9 - 2 Format of Peripheral enable register 1 (PER1)

Address: F007AH After reset: 00H R/W

Symbol	<7>	6	5	<4>	<3>	<2>	<1>	<0>
PER1	TMKAEN	0	0	AMPEN Note	DTCEN	PGAEN Note	AFEEN Note	DACEN Note

TMKAEN	Control of 12-bit interval timer input clock supply
0	Stops input clock supply. • SFRs used by the 12-bit interval timer cannot be written. • The 12-bit interval timer is in the reset status.
1	Enables input clock supply. • SFRs used by the 12-bit interval timer can be read and written.

Note R5F11N and R5F11P only.

Caution 1. When using the 12-bit interval timer, be sure to first set the TMKAEN bit to 1 and then set the interval timer control register (ITMC), while oscillation of the count clock (f_{RTC}) is stable. If TMKAEN = 0, writing to the registers controlling the 12-bit interval timer is ignored, and, even if the register is read, only the default value is read (except the subsystem clock supply mode control register (OSMC)).

Caution 2. Clock supply to peripheral functions other than the real-time clock 2, 12-bit interval timer, 8-bit interval timer, clock output/buzzer output, LCD controller/driver, serial interface UARTMG0, external signal sampler, and sampling output timer detector can be stopped in STOP mode or HALT mode when the subsystem clock is used, by setting the RTCLPC bit of the subsystem clock supply mode control register (OSMC) to 1.

Caution 3. Be sure to clear bits 5 and 6 to "0".

9.3.2 Subsystem clock supply mode control register (OSMC)

The WUTMMCK0 bit can be used to select the 12-bit interval timer operation clock.

In addition, by stopping clock functions that are unnecessary, the RTCLPC bit can be used to reduce power consumption. For details about setting the RTCLPC bit, see **CHAPTER 5 CLOCK GENERATOR**.

The OSMC register can be set by an 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 9 - 3 Format of Subsystem clock supply mode control register (OSMC)

Address: F00F3H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
OSMC	RTCLPC	0	0	WUTMMCK0	0	0	0	0

WUTMMCK0 Note	Selection of operation clock for real-time clock 2, 12-bit interval timer, 8-bit interval timer, LCD controller/driver, and timers RJ0 and RJ1	Selection of clock output from PCLBUZn pin of clock output/buzzer output
0	Subsystem clock (f_{SUB}) • The subsystem clock is selected as the operation clock for the real-time clock 2, 12-bit interval timer, 8-bit interval timer, and LCD controller/driver. • The low-speed on-chip oscillator cannot be selected as the count source for timers RJ0 and RJ1.	Selecting the subsystem clock (f_{SUB}) is enabled.
1	Low-speed on-chip oscillator clock (f_{IL}) • The low-speed on-chip oscillator clock is selected as the operation clock for the real-time clock 2, 12-bit interval timer, 8-bit interval timer, and LCD controller/driver. • Either the low-speed on-chip oscillator or subsystem clock can be selected as the count source for timers RJ0 and RJ1.	Selecting the subsystem clock (f_{SUB}) is disabled.

Note Be sure to select the subsystem clock (WUTMMCK0 bit = 0) if the subsystem clock is oscillating.

Caution 1. The subsystem clock and low-speed on-chip oscillator clock can only be switched by using the WUTMMCK0 bit if the real-time clock 2, 12-bit interval timer, 8-bit interval timer, and LCD controller/driver are all stopped.

Caution 2. Do not select f_{SUB} as the clock output or buzzer output clock when the WUTMMCK0 bit is 1.

9.3.3 12-bit interval timer control register (ITMC)

This register is used to set up the starting and stopping of the 12-bit interval timer operation and to specify the timer compare value.

The ITMC register can be set by a 16-bit memory manipulation instruction.

Reset signal generation clears this register to 0FFFH.

Figure 9 - 4 Format of 12-bit interval timer control register (ITMC)

Address: FFF90H After reset: 0FFFH R/W

Symbol	15	14	13	12	11 to 0
ITMC	RINTE	0	0	0	ITCMP11 to ITCMP0

RINTE	12-bit interval timer operation control
0	Count operation stopped (count clear)
1	Count operation started

ITCMP11 to ITCMP0	Specification of the 12-bit interval timer compare value
001H	These bits generate an interrupt at the fixed cycle (count clock cycles × (ITCMP setting + 1)).
• • •	
FFFH	
000H	Setting prohibited
Example interrupt cycles when 001H or FFFH is specified for ITCMP11 to ITCMP0 • ITCMP11 to ITCMP0 = 001H, count clock: when f_{SUB} = 32.768 kHz 1/32.768 [kHz] × (1 + 1) = 0.06103515625 [ms] ≈ 61.03 [μs] • ITCMP11 to ITCMP0 = FFFH, count clock: when f_{SUB} = 32.768 kHz 1/32.768 [kHz] × (4095 + 1) = 125 [ms]	

Caution 1. Before changing the RINTE bit from 1 to 0, use the interrupt mask flag register to disable the INTIT interrupt servicing. When the operation starts (from 0 to 1) again, clear the ITIF flag, and then enable the interrupt servicing.

Caution 2. The value read from the RINTE bit is applied one count clock cycle after setting the RINTE bit.

Caution 3. When setting the RINTE bit after returned from standby mode and entering standby mode again, confirm that the written value of the RINTE bit is reflected, or wait that more than one clock of the count clock has elapsed after returned from standby mode. Then enter standby mode.

Caution 4. Only change the setting of the ITCMP11 to ITCMP0 bits when RINTE = 0.
However, it is possible to change the settings of the ITCMP11 to ITCMP0 bits at the same time as when changing RINTE from 0 to 1 or 1 to 0.

9.4 12-bit Interval Timer Operation

9.4.1 12-bit interval timer operation timing

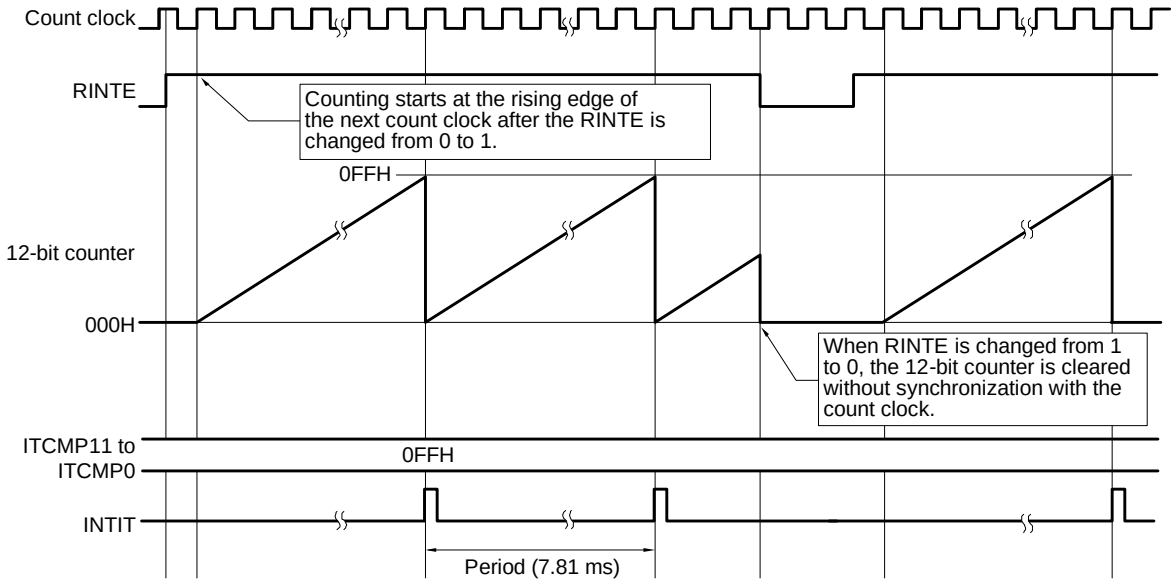
The count value specified for the ITCMP11 to ITCMP0 bits is used as an interval to operate an 12-bit interval timer that repeatedly generates interrupt requests (INTIT).

When the RINTE bit is set to 1, the 12-bit counter starts counting.

When the 12-bit counter value matches the value specified for the ITCMP11 to ITCMP0 bits, the 12-bit counter value is cleared to 0, counting continues, and an interrupt request signal (INTIT) is generated at the same time.

The basic operation of the 12-bit interval timer is as follows.

Figure 9 - 5 12-bit Interval Timer Operation Timing (ITCMP11 to ITCMP0 = 0FFH, count clock: f_{SUB} = 32.768 kHz)

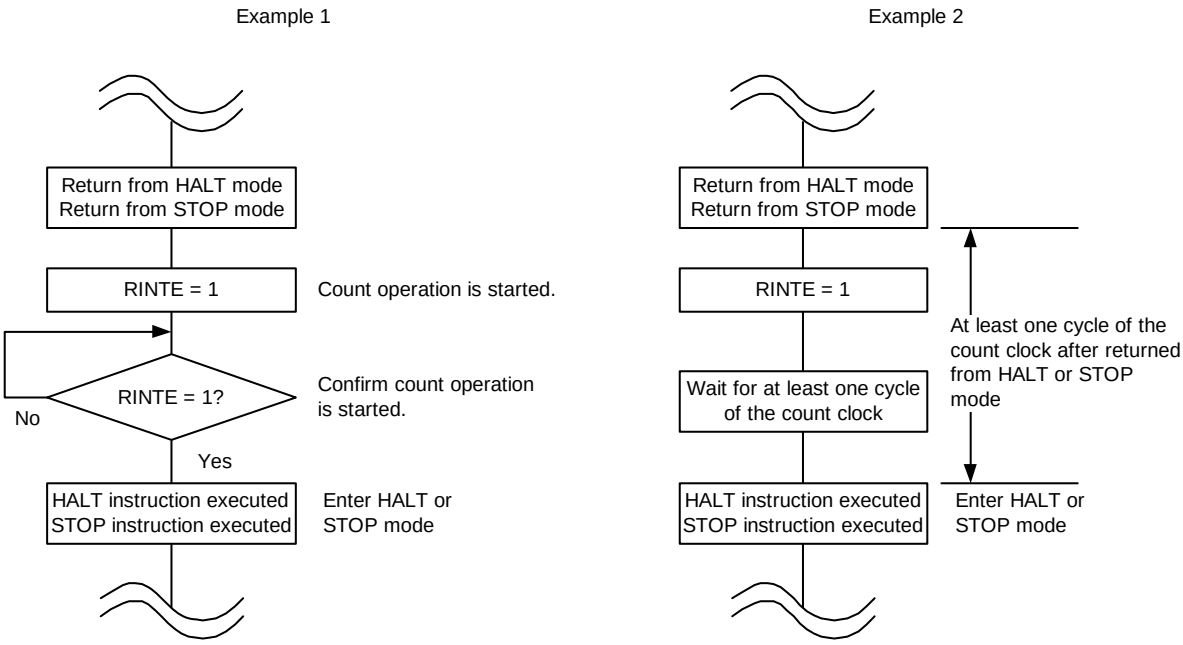


9.4.2 Start of count operation and re-enter to HALT/STOP mode after returned from HALT/STOP mode

When setting the RINTE bit after returned from HALT or STOP mode and entering HALT or STOP mode again, write 1 to the RINTE bit, and confirm the written value of the RINTE bit is reflected or wait for at least one cycle of the count clock.
Then, enter HALT or STOP mode.

- After setting RINTE to 1, confirm by polling that the RINTE bit has become 1, and then enter HALT or STOP mode (see **Example 1** in **Figure 9 - 6**).
- After setting RINTE to 1, wait for at least one cycle of the count clock and then enter HALT or STOP mode (see **Example 2** in **Figure 9 - 6**).

Figure 9 - 6 Procedure of entering to HALT or STOP mode after setting RINTE to 1



CHAPTER 10 TIMER RJ (R5F11R only)

10.1 Functions of Timer RJn

Timer RJn is a 16-bit timer that can be used for pulse output, external pulse width or period measurement, and counting external events. R5F11R has two timer RJ units.

This 16-bit timer consists of a reload register and a down counter. The reload register and the down counter are allocated to the same address, and they can be accessed by accessing the TRJn register.

Table 10 - 1 lists the Timer RJn Specifications. Figure 10 - 1 shows the Timer RJn Block Diagram.

Table 10 - 1 Timer RJn Specifications

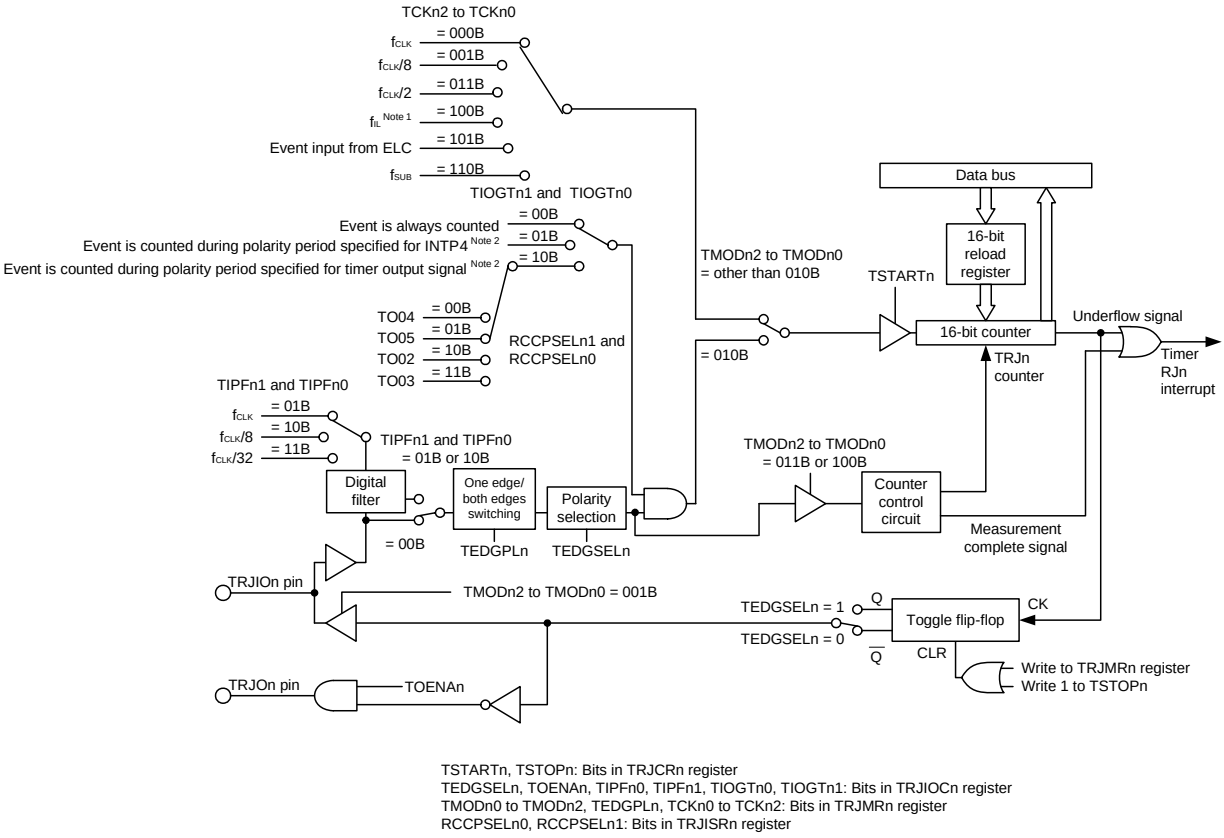
Item		Description
Operating modes	Timer mode	The count source is counted.
	Pulse output mode	The count source is counted and the output is inverted at each underflow of the timer.
	Event counter mode	An external event is counted. Operation is possible in STOP mode.
	Pulse width measurement mode	An external pulse width is measured.
	Pulse period measurement mode	An external pulse period is measured.
Count source (Operating clock)		f_{CLK}, $f_{CLK}/2$, $f_{CLK}/8$, f_{IL}, f_{SUB}, or event input from the event link controller (ELC) selectable
Interrupt		• When the counter underflows. • When the measurement of the active width of the external input (TRJIOn) is completed in pulse width measurement mode. • When the set edge of the external input (TRJIOn) is input in pulse period measurement mode.
Selectable functions		• Coordination with the event link controller (ELC). Event input from the ELC is selectable as a count source.

Remark n: Channel number (n = 0, 1)

10.2 Configuration of Timer RJn

Figure 10 - 1 shows the Timer RJn Block Diagram and Table 10 - 2 lists the Timer RJn Pin Configuration.

Figure 10 - 1 Timer RJn Block Diagram



TSTARTn, TSTOPn: Bits in TRJCRn register
TEDGSELn, TOENAn, TIPFn0, TIPFn1, TIOGTn0, TIOGTn1: Bits in TRJIOCn register
TMODn0 to TMODn2, TEDGPLn, TCKn0 to TCKn2: Bits in TRJMRn register
RCCPSELn0, RCCPSELn1: Bits in TRJISRn register

Note 1. When selecting fIL as the count source, set the WUTMMCK0 bit in the subsystem clock supply mode control register (OSMC) to 1. However, fIL cannot be selected as the count source for timer RJn when fSUB is selected as the operation clock for the real-time clock 2, 12-bit interval timer, 8-bit interval timer, and LCD controller/driver.

Note 2. The polarity can be selected by the RCCPSELn2 bit in the TRJISRn register.

Table 10 - 2 Timer RJn Pin Configuration

Pin Name	I/O	Function
INTP4	Input	Event counter mode control for timer RJn
TRJIO	Input/output	External event input and pulse output for timer RJn
TRJO	Output	Pulse output for timer RJn

Remark n: Channel number (n = 0, 1)

10.3 Registers Controlling Timer RJn

Table 10 - 3 lists the Registers Controlling Timer RJn.

Table 10 - 3 Registers Controlling Timer RJn

Register Name	Symbol
Peripheral enable register 2	PER2
Subsystem clock supply mode control register	OSMC
Timer RJ counter register n Note	TRJn
Timer RJ control register n	TRJCRn
Timer RJ I/O control register n	TRJIOCn
Timer RJ mode register n	TRJMRn
Timer RJ event pin select register n	TRJISRn
Port register 1	P1
Port register 8	P8
Port mode register 1	PM1
Port mode register 8	PM8

Note When the TRJn register is accessed, the CPU does not proceed to the next instruction processing but enters the wait state for CPU processing. For this reason, if this wait state occurs, the number of instruction execution clocks is increased by the number of wait clocks. The number of wait clocks for access to the TRJn register is one clock for both writing and reading.

Remark n: Channel number (n = 0, 1)

10.3.1 Peripheral enable register 2 (PER2)

The PER2 register is used to enable or disable supplying the clock to the peripheral hardware. Clock supply to the hardware that is not used is also stopped so as to decrease the power consumption and noise.

To use timer RJ0, be sure to set bit 0 (TRJ0EN) to 1.

To use timer RJ1, be sure to set bit 1 (TRJ1EN) to 1.

The PER2 register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 10 - 2 Format of Peripheral enable register 2 (PER2)

Address: F00FDH After reset: 00H R/W

Symbol	7	6	5	<4>	<3>	<2>	<1>	<0>
PER2	0	0	0	UARTMG0EN	SMOTDEN	EXSDEN	TRJ1EN	TRJ0EN

TRJnEN	Control of timer RJn input clock supply
0	Stops input clock supply. • SFR used by timer RJn cannot be written. • Timer RJn is in the reset status.
1	Enables input clock supply. • SFR used by timer RJn can be read and written.

Caution 1. When setting timer RJn, be sure to set the TRJnEN bit to 1 first. If TRJnEN = 0, writing to a control register of timer RJn is ignored, and all read values are default values (except for port mode registers 1, 8 (PM1, PM8), and port registers 1, 8 (P1, P8)).

Caution 2. Be sure to set bits 5 to 7 to "0".

Remark n: Channel number (n = 0, 1)

10.3.2 Subsystem clock supply mode control register (OSMC)

The WUTMMCK0 bit can be used to select the timer RJn operation clock.

In addition, by stopping clock functions that are unnecessary, the RTCLPC bit can be used to reduce power consumption. For details about setting the RTCLPC bit, see **CHAPTER 5 CLOCK GENERATOR**.

The OSMC register can be set by an 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 10 - 3 Format of Subsystem clock supply mode control register (OSMC)

Address: F00F3H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
OSMC	RTCLPC	0	0	WUTMMCK0	0	0	0	0

WUTMMCK0 Note	Selection of operation clock for real-time clock 2, 12-bit interval timer, 8-bit interval timer, LCD controller/driver, and timers RJ0 and RJ1	Selection of clock output from PCLBUZn pin of clock output/buzzer output controller
0	Subsystem clock (f_{SUB}) • The subsystem clock is selected as the operation clock for the real-time clock 2, 12-bit interval timer, 8-bit interval timer, and LCD controller/driver. • The low-speed on-chip oscillator cannot be selected as the count source for timers RJ0 and RJ1.	Selecting the subsystem clock (f_{SUB}) is enabled.
1	Low-speed on-chip oscillator clock (f_{IL}) • The low-speed on-chip oscillator clock is selected as the operation clock for the real-time clock 2, 12-bit interval timer, 8-bit interval timer, and LCD controller/driver. • The low-speed on-chip oscillator or subsystem clock can be selected as the count source for timers RJ0 an RJ1.	Selecting the subsystem clock (f_{SUB}) is disabled.

Note Be sure to select the subsystem clock (WUTMMCK0 bit = 0) while the subsystem clock is oscillating.

Caution 1. The subsystem clock and low-speed on-chip oscillator clock can only be switched by using the WUTMMCK0 bit if the real-time clock 2, 12-bit interval timer, 8-bit interval timer, and LCD controller/driver are all stopped.

Caution 2. Do not select f_{SUB} as the clock output or buzzer output clock when the WUTMMCK0 bit is 1.

10.3.3 Timer RJ counter register n (TRJn)

TRJn is a 16-bit register. The write value is written to the reload register and the read value is read from the counter.

The states of the reload register and the counter are changed depending on the TSTARTn bit in the TRJCRn register. For details, see **10.4.1 Reload Register and Counter Rewrite Operation**.

The TRJn register can be set by a 16-bit memory manipulation instruction.

Reset signal generation clears this register to FFFFH.

Figure 10 - 4 Format of timer RJ counter register n (TRJn)

Address: F0508H (TRJ0), F050AH (TRJ1) After reset: FFFFH R/W

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TRJn																

—	Function	Setting Range
Bits 15 to 0	16-bit counter Notes 1, 2	0000H to FFFFH

Note 1. When 1 is written to the TSTOPn bit in the TRJCRn register, the 16-bit counter is forcibly stopped and set to FFFFH.

Note 2. When the setting of bits TCKn2 to TCKn0 in the TRJMRn register is other than 001B (f_{CLK}/8) or 011B (f_{CLK}/2), if the TRJn register is set to 0000H, a request signal to the DTC and the ELC is generated only once immediately after the count starts. However, the TRJOn and TRJIOn output is toggled.
When the TRJn register is set to 0000H in event counter mode, regardless of the value of bits TCKn2 to TCKn0, a request signal to the DTC and the ELC is generated only once immediately after the count starts. In addition, the TRJOn output is toggled even during a period other than the specified count period.
When the TRJn register is set to 0000H or a higher value, a request signal is generated each time TRJn underflows.

Caution **When the TRJn register is accessed, the CPU does not proceed to the next instruction processing but enters the wait state for CPU processing. For this reason, if this wait state occurs, the number of instruction execution clocks is increased by the number of wait clocks. The number of wait clocks for access to the TRJn register is one clock for both writing and reading.**

Remark n: Channel number (n = 0, 1)

10.3.4 Timer RJ control register n (TRJCRn)

The TRJCRn register starts or stops count operation and indicates the status of timer RJn.

The TRJCRn register can be set by an 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Remark n: Channel number (n = 0, 1)

Figure 10 - 5 Format of timer RJ control register n (TRJCRn)

Address: F0240H (TRJCR0), F0244H (TRJCR1) After Reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
TRJCRn	0	0	TUNDFn	TEDGFn	0	TSTOPn	TCSTFn	TSTARTn

TUNDFn	Timer RJn underflow flag
0	No underflow
1	Underflow
[Condition for setting to 0] • When 0 is written to this bit by a program. [Condition for setting to 1] • When the counter underflows.	

TEDGFn	Active edge judgement flag
0	No active edge received
1	Active edge received
[Condition for setting to 0] • When 0 is written to this bit by a program. [Conditions for setting to 1] • When the measurement of the active width of the external input (TRJIOn) is completed in pulse width measurement mode. • The set edge of the external input (TRJIOn) is input in pulse period measurement mode.	

TSTOPn	Timer RJn count forced stop Note 1
When 1 is written to this bit, the count is forcibly stopped. The read value is 0.	

TCSTFn	Timer RJn count status flag Note 2
0	Count stops
1	Count in progress
[Conditions for setting to 0] • When 0 is written to the TSTARTn bit (the TCSTF bit is set to 0 in synchronization with the count source). • When 1 is written to the TSTOPn bit. [Condition for setting to 1] • When 1 is written to the TSTARTn bit (the TCSTF bit is set to 1 in synchronization with the count source).	

TSTARTn	Timer RJn count start Note 2
0	Count stops
1	Count starts
Count operation is started by writing 1 to the TSTARTn bit and stopped by writing 0. When the TSTARTn bit is set to 1 (count starts), the TCSTFn bit is set to 1 (count in progress) in synchronization with the count source. Also, after 0 is written to the TSTARTn bit, the TCSTFn bit is set to 0 (count stops) in synchronization with the count source. For details, see **10.5.1 Count Operation Start and Stop Control**.	

Note 1. When 1 (count is forcibly stopped) is written to the TSTOPn bit, bits TSTARTn and TCSTFn are initialized at the same time. The pulse output level is also initialized.

Note 2. For notes on using bits TSTARTn and TCSTFn, see **10.5.1 Count Operation Start and Stop Control**.

Remark n: Channel number (n = 0, 1)

10.3.5 Timer RJ I/O control register n (TRJIOCn)

The TRJIOCn register sets the input/output of timer RJn.

The TRJIOCn register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Remark n: Channel number (n = 0, 1)

Figure 10 - 6 Format of Timer RJ I/O control register n (TRJIOCn)

Address: F0241H (TRJIOC0), F0245H (TRJIOC1) After Reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
TRJIOCn	TIOGTn1	TIOGTn0	TIPFn1	TIPFn0	0	TOENAn	0	TEDGSELn

TIOGTn1	TIOGTn0	TRJIOn count control Notes 1, 2
0	0	Event is always counted
0	1	Event is counted during polarity period specified for INTP4
1	0	Event is counted during polarity period specified for timer output signal
Other than above		Setting prohibited

TIPFn1	TIPFn0	TRJIOn input filter select
0	0	No filter
0	1	Filter sampled at f_{CLK}
1	0	Filter sampled at $f_{CLK}/8$
1	1	Filter sampled at $f_{CLK}/32$
These bits are used to specify the sampling frequency of the filter for the TRJIOn input. If the input to the TRJIOn pin is sampled and the value matches three successive times, that value is taken as the input value.		

TOENAnn	TRJOn output enable
0	TRJOn output disabled (port)
1	TRJOn output enabled

TEDGSELn	I/O polarity switch
Function varies depending on the operating mode (see **Tables 10 - 4** and **10 - 5**).	

Note 1. When INTP4 or the timer output signal is used, the polarity to count an event can be selected by the RCCPSELn2 bit in the TRJISRn register.

Note 2. Bits TIOGTn0 and TIOGTn1 are enabled only in event counter mode.

Remark n: Channel number (n = 0, 1)

Table 10 - 4 TRJIOn I/O Edge and Polarity Switching

Operating Mode	Function
Timer mode	Not used (I/O port)
Pulse output mode	0: Output is started at high (Initialization level: High) 1: Output is started at low (Initialization level: Low)
Event counter mode	0: Count at rising edge 1: Count at falling edge
Pulse width measurement mode	0: Low-level width is measured 1: High-level width is measured
Pulse period measurement mode	0: Measure from one rising edge to the next rising edge 1: Measure from one falling edge to the next falling edge

Remark n: Channel number (n = 0, 1)

Table 10 - 5 TRJOn Output Polarity Switching

Operating Mode	Function
All modes	0: Output is started at low (Initialization level: Low) 1: Output is started at high (Initialization level: High)

Remark n: Channel number (n = 0, 1)

10.3.6 Timer RJ mode register n (TRJMRn)

The TRJMRn register sets the operating mode of timer RJn.

The TRJMRn register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Remark n: Channel number (n = 0, 1)

Figure 10 - 7 Format of Timer RJ mode register n (TRJMRn)

Address: F0242H (TRJMR0), F0246H (TRJMR1) After Reset: 0000H R/W

Symbol	7	6	5	4	3	2	1	0
TKBCRn	0	TCKn2	TCKn1	TCKn0	TEDGPLn	TMODn2	TMODn1	TMODn0

TCKn2	TCKn1	TCKn0	Timer RJn count source select Notes 1, 2
0	0	0	f_{CLK}
0	0	1	$f_{CLK}/8$
0	1	1	$f_{CLK}/2$
1	0	0	f_{IL} Note 3
1	0	1	Event input from ELC
1	1	0	f_{SUB}
Other than above			Setting prohibited

TEDGPLn	TRJIOn edge polarity select Note 4
0	One edge
1	Both edges

TMODn2	TMODn1	TMODn0	Timer RJn operating mode select Note 5
0	0	0	Timer mode
0	0	1	Pulse output mode
0	1	0	Event counter mode
0	1	1	Pulse width measurement mode
1	0	0	Pulse period measurement mode
Other than above			Setting prohibited

Note 1. When event counter mode is selected, the external input (TRJIOn) is selected as the count source regardless of the setting of bits TCKn0 to TCKn2.

Note 2. Do not switch count sources during count operation. Count sources should be switched when both the TSTARTn and TCSTFn bits in the TRJCRn register are set to 0 (count stops).

Note 3. When selecting f_{IL} as the count source, set the WUTMMCK0 bit in the subsystem clock supply mode control register (OSMC) to 1.
However, f_{IL} cannot be selected as the count source for timer RJn when f_{SUB} is selected as the operation clock for the real-time clock 2, 12-bit interval timer, 8-bit interval timer, and LCD controller/driver.

Note 4. The TEDGPLn bit is enabled only in event counter mode.

Note 5. The operating mode can be changed only when the count is stopped while both the bits TSTARTn and TCSTFn in the TRJCRn register are set to 0 (count stops). Do not change the operating mode during count operation.

Caution **Write access to the TRJMRn register initializes the output from pins TRJOn and TRJIOn of timer RJn. For details on the output level at initialization, refer to the description of Figure 10 - 6 Format of Timer RJ I/O control register n (TRJIOCn).**

Remark n: Channel number (n = 0, 1)

10.3.7 Timer RJ event pin select register n (TRJISRn)

The TRJISRn register selects the timer for controlling the event count period and sets the polarity in event counter mode.

The TRJISRn register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 10 - 8 Format of Timer RJ event pin select register n (TRJISRn)

Address: F0243H (TRJISR0), F0247H (TRJISR1) After Reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
TRJISRn	0	0	0	0	0	RCCPSELn2 Note	RCCPSELn1 Note	RCCPSELn0 Note

RCCPSELn2 Note	Timer output signal and INTP4 polarity selection
0	An event is counted during the low-level period
1	An event is counted during the high-level period

RCCPSELn1 Note	RCCPSELn0 Note	Timer output signal selection
0	0	TO04
0	1	TO05
1	0	TO02
1	1	TO03

Note Bits RCCPSELn0 to RCCPSELn2 are enabled only in event counter mode.

Remark n: Channel number (n = 0, 1)

10.3.8 Port mode registers 1, 8 (PM1, PM8)

These registers set input/output of ports 1 and 8 in 1-bit units.
When using the ports (P15/TRJIO0/SEG34, P80/(SO20/TxD2)/(TI02/TO02)/TRJO0, etc.) to be shared with the timer output pin for timer output, set the port mode register (PMxx) bit and port register (Pxx) bit corresponding to each port to 0.

Example: When using P15/TRJIO0/SEG34 for timer output
Set the PM15 bit of port mode register 1 to 0.
Set the P15 bit of port register 1 to 0.
Set the PFSEG34 bit of LCD port function register 4 to 0.

When using the ports (P15/TRJIO0/SEG34, etc.) to be shared with the timer input pin for timer input, set the port mode register (PMxx) bit corresponding to each port to 1. At this time, the port register (Pxx) bit may be 0 or 1.

Example: When using P15/TRJIO0/SEG34 for timer input
Set the PM15 bit of port mode register 1 to 1.
Set the P15 bit of port register 1 to 0 or 1.
Set the PFSEG34 bit of LCD port function register 4 to 0.

The PM1 and PM8 registers can be set by a 1-bit or 8-bit memory manipulation instruction.
Reset signal generation sets these registers to FFH.

Remark When using the ports to be shared with the segment output pin for timer I/O, be sure to clear the corresponding bit of LCD port function registers 0 to 4 (PFSEG0 to PFSEG4) to “0”.

Figure 10 - 9 Format of Port Mode Registers 1, 8 (PM1, PM8)

Address: FFF21H After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
PM1	PM17	PM16	PM15	PM14	PM13	PM12	PM11	PM10

Address: FFF28H After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
PM8	1	PM86	PM85	PM84	PM83	PM82	PM81	PM80

PMmn	Pmn pin I/O mode selection (m = 1, 8; n = 0 to 7)
0	Output mode (output buffer on)
1	Input mode (output buffer off)

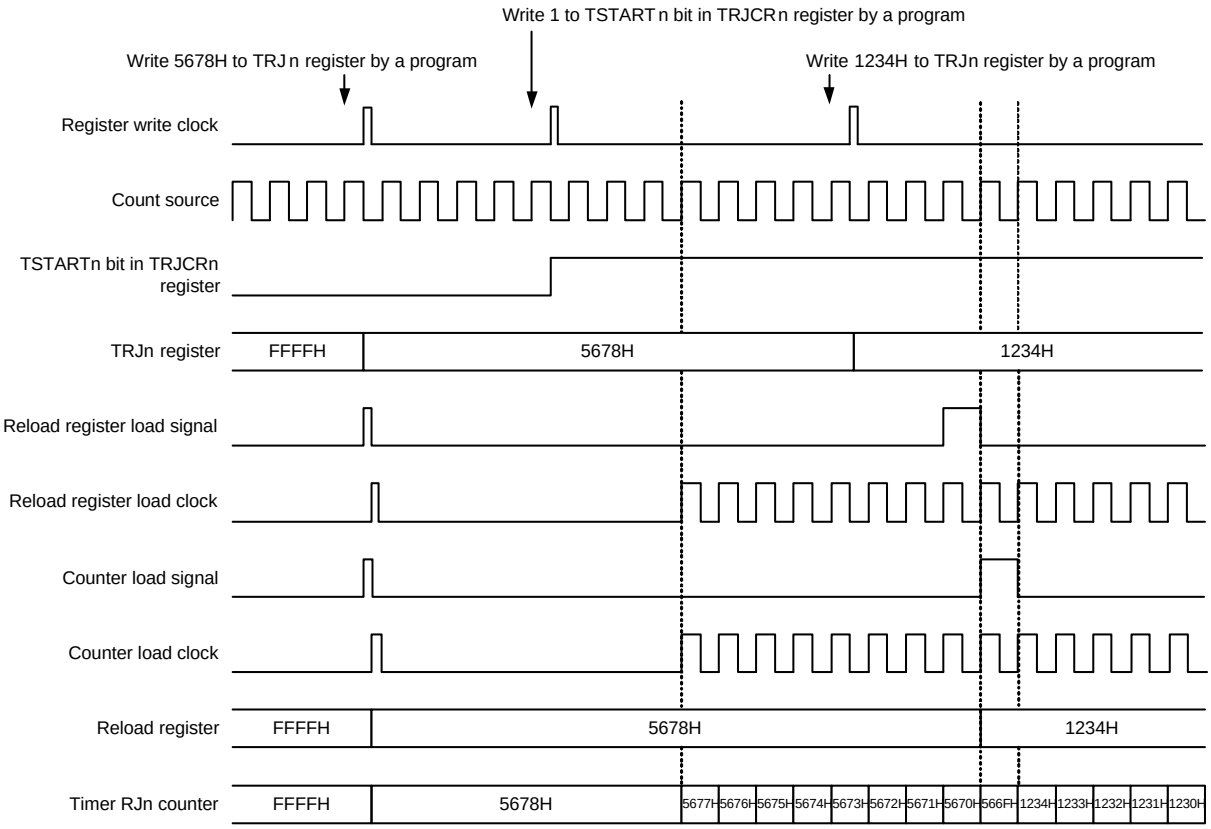
10.4 Timer RJn Operation

10.4.1 Reload Register and Counter Rewrite Operation

Regardless of the operating mode, the timing of the rewrite operation to the reload register and the counter differs depending on the value in the TSTARTn bit in the TRJCRn register. When the TSTARTn bit is 0 (count stops), the count value is directly written to the reload register and the counter. When the TSTARTn bit is 1 (count starts), the value is written to the reload register in synchronization with the count source, and then to the counter in synchronization with the next count source.

Figure 10 - 10 shows the Timing of Rewrite Operation with TSTARTn Bit Value.

Figure 10 - 10 Timing of Rewrite Operation with TSTARTn Bit Value



Remark n: Channel number (n = 0, 1)

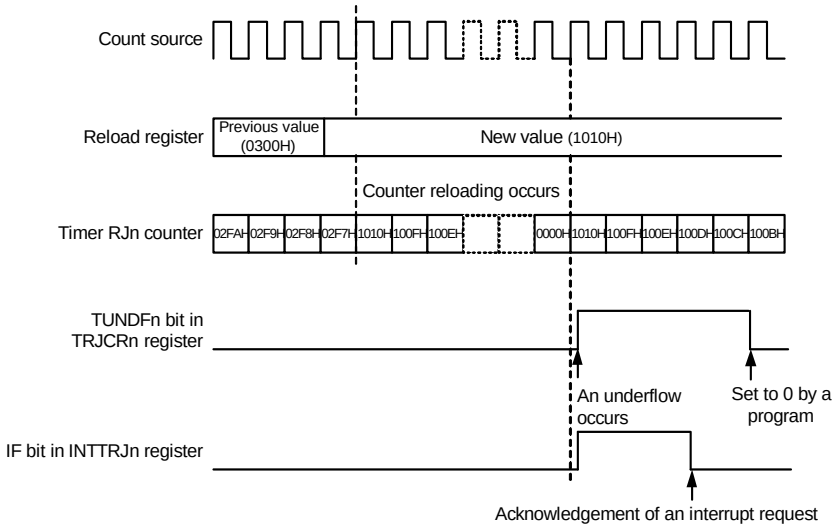
10.4.2 Timer Mode

In this mode, the counter is decremented by the count source selected by bits TCKn0 to TCKn2 in the TRJMRn register.

In timer mode, the count value is decremented by 1 each time the count source is input. When the count value reaches 0000H and the next count source is input, an underflow occurs and an interrupt request is generated.

Figure 10 - 11 shows the Operation Example in Timer Mode.

Figure 10 - 11 Operation Example in Timer Mode



Remark n: Channel number (n = 0, 1)

10.4.3 Pulse Output Mode

In this mode, the counter is decremented by the count source selected by bits TCKn0 to TCKn2 in the TRJMRn register, and the output level of pins TRJIOn and TRJOn pin is inverted each time an underflow occurs.

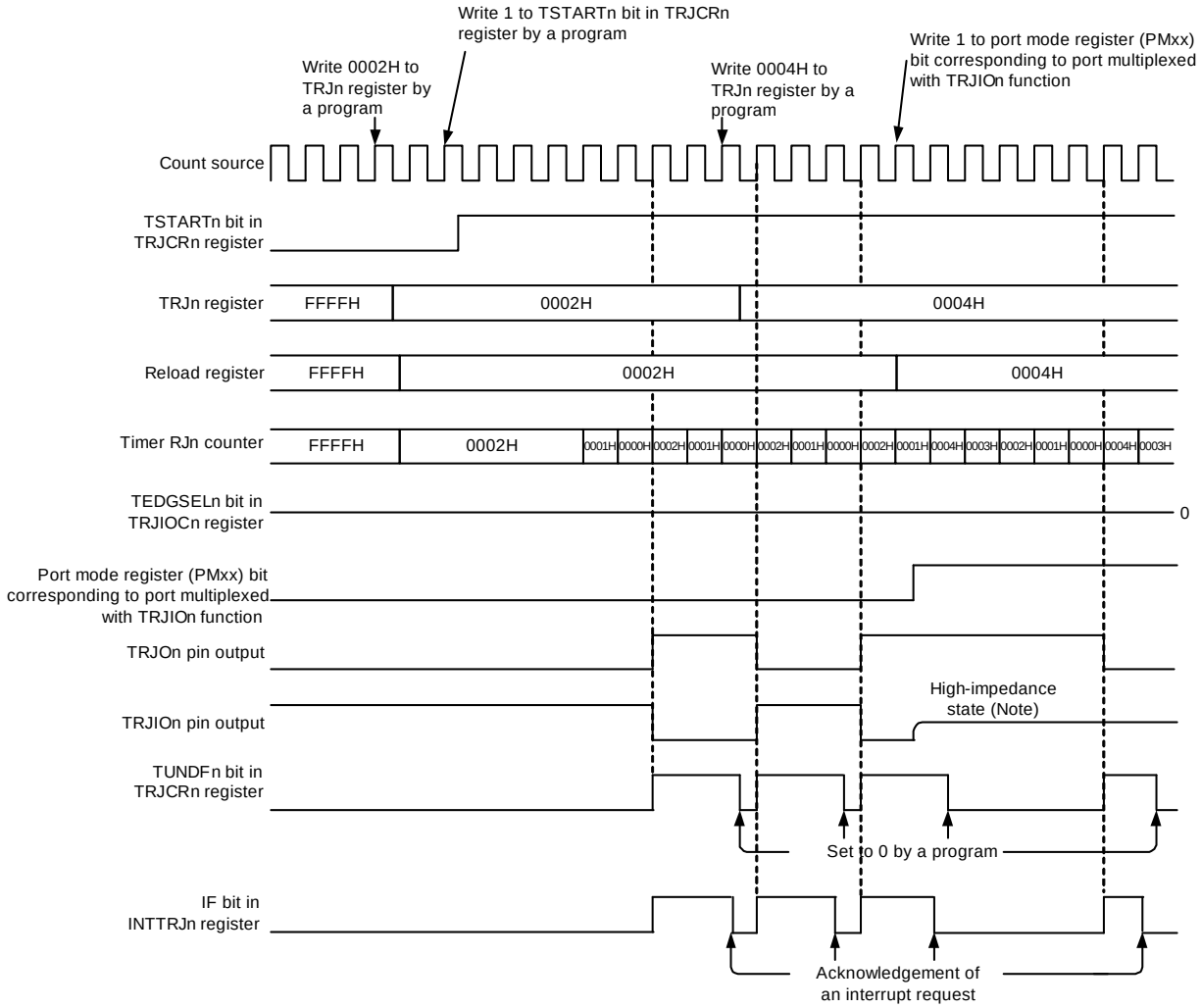
In pulse output mode, the count value is decremented by 1 each time the count source is input. When the count value reaches 0000H and the next count source is input, an underflow occurs and an interrupt request is generated.

In addition, a pulse can be output from pins TRJIOn and TRJOn. The output level is inverted each time an underflow occurs. The pulse output from the TRJOn pin can be stopped by the TOENAn bit in the TRJIOCn register.

Also, the output level can be selected by the TEDGSELn bit in the TRJIOCn register.

Figure 10 - 12 shows the Operation Example in Pulse Output Mode.

Figure 10 - 12 Operation Example in Pulse Output Mode



Note: The TRJIOn pin becomes high impedance by output enable control on the port selected as the TRJIOn function.

Remark n: Channel number (n = 0, 1)

10.4.4 Event Counter Mode

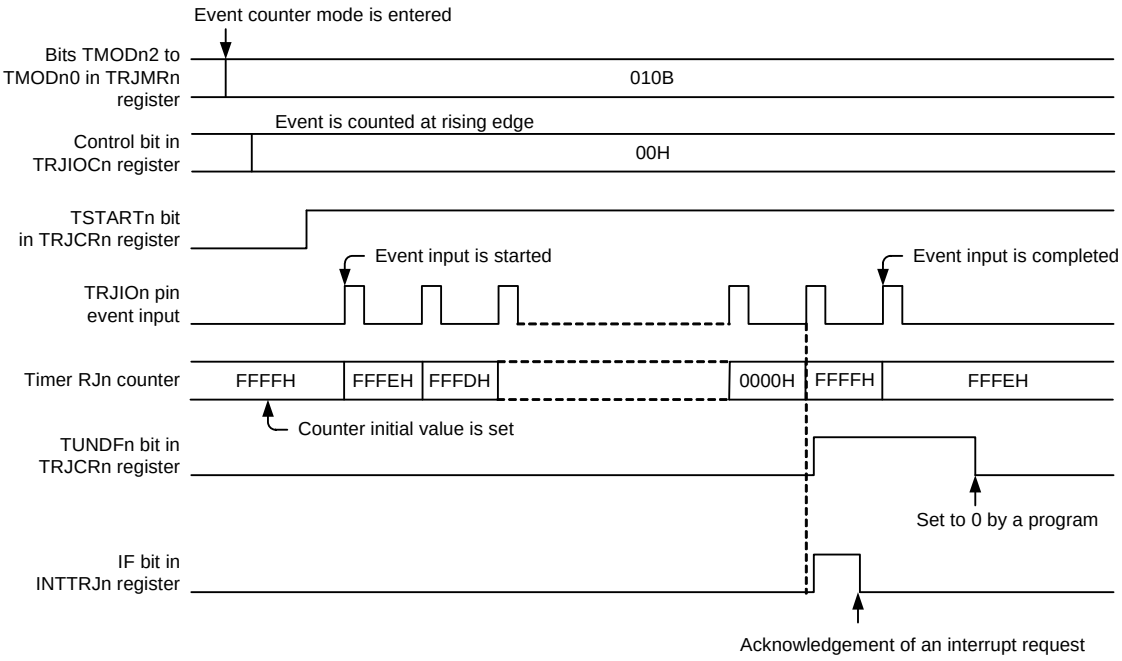
In this mode, the counter is decremented by an external event signal (count source) input to the TRJIOn pin. Various periods for counting events can be set by bits TIOGTn0 and TIOGTn1 in the TRJIOCn register and the TRJISRn register. In addition, the filter function for the TRJIOn input can be specified by bits TIPFn0 and TIPFn1 in the TRJIOCn register.

Also, the output from the TRJOn pin can be toggled even in event counter mode.

When event counter mode is used, see **10.5.5 Procedure for Setting Pins TRJOn and TRJIOn**.

Figure 10 - 13 shows the Operation Example 1 in Event Counter Mode.

Figure 10 - 13 Operation Example 1 in Event Counter Mode

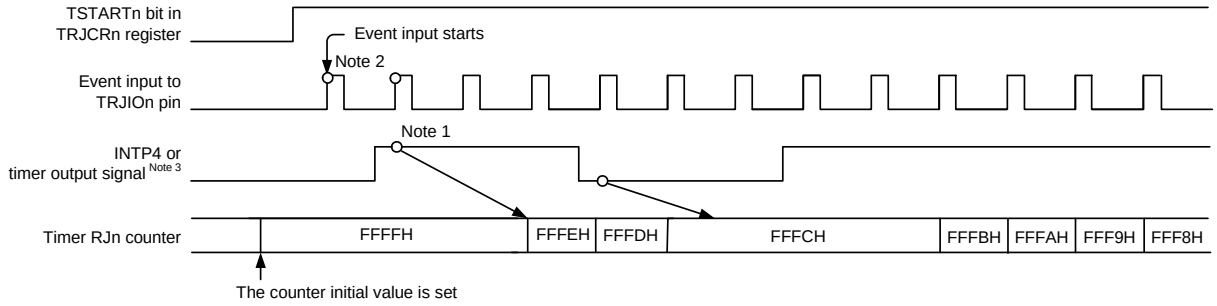


Remark n: Channel number (n = 0, 1)

Figure 10 - 14 shows an operation example for counting during the specified period in event counter mode (bits TIOGTn1 and TIOGTn0 in the TRJIOn0 register are set to 01B or 10B).

Figure 10 - 14 Operation Example 2 in Event Counter Mode

Timing example when the setting of operating mode is as follows:
TRJMRn register: TMODn2, TMODn1, TMODn0 = 010B (event counter mode)
TRJIOCn register: TIOGTn1, TIOGTn0 = 01B (event is counted during specified period for external interrupt pin)
TIPFn1, TIPFn0 = 00B (no filter)
TEDGSELn = 0 (count at rising edge)
TRJISRn register: RCCPSELn2 = 1 (high-level period is counted)



The following notes apply only when bits TIOGTn1 and TIOGTn0 in the TRJIOCn register are 01B or 10B for the setting of operating mode in event count mode.

Note 1. To control synchronization, there is a delay of two cycles of the count source until count operation is affected.

Note 2. Count operation may be performed for two cycles of the count source immediately after the count is started, depending on the previous state before the count is stopped.
To disable the count for two cycles immediately after the count is started, write 1 to the TSTOPn bit in the TRJCRn register to initialize the internal circuit, and then make operation settings before starting count operation.

Note 3. For the timer output signal selected by the RCCPSELn1 and RCCPSELn0 bits in the TRJISRn register, the pin assigned to the timer output function cannot be used as the output of any multiplexed function other than the timer.

Remark n: Channel number (n = 0, 1)

10.4.5 Pulse Width Measurement Mode

In this mode, the pulse width of an external signal input to the TRJIOn pin is measured.

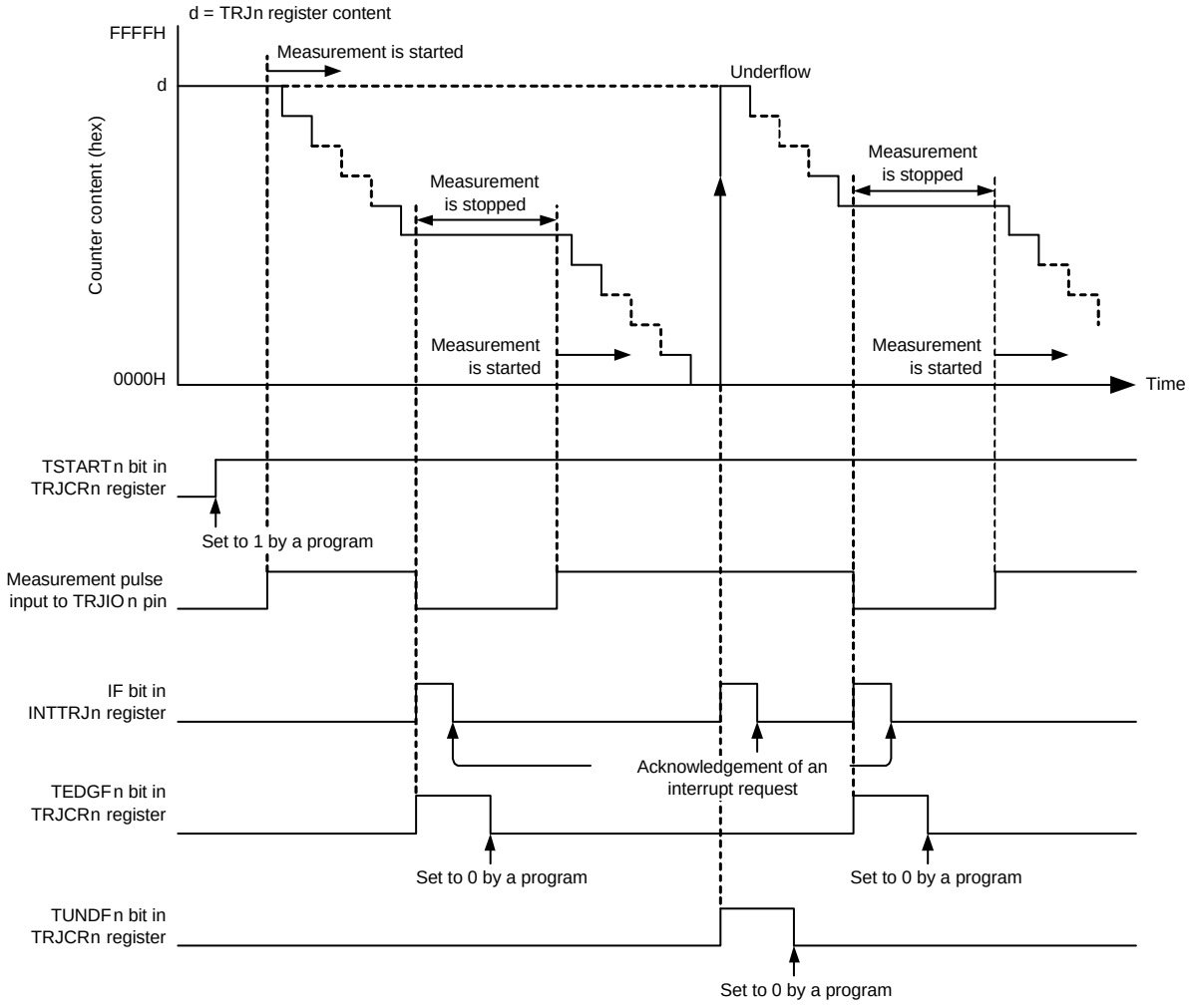
When the level specified by the TEDGSELn bit in the TRJIOCn register is input to the TRJIOn pin, the decrement is started with the selected count source. When the specified level on the TRJIOn pin ends, the counter is stopped, the TEDGFn bit in the TRJCRn register is set to 1 (active edge received), and an interrupt request is generated. The measurement of pulse width data is performed by reading the count value while the counter is stopped. Also, when the counter underflows during measurement, the TUNDFn bit in the TRJCRn register is set to 1 (underflow) and an interrupt request is generated.

Figure 10 - 15 shows the Operation Example in Pulse Width Measurement Mode.

When accessing bits TEDGFn and TUNDFn in the TRJCR0 register, see **10.5.2 Access to Flags (Bits TEDGFn and TUNDFn in TRJCRn Register)**.

Figure 10 - 15 Operation Example in Pulse Width Measurement Mode

This example applies when the high -level width of the measurement pulse is measured (TEDGSEL n bit in TRJIOC n register = 1)



Remark n: Channel number (n = 0, 1)

10.4.6 Pulse Period Measurement Mode

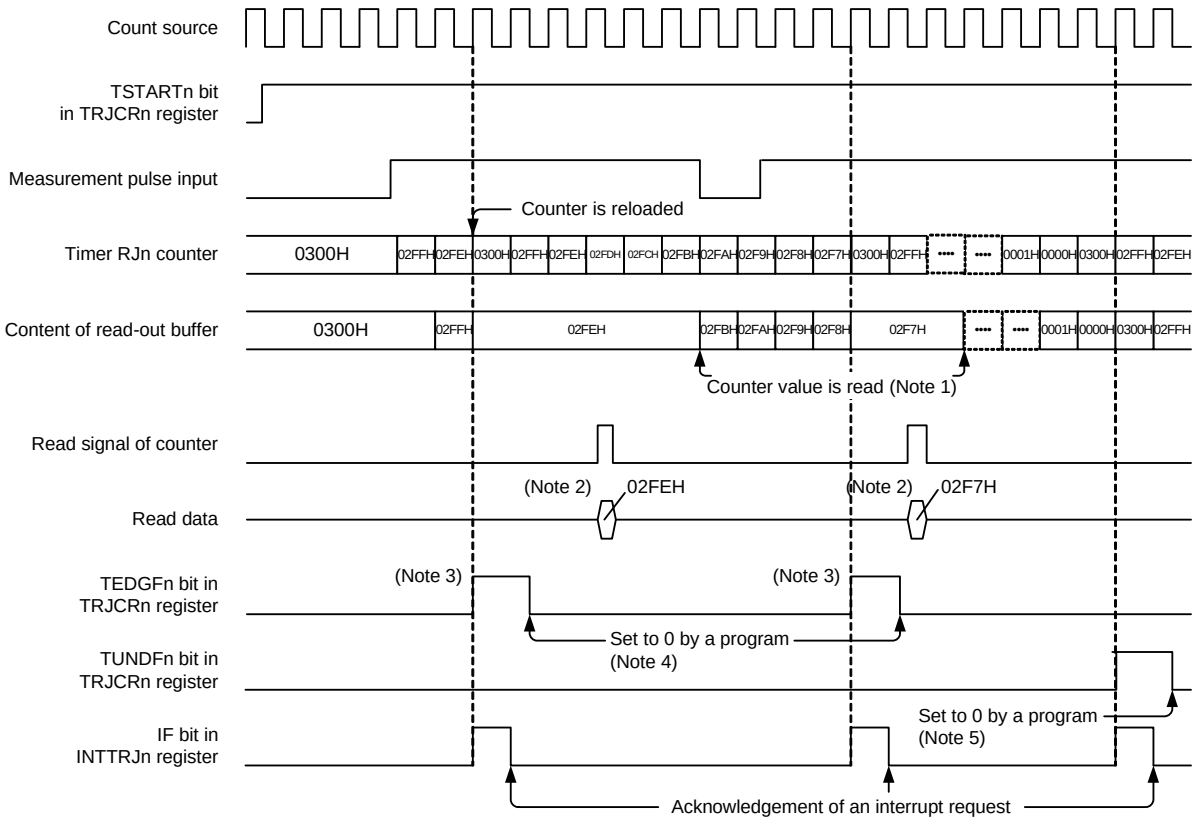
In this mode, the pulse period of an external signal input to the TRJIOn pin is measured.

The counter is decremented by the count source selected by bits TCKn0 to TCKn2 in the TRJMRn register. When a pulse with the period specified by the TEDGSELn bit in the TRJIOCn register is input to the TRJIO0 pin, the count value is transferred to the read-out buffer at the rising edge of the count source. The value in the reload register is loaded to the counter at the next rising edge. Simultaneously, the TEDGFn bit in the TRJCRn register is set to 1 (active edge received) and an interrupt request is generated. The read-out buffer (TRJn register) is read at this time and the difference from the reload value is the period data of the input pulse. The period data is retained until the read-out buffer is read. When the counter underflows, the TUNDFn bit in the TRJCRn register is set to 1 (underflow) and an interrupt request is generated.

Figure 10 - 16 shows the Operation Example in Pulse Period Measurement Mode.

Only input pulses with a period longer than twice the period of the count source. Also, the low-level and high-level widths must be both longer than the period of the count source. If a pulse period shorter than these conditions is input, the input may be ignored

Figure 10 - 16 Operation Example in Pulse Period Measurement Mode



This example applies when the initial value of the TRJn register is set to 0300H, the TEDGSELn bit in the TRJIOCn register is set to 0, and the period from one rising edge to the next edge of the measurement pulse is measured.

Note 1. Reading from the TRJn register must be performed during the period from when the TEDGFn bit is set to 1 (active edge received) until the next active edge is input. The content of the read-out buffer is retained until the TRJn register is read. If it is not read before the active edge is input, the measurement result of the previous period is retained.

Note 2. When the TRJn register is read in pulse period measurement mode, the content of the read-out buffer is read.

Note 3. When the active edge of the measurement pulse is input and then the set edge of an external pulse is input, the TEDGFn bit in the TRJCRn register is set to 1 (active edge received).

Note 4. To set to 0 by a program, write 0 to the TEDGFn bit in the TRJCRn register using an 8-bit memory manipulation instruction.

Note 5. To set to 0 by a program, write 0 to the TUNDFn bit in the TRJCRn register using an 8-bit memory manipulation instruction.

Remark n: Channel number (n = 0, 1)

10.4.7 Coordination with Event Link Controller (ELC)

Through coordination with the ELC, event input from the ELC can be set to be the count source. Bits TCKn0 to TCKn2 in the TRJMRn register count at the rising edge of event input from the ELC. However, ELC input does not function in event counter mode.

The ELC setting procedure is shown below:

• Procedure for starting operation

(1) Set the event output destination select register (ELSELRn) for the ELC.
(2) Set the operating mode for the event generation source.
(3) Set the mode for timer RJn.
(4) Start the count operation of timer RJn.
(5) Start the operation of the event generation source.

• Procedure for stopping operation

(1) Stop the operation of the event generation source.
(2) Stop the count operation of timer RJn.
(3) Set the event output destination select register (ELSELRn) for the ELC to 0.

Remark n: Channel number (n = 0, 1)
For ELSELRn, n = 00 to 25

10.4.8 Output Settings for Each Mode

Tables 10 - 6 and 10 - 7 list the states of pins TRJOn and TRJIOn in each mode.

Table 10 - 6 TRJOn Pin Setting

Operating Mode	TRJIOCn Register		TRJOn Pin Output
	TOENAn Bit	TEDGSELn Bit	
All modes	1	1	Inverted output
		0	Normal output
	0	0 or 1	Output disabled

Table 10 - 7 TRJIOn Pin Setting

Operating Mode	TRJIOCn Register		TRJIOn Pin I/O
	PMXX Bit Note	TEDGSELn Bit	
Timer mode	0 or 1	0 or 1	Input (Not used)
Pulse output mode	1	0 or 1	Output disabled (Hi-z output)
	0	1	Normal output
		0	Inverted output
Event counter mode	1	0 or 1	Input
Pulse width measurement mode			
Pulse period measurement mode			

Note The port mode register (PMxx) bit corresponding to port multiplexed with TRJIOn function.

Remark n: Channel number (n = 0, 1)

10.5 Cautions for Timer RJn

10.5.1 Count Operation Start and Stop Control

• When event count mode is set or the count source is set to other than the ELC

After 1 (count starts) is written to the TSTARTn bit in the TRJCRn register while the count is stopped, the TCSTFn bit in the TRJCRn register remains 0 (count stops) for three cycles of the count source. Do not access the registers associated with timer RJn Note other than the TCSTFn bit until this bit is set to 1 (count in progress).

After 0 (count stops) is written to the TSTARTn bit during a count operation, the TCSTFn bit remains 1 for three cycles of the count source. When the TCSTFn bit is set to 0, the count is stopped. Do not access the registers associated with timer RJn Note other than the TCSTFn bit until this bit is set to 0.

Clear the interrupt register before changing the TATARTn bit from 0 to 1. Refer to **CHAPTER 26 INTERRUPT FUNCTIONS** for details.

Note Registers associated with timer RJn: TRJn, TRJCRn, TRJIOCn, TRJMRn, and TRJISRn

• When event count mode is set or the count source is set to the ELC

After 1 (count starts) is written to the TSTARTn bit in the TRJCRn register while the count is stopped, the TCSTFn bit in the TRJCRn register remains 0 (count stops) for two cycles of the CPU clock. Do not access the registers associated with timer RJn Note other than the TCSTFn bit until this bit is set to 1 (count in progress).

After 0 (count stops) is written to the TSTARTn bit during a count operation, the TCSTFn bit remains 1 for two cycles of the CPU clock. When the TCSTFn bit is set to 0, the count is stopped. Do not access the registers associated with timer RJn Note other than the TCSTFn bit until this bit is set to 0.

Clear the interrupt register before changing the TATARTn bit from 0 to 1. Refer to **CHAPTER 26 INTERRUPT FUNCTIONS** for details.

Note Registers associated with timer RJn: TRJn, TRJCRn, TRJIOCn, TRJMRn, and TRJISRn

10.5.2 Access to Flags (Bits TEDGFn and TUNDFn in TRJCRn Register)

Bits TEDGFn and TUNDFn in the TRJCRn register are set to 0 by writing 0 by a program, but writing 1 to these bits has no effect. If a read-modify-write instruction is used to set the TRJCRn register, bits TEDGFn and TUNDFn may be erroneously set to 0 depending on the timing, even when the TEDGFn bit is set to 1 (active edge received) and the TUNDFn bit is set to 1 (underflow) during execution of the instruction. Use an 8-bit memory manipulation instruction to access to the TRJCRn register.

10.5.3 Access to Counter Register

When bits TSTARTn and TCSTFn in the TRJCRn register are both 1 (count starts), allow at least three cycles of the count source clock between writes when writing to the TRJn register successively.

Remark n: Channel number (n = 0, 1)

10.5.4 When Changing Mode

The registers associated with timer RJn operating mode (TRJIOCn, TRJMRn, and TRJISRn) can be changed only when the count is stopped with both the TSTARTn and TCSTFn bits set to 0 (count stops). Do not change these registers during count operation.

When the registers associated with timer RJn operating mode are changed, the values of bits TSTARTn and TCSTFn are undefined. Write 0 (no active edge received) to the TEDGFn bit and 0 (no underflow) to the TUNDFn bit before starting the count.

10.5.5 Procedure for Setting Pins TRJOn and TRJIOn

After a reset, the I/O ports multiplexed with pins TRJOn and TRJIOn function as input ports.

To output from pins TRJOn and TRJIOn, use the following setting procedure:

Changing procedure

(1) Set the mode.
(2) Set the initial value/output enabled.
(3) Set the port register bits corresponding to pins TRJOn and TRJIOn to 0.
(4) Set the port mode register bits corresponding to pins TRJOn and TRJIOn to output mode.
(Output is started from pins TRJOn and TRJIOn)
(5) Start the count (TSTARTn in TRJCRn register = 1).

To input from the TRJIOn pin, use the following setting procedure:

(1) Set the mode.
(2) Set the initial value/edge selected.
(3) Set the port mode register bit corresponding to TRJIOn pin to input mode.
(Input is started from the TRJIOn pin)
(4) Start the count (TSTARTn in TRJMRn register = 1).
(5) Wait until the TCSTFn bit in the TRJCRn register is set to 1 (count in progress).
(In event counter mode only)
(6) Input an external event from the TRJIOn pin.
(7) The processing on completion of the first measurement is invalid (the measured value is valid for the second and subsequent times). (In pulse width measurement mode and pulse period measurement mode only)

10.5.6 When Timer RJn is not Used

When timer RJn is not used, set bits TMODn2 to TMODn0 in the TRJMRn register to 000B (timer mode) and set the TOENAn bit in the TRJIOCn register to 0 (TRJOn output disabled).

10.5.7 When Timer RJn Operating Clock is Stopped

Supplying or stopping the timer RJn clock can be controlled by the TRJnEN bit in the PER2 register. Note that the following SFRs cannot be accessed while the timer RJn clock is stopped. Make sure the timer RJn clock is supplied before accessing any of these registers.

Registers TRJn, TRJCRn, TRJMRn, TRJIOCn, and TRJISRn.

Remark n: Channel number (n = 0, 1)

10.5.8 Procedure for Setting STOP Mode (Event Counter Mode)

To perform event counter mode operation during STOP mode, first supply the timer RJn clock and then use the following procedure to enter STOP mode.

Setting procedure

(1) Set the operating mode.
(2) Start the count (TSTARTn = 1, TCSTFn = 1).
(3) Stop supplying the timer RJn clock.

To stop event counter mode operation during STOP mode, use the following procedure to stop operation.

(1) Supply the timer RJn clock.
(2) Stop the count (TSTARTn = 0, TCSTFn = 0)

10.5.9 Functional Restriction in STOP Mode (Event Counter Mode Only)

When event counter mode operation is performed during STOP mode, the digital filter function cannot be used.

10.5.10 When Count is Forcibly Stopped by TSTOP Bit

After the counter is forcibly stopped by the TSTOPn bit in the TRJCRn register, do not access the following SFRs for one cycle of the count source.

Registers TRJn, TRJCRn, and TRJMRn

10.5.11 Digital Filter

When the digital filter is used, do not start timer operation for five cycles of the digital filter clock after setting bits TIPFn1 and TIPFn0 in the TRJIOCn.

Also, do not start timer operation for five cycles of the digital filter clock when the TEDGSELn bit in the TRJIOCn register is changed while the digital filter is used.

10.5.12 When Selecting f_{IL} as Count Source

When selecting f_{IL} as the count source, set the WUTMMCK0 bit in the subsystem clock supply mode control register (OSMC) to 1. However, f_{IL} cannot be selected as the count source for timer RJn when f_{SUB} is selected as the operation clock for the real-time clock 2, 12-bit interval timer, 8-bit interval timer, and LCD controller/driver.

Remark n: Channel number (n = 0, 1)

CHAPTER 11 SAMPLING OUTPUT TIMER DETECTOR (R5F11R only)

11.1 Functions of Sampling Output Timer Detector

The sampling output timer detector (SMOTD) has the sampling clock output function and sampling detector function.

The sampling clock output function outputs the sampling clock signal periodically from the SMOm pin (m = 0 to 2). The sampling detector function detects the levels being input on the SMP0 to SMP5 pins on falling edges of the sampling clock signal, and outputs the corresponding interrupt signals (INTSMP0 to INTSMP5) if the active level is detected.

Table 11 - 1 describes the function of the sampling output timer detector.

Table 11 - 1 Function of Sampling Output Timer Detector

Item	Description	
PWM performance	High pulse width	MIN. $1/f_{SUB}$ MAX. $2^8 \times 2^6/f_{SUB}$ Note
	PWM waveform period	MIN. $2/f_{SUB}$ MAX. $2^8 \times 2^{14}/f_{SUB}$
Functions	• Sampling clock output function • Sampling detector function	
Interrupt output	• Sampling output timer interval interrupt (INTSMOTA) • Sampling output timer compare match interrupt (INTSMOTB) • Sampling detector detection interrupt (INTSMPn) (n = 0 to 5)	

Note Setting a longer pulse width at high level than the period of the PWM waveform is prohibited. Be sure to set a pulse width that is shorter than the period of the PWM waveform.

11.2 Configuration of Sampling Output Timer Detector

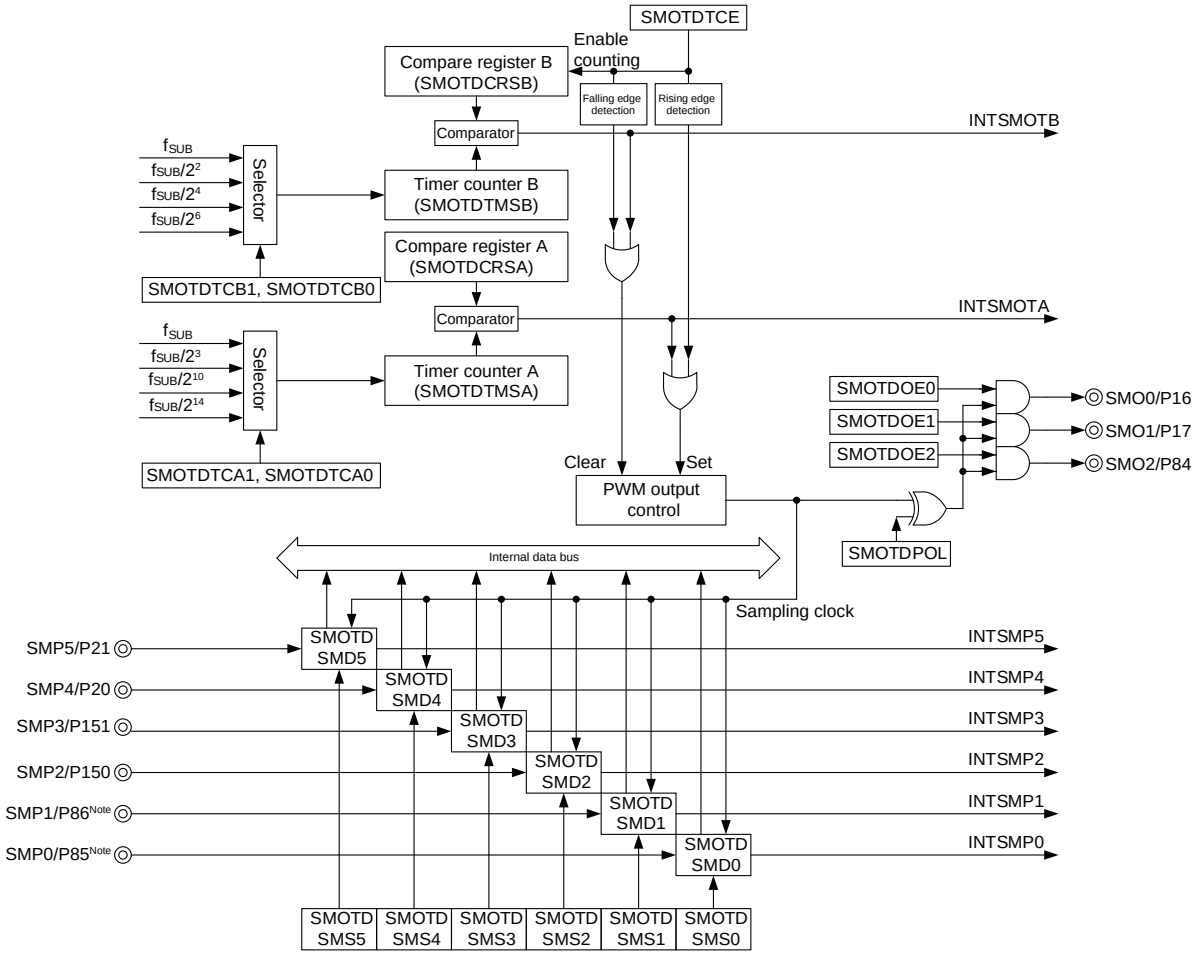
The sampling output timer detector includes the following hardware.

Table 11 - 2 Configuration of Sampling Output Timer Detector

Item	Configuration
Input clock to sampling output timer	f_{SUB} or frequency-divided f_{SUB}
Output from sampling output timer	Output signals from SMO0 to SMO2 (PWM output)
Sampling input	SMP0 to SMP5
Control registers	Peripheral enable register 2 (PER2) SMOTD timer counter A (SMOTDTMSA) SMOTD timer counter B (SMOTDTMSB) SMOTD compare register A (SMOTDCRSA) SMOTD compare register B (SMOTDCRSB) SMOTD clock select register (SMOTDTCS) SMOTD control register (SMOTDCR) SMOTD sampling level setting register (SMOTDSMS) SMOTD sampling pin status register (SMOTDSMD) SMOTD output control register (SMOTDOE) Port mode registers 1, 2, 4, 8, 15 (PM1, PM2, PM4, PM8, PM15) Port registers 1, 2, 4, 8, 15 (P1, P2, P4, P8, P15)

Figure 11 - 1 shows a block diagram of the sampling output timer detector.

Figure 11 - 1 Block Diagram of Sampling Output Timer Detector



Note The functions of the SMP0 and SMP1 pins can be selected by the PIOR04 bit of the PIOR0 register. For details, see **CHAPTER 4 PORT FUNCTIONS**.

Caution When using the sampling output timer detector, be sure to select the subsystem clock (WUTMMCK0 = 0).

11.3 Registers Controlling the Sampling Output Timer Detector

The sampling output timer detector is controlled by the following registers.

- Peripheral enable register 2 (PER2)
- SMOTD timer counter A (SMOTDTMSA)
- SMOTD timer counter B (SMOTDTMSB)
- SMOTD compare register A (SMOTDCRSA)
- SMOTD compare register B (SMOTDCRSB)
- SMOTD clock select register (SMOTDTCS)
- SMOTD control register (SMOTDCR)
- SMOTD sampling level setting register (SMOTDSMS)
- SMOTD sampling pin status register (SMOTDSMD)
- SMOTD output control register (SMOTDOE)
- Port mode registers 1, 2, 4, 8, 15 (PM1, PM2, PM4, PM8, PM15)
- Port registers 1, 2, 4, 8, 15 (P1, P2, P4, P8, P15)

(1) Peripheral enable register 2 (PER2)

The PER2 register is used to enable or disable supplying the clock to the peripheral hardware. Clock supply to the hardware that is not used is also stopped so as to decrease the power consumption and noise.

When using the sampling output timer detector, be sure to set bit 3 (SMOTDEN) to 1.

The PER2 register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 11 - 2 Format of Peripheral Enable Register 2 (PER2)

Address: F00FDH After reset: 00H R/W

Symbol	7	6	5	<4>	<3>	<2>	<1>	<0>
PER2	0	0	0	UARTMG0EN	SMOTDEN	EXSDEN	TRJ1EN	TRJ0EN

SMOTDEN	Control of sampling output timer detector input clock supply
0	Stops input clock supply. • SFRs used by the sampling output timer detector cannot be written. • The sampling output timer detector is in the reset status.
1	Enables input clock supply. • SFRs used by the sampling output timer detector can be read and written.

Caution When setting the sampling output timer detector, be sure to set SMOTDEN to 1 first. If SMOTDEN = 0, writing to a control register of the sampling output timer detector is ignored, and rall read values are default values (except for port mode registers 1, 2, 4, 8, and 15 (PM1, PM2, PM4, PM8, and PM15), and port registers 1, 2, 4, 8, and 15 (P1, P2, P4, P8, and P15)).

(2) SMOTD timer counter A (SMOTDTMSA)

The SMOTDTMSA counter is an 8-bit counter that is used to generate the period of the PWM waveform of the sampling clock output from the SMOm pin.

The SMOTDTMSA counter cannot be directly manipulated by a program (cannot be read/written).

The counter value is cleared to 00H in the following cases.

(i) The reset signal is generated.

(ii) SMOTDTCE is cleared (when "1" is changed to "0").

(iii) SMOTDTMSA matches SMOTDCRSA.

Figure 11 - 3 Format of SMOTD Timer Counter A (SMOTDTMSA)

Address: - After reset: 00H R/W disabled

Symbol	7	6	5	4	3	2	1	0
SMOTD TMSA	SMOTDTMSA[7:0]							

SMOTD TMSA[7:0]	SMOTD timer counter A
00H to FFH	Counting start condition: SMOTDTCE is set (when "0" is changed to "1"). Counting condition: Counter is incremented by the clock source selected with the SMOTDTCA1 and SMOTDTCA0 bits when SMOTDTCE = 1. Counter clear condition: • The reset signal is generated. • SMOTDTCE is cleared (when "1" is changed to "0"). • SMOTDTCA matches SMOTDCRSA.

Caution If the counting condition and counter clear condition are generated simultaneously, the counter is cleared.

(3) SMOTD timer counter B (SMOTDTMSB)

The SMOTDTMSB counter is an 8-bit counter that is used to generate a high pulse width of the PWM waveform of the sampling clock output from the SMOm pin.

The SMOTDTMSB counter cannot be directly manipulated by a program (cannot be read/written).

The counter value is cleared to 00H in the following cases.

(i) The reset signal is generated.

(ii) SMOTDTCE is cleared (when "1" is changed to "0").

(iii) SMOTDTMSB matches SMOTDCRSB.

Figure 11 - 4 Format of SMOTD Timer Counter B (SMOTDTMSB)

Address: - After reset: 00H R/W disabled

Symbol	7	6	5	4	3	2	1	0
SMOTDTMSB	SMOTDTMSB[7:0]							

SMOTDTMSB[7:0]	SMOTD timer counter B
00H to FFH	Counting start condition: SMOTDTCE is set (when "0" is changed to "1"). Counting condition: Counter is incremented by the clock source selected with the SMOTDTCB bit when SMOTDTCE = 1. Counter clear condition: • The reset signal is generated. • SMOTDTCE is cleared (when "1" is changed to "0"). • SMOTDTMSB matches SMOTDCRSB

Caution If the counting condition and counter clear condition are generated simultaneously, the counter is cleared.

(4) SMOTD compare register A (SMOTDCRSA)

The SMOTDCRSA register is used to set the period of the PWM waveform of the sampling clock output from the SMOm pin.

The SMOTDCRSA register can be set by an 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 11 - 5 Format of SMOTD Compare Register A (SMOTDCRSA)

Address: F0270H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
SMOTDCRSA	SMOTDCRSA[7:0]							

SMOTDCRSA[7:0]	Setting of compare value for generating the sampling clock output period
00H (default)	Setting prohibited
01H • • • FFH	PWM waveform whose period is $(1/f_{SUB})^{Note}$ × (SMOTDCRSA + 1) is output from the SMOm pin (m = 0 to 2). Setting example: SMOTDCRSA = 01H $(1/f_{SUB})^{Note}$ × (1 + 1) = 52 µs@38.4 kHz SMOTDCRSA = 57H (in case of 2^3 division) $(2^3/f_{SUB})^{Note}$ × (87 + 1) = 18.33 ms@38.4 kHz

Note The clock of the timer counter A is set by the SMOTDTCA1 and SMOTDTCA0 bits.

Caution 1. Do not change the setting of the SMOTDCRSA register during counting (SMOTDTCE = 1).

Caution 2. Using this register (SMOTDTCE = 1) with the default (00H) is prohibited. Set any value other than 00H.

(5) SMOTD compare register B (SMOTDCRSB)

The SMOTDCRSB register is used to set the high pulse width of the PWM waveform of the sampling clock output from the SMOm pin.

The SMOTDCRSB register can be set by an 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 11 - 6 Format of SMOTD Compare Register B (SMOTDCRSB)

Address: F0271H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
SMOTDCRSB	SMOTDCRSB[7:0]							

SMOTDCRSB[7:0]	Setting of compare value for generating the sampling clock output high pulse width
00H (default) • • • FFH	PWM waveform whose high pulse width is (1/f_{SUB}) × (SMOTDCRSB + 1) is output from the SMOm pin (m = 0 to 2). Setting example: SMOTDCRSB = 00H (1/f_{SUB})Note × (0 + 1) = 26 μs@38.4 kHz SMOTDCRSB = 01H (1/f_{SUB})Note × (1 + 1) = 52 μs@38.4 kHz SMOTDCRSB = 99H (1/f_{SUB})Note × (153 + 1) = 4.01 ms@38.4 kHz

Note The clock of the timer counter B is set by the SMOTDTCB1 and SMOTDTCB0 bits.

Caution 1. Do not change the setting of the SMOTDCRSB register during counting (SMOTDTCE = 1).

Caution 2. Set this register to satisfy SMOTDCRSA > SMOTDCRSB.

(6) SMOTD clock select register (SMOTDTCS)

The SMOTDTCS register is used to select the count clock for the SMOTD timer counter A (SMOTDTMSA) and SMOTD timer counter B (SMOTDTMSB).

The SMOTDTCS register can be set by an 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 11 - 7 Format of SMOTD Clock Select Register (SMOTDTCS)

Address: F0272H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
SMOTDTCS	0	0	SMOTDTCB1	SMOTDTCB0	0	0	SMOTDTCA1	SMOTDTCA0

SMOTDTCB1 SMOTDTCB0	SMOTD timer counter B (SMOTDTMSB) clock select bits
00B (default)	f_{SUB} (30.5 μs/26 μs)
01B	$f_{SUB}/2^2$ (122 μs/104 μs)
10B	$f_{SUB}/2^4$ (488 μs/416.7 μs)
11B	$f_{SUB}/2^6$ (1.95 ms/1.67 ms)

SMOTDTCA1 SMOTDTCA0	SMOTD timer counter A (SMOTDTMSA) clock select bits
00B (default)	f_{SUB} (30.5 μs/26 μs)
01B	$f_{SUB}/2^3$ (244 μs/208 μs)
10B	$f_{SUB}/2^{10}$ (31.3 ms/26.7 ms)
11B	$f_{SUB}/2^{14}$ (500 ms/426.7 ms)

Caution 1. Set bits 7, 6, 3, and 2 to the default value.

Caution 2. Stop counting (SMOTDTCE = 0) before setting the register.

Remark The values in parentheses indicate the settings for f_{SUB} = 32.768 kHz or 38.4 kHz (f_{SUB}: subsystem clock frequency).

(7) SMOTD control register (SMOTDCR)

The SMOTDCR register is used to select the polarity of the sampling clock signal output from the SMOm pin and enable the counting operation of the sampling output timer.

The SMOTDCR can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 11 - 8 Format of SMOTD Control Register (SMOTDCR)

Address: F0273H After reset: 00H R/W

Symbol	7	6	5	<4>	3	2	1	<0>
SMOTDCR	0	0	0	SMOTDPOL	0	0	0	SMOTDTCE

SMOTDPOL	SMOm pin (m = 0 to 2) polarity select bit
0 (default)	Active-high (default: low level output)
1	Active-low (default: high level output)

Caution 1. The setting of this bit applies to all the sampling clock signals output from the SMO0 to SMO2 pins.

Caution 2. Set this bit while counting is stopped (SMOTDTCE = 0) and sampling output is disabled (SMOTDOE2 to SMOTDOE0 = 000B).

SMOTDTCE	Timer counting operation enable
0 (default)	Stops counting.
1	Enables counting.

Caution 1. Set the SMOTDTCE bit to 1 after setting the SMOTDCRSA, SMOTDCRSB, SMOTDTCS, SMOTDSMS, and SMOTDSMD registers and SMOTDPOL bit.

Caution 2. Following a change to the setting after setting the SMOTDTCE bit, wait for at least 3 cycles of the subsystem clock.

(8) SMOTD sampling level setting register (SMOTDSMS)

The SMOTDSMS register is used to set the conditions for generating the sampling detector detection interrupt (INTSMP0 to INTSMP5).

When the level of the sampling input to the SMP0 to SMP5 pins match the active level set with SMOTDSMS, the sampling detector detection interrupt (INTSMP0 to INTSMP5) can be generated.

The input to the SMP0 to SMP5 pins is sampled on the falling edge of the sampling clock signal.

The SMOTDSMS register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 11 - 9 Format of SMOTD Sampling Level Setting Register (SMOTDSMS)

Address: F0274H After reset: 00H R/W

Symbol	7	6	<5>	<4>	<3>	<2>	<1>	<0>
SMOTDSMS	0	0	SMOTDSMS5	SMOTDSMS4	SMOTDSMS3	SMOTDSMS2	SMOTDSMS1	SMOTDSMS0

SMOTDSMSn	Sampling signal active level setting bit (n = 0 to 5)
0 (default)	An interrupt request is generated when the low level on SMPn is detected on the falling edge of the sampling clock signal.
1	An interrupt request is generated when the high level on SMPn is detected on the falling edge of the sampling clock signal.

Caution 1. Do not change the setting of the SMOTDSMS register during counting (SMOTDTCE = 1).

Caution 2. Set bits 7 and 6 to the default value.

(9) SMOTD sampling pin status register (SMOTDSMD)

The SMOTDSMD register is used to detect the status of the SMP0 to SMP5 pins on the falling edge of the PWM output waveform output to the sampling clock pin (SMOm).

The SMOTDSMD register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 11 - 10 Format of SMOTD Sampling Pin Status Register (SMOTDSMD)

Address: F0275H After reset: 00H R

Symbol	7	6	<5>	<4>	<3>	<2>	<1>	<0>
SMOTDSMD	0	0	SMOTDSMD5	SMOTDSMD4	SMOTDSMD3	SMOTDSMD2	SMOTDSMD1	SMOTDSMD0

SMOTDSMDn	SMPn pin status (n = 0 to 5)
0 (default)	Low level
1	High level

Caution Read the SMOTDSMD register after the INTSMPn interrupt is generated (n = 0 to 5).

(10) SMOTD output control register (SMOTDOE)

The SMOTDOE register is used to disable or enable output of the sampling clock from the SMOm pin.

The SMOTDOE register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 11 - 11 Format of SMOTD Output Control Register (SMOTDOE)

Address: F0276H After reset: 00H R/W

Symbol	7	6	5	4	3	<2>	<1>	<0>
SMOTDOE	0	0	0	0	0	SMOTDOE2	SMOTDOE1	SMOTDOE0

SMOTDOEm	SMOm pin output control bit (m = 0 to 2)
0 (default)	Output disabled (port mode).
1	Output enabled (sampling mode).

Caution 1. Do not change the setting of the SMOTDOE register during counting (SMOTDTCE = 1).

Caution 2. Set bits 7 through 3 to the default value.

(11) Port mode registers 1, 2, 4, 8, 15 (PM1, PM2, PM4, PM8, PM15)

These registers specify input or output mode for the ports 1, 2, 4, 8, and 15 in 1-bit units.

To use the port pin (such as P85/SMP0/EXSDI0, P86/SMP1/EXSDI1) on which a sampling input pin function is multiplexed for sampling input, set the corresponding bit in the port mode register (PMxx) to 1. At this time, the bit in the port register (Pxx) may be 0 or 1.

Example: When P85/SMP0/EXSDI0 is to be used for sampling input:

Set the PM85 bit of port mode register 8 to 1.

Set the P85 bit of port register 8 to 0 or 1.

To use the port pin (such as P16/SMO0/SEG35, P17/SMO1) on which a sampling output pin function is multiplexed for sampling output, set the corresponding bits in the port mode register (PMxx) and port register (Pxx) to 0.

Example: When P16/SMO0/SEG35 is to be used for sampling output:

Set the PM16 bit of port mode register 1 to 0.

Set the P16 bit of port register 1 to 0.

Set the PFSEG35 bit of LCD port function register 4 to 0.

The PM1, PM2, PM4, PM8, and PM15 registers can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets these registers to FFH.

Figure 11 - 12 Format of Port Mode Registers (PM1, PM2, PM4, PM8, PM15)

Address: FFF21H After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
PM1	PM17	PM16	PM15	PM14	PM13	PM12	PM11	PM10

Address: FFF22H After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
PM2	PM27	PM26	PM25	PM24	PM23	PM22	PM21	PM20

Address: FFF24H After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
PM4	1	1	1	PM44	PM43	1	1	PM40

Address: FFF28H After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
PM8	1	PM86	PM85	PM84	PM83	PM82	PM81	PM80

Address: FFF2FH After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
PM15	1	1	1	1	1	1	PM151	PM150

PMmn	Selection of I/O mode for Pmn pin (m = 1, 2, 4, 8, 15; n = 0 to 7)
0	Output mode (output buffer on)
1	Input mode (output buffer off)

11.4 Operation of Sampling Output Timer Detector

Figure 11 - 13 shows the sampling clock output timing and **Figure 11 - 14** shows the sampling detection timing.

Figure 11 - 13 SMO0 to SMO2 Output Timing

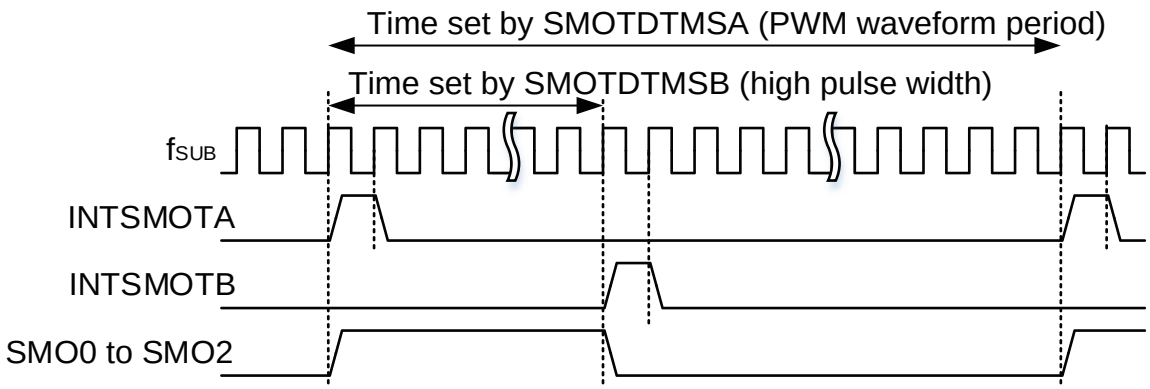
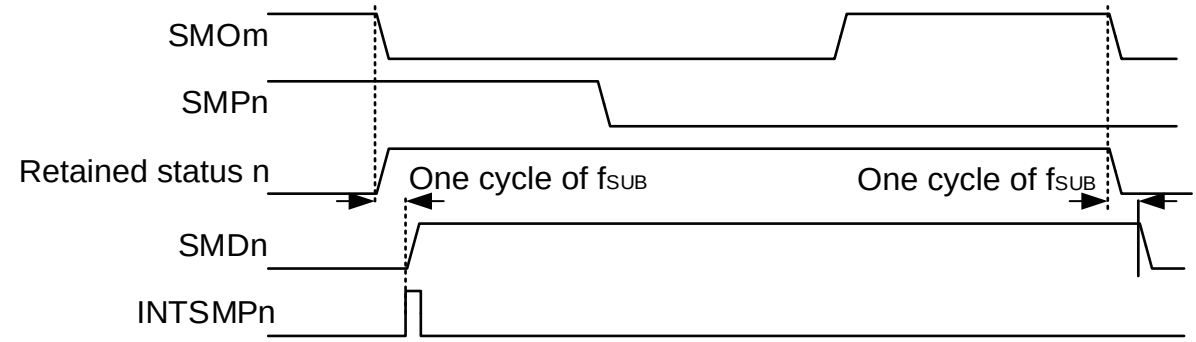
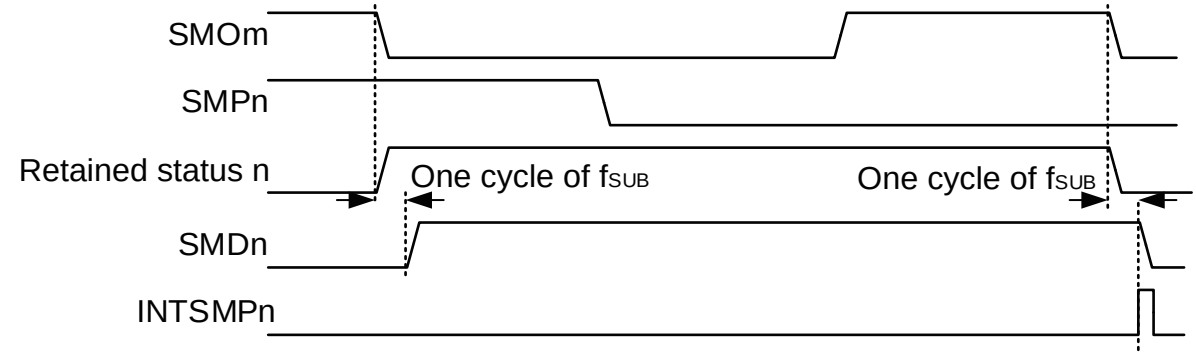


Figure 11 - 14 Sampling Detection Timing

<High level detection setting: SMOTDSMSn = 1 (n = 0 to 5)>



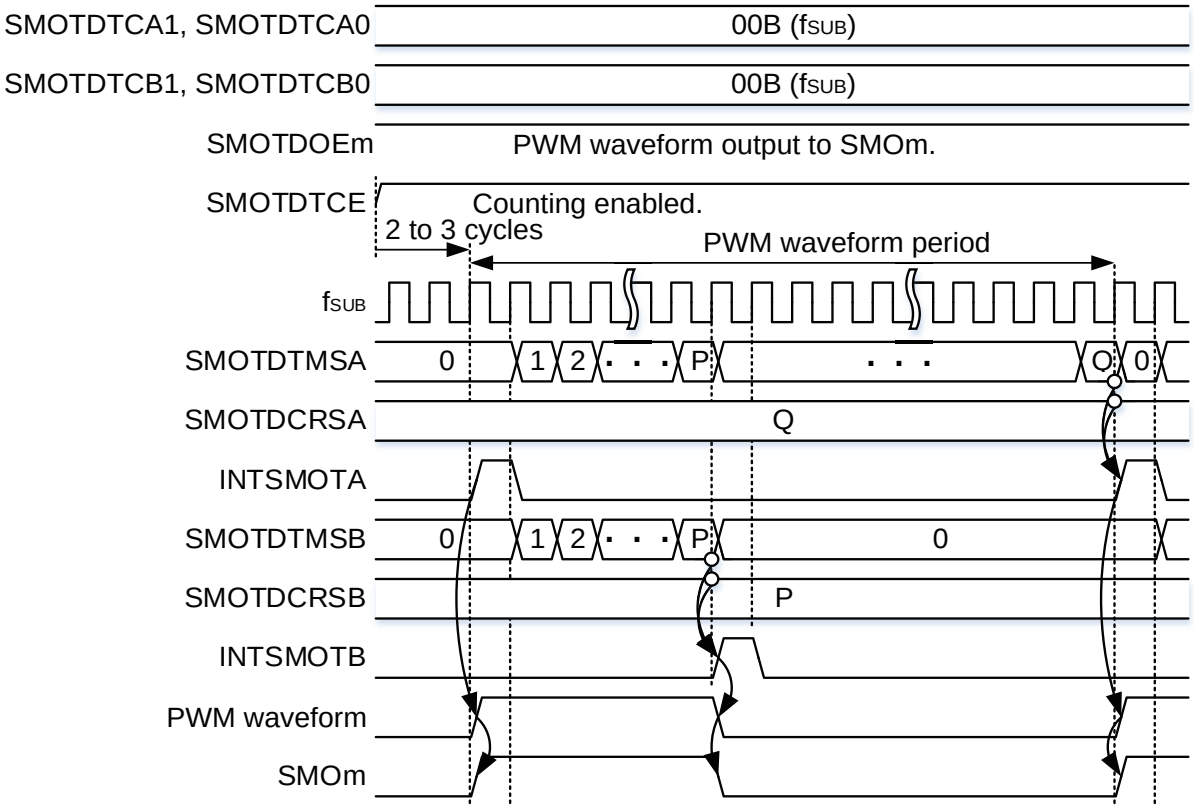
<Low level detection setting: SMOTDSMSn = 0 (n = 0 to 5)>



11.4.1 Sampling Clock Output Function

The sampling clock output function outputs the PWM waveform. The PWM waveform is generated by setting the period and high pulse width. The PWM waveform period is set by the SMOTDTCA1 and SMOTDTCA0 bits and SMOTDCRSA register. The high pulse width of the PWM waveform is set by the SMOTDTCB1 and SMOTDTCB0 bits and SMOTDCRSB register. The generated PWM waveform is output to the SMO0 to SMO2 pins according to the setting of the PWM waveform output (SMOTDOEm bit). On the falling edge of the PWM waveform, the sampling output timer compare match interrupt (INTSMOTB) is output. On the rising edge of the PWM waveform, the sampling output timer interval interrupt (INTSMOTA) is output. The polarity of the value to be output to SMO2 to SMO0 can be selected by the SMOTDPOL bit. **Figure 11 - 15** shows the timing of the sampling clock output (without division).

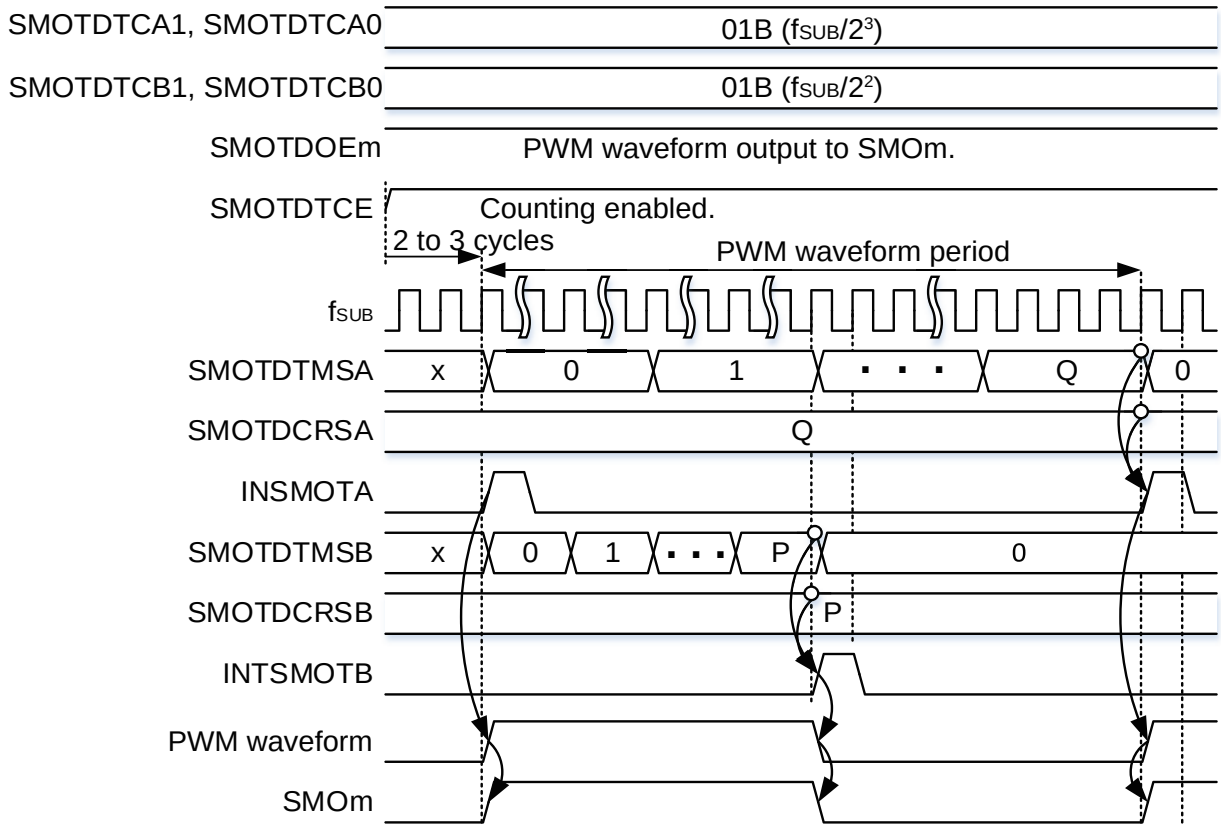
Figure 11 - 15 Sampling Clock Output (without division)



Remark The above figure applies to the case in which SMOTDPOL = 0 (active-high).

The sampling output timer detector has a function of dividing the PWM waveform. **Figure 11 - 16** shows the timing of the sampling clock output (with division).

Figure 11 - 16 Sampling Clock Output (with division)



Remark The above figure applies to the case in which SMOTDPOL = 0 (active-high).

Table 11 - 3 PWM Waveform of Sampling Clock Output (f_{SUB} = 38.4 kHz)

SMOTD TCA1	SMOTD TCA0	SMOTD TCB1	SMOTD TCB0	High Pulse Width		PWM Waveform Period	
0	0	0	0	(b + 1)(1/f_{SUB})	26.0 µs to 6.7 ms	(a + 1)(1/f_{SUB})	52.0 µs to 6.7 ms
0	1	0	0	(b + 1)(1/f_{SUB})	26.0 µs to 6.7 ms	(a + 1)(2^3/f_{SUB})	416.7 µs to 53.3 ms
		0	1	(b + 1)(2^2/f_{SUB})	104.2 µs to 26.7 ms		
1	0	0	0	(b + 1)(1/f_{SUB})	26.0 µs to 6.7 ms	(a + 1)(2^{10}/f_{SUB})	53.3 ms to 6.8 s
		0	1	(b + 1)(2^2/f_{SUB})	104.2 µs to 26.7 ms		
		1	0	(b + 1)(2^4/f_{SUB})	416.7 µs to 106.7 ms		
		1	1	(b + 1)(2^6/f_{SUB})	1.7 ms to 426.7 ms		
1	1	0	0	(b + 1)(1/f_{SUB})	26.0 µs to 6.7 ms	(a + 1)(2^{14}/f_{SUB})	853.3 ms to 109.2 s
		0	1	(b + 1)(2^2/f_{SUB})	104.2 µs to 26.7 ms		
		1	0	(b + 1)(2^4/f_{SUB})	416.7 µs to 106.7 ms		
		1	1	(b + 1)(2^6/f_{SUB})	1.7 ms to 426.7 ms		

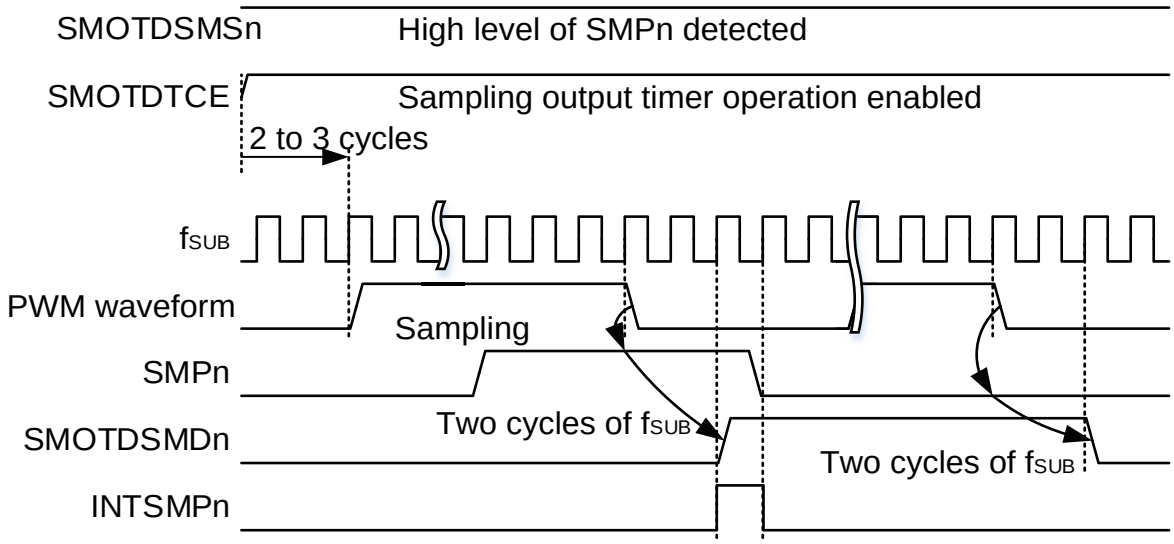
Caution 1. "a" represents the SMOTDCRSA[7:0] value, and "b" represents the SMOTDCRSB[7:0] value.

Caution 2. Combinations of SMOTDTCA1, SMOTDTCA0, SMOTDTCB1, and SMOTDTCB0 settings not shown in Table 11 - 3 are prohibited. Set the bits to satisfy PWM period > high pulse width.

11.4.2 Sampling Detector Function

The sampling detector function stores the sampling signal (SMPn) in the SMOTDSMDn bit on the falling edge of the PWM waveform provided by the sampling clock output function. Here, a delay of two cycles of f_{SUB} is produced relative to the falling edge of the PWM waveform. If the sampling signal (SMPn) matches the condition set with the SMOTDSMSn bit, the sampling detector detection interrupt (INTSMPn) is output simultaneously with the storage of the sampling signal in the SMOTDSMDn bit.

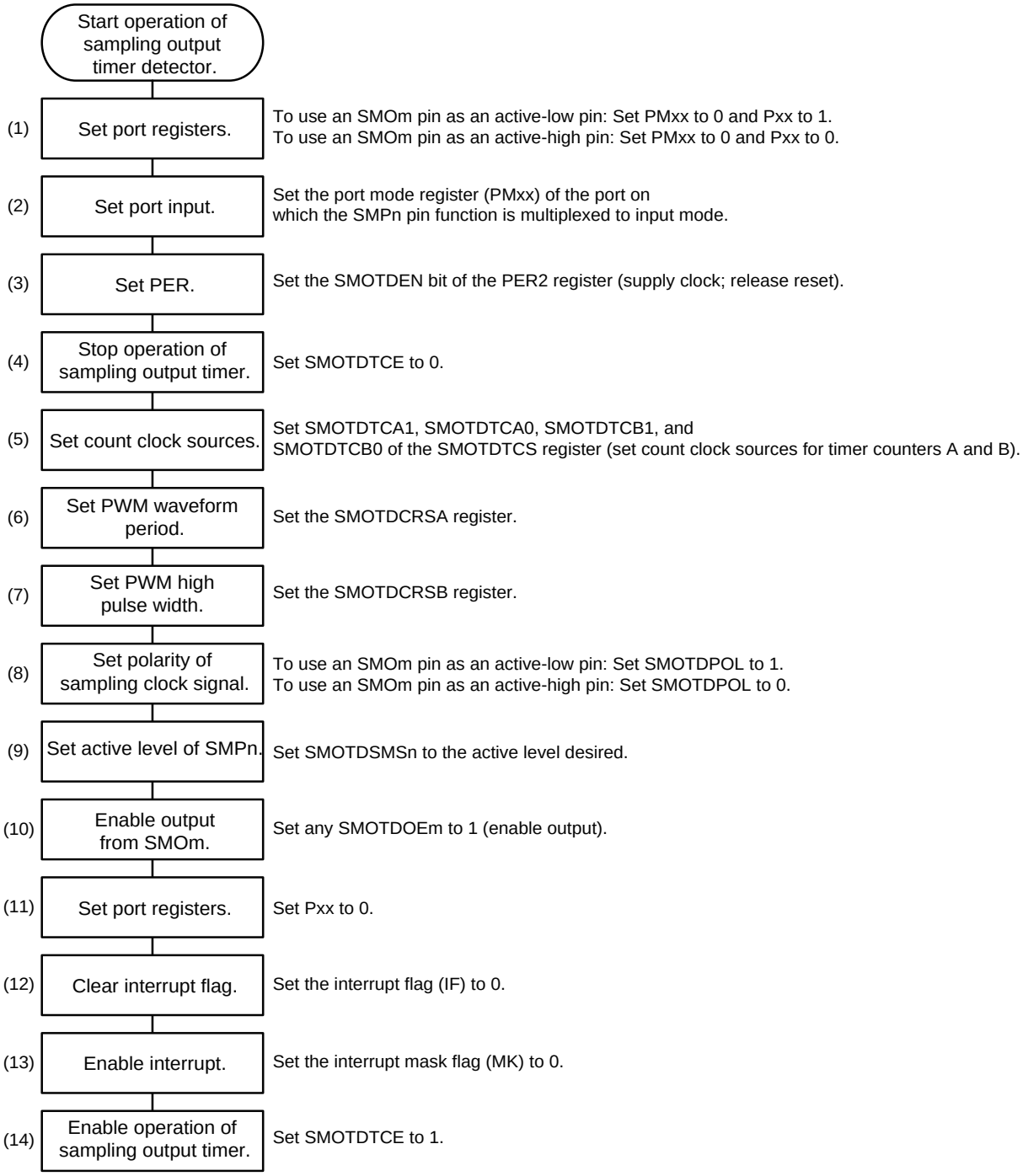
Figure 11 - 17 Sampling Clock Output Function



11.4.3 Setting the Operation of the Sampling Output Timer Detector

Figure 11 - 18 shows the procedure for starting the operation of the sampling output timer detector.

Figure 11 - 18 Procedure for Starting Operation



Caution For setting the Pxx and PMxx registers, refer to (11) in 11.3 Registers Controlling the Sampling Output Timer Detector.

Figure 11 - 19 and **Figure 11 - 20** show the timing of starting the operation when an SMOm pin is used as an active-low pin and an active-high pin, respectively.

Figure 11 - 19 Timing of Stating Operation When SMOm Pin is Active High (when SMOTDPOL = 0)

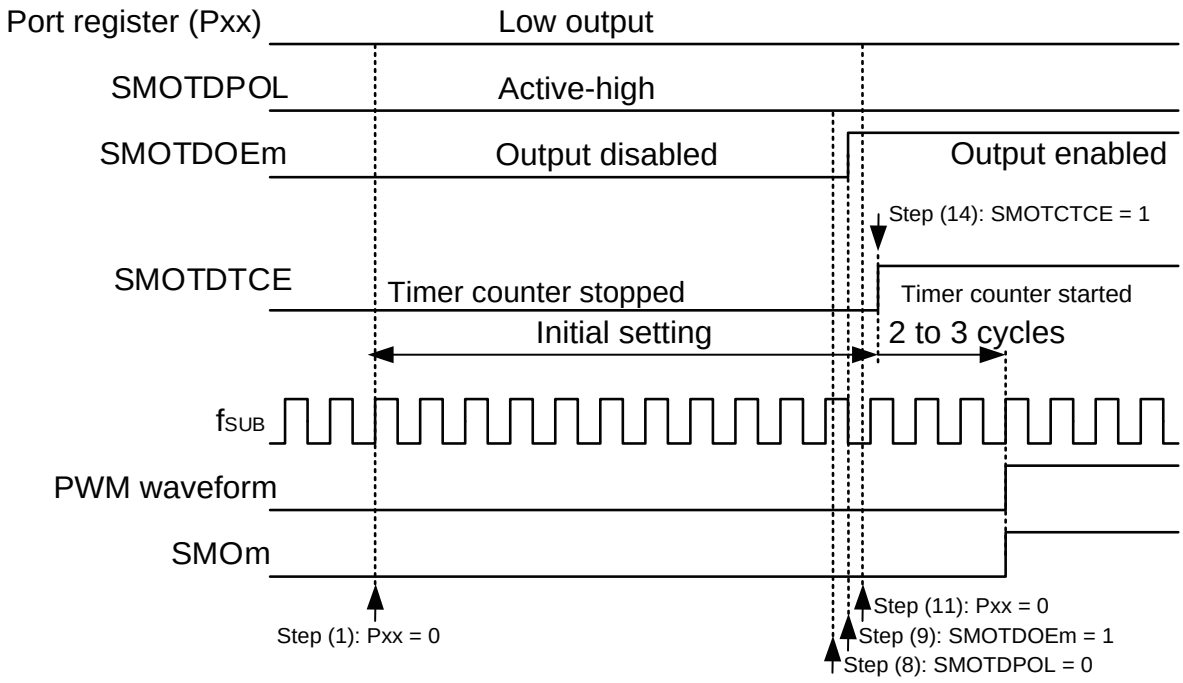


Figure 11 - 20 Timing of Stating Operation When SMOm Pin is Active Low (when SMOTDPOL = 1)

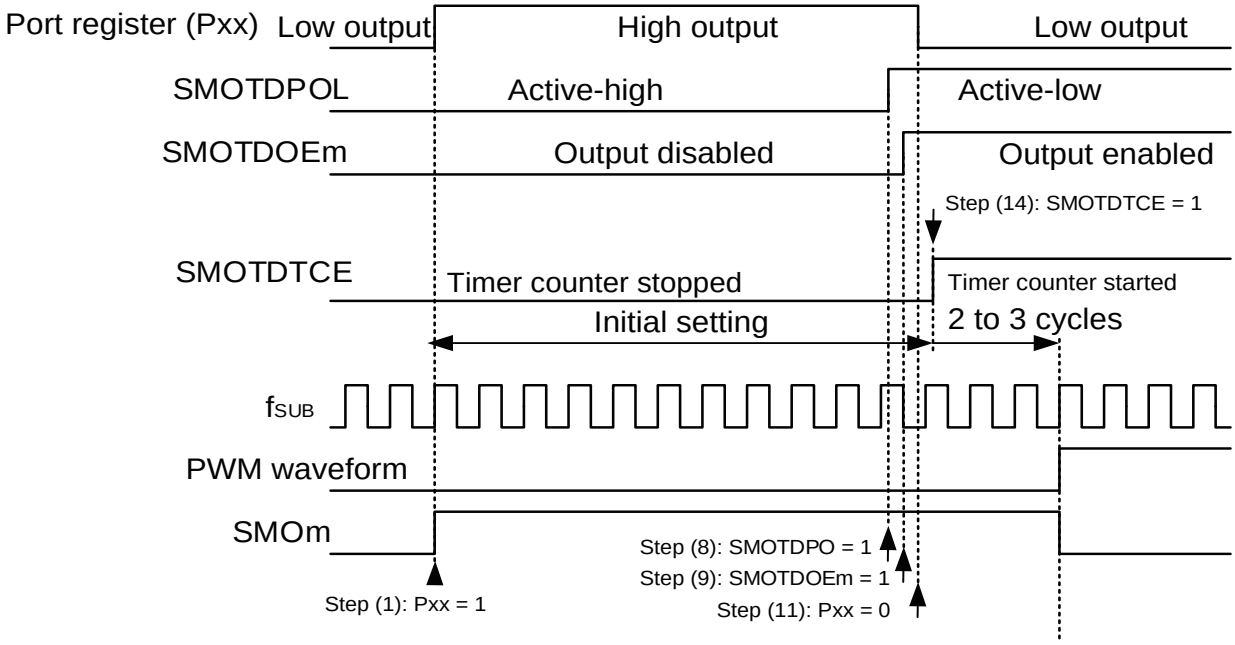
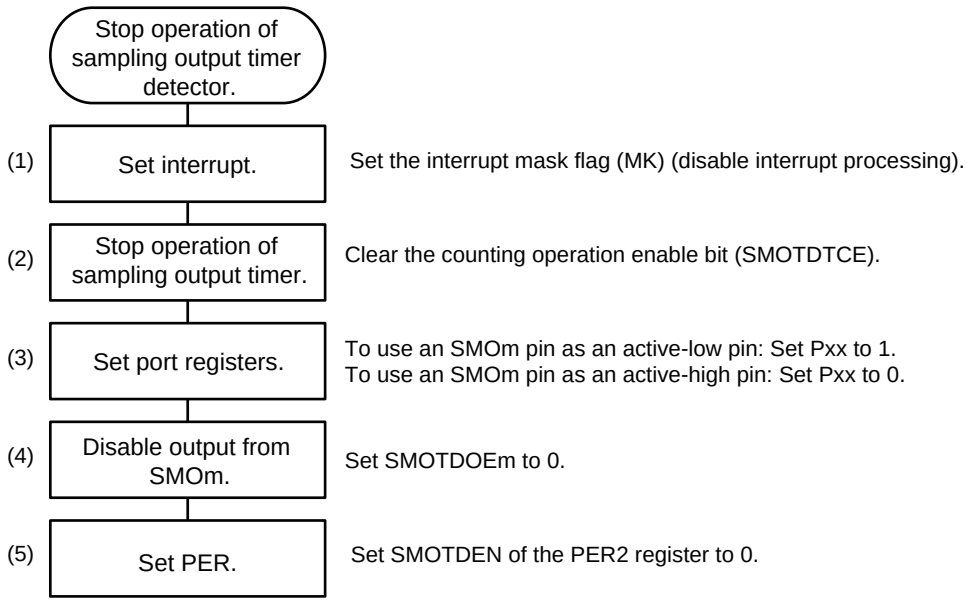


Figure 11 - 21 shows the procedure for stopping the operation of the sampling output timer detector.

Figure 11 - 21 Procedure for Stopping Operation



The sampling output timer stops three cycles of the subsystem clock after the setting to stop it is made. The interrupt may thus be generated before it stops completely. Executing step (5) of the procedure for stopping operation, it stops immediately. **Figure 11 - 22** shows the timing of stopping the operation when an SMOm pin is used as an active-high pin and **Figure 11 - 23** shows the timing of stopping the operation when an SMOm pin is used as an active-low pin.

Figure 11 - 22 Timing of Stopping Operation When SMOm Pin is Active High (when SMOTDPOL = 0)

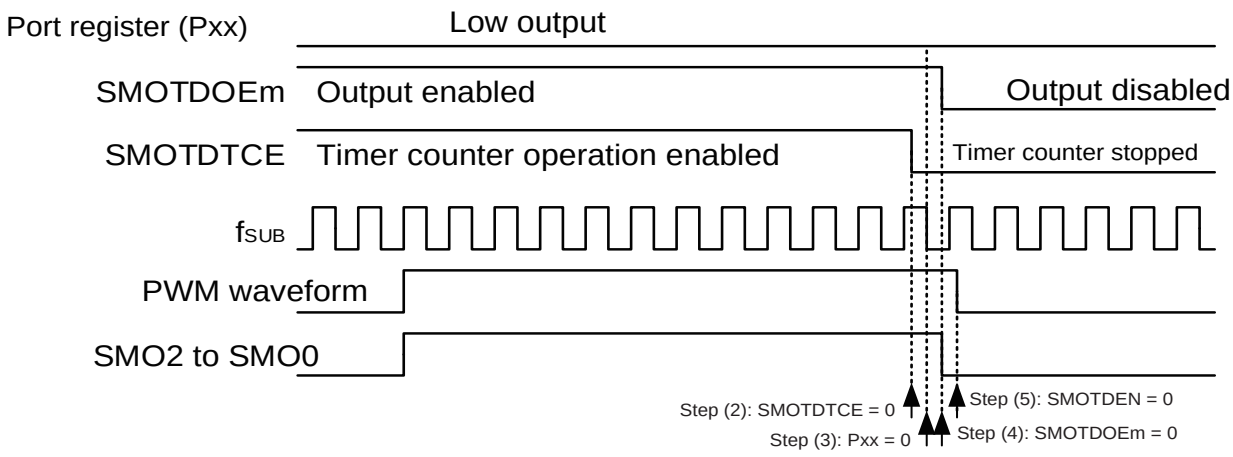
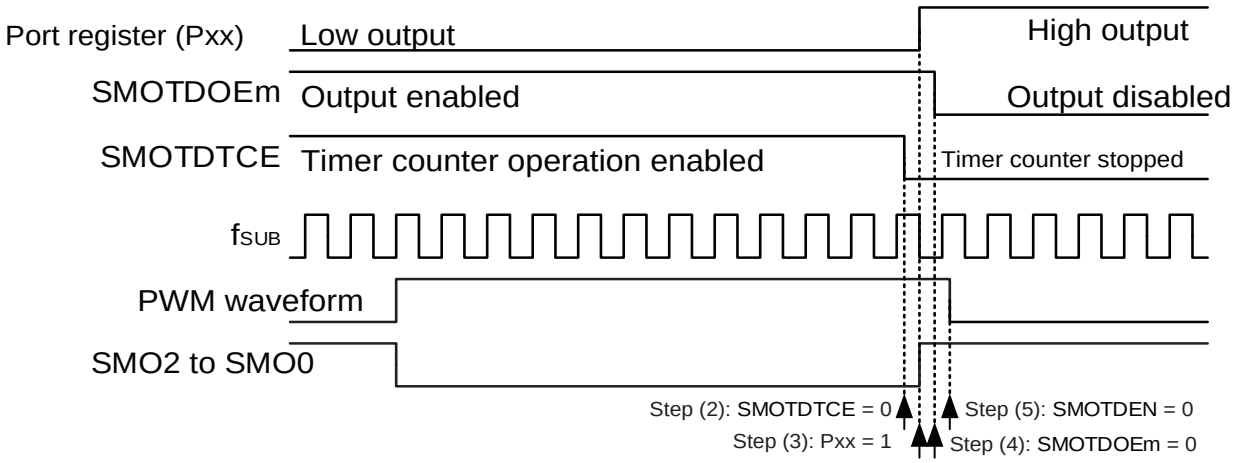


Figure 11 - 23 Timing of Stopping Operation When SMOm Pin is Active High (when SMOTDPOL = 1)



CHAPTER 12 EXTERNAL SIGNAL SAMPLER (R5F11R only)

12.1 Functions of External Signal Sampler

The external signal sampler has the following features.

- Generates a sampling clock based on the 8-bit interval timer 00 interrupt signal (INTIT00) generation timing and outputs the clock from the EXSDO0 and EXSDO1 pins.
- Latches the levels of input signals to the EXSDI0 and EXSDI1 pins on the falling edge of the generated sampling clock and shapes the input waveforms. In addition, detects the phase of shaped waveforms .
- Generates the interrupt signal (INTEXSD) on the falling and rising edges of the shaped waveforms derived from the input signal to the EXSDI1 pin.

12.2 Configuration of External Signal Sampler

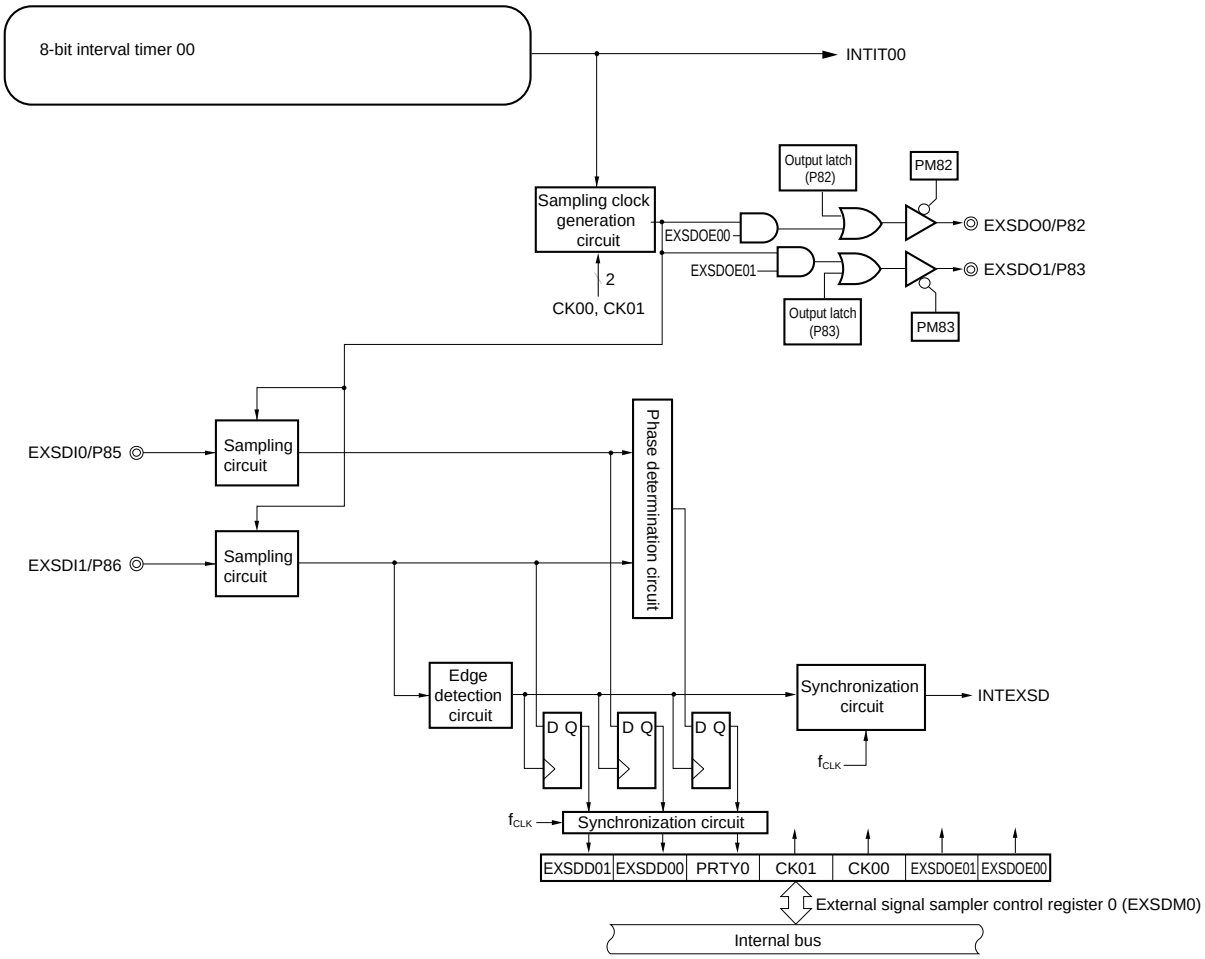
The external signal sampler includes the following hardware.

Table 12 - 1 Configuration of External Signal Sampler

Item	Configuration
Control registers	Peripheral enable register 2 (PER2) External signal sampler control register 0 (EXSDM0) Port mode register 8 (PM8) Port register 8 (P8)

Figure 12 - 1 shows a block diagram of the external signal sampler.

Figure 12 - 1 Block Diagram of External Signal Sampler



Remark f_{CLK}: CPU/peripheral hardware clock

12.3 Registers Controlling External Signal Sampler

The external signal sampler is controlled by the following registers.

- Peripheral enable register 2 (PER2)
- External signal sampler control register 0 (EXSDM0)
- Port mode register 8 (PM8)
- Port register 8 (P8)

(1) Peripheral enable register 2 (PER2)

The PER2 register is used to enable or disable supplying the clock to the peripheral hardware. Clock supply to the hardware that is not used is also stopped so as to decrease the power consumption and noise.

When using the external signal sampler, be sure to set bit 2 (EXSDEN) to 1.

The PER2 register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 12 - 2 Format of Peripheral Enable Register 2 (PER2)

Address: F00FDH After reset: 00H R/W

Symbol	7	6	5	<4>	<3>	<2>	<1>	<0>
PER2	0	0	0	UARTMG0EN	SMOTDEN	EXSDEN	TRJ1EN	TRJ0EN

EXSDEN	Control of external signal sampler input clock supply
0	Stops input clock supply. • SFRs used by the external signal sampler cannot be written. • The external signal sampler is in the reset status.
1	Enables input clock supply. • SFRs used by the external signal sampler can be read and written.

Caution 1. When setting the external signal sampler, be sure to set EXSDEN to 1 first. If EXSDEN = 0, writing to a control register of the external signal sampler is ignored, and all read values are default values (except for the port mode register 8 (PM8) and port register 8 (PM8)).

Caution 2. Be sure to clear bits 7 through 5 to 0.

(2) External signal sampler control register 0 (EXSDM0)

The EXSDM0 register is used to indicate the sampling status and control the operation of the EXSDO0, EXSDO1, EXSDI0, and EXSDI1 pins.

The EXSDM0 register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 12 - 3 Format of External Signal Sampler Control Register 0 (EXSDM0)

Address: F026BH After reset: 00H R/W[Note]

Symbol	<7>	<6>	<5>	4	3	2	<1>	<0>
EXSDM0	EXSDD01	EXSDD00	PRTY0	0	CK01	CK00	EXSDOE01	EXSDOE00

EXSDD01	Status flag of the internally-shaped waveform level derived from the input signal to EXSDI1
0	Low level
1	High level

EXSDD00	Status flag of the internally-shaped waveform level derived from the input signal to EXSDI0 on the rising edge of the internally-shaped waveform derived from the input signal to EXSDI1
0	Internally-shaped waveform derived from the input signal to EXSDI0 pin is low.
1	Internally-shaped waveform derived from the input signal to EXSDI0 pin is high.

PRTY0	Status flag of the internally-shaped waveform derived from the input signal to EXSDI0 on the rising or falling edge of the internally-shaped waveform derived from the input signal to EXSDI1
0	Internally-shaped waveform derived from the input signal to EXSDI0 is high on the rising edge of internally-shaped waveform derived from the input signal to EXSDI1, or low on the falling edge of internally-shaped waveform derived from input signal to EXSDI1.
1	Internally-shaped waveform derived from the input signal to EXSDI0 is low on the rising edge of the internally-shaped waveform derived from the input signal to EXSDI1, or high on the falling edge of the internally-shaped waveform derived from the input signal to EXSDI1.

CK01	CK00	Setting of pulse width of clock signal output from EXSDO1 and EXSDO0 pins
0	0	$1/2f_{SUB}$ (15 μs)
0	1	$1/f_{SUB}$ (30.5 μs)
1	0	$2/f_{SUB}$ (61 μs)
1	1	$2^5/f_{SUB}$ (977 μs)

EXSDOE01	EXSDO1 pin output control flag
0	Disables output.
1	Enables output.

EXSDOE00	EXSDO0 pin output control flag
0	Disables output.
1	Enables output.

Note Bits 5 to 7 are read-only bits.

Remark The values in parentheses indicate the settings for f_{SUB} = 32.768 kHz.

(3) Port mode register 8 (PM8)

This register specifies input or output mode for the port 8 in 1-bit units.

When using the P82/EXSDO0 and P83/EXSDO1 pins for clock output from the external signal sampler, set PM82 and PM83 to 0 and output latches of P82 and P83 to 0.

When using the P85/EXSDI0 and P86/EXSDI1 pins for phase detection input of the external signal sampler, set PM85 and PM86 to 1. At this time, output latches of P85 and P86 may be 0 or 1.

The PM8 register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets this register to FFH.

Figure 12 - 4 Format of Port Mode Register 8 (PM8)

Address: FFF28H After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
PM8	1	PM86	PM85	PM84	PM83	PM82	PM81	PM80

PM8n	PM8n pin I/O mode selection (n = 0 to 6)
0	Output mode (output buffer on)
1	Input mode (output buffer off)

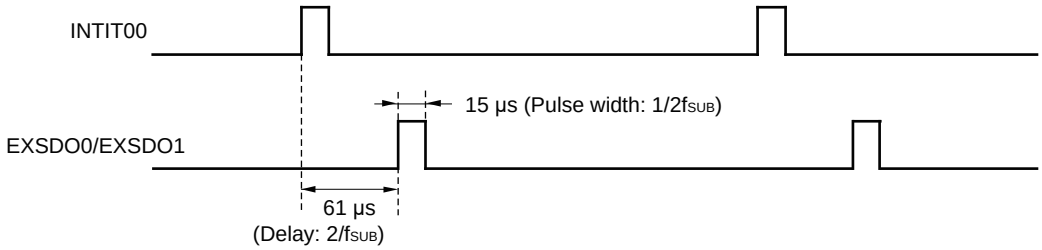
12.4 Sampling Clock Output Operation

The output period of the output signal from EXSDO0 and EXSDO1 pins is set by the 8-bit interval timer 00 interrupt signal (INTIT00) generation period. The pulse width is set by bits 2 and 3 (CK00 and CK01) of the external signal sampler control register 0 (EXSDM0).

Figure 12 - 5 shows an example of the waveform of the output signal from EXSDO0 and EXSDO1.

Figure 12 - 5 Example of Waveforms of Output Signal from EXSDO0 and EXSDO1 Pins

● When CK01, CK00 = 00B



Caution 1. Set the TRTCMP00 register so that the INTIT00 signal generation interval is at least 4/fSUB. If fSUB is selected for 8-bit interval timer 00, set TRTCMP00 ≥ 0002H. If fSUB/2 is selected, set TRTCMP00 ≥ 0001H. In the other cases, set TRTCMP00 ≥ 0000H.

Caution 2. Set the pulse width of the output signal from the EXSDO0 and EXSDO1 pins so that the duty cycle is no greater than 1/2.

Caution 3. When using the external signal sampler, set the WUTMMCK0 bit of the subsystem clock supply mode control register (OSMC) to 0 to select the subsystem clock as the operation clock.

Remark fSUB = 32.768 kHz

12.5 Operation of External Signal Sampler

(1) Initial setting

The initial setting of the external signal sampler is made in the following procedure.

- Set bits 2 and 3 (PM82, PM83) of the port mode register 8 (PM8) to output mode and set output latches of bits P82 and P83 to 0. Set bits 5 and 6 (PM85 and PM86) of the port mode register 8 (PM8) to input mode.
- Set the interrupt mask flag (EXSDMK) for the external signal sampler edge detection interrupt (INTEXSD) to 0 (to enable interrupt processing).
- Stop the counting operation of 8-bit interval timer 00.
- Set an arbitrary count value to 8-bit interval timer 00.
- Set bit 2 (EXSDEN) of the peripheral enable register 2 (PER2) to 1.
- Set the pulse width of the sampling clock output from the EXSDO0 and EXSDO1 pins by bits 2 and 3 (CK00 and CK01) of the external signal sampler control register 0 (EXSDM0).

(2) Starting external signal sampler

The external signal sampler starts in the following procedure.

- Enable output from EXSDO0 and EXSDO1 pins by bits 0 and 1 (EXSDOE00 and EXSDOE01) of the EXSDM0 register.
- Start the counting operation of channel 0 of 8-bit interval time 00.
- The levels of input signals to the EXSDI0 and EXSDI1 pins are latched on falling edges of the sampling clock signals from the EXSDO0 and EXSDO1 pins and the waveforms of the input signal are shaped in response.
- The interrupt signal (INTEXSD) is generated on the rising and falling edges of the internally shaped waveform derived from the input signal to EXSDI1 pin. The generation of INTEXSD is delayed by $1/(2 \times f_{SUB}) + 1/f_{CLK}$ or $1/(2 \times f_{SUB}) + 2/f_{CLK}$ relative to the shaped waveform derived from the input signal to EXSDI1.
- The level of the shaped waveform derived from the input signal to EXSDI1 pin is latched at the INTEXSD generation timing and the level is sent to bit 7 (EXSDD01) of the EXSDM0 register. When the level being input to EXSDI1 pin is high, the bit is set to 1, and when the level is low, the bit is cleared to 0.
- The level of the shaped waveform derived from the input signal to EXSDI0 pin is latched on the falling and rising edges of the internally-shaped waveform derived from the input signal to EXSDI1 pin and the level is sent to bit 6 (EXSDD00) of the EXSDM0 register at the INTEXSD generation timing. When the level being input to EXSDI0 pin is high, the bit is set to 1, and when the level is low, the bit is cleared to 0.
- Bit 5 (PRTY0) of the EXSDM0 register is cleared to 0 when the level of the shaped waveform derived from the input signal to EXSDI0 pin is high on the rising edge of the shaped waveform derived from the input signal to EXSDI1 pin or when the level being input to EXSDI0 pin is low on the falling edge of the input signal to EXSDI1 pin. The PRTY0 flag is set to 1 when the level of the shaped waveform derived from the input signal to EXSDI0 pin is low on the rising edge of the shaped waveform derived from the input signal to EXSDI1 pin or when the level being input to EXSDI0 pin is high on the falling edge of the input signal to EXSDI1 pin.

(3) Stopping external signal sampler

The external signal sampler stops in the following procedure.

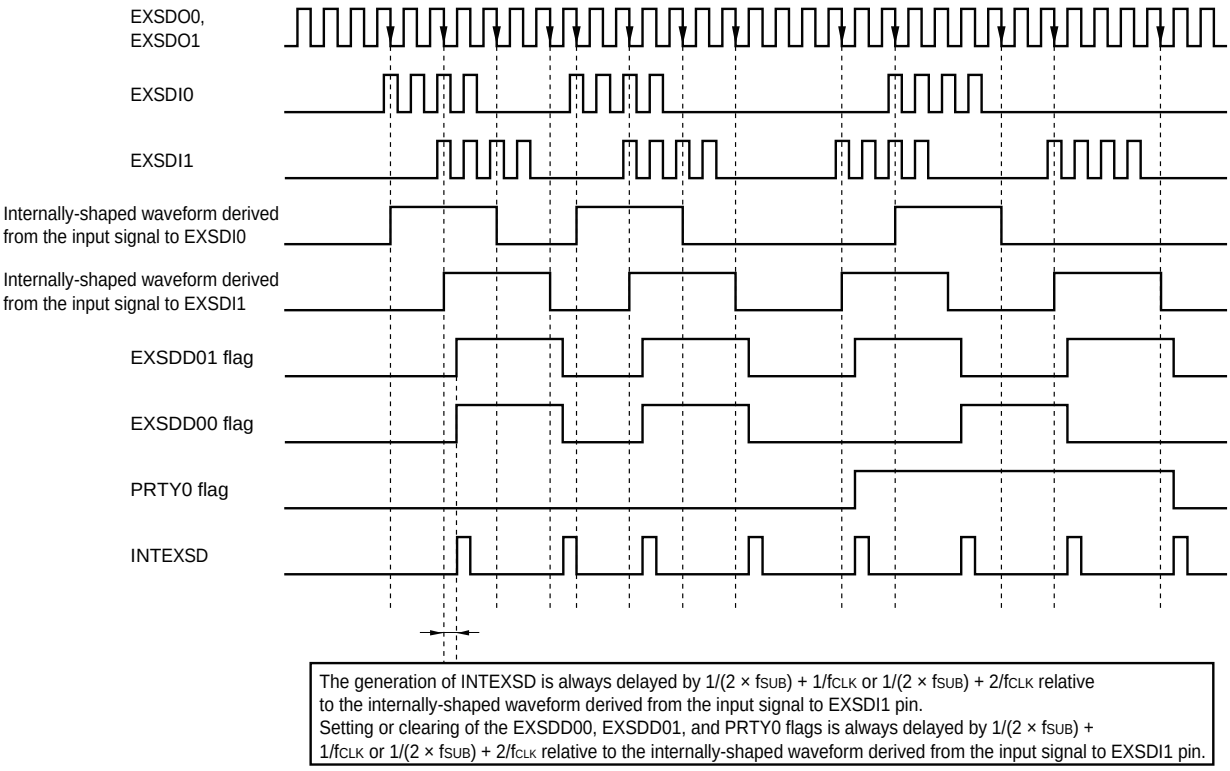
- Set the interrupt mask flag (EXSDMK) for the external signal sampler edge detection interrupt (INTEXSD) to 1 (to disable interrupt processing).
- Stop the counting operation of 8-bit interval time 00.
- Disable output from the EXSDO0 and EXSDO1 pins by bits 0 and 1 (EXSDOE00 and EXSDOE01) of the EXSDM0 register.

Caution 1. The generation of INTEXSD is always delayed by 1/(2 × f_{SUB}) + 1/f_{CLK} or 1/(2 × f_{SUB}) + 2/f_{CLK} relative to the internally-shaped waveform derived from the input signal to EXSDI1 pin.

Caution 2. Setting or clearing of the EXSDD00, EXSDD01, and PRTY0 flags is always delayed by 1/(2 × f_{SUB}) + 1/f_{CLK} or 1/(2 × f_{SUB}) + 2/f_{CLK} relative to the internally-shaped waveform derived from the input signal to EXSDI1 pin.

Figure 12 - 6 shows a timing of the operation of the external signal sampler.

Figure 12 - 6 Example of Operation of External Signal Sampler



12.6 Cautions

(1) If edges of input signals to EXSDI0 and EXSDI1 pins occur simultaneously, the value of the level status flag for the internally-shaped waveform derived from the input signal to EXSDI0 pin is undefined.

(2) The interrupt signal (INTEXSD) and status flags (EXSDD00, EXSDD01, and PRTY0) change simultaneously.

(3) Set the EXSDM0 register while 8-bit interval timer 00 is stopped.

(4) Set the TRTCMP00 register so that the 8-bit interval timer 00 interrupt signal (INTIT00) generation interval is at least 4/f_{SUB}. If f_{SUB} is selected for 8-bit interval timer 00, set TRTCMP00 ≥ 0002H. If f_{SUB}/2 is selected, set TRTCMP00 ≥ 0001H. In the other cases, set TRTCMP00 ≥ 0000H.

(5) Set the pulse width of the EXSDO0 and EXSDO1 pins so that the duty cycle is no greater than 1/2.

(6) The following functions cannot be used in STOP mode, because supply of the CPU/peripheral hardware clock (f_{CLK}) is stopped.

- Generation of the external signal sampler edge detection interrupt signal (INTEXSD)
- Updating of the EXSDD01, EXSDD00, and PRTY0 bits in external signal sampler control register 0 (EXSDM0)

CHAPTER 13 CLOCK OUTPUT/BUZZER OUTPUT CONTROLLER

The number of pins of the clock output/buzzer output depends on the product.

Clock output/buzzer output pins	R5F11NM	R5F11NL	R5F11PL, R5F11NG	R5F11RM
PCLBUZ0	√	—	√	√
PCLBUZ1	√	√	√	√

Caution Most of the following descriptions in this chapter use the configuration of R5F11NM as an example.

13.1 Functions of Clock Output/Buzzer Output Controller

The clock output controller is intended for clock output for supply to peripheral ICs.

Buzzer output is a function to output a square wave of buzzer frequency.

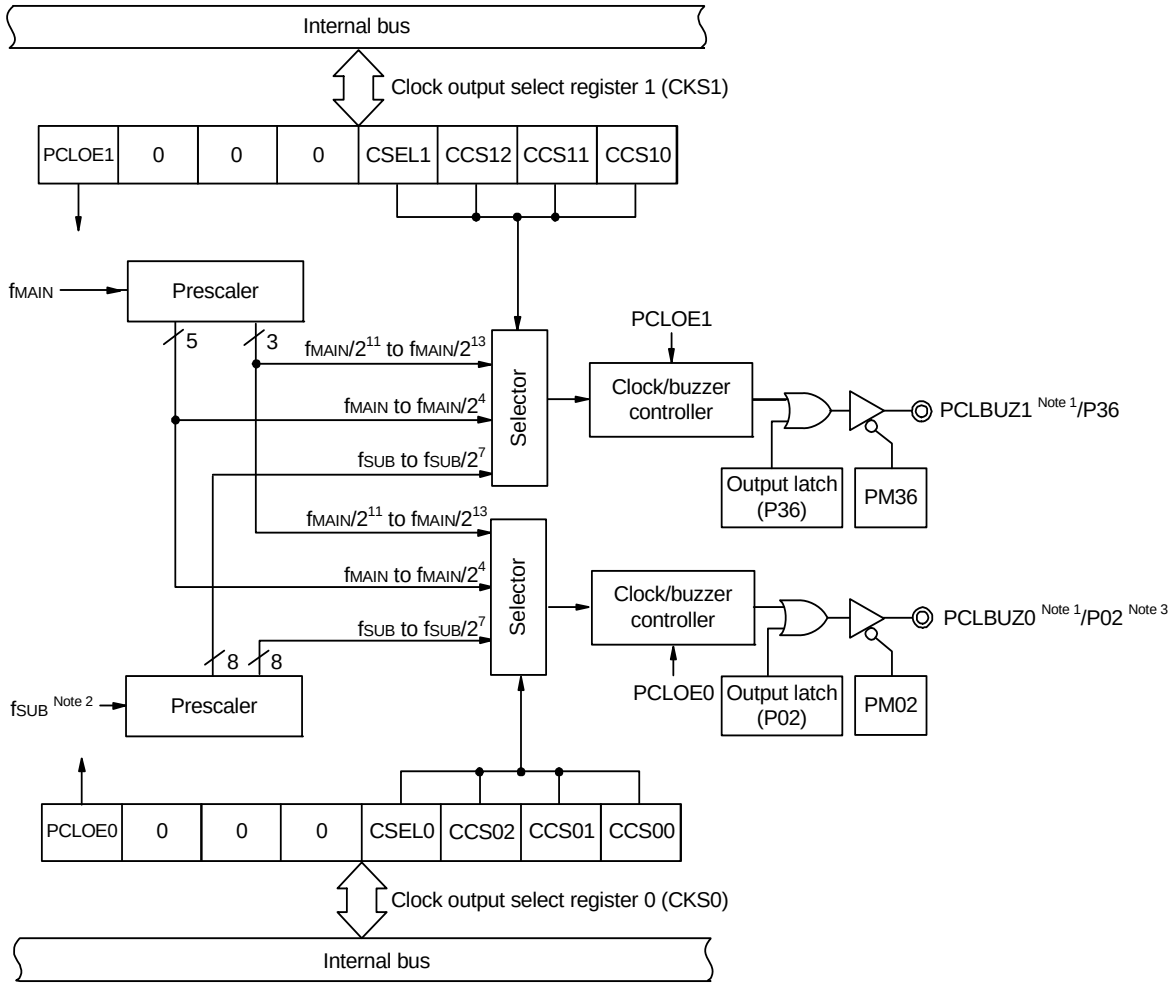
One pin can be used to output a clock or buzzer sound.

The PCLBUZn pin outputs a clock selected by clock output select register n (CKSn).

Figure 13 - 1 shows the Block Diagram of Clock Output/Buzzer Output Controller.

Remark n = 0, 1

Figure 13 - 1 Block Diagram of Clock Output/Buzzer Output Controller



Note 1. For output frequencies available from PCLBUZ0 and PCLBUZ1, refer to **38.4** or **39.4 AC Characteristics**.

Note 2. Selecting f_{SUB} as the output clock of the clock output/buzzer output controller is prohibited when the WUTMMCK0 bit of the OSMC register is set to 1.

Note 3. R5F11NM, R5F11PL, R5F11NG, and R5F11RM only

Remark The clock output/buzzer output pins in above diagram are those when PIOR03 is 0.

13.2 Configuration of Clock Output/Buzzer Output Controller

The clock output/buzzer output controller includes the following hardware.

Table 13 - 1 Configuration of Clock Output/Buzzer Output Controller

Item	Configuration
Control registers	Clock output select registers n (CKSn) Port mode registers 0, 3, 8 (PM0, PM3, PM8) Port registers 0, 3, 8 (P0, P3, P8)

13.3 Registers Controlling Clock Output/Buzzer Output Controller

The following register is used to control the clock output/buzzer output controller.

- Clock output select registers n (CKSn)
- Port mode registers 0, 3, 8 (PM0, PM3, PM8)
- Port registers 0, 3, 8 (P0, P3, P8)

13.3.1 Clock output select registers n (CKSn)

These registers set output enable/disable for clock output or for the buzzer frequency output pin (PCLBUZn), and set the output clock.

Select the clock to be output from the PCLBUZn pin by using the CKSn register.

The CKSn register are set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears these registers to 00H.

Figure 13 - 2 Format of Clock output select registers n (CKSn)

Address: FFFA5H (CKS0), FFFA6H (CKS1) After reset: 00H R/W

Symbol	<7>	6	5	4	3	2	1	0
CKSn	PCLOEn	0	0	0	CSELn	CCSn2	CCSn1	CCSn0

PCLOEn	PCLBUZn pin output enable/disable specification
0	Output disable (default)
1	Output enable

CSELn	CCSn2	CCSn1	CCSn0	PCLBUZn pin output clock selection				
					f_{MAIN} = 5 MHz	f_{MAIN} = 10 MHz	f_{MAIN} = 20 MHz	f_{MAIN} = 24 MHz
0	0	0	0	f_{MAIN}	5 MHz	10 MHz	Setting prohibited Note 1	Setting prohibited Note 1
0	0	0	1	$f_{MAIN}/2$	2.5 MHz	5 MHz	10 MHz	12 MHz
0	0	1	0	$f_{MAIN}/2^2$	1.25 MHz	2.5 MHz	5 MHz	6 MHz
0	0	1	1	$f_{MAIN}/2^3$	625 kHz	1.25 MHz	2.5 MHz	3 MHz
0	1	0	0	$f_{MAIN}/2^4$	312.5 kHz	625 kHz	1.25 MHz	1.5 MHz
0	1	0	1	$f_{MAIN}/2^{11}$	2.44 kHz	4.88 kHz	9.77 kHz	11.7 kHz
0	1	1	0	$f_{MAIN}/2^{12}$	1.22 kHz	2.44 kHz	4.88 kHz	5.86 kHz
0	1	1	1	$f_{MAIN}/2^{13}$	610 Hz	1.22 kHz	2.44 kHz	2.93 kHz
1	0	0	0	f_{SUB} Note 2	32.768 kHz/38.4 kHz Note 3			
1	0	0	1	$f_{SUB}/2$ Note 2	16.384 kHz/19.2 kHz Note 3			
1	0	1	0	$f_{SUB}/2^2$ Note 2	8.192 kHz/9.6 kHz Note 3			
1	0	1	1	$f_{SUB}/2^3$ Note 2	4.096 kHz/4.8 kHz Note 3			
1	1	0	0	$f_{SUB}/2^4$ Note 2	2.048 kHz/2.4 kHz Note 3			
1	1	0	1	$f_{SUB}/2^5$ Note 2	1.024 kHz/1.2 kHz Note 3			
1	1	1	0	$f_{SUB}/2^6$ Note 2	512 Hz/600 Hz Note 3			
1	1	1	1	$f_{SUB}/2^7$ Note 2	256 Hz/300 Hz Note 3			

Note 1. Use the output clock within a range of 12 MHz. See **38.4** or **39.4 AC Characteristics**for details.

Note 2. Selecting f_{SUB} as the output clock of the clock output/buzzer output controller is prohibited when the WUTMMCK0 bit of the OSMC register is set to 1.

Note 3. Only the R5F11RM supports f_{SUB} = 38.4 kHz.

Caution 1. Change the output clock after disabling clock output (PCLOEn = 0).

Caution 2. To shift to STOP mode when the main system clock is selected (CSELn = 0), set PCLOEn = 0 before executing the STOP instruction.

Caution 3. Setting the CKS0 register in R5F11NL is prohibited.

Remark 1. n = 0, 1

Remark 2. f_{MAIN}: Main system clock frequency
f_{SUB}: Subsystem clock frequency

13.3.2 Registers that control port functions of clock output/buzzer output pins

Using the clock output/buzzer output requires setting of the registers that control the port functions for the port pins with which the clock output/buzzer output pin functions for the target channel are multiplexed (port mode register (PMxx), port register (Pxx)). For details, see **4.4.1 Port mode registers (PMxx)** and **4.4.2 Port registers (Pxx)**.

Using a port pin which is multiplexed with a clock output/buzzer output pin function (e.g. P02/(SO10/TxD1)/PCLBUZ0/SEG23, P36/SI00/RxD0/TOOLRxD/SDA00/PCLBUZ1/SEG20) for clock output/buzzer output requires setting the corresponding bits in the port mode register (PMxx) and port register (Pxx) to 0.

Example: When P02/(SO10/TxD1)/PCLBUZ0/SEG23 is to be used for clock output/buzzer output
Set the PM02 bit of port mode register 1 to 0.
Set the P02 bit of port register 1 to 0.
Set the PFSEG23 bit of LCD port function register 2 to 0.

Remark When using a port pin which is multiplexed with a segment output pin function for clock output/buzzer output, be sure to set the corresponding bit of the LCD port function registers 0 to 4 (PFSEG0 to PFSEG4) to “0”.

13.4 Operations of Clock Output/Buzzer Output Controller

One pin can be used to output a clock or buzzer sound.

The PCLBUZ0 pin outputs a clock/buzzer selected by clock output select register 0 (CKS0).

The PCLBUZ1 pin outputs a clock/buzzer selected by clock output select register 1 (CKS1).

13.4.1 Operation as output pin

The PCLBUZn pin is output as the following procedures.

<1> Set 0 in the bit of the port mode register (PMxx) and port register (Px) which correspond to the port which has a pin used as the PCLBUZ0 pin.

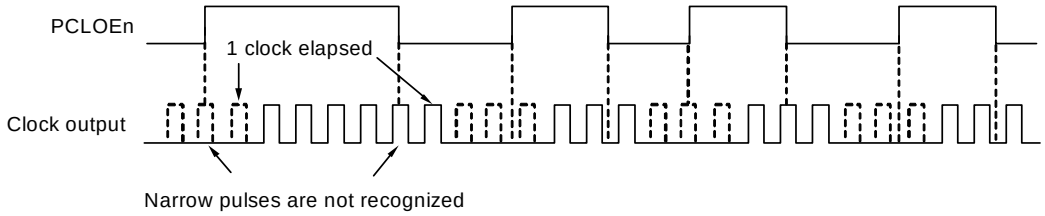
<2> Select the output frequency with bits 0 to 3 (CCSn0 to CCSn2, CSELn) of the clock output select register (CKSn) of the PCLBUZn pin (output in disabled status).

<3> Set bit 7 (PCLOEn) of the CKSn register to 1 to enable clock/buzzer output.

Remark 1. The controller used for outputting the clock starts or stops outputting the clock one clock after enabling or disabling clock output (PCLOEn bit) is switched. At this time, pulses with a narrow width are not output. Figure 13 - 3 shows enabling or stopping output using the PCLOEn bit and the timing of outputting the clock.

Remark 2. n = 0, 1

Figure 13 - 3 Timing of Outputting Clock from PCLBUZn Pin



13.5 Cautions of clock output/buzzer output controller

When the main system clock is selected for the PCLBUZn output (CSELn = 0), if STOP or HALT mode is entered within 1.5 clock cycles output from the PCLBUZn pin after the output is disabled (PCLOEn = 0), the PCLBUZn output width becomes shorter.

CHAPTER 14 WATCHDOG TIMER

14.1 Functions of Watchdog Timer

The counting operation of the watchdog timer is set by the option byte (000C0H).
The watchdog timer operates on the low-speed on-chip oscillator clock (f_{IL}).
The watchdog timer is used to detect an inadvertent program loop. If a program loop is detected, an internal reset signal is generated.
Program loop is detected in the following cases.

- If the watchdog timer counter overflows
- If a 1-bit manipulation instruction is executed on the watchdog timer enable register (WDTE)
- If data other than “ACH” is written to the WDTE register
- If data is written to the WDTE register during a window close period

When a reset occurs due to the watchdog timer, bit 4 (WDTRF) of the reset control flag register (RESF) is set to 1.
For details of the RESF register, see **CHAPTER 28 RESET FUNCTION**.
When 75% of the overflow time + 1/2f_{IL} is reached, an interval interrupt can be generated.

14.2 Configuration of Watchdog Timer

The watchdog timer includes the following hardware.

Table 14 - 1 Configuration of Watchdog Timer

Item	Configuration
Counter	Internal counter (17 bits)
Control register	Watchdog timer enable register (WDTE)

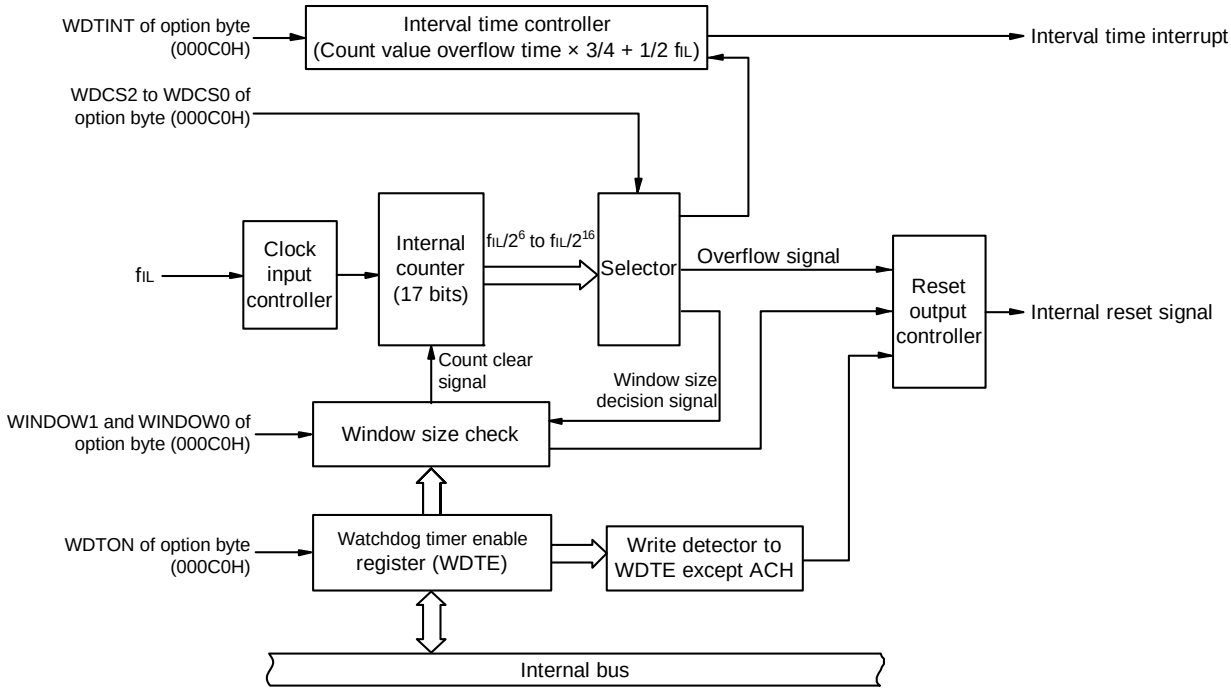
How the counter operation is controlled, overflow time, window open period, and interval interrupt are set by the option byte.

Table 14 - 2 Setting of Option Bytes and Watchdog Timer

Setting of Watchdog Timer	Option Byte (000C0H)
Watchdog timer interval interrupt	Bit 7 (WDTINT)
Window open period	Bits 6 and 5 (WINDOW1, WINDOW0)
Controlling counter operation of watchdog timer	Bit 4 (WDTON)
Overflow time of watchdog timer	Bits 3 to 1 (WDCS2 to WDCS0)
Controlling counter operation of watchdog timer (in HALT/STOP mode)	Bit 0 (WDSTBYON)

Remark For the option byte, see **CHAPTER 33 OPTION BYTE**.

Figure 14 - 1 Block Diagram of Watchdog Timer



Remark fIL: Low-speed on-chip oscillator clock

14.3 Register Controlling Watchdog Timer

The watchdog timer is controlled by the watchdog timer enable register (WDTE).

14.3.1 Watchdog timer enable register (WDTE)

Writing “ACH” to the WDTE register clears the watchdog timer counter and starts counting again.

This register can be set by an 8-bit memory manipulation instruction.

Reset signal generation sets this register to 9AH or 1AH Note.

Figure 14 - 2 Format of Watchdog timer enable register (WDTE)

Address: FFFABH After reset: 9AH/1AH Note R/W

Symbol	7	6	5	4	3	2	1	0
WDTE								

Note The WDTE register reset value differs depending on the WDTON bit setting value of the option byte (000C0H). To operate watchdog timer, set the WDTON bit to 1.

WDTON Bit Setting Value	WDTE Register Reset Value
0 (watchdog timer count operation disabled)	1AH
1 (watchdog timer count operation enabled)	9AH

Caution 1. If a value other than “ACH” is written to the WDTE register, an internal reset signal is generated.

Caution 2. If a 1-bit memory manipulation instruction is executed for the WDTE register, an internal reset signal is generated.

Caution 3. The value read from the WDTE register is 9AH/1AH (this differs from the written value (ACH)).

14.4 Operation of Watchdog Timer

14.4.1 Controlling operation of watchdog timer

1. When the watchdog timer is used, its operation is specified by the option byte (000C0H).

   • Enable counting operation of the watchdog timer by setting bit 4 (WDTON) of the option byte (000C0H) to 1 (the counter starts operating after a reset release) (for details, see **CHAPTER 33 OPTION BYTE**).

WDTON	Watchdog Timer Counter
0	Counter operation disabled (counting stopped after release from the reset state)
1	Counter operation enabled (counting started after release from the reset state)

   • Set an overflow time by using bits 3 to 1 (WDCS2 to WDCS0) of the option byte (000C0H) (for details, see **14.4.2 Setting overflow time of watchdog timer** and **CHAPTER 33 OPTION BYTE**).
   • Set a window open period by using bits 6 and 5 (WINDOW1 and WINDOW0) of the option byte (000C0H) (for details, see **14.4.3 Setting window open period of watchdog timer** and **CHAPTER 33 OPTION BYTE**).

2. After a reset release, the watchdog timer starts counting.
3. By writing “ACH” to the watchdog timer enable register (WDTE) after the watchdog timer starts counting and before the overflow time set by the option byte, the watchdog timer is cleared and starts counting again.
4. After that, write the WDTE register the second time or later after a reset release during the window open period. If the WDTE register is written during a window close period, an internal reset signal is generated.
5. If the overflow time expires without “ACH” written to the WDTE register, an internal reset signal is generated.
   An internal reset signal is generated in the following cases.

   • If a 1-bit manipulation instruction is executed on the WDTE register
   • If data other than “ACH” is written to the WDTE register

Caution 1. When data is written to the watchdog timer enable register (WDTE) for the first time after reset release, the watchdog timer is cleared in any timing regardless of the window open time, as long as the register is written before the overflow time, and the watchdog timer starts counting again.

Caution 2. After “ACH” is written to the WDTE register, an error of up to 2 clocks (f_{IL}) may occur before the watchdog timer is cleared.

Caution 3. The watchdog timer can be cleared immediately before the count value overflows.

Caution 4. The operation of the watchdog timer in the HALT and STOP and SNOOZE modes differs as follows depending on the set value of bit 0 (WDSTBYON) of the option byte (000C0H).

	WDSTBYON = 0	WDSTBYON = 1
In HALT mode	Watchdog timer operation stops.	Watchdog timer operation continues.
In STOP mode		
In SNOOZE mode		

If WDSTBYON = 0, the watchdog timer resumes counting after the HALT or STOP mode is released. At this time, the counter is cleared to 0 and counting starts.

When operating with the X1 oscillation clock after releasing the STOP mode, the CPU starts operating after the oscillation stabilization time has elapsed.

Therefore, if the period between the STOP mode release and the watchdog timer overflow is short, an overflow occurs during the oscillation stabilization time, causing a reset.

Consequently, set the overflow time in consideration of the oscillation stabilization time when operating with the X1 oscillation clock and when the watchdog timer is to be cleared after the STOP mode release by an interval interrupt.

14.4.2 Setting overflow time of watchdog timer

Set the overflow time of the watchdog timer by using bits 3 to 1 (WDCS2 to WDCS0) of the option byte (000C0H).

If an overflow occurs, an internal reset signal is generated. The present count is cleared and the watchdog timer starts counting again by writing “ACH” to the watchdog timer enable register (WDTE) during the window open period before the overflow time.

The following overflow times can be set.

Table 14 - 3 Setting of Overflow Time of Watchdog Timer

WDCS2	WDCS1	WDCS0	Overflow Time of Watchdog Timer (f_{IL} = 17.25 kHz (MAX.))
0	0	0	$2^6/f_{IL}$ (3.71 ms)
0	0	1	$2^7/f_{IL}$ (7.42 ms)
0	1	0	$2^8/f_{IL}$ (14.84 ms)
0	1	1	$2^9/f_{IL}$ (29.68 ms)
1	0	0	$2^{11}/f_{IL}$ (118.72 ms)
1	0	1	$2^{13}/f_{IL}$ (474.89 ms)
1	1	0	$2^{14}/f_{IL}$ (949.79 ms)
1	1	1	$2^{16}/f_{IL}$ (3799.18 ms)

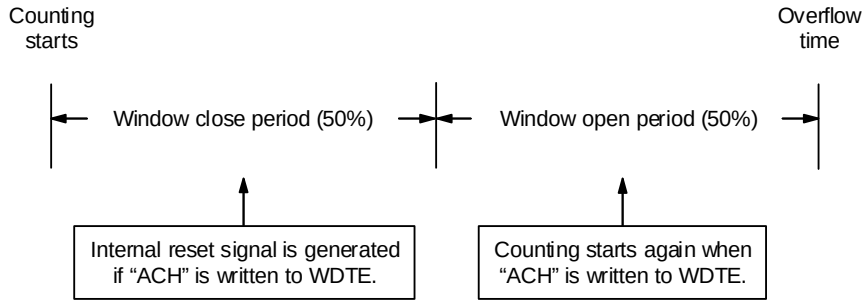
Remark f_{IL}: Low-speed on-chip oscillator clock frequency

14.4.3 Setting window open period of watchdog timer

Set the window open period of the watchdog timer by using bits 6 and 5 (WINDOW1, WINDOW0) of the option byte (000C0H). The outline of the window is as follows.

- If “ACH” is written to the watchdog timer enable register (WDTE) during the window open period, the watchdog timer is cleared and starts counting again.
- Even if “ACH” is written to the WDTE register during the window close period, an abnormality is detected and an internal reset signal is generated.

Example: If the window open period is 50%



Caution When data is written to the WDTE register for the first time after reset release, the watchdog timer is cleared in any timing regardless of the window open time, as long as the register is written before the overflow time, and the watchdog timer starts counting again.

The window open period can be set is as follows.

Table 14 - 4 Setting Window Open Period of Watchdog Timer

WINDOW1	WINDOW0	Window Open Period of Watchdog Timer
0	1	50%
1	1	100%
Other than above		Setting prohibited

Caution When bit 0 (WDSTBYON) of the option byte (000C0H) = 0, the window open period is 100% regardless of the values of the WINDOW1 and WINDOW0 bits.

Remark If the overflow time is set to $2^9/f_{IL}$, the window close time and open time are as follows.

	Setting of Window Open Period	
	50%	100%
Window close time	0 to 20.08 ms	None
Window open time	20.08 to 29.68 ms	0 to 29.68 ms

<When window open period is 50%>

- Overflow time:
  $2^9/f_{IL}$ (MAX.) = 2^9/17.25 kHz = 29.68 ms
- Window close time:
  0 to $2^9/f_{IL}$ (MIN.) × (1 - 0.5) = 0 to 2^9/12.75 kHz × 0.5 = 0 to 20.08 ms
- Window open time:
  $2^9/f_{IL}$ (MIN.) × (1 - 0.5) to $2^9/f_{IL}$ (MAX.) = 2^9/12.75 kHz × 0.5 to 2^9/17.25 kHz = 20.08 to 29.68 ms

14.4.4 Setting watchdog timer interval interrupt

Depending on the setting of bit 7 (WDTINT) of an option byte (000C0H), an interval interrupt (INTWDTI) can be generated when 75% of the overflow time + 1/2f_{IL} is reached.

Table 14 - 5 Setting of Watchdog Timer Interval Interrupt

WDTINT	Use of Watchdog Timer Interval Interrupt
0	Interval interrupt is not used.
1	Interval interrupt is generated when 75% of the overflow time + 1/2f_{IL} is reached.Note

Note When the interval interrupt of the watchdog timer is in use, clear the counter of the watchdog timer by following the procedure under **14.4.5 Cautions on the watchdog timer**.

Caution **When operating with the X1 oscillation clock after releasing the STOP mode, the CPU starts operating after the oscillation stabilization time has elapsed.**
Therefore, if the period between the STOP mode release and the watchdog timer overflow is short, an overflow occurs during the oscillation stabilization time, causing a reset.
Consequently, set the overflow time in consideration of the oscillation stabilization time when operating with the X1 oscillation clock and when the watchdog timer is to be cleared after the STOP mode release by an interval interrupt.

Remark The watchdog timer continues counting even after INTWDTI is generated (until ACH is written to the watchdog timer enable register (WDTE)). If ACH is not written to the WDTE register before the overflow time, an internal reset signal is generated.

14.4.5 Cautions on the watchdog timer

When the interval interrupt of the watchdog timer is in use, clear the counter of the watchdog timer in accord with the procedure given as steps 1 to 5 below.

(1) Set the WDTIMK bit in interrupt mask flag register 0 (MK0L) to 1 before clearing the counter for the watchdog timer.
(2) Clear the counter of the watchdog timer.
(3) Wait for at least 80 μs.
(4) Clear the WDTIIF bit in interrupt request flag register 0 (IF0L) to 0.
(5) Clear the WDTIMK bit in interrupt mask flag register 0 (MK0L) to 0.

CHAPTER 15 ANALOG FRONT-END POWER SUPPLY CIRCUIT (R5F11N and R5F11P only)

15.1 Functions of Analog Front-End Power Supply Circuit

The analog front-end (AFE) power supply circuit consists of an AFE reference power supply (ABGR), LDO for supplying power to internal circuits (REGA), and LDO for supplying power to an external sensor device (SBIAS).

The operating mode can be selected by setting a PON signal that controls the power to the corresponding function and the AFEPON signal that controls the reference power supply for the entire AFE by using a control register. All the PON signals are initialized when the AFEEN bit of peripheral enable register 1 (PER1) is cleared to 0.

You can check the power status of ABGR by reading the AFESTAT bit of the analog front-end power supply detection register (AFEPWD).You can check the power status of REGA and SBIAS by reading the PGASTAT bit of the AFEPWD register.

Table 15 - 1 Control over Power Supply of Analog Front-end (AFE)

Functional Block		Bit in the register controlling the power supply of the analog front-end (AFE)								
		AFE PON	PGA PON	AMP PON	AMP E0	AMP E1	AMP E2	AMP E3	DAC0 PON	DAC1 PON
PGA0 and 24-bit ΔΣ A/D converter		√	√	—	—	—	—	—	—	—
Amplifier unit 0 (PGA1)		√	—	√	√	—	—	—	—	√
Amplifier unit 1 (AMP0)		√	—	√	—	√	—	—	Note 1	—
Amplifier unit 2 (AMP1)		√	Note 2	√	—	—	√	—	—	Note 1
Amplifier unit 3 (AMP2)		√	Note 2	√	—	—	—	√	—	Note 1
8-bit D/A converter (DAC0)		√	√	—	—	—	—	—	√	—
12-bit D/A converter (DAC1)	When AV_{DD} is selected as the reference voltage	√	—	—	—	—	—	—	—	√
	When SBIAS is selected as the reference voltage	√	√	—	—	—	—	—	—	√

Note 1. When the D/A converter is selected to provide the positive input voltage of the amplifier unit, set this bit to 1 (power-on).

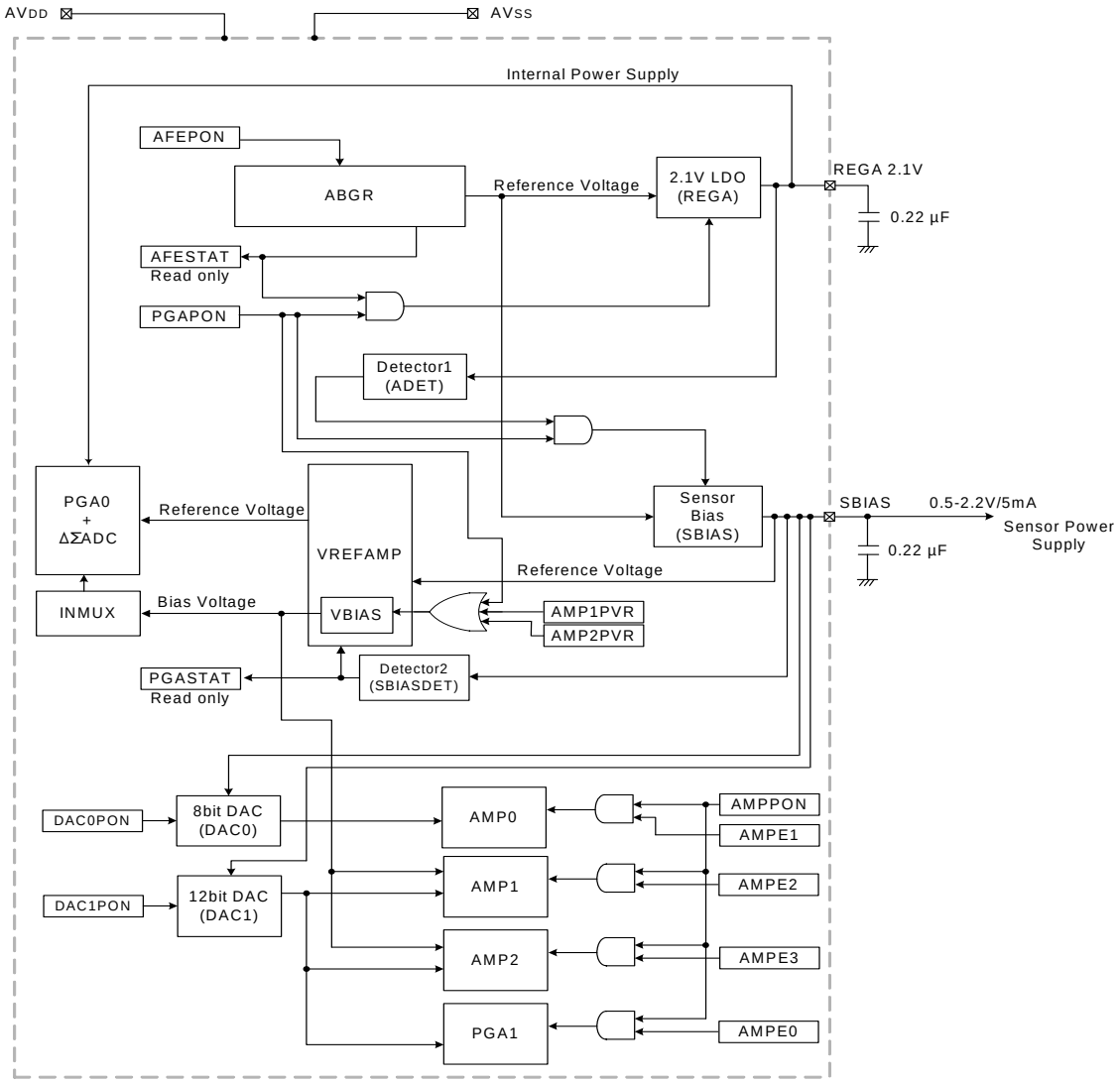
Note 2. When the internal bias voltage (VBIAS) is selected to provide the positive input voltage of the amplifier unit, set this bit to 1 (power-on).

Remark Set the analog front-end power supply circuit by the bit of the analog front-end power supply selection register (AFEPWS) and amplifier control register (AMPC) in the amplifier unit.

15.2 Configuration of Analog Front-End Power Supply Circuit

Figure 15 - 1 shows the block diagram of the analog front-end power supply circuit.

Figure 15 - 1 Block Diagram of Analog Front-End Power Supply Circuit



15.3 Registers Controlling the Analog Front-End Power Supply Circuit

The following registers are used to control the analog front-end power supply circuit.

- Peripheral enable register 1 (PER1)
- Analog front-end power supply selection register (AFEPWS)
- Analog front-end power supply detection register (AFEPWD)
- Sensor reference voltage setting register (VSBIAS)

15.3.1 Peripheral enable register 1 (PER1)

This register is used to enable or disable supplying the clock to the peripheral hardware. Clock supply to the hardware that is not used is also stopped so as to decrease the power consumption and noise.

The PER1 register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 15 - 2 Format of Peripheral Enable Register 1 (PER1)

Address: F007AH After reset: 00H R/W

Symbol	<7>	6	5	<4>	<3>	<2>	<1>	<0>
PER1	TMKAEN	0	0	AMPEN Note	DTCEN	PGAEN Note	AFEEN Note	DACEN Note

AFEEN Note	Control of input clock supplied to clock control block in AFE power supply
0	Stops input clock supply. • SFRs used by the clock control block in AFE power supply cannot be written. • The clock control block in AFE power supply is in the reset status.
1	Enables input clock supply. • SFRs used by the clock control block in AFE power supply can be read and written.

Note R5F11N and R5F11P only.

Caution 1. When setting the analog front-end power supply circuit, be sure to set the AFEEN bit to 1 first. If AFEEN = 0, writing to a control register of the analog front-end power supply circuit is ignored, and all read values are default values.

Caution 2. Be sure to clear following bits to "0".
R5F11N, R5F11P: Bits 5 and 6
R5F11R: Bits 0 to 2, and 4 to 6

15.3.2 Analog front-end power supply selection register (AFEPWS)

The operating mode can be selected by setting a PON signal that controls the power to the corresponding function and the AFEPON signal that controls the reference power supply for the entire AFE by using the AFEPWS register.
The AFEPWS register can be set by a 1-bit or 8-bit memory manipulation instruction.
Reset signal generation clears this register to 00H.

Figure 15 - 3 Format of Analog Front-End Power Supply Selection Register (AFEPWS)

Address: F0440H After reset:00H R/W

Symbol	<7>	<6>	5	<4>	3	<2>	1	<0>
AFEPWS	DAC1PON	DAC0PON	0	AMP0PON	0	PGAPON	0	AFEPON

DAC1PON	Control of power supplied to 12-bit D/A converter (DAC1) block
0	Power-off (default)
1	Power-on

DAC0PON	Control of power supplied to 8-bit D/A converter (DAC0) block
0	Power-off (default)
1	Power-on

AMPPON	Control of power supplied to amplifier unit block
0	Power-off (default)
1	Power-on

PGAPON	Control of power supplied to programmable gain instrumentation amplifier (PGA0) and sensor reference voltage source (SBIAS) blocks
0	Power-off (default)
1	Power-on

AFEPON	Control of power supplied to AFE reference power supply (ABGR) block
0	Power-off (default)
1	Power-on

Caution Be sure to clear bits 1, 3, and 5 to “0”.

15.3.3 Analog front-end power supply detection register (AFEPWD)

You can check the power status of the AFE reference power supply (ABGR) by reading the AFESTAT bit of the analog front-end power supply detection register (AFEPWD).

You can check the power status of REGA and SBIAS by reading the PGASTAT bit of the AFEPWD register.

The AFEPWD register can be read by a 1-bit or an 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 15 - 4 Format of Analog Front-End Power Supply Detection Register (AFEPWD)

Address: F0441H After reset: 00H R

Symbol	7	6	5	4	3	<2>	1	<0>
AFEPWD	0	0	0	0	0	PGASTAT	0	AFESTAT

PGASTAT	Status of power supplied to programmable gain instrumentation amplifier (PGA0) and sensor reference voltage source (SBIAS) blocks
0	Off or stabilizing
1	Stabilized

AFESTAT	Status of power supplied to AFE reference power supply (ABGR) block
0	Off or stabilizing
1	Stabilized

15.3.4 Sensor reference voltage setting register (VSBIAS)

This register is used to specify the SBIAS reference voltage source.

The VSBIAS register can be set by an 8-bit memory manipulation instruction.

Reset signal generation sets this register to 19H.

Figure 15 - 5 Format of Sensor Reference Voltage Setting Register (VSBIAS)

Address: F0443H After reset: 19H R/W

Symbol	7	6	5	4	3	2	1	0
VSBIAS	0	0	0	VSBIAS4	VSBIAS3	VSBIAS2	VSBIAS1	VSBIAS0

VSBIAS4	VSBIAS3	VSBIAS2	VSBIAS1	VSBIAS0	SBIAS output voltage (V)
0	1	0	0	1	0.5
0	1	0	1	0	0.6
0	1	0	1	1	0.7
0	1	1	0	0	0.8
0	1	1	0	1	0.9
0	1	1	1	0	1.0
0	1	1	1	1	1.1
1	0	0	0	0	1.2
1	0	0	0	1	1.3
1	0	0	1	0	1.4
1	0	0	1	1	1.5
1	0	1	0	0	1.6
1	0	1	0	1	1.7
1	0	1	1	0	1.8
1	0	1	1	1	1.9
1	1	0	0	0	2.0
1	1	0	0	1	2.1 (initial value)
1	1	0	1	0	2.2
Other than above					Setting prohibited

Caution 1. Be sure to clear bits 5 to 7 to “0”.

Caution 2. Set the voltage to at least 1.8 V if the 8-bit D/A converter (DAC0) is to be used.

Caution 3. Set the voltage to at least 1.5 V if the 12-bit D/A converter (DAC1) is to be used.

15.4 AFE Internal Reference Voltage Generator

15.4.1 Overview of AFE internal reference voltage generator

The AFE internal reference voltage generator consists of an AFE reference power supply (ABGR) and an analog circuit reference voltage generator (VREFAMP).

The VREF reference voltage output from ABGR is supplied to the REGA and SBIAS circuits.

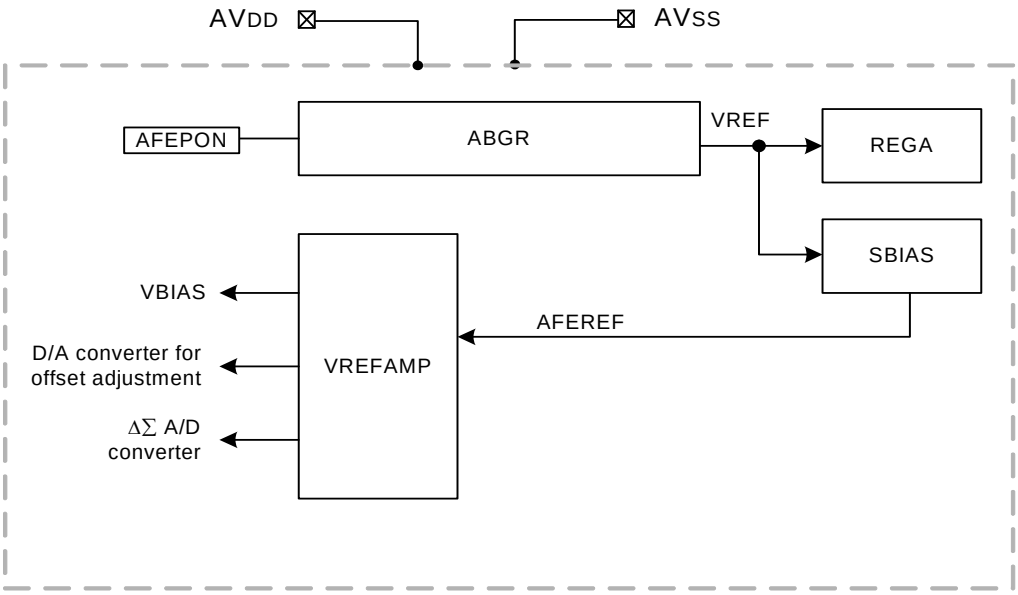
The VREF reference voltage output from ABGR passes through the SBIAS circuit and is supplied to the VREFAMP circuit, and is then used as a reference voltage in the 24-bit ΔΣ A/D converter, as a reference voltage in the D/A converter for offset voltage adjustment, and as an internal bias voltage (VBIAS) to be connected to input multiplexers.

ABGR can achieve high precision in the output voltage because it is less dependent on the temperature.

15.4.2 Configuration of AFE internal reference voltage generator

Figure 15 - 6 shows the block diagram of the AFE internal reference voltage generator.

Figure 15 - 6 Block Diagram of AFE Internal Reference Voltage Generator



15.4.3 Operation of AFE internal reference voltage generator

The AFEPON bit of the AFEPWS register controls whether to turn ABGR on and off. It is recommended to power off ABGR (by clearing the AFEPON bit to 0) after the 24-bit ΔΣ A/D converter, amplifier unit, 8-bit D/A converter, and 12-bit D/A converter turn off.

15.5 Sensor Power Supply (SBIAS)

15.5.1 Overview of sensor power supply (SBIAS)

SBIAS supplies power to the sensor connected to the RL78/H1D. The VREF reference voltage output from ABGR is input. SBIAS outputs a voltage between 0.5 to 2.2 V, which can be specified in units of 0.1 V. SBIAS outputs up to 5 mA of current. An external capacitor of 0.22 µF (recommended) must be connected to the SBIAS pin.

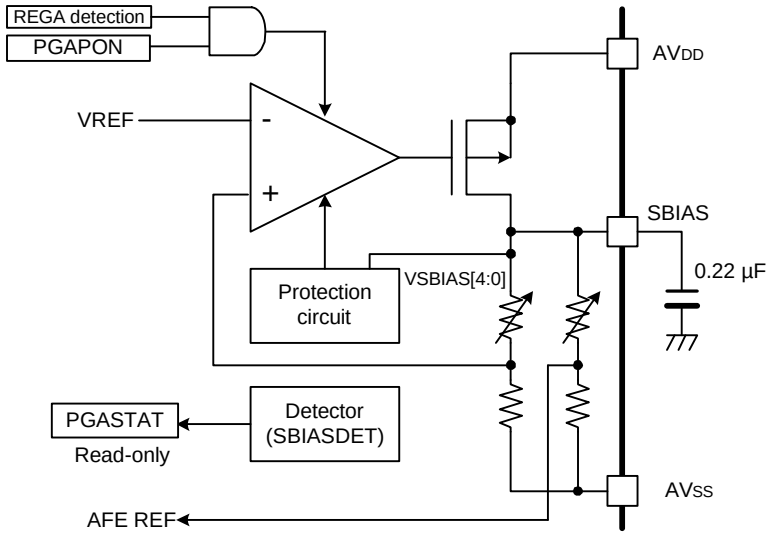
SBIAS has a protection circuit against an overcurrent (a current exceeding the rated upper limit). When an overcurrent occurs, the protection circuit works to protect the internal circuits. SBIAS also has a circuit (SBIASDET) that monitors and detects the voltage output by SBIAS.

The VREF reference voltage output from ABGR passes through the SBIAS circuit and is then used as a reference voltage in the D/A converter for offset voltage adjustment and ΔΣ A/D converter, and as an internal bias voltage (VBIAS) to be connected to input multiplexers.

15.5.2 Configuration of sensor power supply (SBIAS)

Figure 15 - 7 shows the block diagram of the sensor power supply (SBIAS).

Figure 15 - 7 Block Diagram of Sensor Power Supply (SBIAS)



15.5.3 Operation of sensor power supply (SBIAS)

In addition to supplying power to the sensor connected to the RL78/H1D, SBIAS is involved in generating reference voltages used in the ΔΣ A/D converter and the D/A converter for offset voltage adjustment, and an internal bias voltage (VBIAS) to be connected to input multiplexers.

SBIAS has SBIASDET, a circuit that monitors and detects the voltage output by SBIAS, and is used to start analog circuits such as VREFAMP, programmable gain instrumentation amplifier (PGA0), and ΔΣ A/D converter. When SBIASDET detects the SBIAS output voltage, starting the analog circuits is enabled. When SBIASDET detects that the SBIAS output voltage has not risen normally, analog circuits stop operating.

When "0" is written to the AFEPON bit of the analog front-end power supply selection register (AFEPWS), SBIASDET detects the SBIAS output voltage and analog circuits such as VREFAMP, PGA0, ΔΣ A/D converter, and SBIAS stop operating. When VREFAMP stops operating, a reference voltage in the ΔΣ A/D converter and D/A converter for offset voltage adjustment and an internal bias voltage (VBIAS) to be connected to input multiplexers are not generated.

15.6 Internal Power Supply for PGA0 and ΔΣ A/D Converter (REGA)

15.6.1 Overview of internal power supply (REGA)

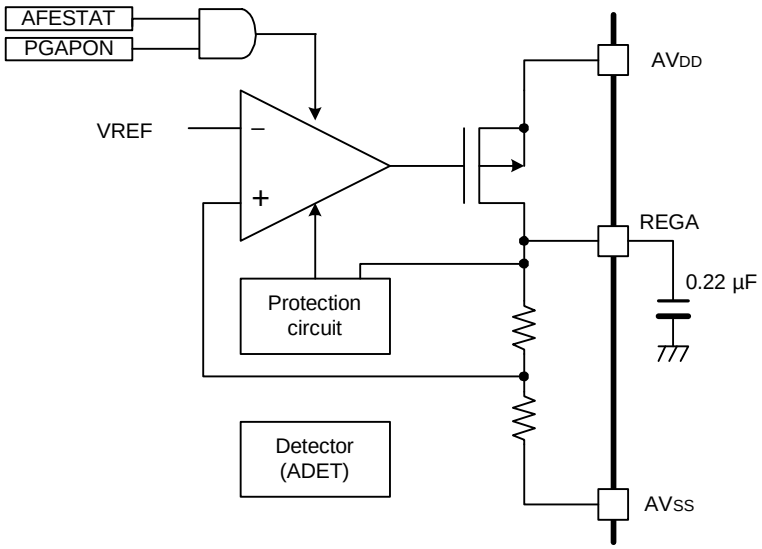
REGA generates a voltage based on the voltage output from the ABGR, and supplies power to the PGA0 and ΔΣ A/D converter. REGA outputs a voltage of 2.1 V (Typ.). An external capacitor of 0.22 µF (recommended) must be connected to the REGA output pin.

REGA has a protection circuit against an overcurrent and a low voltage detector (ADET).

15.6.2 Configuration of internal power supply (REGA)

Figure 15 - 8 shows the block diagram of the internal power supply (REGA).

Figure 15 - 8 Block Diagram of Internal Power Supply (REGA)



15.7 Procedure for Controlling Analog Front-End Power Supply Circuit

Figure 15 - 9 and Figure 15 - 10 show the flowcharts for powering on/off the analog front-end power supply. Figure 15 - 11 shows the timing diagram for the power-on sequence.

Figure 15 - 9 Flowchart for Powering on the Analog Front-End (AFE) Power Supply

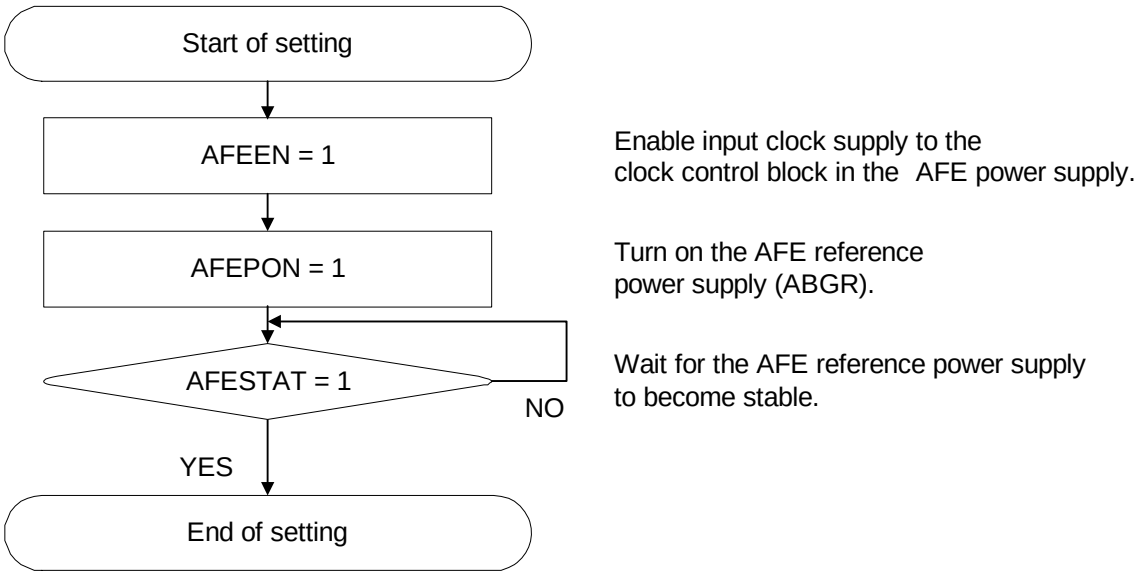


Figure 15 - 10 Flowchart for Powering off the Analog Front-End (AFE) Power Supply

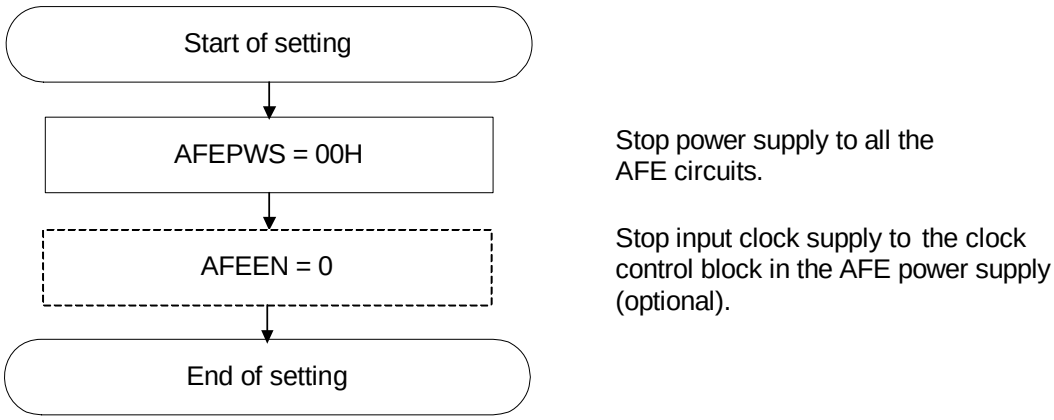
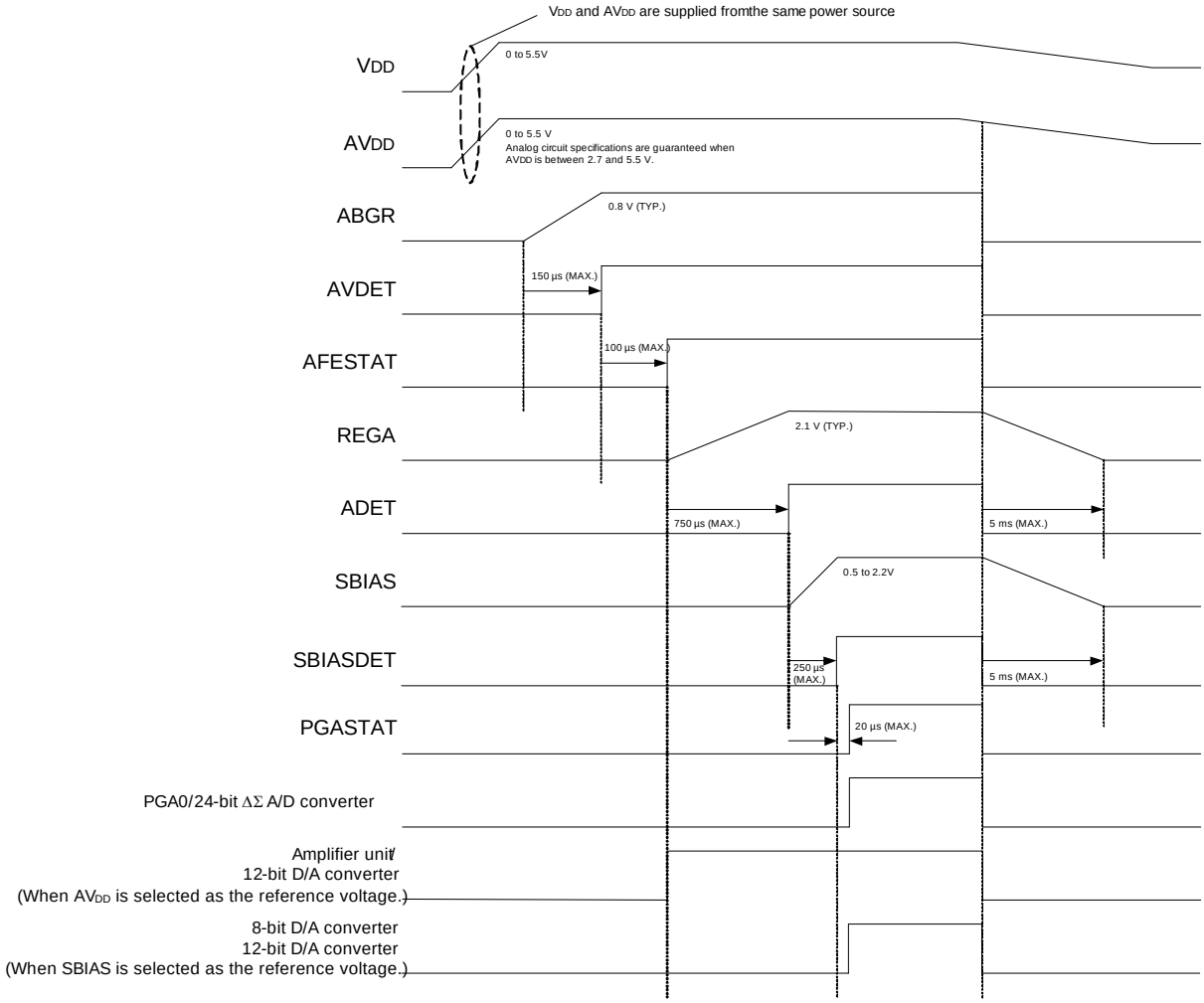


Figure 15 - 11 Timing for Power Supply Startup Sequence



Remark AVDET is the low voltage detection circuit for the output voltage from the AFE reference power supply (ABGR).

CHAPTER 16 24-BIT ΔΣ A/D CONVERTER WITH PROGRAMMABLE GAIN INSTRUMENTATION AMPLIFIER (R5F11N and R5F11P only)

16.1 Functions of 24-bit ΔΣ A/D Converter with Programmable Gain Instrumentation Amplifier

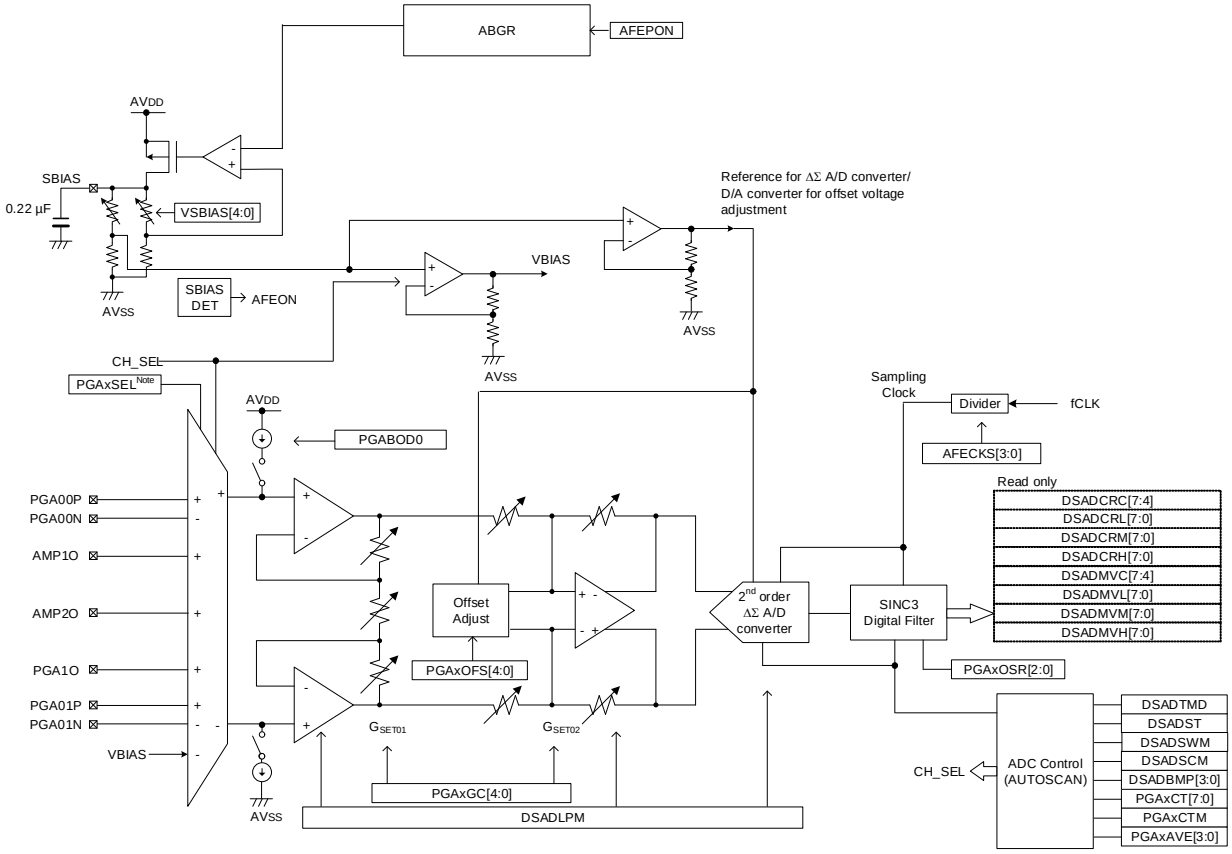
The RL78/H1D incorporates a 24-bit ΔΣ A/D converter with programmable gain instrumentation amplifier. The signal from an input multiplexer (there are 5 channels in total) is input to the 24-bit ΔΣ A/D converter via the programmable gain instrumentation amplifier (PGA0). The A/D conversion result is filtered by the SINC3 digital filter, and is then stored in an output register.

A/D conversion is performed based on the clock generated in the high-speed on-chip oscillator (HOCO) (sampling frequency = 1 MHz (TYP.)). The high-speed system clock can also be used. A/D conversion is performed based on a built-in sequencer called AUTOSCAN. The data rate (frequency with which each A/D conversion result is output) can be specified for each channel.

16.2 Configuration of 24-bit ΔΣ A/D Converter with Programmable Gain Instrumentation Amplifier

Figure 16 - 1 shows the block diagram of the 24-bit ΔΣ A/D converter with programmable gain instrumentation amplifier.

Figure 16 - 1 Block Diagram of 24-bit ΔΣ A/D Converter with Programmable Gain Instrumentation Amplifier



Note This is the case for input multiplexer 0. In the case of input multiplexer 3, the setting is made by the PGA3SEL0 and PGA3SEL1 bits. For details, see **16.3.3 Registers controlling input multiplexers**.

16.3 Input Multiplexer

16.3.1 Overview of input multiplexer

The input multiplexer has five analog input channels, two of which (input multiplexers 0 and 3) can be used for the input of an external signal. The remaining three (input multiplexers 1 to 3) are connected to the output from the internal amplifier unit. Input multiplexer 3 is used for an external input or internal connection (exclusive of each other). For the 2 channels (input multiplexers 0 and 3) which can be used for external input, differential input mode or single-ended input mode can be selected for each. The other channels are fixed to the single-ended input mode. If the single-ended input mode is selected, an internal bias voltage (VBIAS) is connected to the negative input pin of the programmable gain instrumentation amplifier (PGA0).

The number of analog input channels to the input multiplexers depends on the product.

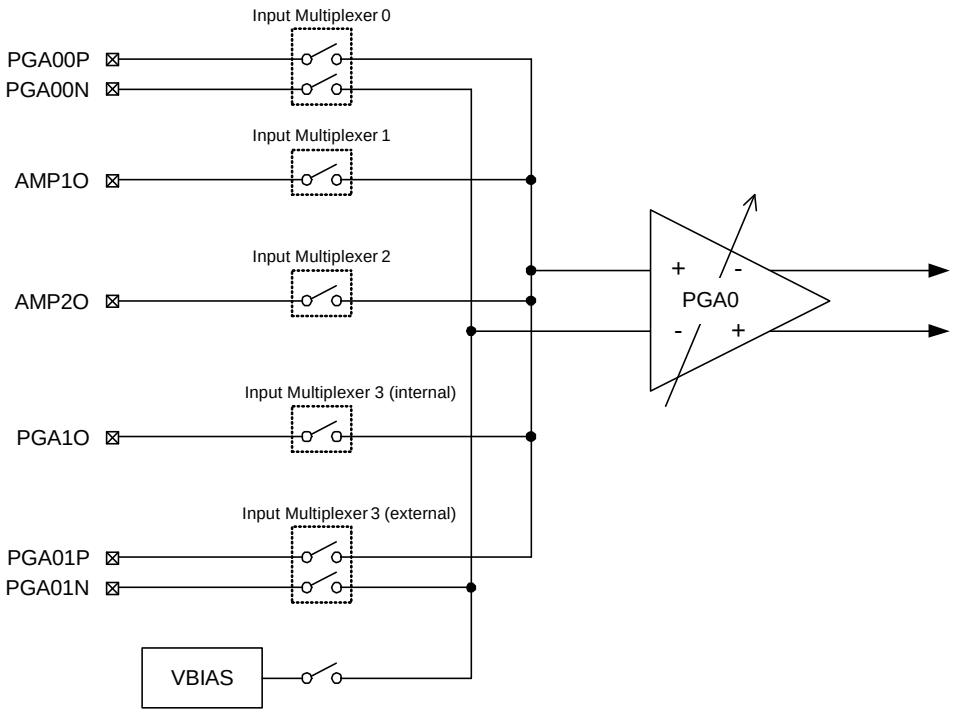
Table 16 - 1 Input Multiplexer

Input Multiplexer		R5F11NM	R5F11NL	R5F11PL, R5F11NG
Input multiplexer 0		√	√	√
Input multiplexer 1		—	√	√
Input multiplexer 2		—	√	√
Input multiplexer 3	Internal	—	√	√
	External	—	—	√
Number of valid channels		1 channel	4 channels	5 channels

16.3.2 Configuration of input multiplexer

Figure 16 - 2 shows the block diagram of an input multiplexer.

Figure 16 - 2 Block Diagram of Input Multiplexer



16.3.3 Registers controlling input multiplexers

The following register is used to control input multiplexers.

(1) Input multiplexer 0 setting register 1 (PGA0CTL1)

This register is used to specify the input setting for the input multiplexer 0.

The PGA0CTL1 register can be set by an 8-bit memory manipulation instruction.

Reset signal generation sets this register to 10H.

Figure 16 - 3 Format of Input Multiplexer 0 Setting Register 1 (PGA0CTL1)

Address: F045BH (PGA0CTL1) After reset: 10H R/W

Symbol	7	6	5	4	3	2	1	0
PGA0CTL1	PGA0SEL	0	0	PGA0OFS4 Note	PGA0OFS3 Note	PGA0OFS2 Note	PGA0OFS1 Note	PGA0OFS0 Note

PGA0SEL	Control of input multiplexer 0
0	Differential input
1	Single-ended input

Note For details about the PGA0OFS0 to PGA0OFS4 bits, refer to **16.4.6 (2) Input multiplexer x (x = 0 to 3) setting register 1 (PGAxCTL1)**.

Caution Be sure to clear bits 5 and 6 to "0".

(2) Input multiplexer 3 setting register 1 (PGA3CTL1)

This register is used to specify the input setting for the input multiplexer 3.

The PGA3CTL1 register can be set by an 8-bit memory manipulation instruction.

Reset signal generation sets this register to 10H.

Figure 16 - 4 Format of Input Multiplexer 3 Setting Register 1 (PGA3CTL1)

Address: F0467H (PGA3CTL1) After reset: 10H R/W

Symbol	7	6	5	4	3	2	1	0
PGA3CTL1	PGA3SEL1	PGA3SEL0	0	PGA3OFS4 Note	PGA3OFS3 Note	PGA3OFS2 Note	PGA3OFS1 Note	PGA3OFS0 Note

PGA3SEL1	PGA3SEL0	Control of input multiplexer 3
0	0	Single-ended input (PGA1O output is connected internally)
1	0	
0	1	Differential input (external input from PGA01P/PGA01N pin)
1	1	Single-ended input (external input from PGA01P pin)

Note For details about the PGA3OFS0 to PGA3OFS4 bits, refer to **16.4.6 (2) Input multiplexer x (x = 0 to 3) setting register 1 (PGAxCTL1)**.

Caution Be sure to clear bit 5 to "0".

16.4 Programmable Gain Instrumentation Amplifier (PGA0)

16.4.1 Overview of programmable gain instrumentation amplifier (PGA0)

The programmable gain instrumentation amplifier (PGA0) features low offset voltage, low 1/f noise, and high impedance. The PGA operates in differential input mode or single-ended input mode according to the setting of the input multiplexer used.

In differential input mode and single-ended input mode, a gain from x1 to x64 (G_{TOTAL0}) can be specified by combining the gain in the 1st amplifier (G_{SET01}) and the gain in the 2nd amplifier (G_{SET02}) in the instrumentation amplifier.

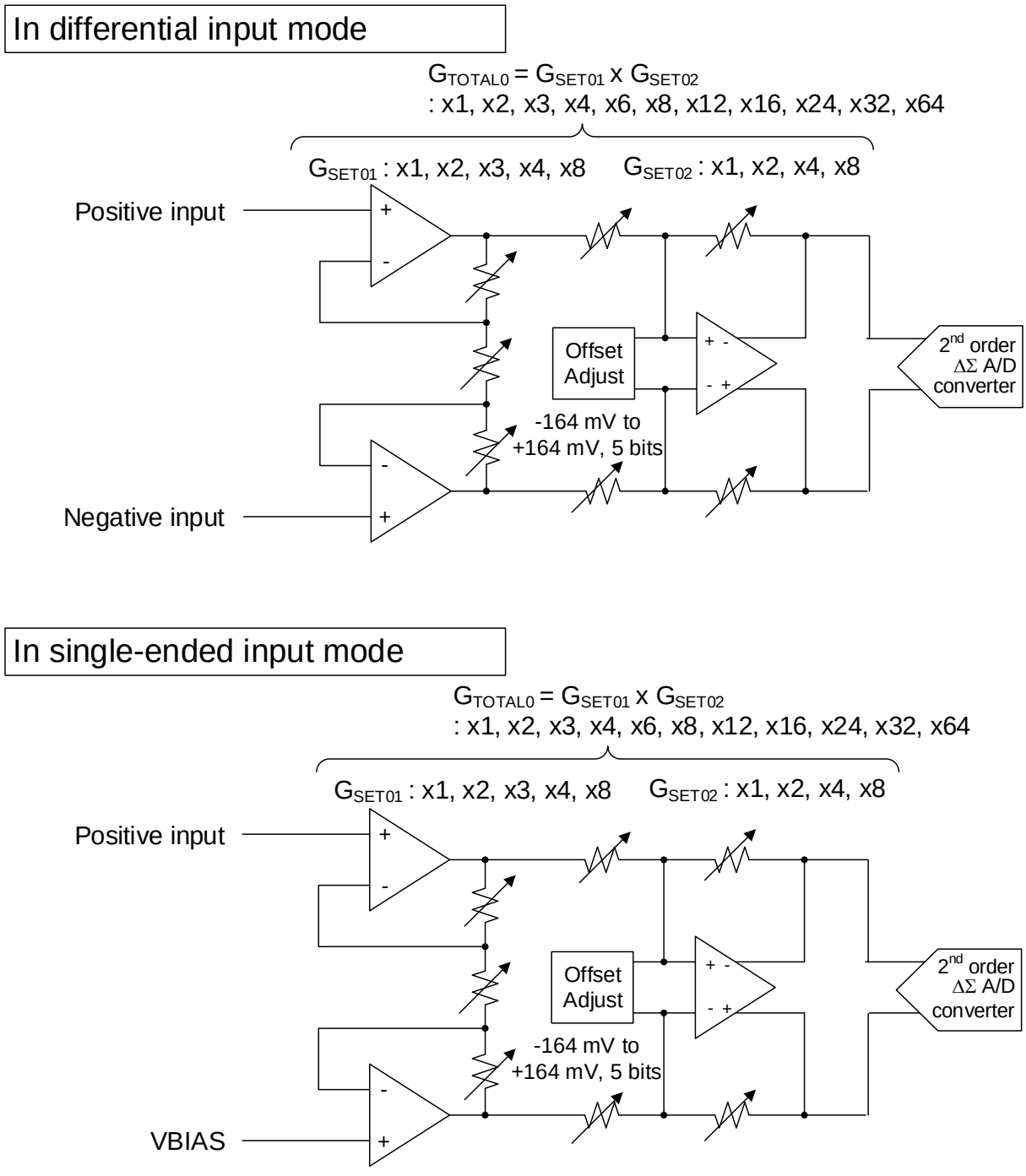
A D/A converter for adjusting the offset voltage is connected to the 2nd amplifier. In differential input mode and single-ended input mode, the offset voltage can be adjusted (from -164 mV to +164 mV, in 31 steps (5 bits)) by using this D/A converter.

To detect disconnection between a sensor and a PGA0 input, a current source load can be internally connected to the PGA0 input.

16.4.2 Configuration of programmable gain instrumentation amplifier (PGA0)

Figure 16 - 5 shows the block diagram of the programmable gain instrumentation amplifier (PGA0).

Figure 16 - 5 Block Diagram of Programmable Gain Instrumentation Amplifier (PGA0)



16.4.3 Input voltage range

This section describes the range of voltage input to the programmable gain instrumentation amplifier (PGA0). Figure 16 - 6 and Figure 16 - 8 show the input voltage range in differential input mode and single-ended input mode.

16.4.4 Input voltage range in differential input mode

V_{SIG} indicates the input-referred amplitude of the differential voltage input signal, V_{COM} indicates the input-referred common mode input voltage, and d_{OFR} indicates the input-referred D/A converter output voltage for adjusting the offset voltage. The voltage input to an amplifier should be 0.2 to 1.8 V. Therefore, the signal that passes through the 1st amplifier in the instrumentation amplifier and is then input to the 2nd amplifier must satisfy the conditions in Formula 1.

The signal that passes through the 1st amplifier in the instrumentation amplifier and is then output from the 2nd amplifier must satisfy the conditions in Formula 2.

Formula 1

$$0.2\ \mathrm{V} + \frac{|V_{SIG}| \times G_{SET01}}{2} \leq V_{COM} \leq 1.8\ \mathrm{V} - \frac{|V_{SIG}| \times G_{SET01}}{2}$$

Formula 2

$$-0.8\ \mathrm{V} \leq (V_{SIG} + d_{OFR}) \times G_{TOTAL0} \leq 0.8\ \mathrm{V}$$

When d_{OFR} = 0 mV, the input signal is equivalent to the full-scale differential input voltage. V_{COM} can be expressed by using Formula 3, where $V_{SIG} = V_{ID}$ (full-scale differential input voltage).

Formula 3

$$0.2\ \mathrm{V} + \frac{|V_{ID}| \times G_{SET01}}{2} \leq V_{COM} \leq 1.8\ \mathrm{V} - \frac{|V_{ID}| \times G_{SET01}}{2}$$

Figure 16 - 6 Input Voltage Range in Differential Input Mode

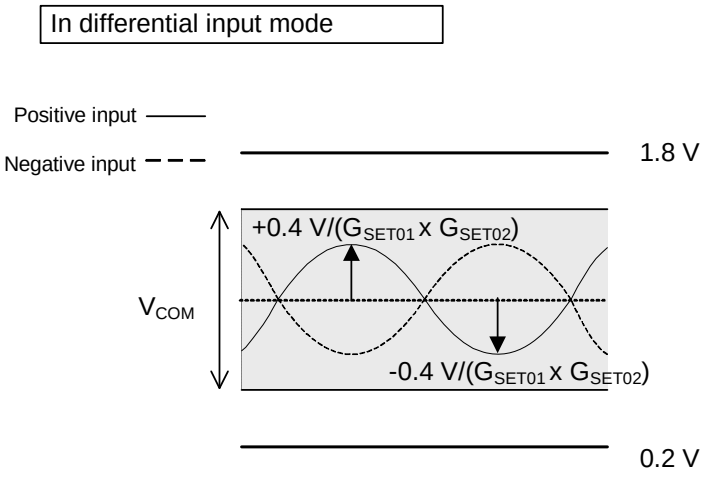
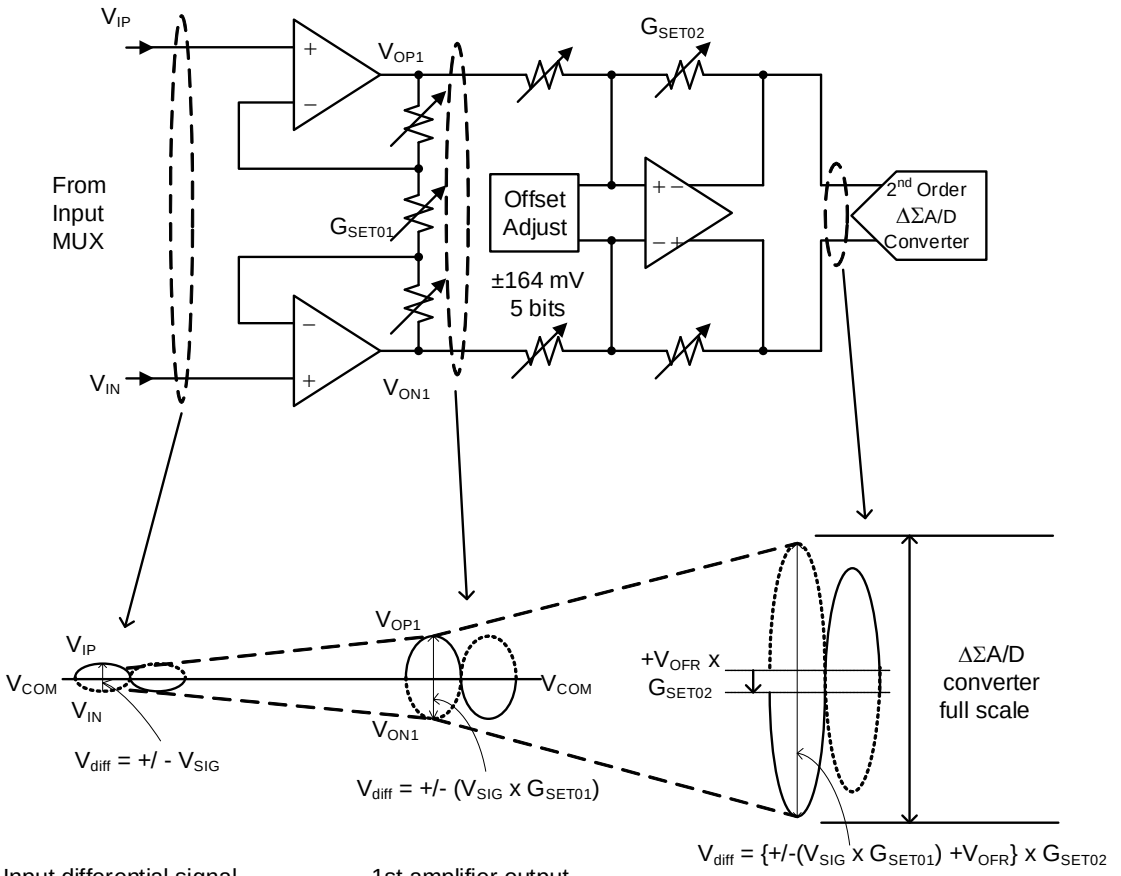


Figure 16 - 7 shows the transition of the differential input voltage level in the programmable gain instrumentation amplifier (PGA0).

Figure 16 - 7 Transition of the Differential Input Voltage Level in the Programmable Gain Instrumentation Amplifier (PGA0)

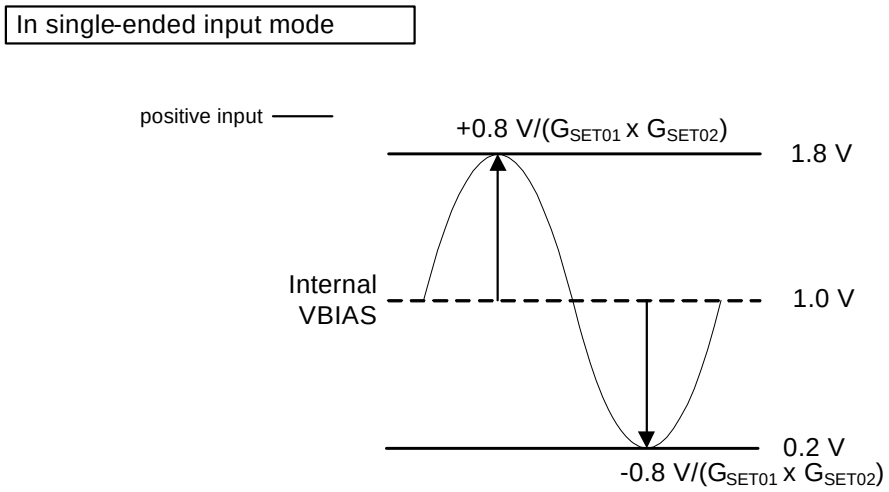


16.4.5 Input voltage range in single-ended input mode

In single-ended input mode, the signal from input multiplexer x (x = 0 to 3) is connected to the positive input in the programmable gain instrumentation amplifier (PGA0). The internal bias voltage (VBIAS = 1.0 V (TYP.)) is connected to the negative input in the programmable gain instrumentation amplifier (PGA0) as a reference voltage. A differential signal in the range of 0.2 to 1.8 V is output based on the reference voltage.
The input voltage range (V_I) must satisfy the conditions in the following formulas:

Formula 1: $0.2\ V \leq V_I \leq 1.8\ V$
Formula 2: $-0.8\ V \leq (V_I - 1.0\ V + d_{OFR}) \times G_{TOTAL0} \leq +0.8\ V$

Figure 16 - 8 Input Voltage Range in Single-Ended Input Mode



16.4.6 Registers controlling the programmable gain instrumentation amplifier (PGA0)

The following registers are used to control the programmable gain instrumentation amplifier (PGA0).

- Input multiplexer x (x = 0 to 3) setting register 0 (PGAxCTL0)
- Input multiplexer x (x = 0 to 3) setting register 1 (PGAxCTL1)
- Disconnection detection setting register (PGABOD)

(1) Input multiplexer x (x = 0 to 3) setting register 0 (PGAxCTL0)

This register is used to specify the gain of the programmable gain instrumentation amplifier for input multiplexer x (x = 0 to 3).

The PGAxCTL0 register can be set by an 8-bit memory manipulation instruction.

Reset signal generation sets this register to 40H.

Figure 16 - 9 Format of Input Multiplexer x (x = 0 to 3) Setting Register 0 (PGAxCTL0)

Address: F045AH (PGA0CTL0), F045EH (PGA1CTL0), F0462H (PGA2CTL0), F0466H (PGA3CTL0) After reset: 40H R/W

Symbol	7	6	5	4	3	2	1	0
PGAxCTL0	PGAxOSR2Note	PGAxOSR1Note	PGAxOSR0Note	PGAxGC4	PGAxGC3	PGAxGC2	PGAxGC1	PGAxGC0

PGAxGC4	PGAxGC3	PGAxGC2	PGAxGC1	PGAxGC0	Gain setting		
					GSET01	GSET02	GTOTAL0
0	0	0	0	0	1	1	1
0	0	1	0	0	2	1	2
0	1	0	0	0	3	1	3
0	1	1	0	0	4	1	4
1	0	0	0	0	8	1	8
0	0	0	0	1	1	2	2
0	0	1	0	1	2	2	4
0	1	0	0	1	3	2	6
0	1	1	0	1	4	2	8
1	0	0	0	1	8	2	16
0	0	0	1	0	1	4	4
0	0	1	1	0	2	4	8
0	1	0	1	0	3	4	12
0	1	1	1	0	4	4	16
1	0	0	1	0	8	4	32
0	0	0	1	1	1	8	8
0	0	1	1	1	2	8	16
0	1	0	1	1	3	8	24
0	1	1	1	1	4	8	32
1	0	0	1	1	8	8	64
Other than above					Setting prohibited		

Note For details about the PGAxOSR2 to PGAxOSR0 bits, refer to **16.5.4 (7) Input multiplexer x (x = 0 to 3) setting register 0 (PGAxCTL0)**.

(2) Input multiplexer x (x = 0 to 3) setting register 1 (PGAxCTL1)

This register is used to adjust the offset voltage for each input multiplexer channel.

The offset voltage dOFR (input-referred D/A converter output voltage for adjusting the offset voltage) is calculated from the following formula.

dOFR (mV) = (-175 + 350/32 x m)/G_{SET01}

(m = 1 to 31: value set in the PGAxCTL1 register)

The PGAxCTL1 register can be set by an 8-bit memory manipulation instruction.

Reset signal generation sets this register to 10H.

Figure 16 - 10 Format of Input Multiplexer x (x = 0 to 3) Setting Register 1 (PGAxCTL1)

Address: F045BH (PGA0CTL1), F045FH (PGA1CTL1), F0463H (PGA2CTL1) After reset: 10H R/W

Symbol	7	6	5	4	3	2	1	0
PGAxCTL1	PGAxSEL Note	0	0	PGAxOFS4	PGAxOFS3	PGAxOFS2	PGAxOFS1	PGAxOFS0

Address: F0467H (PGA3CTL1) After reset: 10H R/W

Symbol	7	6	5	4	3	2	1	0
PGA3CTL1	PGA3SEL1 Note	PGA3SEL0 Note	0	PGA3OFS4	PGA3OFS3	PGA3OFS2	PGA3OFS1	PGA3OFS0

PGAxOFS4	PGAxOFS3	PGAxOFS2	PGAxOFS1	PGAxOFS0	dOFR
0	0	0	0	0	Setting prohibited
0	0	0	0	1	−164.06/G_{SET01}
0	0	0	1	0	−153.13/G_{SET01}
...	...	...	...	...	...
1	0	0	0	0	0
...	...	...	...	...	...
1	1	1	0	1	+142.19/G_{SET01}
1	1	1	1	0	+153.13/G_{SET01}
1	1	1	1	1	+164.06/G_{SET01}

Note For details about the PGAxSEL bits, refer to **16.3.3 (1) Input multiplexer 0 setting register 1 (PGA0CTL1)** or **(2) Input multiplexer 3 setting register 1 (PGA3CTL1)**.

Caution **Be sure to clear bits 5 and 6 in the PGAxCTL1 register (x = 0, 1, or 2) to "0".**
Be sure to clear bit 5 in the PGA3CTL1 register to "0".

(3) Disconnection detection setting register (PGABOD)

This register is used to specify whether to enable detection of a disconnection of signal lines connected to PGA0xP or PGA0xN (x = 0, 3).

When the PGABOD register is set for detection of the disconnection state, 1 μA (typ.) from the current supply DAC is connected for input to the PGA0. When a signal line is disconnected or the power supply capacity falls below 1 μA (typ.), the result of A/D conversion is clipped.

The PGABOD register can be set by an 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 16 - 11 Format of Disconnection Detection Setting Register (PGABOD)

Address: F046EH After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
PGABOD	0	0	0	0	0	0	0	PGABOD0

PGABOD0	Control of disconnection detection
0	Normal operation
1	State of disconnection detection

Caution Be sure to clear bits 1 to 7 to "0".

16.5 24-bit ΔΣ A/D Converter

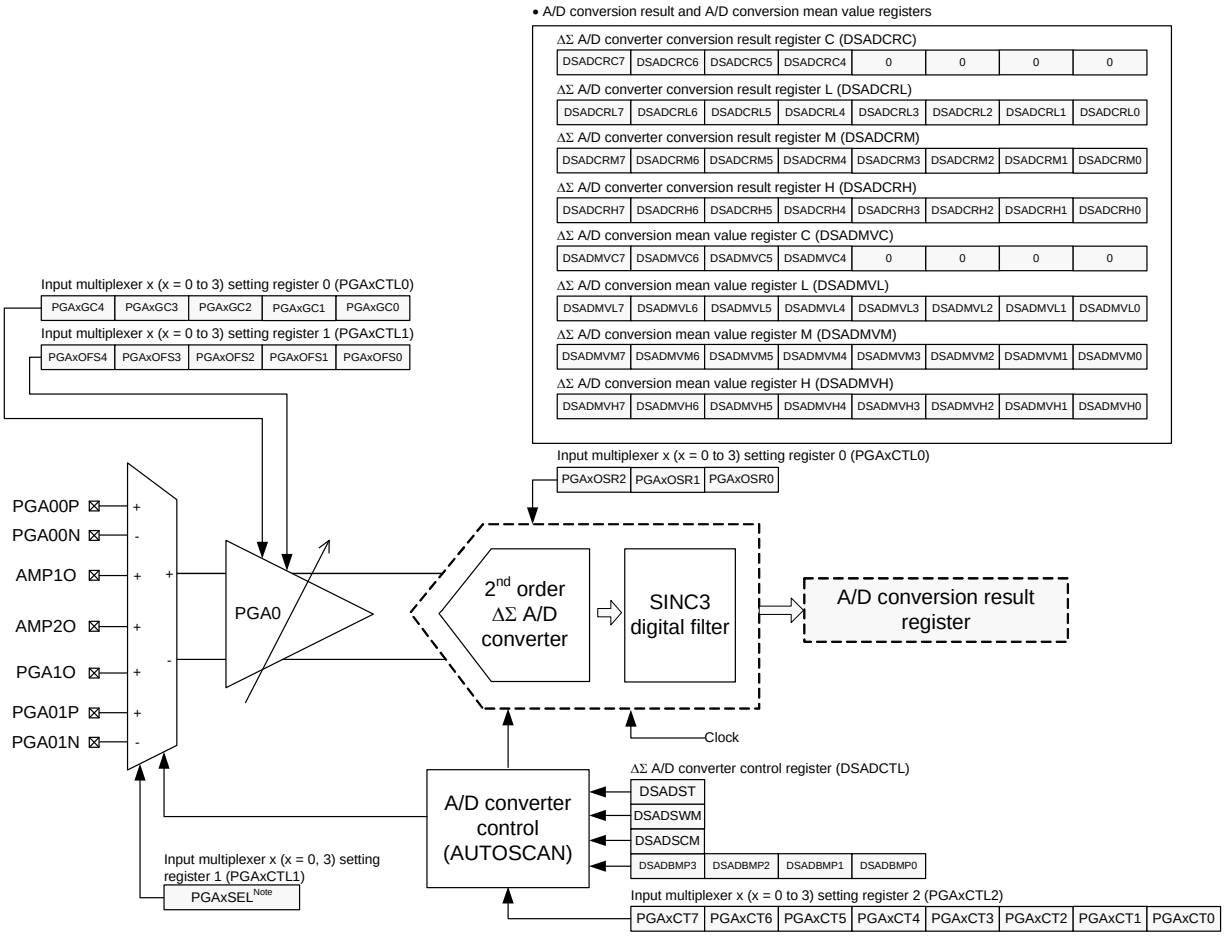
16.5.1 Overview of 24-bit ΔΣ A/D converter

The RL78/H1D incorporates a 24-bit ΔΣ A/D converter. The signal from an input multiplexer (there are 5 channels in total) is input to the 24-bit ΔΣ A/D converter via the programmable gain instrumentation amplifier (PGA0). The A/D conversion result is filtered by the SINC3 digital filter, and is then stored in an output register. A/D conversion is performed based on the clock generated in the high-speed on-chip oscillator (HOCO) (sampling frequency = 1 MHz (TYP.)). The high-speed system clock can also be used. A/D conversion is performed based on a built-in sequencer called AUTOSCAN. The data rate (frequency with which each A/D conversion result is output) can be specified for each channel.

16.5.2 Configuration of 24-bit ΔΣ A/D converter

Figure 16 - 12 shows the block diagram of the 24-bit ΔΣ A/D converter.

Figure 16 - 12 Block Diagram of 24-bit ΔΣ A/D Converter



Note This is the case for input multiplexer 0. In the case of input multiplexer 3, the setting is made by the PGA3SEL0 and PGA3SEL1 bits.

16.5.3 Voltage input to the 24-bit ΔΣ A/D converter and A/D conversion result

This section describes the relationship between the voltage input to the 24-bit ΔΣ A/D converter and A/D conversion result. The figure and table below show the A/D conversion result when the full-scale range of voltage can be input to the A/D converter.

Figure 16 - 13 Voltage Input to the 24-bit ΔΣ A/D Converter and A/D Conversion Result

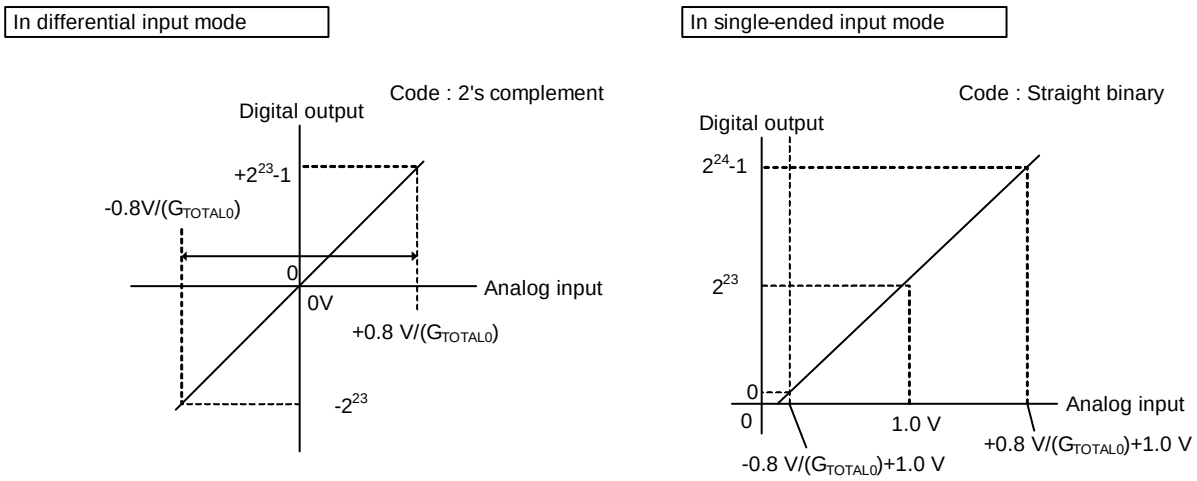


Table 16 - 2 Voltage Input to the 24-bit ΔΣ A/D Converter and A/D Conversion Result

Differential input mode		Single-ended input mode	
Voltage input to ΔΣ A/D converter	A/D conversion result (2's complement)	Voltage input to ΔΣ A/D converter	A/D conversion result (straight binary)
+0.8 V/(G_{TOTAL0})	2^{23}-1	+0.8 V/(G_{TOTAL0}) + 1.0 V	2^{24} − 1
0 V	0	1.0 V	2^{23}
−0.8 V/(G_{TOTAL0})	-2^{23}	−0.8 V/(G_{TOTAL0}) + 1.0 V	0

The results in Table 16 - 2 are calculated from the following formulas.

- In differential input mode

  Voltage input to ΔΣ A/D converter = (1.6 V/G_{TOTAL0}) x (ADCDATA1/2^{24})

  ADCDATA1: 2's complement of 24-bit result of A/D conversion (the higher-order 8 bits in DSADCRH, the middle-order 8 bits in DSADCRM, and the lower-order 8 bits in DSADCRL)

- In single-ended input mode

  Voltage input to ΔΣ A/D converter = (1.6 V/G_{TOTAL0}) x (ADCDATA2/2^{24}– 0.5) + 1.0 V

  ADCDATA2: Straight binary value of 24-bit result of A/D conversion (the higher-order 8 bits in DSADCRH, the middle-order 8 bits in DSADCRM, and the lower-order 8 bits in DSADCRL)

16.5.4 Registers controlling the 24-bit ΔΣ A/D converter

The following registers are used to control the 24-bit ΔΣ A/D converter.

- Peripheral enable register (PER1)
- Analog front-end power supply selection register (AFEPWS)
- Analog front-end power supply detection register (AFEPWD)
- Analog front-end clock selection register (AFECKS)
- ΔΣ A/D converter mode register (DSADMR)
- ΔΣ A/D converter control register (DSADCTL)
- Input multiplexer x (x = 0 to 3) setting register 0 (PGAxCTL0)
- Input multiplexer x (x = 0 to 3) setting register 2 (PGAxCTL2)
- Input multiplexer x (x = 0 to 3) setting register 3 (PGAxCTL3)
- ΔΣ A/D converter conversion result register C (DSADCRC)
- ΔΣ A/D converter conversion result register L (DSADCRL)
- ΔΣ A/D converter conversion result register M (DSADCRM)
- ΔΣ A/D converter conversion result register H (DSADCRH)
- ΔΣ A/D converter mean value register C (DSADMVC)
- ΔΣ A/D converter mean value register L (DSADMVL)
- ΔΣ A/D converter mean value register M (DSADMVM)
- ΔΣ A/D converter mean value register H (DSADMVH)
- ΔΣ A/D converter conversion result register 0 (DSADCR0)
- ΔΣ A/D converter conversion result register 1 (DSADCR1)
- ΔΣ A/D converter mean value register 0 (DSADMV0)
- ΔΣ A/D converter mean value register 1 (DSADMV1)

(1) Peripheral enable register 1 (PER1)

This register is used to enable or disable supplying the clock to the peripheral hardware. Clock supply to the hardware that is not used is also stopped so as to decrease the power consumption and noise.

The PER1 register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 16 - 14 Format of Peripheral Enable Register 1 (PER1)

Address: F007AH After reset: 00H R/W

Symbol	<7>	6	5	<4>	<3>	<2>	<1>	<0>
PER1	TMKAEN	0	0	AMPEN Note	DTCEN	PGAEN Note	AFEEN Note	DACEN Note

PGAEN Note	Control of input clock supplied to PGA0 and 24-bit ΔΣ A/D converter
0	Stops input clock supply. • SFRs used by PGA0 and the 24-bit ΔΣ A/D converter cannot be written. • PGA0 and the 24-bit ΔΣ A/D converter are in the reset status.
1	Enables input clock supply. • SFRs used by PGA0 and the 24-bit ΔΣ A/D converter can be read and written.

Note R5F11N and R5F11P only.

Caution Be sure to clear following bits to "0".
R5F11N and R5F11P: Bits 5 and 6
R5F11R: Bits 0 to 2, 4 to 6

(2) Analog front-end power supply selection register (AFEPWS)

The AFEPWS register is used to control the power supplied to the programmable gain instrumentation amplifier (PGA0), sensor reference voltage source (SBIAS), and AFE reference voltage (ABGR) blocks.

The AFEPWS register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 16 - 15 Format of Analog Front-End Power Supply Selection Register (AFEPWS)

Address: F0440H After reset: 00H R/W

Symbol	<7>	<6>	5	<4>	3	<2>	1	<0>
AFEPWS	DAC1PON	DAC0PON	0	AMP0PON	0	PGAPON	0	AFEPON

PGAPON	Control of power supplied to programmable gain instrumentation amplifier (PGA0) and sensor reference voltage source (SBIAS) blocks
0	Power-off (default)
1	Power-on

AFEPON	Control of power supplied to AFE reference voltage (ABGR) block
0	Power-off (default)
1	Power-on

Caution Be sure to clear bits 1, 3 and 5 to "0".
For the setting of bits 4, 6, and 7, refer to 15.3.2 Analog front-end power supply selection register (AFEPWS).

(3) Analog front-end power supply detection register (AFEPWD)

The AFEPWD register is a status register that shows the status of the power supplied to the programmable gain instrumentation amplifier (PGA0), sensor reference voltage source (SBIAS), and AFE reference voltage (ABGR) blocks.

The AFEPWD register can be read by a 1-bit or an 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 16 - 16 Format of Analog Front-End Power Supply Detection Register (AFEPWD)

Address: F0441H After reset: 00H R

Symbol	7	6	5	4	3	<2>	1	<0>
AFEPWD	0	0	0	0	0	PGASTAT	0	AFESTAT

PGASTAT	Status of power supplied to programmable gain instrumentation amplifier (PGA0) and sensor reference voltage source (SBIAS) blocks
0	Off or stabilizing
1	Stabilized

AFESTAT	Status of power supplied to AFE reference voltage (ABGR) block
0	Off or stabilizing
1	Stabilized

(4) Analog front-end clock selection register (AFECKS)

This register is used to generate the AFE operating clock (f_{DSADCK}) that is only used by the ΔΣ A/D converter based on the CPU/peripheral hardware clock (f_{CLK}). The setting that makes the frequency of the AFE operating clock (f_{DSADCK}) to be 4 MHz must be specified by using the AFECKS3 to AFECKS0 bits, according to the base clock frequency. When the ΔΣ A/D converter is used in low power mode, the specified frequency of the AFE operating clock (f_{DSADCK}) is divided by 8 by using an internal frequency divider.

The AFECKS register can be set by an 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 16 - 17 Format of Analog Front-End Clock Selection Register (AFECKS)

Address: F0442H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
AFECKS	0	0	0	0	AFECKS3	AFECKS2	AFECKS1	AFECKS0

AFECKS3	AFECKS2	AFECKS1	AFECKS0	Selection of AFE operating clock (f_{DSADCK})
0	×	×	×	Stop the clock output (default)
1	0	0	0	f_{CLK} (undivided)
1	0	0	1	f_{CLK}/2 (divided by 2)
1	0	1	0	f_{CLK}/3 (divided by 3)
1	0	1	1	f_{CLK}/4 (divided by 4)
1	1	0	0	f_{CLK}/5 (divided by 5)
1	1	0	1	f_{CLK}/6 (divided by 6)
1	1	1	×	f_{CLK}/8 (divided by 8)

Caution **Be sure to clear bits 4 to 7 to “0”.**

Remark ×: Don't care

(5) ΔΣ A/D converter mode register (DSADMR)

This register is used to select the trigger signal for the ΔΣ A/D converter to start operating and its operating mode.

The DSADMR register can be set by an 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 16 - 18 Format of ΔΣ A/D Converter Mode Register (DSADMR)

Address: F0458H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
DSADMR	DSADTMD	DSADLPM	0	0	0	0	0	0

DSADTMD	Selection of A/D conversion trigger signal
0	Software trigger (Conversion starts when the corresponding SFR is written; default)
1	Hardware trigger (Conversion starts when an event signal selected for the ELC is received)

DSADLPM	Selection of A/D conversion mode
0	Normal mode Frequency of AFE operating clock (f_{DSADCK}) is 4 MHz (default).
1	Low power mode Frequency of AFE operating clock (f_{DSADCK}) / 8 is 500 kHz (1/8 the frequency in normal mode).

Caution 1. The setting to specify the frequency of AFE operating clock (f_{DSADCK}) to be 4 MHz must be specified by using the AFECKS3 to AFECKS0 bits in advance. For details, refer to (4) Analog front-end clock selection register (AFECKS).

Caution 2. Be sure to clear bits 0 to 5 to "0".

(6) ΔΣ A/D converter control register (DSADCTL)

This register is used to start and stop ΔΣ A/D converter operation. This register is also used to enable or disable A/D conversion of input signals, for each input multiplexer channel. For details, refer to **16.5.5 Control of ΔΣ A/D converter (AUTOSCAN)**.

The DSADCTL register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 16 - 19 Format of ΔΣ A/D Converter Control Register (DSADCTL)

Address: F0459H After reset: 00H R/W

Symbol	<7>	6	5	4	3	2	1	0
DSADCTL	DSADST	DSADSWM	DSADSCM	0	DSADBMP3	DSADBMP2	DSADBMP1	DSADBMP0

DSADST	Control of A/D conversion (based on AUTOSCAN)
0	Stop A/D conversion.
1	Start A/D conversion.

DSADSWM	Selection of stabilization wait time for starting the A/D conversion or switching the channel T = M/fin = OSR/fin = OSR [usec]
0	128 usec + 3T
1	4T (OSR = 128, 256, 512, 1024, or 2048) or 5T (OSR = 64)

DSADSCM	Selection of the autoscan mode
0	Continuous scan mode
1	Single scan mode

DSADBMPn	Signal from input multiplexer n (n = 0 to 3)
0	Enable A/D conversion.
1	Disable A/D conversion (skip A/D conversion of the signal on the channel).

Caution 1. Following the start of A/D conversion (immediately after the DSADST bit is set to 1), up to a further 1 μsec may be required in addition to the stabilization wait time (settling time) set by DSADSWM bit.

Caution 2. When the hardware trigger is selected by the DSADTMD bit of the DSADMR register, the setting of the DSADSCM bit is ignored and scanning is fixed to single-scan mode.

Caution 3. When the A/D conversion of the signal from the input multiplexer 0 is enabled (DSADBMP0 = 0), be sure to clear bits PGA1CS0, AMP1PS2, and AMP2PS2 of the PGA1S, AMP1S, and AMP2S registers in the amplifier unit to "0".

Caution 4. When the A/D conversion of the signal from the input multiplexer 3 (external) is enabled (DSADBMP3 = 0, PGA3SEL0 = 1), be sure to clear PGA1CS1 bit of the PGA1S register in the amplifier unit to "0".

Caution 5. Be sure to clear bit 4 to "0".

(7) Input multiplexer x (x = 0 to 3) setting register 0 (PGAxCTL0)

This register is used to specify the data rate (frequency with which each A/D conversion result is output) for input multiplexer x (x = 0 to 3). For details, refer to **16.5.5 Control of ΔΣ A/D converter (AUTOSCAN)**.

The PGAxCTL0 register can be set by an 8-bit memory manipulation instruction.

Reset signal generation sets this register to 40H.

Figure 16 - 20 Format of Input Multiplexer x (x = 0 to 3) Setting Register 0 (PGAxCTL0)

Address: F045AH (PGA0CTL0), F045EH (PGA1CTL0), F0462H (PGA2CTL0), F0466H (PGA3CTL0) After reset: 40H R/W

Symbol	7	6	5	4	3	2	1	0
PGAxCTL0	PGAxOSR2	PGAxOSR1	PGAxOSR0	PGAxGC4Note	PGAxGC3Note	PGAxGC2Note	PGAxGC1Note	PGAxGC0Note

PGAxOSR2	PGAxOSR1	PGAxOSR0	OSR (oversampling ratio)
0	0	0	64
0	0	1	128
0	1	0	256
0	1	1	512
1	0	0	1024
1	0	1	2048
Other than above			Setting prohibited

Note For details about the PGAxGC4 to PGAxGC0 bits of the PGAxCTL0 register (x = 0 to 3), refer to **16.4.6 (1) Input multiplexer x (x = 0 to 3) setting register 0 (PGAxCTL0)**.

(8) Input multiplexer x (x = 0 to 3) setting register 2 (PGAxCTL2)

This register is used to specify the number of A/D conversions per AUTOSCAN cycle for input multiplexer x (x = 0 to 3). The number of A/D conversions *N* can be expressed by using the formula below. For details, refer to **16.5.5 Control of ΔΣ A/D converter (AUTOSCAN)**.

The PGAxCTL2 register can be set by an 8-bit memory manipulation instruction.

Reset signal generation sets this register to 01H.

In the case of PGAxCTM = 0, $N = 32 \times (2^n - 1) + m \times 2^n$

In the case of PGAxCTM = 1, $N = 32 \times n + m$

(m and n are the values set to the PGAxCTL2 register)

Figure 16 - 21 Format of Input Multiplexer x (x = 0 to 3) Setting Register 2 (PGAxCTL2)

Address: F045CH (PGA0CTL2), F0460H (PGA1CTL2), F0464H (PGA2CTL2), F0468H (PGA3CTL2) After reset: 01H R/W

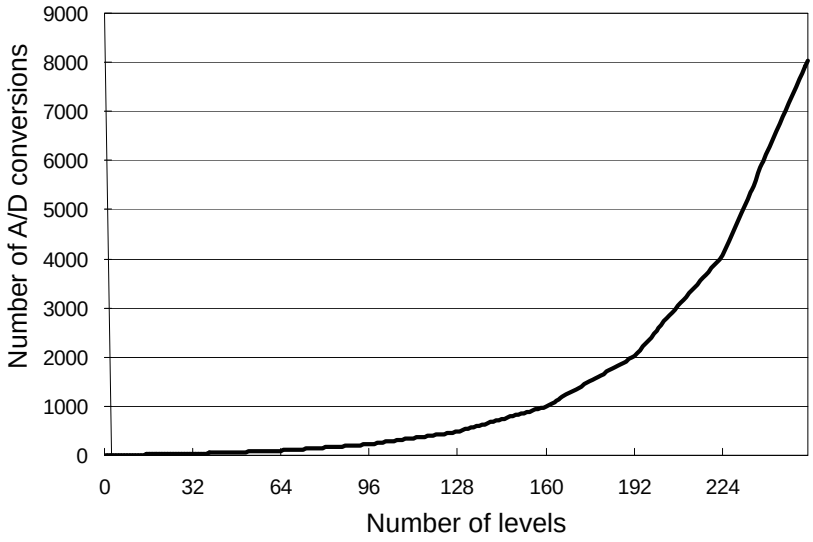
Symbol	7	6	5	4	3	2	1	0
PGAxCTL2	PGAxCT7	PGAxCT6	PGAxCT5	PGAxCT4	PGAxCT3	PGAxCT2	PGAxCT1	PGAxCT0

PGAxCT4	PGAxCT3	PGAxCT2	PGAxCT1	PGAxCT0	m
0	0	0	0	0	0
0	0	0	0	1	1
0	0	0	1	0	2
...	...	...	...	...	...
1	0	0	0	0	16
...	...	...	...	...	...
1	1	1	0	1	29
1	1	1	1	0	30
1	1	1	1	1	31

PGAxCT7	PGAxCT6	PGAxCT5	n
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

Up to 256 levels can be selected by combining m and n. The following shows the correlation of the number of levels (register value) and the number of A/D conversions.

Figure 16 - 22 Correlation of the Number of Levels (Register Value) and the Number of A/D Conversions



(9) Input multiplexer x (x = 0 to 3) setting register 3 (PGAxCTL3)

This register is used to specify the mode for specifying the number of A/D conversions per AUTOSCAN cycle for input multiplexer x (x = 0 to 3) and how A/D conversion results are averaged.

The PGAxCTL3 register can be set by an 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 16 - 23 Format of Input Multiplexer x (x = 0 to 3) Setting Register 3 (PGAxCTL3)

Address: F045DH (PGA0CTL3), F0461H (PGA1CTL3), F0465H (PGA2CTL3), F0469H (PGA3CTL3) After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
PGAxCTL3	PGAxCTM	0	0	0	PGAxAVE3	PGAxAVE2	PGAxAVE1	PGAxAVE0

PGAxCTM	Selection of the mode for specifying the number of A/D conversions
0	Specify 1 to 8,032 times by using the value set in the PGAxCTL2 register (default)
1	Specify 1 to 255 times linearly by using the value set in the PGAxCTL2 register

PGAxAVE3	PGAxAVE2	Selection of averaging processing
0	0	Do not average the A/D conversion results (default)
0	1	
1	0	Average the A/D conversion results and generates INTDSAD each time an A/D conversion occurs.
1	1	Average the A/D conversion results and generates INTDSAD each time the mean value (N consecutive results of A/D conversion) is output.

PGAxAVE1	PGAxAVE0	Selection of N (the number of data units to be averaged)
0	0	8
0	1	16
1	0	32
1	1	64

Caution Be sure to clear bits 4 to 6 to “0”.

(10) ΔΣ A/D converter conversion result register C (DSADCRC)

This is a read-only register that is used to check the number of the channel corresponding to the A/D conversion result. You can check the state of the result of A/D conversion and the number of the input multiplexer channel corresponding to the conversion result. For details, refer to **16.5.5 Control of ΔΣ A/D converter (AUTOSCAN)**.

The DSADCRC register can be read by using an 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 16 - 24 Format of ΔΣ A/D Converter Conversion Result Register C (DSADCRC)

Address: F0450H After reset: 00H R

Symbol	7	6	5	4	3	2	1	0
DSADCRC	DSADCRC7	DSADCRC6	DSADCRC5	DSADCRC4	0	0	0	0

DSADCRC7	DSADCRC6	DSADCRC5	Number of the channel corresponding to the A/D conversion result
0	0	0	Invalid
0	0	1	Input multiplexer 0 (PGA00P/PGA00N)
0	1	0	Input multiplexer 1 (AMP1O)
0	1	1	Input multiplexer 2 (AMP2O)
1	0	0	Input multiplexer 3 (PGA1O or PGA01P/PGA01N)
1	0	1	Invalid
1	1	0	Invalid
1	1	1	Invalid

DSADCRC4	Flag that indicates the state of the result of A/D conversion
0	Normal state (within range)
1	Clipping has occurred.Note

Note The result of A/D conversion is clipped in the range listed in Table 16 - 2.

(11) ΔΣ A/D converter conversion result register L (DSADCRL)

This is a read-only register that is used to check the A/D conversion result. This register stores the lower 8 bits of the 24-bit A/D conversion result. For details, refer to **16.5.5 Control of ΔΣ A/D converter (AUTOSCAN)**.

The DSADCRL register can be read by using an 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 16 - 25 Format of ΔΣ A/D Converter Conversion Result Register L (DSADCRL)

Address: F0451H After reset: 00H R

Symbol	7	6	5	4	3	2	1	0
DSADCRL	DSADCRL7	DSADCRL6	DSADCRL5	DSADCRL4	DSADCRL3	DSADCRL2	DSADCRL1	DSADCRL0

(12) ΔΣ A/D converter conversion result register M (DSADCRM)

This is a read-only register that is used to check the A/D conversion result. This register stores the middle 8 bits of the 24-bit A/D conversion result. For details, refer to **16.5.5 Control of ΔΣ A/D converter (AUTOSCAN)**.

The DSADCRM register can be read by using an 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 16 - 26 Format of ΔΣ A/D Converter Conversion Result Register M (DSADCRM)

Address: F0452H After reset: 00H R

Symbol	7	6	5	4	3	2	1	0
DSADCRM	DSADCRM7	DSADCRM6	DSADCRM5	DSADCRM4	DSADCRM3	DSADCRM2	DSADCRM1	DSADCRM0

(13) ΔΣ A/D converter conversion result register H (DSADCRH)

This is a read-only register that is used to check the A/D conversion result. This register stores the higher 8 bits of the 24-bit A/D conversion result. For details, refer to **16.5.5 Control of ΔΣ A/D converter (AUTOSCAN)**.

The DSADCRH register can be read by using an 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 16 - 27 Format of ΔΣ A/D Converter Conversion Result Register H (DSADCRH)

Address: F0453H After reset: 00H R

Symbol	7	6	5	4	3	2	1	0
DSADCRH	DSADCRH7	DSADCRH6	DSADCRH5	DSADCRH4	DSADCRH3	DSADCRH2	DSADCRH1	DSADCRH0

(14) ΔΣ A/D converter mean value register C (DSADMVC)

This is a read-only register that is used to check the number of the channel corresponding to the mean value. You can check the state of the mean value and the number of the input multiplexer channel corresponding to the mean value. For details, refer to **16.5.5 Control of ΔΣ A/D converter (AUTOSCAN)**.

The DSADMVC register can be read by using an 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 16 - 28 Format of ΔΣ A/D Converter Mean Value Register C (DSADMVC)

Address: F0454H After reset: 00H R

Symbol	7	6	5	4	3	2	1	0
DSADMVC	DSADMVC7	DSADMVC6	DSADMVC5	DSADMVC4	0	0	0	0

DSADMVC7	DSADMVC6	DSADMVC5	Number of the channel corresponding to the mean value
0	0	0	Invalid
0	0	1	Input multiplexer 0 (PGA00P/PGA00N)
0	1	0	Input multiplexer 1 (AMP1O)
0	1	1	Input multiplexer 2 (AMP2O)
1	0	0	Input multiplexer 3 (PGA1O or PGA01P/PGA01N)
1	0	1	Invalid
1	1	0	Invalid
1	1	1	Invalid

DSADMVC4	Flag that indicates the state of the mean value
0	Normal state (within range)
1	Clipping has occurred.[Note]

Note DSADMVC4 being 1 indicates that at least one result of A/D conversion used for averaging was clipped in the range listed in Table 16 - 2. The mean value is not limited to having the maximum or minimum value.

(15) ΔΣ A/D converter mean value register L (DSADMVL)

This is a read-only register that is used to check the mean value. This register stores the lower 8 bits of the 24-bit mean value. For details, refer to **16.5.5 Control of ΔΣ A/D converter (AUTOSCAN)**.

The DSADMVL register can be read by using an 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 16 - 29 Format of ΔΣ A/D Converter Mean Value Register L (DSADMVL)

Address: F0455H After reset: 00H R

Symbol	7	6	5	4	3	2	1	0
DSADMVL	DSADMVL7	DSADMVL6	DSADMVL5	DSADMVL4	DSADMVL3	DSADMVL2	DSADMVL1	DSADMVL0

(16) ΔΣ A/D converter mean value register M (DSADMVM)

This is a read-only register that is used to check the mean value. This register stores the middle 8 bits of the 24-bit mean value. For details, refer to **16.5.5 Control of ΔΣ A/D converter (AUTOSCAN)**.

The DSADMVM register can be read by using an 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 16 - 30 Format of ΔΣ A/D Converter Mean Value Register M (DSADMVM)

Address: F0456H After reset: 00H R

Symbol	7	6	5	4	3	2	1	0
DSADMVM	DSADMVM7	DSADMVM6	DSADMVM5	DSADMVM4	DSADMVM3	DSADMVM2	DSADMVM1	DSADMVM0

(17) ΔΣ A/D converter mean value register H (DSADMVH)

This is a read-only register that is used to check the mean value. This register stores the higher 8 bits of the 24-bit mean value. For details, refer to **16.5.5 Control of ΔΣ A/D converter (AUTOSCAN)**.

The DSADMVH register can be read by using an 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 16 - 31 Format of ΔΣ A/D Converter Mean Value Register H (DSADMVH)

Address: F0457H After reset: 00H R

Symbol	7	6	5	4	3	2	1	0
DSADMVH	DSADMVH7	DSADMVH6	DSADMVH5	DSADMVH4	DSADMVH3	DSADMVH2	DSADMVH1	DSADMVH0

(18) ΔΣ A/D converter conversion result register 0 (DSADCR0)

This is a read-only register that is used to check the A/D conversion result. The DSADCRC and DSADCRL registers can be read in a batch by using a 16-bit memory manipulation instruction. For details, refer to **16.5.5 Control of ΔΣ A/D converter (AUTOSCAN)**.

The DSADCRC register can be read by using a 16-bit memory manipulation instruction.

Reset signal generation clears this register to 0000H.

Figure 16 - 32 Format of ΔΣ A/D Converter Conversion Result Register 0 (DSADCR0)

Address: F0450H After reset: 0000H R

Symbol	15	14	13	12	11	10	9	8
DSADCR0	DSADCRL							
	7	6	5	4	3	2	1	0
	DSADCRC							

(19) ΔΣ A/D converter conversion result register 1 (DSADCR1)

This is a read-only register that is used to check the A/D conversion result. The DSADCRM and DSADCRH registers can be read in a batch by using a 16-bit memory manipulation instruction. For details, refer to **16.5.5 Control of ΔΣ A/D converter (AUTOSCAN)**.

The DSADCR1 register can be read by using a 16-bit memory manipulation instruction.

Reset signal generation clears this register to 0000H.

Figure 16 - 33 Format of ΔΣ A/D Converter Conversion Result Register 1 (DSADCR1)

Address: F0452H After reset: 0000H R

Symbol	15	14	13	12	11	10	9	8
DSADCR1	DSADCRH							
	7	6	5	4	3	2	1	0
	DSADCRM							

(20) ΔΣ A/D converter mean value register 0 (DSADMV0)

This is a read-only register that is used to check the mean value. The DSADMVC and DSADMVL registers can be read in a batch by using a 16-bit memory manipulation instruction. For details, refer to **16.5.5 Control of ΔΣ A/D converter (AUTOSCAN)**.

The DSADMV0 register can be read by using a 16-bit memory manipulation instruction.

Reset signal generation clears this register to 0000H.

Figure 16 - 34 Format of ΔΣ A/D Converter Mean Value Register 0 (DSADMV0)

Address: F0454H After reset: 0000H R

Symbol	15	14	13	12	11	10	9	8
DSADMV0	DSADMVL							
	7	6	5	4	3	2	1	0
	DSADMVC							

(21) ΔΣ A/D converter mean value register 1 (DSADMV1)

This is a read-only register that is used to check the mean value. The DSADMVM and DSADMVH registers can be read in a batch by using a 16-bit memory manipulation instruction. For details, refer to **16.5.5 Control of ΔΣ A/D converter (AUTOSCAN)**.

The DSADMV1 register can be read by using a 16-bit memory manipulation instruction.

Reset signal generation clears this register to 0000H.

Figure 16 - 35 Format of ΔΣ A/D Converter Mean Value Register 1 (DSADMV1)

Address: F0456H After reset: 0000H R

Symbol	15	14	13	12	11	10	9	8
DSADMV1	DSADMVH							
	7	6	5	4	3	2	1	0
	DSADMVM							

16.5.5 Control of ΔΣ A/D converter (AUTOSCAN)

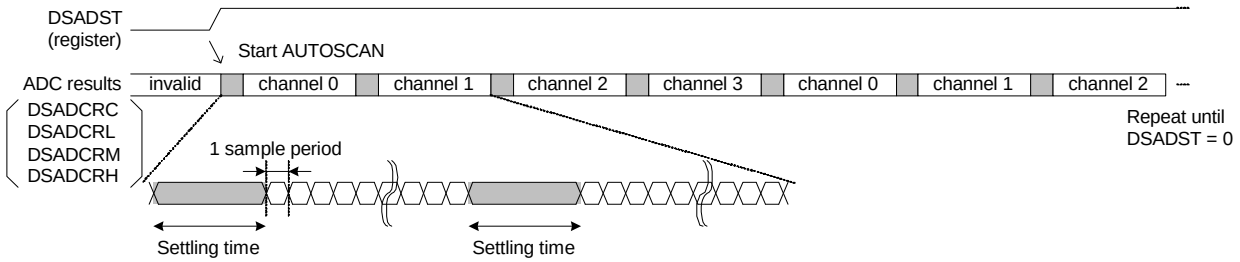
All A/D conversions is controlled based on a built-in sequencer called AUTOSCAN. When "1" is written to the DSADST bit of the DSADCTL register to enable AUTOSCAN, the signal input from each channel is A/D-converted in round-robin fashion. A/D conversion of the signal input from a specific channel can be skipped by setting the DSADBMPn bit (n = 0 to 3) of the DSADCTL register.

Use the PGAxCTy bit (x = 0 to 3, y = 0 to 7) of the PGAxCTL2 register to specify the number of times A/D conversion is to be performed in an active channel until execution shifts to the next channel. If PGAxCTy is set to 00H, it sets one-shot operation, which stops A/D conversion each time a conversion ends. Other A/D conversion parameters such as the PGA0 gain and oversampling ratio can also be configured for each channel.

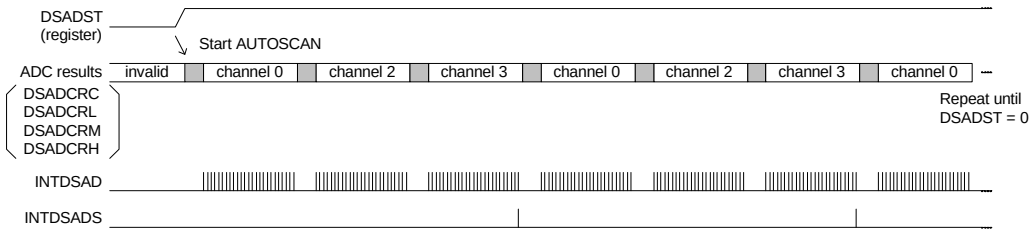
The A/D conversion result is stored in the DSADCRC, DSADCRH, DSADCRM, and DSADCRL registers.

An interrupt request (INTDSAD) is generated each time A/D conversion is completed. When averaging of the results of A/D conversion is enabled by the setting of the PGAxCTL3 register, an interrupt request (INTDSAD) can be generated each time A/D conversion is completed or each time the mean value is updated. The interrupt request (INTDSADS) is generated on completion of each cycle of AUTOSCAN from channels 0 to 3.

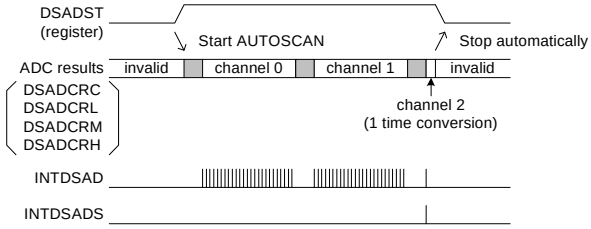
Figure 16 - 36 AUTOSCAN Sequence



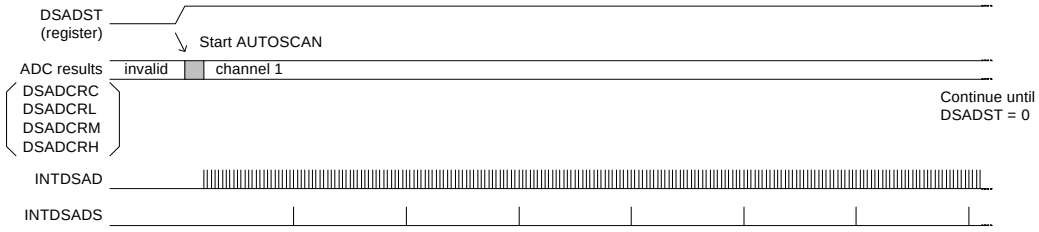
Example 1: Skipping an A/D conversion channel (DSADBMP3 to DSADBMP0 = 0010B, PGAxCTy (x = 0, 2, 3) > 0, and DASDSCM = 0)



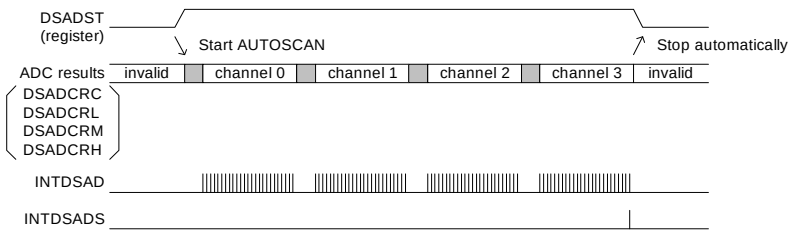
Example 2: One-shot operation (DSADBMP3 to DSADBMP0 = 1000B, PGAxCTy (x = 0 or 1) > 0, PGA2CTy = 0, and DSADSCM = 0)



Example 3: Sequential conversion on a single channel (DSADBMP3 to DSADBMP0 = 1101B, PGA1CTy > 0, and DSADSCM = 0)



Example 4: Single-scan operation (DSADBMP3 to DSADBMP0 = 0000B and DSADSCM = 1)



Remark Even for sequential conversion, an interrupt request (INTDSADS) is generated each time the number of rounds of A/D conversion set in the PGAxCTL2 register is completed.

16.5.6 Overview of digital filter

A SINC3 digital filter is used to downsample A/D conversion results. The digital filter transfer function is expressed by using the following equation. M in the equation of the transfer function represents the factor of decimation by the digital filter, which is itself determined by the OSR (oversampling ratio) set in the PGAxOSRn bit of the PGAxCTL0 register (x = 0 to 3, n = 0 to 2).

$$H(z) = \left(\frac{1}{M} \cdot \frac{1 - z^{-M}}{1 - z^{-1}} \right)^3$$

16.5.7 Configuration of digital filter

Figure 16 - 37 shows the block diagram of the digital filter. Three integrators and three differentiators are cascaded. Considering the A/D converter stabilization time, clock synchronization at the input stage in the digital filter, and a delay caused due to 3 stages of the differentiator, three times the sampling period (= 3 x 1/fout) + 128 µs is required as the settling time.

Remark The settling time is automatically generated by the built-in sequencer AUTOSCAN.

Figure 16 - 37 Block Diagram of Digital Filter

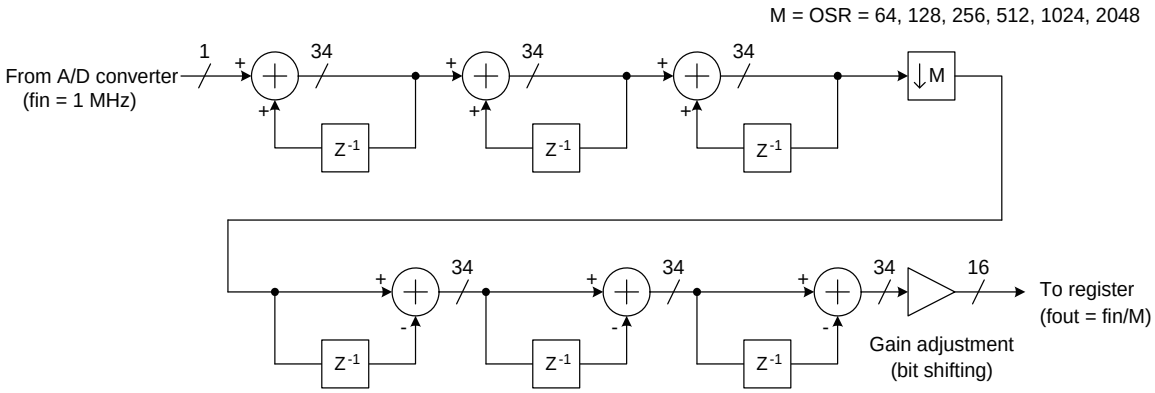
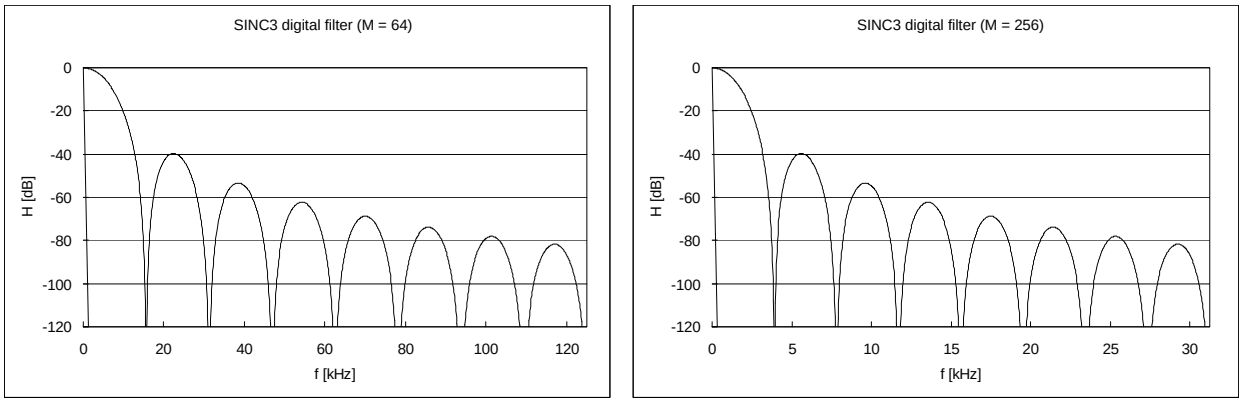


Figure 16 - 38 shows the frequency response of the digital filter.

Figure 16 - 38 SINC3 Filter Frequency Response



16.6 Procedure for Controlling 24-bit ΔΣ A/D Converter with Programmable Gain Instrumentation Amplifier

Figure 16 - 39 to **16 - 41** show the flowchart for starting the 24-bit ΔΣ A/D converter with programmable gain instrumentation amplifier, A/D conversion, and stopping the A/D converter.

Figure 16 - 39 Flowchart for Starting the 24-bit ΔΣ A/D Converter with Programmable Gain Instrumentation Amplifier

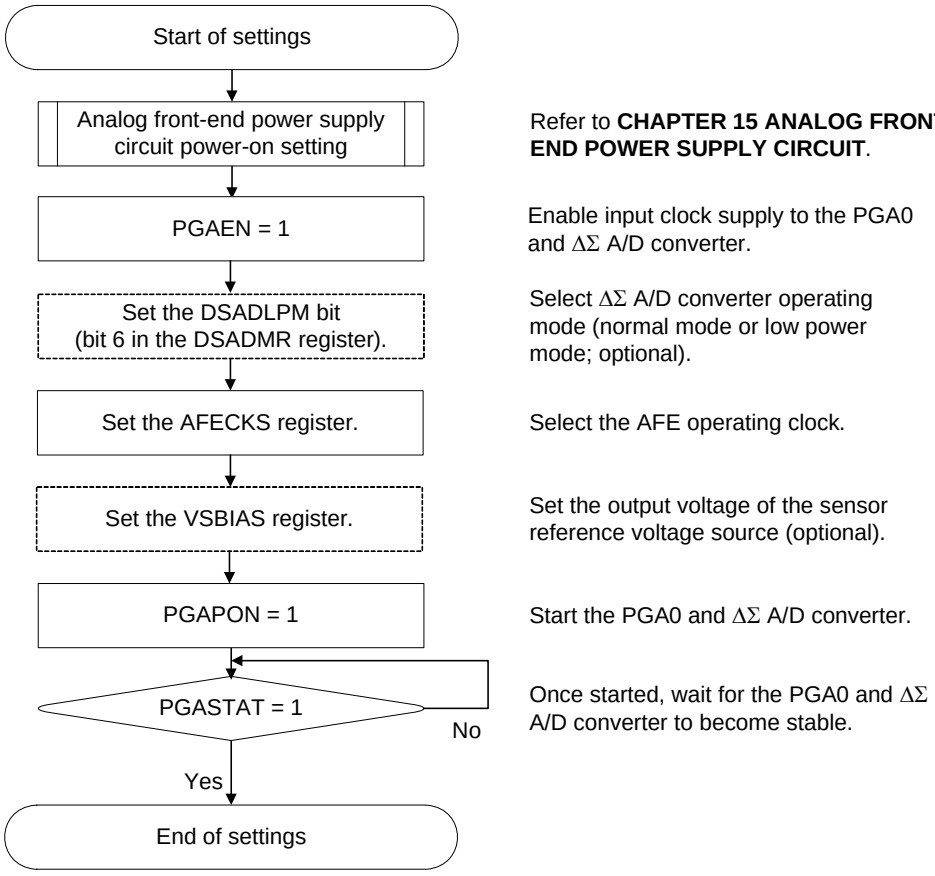


Figure 16 - 40 Flowchart for A/D Conversion by the 24-bit ΔΣ A/D Converter with Programmable Gain Instrumentation Amplifier

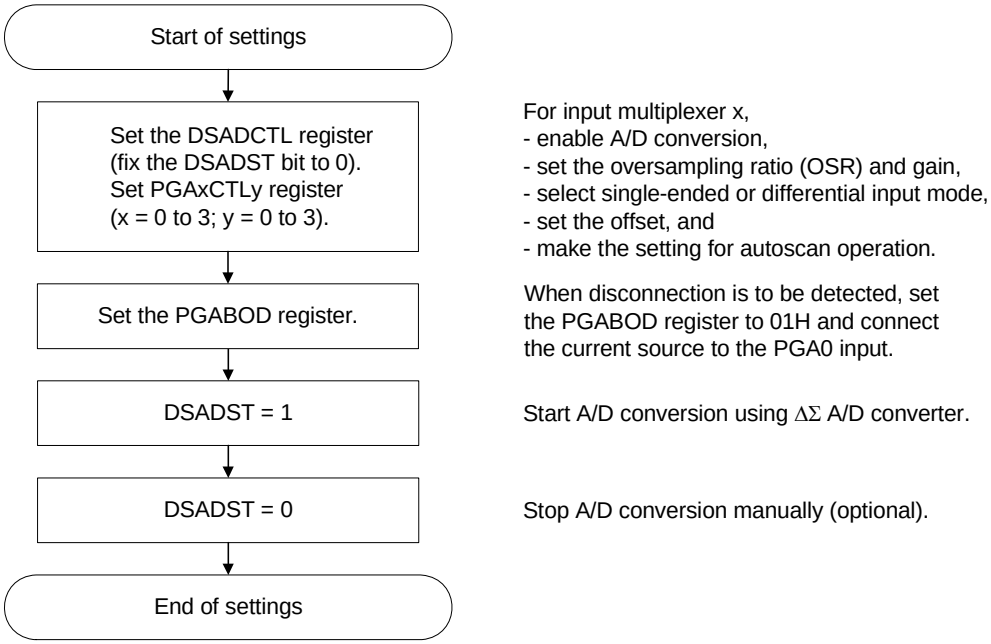
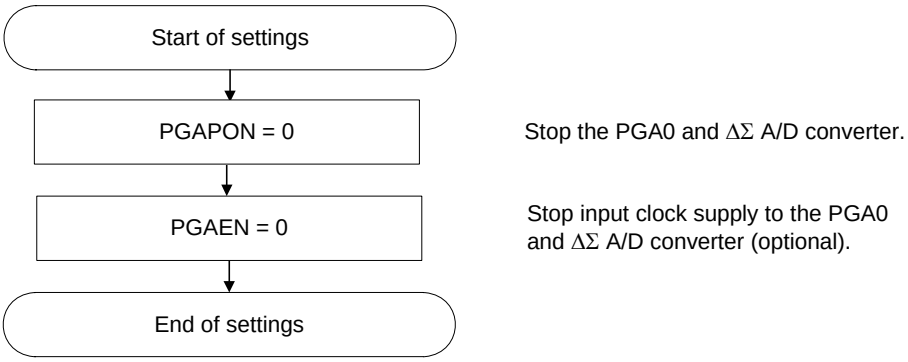


Figure 16 - 41 Flowchart for Stopping the 24-bit ΔΣ A/D Converter with Programmable Gain Instrumentation Amplifier



16.7 Cautions for the 24-bit ΔΣ A/D Converter with Programmable Gain Instrumentation Amplifier

It is recommended to change the low power mode setting (by using the DSADLPM bit) and division ratio setting (by using the AFECKS bit) before turning on on the power to the programmable gain instrumentation amplifier (PGA0) and sensor reference voltage (SBIAS) blocks (PGAPON = 0).

CHAPTER 17 AMPLIFIER UNIT (R5F11N and R5F11P only)

The number of input and output pins of the amplifier unit differs depending on the product.

Table 17 - 1 shows the pins of the amplifier unit.

Table 17 - 1 Pins of Amplifier Unit

Unit	I/O Pin	R5F11NM	R5F11NL	R5F11PL	R5F11NG
Amplifier unit 0 (Instrumentation amplifier 1: PGA1)	PGA10P, PGA10N (input)	–	√	√	√
	PGA11P, PGA11N (input)	–	–	√	√
	PGA1O (output)	–	√	√	√
Amplifier unit 1 (Operational amplifier 0: AMP0)	AMP0P (input)	√	√	√	√
	AMP0N (input)	√	√	√	√
	AMP0O (output)	√	√	√	√
Amplifier unit 2 (Operational amplifier 1: AMP1)	AMP1P (input)	–	√	√	√
	AMP1N (input)	–	√	√	√
	AMP1O (output)	–	√	√	√
Amplifier unit 3 (Operational amplifier 2: AMP2)	AMP2P (input)	–	√	√	√
	AMP2N (input)	–	√	√	√
	AMP2O (output)	–	√	√	√

The input to each amplifier unit is selected from among multiplexed AFE input 0 to 7 as listed in Table 17 - 2.
The multiplexed AFE input 0 to 7 are analog input pins. Switching the input multiplexer through register settings can change the destination for connection of each input pin.

Table 17 - 2 Multiplexed AFE Input Setting

Pin Name	Selectable Input	Settings for the connection Note	Pin Number			
			80-pin LFQFP (R5F11NM)	64-pin LFQFP (R5F11NL)	64-pin TFBGA (R5F11PL)	48-pin LFQFP (R5F11NG)
Multiplexed AFE input 0	PGA10P	PGA1CS0 = 1, DSADBMP0 = 1, AMP1PS2 = 0	–	62	F1	47
	PGA00P	PGA1CS0 = 0, DSADBMP0 = 0, AMP1PS2 = 0	78			
	AMP1P	PGA1CS0 = 0, DSADBMP0 = 1, AMP1PS2 = 1	–			
Multiplexed AFE input 1	PGA10N	PGA1CS0 = 1, DSADBMP0 = 1, AMP2PS2 = 0	–	63	G1	48
	PGA00N	PGA1CS0 = 0, DSADBMP0 = 0, AMP2PS2 = 0	79			
	AMP2P	PGA1CS0 = 0, DSADBMP0 = 1, AMP2PS2 = 1	–			
Multiplexed AFE input 2	PGA11P	PGA1CS1 = 1, DSADBMP3 = 1	–	–	C2	43
	PGA01P	PGA1CS1 = 0, DSADBMP3 = 0				
Multiplexed AFE input 3	PGA11N	PGA1CS1 = 1, DSADBMP3 = 1	–	–	D2	44
	PGA01N	PGA1CS1 = 0, DSADBMP3 = 0				
Multiplexed AFE input 4	AMP0N	AMP0NS0 = 1, AMP0PS0 = 0	76	61	E2	46
	AMP0P	AMP0NS0 = 0, AMP0PS0 = 1				
Multiplexed AFE input 5	AMP1N	AMP1NS0 = 1, AMP1PS0 = 0, AMP0PS1 = 0	–	57	B2	40
	AMP1P	AMP1NS0 = 0, AMP1PS0 = 1, AMP0PS1 = 0				
	AMP0P	AMP1NS0 = 0, AMP1PS0 = 0, AMP0PS1 = 1				
Multiplexed AFE input 6	AMP2N	AMP2NS0 = 1, AMP2PS0 = 0, AMP1PS1 = 0	–	55	B1	38
	AMP2P	AMP2NS0 = 0, AMP2PS0 = 1, AMP1PS1 = 0				
	AMP1P	AMP2NS0 = 0, AMP2PS0 = 0, AMP1PS1 = 1				
Multiplexed AFE input 7	AMP0P	AMP0NS0 = 0, AMP0PS0 = 0	77	–	–	–

Note Do not make combinations of settings other than those indicated in the table.

Remark The input to each amplifier unit is set by the bits of PGA1S, AMP0S, AMP1S, and AMP2S registers in the amplifier unit and the bits of DSADCTL register in the 24-bit ΔΣ A/D converter with programmable gain instrumentation amplifier.

17.1 Functions of Amplifier Unit

The amplifier unit can be used to amplify small analog input voltages and output the amplified voltages. This MCU has one unit of the instrumentation amplifier and three units of differential operational amplifier.

The amplifier unit have the following functions.

- The reference voltage of PGA1 is controlled by the signal from the 12-bit D/A converter.
- The signal from the 8-bit D/A converter can be selected as the positive input signal for AMP0 by switching the input multiplexer.
- The signal from the 12-bit D/A converter can be selected as the positive input signal for AMP1 and AMP2 by switching the input multiplexer.
- The signals from PGA1, AMP1, and AMP2 can be used as the input signal for the 24-bit ΔΣ A/D converter with programmable gain instrumentation amplifier.
- High-speed mode and low-power mode are supported and either mode can be selected based on trade-offs between the response speed and current consumption.
- Operation can be started by each trigger from the ELC, and operation can also be started by an ELC trigger even in STOP mode.
- Operation can be stopped by a 24-bit ΔΣ A/D scan end trigger.

17.2 Configuration of Amplifier Unit

Figure 17 - 1 to Figure 17 - 5 show block diagrams of the amplifier unit.

Figure 17 - 1 Block Diagram of Amplifier Unit

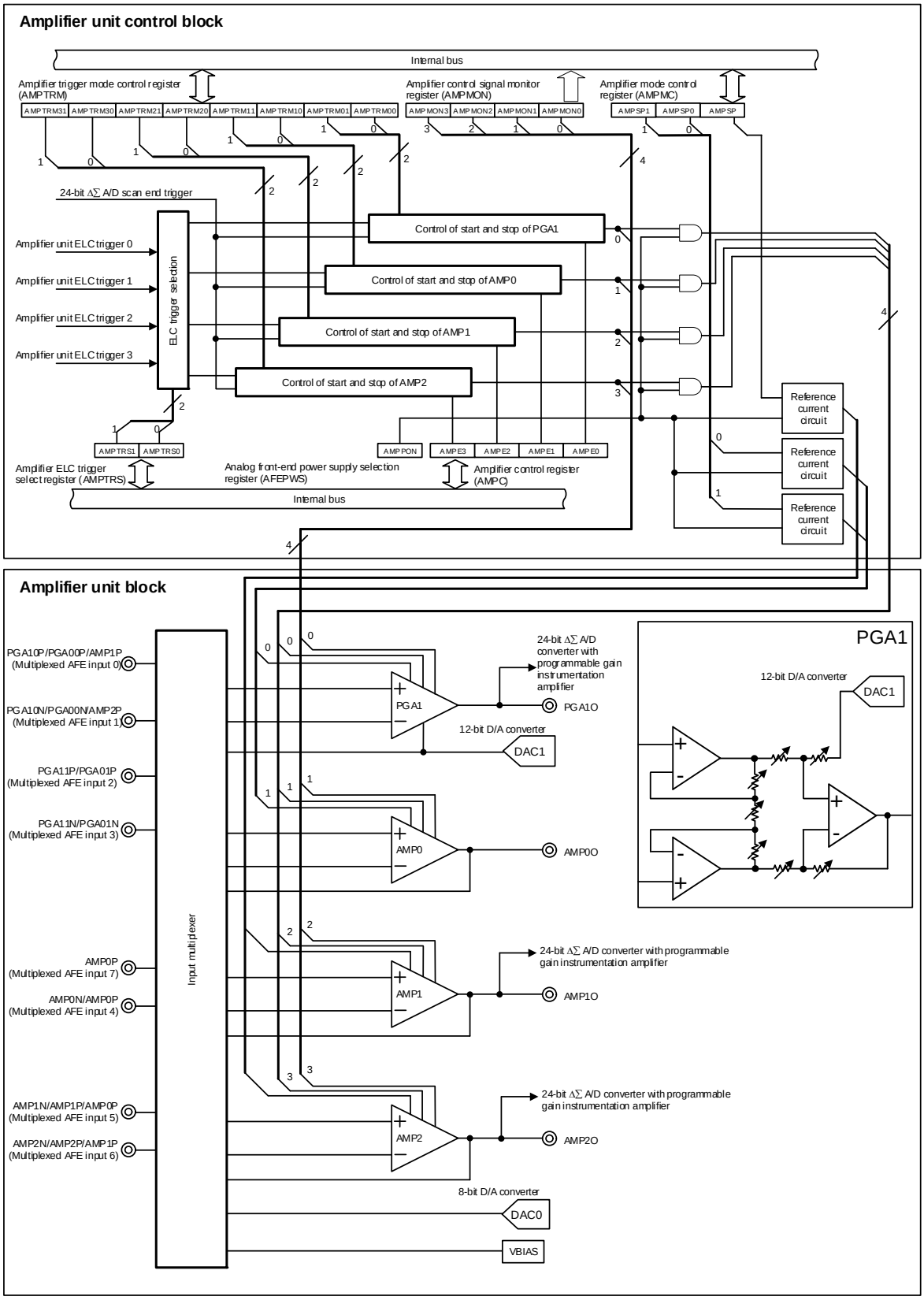
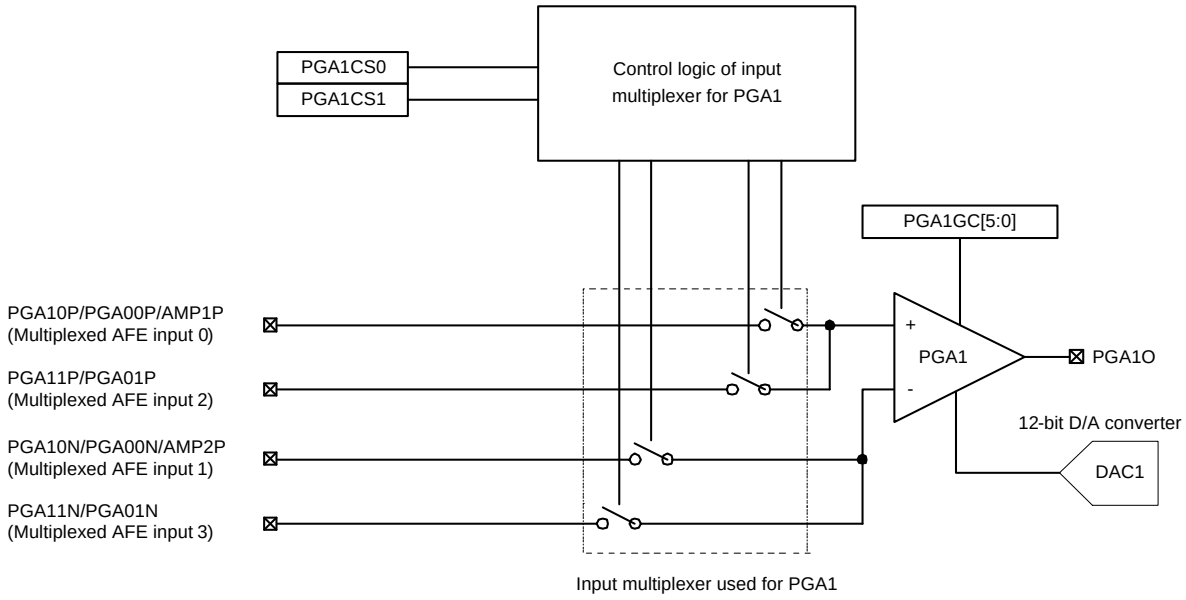


Figure 17 - 2 Block Diagram and Peripheral Circuit Diagram of PGA1



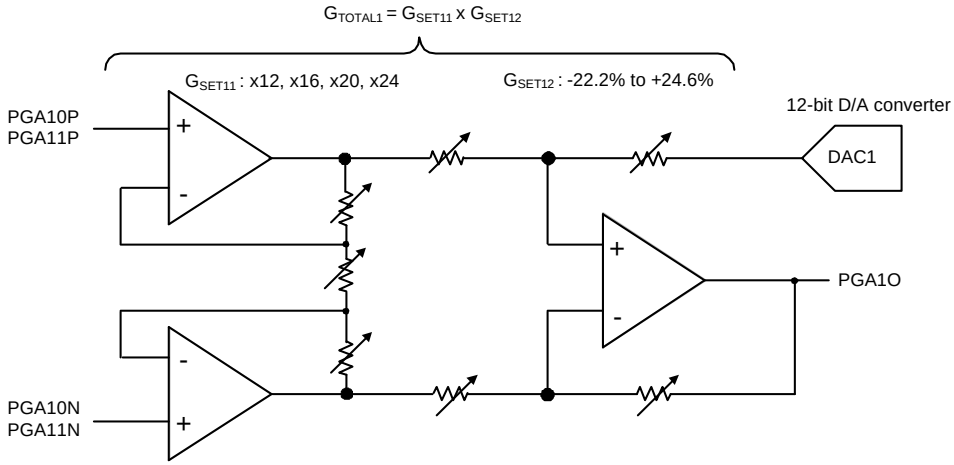
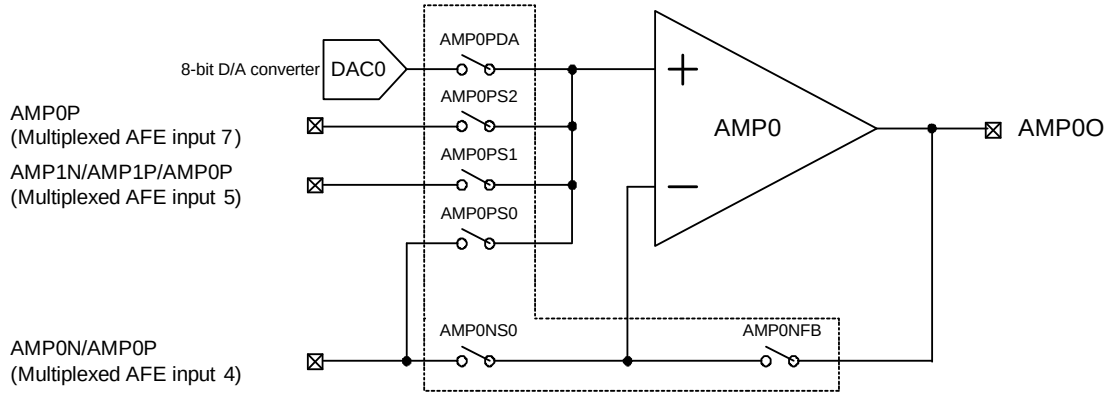
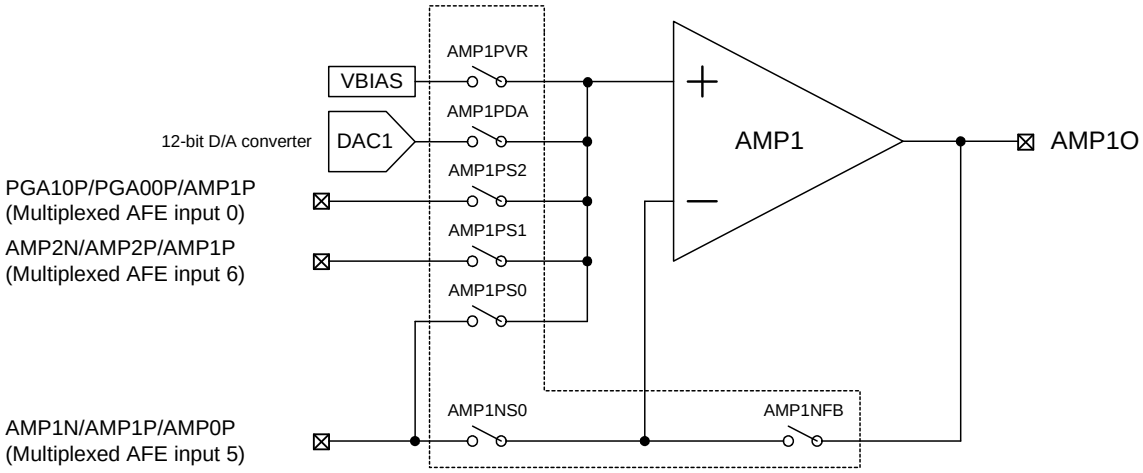


Figure 17 - 3 Block Diagram and Peripheral Circuit Diagram of AMP0



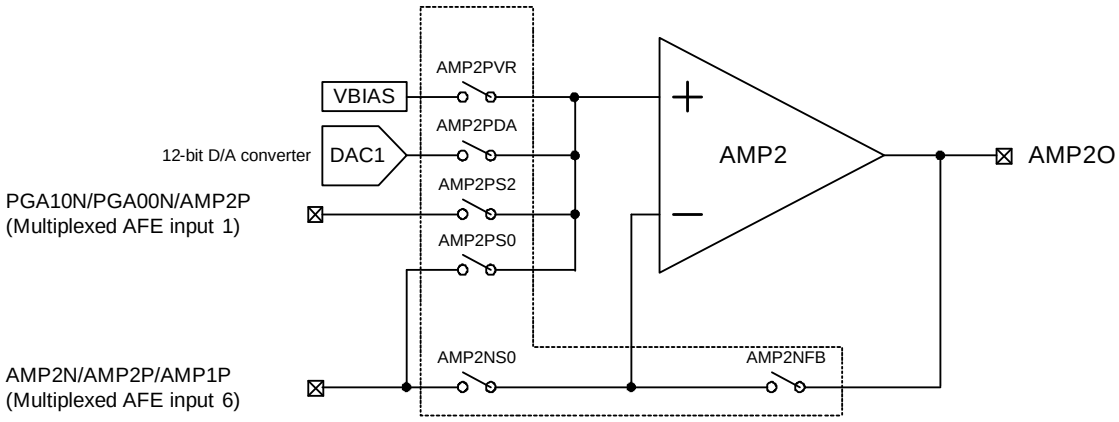
Input multiplexer used for AMP0

Figure 17 - 4 Block Diagram and Peripheral Circuit Diagram of AMP1



Input multiplexer used for AMP1

Figure 17 - 5 Block Diagram and Peripheral Circuit Diagram of AMP2



Input multiplexer used for AMP2

17.3 Registers Controlling Amplifier Unit

Table 17 - 3 lists the registers used to control the amplifier unit.

Table 17 - 3 Registers Used to Control the Amplifier Unit

Item	Configuration
Control registers	Peripheral enable register 1 (PER1)
	Analog front-end power supply selection register (AFEPWS)
	Amplifier mode control register (AMPMC)
	Amplifier trigger mode control register (AMPTRM)
	Amplifier ELC trigger select register (AMPTRS)
	Amplifier control register (AMPC)
	Amplifier control signal monitor register (AMPMON)
	Amplifier unit 0 gain setting register (PGA1GC)
	Amplifier unit 0 input select register (PGA1S)
	Amplifier unit 1 input select register (AMP0S)
	Amplifier unit 2 input select register (AMP1S)
	Amplifier unit 3 input select register (AMP2S)

17.3.1 Peripheral enable register 1 (PER1)

This register is used to enable or disable supplying the clock to the peripheral hardware. Clock supply to the hardware that is not used is also stopped so as to decrease the power consumption and noise.

The PER1 register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 17 - 6 Format of Peripheral Enable Register 1 (PER1)

Address: F007AH After reset: 00H R/W

Symbol	<7>	6	5	<4>	<3>	<2>	<1>	<0>
PER1	TMKAEN	0	0	AMPEN Note	DTCEN	PGAEN Note	AFEEN Note	DACEN Note

AMPEN Note	Control of amplifier unit input clock supply
0	Stops input clock supply. • SFRs used by the amplifier unit cannot be written. • The amplifier unit is in the reset status.
1	Enables input clock supply. • SFRs used by the amplifier unit can be read and written.

Note R5F11N and R5F11P only.

Caution 1. When setting the amplifier unit, be sure to set the AMPEN bit to 1 first. If AMPEN = 0, writing to a control register of the amplifier unit is ignored, and all read values are default values.

Caution 2. Be sure to clear following bits to “0”.
R5F11N and R5F11P: Bits 5 and 6
R5F11R: Bits 0 to 2, 4 to 6

17.3.2 Analog front-end power supply selection register (AFEPWS)

The AFEPWS register is used to control the power supplied to the amplifier unit.

The AFEPWS register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 17 - 7 Format of Analog Front-End Power Supply Selection Register (AFEPWS)

Address: F0440H After reset: 00H R/W

Symbol	<7>	<6>	5	<4>	3	<2>	1	<0>
AFEPWS	DAC1PON	DAC0PON	0	AMP0PON	0	PGAPON	0	AFEPON

AMPPON	Control of the power supplied to the amplifier unit
0	Power-off (default)
1	Power-on

Caution Be sure to clear bits 1, 3, and 5 to “0”.

17.3.3 Amplifier mode control register (AMPMC)

The AMPMC register is used to select the operating mode of the amplifier unit.

The AMPMC register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 17 - 8 Format of Amplifier mode control register (AMPMC)

Address: F0470H After reset: 00H R/W

Symbol	<7>	6	<5>	<4>	3	2	1	0
AMPMC	AMPSP	0	AMPSP1	AMPSP0	0	0	0	0

AMPSP	Selection of operating mode for amplifier unit 2 (AMP1) and amplifier unit 3 (AMP2)
0	Low-power mode
1	High-speed mode

AMPSP1	Selection of operating mode for amplifier unit 1 (AMP0)
0	Low-power mode
1	High-speed mode

AMPSP0	Selection of operating mode for amplifier unit 0 (PGA1)
0	Low-power mode
1	High-speed mode

17.3.4 Amplifier trigger mode control register (AMPTRM)

The AMPTRM register is used to select the trigger for activating or stopping the amplifier.

The AMPTRM register can be set by an 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 17 - 9 Format of amplifier trigger mode control register (AMPTRM)

Address: F0471H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
AMPTRM	AMPTRM31	AMPTRM30	AMPTRM21	AMPTRM20	AMPTRM11	AMPTRM10	AMPTRM01	AMPTRM00

AMPTRMn1	AMPTRMn0	Control of activation/stop trigger for the amplifier unit n Note 3
0	0	Software trigger mode • The amplifier unit can be activated/stopped by setting the AMPC register • The amplifier unit cannot be activated by an ELC trigger • The amplifier unit cannot be controlled by a 24-bit ΔΣ A/D scan end trigger
0	1	ELC trigger mode • The amplifier unit can be set to wait for an ELC trigger or stopped by setting the AMPC register • The amplifier unit can be activated by an ELC trigger Note 1 • The amplifier unit cannot be controlled by a 24-bit ΔΣ A/D scan end trigger
1	0	Setting prohibited
1	1	ELC and A/D trigger mode • The amplifier unit can be set to wait for an ELC trigger or stopped by setting the AMPC register • The amplifier unit can be activated by an ELC trigger Note 1 • The amplifier unit can be stopped by a 24-bit ΔΣ A/D scan end trigger Note 2

Note 1. When using an ELC trigger to activate the amplifier unit, first specify various settings related to the event link controller (ELC), set the AMPTRS register, and then use the AMPC register to set the operation control bit of the amplifier unit to be activated to 1 (amplifier unit wait state is enabled).

Note 2. A 24-bit ΔΣ A/D scan end trigger is always generated at the end of A/D conversion.

Note 3. When changing the set values of AMPTRMn1 and AMPTRMn0, make sure that the AMPEn bit in the AMPC register is 0 (amplifier unit is stopped).

Remark n: Unit number (n = 0 to 3)

17.3.5 Amplifier ELC trigger select register (AMPTRS)

The AMPTRS register is used to select the ELC trigger of the amplifier unit.

The AMPTRS register can be set by an 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 17 - 10 Format of amplifier ELC trigger select register (AMPTRS)

Address: F0472H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
AMPTRS	0	0	0	0	0	0	AMPTRS1	AMPTRS0

AMPTRS1	AMPTRS0	ELC trigger selection Note
0	0	Amplifier unit 0: Amplifier ELC trigger 0 Amplifier unit 1: Amplifier ELC trigger 1 Amplifier unit 2: Amplifier ELC trigger 2 Amplifier unit 3: Amplifier ELC trigger 3
0	1	Amplifier unit 0: Amplifier ELC trigger 0 Amplifier unit 1: Amplifier ELC trigger 0 Amplifier unit 2: Amplifier ELC trigger 1 Amplifier unit 3: Amplifier ELC trigger 1
1	0	Setting prohibited
1	1	Amplifier unit 0: Amplifier ELC trigger 0 Amplifier unit 1: Amplifier ELC trigger 0 Amplifier unit 2: Amplifier ELC trigger 0 Amplifier unit 3: Amplifier ELC trigger 0

Note Do not change the value of the AMPTRS register after setting the AMPTRM register.

Caution Be sure to clear bits 2 to 7 to “0”.

17.3.6 Amplifier control register (AMPC)

The AMPC register is used to control the operation of the amplifier unit.

The AMPC register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 17 - 11 Format of amplifier control register (AMPC)

Address: F0473H After reset: 00H R/W

Symbol	7	6	5	4	<3>	<2>	<1>	<0>
AMPC	0	0	0	0	AMPE3	AMPE2	AMPE1	AMPE0

AMPEn	Operation control of amplifier unit n
0	An amplifier unit n is stopped
1	Software trigger mode: Operation of amplifier unit n is enabled ELC trigger mode or ELC and A/D trigger mode: Wait for ELC is enabled

Caution Be sure to clear bits 4 to 7 to “0”.

Remark n: Unit number (n = 0 to 3)

17.3.7 Amplifier control signal monitor register (AMPMON)

The AMPMON register is used to confirm whether the amplifier unit is operating or stopped.

The AMPMON register can be read by an 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 17 - 12 Format of amplifier control signal monitor register (AMPMON)

Address: F0474H After reset: 00H R

Symbol	7	6	5	4	3	2	1	0
AMPMON	0	0	0	0	AMPMON3	AMPMON2	AMPMON1	AMPMON0

AMPMONn	Status of amplifier unit n
0	An amplifier unit n is stopped
1	An amplifier unit n is operating

Caution This register is used to asynchronously reflect whether each amplifier unit is operating or stopped. To determine the state of the amplifier unit, read this register continuously and confirm that the bit state has changed. After that, read this register again for confirmation and determine whether the state of the amplifier unit has changed.
When an ELC trigger or a 24-bit ΔΣ A/D scan end trigger synchronized with the clock or a software trigger in the other interrupt routine is used to control the amplifier unit, the timing to operate or stop the amplifier unit can be estimated, such as for checking normal operation. In this case, read this register after one CPU/peripheral clock cycle when the corresponding trigger or interrupt affecting the state of the amplifier unit has occurred.

Remark n: Unit number (n = 0 to 3)

17.3.8 Amplifier unit 0 gain setting register (PGA1GC)

The PGA1GC register is used to specify the gain of the amplifier unit 0.

The PGA1GC register can be set by an 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 17 - 13 Format of Amplifier Unit 0 Gain Setting Register (PGA1GC)

Address: F0476H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
PGA1GC	0	0	PGA1GC5	PGA1GC4	PGA1GC3	PGA1GC2	PGA1GC1	PGA1GC0

PGA1GC5	PGA1GC4	Specification of the gain for the 1st amplifiers of PGA1 (G_{SET11})
0	0	G_{SET11} = 12
0	1	G_{SET11} = 16
1	0	G_{SET11} = 20
1	1	G_{SET11} = 24

PGA1GC3	PGA1GC2	PGA1GC1	PGA1GC0	Specification of the gain for the 2nd amplifiers of PGA1 (G_{SET12})
0	1	1	1	G_{SET12} = 1.246 (+24.6%)
0	1	1	0	G_{SET12} = 1.207 (+20.7%)
0	1	0	1	G_{SET12} = 1.169 (+16.9%)
0	1	0	0	G_{SET12} = 1.133 (+13.3%)
0	0	1	1	G_{SET12} = 1.098 (+9.8%)
0	0	1	0	G_{SET12} = 1.065 (+6.5%)
0	0	0	1	G_{SET12} = 1.032 (+3.2%)
0	0	0	0	G_{SET12} = 1.000 (0.0%)
1	1	1	1	G_{SET12} = 0.969 (-3.1%)
1	1	1	0	G_{SET12} = 0.939 (-6.1%)
1	1	0	1	G_{SET12} = 0.910 (-9.0%)
1	1	0	0	G_{SET12} = 0.882 (-11.8%)
1	0	1	1	G_{SET12} = 0.855 (-14.5%)
1	0	1	0	G_{SET12} = 0.829 (-17.1%)
1	0	0	1	G_{SET12} = 0.803 (-19.7%)
1	0	0	0	G_{SET12} = 0.778 (-22.2%)

Caution Be sure to clear bits 6 and 7 to "0".

17.3.9 Amplifier unit 0 input select register (PGA1S)

The PGA1S register is used to select the source of the connection to (or non-connection of) the input terminal of PGA1.

The PGA1S register can be set by an 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 17 - 14 Format of Amplifier Unit 0 Input Select Register (PGA1S)

Address: F0477H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
PGA1S	0	0	0	0	0	0	PGA1CS1	PGA1CS0

PGA1CS1	PGA1CS0	Selection of the source of the connection to the input terminal of PGA1
0	0	Not connected Note
0	1	Connect the PGA10P pin to the positive input terminal of PGA1, and the PGA10N pin to the negative input terminal of PGA1.
1	0	Connect the PGA11P pin to the positive input terminal of PGA1, and the PGA11N pin to the negative input terminal of PGA1.
1	1	Setting prohibited

Note If there is no connection to the input terminal, PGA1 stops regardless of the setting of AMPE0 bit in the AMPC register.

Caution Be sure to clear bits 2 to 7 to “0”.

17.3.10 Amplifier unit 1 input select register (AMP0S)

The AMP0S register is used to select the source of the connection to (or non-connection of) the input terminal of AMP0.

The AMP0S register can be set by an 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 17 - 15 Format of Amplifier Unit 1 Input Select Register (AMP0S)

Address: F0478H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
AMP0S	AMP0NFB	AMP0NS0	0	AMP0PDA	0	AMP0PS2	AMP0PS1	AMP0PS0

AMP0NFB	AMP0NS0	Selection of the source of the connection to the negative input terminal of AMP0
0	0	Not connected Note
0	1	Connect the AMP0N pin (multiplexed AFE input 4) to the negative input terminal of AMP0.
1	0	The output from AMP0 is fed back to its own negative input terminal.
1	1	Setting prohibited

AMP0PDA	AMP0PS2	AMP0PS1	AMP0PS0	Selection of the source of the connection to the positive input terminal of AMP0
0	0	0	0	Not connected Note
0	0	0	1	Connect the AMP0P pin (multiplexed AFE input 4) to the positive input terminal of AMP0.
0	0	1	0	Connect the AMP0P pin (multiplexed AFE input 5) to the positive input terminal of AMP0.
0	1	0	0	Connect the AMP0P pin (multiplexed AFE input 7) to the positive input terminal of AMP0.
1	0	0	0	Connect 8-bit D/A converter (DAC0) to the positive input terminal of AMP0.
Other than above				Setting prohibited

Note If there is no connection to the input terminal, AMP0 stops regardless of the setting of AMPE1 bit in the AMPC register.

Caution Be sure to clear bits 3 and 5 to "0".

17.3.11 Amplifier unit 2 input select register (AMP1S)

The AMP1S register is used to select the source of the connection to (or non-connection of) the input terminal of AMP1.

The AMP1S register can be set by an 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 17 - 16 Format of amplifier unit 2 input select register (AMP1S)

Address: F0479H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
AMP1S	AMP1NFB	AMP1NS0	AMP1PVR	AMP1PDA	0	AMP1PS2	AMP1PS1	AMP1PS0

AMP1NFB	AMP1NS0	Selection of the source of the connection to the negative input terminal of AMP1
0	0	Not connected Note
0	1	Connect the AMP1N pin (multiplexed AFE input 5) to the negative input terminal of AMP1.
1	0	The output from AMP1 is fed back to its own negative input terminal.
1	1	Setting prohibited

AMP1PVR	AMP1PDA	AMP1PS2	AMP1PS1	AMP1PS0	Selection of the source of the connection to the positive input terminal of AMP1
0	0	0	0	0	Not connected Note
0	0	0	0	1	Connect the AMP1P pin (multiplexed AFE input 5) to the positive input terminal of AMP1.
0	0	0	1	0	Connect AMP1P pin (multiplexed AFE input 6) to the positive input terminal of AMP1.
0	0	1	0	0	Connect AMP1P pin (multiplexed AFE input 0) to the positive input terminal of AMP1.
0	1	0	0	0	Connect 12-bit D/A converter (DAC1) to the positive input terminal of AMP1.
1	0	0	0	0	Connect the internal bias voltage (VBIAS) to the positive input terminal of AMP1.
Other than above					Setting prohibited

Note If there is no connection to the input terminal, AMP1 stops regardless of the setting of AMPE2 bit in the AMPC register.

Caution Be sure to clear bit 3 to "0".

17.3.12 Amplifier unit 3 input select register (AMP2S)

The AMP2S register is used to select the source of the connection to (or non-connection of) the input terminal of AMP2.

The AMP2S register can be set by an 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 17 - 17 Format of Amplifier Unit 3 Input Select Register (AMP2S)

Address: F047AH After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
AMP2S	AMP2NFB	AMP2NS0	AMP2PVR	AMP2PDA	0	AMP2PS2	0	AMP2PS0

AMP2NFB	AMP2NS0	Selection of the source of the connection to the negative input terminal of AMP2
0	0	Not connected Note
0	1	Connect the AMP2N pin (multiplexed AFE input 6) to the negative input terminal of AMP2.
1	0	The output from AMP2 is fed back to its own negative input pin.
1	1	Setting prohibited

AMP2PVR	AMP2PDA	AMP2PS2	AMP2PS0	Selection of the source of the connection to the positive input terminal of AMP2
0	0	0	0	Not connected Note
0	0	0	1	Connect AMP2P pin (multiplexed AFE input 6) to the positive input terminal of AMP2.
0	0	1	0	Connect AMP2P pin (multiplexed AFE input 1) to the positive input terminal of AMP2.
0	1	0	0	Connect 12-bit D/A converter (DAC1) to the positive input terminal of AMP2.
1	0	0	0	Connect the internal bias voltage (VBIAS) to the positive input terminal of AMP2.
Other than above				Setting prohibited

Note If there is no connection to the input terminal, AMP2 stops regardless of the setting of AMPE3 bit in the AMPC register.

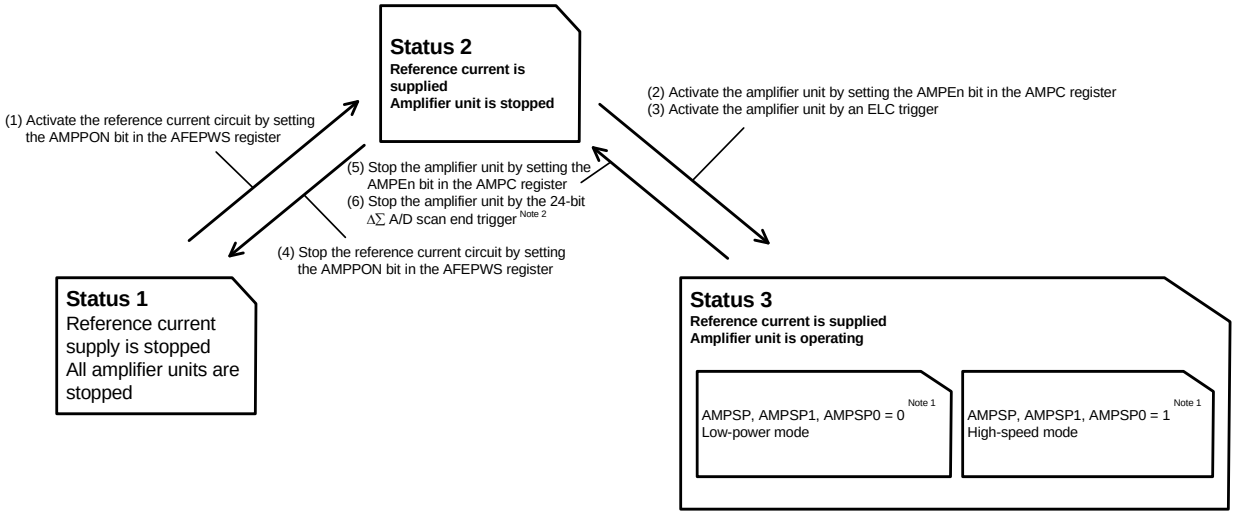
Caution Be sure to clear bits 1 and 3 to “0”.

17.4 Operation

17.4.1 State Transitions

Figure 17 - 18 shows state transitions when the amplifier unit and reference current circuit are activated or stopped using the amplifier unit control circuit.

Figure 17 - 18 Amplifier Unit State Transitions



Note 1. Set the AMPSP, AMPSP1, and AMPSP0 bits in the AMPMC register, and the AMPTRS and AMPTRM registers in status 1.

Note 2. To stop only the amplifier unit at the end of 24-bit ΔΣ A/D scan, it is necessary to preset operation of the reference current circuit to be enabled (operate the amplifier unit via status 2) by setting the AMPPON bit of the AFEPWS register.

Remark 1. A stabilization wait time is necessary after supply of the reference current and operation of the amplifier unit are set before each operation actually starts. For details on the stabilization wait time, refer to **CHAPTER 38 ELECTRICAL SPECIFICATIONS**.

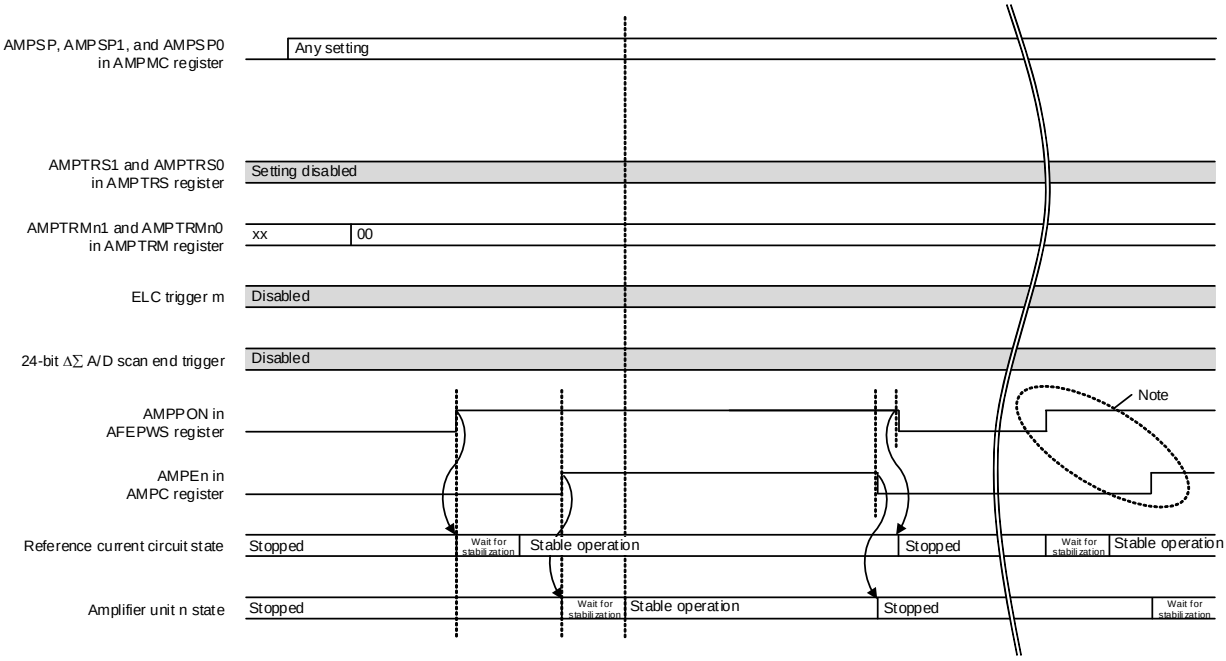
Remark 2. The amplifier unit cannot be activated/stopped continuously in steps (2) → (6).

Remark 3. An ELC trigger and 24-bit ΔΣ A/D scan end trigger can be used to activate/stop only the amplifier unit that is preset to be used by setting the AMPTRM register.

17.4.2 Amplifier Unit Control Operation

Figures 17 - 19 to 17 - 22 show the amplifier unit control operation.

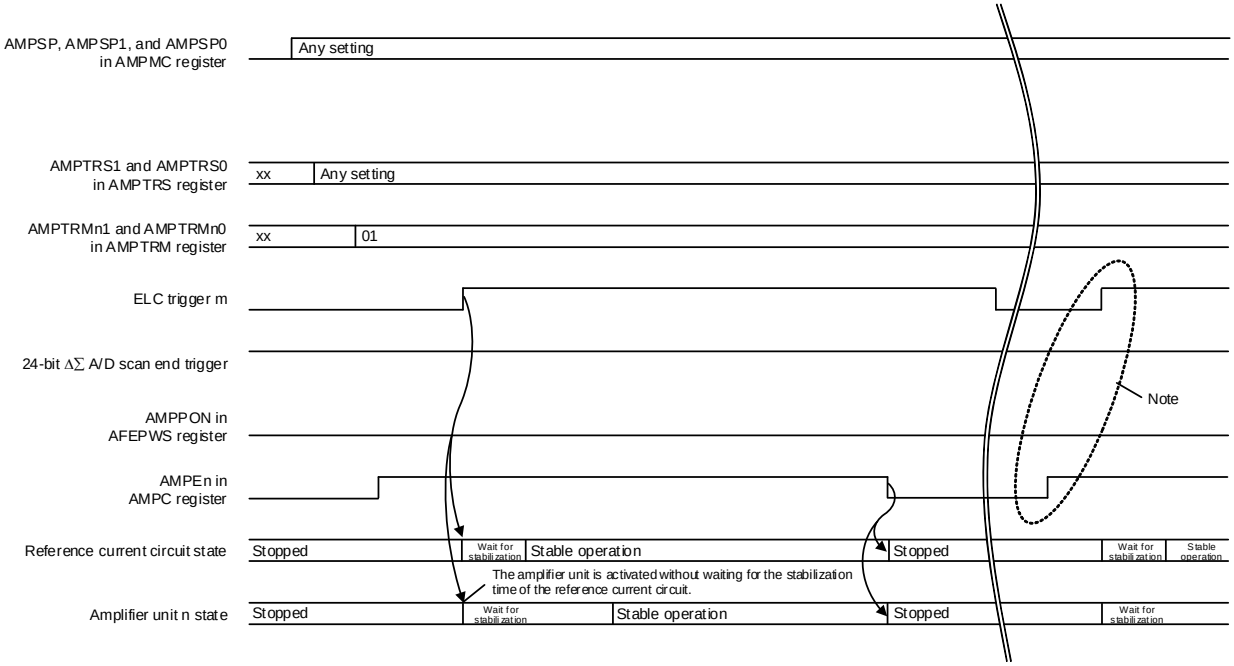
Figure 17 - 19 Amplifier Unit Control Operation (Software trigger mode is used for control)
(When the reference current circuit and amplifier unit are activated/stopped by software trigger mode)



Note When operating/stopping the amplifier unit continuously, set the AMPPON and AMPEn bits again as in the first setting after the amplifier unit is stopped.

Remark n: Unit number (n = 0 to 3)
m: ELC trigger used to control amplifier unit n selected by the AMPTRS register

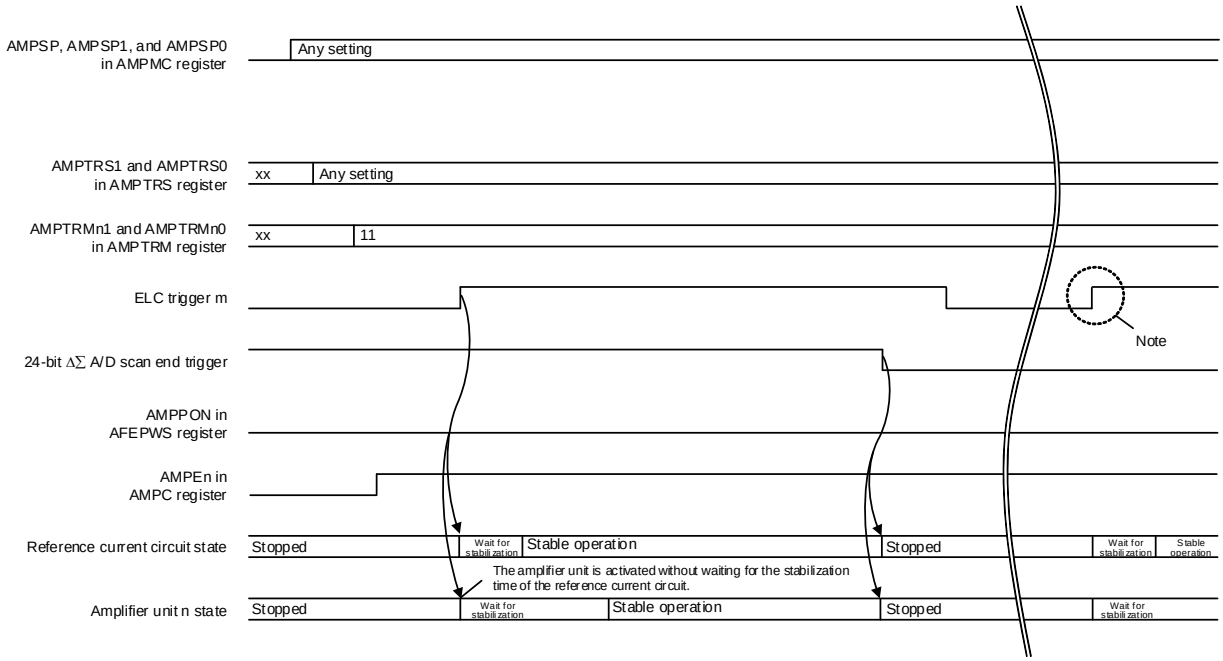
Figure 17 - 20 Amplifier Unit Control Operation (ELC trigger mode is used for activation)
(When the reference current circuit and amplifier unit are activated by an ELC trigger and stopped by setting the SFR)



Note When operating/stopping the amplifier unit continuously, use the AMPEn bit again as in the first setting, and set the amplifier unit to wait for an ELC trigger after it is stopped.

Remark n: Unit number (n = 0 to 3)
m: ELC trigger used to control amplifier unit n selected by the AMPTRS register
Set the function used for ELC event generation and the peripheral function to be linked (the ELSELR register) in advance.

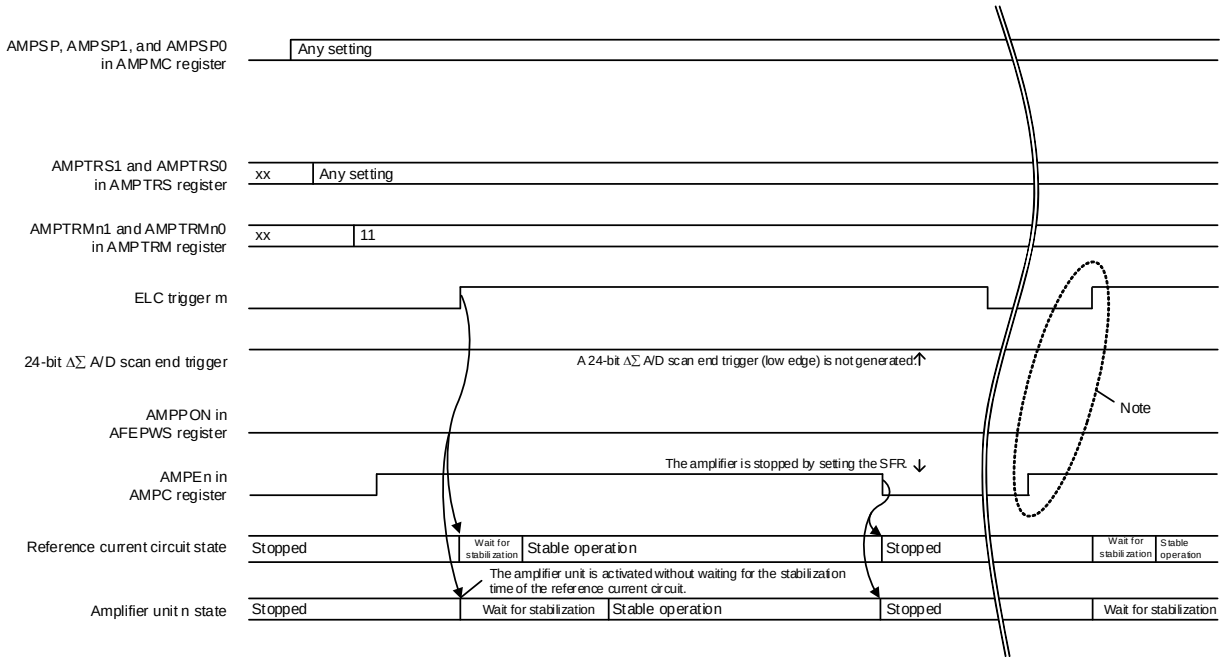
Figure 17 - 21 Amplifier Unit Control Operation (ELC and A/D trigger mode (1))
(When the reference current circuit and amplifier unit are activated by an ELC trigger and stopped by a 24-bit ΔΣ A/D scan end trigger)



Note When operating/stopping the amplifier unit continuously, it is not necessary to set the registers again because the amplifier unit waits for an ELC trigger after it is stopped.

Remark n: Unit number (n = 0 to 3)
m: ELC trigger used to control amplifier unit n selected by the AMPTRS register
Set the function used for ELC event generation and the peripheral function to be linked (the ELSELR register) in advance.

Figure 17 - 22 Amplifier Unit Control Operation (ELC and A/D trigger mode (2))
(When the reference current circuit and amplifier unit are stopped by setting the SFR under the setting that they can be activated by an ELC trigger and stopped by a 24-bit ΔΣ A/D scan end trigger)

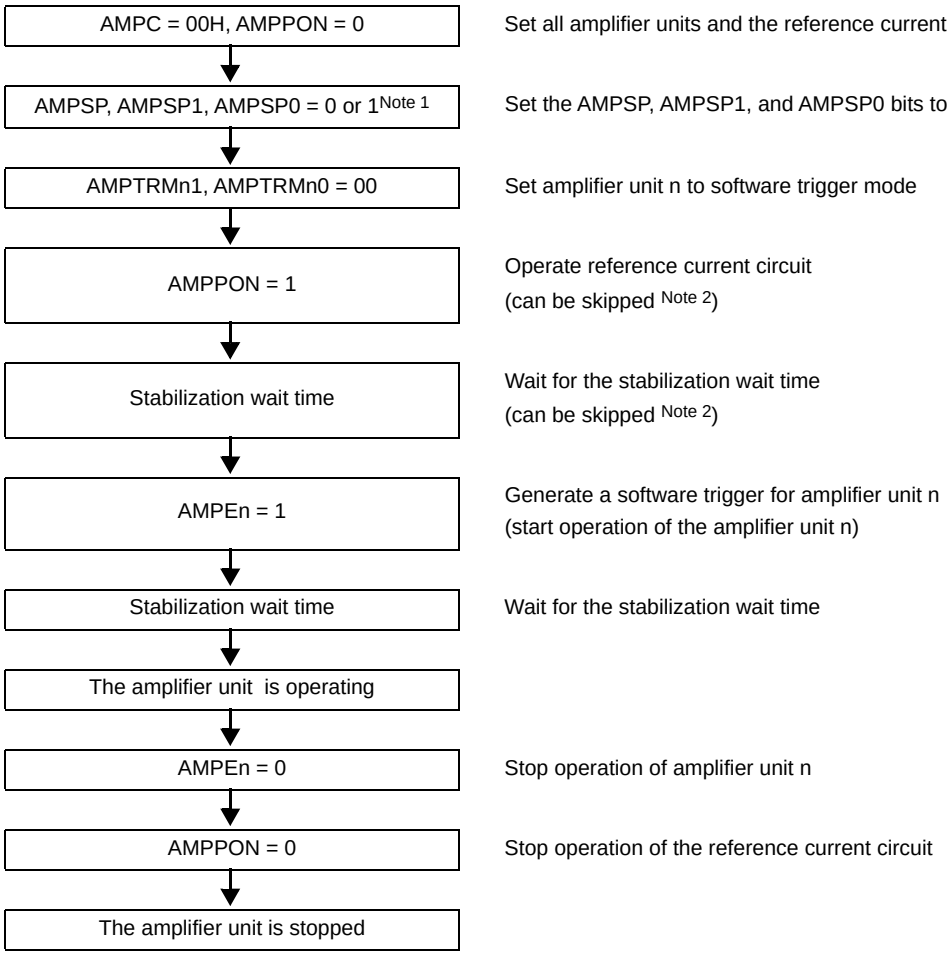


Note When operating/stopping the amplifier unit continuously, use the AMPEn bit again as in the first setting, and set the amplifier unit to wait for an ELC trigger after it is stopped.

Remark n: Unit number (n = 0 to 3)
m: ELC trigger used to control amplifier unit n selected by the AMPTRS register
Set the function used for ELC event generation and the peripheral function to be linked (the ELSELR register) in advance.

17.4.3 Software trigger mode

The following flowchart shows the procedure to operate and stop the amplifier unit using a software trigger with examples of register settings.



Note 1. Set AMPSP, AMPSP1, and AMPSP0 bits while the value of the AMPC register is 00H (the amplifier unit is stopped) and the AMPPON bit in the AFEPWS register is 0.

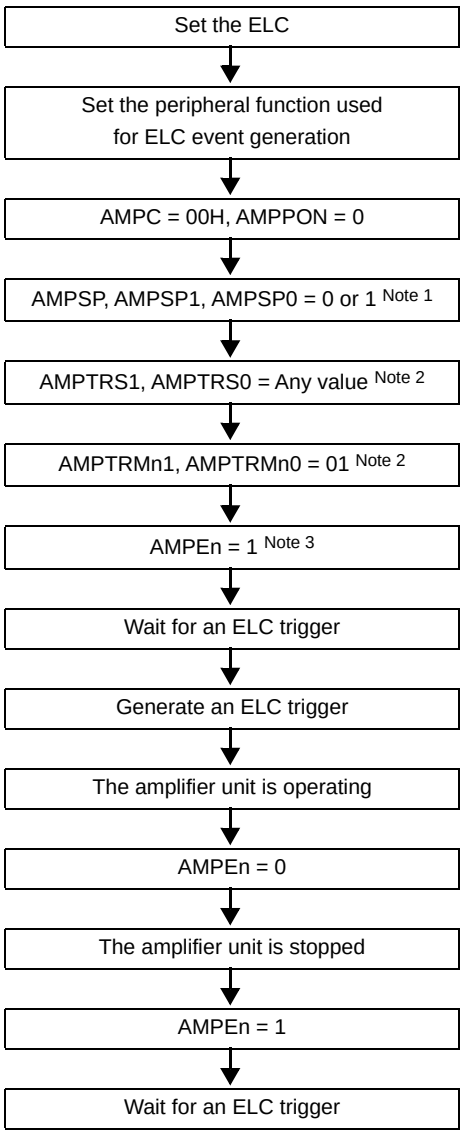
Note 2. If setting AMPPON = 1 and the wait for stabilization are skipped, the stabilization wait time after setting AMPEn =1 will be longer.

Caution For details on the stabilization wait time, refer to CHAPTER 38 ELECTRICAL SPECIFICATIONS (R5F11N, R5F11P) (A: T_A = -40 to +85°C).

17.4.4 ELC trigger mode

The following flowchart shows the procedure to operate the amplifier unit using an ELC trigger with examples of register settings.

This is an example of processing when the amplifier unit is activated by an ELC trigger and stopped by software repeatedly.



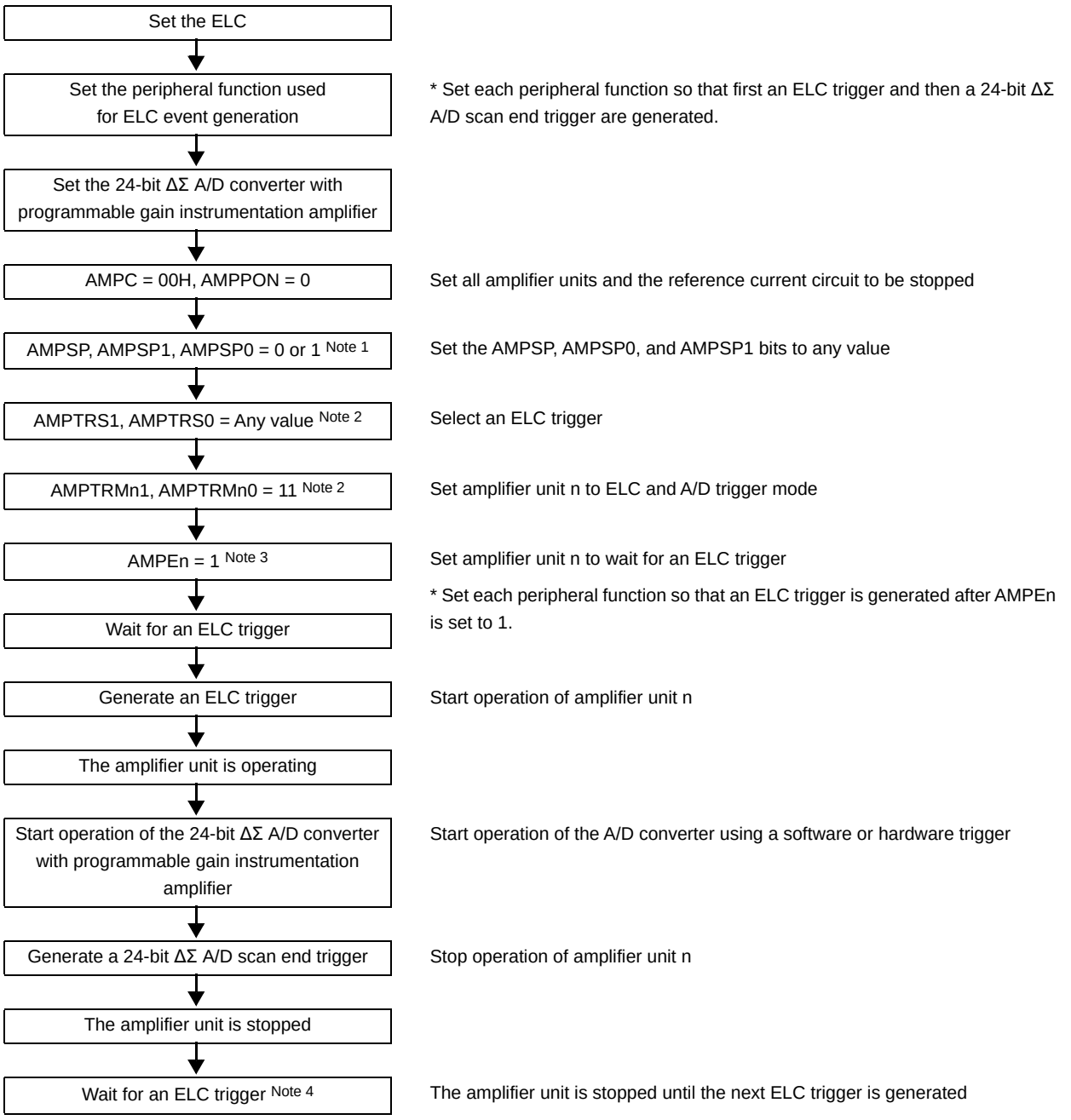
Note 1. Set AMPSP, AMPSP1, and AMPSP0 bits while the value of the AMPC register is 00H (the amplifier unit is stopped) and the AMPPON bit in the AFEPWS register is 0.

Note 2. Set these bits while the AMPEn bit in the AMPC register is 0.

Note 3. To operate the reference current circuit continuously, set the AFEPWS bit in the AMPPON register to 1 at this timing.

17.4.5 ELC and A/D Trigger Mode

The following flowchart shows the procedure to activate the amplifier unit using an ELC trigger and to stop the amplifier unit using a 24-bit ΔΣ A/D scan end trigger with examples of register settings. This is an example of processing when the amplifier unit is activated by an ELC trigger and stopped by a 24-bit ΔΣ A/D scan end trigger repeatedly.



Note 1. Set AMPSP, AMPSP1, and AMPSP0 bits while the value of the AMPC register is 00H (the amplifier unit is stopped) and the AMPPON bit in the AFEPWS register is 0.

Note 2. Set these bits while the AMPEn bit in the AMPC register is 0.

Note 3. Set this bit while the peripheral function used for ELC trigger event generation and the 24-bit ΔΣ A/D converter are stopped. To operate the reference current circuit continuously, set the AMPPON bit in the AFEPWS register to 1 at this timing.

Note 4. To stop wait operation for a trigger, set the AMPEn bit in the AMPC register to 0.
To forcibly stop the amplifier unit after it is activated by an ELC trigger, also set the AMPEn bit in the AMPC register to 0.

17.5 Usage Notes on Amplifier Unit

(1) When connecting bypass capacitors to the AV_{DD} and AV_{SS} pins that are the power supply pins for the amplifier unit function, place them as close to the chip as possible (to keep the wiring short) and prevent noise from the device, board, and peripheral components.

(2) In addition to SFR settings, the amplifier unit function can be activated by an ELC trigger and stopped at the 24-bit ΔΣ A/D scan end trigger. Therefore, design applications (circuits and programs) conforming to the operation flows in order to prevent these asynchronous triggers from causing conflicts between activation/stop control (conflicting control).

CHAPTER 18 D/A CONVERTER (R5F11N and R5F11P only)

18.1 Functions of D/A Converter

The D/A converter is an 8-bit or a 12-bit resolution converter that converts digital inputs into analog signals.

The D/A converter has the following features.

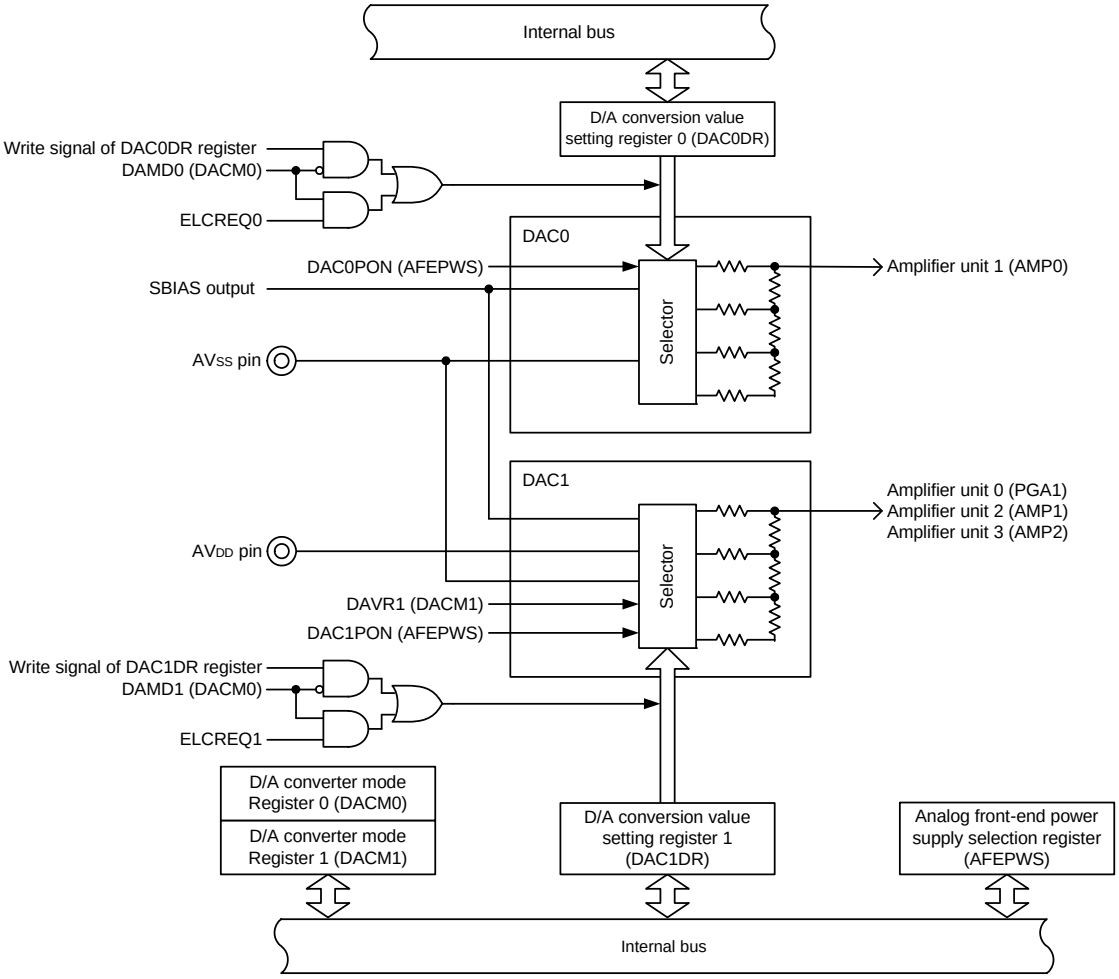
- 8-bit resolution × 1 channel, 12-bit resolution × 1 channel
- R-2R ladder method
- Output analog voltage
  - 8-bit resolution: SBIAS output voltage × m8/256 (m8: Value set to DAC0DR register)
  - 12-bit resolution: AV_{DD} (or SBIAS output voltage) × m12/4096 (m12: Value set to DAC1DR register)
- Operation mode
  - Normal mode
  - Real-time output mode

Caution The D/A converter does not have external output pins. External output must go through the amplifier unit.

18.2 Configuration of D/A Converter

Figure 18 - 1 shows the Block Diagram of D/A Converter. DAC0 is an 8-bit resolution D/A converter and DAC1 is a 12-bit resolution D/A converter.

Figure 18 - 1 Block Diagram of D/A Converter



Remark ELCREQ0 and ELCREQ1 are trigger signals (event signals from the ELC) that are used in the real-time output mode.

18.3 Registers Controlling D/A Converter

The D/A converter is controlled by the following registers.

- Peripheral enable register 1 (PER1)
- Analog front-end power supply selection register (AFEPWS)
- D/A converter mode registers 0, 1 (DACM0, DACM1)
- D/A conversion value setting registers 0, 1 (DAC0DR, DAC1DR)
- Event output destination select register n (ELSELRn), n = 00 to 25

18.3.1 Peripheral enable register 1 (PER1)

The PER1 register is used to enable or disable supplying the clock to the peripheral hardware. Clock supply to the hardware that is not used is also stopped so as to decrease the power consumption and noise.

When the D/A converter is used, be sure to set bit 0 (DACEN) of this register to 1.

The PER1 register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 18 - 2 Format of Peripheral enable register 1 (PER1)

Address: F007AH After reset: 00H R/W

Symbol	<7>	6	5	<4>	<3>	<2>	<1>	<0>
PER1	TMKAEN	0	0	AMPEN Note	DTCEN	PGAEN Note	AFEEN Note	DACEN Note

DACEN Note	Control of input clock supplied to D/A converter
0	Stops input clock supply. • SFR used by the D/A converter cannot be written. • The D/A converter is in the reset status.
1	Supplies input clock. • SFR used by the D/A converter can be read/written.

Note R5F11N and R5F11P only.

Caution 1. When setting the D/A converter, be sure to set DACEN to 1 first.
If DACEN = 0, writing to a control register of the D/A converter is ignored, and all read values are default values.

Caution 2. Be sure to clear following bits to “0”.
R5F11N, R5F11P: Bits 5 and 6
R5F11R: Bits 0 to 2, 4 to 6

18.3.2 Analog front-end power supply selection register (AFEPWS)

This register is used to control the power supplied to the D/A converter.

The AFEPWS register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 18 - 3 Format of Analog Front-End Power Supply Selection Register (AFEPWS)

Address: F0440H After reset: 00H R/W

Symbol	<7>	<6>	5	<4>	3	<2>	1	<0>
AFEPWS	DAC1PON	DAC0PON	0	AMP0PON	0	PGAPON	0	AFEPON

DAC1PON	Control of power supplied to 12-bit D/A converter (DAC1) block
0	Power-off (default)
1	Power-on

DAC0PON	Control of power supplied to 8-bit D/A converter (DAC0) block
0	Power-off (default)
1	Power-on

Caution Be sure to clear bits 1, 3, and 5 to “0”.

18.3.3 D/A converter mode register 0 (DACM0)

This register controls the operation of the D/A converter.

The DACM0 register can be set by an 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 18 - 4 Format of D/A converter mode register 0 (DACM0)

Address: F0484H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
DACM0	DPSEL	0	0	0	0	0	DAMD1	DAMD0

DPSEL	D/A conversion data format selection
0	The flush-right format is selected for the D/A conversion value setting register 1 (DAC1DR).
1	The flush-left format is selected for the D/A conversion value setting register 1 (DAC1DR).

DAMDi	Selection of operation mode for D/A converter (DACi)
0	Normal mode
1	Real-time output mode

Caution Be sure to clear bits 2 to 6 to “0”.

Remark i = 0, 1

18.3.4 D/A converter mode register 1 (DACM1)

This register controls the operation of the D/A converter.

The DACM1 register can be set by an 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 18 - 5 Format of D/A converter mode register 1 (DACM1)

Address: F0485H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
DACM1	0	0	0	0	0	0	DAVR1	0

DAVR1	Selection of reference voltage for D/A converter (DAC1)
0	AV_{DD}
1	SBIAS output

Caution 1. Changing the reference voltage during D/A conversion by DAC1 is prohibited. Be sure to make settings to change the reference voltage while D/A conversion is stopped.

Caution 2. Be sure to clear bits 0 and 2 to 7 to “0”.

18.3.5 D/A conversion value setting register 0 (DAC0DR)

This register is used to set the analog voltage value to be output when the 8-bit D/A converter is used.

The DAC0DR register can be set by an 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 18 - 6 Format of D/A conversion value setting register 0 (DAC0DR)

Address: F0480H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
DAC0DR	DAC0DR7	DAC0DR6	DAC0DR5	DAC0DR4	DAC0DR3	DAC0DR2	DAC0DR1	DAC0DR0

Remark The analog output voltage from the 8-bit D/A converter is determined as follows.
DAC0 output voltage = SBIAS output voltage × (DAC0DR)/256

When the 8-bit D/A converter is not used, set the DAC0PON bit to 0 (power-off) and set the DAC0DR register to 00H to prevent current from flowing into the R-2R resistor ladder to reduce unnecessary current consumption.

18.3.6 D/A conversion value setting register 1 (DAC1DR)

This register is used to set the analog voltage value to be output when the 12-bit D/A converter is used.

The DAC1DR register can be read by a 16-bit memory manipulation instruction.

Reset signal generation clears this register to 0000H.

Figure 18 - 7 Format of D/A conversion value setting register 1 (DAC1DR)

Address: F0482H After reset: 0000H R/W

When the flush-right format is selected (DPSEL = 0)

Symbol	15	14	13	12	11	10	9	8
DAC1DR	0	0	0	0	DAC1DR11	DAC1DR10	DAC1DR9	DAC1DR8
	7	6	5	4	3	2	1	0
	DAC1DR7	DAC1DR6	DAC1DR5	DAC1DR4	DAC1DR3	DAC1DR	DAC1DR1	DAC1DR0

When the flush-left format is selected (DPSEL = 1)

Symbol	15	14	13	12	11	10	9	8
DAC1DR	DAC1DR11	DAC1DR10	DAC1DR9	DAC1DR8	DAC1DR7	DAC1DR6	DAC1DR5	DAC1DR4
	7	6	5	4	3	2	1	0
	DAC1DR3	DAC1DR2	DAC1DR1	DAC1DR0	0	0	0	0

Remark The analog output voltages from the 12-bit D/A converter are determined by the setting of DAVR1 as follows.
When DAVR1 = 0: DAC1 output voltage = AV_{DD} voltage × (DAC1DR)/4096
When DAVR1 = 1: DAC1 output voltage = SBIAS output voltage × (DAC1DR)/4096

When the 12-bit D/A converter is not used, set the DAC1PON bit to 0 (power-off) and set the DAC1DR register to 0000H to prevent current from flowing into the R-2R resistor ladder to reduce unnecessary current consumption.

18.3.7 Event output destination select register n (ELSELRn), n = 00 to 25

When the real-time output mode of the D/A converter is used, D/A conversion is performed using an event signal from the event link controller as an activation trigger.

For details, see **25.3.1 Event output destination select register n (ELSELRn) (n = 00 to 25)**.

18.4 Operations of D/A Converter

18.4.1 Operation in Normal Mode

D/A conversion is performed using write operation to the DACiDR register as the trigger.
The setting method is described below.

<1> Make the setting to start the AFE reference power supply (ABGR) and sensor reference voltage source (SBIAS)[Note].
<2> Set the DACEN bit of the PER1 register (peripheral enable register 1) to 1 to start the supply of the input clock to the D/A converter.
<3> Set the DAMDi bit of the DACM0 register (D/A converter mode register 0) to 0 (normal mode).
<4> Set the value corresponding to the analog voltage to be output, to the DACiDR register (D/A conversion value setting register i).

Steps <1> and <4> above constitute the initial settings.

<5> Set the DACiPON bit of the AFEPWS register to 1 (power-on).
D/A conversion starts, and then, after the settling time elapses, the analog voltage set in step <4> is output.
<6> To perform subsequent D/A conversions, write to the DACiDR register.

The previous D/A conversion result is held until the next D/A conversion is performed.
When the DACiPON bit of the AFEPWS register is set to 0 (power-off), D/A conversion stops.

Note The sensor reference voltage source (SBIAS) need not be started if AV_{DD} is to be the reference voltage for DAC1.

Caution 1. Even if 1, 0, and then 1 is set to the DACiPON bit, the analog voltage set by the DACiDR register is output when a settling time has elapsed after 1 is set for the last time.

Caution 2. If the DACiDR register is rewritten during the settling time, D/A conversion is aborted and reconversion by using the rewritten values starts.

Remark i = 0, 1

18.4.2 Operation in Real-Time Output Mode

D/A conversion is performed on each channel using the event signals from the ELC as triggers. The setting method is described below.

<1> Make the setting to start the AFE reference power supply (ABGR) and sensor reference voltage source (SBIAS)[Note].
<2> Set the DACEN bit of the PER1 register (peripheral enable register 1) to 1 to start the supply of the input clock to the D/A converter.
<3> Set the DAMDi bit of the DACM0 register (D/A converter mode register 0) to 0 (normal mode).
<4> Set the value corresponding to the analog voltage to be output, to the DACiDR register (D/A conversion value setting register i).
<5> Set the DACiPON bit of the AFEPWS register to 1 (power-on).
D/A conversion starts, and then, after the settling time elapses, the analog voltage set in step <4> is output.
<6> Use the event output destination select register (ELSELRn; n = 00 to 25) to set the trigger signal used for real-time output mode.
<7> Set the DAMDi bit of the DACM0 register to 1 (real-time output mode).
<8> Start the operation of the event source.

Steps <1> to <8> above constitute the initial settings.

<9> Upon generation of the trigger signals used for real-time output mode, D/A conversion starts and the analog voltage set in step <4> will be output after a settling time has elapsed.

Set the value corresponding to the analog voltage to be output, to the DACiDR register before performing the next D/A conversion (trigger signal used for real-time output mode is generated).
When the DACiPON bit of the AFEPWS register is set to 0 (power-off), D/A conversion stops.

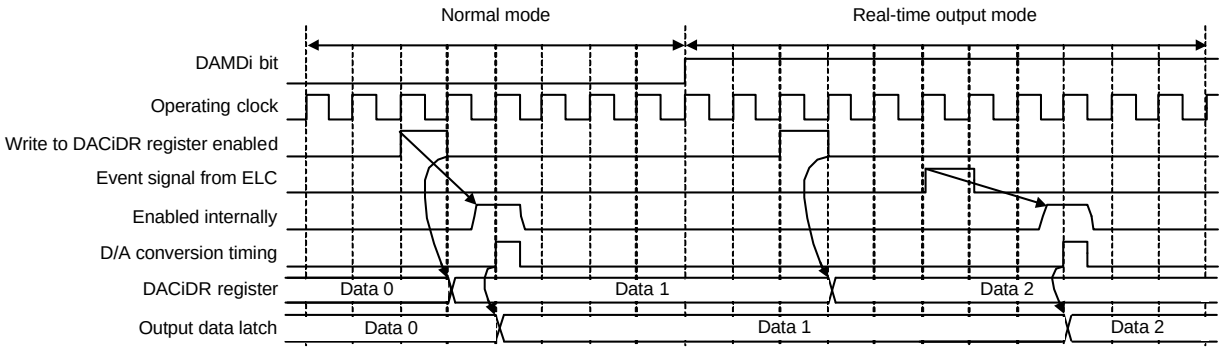
Note The sensor reference voltage source (SBIAS) need not be started if AV_{DD} is to be the reference voltage for DAC1.

Caution 1. Even if 1, 0, and then 1 is set to the DACiPON bit, the analog voltage set by the DACiDR register is output when a settling time has elapsed after 1 is set for the last time.
Caution 2. Set the interval between each generation of the trigger signal used for real-time output mode of the same channel to longer than the settling time. If a trigger signal used for real-time output mode is generated during the settling time, D/A conversion is aborted and reconversion starts.
Caution 3. Set the interval between each generation of the trigger signal used for real-time output mode of the same channel to longer than the three clocks of f_{CLK}. When a trigger is generated consecutively at intervals of three or fewer f_{CLK} clock cycles, D/A conversion is performed using only the first trigger.

18.4.3 Timing for Outputting D/A Conversion Value

Figure 18 - 8 shows the timing for outputting D/A conversion value.

Figure 18 - 8 Timing for Outputting D/A Conversion Value



Remark i = 0, 1

- Normal mode
  The value is written to the data latch after one cycle of the operating clock when the DACiDR register is written.
- Real-time output mode (when conversion operation is enabled)
  The value is written to the data latch (output to the amplifier unit) after two or three cycles of the operating clock when the event signal from the ELC is accepted.

18.5 Cautions for D/A Converter

Observe the following cautions when using the D/A converter.

(1) The operation of the D/A converter continues in the HALT and STOP modes. To lower the power consumption, therefore, clear the DACiPON bit to 0, and execute the HALT or STOP instruction after stopping the operation of the D/A converter.

Remark i = 0, 1

(2) To stop the real-time output mode (including when changing to normal mode), one of the following procedures must be used:

- Wait for at least three clocks after stopping the trigger output source and then set bits DACiPON and DAMDi to 0.
- After setting bits DACiPON and DAMDi, set the DACEN bit of the PER1 register to 0 (DAC stop).
  When the DACEN bit is set to 0, all the registers in the DAC are cleared, so the settings of the SFRs are required to start the operation again.

(3) In real-time output mode, set the value of the DACiDR register before a trigger signal used for real-time output mode is generated. Do not change the set value of the DACiDR register while the trigger signal is output.

(4) When entering STOP mode while real-time output mode is enabled, disable linking of ELC events before entering STOP mode.

CHAPTER 19 A/D CONVERTER

The number of analog input channels of the A/D converter differs, depending on the product.

	R5F11NM	R5F11NL	R5F11PL, R5F11NG	R5F11RM
Number of analog input channels	3 ch (ANI12 to ANI14)	3 ch (ANI8, ANI10, ANI11)	3 ch (ANI8 to ANI10)	3 ch (ANI8 to ANI10)

19.1 Function of A/D Converter

The A/D converter is a converter that converts analog input signals into digital values, and is configured to control analog inputs, including up to ten channels of A/D converter analog inputs (ANI8 to ANI14). 10-bit or 8-bit resolution can be selected by the ADTYP bit of the A/D converter mode register 2 (ADM2).
The A/D converter has the following function.

- 10-bit or 8-bit resolution A/D conversion

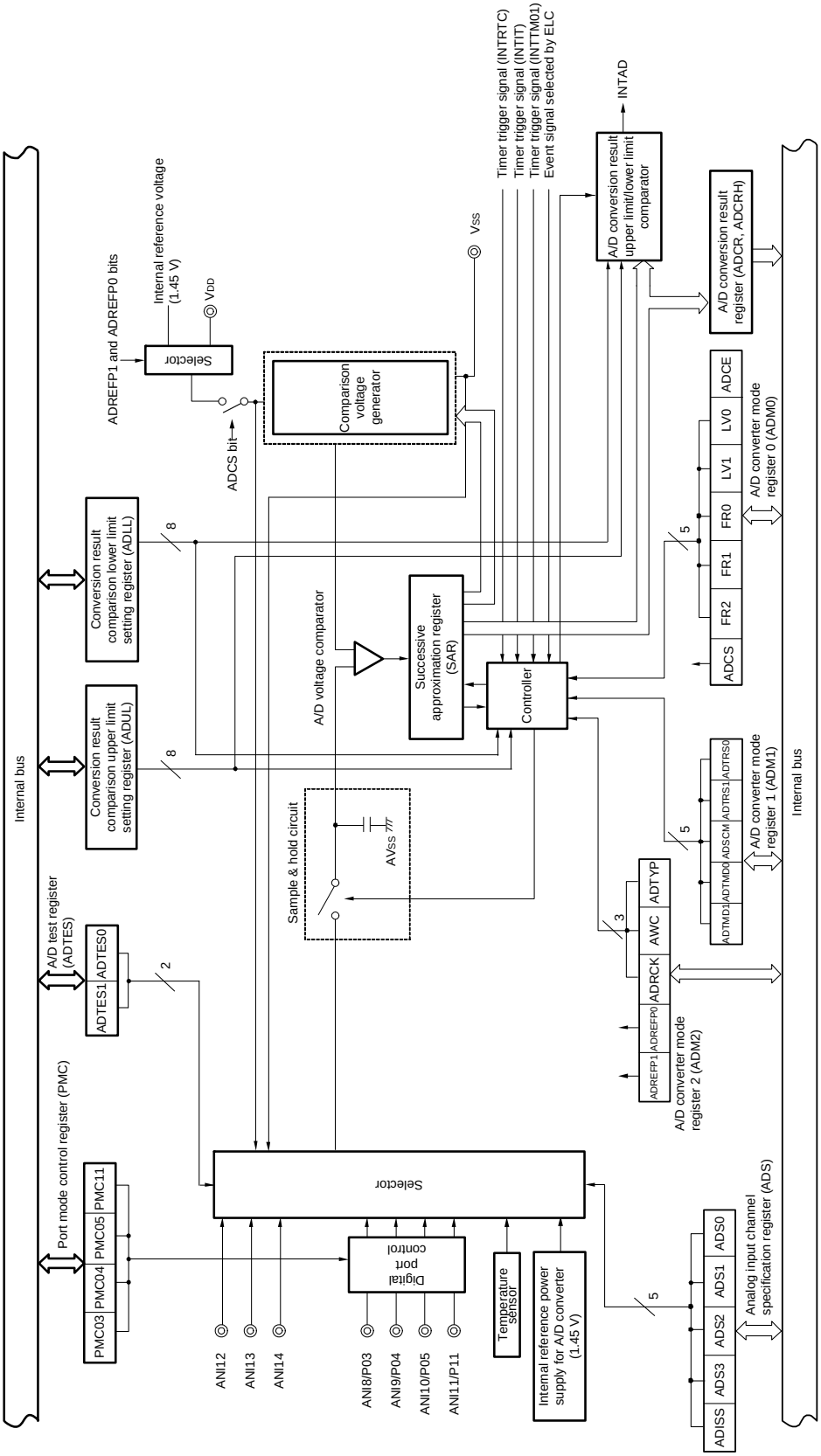
  10-bit or 8-bit resolution A/D conversion is carried out repeatedly for one analog input channel selected from ANI8 to ANI14. Each time an A/D conversion operation ends, an interrupt request (INTAD) is generated.

Various A/D conversion modes can be specified by using the mode combinations below.

Trigger mode	Software trigger	Conversion is started by software.
	Hardware trigger no-wait mode	Conversion is started by detecting a hardware trigger.
	Hardware trigger wait mode	The power is turned on by detecting a hardware trigger while the system is off and in the conversion standby state, and conversion is then started automatically after the stabilization wait time passes. When using the SNOOZE mode function, specify the hardware trigger wait mode.
Conversion operation mode	One-shot conversion mode	A/D conversion is performed on the selected channel once.
	Sequential conversion mode	A/D conversion is sequentially performed on the selected channels until it is stopped by software.
Operation voltage mode	Standard 1 or standard 2 mode	Select this mode for conversion in the operation voltage range of 2.7 V ≤ V_{DD} ≤ 5.5 V.
	Low voltage 1 or low voltage 2 mode	Conversion is done in the operation voltage range of 1.8 V^{Note} ≤ V_{DD} ≤ 5.5 V. Select this mode for conversion at a low voltage. Because the operation voltage is low, it is internally boosted during conversion.
Sampling time selection	Sampling clock cycles: 7 f_{AD}	The sampling time in standard 1 mode is seven cycles of the conversion clock (f_{AD}). Select this mode when the output impedance of the analog input source is high and the sampling time should be long.
	Sampling clock cycles: 5 f_{AD}	The sampling time in standard 2 mode is five cycles of the conversion clock (f_{AD}). Select this mode when enough sampling time is ensured (for example, when the output impedance of the analog input source is low).

Note This is the case for the R5F11R. The minimum for the R5F11N and R5F11P is 2.4 V.

Figure 19 - 1 Block Diagram of A/D Converter



Caution The above figure includes all possible analog input pins provided for products of the RL78/H1D group. For the analog input pins actually supported by individual products and the pins on which functions other than port functions are multiplexed, see CHAPTER 2 PIN FUNCTIONS.

19.2 Configuration of A/D Converter

The A/D converter includes the following hardware.

(1) ANI8 to ANI14 pins

These are the analog input pins of the seven channels of the A/D converter. They input analog signals to be converted into digital signals. Each of ANI8 to ANI11 can be used as an I/O port pin when it is not selected as an analog input pin.

(2) Sample & hold circuit

The sample & hold circuit samples each of the analog input voltages sequentially sent from the input circuit, and sends them to the A/D voltage comparator. This circuit also holds the sampled analog input voltage during A/D conversion.

(3) A/D voltage comparator

This A/D voltage comparator compares the voltage generated from the voltage tap of the comparison voltage generator with the analog input voltage. If the analog input voltage is found to be greater than the reference voltage (1/2 AV_{REF}) as a result of the comparison, the most significant bit (MSB) of the successive approximation register (SAR) is set. If the analog input voltage is less than the reference voltage (1/2 AV_{REF}), the MSB bit of the SAR is reset.

After that, bit 8 of the SAR register is automatically set, and the next comparison is made. The voltage tap of the comparison voltage generator is selected by the value of bit 9, to which the result has been already set.

Bit 9 = 0: (1/4 AV_{REF})
Bit 9 = 1: (3/4 AV_{REF})

The voltage tap of the comparison voltage generator and the analog input voltage are compared and bit 8 of the SAR register is manipulated according to the result of the comparison.

Analog input voltage ≥ Voltage tap of comparison voltage generator: Bit 8 = 1
Analog input voltage ≤ Voltage tap of comparison voltage generator: Bit 8 = 0

Comparison is continued like this to bit 0 of the SAR register.

When performing A/D conversion at a resolution of 8 bits, the comparison continues until bit 2 of the SAR register.

Remark AV_{REF}: The positive reference voltage of the A/D converter. This can be selected from the internal reference voltage (1.45 V) and V_{DD}.

(4) Comparison voltage generator

The comparison voltage generator generates the comparison voltage input from an analog input pin.

(5) Successive approximation register (SAR)

The SAR register is a register that sets voltage tap data whose values from the comparison voltage generator match the voltage values of the analog input pins, 1 bit at a time starting from the most significant bit (MSB).

If data is set in the SAR register all the way to the least significant bit (LSB) (end of A/D conversion), the contents of the SAR register (conversion results) are held in the A/D conversion result register (ADCR). When all the specified A/D conversion operations have ended, an A/D conversion end interrupt request signal (INTAD) is generated.

(6) 10-bit A/D conversion result register (ADCR)

The A/D conversion result is loaded from the successive approximation register to this register each time A/D conversion is completed, and the ADCR register holds the A/D conversion result in its higher 10 bits (the lower 6 bits are fixed to 0).

(7) 8-bit A/D conversion result register (ADCRH)

The A/D conversion result is loaded from the successive approximation register to this register each time A/D conversion is completed, and the ADCRH register stores the higher 8 bits of the A/D conversion result.

(8) Controller

This circuit controls the conversion time of an input analog signal that is to be converted into a digital signal, as well as starting and stopping of the conversion operation. When A/D conversion has been completed, this controller generates INTAD through the A/D conversion result upper limit/lower limit comparator.

19.3 Registers Controlling A/D Converter

The A/D converter is controlled by the following registers.

- Peripheral enable register 0 (PER0)
- A/D converter mode register 0 (ADM0)
- A/D converter mode register 1 (ADM1)
- A/D converter mode register 2 (ADM2)
- 10-bit A/D conversion result register (ADCR)
- 8-bit A/D conversion result register (ADCRH)
- Analog input channel specification register (ADS)
- Conversion result comparison upper limit setting register (ADUL)
- Conversion result comparison lower limit setting register (ADLL)
- A/D test register (ADTES)
- Port mode control registers 0, 1 (PMC0, PMC1)
- Port mode registers 0, 1 (PM0, PM1)

19.3.1 Peripheral enable register 0 (PER0)

This register is used to enable or disable supplying the clock to the peripheral hardware. Clock supply to the hardware that is not used is also stopped so as to decrease the power consumption and noise.

When the A/D converter is used, be sure to set bit 5 (ADCEN) of this register to 1.

The PER0 register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 19 - 2 Format of Peripheral enable register 0 (PER0)

Address: F00F0H After reset: 00H R/W

Symbol	<7>	6	<5>	<4>	<3>	<2>	1	<0>
PER0	RTCWEN	0	ADCEN	IICA0EN	SAU1EN	SAU0EN	0	TAU0EN

ADCEN	Control of A/D converter input clock supply
0	Stops input clock supply. • SFRs used by the A/D converter cannot be written. • The A/D converter is in the reset status.
1	Enables input clock supply. • SFRs used by the A/D converter can be read/written.

Caution 1. When setting the A/D converter, be sure to set the following registers first while the ADCEN bit is set to 1.
If ADCEN = 0, the values of the A/D converter control registers are cleared to their initial values and writing to them is ignored (except for port mode registers 0, 1 (PM0, PM1), port mode control registers 0, 1 (PMC0, PMC1)).
- **A/D converter mode register 0 (ADM0)**
- **A/D converter mode register 1 (ADM1)**
- **A/D converter mode register 2 (ADM2)**
- **10-bit A/D conversion result register (ADCR)**
- **8-bit A/D conversion result register (ADCRH)**
- **Analog input channel specification register (ADS)**
- **Conversion result comparison upper limit setting register (ADUL)**
- **Conversion result comparison lower limit setting register (ADLL)**
- **A/D test register (ADTES)**

Caution 2. Be sure to clear bits 1 and 6 to 0.

19.3.2 A/D converter mode register 0 (ADM0)

This register sets the conversion time for analog input to be A/D converted, and starts/stops conversion.

The ADM0 register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 19 - 3 Format of A/D converter mode register 0 (ADM0)

Address: FFF30H After reset: 00H R/W

Symbol	<7>	6	5	4	3	2	1	<0>
ADM0	ADCS	0	FR2 Note 1	FR1 Note 1	FR0 Note 1	LV1 Note 1	LV0 Note 1	ADCE

ADCS	A/D conversion operation control
0	Stops conversion operation [When read] Conversion stopped/standby status
1	Enables conversion operation [When read] While in the software trigger mode: Conversion operation status While in the hardware trigger wait mode: A/D power supply stabilization wait status + conversion operation status

ADCE	A/D voltage comparator operation control Note 2
0	Stops A/D voltage comparator operation
1	Enables A/D voltage comparator operation

Note 1. For details of the FR2 to FR0, LV1, LV0 bits, and A/D conversion, see **Table 19 - 3 A/D Conversion Time Selection**.

Note 2. While in the software trigger mode or hardware trigger no-wait mode, the operation of the A/D voltage comparator is controlled by the ADCS and ADCE bits, and it takes 1 µs from the start of operation for the operation to stabilize. Therefore, when the ADCS bit is set to 1 after 1 µs or more has elapsed from the time ADCE bit is set to 1, the conversion result at that time has priority over the first conversion result. Otherwise, ignore data of the first conversion.

Caution 1. Change the FR2 to FR0, LV1, and LV0 bits while conversion is stopped (ADCS = 0, ADCE = 0).

Caution 2. Do not set the ADCS bit to 1 and the ADCE bit to 0 at the same time.

Caution 3. Do not change the ADCS and ADCE bits from 0 to 1 at the same time by using an 8-bit manipulation instruction. Be sure to set these bits in the order described in 19.7 A/D Converter Setup Flowchart.

Caution 4. Be sure to clear bit 6 to 0.

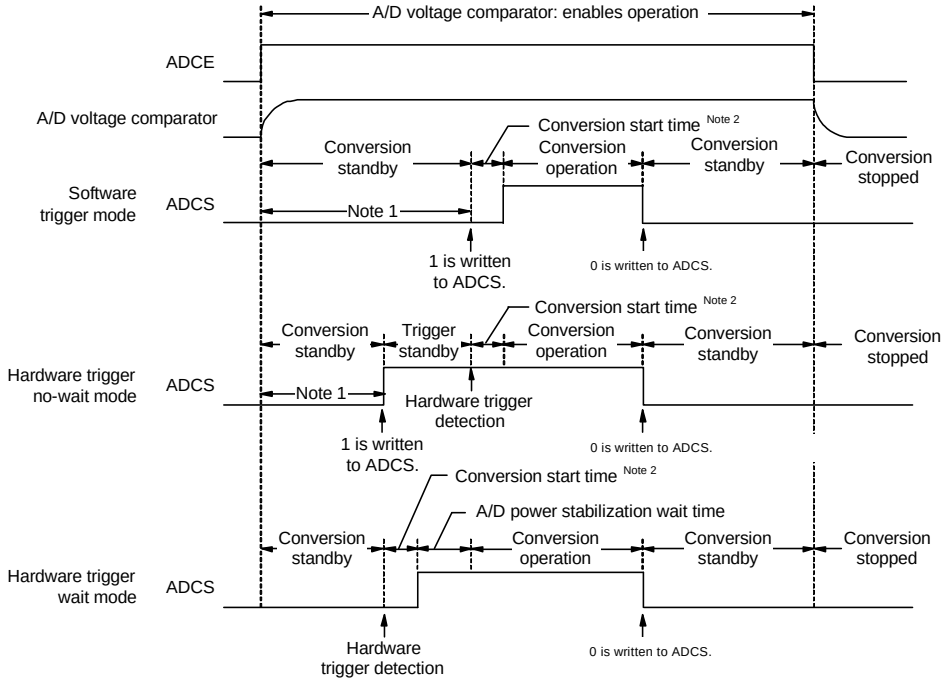
Table 19 - 1 Settings of ADCS and ADCE Bits

ADCS	ADCE	A/D Conversion Operation
0	0	Conversion stopped state
0	1	Conversion standby state
1	0	Setting prohibited
1	1	Conversion-in-progress state

Table 19 - 2 Setting and Clearing Conditions for ADCS Bit

A/D Conversion Mode		Set Conditions	Clear Conditions
Software trigger	Sequential conversion mode	When 1 is written to ADCS	When 0 is written to ADCS
	One-shot conversion mode		• When 0 is written to ADCS • The bit is automatically cleared to 0 when A/D conversion ends.
Hardware trigger no-wait mode	Sequential conversion mode		When 0 is written to ADCS
	One-shot conversion mode		When 0 is written to ADCS
Hardware trigger wait mode	Sequential conversion mode	When a hardware trigger is input	When 0 is written to ADCS
	One-shot conversion mode		• When 0 is written to ADCS • The bit is automatically cleared to 0 when A/D conversion ends.

Figure 19 - 4 Timing Chart When A/D Voltage Comparator Is Used



Note 1. While in the software trigger mode or hardware trigger no-wait mode, the time from the rising of the ADCE bit to the falling of the ADCS bit must be 1 μs or longer to stabilize the internal circuit.

Note 2. The following time is the maximum amount of time necessary to start conversion.

ADM0			Conversion Clock (f_{AD})	Conversion Start Time (Number of f_{CLK} Clocks)	
FR2	FR1	FR0		Software trigger mode/ Hardware trigger no wait mode	Hardware trigger wait mode
0	0	0	f_{CLK}/64	63	1
0	0	1	f_{CLK}/32	31	
0	1	0	f_{CLK}/16	15	
0	1	1	f_{CLK}/8	7	
1	0	0	f_{CLK}/6	5	
1	0	1	f_{CLK}/5	4	
1	1	0	f_{CLK}/4	3	
1	1	1	f_{CLK}/2	1	

For the second and subsequent conversion in sequential conversion mode, the conversion start time and the stabilization wait time for A/D power supply do not occur after a hardware trigger is detected.

Caution 1. If using the hardware trigger wait mode, setting the ADCS bit to 1 is prohibited (but the bit is automatically switched to 1 when the hardware trigger signal is detected). However, it is possible to clear the ADCS bit to 0 to specify the A/D conversion standby status.

Caution 2. While in the one-shot conversion mode of the hardware trigger no-wait mode, the ADCS flag is not automatically cleared to 0 when A/D conversion ends. Instead, 1 is retained.

Caution 3. Only rewrite the value of the ADCE bit when ADCS = 0 (while in the conversion stopped/conversion standby status).

Caution 4. To complete A/D conversion, specify at least the following time as the hardware trigger interval:
Hardware trigger no wait mode: 2 f_{CLK} clock + Conversion start time + A/D conversion time
Hardware trigger wait mode: 2 f_{CLK} clock + Conversion start time + A/D power supply stabilization wait time + A/D conversion time

Remark f_{CLK}: CPU/peripheral hardware clock frequency

Table 19 - 3 A/D Conversion Time Selection (1/4)

(1) When there is no A/D power supply stabilization wait time Normal mode 1, 2 (software trigger mode/hardware trigger no-wait mode)

A/D Converter Mode Register 0 (ADM0)					Mode	Conversion Clock (f_{AD})	Number of Conversion Clock Note	Conversion Time	Conversion Time at 10-Bit Resolution				
									2.7 V ≤ V_{DD} ≤ 5.5 V				
FR2	FR1	FR0	LV1	LV0					f_{CLK} = 1 MHz	f_{CLK} = 4 MHz	f_{CLK} = 8 MHz	f_{CLK} = 16 MHz	f_{CLK} = 24 MHz
0	0	0	0	0	Normal 1	f_{CLK}/64	19 f_{AD} (number of sampling clock: 7 f_{AD})	1216/f_{CLK}	Setting prohibited	Setting prohibited	Setting prohibited	76 µs	50.667 µs
0	0	1				f_{CLK}/32		608/f_{CLK}			76 µs	38 µs	25.333 µs
0	1	0				f_{CLK}/16		304/f_{CLK}		76 µs	38 µs	19 µs	12.667 µs
0	1	1				f_{CLK}/8		152/f_{CLK}		38 µs	19 µs	9.5 µs	6.333 µs
1	0	0				f_{CLK}/6		114/f_{CLK}		28.5 µs	14.25 µs	7.125 µs	4.75 µs
1	0	1				f_{CLK}/5		95/f_{CLK}	95 µs	23.75 µs	11.875 µs	5.938 µs	3.958 µs
1	1	0				f_{CLK}/4		76/f_{CLK}	76 µs	19 µs	9.5 µs	4.75 µs	3.167 µs
1	1	1				f_{CLK}/2		38/f_{CLK}	38 µs	9.5 µs	4.75 µs	2.375 µs	Setting prohibited
0	0	0	0	1	Normal 2	f_{CLK}/64	17 f_{AD} (number of sampling clock: 5 f_{AD})	1088/f_{CLK}	Setting prohibited	Setting prohibited	Setting prohibited	68 µs	45.333 µs
0	0	1				f_{CLK}/32		544/f_{CLK}			68 µs	34 µs	22.667 µs
0	1	0				f_{CLK}/16		272/f_{CLK}		68 µs	34 µs	17 µs	11.333 µs
0	1	1				f_{CLK}/8		136/f_{CLK}		34 µs	17 µs	8.5 µs	5.667 µs
1	0	0				f_{CLK}/6		102/f_{CLK}		25.5 µs	12.75 µs	6.375 µs	4.25 µs
1	0	1				f_{CLK}/5		85/f_{CLK}	85 µs	21.25 µs	10.625 µs	5.3125 µs	3.542 µs
1	1	0				f_{CLK}/4		68/f_{CLK}	68 µs	17 µs	8.5 µs	4.25 µs	2.833 µs
1	1	1				f_{CLK}/2		34/f_{CLK}	34 µs	8.5 µs	4.25 µs	2.125 µs	Setting prohibited

Note These are the numbers of clock cycles when conversion is with 10-bit resolution. When eight-bit resolution is selected, the values are shorter by two cycles of the conversion clock (f_{AD}).

Caution 1. The A/D conversion time must also be within the relevant range of conversion times (t_{CONV}) described in 38.6.1 or 39.6.3 POR circuit characteristics.

Caution 2. Rewrite the FR2 to FR0, LV1 and LV0 bits to other than the same data while conversion is stopped (ADCS = 0, ADCE = 0).

Caution 3. The above conversion time does not include conversion state time. Conversion state time add in the first conversion. Select conversion time, taking clock frequency errors into consideration.

Remark f_{CLK}: CPU/peripheral hardware clock frequency

Table 19 - 3 A/D Conversion Time Selection (2/4)

(2) When there is no A/D power supply stabilization wait time Low-voltage mode 1, 2 (software trigger mode/hardware trigger no-wait mode)

A/D Converter Mode Register 0 (ADM0)					Mode	Conversion Clock (f_{AD})	Number of Conversion Clock Note 4	Conversion Time	Conversion Time at 10-Bit Resolution				
									1.8 V Note 1 ≤ V_{DD} ≤ 5.5 V			Note 2.	Note 3.
FR2	FR1	FR0	LV1	LV0					f_{CLK} = 1 MHz	f_{CLK} = 4 MHz	f_{CLK} = 8 MHz	f_{CLK} = 16 MHz	f_{CLK} = 24 MHz
0	0	0	1	0	Low-voltage 1	f_{CLK}/64	19 f_{AD} (number of sampling clock: 7 f_{AD})	1216/f_{CLK}	Setting prohibited	Setting prohibited	Setting prohibited	76 µs	50.667 µs
0	0	1				f_{CLK}/32		608/f_{CLK}			76 µs	38 µs	25.333 µs
0	1	0				f_{CLK}/16		304/f_{CLK}		76 µs	38 µs	19 µs	12.667 µs
0	1	1				f_{CLK}/8		152/f_{CLK}		38 µs	19 µs	9.5 µs	6.333 µs
1	0	0				f_{CLK}/6		114/f_{CLK}		28.5 µs	14.25 µs	7.125 µs	4.75 µs
1	0	1				f_{CLK}/5		95/f_{CLK}	95 µs	23.75 µs	11.875 µs	5.938 µs	3.958 µs
1	1	0				f_{CLK}/4		76/f_{CLK}	76 µs	19 µs	9.5 µs	4.75 µs	3.167 µs
1	1	1				f_{CLK}/2		38/f_{CLK}	38 µs	9.5 µs	4.75 µs	2.375 µs	Setting prohibited
0	0	0	1	1	Low-voltage 2	f_{CLK}/64	17 f_{AD} (number of sampling clock: 5 f_{AD})	1088/f_{CLK}	Setting prohibited	Setting prohibited	Setting prohibited	68 µs	45.333 µs
0	0	1				f_{CLK}/32		544/f_{CLK}			68 µs	34 µs	22.667 µs
0	1	0				f_{CLK}/16		272/f_{CLK}		68 µs	34 µs	17 µs	11.333 µs
0	1	1				f_{CLK}/8		136/f_{CLK}		34 µs	17 µs	8.5 µs	5.667 µs
1	0	0				f_{CLK}/6		102/f_{CLK}		25.5 µs	12.75 µs	6.375 µs	4.25 µs
1	0	1				f_{CLK}/5		85/f_{CLK}	85 µs	21.25 µs	10.625 µs	5.3125 µs	3.542 µs
1	1	0				f_{CLK}/4		68/f_{CLK}	68 µs	17 µs	8.5 µs	4.25 µs	2.833 µs
1	1	1				f_{CLK}/2		34/f_{CLK}	34 µs	8.5 µs	4.25 µs	2.125 µs	Setting prohibited

Note 1. This is the case for the R5F11R. The minimum for the R5F11N and R5F11P is 2.4 V.

Note 2. 2.4 V ≤ V_{DD} ≤ 5.5 V

Note 3. 2.7 V ≤ V_{DD} ≤ 5.5 V

Note 4. These are the numbers of clock cycles when conversion is with 10-bit resolution. When eight-bit resolution is selected, the values are shorter by two cycles of the conversion clock (f_{AD}).

Caution 1. The A/D conversion time must also be within the relevant range of conversion times (t_{CONV}) described in 38.6.1 or 39.6.1 A/D converter Characteristics.
Note that the conversion time (t_{CONV}) does not include the A/D power supply stabilization wait time.

Caution 2. Rewrite the FR2 to FR0, LV1 and LV0 bits to other than the same data while conversion is stopped (ADCS = 0, ADCE = 0).

Caution 3. The above conversion time does not include conversion state time. Conversion state time add in the first conversion. Select conversion time, taking clock frequency errors into consideration.

Caution 4. When hardware trigger wait mode, specify the conversion time, including the A/D power supply stabilization wait time from the hardware trigger detection.

Remark f_{CLK}: CPU/peripheral hardware clock frequency

Table 19 - 3 A/D Conversion Time Selection (3/4)

(3) When there is A/D power supply stabilization wait time Normal mode 1, 2

(hardware trigger wait mode[Note 1])

A/D Converter Mode Register 0 (ADM0)					Mode	Conversion Clock (f_{AD})	Number of A/D Power Supply Stabilization Wait Clock	Number of Conversion Clock Note 2	A/D Power Supply Stabilization Wait Time + Conversion Time	A/D Power Supply Stabilization Wait Time + Conversion Time at 10-Bit Resolution				
										2.7 V ≤ V_{DD} ≤ 5.5 V				
FR2	FR1	FR0	LV1	LV0						f_{CLK} = 1 MHz	f_{CLK} = 4 MHz	f_{CLK} = 8 MHz	f_{CLK} = 16 MHz	f_{CLK} = 24 MHz
0	0	0	0	0	Normal 1	f_{CLK}/64	8 f_{AD}	19 f_{AD} (number of sampling clock: 7 f_{AD})	1728/f_{CLK}	Setting prohibited	Setting prohibited	Setting prohibited	108 μs	72 μs
0	0	1				f_{CLK}/32			864/f_{CLK}			108 μs	54 μs	36 μs
0	1	0				f_{CLK}/16			432/f_{CLK}		108 μs	54 μs	27 μs	18 μs
0	1	1				f_{CLK}/8			216/f_{CLK}		54 μs	27 μs	13.5 μs	9 μs
1	0	0				f_{CLK}/6			162/f_{CLK}		40.5 μs	20.25 μs	10.125 μs	6.75 μs
1	0	1				f_{CLK}/5			135/f_{CLK}	135 μs	33.75 μs	16.875 μs	8.4375 μs	5.625 μs
1	1	0				f_{CLK}/4			108/f_{CLK}	108 μs	27 μs	13.5 μs	6.75 μs	4.5 μs
1	1	1				f_{CLK}/2			54/f_{CLK}	54 μs	13.5 μs	6.75 μs	3.375 μs	2.25 μs
0	0	0	0	1	Normal 2	f_{CLK}/64	8 f_{AD}	17 f_{AD} (number of sampling clock: 5 f_{AD})	1600/f_{CLK}	Setting prohibited	Setting prohibited	Setting prohibited	100 μs	66.667 μs
0	0	1				f_{CLK}/32			800/f_{CLK}			100 μs	50 μs	33.333 μs
0	1	0				f_{CLK}/16			400/f_{CLK}		100 μs	50 μs	25 μs	16.667 μs
0	1	1				f_{CLK}/8			200/f_{CLK}		50 μs	25 μs	12.5 μs	8.333 μs
1	0	0				f_{CLK}/6			150/f_{CLK}		37.5 μs	18.75 μs	9.375 μs	6.25 μs
1	0	1				f_{CLK}/5			125/f_{CLK}	125 μs	31.25 μs	15.625 μs	7.8125 μs	5.208 μs
1	1	0				f_{CLK}/4			100/f_{CLK}	100 μs	25 μs	12.5 μs	6.25 μs	4.167 μs
1	1	1				f_{CLK}/2			50/f_{CLK}	50 μs	12.5 μs	6.25 μs	3.125 μs	2.083 μs

Note 1. For the second and subsequent conversion in sequential conversion, the conversion start time and stabilization wait time for A/D power supply do not occur after a hardware trigger is detected (see **Table 19 - 3**).

Note 2. These are the numbers of clock cycles when conversion is with 10-bit resolution. When eight-bit resolution is selected, the values are shorter by two cycles of the conversion clock (f_{AD}).

Caution 1. The A/D conversion time must also be within the relevant range of conversion times (t_{CONV}) described in 38.6.1 or 39.6.1 A/D converter Characteristics.
Note that the conversion time (t_{CONV}) does not include the A/D power supply stabilization wait time.

Caution 2. Rewrite the FR2 to FR0, LV1 and LV0 bits to other than the same data while conversion is stopped (ADCS = 0, ADCE = 0).

Caution 3. The above conversion time does not include conversion state time. Conversion state time add in the first conversion. Select conversion time, taking clock frequency errors into consideration.

Caution 4. When hardware trigger wait mode, specify the conversion time, including the A/D power supply stabilization wait time from the hardware trigger detection.

Remark f_{CLK}: CPU/peripheral hardware clock frequency

Table 19 - 3 A/D Conversion Time Selection (4/4)

(4) When there is A/D power supply stabilization wait time Low-voltage mode 1, 2

(hardware trigger wait mode[Note 1])

A/D Converter Mode Register 0 (ADM0)					Mode	Conversion Clock (f_{AD})	Number of A/D Power Supply Stabilization Wait Clock	Number of Conversion Clock Note 5	A/D Power Supply Stabilization Wait Time + Conversion Time	A/D Power Supply Stabilization Wait Time + Conversion Time at 10-Bit Resolution				
										1.8 V[Note 2] ≤ V_{DD} ≤ 5.5 V			Note 3.	Note 4.
FR2	FR1	FR0	LV1	LV0						f_{CLK} = 1 MHz	f_{CLK} = 4 MHz	f_{CLK} = 8 MHz	f_{CLK} = 16 MHz	f_{CLK} = 24 MHz
0	0	0	1	0	Low-voltage 1	f_{CLK}/64	8 f_{AD}	19 f_{AD} (number of sampling clock: 7 f_{AD})	1344/f_{CLK}	Setting prohibited	Setting prohibited	Setting prohibited	84 µs	56µs
0	0	1				f_{CLK}/32			672/f_{CLK}			84 µs	42 µs	28 µs
0	1	0				f_{CLK}/16			336/f_{CLK}		84 µs	42 µs	21 µs	14 µs
0	1	1				f_{CLK}/8			168/f_{CLK}		42 µs	21 µs	10.5 µs	7 µs
1	0	0				f_{CLK}/6			126/f_{CLK}		31.25 µs	15.75 µs	7.875 µs	5.25 µs
1	0	1				f_{CLK}/5			105/f_{CLK}	105 µs	26.25 µs	13.125 µs	6.5625 µs	4.375 µs
1	1	0				f_{CLK}/4			84/f_{CLK}	84 µs	21 µs	10.5 µs	5.25 µs	3.5 µs
1	1	1				f_{CLK}/2			42/f_{CLK}	42µs	10.5 µs	5.25 µs	2.625 µs	1.75 µs
0	0	0	1	1	Low-voltage 2	f_{CLK}/64	8 f_{AD}	17 f_{AD} (number of sampling clock: 5 f_{AD})	1216/f_{CLK}	Setting prohibited	Setting prohibited	Setting prohibited	76 µs	50.667 µs
0	0	1				f_{CLK}/32			608/f_{CLK}			76 µs	38 µs	25.333 µs
0	1	0				f_{CLK}/16			304/f_{CLK}		76 µs	38 µs	19 µs	12.667 µs
0	1	1				f_{CLK}/8			152/f_{CLK}		38 µs	19 µs	9.5 µs	6.333 µs
1	0	0				f_{CLK}/6			114/f_{CLK}		28.5 µs	14.25 µs	7.125 µs	4.75 µs
1	0	1				f_{CLK}/5			95/f_{CLK}	96 µs	23.75 µs	11.875 µs	5.938 µs	3.958 µs
1	1	0				f_{CLK}/4			76/f_{CLK}	76 µs	19 µs	9.5 µs	4.75 µs	3.167 µs
1	1	1				f_{CLK}/2			38/f_{CLK}	38 µs	9.5 µs	4.75 µs	2.375 µs	Setting prohibited

Note 1. For the second and subsequent conversion in sequential conversion mode, the conversion start time and stabilization wait time for A/D power supply do not occur after a hardware trigger is detected (see **Table 19 - 3**).

Note 2. This is the case for the R5F11R. The minimum for the R5F11N and R5F11P is 2.4 V.

Note 3. 2.4 V ≤ V_{DD} ≤ 5.5 V

Note 4. 2.7 V ≤ V_{DD} ≤ 5.5 V

Note 5. These are the numbers of clock cycles when conversion is with 10-bit resolution. When eight-bit resolution is selected, the values are shorter by two cycles of the conversion clock (f_{AD}).

Caution 1. The A/D conversion time must also be within the relevant range of conversion times (t_{CONV}) described in 38.6.1 or 39.6.1 A/D converter Characteristics.
Note that the conversion time (t_{CONV}) does not include the A/D power supply stabilization wait time.

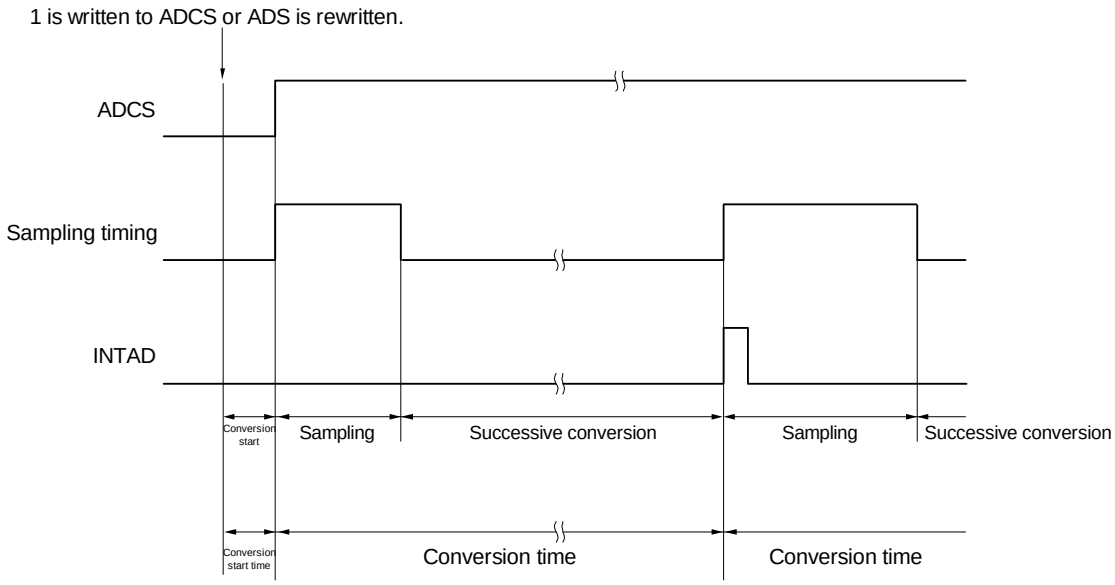
Caution 2. Rewrite the FR2 to FR0, LV1 and LV0 bits to other than the same data while conversion is stopped (ADCS = 0, ADCE = 0).

Caution 3. The above conversion time does not include conversion state time. Conversion state time add in the first conversion. Select conversion time, taking clock frequency errors into consideration.

Caution 4. When hardware trigger wait mode, specify the conversion time, including the A/D power supply stabilization wait time from the hardware trigger detection.

Remark f_{CLK}: CPU/peripheral hardware clock frequency

Figure 19 - 5 A/D Converter Sampling and A/D Conversion Timing (Example for Software Trigger Mode)



19.3.3 A/D converter mode register 1 (ADM1)

This register is used to specify the A/D conversion trigger, conversion mode, and hardware trigger signal.

The ADM1 register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 19 - 6 Format of A/D converter mode register 1 (ADM1)

Address: FFF32H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
ADM1	ADTMD1	ADTMD0	ADSCM	0	0	0	ADTRS1	ADTRS0

ADTMD1	ADTMD0	Selection of the A/D conversion trigger mode
0	0	Software trigger mode
0	1	
1	0	Hardware trigger no-wait mode
1	1	Hardware trigger wait mode

ADSCM	Specification of the A/D conversion mode
0	Sequential conversion mode
1	One-shot conversion mode

ADTRS1	ADTRS0	Selection of the hardware trigger signal
0	0	End of timer channel 1 count or capture interrupt signal (INTTM01)
0	1	Event signal selected by ELC
1	0	Real-time clock 2 interrupt signal (INTRTC)
1	1	12-bit Interval timer interrupt signal (INTIT)

Caution 1. Rewrite the value of the ADM1 register while conversion is stopped (ADCS = 0, ADCE = 0).

Caution 2. To complete A/D conversion, specify at least the following time as the hardware trigger interval:
Hardware trigger no wait mode: 2 f_{CLK} clock + conversion start time + A/D conversion time
Hardware trigger wait mode: 2 f_{CLK} clock + conversion start time + A/D power supply stabilization wait time + A/D conversion time

Caution 3. In modes other than SNOOZE mode, input of the next INTRTC or INTIT will not be recognized as a valid hardware trigger for up to four f_{CLK} cycles after the first INTRTC or INTIT is input.

Remark f_{CLK}: CPU/peripheral hardware clock frequency

19.3.4 A/D converter mode register 2 (ADM2)

This register is used to select the positive or negative reference voltage of the A/D converter, check the upper limit and lower limit A/D conversion result values, select the resolution, and specify whether to use the SNOOZE mode.

The ADM2 register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 19 - 7 Format of A/D converter mode register 2 (ADM2) (1/2)

Address: F0010H After reset: 00H R/W

Symbol	7	6	5	4	<3>	<2>	1	<0>
ADM2	ADREFP1	ADREFP0	0	0	ADRCK	AWC	0	ADTYP

ADREFP1	ADREFP0	Selection of the positive reference voltage source of the A/D converter
0	0	Supplied from V_{DD}
0	1	Setting prohibited
1	0	Supplied from the internal reference voltage (1.45 V) Note
1	1	Setting prohibited

- When ADREFP1 or ADREFP0 bit is rewritten, this must be configured in accordance with the following procedures.

(1) Set ADCE = 0
(2) Change the values of ADREFP1 and ADREFP0
(3) Reference voltage stabilization wait time (A)
(4) Set ADCE = 1
(5) Reference voltage stabilization wait time (B)

When ADREFP1 and ADREFP0 are set to 1 and 0, the setting is changed to A = 5 µs, B = 1 µs.
When ADREFP1 and ADREFP0 are set to 0 and 0, A needs no wait and B = 1 µs.

- When ADREFP1 and ADREFP0 are set to 1 and 0, respectively, A/D conversion cannot be performed on the internal reference voltage.
  Be sure to perform A/D conversion while ADISS = 0.

Note Operation is possible only in HS (high-speed main) mode.

Caution 1. Rewrite the value of the ADM2 register while conversion is stopped (ADCS = 0, ADCE = 0).

Caution 2. When entering STOP mode, do not set ADREFP1 to 1. When selecting the internal reference voltage (ADREFP1, ADREFP0 = 1, 0), the current value of A/D converter reference voltage current (I_{ADREF}) shown in 38.3.2 or 39.3.2 Supply current characteristics is added.

Caution 3. Be sure to clear bit 5 to "0".

Remark The negative reference voltage of the A/D converter is supplied from V_{SS}.

Figure 19 - 7 Format of A/D converter mode register 2 (ADM2) (2/2)

Address: F0010H After reset: 00H R/W

Symbol	7	6	5	4	<3>	<2>	1	<0>
ADM2	ADREFP1	ADREFP0	0	0	ADRCK	AWC	0	ADTYP

ADRCK	Checking the upper limit and lower limit conversion result values
0	The interrupt signal (INTAD) is output when the ADLL register ≤ the ADCR register ≤ the ADUL register (AREA1).
1	The interrupt signal (INTAD) is output when the ADCR register < the ADLL register (AREA2) or the ADUL register < the ADCR register (AREA3).
Figure 19 - 8 shows the generation range of the interrupt signal (INTAD) for AREA1 to AREA3.	

AWC	Specification of the SNOOZE mode
0	Do not use the SNOOZE mode function.
1	Use the SNOOZE mode function.

When there is a hardware trigger signal in the STOP mode, the STOP mode is exited, and A/D conversion is performed without operating the CPU (the SNOOZE mode).

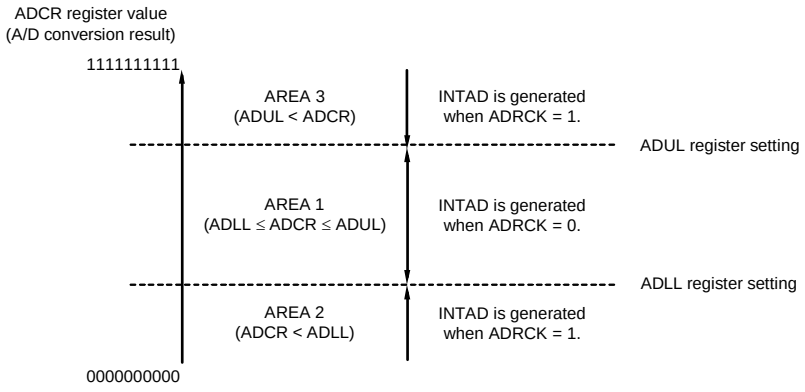
- The SNOOZE mode function can only be specified when the high-speed on-chip oscillator clock is selected for the CPU/peripheral hardware clock (f_{CLK}). If any other clock is selected, specifying this mode is prohibited.
- Using the SNOOZE mode function in the software trigger mode or hardware trigger no-wait mode is prohibited.
- Using the SNOOZE mode function in the sequential conversion mode is prohibited.
- When using the SNOOZE mode function, specify a hardware trigger interval of at least "shift time to SNOOZE mode Note + conversion start time + A/D power supply stabilization wait time + A/D conversion time + 2 f_{CLK} clock"
- Even when using SNOOZE mode, be sure to set the AWC bit to 0 in normal operation and change it to 1 just before shifting to STOP mode.
  Also, be sure to change the AWC bit to 0 after returning from STOP mode to normal operation.
  If the AWC bit is left set to 1, A/D conversion will not start normally in spite of the subsequent SNOOZE or normal operation mode.

ADTYP	Selection of the A/D conversion resolution
0	10-bit resolution
1	8-bit resolution

Note Refer to "Transition time from STOP mode to SNOOZE mode" in **27.3.3 SNOOZE mode**.

Caution **Only rewrite the value of the ADM2 register while conversion operation is stopped (which is indicated by the ADCS and ADCE bits of A/D converter mode register 0 (ADM0) being 0).**

Figure 19 - 8 ADRCK Bit Interrupt Signal Generation Range



Remark If INTAD does not occur, the A/D conversion result is not stored in the ADCR or ADCRH register.

19.3.5 10-bit A/D conversion result register (ADCR)

This register is a 16-bit register that stores the A/D conversion result in the select mode. The lower 6 bits are fixed to 0. Each time A/D conversion ends, the conversion result is loaded from the successive approximation register (SAR). The higher 8 bits of the conversion result are stored in FFF1FH and the lower 2 bits are stored in the higher 2 bits of FFF1EH Note.

The ADCR register can be read by a 16-bit memory manipulation instruction.

Reset signal generation clears this register to 0000H.

Note If the A/D conversion result is outside the range specified by using the A/D conversion comparison function (the value specified by the ADRCK bit of the ADM2 register and ADUL/ADLL registers; see **Figure 19 - 8**), the result is not stored.

Figure 19 - 9 Format of 10-bit A/D conversion result register (ADCR)

Address: FFF1FH, FFF1EH After reset: 0000H R

Symbol	FFF1FH								FFF1EH							
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADCR											0	0	0	0	0	0

Caution 1. When 8-bit resolution A/D conversion is selected (when the ADTYP bit of A/D converter mode register 2 (ADM2) is 1) and the ADCR register is read, 0 is read from the lower two bits (bits 7 and 6 of the ADCR register).

Caution 2. When the ADCR register is accessed in 16-bit units, the 10 bits of the conversion result are read in order starting at bit 15.

19.3.6 8-bit A/D conversion result register (ADCRH)

This register is an 8-bit register that stores the A/D conversion result. The higher 8 bits of 10-bit resolution are stored.

The ADCRH register can be read by an 8-bit memory manipulation instruction Note.

Reset signal generation clears this register to 00H.

Note If the A/D conversion result is outside the range specified by using the A/D conversion comparison function (the value specified by the ADRCK bit of the ADM2 register and ADUL/ADLL registers; see **Figure 19 - 8**), the result is not stored.

Figure 19 - 10 Format of 8-bit A/D conversion result register (ADCRH)

Address: FFF1FH After reset: 00H R

Symbol	7	6	5	4	3	2	1	0
ADCRH								

Caution When writing to A/D converter mode register 0 (ADM0) or analog input channel specification register (ADS), the contents of the ADCRH register may become undefined. Read the conversion result following conversion completion before writing to the ADM0 or ADS register. Using timing other than the above may cause an incorrect conversion result to be read.

19.3.7 Analog input channel specification register (ADS)

This register specifies the input channel of the analog voltage to be A/D converted.

The ADS register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 19 - 11 Format of Analog input channel specification register (ADS)

Address: FFF31H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
ADS	ADISS	0	0	0	ADS3	ADS2	ADS1	ADS0

ADISS	ADS3	ADS2	ADS1	ADS0	Analog input channel	Input source
0	1	0	0	0	ANI8	P03/ANI8 pin Note 1
0	1	0	0	1	ANI9	P04/ANI9 pin Note 2
0	1	0	1	0	ANI10	P05/ANI10 pin Note 1
0	1	0	1	1	ANI11	P11/ANI11 pin Note 3
0	1	1	0	0	ANI12	ANI12 pin Note 4
0	1	1	0	1	ANI13	ANI13 pin Note 4
0	1	1	1	0	ANI14	ANI14 pin Note 4
1	0	0	0	0	—	Temperature sensor output voltage Note 5
1	0	0	0	1	—	Internal reference voltage (1.45 V) Note 5
Other than above					Setting prohibited	

Note 1. R5F11NL, R5F11PL, R5F11NG, and R5F11RM only.

Note 2. R5F11PL, R5F11NG, and R5F11RM only.

Note 3. R5F11NL only.

Note 4. R5F11NM only.

Note 5. Operation is possible only in HS (high-speed main) mode.

Caution 1. Be sure to clear bits 4 to 6 to 0.

Caution 2. For pins set to the analog input mode in port mode control register 0 or 1 (PMC0 or PMC1), use the corresponding port mode register 0 or 1 (PM0 or PM1) to select the input mode.

Caution 3. Do not set the pin that is set to be a digital I/O pin by using the PMC0 or PMC1 register, by using the ADS register.

Caution 4. Rewrite the value of the ADISS bit while conversion is not running (ADCS = 0, ADCE = 0).

Caution 5. If the ADISS bit is set to 1, the internal reference voltage (1.45 V) cannot be used for the positive reference voltage. The result of conversion immediately after the ADISS bit is set to 1 cannot be used. For the setting procedure, see 19.7.4 Setup when temperature sensor output voltage/internal reference voltage is selected (example for software trigger mode and one-shot conversion mode).

Caution 6. Do not set the ADISS bit to 1 when shifting to STOP mode. When the ADISS bit is set to 1, the A/D converter reference voltage current (I_{ADREF}) indicated in 38.3.2 or 39.3.2 Supply current characteristics will be added.

19.3.8 Conversion result comparison upper limit setting register (ADUL)

This register is used to specify the setting for checking the upper limit of the A/D conversion results.

The A/D conversion results and ADUL register value are compared, and interrupt signal (INTAD) generation is controlled in the range specified for the ADRCK bit of A/D converter mode register 2 (ADM2) (shown in **Figure 19 - 8**).

The ADUL register can be set by an 8-bit memory manipulation instruction.

Reset signal generation sets this register to FFH.

Caution 1. When 10-bit resolution A/D conversion is selected, the higher eight bits of the 10-bit A/D conversion result register (ADCR) are compared with the ADUL and ADLL registers.

Caution 2. Only write new values to the ADUL and ADLL registers while conversion is stopped (ADCS = 0, ADCE = 0).

Caution 3. The setting of the ADUL and ADLL registers must be greater than that of the ADLL register.

Figure 19 - 12 Format of Conversion result comparison upper limit setting register (ADUL)

Address: F0011H After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
ADUL	ADUL7	ADUL6	ADUL5	ADUL4	ADUL3	ADUL2	ADUL1	ADUL0

19.3.9 Conversion result comparison lower limit setting register (ADLL)

This register is used to specify the setting for checking the lower limit of the A/D conversion results.

The A/D conversion results and ADLL register value are compared, and interrupt signal (INTAD) generation is controlled in the range specified for the ADRCK bit of A/D converter mode register 2 (ADM2) (shown in **Figure 19 - 8**).

The ADLL register can be set by an 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 19 - 13 Format of Conversion result comparison lower limit setting register (ADLL)

Address: F0012H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
ADLL	ADLL7	ADLL6	ADLL5	ADLL4	ADLL3	ADLL2	ADLL1	ADLL0

Caution 1. When 10-bit resolution A/D conversion is selected, the higher eight bits of the 10-bit A/D conversion result register (ADCR) are compared with the ADUL and ADLL registers.

Caution 2. Only write new values to the ADUL and ADLL registers while conversion is stopped (ADCS = 0, ADCE = 0).

Caution 3. The setting of the ADUL and ADLL registers must be greater than that of the ADLL register.

19.3.10 A/D test register (ADTES)

This register is used to select the item subject to A/D conversion from the positive reference voltage or negative reference voltage for the converter, an analog input channel (ANIxx), temperature sensor output, or the internal reference voltage for A/D converter (1.45 V).

When using this register to test the converter, set as follows.

- For zero-scale measurement, select the negative reference voltage as the item subject to A/D conversion.
- For full-scale measurement, select the positive reference voltage as the item subject to A/D conversion.

The ADTES register can be set by an 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 19 - 14 Format of A/D test register (ADTES)

Address: F0013H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
ADTES	0	0	0	0	0	0	ADTES1	ADTES0

ADTES1	ADTES0	Item subject to A/D conversion
0	0	ANIxx/temperature sensor output voltage[Note]/internal reference voltage (1.45 V)[Note] One specified by using the analog input channel specification register (ADS)
1	0	Negative reference voltage (Vss)
1	1	Positive reference voltage. (Select by using the ADREFP1 and ADREFP0 bits of A/D converter mode register (ADM2).)
Other than above		Setting prohibited

Note The temperature sensor output voltage and internal reference voltage (1.45 V) can be selected only in the HS (high-speed main) mode.

Caution Be sure to clear bits 2 to 7 to "0".

19.3.11 Registers that control port functions of analog input pins

Set the registers that control the port functions for the port pins with which the analog input pin functions of the A/D converter are multiplexed (port mode registers (PMxx) and port mode control registers (PMCxx)). For details, see **4.4.1 Port mode registers (PMxx)** and **4.4.6 Port mode control registers (PMCxx)**.

Using the ANI8 to ANI11 pins for analog input to the A/D converter requires setting the corresponding bits in the port mode register (PMxx) and port mode control register (PMCxx) to 1.

19.4 A/D Converter Conversion Operations

The A/D converter conversion operations are described below.

<1> The voltage input to the selected analog input channel is sampled by the sample & hold circuit.

<2> When sampling has been done for a certain time, the sample & hold circuit is placed in the hold state and the sampled voltage is held until the A/D conversion operation has ended.

<3> Bit 9 of the successive approximation register (SAR) is set. The series resistor string voltage tap is set to (1/2) AV_{REF} by the tap selector.

<4> The voltage difference between the series resistor string voltage tap and sampled voltage is compared by the voltage comparator. If the analog input is greater than (1/2) AV_{REF}, the MSB bit of the SAR register remains set to 1. If the analog input is smaller than (1/2) AV_{REF}, the MSB bit is reset to 0.

<5> Next, bit 8 of the SAR register is automatically set to 1, and the operation proceeds to the next comparison. The series resistor string voltage tap is selected according to the preset value of bit 9, as described below.

- Bit 9 = 1: (3/4) AV_{REF}
- Bit 9 = 0: (1/4) AV_{REF}

The voltage tap and sampled voltage are compared and bit 8 of the SAR register is manipulated as follows.

- Sampled voltage ≥ Voltage tap: Bit 8 = 1
- Sampled voltage < Voltage tap: Bit 8 = 0

<6> Comparison is continued in this way up to bit 0 of the SAR register.

<7> Upon completion of the comparison of 10 bits, an effective digital result value remains in the SAR register, and the result value is transferred to the A/D conversion result register (ADCR, ADCRH) and then latched Note 1. At the same time, the A/D conversion end interrupt request (INTAD) can also be generated.

<8> Repeat steps <1> to <7>, until the ADCS bit is cleared to 0 Note 2.
To stop the A/D converter, clear the ADCS bit to 0.

Note 1. If the A/D conversion result is outside the A/D conversion result range specified by the ADRCK bit and the ADUL and ADLL registers (see **Figure 19 - 8**), the A/D conversion result interrupt request signal is not generated and no A/D conversion results are stored in the ADCR and ADCRH registers.

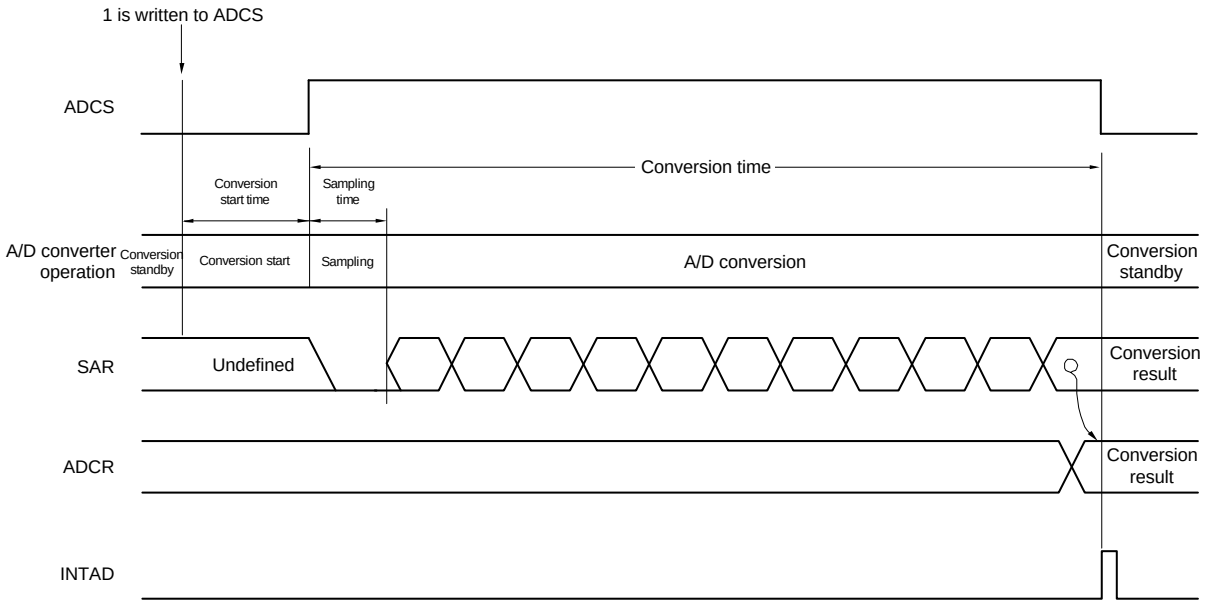
Note 2. While in the sequential conversion mode, the ADCS flag is not automatically cleared to 0. This flag is not automatically cleared to 0 while in the one-shot conversion mode of the hardware trigger no-wait mode, either. Instead, 1 is retained.

Remark 1. Two types of the A/D conversion result registers are available.

- ADCR register (16 bits): Store 10-bit A/D conversion value
- ADCRH register (8 bits): Store 8-bit A/D conversion value

Remark 2. AV_{REF}: The positive reference voltage of the A/D converter. This can be selected from the internal reference voltage (1.45 V) and V_{DD}.

Figure 19 - 15 Conversion Operation of A/D Converter (Software Trigger Mode)



In one-shot conversion mode, the ADCS bit is automatically cleared to 0 after completion of A/D conversion.

In sequential conversion mode, A/D conversion operations proceed continuously until the software clears bit 7 (ADCS) of the A/D converter mode register 0 (ADM0) to 0.

Writing to the analog input channel specification register (ADS) during A/D conversion interrupts the current conversion after which A/D conversion of the analog input specified by the ADS register proceeds. Data from the A/D conversion that was in progress are discarded.

Reset signal generation clears the A/D conversion result register (ADCR, ADCRH) to 0000H or 00H.

19.5 Input Voltage and Conversion Results

The relationship between the analog input voltage input to the analog input pins (ANI8 to ANI14) and the theoretical A/D conversion result (stored in the 10-bit A/D conversion result register (ADCR)) is shown by the following expression.

$$SAR = INT\left(\frac{V_{AIN}}{AV_{REF}} \times 1024 + 0.5\right)$$

$$ADCR = SAR \times 64$$

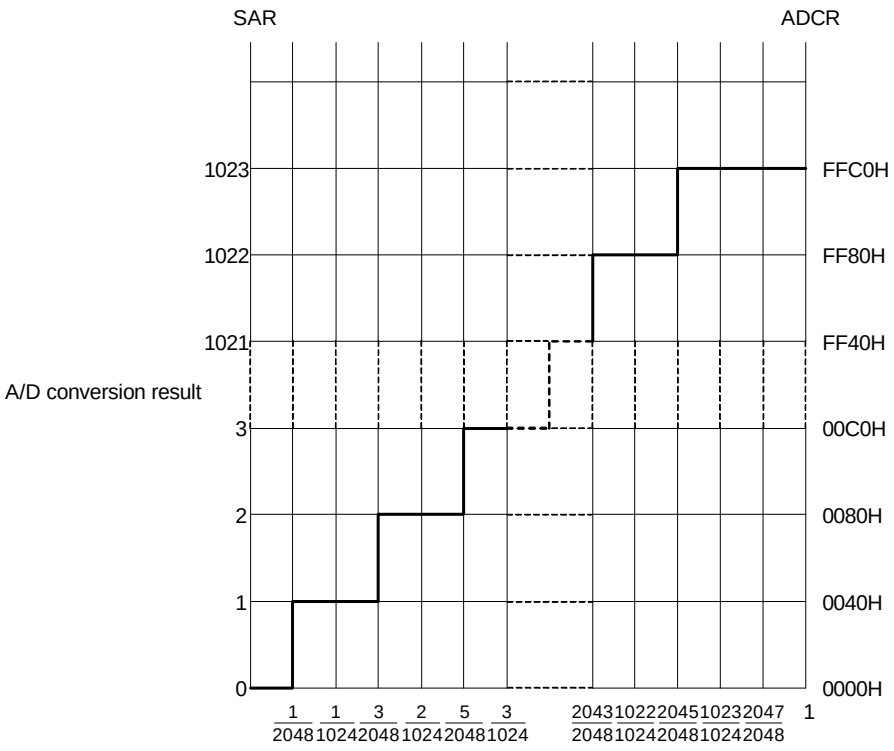
or

$$\left(\frac{ADCR}{64} - 0.5\right) \times \frac{AV_{REF}}{1024} \leq V_{AIN} < \left(\frac{ADCR}{64} + 0.5\right) \times \frac{AV_{REF}}{1024}$$

where, INT( ): Function which returns integer part of value in parentheses
V_{AIN}: Analog input voltage
AV_{REF}: AV_{REF} pin voltage
ADCR: A/D conversion result register (ADCR) value
SAR: Successive approximation register

Figure 19 - 16 shows the Relationship Between Analog Input Voltage and A/D Conversion Result.

Figure 19 - 16 Relationship Between Analog Input Voltage and A/D Conversion Result



Remark AV_{REF}: The positive reference voltage of the A/D converter. This can be selected from the internal reference voltage (1.45 V) and V_{DD}.

19.6 A/D Converter Operation Modes

The operation of each A/D converter mode is described below. In addition, the procedure for specifying each mode is described in **19.7 A/D Converter Setup Flowchart**.

19.6.1 Software trigger mode (sequential conversion mode)

<1> In the stop status, the ADCE bit of A/D converter mode register 0 (ADM0) is set to 1, and the system enters the A/D conversion standby status.

<2> After the software counts up to the stabilization wait time (1 μs), the ADCS bit of the ADM0 register is set to 1 to perform the A/D conversion of the analog input specified by the analog input channel specification register (ADS).

<3> When A/D conversion ends, the conversion result is stored in the A/D conversion result register (ADCR, ADCRH), and the A/D conversion end interrupt request signal (INTAD) is generated. After A/D conversion ends, the next A/D conversion immediately starts.

<4> When ADCS is overwritten with 1 during conversion operation, the current A/D conversion is interrupted, and conversion restarts. The partially converted data is discarded.

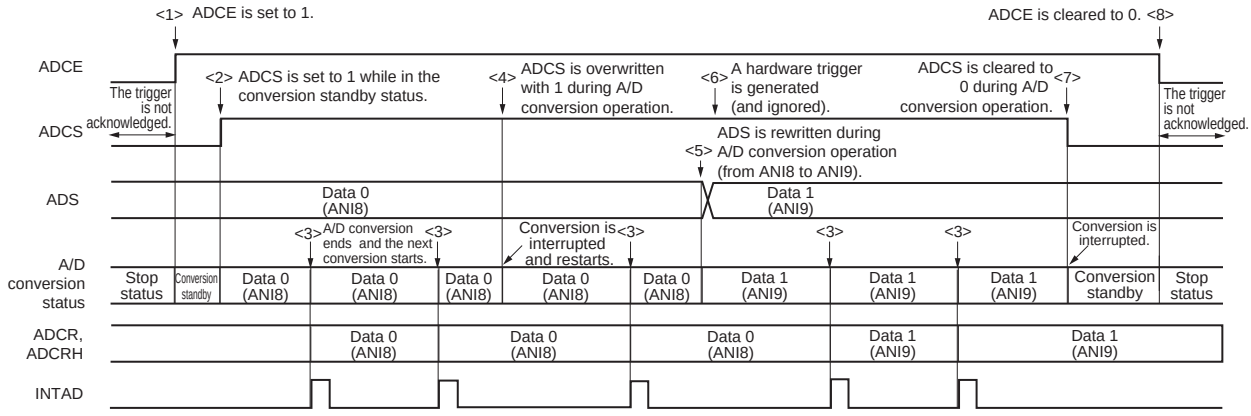
<5> When the value of the ADS register is rewritten or overwritten during conversion operation, the current A/D conversion is interrupted, and A/D conversion is performed on the analog input respecified by the ADS register. The partially converted data is discarded.

<6> Even if a hardware trigger is input during conversion operation, A/D conversion does not start.

<7> When ADCS is cleared to 0 during conversion operation, the current A/D conversion is interrupted, and the system enters the A/D conversion standby status.

<8> When ADCE is cleared to 0 while in the A/D conversion standby status, the A/D converter enters the stop status. When ADCE = 0, specifying 1 for ADCS is ignored and A/D conversion does not start.

Figure 19 - 17 Example of Software Trigger Mode (Sequential Conversion Mode) Operation Timing



19.6.2 Software trigger mode (one-shot conversion mode)

<1> In the stop status, the ADCE bit of A/D converter mode register 0 (ADM0) is set to 1, and the system enters the A/D conversion standby status.

<2> After the software counts up to the stabilization wait time (1 μs), the ADCS bit of the ADM0 register is set to 1 to perform the A/D conversion of the analog input specified by the analog input channel specification register (ADS).

<3> When A/D conversion ends, the conversion result is stored in the A/D conversion result register (ADCR, ADCRH), and the A/D conversion end interrupt request signal (INTAD) is generated.

<4> After A/D conversion ends, the ADCS bit is automatically cleared to 0, and the system enters the A/D conversion standby status.

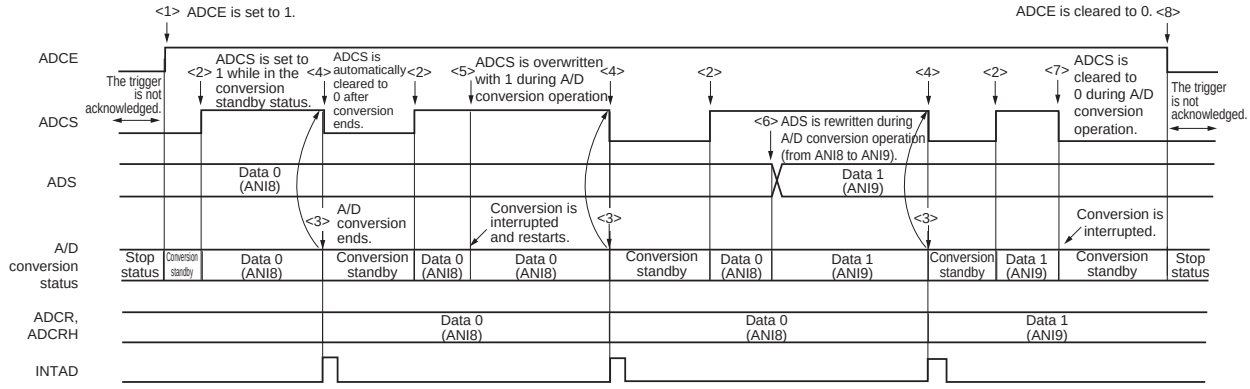
<5> When ADCS is overwritten with 1 during conversion operation, the current A/D conversion is interrupted, and conversion restarts. The partially converted data is discarded.

<6> When the value of the ADS register is rewritten or overwritten during conversion operation, the current A/D conversion is interrupted, and A/D conversion is performed on the analog input respecified by the ADS register. The partially converted data is discarded.

<7> When ADCS is cleared to 0 during conversion operation, the current A/D conversion is interrupted, and the system enters the A/D conversion standby status.

<8> When ADCE is cleared to 0 while in the A/D conversion standby status, the A/D converter enters the stop status. When ADCE = 0, specifying 1 for ADCS is ignored and A/D conversion does not start. In addition, A/D conversion does not start even if a hardware trigger is input while in the A/D conversion standby status.

Figure 19 - 18 Example of Software Trigger Mode (One-Shot Conversion Mode) Operation Timing



19.6.3 Hardware trigger no-wait mode (sequential conversion mode)

<1> In the stop status, the ADCE bit of A/D converter mode register 0 (ADM0) is set to 1, and the system enters the A/D conversion standby status.

<2> After the software counts up to the stabilization wait time (1 μs), the ADCS bit of the ADM0 register is set to 1 to place the system in the hardware trigger standby status (and conversion does not start at this stage). Note that, while in this status, A/D conversion does not start even if ADCS is set to 1.

<3> If a hardware trigger is input while ADCS = 1, A/D conversion is performed on the analog input specified by the analog input channel specification register (ADS).

<4> When A/D conversion ends, the conversion result is stored in the A/D conversion result register (ADCR, ADCRH), and the A/D conversion end interrupt request signal (INTAD) is generated. After A/D conversion ends, the next A/D conversion immediately starts.

<5> If a hardware trigger is input during conversion operation, the current A/D conversion is interrupted, and conversion restarts. The partially converted data is discarded.

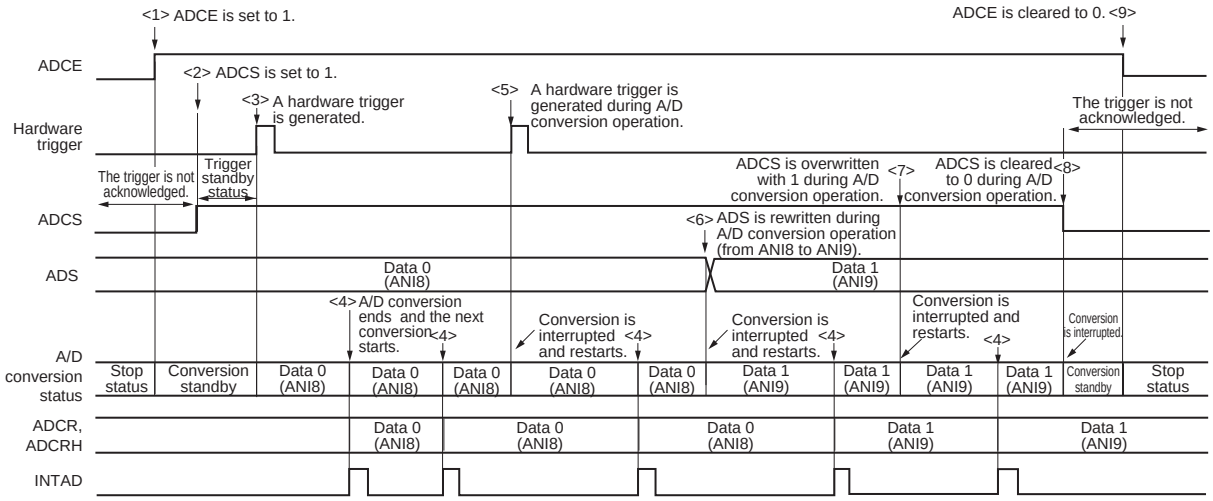
<6> When the value of the ADS register is rewritten or overwritten during conversion operation, the current A/D conversion is interrupted, and A/D conversion is performed on the analog input respecified by the ADS register. The partially converted data is discarded.

<7> When ADCS is overwritten with 1 during conversion operation, the current A/D conversion is interrupted, and conversion restarts. The partially converted data is discarded.

<8> When ADCS is cleared to 0 during conversion operation, the current A/D conversion is interrupted, and the system enters the A/D conversion standby status. However, the A/D converter does not stop in this status.

<9> When ADCE is cleared to 0 while in the A/D conversion standby status, the A/D converter enters the stop status. When ADCS = 0, inputting a hardware trigger is ignored and A/D conversion does not start.

Figure 19 - 19 Example of Hardware Trigger No-Wait Mode (Sequential Conversion Mode) Operation Timing



19.6.4 Hardware trigger no-wait mode (one-shot conversion mode)

<1> In the stop status, the ADCE bit of A/D converter mode register 0 (ADM0) is set to 1, and the system enters the A/D conversion standby status.

<2> After the software counts up to the stabilization wait time (1 μs), the ADCS bit of the ADM0 register is set to 1 to place the system in the hardware trigger standby status (and conversion does not start at this stage). Note that, while in this status, A/D conversion does not start even if ADCS is set to 1.

<3> If a hardware trigger is input while ADCS = 1, A/D conversion is performed on the analog input specified by the analog input channel specification register (ADS).

<4> When A/D conversion ends, the conversion result is stored in the A/D conversion result register (ADCR, ADCRH), and the A/D conversion end interrupt request signal (INTAD) is generated.

<5> After A/D conversion ends, the ADCS bit remains set to 1, and the system enters the A/D conversion standby status.

<6> If a hardware trigger is input during conversion operation, the current A/D conversion is interrupted, and conversion restarts. The partially converted data is discarded.

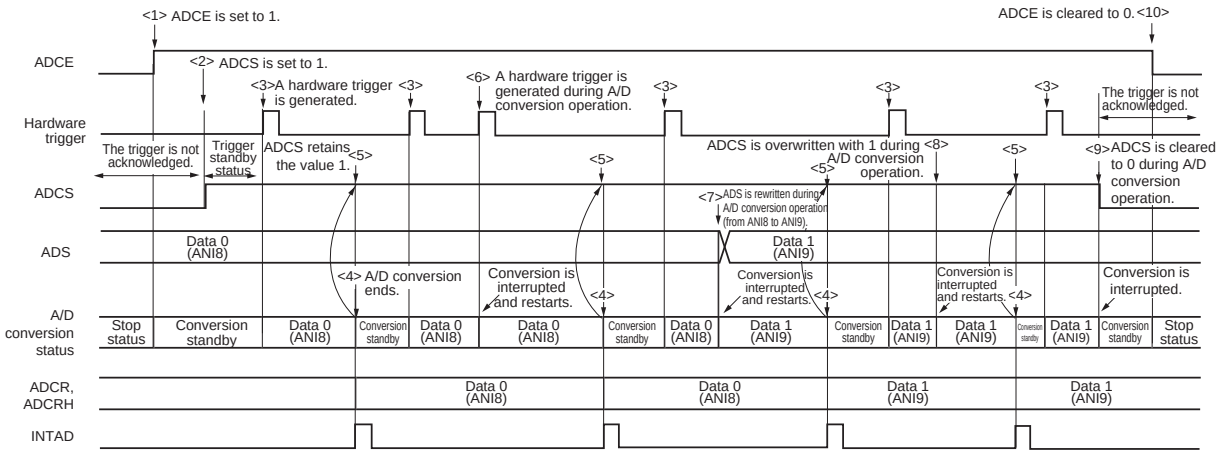
<7> When the value of the ADS register is rewritten or overwritten during conversion operation, the current A/D conversion is interrupted, and A/D conversion is performed on the analog input respecified by the ADS register. The partially converted data is discarded.

<8> When ADCS is overwritten with 1 during conversion operation, the current A/D conversion is interrupted, and conversion restarts. The partially converted data is discarded.

<9> When ADCS is cleared to 0 during conversion operation, the current A/D conversion is interrupted, and the system enters the A/D conversion standby status. However, the A/D converter does not stop in this status.

<10> When ADCE is cleared to 0 while in the A/D conversion standby status, the A/D converter enters the stop status. When ADCS = 0, inputting a hardware trigger is ignored and A/D conversion does not start.

Figure 19 - 20 Example of Hardware Trigger No-Wait Mode (One-Shot Conversion Mode) Operation Timing



19.6.5 Hardware trigger wait mode (sequential conversion mode)

<1> In the stop status, the ADCE bit of A/D converter mode register 0 (ADM0) is set to 1, and the system enters the hardware trigger standby status.

<2> If a hardware trigger is input while in the hardware trigger standby status, A/D conversion is performed on the analog input specified by the analog input channel specification register (ADS). The ADCS bit of the ADM0 register is automatically set to 1 according to the hardware trigger input.

<3> When A/D conversion ends, the conversion result is stored in the A/D conversion result register (ADCR, ADCRH), and the A/D conversion end interrupt request signal (INTAD) is generated. After A/D conversion ends, the next A/D conversion immediately starts. (At this time, no hardware trigger is necessary.)

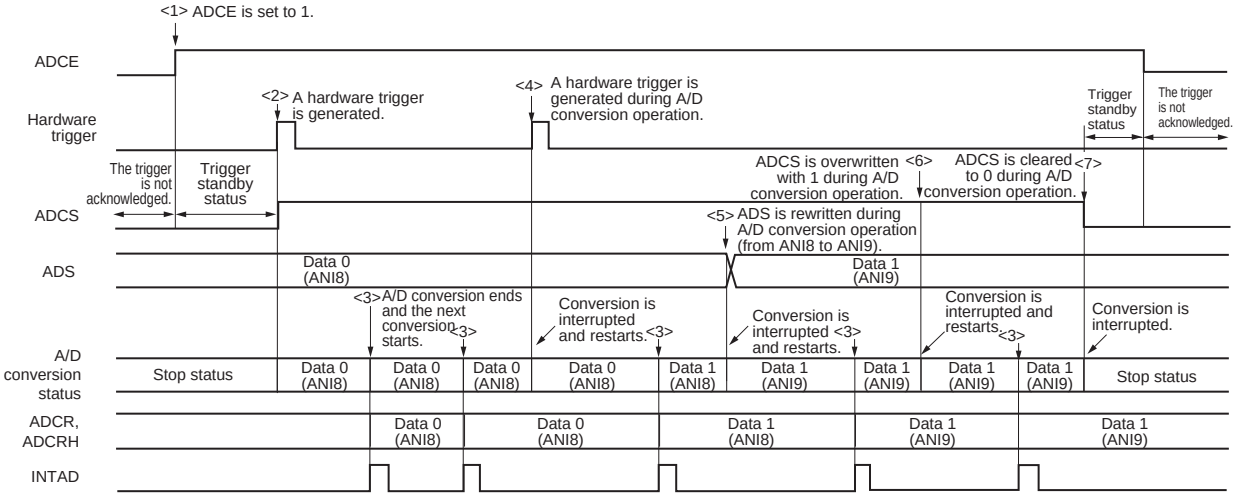
<4> If a hardware trigger is input during conversion operation, the current A/D conversion is interrupted, and conversion restarts. The partially converted data is discarded.

<5> When the value of the ADS register is rewritten or overwritten during conversion operation, the current A/D conversion is interrupted, and A/D conversion is performed on the analog input respecified by the ADS register. The partially converted data is discarded.

<6> When ADCS is overwritten with 1 during conversion operation, the current A/D conversion is interrupted, and conversion restarts. The partially converted data is discarded.

<7> When ADCS is cleared to 0 during conversion operation, the current A/D conversion is interrupted, the system enters the hardware trigger standby status, and the A/D converter enters the stop status. When ADCE = 0, inputting a hardware trigger is ignored and A/D conversion does not start.

Figure 19 - 21 Example of Hardware Trigger Wait Mode (Sequential Conversion Mode) Operation Timing



19.6.6 Hardware trigger wait mode (one-shot conversion mode)

<1> In the stop status, the ADCE bit of A/D converter mode register 0 (ADM0) is set to 1, and the system enters the hardware trigger standby status.

<2> If a hardware trigger is input while in the hardware trigger standby status, A/D conversion is performed on the analog input specified by the analog input channel specification register (ADS). The ADCS bit of the ADM0 register is automatically set to 1 according to the hardware trigger input.

<3> When A/D conversion ends, the conversion result is stored in the A/D conversion result register (ADCR, ADCRH), and the A/D conversion end interrupt request signal (INTAD) is generated.

<4> After A/D conversion ends, the ADCS bit is automatically cleared to 0, and the A/D converter enters the stop status.

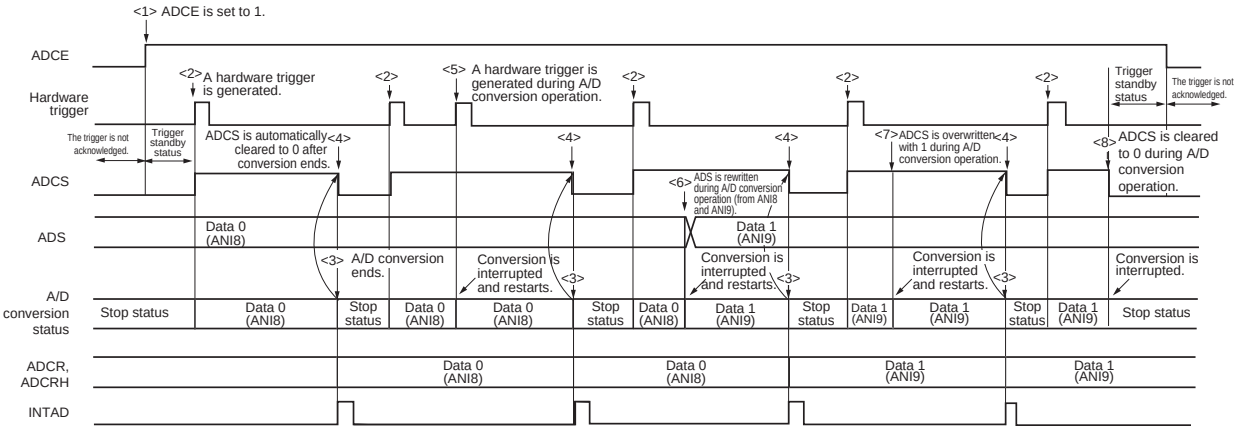
<5> If a hardware trigger is input during conversion operation, the current A/D conversion is interrupted, and conversion restarts. The partially converted data is discarded.

<6> When the value of the ADS register is rewritten or overwritten during conversion operation, the current A/D conversion is interrupted, and A/D conversion is performed on the analog input respecified by the ADS register. The partially converted data is discarded.

<7> When ADCS is overwritten with 1 during conversion operation, the current A/D conversion is interrupted, and conversion restarts. The partially converted data is initialized.

<8> When ADCS is cleared to 0 during conversion operation, the current A/D conversion is interrupted, the system enters the hardware trigger standby status, and the A/D converter enters the stop status. When ADCE = 0, inputting a hardware trigger is ignored and A/D conversion does not start.

Figure 19 - 22 Example of Hardware Trigger Wait Mode (One-Shot Conversion Mode) Operation Timing

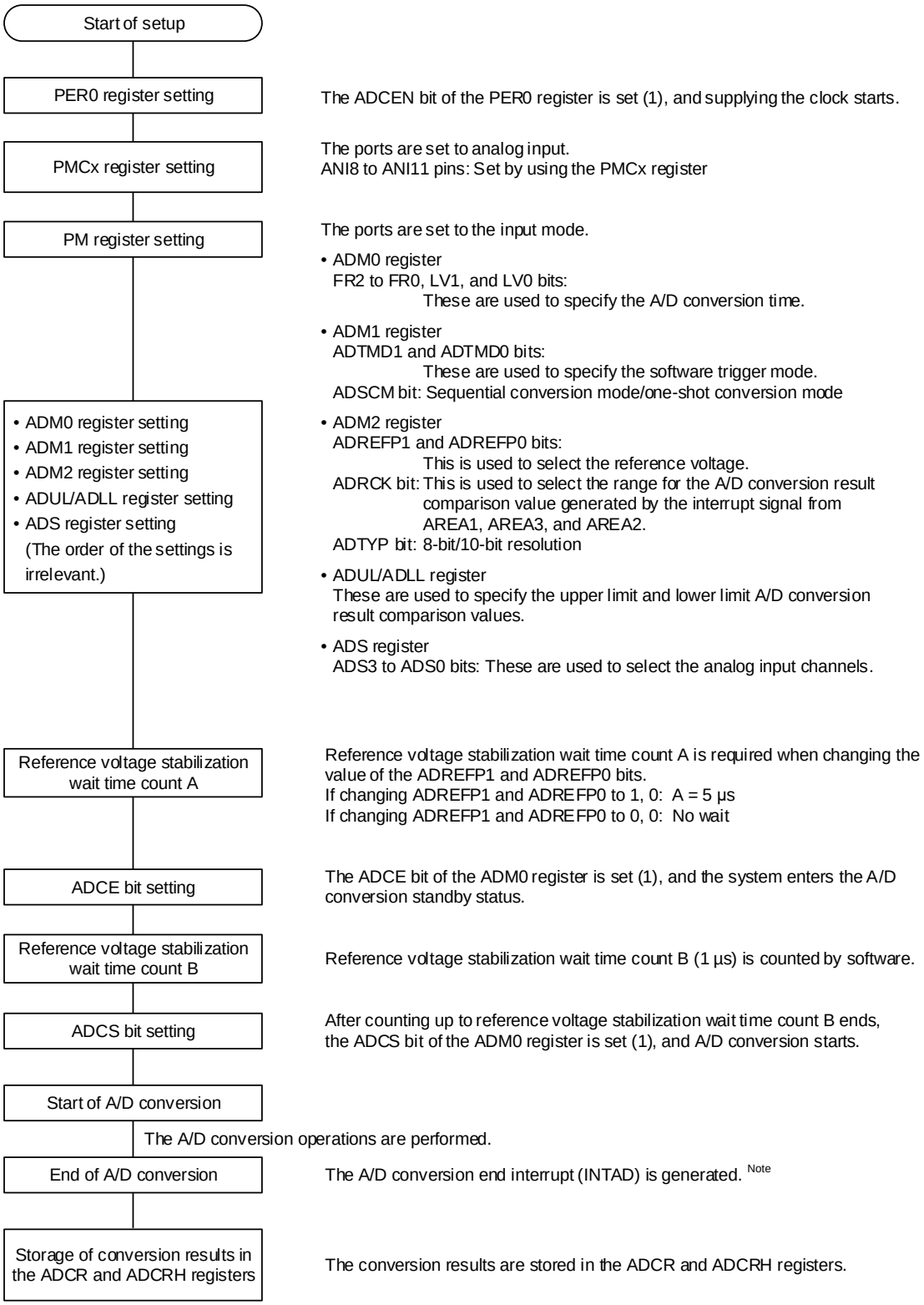


19.7 A/D Converter Setup Flowchart

The A/D converter setup flowchart in each operation mode is described below.

19.7.1 Setting up software trigger mode

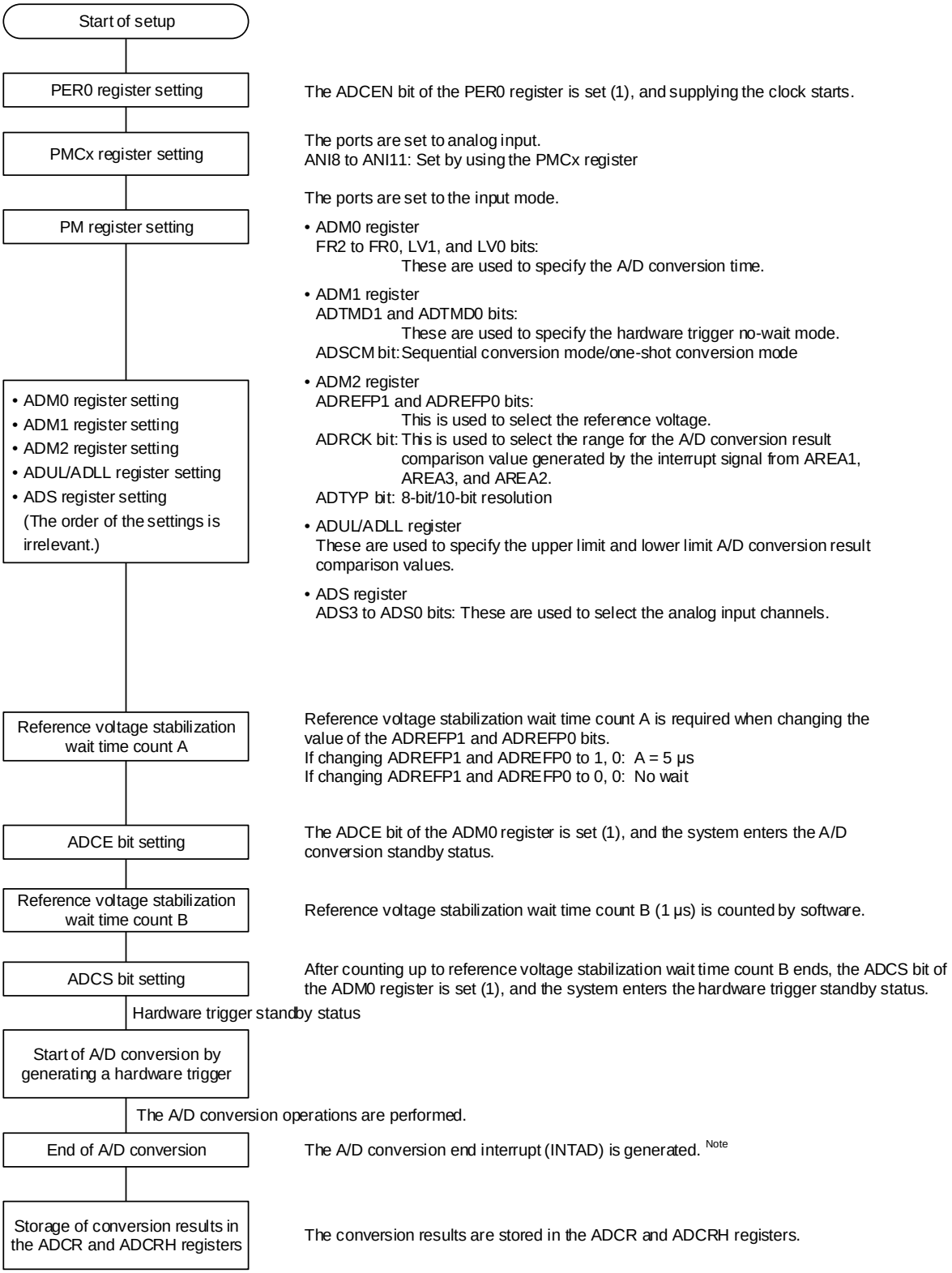
Figure 19 - 23 Setting up Software Trigger Mode



Note Depending on the settings of the ADRCK bit and ADUL/ADLL register, there is a possibility of no interrupt signal being generated. In this case, the results are not stored in the ADCR, ADCRH register.

19.7.2 Setting up hardware trigger no-wait mode

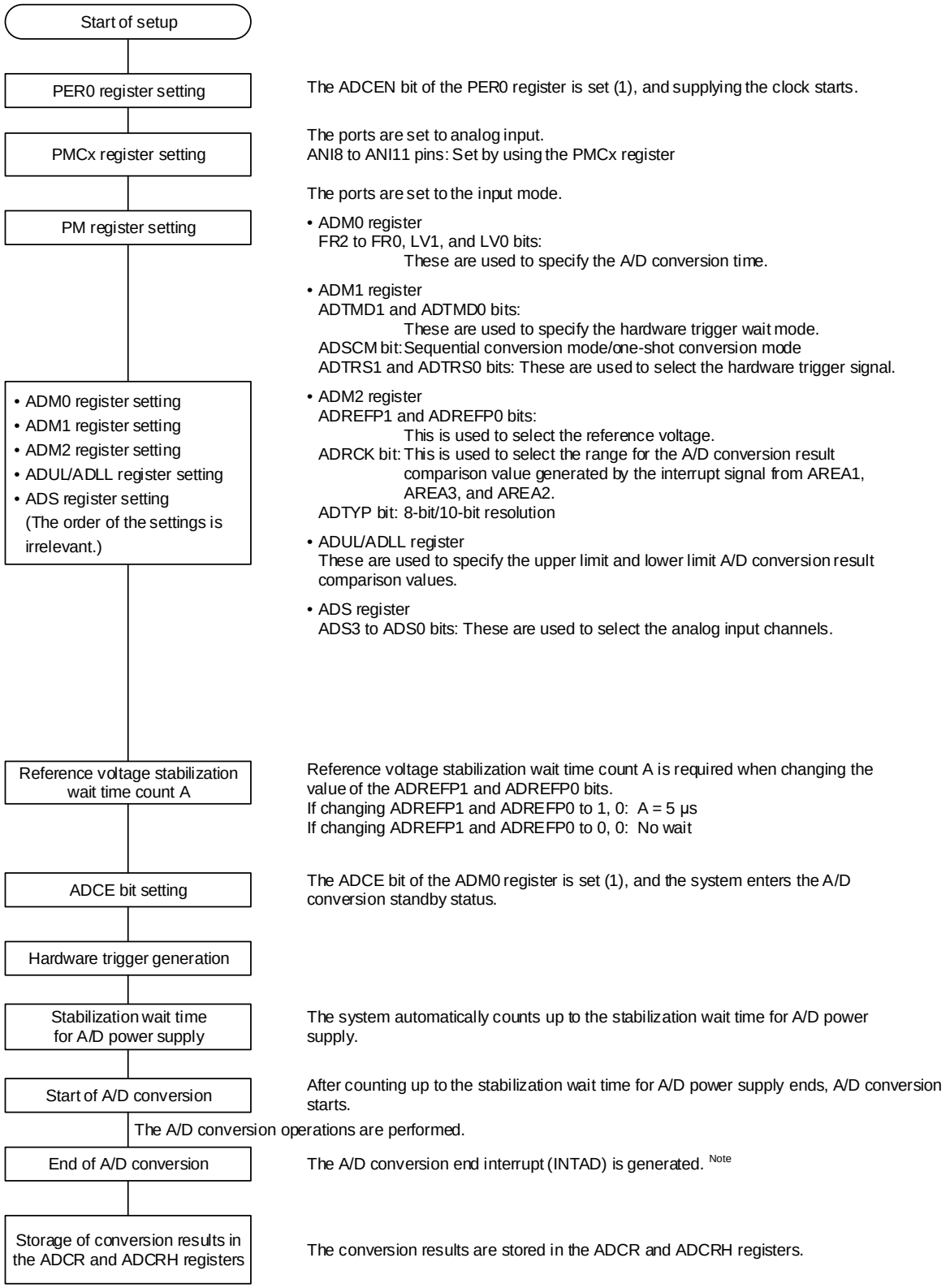
Figure 19 - 24 Setting up Hardware Trigger No-Wait Mode



Note Depending on the settings of the ADRCK bit and ADUL/ADLL register, there is a possibility of no interrupt signal being generated. In this case, the results are not stored in the ADCR, ADCRH register.

19.7.3 Setting up hardware trigger wait mode

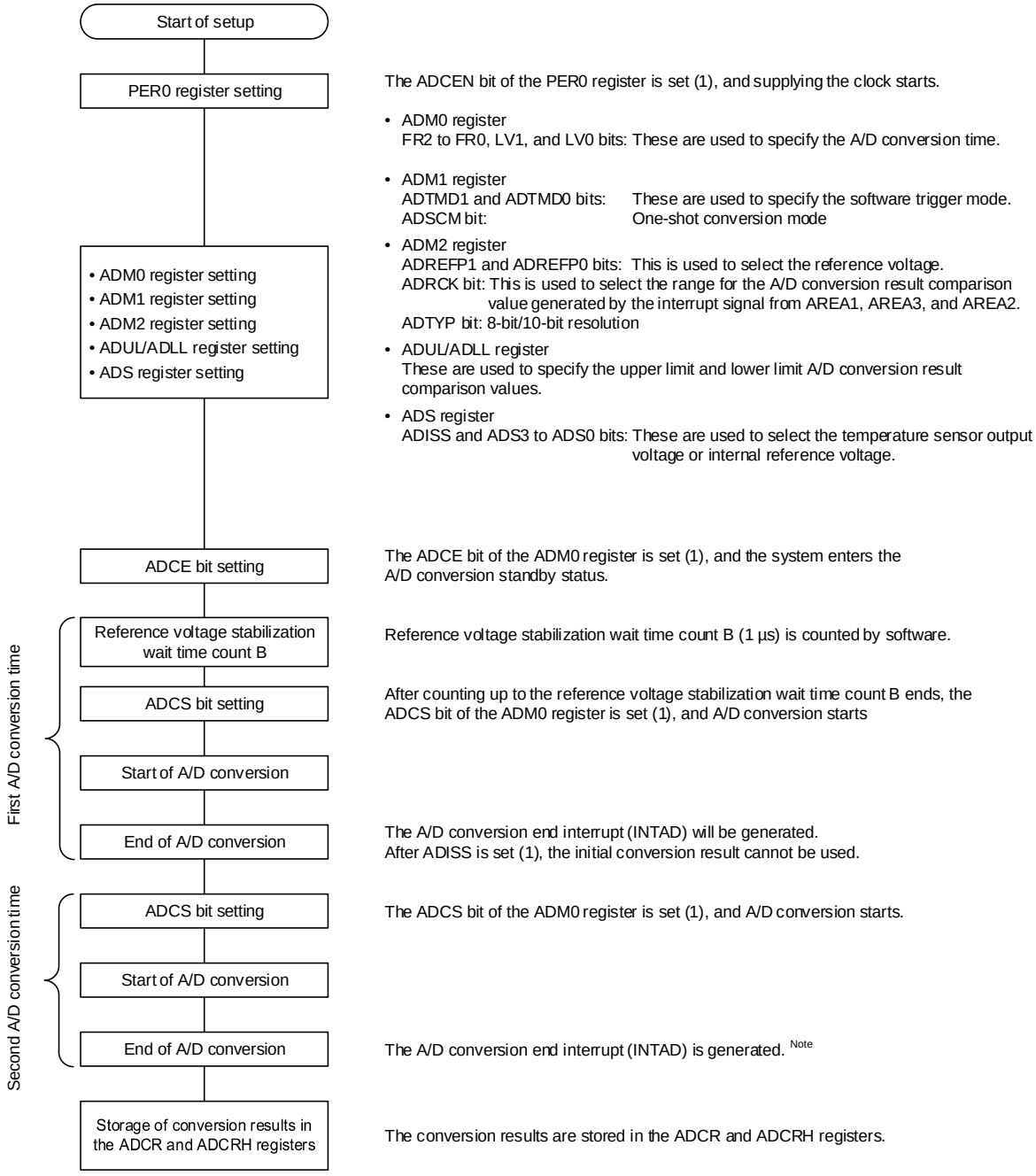
Figure 19 - 25 Setting up Hardware Trigger Wait Mode



Note Depending on the settings of the ADRCK bit and ADUL/ADLL register, there is a possibility of no interrupt signal being generated. In this case, the results are not stored in the ADCR, ADCRH register.

19.7.4 Setup when temperature sensor output voltage/internal reference voltage is selected (example for software trigger mode and one-shot conversion mode)

Figure 19 - 26 Setup when temperature sensor output voltage/internal reference voltage is selected

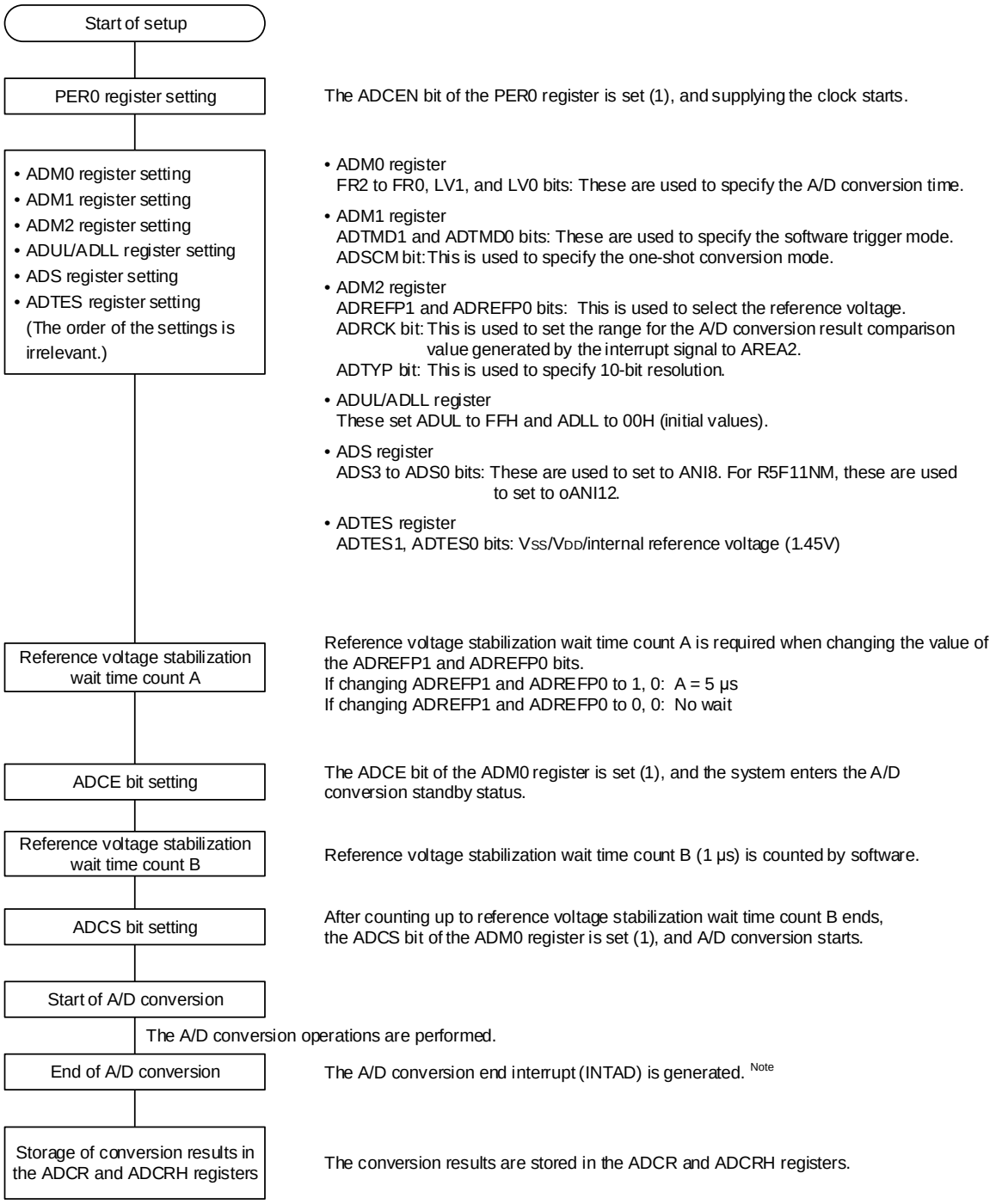


Note Depending on the settings of the ADRCK bit and ADUL/ADLL register, there is a possibility of no interrupt signal being generated. In this case, the results are not stored in the ADCR, ADCRH register.

Caution This setting can be used only in HS (high-speed main) mode.

19.7.5 Setting up test mode

Figure 19 - 27 Setting up Test Mode



Note Depending on the settings of the ADRCK bit and ADUL/ADLL register, there is a possibility of no interrupt signal being generated. In this case, the results are not stored in the ADCR, ADCRH register.

Caution For the procedure for testing the A/D converter, see 31.3.8 A/D test function.

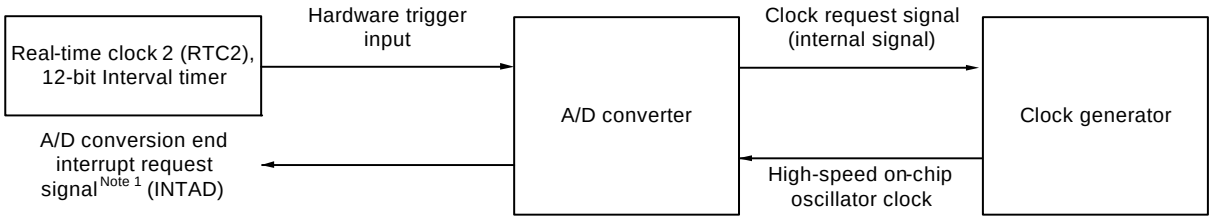
19.8 SNOOZE Mode Function

In the SNOOZE mode, A/D conversion is triggered by inputting a hardware trigger in the STOP mode. Normally, A/D conversion is stopped while in the STOP mode, but, by using the SNOOZE mode, A/D conversion can be performed without operating the CPU by inputting a hardware trigger. This is effective for reducing the operation current.
If the A/D conversion result range is specified using the ADUL and ADLL registers, A/D conversion results can be judged at a certain interval of time in SNOOZE mode. Using this function enables power supply voltage monitoring and input key judgment based on A/D inputs.

In the SNOOZE mode, only the following conversion mode can be used:
• Hardware trigger wait mode (one-shot conversion mode)

Caution That the SNOOZE mode can only be specified when the high-speed on-chip oscillator clock is selected for f_{CLK}.

Figure 19 - 28 Block Diagram When Using SNOOZE Mode Function



When using the SNOOZE mode function, specify the initial hardware trigger and wait mode settings for each register before shifting to the STOP mode. (For details about these settings, see **19.7.3 Setting up hardware trigger wait mode** Note 2.) At this time, bit 2 (AWC) of A/D converter mode register 2 (ADM2) is set to 1. After the initial settings are specified, bit 0 (ADCE) of A/D converter mode register 0 (ADM0) is set to 1.
If a hardware trigger is input after switching to the STOP mode, the high-speed on-chip oscillator clock is supplied to the A/D converter. After supplying this clock, the system automatically counts up to the A/D power supply stabilization wait time, and then A/D conversion starts.
The SNOOZE mode operation after A/D conversion ends differs depending on whether an interrupt signal is generated Note 1.

Note 1. Depending on the setting of the A/D conversion result comparison function (ADRCK bit, ADUL/ADLL register), there is a possibility of no interrupt signal being generated.
Note 2. Be sure to set the ADM1 register to E1H, E2H or E3H.

Remark The hardware trigger is event selected by ELC, INTRTC or INTIT.
Specify the hardware trigger by using the A/D Converter Mode Register 1 (ADM1).

(1) If an interrupt is generated after A/D conversion ends

If the A/D conversion result value is inside the range of values specified by the A/D conversion result comparison function (which is set up by using the ADRCK bit and ADUL/ADLL register), the A/D conversion end interrupt request signal (INTAD) is generated.

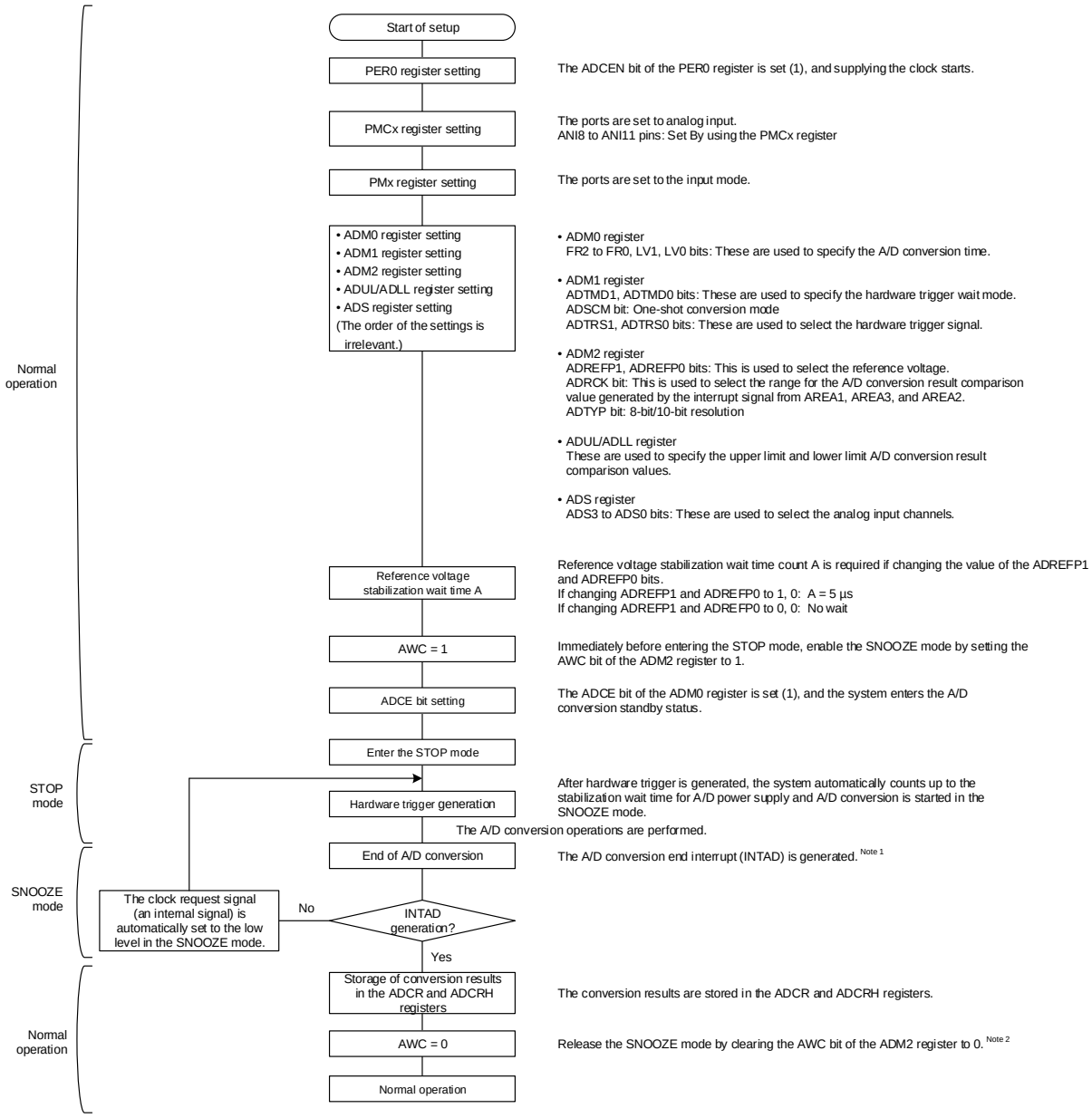
When A/D conversion ends and an A/D conversion end interrupt request signal (INTAD) is generated, the A/D converter returns to normal operation mode from SNOOZE mode. At this time, be sure to clear bit 2 (AWC = 0: SNOOZE mode release) of the A/D converter mode register 2 (ADM2). If the AWC bit is left set to 1, A/D conversion will not start normally in the subsequent SNOOZE or normal operation mode.

(2) If no interrupt is generated after A/D conversion ends

If the A/D conversion result value is outside the range of values specified by the A/D conversion result comparison function (which is set up by using the ADRCK bit and ADUL/ADLL register), the A/D conversion end interrupt request signal (INTAD) is not generated.

If the A/D conversion end interrupt request signal (INTAD) is not generated after A/D conversion ends, the clock request signal (an internal signal) is automatically set to the low level, and supplying the high-speed on-chip oscillator clock stops. If a hardware trigger is input later, A/D conversion work is again performed in the SNOOZE mode.

Figure 19 - 29 Flowchart for Setting up SNOOZE Mode



Note 1. If the A/D conversion end interrupt request signal (INTAD) is not generated by setting ADRCK bit and ADUL/ADLL register, the result is not stored in the ADCR and ADCRH registers.
The system enters the STOP mode again. If a hardware trigger is input later, A/D conversion operation is again performed in the SNOOZE mode.

Note 2. If the AWC bit is left set to 1, A/D conversion will not start normally in spite of the subsequent SNOOZE or normal operation mode. Be sure to clear the AWC bit to 0.

19.9 How to Read A/D Converter Characteristics Table

Here, special terms unique to the A/D converter are explained.

(1) Resolution

This is the minimum analog input voltage that can be identified. That is, the percentage of the analog input voltage per bit of digital output is called 1LSB (Least Significant Bit). The percentage of 1LSB with respect to the full scale is expressed by %FSR (Full Scale Range).

1LSB is as follows when the resolution is 10 bits.

$1\ LSB = 1/2^{10} = 1/1024$
$= 0.098\%FSR$

Accuracy has no relation to resolution, but is determined by overall error.

(2) Overall error

This shows the maximum error value between the actual measured value and the theoretical value.
Zero-scale error, full-scale error, integral linearity error, and differential linearity errors that are combinations of these express the overall error.
Note that the quantization error is not included in the overall error in the characteristics table.

(3) Quantization error

When analog values are converted to digital values, a ±1/2LSB error naturally occurs. In an A/D converter, an analog input voltage in a range of ±1/2LSB is converted to the same digital code, so a quantization error cannot be avoided.
Note that the quantization error is not included in the overall error, zero-scale error, full-scale error, integral linearity error, and differential linearity error in the characteristics table.

Figure 19 - 30 Overall Error

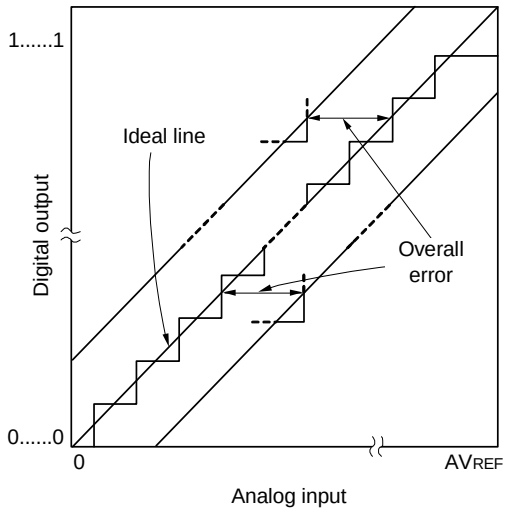
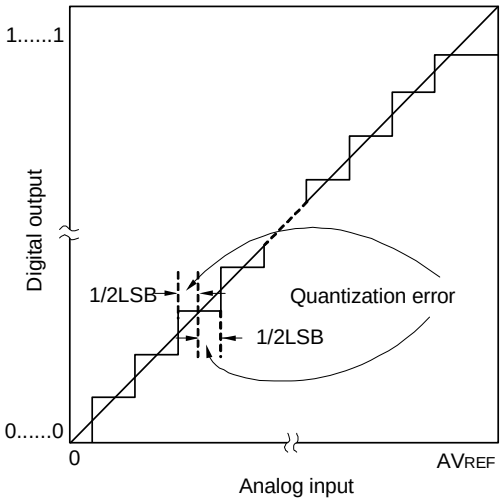


Figure 19 - 31 Quantization Error



(4) Zero-scale error

This shows the difference between the actual measurement value of the analog input voltage and the theoretical value (1/2LSB) when the digital output changes from 0.....000 to 0.....001.

If the actual measurement value is greater than the theoretical value, it shows the difference between the actual measurement value of the analog input voltage and the theoretical value (3/2LSB) when the digital output changes from 0……001 to 0……010.

(5) Full-scale error

This shows the difference between the actual measurement value of the analog input voltage and the theoretical value (Full-scale - 3/2LSB) when the digital output changes from 1.....110 to 1.....111.

(6) Integral linearity error

This shows the degree to which the conversion characteristics deviate from the ideal linear relationship. It expresses the maximum value of the difference between the actual measurement value and the ideal straight line when the zero-scale error and full-scale error are 0.

(7) Differential linearity error

While the ideal width of code output is 1LSB, this indicates the difference between the actual measurement value and the ideal value.

Figure 19 - 32 Zero-Scale Error

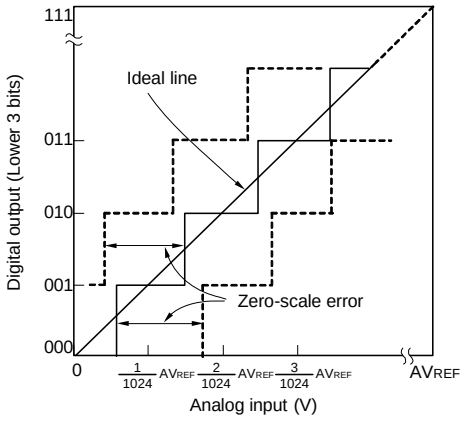


Figure 19 - 33 Full-Scale Error

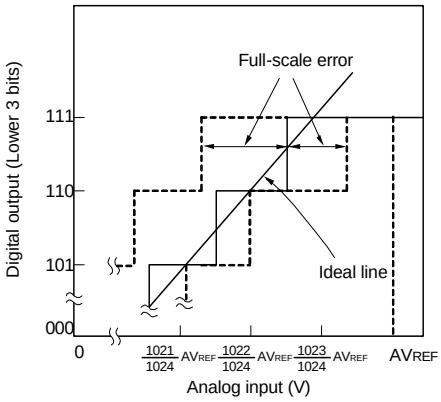


Figure 19 - 34 Integral Linearity Error

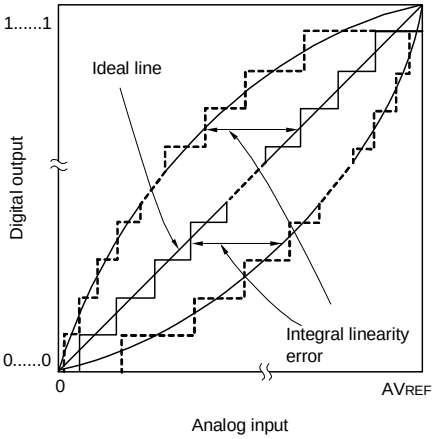
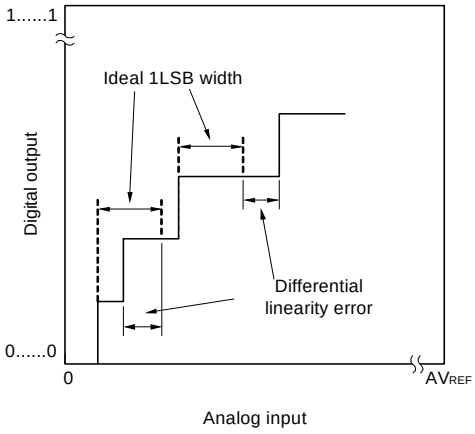


Figure 19 - 35 Differential Linearity Error



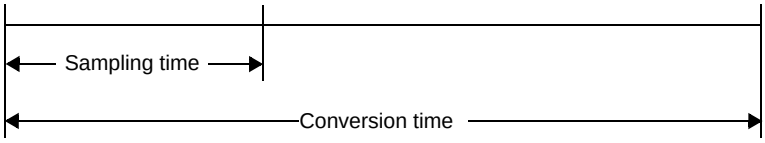
(8) Conversion time

This expresses the time from the start of sampling to when the digital output is obtained.

The sampling time is included in the conversion time in the characteristics table.

(9) Sampling time

This is the time the analog switch is turned on for the analog voltage to be sampled by the sample & hold circuit.



19.10 Cautions for A/D Converter

(1) Operating current in STOP mode

Shift to STOP mode after stopping the A/D converter (by setting bit 7 (ADCS) of A/D converter mode register 0 (ADM0) to 0). The operating current can be reduced by setting bit 0 (ADCE) of the ADM0 register to 0 at the same time.

To restart from the standby status, clear bit 2 (ADIF) of interrupt request flag register 1H (IF1H) to 0 and start operation.

(2) Input range of ANI8 to ANI14 pins

Observe the rated range of the ANI8 to ANI14 pins input voltage. If a voltage exceeding V_{DD} or below V_{SS} (even in the range of absolute maximum ratings) is input to an analog input channel, the converted value of that channel becomes undefined. In addition, the converted values of the other channels may also be affected.

When the internal reference voltage for A/D converter (1.45 V) is selected reference voltage for the positive of the A/D converter, do not input voltage exceeding the internal reference voltage to a pin selected by the ADS register. However, it is no problem that a pin not selected by the ADS register is input voltage exceeding the internal reference voltage.

Caution Internal reference voltage (1.45 V) can be selected only in the HS (high-speed main) mode.

(3) Conflicting operations

<1> Conflict between the A/D conversion result register (ADCR, ADCRH) write and the ADCR or ADCRH register read by instruction upon the end of conversion

The ADCR or ADCRH register read has priority. After the read operation, the new conversion result is written to the ADCR or ADCRH registers.

<2> Conflict between writing to the ADCR or ADCRH register and writing to A/D converter mode register 0 (ADM0) or analog input channel specification register (ADS) at the end of A/D conversion

Writing to the ADM0 and ADS registers has priority. Writing to the ADCR or ADCRH register is not performed, nor is the conversion end interrupt signal (INTAD) generated.

(4) Noise countermeasures

To maintain the 10-bit resolution, attention must be paid to noise input to the V_{DD} and ANI8 to ANI14 pins.

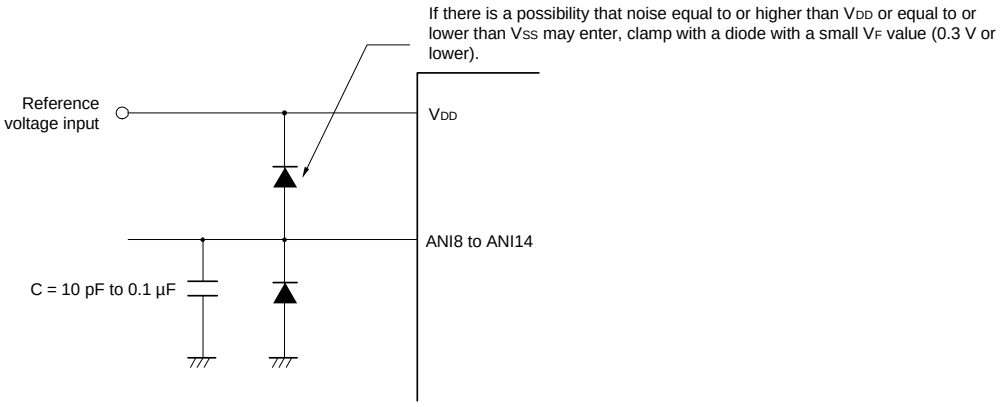
<1> Connect a capacitor with a low equivalent resistance and a good frequency response to the power supply.

<2> The higher the output impedance of the analog input source, the greater the influence. To reduce the noise, connecting external capacitor as shown in Figure 19 - 36 is recommended.

<3> Do not switch these pins with other pins during conversion.

<4> The accuracy is improved if the HALT mode is set immediately after the start of conversion.

Figure 19 - 36 Analog Input Pin Connection



(5) Analog input (ANIn) pins

<1> The analog input pins (ANI8 to ANI11) are also used as input port pins (P3 to P5, and P11).
When A/D conversion is performed with any of the ANI8 to ANI11 pins selected, do not change to the value output to P3 to P5 and P11 while conversion is in progress; otherwise the conversion resolution may be degraded.

<2> If a pin adjacent to a pin that is being A/D converted is used as a digital I/O port pin, the A/D conversion result might differ from the expected value due to a coupling noise. Be sure to prevent such a pulse from being input or output.

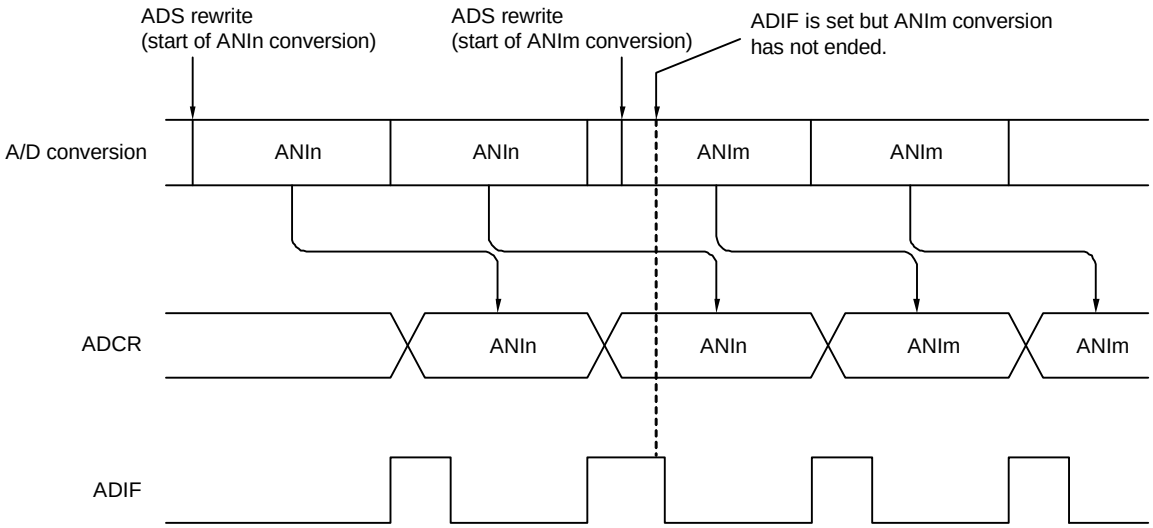
(6) Input impedance of analog input (ANIn) pins

This A/D converter charges a sampling capacitor for sampling during sampling time.
Therefore, only a leakage current flows when sampling is not in progress, and a current that charges the capacitor flows during sampling. Consequently, the input impedance fluctuates depending on whether sampling is in progress, and on the other states.
To make sure that sampling is effective, however, we recommend using the converter with analog input sources that have output impedances no greater than 1 kΩ. If a source has a higher output impedance, lengthen the sampling time or connect a larger capacitor (with a value of about 0.1 µF) to the pin from among ANI8 to ANI14 which the source is connected (see **Figure 19 - 36 Analog Input Pin Connection**). The sampling capacitor may be being charged while the setting of the ADCS bit is 0 and immediately after sampling is restarted and so is not defined at these times. Accordingly, the state of conversion is undefined after charging starts in the next round of conversion after the value of the ADCS bit has been 1 or when conversion is repeated. Thus, to secure full charging regardless of the size of fluctuations in the analog signal, ensure that the output impedances of the sources of analog inputs are low or secure sufficient time for the completion of conversion.

(7) Interrupt request flag (ADIF)

The interrupt request flag (ADIF) is not cleared even if the analog input channel specification register (ADS) is changed.
Therefore, if an analog input pin is changed during A/D conversion, the A/D conversion result and ADIF flag for the pre-change analog input may be set just before the ADS register rewrite. Caution is therefore required since, at this time, when ADIF flag is read immediately after the ADS register rewrite, ADIF flag is set despite the fact A/D conversion for the post-change analog input has not ended.
When A/D conversion is stopped and then resumed, clear ADIF flag before the A/D conversion operation is resumed.

Figure 19 - 37 Timing of A/D Conversion End Interrupt Request Generation



(8) Conversion results just after A/D conversion start

While in the software trigger mode or hardware trigger no-wait mode, the first A/D conversion value immediately after A/D conversion starts may not fall within the rating range if the ADCS bit is set to 1 within 1 μs after the ADCE bit was set to 1. Take measures such as polling the A/D conversion end interrupt request (INTAD) and removing the first conversion result.

(9) A/D conversion result register (ADCR, ADCRH) read operation

When a write operation is performed to A/D converter mode register 0 (ADM0), analog input channel specification register (ADS), and port mode control register (PMCxx), the contents of the ADCR and ADCRH registers may become undefined. Read the conversion result following conversion completion before writing to the ADM0, ADS, or PMC register. Using a timing other than the above may cause an incorrect conversion result to be read.

(10) Internal equivalent circuit

The equivalent circuit of the analog input block is shown below.

Figure 19 - 38 Internal Equivalent Circuit of ANIn Pin

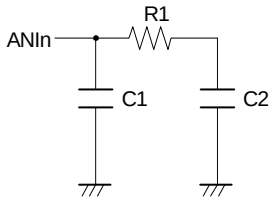


Table 19 - 4 Resistance and Capacitance Values of Equivalent Circuit (Reference Values)

V_{DD}	ANIn Pins	R1 [kΩ]	C1 [pF]	C2 [pF]
3.6 V ≤ V_{DD} ≤ 5.5 V	ANI8 to ANI14	18	8	7.0
2.7 V ≤ V_{DD} < 3.6 V	ANI8 to ANI14	53	8	7.0
1.8 V ≤ V_{DD} < 2.7 V	ANI8 to ANI14	321	8	7.0

Remark The resistance and capacitance values shown in Table 19 - 4 are not guaranteed values.

(11) Starting the A/D converter

Start the A/D converter after the V_{DD} voltage stabilizes.

CHAPTER 20 SERIAL ARRAY UNIT

Serial array unit has up to four serial channels. Each channel can achieve Simplified SPI(CSI Note), UART, and simplified I2C communication.

Function assignment of each channel supported by the RL78/H1D is as shown below.

Note Although the Simplified SPI(CSI) function is generally called SPI, it is also called CSI in this product, so it is referred to as such in this manual.

Unit	Channel	Used as Simplified SPI(CSI)	Used as UART	Used as Simplified I2C
0	0	CSI00 (supporting slave select input function)	UART0 (supporting LIN-bus)	IIC00
	1	—		—
	2	CSI10	UART1	IIC10
	3	—		—
1	0	CSI20	UART2	IIC20
	1	—		—

When “UART0” is used for channels 0 and 1 of the unit 0, CSI00 and IIC00 cannot be used, but CSI10, UART1, or IIC10 can be used for channels 2 and 3.

20.1 Functions of Serial Array Unit

Each serial interface supported by the RL78/H1D has the following features.

20.1.1 Simplified SPI (CSI00, CSI10, CSI20)

Data is transmitted or received in synchronization with the serial clock (SCK) output from the master channel. Simplified SPI communication is clocked communication performed by using three communication lines: one for the serial clock (SCK), one for transmitting serial data (SO), one for receiving serial data (SI).

For details about the settings, see **20.5 Operation of Simplified SPI(CSI) (CSI00, CSI10, CSI20) Communication**.

[Data transmission/reception]

- Data length of 7 or 8 bits
- Phase control of transmit/receive data
- MSB/LSB first selectable

[Clock control]

- Master/slave selection
- Phase control of I/O clock
- Setting of transfer period by prescaler and internal counter of each channel
- Maximum transfer rate Note

  During master communication: Max. f_{CLK}/2 (CSI00 only)

  Max. f_{CLK}/4

  During slave communication: Max. f_{MCK}/6

[Interrupt function]

- Transfer end interrupt/buffer empty interrupt

[Error detection flag]

- Overrun error

In addition, CSI00 and CSI20 support the SNOOZE mode. When SCK input is detected while in the STOP mode, the SNOOZE mode makes data reception that does not require the CPU possible. Only CSI00 and CSI20 can be specified for asynchronous reception.

CSI00 support the slave select function.

Note Use the clocks within a range satisfying the SCK cycle time (t_{KCY}) characteristics. For details, see **CHAPTER 38** or **CHAPTER 39 ELECTRICAL SPECIFICATIONS**.

20.1.2 UART (UART0 to UART2)

This is a start-stop synchronization function using two lines: serial data transmission (TxD) and serial data reception (RxD) lines. By using these two communication lines, each data frame, which consist of a start bit, data, parity bit, and stop bit, is transferred asynchronously (using the internal baud rate) between the microcontroller and the other communication party. Full-duplex UART communication can be performed by using a channel dedicated to transmission (even-numbered channel) and a channel dedicated to reception (odd-numbered channel). The LIN-bus can be implemented by using timer array unit with an external interrupt (INTP0).

For details about the settings, see **20.7 Operation of UART (UART0 to UART2) Communication**.

[Data transmission/reception]

- Data length of 7, 8, or 9 bits Note
- Select the MSB/LSB first
- Level setting of transmit/receive data and select of reverse
- Parity bit appending and parity check functions
- Stop bit appending

[Interrupt function]

- Transfer end interrupt/buffer empty interrupt
- Error interrupt in case of framing error, parity error, or overrun error

[Error detection flag]

- Framing error, parity error, or overrun error

In addition, UART0 and UART2 reception support the SNOOZE mode. When RxD input is detected while in the STOP mode, the SNOOZE mode makes data reception that does not require the CPU possible. Only UART0, UART2 can be specified for asynchronous reception.

The LIN-bus is accepted in UART0 (0 and 1 channels of unit 0).

[LIN-bus functions]

- Wakeup signal detection
- Break field (BF) detection
- Sync field measurement, baud rate calculation

} Using the external interrupt (INTP0) and timer array unit

Note Only UART0 can be specified for the 9-bit data length.

20.1.3 Simplified I²C (IIC00, IIC10, IIC20)

This is a clocked communication function to communicate with two or more devices by using two lines: serial clock (SCL) and serial data (SDA). This simplified I²C is designed for single communication with a device such as EEPROM, flash memory, or A/D converter, and therefore, it functions only as a master.
Make sure by using software, as well as operating the control registers, that the AC specifications of the start and stop conditions are observed.
For details about the settings, see **20.9 Operation of Simplified I²C (IIC00, IIC10, IIC20) Communication**.

[Data transmission/reception]
- Master transmission, master reception (only master function with a single master)
- ACK output function Note and ACK detection function
- Data length of 8 bits (When an address is transmitted, the address is specified by the higher 7 bits, and the least significant bit is used for R/W control.)
- Manual generation of start condition and stop condition

[Interrupt function]
- Transfer end interrupt

[Error detection flag]
- ACK error, or overrun error

* [Functions not supported by simplified I²C]
- Slave transmission, slave reception
- Arbitration loss detection function
- Wait detection functions

Note When receiving the last data, ACK will not be output if 0 is written to the SOEmn bit (serial output enable register m (SOEm)) and serial communication data output is stopped. See the processing flow in **20.9.3 (2)** for details.

Remark 1. To use an I²C bus of full function, see **CHAPTER 21 SERIAL INTERFACE IICA**.
Remark 2. m: Unit number (m = 0, 1), n: Channel number (n = 0, 2), mn = 00, 02, 10

20.2 Configuration of Serial Array Unit

The serial array unit includes the following hardware.

Table 20 - 1 Configuration of Serial Array Unit

Item	Configuration
Shift register	8 bits or 9 bits Note 1
Buffer register	Lower 8 bits or 9 bits of serial data register mn (SDRmn) Notes 1, 2
Serial clock I/O	SCK00, SCK10, SCK20 pins (for Simplified SPI), SCL00, SCL10, SCL20 pins (for simplified I^2C)
Serial data input	SI00, SI10, SI20 pins (for Simplified SPI), RxD1, RxD2 pins (for UART), RXD0 pin (for UART supporting LIN-bus)
Serial data output	SO00, SO10, SO20 pins (for Simplified SPI), TxD1, TxD2 pins (for UART), TXD0 pin (for UART supporting LIN-bus)
Serial data I/O	SDA00, SDA10, SDA20 pins (for simplified I^2C)
Slave select input	$\overline{SSI00}$ pin (for slave select input function)
Control registers	<Registers of unit setting block> • Peripheral enable register 0 (PER0) • Serial clock select register m (SPSm) • Serial channel enable status register m (SEm) • Serial channel start register m (SSm) • Serial channel stop register m (STm) • Serial output enable register m (SOEm) • Serial output register m (SOm) • Serial output level register m (SOLm) • Serial standby control register m (SSCm) • Input switch control register (ISC) • Noise filter enable register 0 (NFEN0)
	<Registers of each channel> • Serial data register mn (SDRmn) • Serial mode register mn (SMRmn) • Serial communication operation setting register mn (SCRmn) • Serial status register mn (SSRmn) • Serial flag clear trigger register mn (SIRmn)
	• Port input mode registers 0, 1, 3, 4, 5, 8 (PIM0, PIM1, PIM3, PIM4, PIM5, PIM8) • Port output mode registers 0, 1, 3, 4, 5, 8 (POM0, POM1, POM3, POM4, POM5, POM8) • Port mode control register 0 (PMC0) • Port mode registers 0, 1, 3, 4, 5, 8 (PM0, PM1, PM3, PM4, PM5, PM8) • Port registers 0, 1, 3, 4, 5, 8 (P0, P1, P3, P4, P5, P8)

Note 1. The number of bits used as the shift register and buffer register differs depending on the unit and channel.
- mn = 00, 01: lower 9 bits
- Other than above: lower 8 bits

Note 2. The lower 8 bits of serial data register mn (SDRmn) can be read or written as the following SFR, depending on the communication mode.
- CSIp communication ..... SIOp (CSIp data register)
- UARTq reception ..... RXDq (UARTq receive data register)
- UARTq transmission ..... TXDq (UARTq transmit data register)
- IICr communication ..... SIOr (IICr data register)

Remark m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), p: CSI number (p = 00, 10, 20),
q: UART number (q = 0 to 2), r: IIC number (r = 00, 10, 20)

Figure 20 - 1 shows the Block Diagram of Serial Array Unit 0.

Figure 20 - 1 Block Diagram of Serial Array Unit 0

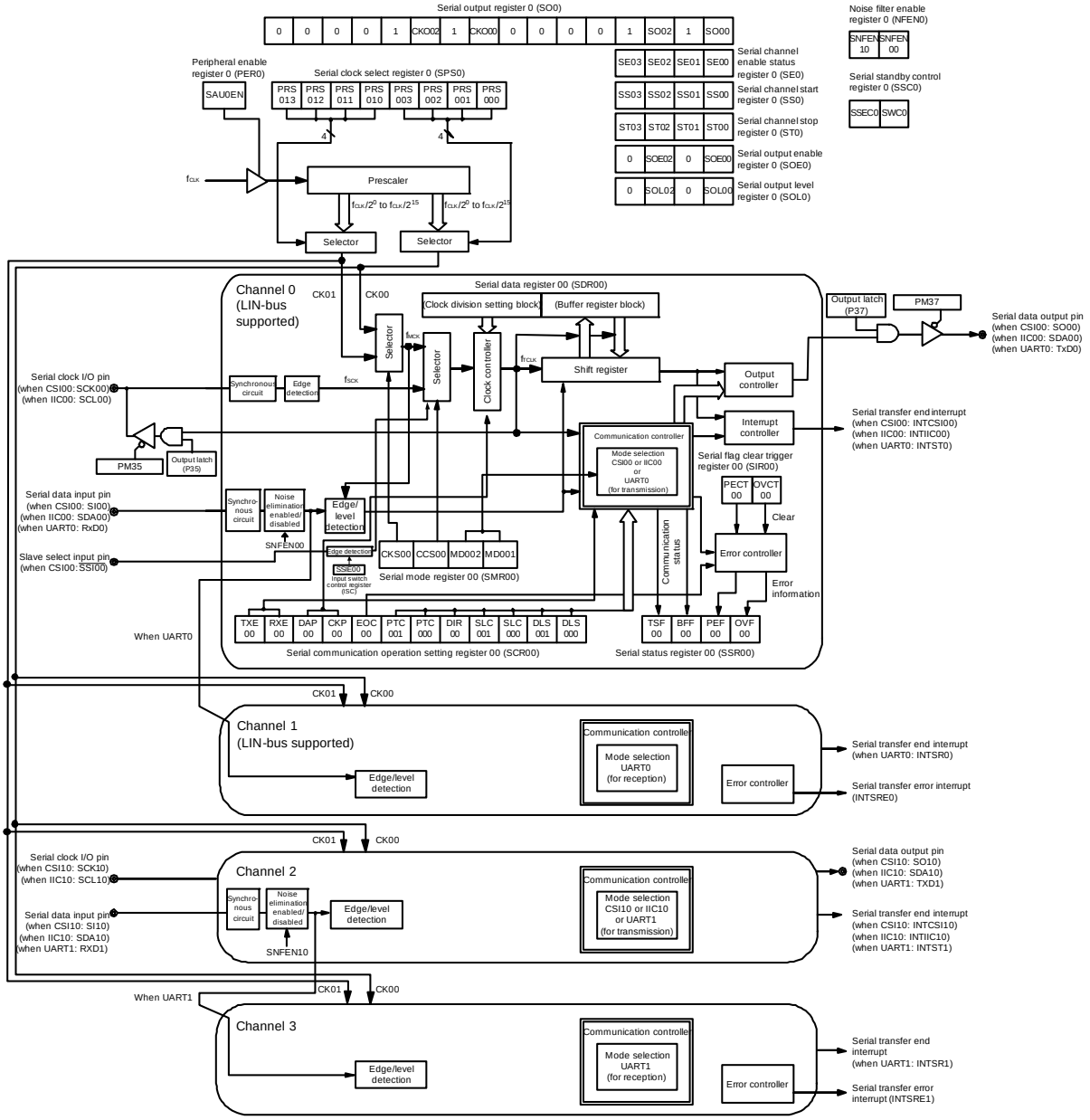
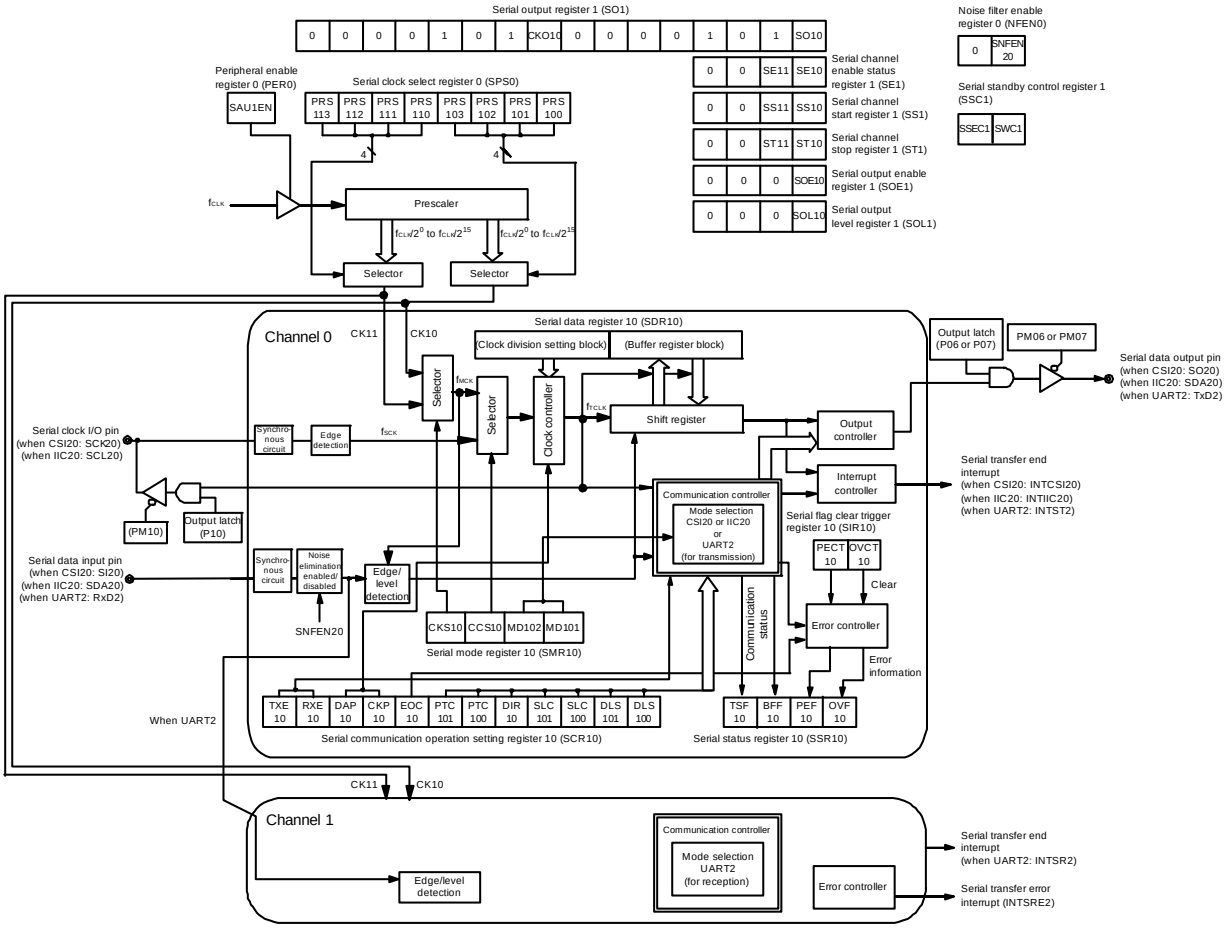


Figure 20 - 2 shows the Block Diagram of Serial Array Unit 1.

Figure 20 - 2 Block Diagram of Serial Array Unit 1



20.2.1 Shift register

This is a 9-bit register that converts parallel data into serial data or vice versa.

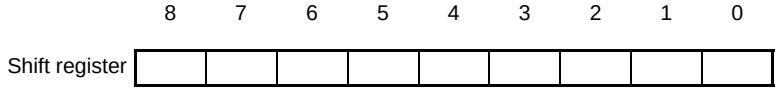
In case of the UART communication of nine bits of data, nine bits (bits 0 to 8) are used Note.

During reception, it converts data input to the serial pin into parallel data.

When data is transmitted, the value set to this register is output as serial data from the serial output pin.

The shift register cannot be directly manipulated by program.

To read or write the shift register, use the lower 8/9 bits of serial data register mn (SDRmn).



Note Only UART0 can be specified for the 9-bit data length.

20.2.2 Lower 8/9 bits of the serial data register mn (SDRmn)

The SDRmn register is the transmit/receive data register (16 bits) of channel n. Bits 8 to 0 (lower 9 bits) Note 1 or bits 7 to 0 (lower 8 bits) function as a transmit/receive buffer register, and bits 15 to 9 are used as a register that sets the division ratio of the operation clock (f_{MCK}).

When data is received, parallel data converted by the shift register is stored in the lower 8/9 bits. When data is to be transmitted, set transmit data to be transferred to the shift register to the lower 8/9 bits.

The data stored in the lower 8/9 bits of this register is as follows, depending on the setting of bits 0 and 1 (DLSmn0, DLSmn1) of serial communication operation setting register mn (SCRmn), regardless of the output sequence of the data.

- 7-bit data length (stored in bits 0 to 6 of SDRmn register)
- 8-bit data length (stored in bits 0 to 7 of SDRmn register)
- 9-bit data length (stored in bits 0 to 8 of SDRmn register) Note 1

The SDRmn register can be read or written in 16-bit units.

The lower 8/9 bits of the SDRmn register can be read or written Note 2 as the following SFR, depending on the communication mode.

- CSIp communication..... SIOp (CSIp data register)
- UARTq reception ..... RXDq (UARTq receive data register)
- UARTq transmission..... TXDq (UARTq transmit data register)
- IICr communication..... SIOr (IICr data register)

Reset signal generation clears the SDRmn register to 0000H.

Note 1. Only UART0 can be specified for the 9-bit data length.

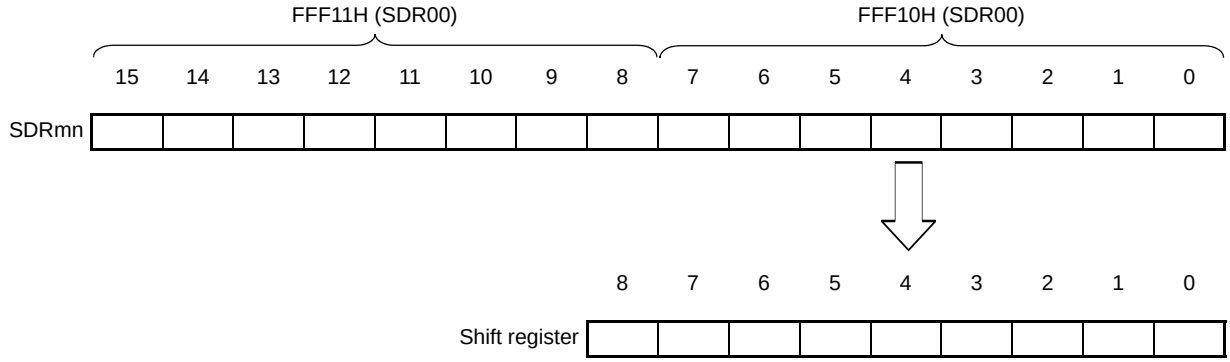
Note 2. Writing in 8-bit units is prohibited when the operation is stopped (SEmn = 0).

Remark 1. After data is received, “0” is stored in bits 0 to 8 in bit portions that exceed the data length.

Remark 2. m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), p: CSI number (p = 00, 10, 20), q: UART number (q = 0 to 2), r: IIC number (r = 00, 10, 20)

Figure 20 - 3 Format of Serial data register mn (SDRmn) (mn = 00, 01)

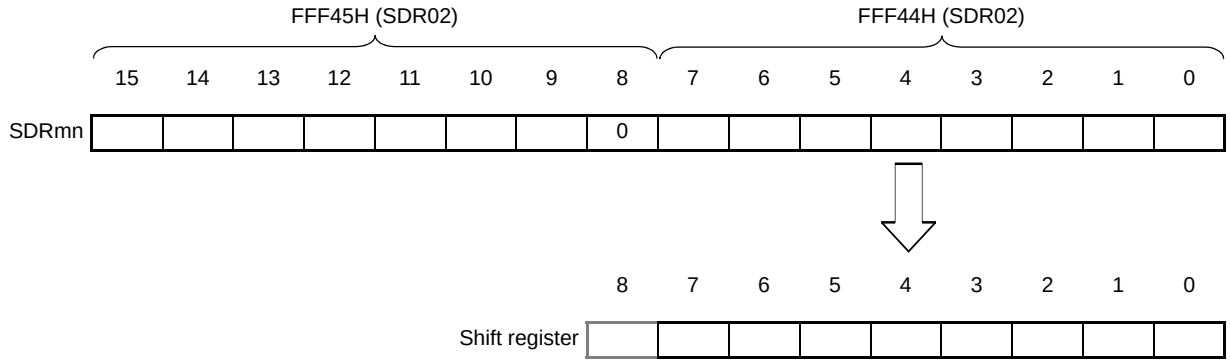
Address: FFF10H, FFF11H (SDR00), FFF12H, FFF13H (SDR01) After reset: 0000H R/W



Remark For the function of the higher 7 bits of the SDRmn register, see **20.3 Registers Controlling Serial Array Unit**.

Figure 20 - 4 Format of Serial data register mn (SDRmn) (mn = 02, 03, 10, 11)

Address: FFF44H, FFF45H (SDR02), FFF46H, FFF47H (SDR03), FFF48H, FFF49H (SDR10), FFF4AH, FFF4BH (SDR11) After reset: 0000H R/W



Caution Be sure to clear bit 8 to "0".

Remark For the function of the higher 7 bits of the SDRmn register, see **20.3 Registers Controlling Serial Array Unit**.

20.3 Registers Controlling Serial Array Unit

Serial array unit is controlled by the following registers.

- Peripheral enable register 0 (PER0)
- Serial clock select register m (SPSm)
- Serial mode register mn (SMRmn)
- Serial communication operation setting register mn (SCRmn)
- Serial data register mn (SDRmn)
- Serial flag clear trigger register mn (SIRmn)
- Serial status register mn (SSRmn)
- Serial channel start register m (SSm)
- Serial channel stop register m (STm)
- Serial channel enable status register m (SEm)
- Serial output enable register m (SOEm)
- Serial output level register m (SOLm)
- Serial output register m (SOm)
- Serial standby control register m (SSCm)
- Input switch control register (ISC)
- Noise filter enable register 0 (NFEN0)
- Port input mode registers 0, 1, 3, 4, 5, 8 (PIM0, PIM1, PIM3, PIM4, PIM5, PIM8)
- Port output mode registers 0, 1, 3, 4, 5, 8 (POM0, POM1, POM3, POM4, POM5, POM8)
- Port mode control register 0 (PMC0)
- Port mode registers 0, 1, 3, 4, 5, 8 (PM0, PM1, PM3, PM4, PM5, PM8)
- Port registers 0, 1, 3, 4, 5, 8 (P0, P1, P3, P4, P5, P8)

Remark m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3)

20.3.1 Peripheral enable register 0 (PER0)

PER0 is used to enable or disable supplying the clock to the peripheral hardware. Clock supply to the hardware that is not used is also stopped so as to decrease the power consumption and noise.

When serial array unit 0 is used, be sure to set bit 2 (SAU0EN) of this register to 1.

When serial array unit 1 is used, be sure to set bit 3 (SAU1EN) of this register to 1.

The PER0 register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears the PER0 register to 00H.

Figure 20 - 5 Format of Peripheral enable register 0 (PER0)

Address: F00F0H After reset: 00H R/W

Symbol	<7>	6	<5>	<4>	<3>	<2>	1	<0>
PER0	RTCWEN	0	ADCEN	IICA0EN	SAU1EN	SAU0EN	0	TAU0EN

SAUmEN	Control of serial array unit m input clock supply
0	Stops supply of input clock. • SFR used by serial array unit m cannot be written. • Serial array unit m is in the reset status.
1	Enables input clock supply. • SFR used by serial array unit m can be read/written.

Caution 1. When setting serial array unit m, be sure to first set the following registers with the SAUmEN bit set to 1. If SAUmEN = 0, control registers of serial array unit m become default values and writing to them is ignored (except for the input switch control register (ISC), noise filter enable register 0 (NFEN0), port input mode registers 0, 1, 3, 4, 5, 8 (PIM0, PIM1, PIM3, PIM4, PIM5, PIM8), port output mode registers 0, 1, 3, 4, 5, 8 (POM0, POM1, POM3, POM4, POM5, POM8), port mode control register 0 (PMC0), port mode registers 0, 1, 3, 4, 5, 8 (PM0, PM1, PM3, PM4, PM5, PM8), and port registers 0, 1, 3, 4, 5, 8 (P0, P1, P3, P4, P5, P8)).

- **Serial clock select register m (SPSm)**
- **Serial mode register mn (SMRmn)**
- **Serial communication operation setting register mn (SCRmn)**
- **Serial data register mn (SDRmn)**
- **Serial flag clear trigger register mn (SIRmn)**
- **Serial status register mn (SSRmn)**
- **Serial channel start register m (SSm)**
- **Serial channel stop register m (STm)**
- **Serial channel enable status register m (SEm)**
- **Serial output enable register m (SOEm)**
- **Serial output level register m (SOLm)**
- **Serial output register m (SOm)**
- **Serial standby control register m (SSCm)**

Caution 2. Be sure to clear bits 1 and 6 to 0.

20.3.2 Serial clock select register m (SPSm)

The SPSm register is a 16-bit register that is used to select two types of operation clocks (CKm0, CKm1) that are commonly supplied to each channel. CKm1 is selected by bits 7 to 4 of the SPSm register, and CKm0 is selected by bits 3 to 0.

Rewriting the SPSm register is prohibited when the register is in operation (when SEmn = 1).

The SPSm register can be set by a 16-bit memory manipulation instruction.

The lower 8 bits of the SPSm register can be set with an 8-bit memory manipulation instruction with SPSmL.

Reset signal generation clears the SPSm register to 0000H.

Figure 20 - 6 Format of Serial clock select register m (SPSm)

Address: F0126H, F0127H (SPS0), F0166H, F0167H (SPS1) After reset: 0000H R/W

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SPSm	0	0	0	0	0	0	0	0	PRS m13	PRS m12	PRS m11	PRS m10	PRS m03	PRS m02	PRS m01	PRS m00

PRS mk3	PRS mk2	PRS mk1	PRS mk0	Section of operation clock (CKmk) Note					
					f_{CLK} = 2 MHz	f_{CLK} = 5 MHz	f_{CLK} = 10 MHz	f_{CLK} = 20 MHz	f_{CLK} = 24 MHz
0	0	0	0	f_{CLK}	2 MHz	5 MHz	10 MHz	20 MHz	24 MHz
0	0	0	1	$f_{CLK}/2$	1 MHz	2.5 MHz	5 MHz	10 MHz	12 MHz
0	0	1	0	$f_{CLK}/2^2$	500 kHz	1.25 MHz	2.5 MHz	5 MHz	6 MHz
0	0	1	1	$f_{CLK}/2^3$	250 kHz	625 kHz	1.25 MHz	2.5 MHz	3 MHz
0	1	0	0	$f_{CLK}/2^4$	125 kHz	313 kHz	625 kHz	1.25 MHz	1.5 MHz
0	1	0	1	$f_{CLK}/2^5$	62.5 kHz	156 kHz	313 kHz	625 kHz	750 kHz
0	1	1	0	$f_{CLK}/2^6$	31.3 kHz	78.1 kHz	156 kHz	313 kHz	375 kHz
0	1	1	1	$f_{CLK}/2^7$	15.6 kHz	39.1 kHz	78.1 kHz	156 kHz	187.5 kHz
1	0	0	0	$f_{CLK}/2^8$	7.81 kHz	19.5 kHz	39.1 kHz	78.1 kHz	93.8 kHz
1	0	0	1	$f_{CLK}/2^9$	3.91 kHz	9.77 kHz	19.5 kHz	39.1 kHz	46.9 kHz
1	0	1	0	$f_{CLK}/2^{10}$	1.95 kHz	4.88 kHz	9.77 kHz	19.5 kHz	23.4 kHz
1	0	1	1	$f_{CLK}/2^{11}$	977 Hz	2.44 kHz	4.88 kHz	9.77 kHz	11.7 kHz
1	1	0	0	$f_{CLK}/2^{12}$	488 Hz	1.22 kHz	2.44 kHz	4.88 kHz	5.86 kHz
1	1	0	1	$f_{CLK}/2^{13}$	244 Hz	610 Hz	1.22 kHz	2.44 kHz	2.93 kHz
1	1	1	0	$f_{CLK}/2^{14}$	122 Hz	305 Hz	610 Hz	1.22 kHz	1.46 kHz
1	1	1	1	$f_{CLK}/2^{15}$	61 Hz	153 Hz	305 Hz	610 Hz	732 Hz

Note When changing the clock selected for f_{CLK} (by changing the system clock control register (CKC) value), do so after having stopped (serial channel stop register m (STm) = 000FH) the operation of the serial array unit (SAU).

Caution Be sure to clear bits 15 to 8 to "0".

Remark 1. f_{CLK}: CPU/peripheral hardware clock frequency
Remark 2. m: Unit number (m = 0, 1)
Remark 3. k = 0, 1

20.3.3 Serial mode register mn (SMRmn)

The SMRmn register is a register that sets an operation mode of channel n. It is also used to select an operation clock (f_{MCK}), specify whether the serial clock (f_{SCK}) may be input or not, set a start trigger, an operation mode (Simplified SPI(CSI), UART, or simplified I^2C), and an interrupt source. This register is also used to invert the level of the receive data only in the UART mode.

Rewriting the SMRmn register is prohibited when the register is in operation (when SEmn = 1). However, the MDmn0 bit can be rewritten during operation.

The SMRmn register can be set by a 16-bit memory manipulation instruction.

Reset signal generation sets the SMRmn register to 0020H.

Figure 20 - 7 Format of Serial mode register mn (SMRmn) (1/2)

Address: F0110H, F0111H (SMR00) to F0116H, F0117H (SMR03), F0150H, F0151H (SMR10), F0152H, F0153H (SMR11) After reset: 0020H R/W

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SMRmn	CKSmn	CCSmn	0	0	0	0	0	STSmn Note	0	SISmn0 Note	1	0	0	MDmn2	MDmn1	MDmn0

CKSmn	Selection of operation clock (f_{MCK}) of channel n
0	Operation clock CKm0 set by the SPSm register
1	Operation clock CKm1 set by the SPSm register
Operation clock (f_{MCK}) is used by the edge detector. In addition, depending on the setting of the CCSmn bit and the higher 7 bits of the SDRmn register, a transfer clock (f_{TCLK}) is generated.	

CCSmn	Selection of transfer clock (f_{TCLK}) of channel n
0	Divided operation clock f_{MCK} specified by the CKSmn bit
1	Clock input f_{SCK} from the SCKp pin (slave transfer in Simplified SPI(CSI) mode)
Transfer clock f_{TCLK} is used for the shift register, communication controller, output controller, interrupt controller, and error controller. When CCSmn = 0, the division ratio of operation clock (f_{MCK}) is set by the higher 7 bits of the SDRmn register.	

STSmn Note	Selection of start trigger source
0	Only software trigger is valid (selected for Simplified SPI(CSI), UART transmission, and simplified I^2C).
1	Valid edge of the RxDq pin (selected for UART reception)
Transfer is started when the above source is satisfied after 1 is set to the SSm register.	

Note The SMR01, SMR03, and SMR11 registers only.

Caution **Be sure to clear bits 13 to 9, 7, 4, and 3 (or bits 13 to 6, 4, and 3 for the SMR00, SMR02, or SMR10 register) to "0". Be sure to set bit 5 to "1".**

Remark m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), p: CSI number (p = 00, 10, 20), q: UART number (q = 0 to 2), r: IIC number (r = 00, 10, 20)

Figure 20 - 7 Format of Serial mode register mn (SMRmn) (2/2)

Address: F0110H, F0111H (SMR00) to F0116H, F0117H (SMR03), F0150H, F0151H (SMR10), F0152H, F0153H (SMR11) After reset: 0020H R/W

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SMRmn	CKS mn	CCS mn	0	0	0	0	0	STS mn Note	0	SIS mn0 Note	1	0	0	MD mn2	MD mn1	MD mn0

SIS mn0 Note	Controls inversion of level of receive data of channel n in UART mode
0	Falling edge is detected as the start bit. The input communication data is captured as is.
1	Rising edge is detected as the start bit. The input communication data is inverted and captured.

MD mn2	MD mn1	Setting of operation mode of channel n
0	0	Simplified SPI(CSI) mode
0	1	UART mode
1	0	Simplified I^2C mode
1	1	Setting prohibited

MD mn0	Selection of interrupt source of channel n
0	Transfer end interrupt
1	Buffer empty interrupt (Occurs when data is transferred from the SDRmn register to the shift register.)
For successive transmission, the next transmit data is written by setting the MDmn0 bit to 1 when SDRmn data has run out.	

Note The SMR01, SMR03, and SMR11 registers only.

Caution **Be sure to clear bits 13 to 9, 7, 4, and 3 (or bits 13 to 6, 4, and 3 for the SMR00, SMR02, or SMR10 register) to "0". Be sure to set bit 5 to "1".**

Remark m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), p: CSI number (p = 00, 10, 20,), q: UART number (q = 0 to 2), r: IIC number (r = 00, 10, 20)

20.3.4 Serial communication operation setting register mn (SCRmn)

The SCRmn register is a communication operation setting register of channel n. It is used to set a data transmission/reception mode, phase of data and clock, whether an error signal is to be masked or not, parity bit, start bit, stop bit, and data length.

Rewriting the SCRmn register is prohibited when the register is in operation (when SEmn = 1).

The SCRmn register can be set by a 16-bit memory manipulation instruction.

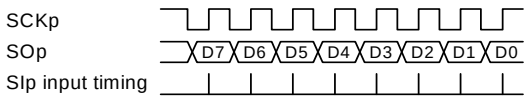
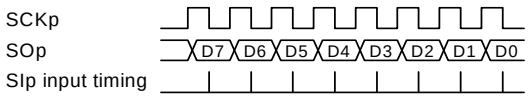
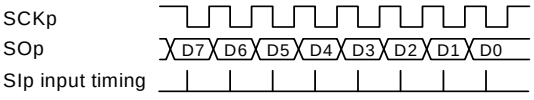
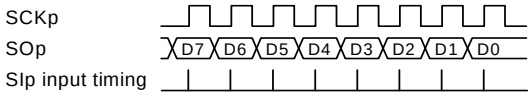
Reset signal generation sets the SCRmn register to 0087H.

Figure 20 - 8 Format of Serial communication operation setting register mn (SCRmn) (1/2)

Address: F0118H, F0119H (SCR00) to F011EH, F011FH (SCR03), F0158H, F0159H (SCR10), F015AH, F015BH (SCR11) After reset: 0087H R/W

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SCRmn	TXE mn	RXE mn	DAP mn	CKP mn	0	EOC mn	PTC mn1	PTC mn0	DIR mn	0	SLCmn1 Note 1	SLC mn0	0	1	DLSmn1 Note 2	DLS mn0

TXE mn	RXE mn	Setting of operation mode of channel n
0	0	Disable communication.
0	1	Reception only
1	0	Transmission only
1	1	Transmission/reception

DAP mn	CKP mn	Selection of data and clock phase in Simplified SPI(CSI) mode	Type
0	0		1
0	1		2
1	0		3
1	1		4
Be sure to set DAPmn, CKPmn = 0, 0 in the UART mode and simplified I2C mode.			

EOC mn	Mask control of error interrupt signal (INTSREx (x = 0 to 3))
0	Disables generation of error interrupt INTSREx (INTSRx is generated).
1	Enables generation of error interrupt INTSREx (INTSRx is not generated if an error occurs).
Set EOCmn = 0 in the Simplified SPI(CSI) mode, simplified I2C mode, and during UART transmission Note 3.	

Note 1. The SCR00, SCR02, and SCR10 registers only.

Note 2. The SCR00 and SCR01 registers only. Others are fixed to 1.

Note 3. When using CSImn not with EOCmn = 0, error interrupt INTSREn may be generated.

Caution Be sure to clear bits 3, 6, and 11 to "0" (Also clear bit 5 of the SCR01, SCR03, or SCR11 register to 0). Be sure to set bit 2 to "1" (Also clear bit 1 of the SCR01, SCR03, SCR10, or SCR11 register to 1).

Remark m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), p: CSI number (p = 00, 10, 20)

Figure 20 - 8 Format of Serial communication operation setting register mn (SCRmn) (2/2)

Address: F0118H, F0119H (SCR00) to F011EH, F011FH (SCR03), F0158H, F0159H (SCR10), F015AH, F015BH (SCR11) After reset: 0087H R/W

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SCRmn	TXEmn	RXEmn	DAPmn	CKPmn	0	EOCmn	PTCmn1	PTCmn0	DIRmn	0	SLCmn1 Note 1	SLCmn0	0	1	DLSmn1 Note 2	DLSmn0

PTC mn1	PTC mn0	Setting of parity bit in UART mode	
		Transmission	Reception
0	0	Does not output the parity.	Receives without parity
0	1	Outputs the parity Note 3.	No parity judgment
1	0	Outputs even parity.	Judged as even parity.
1	1	Outputs odd parity.	Judges as odd parity.
Be sure to set PTCmn1, PTCmn0 = 0, 0 in the Simplified SPI(CSI) mode and simplified I2C mode.			

DIR mn	Selection of data transfer sequence in Simplified SPI(CSI) and UART modes
0	Inputs/outputs data with MSB first.
1	Inputs/outputs data with LSB first.
Be sure to clear DIRmn = 0 in the simplified I2C mode.	

SLCmn1 Note 1	SLC mn0	Setting of stop bit in UART mode
0	0	No stop bit
0	1	Stop bit length = 1 bit
1	0	Stop bit length = 2 bits (mn = 00, 02, 10 only)
1	1	Setting prohibited
When the transfer end interrupt is selected, the interrupt is generated when all stop bits have been completely transferred. Set 1 bit (SLCmn1, SLCmn0 = 0, 1) during UART reception and in the simplified I2C mode. Set no stop bit (SLCmn1, SLCmn0 = 0, 0) in the Simplified SPI(CSI) mode. Set 1 bit (SLCmn1, SLCmn0 = 0, 1) or 2 bits (SLCmn1, SLCmn0 = 1, 0) during UART transmission.		

DLSmn1 Note 2	DLS mn0	Setting of data length in Simplified SPI(CSI) and UART modes
0	1	9-bit data length (stored in bits 0 to 8 of the SDRmn register) (settable in UART mode only)
1	0	7-bit data length (stored in bits 0 to 6 of the SDRmn register)
1	1	8-bit data length (stored in bits 0 to 7 of the SDRmn register)
Other than above		Setting prohibited
Be sure to set DLSmn1, DLSmn0 = 1, 1 in the simplified I2C mode.		

Note 1. The SCR00, SCR02, and SCR10 registers only.

Note 2. The SCR00 and SCR01 registers only. Others are fixed to 1.

Note 3. 0 is always added regardless of the data contents.

Caution **Be sure to clear bits 3, 6, and 11 to "0" (Also clear bit 5 of the SCR01, SCR03, or SCR11 register to 0). Be sure to set bit 2 to "1" (Also clear bit 1 of the SCR01, SCR03, SCR10, or SCR11 register to 1).**

Remark m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), p: CSI number (p = 00, 10, 20)

20.3.5 Serial data register mn (SDRmn)

The SDRmn register is the transmit/receive data register (16 bits) of channel n. Bits 8 to 0 (lower 9 bits) of SDR00 and SDR01 or bits 7 to 0 (lower 8 bits) of SDR02, SDR03, SDR10, and SDR11 function as a transmit/receive buffer register, and bits 15 to 9 (higher 7 bits) are used as a register that sets the division ratio of the operation clock (f_{MCK}).

If the CCSmn bit of serial mode register mn (SMRmn) is cleared to 0, the clock set by dividing the operation clock by bits 15 to 9 (higher 7 bits) of the SDRmn register is used as the transfer clock.

If the CCSmn bit of serial mode register mn (SMRmn) is set to 1, set bits 15 to 9 (upper 7 bits) of SDR00 and SDR01 to 0000000B. The input clock f_{SCK} (slave transfer in Simplified SPI(CSI) mode) from the SCKp pin is used as the transfer clock.

The lower 8/9 bits of the SDRmn register function as a transmit/receive buffer register. During reception, the parallel data converted by the shift register is stored in the lower 8/9 bits, and during transmission, the data to be transmitted to the shift register is set to the lower 8/9 bits.

The SDRmn register can be read or written in 16-bit units.

However, the higher 7 bits can only be written or read when the operation is stopped (SEmn = 0). During operation (SEmn = 1), a value is written only to the lower 8/9 bits of the SDRmn register. When the SDRmn register is read during operation, the higher 7 bits are always read as 0.

Reset signal generation clears the SDRmn register to 0000H.

Figure 20 - 9 Format of Serial data register mn (SDRmn)

Address: FFF10H, FFF11H (SDR00), FFF12H, FFF13H (SDR01) After reset: 0000H R/W

	FFF11H (SDR00)								FFF10H (SDR00)							
Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SDRmn																

Address: FFF44H, FFF45H (SDR02), FFF46H, FFF47H (SDR03) After reset: 0000H R/W
FFF48H, FFF49H (SDR10), FFF4AH, FFF4BH (SDR11)

	FFF45H (SDR02)								FFF44H (SDR02)							
Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SDRmn								0								

SDRmn[15:9]							Transfer clock set by dividing the operating clock
0	0	0	0	0	0	0	$f_{MCK}/2$
0	0	0	0	0	0	1	$f_{MCK}/4$
0	0	0	0	0	1	0	$f_{MCK}/6$
0	0	0	0	0	1	1	$f_{MCK}/8$
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
1	1	1	1	1	1	0	$f_{MCK}/254$
1	1	1	1	1	1	1	$f_{MCK}/256$

Caution 1. Be sure to clear bit 8 of the SDR02 and SDR03 registers to "0".

Caution 2. Setting SDRmn[15:9] = (0000000B, 0000001B) is prohibited when UART is used.

Caution 3. Setting SDRmn[15:9] = 0000000B is prohibited when simplified I^2C is used. Set SDRmn[15:9] to 0000001B or greater.

Caution 4. Do not write eight bits to the lower eight bits if operation is stopped (SEmn = 0). (If these bits are written to, the higher seven bits are cleared to 0.)

Remark 1. For the function of the lower 8/9 bits of the SDRmn register, see **20.2 Configuration of Serial Array Unit**.

Remark 2. m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3)

20.3.6 Serial flag clear trigger register mn (SIRmn)

The SIRmn register is a trigger register that is used to clear each error flag of channel n.

When each bit (FECTmn, PECTmn, OVCTmn) of this register is set to 1, the corresponding bit (FEFmn, PEFmn, OVFmn) of serial status register mn is cleared to 0. Because the SIRmn register is a trigger register, it is cleared immediately when the corresponding bit of the SSRmn register is cleared.

The SIRmn register can be set by a 16-bit memory manipulation instruction.

The lower 8 bits of the SIRmn register can be set with an 8-bit memory manipulation instruction with SIRmnL.

Reset signal generation clears the SIRmn register to 0000H.

Figure 20 - 10 Format of Serial flag clear trigger register mn (SIRmn)

Address: F0108H, F0109H (SIR00) to F010EH, F010FH (SIR03), F0148H, F0149H (SIR10), F014AH, F014BH (SIR11) After reset: 0000H R/W

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SIRmn	0	0	0	0	0	0	0	0	0	0	0	0	0	FECTmn Note	PECTmn	OVCTmn

FECTmn Note	Clear trigger of framing error of channel n
0	Not cleared
1	Clears the FEFmn bit of the SSRmn register to 0.

PECTmn	Clear trigger of parity error flag of channel n
0	Not cleared
1	Clears the PEFmn bit of the SSRmn register to 0.

OVCTmn	Clear trigger of overrun error flag of channel n
0	Not cleared
1	Clears the OVFmn bit of the SSRmn register to 0.

Note The SIR01, SIR03, and SIR11 registers only.

Caution Be sure to clear bits 15 to 3 (or bits 15 to 2 for the SIR00, SIR02, or SIR10 register) to "0".

Remark 1. m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3)

Remark 2. When the SIRmn register is read, 0000H is always read.

20.3.7 Serial status register mn (SSRmn)

The SSRmn register is a register that indicates the communication status and error occurrence status of channel n. The errors indicated by this register are a framing error, parity error, and overrun error.

The SSRmn register can be read by a 16-bit memory manipulation instruction.

The lower 8 bits of the SSRmn register can be set with an 8-bit memory manipulation instruction with SSRmnL.

Reset signal generation clears the SSRmn register to 0000H.

Figure 20 - 11 Format of Serial status register mn (SSRmn) (1/2)

Address: F0100H, F0101H (SSR00) to F0106H, F0107H (SSR03), F0140H, F0141H (SSR10), F0142H, F0143H (SSR11) After reset: 0000H R

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SSRmn	0	0	0	0	0	0	0	0	0	TSFmn Note 1	BFFmn Note 1	0	0	FEFmn Note 2	PEFmn	OVFmn

TSFmn Note 1	Communication status indication flag of channel n
0	Communication is stopped or suspended.
1	Communication is in progress.
<Clear conditions> • The STmn bit of the STm register is set to 1 (communication is stopped) or the SSmn bit of the SSm register is set to 1 (communication is suspended). • Communication ends. <Set condition> • Communication starts.	

BFFmn Note 1	Buffer register status indication flag of channel n
0	Valid data is not stored in the SDRmn register.
1	Valid data is stored in the SDRmn register.
<Clear conditions> • Transferring transmit data from the SDRmn register to the shift register ends during transmission. • Reading receive data from the SDRmn register ends during reception. • The STmn bit of the STm register is set to 1 (communication is stopped) or the SSmn bit of the SSm register is set to 1 (communication is enabled). <Set conditions> • Transmit data is written to the SDRmn register while the TXEmn bit of the SCRmn register is set to 1 (transmission or transmission and reception mode in each communication mode). • Receive data is stored in the SDRmn register while the RXEmn bit of the SCRmn register is set to 1 (reception or transmission and reception mode in each communication mode). • A reception error occurs.	

Note 1. The SSR00, SSR02, and SSR10 registers only.

Note 2. The SSR01, SSR03, and SSR11 registers only.

Caution When the Simplified SPI(CSI) is performing reception operations in the SNOOZE mode (SWCm = 1), the BFFmn flag will not change.

Remark m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3)

Figure 20 - 11 Format of Serial status register mn (SSRmn) (2/2)

Address: F0100H, F0101H (SSR00) to F0106H, F0107H (SSR03), F0140H, F0141H (SSR10), F0142H, F0143H (SSR11) After reset: 0000H R

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SSRmn	0	0	0	0	0	0	0	0	0	TSFmn Note 1	BFFmn Note 1	0	0	FEFmn Note 2	PEFmn	OVFmn

FEFmn Note 2	Framing error detection flag of channel n
0	No error occurs.
1	An error occurs (during UART reception).
<Clear condition> • 1 is written to the FECTmn bit of the SIRmn register. <Set condition> • A stop bit is not detected when UART reception ends.	

PEFmn	Parity/ACK error detection flag of channel n
0	No error occurs.
1	Parity error occurs (during UART reception) or ACK is not detected (during I^2C transmission).
<Clear condition> • 1 is written to the PECTmn bit of the SIRmn register. <Set condition> • The parity of the transmit data and the parity bit do not match when UART reception ends (parity error). • No ACK signal is returned from the slave channel at the ACK reception timing during I^2C transmission (ACK is not detected).	

OVFmn	Overrun error detection flag of channel n
0	No error occurs.
1	An error occurs
<Clear condition> • 1 is written to the OVCTmn bit of the SIRmn register. <Set condition> • Even though receive data is stored in the SDRmn register, that data is not read and transmit data or the next receive data is written while the RXEmn bit of the SCRmn register is set to 1 (reception or transmission and reception mode in each communication mode). • Transmit data is not ready for slave transmission or transmission and reception in Simplified SPI(CSI) mode.	

Note 1. The SSR00, SSR02, and SSR10 registers only.

Note 2. The SSR01, SSR03, and SSR11 registers only.

Caution 1. If data is written to the SDRmn register when BFFmn = 1, the transmit/receive data stored in the register is discarded and an overrun error (OVEmn = 1) is detected.

Caution 2. When the Simplified SPI(CSI) is performing reception operations in the SNOOZE mode (SWCm = 1), the OVFmn flag will not change.

Remark m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3)

20.3.8 Serial channel start register m (SSm)

The SSm register is a trigger register that is used to enable starting communication/count by each channel.

When 1 is written a bit of this register (SSmn), the corresponding bit (SEmn) of serial channel enable status register m (SEm) is set to 1 (Operation is enabled). Because the SSmn bit is a trigger bit, it is cleared immediately when SEmn = 1.

The SSm register can be set by a 16-bit memory manipulation instruction.

The lower 8 bits of the SSm register can be set with an 1-bit or 8-bit memory manipulation instruction with SSmL.

Reset signal generation clears the SSm register to 0000H.

Figure 20 - 12 Format of Serial channel start register m (SSm)

Address: F0122H, F0123H (SS0) After reset: 0000H R/W

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SS0	0	0	0	0	0	0	0	0	0	0	0	0	SS03	SS02	SS01	SS00

Address: F0162H, F0163H (SS1) After reset: 0000H R/W

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SS1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	SS11	SS10

SSmn	Operation start trigger of channel n
0	No trigger operation
1	Sets the SEmn bit to 1 and enters the communication wait status Note.

Note If set the SSmn = 1 to during a communication operation, will wait status to stop the communication. At this time, holding status value of control register and shift register, SCKmn and SOmn pins, and FEFmn, PEFmn, OVFmn flags.

Caution 1. Be sure to clear bits 15 to 4 of the SS0 register and bits 15 to 2 of the SS1 register to "0".

Caution 2. For the UART reception, set the RXEmn bit of SCRmn register to 1, and then be sure to set SSmn to 1 after 4 or more f_{MCK} clocks have elapsed.

Remark 1. m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3)

Remark 2. When the SSm register is read, 0000H is always read.

20.3.9 Serial channel stop register m (STm)

The STm register is a trigger register that is used to enable stopping communication/count by each channel.

When 1 is written a bit of this register (STmn), the corresponding bit (SEmn) of serial channel enable status register m (SEm) is cleared to 0 (operation is stopped). Because the STmn bit is a trigger bit, it is cleared immediately when SEmn = 0.

The STm register can set written by a 16-bit memory manipulation instruction.

The lower 8 bits of the STm register can be set with a 1-bit or 8-bit memory manipulation instruction with STmL.

Reset signal generation clears the STm register to 0000H.

Figure 20 - 13 Format of Serial channel stop register m (STm)

Address: F0124H, F0125H (ST0) After reset: 0000H R/W

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ST0	0	0	0	0	0	0	0	0	0	0	0	0	ST03	ST02	ST01	ST00

Address: F0164H, F0165H (ST1) After reset: 0000H R/W

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ST1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	ST11	ST10

STmn	Operation stop trigger of channel n
0	No trigger operation
1	Clears the SEmn bit to 0 and stops the communication operation Note.

Note Holding status value of the control register and shift register, the SCKmn and SOmn pins, and FEFmn, PEFmn, OVFmn flags.

Caution Be sure to clear bits 15 to 4 of the ST0 register and bits 15 to 2 of the ST1 register to “0”.

Remark 1. m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3)

Remark 2. When the STm register is read, 0000H is always read.

20.3.10 Serial channel enable status register m (SEm)

The SEm register indicates whether data transmission/reception operation of each channel is enabled or stopped.

When 1 is written a bit of serial channel start register m (SSm), the corresponding bit of this register is set to 1.

When 1 is written a bit of serial channel stop register m (STm), the corresponding bit is cleared to 0.

Channel n that is enabled to operate cannot rewrite by software the value of the CKOmn bit (serial clock output of channel n) of serial output register m (SOm) to be described below, and a value reflected by a communication operation is output from the serial clock pin.

Channel n that stops operation can set the value of the CKOmn bit of the SOm register by software and output its value from the serial clock pin. In this way, any waveform, such as that of a start condition/stop condition, can be created by software.

The SEm register can be read by a 16-bit memory manipulation instruction.

The lower 8 bits of the SEm register can be set with a 1-bit or 8-bit memory manipulation instruction with SEmL.

Reset signal generation clears the SEm register to 0000H.

Figure 20 - 14 Format of Serial channel enable status register m (SEm)

Address: F0120H, F0121H (SE0) After reset: 0000H R

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SE0	0	0	0	0	0	0	0	0	0	0	0	0	SE03	SE02	SE01	SE00

Address: F0160H, F0161H (SE1) After reset: 0000H R

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SE1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	SE11	SE10

SEmn	Indication of operation enable/stop status of channel n
0	Operation stops
1	Operation is enabled.

Remark m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3)

20.3.11 Serial output enable register m (SOEm)

The SOEm register is a register that is used to enable or stop output of the serial communication operation of each channel.

Channel n that enables serial output cannot rewrite by software the value of the SOmn bit of serial output register m (SOm) to be described below, and a value reflected by a communication operation is output from the serial data output pin.

For channel n, whose serial output is stopped, the SOmn bit value of the SOm register can be set by software, and that value can be output from the serial data output pin. In this way, any waveform of the start condition and stop condition can be created by software.

The SOEm register can be set by a 16-bit memory manipulation instruction.

The lower 8 bits of the SOEm register can be set with a 1-bit or 8-bit memory manipulation instruction with SOEmL.

Reset signal generation clears the SOEm register to 0000H.

Figure 20 - 15 Format of Serial output enable register m (SOEm)

Address: F012AH, F012BH (SOE0) After reset: 0000H R/W

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SOE0	0	0	0	0	0	0	0	0	0	0	0	0	0	SOE02	0	SOE00

Address: F016AH, F016BH (SOE1) After reset: 0000H R/W

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SOE1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	SOE10

SOEmn	Serial output enable/stop of channel n
0	Stops output by serial communication operation.
1	Enables output by serial communication operation.

Caution **Be sure to clear bits 15 to 3 and 1 of the SOEm register to “0”.**

Remark m: Unit number (m = 0, 1), n: Channel number (n = 0, 2)

20.3.12 Serial output register m (SOm)

The SOm register is a buffer register for serial output of each channel.

The value of the SOmn bit of this register is output from the serial data output pin of channel n.

The value of the CKOmn bit of this register is output from the serial clock output pin of channel n.

The SOmn bit of this register can be rewritten by software only when serial output is disabled (SOEmn = 0). When serial output is enabled (SOEmn = 1), rewriting by software is ignored, and the value of the register can be changed only by a serial communication operation.

The CKOmn bit of this register can be rewritten by software only when the channel operation is stopped (SEmn = 0). While channel operation is enabled (SEmn = 1), rewriting by software is ignored, and the value of the CKOmn bit can be changed only by a serial communication operation.

To use the pin for serial interface as a port function pin, set the corresponding CKOmn and SOmn bits to “1”.

The SOm register can be set by a 16-bit memory manipulation instruction.

Reset signal generation sets the SO0 register to 0F0FH, and the SO1 register to 0303H.

Figure 20 - 16 Format of Serial output register m (SOm)

Address: F0128H, F0129H (SO0) After reset: 0F0FH R/W

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SO0	0	0	0	0	1	CKO 02	1	CKO 00	0	0	0	0	1	SO 02	1	SO 00

Address: F0168H, F0169H (SO1) After reset: 0303H R/W

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SO1	0	0	0	0	0	0	1	CKO 10	0	0	0	0	0	0	1	SO 10

CKO mn	Serial clock output of channel n
0	Serial clock output value is “0”.
1	Serial clock output value is “1”.

SO mn	Serial data output of channel n
0	Serial data output value is “0”.
1	Serial data output value is “1”.

Caution **Be sure to clear bits 15 to 12 and 7 to 4 of the SO0 register to “0”. And be sure to set bits 11, 9, 3 and 1 to “1”.**
Be sure to clear bits 15 to 10 and 7 to 2 of the SO1 register to “0”. And be sure to set bits 9 and 1 to “1”.

Remark m: Unit number (m = 0, 1), n: Channel number (n = 0, 2)

20.3.13 Serial output level register m (SOLm)

The SOLm register is a register that is used to set inversion of the data output level of each channel.

This register can be set only in the UART mode. Be sure to set 0 for corresponding bit in the Simplified SPI(CSI) mode and simplifies I^2C mode.

Inverting channel n by using this register is reflected on pin output only when serial output is enabled (SOEmn = 1). When serial output is disabled (SOEmn = 0), the value of the SOmn bit is output as is.

Rewriting the SOLm register is prohibited when the register is in operation (when SEmn = 1).

The SOLm register can be set by a 16-bit memory manipulation instruction.

The lower 8 bits of the SOLm register can be set with an 8-bit memory manipulation instruction with SOLmL.

Reset signal generation clears the SOLm register to 0000H.

Figure 20 - 17 Format of Serial output level register m (SOLm)

Address: F0134H, F0135H (SOL0) After reset: 0000H R/W

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SOL0	0	0	0	0	0	0	0	0	0	0	0	0	0	SOL02	0	SOL00

Address: F0174H, F0175H (SOL1) After reset: 0000H R/W

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SOL1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	SOL10

SOLmn	Selects inversion of the level of the transmit data of channel n in UART mode
0	Communication data is output as is.
1	Communication data is inverted and output.

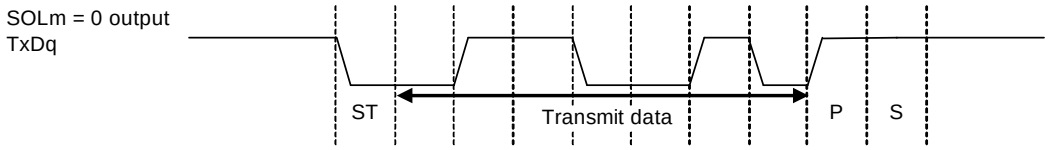
Caution **Be sure to clear bits 15 to 3, and 1 of the SOL0 register to “0”.**
Be sure to clear bits 15 to 1 of the SOL1 register to “0”.

Remark m: Unit number (m = 0, 1), n: Channel number (n = 0, 2)

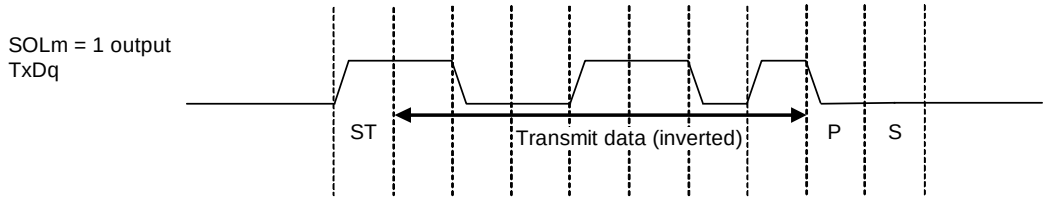
Figure 20 - 18 shows examples in which the level of transmit data is reversed during UART transmission.

Figure 20 - 18 Examples of Reverse Transmit Data

(a) Non-reverse Output (SOLmn = 0)



(b) Reverse Output (SOLmn = 1)



Remark m: Unit number (m = 0, 1), n: Channel number (n = 0, 2)

20.3.14 Serial standby control register m (SSCm)

The SSC0 register is used to control the startup of reception (the SNOOZE mode) while in the STOP mode when receiving CSI00 or UART0 serial data.

The SSC1 register is used to control the startup of reception (the SNOOZE mode) while in the STOP mode when receiving CSI20 and UART2 serial data.

The SSCm register can be set by a 16-bit memory manipulation instruction.

The lower 8 bits of the SSCm register can be set with an 8-bit memory manipulation instruction with SSCmL.

Reset signal generation clears the SSCm register to 0000H.

Caution The maximum transfer rate in the SNOOZE mode is as follows.

- **When using CSI00, CSI20: Up to 1 Mbps**
- **When using UART0, UART2: 4800 bps only**

Figure 20 - 19 Format of Serial standby control register m (SSCm)

Address: F0138H (SSC0), F0178H (SSC1) After reset: 0000H R/W

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SSCm	0	0	0	0	0	0	0	0	0	0	0	0	0	0	SSECm	SWCm

SSECm	Selection of whether to enable or disable the generation of communication error interrupts in the SNOOZE mode
0	Enable the generation of error interrupts (INTSRE0/INTSRE2).
1	Stop the generation of error interrupts (INTSRE0/INTSRE2).
• The SSECm bit can be set to 1 or 0 only when both the SWCm and EOCmn bits are set to 1 during UART reception in the SNOOZE mode. In other cases, clear the SSECm bit to 0. • Setting SSECm, SWCm = 1, 0 is prohibited.	

SWCm	Setting of the SNOOZE mode
0	Do not use the SNOOZE mode function.
1	Use the SNOOZE mode function.
• When there is a hardware trigger signal in the STOP mode, the STOP mode is exited, and A/D conversion is performed without operating the CPU (the SNOOZE mode). • The SNOOZE mode function can only be specified when the high-speed on-chip oscillator clock is selected for the CPU/peripheral hardware clock (f_{CLK}). If any other clock is selected, specifying this mode is prohibited. • Even when using SNOOZE mode, be sure to set the SWCm bit to 0 in normal operation mode and change it to 1 just before shifting to STOP mode. Also, be sure to change the SWCm bit to 0 after returning from STOP mode to normal operation mode.	

Caution Setting SSECm, SWCm = 1, 0 is prohibited.

Figure 20 - 20 Interrupt in UART Reception Operation in SNOOZE Mode

EOCmn Bit	SSECm Bit	Reception Ended Successfully	Reception Ended in an Error
0	0	INTSRx is generated.	INTSRx is generated.
0	1	INTSRx is generated.	INTSRx is generated.
1	0	INTSRx is generated.	INTSREx is generated.
1	1	INTSRx is generated.	No interrupt is generated.

20.3.15 Input switch control register (ISC)

The ISC1 and ISC0 bits of the ISC register are used to realize a LIN-bus communication operation by UART0 in coordination with an external interrupt and the timer array unit.

When bit 0 is set to 1, the input signal of the serial data input (RXD0) pin is selected as an external interrupt (INTP0) that can be used to detect a wakeup signal.

When bit 1 is set to 1, the input signal of the serial data input (RXD0) pin is selected as a timer input, so that wake up signal can be detected, the low width of the break field, and the pulse width of the sync field can be measured by the timer.

The SSIE00 bit controls the $\overline{\text{SSI00}}$ pin input of channel 0 during CSI00 communication and in slave mode. While a high level is being input to the $\overline{\text{SSI00}}$ pin, no transmission/reception operation is performed even if a serial clock is input. While a low level is being input to the $\overline{\text{SSI00}}$ pin, a transmission/reception operation is performed according to each mode setting if a serial clock is input.

The ISC register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears the ISC register to 00H.

Figure 20 - 21 Format of Input switch control register (ISC)

Address: F0073H After reset: 00H R/W

Symbol	<7>	6	5	4	3	2	1	0
ISC	SSIE00	0	0	0	0	0	ISC1	ISC0

SSIE00	Channel 0 $\overline{\text{SSI00}}$ input setting in CSI00 communication and slave mode
0	Disables $\overline{\text{SSI00}}$ pin input.
1	Enables $\overline{\text{SSI00}}$ pin input.

ISC1	Switching channel 7 input of timer array unit
0	Uses the input signal of the TI07 pin as a timer input (normal operation).
1	Input signal of the RxD0 pin is used as timer input (detects the wakeup signal and measures the low width of the break field and the pulse width of the sync field).

ISC0	Switching external interrupt (INTP0) input
0	Uses the input signal of the INTP0 pin as an external interrupt (normal operation).
1	Uses the input signal of the RxD0 pin as an external interrupt (wakeup signal detection).

Caution Be sure to clear bits 6 to 2 to “0”.

20.3.16 Noise filter enable register 0 (NFEN0)

The NFEN0 register is used to set whether the noise filter can be used for the input signal from the serial data input pin to each channel.

Disable the noise filter of the pin used for Simplified SPI(CSI) or simplified I^2C communication, by clearing the corresponding bit of this register to 0.

Enable the noise filter of the pin used for UART communication, by setting the corresponding bit of this register to 1.

When the noise filter is enabled, after synchronization is performed with the operation clock (f_{MCK}) of the target channel, 2-clock match detection is performed. When the noise filter is disabled, only synchronization is performed with the operation clock (f_{MCK}) of the target channel.

The NFEN0 register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears the NFEN0 register to 00H.

Figure 20 - 22 Format of Noise filter enable register 0 (NFEN0)

Address: F0070H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
NFEN0	0	0	0	SNFEN20	0	SNFEN10	0	SNFEN00

SNFEN20	Use of noise filter of RxD2 pin
0	Noise filter OFF
1	Noise filter ON
Set SNFEN20 to 1 to use the RxD2 pin. Clear SNFEN20 to 0 to use the other than RxD2 pin.	

SNFEN10	Use of noise filter of RxD1 pin
0	Noise filter OFF
1	Noise filter ON
Set the SNFEN10 bit to 1 to use the RxD1 pin. Clear the SNFEN10 bit to 0 to use the other than RxD1 pin.	

SNFEN00	Use of noise filter of RxD0 pin
0	Noise filter OFF
1	Noise filter ON
Set the SNFEN00 bit to 1 to use the RxD0 pin. Clear the SNFEN00 bit to 0 to use the other than RxD0 pin.	

Caution Be sure to clear bits 7 to 5, 3, and 1 to “0”.

20.3.17 Registers that control port functions of serial input/output pins

Using the serial array unit requires setting of the registers that control the port functions for the port pins with which the serial array unit pin functions for the target channel are multiplexed (port mode register (PMxx), port register (Pxx), port input mode register (PIMxx), port output mode register (POMxx), port mode control registers (PMCxx)).

For details, see **4.4.1 Port mode registers (PMxx)**, **4.4.2 Port registers (Pxx)**, **4.4.4 Port input mode registers (PIMxx)**, **4.4.5 Port output mode registers (POMxx)**, and **4.4.6 Port mode control registers (PMCxx)**.

Using a port pin which is multiplexed with a serial data output or serial clock output pin function (e.g. P06/SO20/TxD2/TI00/SEG27) for serial data output or serial clock output requires setting the corresponding bits in the LCD port function register (PFSEGx), port mode control register (PMCxx), and port mode register (PMxx) to 0, and the corresponding bit in the port register (Pxx) to 1.

Using a port pin in N-ch open-drain output (V_{DD} tolerance) mode requires setting the corresponding bit in the port output mode register (POMxx) to 1. When connecting an external device operating at a different voltage (1.8 V Note, 2.5 V, or 3 V), see **4.5.4 Handling different potential (1.8 V Note, 2.5 V, 3 V) by using I/O buffers**.

Example When P06/SO20/TxD2/TI00/SEG27 is to be used for serial data output
Set the PFSEG27 bit of LCD port function register 4 to 0.
Set the PM06 bit of port mode register 0 to 0.
Set the P06 bit of port register 0 to 1.

Using a port pin which is multiplexed with a serial data input or serial clock input pin function (e.g. P07/SI20/RxD2/SDA20/TI05/TO05/SEG28) for serial data input or serial clock input requires setting the corresponding bits in the LCD port function register (PFSEGx) and port mode control register (PMCxx) to 0, and the corresponding bit in the port mode register (PMxx) to 1. At this time, the value of the corresponding bit in the port register (Pxx) may be 0 or 1.

Using a TTL input buffer requires setting the corresponding bit in the port input mode register (PIMxx) to 1. When connecting an external device operating at a different voltage (1.8 V Note, 2.5 V, or 3 V), see **4.5.4 Handling different potential (1.8 V Note, 2.5 V, 3 V) by using I/O buffers**.

Example When P07/SI20/RxD2/SDA20/TI05/TO05/SEG28 is to be used for serial data input
Set the PFSEG28 bit of LCD port function register 4 to 0.
Set the PM07 bit of port mode register 0 to 1.
Set the P07 bit of port register 0 to 0 or 1.

Note R5F11R only.

20.4 Operation Stop Mode

Each serial interface of serial array unit has the operation stop mode.

In this mode, serial communication cannot be executed, thus reducing the power consumption.

In addition, the pin for serial interface can be used as port function pins in this mode.

20.4.1 Stopping the operation by units

The stopping of the operation by units is set by using peripheral enable register 0 (PER0).

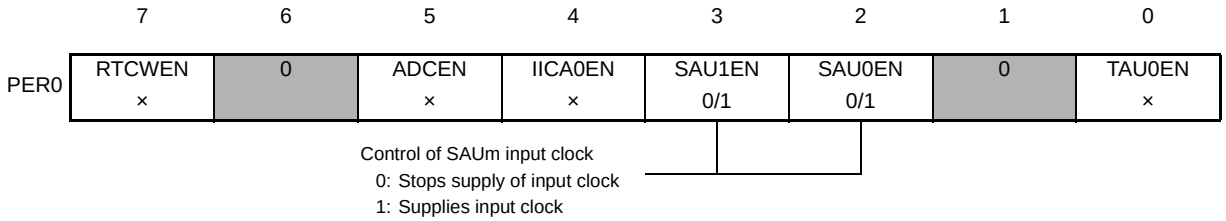
The PER0 register is used to enable or disable supplying the clock to the peripheral hardware. Clock supply to the hardware that is not used is also stopped so as to decrease the power consumption and noise.

To stop the operation of serial array unit 0, set bit 2 (SAU0EN) to 0.

To stop the operation of serial array unit 1, set bit 3 (SAU1EN) to 0.

Figure 20 - 23 Peripheral Enable Register 0 (PER0) Setting When Stopping the Operation by Units

(a) Peripheral enable register 0 (PER0)... Set only the bit of SAUm to be stopped to 0.



Caution 1. If SAUmEN = 0, writing to a control register of serial array unit m is ignored, and, even if the register is read, only the default value is read Note that this does not apply to the following registers.

- **Input switch control register (ISC)**
- **Noise filter enable register 0 (NFEN0)**
- **Port input mode registers 0, 1, 3, 4, 5, 8 (PIM0, PIM1, PIM3, PIM4, PIM5, PIM8)**
- **Port output mode registers 0, 1, 3, 4, 5, 8 (POM0, POM1, POM3, POM4, POM5, POM8)**
- **Port mode registers 0, 1, 3, 4, 5, 8 (PM0, PM1, PM3, PM4, PM5, PM8)**
- **Port registers 0, 1, 3, 4, 5, 8 (P0, P1, P3, P4, P5, P8)**

Caution 2. Be sure to clear bits 1 and 6 to "0".

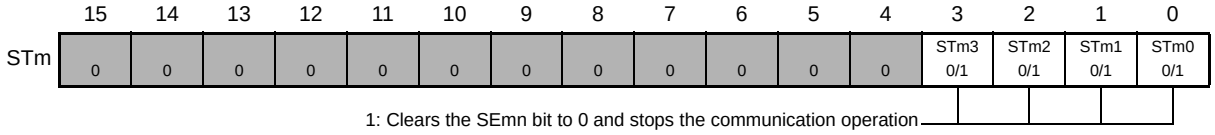
Remark ×: Bits not used with serial array units (depending on the settings of other peripheral functions)
0/1: Set to 0 or 1 depending on the usage of the user

20.4.2 Stopping the operation by channels

The stopping of the operation by channels is set using each of the following registers.

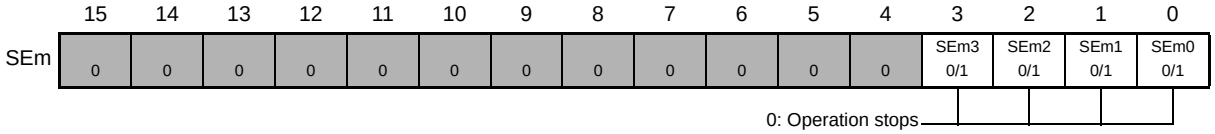
Figure 20 - 24 Each Register Setting When Stopping the Operation by Channels

(a) Serial channel stop register m (STm)... This register is a trigger register that is used to enable stopping communication/count by each channel.



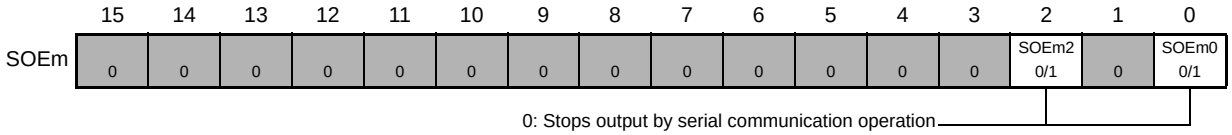
* Because the STmn bit is a trigger bit, it is cleared immediately when SEmn = 0.

(b) Serial Channel Enable Status Register m (SEm)... This register indicates whether data transmission/reception operation of each channel is enabled or stopped.



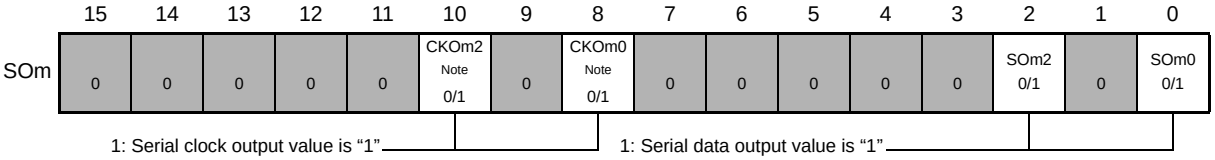
* The SEm register is a read-only status register, whose operation is stopped by using the STm register.
With a channel whose operation is stopped, the value of the CKOmn bit of the SOm register can be set by software.

(c) Serial output enable register m (SOEm)... This register is a register that is used to enable or stop output of the serial communication operation of each channel.



* For channel n, whose serial output is stopped, the SOmn bit value of the SOm register can be set by software.

(d) Serial output register m (SOm)... This register is a buffer register for serial output of each channel.



* When using pins corresponding to each channel as port function pins, set the corresponding CKOmn, SOmn bits to “1”.

Note Serial array unit 0 only.

Remark 1. m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3)

Remark 2. ■: Setting disabled (set to the initial value)
0/1: Set to 0 or 1 depending on the usage of the user

20.5 Operation of Simplified SPI(CSI) (CSI00, CSI10, CSI20) Communication

This is a clocked communication function that uses three lines: serial clock (SCK) and serial data (SI and SO) lines.

[Data transmission/reception]
- Data length of 7 or 8 bits
- Phase control of transmit/receive data
- MSB/LSB first selectable

[Clock control]
- Master/slave selection
- Phase control of I/O clock
- Setting of transfer period by prescaler and internal counter of each channel
- Maximum transfer rate Note

  During master communication: Max. f_{CLK}/2 (CSI00 only)
  Max. f_{CLK}/4
  During slave communication: Max. f_{MCK}/6

[Interrupt function]
- Transfer end interrupt/buffer empty interrupt

[Error detection flag]
- Overrun error

In addition, CSI00 and CSI20 support the SNOOZE mode. When SCK input is detected while in the STOP mode, the SNOOZE mode makes data reception that does not require the CPU possible.
CSI00 support the slave select function. For details, refer to **20.6 Clock Synchronous Serial Communication with Slave Select Input Function**.

Note Use the clocks within a range satisfying the SCK cycle time (t_{KCY}) characteristics. For details, see **CHAPTER 38** or **CHAPTER 39 ELECTRICAL SPECIFICATIONS**.

The channels supporting Simplified SPI (CSI00, CSI10, CSI20) are channels 0 and 2 of SAU0, and channels 0 and 2 of SAU1.

Unit	Channel	Used as Simplified SPI(CSI)	Used as UART	Used as Simplified I^2C
0	0	CSI00 (supporting slave select input function)	UART0 (supporting LIN-bus)	IIC00
	1	—		—
	2	CSI10	UART1	IIC10
	3	—		—
1	0	CSI20	UART2	IIC20
	1	—		—

Simplified SPI (CSI00, CSI10, CSI20) performs the following seven types of communication operations.

- Master transmission (See **20.5.1**.)
- Master reception (See **20.5.2**.)
- Master transmission/reception (See **20.5.3**.)
- Slave transmission (See **20.5.4**.)
- Slave reception (See **20.5.5**.)
- Slave transmission/reception (See **20.5.6**.)
- SNOOZE mode function (See **20.5.7**.)

20.5.1 Master transmission

Master transmission is that the RL78 microcontroller outputs a transfer clock and transmits data to another device.

Simplified SPI	CSI00	CSI10	CSI20
Target channel	Channel 0 of SAU0	Channel 2 of SAU0	Channel 0 of SAU1
Pins used	SCK00, SO00	SCK10, SO10	SCK20, SO20
Interrupt	INTCSI00	INTCSI10	INTCSI20
	Transfer end interrupt (in single-transfer mode) or buffer empty interrupt (in continuous transfer mode) can be selected.		
Error detection flag	None		
Transfer data length	7 or 8 bits		
Transfer rate Note	Max. $f_{CLK}/2$ [Hz] (CSI00 only), $f_{CLK}/4$ [Hz] Min. $f_{CLK}/(2 \times 2^{15} \times 128)$ [Hz] f_{CLK}: System clock frequency		
Data phase	Selectable by the DAPmn bit of the SCRmn register • DAPmn = 0: Data output starts from the start of the operation of the serial clock. • DAPmn = 1: Data output starts half a clock before the start of the serial clock operation.		
Clock phase	Selectable by the CKPmn bit of the SCRmn register • CKPmn = 0: Non-reverse • CKPmn = 1: Reverse		
Data direction	MSB or LSB first		

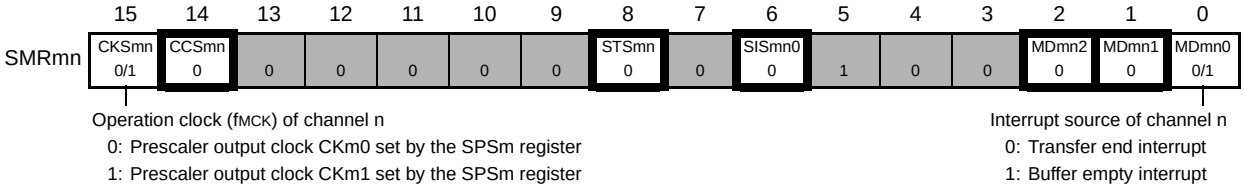
Note Use this operation within a range that satisfies the conditions above and the peripheral functions characteristics in the electrical specifications (see **CHAPTER 38** or **CHAPTER 39 ELECTRICAL SPECIFICATIONS**).

Remark m: Unit number (m = 0, 1), n: Channel number (n = 0, 2), mn = 00, 02, 10

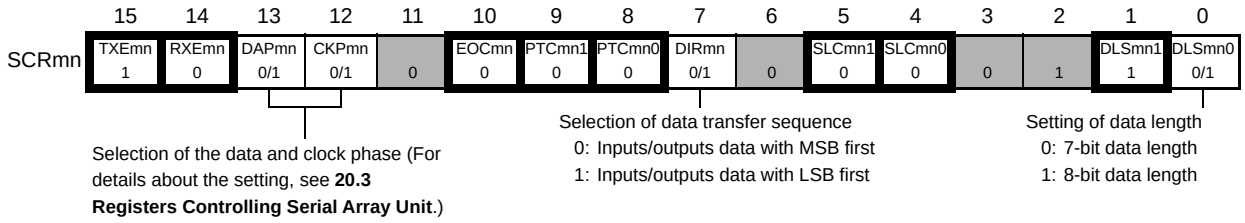
(1) Register setting

Figure 20 - 25 Example of Contents of Registers for Master Transmission of Simplified SPI (CSI00, CSI10, CSI20)

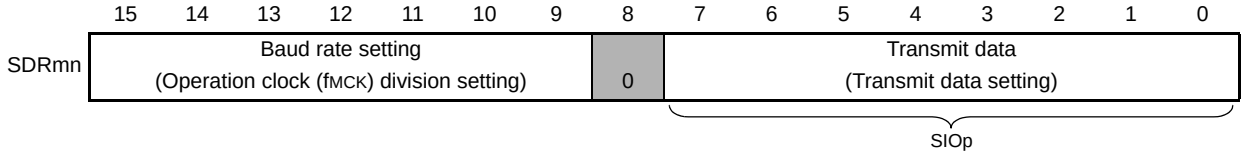
(a) Serial mode register mn (SMRmn)



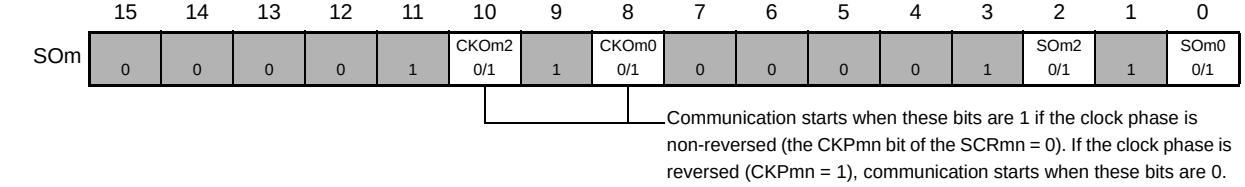
(b) Serial communication operation setting register mn (SCRmn)



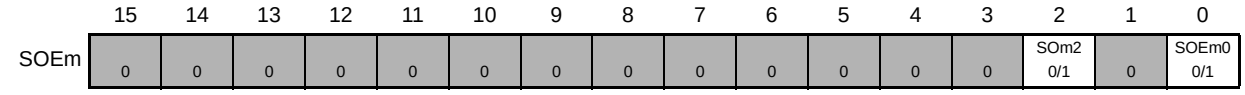
(c) Serial data register mn (SDRmn) (lower 8 bits: SIOp)



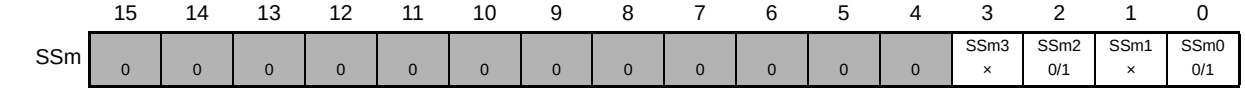
(d) Serial output register m (SOm)... Sets only the bits of the target channel.



(e) Serial output enable register m (SOEm)... Sets only the bits of the target channel to 1.



(f) Serial channel start register m (SSm)... Sets only the bits of the target channel to 1.



Remark 1. m: Unit number (m = 0, 1), n: Channel number (n = 0, 2), p: CSI number (p = 00, 10, 20), mn = 00, 02, 10

Remark 2. ■: Setting is fixed in the Simplified SPI(CSI) master transmission mode,
■: Setting disabled (set to the initial value)
0/1: Set to 0 or 1 depending on the usage of the user

(2) Operation procedure

Figure 20 - 26 Initial Setting Procedure for Master Transmission

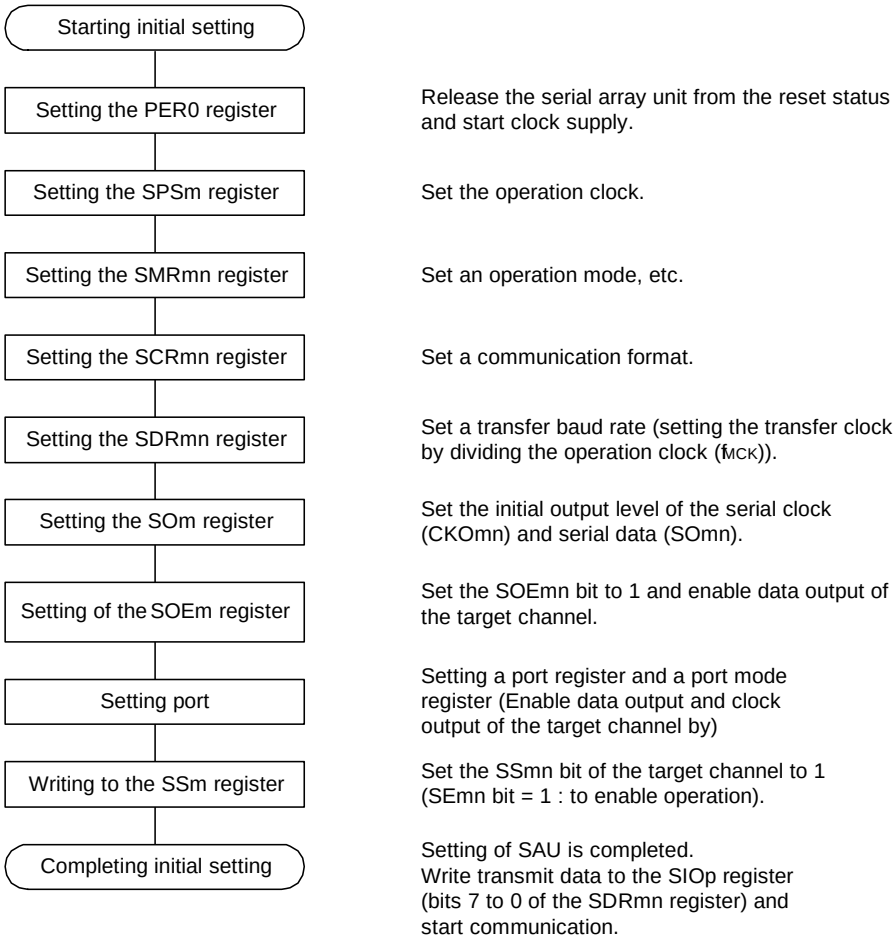


Figure 20 - 27 Procedure for Stopping Master Transmission

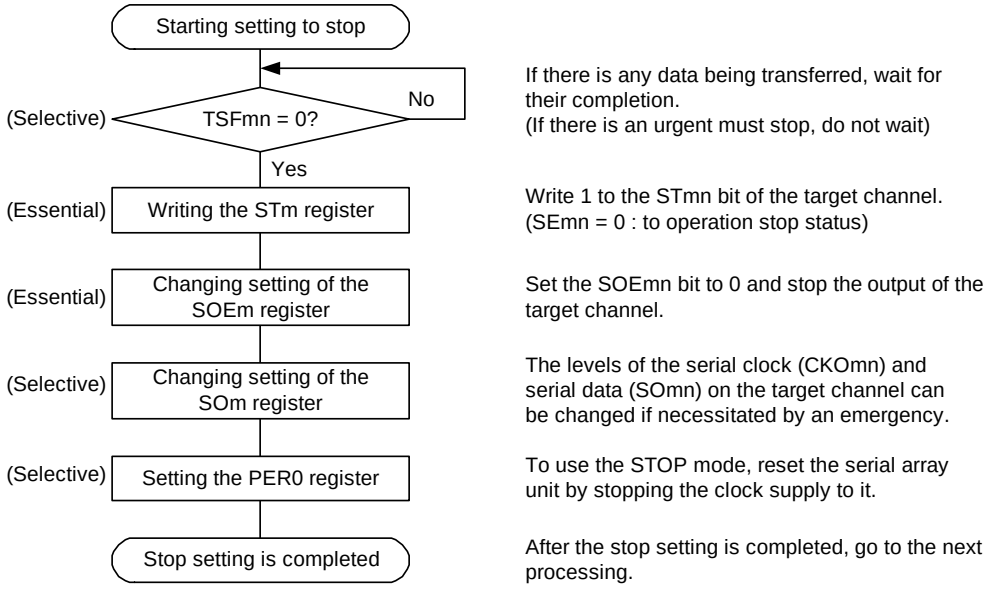
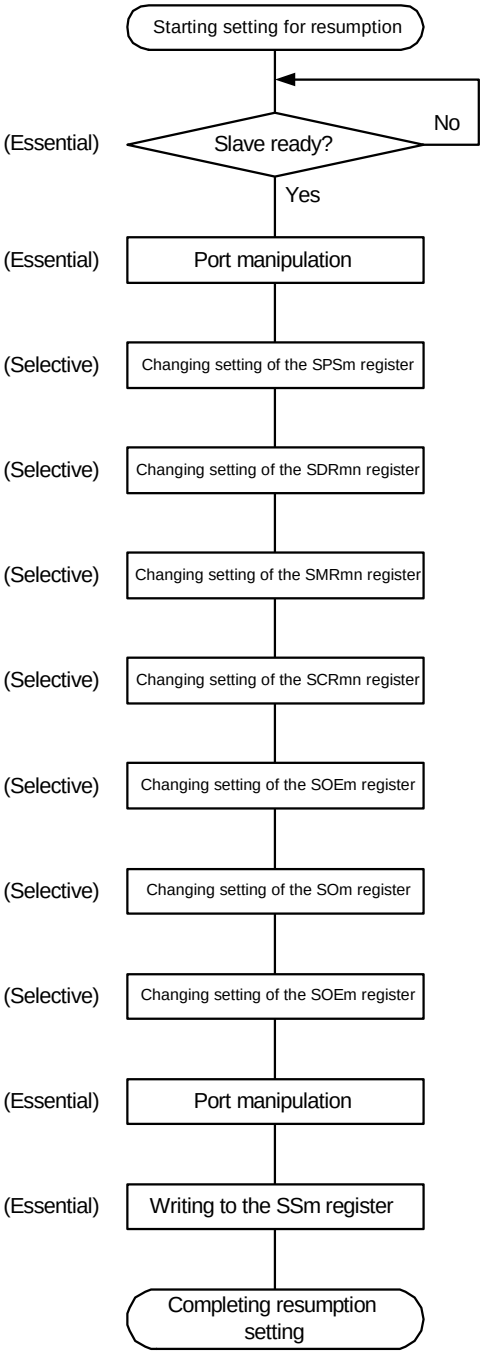


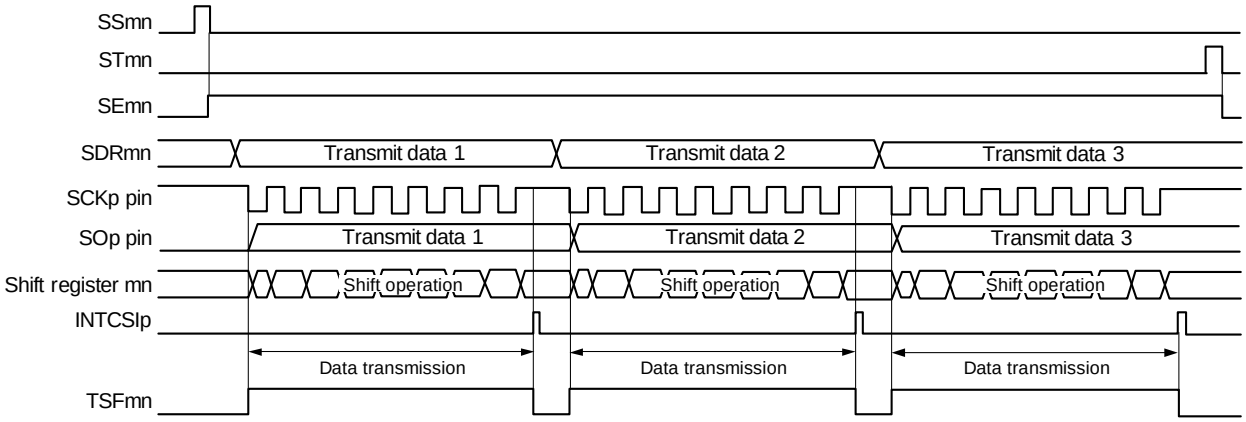
Figure 20 - 28 Procedure for Resuming Master Transmission



Remark If PER0 is rewritten while stopping the master transmission and the clock supply is stopped, wait until the transmission target (slave) stops or transmission finishes, and then perform initialization instead of restarting the transmission.

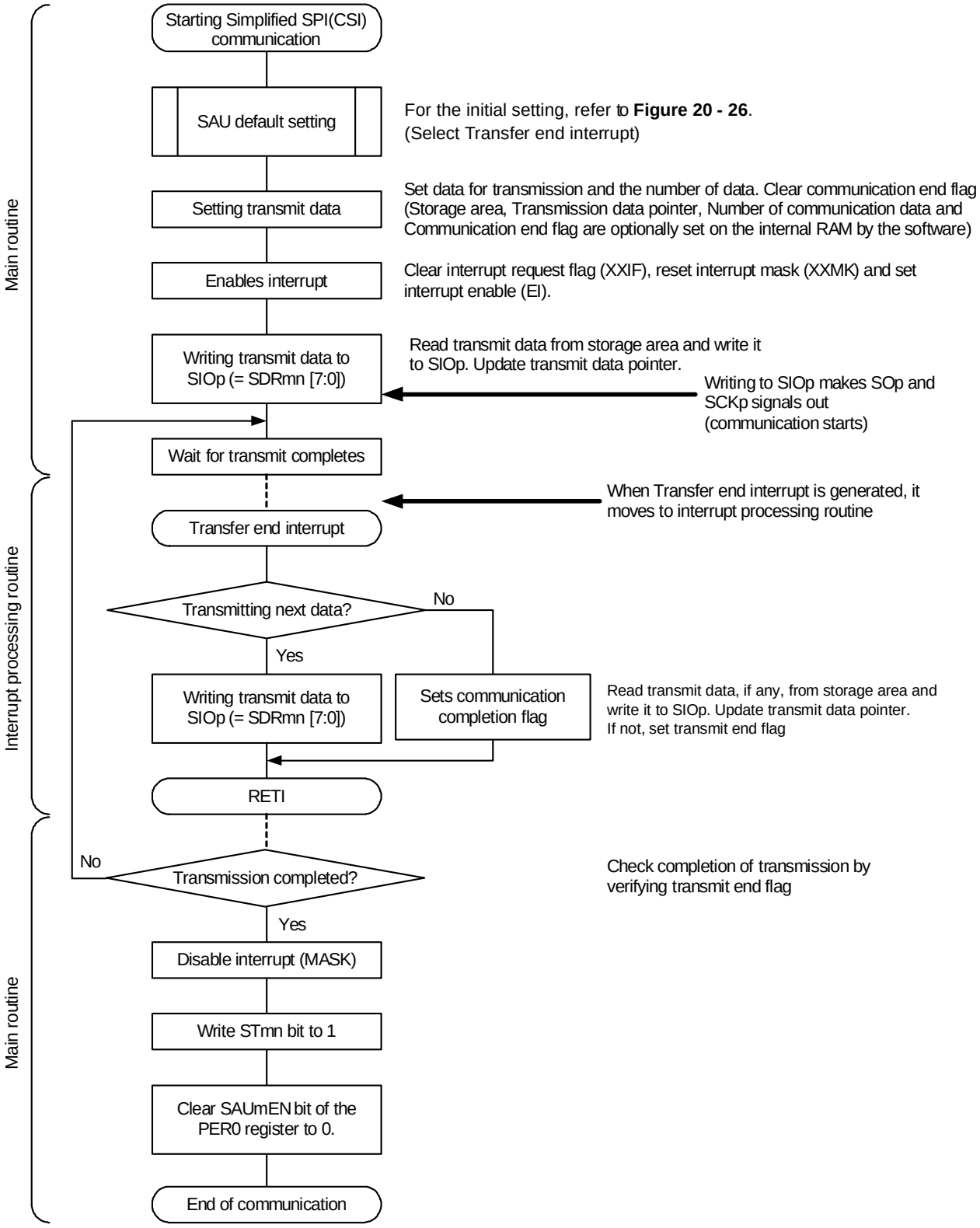
(3) Processing flow (in single-transmission mode)

Figure 20 - 29 Timing Chart of Master Transmission (in Single-Transmission Mode)
(Type 1: DAPmn = 0, CKPmn = 0)



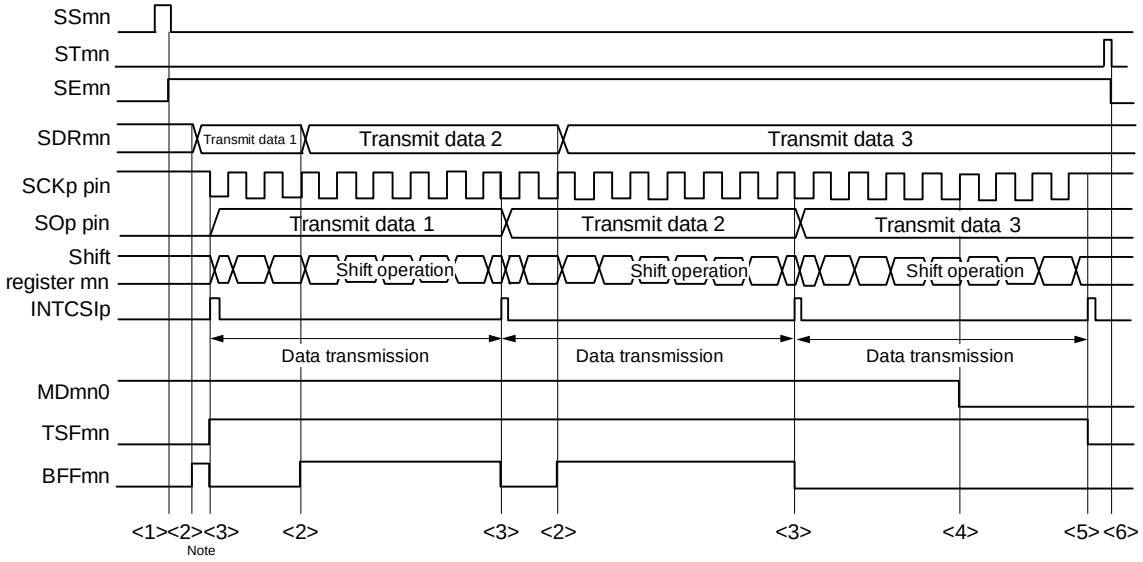
Remark m: Unit number (m = 0, 1), n: Channel number (n = 0, 2), p: CSI number (p = 00, 10, 20), mn = 00, 02, 10

Figure 20 - 30 Flowchart of Master Transmission (in Single-Transmission Mode)



(4) Processing flow (in continuous transmission mode)

Figure 20 - 31 Timing Chart of Master Transmission (in Continuous Transmission Mode)
(Type 1: DAPmn = 0, CKPmn = 0)

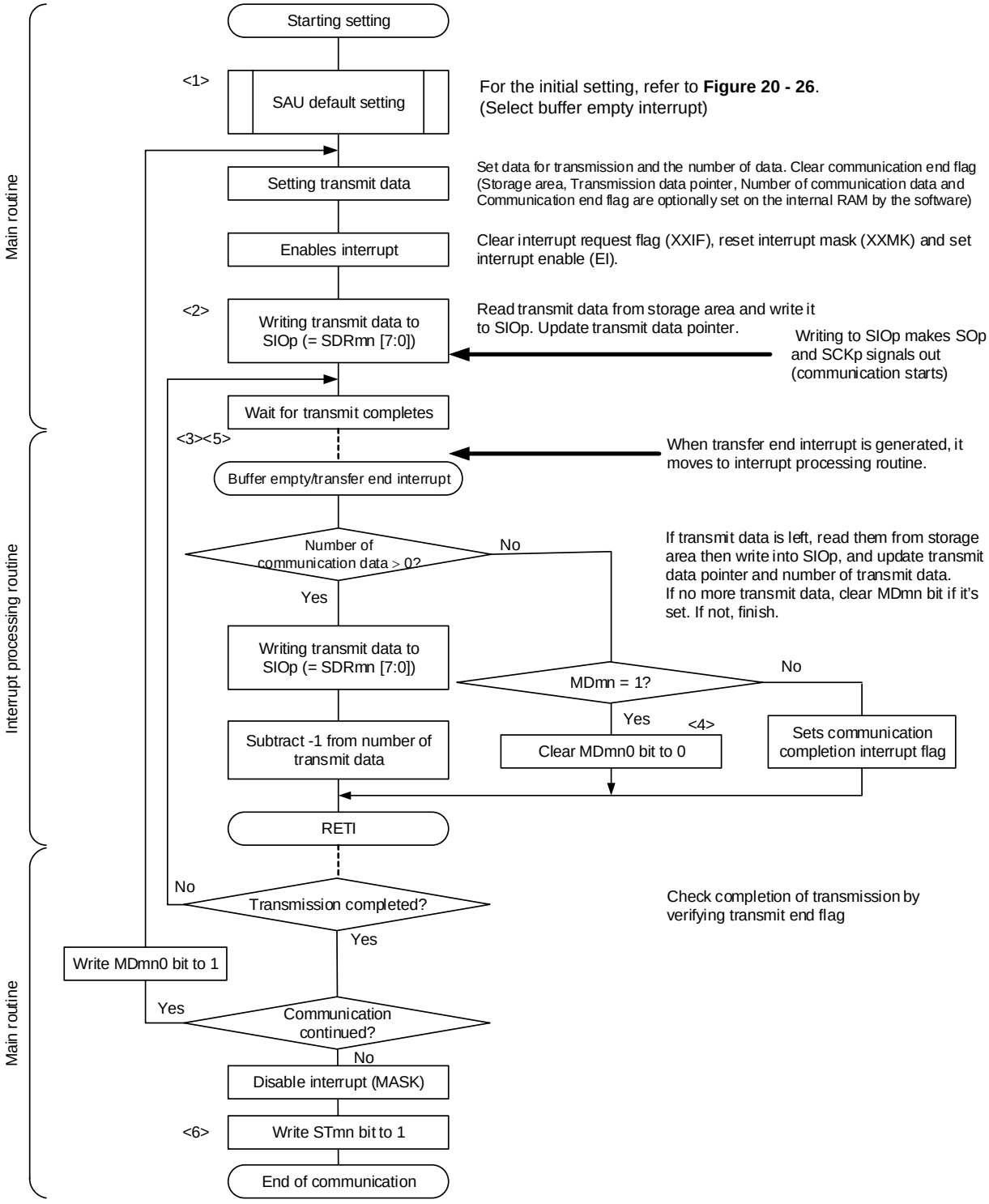


Note If transmit data is written to the SDRmn register while the BFFmn bit of serial status register mn (SSRmn) is 1 (valid data is stored in serial data register mn (SDRmn)), the transmit data is overwritten.

Caution **The MDmn0 bit of serial mode register mn (SMRmn) can be rewritten even during operation. However, rewrite it before transfer of the last bit is started, so that it will be rewritten before the transfer end interrupt of the last transmit data.**

Remark m: Unit number (m = 0, 1), n: Channel number (n = 0, 2), p: CSI number (p = 00, 10, 20), mn = 00, 02, 10

Figure 20 - 32 Flowchart of Master Transmission (in Continuous Transmission Mode)



Remark <1> to <6> in the figure correspond to <1> to <6> in **Figure 20 - 31 Timing Chart of Master Transmission (in Continuous Transmission Mode)**.

20.5.2 Master reception

Master reception is that the RL78 microcontroller outputs a transfer clock and receives data from other device.

Simplified SPI	CSI00	CSI10	CSI20
Target channel	Channel 0 of SAU0	Channel 2 of SAU0	Channel 0 of SAU1
Pins used	SCK00, SI00	SCK10, SI10	SCK20, SI20
Interrupt	INTCSI00	INTCSI10	INTCSI20
	Transfer end interrupt (in single-transfer mode) or buffer empty interrupt (in continuous transfer mode) can be selected.		
Error detection flag	Overrun error detection flag (OVFmn) only		
Transfer data length	7 or 8 bits		
Transfer rate Note	Max. $f_{CLK}/2$ [Hz] (CSI00 only), $f_{CLK}/4$ [Hz] Min. $f_{CLK}/(2 \times 2^{15} \times 128)$ [Hz] f_{CLK}: System clock frequency		
Data phase	Selectable by the DAPmn bit of the SCRmn register • DAPmn = 0: Data input starts from the start of the operation of the serial clock. • DAPmn = 1: Data input starts half a clock before the start of the serial clock operation.		
Clock phase	Selectable by the CKPmn bit of the SCRmn register • CKPmn = 0: Non-reverse • CKPmn = 1: Reverse		
Data direction	MSB or LSB first		

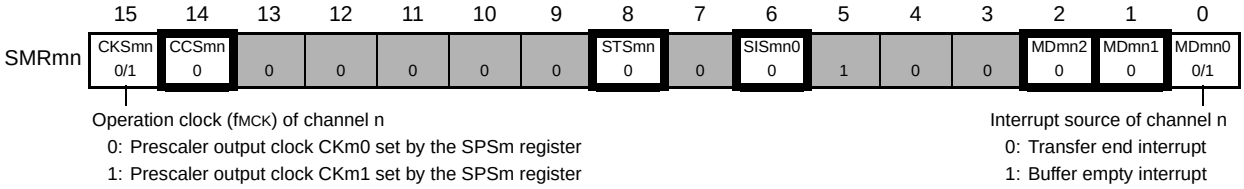
Note Use this operation within a range that satisfies the conditions above and the peripheral functions characteristics in the electrical specifications (see **CHAPTER 38** or **CHAPTER 39 ELECTRICAL SPECIFICATIONS**).

Remark m: Unit number (m = 0, 1), n: Channel number (n = 0, 2), mn = 00, 02, 10

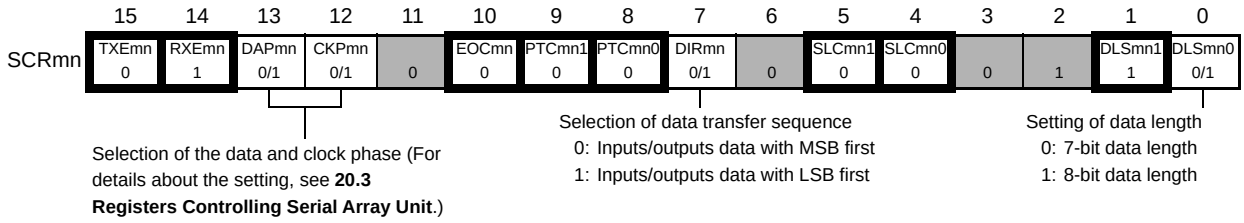
(1) Register setting

Figure 20 - 33 Example of Contents of Registers for Master Reception of Simplified SPI (CSI00, CSI10, CSI20)

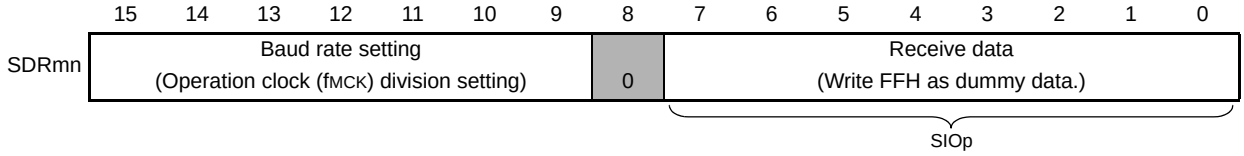
(a) Serial mode register mn (SMRmn)



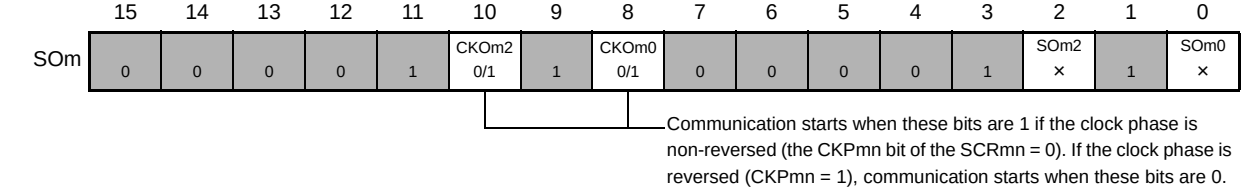
(b) Serial communication operation setting register mn (SCRmn)



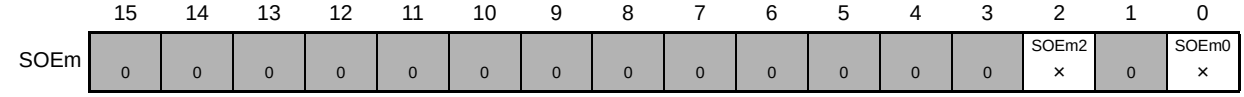
(c) Serial data register mn (SDRmn) (lower 8 bits: SIOp)



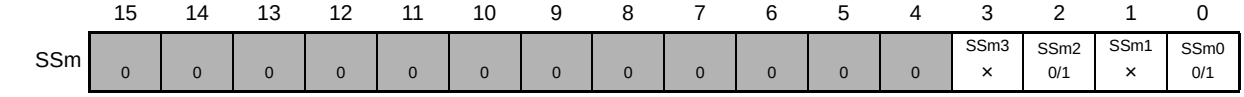
(d) Serial output register m (SOm)... Sets only the bits of the target channel.



(e) Serial output enable register m (SOEm)... The register that not used in this mode.



(f) Serial channel start register m (SSm)... Sets only the bits of the target channel to 1.



Remark 1. m: Unit number (m = 0, 1), n: Channel number (n = 0, 2), p: CSI number (p = 00, 10, 20), mn = 00, 02, 10

Remark 2. ■: Setting is fixed in the Simplified SPI(CSI) master reception mode,
■: Setting disabled (set to the initial value)
×: Bit that cannot be used in this mode (set to the initial value when not used in any mode)
0/1: Set to 0 or 1 depending on the usage of the user

(2) Operation procedure

Figure 20 - 34 Initial Setting Procedure for Master Reception

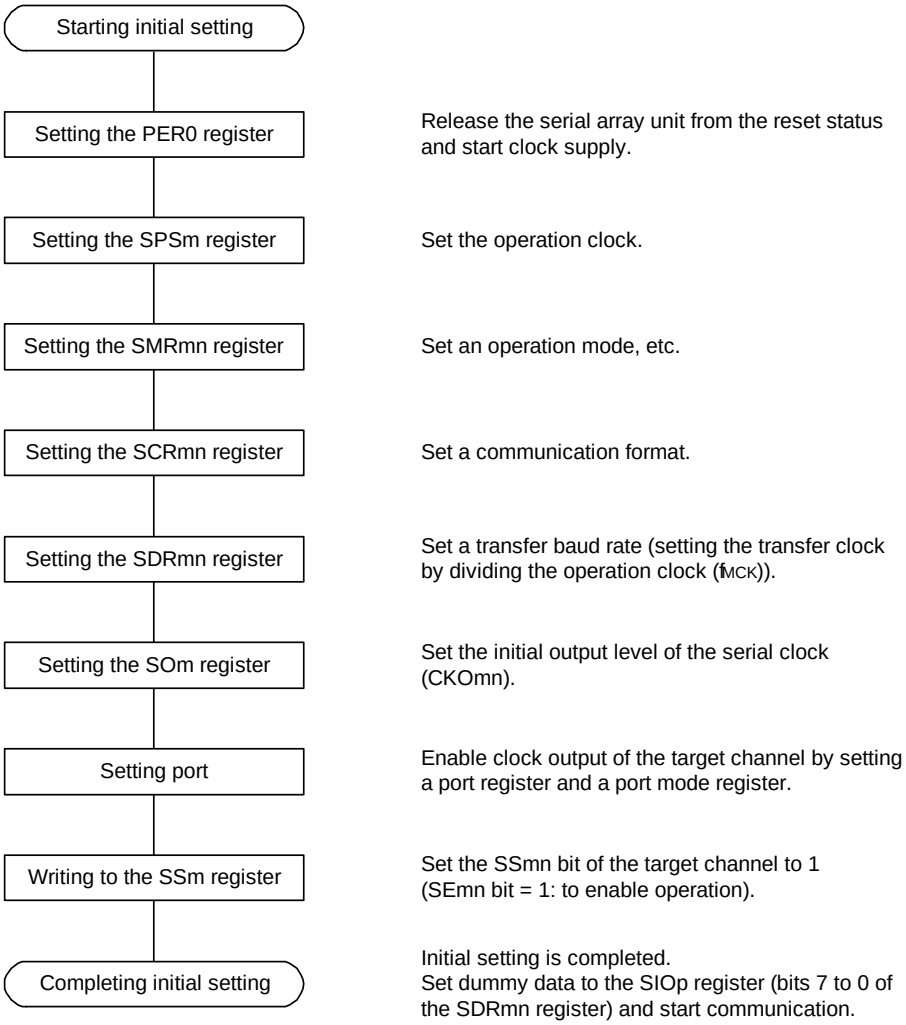


Figure 20 - 35 Procedure for Stopping Master Reception

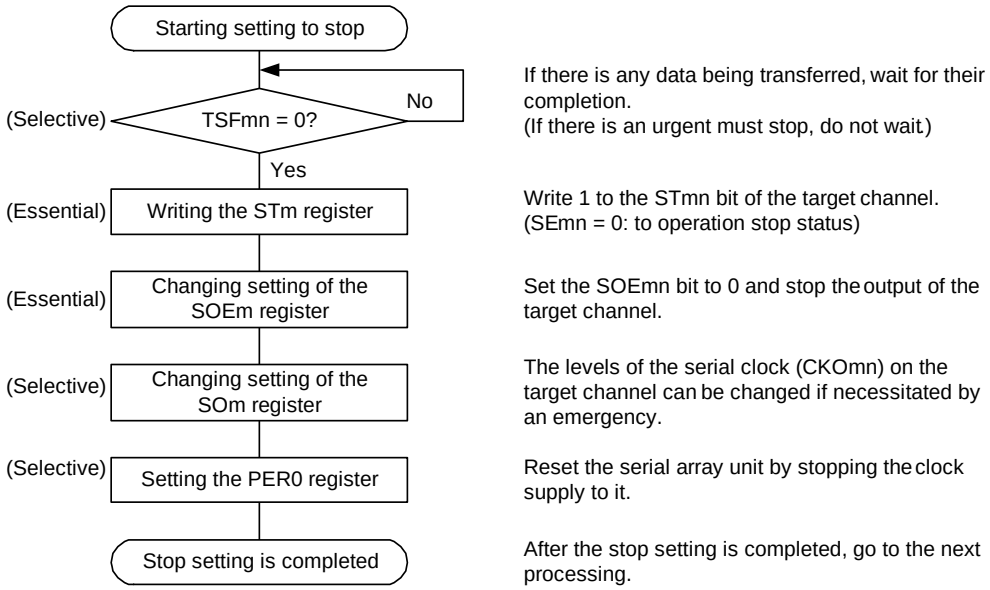
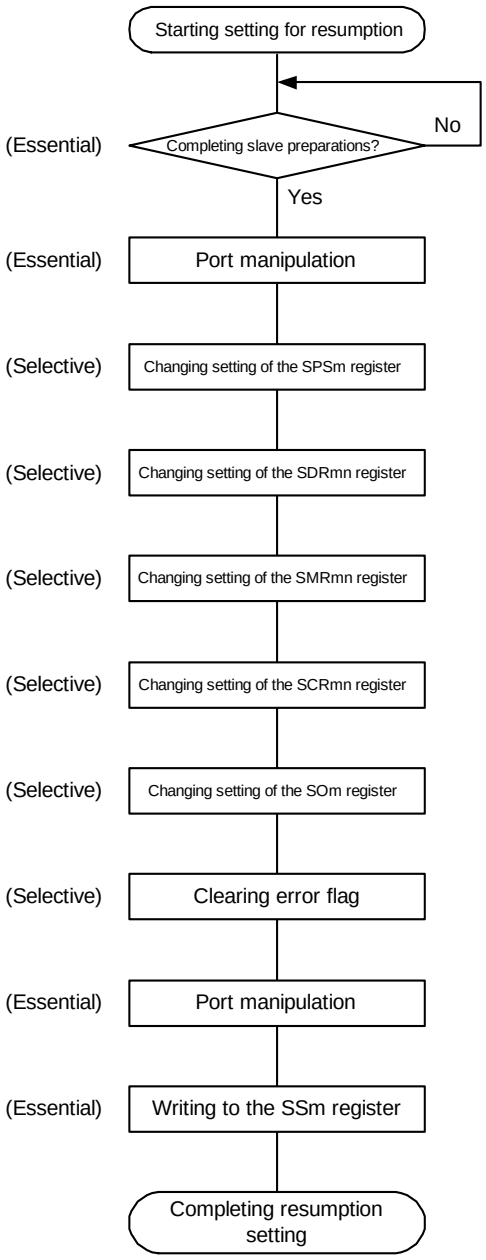


Figure 20 - 36 Procedure for Resuming Master Reception



Wait until stop the communication target (slave) or communication operation completed.

Disable clock output of the target channel by setting a port register and a port mode register.

Re-set the register to change the operation clock setting.

Re-set the register to change the transfer baud rate setting (setting the transfer clock by dividing the operation clock (f_{MCK})).

Re-set the register to change serial mode register mn (SMRmn) setting.

Re-set the register to change serial communication operation setting register mn (SCRmn) setting.

Set the initial output level of the serial clock (CKOmn).

If the OVF flag remains set, clear this using serial flag clear trigger register mn (SIRmn).

Enable clock output of the target channel by setting a port register and a port mode register.

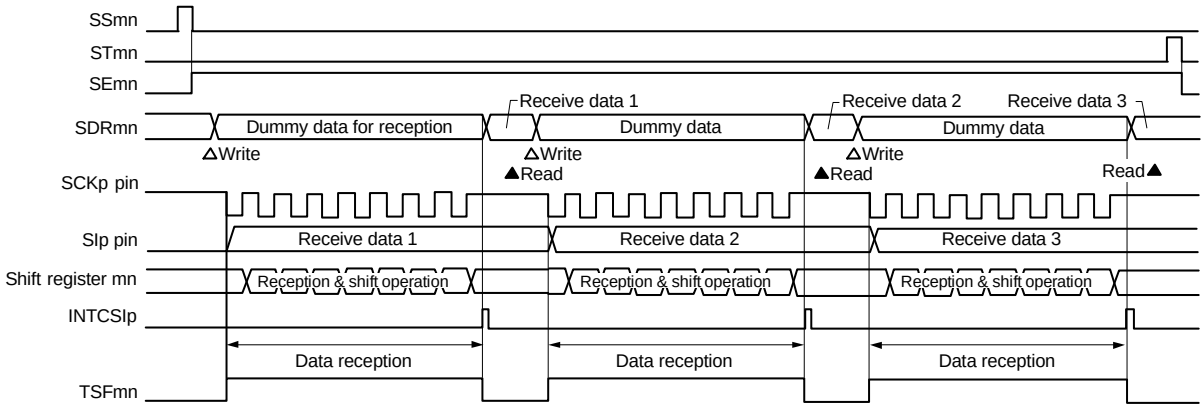
Set the SSmn bit of the target channel to 1 (SEmn bit = 1: to enable operation).

Setting is completed.
Sets dummy data to the SIOp register (bits 7 to 0 of the SDRmn register) and start communication.

Remark If PER0 is rewritten while stopping the master transmission and the clock supply is stopped, wait until the transmission target (slave) stops or transmission finishes, and then perform initialization instead of restarting the transmission.

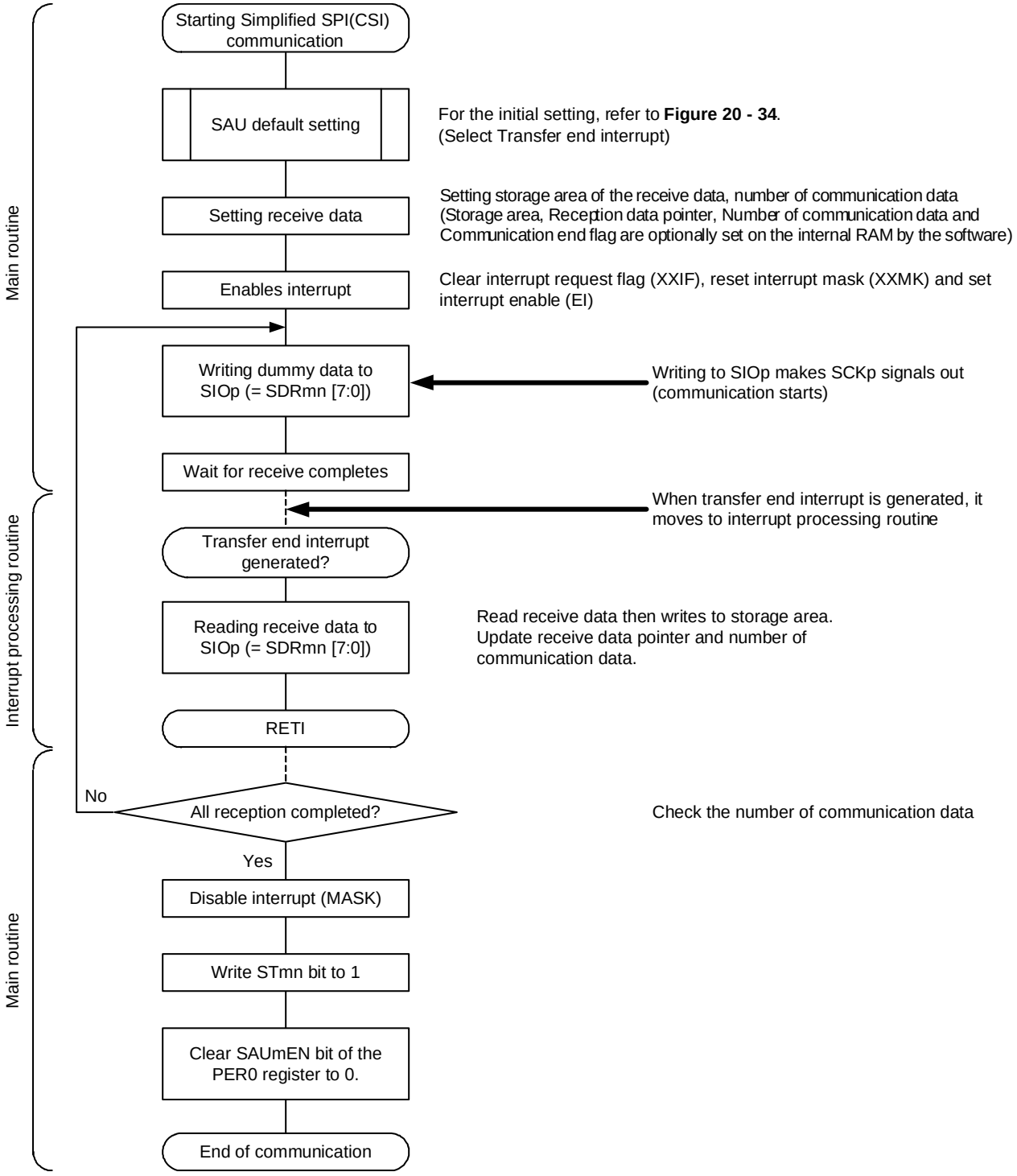
(3) Processing flow (in single-reception mode)

Figure 20 - 37 Timing Chart of Master Reception (in Single-Reception Mode) (Type 1: DAPmn = 0, CKPmn = 0)



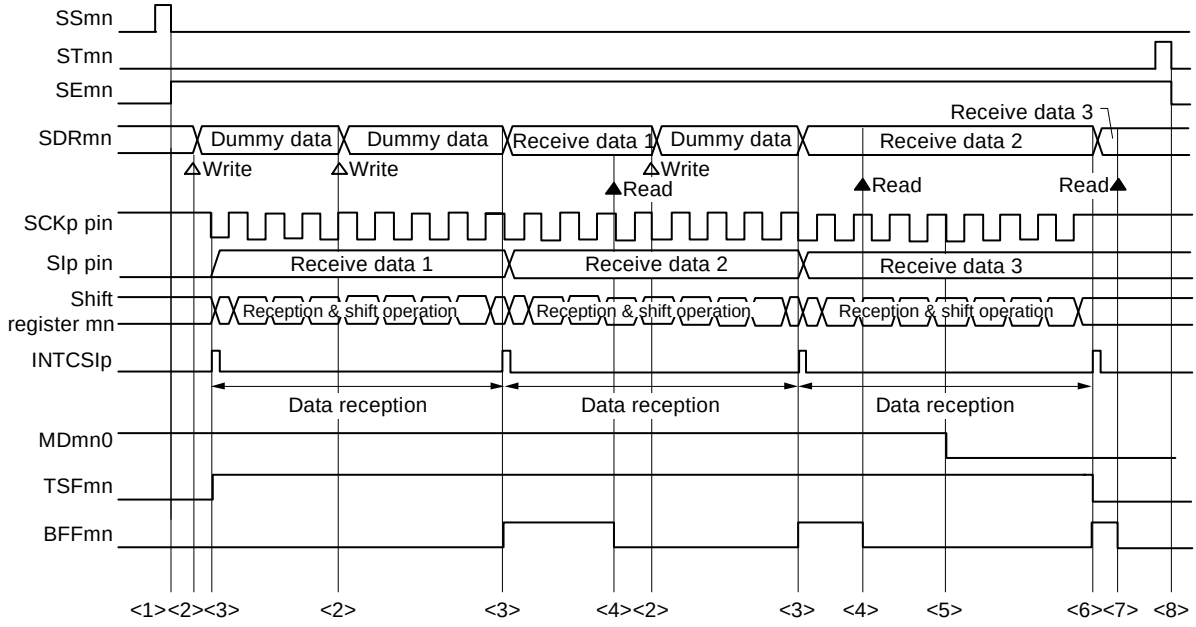
Remark m: Unit number (m = 0, 1), n: Channel number (n = 0, 2), p: CSI number (p = 00, 10, 20), mn = 00, 02, 10

Figure 20 - 38 Flowchart of Master Reception (in Single-Reception Mode)



(4) Processing flow (in continuous reception mode)

Figure 20 - 39 Timing Chart of Master Reception (in Continuous Reception Mode) (Type 1: DAPmn = 0, CKPmn = 0)

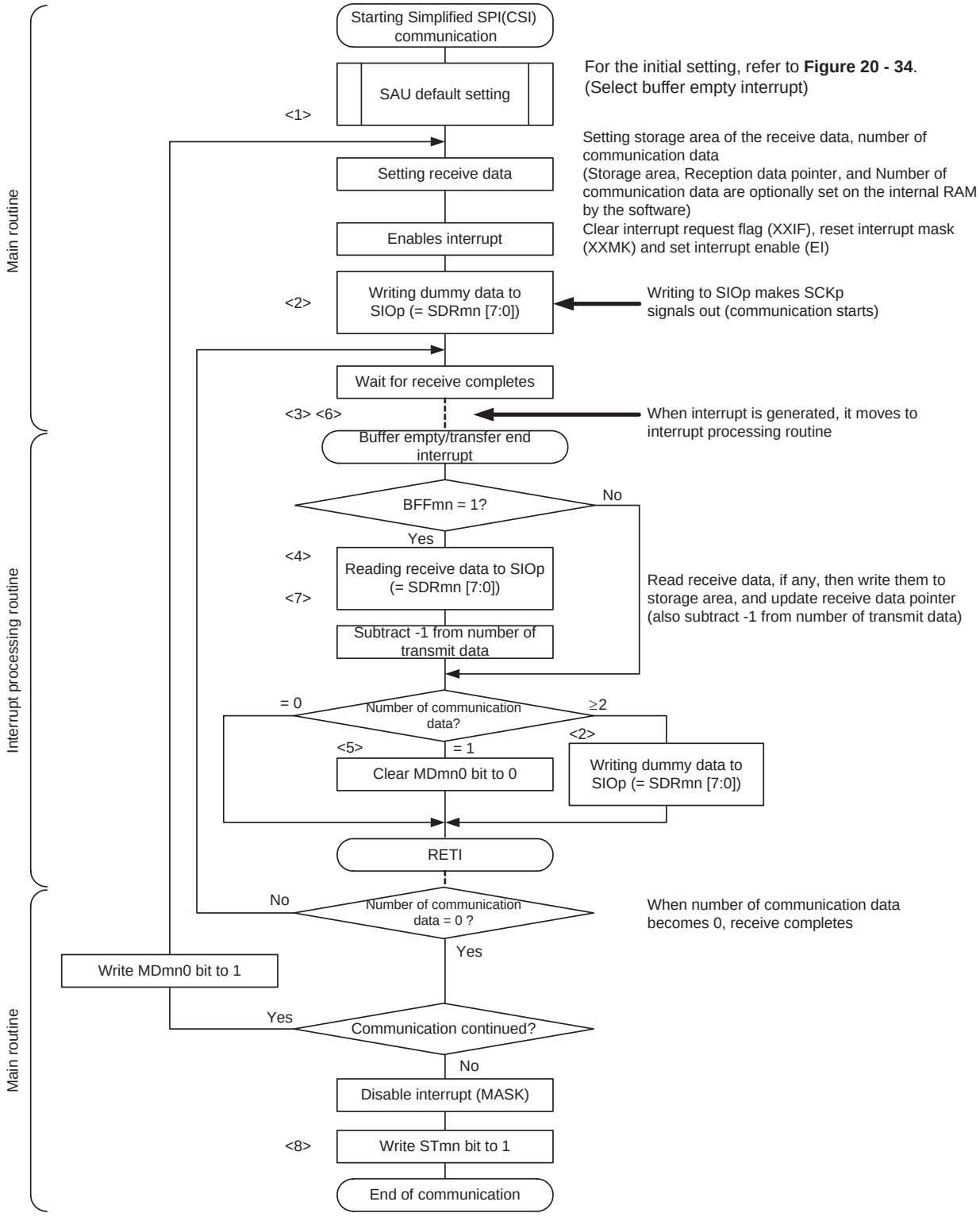


Caution The MDmn0 bit can be rewritten even during operation.
However, rewrite it before receive of the last bit is started, so that it has been rewritten before the transfer end interrupt of the last receive data.

Remark 1. <1> to <8> in the figure correspond to <1> to <8> in **Figure 20 - 40 Flowchart of Master Reception (in Continuous Reception Mode)**.

Remark 2. m: Unit number (m = 0, 1), n: Channel number (n = 0, 2), p: CSI number (p = 00, 10, 20), mn = 00, 02, 10

Figure 20 - 40 Flowchart of Master Reception (in Continuous Reception Mode)



Remark <1> to <8> in the figure correspond to <1> to <8> in **Figure 20 - 39 Timing Chart of Master Reception (in Continuous Reception Mode) (Type 1: DAPmn = 0, CKPmn = 0)**.

20.5.3 Master transmission/reception

Master transmission/reception is that the RL78 microcontroller outputs a transfer clock and transmits/receives data to/from other device.

Simplified SPI	CSI00	CSI10	CSI20
Target channel	Channel 0 of SAU0	Channel 2 of SAU0	Channel 0 of SAU1
Pins used	SCK00, SI00, SO00	SCK10, SI10, SO10	SCK20, SI20, SO20
Interrupt	INTCSI00	INTCSI10	INTCSI20
	Transfer end interrupt (in single-transfer mode) or buffer empty interrupt (in continuous transfer mode) can be selected.		
Error detection flag	Overrun error detection flag (OVFmn) only		
Transfer data length	7 or 8 bits		
Transfer rate Note	Max. $f_{CLK}/2$ [Hz] (CSI00 only), $f_{CLK}/4$ [Hz] Min. $f_{CLK}/(2 \times 2^{15} \times 128)$ [Hz] f_{CLK}: System clock frequency		
Data phase	Selectable by the DAPmn bit of the SCRmn register • DAPmn = 0: Data I/O starts at the start of the operation of the serial clock. • DAPmn = 1: Data I/O starts half a clock before the start of the serial clock operation.		
Clock phase	Selectable by the CKPmn bit of the SCRmn register • CKPmn = 0: Non-reverse • CKPmn = 1: Reverse		
Data direction	MSB or LSB first		

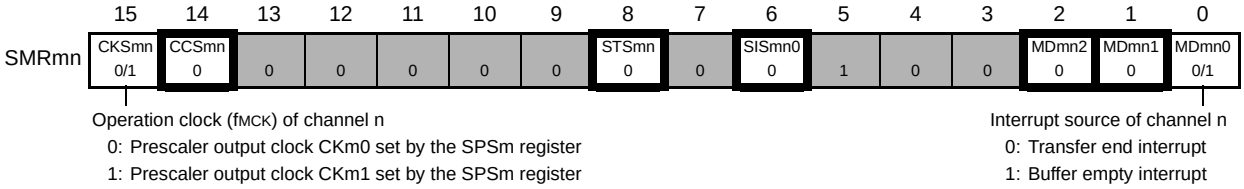
Note Use this operation within a range that satisfies the conditions above and the peripheral functions characteristics in the electrical specifications (see **CHAPTER 38** or **CHAPTER 39 ELECTRICAL SPECIFICATIONS**).

Remark m: Unit number (m = 0, 1), n: Channel number (n = 0, 2), p: CSIl number (p = 00, 10, 20), mn = 00, 02, 10

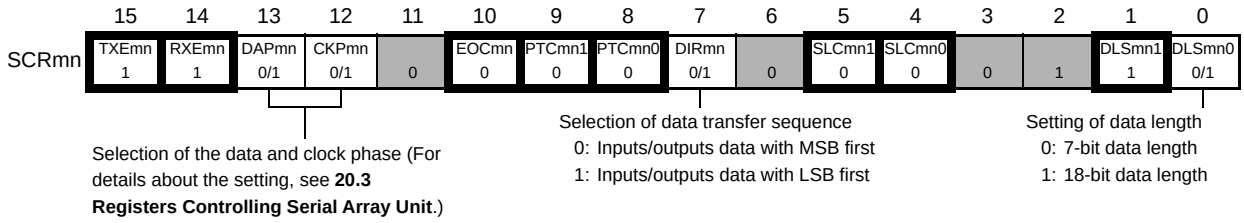
(1) Register setting

Figure 20 - 41 Example of Contents of Registers for Master Transmission/Reception of Simplified SPI (CSI00, CSI10, CSI20)

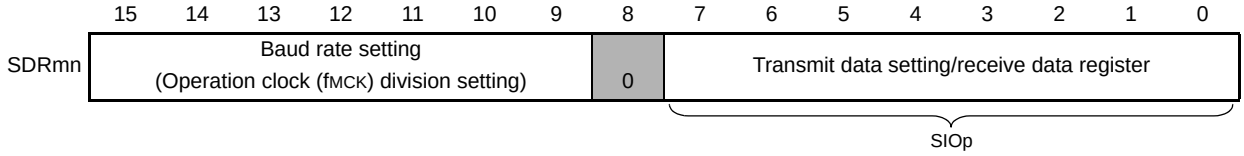
(a) Serial mode register mn (SMRmn)



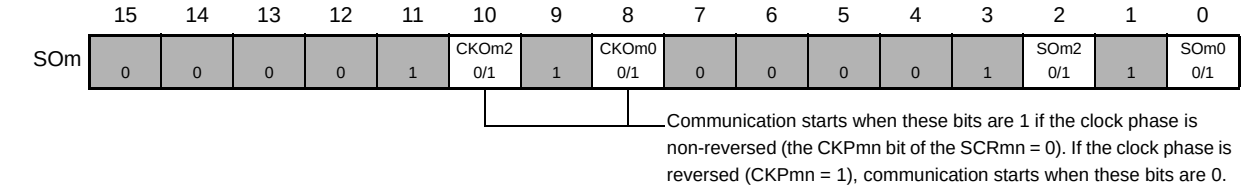
(b) Serial communication operation setting register mn (SCRmn)



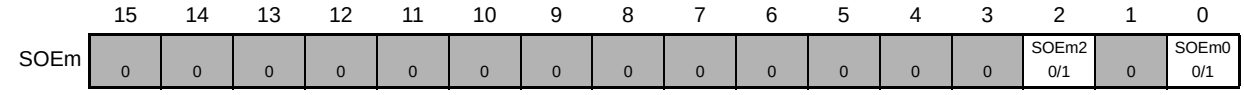
(c) Serial data register mn (SDRmn) (lower 8 bits: SIOp)



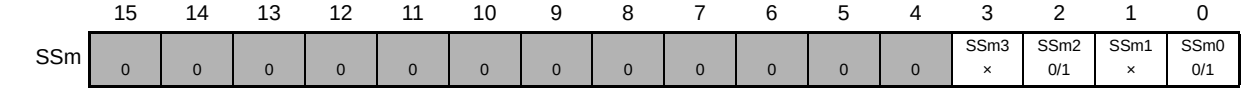
(d) Serial output register m (SOm)... Sets only the bits of the target channel.



(e) Serial output enable register m (SOEm)... Sets only the bits of the target channel to 1.



(f) Serial channel start register m (SSm)... Sets only the bits of the target channel to 1.



Remark 1. m: Unit number (m = 0, 1), n: Channel number (n = 0, 2), p: CSI number (p = 00, 10, 20), mn = 00, 02, 10

Remark 2. : Setting is fixed in the Simplified SPI(CSI) master transmission/reception mode,

: Setting disabled (set to the initial value)

×: Bit that cannot be used in this mode (set to the initial value when not used in any mode)

0/1: Set to 0 or 1 depending on the usage of the user

(2) Operation procedure

Figure 20 - 42 Initial Setting Procedure for Master Transmission/Reception

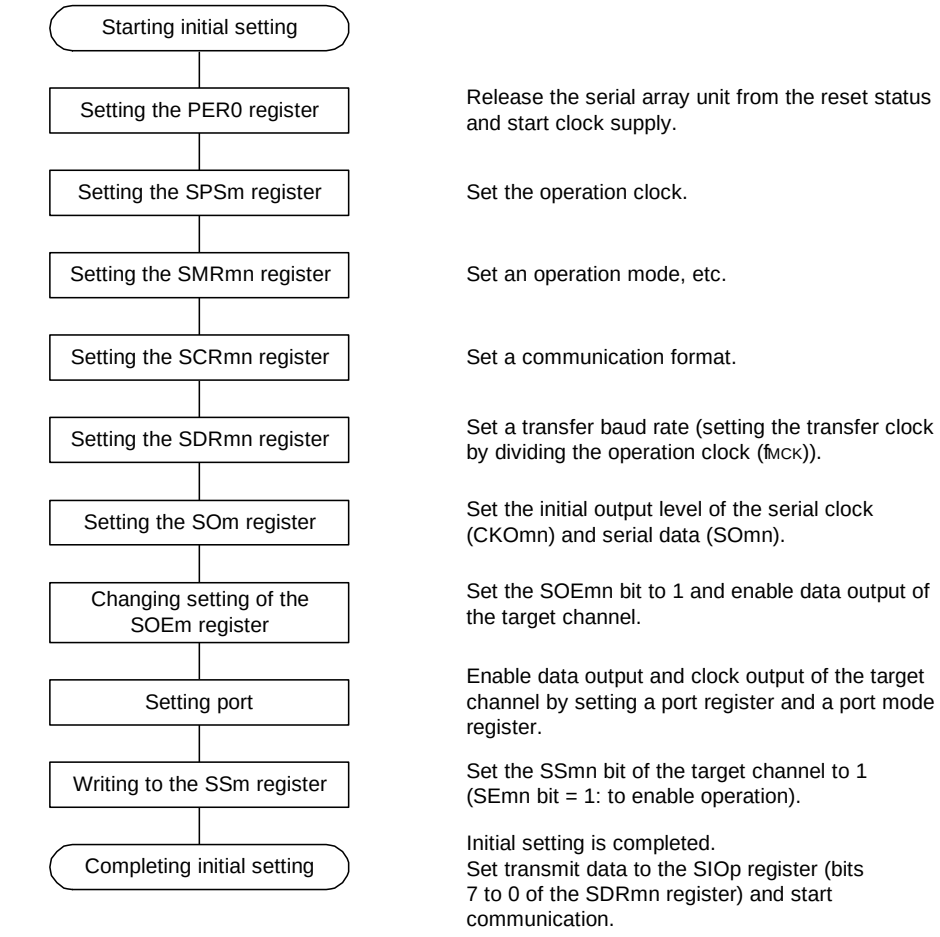


Figure 20 - 43 Procedure for Stopping Master Transmission/Reception

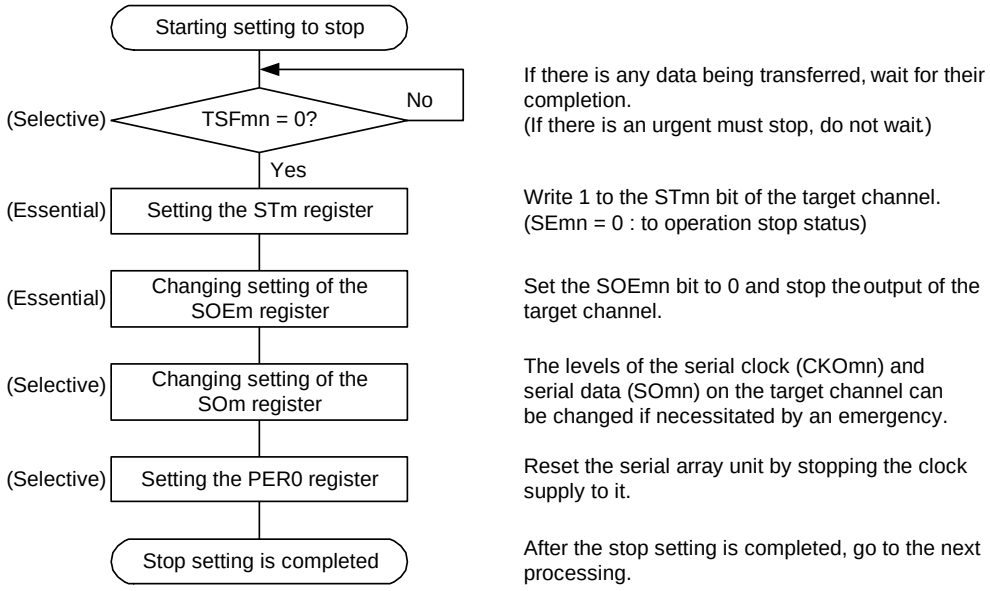
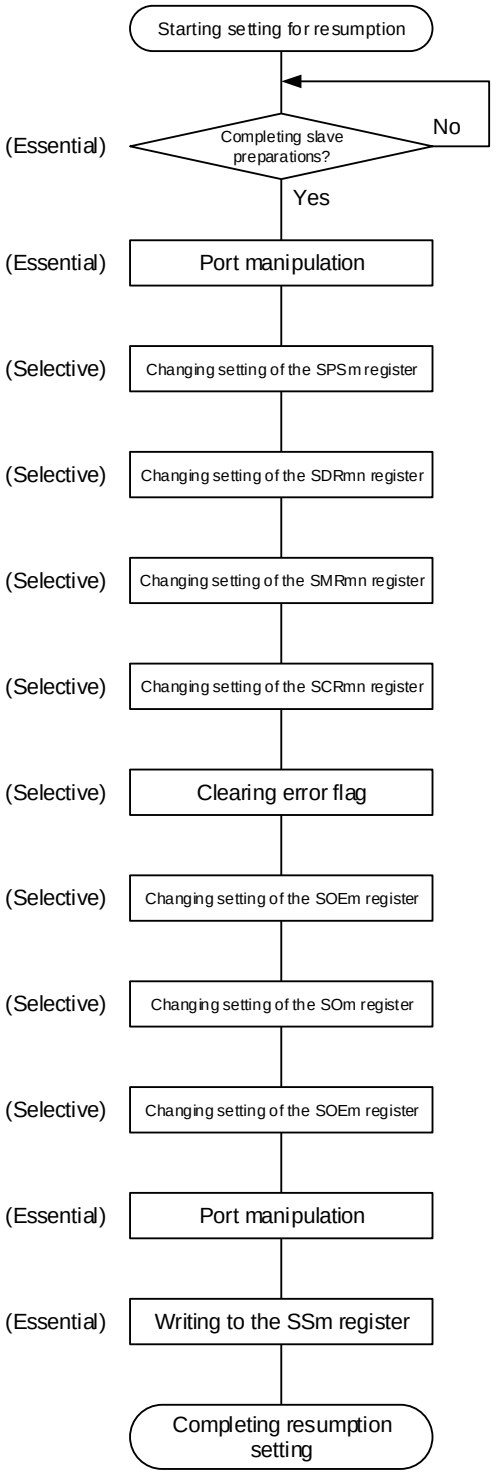


Figure 20 - 44 Procedure for Resuming Master Transmission/Reception



Wait until stop the communication target (slave) or communication operation completed.

Disable data output and clock output of the target channel by setting a port register and a port mode register.

Re-set the register to change the operation clock setting.

Re-set the register to change the transfer baud rate setting (setting the transfer clock by dividing the operation clock (f_{MCK})).

Re-set the register to change serial mode register mn (SMRmn) setting.

Re-set the register to change serial communication operation setting register mn (SCRmn) setting.

If the OVF flag remains set, clear this using serial flag clear trigger register mn (SIRmn).

Set the SOEmn bit to 0 to stop output from the target channel.

Set the initial output level of the serial clock (CKOmn) and serial data (SOmn).

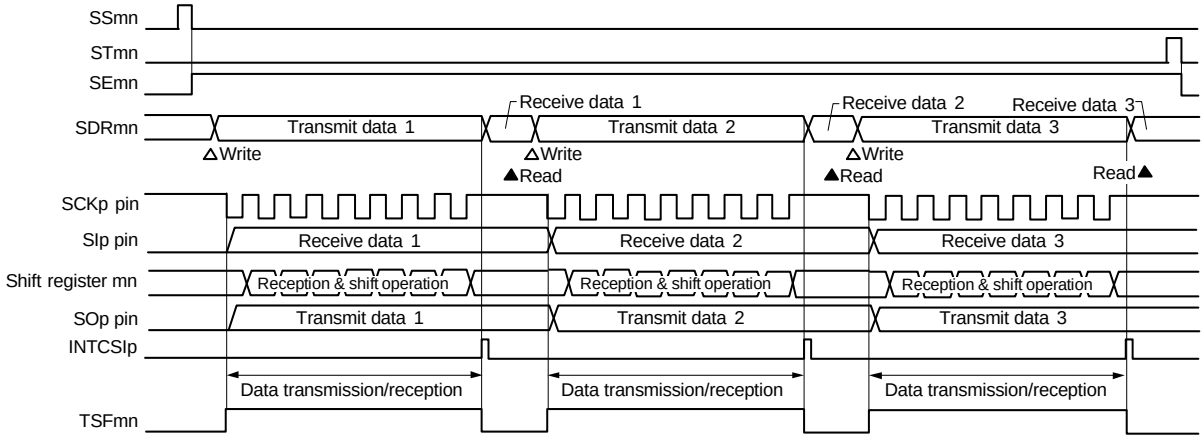
Set the SOEmn bit to 1 and enable output from the target channel.

Enable data output and clock output of the target channel by setting a port register and a port mode register.

Set the SSmn bit of the target channel to 1 and set the SEmn bit to 1 (to enable operation).

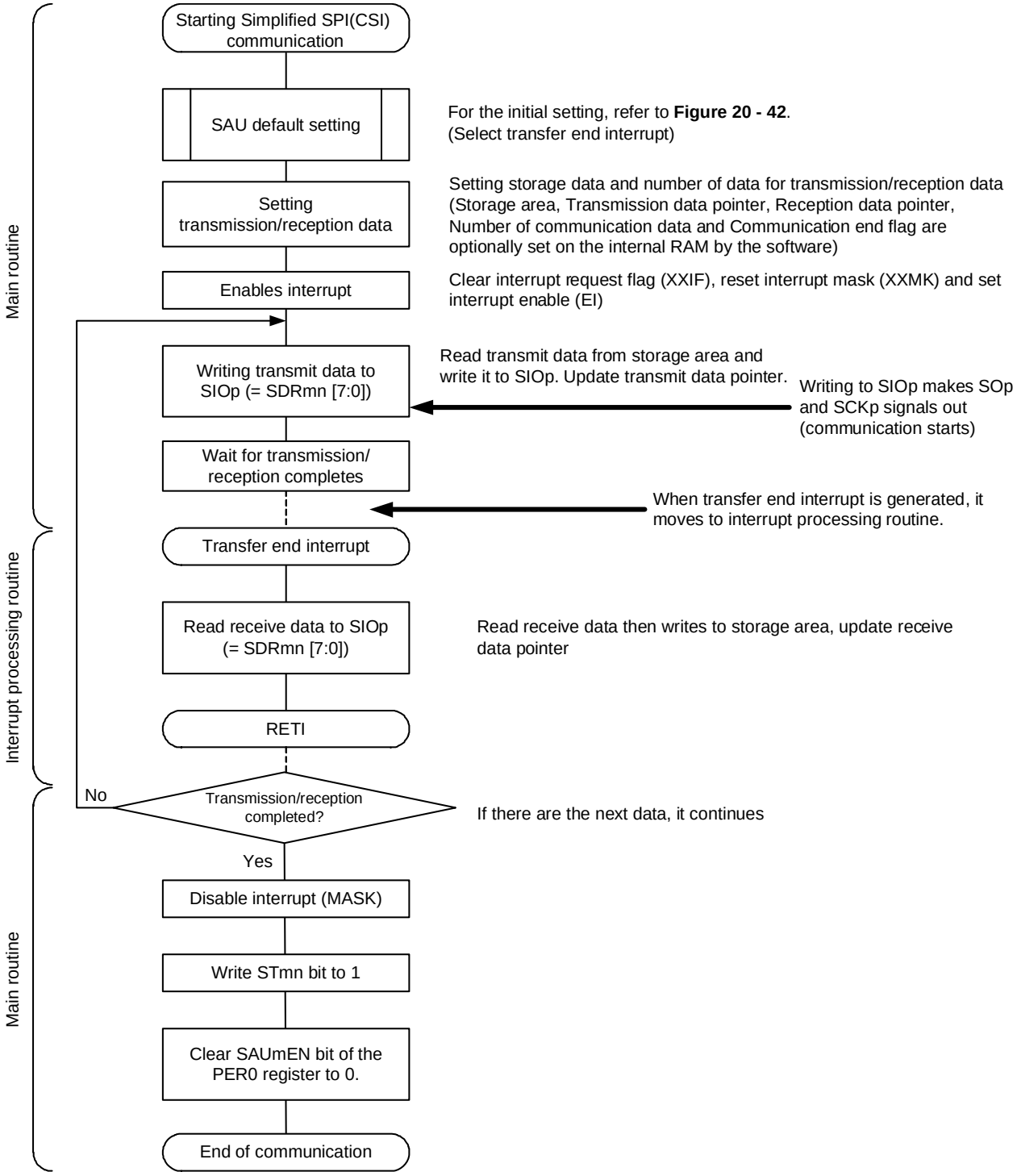
(3) Processing flow (in single-transmission/reception mode)

Figure 20 - 45 Timing Chart of Master Transmission/Reception (in Single-Transmission/Reception Mode) (Type 1: DAPmn = 0, CKPmn = 0)



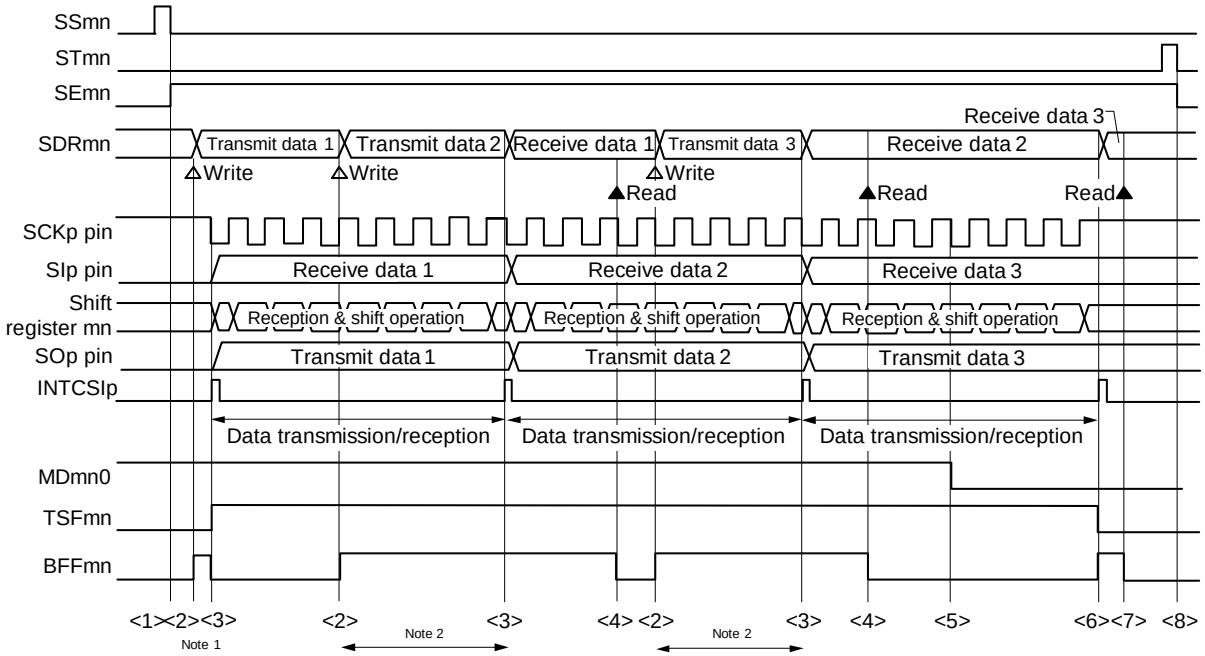
Remark m: Unit number (m = 0, 1), n: Channel number (n = 0, 2), p: CSI number (p = 00, 10, 20), mn = 00, 02, 10

Figure 20 - 46 Flowchart of Master Transmission/Reception (in Single- Transmission/Reception Mode)



(4) Processing flow (in continuous transmission/reception mode)

Figure 20 - 47 Timing Chart of Master Transmission/Reception (in Continuous Transmission/Reception Mode) (Type 1: DAPmn = 0, CKPmn = 0)



Note 1. If transmit data is written to the SDRmn register while the BFFmn bit of serial status register mn (SSRmn) is 1 (valid data is stored in serial data register mn (SDRmn)), the transmit data is overwritten.

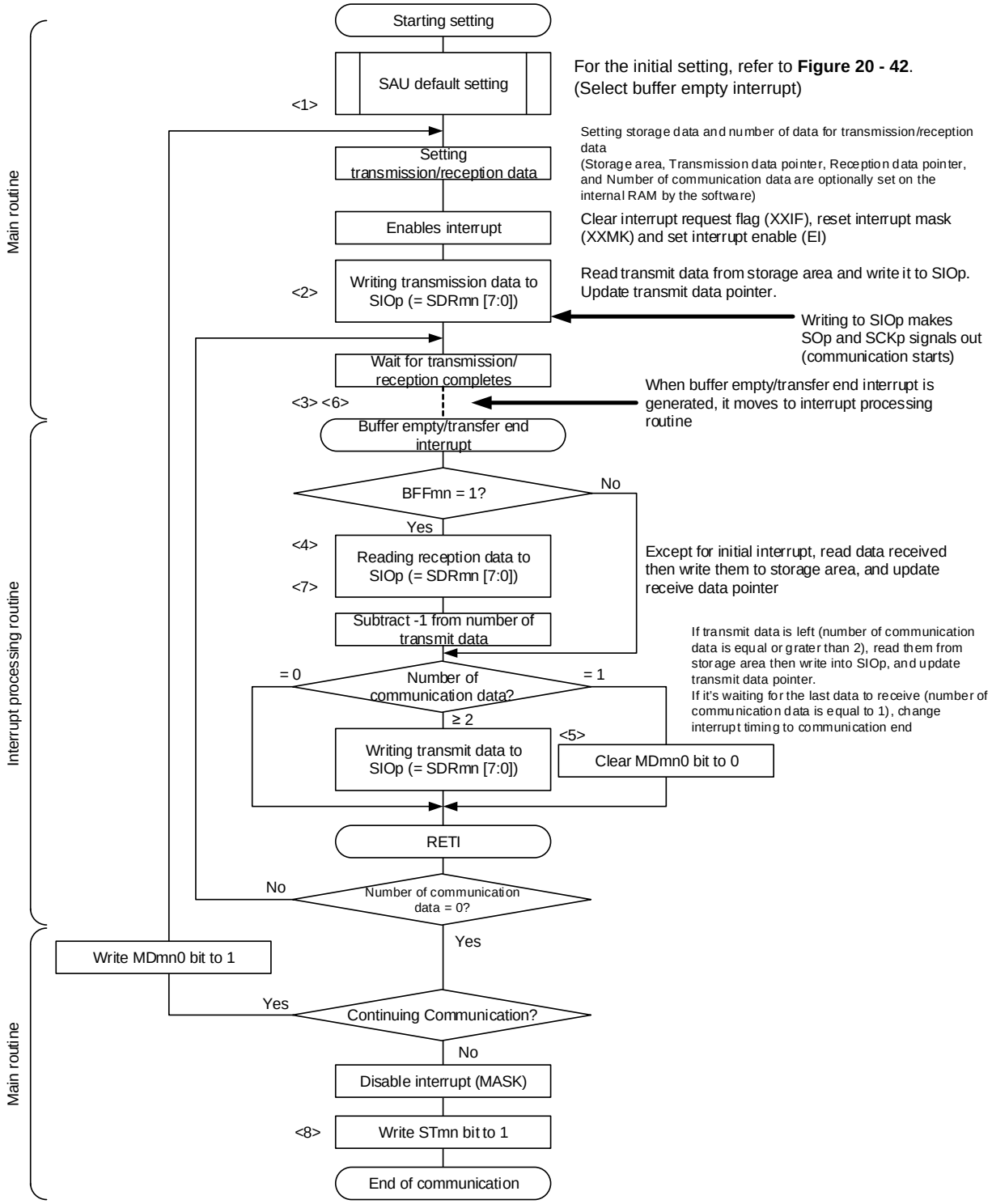
Note 2. The transmit data can be read by reading the SDRmn register during this period. At this time, the transfer operation is not affected.

Caution The MDmn0 bit of serial mode register mn (SMRmn) can be rewritten even during operation. However, rewrite it before transfer of the last bit is started, so that it has been rewritten before the transfer end interrupt of the last transmit data.

Remark 1. <1> to <8> in the figure correspond to <1> to <8> in **Figure 20 - 48 Flowchart of Master Transmission/Reception (in Continuous Transmission/Reception Mode)**.

Remark 2. m: Unit number (m = 0, 1), n: Channel number (n = 0, 2), p: CSI number (p = 00, 10, 20), mn = 00, 02, 10

Figure 20 - 48 Flowchart of Master Transmission/Reception (in Continuous Transmission/Reception Mode)



Remark <1> to <8> in the figure correspond to <1> to <8> in **Figure 20 - 47 Timing Chart of Master Transmission/Reception (in Continuous Transmission/Reception Mode) (Type 1: DAPmn = 0, CKPmn = 0)**.

20.5.4 Slave transmission

Slave transmission is that the RL78 microcontroller transmits data to another device in the state of a transfer clock being input from another device.

Simplified SPI	CSI00	CSI10	CSI20
Target channel	Channel 0 of SAU0	Channel 2 of SAU0	Channel 0 of SAU1
Pins used	SCK00, SO00	SCK10, SO10	SCK20, SO20
Interrupt	INTCSI00	INTCSI10	INTCSI20
	Transfer end interrupt (in single-transfer mode) or buffer empty interrupt (in continuous transfer mode) can be selected.		
Error detection flag	Overrun error detection flag (OVFmn) only		
Transfer data length	7 or 8 bits		
Transfer rate	Max. f_{MCK}/6 [Hz] Notes 1, 2.		
Data phase	Selectable by the DAPmn bit of the SCRmn register • DAPmn = 0: Data output starts from the start of the operation of the serial clock. • DAPmn = 1: Data output starts half a clock before the start of the serial clock operation.		
Clock phase	Selectable by the CKPmn bit of the SCRmn register • CKPmn = 0: Non-reverse • CKPmn = 1: Reverse		
Data direction	MSB or LSB first		

Note 1. Because the external serial clock input to the SCK00, SCK10, and SCK20 pins is sampled internally and used, the fastest transfer rate is f_{MCK}/6 [Hz].

Note 2. Use this operation within a range that satisfies the conditions above and the peripheral functions characteristics in the electrical specifications (see **CHAPTER 38** or **CHAPTER 39 ELECTRICAL SPECIFICATIONS**).

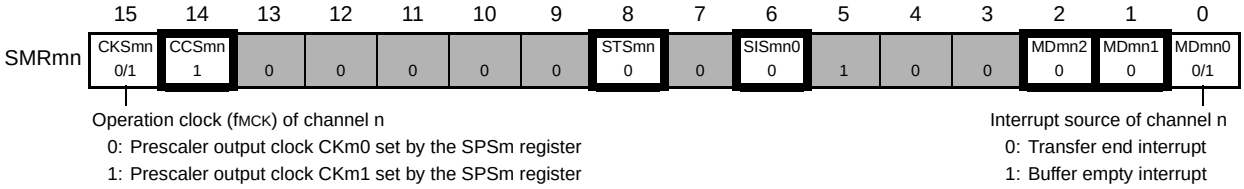
Remark 1. f_{MCK}: Operation clock frequency of target channel
f_{SCK}: Serial clock frequency

Remark 2. m: Unit number (m = 0, 1), n: Channel number (n = 0, 2), mn = 00, 02, 10

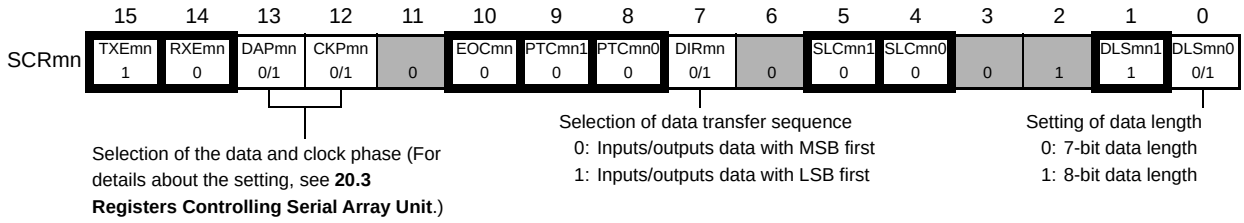
(1) Register setting

Figure 20 - 49 Example of Contents of Registers for Slave Transmission of Simplified SPI (CSI00, CSI10, CSI20)

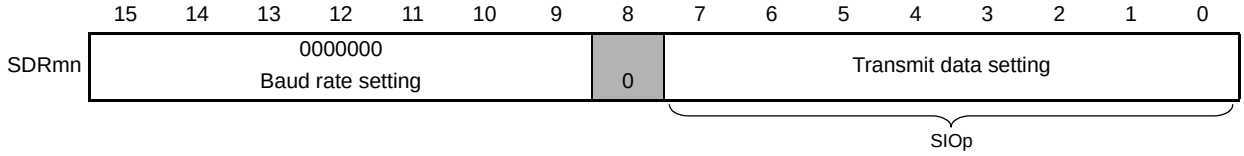
(a) Serial mode register mn (SMRmn)



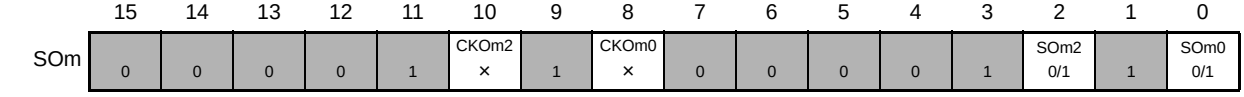
(b) Serial communication operation setting register mn (SCRmn)



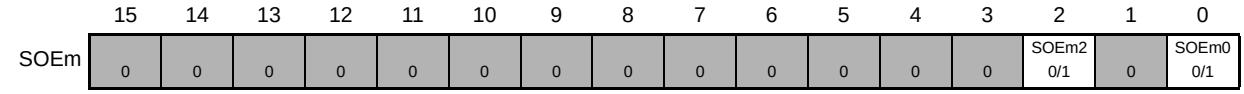
(c) Serial data register mn (SDRmn) (lower 8 bits: SIOp)



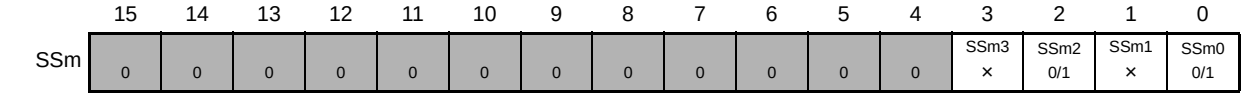
(d) Serial output register m (SOm)... Sets only the bits of the target channel.



(e) Serial output enable register m (SOEm)... Sets only the bits of the target channel to 1.



(f) Serial channel start register m (SSm)... Sets only the bits of the target channel to 1.



Remark 1. mm: Unit number (m = 0, 1), n: Channel number (n = 0, 2), p: CSI number (p = 00, 10, 20), mn = 00, 02, 10

Remark 2. ■: Setting is fixed in the Simplified SPI(CSI) slave transmission mode,
■: Setting disabled (set to the initial value)
×: Bit that cannot be used in this mode (set to the initial value when not used in any mode)
0/1: Set to 0 or 1 depending on the usage of the user

(2) Operation procedure

Figure 20 - 50 Initial Setting Procedure for Slave Transmission

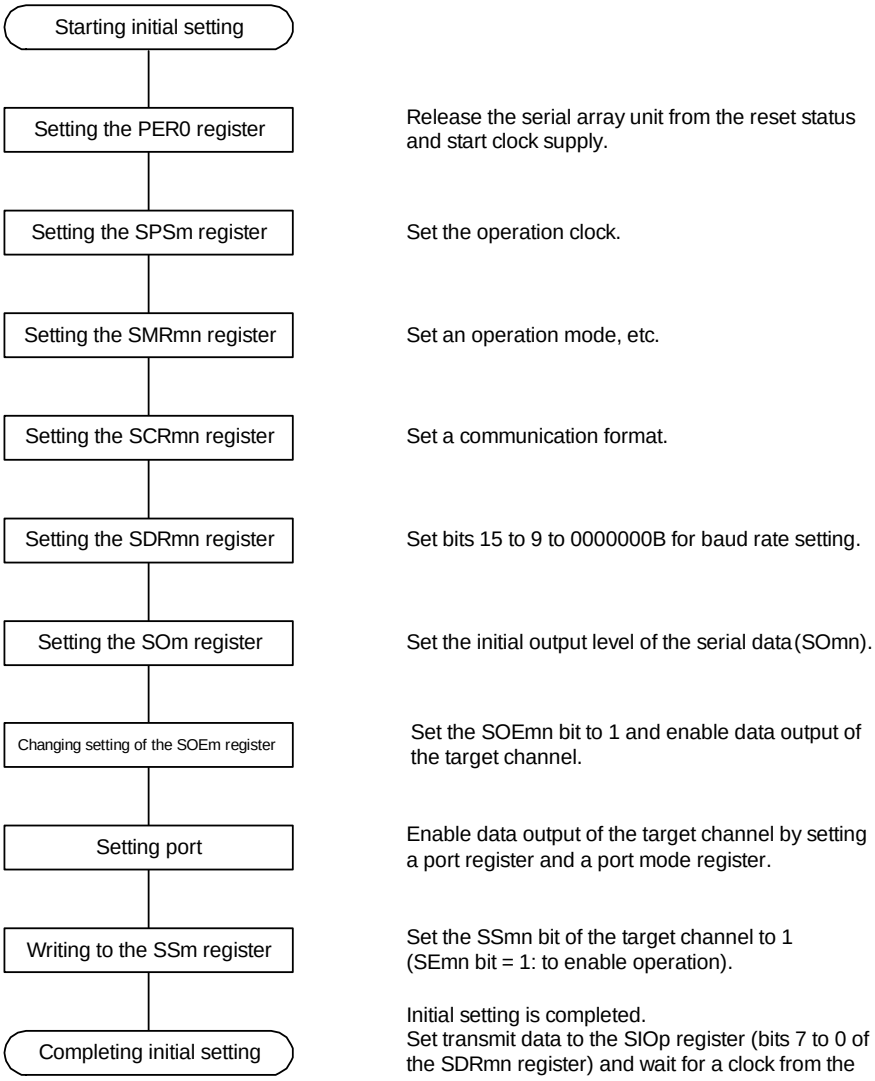


Figure 20 - 51 Procedure for Stopping Slave Transmission

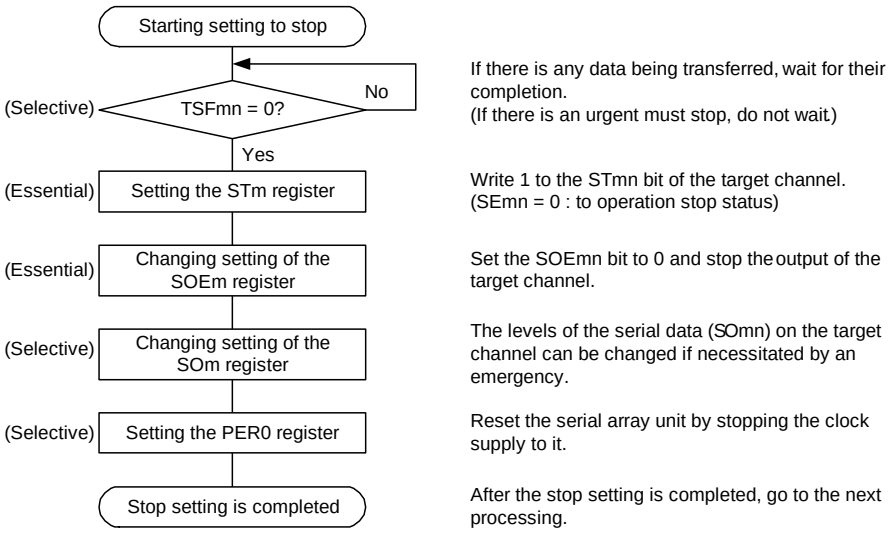
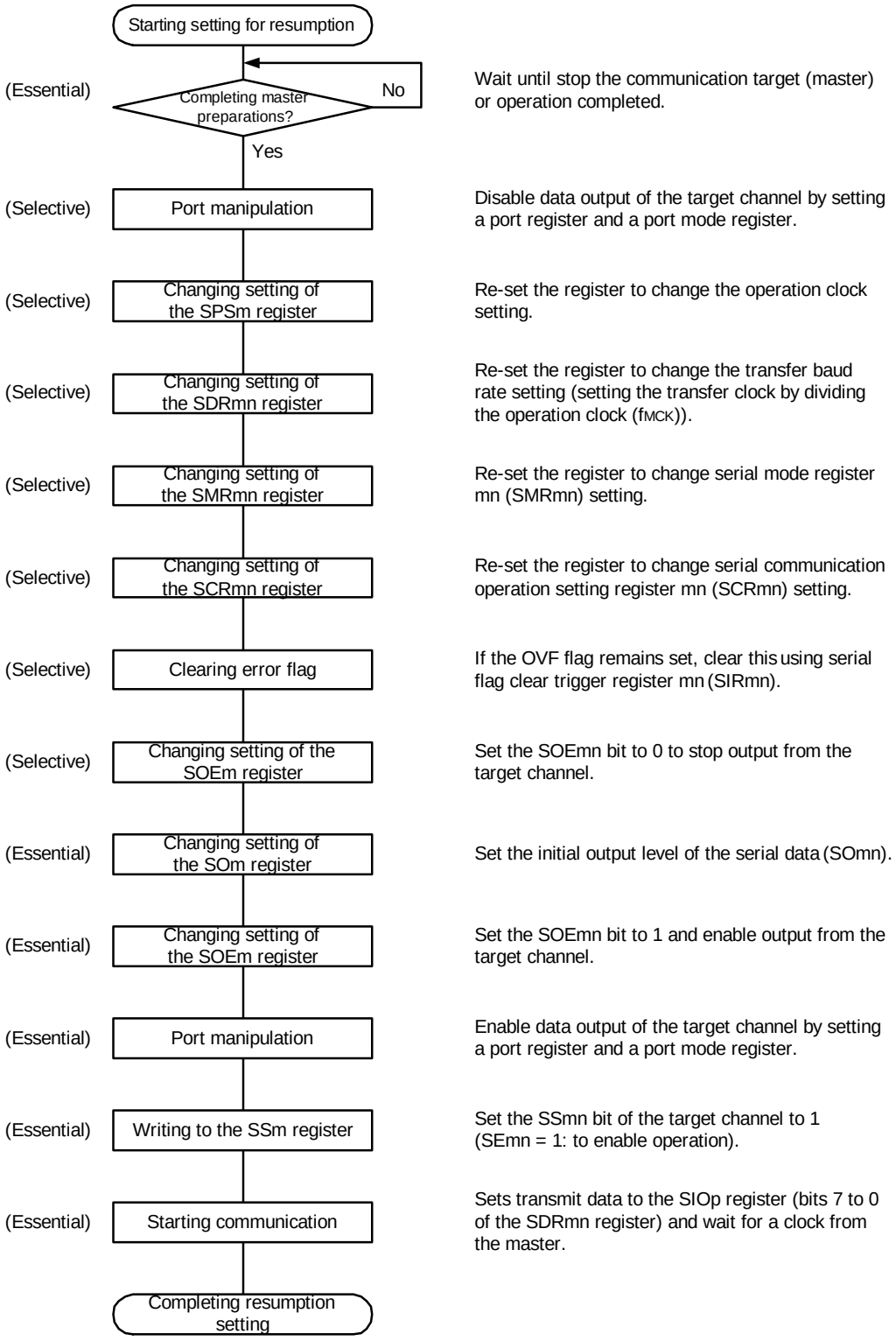


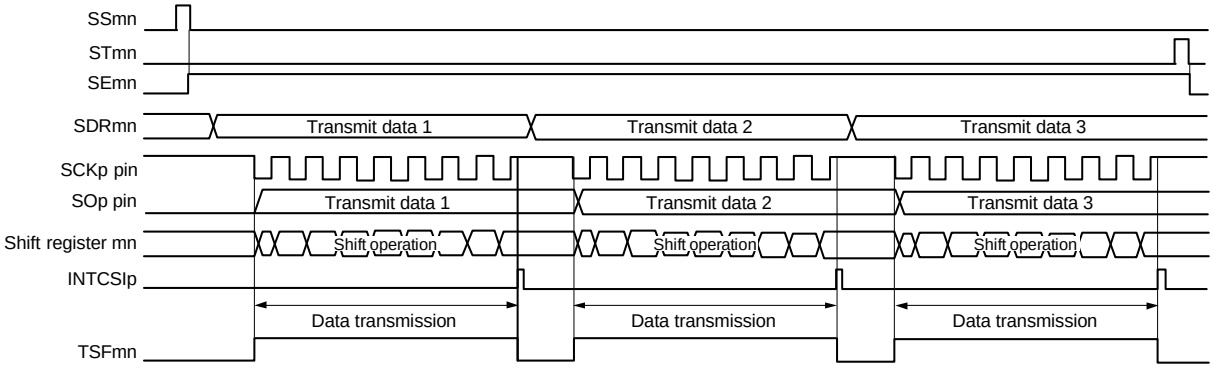
Figure 20 - 52 Procedure for Resuming Slave Transmission



Remark If PER0 is rewritten while stopping the master transmission and the clock supply is stopped, wait until the transmission target (master) stops or transmission finishes, and then perform initialization instead of restarting the transmission.

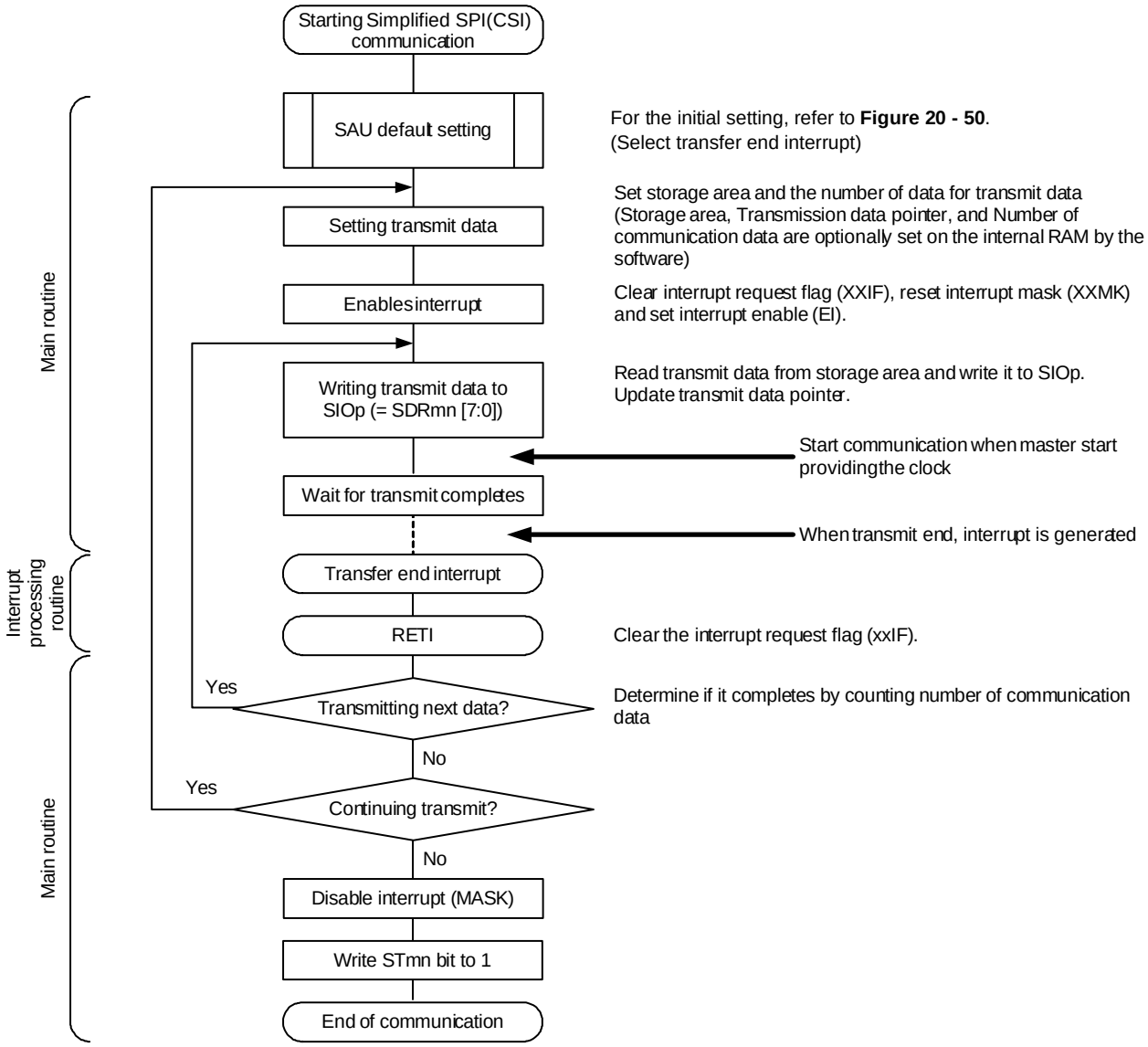
(3) Processing flow (in single-transmission mode)

Figure 20 - 53 Timing Chart of Slave Transmission (in Single-Transmission Mode)
(Type 1: DAPmn = 0, CKPmn = 0)



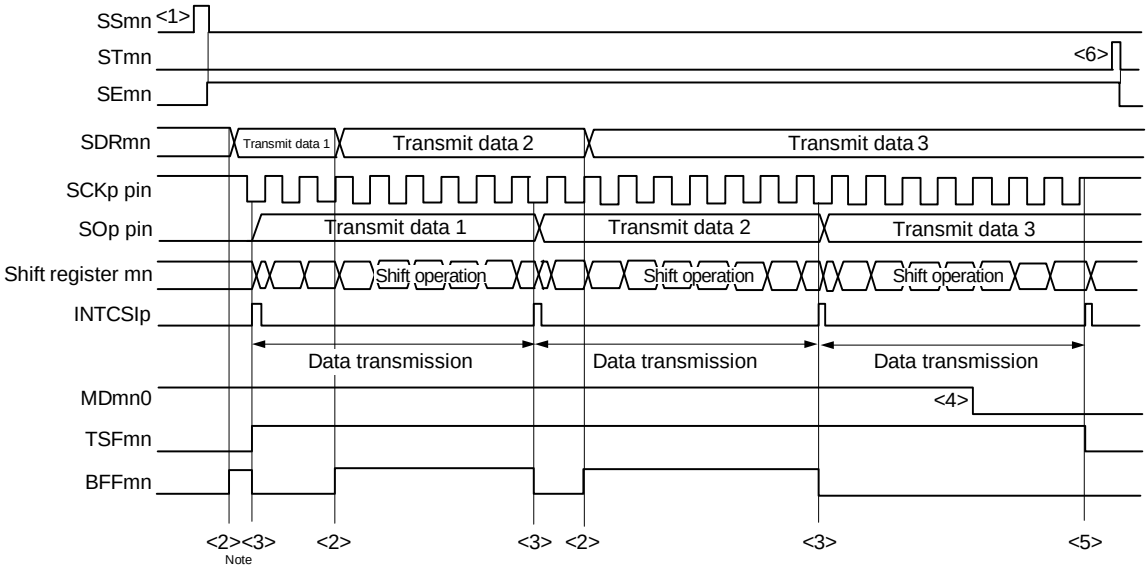
Remark m: Unit number (m = 0, 1), n: Channel number (n = 0, 2), p: CSI number (p = 00, 10, 20), mn = 00, 02, 10

Figure 20 - 54 Flowchart of Slave Transmission (in Single-Transmission Mode)



(4) Processing flow (in continuous transmission mode)

Figure 20 - 55 Timing Chart of Slave Transmission (in Continuous Transmission Mode)
(Type 1: DAPmn = 0, CKPmn = 0)

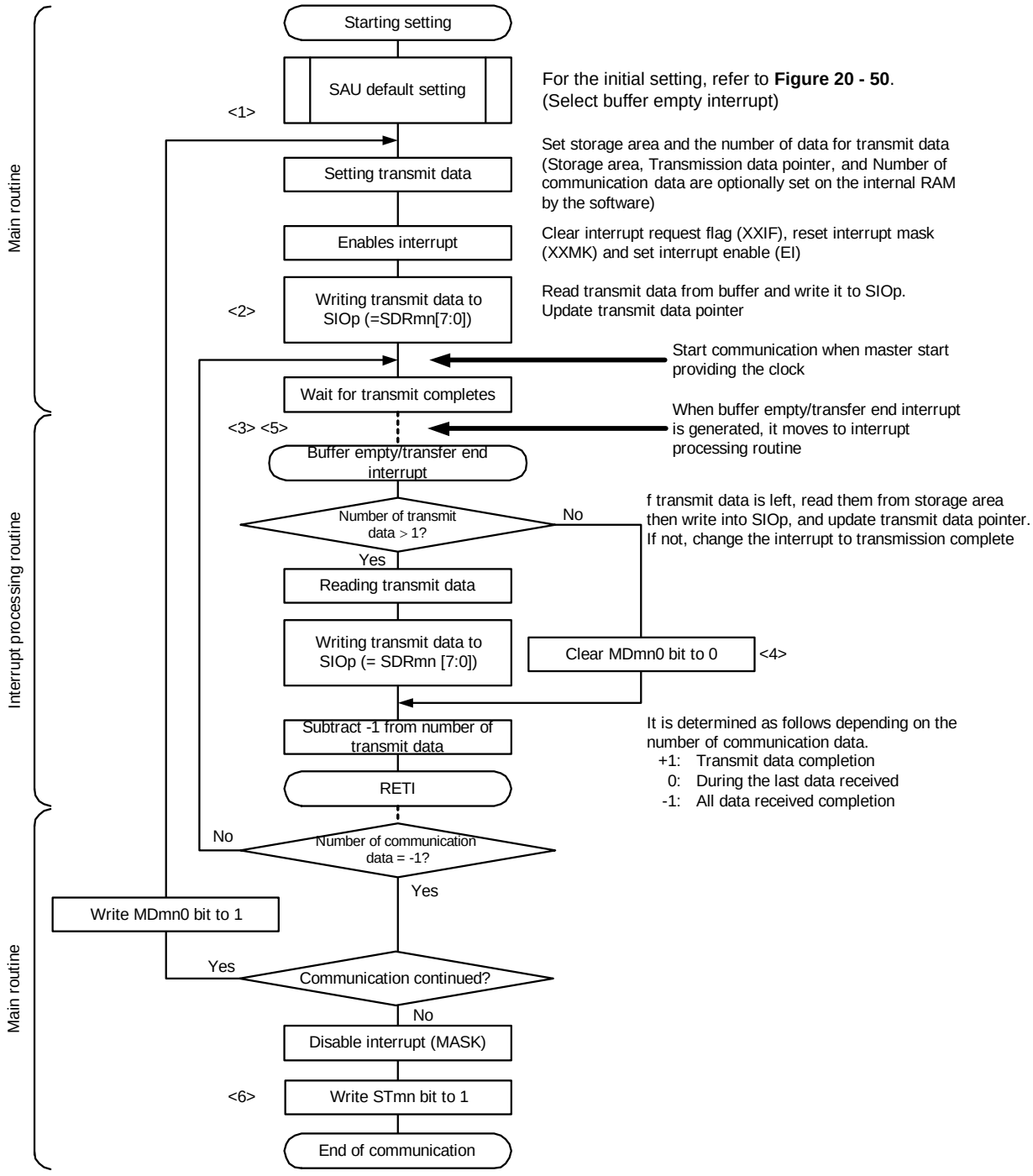


Note If transmit data is written to the SDRmn register while the BFFmn bit of serial status register mn (SSRmn) is 1 (valid data is stored in serial data register mn (SDRmn)), the transmit data is overwritten.

Caution **The MDmn0 bit of serial mode register mn (SMRmn) can be rewritten even during operation. However, rewrite it before transfer of the last bit is started.**

Remark m: Unit number (m = 0, 1), n: Channel number (n = 0, 2), p: CSI number (p = 00, 10, 20), mn = 00, 02, 10

Figure 20 - 56 Flowchart of Slave Transmission (in Continuous Transmission Mode)



Remark <1> to <6> in the figure correspond to <1> to <6> in **Figure 20 - 55 Timing Chart of Slave Transmission (in Continuous Transmission Mode)**.

20.5.5 Slave reception

Slave reception is that the RL78 microcontroller receives data from another device in the state of a transfer clock being input from another device.

Simplified SPI	CSI00	CSI10	CSI20
Target channel	Channel 0 of SAU0	Channel 2 of SAU0	Channel 0 of SAU1
Pins used	SCK00, SI00	SCK10, SI10	SCK20, SI20
Interrupt	INTCSI00	INTCSI10	INTCSI20
	Transfer end interrupt only (Setting the buffer empty interrupt is prohibited.)		
Error detection flag	Overrun error detection flag (OVFmn) only		
Transfer data length	7 or 8 bits		
Transfer rate	Max. f_{MCK}/6 [Hz] Notes 1, 2		
Data phase	Selectable by the DAPmn bit of the SCRmn register • DAPmn = 0: Data input starts from the start of the operation of the serial clock. • DAPmn = 1: Data input starts half a clock before the start of the serial clock operation.		
Clock phase	Selectable by the CKPmn bit of the SCRmn register • CKPmn = 0: Non-reverse • CKPmn = 1: Reverse		
Data direction	MSB or LSB first		

Note 1. Because the external serial clock input to the SCK00 and SCK10 pins is sampled internally and used, the fastest transfer rate is f_{MCK}/6 [Hz].

Note 2. Use this operation within a range that satisfies the conditions above and the peripheral functions characteristics in the electrical specifications (see **CHAPTER 38** or **CHAPTER 39 ELECTRICAL SPECIFICATIONS**).

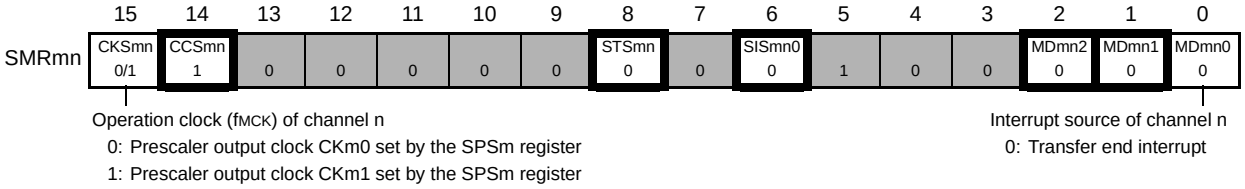
Remark 1. f_{MCK}: Operation clock frequency of target channel
f_{SCK}: Serial clock frequency

Remark 2. m: Unit number (m = 0, 1), n: Channel number (n = 0, 2), mn = 00, 02, 10

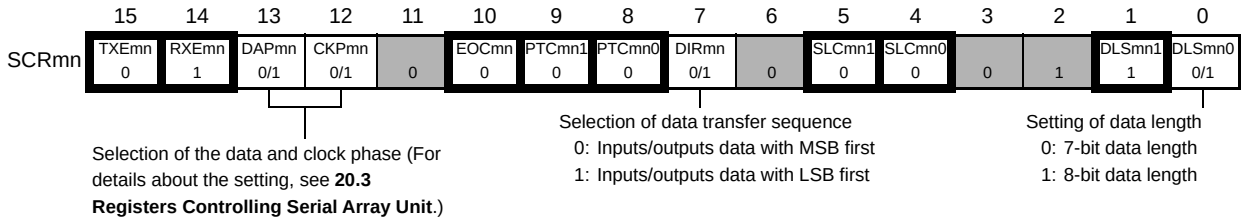
(1) Register setting

Figure 20 - 57 Example of Contents of Registers for Slave Reception of Simplified SPI (CSI00, CSI10, CSI20)

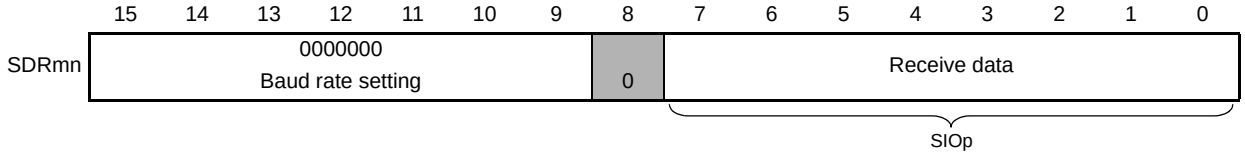
(a) Serial mode register mn (SMRmn)



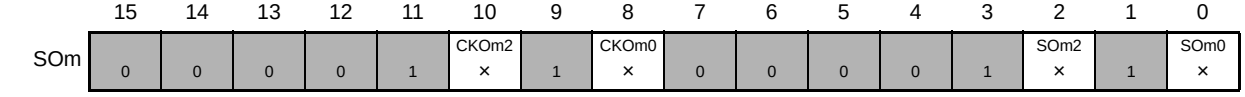
(b) Serial communication operation setting register mn (SCRmn)



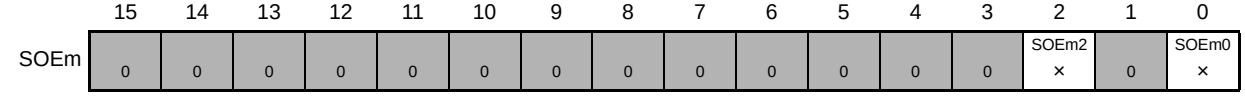
(c) Serial data register mn (SDRmn) (lower 8 bits: SIOp)



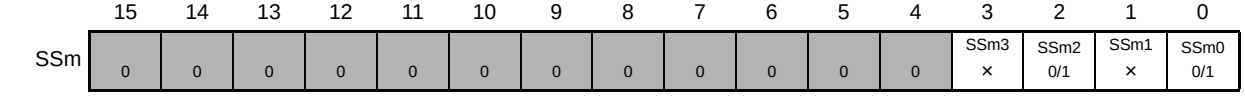
(d) Serial output register m (SOm)... The Register that not used in this mode.



(e) Serial output enable register m (SOEm)... The Register that not used in this mode.



(f) Serial channel start register m (SSm)... Sets only the bits of the target channel to 1.



Remark 1. m: Unit number (m = 0, 1), n: Channel number (n = 0, 2), p: CSI number (p = 00, 10, 20), mn = 00, 02, 10

Remark 2. ■: Setting is fixed in the Simplified SPI(CSI) slave reception mode,
■: Setting disabled (set to the initial value)
×: Bit that cannot be used in this mode (set to the initial value when not used in any mode)
0/1: Set to 0 or 1 depending on the usage of the user

(2) Operation procedure

Figure 20 - 58 Initial Setting Procedure for Slave Reception

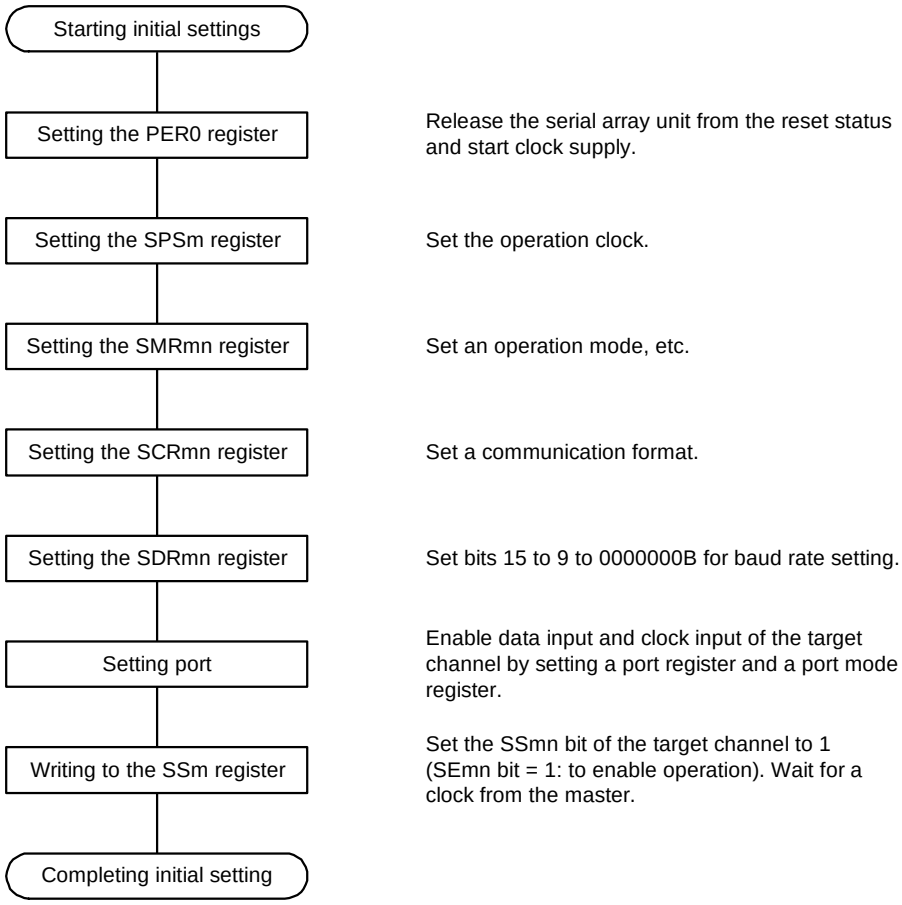


Figure 20 - 59 Procedure for Stopping Slave Reception

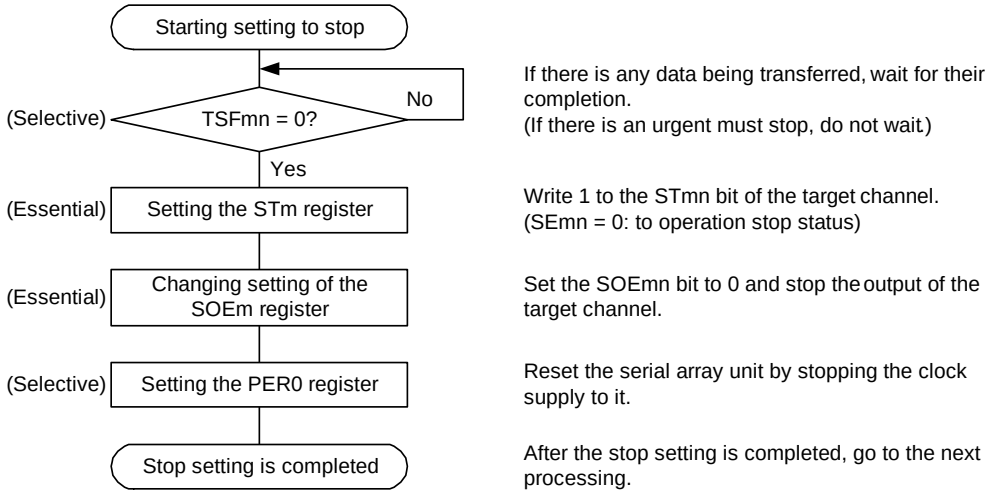
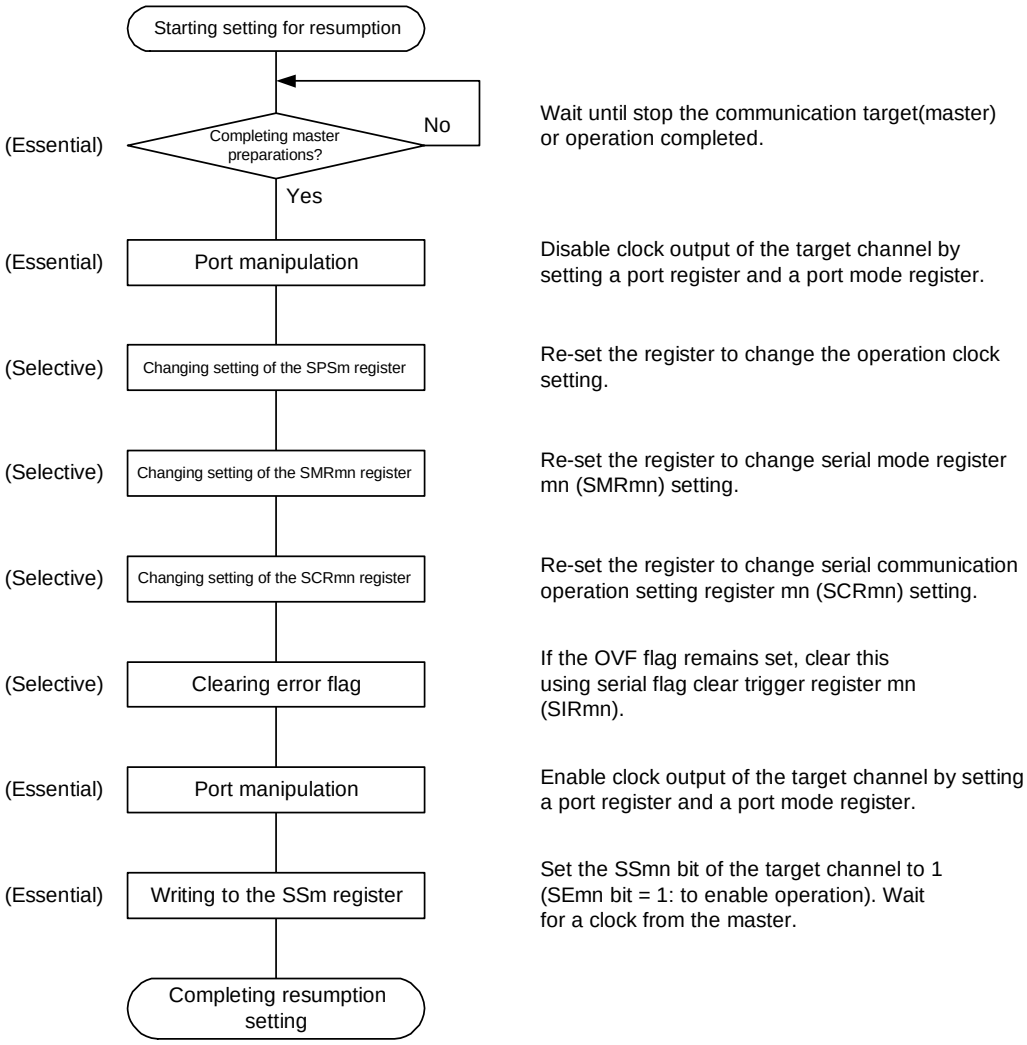


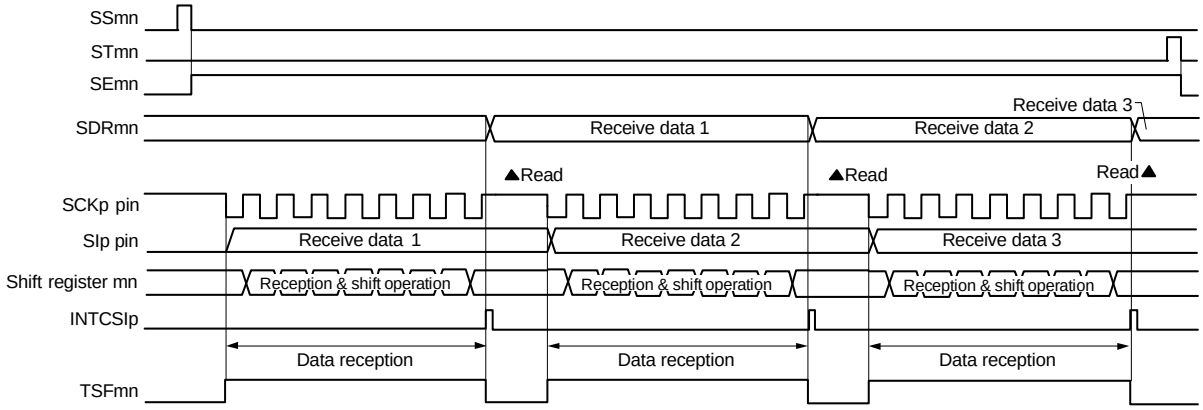
Figure 20 - 60 Procedure for Resuming Slave Reception



Remark If PER0 is rewritten while stopping the master transmission and the clock supply is stopped, wait until the transmission target (master) stops or transmission finishes, and then perform initialization instead of restarting the transmission.

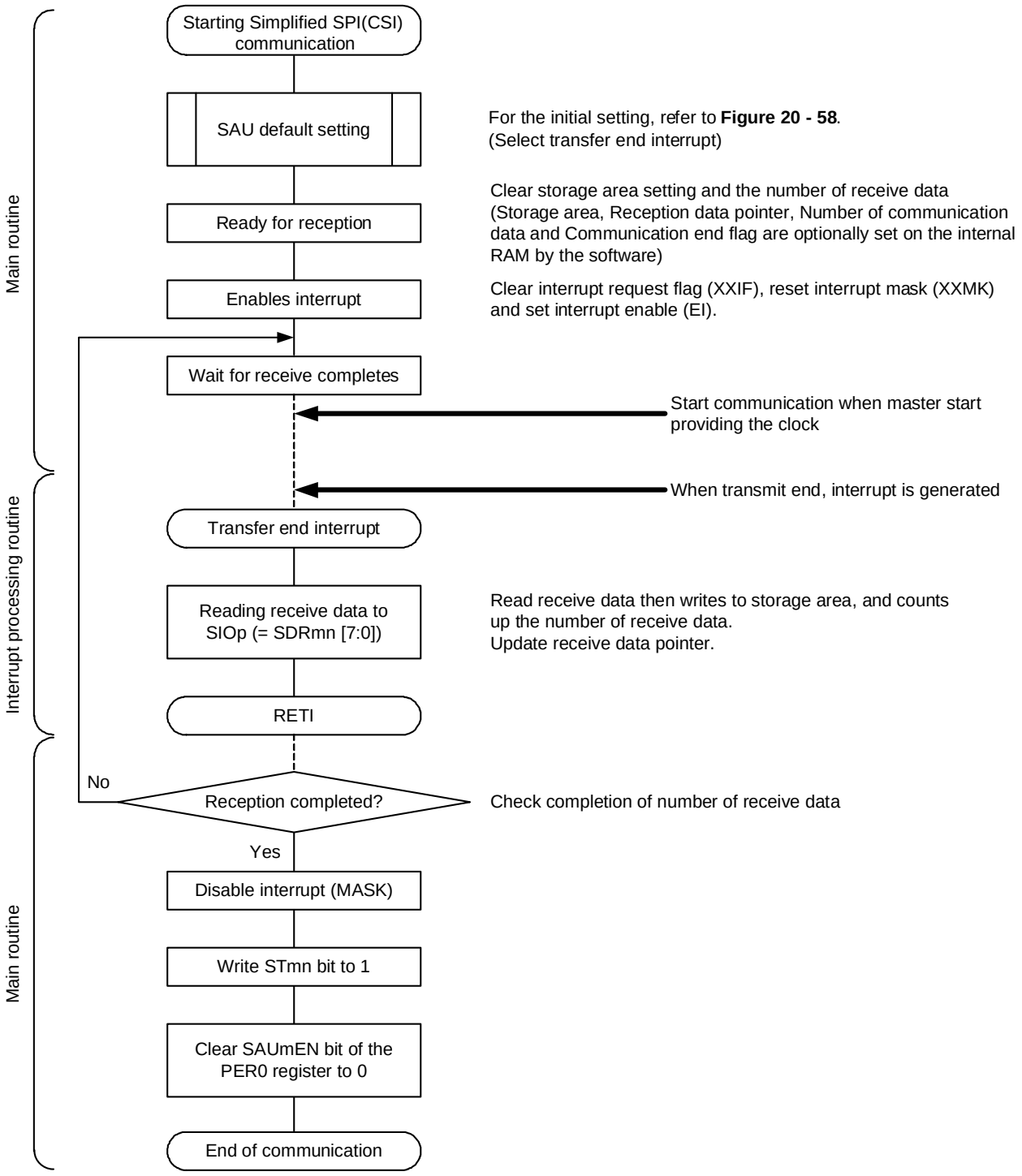
(3) Processing flow (in single-reception mode)

Figure 20 - 61 Timing Chart of Slave Reception (in Single-Reception Mode)
(Type 1: DAPmn = 0, CKPmn = 0)



Remark m: Unit number (m = 0, 1), n: Channel number (n = 0, 2), p: CSI number (p = 00, 10, 20), mn = 00, 02, 10

Figure 20 - 62 Flowchart of Slave Reception (in Single-Reception Mode)



20.5.6 Slave transmission/reception

Slave transmission/reception is that the RL78 microcontroller transmits/receives data to/from another device in the state of a transfer clock being input from another device.

Simplified SPI	CSI00	CSI10	CSI20
Target channel	Channel 0 of SAU0	Channel 2 of SAU0	Channel 0 of SAU1
Pins used	SCK00, SI00, SO00	SCK10, SI10, SO10	SCK20, SI20, SO20
Interrupt	INTCSI00	INTCSI10	INTCSI20
	Transfer end interrupt (in single-transfer mode) or buffer empty interrupt (in continuous transfer mode) can be selected.		
Error detection flag	Overrun error detection flag (OVFmn) only		
Transfer data length	7 or 8 bits		
Transfer rate	Max. f_{MCK}/6 [Hz] Notes 1, 2.		
Data phase	Selectable by the DAPmn bit of the SCRmn register • DAPmn = 0: Data I/O starts from the start of the operation of the serial clock. • DAPmn = 1: Data I/O starts half a clock before the start of the serial clock operation.		
Clock phase	Selectable by the CKPmn bit of the SCRmn register • CKPmn = 0: Non-reverse • CKPmn = 1: Reverse		
Data direction	MSB or LSB first		

Note 1. Because the external serial clock input to the SCK00, SCK10, and SCK20 pins is sampled internally and used, the fastest transfer rate is f_{MCK}/6 [Hz].

Note 2. Use this operation within a range that satisfies the conditions above and the peripheral functions characteristics in the electrical specifications (see **CHAPTER 38** or **CHAPTER 39 ELECTRICAL SPECIFICATIONS**).

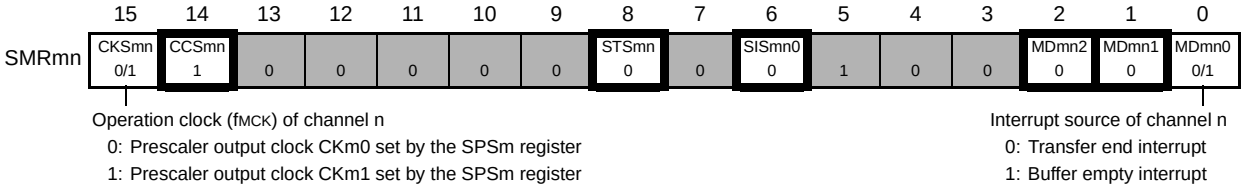
Remark 1. f_{MCK}: Operation clock frequency of target channel
f_{CLK}: Serial clock frequency

Remark 2. m: Unit number (m = 0, 1), n: Channel number (n = 0, 2), mn = 00, 02, 10

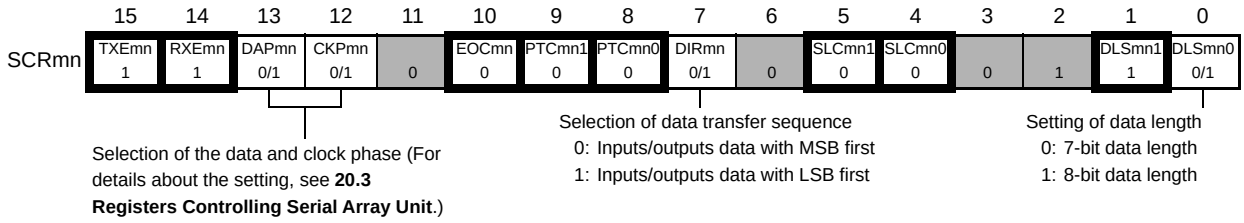
(1) Register setting

Figure 20 - 63 Example of Contents of Registers for Slave Transmission/Reception of Simplified SPI (CSI00, CSI10, CSI20)

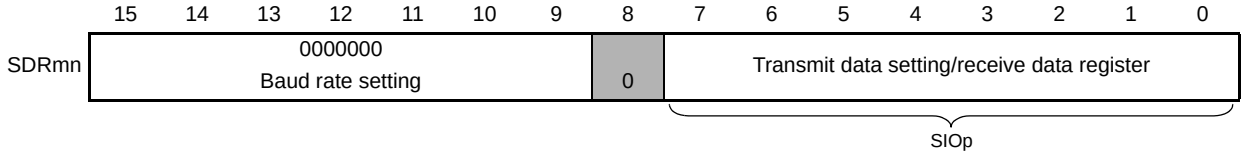
(a) Serial mode register mn (SMRmn)



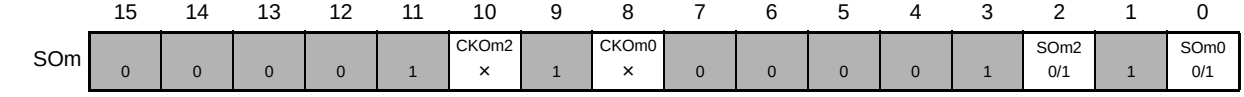
(b) Serial communication operation setting register mn (SCRmn)



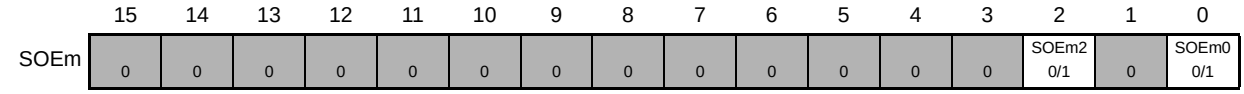
(c) Serial data register mn (SDRmn) (lower 8 bits: SIOp)



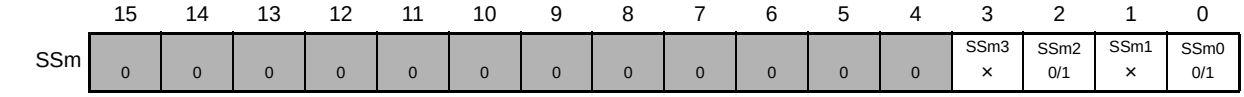
(d) Serial output register m (SOm)... Sets only the bits of the target channel.



(e) Serial output enable register m (SOEm)... Sets only the bits of the target channel to 1.



(f) Serial channel start register m (SSm)... Sets only the bits of the target channel to 1.



Caution Be sure to set transmit data to the SIOp register before the clock from the master is started.

Remark 1. m: Unit number (m = 0, 1), n: Channel number (n = 0, 2), p: CSI number (p = 00, 10, 20), mn = 00, 02, 10

Remark 2. ■: Setting is fixed in the Simplified SPI(CSI) master transmission/reception mode

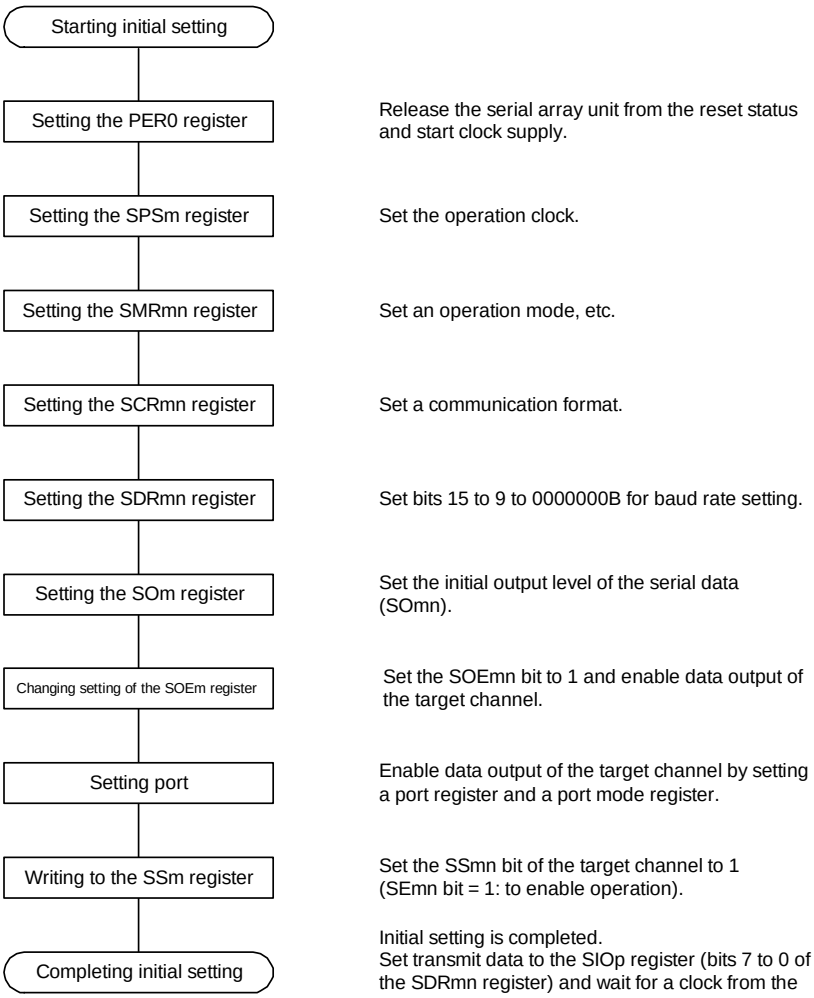
■: Setting disabled (set to the initial value)

×: Bit that cannot be used in this mode (set to the initial value when not used in any mode)

0/1: Set to 0 or 1 depending on the usage of the user

(2) Operation procedure

Figure 20 - 64 Initial Setting Procedure for Slave Transmission/Reception



Caution Be sure to set transmit data to the SIOp register before the clock from the master is started.

Figure 20 - 65 Procedure for Stopping Slave Transmission/Reception

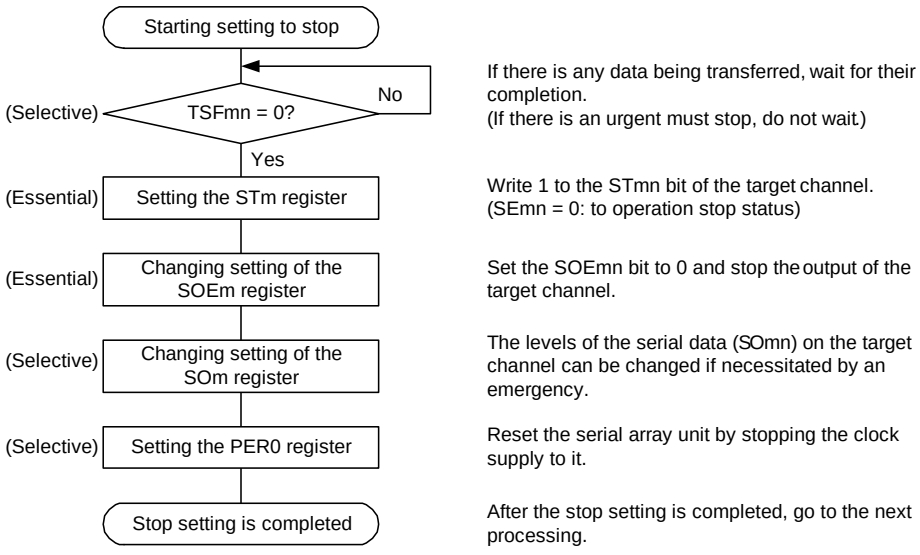
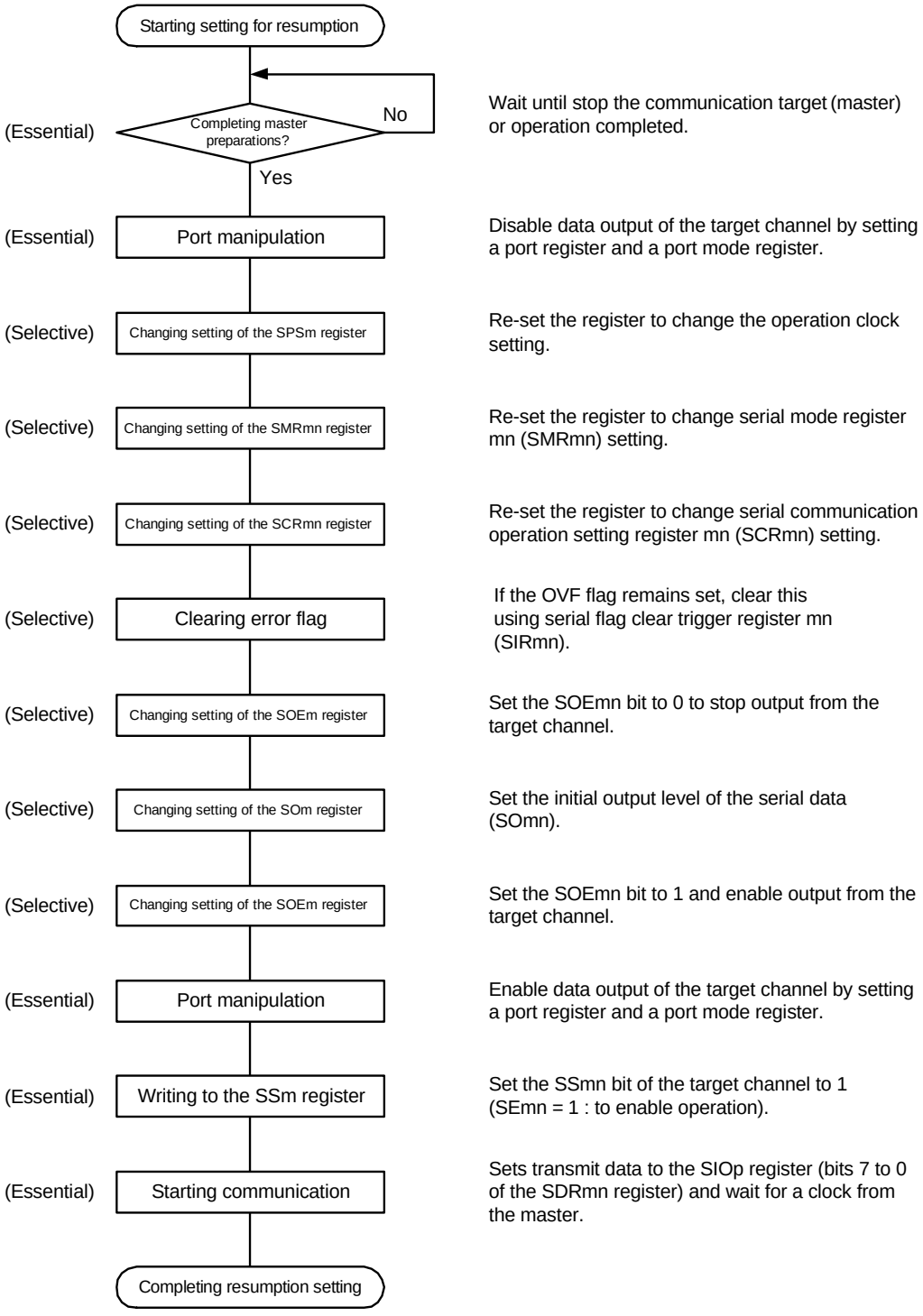


Figure 20 - 66 Procedure for Resuming Slave Transmission/Reception

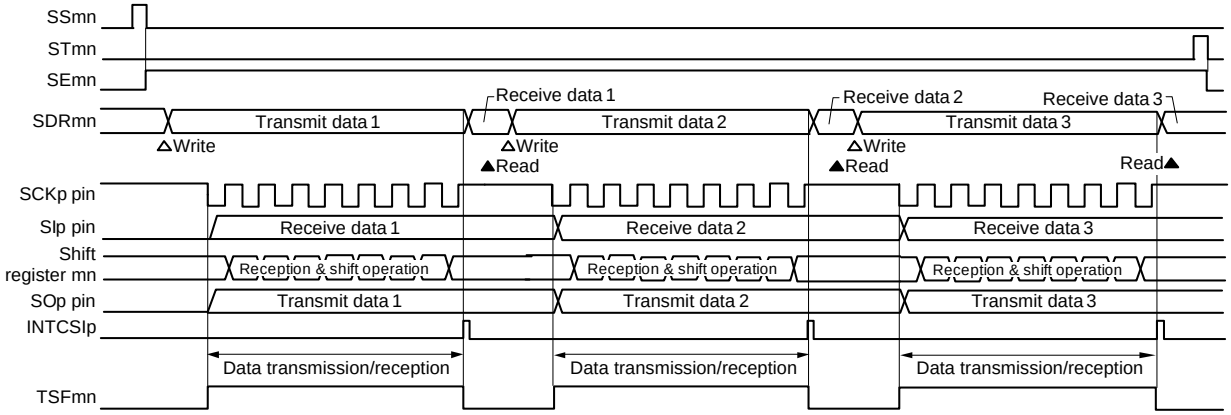


Caution 1. Be sure to set transmit data to the SIOp register before the clock from the master is started.

Caution 2. If PER0 is rewritten while stopping the master transmission and the clock supply is stopped, wait until the transmission target (master) stops or transmission finishes, and then perform initialization instead of restarting the transmission.

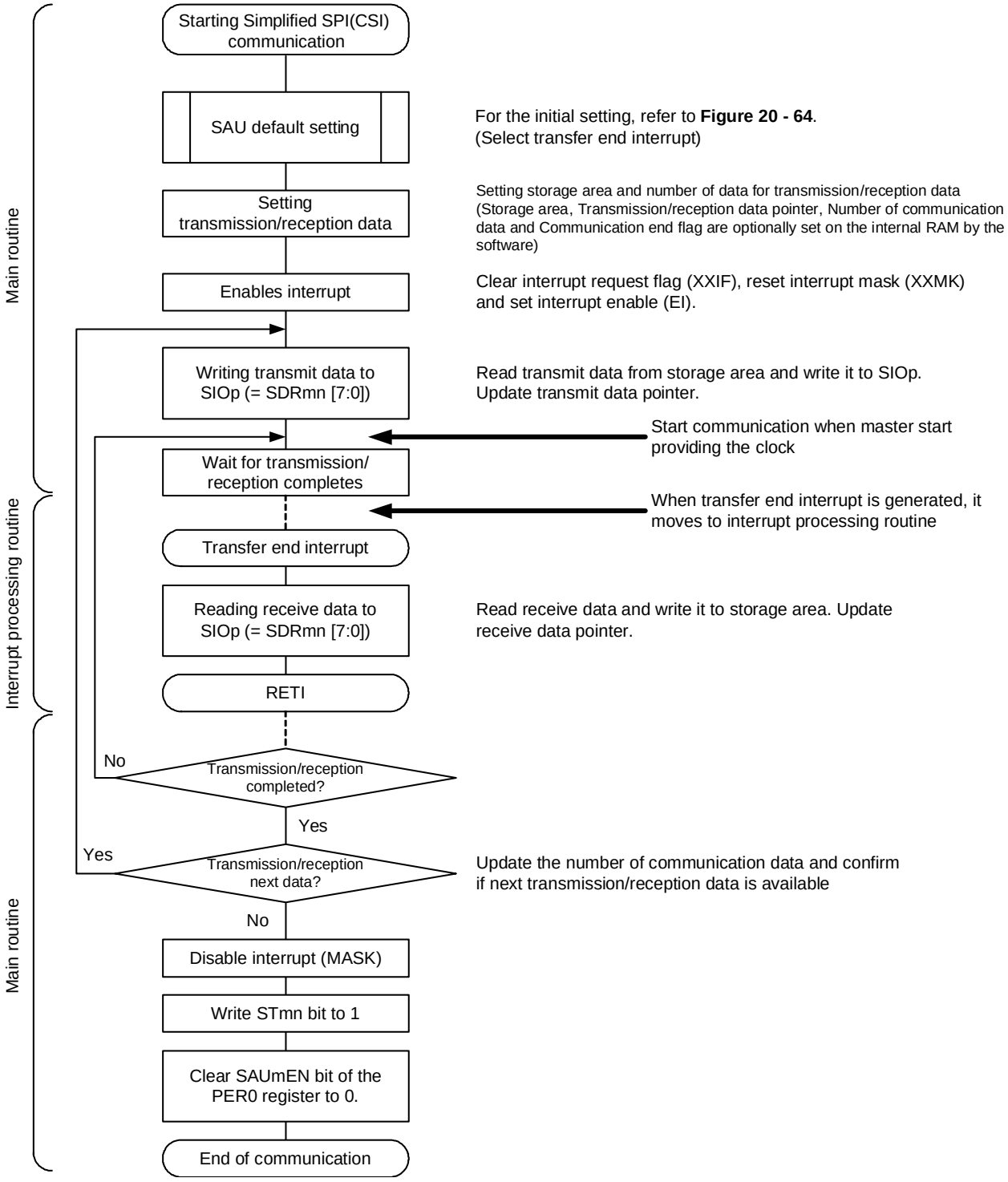
(3) Processing flow (in single-transmission/reception mode)

Figure 20 - 67 Timing Chart of Slave Transmission/Reception (in Single-Transmission/Reception Mode) (Type 1: DAPmn = 0, CKPmn = 0)



Remark m: Unit number (m = 0, 1), n: Channel number (n = 0, 2), p: CSI number (p = 00, 10, 20), mn = 00, 02, 10

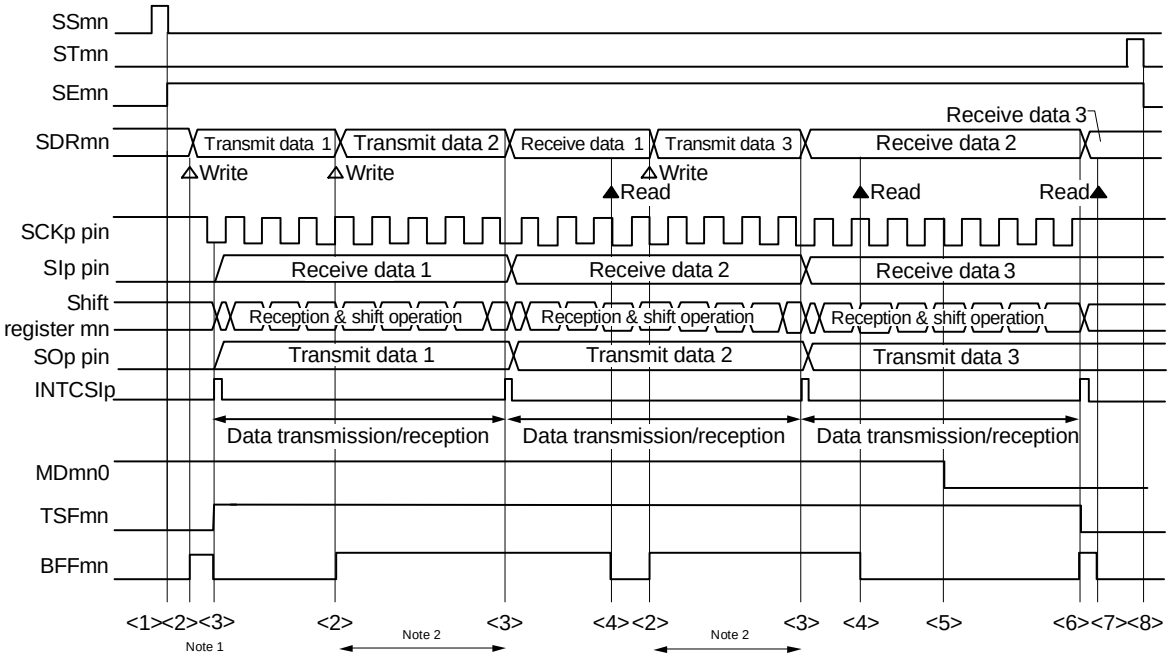
Figure 20 - 68 Flowchart of Slave Transmission/Reception (in Single- Transmission/Reception Mode)



Caution Be sure to set transmit data to the SIOp register before the clock from the master is started.

(4) Processing flow (in continuous transmission/reception mode)

Figure 20 - 69 Timing Chart of Slave Transmission/Reception (in Continuous Transmission/Reception Mode) (Type 1: DAPmn = 0, CKPmn = 0)



Note 1. If transmit data is written to the SDRmn register while the BFFmn bit of serial status register mn (SSRmn) is 1 (valid data is stored in serial data register mn (SDRmn)), the transmit data is overwritten.

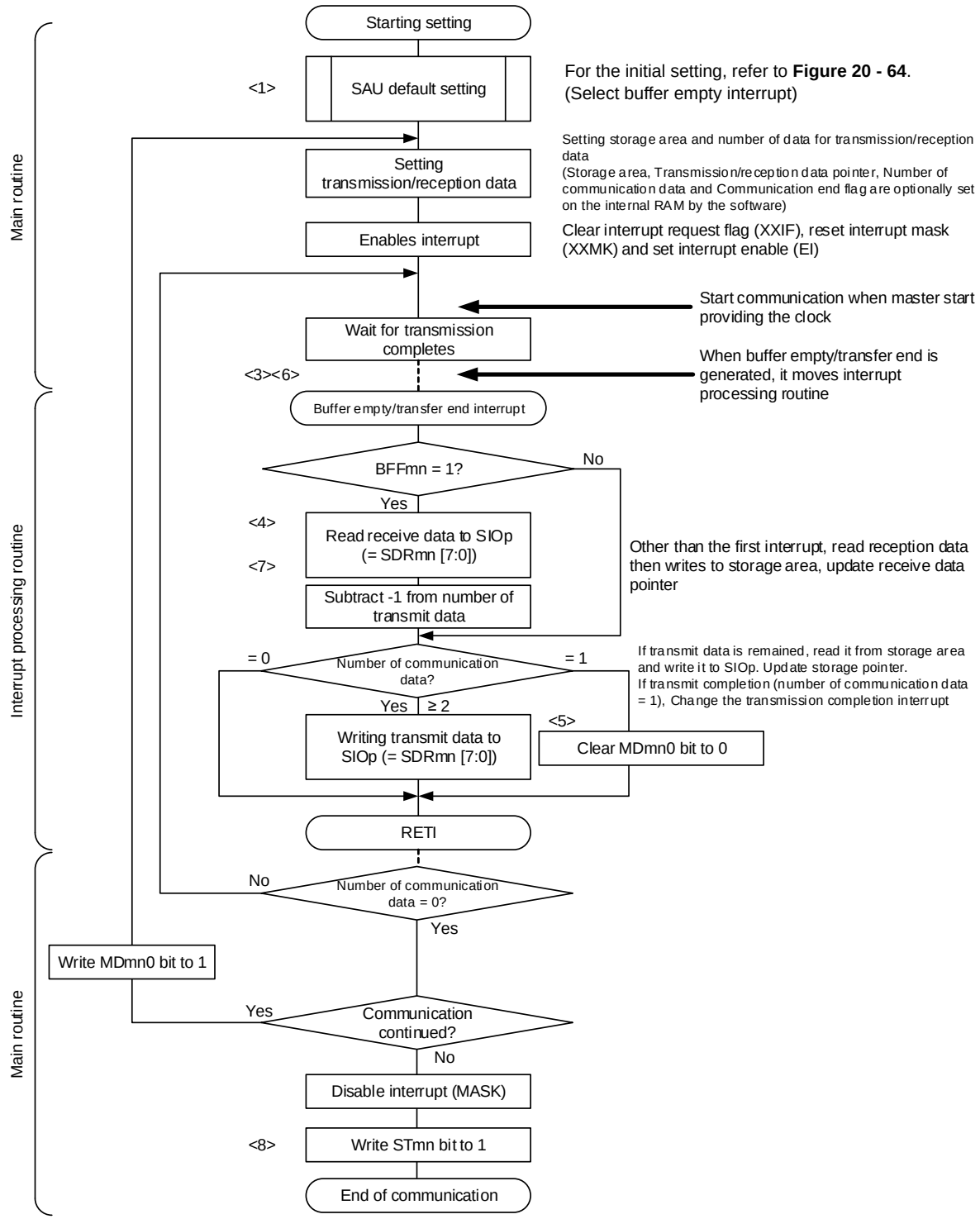
Note 2. The transmit data can be read by reading the SDRmn register during this period. At this time, the transfer operation is not affected.

Caution The MDmn0 bit of serial mode register mn (SMRmn) can be rewritten even during operation. However, rewrite it before transfer of the last bit is started, so that it has been rewritten before the transfer end interrupt of the last transmit data.

Remark 1. <1> to <8> in the figure correspond to <1> to <8> in **Figure 20 - 70 Flowchart of Slave Transmission/Reception (in Continuous Transmission/Reception Mode)**.

Remark 2. m: Unit number (m = 0, 1), n: Channel number (n = 0, 2), p: CSI number (p = 00, 10, 20), mn = 00, 02, 10

Figure 20 - 70 Flowchart of Slave Transmission/Reception (in Continuous Transmission/Reception Mode)



Caution **Be sure to set transmit data to the SIOp register before the clock from the master is started.**

Remark <1> to <8> in the figure correspond to <1> to <8> in **Figure 20 - 69 Timing Chart of Slave Transmission/Reception (in Continuous Transmission/Reception Mode) (Type 1: DAPmn = 0, CKPmn = 0)**.

20.5.7 SNOOZE mode function

SNOOZE mode makes Simplified SPI(CSI) operate reception by SCKp pin input detection while the STOP mode. Normally Simplified SPI(CSI) stops communication in the STOP mode. But, using the SNOOZE mode makes reception Simplified SPI(CSI) operate unless the CPU operation by detecting SCKp pin input. Only CSI00 and CSI20 can be set to the SNOOZE mode.

When using the Simplified SPI(CSI) in SNOOZE mode, make the following setting before switching to the STOP mode (see **Figure 20 - 72 Flowchart of SNOOZE Mode Operation (once startup)** and **Figure 20 - 74 Flowchart of SNOOZE Mode Operation (continuous startup)**.

- When using the SNOOZE mode function, set the SWCm bit of serial standby control register m (SSCm) to 1 just before switching to the STOP mode. After the initial setting has been completed, set the SSm1 bit of serial channel start register m (SSm) to 1.

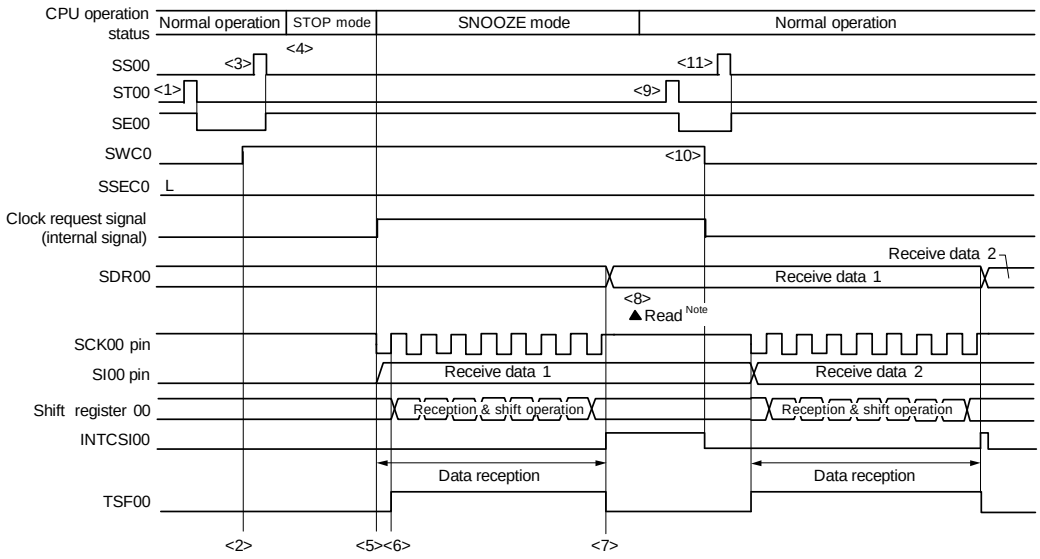
After a transition to the STOP mode, the Simplified SPI(CSI) starts reception operations upon detection of an edge of the SCKp pin.

Caution 1. The SNOOZE mode can only be specified when the high-speed on-chip oscillator clock is selected for f_{CLK}.

Caution 2. The maximum transfer rate when using CSIp in the SNOOZE mode is 1 Mbps.

(1) SNOOZE mode operation (once startup)

Figure 20 - 71 Timing Chart of SNOOZE Mode Operation (once startup) (Type 1: DAPmn = 0, CKPmn = 0)



Note Only read received data while SWCm = 1 and before the next edge of the SCKp pin input is detected.

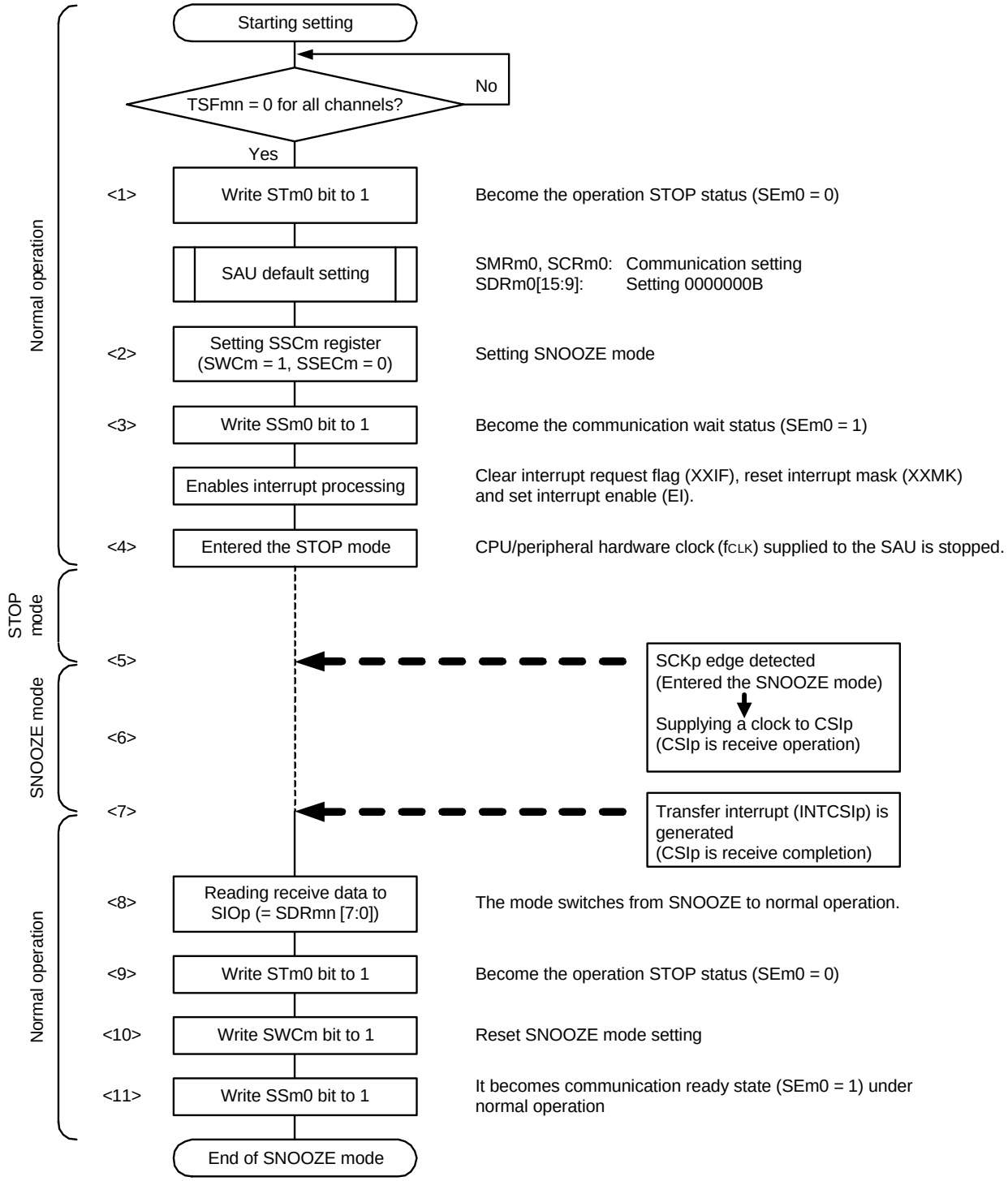
Caution 1. Before switching to the SNOOZE mode or after reception operation in the SNOOZE mode finishes, set the STm0 bit to 1 (clear the SEm0 bit, and stop the operation).
And after completion the receive operation, also clearing SWCm bit to 0 (SNOOZE mode release).

Caution 2. When SWCm = 1, the BFFm1 and OVFm1 flags will not change.

Remark 1. <1> to <11> in the figure correspond to <1> to <11> in **Figure 20 - 72 Flowchart of SNOOZE Mode Operation (once startup)**.

Remark 2. m: Unit number (m = 0, 1), p: CSI number (p = 00, 20)

Figure 20 - 72 Flowchart of SNOOZE Mode Operation (once startup)

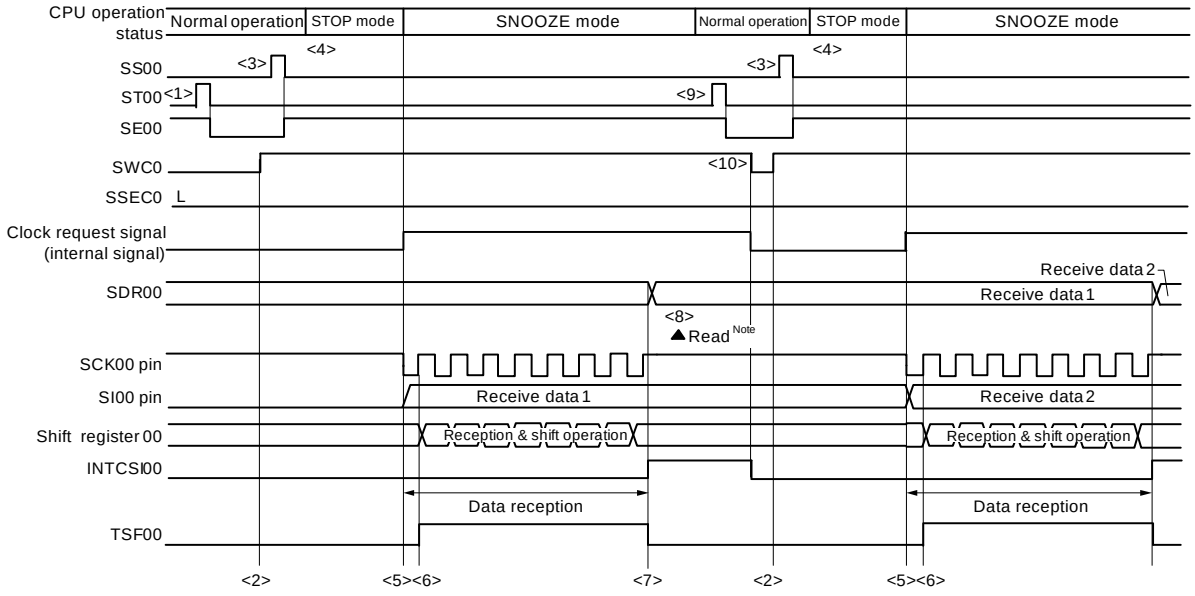


Remark 1. <1> to <11> in the figure correspond to <1> to <11> in **Figure 20 - 71 Timing Chart of SNOOZE Mode Operation (once startup)**.

Remark 2. m: Unit number (m = 0, 1), p: CSI number (p = 00, 20)

(2) SNOOZE mode operation (continuous startup)

Figure 20 - 73 Timing Chart of SNOOZE Mode Operation (continuous startup) (Type 1: DAPmn = 0, CKPmn = 0)



Note Only read received data while SWCm = 1 and before the next edge of the SCKp pin input is detected.

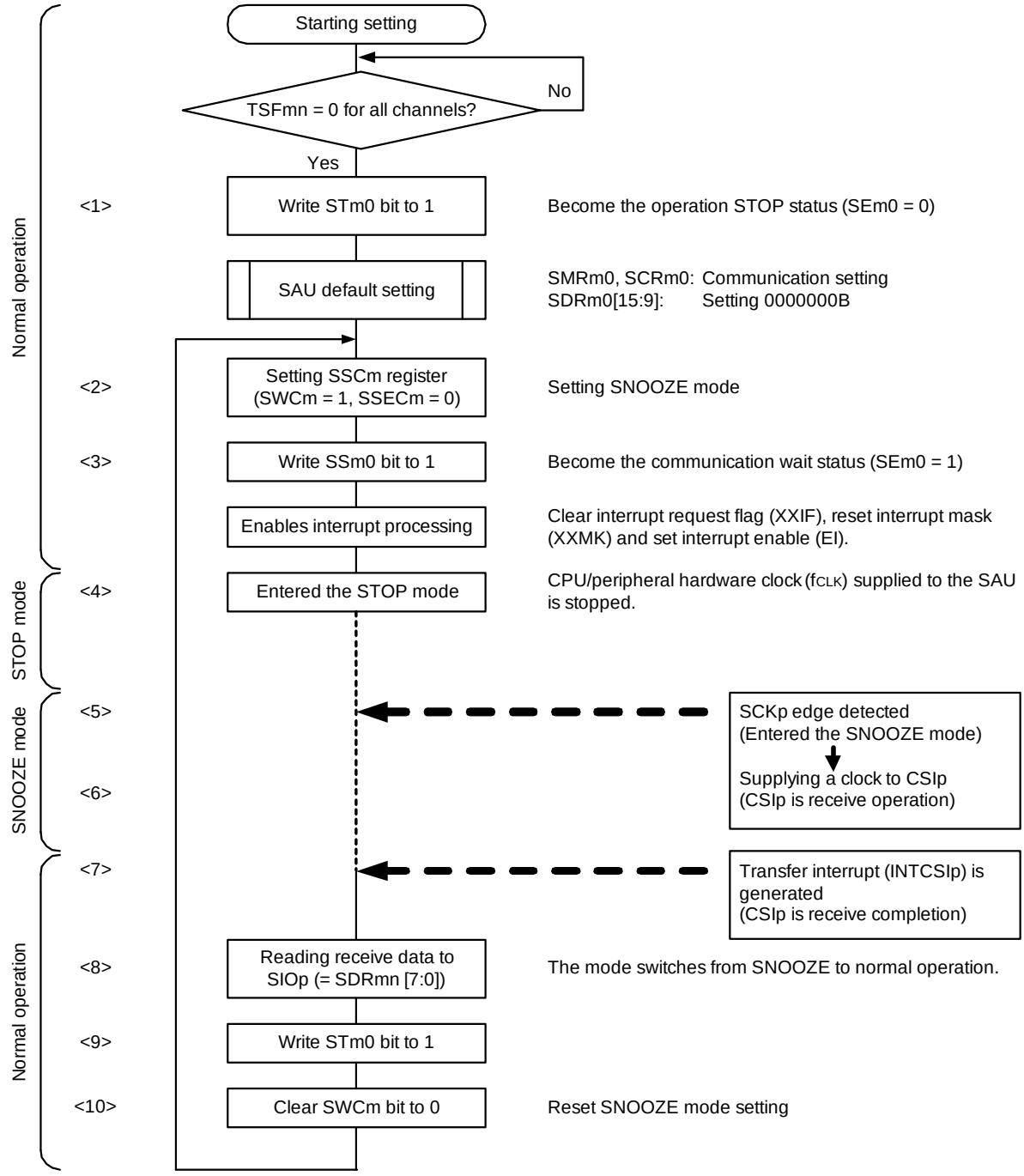
Caution 1. Before switching to the SNOOZE mode or after reception operation in the SNOOZE mode finishes, set the STm0 bit to 1 (clear the SEm0 bit, and stop the operation).
And after completion the receive operation, also clearing SWCm bit to 0 (SNOOZE release).

Caution 2. When SWCm = 1, the BFFm1 and OVFm1 flags will not change.

Remark 1. <1> to <10> in the figure correspond to <1> to <10> in **Figure 20 - 74 Flowchart of SNOOZE Mode Operation (continuous startup)**.

Remark 2. m: Unit number (m = 0, 1), p: CSI number (p = 00, 20)

Figure 20 - 74 Flowchart of SNOOZE Mode Operation (continuous startup)



Remark 1. <1> to <10> in the figure correspond to <1> to <10> in **Figure 20 - 73 Timing Chart of SNOOZE Mode Operation (continuous startup)**.

Remark 2. m: Unit number (m = 0, 1), p: CSI number (p = 00, 20)

20.5.8 Calculating transfer clock frequency

The transfer clock frequency for Simplified SPI (CSI00, CSI10) communication can be calculated by the following expressions.

(1) Master

(Transfer clock frequency) = {Operation clock (f_{MCK}) frequency of target channel} ÷ (SDRmn[15:9] + 1) ÷ 2 [Hz]

(2) Slave

(Transfer clock frequency) = {Frequency of serial clock (SCK) supplied by master} Note [Hz]

Note The permissible maximum transfer clock frequency is f_{MCK}/6.

Remark The value of SDRmn[15:9] is the value of bits 15 to 9 of serial data register mn (SDRmn) (0000000B to 1111111B) and therefore is 0 to 127.

The operation clock (f_{MCK}) is determined by serial clock select register m (SPSm) and bit 15 (CKSmn) of serial mode register mn (SMRmn).

Table 20 - 2 Selection of Operation Clock For Simplified SPI

SMRmn Register	SPSm Register								Operation Clock (f_{MCK}) Note	
CKSmn	PRS m13	PRS m12	PRS m11	PRS m10	PRS m03	PRS m02	PRS m01	PRS m00		f_{CLK} = 24 MHz
0	×	×	×	×	0	0	0	0	f_{CLK}	24 MHz
	×	×	×	×	0	0	0	1	$f_{CLK}/2$	12 MHz
	×	×	×	×	0	0	1	0	$f_{CLK}/2^2$	6 MHz
	×	×	×	×	0	0	1	1	$f_{CLK}/2^3$	3 MHz
	×	×	×	×	0	1	0	0	$f_{CLK}/2^4$	1.5 MHz
	×	×	×	×	0	1	0	1	$f_{CLK}/2^5$	750 kHz
	×	×	×	×	0	1	1	0	$f_{CLK}/2^6$	375 kHz
	×	×	×	×	0	1	1	1	$f_{CLK}/2^7$	187.5 kHz
	×	×	×	×	1	0	0	0	$f_{CLK}/2^8$	93.8 kHz
	×	×	×	×	1	0	0	1	$f_{CLK}/2^9$	46.9 kHz
	×	×	×	×	1	0	1	0	$f_{CLK}/2^{10}$	23.4 kHz
	×	×	×	×	1	0	1	1	$f_{CLK}/2^{11}$	11.7 kHz
	×	×	×	×	1	1	0	0	$f_{CLK}/2^{12}$	5.86 kHz
	×	×	×	×	1	1	0	1	$f_{CLK}2^{13}$	2.93 kHz
	×	×	×	×	1	1	1	0	$f_{CLK}/2^{14}$	1.46 kHz
	×	×	×	×	1	1	1	1	$f_{CLK}/2^{15}$	732 Hz
1	0	0	0	0	×	×	×	×	f_{CLK}	24 MHz
	0	0	0	1	×	×	×	×	$f_{CLK}/2$	12 MHz
	0	0	1	0	×	×	×	×	$f_{CLK}/2^2$	6 MHz
	0	0	1	1	×	×	×	×	$f_{CLK}/2^3$	3 MHz
	0	1	0	0	×	×	×	×	$f_{CLK}/2^4$	1.5 MHz
	0	1	0	1	×	×	×	×	$f_{CLK}/2^5$	750 kHz
	0	1	1	0	×	×	×	×	$f_{CLK}/2^6$	375 kHz
	0	1	1	1	×	×	×	×	$f_{CLK}/2^7$	187.5 kHz
	1	0	0	0	×	×	×	×	$f_{CLK}/2^8$	93.8 kHz
	1	0	0	1	×	×	×	×	$f_{CLK}/2^9$	46.9 kHz
	1	0	1	0	×	×	×	×	$f_{CLK}/2^{10}$	23.4 kHz
	1	0	1	1	×	×	×	×	$f_{CLK}/2^{11}$	11.7 kHz
	1	1	0	0	×	×	×	×	$f_{CLK}/2^{12}$	5.86 kHz
	1	1	0	1	×	×	×	×	$f_{CLK}/2^{13}$	2.93 kHz
	1	1	1	0	×	×	×	×	$f_{CLK}/2^{14}$	1.46 kHz
	1	1	1	1	×	×	×	×	$f_{CLK}/2^{15}$	732 Hz

Note When changing the clock selected for f_{CLK} (by changing the system clock control register (CKC) value), do so after having stopped (serial channel stop register m (STm) = 000FH) the operation of the serial array unit (SAU).

Remark 1. ×: Don't care

Remark 2. m: Unit number (m = 0, 1), n: Channel number (n = 0, 2), mn = 00, 02, 10

20.5.9 Procedure for processing errors that occurred during Simplified SPI (CSI00, CSI10, CSI20) communication

The procedure for processing errors that occurred during Simplified SPI (CSI00, CSI10, CSI20) communication is described in **Figure 20 - 75**.

Figure 20 - 75 Processing Procedure in Case of Overrun Error

Software Manipulation	Hardware Status	Remark
Reads serial data register mn (SDRmn). →	The BFFmn bit of the SSRmn register is set to 0 and channel n is enabled to receive data.	This is to prevent an overrun error if the next reception is completed during error processing.
Reads serial status register mn (SSRmn).		Error type is identified and the read value is used to clear error flag.
Writes 1 to serial flag clear trigger register mn (SIRmn). →	Error flag is cleared.	Error can be cleared only during reading, by writing the value read from the SSRmn register to the SIRmn register without modification.

Remark m: Unit number (m = 0, 1), n: Channel number (n = 0, 2), mn = 00, 02, 10

20.6 Clock Synchronous Serial Communication with Slave Select Input Function

Channel 0 of SAU0 correspond to the clock synchronous serial communication with slave select input function.

[Data transmission/reception]
- Data length of 7 or 8 bits
- Phase control of transmit/receive data
- MSB/LSB first selectable
- Level setting of transmit/receive data

[Clock control]
- Phase control of I/O clock
- Setting of transfer period by prescaler and internal counter of each channel
- Maximum transfer rate Note

  During slave communication: Max. $f_{MCK}/6$

[Interrupt function]
- Transfer end interrupt/buffer empty interrupt

[Error detection flag]
- Overrun error

Note Use the clocks within a range satisfying the SCK cycle time (t_{KCY}) characteristics. For details, see **CHAPTER 38** or **CHAPTER 39 ELECTRICAL SPECIFICATIONS**.

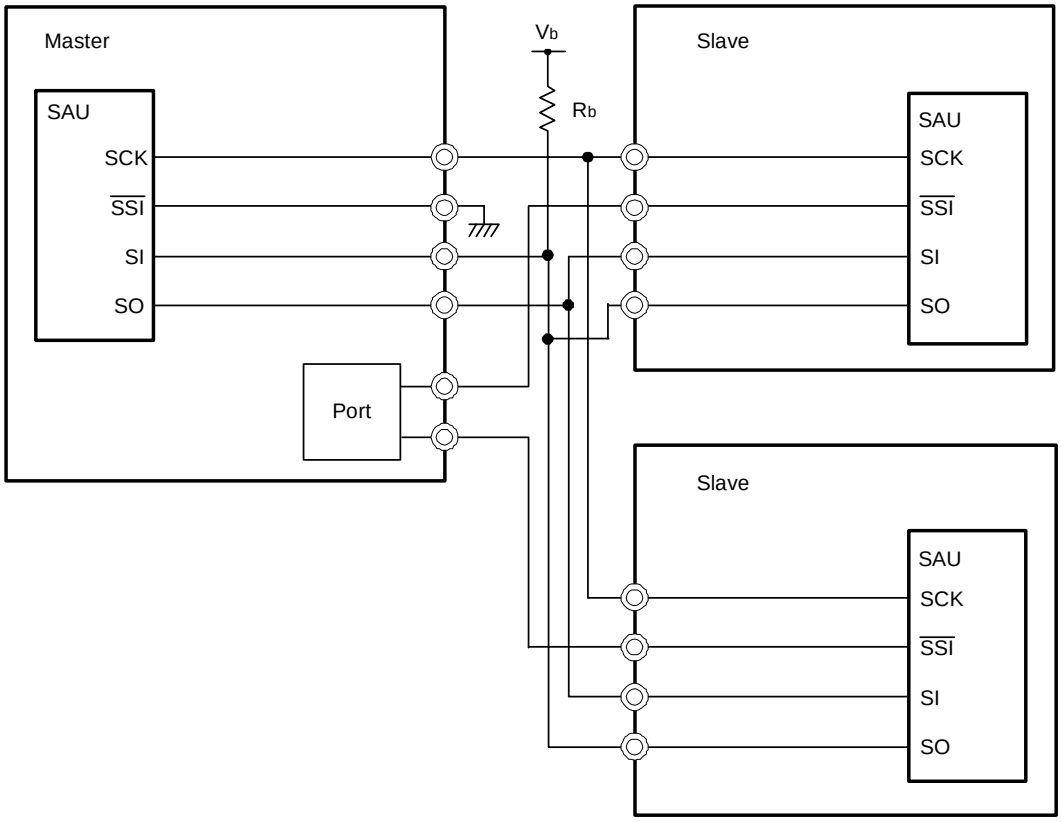
Unit	Channel	Used as Simplified SPI(CSI)	Used as UART	Used as Simplified I^2C
0	0	CSI00 (supporting slave select input function)	UART0 (supporting LIN-bus)	IIC00
	1	—		—
	2	CSI10	UART1	IIC10
	3	—		—
1	0	CSI20	UART2	IIC20
	1	—		—

Slave select input function performs the following three types of communication operations.
- Slave transmission (See **20.6.1**.)
- Slave reception (See **20.6.2**.)
- Slave transmission/reception (See **20.6.3**.)

Multiple slaves can be connected to a master and communication can be performed by using the slave select input function. The master outputs a slave select signal to the slave (one) that is the other party of communication, and each slave judges whether it has been selected as the other party of communication and controls the SO pin output. When a slave is selected, transmit data can be communicated from the SO pin to the master. When a slave is not selected, the SO pin is set to high-level output. Therefore, in an environment where multiple slaves are connected, it is necessary set the SO pin to N-ch open-drain and pull up the node. Furthermore, when a slave is not selected, no transmission/reception operation is performed even if a serial clock is input from the master.

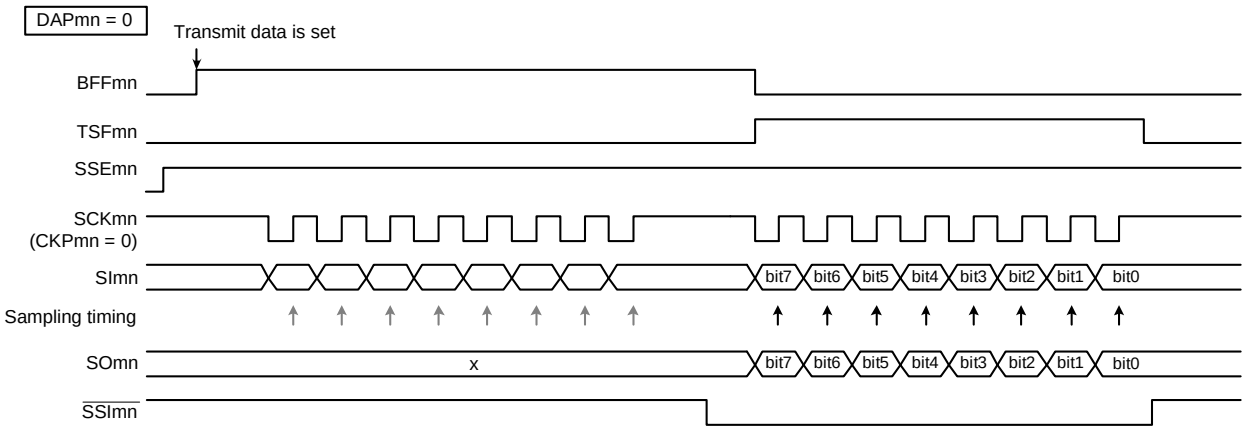
Caution Output the slave select signal by port manipulation.

Figure 20 - 76 Example of Slave Select Input Function Configuration

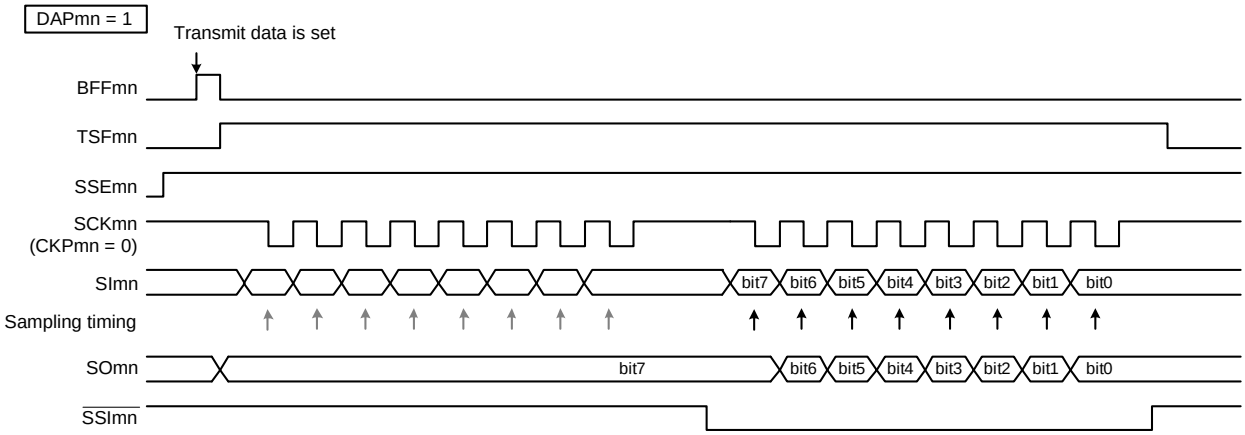


Caution Make sure $EV_{DD0} \geq V_b$.
Select the N-ch open-drain output (EV_{DD} tolerance) mode for the SO00 pin.

Figure 20 - 77 Slave Select Input Function Timing Diagram



While $\overline{\text{SSImn}}$ is at high level, transmission is not performed even if the falling edge of SCKmn (serial clock) arrives, and neither is receive data sampled in synchronization with the rising edge.
When $\overline{\text{SSImn}}$ goes to low level, data is output (shifted) in synchronization with the falling edge of the serial clock and a reception operation is performed in synchronization with the rising edge.



If DAPmn = 1, when transmit data is set while $\overline{\text{SSImn}}$ is at high level, the first data (bit 7) is output to the data output. However, no shift operation is performed even if the rising edge of SCKmn (serial clock) arrives, and neither is receive data sampled in synchronization with the falling edge. When $\overline{\text{SSImn}}$ goes to low level, data is output (shifted) in synchronization with the next rising edge and a reception operation is performed in synchronization with the falling edge.

Remark m: Unit number (m = 0), n: Channel number (n = 0)

20.6.1 Slave transmission

Slave transmission is that the RL78 microcontroller transmits data to another device in the state of a transfer clock being input from another device.

Slave Select Input Function	CSI00
Target channel	Channel 0 of SAU0
Pins used	SCK00, SO00, $\overline{\text{SSI00}}$
Interrupt	INTCSI00
	Transfer end interrupt (in single-transfer mode) or buffer empty interrupt (in continuous transfer mode) can be selected.
Error detection flag	Overrun error detection flag (OVFmn) only
Transfer data length	7 or 8 bits
Transfer rate	Max. f_{MCK}/6 [Hz] Notes 1, 2
Data phase	Selectable by the DAPmn bit of the SCRmn register • DAPmn = 0: Data output starts from the start of the operation of the serial clock. • DAPmn = 1: Data output starts half a clock before the start of the serial clock operation.
Clock phase	Selectable by the CKPmn bit of the SCRmn register • CKPmn = 0: Non-reverse • CKPmn = 1: Reverse
Data direction	MSB or LSB first
Slave select input function	Slave select input function operation selectable

Note 1. Because the external serial clock input to the SCK00 pin is sampled internally and used, the fastest transfer rate is f_{MCK}/6 [Hz].

Note 2. Use this operation within a range that satisfies the conditions above and the peripheral functions characteristics in the electrical specifications (see **CHAPTER 38** or **CHAPTER 39 ELECTRICAL SPECIFICATIONS**).

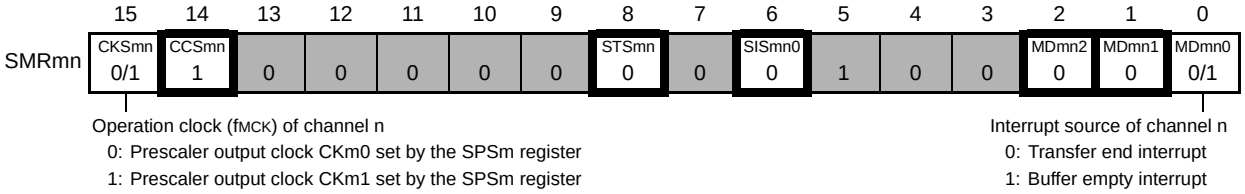
Remark 1. f_{MCK}: Operation clock frequency of target channel

Remark 2. m: Unit number (m = 0), n: Channel number (n = 0)

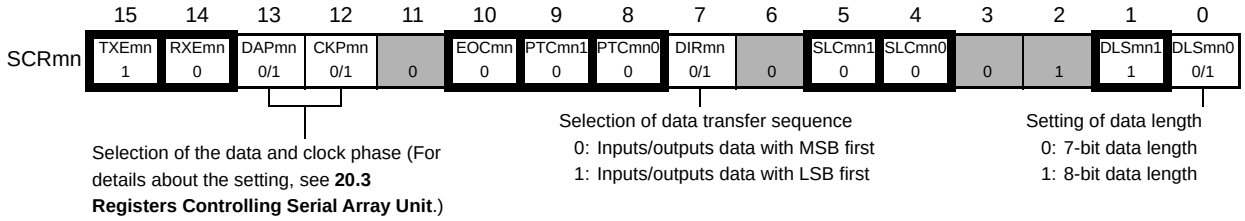
(1) Register setting

Figure 20 - 78 Example of Contents of Registers for Slave Transmission of Slave Select Input Function (CSI00) (1/2)

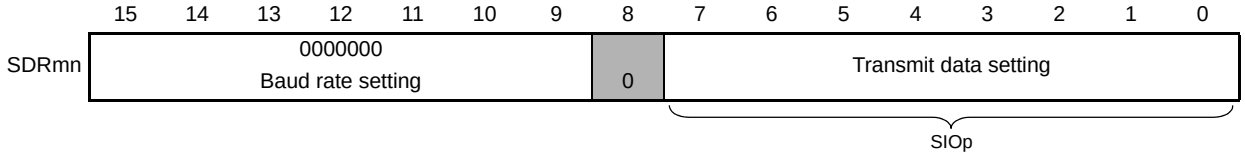
(a) Serial mode register mn (SMRmn)



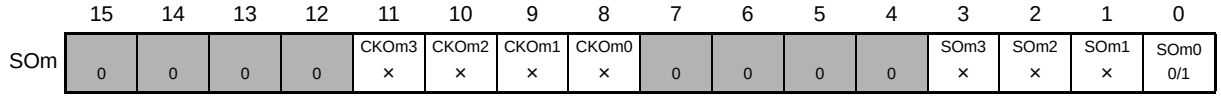
(b) Serial communication operation setting register mn (SCRmn)



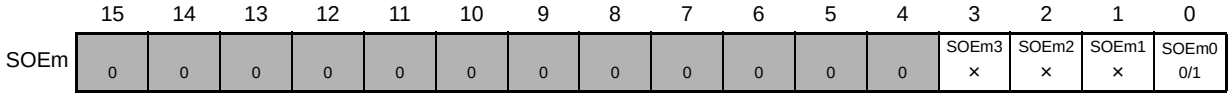
(c) Serial data register mn (SDRmn) (lower 8 bits: SIOp)



(d) Serial output register m (SOm)... Sets only the bits of the target channel.



(e) Serial output enable register m (SOEm)... Sets only the bits of the target channel to 1.



Remark 1. m: Unit number (m = 0), n: Channel number (n = 0), p: CSI number (p = 00)

Remark 2. ■: Setting is fixed in the Simplified SPI(CSI) slave transmission mode,

■: Setting disabled (set to the initial value)

×: Bit that cannot be used in this mode (set to the initial value when not used in any mode)

0/1: Set to 0 or 1 depending on the usage of the user

Figure 20 - 78 Example of Contents of Registers for Slave Transmission of Slave Select Input Function (CSI00) (2/2)

(f) Serial channel start register m (SSm)... Sets only the bits of the target channel to 1.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SSm	0	0	0	0	0	0	0	0	0	0	0	0	SSm3 ×	SSm2 ×	SSm1 ×	SSm0 0/1

(g) Input switch control register (ISC)... $\overline{\text{SSI00}}$ input setting in CSI00 slave channel (channel 0 of unit 0).

	7	6	5	4	3	2	1	0
ISC	SSIE00 0/1	0	0	0	0	0	ISC1 0/1	ISC0 0/1

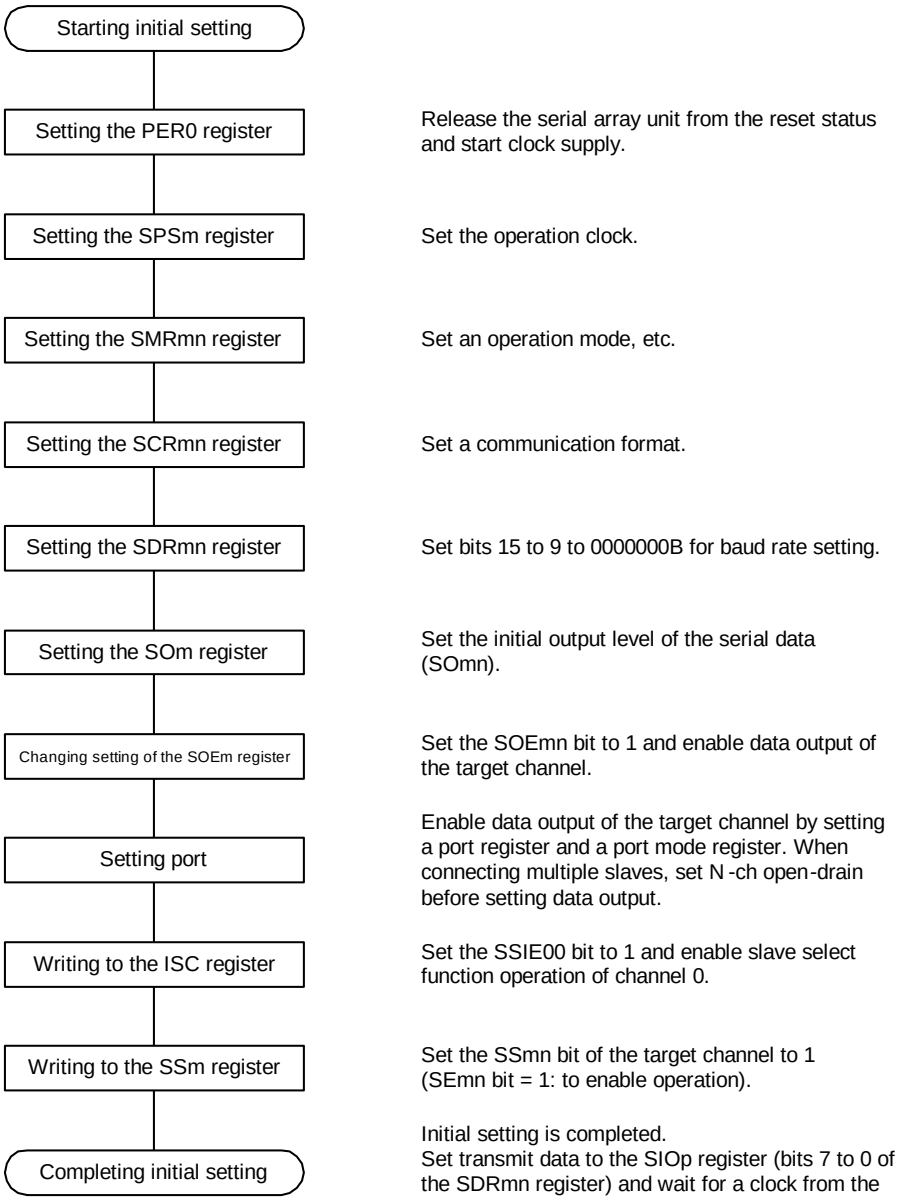
0: Disables the input value of the $\overline{\text{SSI00}}$ pin
1: Enables the input value of the $\overline{\text{SSI00}}$ pin

Remark 1. m: Unit number (m = 0), n: Channel number (n = 0), p: CSI number (p = 00)

Remark 2. : Setting disabled (set to the initial value)
×: Bit that cannot be used in this mode (set to the initial value when not used in any mode)
0/1: Set to 0 or 1 depending on the usage of the user

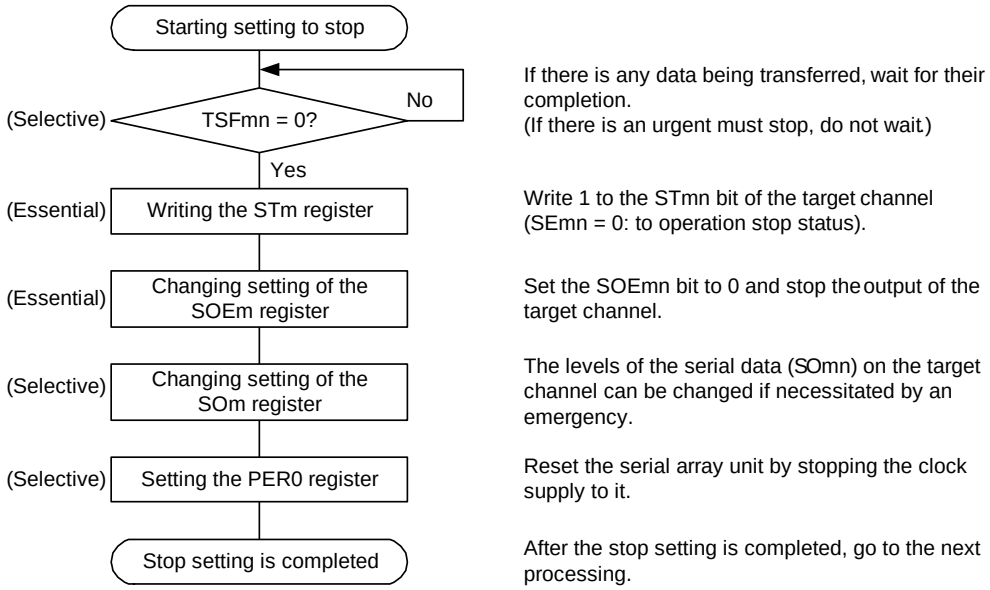
(2) Operation procedure

Figure 20 - 79 Initial Setting Procedure for Slave Transmission



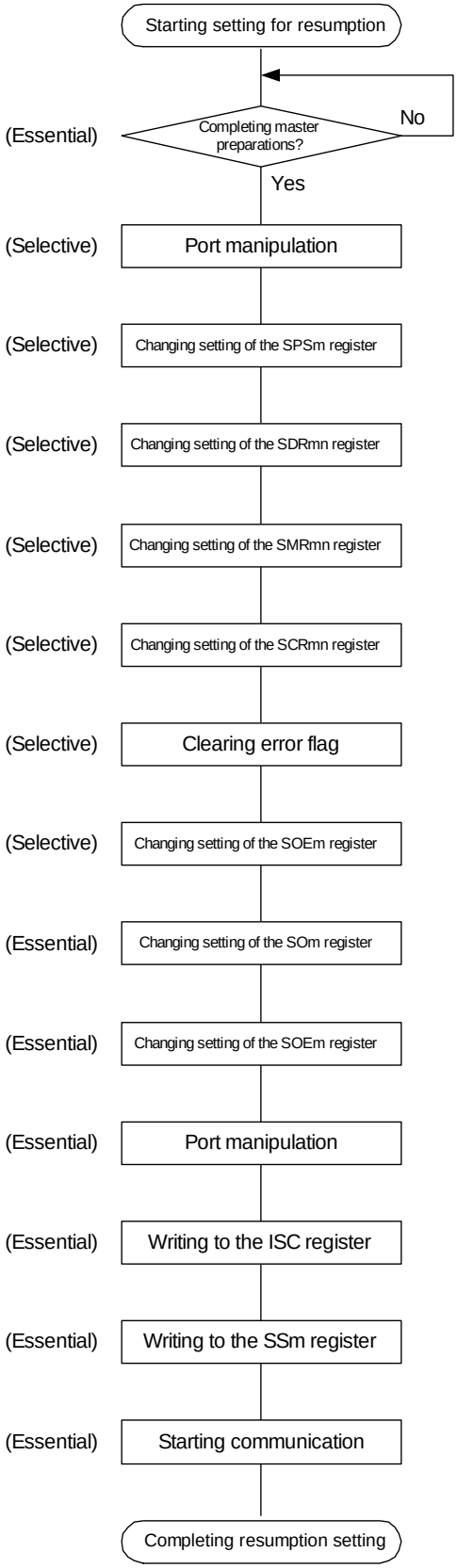
Remark m: Unit number (m = 0), n: Channel number (n = 0), p: CSI number (p = 00)

Figure 20 - 80 Procedure for Stopping Slave Transmission



Remark m: Unit number (m = 0), n: Channel number (n = 0), p: CSI number (p = 00)

Figure 20 - 81 Procedure for Resuming Slave Transmission



Wait until stop the communication target (master) or operation completed.

Disable data output of the target channel by setting a port register and a port mode register.

Re-set the register to change the operation clock setting.

Re-set the register to change the transfer baud rate setting (setting the transfer clock by dividing the operation clock (f_{MCK})).

Re-set the register to change serial mode register mn (SMRmn) setting.

Re-set the register to change serial communication operation setting register mn (SCRmn) setting.

If the OVF flag remains set, clear this using serial flag clear trigger register mn (SIRmn).

Set the SOEmn bit to 0 to stop output from the target channel.

Set the initial output level of the serial data (SOmn).

Set the SOEmn bit to 1 and enable output from the target channel.

Enable data output of the target channel by setting a port register and a port mode register. When connecting multiple slaves, set N-ch open-drain before setting data output.

Set the SSIE00 bit to 1 and enable slave select function operation of channel 0.

Set the SSmn bit of the target channel to 1 (SEmn = 1: to enable operation).

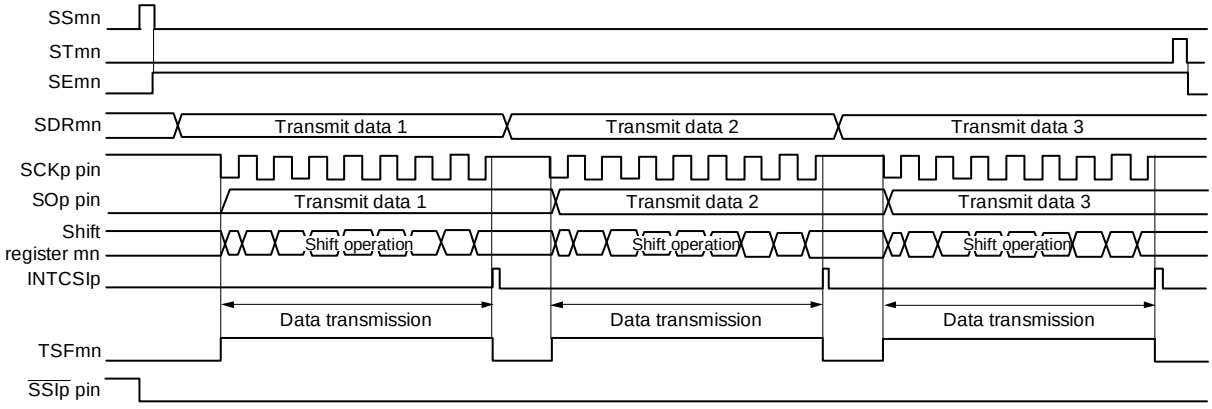
Sets transmit data to the SIOp register (bits 7 to 0 of the SDRmn register) and wait for a clock from the master.

Remark 1. If PER0 is rewritten while stopping the master transmission and the clock supply is stopped, wait until the transmission target (master) stops or transmission finishes, and then perform initialization instead of restarting the transmission.

Remark 2. m: Unit number (m = 0), n: Channel number (n = 0), p: CSI number (p = 00)

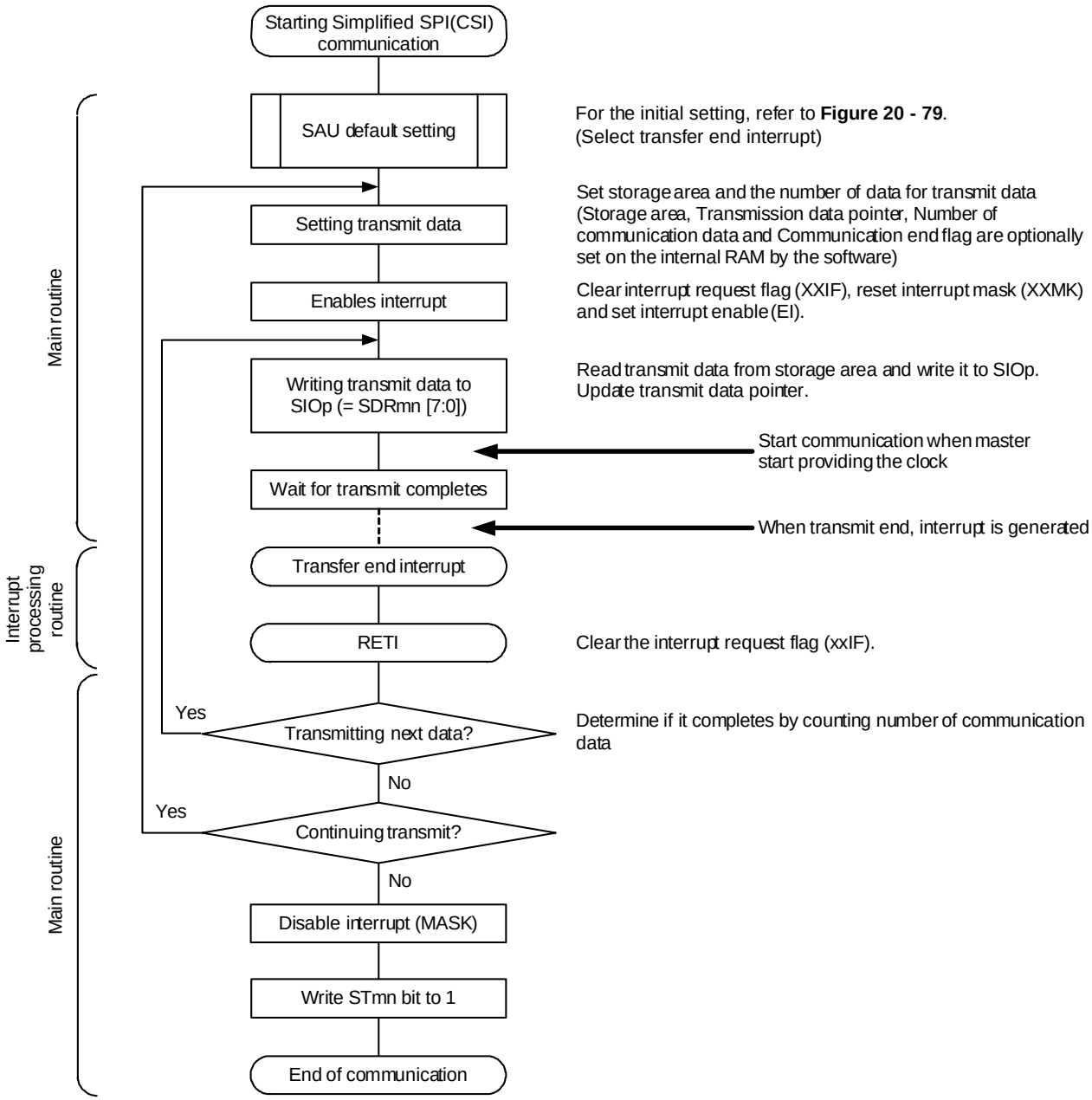
(3) Processing flow (in single-transmission mode)

Figure 20 - 82 Timing Chart of Slave Transmission (in Single-Transmission Mode)
(Type 1: DAPmn = 0, CKPmn = 0)



Remark m: Unit number (m = 0), n: Channel number (n = 0), p: CSI number (p = 00)

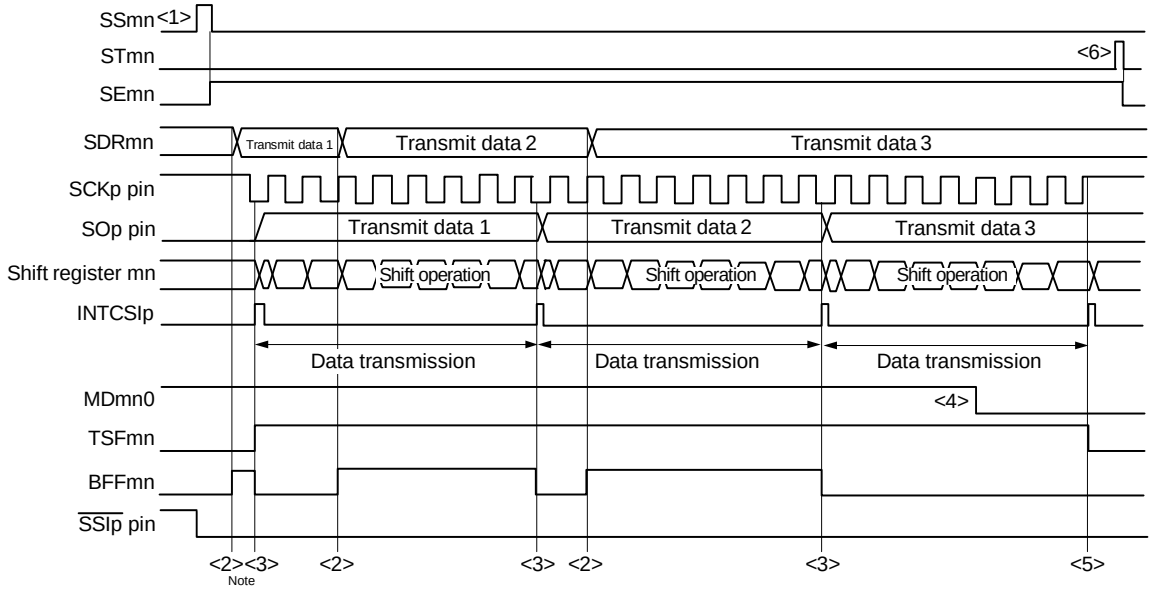
Figure 20 - 83 Flowchart of Slave Transmission (in Single-Transmission Mode)



Remark m: Unit number (m = 0), n: Channel number (n = 0), p: CSI number (p = 00)

(4) Processing flow (in continuous transmission mode)

Figure 20 - 84 Timing Chart of Slave Transmission (in Continuous Transmission Mode)
(Type 1: DAPmn = 0, CKPmn = 0)

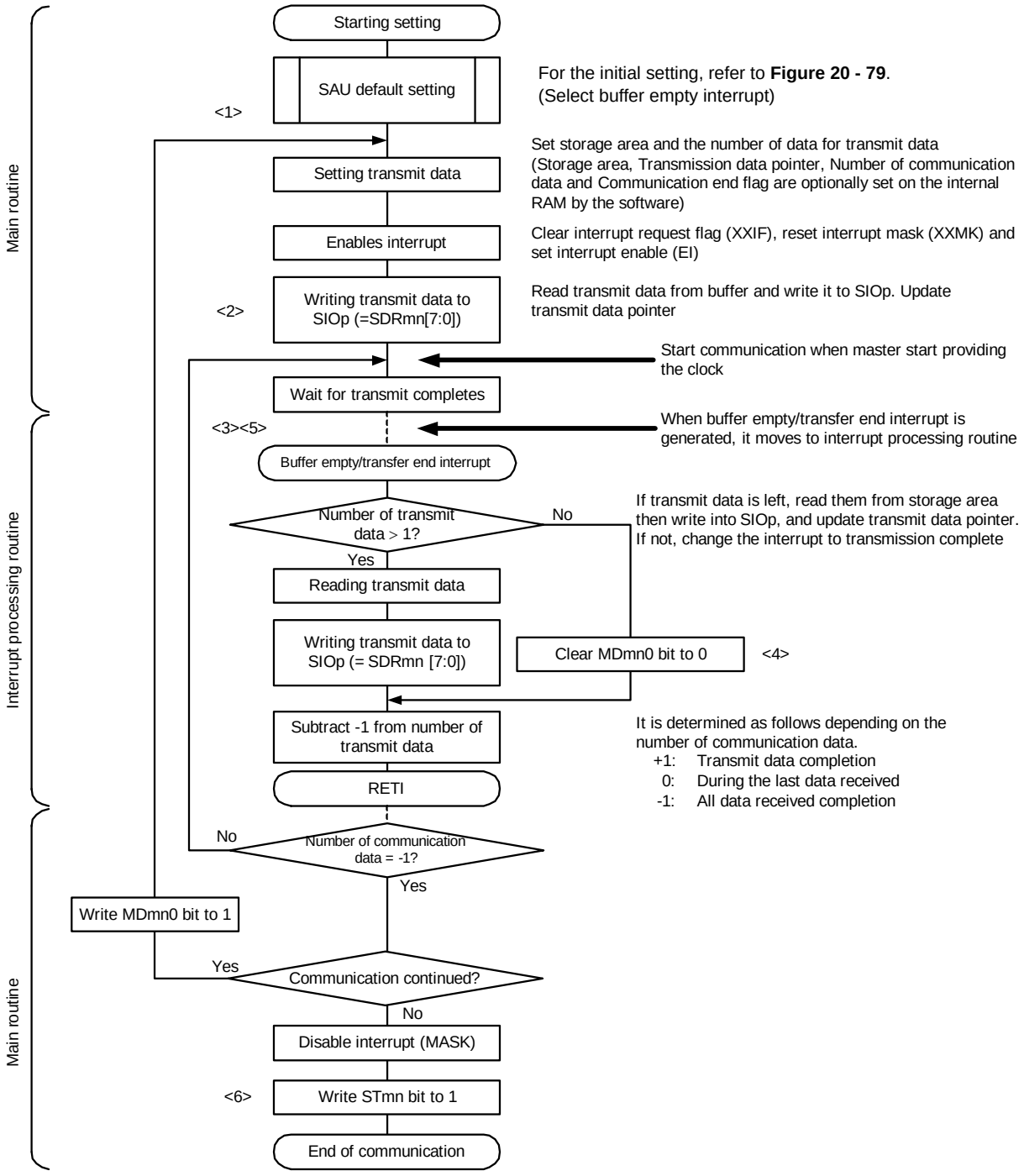


Note If transmit data is written to the SDRmn register while the BFFmn bit of serial status register mn (SSRmn) is 1 (valid data is stored in serial data register mn (SDRmn)), the transmit data is overwritten.

Caution The MDmn0 bit of serial mode register mn (SMRmn) can be rewritten even during operation. However, rewrite it before transfer of the last bit is started.

Remark m: Unit number (m = 0), n: Channel number (n = 0), p: CSI number (p = 00)

Figure 20 - 85 Flowchart of Slave Transmission (in Continuous Transmission Mode)



Remark 1. <1> to <6> in the figure correspond to <1> to <6> in **Figure 20 - 84 Timing Chart of Slave Transmission (in Continuous Transmission Mode) (Type 1: DAPmn = 0, CKPmn = 0)**.

Remark 2. m: Unit number (m = 0), n: Channel number (n = 0), p: CSI number (p = 00)

20.6.2 Slave reception

Slave reception is that the RL78 microcontroller receives data from another device in the state of a transfer clock being input from another device.

Slave Select Input Function	CSI00
Target channel	Channel 0 of SAU0
Pins used	SCK00, SI00, $\overline{\text{SSI00}}$
Interrupt	INTCSI00
	Transfer end interrupt only (Setting the buffer empty interrupt is prohibited.)
Error detection flag	Overrun error detection flag (OVFmn) only
Transfer data length	7 or 8 bits
Transfer rate	Max. f_{MCK}/6 [Hz] Notes 1, 2
Data phase	Selectable by the DAPmn bit of the SCRmn register • DAPmn = 0: Data input starts from the start of the operation of the serial clock. • DAPmn = 1: Data input starts half a clock before the start of the serial clock operation.
Clock phase	Selectable by the CKPmn bit of the SCRmn register • CKPmn = 0: Non-reverse • CKPmn = 1: Reverse
Data direction	MSB or LSB first
Slave select input function	Slave select input function operation selectable

Note 1. Because the external serial clock input to the SCK00 pin is sampled internally and used, the fastest transfer rate is f_{MCK}/6 [Hz].

Note 2. Use this operation within a range that satisfies the conditions above and the peripheral functions characteristics in the electrical specifications (see **CHAPTER 38** or **CHAPTER 39 ELECTRICAL SPECIFICATIONS**).

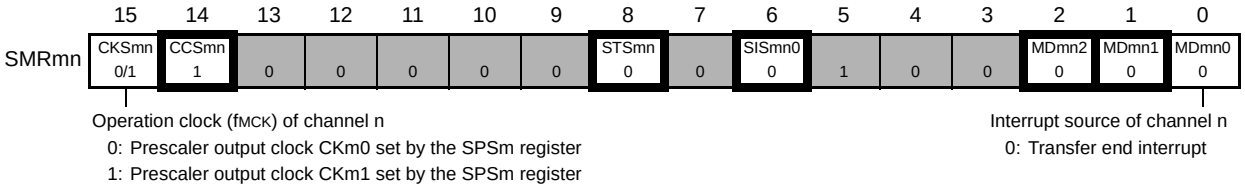
Remark 1. f_{MCK}: Operation clock frequency of target channel

Remark 2. m: Unit number (m = 0), n: Channel number (n = 0)

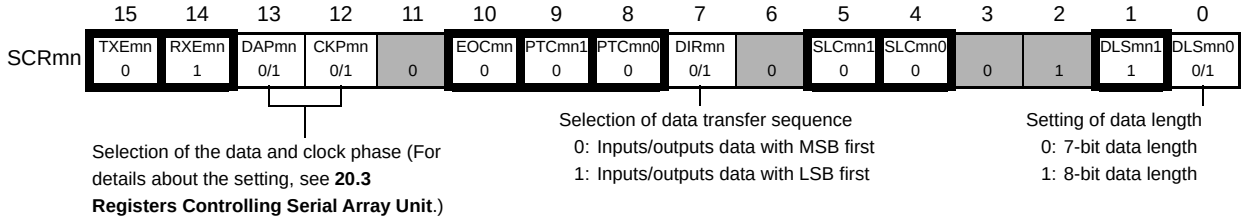
(1) Register setting

Figure 20 - 86 Example of Contents of Registers for Slave Reception of Slave Select Input Function (CSI00) (1/2)

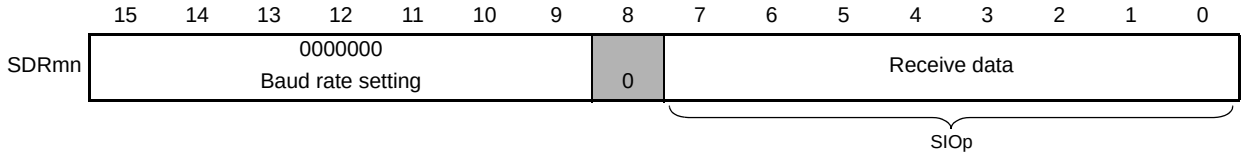
(a) Serial mode register mn (SMRmn)



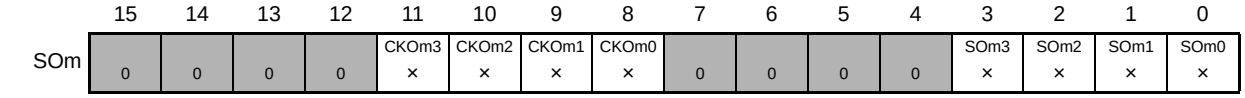
(b) Serial communication operation setting register mn (SCRmn)



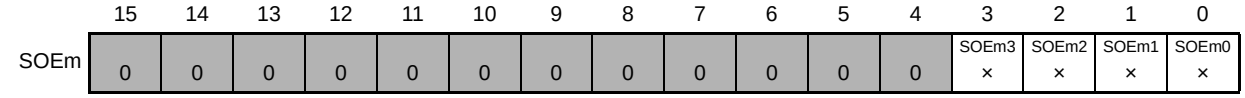
(c) Serial data register mn (SDRmn) (lower 8 bits: SIOp)



(d) Serial output register m (SOm)... The Register that not used in this mode.



(e) Serial output enable register m (SOEm)... The Register that not used in this mode.



Remark 1. m: Unit number (m = 0), n: Channel number (n = 0), p: CSI number (p = 00)

Remark 2. : Setting is fixed in the Simplified SPI(CSI) slave reception mode,

: Setting disabled (set to the initial value)

×: Bit that cannot be used in this mode (set to the initial value when not used in any mode)

0/1: Set to 0 or 1 depending on the usage of the user

Figure 20 - 86 Example of Contents of Registers for Slave Reception of Slave Select Input Function (CSI00) (2/2)

(f) Serial channel start register m (SSm)... Sets only the bits of the target channel to 1.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SSm	0	0	0	0	0	0	0	0	0	0	0	0	SSm3 ×	SSm2 ×	SSm1 ×	SSm0 0/1

(g) Input switch control register (ISC)... $\overline{\text{SSI00}}$ input setting in CSI00 slave channel (channel 0 of unit 0).

	7	6	5	4	3	2	1	0
ISC	SSIE00 0/1	0	0	0	0	0	ISC1 0/1	ISC0 0/1

0: Disables the input value of the $\overline{\text{SSI00}}$ pin
1: Enables the input value of the $\overline{\text{SSI00}}$ pin

Remark 1. m: Unit number (m = 0), n: Channel number (n = 0), p: CSI number (p = 00)

Remark 2. ■: Setting disabled (set to the initial value)
×: Bit that cannot be used in this mode (set to the initial value when not used in any mode)
0/1: Set to 0 or 1 depending on the usage of the user

(2) Operation procedure

Figure 20 - 87 Initial Setting Procedure for Slave Reception

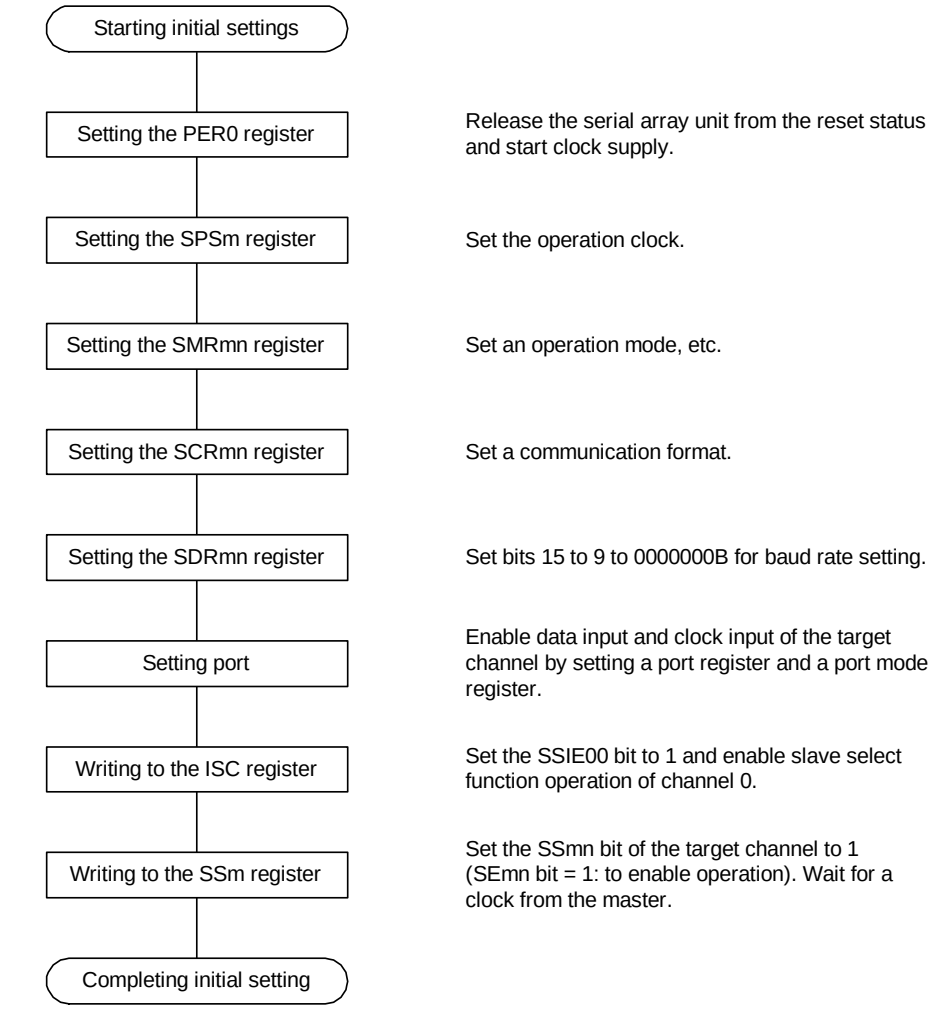
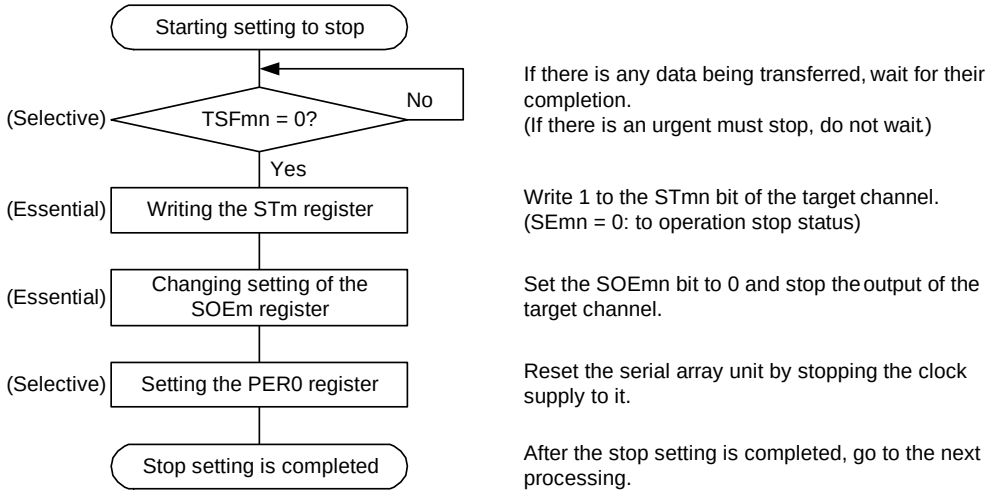
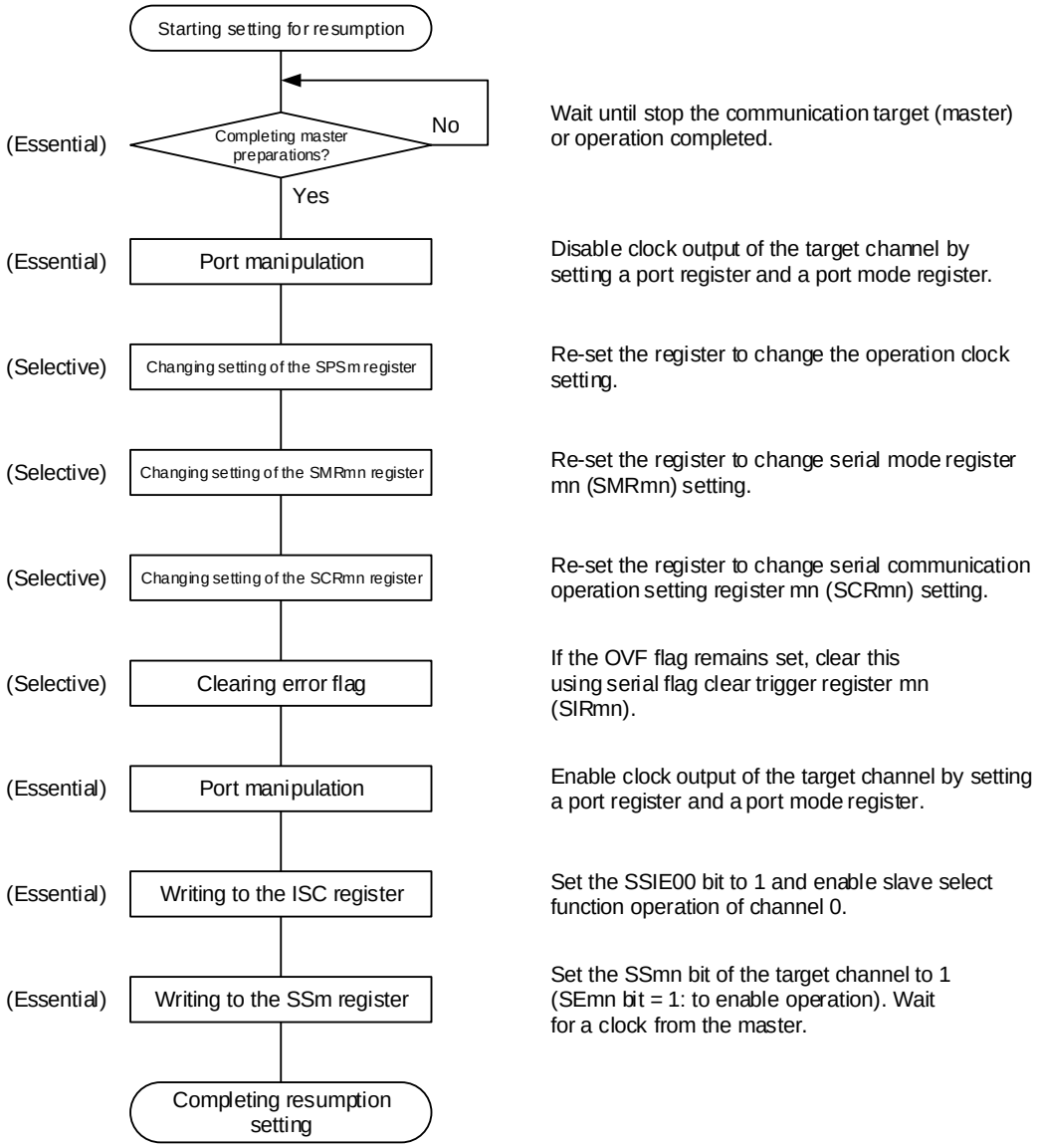


Figure 20 - 88 Procedure for Stopping Slave Reception



Remark m: Unit number (m = 0), n: Channel number (n = 0), p: CSI number (p = 00)

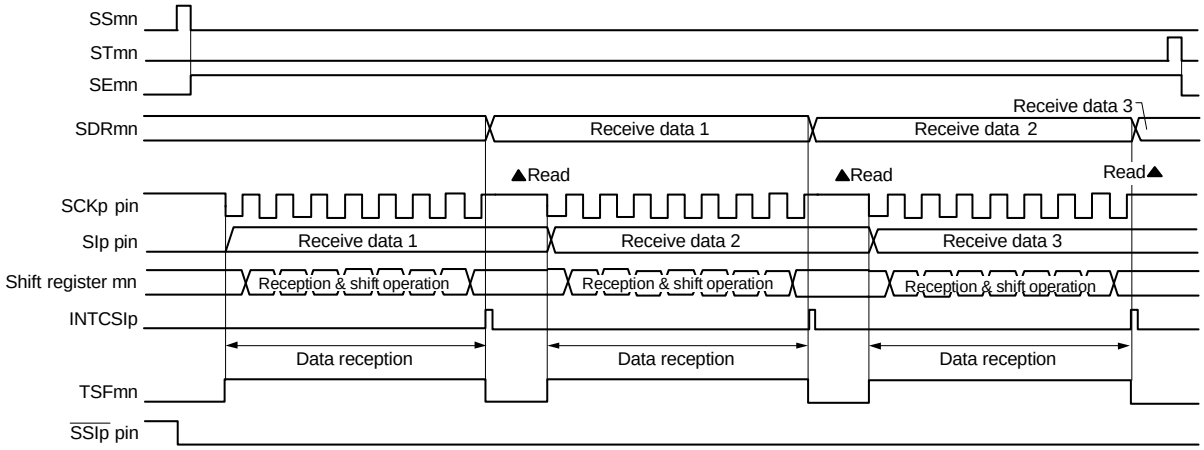
Figure 20 - 89 Procedure for Resuming Slave Reception



Remark m: Unit number (m = 0), n: Channel number (n = 0), p: CSI number (p = 00)

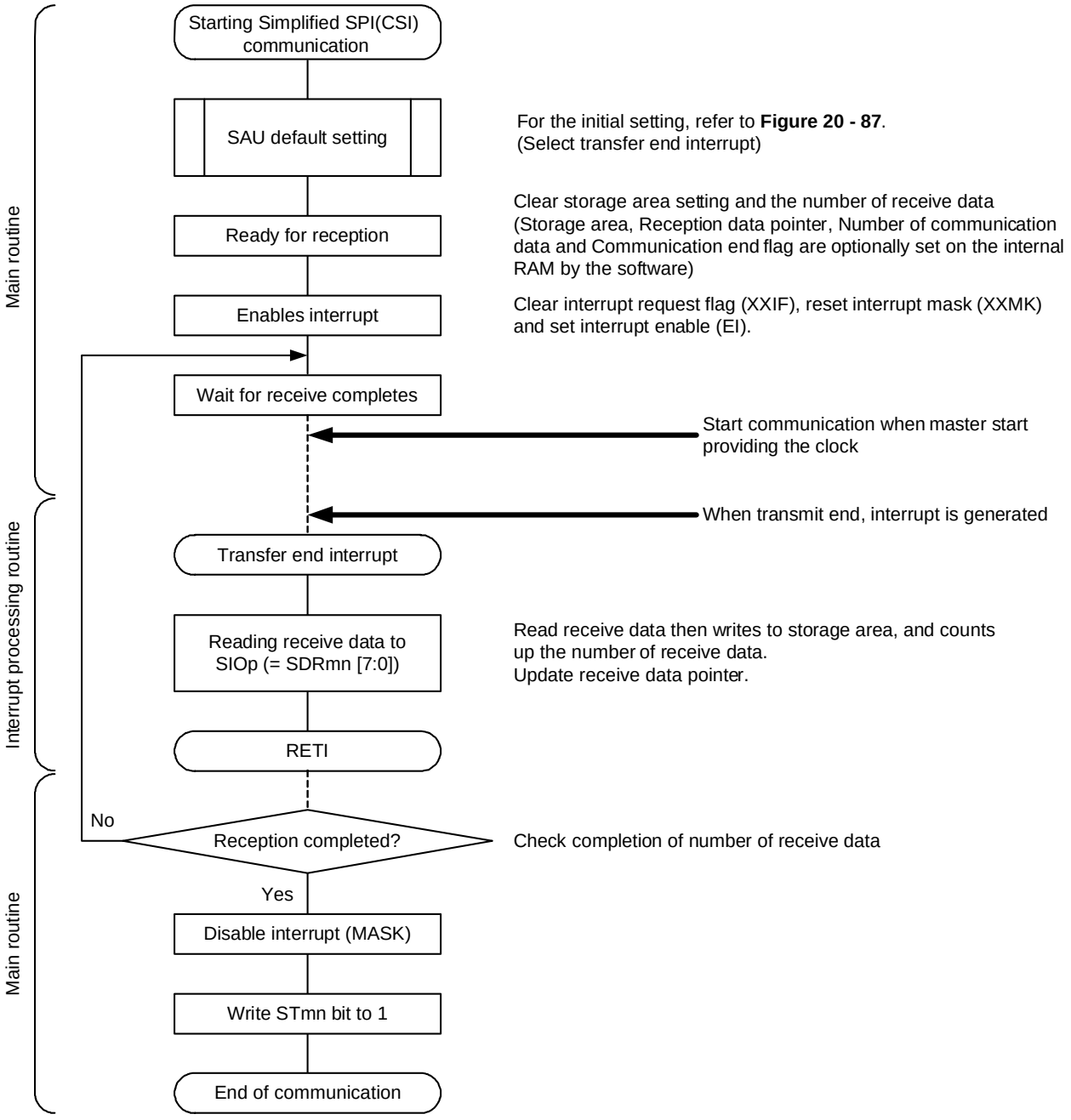
(3) Processing flow (in single-reception mode)

Figure 20 - 90 Timing Chart of Slave Reception (in Single-Reception Mode)
(Type 1: DAPmn = 0, CKPmn = 0)



Remark m: Unit number (m = 0), n: Channel number (n = 0), p: CSI number (p = 00)

Figure 20 - 91 Flowchart of Slave Reception (in Single-Reception Mode)



20.6.3 Slave transmission/reception

Slave transmission/reception is that the RL78 microcontroller transmits/receives data to/from another device in the state of a transfer clock being input from another device.

Slave Select Input Function	CSI00
Target channel	Channel 0 of SAU0
Pins used	SCK00, SI00, SO00, $\overline{\text{SSI00}}$
Interrupt	INTCSI00
	Transfer end interrupt (in single-transfer mode) or buffer empty interrupt (in continuous transfer mode) can be selected.
Error detection flag	Overrun error detection flag (OVFmn) only
Transfer data length	7 or 8 bits
Transfer rate	Max. f_{MCK}/6 [Hz] Notes 1, 2
Data phase	Selectable by the DAPmn bit of the SCRmn register • DAPmn = 0: Data I/O starts from the start of the operation of the serial clock. • DAPmn = 1: Data I/O starts half a clock before the start of the serial clock operation.
Clock phase	Selectable by the CKPmn bit of the SCRmn register • CKPmn = 0: Non-reverse • CKPmn = 1: Reverse
Data direction	MSB or LSB first
Slave select input function	Slave select input function operation selectable

Note 1. Because the external serial clock input to the SCK00 pin is sampled internally and used, the fastest transfer rate is f_{MCK}/6 [Hz].

Note 2. Use this operation within a range that satisfies the conditions above and the peripheral functions characteristics in the electrical specifications (see **CHAPTER 38** or **CHAPTER 39 ELECTRICAL SPECIFICATIONS**).

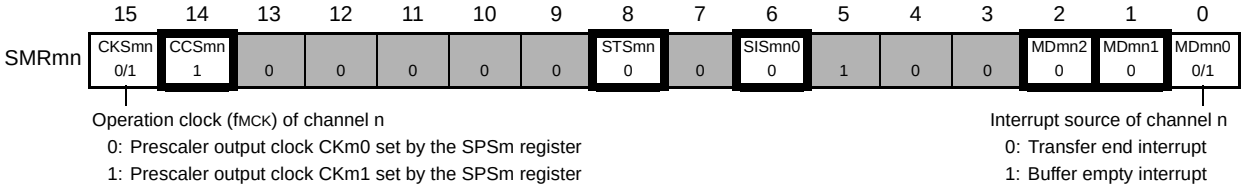
Remark 1. f_{MCK}: Operation clock frequency of target channel

Remark 2. m: Unit number (m = 0), n: Channel number (n = 0)

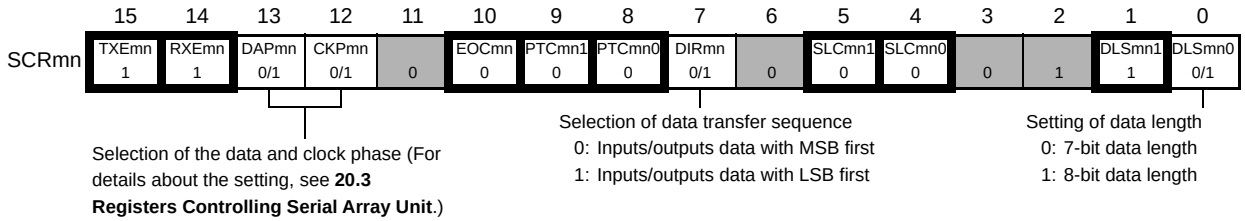
(1) Register setting

Figure 20 - 92 Example of Contents of Registers for Slave Transmission/Reception of Slave Select Input Function (CSI00) (1/2)

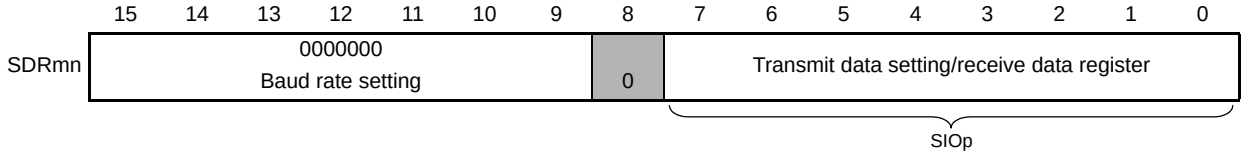
(a) Serial mode register mn (SMRmn)



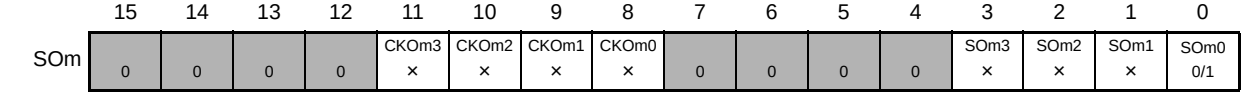
(b) Serial communication operation setting register mn (SCRmn)



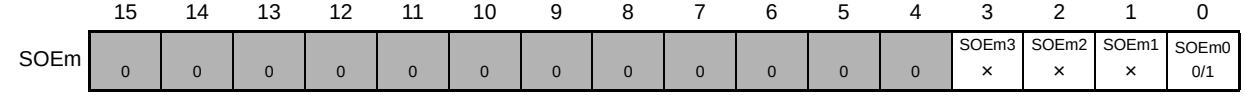
(c) Serial data register mn (SDRmn) (lower 8 bits: SIOp)



(d) Serial output register m (SOm)... Sets only the bits of the target channel.



(e) Serial output enable register m (SOEm)... Sets only the bits of the target channel to 1.



Caution Be sure to set transmit data to the SIOp register before the clock from the master is started.

Remark 1. m: Unit number (m = 0), n: Channel number (n = 0), p: CSI number (p = 00)

Remark 2. ■: Setting is fixed in the Simplified SPI(CSI) slave transmission/reception mode

▒: Setting disabled (set to the initial value)

×: Bit that cannot be used in this mode (set to the initial value when not used in any mode)

0/1: Set to 0 or 1 depending on the usage of the user

Figure 20 - 92 Example of Contents of Registers for Slave Transmission/Reception of Slave Select Input Function (CSI00) (2/2)

(f) Serial channel start register m (SSm)... Sets only the bits of the target channel to 1.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SSm	0	0	0	0	0	0	0	0	0	0	0	0	SSm3 ×	SSm2 ×	SSm1 ×	SSm0 0/1

(g) Input switch control register (ISC)... $\overline{\text{SSI00}}$ input setting in CSI00 slave channel (channel 0 of unit 0).

	7	6	5	4	3	2	1	0
ISC	SSIE00 0/1	0	0	0	0	0	ISC1 0/1	ISC0 0/1

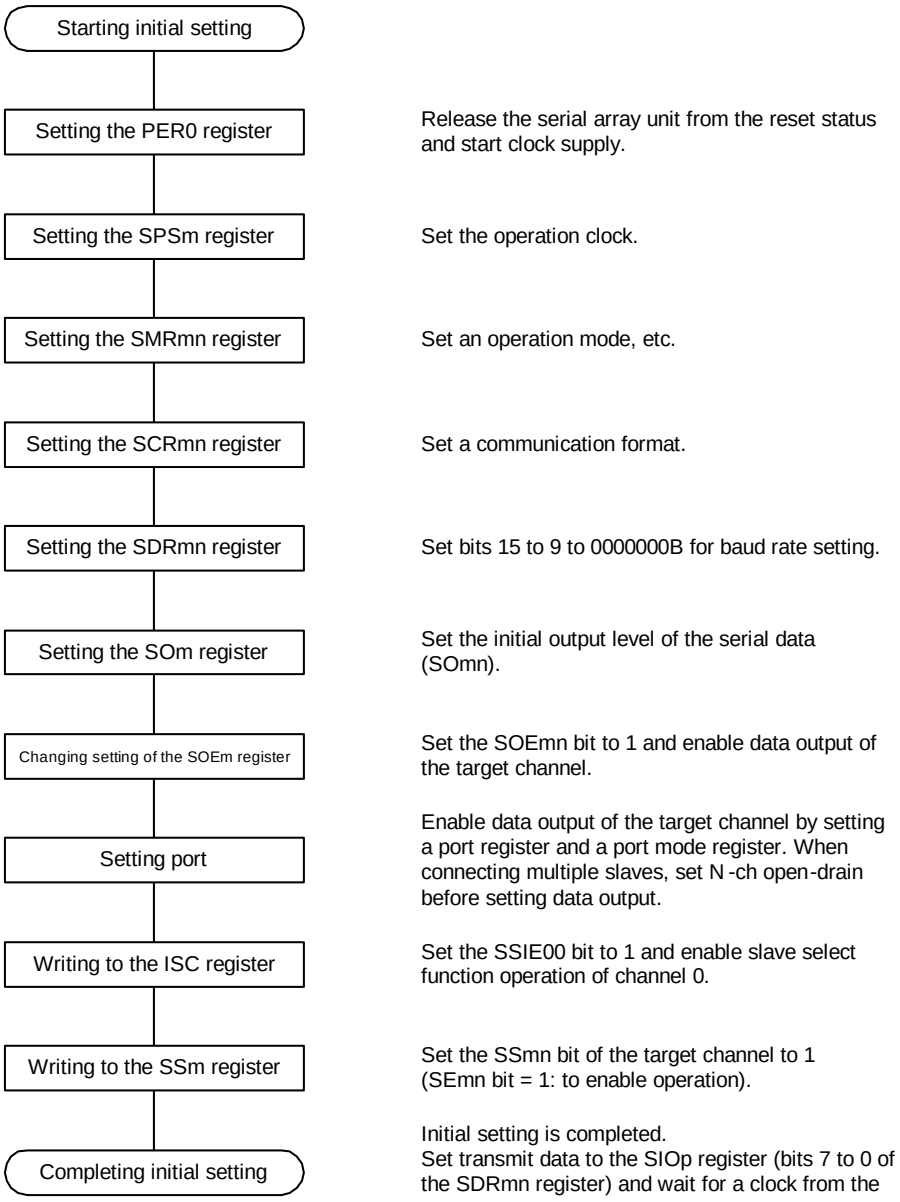
0: Disables the input value of the $\overline{\text{SSI00}}$ pin
1: Enables the input value of the $\overline{\text{SSI00}}$ pin

Remark 1. m: Unit number (m = 0), n: Channel number (n = 0), p: CSI number (p = 00)

Remark 2. ■: Setting disabled (set to the initial value)
×: Bit that cannot be used in this mode (set to the initial value when not used in any mode)
0/1: Set to 0 or 1 depending on the usage of the user

(2) Operation procedure

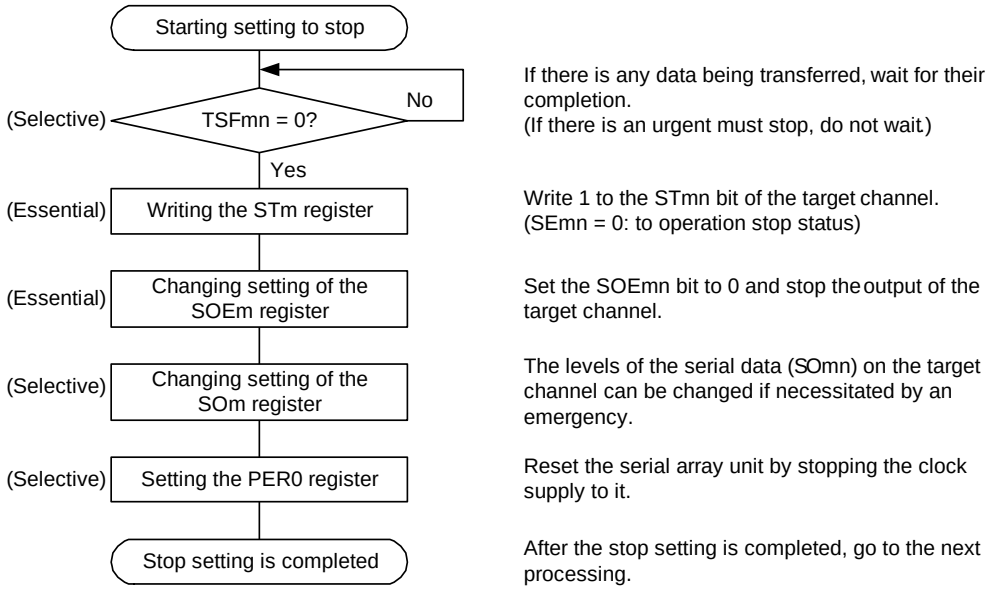
Figure 20 - 93 Initial Setting Procedure for Slave Transmission/Reception



Caution Be sure to set transmit data to the SIOp register before the clock from the master is started.

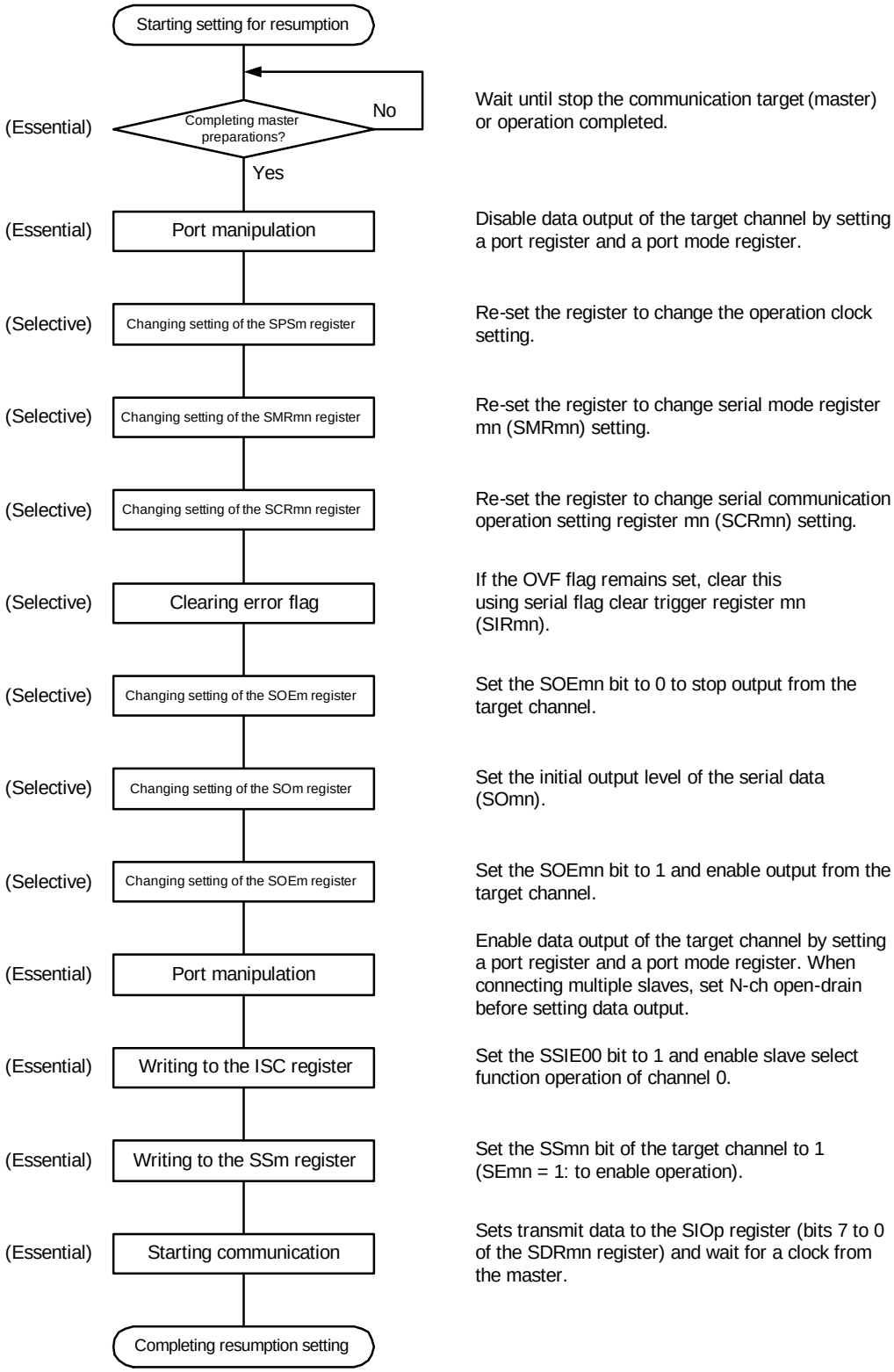
Remark m: Unit number (m = 0), n: Channel number (n = 0), p: CSI number (p = 00)

Figure 20 - 94 Procedure for Stopping Slave Transmission/Reception



Remark m: Unit number (m = 0), n: Channel number (n = 0), p: CSI number (p = 00)

Figure 20 - 95 Procedure for Resuming Slave Transmission/Reception

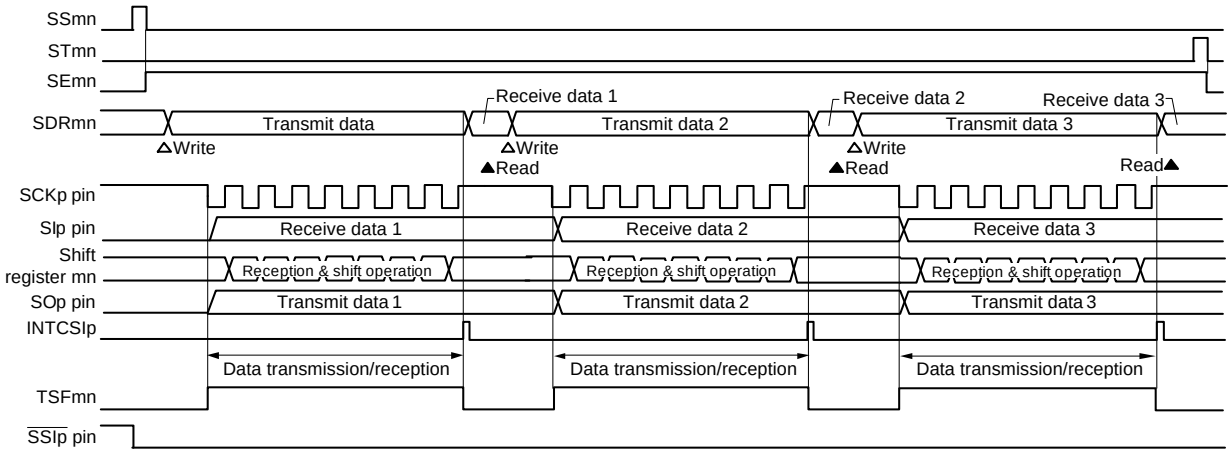


Caution 1. Be sure to set transmit data to the SIOp register before the clock from the master is started.

Caution 2. If PER0 is rewritten while stopping the master transmission and the clock supply is stopped, wait until the transmission target (master) stops or transmission finishes, and then perform initialization instead of restarting the transmission.

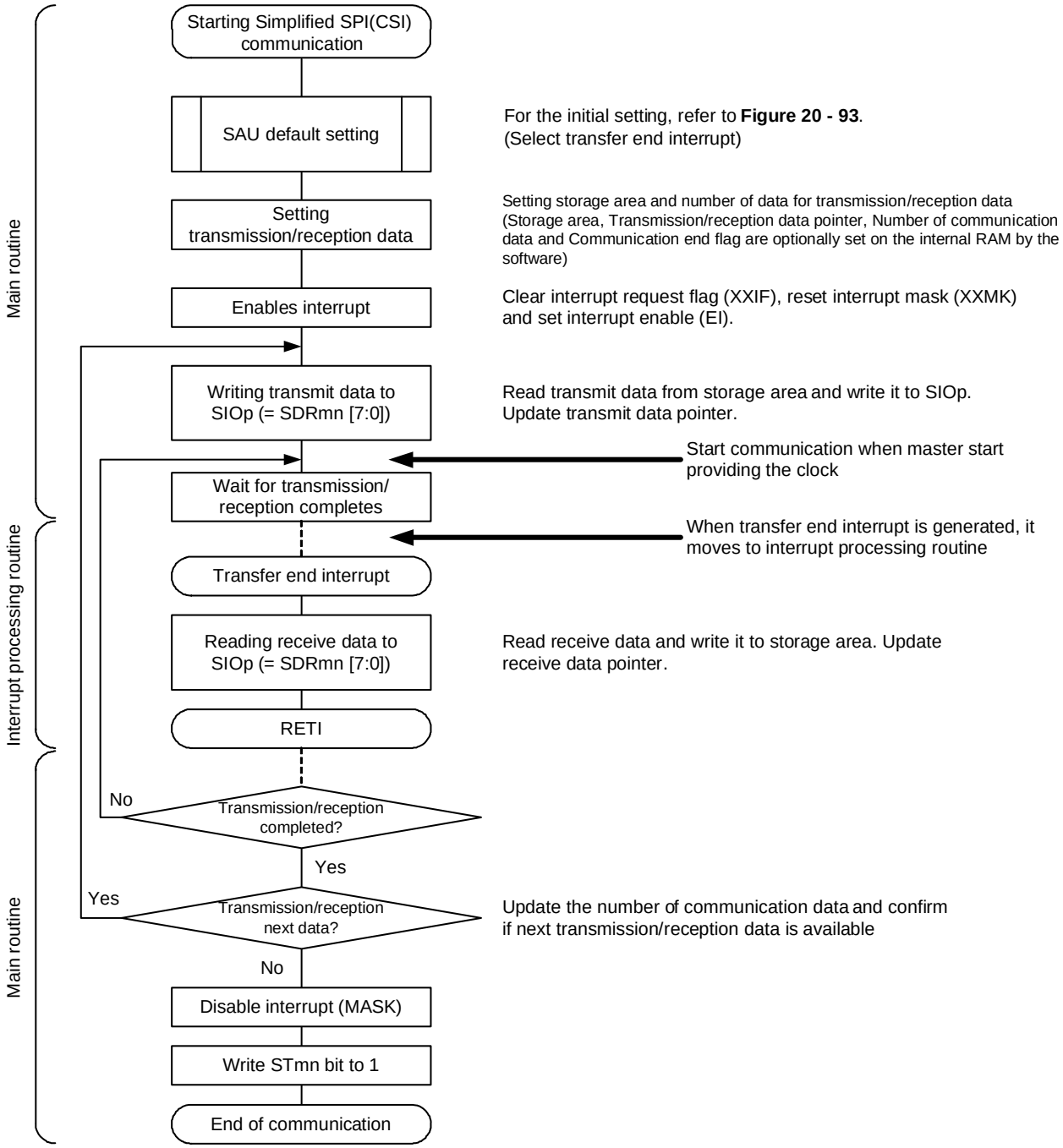
(3) Processing flow (in single-transmission/reception mode)

Figure 20 - 96 Timing Chart of Slave Transmission/Reception (in Single-Transmission/Reception Mode) (Type 1: DAPmn = 0, CKPmn = 0)



Remark m: Unit number (m = 0), n: Channel number (n = 0), p: CSI number (p = 00)

Figure 20 - 97 Flowchart of Slave Transmission/Reception (in Single- Transmission/Reception Mode)

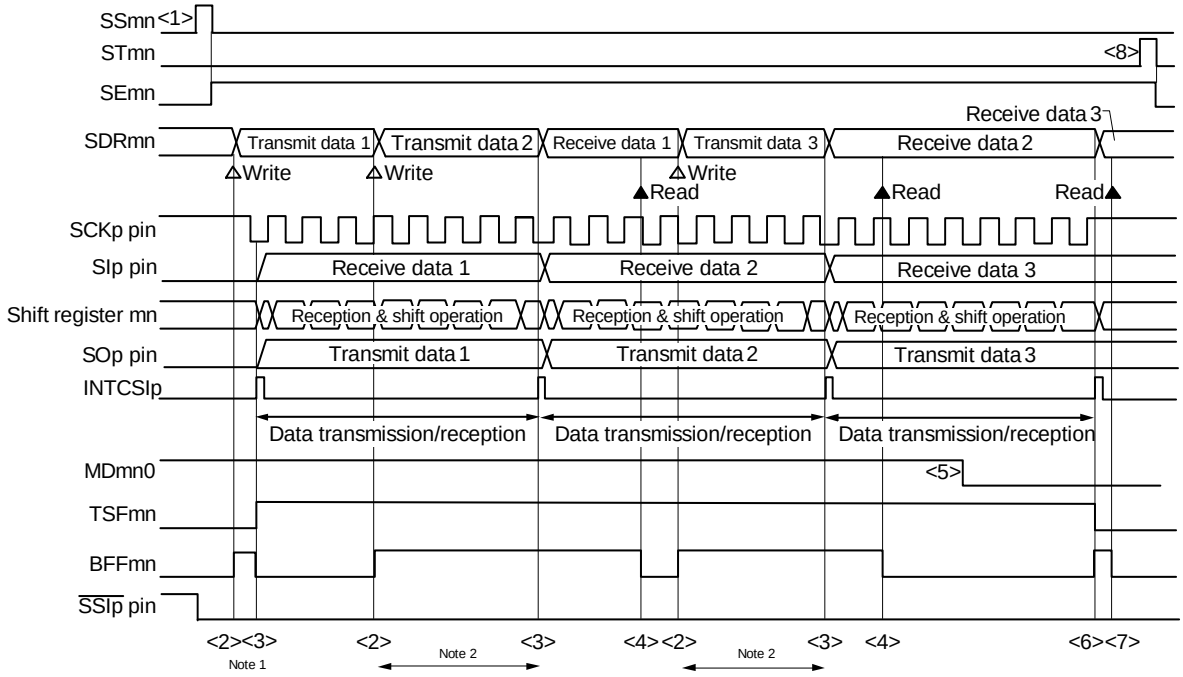


Caution **Be sure to set transmit data to the SIOp register before the clock from the master is started.**

Remark m: Unit number (m = 0), n: Channel number (n = 0), p: CSI number (p = 00)

(4) Processing flow (in continuous transmission/reception mode)

Figure 20 - 98 Timing Chart of Slave Transmission/Reception (in Continuous Transmission/Reception Mode) (Type 1: DAPmn = 0, CKPmn = 0)



Note 1. If transmit data is written to the SDRmn register while the BFFmn bit of serial status register mn (SSRmn) is 1 (valid data is stored in serial data register mn (SDRmn)), the transmit data is overwritten.

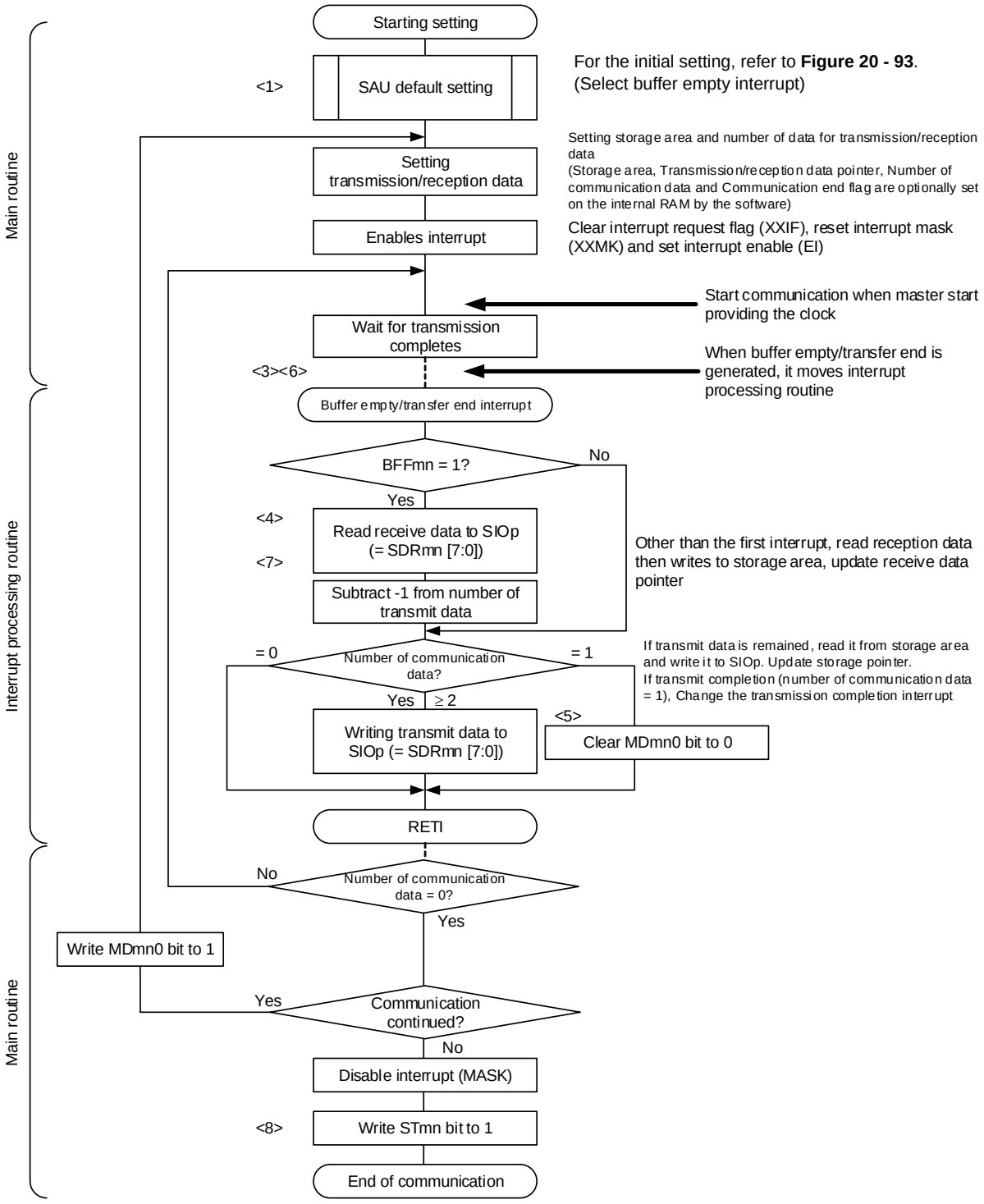
Note 2. The transmit data can be read by reading the SDRmn register during this period. At this time, the transfer operation is not affected.

Caution The MDmn0 bit of serial mode register mn (SMRmn) can be rewritten even during operation. However, rewrite it before transfer of the last bit is started, so that it has been rewritten before the transfer end interrupt of the last transmit data.

Remark 1. <1> to <8> in the figure correspond to <1> to <8> in **Figure 20 - 99 Flowchart of Slave Transmission/Reception (in Continuous Transmission/Reception Mode)**.

Remark 2. m: Unit number (m = 0), n: Channel number (n = 0), p: CSI number (p = 00)

Figure 20 - 99 Flowchart of Slave Transmission/Reception (in Continuous Transmission/Reception Mode)



Caution Be sure to set transmit data to the SIOp register before the clock from the master is started.

Remark 1. <1> to <8> in the figure correspond to <1> to <8> in **Figure 20 - 98 Timing Chart of Slave Transmission/Reception (in Continuous Transmission/Reception Mode) (Type 1: DAPmn = 0, CKPmn = 0)**.

Remark 2. m: Unit number (m = 0), n: Channel number (n = 0), p: CSI number (p = 00)

20.6.4 Calculating transfer clock frequency

The transfer clock frequency for slave select input function (CSI00) communication can be calculated by the following expressions.

(1) Slave

(Transfer clock frequency) = {Frequency of serial clock (SCK) supplied by master} Note [Hz]

Note The permissible maximum transfer clock frequency is f_{MCK}/6.

Remark m: Unit number (m = 0), n: Channel number (n = 0), p: CSI number (p = 00)

Table 20 - 3 Selection of Operation Clock For Slave Select Input Function

SMRmn Register	SPSm Register								Operation Clock (f_{MCK}) Note	
CKSmn	PRS m13	PRS m12	PRS m11	PRS m10	PRS m03	PRS m02	PRS m01	PRS m00		f_{CLK} = 24 MHz
0	×	×	×	×	0	0	0	0	f_{CLK}	24 MHz
	×	×	×	×	0	0	0	1	$f_{CLK}/2$	12 MHz
	×	×	×	×	0	0	1	0	$f_{CLK}/2^2$	6 MHz
	×	×	×	×	0	0	1	1	$f_{CLK}/2^3$	3 MHz
	×	×	×	×	0	1	0	0	$f_{CLK}/2^4$	1.5 MHz
	×	×	×	×	0	1	0	1	$f_{CLK}/2^5$	750 kHz
	×	×	×	×	0	1	1	0	$f_{CLK}/2^6$	375 kHz
	×	×	×	×	0	1	1	1	$f_{CLK}/2^7$	187.5 kHz
	×	×	×	×	1	0	0	0	$f_{CLK}/2^8$	93.8 kHz
	×	×	×	×	1	0	0	1	$f_{CLK}/2^9$	46.9 kHz
	×	×	×	×	1	0	1	0	$f_{CLK}/2^{10}$	23.4 kHz
	×	×	×	×	1	0	1	1	$f_{CLK}/2^{11}$	11.7 kHz
	×	×	×	×	1	1	0	0	$f_{CLK}/2^{12}$	5.86 kHz
	×	×	×	×	1	1	0	1	$f_{CLK}/2^{13}$	2.93 kHz
	×	×	×	×	1	1	1	0	$f_{CLK}/2^{14}$	1.46 kHz
	×	×	×	×	1	1	1	1	$f_{CLK}/2^{15}$	732 Hz

Note When changing the clock selected for f_{CLK} (by changing the system clock control register (CKC) value), do so after having stopped (serial channel stop register m (STm) = 000FH) the operation of the serial array unit (SAU).

Remark 1. ×: Don't care

Remark 2. m: Unit number (m = 0), n: Channel number (n = 0)

20.6.5 Procedure for processing errors that occurred during slave select input function communication

The procedure for processing errors that occurred during slave select input function communication is described in **Figure 20 - 100**.

Figure 20 - 100 Processing Procedure in Case of Overrun Error

Software Manipulation	Hardware Status	Remark
Reads serial data register mn (SDRmn). →	The BFFmn bit of the SSRmn register is set to 0 and channel n is enabled to receive data.	This is to prevent an overrun error if the next reception is completed during error processing.
Reads serial status register mn (SSRmn).		Error type is identified and the read value is used to clear error flag.
Writes 1 to serial flag clear trigger register mn (SIRmn). →	Error flag is cleared.	Error can be cleared only during reading, by writing the value read from the SSRmn register to the SIRmn register without modification.

Remark m: Unit number (m = 0), n: Channel number (n = 0)

20.7 Operation of UART (UART0 to UART2) Communication

This is a start-stop synchronization function using two lines: serial/data transmission (TxD) and serial/data reception (RxD) lines. By using these two communication lines, each data frame, which consist of a start bit, data, parity bit, and stop bit, is transferred asynchronously (using the internal baud rate) between the microcontroller and the other communication party. Full-duplex asynchronous communication UART communication can be performed by using a channel dedicated to transmission (even-numbered channel) and a channel dedicated to reception (odd-numbered channel). The LIN-bus can be implemented by using UART0 and timer array unit 0 (channel 7) with an external interrupt (INTP0).

[Data transmission/reception]
- Data length of 7, 8, or 9 bits Note
- Select the MSB/LSB first
- Level setting of transmit/receive data (selecting whether to reverse the level)
- Parity bit appending and parity check functions
- Stop bit appending, stop bit check function

[Interrupt function]
- Transfer end interrupt/buffer empty interrupt
- Error interrupt in case of framing error, parity error, or overrun error

[Error detection flag]
- Framing error, parity error, or overrun error

In addition, UART0 and UART2 reception support the SNOOZE mode. When RxD pin input is detected while in the STOP mode, the SNOOZE mode makes data reception that does not require the CPU possible. Only UART0, UART2 can be specified for the reception baud rate adjustment function.

The LIN-bus is accepted in UART0 (channels 0 and 1 of unit 0).

[LIN-bus functions]
- Wakeup signal detection
- Break field (BF) detection
- Sync field measurement, baud rate calculation

} Using the external interrupt (INTP0) and timer array unit 0 (channel 7)

Note Only UART0 can be specified for the 9-bit data length.

UART0 uses channels 0 and 1 of SAU0.
UART1 uses channels 2 and 3 of SAU0.
UART2 uses channels 0 and 1 of SAU1.

Unit	Channel	Used as Simplified SPI(CSI)	Used as UART	Used as Simplified I^2C
0	0	CSI00	UART0 (supporting LIN-bus)	IIC00
	1	—		—
	2	CSI10	UART1	IIC10
	3	—		—
1	0	CSI20	UART2	IIC20
	1	—		—

Select any function for each channel. Only the selected function is possible. If UART0 is selected for channels 0 and 1 of unit 0, for example, these channels cannot be used for CSI00. At this time, however, channel 2 or 3 of the same unit can be used for a function other than UART0, such as CSI10, UART1, and IIC10.

Caution When using a serial array unit for UART, both the transmitter side (even-numbered channel) and the receiver side (odd-numbered channel) can only be used for UART.

UART performs the following four types of communication operations.

- UART transmission (See **20.7.1**.)
- UART reception (See **20.7.2**.)
- LIN transmission (UART0 only) (See **20.8.1**.)
- LIN reception (UART0 only) (See **20.8.2**.)

20.7.1 UART transmission

UART transmission is an operation to transmit data from the RL78 microcontroller to another device asynchronously (start-stop synchronization).

Of two channels used for UART, the even channel is used for UART transmission.

UART	UART0	UART1	UART2
Target channel	Channel 0 of SAU0	Channel 2 of SAU0	Channel 0 of SAU1
Pins used	TxD0	TxD1	TxD2
Interrupt	INTST0	INTST1	INTST2
	Transfer end interrupt (in single-transfer mode) or buffer empty interrupt (in continuous transfer mode) can be selected.		
Error detection flag	None		
Transfer data length	7, 8, or 9 bits Note 1		
Transfer rate Note 2	Max. f_{MCK}/6 [bps] (SDRmn [15:9] = 2 or more), Min. $f_{CLK}/(2 \times 2^{15} \times 128)$ [bps]		
Data phase	Non-reverse output (default: high level) Reverse output (default: low level)		
Parity bit	The following selectable • No parity bit • Appending 0 parity • Appending even parity • Appending odd parity		
Stop bit	The following selectable • Appending 1 bit • Appending 2 bits		
Data direction	MSB or LSB first		

Note 1. Only UART0, UART2 can be specified for the 9-bit data length.

Note 2. Use this operation within a range that satisfies the conditions above and the peripheral functions characteristics in the electrical specifications (see **CHAPTER 38** or **CHAPTER 39 ELECTRICAL SPECIFICATIONS**).

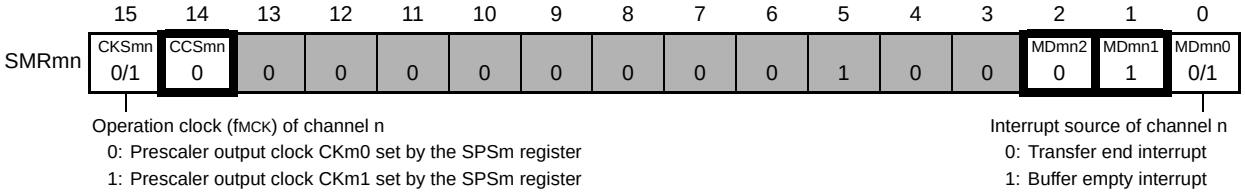
Remark 1. f_{MCK}: Operation clock frequency of target channel
f_{CLK}: System clock frequency

Remark 2. m: Unit number (m = 0, 1), n: Channel number (n = 0, 2), mn = 00, 02, 10

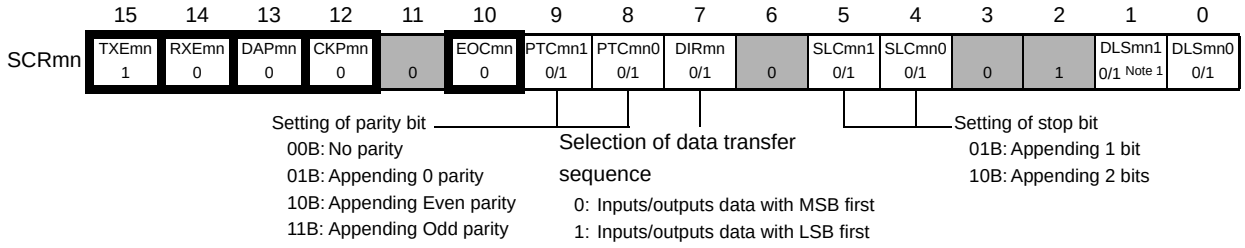
(1) Register setting

Figure 20 - 101 Example of Contents of Registers for UART Transmission of UART (UART0 to UART2) (1/2)

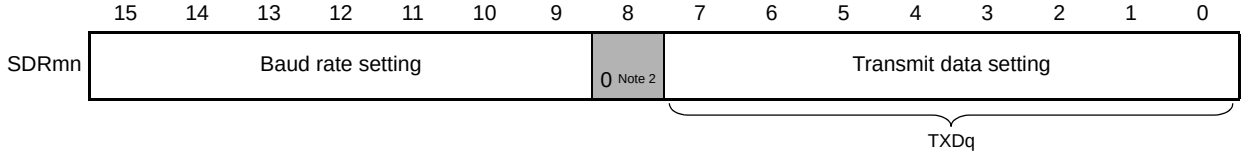
(a) Serial mode register mn (SMRmn)



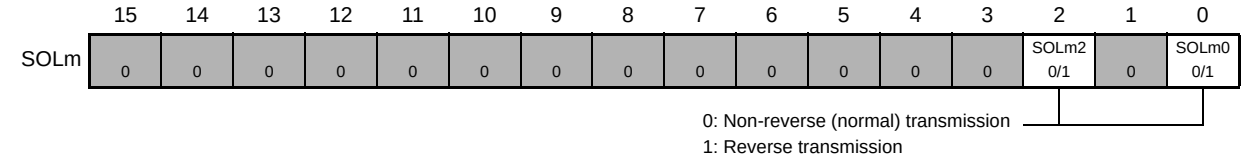
(b) Serial communication operation setting register mn (SCRmn)



(c) Serial data register mn (SDRmn) (lower 8 bits: TXDq)



(d) Serial output level register m (SOLm)... Sets only the bits of the target channel.



Note 1. Only provided for the SCR00 and SCR01 registers. This bit is fixed to 1 for the other registers.

Note 2. When UART0 performs 9-bit communication (by setting the DLS001 and DLS000 bits of the SCR00 register to 1), bits 0 to 8 of the SDR00 register are used as the transmission data specification area. Only UART0 can be specified for the 9-bit data length.

Remark 1. m: Unit number (m = 0, 1), n: Channel number (n = 0, 2), q: UART number (q = 0 to 2), mn = 00, 02, 10

Remark 2. ■: Setting is fixed in the UART transmission mode,
▒: Setting disabled (set to the initial value)
0/1: Set to 0 or 1 depending on the usage of the user

Figure 20 - 101 Example of Contents of Registers for UART Transmission of UART (UART0 to UART2) (2/2)

(e) Serial output register m (SOm)... Sets only the bits of the target channel.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SOm	0	0	0	0	1	CKOm2 Note 2 ×	1	CKOm0 Note 2 ×	0	0	0	0	1	SOm2 0/1 Note 1	1	SOm0 0/1 Note 1

0: Serial data output value is “0”
1: Serial data output value is “1”

(f) Serial output enable register m (SOEm)... Sets only the bits of the target channel to 1.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SOEm	0	0	0	0	0	0	0	0	0	0	0	0	0	SOEm2 0/1	0	SOEm0 0/1

(g) Serial channel start register m (SSm)... Sets only the bits of the target channel to 1.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SSm	0	0	0	0	0	0	0	0	0	0	0	0	SSm3 ×	SSm2 0/1	SSm1 ×	SSm0 0/1

Note 1. Before transmission is started, be sure to set to 1 when the SOLmn bit of the target channel is set to 0, and set to 0 when the SOLmn bit of the target channel is set to 1. The value varies depending on the communication data during communication operation.

Note 2. Serial array unit 0 only.

Remark 1. m: Unit number (m = 0, 1), n: Channel number (n = 0, 2), mn = 00, 02, 10

Remark 2. : Setting disabled (set to the initial value)
×: Bit that cannot be used in this mode (set to the initial value when not used in any mode)
0/1: Set to 0 or 1 depending on the usage of the user

(2) Operation procedure

Figure 20 - 102 Initial Setting Procedure for UART Transmission

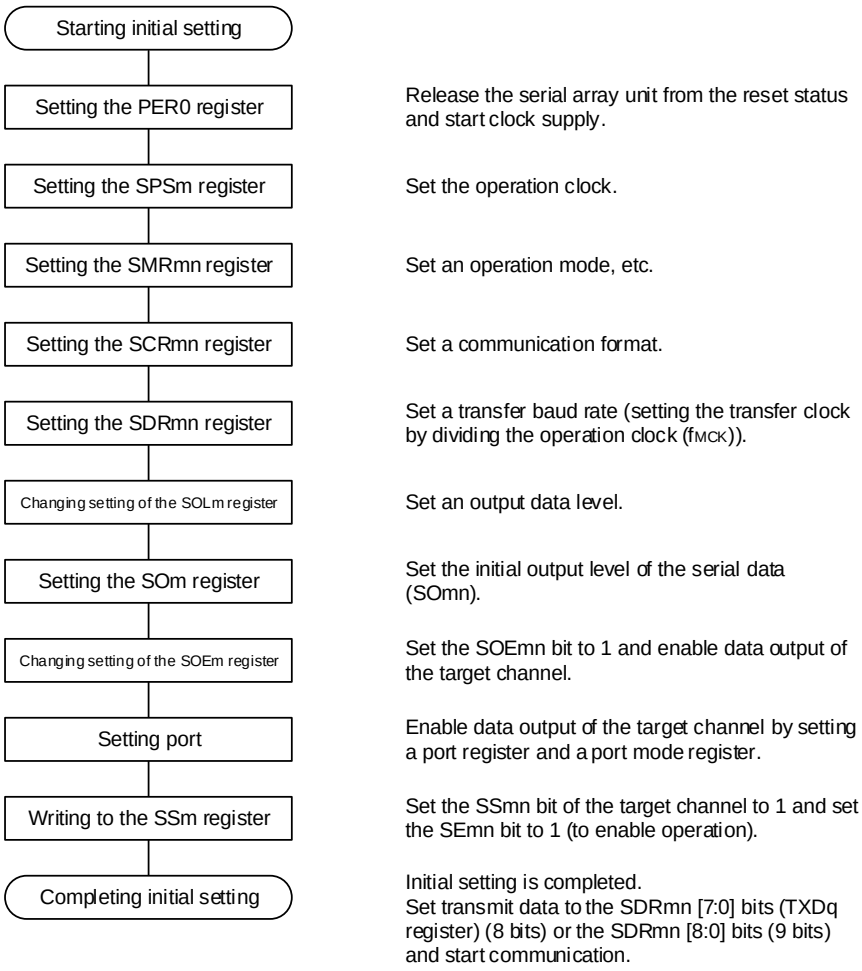


Figure 20 - 103 Procedure for Stopping UART Transmission

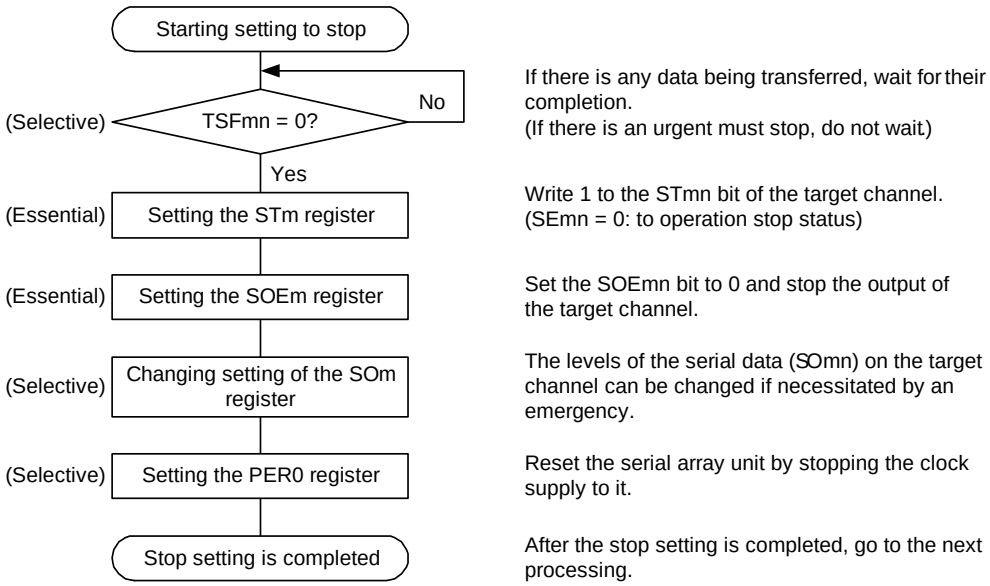
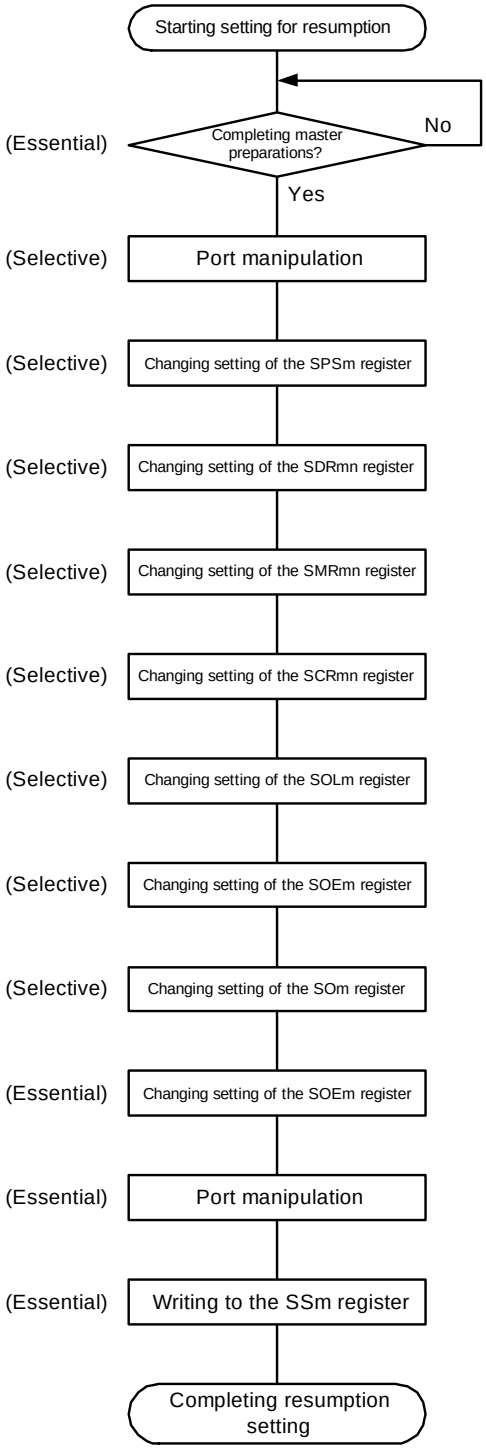


Figure 20 - 104 Procedure for Resuming UART Transmission



Wait until stop the communication target or communication operation completed

Disable data output of the target channel by setting a port register and a port mode register.

Re-set the register to change the operation clock setting.

Re-set the register to change the transfer baud rate setting (setting the transfer clock by dividing the operation clock (f_{MCK})).

Re-set the register to change serial mode register mn (SMRmn) setting.

Re-set the register to change the serial communication operation setting register mn (SCRmn) setting.

Re-set the register to change serial output level register m (SOLm) setting.

Clear the SOEmn bit to 0 and stop output.

Set the initial output level of the serial data (SOmn).

Set the SOEmn bit to 1 and enable output.

Enable data output of the target channel by setting a port register and a port mode register.

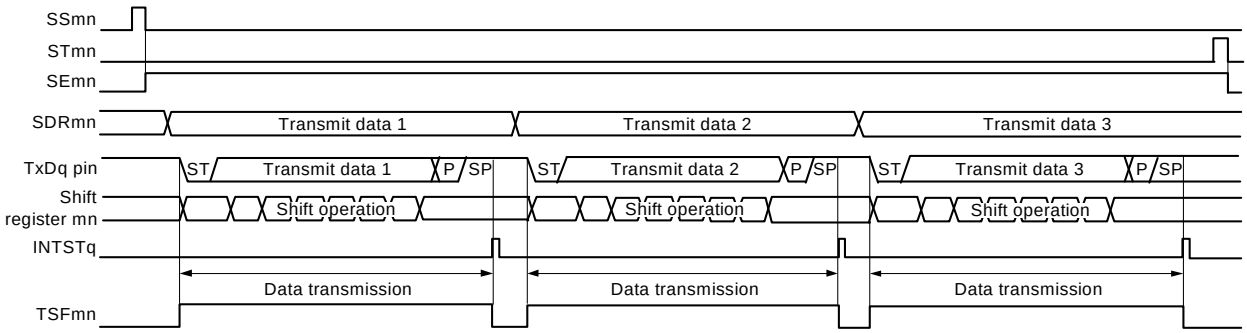
Set the SSmn bit of the target channel to 1 and set the SEmn bit to 1 (to enable operation).

Initial setting is completed.
Set transmit data to the SDRmn [7:0] bits (TXDq register) (8 bits) or the SDRmn [8:0] bits (9 bits) and start communication.

Remark If PER0 is rewritten while stopping the master transmission and the clock supply is stopped, wait until the transmission target stops or transmission finishes, and then perform initialization instead of restarting the transmission.

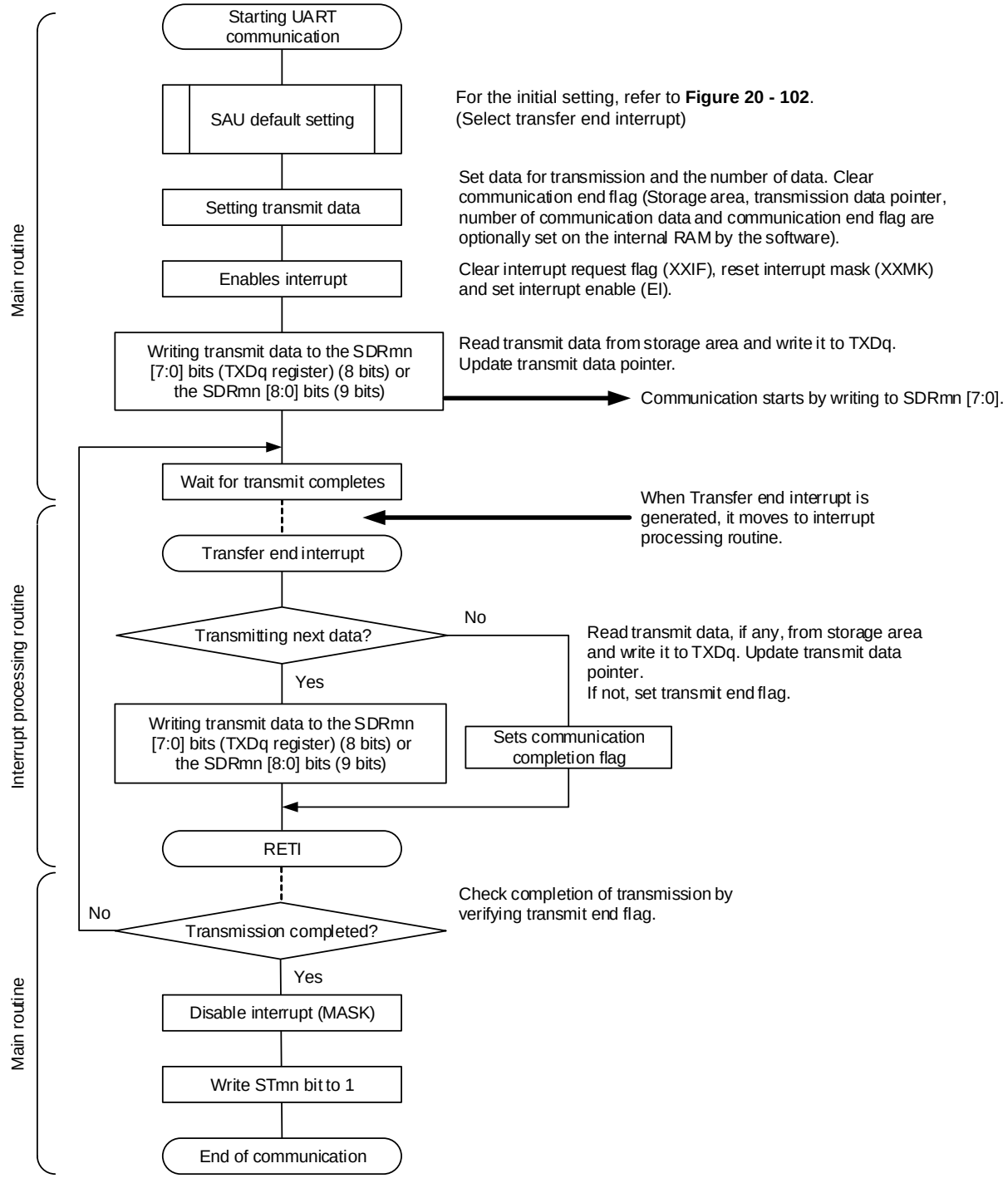
(3) Processing flow (in single-transmission mode)

Figure 20 - 105 Timing Chart of UART Transmission (in Single-Transmission Mode)



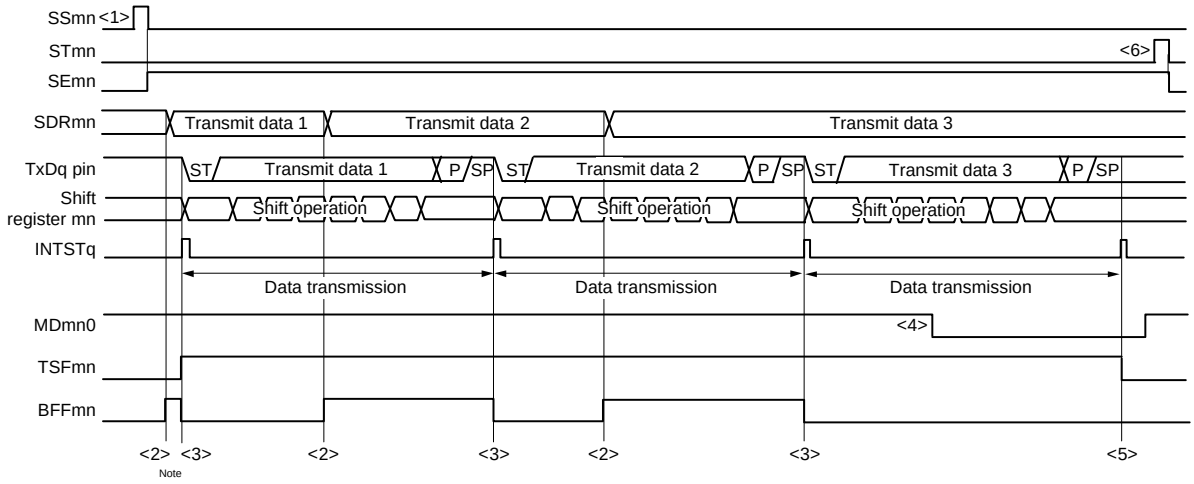
Remark m: Unit number (m = 0, 1), n: Channel number (n = 0, 2), q: UART number (q = 0 to 2)
mn = 00, 02, 10

Figure 20 - 106 Flowchart of UART Transmission (in Single-Transmission Mode)



(4) Processing flow (in continuous transmission mode)

Figure 20 - 107 Timing Chart of UART Transmission (in Continuous Transmission Mode)

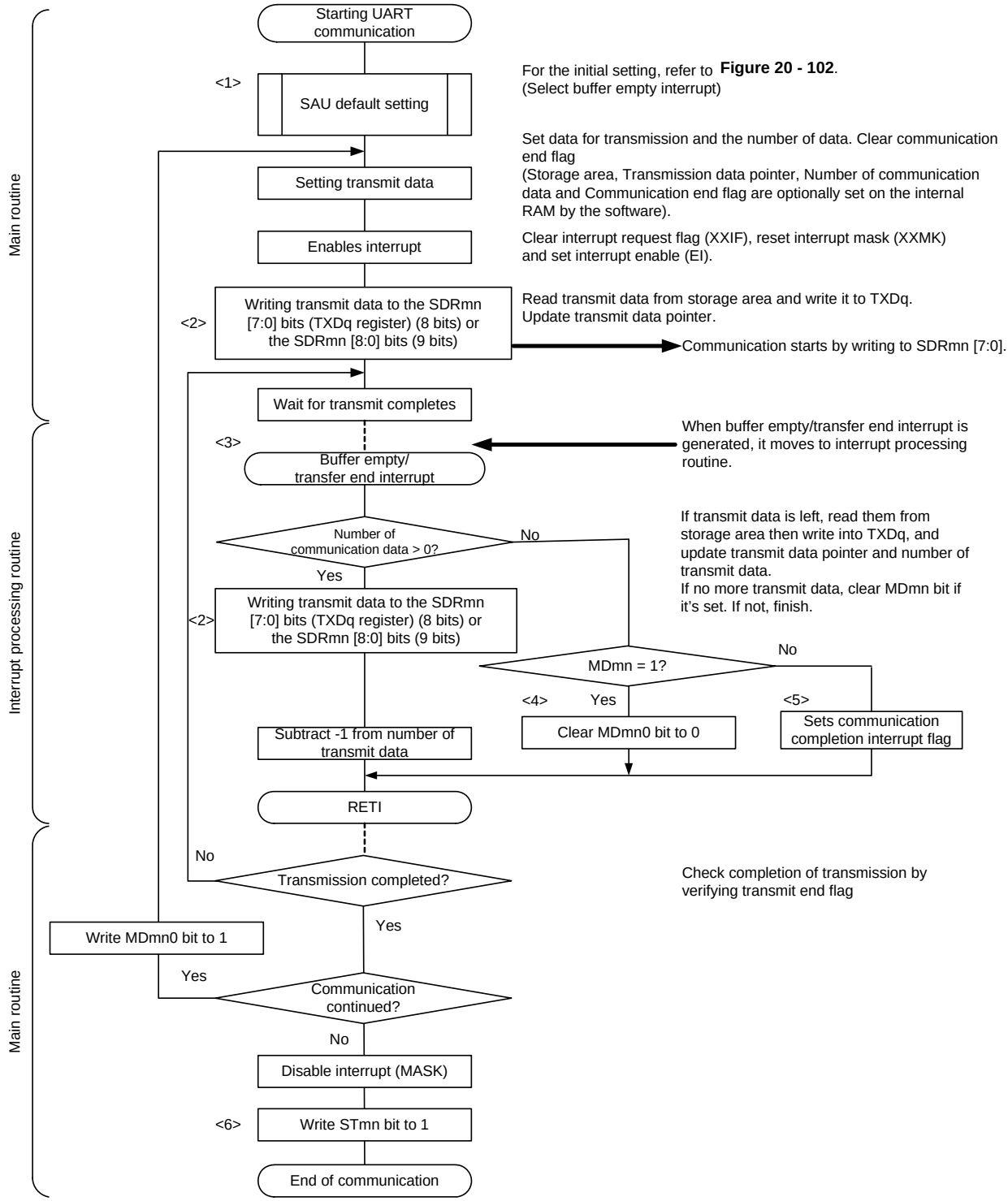


Note If transmit data is written to the SDRmn register while the BFFmn bit of serial status register mn (SSRmn) is 1 (valid data is stored in serial data register mn (SDRmn)), the transmit data is overwritten.

Caution **The MDmn0 bit of serial mode register mn (SMRmn) can be rewritten even during operation. However, rewrite it before transfer of the last bit is started, so that it will be rewritten before the transfer end interrupt of the last transmit data.**

Remark m: Unit number (m = 0, 1), n: Channel number (n = 0, 2), q: UART number (q = 0 to 2)
mn = 00, 02, 10

Figure 20 - 108 Flowchart of UART Transmission (in Continuous Transmission Mode)



Remark <1> to <6> in the figure correspond to <1> to <6> in **Figure 20 - 107 Timing Chart of UART Transmission (in Continuous Transmission Mode)**.

20.7.2 UART reception

UART reception is an operation wherein the RL78 microcontroller asynchronously receives data from another device (start-stop synchronization).

For UART reception, the odd-number channel of the two channels used for UART is used. The SMR register of both the odd- and even-numbered channels must be set.

UART	UART0	UART1	UART2
Target channel	Channel 1 of SAU0	Channel 3 of SAU0	Channel 1 of SAU1
Pins used	RxD0	RxD1	RxD2
Interrupt	INTST0	INTST1	INTST2
	Transfer end interrupt only (Setting the buffer empty interrupt is prohibited.)		
Error interrupt	INTSRE0	INTSRE1	INTSRE2
Error detection flag	• Framing error detection flag (FEFmn) • Parity error detection flag (PEFmn) • Overrun error detection flag (OVFmn)		
Transfer data length	7, 8 or 9 bits Note 1		
Transfer rate Note 2	Max. f_{MCK}/6 [bps] (SDRmn [15:9] = 2 or more), Min. $f_{CLK}/(2 \times 2^{15} \times 128)$ [bps]		
Data phase	Non-reverse output (default: high level) Reverse output (default: low level)		
Parity bit	The following selectable • No parity bit (no parity check) • No parity judgment (0 parity) • Even parity check • Odd parity check		
Stop bit	Appending 1 bit		
Data direction	MSB or LSB first		

Note 1. Only UART0, UART2 can be specified for the 8-bit data length.

Note 2. Use this operation within a range that satisfies the conditions above and the peripheral functions characteristics in the electrical specifications (see **CHAPTER 38** or **CHAPTER 39 ELECTRICAL SPECIFICATIONS**).

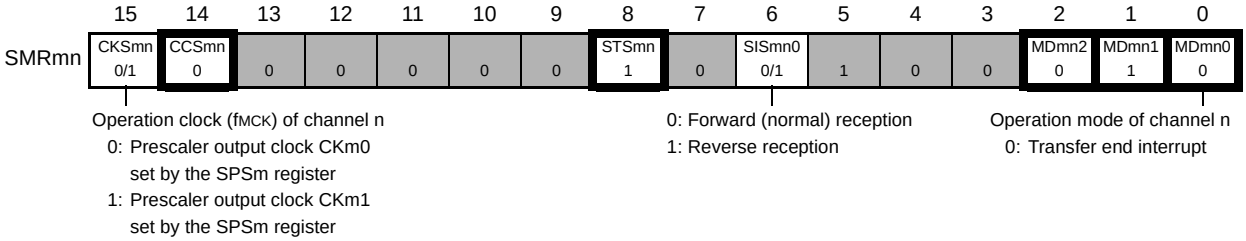
Remark 1. f_{MCK}: Operation clock frequency of target channel
f_{CLK}: System clock frequency

Remark 2. m: Unit number (m = 0, 1), n: Channel number (n = 1, 3), mn = 01, 03, 11

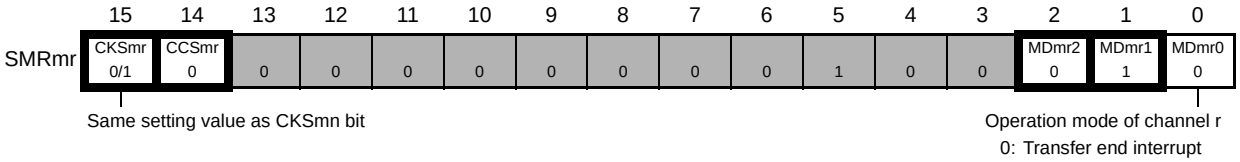
(1) Register setting

Figure 20 - 109 Example of Contents of Registers for UART Reception of UART (UART0 to UART2) (1/2)

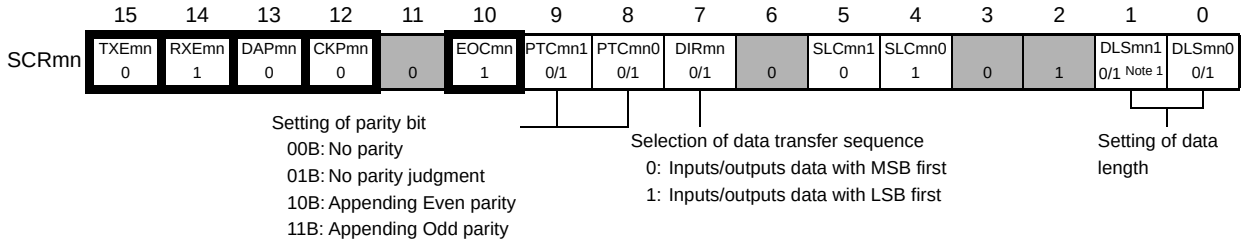
(a) Serial mode register mn (SMRmn)



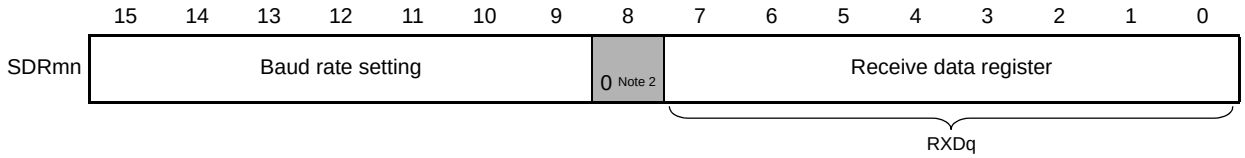
(b) Serial mode register mr (SMRmr)



(c) Serial communication operation setting register mn (SCRmn)



(d) Serial data register mn (SDRmn) (lower 8 bits: RXDq)



Note 1. Only provided for the SCR00 and SCR01 registers. This bit is fixed to 1 for the other registers.

Note 2. When UART performs 9-bit communication, bits 0 to 8 of the SDRm1 register are used as the reception data specification area. Only UART0 can be specified for the 8-bit data length.

Caution For the UART reception, be sure to set the SMRmr register of channel r to UART transmission mode that is to be paired with channel n.

Remark 1. m: Unit number (m = 0, 1), n: Channel number (n = 1, 3), mn = 01, 03, 11
r: Channel number (r = n - 1), q: UART number (q = 0 to 2)

Remark 2. ■: Setting is fixed in the UART reception mode,
■: Setting disabled (set to the initial value)
0/1: Set to 0 or 1 depending on the usage of the user

Figure 20 - 109 Example of Contents of Registers for UART Reception of UART (UART0 to UART2) (2/2)

(e) Serial output register m (SOm)... The register that not used in this mode.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SOm	0	0	0	0	1	CKOm2 Note ×	1	CKOm0 Note ×	0	0	0	0	1	SOm2 ×	1	SOm0 ×

(f) Serial output enable register m (SOEm)... The register that not used in this mode.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SOEm	0	0	0	0	0	0	0	0	0	0	0	0	0	SOEm2 ×	0	SOEm0 ×

(g) Serial channel start register m (SSm)... Sets only the bits of the target channel is 1.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SSm	0	0	0	0	0	0	0	0	0	0	0	0	SSm3 0/1	SSm2 ×	SSm1 0/1	SSm0 ×

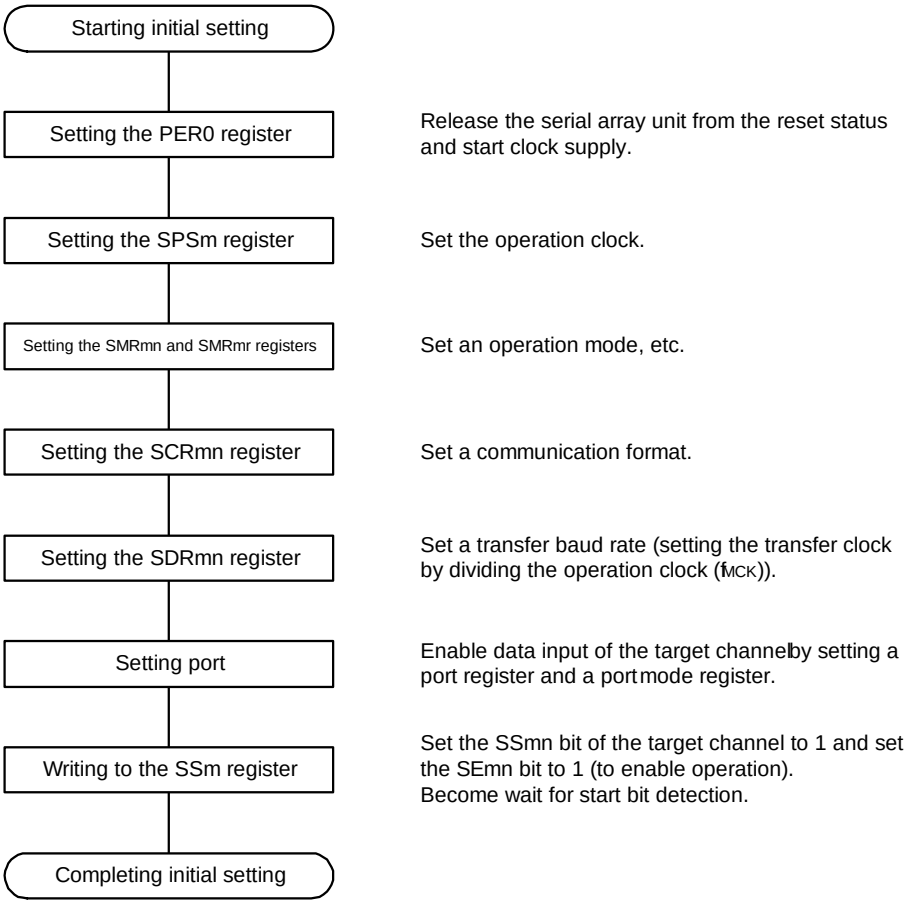
Note Serial array unit 0 only.

Remark 1. m: Unit number (m = 0, 1)

Remark 2. ■: Setting disabled (set to the initial value)
×: Bit that cannot be used in this mode (set to the initial value when not used in any mode)
0/1: Set to 0 or 1 depending on the usage of the user

(2) Operation procedure

Figure 20 - 110 Initial Setting Procedure for UART Reception



Caution Set the RXEmn bit of SCRmn register to 1, and then be sure to set SSmn to 1 after 4 or more fMCK clocks have elapsed.

Figure 20 - 111 Procedure for Stopping UART Reception

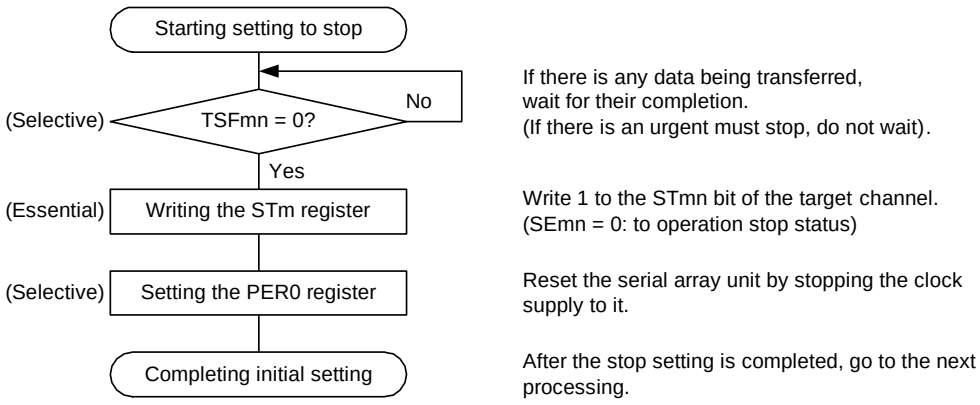
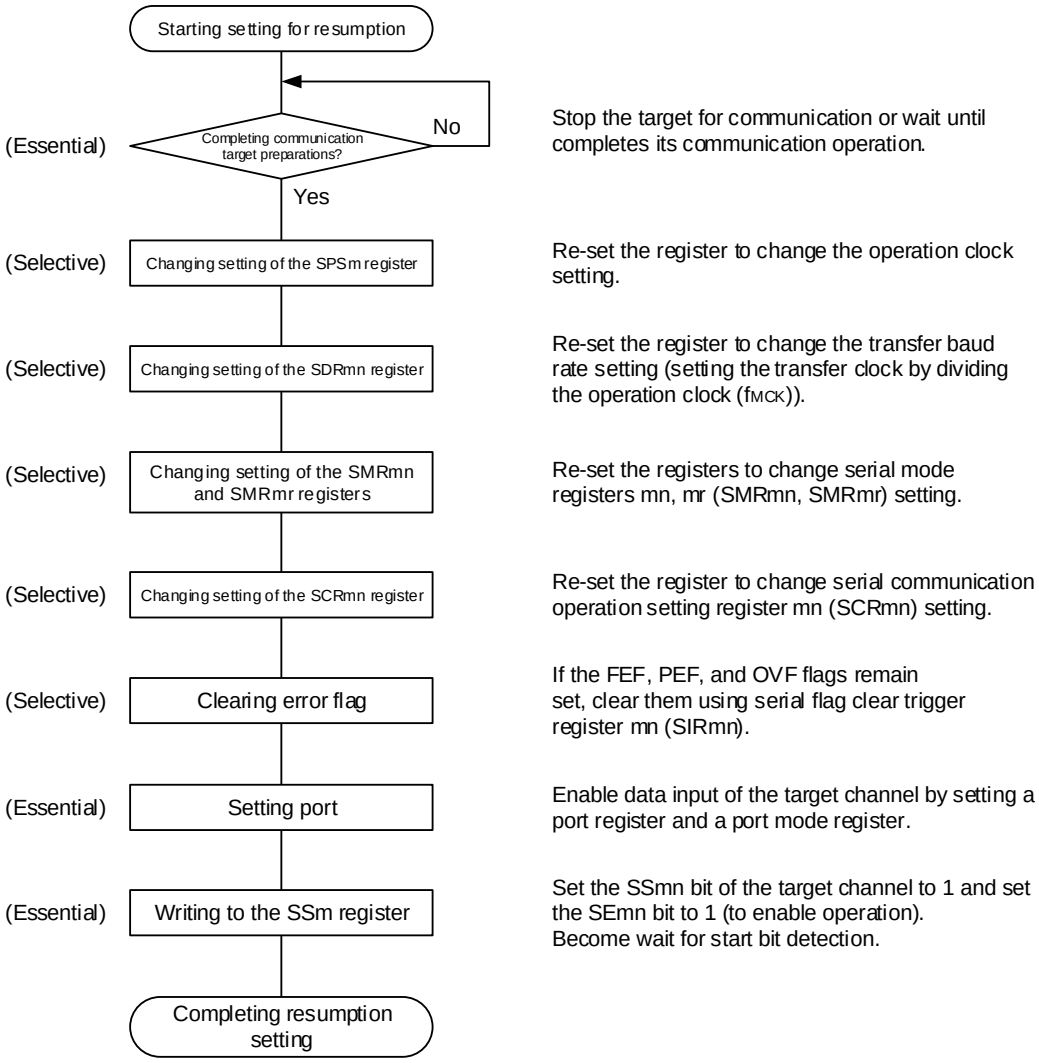


Figure 20 - 112 Procedure for Resuming UART Reception

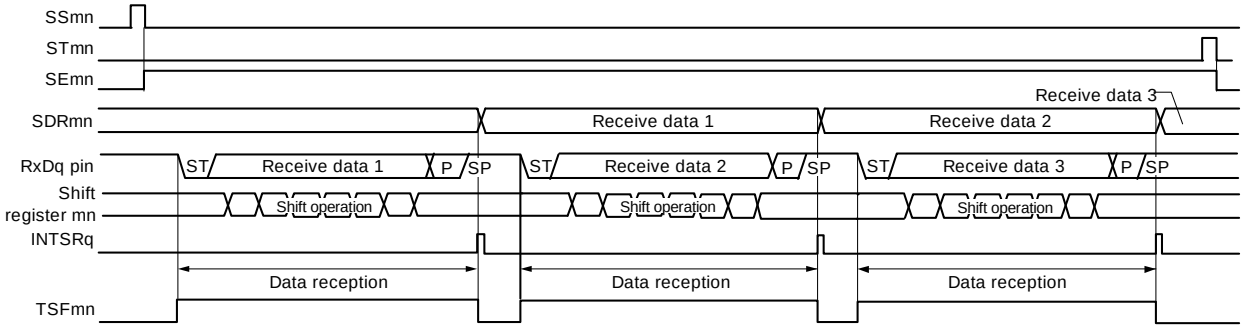


Caution **After is set RXEmn bit to 1 of SCRmn register, set the SSmn = 1 from an interval of at least four clocks of fMCK.**

Remark If PER0 is rewritten while stopping the communication target and the clock supply is stopped, wait until the communication target stops or communication finishes, and then perform initialization instead of restarting the communication.

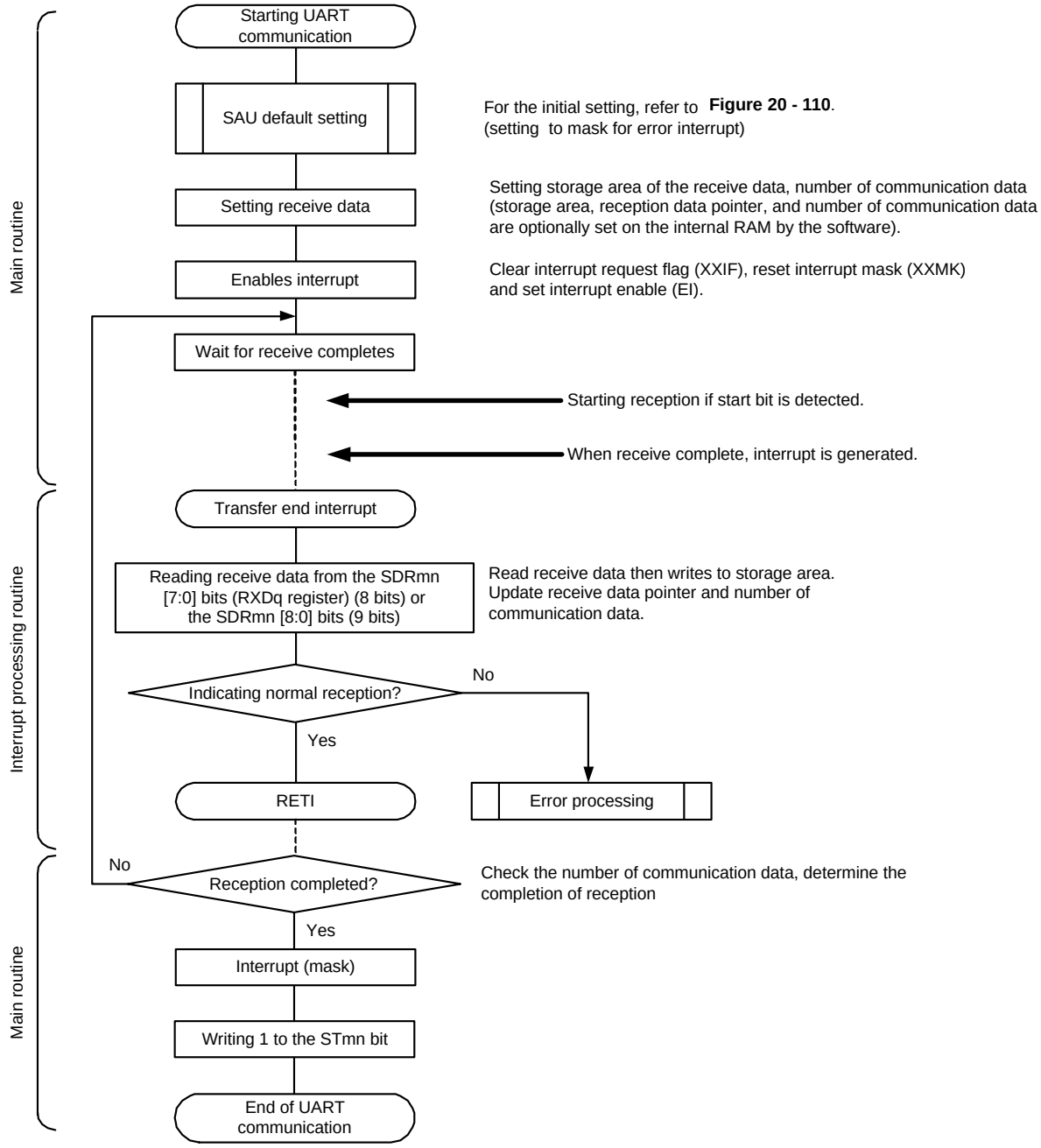
(3) Processing flow

Figure 20 - 113 Timing Chart of UART Reception



Remark m: Unit number (m = 0, 1), n: Channel number (n = 1, 3), mn = 01, 03, 11
r: Channel number (r = n - 1), q: UART number (q = 0 to 2)

Figure 20 - 114 Flowchart of UART Reception



20.7.3 SNOOZE mode function

The SNOOZE mode makes the UART perform reception operations upon RxDq pin input detection while in the STOP mode. Normally the UART stops communication in the STOP mode. However, using the SNOOZE mode enables the UART to perform reception operations without CPU operation.
Only the UART0, UART2 can be set to the SNOOZE mode.

When using UARTq in the SNOOZE mode, make the following settings before entering the STOP mode (See **Figure 20 - 117 Flowchart of SNOOZE Mode Operation (EOCm1 = 0, SSECm = 0/1 or EOCm1 = 1, SSECm = 0)** and **Figure 20 - 119 Flowchart of SNOOZE Mode Operation (EOCm1 = 1, SSECm = 1)**).

- In the SNOOZE mode, the baud rate setting for UART reception needs to be changed to a value different from that in normal operation. Set the SPSm register and bits 15 to 9 of the SDRmn register with reference to **Table 20 - 4**.
- Set the EOCmn and SSECmn bits. This is for enabling or stopping generation of an error interrupt (INTSRE0) when a communication error occurs.
- When using the SNOOZE mode function, set the SWCm bit of serial standby control register m (SSCm) to 1 just before switching to the STOP mode. After the initial setting has completed, set the SSm1 bit of serial channel start register m (SSm) to 1.

Upon detecting the edge of RxDq (start bit input) after a transition was made to the STOP mode, UART reception is started.

Caution 1. The SNOOZE mode can only be used when the high-speed on-chip oscillator clock (f_{IH}) is selected for f_{CLK}.

Caution 2. The transfer rate in the SNOOZE mode is only 4800 bps.

Caution 3. When SWCm = 1, UARTq can be used only when the reception operation is started in the STOP mode. When used simultaneously with another SNOOZE mode function or interrupt, if the reception operation is started in a state other than the STOP mode, such as those given below, data may not be received correctly and a framing error or parity error may be generated.

- **When after the SWCm bit has been set to 1, the reception operation is started before the STOP mode is entered**
- **When the reception operation is started while another function is in the SNOOZE mode**
- **When after returning from the STOP mode to normal operation due to an interrupt or other cause, the reception operation is started before the SWCm bit is returned to 0**

Caution 4. If a parity error, framing error, or overrun error occurs while the SSECm bit is set to 1, the PEFmn, FEFmn, or OVFmn flag is not set and an error interrupt (INTSREq) is not generated. Therefore, when the setting of SSECm = 1 is made, clear the PEFmn, FEFmn, or OVFmn flag before setting the SWC0 bit to 1 and read the value in bits 7 to 0 (RxDq register) of the SDRm1 register.

Caution 5. The CPU shifts from the STOP mode to the SNOOZE mode on detecting the valid edge of the RxDq signal. Note, however, that transfer through the UART channel may not start and the CPU may remain in the SNOOZE mode if an input pulse on the RxDq pin is too short to be detected as a start bit. In such cases, data may not be received correctly, and this may lead to a framing error or parity error in the next UART transfer.

Table 20 - 4 Baud Rate Setting for UART Reception in SNOOZE Mode

High-speed On-chip Oscillator (f_{IH})	Baud Rate for UART Reception in SNOOZE Mode			
	Baud Rate of 4800 bps			
	Operation Clock (f_{MCK})	SDRmn [15:9]	Maximum Permissible Value	Minimum Permissible Value
24 MHz ± 1.0% Note	$f_{CLK}/2^5$	79	1.60%	-2.18%
16 MHz ± 1.0% Note	$f_{CLK}/2^4$	105	2.27%	-1.53%
12 MHz ± 1.0% Note	$f_{CLK}/2^4$	79	1.60%	-2.19%
8 MHz ± 1.0% Note	$f_{CLK}/2^3$	105	2.27%	-1.53%
6 MHz ± 1.0% Note	$f_{CLK}/2^3$	79	1.60%	-2.19%
4 MHz ± 1.0% Note	$f_{CLK}/2^2$	105	2.27%	-1.53%
3 MHz ± 1.0% Note	$f_{CLK}/2^2$	79	1.60%	-2.19%
2 MHz ± 1.0% Note	$f_{CLK}/2$	105	2.27%	-1.54%
1 MHz ± 1.0% Note	f_{CLK}	105	2.27%	-1.57%

Note When the accuracy of the clock frequency of the high-speed on-chip oscillator is ±1.5% or ±2.0%, the permissible range becomes smaller as shown below.

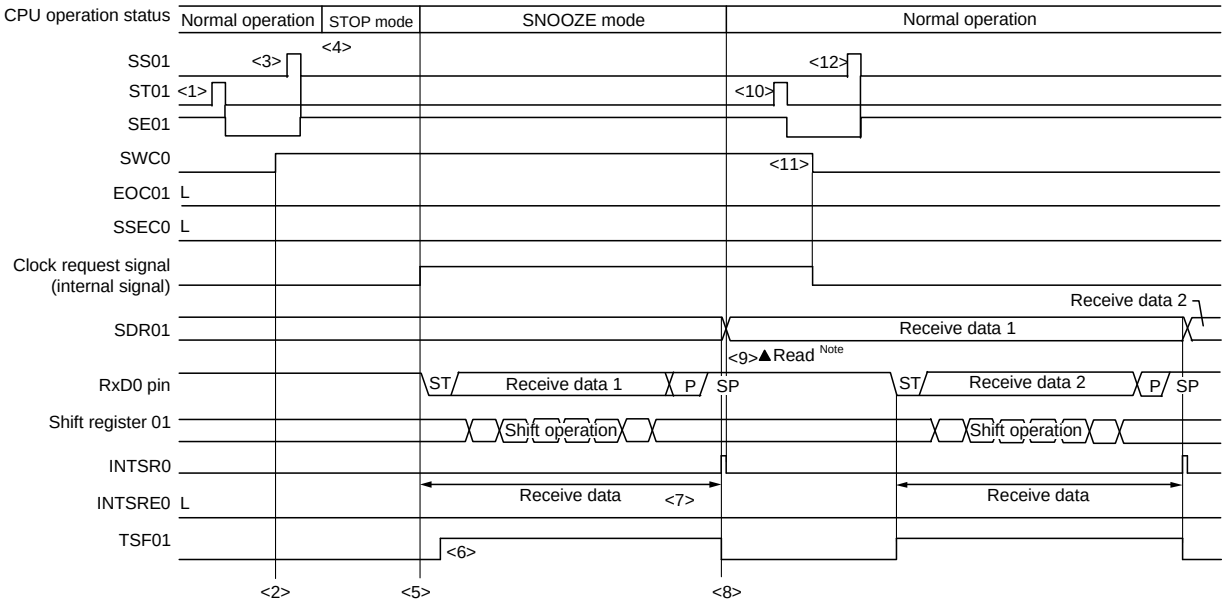
- In the case of f_{IH} ± 1.5%, perform (Maximum permissible value - 0.5%) and (Minimum permissible value + 0.5%) to the values in the above table.
- In the case of f_{IH} ± 2.0%, perform (Maximum permissible value - 1.0%) and (Minimum permissible value + 1.0%) to the values in the above table.

Remark The maximum permissible value and minimum permissible value are permissible values for the baud rate in UART reception. The baud rate on the transmitting side should be set to fall inside this range.

(1) SNOOZE mode operation (EOCm1 = 0, SSECm = 0/1)

Because of the setting of EOCm1 = 0, even though a communication error occurs, an error interrupt (INTSREq) is not generated, regardless of the setting of the SSECm bit. A transfer end interrupt (INTSRq) will be generated.

Figure 20 - 115 Timing Chart of SNOOZE Mode Operation (EOCm1 = 0, SSECm = 0/1)



Note Read the received data when SWCm is 1.

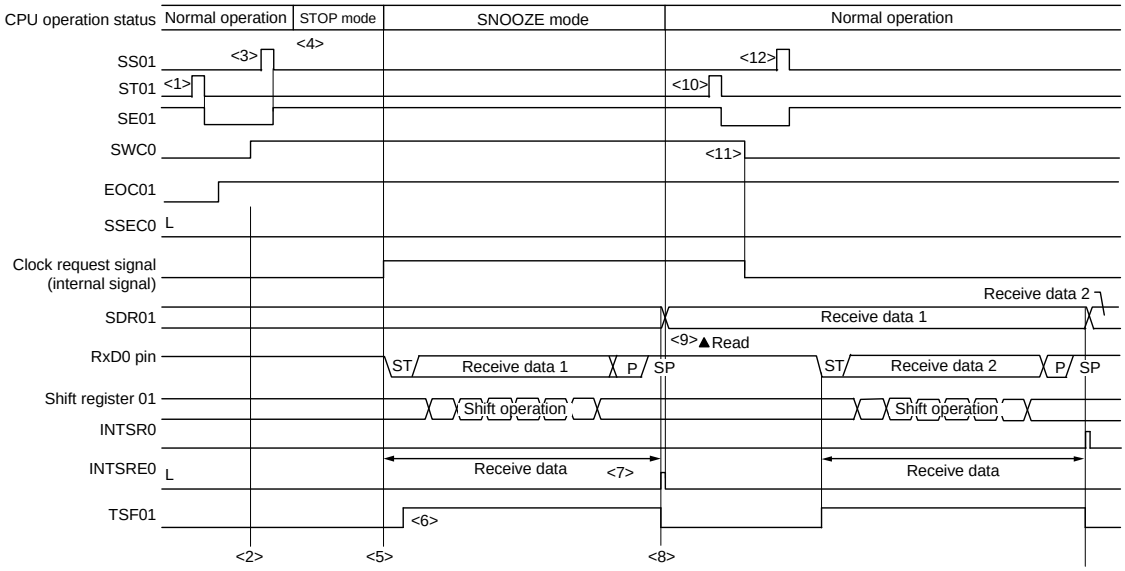
Caution **Before switching to the SNOOZE mode or after reception operation in the SNOOZE mode finishes, set the STm1 bit to 1 (clear the SEm1 bit, and stop the operation).**
After the receive operation completes, also clear the SWCm bit to 0 (SNOOZE mode release).

Remark 1. <1> to <12> in the figure correspond to <1> to <12> in **Figure 20 - 117 Flowchart of SNOOZE Mode Operation (EOCm1 = 0, SSECm = 0/1 or EOCm1 = 1, SSECm = 0)**.

Remark 2. m = 0, 1; q = 0, 2

(2) SNOOZE mode operation (EOCm1 = 1, SSECm = 0: Error interrupt (INTSREq) generation is enabled)
Because EOCm1 = 1 and SSECm = 0, an error interrupt (INTSREq) is generated when a communication error occurs.

Figure 20 - 116 Timing Chart of SNOOZE Mode Operation (EOCm1 = 1, SSECm = 0)

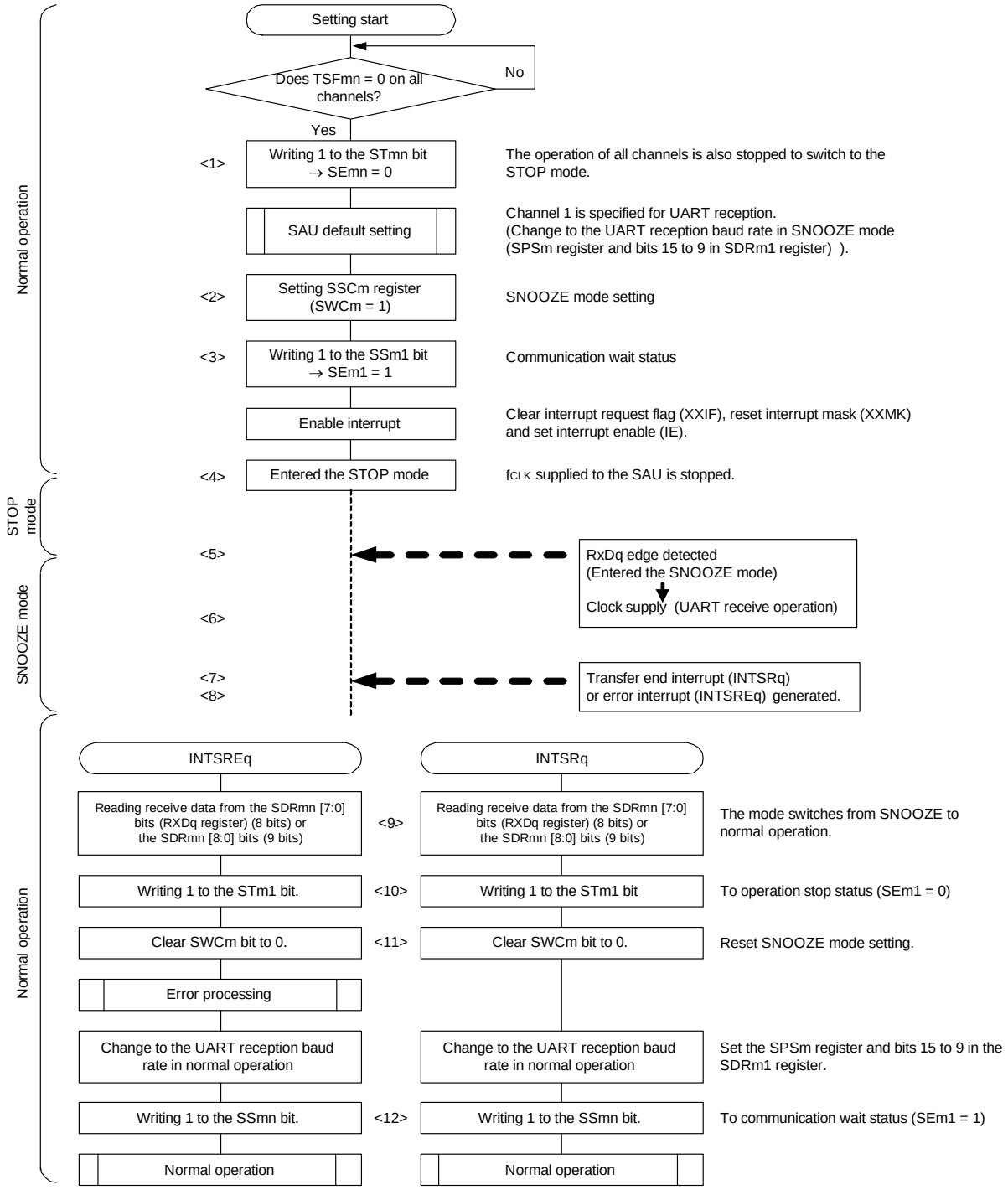


Caution Before switching to the SNOOZE mode or after reception operation in the SNOOZE mode finishes, set the STm1 bit to 1 (clear the SEm1 bit, and stop the operation).
After the receive operation completes, also clear the SWCm bit to 0 (SNOOZE mode release).

Remark 1. <1> to <12> in the figure correspond to <1> to <12> in **Figure 20 - 117 Flowchart of SNOOZE Mode Operation (EOCm1 = 0, SSECm = 0/1 or EOCm1 = 1, SSECm = 0)**.

Remark 2. m = 0, 1; q = 0, 2

Figure 20 - 117 Flowchart of SNOOZE Mode Operation (EOCm1 = 0, SSECm = 0/1 or EOCm1 = 1, SSECm = 0)



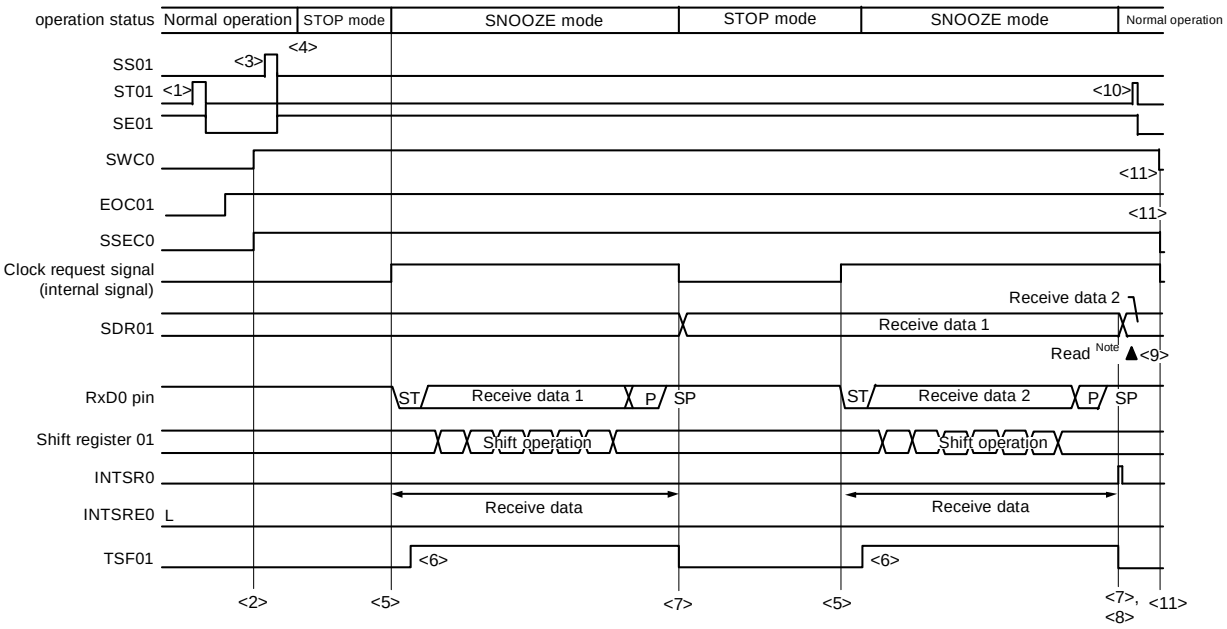
Remark 1. <1> to <12> in the figure correspond to <1> to <12> in **Figure 20 - 115 Timing Chart of SNOOZE Mode Operation (EOCm1 = 0, SSECm = 0/1)** and **Figure 20 - 116 Timing Chart of SNOOZE Mode Operation (EOCm1 = 1, SSECm = 0)**.

Remark 2. m = 0, 1; q = 0, 2

(3) SNOOZE mode operation (EOCm1 = 1, SSECm = 1: Error interrupt (INTSREq) generation is stopped)

Because EOCm1 = 1 and SSECm = 1, an error interrupt (INTSREq) is not generated when a communication error occurs.

Figure 20 - 118 Timing Chart of SNOOZE Mode Operation (EOCm1 = 1, SSECm = 1)



Note Read the received data when SWCm = 1.

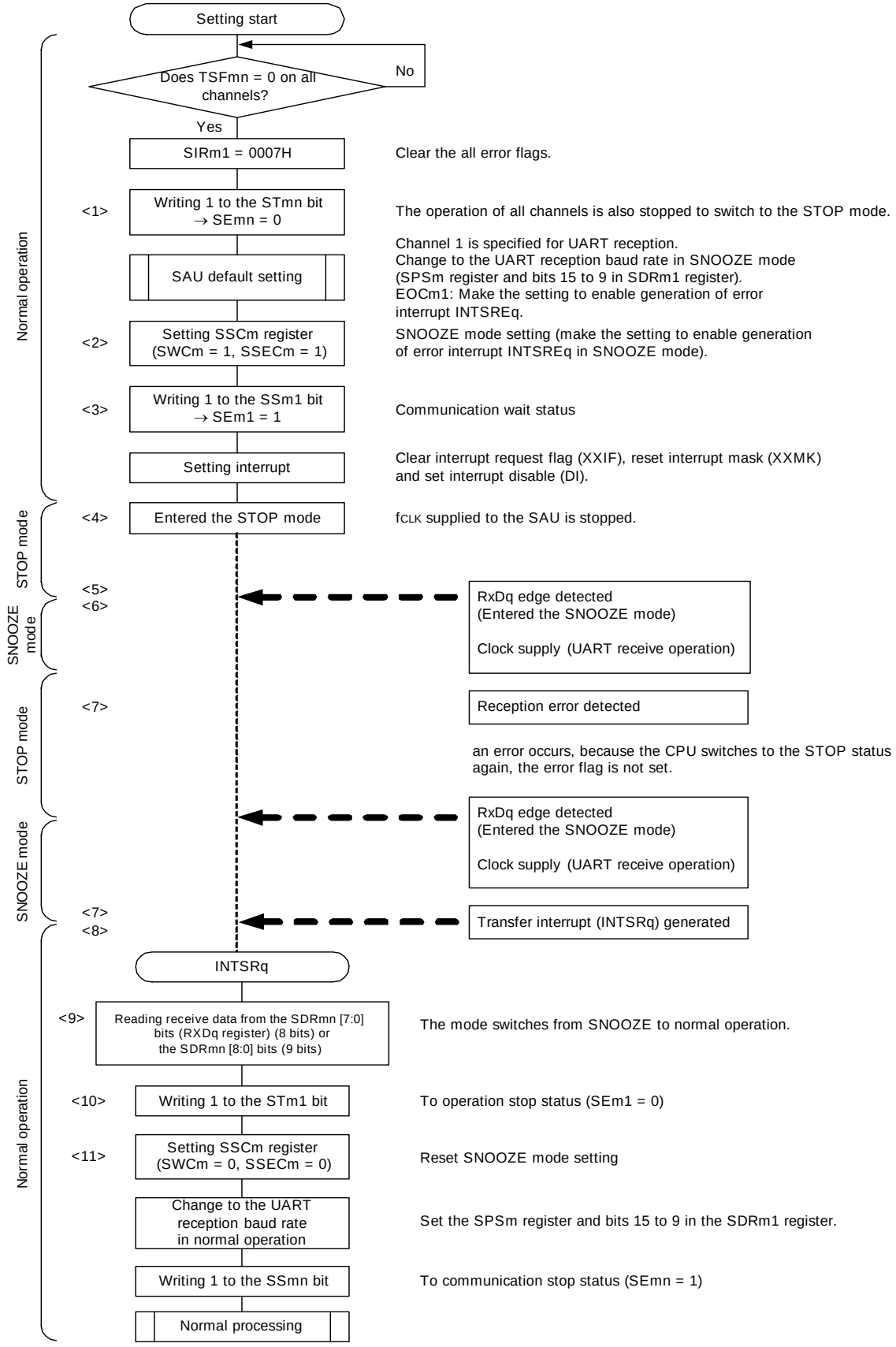
Caution 1. Before switching to the SNOOZE mode or after reception operation in the SNOOZE mode finishes, set the STm1 bit to 1 (clear the SEm1 bit and stop the operation).
After the receive operation completes, also clear the SWCm bit to 0 (SNOOZE mode release).

Caution 2. If a parity error, framing error, or overrun error occurs while the SSECm bit is set to 1, the PEFm1, FEFm1, or OVFm1 flag is not set and an error interrupt (INTSREq) is not generated. Therefore, when the setting of SSECm = 1 is made, clear the PEFm1, FEFm1, or OVFm1 flag before setting the SWCm bit to 1 and read the value in SDRm1[7:0] (RxDq register) (8 bits) or SDRm1[8:0] (9 bits).

Remark 1. <1> to <11> in the figure correspond to <1> to <11> in **Figure 20 - 119 Flowchart of SNOOZE Mode Operation (EOCm1 = 1, SSECm = 1)**.

Remark 2. m = 0, 1; q = 0, 2

Figure 20 - 119 Flowchart of SNOOZE Mode Operation (EOCm1 = 1, SSECm = 1)



(**Caution** and **Remarks** are listed on the next page.)

Caution **If a parity error, framing error, or overrun error occurs while the SSECm bit is set to 1, the PEFm1, FEFm1, or OVFm1 flag is not set and an error interrupt (INTSREq) is not generated. Therefore, when the setting of SSECm = 1 is made, clear the PEFm1, FEFm1, or OVFm1 flag before setting the SWCm bit to 1 and read the value in SDRm1[7:0] (RxDq register) (8 bits) or SDRm1[8:0] (9 bits).**

Remark 1. <1> to <11> in the figure correspond to <1> to <11> in **Figure 20 - 118 Timing Chart of SNOOZE Mode Operation (EOCm1 = 1, SSECm = 1)**.

Remark 2. m = 0, 1; q = 0, 2

20.7.4 Calculating baud rate

(1) Baud rate calculation expression

The baud rate for UART (UART0 to UART2) communication can be calculated by the following expressions.

(Baud rate) = {Operation clock (f_{MCK}) frequency of target channel} ÷ (SDRmn[15:9] + 1) ÷ 2 [bps]

Caution Setting serial data register mn (SDRmn) SDRmn[15:9] = (0000000B, 0000001B) is prohibited.

Remark 1. When UART is used, the value of SDRmn[15:9] is the value of bits 15 to 9 of the SDRmn register (0000010B to 1111111B) and therefore is 2 to 127.

Remark 2. m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), mn = 00 to 03, 10, 11

The operation clock (f_{MCK}) is determined by serial clock select register m (SPSm) and bit 15 (CKSmn) of serial mode register mn (SMRmn).

Table 20 - 5 Selection of Operation Clock For UART

SMRmn Register	SPSm Register								Operation Clock (f_{MCK}) Note	
CKSmn	PRS m13	PRS m12	PRS m11	PRS m10	PRS m03	PRS m02	PRS m01	PRS m00		f_{CLK} = 24 MHz
0	×	×	×	×	0	0	0	0	f_{CLK}	24 MHz
	×	×	×	×	0	0	0	1	$f_{CLK}/2$	12 MHz
	×	×	×	×	0	0	1	0	$f_{CLK}/2^2$	6 MHz
	×	×	×	×	0	0	1	1	$f_{CLK}/2^3$	3 MHz
	×	×	×	×	0	1	0	0	$f_{CLK}/2^4$	1.5 MHz
	×	×	×	×	0	1	0	1	$f_{CLK}/2^5$	750 kHz
	×	×	×	×	0	1	1	0	$f_{CLK}/2^6$	375 kHz
	×	×	×	×	0	1	1	1	$f_{CLK}/2^7$	187.5 kHz
	×	×	×	×	1	0	0	0	$f_{CLK}/2^8$	93.8 kHz
	×	×	×	×	1	0	0	1	$f_{CLK}/2^9$	46.9 kHz
	×	×	×	×	1	0	1	0	$f_{CLK}/2^{10}$	23.4 kHz
	×	×	×	×	1	0	1	1	$f_{CLK}/2^{11}$	11.7 kHz
	×	×	×	×	1	1	0	0	$f_{CLK}/2^{12}$	5.86 kHz
	×	×	×	×	1	1	0	1	$f_{CLK}/2^{13}$	2.93 kHz
	×	×	×	×	1	1	1	0	$f_{CLK}/2^{14}$	1.46 kHz
	×	×	×	×	1	1	1	1	$f_{CLK}/2^{15}$	732 Hz
1	0	0	0	0	×	×	×	×	f_{CLK}	24 MHz
	0	0	0	1	×	×	×	×	$f_{CLK}/2$	12 MHz
	0	0	1	0	×	×	×	×	$f_{CLK}/2^2$	6 MHz
	0	0	1	1	×	×	×	×	$f_{CLK}/2^3$	3 MHz
	0	1	0	0	×	×	×	×	$f_{CLK}/2^4$	1.5 MHz
	0	1	0	1	×	×	×	×	$f_{CLK}/2^5$	750 kHz
	0	1	1	0	×	×	×	×	$f_{CLK}/2^6$	375 kHz
	0	1	1	1	×	×	×	×	$f_{CLK}/2^7$	187.5 kHz
	1	0	0	0	×	×	×	×	$f_{CLK}/2^8$	93.8 kHz
	1	0	0	1	×	×	×	×	$f_{CLK}/2^9$	46.9 kHz
	1	0	1	0	×	×	×	×	$f_{CLK}/2^{10}$	23.4 kHz
	1	0	1	1	×	×	×	×	$f_{CLK}/2^{11}$	11.7 kHz
	1	1	0	0	×	×	×	×	$f_{CLK}/2^{12}$	5.86 kHz
	1	1	0	1	×	×	×	×	$f_{CLK}/2^{13}$	2.93 kHz
	1	1	1	0	×	×	×	×	$f_{CLK}/2^{14}$	1.46 kHz
	1	1	1	1	×	×	×	×	$f_{CLK}/2^{15}$	732 Hz

Note When changing the clock selected for f_{CLK} (by changing the system clock control register (CKC) value), do so after having stopped (serial channel stop register m (STm) = 000FH) the operation of the serial array unit (SAU).

Remark 1. ×: Don't care

Remark 2. m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), mn = 00 to 03, 10, 11

(2) Baud rate error during transmission

The baud rate error of UART (UART0 to UART2) communication during transmission can be calculated by the following expression. Make sure that the baud rate at the transmission side is within the permissible baud rate range at the reception side.

(Baud rate error) = (Calculated baud rate value) ÷ (Target baud rate) ×100 -100 [%]

Here is an example of setting a UART baud rate at f_{CLK} = 24 MHz.

UART Baud Rate (Target Baud Rate)	f_{CLK} = 24 MHz			
	Operation Clock (f_{MCK})	SDRmn[15:9]	Calculated Baud Rate	Error from Target Baud Rate
300 bps	$f_{CLK}/2^9$	77	300.48 bps	+0.16%
600 bps	$f_{CLK}/2^8$	77	600.96 bps	+0.16%
1200 bps	$f_{CLK}/2^7$	77	1201.92 bps	+0.16%
2400 bps	$f_{CLK}/2^6$	77	2403.85 bps	+0.16%
4800 bps	$f_{CLK}/2^5$	77	4807.69 bps	+0.16%
9600 bps	$f_{CLK}/2^4$	77	9615.38 bps	+0.16%
19200 bps	$f_{CLK}/2^3$	77	19230.8 bps	+0.16%
31250 bps	$f_{CLK}/2^3$	47	31250.0 bps	±0.0%
38400 bps	$f_{CLK}/2^2$	77	38461.5 bps	+0.16%
76800 bps	$f_{CLK}/2$	77	76923.1 bps	+0.16%
153600 bps	f_{CLK}	77	153846 bps	+0.16%
312500 bps	f_{CLK}	37	315789 bps	+1.05%

Remark m: Unit number (m = 0, 1), n: Channel number (n = 0, 2), mn = 00, 02, 10

(3) Permissible baud rate range for reception

The permissible baud rate range for reception during UART (UART0 to UART2) communication can be calculated by the following expression. Make sure that the baud rate at the transmission side is within the permissible baud rate range at the reception side.

$$\text{(Maximum receivable baud rate)} = \frac{2 \times k \times Nfr}{2 \times k \times Nfr - k + 2} \times Brate$$

$$\text{(Minimum receivable baud rate)} = \frac{2 \times k \times (Nfr - 1)}{2 \times k \times Nfr - k - 2} \times Brate$$

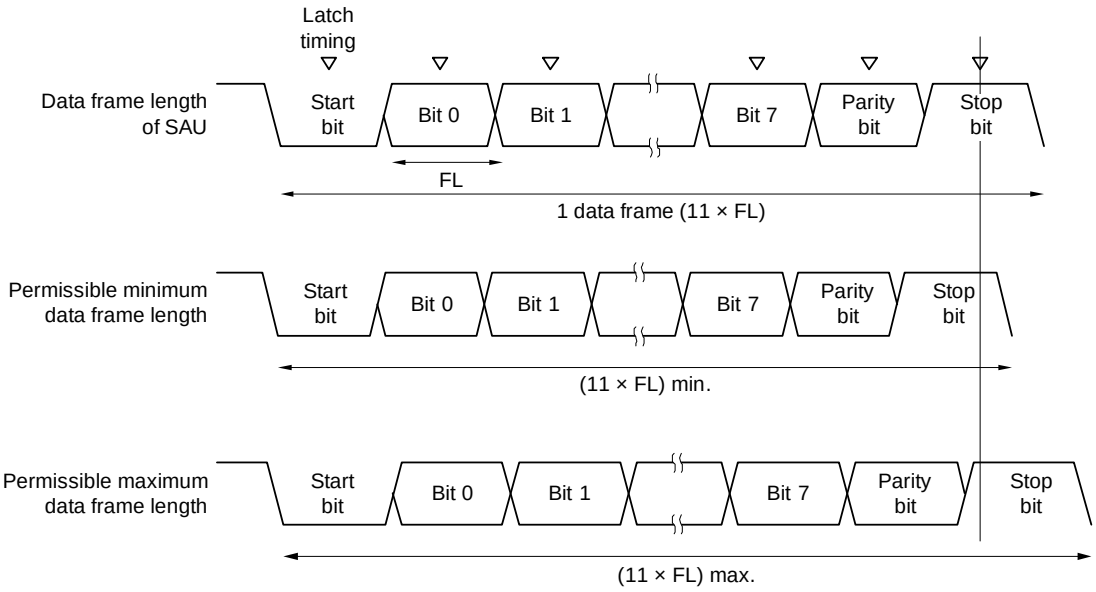
Brate: Calculated baud rate value at the reception side (See **20.7.4 (1) Baud rate calculation expression**.)

k: SDRmn[15:9] + 1

Nfr: 1 data frame length [bits]
= (Start bit) + (Data length) + (Parity bit) + (Stop bit)

Remark m: Unit number (m = 0, 1), n: Channel number (n = 1, 3), mn = 01, 03, 11

Figure 20 - 120 Permissible Baud Rate Range for Reception (1 Data Frame Length = 11 Bits)



As shown in **Figure 20 - 120**, the timing of latching receive data is determined by the division ratio set by bits 15 to 9 of serial data register mn (SDRmn) after the start bit is detected. If the last data (stop bit) is received before this latch timing, the data can be correctly received.

20.7.5 Procedure for processing errors that occurred during UART (UART0 to UART2) communication

The procedure for processing errors that occurred during UART (UART0 to UART2) communication is described in **Figure 20 - 121** and **20 - 122**.

Figure 20 - 121 Processing Procedure in Case of Parity Error or Overrun Error

Software Manipulation	Hardware Status	Remark
Reads serial data register mn (SDRmn) →	The BFFmn bit of the SSRmn register is set to 0 and channel n is enabled to receive data.	This is to prevent an overrun error if the next reception is completed during error processing.
Reads serial status register mn (SSRmn).		Error type is identified and the read value is used to clear error flag.
Writes 1 to serial flag clear trigger register mn (SIRmn). →	Error flag is cleared.	Error can be cleared only during reading, by writing the value read from the SSRmn register to the SIRmn register without modification.

Figure 20 - 122 Processing Procedure in Case of Framing Error

Software Manipulation	Hardware Status	Remark
Reads serial data register mn (SDRmn). →	The BFFmn bit of the SSRmn register is set to 0 and channel n is enabled to receive data.	This is to prevent an overrun error if the next reception is completed during error processing.
Reads serial status register mn (SSRmn).		Error type is identified and the read value is used to clear error flag.
Writes serial flag clear trigger register mn (SIRmn). →	Error flag is cleared.	Error can be cleared only during reading, by writing the value read from the SSRmn register to the SIRmn register without modification.
Sets the STmn bit of serial channel stop register m (STm) to 1. →	The SEmn bit of serial channel enable status register m (SEm) is set to 0 and channel n stops operating.	
Synchronization with other party of communication		Synchronization with the other party of communication is re-established and communication is resumed because it is considered that a framing error has occurred because the start bit has been shifted.
Sets the SSmn bit of serial channel start register m (SSm) to 1. →	The SEmn bit of serial channel enable status register m (SEm) is set to 1 and channel n is enabled to operate.	

Remark m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), mn = 00 to 03, 10, 11

20.8 LIN Communication Operation

20.8.1 LIN transmission

Of UART transmission, UART0 support LIN communication.

For LIN transmission, channel 0 of unit 0 is used.

UART	UART0	UART1	UART2
Support of LIN communication	Supported	Not supported	Not supported
Target channel	Channel 0 of SAU0	—	—
Pins used	TxD0	—	—
Interrupt	INTST0	—	—
	Transfer end interrupt (in single-transfer mode) or buffer empty interrupt (in continuous transfer mode) can be selected.		
Error detection flag	None		
Transfer data length	8 bits		
Transfer rate	Max. f_{MCK}/6 [bps] (SDR00 [15:9] = 2 or more), Min. $f_{CLK}/(2 \times 2^{15} \times 128)$ [bps] Note		
Data phase	Non-reverse output (default: high level) Reverse output (default: low level)		
Parity bit	No parity bit		
Stop bit	Appending 1 bit		
Data direction	LSB first		

Note Use this operation within a range that satisfies the conditions above and the peripheral functions characteristics in the electrical specifications (see **CHAPTER 38** or **CHAPTER 39 ELECTRICAL SPECIFICATIONS**). In general, 2.4/9.6/19.2 kbps is often used in LIN communication.

Remark f_{MCK}: Operation clock frequency of target channel
f_{CLK}: System clock frequency

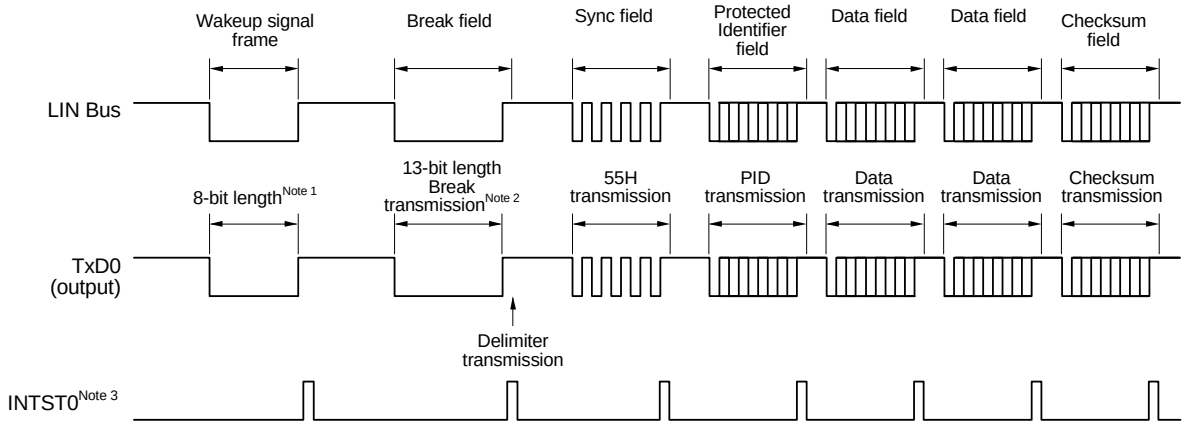
LIN stands for Local Interconnect Network and is a low-speed (1 to 20 kbps) serial communication protocol designed to reduce the cost of an automobile network. Communication of LIN is single-master communication and up to 15 slaves can be connected to one master. The slaves are used to control switches, actuators, and sensors, which are connected to the master via LIN.

Usually, the master is connected to a network such as CAN (Controller Area Network). A LIN bus is a single-wire bus to which nodes are connected via transceiver conforming to ISO9141.

According to the protocol of LIN, the master transmits a frame by attaching baud rate information to it. A slave receives this frame and corrects a baud rate error from the master. If the baud rate error of a slave is within ±15%, communication can be established.

Figure 20 - 123 outlines a transmission operation of LIN.

Figure 20 - 123 Transmission Operation of LIN



Note 1. Set the baud rate in accordance with the wakeup signal regulations and transmit data of 80H.

Note 2. A break field is defined to have a width of 13 bits and output a low level. Where the baud rate for main transfer is N [bps], therefore, the baud rate of the break field is calculated as follows.

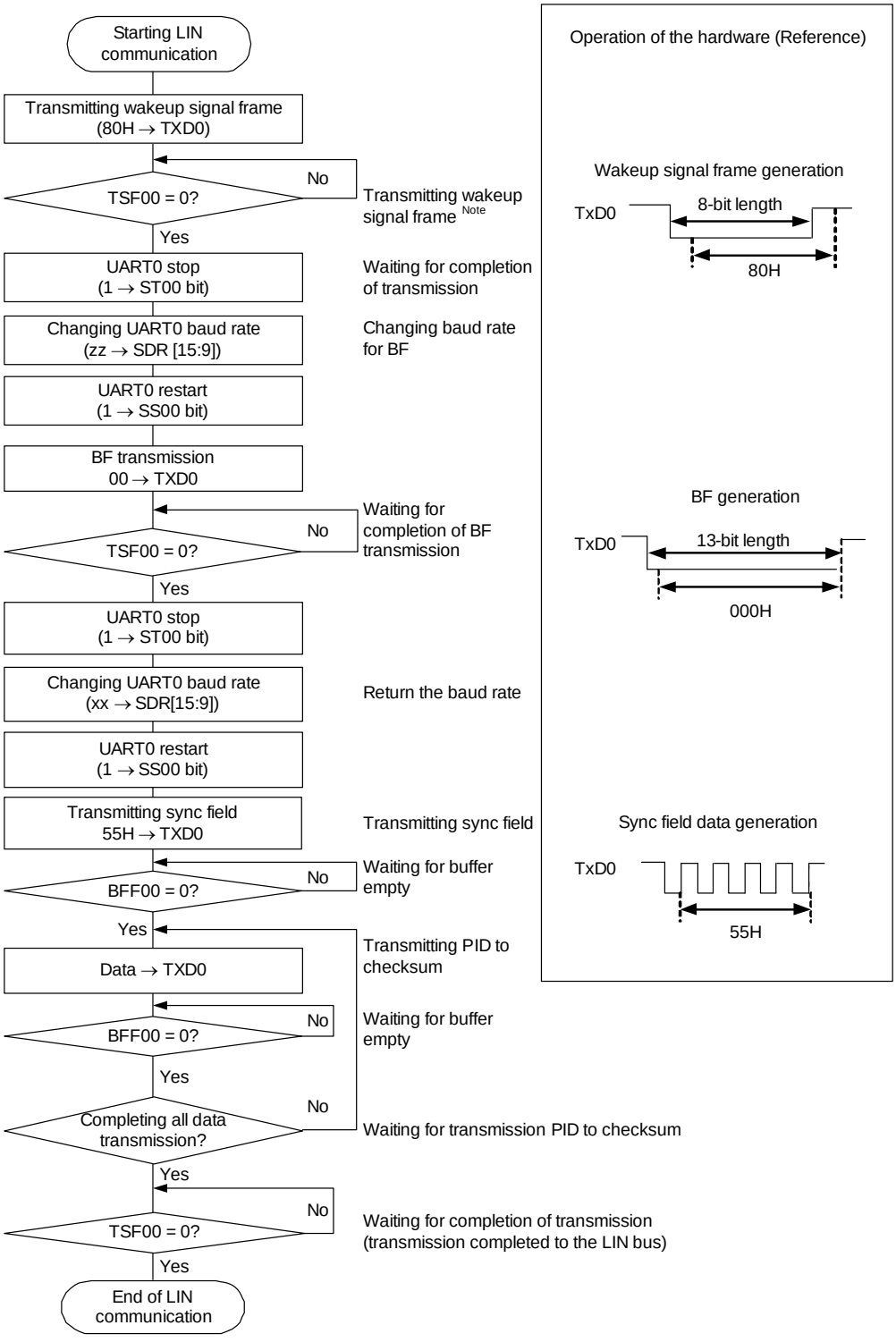
(Baud rate of sync break field) = 9/13 × N

By transmitting data of 00H at this baud rate, a break field is generated.

Note 3. INTST0 is output upon completion of transmission. INTST0 is also output at BF transmission.

Remark The interval between fields is controlled by software.

Figure 20 - 124 Flowchart for LIN Transmission



Note When LIN-bus start from sleep status only

Remark Default setting of the UART is complete, and the flow from the transmission enable status.

20.8.2 LIN reception

Of UART reception, UART0 support LIN communication.

For LIN reception, channel 1 of unit 1 is used.

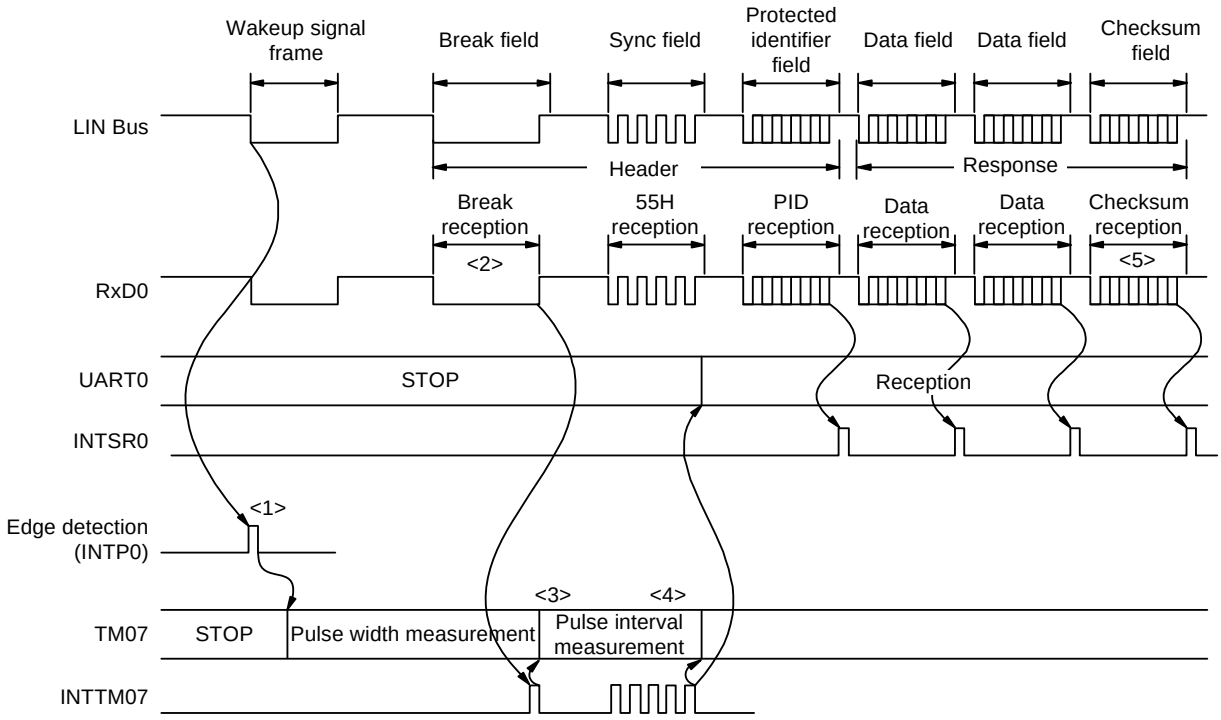
UART	UART0	UART1	UART2
Support of LIN communication	Supported	Not supported	Not supported
Target channel	Channel 1 of SAU0	—	—
Pins used	RxD0	—	—
Interrupt	INTSR0	—	—
	Transfer end interrupt only (Setting the buffer empty interrupt is prohibited.)		
Error interrupt	INTSRE0	—	—
Error detection flag	• Framing error detection flag (FEF01) • Overrun error detection flag (OVF01)		
Transfer data length	8 bits		
Transfer rate Note	Max. f_{MCK}/6 [bps] (SDR01 [15:9] = 2 or more), Min. $f_{CLK}/(2 \times 2^{15} \times 128)$ [bps]		
Data phase	Non-reverse output (default: high level) Reverse output (default: low level)		
Parity bit	No parity bit (The parity bit is not checked.)		
Stop bit	Appending 1 bit		
Data direction	LSB first		

Note Use this operation within a range that satisfies the conditions above and the peripheral functions characteristics in the electrical specifications (see **CHAPTER 38** or **CHAPTER 39 ELECTRICAL SPECIFICATIONS**).

Remark f_{MCK}: Operation clock frequency of target channel
f_{CLK}: System clock frequency

Figure 20 - 125 outlines a reception operation of LIN.

Figure 20 - 125 Reception Operation of LIN



Here is the flow of signal processing.

<1> The wakeup signal is detected by detecting an interrupt edge (INTP0) on a pin. When the wakeup signal is detected, change TM07 to pulse width measurement upon detection of the wakeup signal to measure the low-level width of the BF signal. Then wait for BF signal reception.

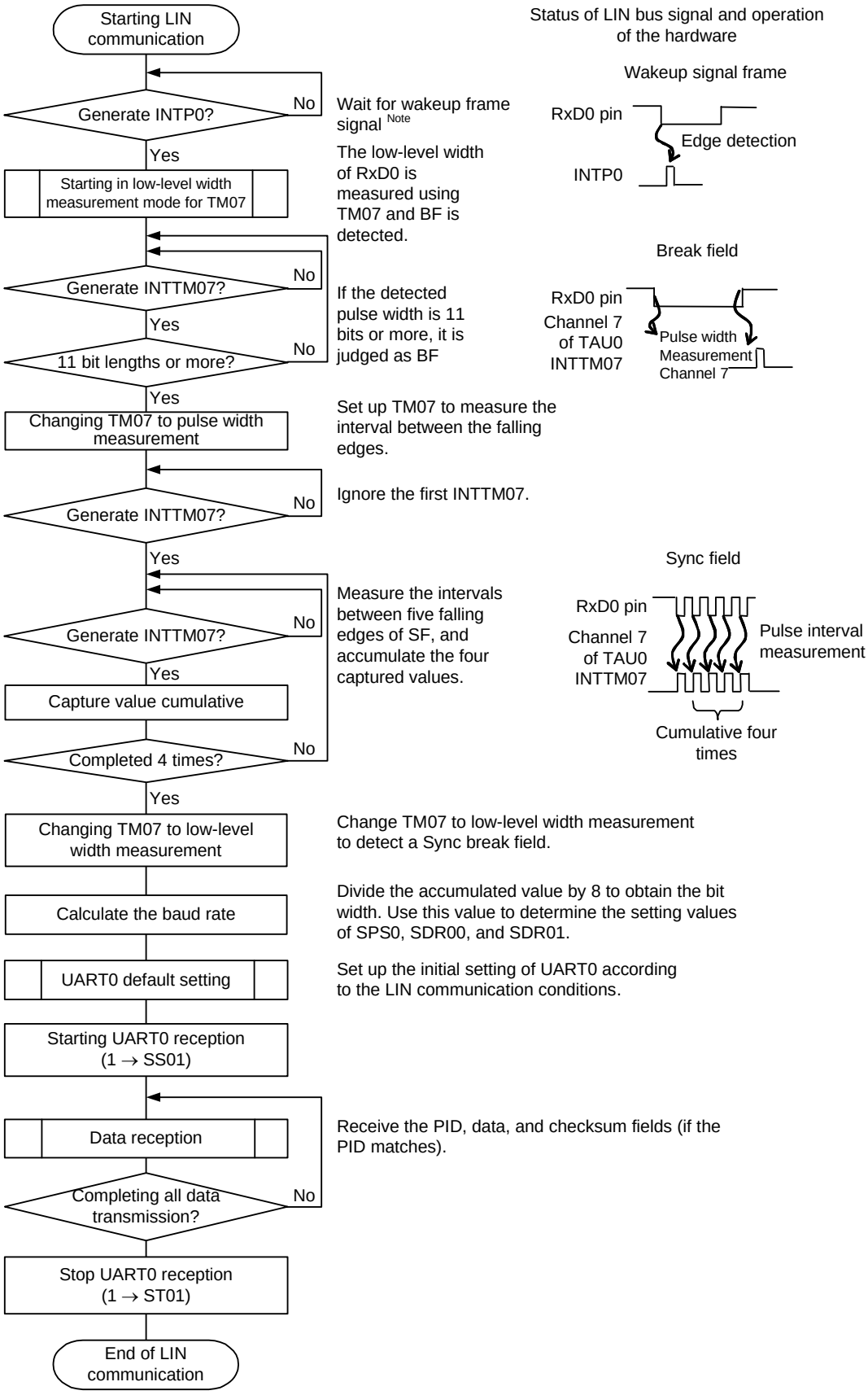
<2> TM07 starts measuring the low-level width upon detection of the falling edge of the BF signal, and then captures the data upon detection of the rising edge of the BF signal. The captured data is used to judge whether it is the BF signal.

<3> When the BF signal has been received normally, change TM07 to pulse interval measurement and measure the interval between the falling edges of the RxD0 signal in the Sync field four times (see **6.8.3 Operation as input pulse interval measurement**).

<4> Calculate a baud rate error from the bit interval of sync field (SF). Stop UART0 once and adjust (re-set) the baud rate.

<5> The checksum field should be distinguished by software. In addition, processing to initialize UART0 after the checksum field is received and to wait for reception of BF should also be performed by software.

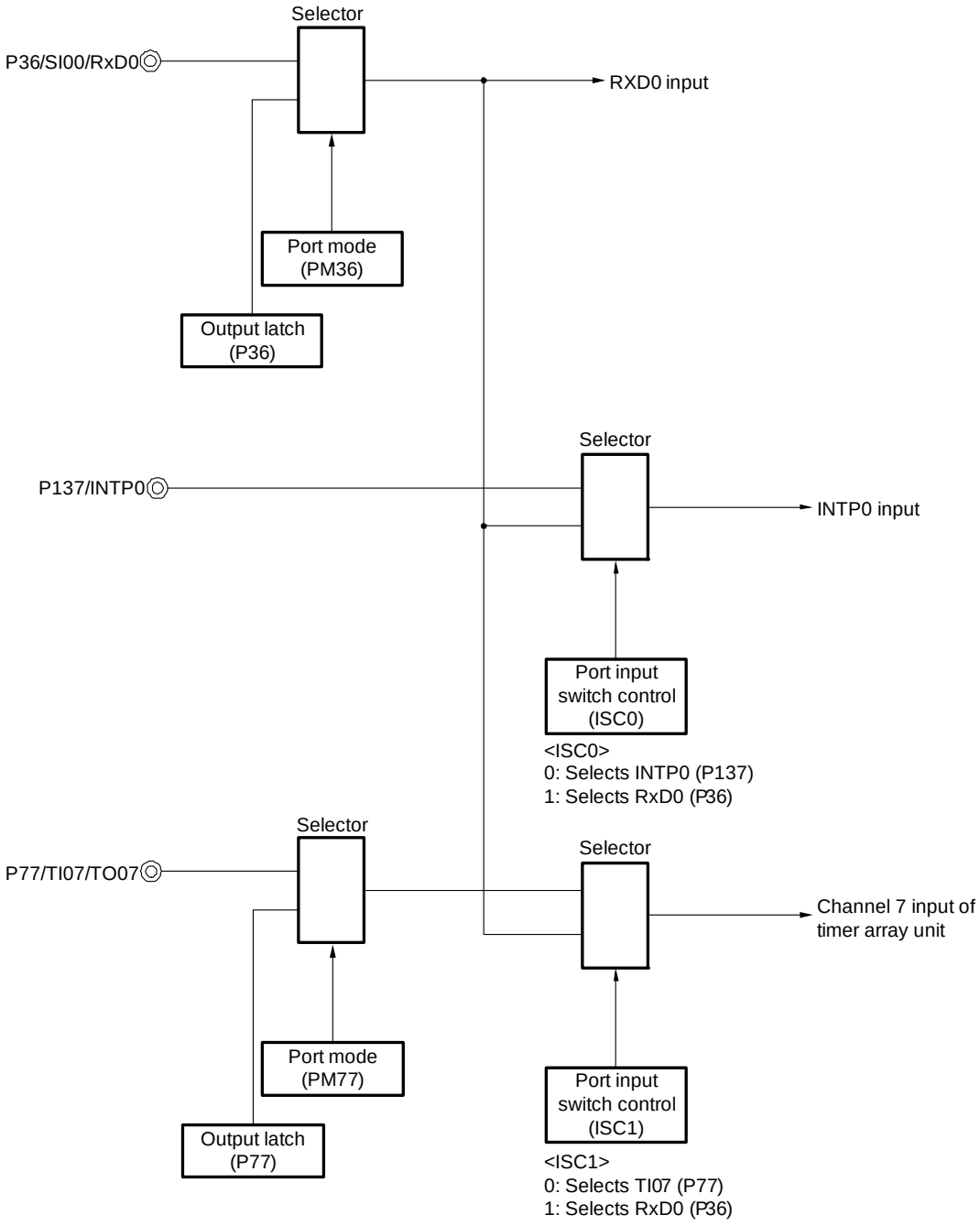
Figure 20 - 126 Flowchart of LIN Reception



Note Required in the sleep status only.

Figure 20 - 127 shows the configuration of a port that manipulates reception of LIN.
The wakeup signal transmitted from the master of LIN is received by detecting an edge of an external interrupt (INTP0). The length of the sync field transmitted from the master can be measured by using the external event capture operation of the timer array unit 0 to calculate a baud-rate error.
By controlling switch of port input (ISC0/ISC1), the input source of port input (RxD0) for reception can be input to the external interrupt pin (INTP0) and timer array unit

Figure 20 - 127 Port Configuration for Manipulating Reception of LIN



Remark ISC0, ISC1: Bits 0 and 1 of the input switch control register (ISC) (See **Figure 20 - 21**.)

The peripheral functions used for the LIN communication operation are as follows.

<Peripheral functions used>

- External interrupt (INTP0); Wakeup signal detection
  Usage: To detect an edge of the wakeup signal and the start of communication
- Channel 7 of timer array unit; Baud rate error detection, break field detection.
  Usage: To detect the length of the sync field (SF) and divide it by the number of bits in order to detect an error
  (The interval of the edge input to RxD0 is measured in the capture mode.)
  Measured the low-level width, determine whether break field (BF).
- Channels 0 and 1 (UART0) of serial array unit 0 (SAU0)

20.9 Operation of Simplified I²C (IIC00, IIC10, IIC20) Communication

This is a clocked communication function to communicate with two or more devices by using two lines: serial clock (SCL) and serial data (SDA). This communication function is designed to execute single communication with devices such as EEPROM, flash memory, and A/D converter, and therefore, can be used only by the master.
Operate the control registers by software for setting the start and stop conditions while observing the specifications of the I²C bus line.

[Data transmission/reception]
- Master transmission, master reception (only master function with a single master)
- ACK output function Note and ACK detection function
- Data length of 8 bits
  (When an address is transmitted, the address is specified by the higher 7 bits, and the least significant bit is used for R/W control.)
- Generation of start condition and stop condition for software

[Interrupt function]
- Transfer end interrupt

[Error detection flag]
- Overrun error
- ACK error

* [Functions not supported by simplified I²C]
- Slave transmission, slave reception
- Multi-master function (arbitration loss detection function)
- Wait detection function

Note When receiving the last data, ACK will not be output if 0 is written to the SOEmn (SOEm register) bit and serial communication data output is stopped. See the processing flow in **20.9.3 (2)** for details.

Remark m: Unit number (m = 0, 1), n: Channel number (n = 0, 2), mn = 00, 02, 10

The channel supporting simplified I^2C (IIC00, IIC10, IIC20) is channels 0 and 2 of SAU0, and channels 0 and 2 of SAU1

Unit	Channel	Used as Simplified SPI(CSI)	Used as UART	Used as Simplified I^2C
0	0	CSI00	UART0 (supporting LIN-bus)	IIC00
	1	—		—
	2	CSI10	UART1	IIC10
	3	—		—
1	0	CSI20	UART2	IIC20
	1	—		—

Simplified I^2C (IIC00, IIC10, IIC20) performs the following four types of communication operations.

- Address field transmission (See **20.9.1**.)
- Data transmission (See **20.9.2**.)
- Data reception (See **20.9.3**.)
- Stop condition generation (See **20.9.4**.)

20.9.1 Address field transmission

Address field transmission is a transmission operation that first executes in I^2C communication to identify the target for transfer (slave). After a start condition is generated, an address (7 bits) and a transfer direction (1 bit) are transmitted in one frame.

Simplified I^2C	IIC00	IIC10	IIC20
Target channel	Channel 0 of SAU0	Channel 2 of SAU0	Channel 0 of SAU1
Pins used	SCL00, SDA00 Note 1	SCL10, SDA10 Note 1	SCL20, SDA20 Note 1
Interrupt	INTIIC00	INTIIC10	INTIIC20
	Transfer end interrupt only (Setting the buffer empty interrupt is prohibited.)		
Error detection flag	ACK error detection flag (PEFmn)		
Transfer data length	8 bits (transmitted with specifying the higher 7 bits as address and the least significant bit as R/W control)		
Transfer rate Note 2	Max. f_{MCK}/4 [Hz] (SDRmn[15:9] = 1 or more) f_{MCK}: Operation clock frequency of target channel However, the following condition must be satisfied in each mode of I^2C. • Max. 1 MHz (fast mode plus) • Max. 400 kHz (fast mode) • Max. 100 kHz (standard mode)		
Data level	Non-reversed output (default: high level)		
Parity bit	No parity bit		
Stop bit	Appending 1 bit (for ACK reception timing)		
Data direction	MSB first		

Note 1. To perform communication via simplified I^2C, set the N-ch open-drain output (V_{DD} tolerance mode (POMxx = 1) with the port output mode register (POMxx). For details, see **4.4 Registers Controlling Port Function** and **4.6 Register Settings When Using Alternate Function**.
When IIC00, IIC10, or IIC20 is communicating with an external device with a different potential, set the N-ch open-drain output (V_{DD} tolerance mode (POMxx = 1) also for the clock input/output pins (SCL00, SCL10, SCL20).
For details, see **4.5.4 Handling different potential (1.8 V Note, 2.5 V, 3 V) by using I/O buffers**.

Note 2. Use this operation within a range that satisfies the conditions above and the peripheral functions characteristics in the electrical specifications (see **CHAPTER 38** or **CHAPTER 39 ELECTRICAL SPECIFICATIONS**).

Remark m: Unit number (m = 0, 1), n: Channel number (n = 0, 2), mn = 00, 02, 10

(1) Register setting

Figure 20 - 128 Example of Contents of Registers for Address Field Transmission of Simplified I²C (IIC00, IIC10, IIC20)

(a) Serial mode register mn (SMRmn)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SMRmn	CKSmn 0/1	CCSmn 0	0	0	0	0	0	STSmn 0	0	SISmn0 0	1	0	0	MDmn2 1	MDmn1 0	MDmn0 0

Operation clock (fMCK) of channel n
0: Prescaler output clock CKm0 set by the SPSm register
1: Prescaler output clock CKm1 set by the SPSm register

Operation mode of channel n
0: Transfer end interrupt

(b) Serial communication operation setting register mn (SCRmn)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SCRmn	TXEmn 1	RXEmn 0	DAPmn 0	CKPmn 0	0	EOCmn 0	PTCmn1 0	PTCmn0 0	DIRmn 0	0	SLCmn1 0	SLCmn0 1	0	1	DLSmn1 1	DLSmn0 1

Setting of parity bit
00B: No parity

Setting of stop bit
01B: Appending 1 bit (ACK)

(c) Serial data register mn (SDRmn) (lower 8 bits: SIOr)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SDRmn	Baud rate setting							0	Transmit data setting (address + R/W)							

SIOr

(d) Serial output register m (SOm)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SOm	0	0	0	0	1	CKOm2 0/1	1	CKOm0 0/1	0	0	0	0	1	SOm2 0/1	1	SOm0 0/1

Start condition is generated by manipulating the SOmn bit.

(e) Serial output enable register m (SOEm)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SOEm	0	0	0	0	0	0	0	0	0	0	0	0	0	SOEm2 0/1	0	SOEm0 0/1

SOEmn = 0 until the start condition is generated, and SOEmn = 1 after generation.

(f) Serial channel start register m (SSm)... Sets only the bits of the target channel is 1.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SSm	0	0	0	0	0	0	0	0	0	0	0	0	SSm3 ×	SSm2 0/1	SSm1 ×	SSm0 0/1

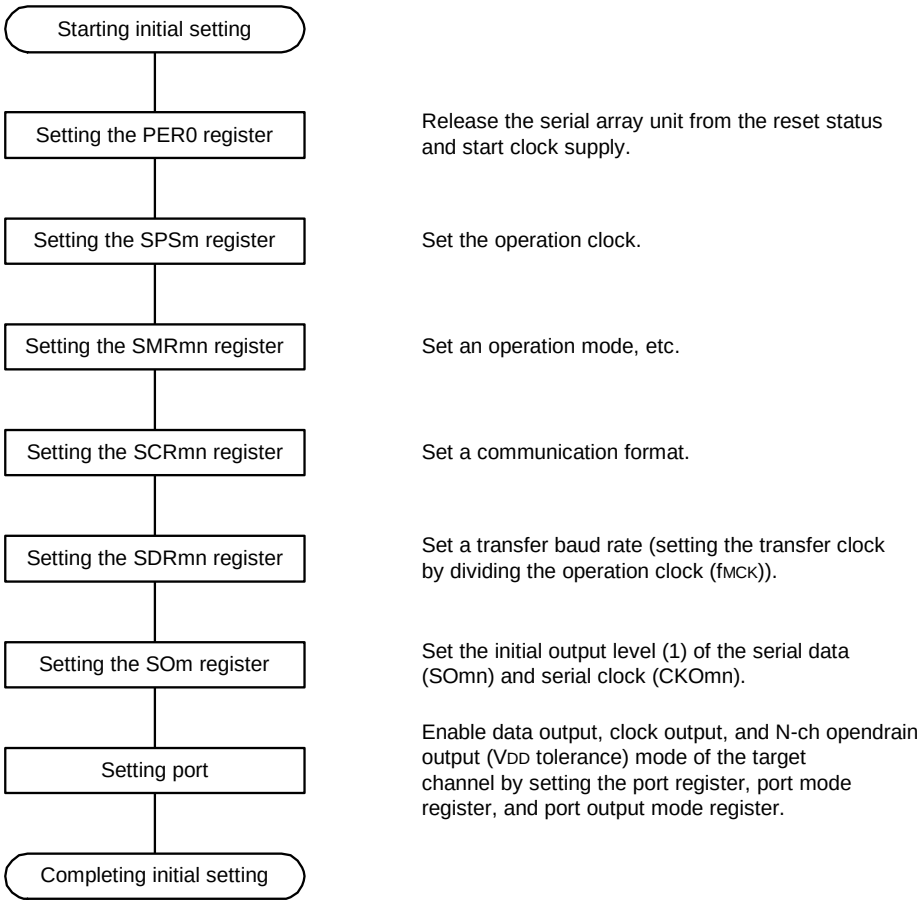
SSmn = 0 until the start condition is generated, and SSmn = 1 after generation.

Remark 1. m: Unit number (m = 0, 1), n: Channel number (n = 0, 2), r: IIC number (r = 00, 10, 20), mn = 00, 02, 10

Remark 2. ■: Setting is fixed in the IIC mode,
■: Setting disabled (set to the initial value)
×: Bit that cannot be used in this mode (set to the initial value when not used in any mode)
0/1: Set to 0 or 1 depending on the usage of the user

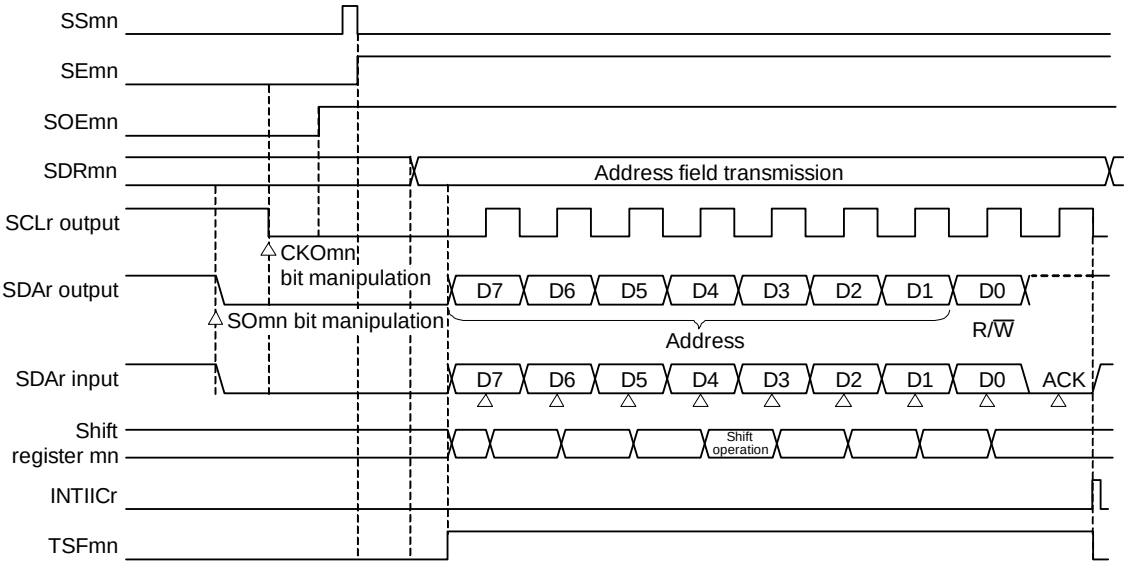
(2) Operation procedure

Figure 20 - 129 Initial Setting Procedure for Address Field Transmission



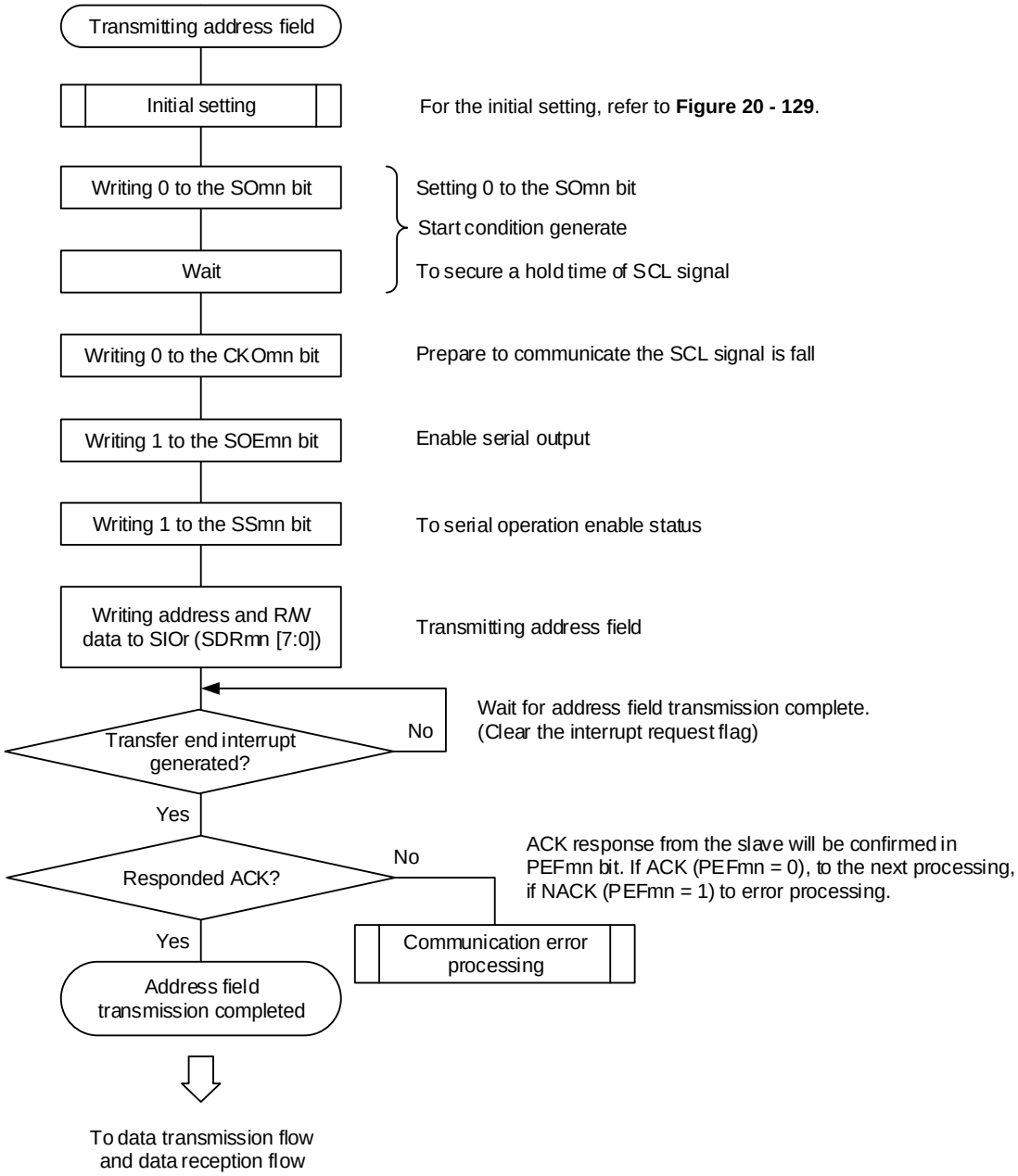
(3) Processing flow

Figure 20 - 130 Timing Chart of Address Field Transmission



Remark m: Unit number (m = 0, 1), n: Channel number (n = 0, 2), r: IIC number (r = 00, 10, 20), mn = 00, 02, 10

Figure 20 - 131 Flowchart of Address Field Transmission



20.9.2 Data transmission

Data transmission is an operation to transmit data to the target for transfer (slave) after transmission of an address field. After all data are transmitted to the slave, a stop condition is generated and the bus is released.

Simplified I2C	IIC00	IIC10	IIC20
Target channel	Channel 0 of SAU0	Channel 2 of SAU0	Channel 0 of SAU1
Pins used	SCL00, SDA00 Note 1	SCL10, SDA10 Note 1	SCL20, SDA20 Note 1
Interrupt	INTIIC00	INTIIC10	INTIIC20
	Transfer end interrupt only (Setting the buffer empty interrupt is prohibited.)		
Error detection flag	ACK error flag (PEFmn)		
Transfer data length	8 bits		
Transfer rate Note 2	Max. fMCK/4 [Hz] (SDRmn[15:9] = 1 or more) fMCK: Operation clock frequency of target channel However, the following condition must be satisfied in each mode of I2C. • Max. 1 MHz (fast mode plus) • Max. 400 kHz (fast mode) • Max. 100 kHz (standard mode)		
Data level	Non-reversed output (default: high level)		
Parity bit	No parity bit		
Stop bit	Appending 1 bit (for ACK reception timing)		
Data direction	MSB first		

Note 1. To perform communication via simplified I2C, set the N-ch open-drain output (VDD tolerance mode (POMxx = 1) with the port output mode register (POMxx). For details, see **4.4 Registers Controlling Port Function** and **4.6 Register Settings When Using Alternate Function**.
When IIC00, IIC10, or IIC20 is communicating with an external device with a different potential, set the N-ch open-drain output (VDD tolerance mode (POMxx = 1) also for the clock input/output pins (SCL00, SCL10, SCL20).
For details, see **4.5.4 Handling different potential (1.8 V Note, 2.5 V, 3 V) by using I/O buffers**.

Note 2. Use this operation within a range that satisfies the conditions above and the peripheral functions characteristics in the electrical specifications (see **CHAPTER 38** or **CHAPTER 39 ELECTRICAL SPECIFICATIONS**).

Remark m: Unit number (m = 0, 1), n: Channel number (n = 0, 2), mn = 00, 02, 10

(1) Register setting

Figure 20 - 132 Example of Contents of Registers for Data Transmission of Simplified I²C (IIC00, IIC10, IIC20)

(a) Serial mode register mn (SMRmn)... Do not manipulate this register during data transmission/reception.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SMRmn	CKSmn	CCSmn	0	0	0	0	0	STSmn	0	SISmn0	1	0	0	MDmn2	MDmn1	MDmn0
	0/1	0						0		0				1	0	0

(b) Serial communication operation setting register mn (SCRmn)... Do not manipulate the bits of this register, except the TXEmn and RXEmn bits, during data transmission/reception.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SCRmn	TXEmn	RXEmn	DAPmn	CKPmn	0	EOCmn	PTCmn1	PTCmn0	DIRmn	0	SLCmn1	SLCmn0	0	1	DLSmn1	DLSmn0
	1	0	0	0		0	0	0	0		0	1			1	1

(c) Serial data register mn (SDRmn) (lower 8 bits: SIOr)... During data transmission/reception, valid only lower 8-bits (SIOr)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SDRmn	Baud rate setting Note 1							0	Transmit data setting							

SIOr

(d) Serial output register m (SOm)... Do not manipulate this register during data transmission/reception.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SOm	0	0	0	0	1	CKOm2	1	CKOm0	0	0	0	0	1	SOm2	1	SOm0
						0/1 Note 2		0/1 Note 2						0/1 Note 2		0/1 Note 2

(e) Serial output enable register m (SOEm)... Do not manipulate this register during data transmission/reception

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SOEm	0	0	0	0	0	0	0	0	0	0	0	0	0	SOEm2	0	SOEm0
														1		1

(f) Serial channel start register m (SSm)... Do not manipulate this register during data transmission/reception.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SSm	0	0	0	0	0	0	0	0	0	0	0	0	SSm3	SSm2	SSm1	SSm0
													×	0/1	×	0/1

Note 1. Because the setting is completed by address field transmission, setting is not required.

Note 2. The value varies depending on the communication data during communication operation.

Remark 1. m: Unit number (m = 0, 1), n: Channel number (n = 0, 2), r: IIC number (r = 00, 10, 20), mn = 00, 02, 10

Remark 2. : Setting is fixed in the IIC mode,

: Setting disabled (set to the initial value)

×: Bit that cannot be used in this mode (set to the initial value when not used in any mode)

0/1: Set to 0 or 1 depending on the usage of the user

(2) Processing flow

Figure 20 - 133 Timing Chart of Data Transmission

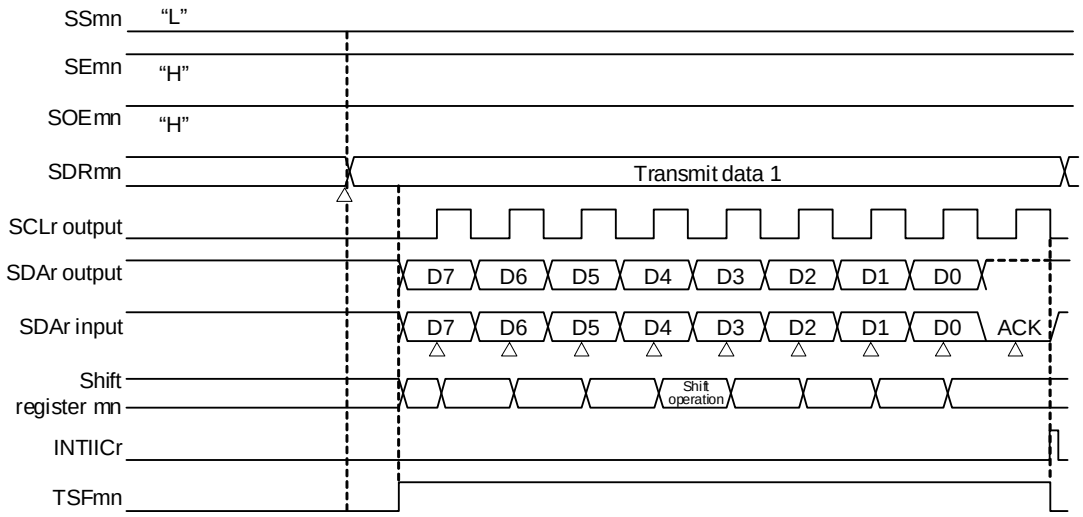
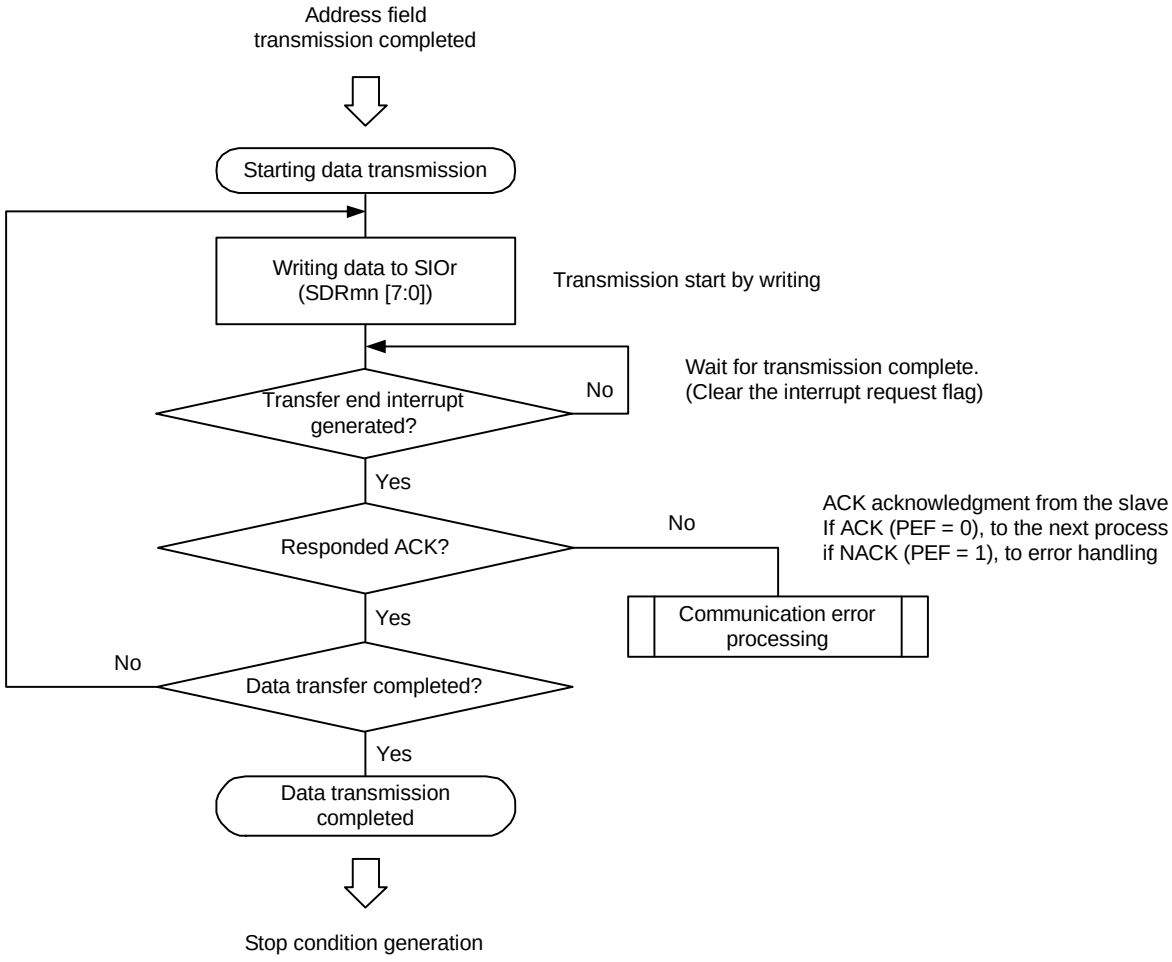


Figure 20 - 134 Flowchart of Simplified I²C Data Transmission



20.9.3 Data reception

Data reception is an operation to receive data to the target for transfer (slave) after transmission of an address field. After all data are received to the slave, a stop condition is generated and the bus is released.

Simplified I²C	IIC00	IIC10	IIC20
Target channel	Channel 0 of SAU0	Channel 2 of SAU0	Channel 0 of SAU1
Pins used	SCL00, SDA00 Note 1	SCL10, SDA10 Note 1	SCL20, SDA20 Note 1
Interrupt	INTIIC00	INTIIC10	INTIIC20
	Transfer end interrupt only (Setting the buffer empty interrupt is prohibited.)		
Error detection flag	Overrun error detection flag (OVFmn) only		
Transfer data length	8 bits		
Transfer rate Note 2	Max. fMCK/4 [Hz] (SDRmn[15:9] = 1 or more) fMCK: Operation clock frequency of target channel However, the following condition must be satisfied in each mode of I²C. • Max. 1 MHz (fast mode plus) • Max. 400 kHz (fast mode) • Max. 100 kHz (standard mode)		
Data level	Non-reversed output (default: high level)		
Parity bit	No parity bit		
Stop bit	Appending 1 bit (ACK transmission)		
Data direction	MSB first		

Note 1. To perform communication via simplified I²C, set the N-ch open-drain output (VDD tolerance mode (POMxx = 1) with the port output mode register (POMxx). For details, see **4.4 Registers Controlling Port Function** and **4.6 Register Settings When Using Alternate Function**.
When IIC00, IIC10, or IIC20 is communicating with an external device with a different potential, set the N-ch open-drain output (VDD tolerance mode (POMxx = 1) also for the clock input/output pins (SCL00, SCL10, SCL20).
For details, see **4.5.4 Handling different potential (1.8 V Note, 2.5 V, 3 V) by using I/O buffers**.

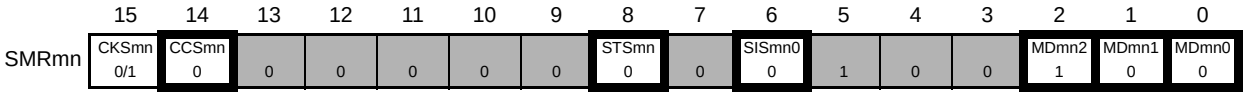
Note 2. Use this operation within a range that satisfies the conditions above and the peripheral functions characteristics in the electrical specifications (see **CHAPTER 38** or **CHAPTER 39 ELECTRICAL SPECIFICATIONS**).

Remark m: Unit number (m = 0, 1), n: Channel number (n = 0, 2), mn = 00, 02, 10

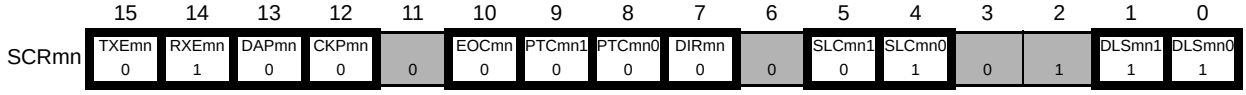
(1) Register setting

Figure 20 - 135 Example of Contents of Registers for Data Reception of Simplified I²C (IIC00, IIC10, IIC20)

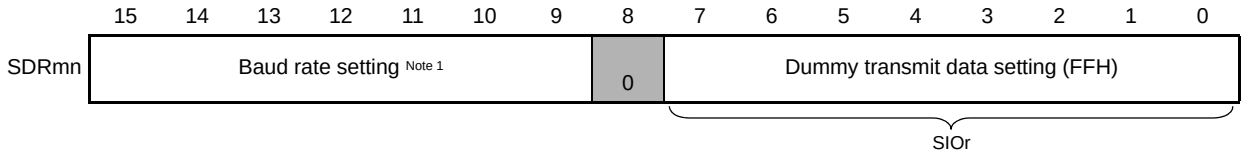
(a) Serial mode register mn (SMRmn)... Do not manipulate this register during data transmission/reception.



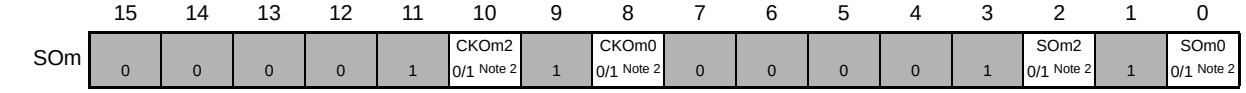
(b) Serial communication operation setting register mn (SCRmn)... Do not manipulate the bits of this register, except the TXEmn and RXEmn bits, during data transmission/reception.



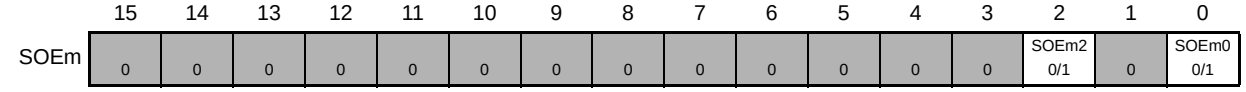
(c) Serial data register mn (SDRmn) (lower 8 bits: SIOr)



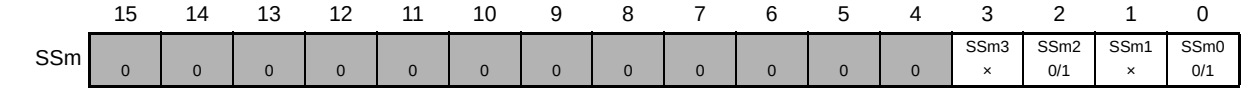
(d) Serial output register m (SOm)... Do not manipulate this register during data transmission/reception.



(e) Serial output enable register m (SOEm)... Do not manipulate this register during data transmission/reception.



(f) Serial channel start register m (SSm)... Do not manipulate this register during data transmission/reception.



Note 1. The baud rate setting is not required because the baud rate has already been set when the address field was transmitted.

Note 2. The value varies depending on the communication data during communication operation.

Remark 1. m: Unit number (m = 0, 1), n: Channel number (n = 0, 2), r: IIC number (r = 00, 10, 20), mn = 00, 02, 10

Remark 2. ■: Setting is fixed in the IIC mode,

▒: Setting disabled (set to the initial value)

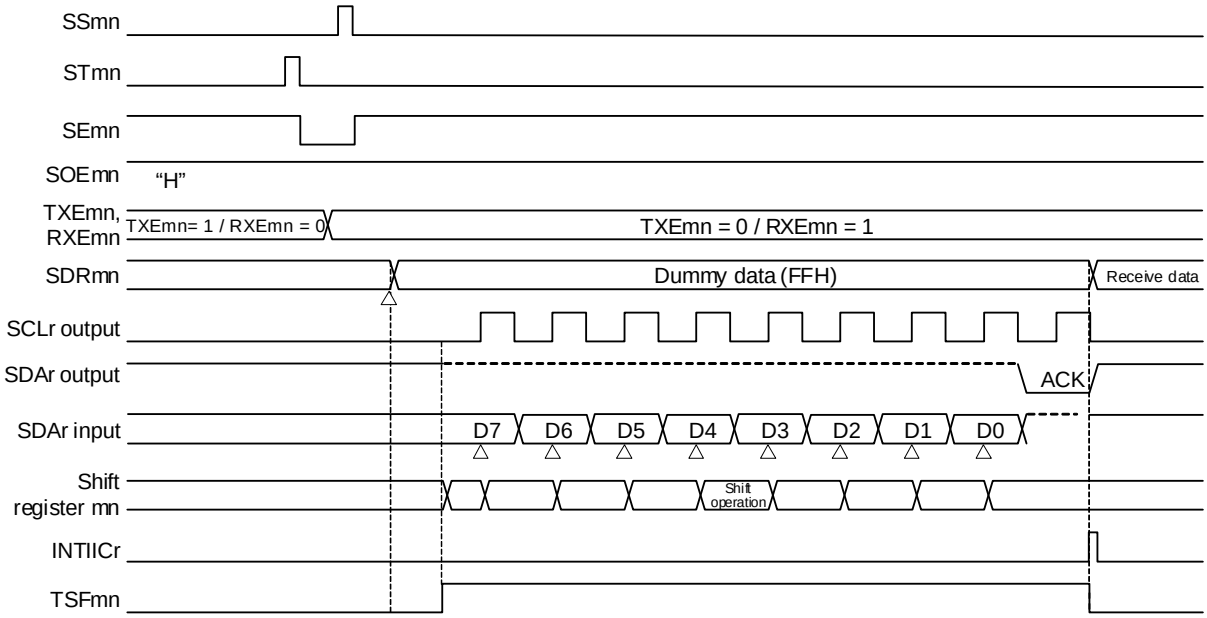
×: Bit that cannot be used in this mode (set to the initial value when not used in any mode)

0/1: Set to 0 or 1 depending on the usage of the user

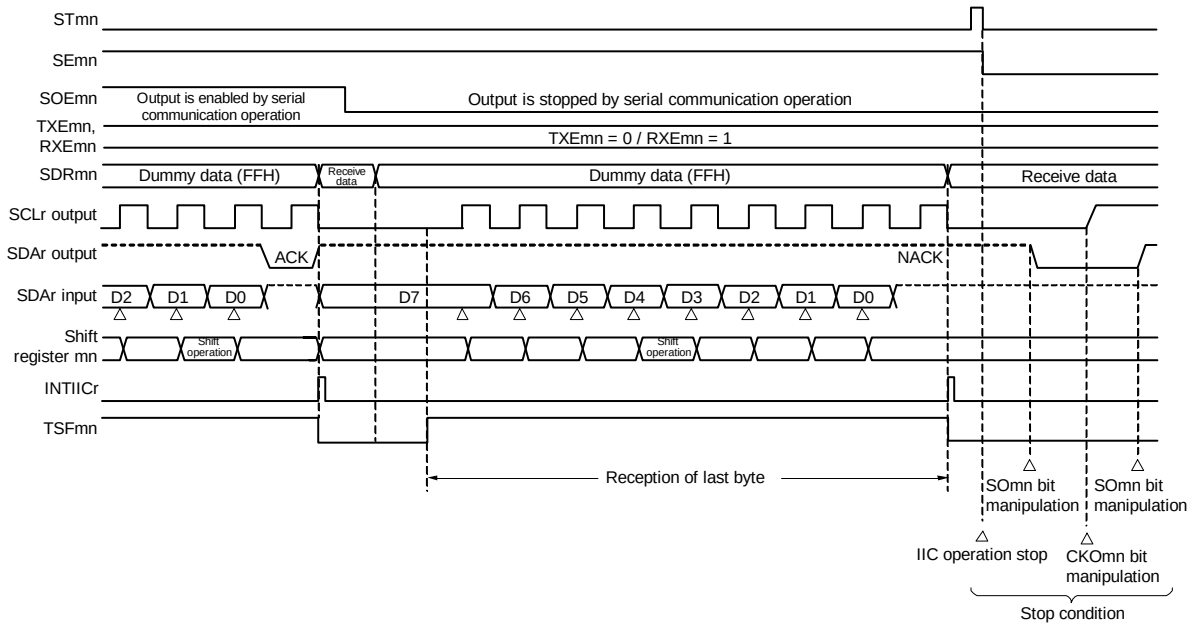
(2) Processing flow

Figure 20 - 136 Timing Chart of Data Reception

(a) When starting data reception

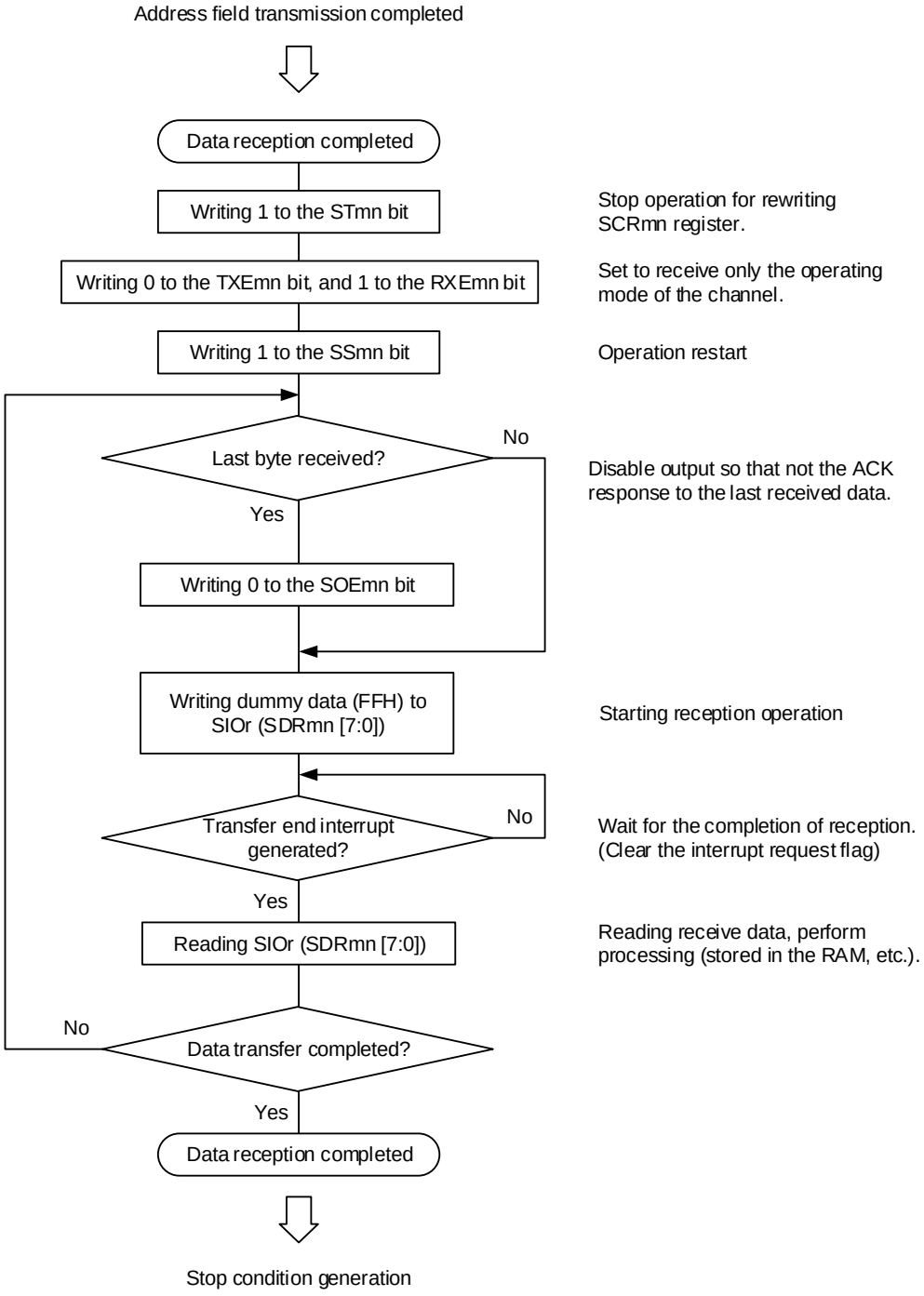


(b) When receiving last data



Remark m: Unit number (m = 0, 1), n: Channel number (n = 0, 2), r: IIC number (r = 00, 10, 20), mn = 00, 02, 10

Figure 20 - 137 Flowchart of Data Reception



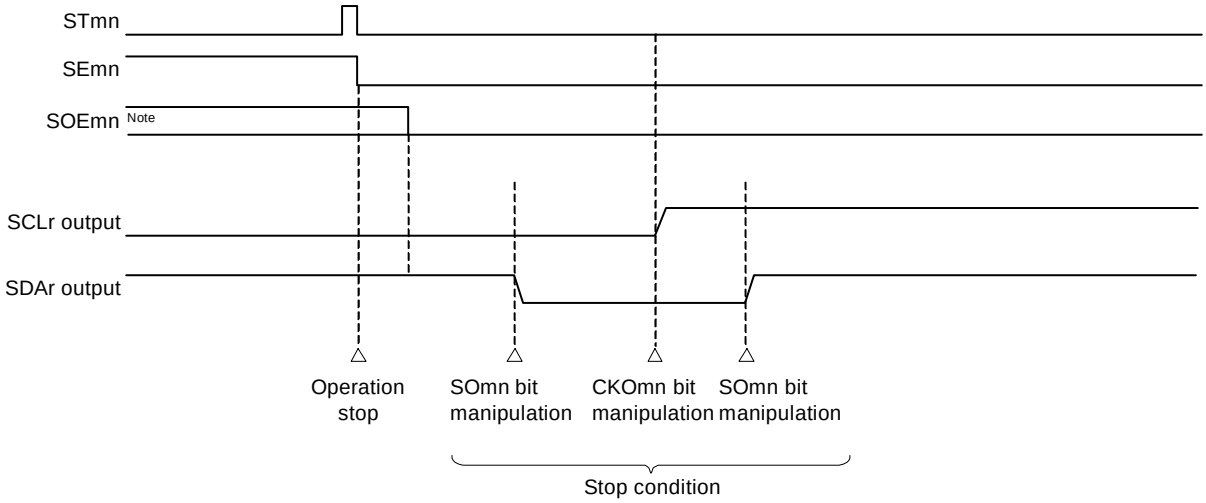
Caution ACK is not output when the last data is received (NACK). Communication is then completed by setting "1" to the STmn bit of serial channel stop register m (STm) to stop operation and generating a stop condition.

20.9.4 Stop condition generation

After all data are transmitted to or received from the target slave, a stop condition is generated and the bus is released.

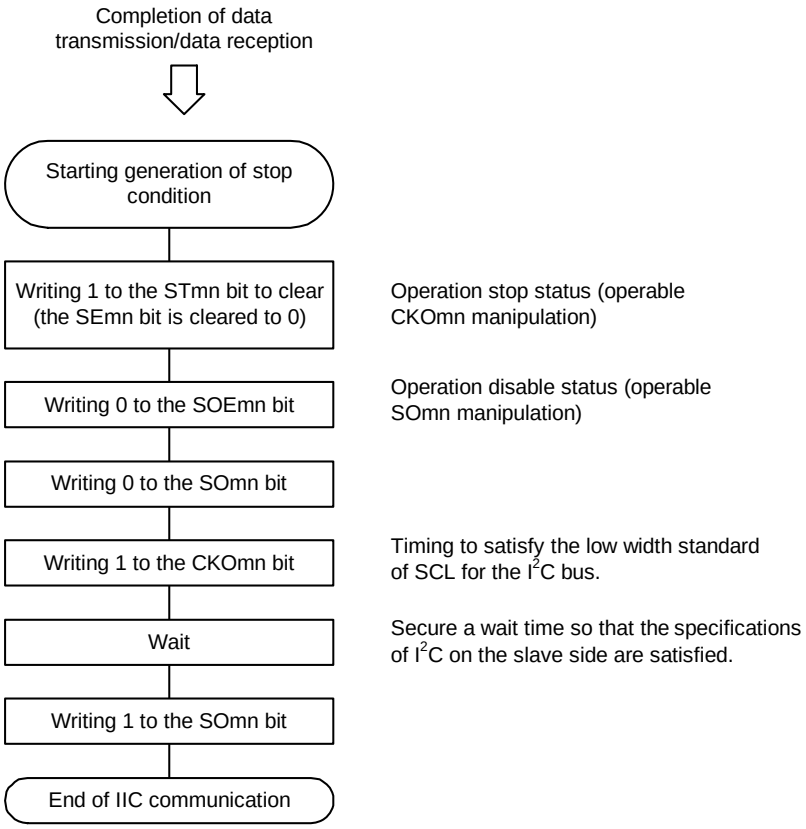
(1) Processing flow

Figure 20 - 138 Timing Chart of Stop Condition Generation



Note During a receive operation, the SOEmn bit of serial output enable register m (SOEm) is cleared to 0 before receiving the last data.

Figure 20 - 139 Flowchart of Stop Condition Generation



20.9.5 Calculating transfer rate

The transfer rate for simplified I^2C (IIC00, IIC10) communication can be calculated by the following expressions.

(Transfer rate) = {Operation clock (f_{MCK}) frequency of target channel} ÷ (SDRmn[15:9] + 1) ÷ 2

Caution SDRmn[15:9] must not be set to 00000000B. Be sure to set a value of 00000001B or greater for SDRmn[15:9]. The duty ratio of the SCL signal output by the simplified I^2C is 50%. The I^2C bus specifications define that the low-level width of the SCL signal is longer than the high-level width. If 400 kbps (fast mode) or 1 Mbps (fast mode plus) is specified, therefore, the low-level width of the SCL output signal becomes shorter than the value specified in the I^2C bus specifications. Make sure that the SDRmn[15:9] value satisfies the I^2C bus specifications.

Remark 1. The value of SDRmn[15:9] is the value of bits 15 to 9 of the SDRmn register (0000001B to 1111111B) and therefore is 1 to 127.

Remark 2. m: Unit number (m = 0, 1), n: Channel number (n = 0, 2), mn = 00, 02, 10

The operation clock (f_{MCK}) is determined by serial clock select register m (SPSm) and bit 15 (CKSmn) of serial mode register mn (SMRmn).

Table 20 - 6 Selection of Operation Clock For Simplified I²C

SMRmn Register	SPSm Register								Operation Clock (f_{MCK}) Note	
CKSmn	PRS m13	PRS m12	PRS m11	PRS m10	PRS m03	PRS m02	PRS m01	PRS m00		f_{CLK} = 24 MHz
0	×	×	×	×	0	0	0	0	f_{CLK}	24 MHz
	×	×	×	×	0	0	0	1	$f_{CLK}/2$	12 MHz
	×	×	×	×	0	0	1	0	$f_{CLK}/2^2$	6 MHz
	×	×	×	×	0	0	1	1	$f_{CLK}/2^3$	3 MHz
	×	×	×	×	0	1	0	0	$f_{CLK}/2^4$	1.5 MHz
	×	×	×	×	0	1	0	1	$f_{CLK}/2^5$	750 kHz
	×	×	×	×	0	1	1	0	$f_{CLK}/2^6$	375 kHz
	×	×	×	×	0	1	1	1	$f_{CLK}/2^7$	187.5 kHz
	×	×	×	×	1	0	0	0	$f_{CLK}/2^8$	93.8 kHz
	×	×	×	×	1	0	0	1	$f_{CLK}/2^9$	46.9 kHz
	×	×	×	×	1	0	1	0	$f_{CLK}/2^{10}$	23.4 kHz
	×	×	×	×	1	0	1	1	$f_{CLK}/2^{11}$	11.7 kHz
1	0	0	0	0	×	×	×	×	f_{CLK}	24 MHz
	0	0	0	1	×	×	×	×	$f_{CLK}/2$	12 MHz
	0	0	1	0	×	×	×	×	$f_{CLK}/2^2$	6 MHz
	0	0	1	1	×	×	×	×	$f_{CLK}/2^3$	3 MHz
	0	1	0	0	×	×	×	×	$f_{CLK}/2^4$	1.5 MHz
	0	1	0	1	×	×	×	×	$f_{CLK}/2^5$	750 kHz
	0	1	1	0	×	×	×	×	$f_{CLK}/2^6$	375 kHz
	0	1	1	1	×	×	×	×	$f_{CLK}/2^7$	187.5 kHz
	1	0	0	0	×	×	×	×	$f_{CLK}/2^8$	93.8 kHz
	1	0	0	1	×	×	×	×	$f_{CLK}/2^9$	46.9 kHz
	1	0	1	0	×	×	×	×	$f_{CLK}/2^{10}$	23.4 kHz
	1	0	1	1	×	×	×	×	$f_{CLK}/2^{11}$	11.7 kHz
Other than above									Setting prohibited	

Note When changing the clock selected for f_{CLK} (by changing the system clock control register (CKC) value), do so after having stopped (serial channel stop register m (STm) = 000FH) the operation of the serial array unit (SAU).

Remark 1. ×: Don't care

Remark 2. m: Unit number (m = 0, 1), n: Channel number (n = 0, 2), mn = 00, 02, 10

Here is an example of setting an I²C transfer rate where $f_{MCK} = f_{CLK}$ = 24 MHz.

I²C Transfer Mode (Desired Transfer Rate)	f_{CLK} = 24 MHz			
	Operation Clock (f_{MCK})	SDRmn[15:9]	Calculated Transfer Rate	Error from Desired Transfer Rate
100 kHz	$f_{CLK}/2$	59	100 kHz	0.0%
400 kHz	f_{CLK}	31	375 kHz	6.25% Note
1 MHz	f_{CLK}	14	0.80 MHz	20.0% Note

Note The error cannot be set to about 0% because the duty ratio of the SCL signal is 50%.

20.9.6 Procedure for processing errors that occurred during simplified I²C (IIC00, IIC10, IIC20) communication

The procedure for processing errors that occurred during simplified I²C (IIC00, IIC10, IIC20) communication is described in **Figure 20 - 140** and **20 - 141**.

Figure 20 - 140 Processing Procedure in Case of Overrun Error

Software Manipulation	Hardware Status	Remark
Reads serial data register mn (SDRmn). →	The BFFmn bit of the SSRmn register is set to 0 and channel n is enabled to receive data.	This is to prevent an overrun error if the next reception is completed during error processing.
Reads serial status register mn (SSRmn).		The error type is identified and the read value is used to clear the error flag.
Writes 1 to serial flag clear trigger register mn (SIRmn). →	The error flag is cleared.	The error only during reading can be cleared, by writing the value read from the SSRmn register to the SIRmn register without modification.

Figure 20 - 141 Processing Procedure in Case of ACK error in Simplified I²C Mode

Software Manipulation	Hardware Status	Remark
Reads serial status register mn (SSRmn).		Error type is identified and the read value is used to clear error flag.
Writes serial flag clear trigger register mn (SIRmn). →	Error flag is cleared.	Error can be cleared only during reading, by writing the value read from the SSRmn register to the SIRmn register without modification.
Sets the STmn bit of serial channel stop register m (STm) to 1. →	The SEmn bit of serial channel enable status register m (SEm) is set to 0 and channel n stops operation.	Slave is not ready for reception because ACK is not returned. Therefore, a stop condition is created, the bus is released, and communication is started again from the start condition. Or, a restart condition is generated and transmission can be redone from address transmission.
Creates stop condition.		
Creates start condition.		
Sets the SSmn bit of serial channel start register m (SSm) to 1. →	The SEmn bit of serial channel enable status register m (SEm) is set to 1 and channel n is enabled to operate.	

Remark m: Unit number (m = 0, 1), n: Channel number (n = 0, 2), r: IIC number (r = 00, 10, 20), mn = 00, 02, 10

CHAPTER 21 SERIAL INTERFACE IICA

21.1 Functions of Serial Interface IICA

Serial interface IICA has the following three modes.

(1) Operation stop mode

This mode is used when serial transfers are not performed. It can therefore be used to reduce power consumption.

(2) I^2C bus mode (multimaster supported)

This mode is used for 8-bit data transfers with several devices via two lines: a serial clock (SCLAn) line and a serial data bus (SDAAn) line.

This mode complies with the I^2C bus format and the master device can generated “start condition”, “address”, “transfer direction specification”, “data”, and “stop condition” data to the slave device, via the serial data bus. The slave device automatically detects these received status and data by hardware. This function can simplify the part of application program that controls the I^2C bus.

Since the SCLAn and SDAAn pins are used for open drain outputs, serial interface IICA requires pull-up resistors for the serial clock line and the serial data bus line.

(3) Wakeup mode

The STOP mode can be released by generating an interrupt request signal (INTIICAn) when an extension code from the master device or a local address has been received while in STOP mode. This can be set by using the WUPn bit of IICA control register n1 (IICCTLn1).

Figure 21 - 1 shows a block diagram of serial interface IICA

Remark n = 0

Figure 21 - 1 Block Diagram of Serial Interface IICA

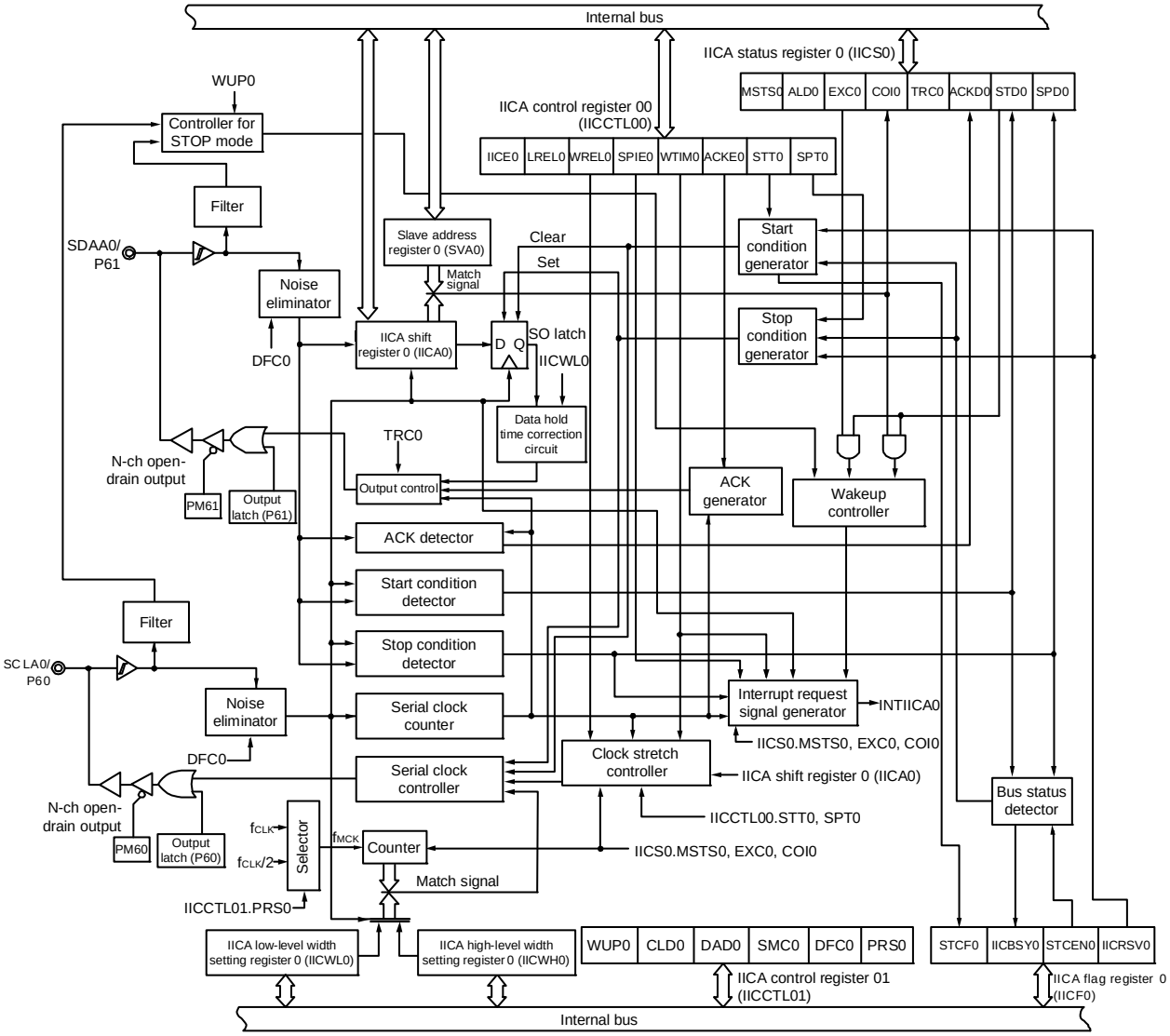
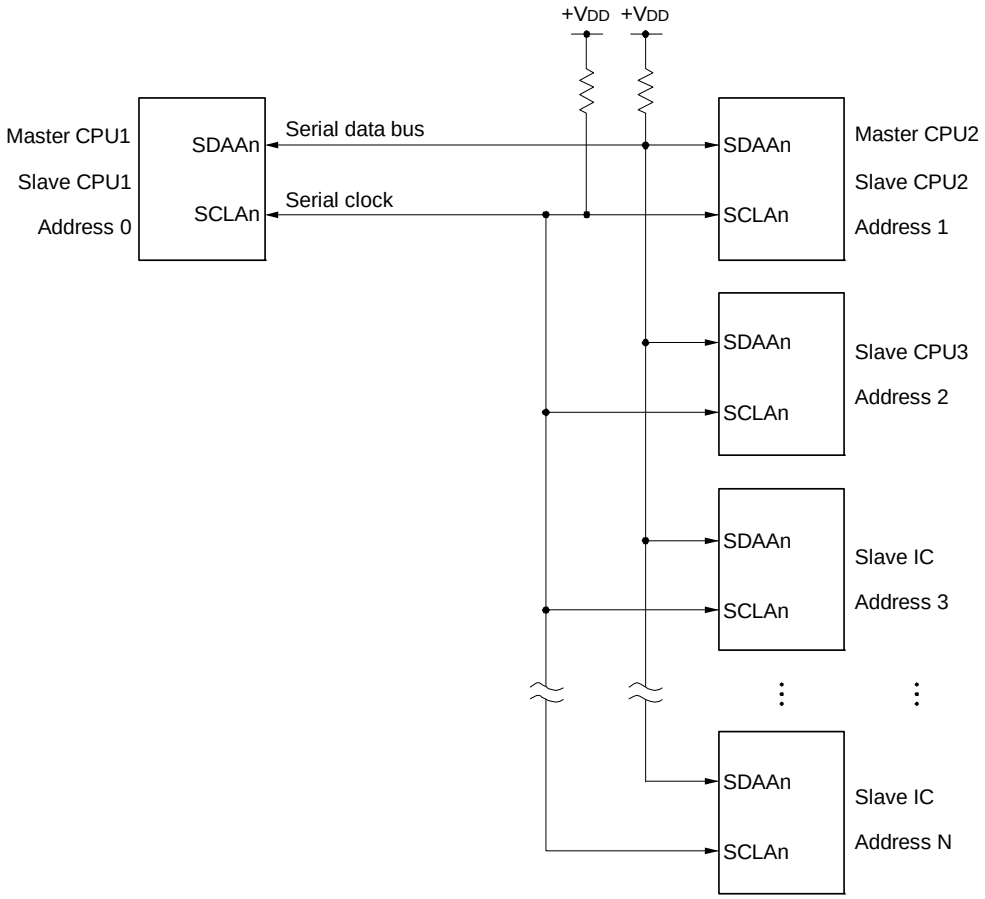


Figure 21 - 2 shows a serial bus configuration example.

Figure 21 - 2 Serial Bus Configuration Example Using I²C Bus



Remark n = 0

21.2 Configuration of Serial Interface IICA

Serial interface IICA includes the following hardware.

Table 21 - 1 Configuration of Serial Interface IICA

Item	Configuration
Registers	IICA shift register n (IICAn) Slave address register n (SVAn)
Control registers	Peripheral enable register 0 (PER0) IICA control register n0 (IICCTLn0) IICA status register n (IICSn) IICA flag register n (IICFn) IICA control register n1 (IICCTLn1) IICA low-level width setting register n (IICWLn) IICA high-level width setting register n (IICWHn) Port mode register 6 (PM6) Port register 6 (P6)

Remark n = 0

(1) IICA shift register n (IICAn)

The IICAn register is used to convert 8-bit serial data to 8-bit parallel data and vice versa in synchronization with the serial clock. The IICAn register can be used for both transmission and reception.

The actual transmit and receive operations can be controlled by writing and reading operations to the IICAn register.

Cancel the clock stretch state and start data transfer by writing data to the IICAn register during the clock stretch period.

The IICAn register can be set by an 8-bit memory manipulation instruction.

Reset signal generation clears IICAn to 00H.

Figure 21 - 3 Format of IICA shift register n (IICAn)

Address: FFF50H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
IICAn								

Caution 1. Do not write data to the IICAn register during data transfer.

Caution 2. Write or read the IICAn register only during the clock stretch period. Accessing the IICAn register in a communication state other than during the clock stretch period is prohibited. When the device serves as the master, however, the IICAn register can be written only once after the communication trigger bit (STTn) is set to 1.

Caution 3. When communication is reserved, write data to the IICAn register after the interrupt triggered by a stop condition is detected.

Remark n = 0

(2) Slave address register n (SVAn)

This register stores seven bits of local addresses {A6, A5, A4, A3, A2, A1, A0} when in slave mode.

The SVAn register can be set by an 8-bit memory manipulation instruction.

However, rewriting to this register is prohibited while STDn = 1 (while the start condition is detected).

Reset signal generation clears the SVAn register to 00H.

Figure 21 - 4 Format of Slave address register n (SVAn)

Address: F0234H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
SVAn	A6	A5	A4	A3	A2	A1	A0	0 Note

Note Bit 0 is fixed to 0.

(3) SO latch

The SO latch is used to retain the SDAAn pin's output level.

(4) Wakeup controller

This circuit generates an interrupt request (INTIICAn) when the address received by this register matches the address value set to the slave address register n (SVAn) or when an extension code is received.

(5) Serial clock counter

This counter counts the serial clocks that are output or input during transmit/receive operations and is used to verify that 8-bit data was transmitted or received.

(6) Interrupt request signal generator

This circuit controls the generation of interrupt request signals (INTIICAn).

An I^2C interrupt request is generated by the following two triggers.

- Falling edge of eighth or ninth clock of the serial clock (set by the WTIMn bit)
- Interrupt request generated when a stop condition is detected (set by the SPIEn bit)

Remark WTIMn bit: Bit 3 of IICA control register n0 (IICCTLn0)
SPIEn bit: Bit 4 of IICA control register n0 (IICCTLn0)

(7) Serial clock controller

In master mode, this circuit generates the clock output via the SCLAn pin from a sampling clock.

(8) Clock stretch controller

This circuit controls the clock stretch.

Remark n = 0

(9) ACK generator, stop condition detector, start condition detector, and ACK detector

These circuits generate and detect each status.

(10) Data hold time correction circuit

This circuit generates the hold time for data corresponding to the falling edge of the serial clock.

(11) Start condition generator

This circuit generates a start condition when the STTn bit is set to 1.

However, in the communication reservation disabled status (IICRSVn bit = 1), when the bus is not released (IICBSYn bit = 1), start condition requests are ignored and the STCFn bit is set to 1.

(12) Stop condition generator

This circuit generates a stop condition when the SPTn bit is set to 1.

(13) Bus status detector

This circuit detects whether or not the bus is released by detecting start conditions and stop conditions.

However, as the bus status cannot be detected immediately following operation, the initial status is set by the STCENn bit.

Remark 1. STTn bit: Bit 1 of IICA control register n0 (IICCTLn0)
SPTn bit: Bit 0 of IICA control register n0 (IICCTLn0)
IICRSVn bit: Bit 0 of IICA flag register n (IICFn)
IICBSYn bit: Bit 6 of IICA flag register n (IICFn)
STCFn bit: Bit 7 of IICA flag register n (IICFn)
STCENn bit: Bit 1 of IICA flag register n (IICFn)

Remark 2. n = 0

21.3 Registers Controlling Serial Interface IICA

Serial interface IICA is controlled by the following registers.

- Peripheral enable register 0 (PER0)
- IICA control register n0 (IICCTLn0)
- IICA flag register n (IICFn)
- IICA status register n (IICSn)
- IICA control register n1 (IICCTLn1)
- IICA low-level width setting register n (IICWLn)
- IICA high-level width setting register n (IICWHn)
- Port mode register 6 (PM6)
- Port register 6 (P6)

Remark n = 0

21.3.1 Peripheral enable register 0 (PER0)

This register is used to enable or disable supplying the clock to the peripheral hardware. Clock supply to the hardware that is not used is also stopped so as to decrease the power consumption and noise.

When serial interface IICAn is used, be sure to set bit 4 (IICAnEN) of this register to 1.

The PER0 register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 21 - 5 Format of Peripheral enable register 0 (PER0)

Address: F00F0H After reset: 00H R/W

Symbol	<7>	6	<5>	<4>	<3>	<2>	1	<0>
PER0	RTCWEN	0	ADCEN	IICAnEN	SAU1EN	SAU0EN	0	TAU0EN

IICAnEN	Control of serial interface IICAn input clock supply
0	Stops input clock supply. • SFR used by serial interface IICAn cannot be written. • Serial interface IICAn is in the reset status.
1	Enables input clock supply. • SFR used by serial interface IICAn can be read/written.

Caution 1. When setting serial interface IICA, be sure to set the following registers first while the IICAnEN bit is set to 1. If IICAnEN = 0, the control registers of serial interface IICA are set to their initial values, and writing to them is ignored (except for port mode register 6 (PM6) and port register 6 (P6)).

- **IICA control register n0 (IICCTLn0)**
- **IICA flag register n (IICFn)**
- **IICA status register n (IICSn)**
- **IICA control register n1 (IICCTLn1)**
- **IICA low-level width setting register n (IICWLn)**
- **IICA high-level width setting register n (IICWHn)**

Caution 2. Be sure to clear bits 1 and 6 to 0.

Remark n = 0

21.3.2 IICA control register n0 (IICCTLn0)

This register is used to enable/stop I^2C operations, set clock stretch timing, and set other I^2C operations.

The IICCTLn0 register can be set by a 1-bit or 8-bit memory manipulation instruction. However, set the SPIEn, WTIMn, and ACKEn bits while IICEn = 0 or during the clock stretch period. These bits can be set at the same time when the IICEn bit is set from “0” to “1”.

Reset signal generation clears this register to 00H.

Remark n = 0

Figure 21 - 6 Format of IICA control register n0 (IICCTLn0) (1/4)

Address: F0230H After reset: 00H R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
IICCTLn0	IICEn	LRELn	WRELn	SPIEn	WTIMn	ACKEn	STTn	SPTn

IICEn	I^2C operation enable
0	Stop operation. Reset the IICA status register n (IICSn) Note 1. Stop internal operation.
1	Enable operation.
Be sure to set this bit (1) while the SCLAn and SDAAn lines are at high level.	
Condition for clearing (IICEn = 0)	Condition for setting (IICEn = 1)
• Cleared by instruction • Reset	• Set by instruction

LRELn Notes 2, 3	Exit from communications
0	Normal operation
1	This exits from the current communications and sets standby mode. This setting is automatically cleared to 0 after being executed. Its uses include cases in which a locally irrelevant extension code has been received. The SCLAn and SDAAn lines are set to high impedance. The following flags of IICA control register n0 (IICCTLn0) and the IICA status register n (IICSn) are cleared to 0. • STTn • SPTn • MSTSn • EXCn • COIn • TRCn • ACKDn • STDn
The standby mode following exit from communications remains in effect until the following communications entry conditions are met. • After a stop condition is detected, restart is in master mode. • An address match or extension code reception occurs after the start condition.	
Condition for clearing (LRELn = 0)	Condition for setting (LRELn = 1)
• Automatically cleared after execution • Reset	• Set by instruction

WRELn Notes 2, 3	Clock stretch cancellation
0	Do not cancel clock stretch
1	Cancel clock stretch. This setting is automatically cleared after clock stretch is canceled.
When the WRELn bit is set (clock stretch canceled) during the clock stretch period at the ninth clock pulse in the transmission status (TRCn = 1), the SDAAn line goes into the high impedance state (TRCn = 0).	
Condition for clearing (WRELn = 0)	Condition for setting (WRELn = 1)
• Automatically cleared after execution • Reset	• Set by instruction

Note 1. The IICA shift register n (IICAn), the STCFn and IICBSYn bits of the IICA flag register n (IICFn), and the CLDn and DADn bits of IICA control register n1 (IICCTLn1) are reset.

Note 2. The signal of this bit is invalid while IICEn is 0.

Note 3. When the LRELn and WRELn bits are read, 0 is always read.

Caution **If the operation of I^2C is enabled (IICEn = 1) when the SCLAn line is high level, the SDAAn line is low level, and the digital filter is turned on (DFCn bit of IICCTLn1 register = 1), a start condition will be inadvertently detected immediately. In this case, set (1) the LRELn bit by using a 1-bit memory manipulation instruction immediately after enabling operation of I^2C (IICEn = 1).**

Remark n = 0

Figure 21 - 7 Format of IICA control register n0 (IICCTLn0) (2/4)

SPIEn Note 1	Enable/disable generation of interrupt request when stop condition is detected
0	Disable
1	Enable
If the WUPn bit of IICA control register n1 (IICCTLn1) is 1, no stop condition interrupt will be generated even if SPIEn = 1.	
Condition for clearing (SPIEn = 0)	Condition for setting (SPIEn = 1)
• Cleared by instruction • Reset	• Set by instruction

WTIMn Note 1	Control of clock stretch and interrupt request generation
0	Interrupt request is generated at the eighth clock's falling edge. Master mode: After output of eight clocks, clock output is set to low level and clock stretch is set. Slave mode: After input of eight clocks, the clock is set to low level and clock stretch is set for master device.
1	Interrupt request is generated at the ninth clock's falling edge. Master mode: After output of nine clocks, clock output is set to low level and clock stretch is set. Slave mode: After input of nine clocks, the clock is set to low level and clock stretch is set for master device.
An interrupt is generated at the falling edge of the ninth clock during address transfer independently of the setting of this bit. The setting of this bit is valid when the address transfer is completed. When in master mode, a clock stretch is inserted at the falling edge of the ninth clock during address transfers. For a slave device that has received a local address, a clock stretch is inserted at the falling edge of the ninth clock after an acknowledge (ACK) is issued. However, when the slave device has received an extension code, a clock stretch is inserted at the falling edge of the eighth clock.	
Condition for clearing (WTIMn = 0)	Condition for setting (WTIMn = 1)
• Cleared by instruction • Reset	• Set by instruction

ACKEn Notes 1, 2	Acknowledgment control
0	Disable acknowledgment.
1	Enable acknowledgment. During the ninth clock period, the SDAAn line is set to low level.
Condition for clearing (ACKEn = 0)	Condition for setting (ACKEn = 1)
• Cleared by instruction • Reset	• Set by instruction

Note 1. The signal of this bit is invalid while IICEn is 0. Set this bit during that period.

Note 2. The set value is invalid during address transfer and if the code is not an extension code.
When the device serves as a slave and the addresses match, an acknowledgment is generated regardless of the set value.

Remark n = 0

Figure 21 - 8 Format of IICA control register n0 (IICCTLn0) (3/4)

STTn Notes 1, 2	Start condition trigger
0	Do not generate a start condition.
1	When bus is released (in standby state, when IICBSYn = 0): If this bit is set (1), a start condition is generated (startup as the master). When a third party is communicating: • When communication reservation function is enabled (IICRSVn = 0) Functions as the start condition reservation flag. When set to 1, automatically generates a start condition after the bus is released. • When communication reservation function is disabled (IICRSVn = 1) Even if this bit is set (1), the STTn bit is cleared and the STTn clear flag (STCFn) is set (1). No start condition is generated. In the clock stretch state (when master device): Generates a restart condition after releasing the clock stretch.

Cautions concerning set timing
- For master reception: Cannot be set to 1 during transfer. Can be set to 1 only in the clock stretch period when the ACKEn bit has been cleared to 0 and slave has been notified of final reception.
- For master transmission: A start condition cannot be generated normally during the acknowledge period. Set to 1 during the clock stretch period that follows output of the ninth clock.
- Cannot be set to 1 at the same time as stop condition trigger (SPTn).
- Once STTn is set (1), setting it again (1) before the clear condition is met is not allowed.

Condition for clearing (STTn = 0)	Condition for setting (STTn = 1)
• Cleared by setting the STTn bit to 1 while communication reservation is prohibited. • Cleared by loss in arbitration • Cleared after start condition is generated by master device • Cleared by LRELn = 1 (exit from communications) • When IICEn = 0 (operation stop) • Reset	• Set by instruction

Note 1. The signal of this bit is invalid while IICEn is 0.
Note 2. The STTn bit is always read as 0.

Remark 1. IICRSVn: Bit 0 of IICA flag register n (IICFn)
STCFn: Bit 7 of IICA flag register n (IICFn)
Remark 2. n = 0

Figure 21 - 9 Format of IICA control register n0 (IICCTLn0) (4/4)

SPTn Note	Stop condition trigger
0	Stop condition is not generated.
1	Stop condition is generated (termination of master device's transfer).

Cautions concerning set timing
- For master reception: Cannot be set to 1 during transfer. Can be set to 1 only in the clock stretch period when the ACKEn bit has been cleared to 0 and slave has been notified of final reception.
- For master transmission: A stop condition cannot be generated normally during the acknowledge period. Therefore, set it during the clock stretch period that follows output of the ninth clock.
- Cannot be set to 1 at the same time as start condition trigger (STTn).
- The SPTn bit can be set to 1 only when in master mode.
- When the WTIMn bit has been cleared to 0, if the SPTn bit is set to 1 during the clock stretch period that follows output of eight clocks, note that a stop condition will be generated during the high-level period of the ninth clock. The WTIMn bit should be changed from 0 to 1 during the clock stretch period following the output of eight clocks, and the SPTn bit should be set to 1 during the clock stretch period that follows the output of the ninth clock.
- Once SPTn is set (1), setting it again (1) before the clear condition is met is not allowed.

Condition for clearing (SPTn = 0)	Condition for setting (SPTn = 1)
• Cleared by loss in arbitration • Automatically cleared after stop condition is detected • Cleared by LRELn = 1 (exit from communications) • When IICEn = 0 (operation stop) • Reset	• Set by instruction

Note The SPTn bit is always read as 0.

Caution **When bit 3 (TRCn) of the IICA status register n (IICSn) is set to 1 (transmission status), bit 5 (WRELn) of IICA control register n0 (IICCTLn0) is set to 1 during the ninth clock and clock stretch is canceled, after which the TRCn bit is cleared (reception status) and the SDAAn line is set to high impedance. Release the clock stretch performed while the TRCn bit is 1 (transmission status) by writing to the IICA shift register n.**

Remark 1. Bit 0 (SPTn) becomes 0 when it is read after data setting.
Remark 2. n = 0

21.3.3 IICA status register n (IICSn)

This register indicates the status of I^2C.

The IICSn register is read by a 1-bit or 8-bit memory manipulation instruction only when STTn = 1 and during the clock stretch period.

Reset signal generation clears this register to 00H.

Caution Reading the IICSn register while the address match wakeup function is enabled (WUPn = 1) in STOP mode is prohibited. When the WUPn bit is changed from 1 to 0 (wakeup operation is stopped), regardless of the INTIICAn interrupt request, the change in status is not reflected until the next start condition or stop condition is detected. To use the wakeup function, therefore, enable (SPIEn = 1) the interrupt generated by detecting a stop condition and read the IICSn register after the interrupt has been detected.

Remark STTn: bit 1 of IICA control register n0 (IICCTLn0)
WUPn: bit 7 of IICA control register n1 (IICCTLn1)

Figure 21 - 10 Format of IICA status register n (IICSn) (1/3)

Address: FFF51H After reset: 00H R

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
IICSn	MSTSn	ALDn	EXCn	COIn	TRCn	ACKDn	STDn	SPDn

MSTSn	Master status check flag
0	Slave device status or communication standby status
1	Master device communication status

Condition for clearing (MSTSn = 0)	Condition for setting (MSTSn = 1)
• When a stop condition is detected • When ALDn = 1 (arbitration loss) • Cleared by LRELn = 1 (exit from communications) • When the IICEn bit changes from 1 to 0 (operation stop) • Reset	• When a start condition is generated

ALDn	Detection of arbitration loss
0	This status means either that there was no arbitration or that the arbitration result was a “win”.
1	This status indicates the arbitration result was a “loss”. The MSTSn bit is cleared.

Condition for clearing (ALDn = 0)	Condition for setting (ALDn = 1)
• Automatically cleared after the IICSn register is read Note • When the IICEn bit changes from 1 to 0 (operation stop) • Reset	• When the arbitration result is a “loss”.

Note This register is also cleared when a 1-bit memory manipulation instruction is executed for bits other than the IICSn register. Therefore, when using the ALDn bit, read the data of this bit before the data of the other bits.

Remark 1. LRELn: Bit 6 of IICA control register n0 (IICCTLn0)
IICEn: Bit 7 of IICA control register n0 (IICCTLn0)

Remark 2. n = 0

Figure 21 - 11 Format of IICA status register n (IICSn) (2/3)

EXCn	Detection of extension code reception
0	Extension code was not received.
1	Extension code was received.

Condition for clearing (EXCn = 0)	Condition for setting (EXCn = 1)
• When a start condition is detected • When a stop condition is detected • Cleared by LRELn = 1 (exit from communications) • When the IICEn bit changes from 1 to 0 (operation stop) • Reset	• When the higher four bits of the received address data is either “0000” or “1111” (set at the rising edge of the eighth clock).

COIn	Detection of matching addresses
0	Addresses do not match.
1	Addresses match.

Condition for clearing (COIn = 0)	Condition for setting (COIn = 1)
• When a start condition is detected • When a stop condition is detected • Cleared by LRELn = 1 (exit from communications) • When the IICEn bit changes from 1 to 0 (operation stop) • Reset	• When the received address matches the local address (slave address register n (SVAn)) (set at the rising edge of the eighth clock).

TRCn	Detection of transmit/receive status
0	Receive status (other than transmit status). The SDAAn line is set for high impedance.
1	Transmit status. The value in the SOn latch is enabled for output to the SDAAn line (valid starting at the falling edge of the first byte’s ninth clock).

Condition for clearing (TRCn = 0)	Condition for setting (TRCn = 1)
<Both master and slave> • When a stop condition is detected • Cleared by LRELn = 1 (exit from communications) • When the IICEn bit changes from 1 to 0 (operation stop) • Cleared by WRELn = 1 Note (clock stretch cancel) • When the ALDn bit changes from 0 to 1 (arbitration loss) • Reset • When not used for communication (MSTSn, EXCn, COIn = 0) <Master> • When “1” is output to the first byte’s LSB (transfer direction specification bit) <Slave> • When a start condition is detected • When “0” is input to the first byte’s LSB (transfer direction specification bit)	<Master> • When a start condition is generated • When 0 (master transmission) is output to the LSB (transfer direction specification bit) of the first byte (during address transfer) <Slave> • When 1 (slave transmission) is input to the LSB (transfer direction specification bit) of the first byte from the master (during address transfer)

Note When bit 3 (TRCn) of the IICA status register n (IICSn) is set to 1 (transmission status), bit 5 (WRELn) of IICA control register n0 (IICCTLn0) is set to 1 during the ninth clock and clock stretch is canceled, after which the TRCn bit is cleared (reception status) and the SDAAn line is set to high impedance. Release the clock stretch performed while the TRCn bit is 1 (transmission status) by writing to the IICA shift register n.

Remark 1. LRELn: Bit 6 of IICA control register n0 (IICCTLn0)
IICEn: Bit 7 of IICA control register n0 (IICCTLn0)

Remark 2. n = 0

Figure 21 - 12 Format of IICA status register n (IICSn) (3/3)

ACKDn	Detection of acknowledge (ACK)
0	Acknowledge was not detected.
1	Acknowledge was detected.

Condition for clearing (ACKDn = 0)	Condition for setting (ACKDn = 1)
• When a stop condition is detected • At the rising edge of the next byte's first clock • Cleared by LRELn = 1 (exit from communications) • When the IICEn bit changes from 1 to 0 (operation stop) • Reset	• After the SDAAn line is set to low level at the rising edge of SCLAn line's ninth clock

STDn	Detection of start condition
0	Start condition was not detected.
1	Start condition was detected. This indicates that the address transfer period is in effect.

Condition for clearing (STDn = 0)	Condition for setting (STDn = 1)
• When a stop condition is detected • At the rising edge of the next byte's first clock following address transfer • Cleared by LRELn = 1 (exit from communications) • When the IICEn bit changes from 1 to 0 (operation stop) • Reset	• When a start condition is detected

SPDn	Detection of stop condition
0	Stop condition was not detected.
1	Stop condition was detected. The master device's communication is terminated and the bus is released.

Condition for clearing (SPDn = 0)	Condition for setting (SPDn = 1)
• At the rising edge of the address transfer byte's first clock following setting of this bit and detection of a start condition • When the WUPn bit changes from 1 to 0 • When the IICEn bit changes from 1 to 0 (operation stop) • Reset	• When a stop condition is detected

Remark 1. LRELn: Bit 6 of IICA control register n0 (IICCTLn0)
IICEn: Bit 7 of IICA control register n0 (IICCTLn0)
Remark 2. n = 0

21.3.4 IICA flag register n (IICFn)

This register sets the operation mode of I^2C and indicates the status of the I^2C bus.
The IICFn register can be set by a 1-bit or 8-bit memory manipulation instruction. However, the STTn clear flag (STCFn) and I^2C bus status flag (IICBSYn) bits are read-only.
The IICRSVn bit can be used to enable/disable the communication reservation function.
The STCENn bit can be used to set the initial value of the IICBSYn bit.
The IICRSVn and STCENn bits can be written only when the operation of I^2C is disabled (bit 7 (IICEn) of IICA control register n0 (IICCTLn0) = 0). When operation is enabled, the IICFn register can be read.
Reset signal generation clears this register to 00H.

Figure 21 - 13 Format of IICA flag register n (IICFn)

Address: FFF52H After reset: 00H R/W Note

Symbol	<7>	<6>	5	4	3	2	<1>	<0>
IICFn	STCFn	IICBSYn	0	0	0	0	STCENn	IICRSVn

STCFn	STTn clear flag
0	Generate start condition
1	Start condition generation unsuccessful: clear the STTn flag

Condition for clearing (STCFn = 0)	Condition for setting (STCFn = 1)
• Cleared by STTn = 1 • When IICEn = 0 (operation stop) • Reset	• Generating start condition unsuccessful and the STTn bit cleared to 0 when communication reservation is disabled (IICRSVn = 1).

IICBSYn	I^2C bus status flag
0	Bus release status (communication initial status when STCENn = 1)
1	Bus communication status (communication initial status when STCENn = 0)

Condition for clearing (IICBSYn = 0)	Condition for setting (IICBSYn = 1)
• Detection of stop condition • When IICEn = 0 (operation stop) • Reset	• Detection of start condition • Setting of the IICEn bit when STCENn = 0

STCENn	Initial start enable trigger
0	After operation is enabled (IICEn = 1), enable generation of a start condition upon detection of a stop condition.
1	After operation is enabled (IICEn = 1), enable generation of a start condition without detecting a stop condition.

Condition for clearing (STCENn = 0)	Condition for setting (STCENn = 1)
• Cleared by instruction • Detection of start condition • Reset	• Set by instruction

IICRSVn	Communication reservation function disable bit
0	Enable communication reservation
1	Disable communication reservation

Condition for clearing (IICRSVn = 0)	Condition for setting (IICRSVn = 1)
• Cleared by instruction • Reset	• Set by instruction

Note Bits 6 and 7 are read-only.

Caution 1. Write to the STCENn bit only when the operation is stopped (IICEn = 0).

Caution 2. As the bus release status (IICBSYn = 0) is recognized regardless of the actual bus status when STCENn = 1, when generating the first start condition (STTn = 1), it is necessary to verify that no third party communications are in progress in order to prevent such communications from being destroyed.

Caution 3. Write to IICRSVn only when the operation is stopped (IICEn = 0).

Remark 1. STTn: Bit 1 of IICA control register n0 (IICCTLn0)
IICEn: Bit 7 of IICA control register n0 (IICCTLn0)

Remark 2. n = 0

21.3.5 IICA control register n1 (IICCTLn1)

This register is used to set the operation mode of I^2C and detect the statuses of the SCLAn and SDAAn pins.

The IICCTLn1 register can be set by a 1-bit or 8-bit memory manipulation instruction. However, the CLDn and DADn bits are read-only.

Set the IICCTLn1 register, except the WUPn bit, while operation of I^2C is disabled (bit 7 (IICEn) of IICA control register n0 (IICCTLn0) is 0).

Reset signal generation clears this register to 00H.

Figure 21 - 14 Format of IICA control register n1 (IICCTLn1) (1/2)

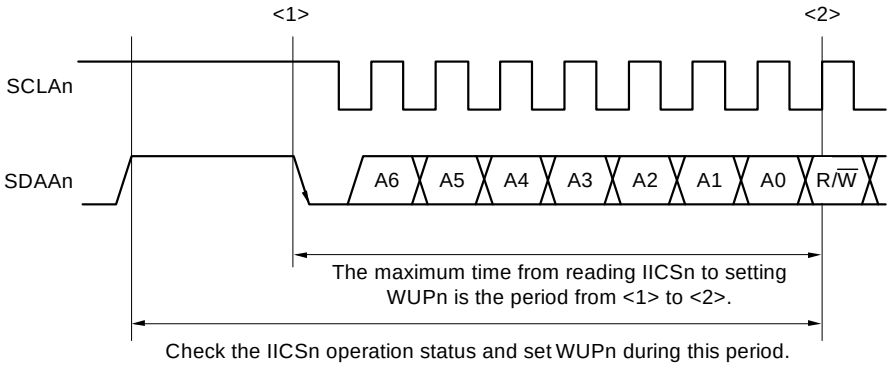
Address: F0231H After reset: 00H R/W Note 1

Symbol	<7>	6	<5>	<4>	<3>	<2>	1	<0>
IICCTLn1	WUPn	0	CLDn	DADn	SMCn	DFCn	0	PRSn

WUPn	Control of address match wakeup
0	Stops operation of address match wakeup function in STOP mode.
1	Enables operation of address match wakeup function in STOP mode.
To shift to STOP mode when WUPn = 1, execute the STOP instruction at least three clocks after setting (1) the WUPn bit (see **Figure 21 - 27 Flow When Setting WUPn = 1**). Clear (0) the WUPn bit after the address has matched or an extension code has been received. The subsequent communication can be entered by the clearing (0) WUPn bit. (The clock stretch must be released and transmit data must be written after the WUPn bit has been cleared (0).) The interrupt timing when the address has matched or when an extension code has been received, while WUPn = 1, is identical to the interrupt timing when WUPn = 0. (A delay of the difference of sampling by the clock will occur.) Furthermore, when WUPn = 1, a stop condition interrupt is not generated even if the SPIEn bit is set to 1.	
Condition for clearing (WUPn = 0)	Condition for setting (WUPn = 1)
• Cleared by instruction (after address match or extension code reception)	• Set by instruction (when the MSTSn, EXCn, and COIn bits are “0”, and the STDn bit also “0” (communication not entered)) Note 2

Note 1. Bits 4 and 5 are read-only.

Note 2. The status of the IICA status register n (IICSn) must be checked and the WUPn bit must be set during the period shown below.



Remark n = 0

Figure 21 - 14 Format of IICA control register n1 (IICCTLn1) (2/2)

CLDn	Detection of SCLAn pin level (valid only when IICEn = 1)
0	The SCLAn pin was detected at low level.
1	The SCLAn pin was detected at high level.

Condition for clearing (CLDn = 0)	Condition for setting (CLDn = 1)
• When the SCLAn pin is at low level • When IICEn = 0 (operation stop) • Reset	• When the SCLAn pin is at high level

DADn	Detection of SDAAn pin level (valid only when IICEn = 1)
0	The SDAAn pin was detected at low level.
1	The SDAAn pin was detected at high level.

Condition for clearing (DADn = 0)	Condition for setting (DADn = 1)
• When the SDAAn pin is at low level • When IICEn = 0 (operation stop) • Reset	• When the SDAAn pin is at high level

SMCn	Operation mode switching
0	Operates in standard mode (fastest transfer rate: 100 kbps).
1	Operates in fast mode (fastest transfer rate: 400 kbps) or fast mode plus (fastest transfer rate: 1 Mbps).

DFCn	Digital filter operation control
0	Digital filter off.
1	Digital filter on.
Use the digital filter only in fast mode and fast mode plus. The digital filter is used for noise elimination. The transfer clock does not vary, regardless of the DFCn bit being set (1) or cleared (0).	

PRSn	Control of IICA operation clock (f_{MCK})
0	Selects f_{CLK} (1 MHz ≤ f_{CLK} ≤ 20 MHz).
1	Selects $f_{CLK}/2$ (20 MHz < f_{CLK}).

Caution 1. The maximum operating frequency of the IICA operating clock (f_{MCK}) is 20 MHz (Max.). Only when f_{CLK} exceeds 20 MHz, set bit 0 (PRSn) of IICA control register n1 (IICCTLn1) to 1.

Caution 2. Note the minimum f_{CLK} operation frequency when setting the transfer clock.
The minimum f_{CLK} operation frequency for serial interface IICA is determined according to the mode.
Fast mode: f_{CLK} = 3.5 MHz (MIN.)
Fast mode plus: f_{CLK} = 10 MHz (MIN.)
Normal mode: f_{CLK} = 1 MHz (MIN.)

Remark 1. IICEn: Bit 7 of IICA control register n0 (IICCTLn0)
Remark 2. n = 0

21.3.6 IICA low-level width setting register n (IICWLn)

This register is used to set the low-level width (tLOW) of the SCLAn pin signal that is output by serial interface IICA and to control the SDAAn pin signal.

The IICWLn register can be set by an 8-bit memory manipulation instruction.

Set the IICWLn register while operation of I^2C is disabled (bit 7 (IICEn) of IICA control register n0 (IICCTLn0) is 0).

Reset signal generation sets this register to FFH.

For details about setting the IICWLn register, see **21.4.2 Setting transfer clock by using IICWLn and IICWHn registers**.

Figure 21 - 15 Format of IICA low-level width setting register n (IICWLn)

Address: F0232H After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
IICWLn								

21.3.7 IICA high-level width setting register n (IICWHn)

This register is used to set the high-level width of the SCLAn pin signal that is output by serial interface IICA and to control the SDAAn pin signal.

The IICWHn register can be set by an 8-bit memory manipulation instruction.

Set the IICWHn register while operation of I^2C is disabled (bit 7 (IICEn) of IICA control register n0 (IICCTLn0) is 0).

Reset signal generation sets this register to FFH.

Figure 21 - 16 Format of IICA high-level width setting register n (IICWHn)

Address: F0233H After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
IICWHn								

Remark 1. For setting procedures of the transfer clock on master side and of the IICWLn and IICWHn registers on slave side, see **21.4.2 (1)** and **21.4.2 (2)**, respectively.

Remark 2. n = 0

21.3.8 Port mode register 6 (PM6)

This register sets the input/output of port 6 in 1-bit units.

When using the P60/SCLA0 pin as clock I/O and the P61/SDAA0 pin as serial data I/O, clear PM60 and PM61, and the output latches of P60 and P61 to 0.

Set the IICEn bit (bit 7 of IICA control register n0 (IICCTLn0)) to 1 before setting the output mode because the P60/SCLA0 and P61/SDAA0 pins output a low level (fixed) when the IICEn bit is 0.

The PM6 register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets this register to FFH.

Figure 21 - 17 Format of Port mode register 6 (PM6)

Address: FFF26H After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
PM6	1	1	1	1	1	1	PM61	PM60

PM6n	P6n pin I/O mode selection (n = 0, 1)
0	Output mode (output buffer on)
1	Input mode (output buffer off)

21.4 I²C Bus Mode Functions

21.4.1 Pin configuration

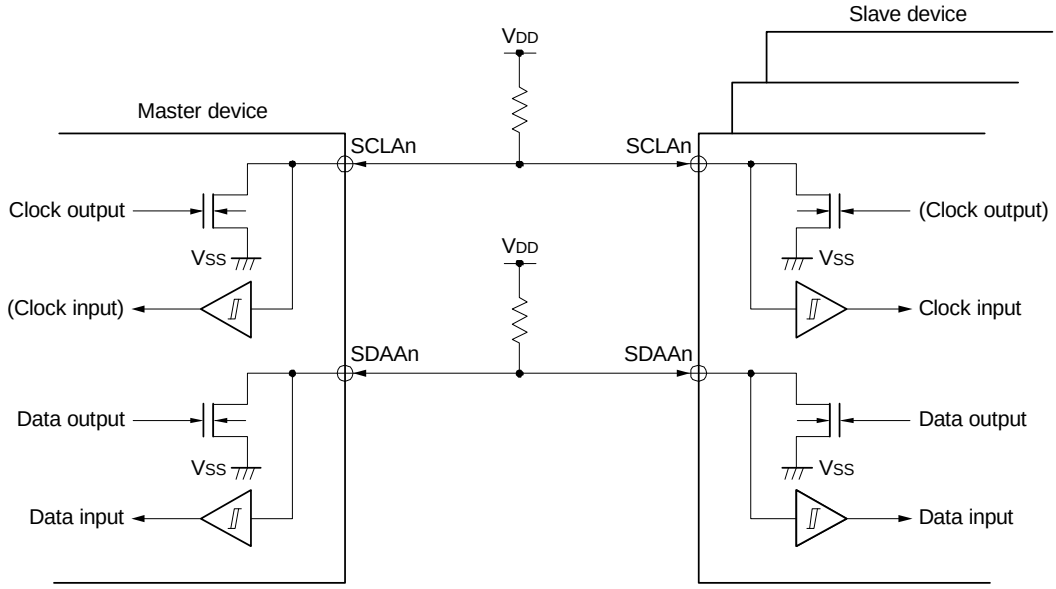
The serial clock pin (SCLAn) and the serial data bus pin (SDAAn) are configured as follows.

(1) SCLAn..... This pin is used for serial clock input and output.
This pin is an N-ch open-drain output for both master and slave devices. Input is Schmitt input.

(2) SDAAn ..... This pin is used for serial data input and output.
This pin is an N-ch open-drain output for both master and slave devices. Input is Schmitt input.

Since outputs from the serial clock line and the serial data bus line are N-ch open-drain outputs, an external pull-up resistor is required.

Figure 21 - 18 Pin Configuration Diagram



Remark n = 0

21.4.2 Setting transfer clock by using IICWLn and IICWHn registers

(1) Setting transfer clock on master side

$$\text{Transfer clock} = \frac{f_{MCK}}{IICWL + IICWH + f_{MCK}(t_R + t_F)}$$

At this time, the optimal setting values of the IICWLn and IICWHn registers are as follows.
(The fractional parts of all setting values are rounded up.)

• When the fast mode

$$IICWLn = \frac{0.52}{\text{Transfer clock}} \times f_{MCK}$$

$$IICWHn = \left(\frac{0.48}{\text{Transfer clock}} - t_R - t_F\right) \times f_{MCK}$$

• When the normal mode

$$IICWLn = \frac{0.47}{\text{Transfer clock}} \times f_{MCK}$$

$$IICWHn = \left(\frac{0.53}{\text{Transfer clock}} - t_R - t_F\right) \times f_{MCK}$$

• When the fast mode plus

$$IICWLn = \frac{0.50}{\text{Transfer clock}} \times f_{MCK}$$

$$IICWHn = \left(\frac{0.50}{\text{Transfer clock}} - t_R - t_F\right) \times f_{MCK}$$

(2) Setting IICWLn and IICWHn registers on slave side
(The fractional parts of all setting values are truncated.)

• When the fast mode

$IICWLn = 1.3\ \mu s \times f_{MCK}$

$IICWHn = (1.2\ \mu s - t_R - t_F) \times f_{MCK}$

• When the normal mode

$IICWLn = 4.7\ \mu s \times f_{MCK}$

$IICWHn = (5.3\ \mu s - t_R - t_F) \times f_{MCK}$

• When the fast mode plus

$IICWLn = 0.50\ \mu s \times f_{MCK}$

$IICWHn = (0.50\ \mu s - t_R - t_F) \times f_{MCK}$

(**Cautions** and **Remarks** are listed on the next page.)

Caution 1. The maximum operating frequency of the IICA operating clock (f_{MCK}) is 20 MHz (Max.). Only when f_{CLK} exceeds 20 MHz, set bit 0 (PRSn) of IICA control register n1 (IICCTLn1) to 1.

Caution 2. Note the minimum f_{CLK} operation frequency when setting the transfer clock. The minimum f_{CLK} operation frequency for serial interface IICA is determined according to the mode.
Fast mode: f_{CLK} = 3.5 MHz (MIN.)
Fast mode plus: f_{CLK} = 10 MHz (MIN.)
Normal mode: f_{CLK} = 1 MHz (MIN.)

Remark 1. Calculate the rise time (t_R) and fall time (t_F) of the SDAAn and SCLAn signals separately, because they differ depending on the pull-up resistance and wire load.

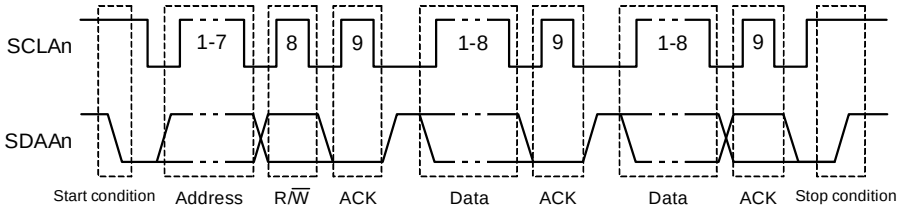
Remark 2. IICWLn: IICA low-level width setting register n
IICWHn: IICA high-level width setting register n
t_F: SDAAn and SCLAn signal falling times
t_R: SDAAn and SCLAn signal rising times
f_{MCK}: IICA operating clock frequency

Remark 3. n = 0

21.5 I²C Bus Definitions and Control Methods

The following section describes the I²C bus's serial data communication format and the signals used by the I²C bus. **Figure 21 - 19** shows the transfer timing for the "start condition", "address", "data", and "stop condition" output via the I²C bus's serial data bus.

Figure 21 - 19 I²C Bus Serial Data Transfer Timing

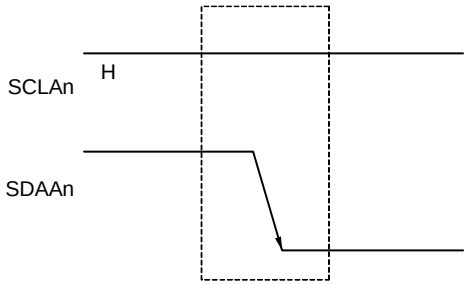


The master device generates the start condition, slave address, and stop condition.
The acknowledge (ACK) can be generated by either the master or slave device (normally, it is output by the device that receives 8-bit data).
The serial clock (SCLAn) is continuously output by the master device. However, in the slave device, the SCLAn pin low level period can be extended and a clock stretch can be inserted.

21.5.1 Start conditions

A start condition is met when the SCLAn pin is at high level and the SDAAn pin changes from high level to low level. The start conditions for the SCLAn pin and SDAAn pin are signals that the master device generates to the slave device when starting a serial transfer. When the device is used as a slave, start conditions can be detected.

Figure 21 - 20 Start Conditions



A start condition is output when bit 1 (STTn) of IICA control register n0 (IICCTLn0) is set (1) after a stop condition has been detected (SPDn: Bit 0 of the IICA status register n (IICSn) = 1). When a start condition is detected, bit 1 (STDn) of the IICSn register is set (1).

Remark n = 0

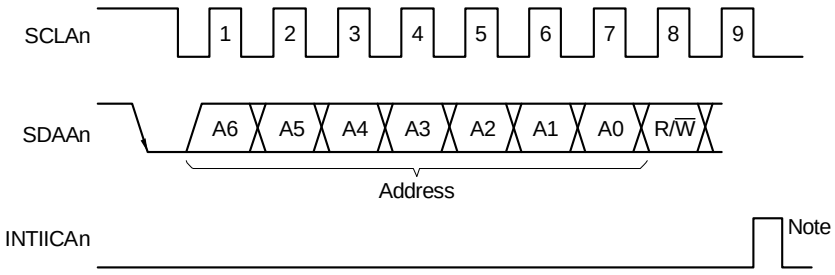
21.5.2 Addresses

The address is defined by the 7 bits of data that follow the start condition.

An address is a 7-bit data segment that is output in order to select one of the slave devices that are connected to the master device via the bus lines. Therefore, each slave device connected via the bus lines must have a unique address.

The slave devices include hardware that detects the start condition and checks whether or not the 7-bit address data matches the data values stored in the slave address register n (SVAn). If the address data matches the SVAn register values, the slave device is selected and communicates with the master device until the master device generates a start condition or stop condition.

Figure 21 - 21 Address



Note INTIICAn is not issued if data other than a local address or extension code is received during slave device operation.

Addresses are output when a total of 8 bits consisting of the slave address and the transfer direction described in **21.5.3 Transfer direction specification** are written to the IICA shift register n (IICAn). The received addresses are written to the IICAn register.

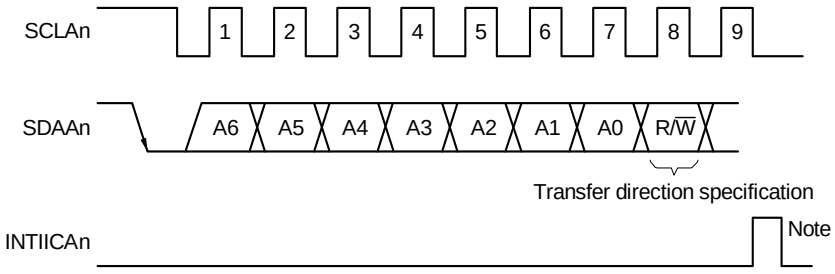
The slave address is assigned to the higher 7 bits of the IICAn register.

21.5.3 Transfer direction specification

In addition to the 7-bit address data, the master device sends 1 bit that specifies the transfer direction.

When this transfer direction specification bit has a value of “0”, it indicates that the master device is transmitting data to a slave device. When the transfer direction specification bit has a value of “1”, it indicates that the master device is receiving data from a slave device.

Figure 21 - 22 Transfer Direction Specification



Note INTIICAn is not issued if data other than a local address or extension code is received during slave device operation.

Remark n = 0

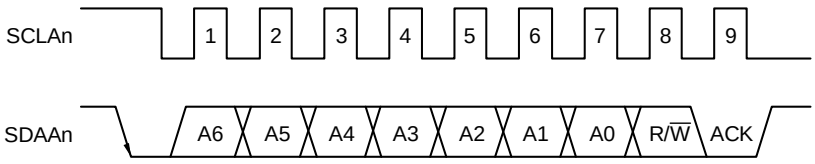
21.5.4 Acknowledge (ACK)

ACK is used to check the status of serial data at the transmission and reception sides.
The reception side returns ACK each time it has received 8-bit data.
The transmission side usually receives ACK after transmitting 8-bit data. When ACK is returned from the reception side, it is assumed that reception has been correctly performed and processing is continued. Whether ACK has been detected can be checked by using bit 2 (ACKDn) of the IICA status register n (IICSn).
When the master receives the last data item, it does not return ACK and instead generates a stop condition. If a slave does not return ACK after receiving data, the master outputs a stop condition or restart condition and stops transmission. If ACK is not returned, the possible causes are as follows.

<1> Reception was not performed normally.
<2> The final data item was received.
<3> The reception side specified by the address does not exist.

To generate ACK, the reception side makes the SDAAn line low at the ninth clock (indicating normal reception).
Automatic generation of ACK is enabled by setting bit 2 (ACKEn) of IICA control register n0 (IICCTLn0) to 1. Bit 3 (TRCn) of the IICSn register is set by the data of the eighth bit that follows 7-bit address information. Usually, set the ACKEn bit to 1 for reception (TRCn = 0).
If a slave can receive no more data during reception (TRCn = 0) or does not require the next data item, then the slave must inform the master, by clearing the ACKEn bit to 0, that it will not receive any more data.
When the master does not require the next data item during reception (TRCn = 0), it must clear the ACKEn bit to 0 so that ACK is not generated. In this way, the master informs a slave at the transmission side that it does not require any more data (transmission will be stopped).

Figure 21 - 23 ACK



When the local address is received, ACK is automatically generated, regardless of the value of the ACKEn bit.
When an address other than that of the local address is received, ACK is not generated (NACK).
When an extension code is received, ACK is generated if the ACKEn bit is set to 1 in advance.
How ACK is generated when data is received differs as follows depending on the setting of the clock stretch timing.

- When 8-clock clock stretch state is selected (bit 3 (WTIMn) of IICCTLn0 register = 0):
  By setting the ACKEn bit to 1 before releasing the clock stretch state, ACK is generated at the falling edge of the eighth clock of the SCLAn pin.
- When 9-clock clock stretch state is selected (bit 3 (WTIMn) of IICCTLn0 register = 1):
  ACK is generated by setting the ACKEn bit to 1 in advance.

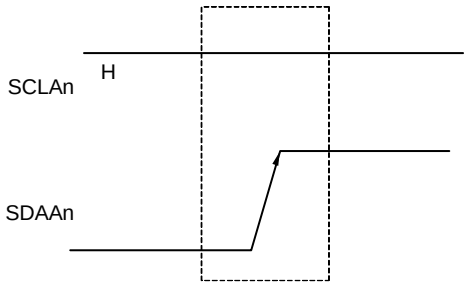
Remark n = 0

21.5.5 Stop condition

When the SCLAn pin is at high level, changing the SDAAn pin from low level to high level generates a stop condition.

A stop condition is a signal that the master device generates to the slave device when serial transfer has been completed. When the device is used as a slave, stop conditions can be detected.

Figure 21 - 24 Stop Condition



A stop condition is generated when bit 0 (SPTn) of IICA control register n0 (IICCTLn0) is set to 1. When the stop condition is detected, bit 0 (SPDn) of the IICA status register n (IICSn) is set to 1 and INTIICAn is generated when bit 4 (SPIEn) of the IICCTLn0 register is set to 1.

Remark n = 0

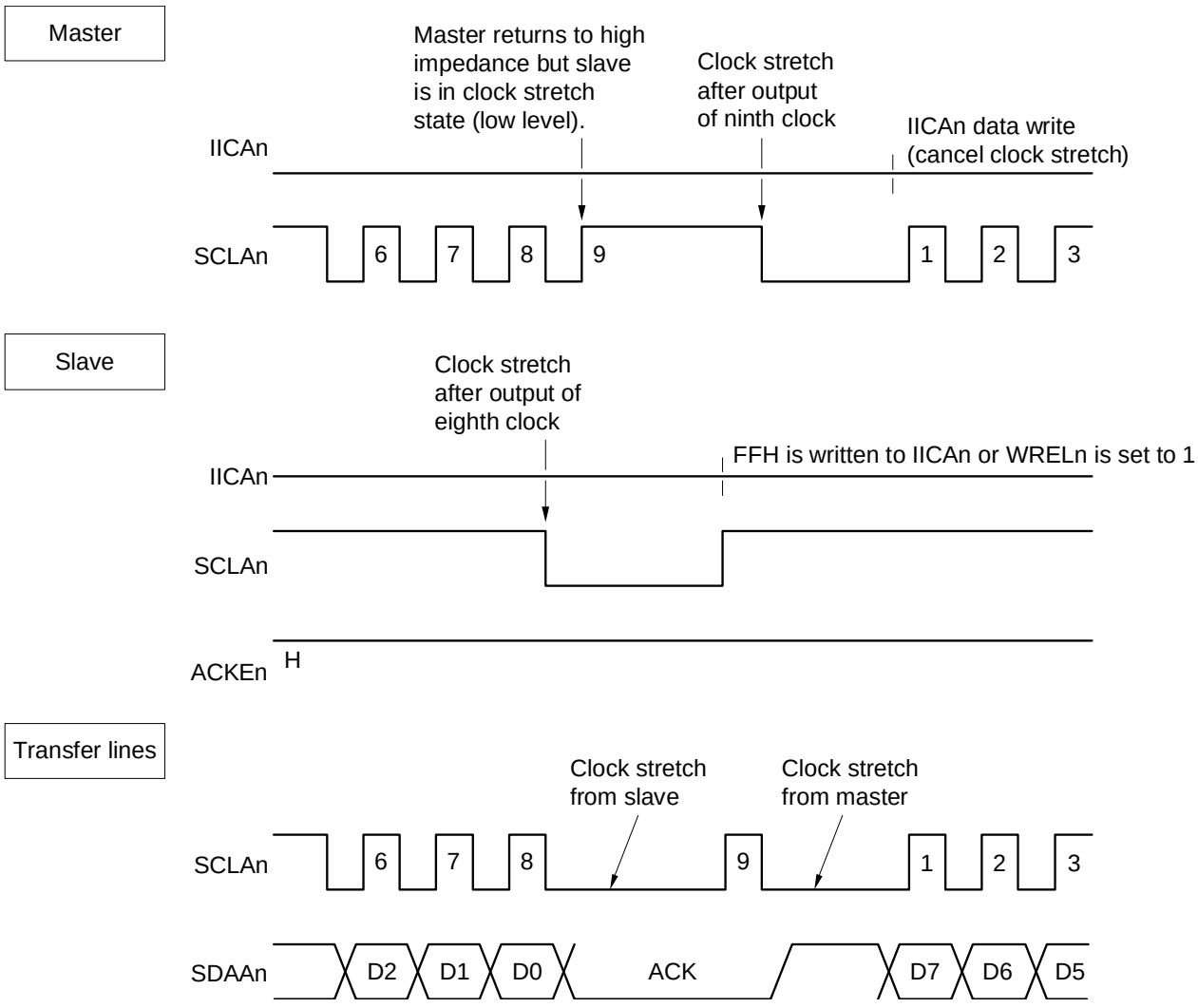
21.5.6 Clock stretch

The clock stretch is used to notify the communication partner that a device (master or slave) is preparing to transmit or receive data (i.e., is in a clock stretch state).

Setting the SCLAn pin to low level notifies the communication partner of the clock stretch state. When clock stretch state has been canceled for both the master and slave devices, the next data transfer can begin.

Figure 21 - 25 Clock stretch (1/2)

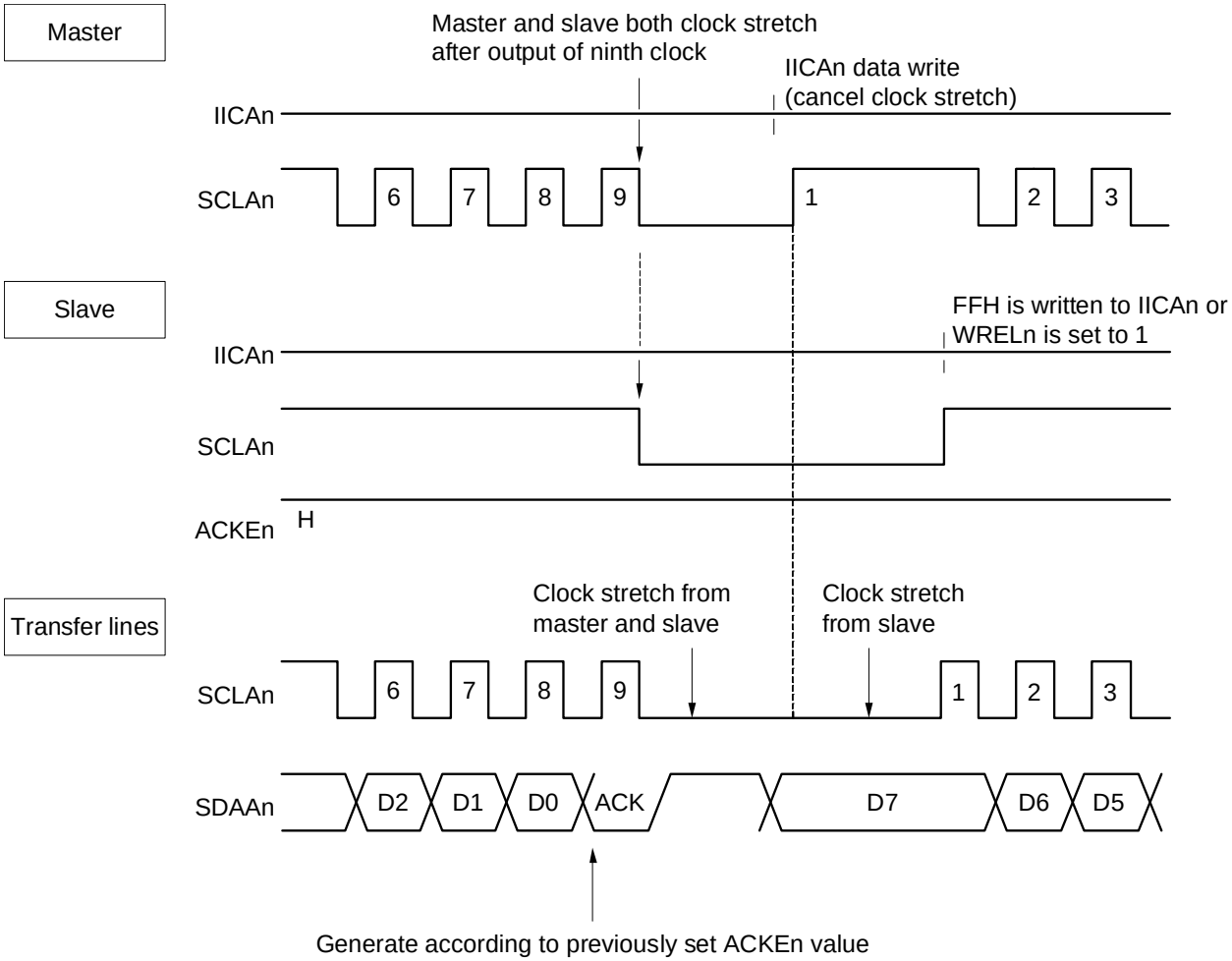
(1) When clock stretch is set for the ninth and eighth clock cycles for the master and slave devices, respectively (master transmits, slave receives, and ACKEn = 1)



Remark n = 0

Figure 21 - 25 Clock stretch (2/2)

(2) When clock stretch is set for the ninth clock cycle for both the master and slave devices (master transmits, slave receives, and ACKEn = 1)



Remark ACKEn: Bit 2 of IICA control register n0 (IICCTLn0)
WRELn: Bit 5 of IICA control register n0 (IICCTLn0)

A clock stretch may be automatically generated depending on the setting of bit 3 (WTIMn) of IICA control register n0 (IICCTLn0).

Normally, the receiving side cancels the clock stretch state when bit 5 (WRELn) of the IICCTLn0 register is set to 1 or when FFH is written to the IICA shift register n (IICAn), and the transmitting side cancels the clock stretch state when data is written to the IICAn register.

The master device can also cancel the clock stretch state via either of the following methods.

- By setting bit 1 (STTn) of the IICCTLn0 register to 1
- By setting bit 0 (SPTn) of the IICCTLn0 register to 1

Remark n = 0

21.5.7 Canceling clock stretch

The I^2C usually cancels a clock stretch state by the following processing.

- Writing data to the IICA shift register n (IICAn)
- Setting bit 5 (WRELn) of IICA control register n0 (IICCTLn0) (canceling clock stretch)
- Setting bit 1 (STTn) of the IICCTLn0 register (generating start condition) Note
- Setting bit 0 (SPTn) of the IICCTLn0 register (generating stop condition) Note

Note Master only

When the above clock stretch canceling processing is executed, the I^2C cancels the clock stretch state and communication is resumed.
To cancel a clock stretch state and transmit data (including addresses), write the data to the IICAn register.
To receive data after canceling a clock stretch state, or to complete data transmission, set bit 5 (WRELn) of the IICCTLn0 register to 1.
To generate a restart condition after canceling a clock stretch state, set bit 1 (STTn) of the IICCTLn0 register to 1.
To generate a stop condition after canceling a clock stretch state, set bit 0 (SPTn) of the IICCTLn0 register to 1.
Execute the canceling processing only once for one clock stretch state.
If, for example, data is written to the IICAn register after canceling a clock stretch state by setting the WRELn bit to 1, an incorrect value may be output to SDAAn line because the timing for changing the SDAAn line conflicts with the timing for writing the IICAn register.
In addition to the above, communication is stopped if the IICEn bit is cleared to 0 when communication has been aborted, so that the clock stretch state can be canceled.
If the I^2C bus has deadlocked due to noise, processing is saved from communication by setting bit 6 (LRELn) of the IICCTLn0 register, so that the clock stretch state can be canceled.

Caution **If a processing to cancel a clock stretch state is executed when WUPn = 1, the clock stretch state will not be canceled.**

Remark n = 0

21.5.8 Interrupt request (INTIICAn) generation timing and clock stretch control

The setting of bit 3 (WTIMn) of IICA control register n0 (IICCTLn0) determines the timing by which INTIICAn is generated and the corresponding clock stretch control, as shown in **Table 21 - 2**.

Table 21 - 2 INTIICAn Generation Timing and Clock Stretch Control

WTIMn	During Slave Device Operation			During Master Device Operation		
	Address	Data Reception	Data Transmission	Address	Data Reception	Data Transmission
0	9 Notes 1, 2	8 Note 2	8 Note 2	9	8	8
1	9 Notes 1, 2	9 Note 2	9 Note 2	9	9	9

Note 1. The slave device's INTIICAn signal and clock stretch period occurs at the falling edge of the ninth clock only when there is a match with the address set to the slave address register n (SVAn).
At this point, ACK is generated regardless of the value set to the IICCTLn0 register's bit 2 (ACKEn). For a slave device that has received an extension code, INTIICAn occurs at the falling edge of the eighth clock.
However, if the address does not match after restart, INTIICAn is generated at the falling edge of the 9th clock, but clock stretch does not occur.

Note 2. If the received address does not match the contents of the slave address register n (SVAn) and extension code is not received, neither INTIICAn nor a clock stretch occurs.

Remark The numbers in the table indicate the number of the serial clock's clock signals. Interrupt requests and clock stretch control are both synchronized with the falling edge of these clock signals.

(1) During address transmission/reception
- Slave device operation: Interrupt and clock stretch timing are determined depending on the conditions described in Notes 1 and 2 above, regardless of the WTIMn bit.
- Master device operation: Interrupt and clock stretch timing occur at the falling edge of the ninth clock regardless of the WTIMn bit.

(2) During data reception
- Master/slave device operation: Interrupt and clock stretch timing are determined according to the WTIMn bit.

(3) During data transmission
- Master/slave device operation: Interrupt and clock stretch timing are determined according to the WTIMn bit.

Remark n = 0

(4) Clock stretch cancellation method

The four clock stretch cancellation methods are as follows.

- Writing data to the IICA shift register n (IICAn)
- Setting bit 5 (WRELn) of IICA control register n0 (IICCTLn0) (canceling clock stretch)
- Setting bit 1 (STTn) of IICCTLn0 register (generating start condition) Note
- Setting bit 0 (SPTn) of IICCTLn0 register (generating stop condition) Note

Note Master only.

When an 8-clock clock stretch has been selected (WTIMn = 0), the presence/absence of ACK generation must be determined prior to clock stretch cancellation.

(5) Stop condition detection

INTIICAn is generated when a stop condition is detected (only when SPIEn = 1).

21.5.9 Address match detection method

In I^2C bus mode, the master device can select a particular slave device by transmitting the corresponding slave address.

Address match can be detected automatically by hardware. An interrupt request (INTIICAn) occurs when the address set to the slave address register n (SVAn) matches the slave address sent by the master device, or when an extension code has been received.

21.5.10 Error detection

In I^2C bus mode, the status of the serial data bus (SDAAn) during data transmission is captured by the IICA shift register n (IICAn) of the transmitting device, so the IICA data prior to transmission can be compared with the transmitted IICA data to enable detection of transmission errors. A transmission error is judged as having occurred when the compared data values do not match.

Remark n = 0

21.5.11 Extension code

(1) When the higher 4 bits of the receive address are either “0000” or “1111”, the extension code reception flag (EXCn) is set to 1 for extension code reception and an interrupt request (INTIICAn) is issued at the falling edge of the eighth clock. The local address stored in the slave address register n (SVAn) is not affected.

(2) The settings below are specified if 11110xx0 is transferred from the master by using a 10-bit address transfer when the SVAn register is set to 11110xx0. Note that INTIICAn occurs at the falling edge of the eighth clock.

- Higher four bits of data match: EXCn = 1
- Seven bits of data match: COIn = 1

Remark EXCn: Bit 5 of IICA status register n (IICSn)
COIn: Bit 4 of IICA status register n (IICSn)

(3) Since the processing after the interrupt request occurs differs according to the data that follows the extension code, such processing is performed by software.
If the extension code is received while a slave device is operating, then the slave device is participating in communication even if its address does not match.
For example, after the extension code is received, if you do not wish to operate the target device as a slave device, set bit 6 (LRELn) of IICA control register n0 (IICCTLn0) to 1 to set the standby mode for the next communication operation.

Table 21 - 3 Bit Definitions of Major Extension Codes

Slave Address	R/W Bit	Description
0000 000	0	General call address
1111 0xx	0	10-bit slave address specification (during address authentication)
1111 0xx	1	10-bit slave address specification (after address match, when read command is issued)

Remark 1. See the I^2C bus specifications issued by NXP Semiconductors for details of extension codes other than those described above.

Remark 2. n = 0

21.5.12 Arbitration

When several master devices simultaneously generate a start condition (when the STTn bit is set to 1 before the STDn bit is set to 1), communication among the master devices is performed as the number of clocks are adjusted until the data differs. This kind of operation is called arbitration.

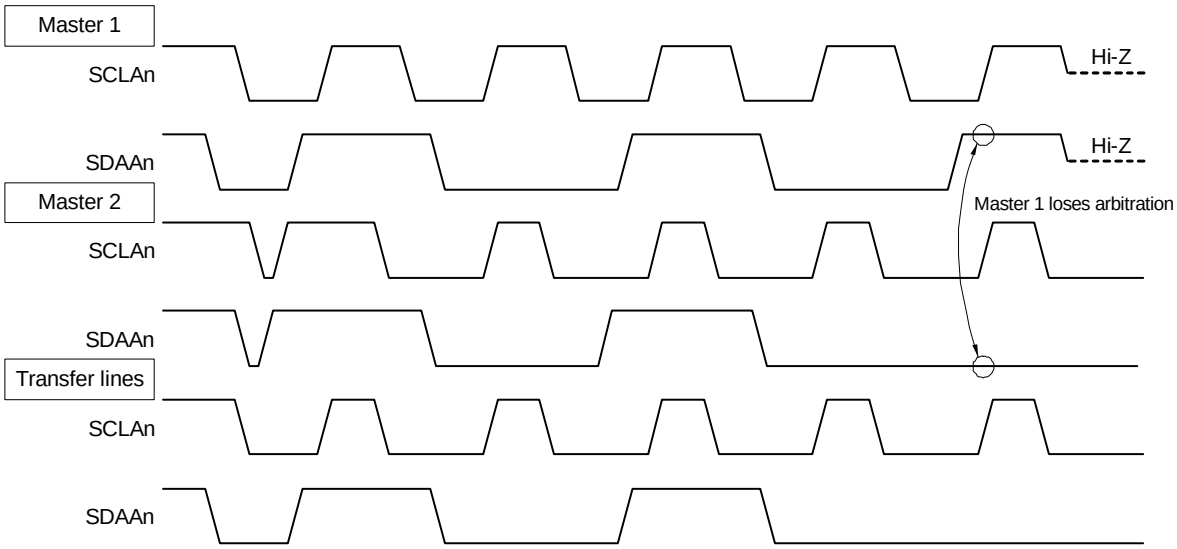
When one of the master devices loses in arbitration, an arbitration loss flag (ALDn) in the IICA status register n (IICSn) is set (1) via the timing by which the arbitration loss occurred, and the SCLAn and SDAAn lines are both set to high impedance, which releases the bus.

The arbitration loss is detected based on the timing of the next interrupt request (the eighth or ninth clock, when a stop condition is detected, etc.) and the ALDn = 1 setting that has been made by software.

For details of interrupt request timing, see **21.5.8 Interrupt request (INTIICAn) generation timing and clock stretch control**.

Remark STDn: Bit 1 of IICA status register n (IICSn)
STTn: Bit 1 of IICA control register n0 (IICCTLn0)

Figure 21 - 26 Arbitration Timing Example



Remark n = 0

Table 21 - 4 Status During Arbitration and Interrupt Request Generation Timing

Status During Arbitration	Interrupt Request Generation Timing
During address transmission	At falling edge of eighth or ninth clock following byte transfer Note 1
Read/write data after address transmission	
During extension code transmission	
Read/write data after extension code transmission	
During data transmission	
During ACK transfer period after data transmission	
When restart condition is detected during data transfer	
When stop condition is detected during data transfer	When stop condition is generated (when SPIEn = 1) Note 2
When data is at low level while attempting to generate a restart condition	At falling edge of eighth or ninth clock following byte transfer Note 1
When stop condition is detected while attempting to generate a restart condition	When stop condition is generated (when SPIEn = 1) Note 2
When data is at low level while attempting to generate a stop condition	At falling edge of eighth or ninth clock following byte transfer Note 1
When SCLAn is at low level while attempting to generate a restart condition	

Note 1. When the WTIMn bit (bit 3 of IICA control register n0 (IICCTLn0)) = 1, an interrupt request occurs at the falling edge of the ninth clock. When WTIMn = 0 and the extension code's slave address is received, an interrupt request occurs at the falling edge of the eighth clock.

Note 2. When there is a chance that arbitration will occur, set SPIEn = 1 for master device operation.

Remark 1. SPIEn: Bit 4 of IICA control register n0 (IICCTLn0)

Remark 2. n = 0

21.5.13 Wakeup function

The I^2C bus slave function is a function that generates an interrupt request signal (INTIICAn) when a local address and extension code have been received.

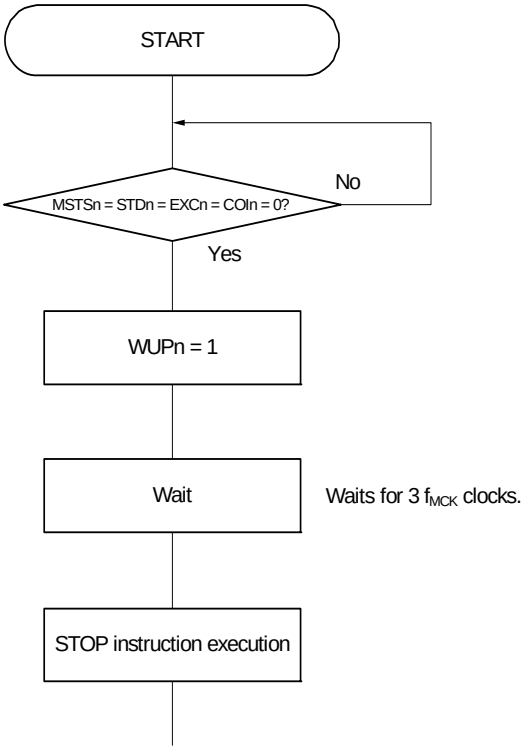
This function makes processing more efficient by preventing unnecessary INTIICAn signal from occurring when addresses do not match.

When a start condition is detected, wakeup standby mode is set. This wakeup standby mode is in effect while addresses are transmitted due to the possibility that an arbitration loss may change the master device (which has generated a start condition) to a slave device.

To use the wakeup function in the STOP mode, set the WUPn bit to 1. Addresses can be received regardless of the operation clock. An interrupt request signal (INTIICAn) is also generated when a local address and extension code have been received. Operation returns to normal operation by using an instruction to clear (0) the WUPn bit after this interrupt has been generated.

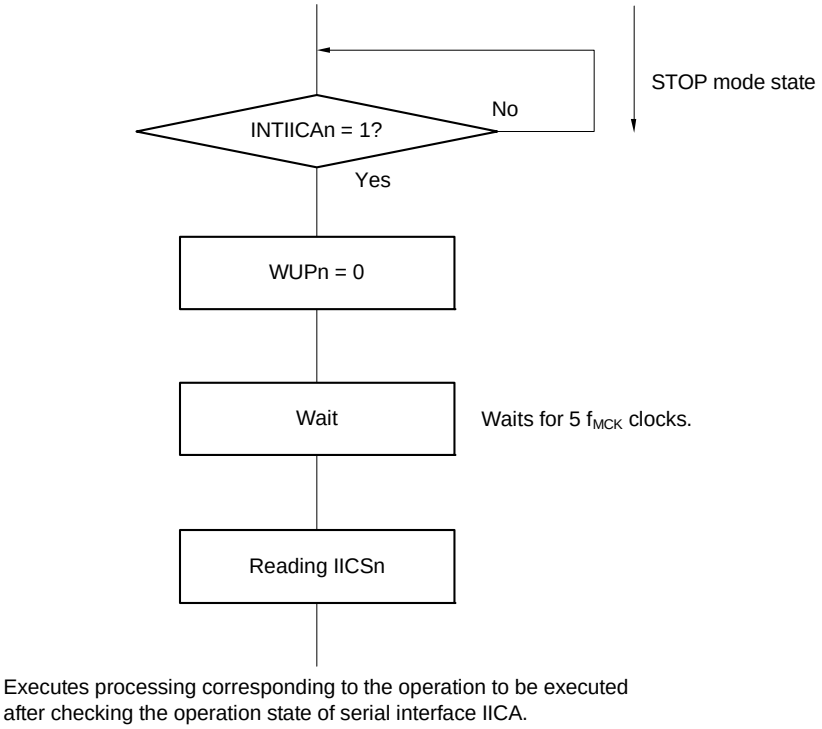
Figure 21 - 27 shows the flow for setting WUPn = 1 and **Figure 21 - 28** shows the flow for setting WUPn = 0 upon an address match.

Figure 21 - 27 Flow When Setting WUPn = 1



Remark n = 0

Figure 21 - 28 Flow When Setting WUPn = 0 upon Address Match (Including Extension Code Reception)

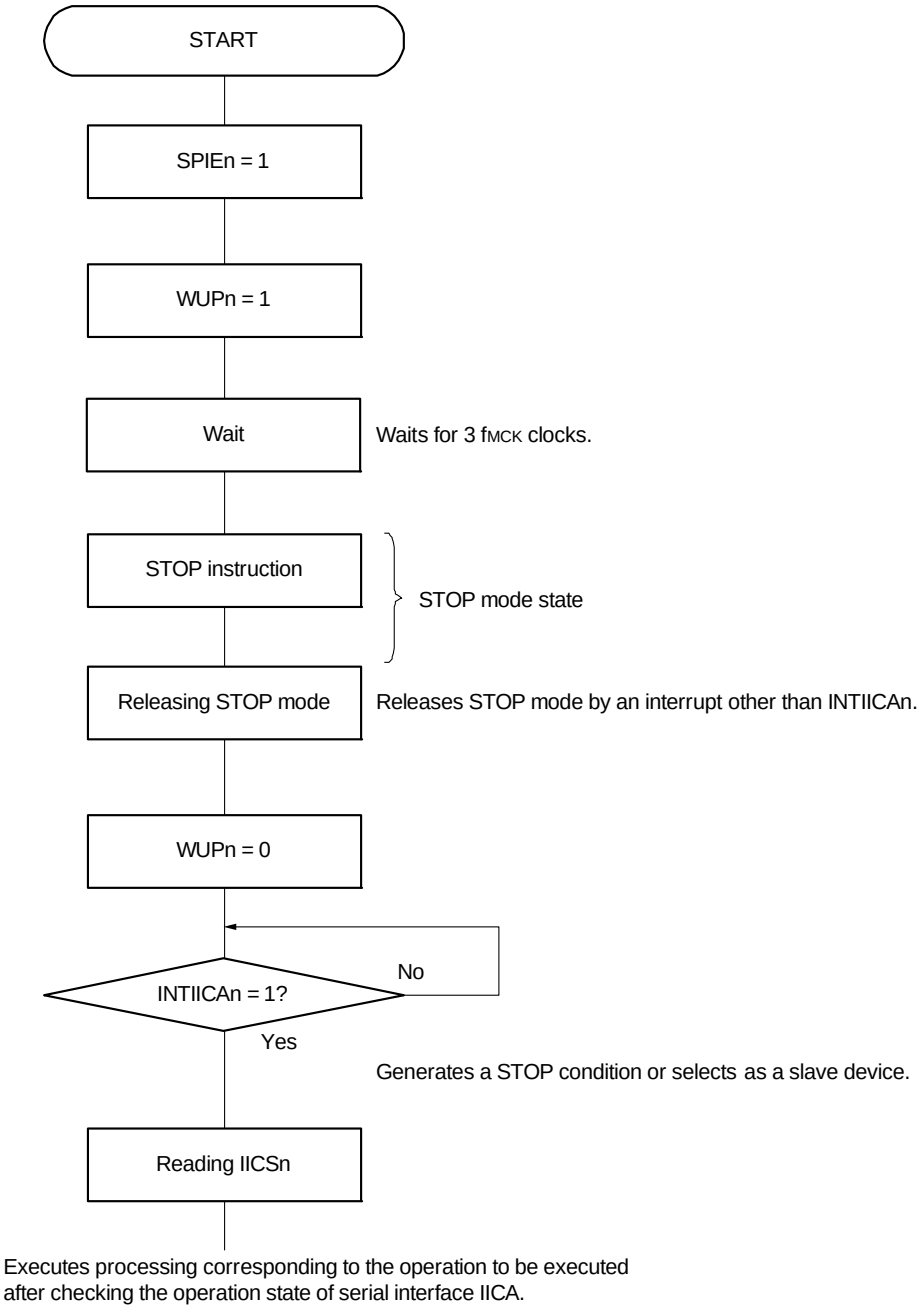


Use the following flows to perform the processing to release the STOP mode other than by an interrupt request (INTIICAn) generated from serial interface IICA.

- When operating as the master device for the next IIC communication: Flow shown in **Figure 21 - 29**
- When operating as a slave device for the next IIC communication:
  - When the INTIICAn interrupt is used to return from the mode:
    - Same as the flow in **Figure 21 - 28**
  - When an interrupt other than the INTIICAn interrupt is used to return from the mode:
    - Continue operation while WUPn = 1 until an INTIICAn interrupt is generated.

Remark n = 0

Figure 21 - 29 When Operating as Master Device after Releasing STOP Mode other than by INTIICAn



Remark n = 0

21.5.14 Communication reservation

(1) When communication reservation function is enabled (bit 0 (IICRSVn) of IICA flag register n (IICFn) = 0)

To start master device communications when not currently using a bus, a communication reservation can be made to enable transmission of a start condition when the bus is released. There are two modes under which the bus is not used.

- When arbitration results in neither master nor slave operation
- When an extension code is received and slave operation is disabled (ACK is not returned and the bus was released by setting bit 6 (LRELn) of IICA control register n0 (IICCTLn0) to 1 and saving communication).

If bit 1 (STTn) of the IICCTLn0 register is set to 1 while the bus is not used (after a stop condition is detected), a start condition is automatically generated and wait state is set.
If an address is written to the IICA shift register n (IICAn) after bit 4 (SPIEn) of the IICCTLn0 register was set to 1, and it was detected by generation of an interrupt request signal (INTIICAn) that the bus was released (detection of the stop condition), then the device automatically starts communication as the master. Data written to the IICAn register before the stop condition is detected is invalid.
When the STTn bit has been set to 1, the operation mode (as start condition or as communication reservation) is determined according to the bus status.

- If the bus has been released.....a start condition is generated
- If the bus has not been released (standby mode).....communication reservation

Check whether the communication reservation operates or not by using the MSTSn bit (bit 7 of the IICA status register n (IICSn)) after the STTn bit is set to 1 and the wait time elapses.
Use software to secure the wait time calculated by the following expression.

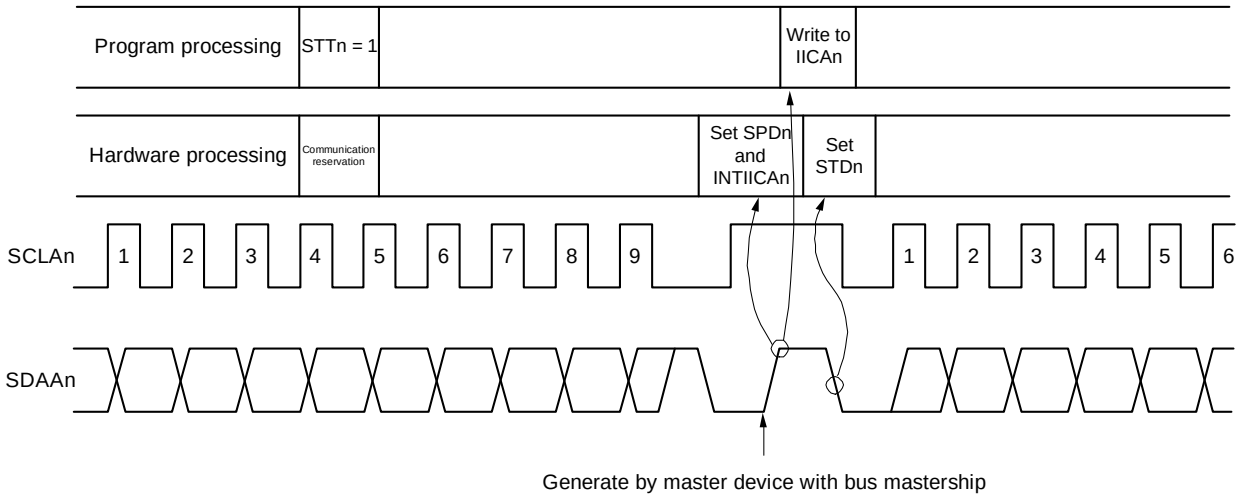
Wait time from setting STTn = 1 to checking the MSTSn flag: (IICWLn setting value + IICWHn setting value + 4) /f_{MCK}+ t_F × 2

Remark 1. IICWLn: IICA low-level width setting register n
IICWHn: IICA high-level width setting register n
t_F: SDAAn and SCLAn signal falling times
f_{MCK}: IICA operating clock frequency

Remark 2. n = 0

Figure 21 - 30 shows the Communication Reservation Timing.

Figure 21 - 30 Communication Reservation Timing



Remark IICAn: IICA shift register n
STTn: Bit 1 of IICA control register n0 (IICCTLn0)
STDn: Bit 1 of IICA status register n (IICSn)
SPDn: Bit 0 of IICA status register n (IICSn)

Communication reservations are accepted via the timing shown in **Figure 21 - 31**. After bit 1 (STDn) of the IICA status register n (IICSn) is set to 1, a communication reservation can be made by setting bit 1 (STTn) of IICA control register n0 (IICCTLn0) to 1 before a stop condition is detected.

Figure 21 - 31 Timing for Accepting Communication Reservations

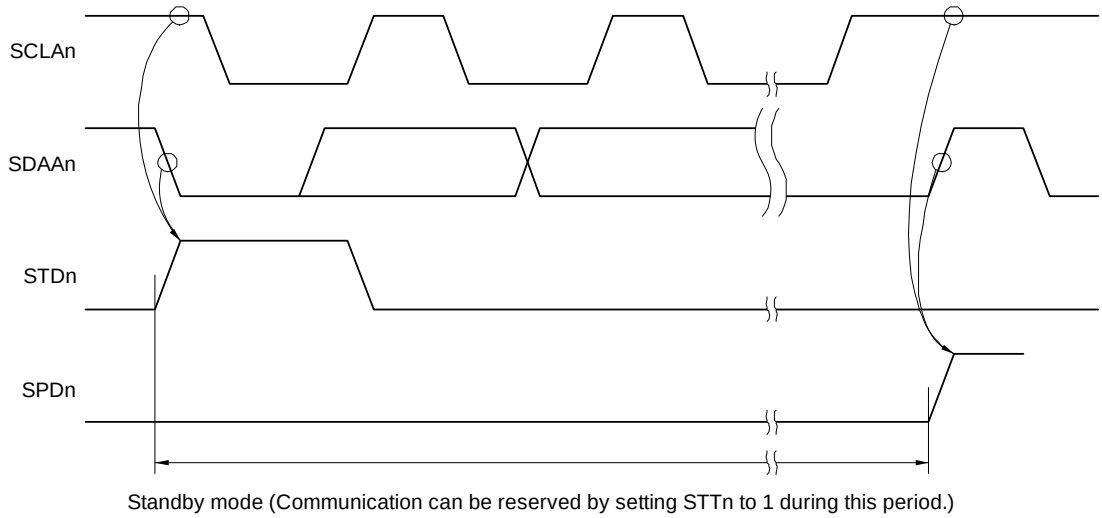
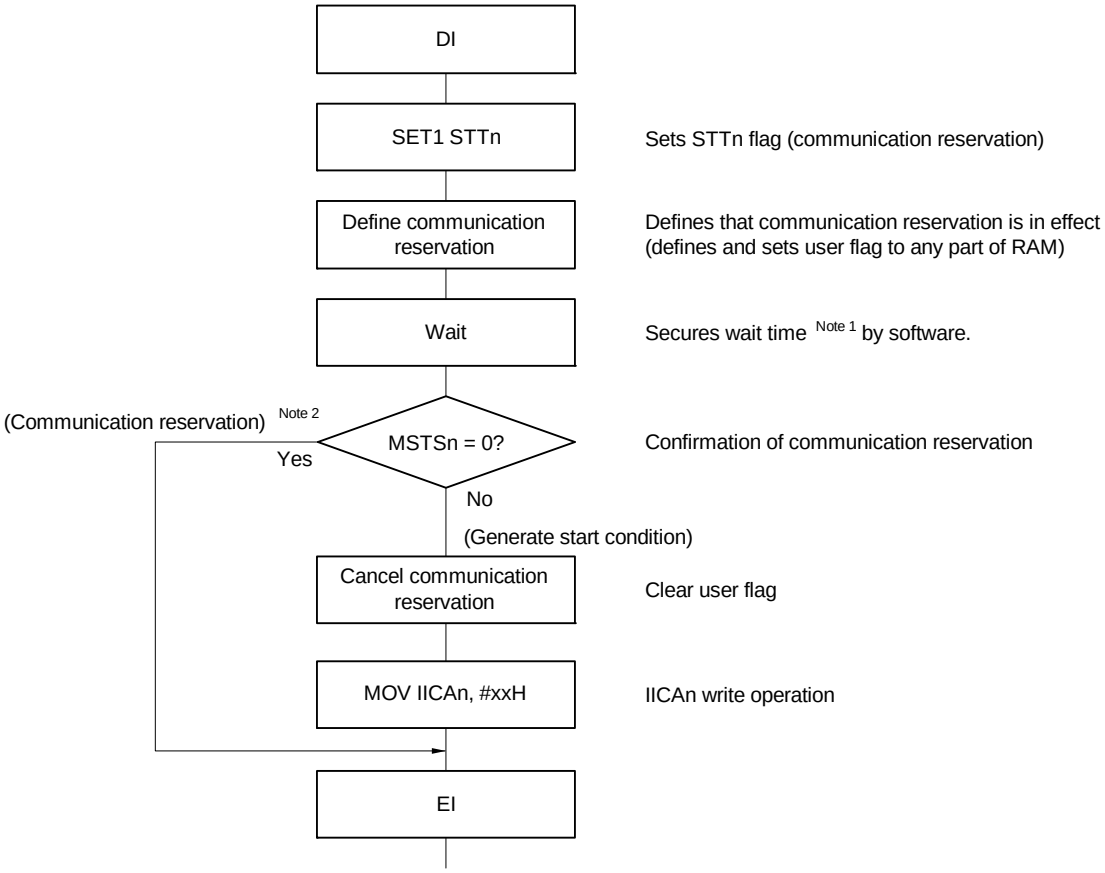


Figure 21 - 32 shows the Communication Reservation Protocol.

Remark n = 0

Figure 21 - 32 Communication Reservation Protocol



Note 1. The wait time is calculated as follows.
(IICWLn setting value + IICWHn setting value + 4) /f_{MCK}+ t_F × 2

Note 2. The communication reservation operation executes a write to the IICA shift register n (IICAn) when a stop condition interrupt request occurs.

Remark 1. STTn: Bit 1 of IICA control register n0 (IICCTLn0)
MSTSn: Bit 7 of IICA status register n (IICSn)
IICAn: IICA shift register n
IICWLn: IICA low-level width setting register n
IICWHn: IICA high-level width setting register n
t_F: SDAAn and SCLAn signal falling times
f_{MCK}: IICA operating clock frequency

Remark 2. n = 0

(2) When communication reservation function is disabled (bit 0 (IICRSVn) of IICA flag register n (IICFn) = 1)
When bit 1 (STTn) of IICA control register n0 (IICCTLn0) is set to 1 when the bus is not used in a communication during bus communication, this request is rejected and a start condition is not generated. The following two statuses are included in the status where bus is not used.

- When arbitration results in neither master nor slave operation
- When an extension code is received and slave operation is disabled (ACK is not returned and the bus was released by setting bit 6 (LRELn) of the IICCTLn0 register to 1 and saving communication)

To confirm whether the start condition was generated or request was rejected, check STCFn (bit 7 of the IICFn register). It takes up to five f_{MCK} clocks until the STCFn bit is set to 1 after setting STTn = 1. Therefore, secure the time by software.

Remark n = 0

21.5.15 Cautions

(1) When STCENn = 0

Immediately after I^2C operation is enabled (IICEn = 1), the bus communication status (IICBSYn = 1) is recognized regardless of the actual bus status. When changing from a mode in which no stop condition has been detected to a master device communication mode, first generate a stop condition to release the bus, then perform master device communication.

When using multiple masters, it is not possible to perform master device communication when the bus has not been released (when a stop condition has not been detected).

Use the following sequence for generating a stop condition.

<1> Set IICA control register n1 (IICCTLn1).
<2> Set bit 7 (IICEn) of IICA control register n0 (IICCTLn0) to 1.
<3> Set bit 0 (SPTn) of the IICCTLn0 register to 1.

(2) When STCENn = 1

Immediately after I^2C operation is enabled (IICEn = 1), the bus released status (IICBSYn = 0) is recognized regardless of the actual bus status. To generate the first start condition (STTn = 1), it is necessary to confirm that the bus has been released, so as to not disturb other communications.

(3) If other I^2C communications are already in progress

If I^2C operation is enabled and the device participates in communication already in progress when the SDAAn pin is low and the SCLAn pin is high, the macro of I^2C recognizes that the SDAAn pin has gone low (detects a start condition). If the value on the bus at this time can be recognized as an extension code, ACK is returned, but this interferes with other I^2C communications. To avoid this, start I^2C in the following sequence.

<1> Clear bit 4 (SPIEn) of the IICCTLn0 register to 0 to disable generation of an interrupt request signal (INTIICAn) when the stop condition is detected.
<2> Set bit 7 (IICEn) of the IICCTLn0 register to 1 to enable the operation of I^2C.
<3> Wait for detection of the start condition.
<4> Set bit 6 (LRELn) of the IICCTLn0 register to 1 before ACK is returned (4 to 80 clocks after setting the IICEn bit to 1), to forcibly disable detection.

(4) Setting the STTn and SPTn bits (bits 1 and 0 of the IICCTLn0 register) again after they are set and before they are cleared to 0 is prohibited.

(5) When transmission is reserved, set the SPIEn bit (bit 4 of the IICCTLn0 register) to 1 so that an interrupt request is generated when the stop condition is detected. Transfer is started when communication data is written to the IICA shift register n (IICAn) after the interrupt request is generated. Unless the interrupt is generated when the stop condition is detected, the device stops in the wait state because the interrupt request is not generated when communication is started. However, it is not necessary to set the SPIEn bit to 1 when the MSTSn bit (bit 7 of the IICA status register n (IICSn)) is detected by software.

Remark n = 0

21.5.16 Communication operations

The following shows three operation procedures with the flowchart.

(1) Master operation in single master system

The flowchart when using the RL78/H1D as the master in a single master system is shown below.

This flowchart is broadly divided into the initial settings and communication processing. Execute the initial settings at startup. If communication with the slave is required, prepare the communication and then execute communication processing.

(2) Master operation in multimaster system

In the I^2C bus multimaster system, whether the bus is released or used cannot be judged by the I^2C bus specifications when the bus takes part in a communication. Here, when data and clock are at a high level for a certain period (1 frame), the RL78/H1D takes part in a communication with bus released state.

This flowchart is broadly divided into the initial settings, communication waiting, and communication processing. The processing when the RL78/H1D looses in arbitration and is specified as the slave is omitted here, and only the processing as the master is shown. Execute the initial settings at startup to take part in a communication. Then, wait for the communication request as the master or wait for the specification as the slave. The actual communication is performed in the communication processing, and it supports the transmission/reception with the slave and the arbitration with other masters.

(3) Slave operation

An example of when the RL78/H1D is used as the I^2C bus slave is shown below.

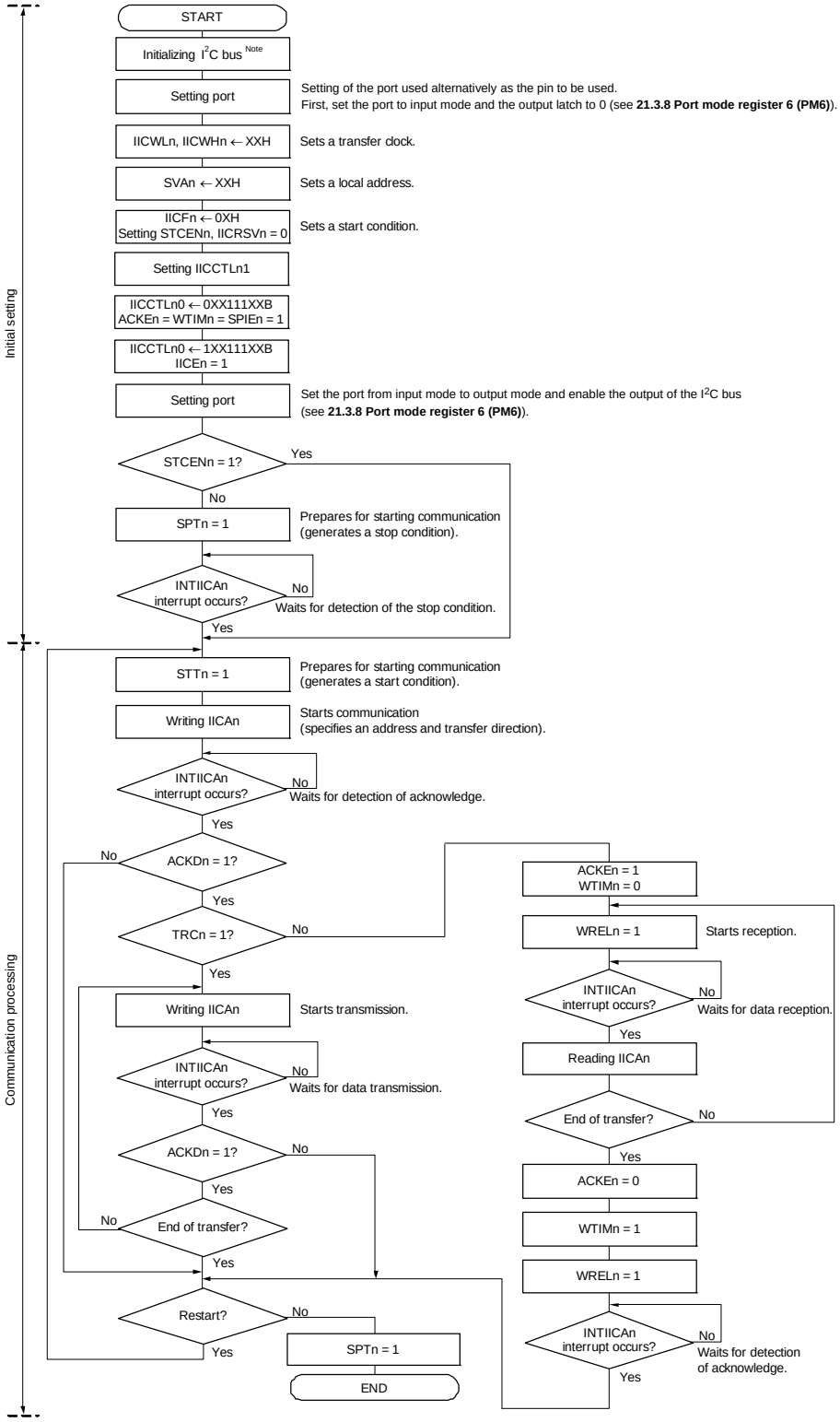
When used as the slave, operation is started by an interrupt. Execute the initial settings at startup, then wait for the INTIICAn interrupt occurrence (communication waiting). When an INTIICAn interrupt occurs, the communication status is judged and its result is passed as a flag over to the main processing.

By checking the flags, necessary communication processing is performed.

Remark n = 0

(1) Master operation in single master system

Figure 21 - 33 Master Operation in Single-Master System



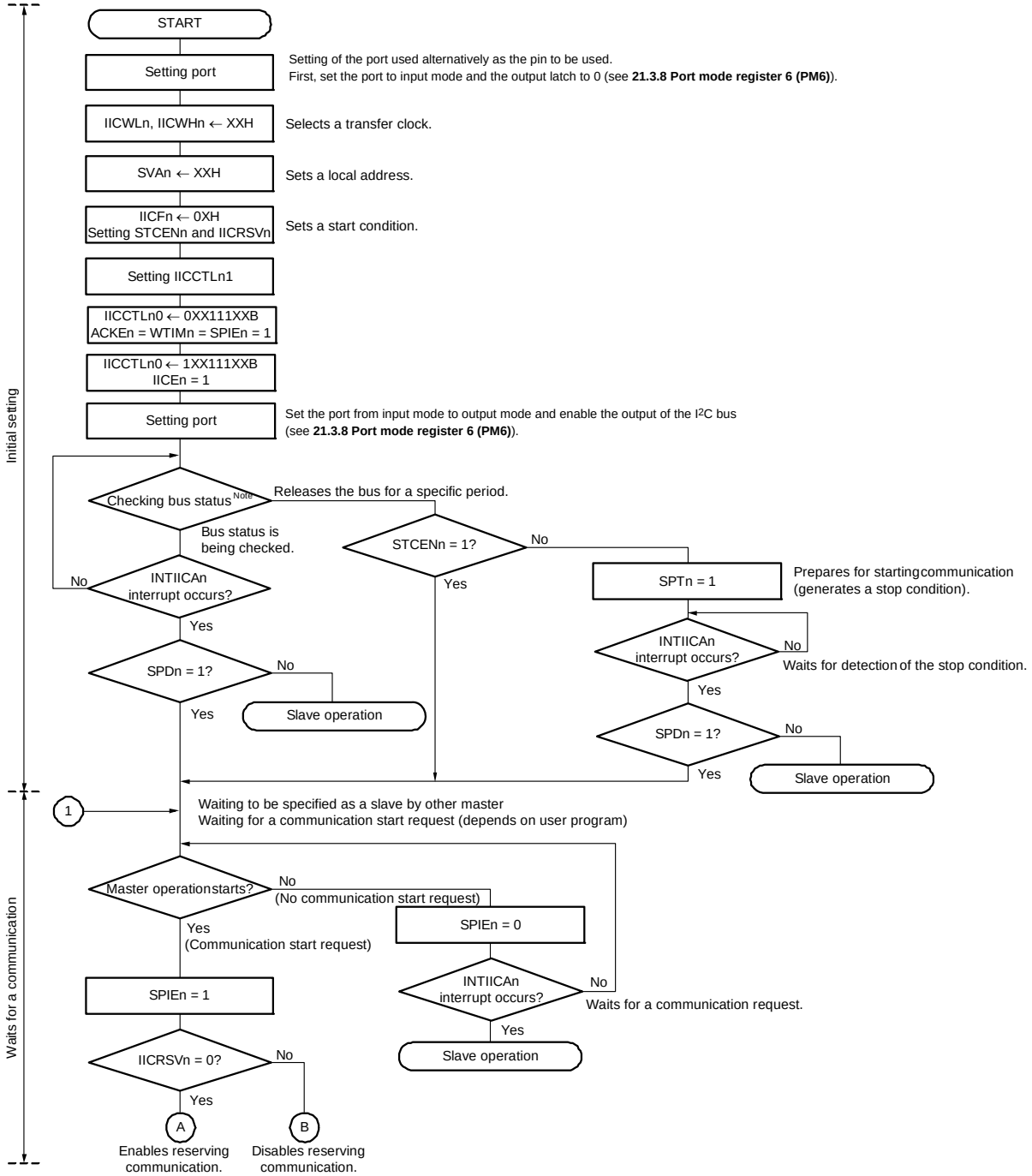
Note Release (SCLAn and SDAAn pins = high level) the I2C bus in conformance with the specifications of the product that is communicating. If EEPROM is outputting a low level to the SDAAn pin, for example, set the SCLAn pin in the output port mode, and output a clock pulse from the output port until the SDAAn pin is constantly at high level.

Remark 1. Conform to the specifications of the product that is communicating, with respect to the transmission and reception formats.

Remark 2. n = 0

(2) Master operation in multimaster system

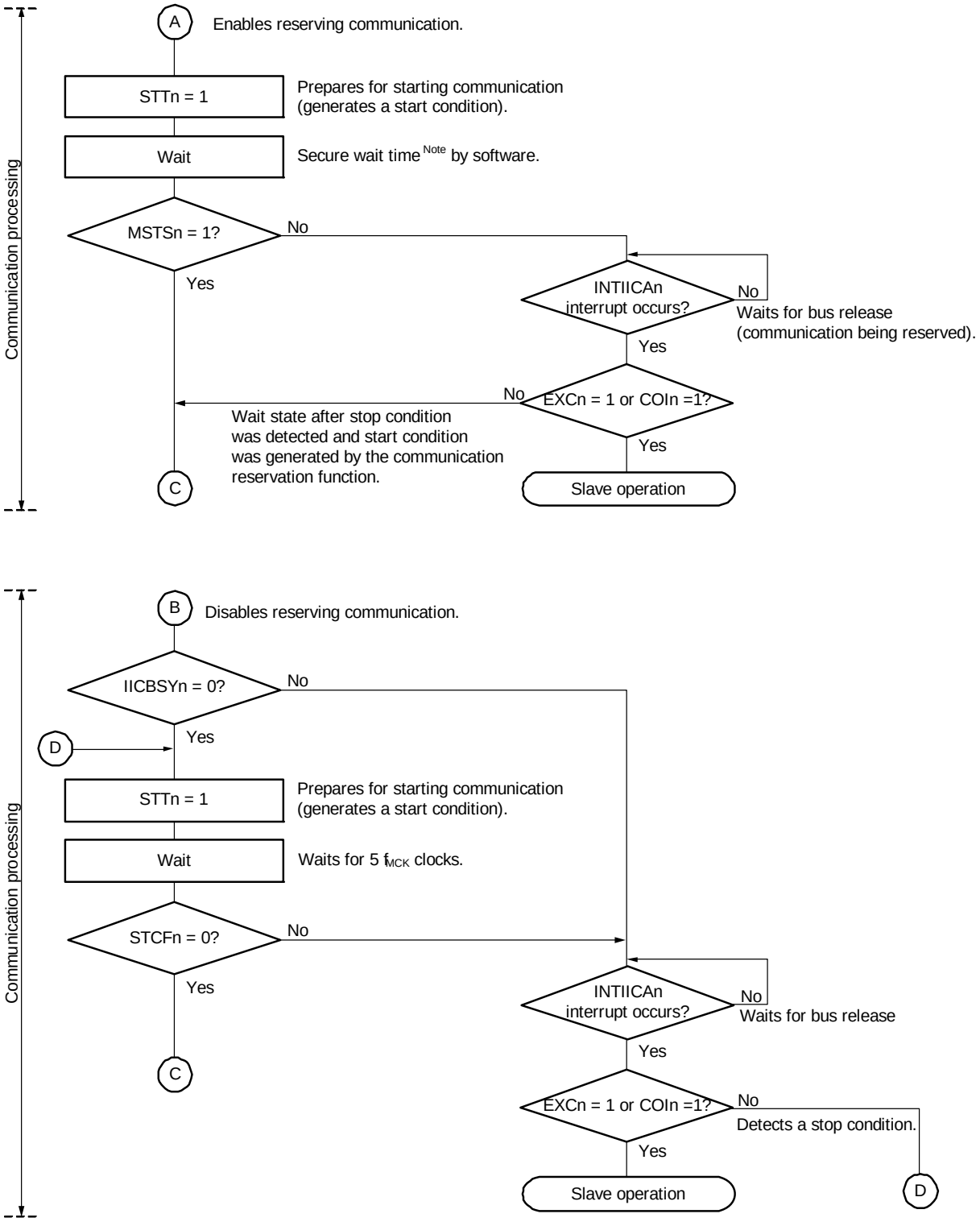
Figure 21 - 34 Master Operation in Multi-Master System (1/3)



Note Confirm that the bus is released (CLDn bit = 1, DADn bit = 1) for a specific period (for example, for a period of one frame). If the SDAAn pin is constantly at low level, decide whether to release the I^2C bus (SCLAn and SDAAn pins = high level) in conformance with the specifications of the product that is communicating.

Remark n = 0

Figure 21 - 35 Master Operation in Multi-Master System (2/3)

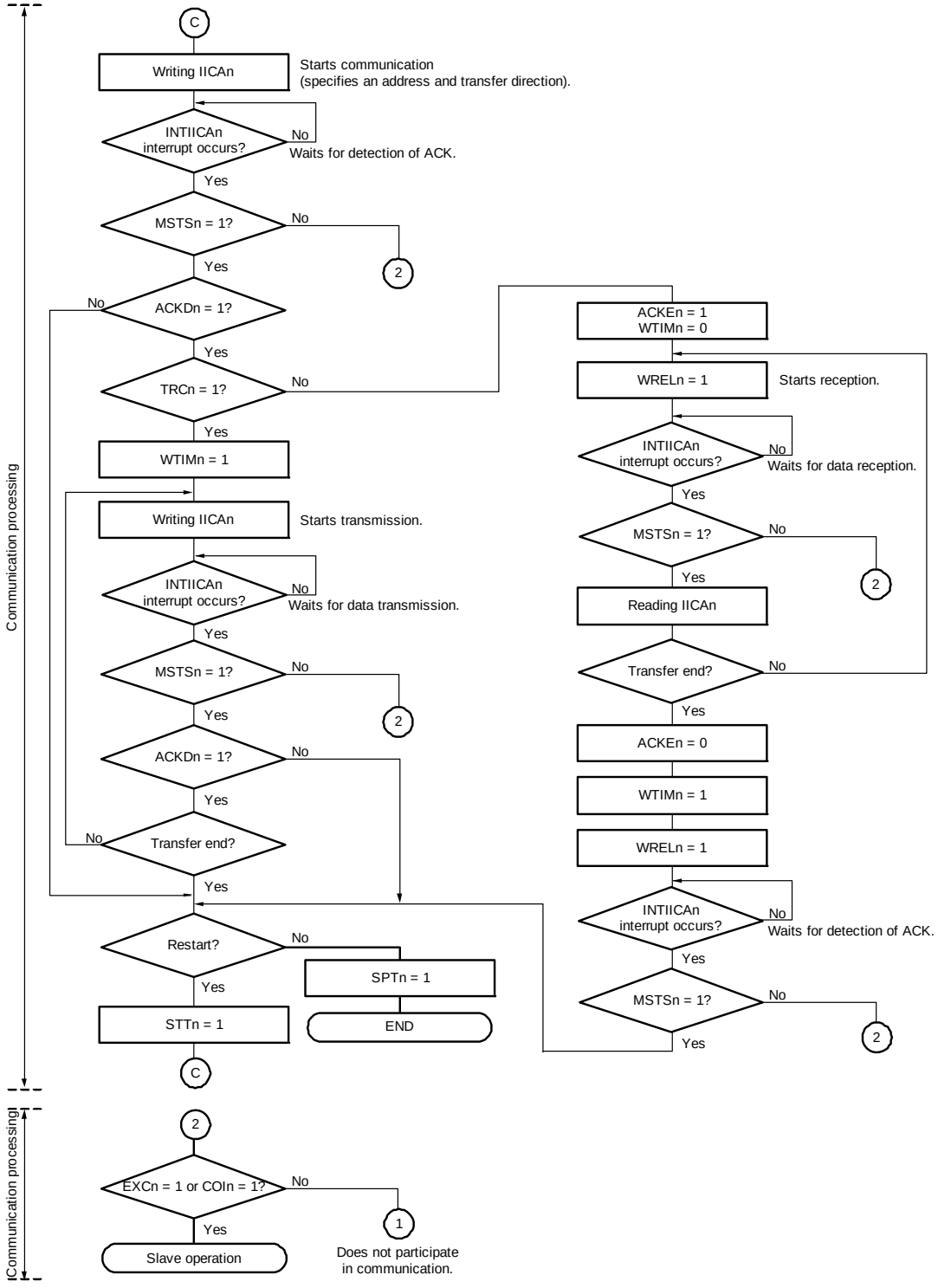


Note The wait time is calculated as follows.
(IICWLn setting value + IICWHn setting value + 4) /f_{MCK} + t_F × 2

Remark 1. IICWLn: IICA low-level width setting register n
IICWHn: IICA high-level width setting register n
t_F: SDAAn and SCLAn signal falling times
f_{MCK}: IICA operating clock frequency

Remark 2. n = 0

Figure 21 - 36 Master Operation in Multi-Master System (3/3)



Remark 1. Conform to the specifications of the product that is communicating, with respect to the transmission and reception formats.

Remark 2. To use the device as a master in a multi-master system, read the MSTSn bit each time interrupt INTIICAn has occurred to check the arbitration result.

Remark 3. To use the device as a slave in a multi-master system, check the status by using the IICA status register n (IICSn) and IICA flag register n (IICFn) each time interrupt INTIICAn has occurred, and determine the processing to be performed next.

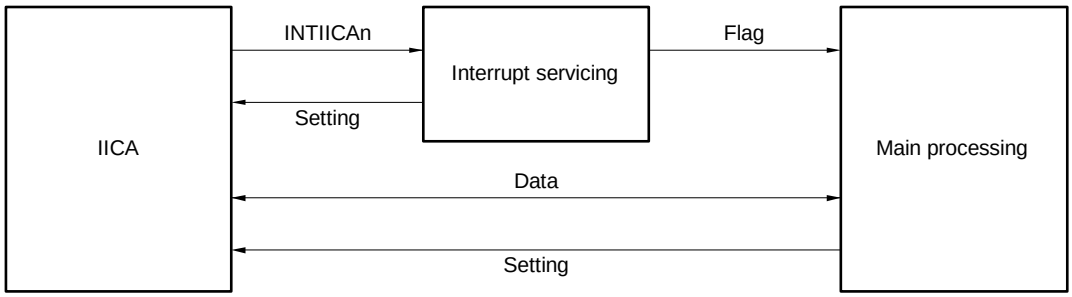
Remark 4. n = 0

(3) Slave operation

The processing procedure of the slave operation is as follows.

Basically, the slave operation is event-driven. Therefore, processing by the INTIICAn interrupt (processing that must substantially change the operation status such as detection of a stop condition during communication) is necessary.

In the following explanation, it is assumed that the extension code is not supported for data communication. It is also assumed that the INTIICAn interrupt servicing only performs status transition processing, and that actual data communication is performed by the main processing.



Therefore, data communication processing is performed by preparing the following three flags and passing them to the main processing instead of INTIICAn.

<1> Communication mode flag

This flag indicates the following two communication statuses.

- •Clear mode: Status in which data communication is not performed
- •Communication mode: Status in which data communication is performed (from valid address detection to stop condition detection, no detection of ACK from master, address mismatch)

<2> Ready flag

This flag indicates that data communication is enabled. Its function is the same as the INTIICAn interrupt for ordinary data communication. This flag is set by interrupt servicing and cleared by the main processing. Clear this flag by interrupt servicing when communication is started. However, the ready flag is not set by interrupt servicing when the first data is transmitted. Therefore, the first data is transmitted without the flag being cleared (an address match is interpreted as a request for the next data).

<3> Communication direction flag

This flag indicates the direction of communication. Its value is the same as the TRCn bit.

Remark n = 0

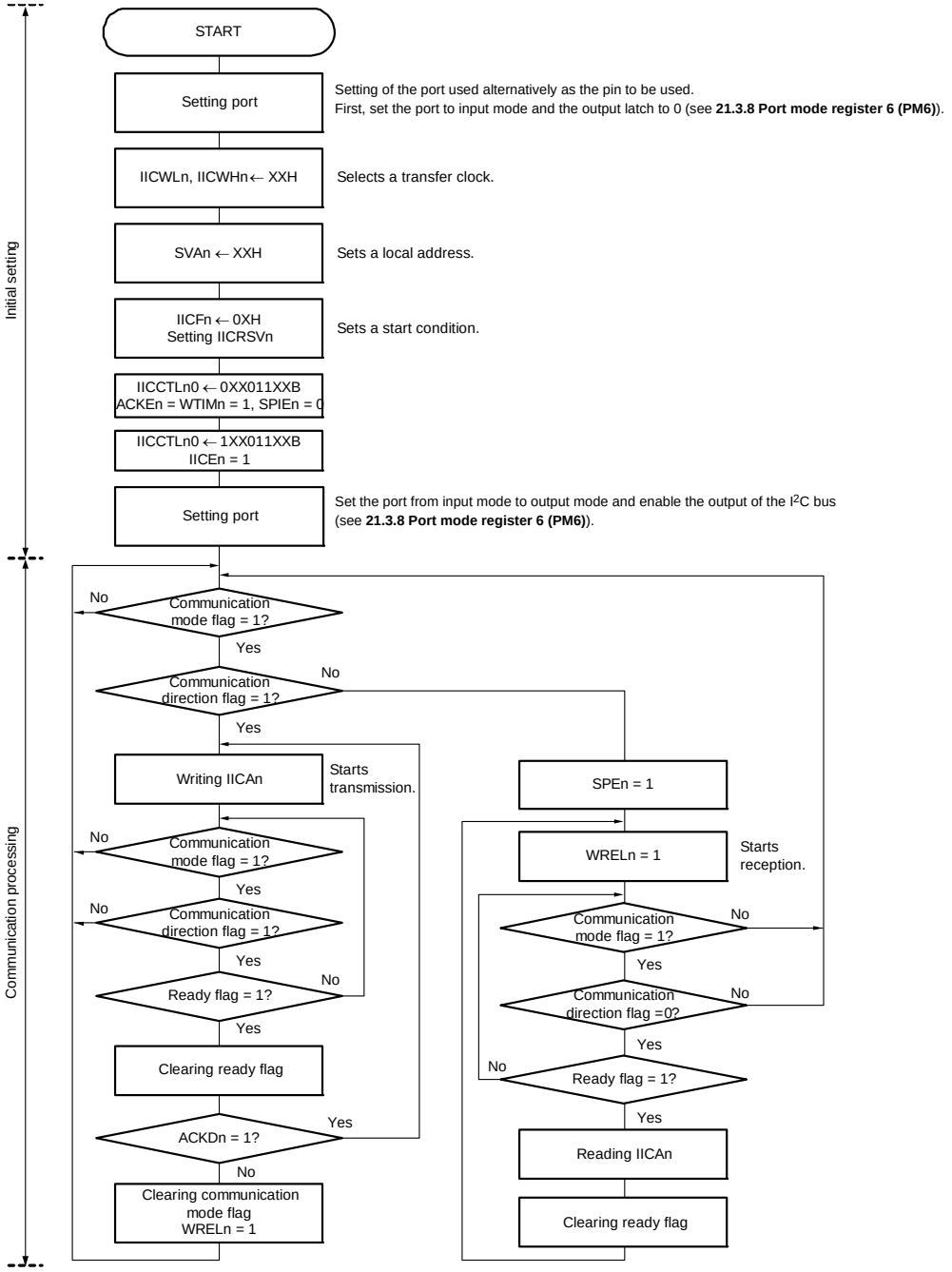
The main processing of the slave operation is explained next.

Start serial interface IICA and wait until communication is enabled. When communication is enabled, execute communication by using the communication mode flag and ready flag (processing of the stop condition and start condition is performed by an interrupt. Here, check the status by using the flags).

The transmission operation is repeated until the master no longer returns ACK. If ACK is not returned from the master, communication is completed.

For reception, the necessary amount of data is received. When communication is completed, ACK is not returned as the next data. After that, the master generates a stop condition or restart condition. Exit from the communication status occurs in this way.

Figure 21 - 37 Slave Operation Flowchart (1)



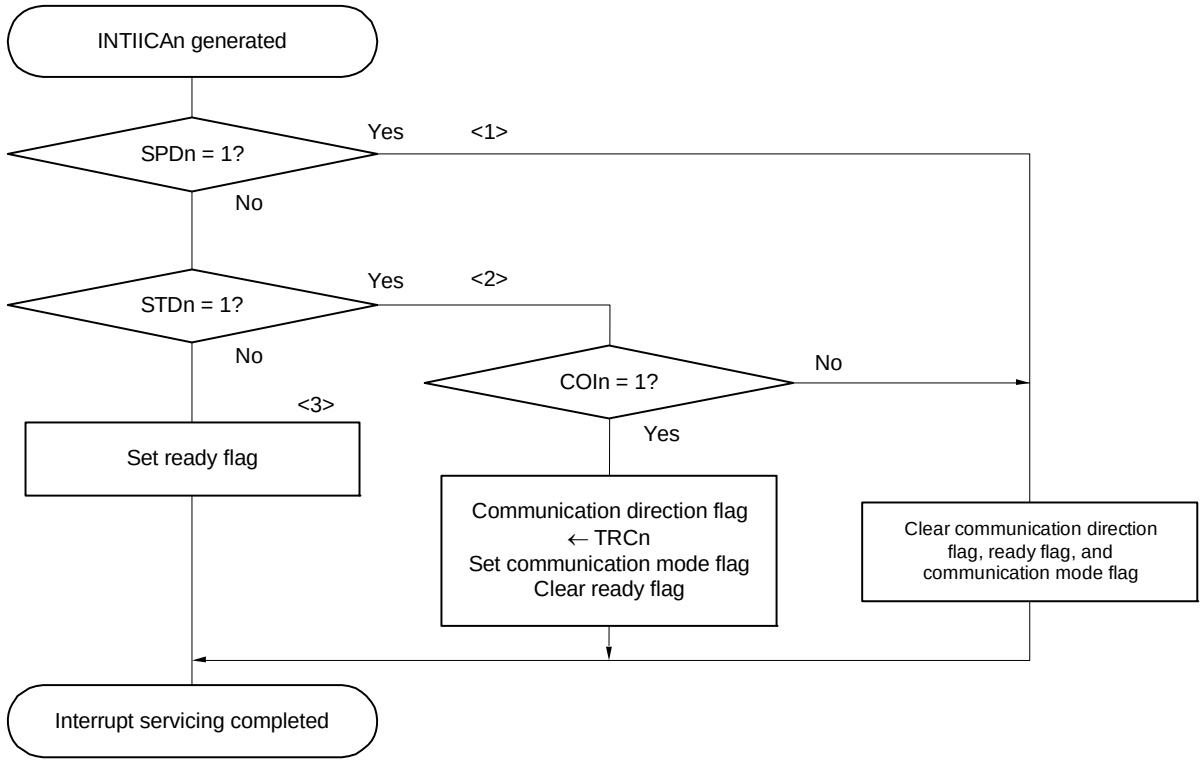
Remark 1. Conform to the specifications of the product that is in communication, regarding the transmission and reception formats.
Remark 2. n = 0

An example of the processing procedure of the slave with the INTIICAn interrupt is explained below (processing is performed assuming that no extension code is used). The INTIICAn interrupt checks the status, and the following operations are performed.

<1> Communication is stopped if the stop condition is issued.
<2> If the start condition is issued, the address is checked and communication is completed if the address does not match. If the address matches, the communication mode is set, wait is cancelled, and processing returns from the interrupt (the ready flag is cleared).
<3> For data transmit/receive, only the ready flag is set. Processing returns from the interrupt with the I^2C bus remaining in the wait state.

Remark <1> to <3> above correspond to <1> to <3> in **Figure 21 - 38 Slave Operation Flowchart (2)**.

Figure 21 - 38 Slave Operation Flowchart (2)



Remark n = 0

21.5.17 Timing of I²C interrupt request (INTIICAn) occurrence

The timing of transmitting or receiving data and generation of interrupt request signal INTIICAn, and the value of the IICA status register n (IICSn) when the INTIICAn signal is generated are shown below.

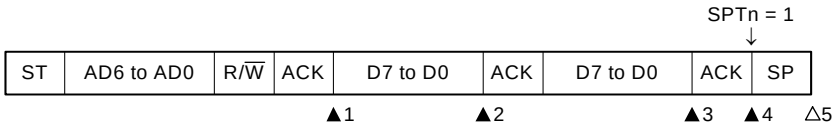
Remark 1. ST: Start condition
AD6 to AD0: Address
R/$\overline{W}$: Transfer direction specification
ACK: Acknowledge
D7 to D0: Data
SP: Stop condition

Remark 2. n = 0

(1) Master device operation

(a) Start ~ Address ~ Data ~ Data ~ Stop (transmission/reception)

(i) When WTIMn = 0



▲1: IICSn = 1000×110B

▲2: IICSn = 1000×000B

▲3: IICSn = 1000×000B (Sets the WTIMn bit to 1) Note

▲4: IICSn = 1000××00B (Sets the SPTn bit to 1) Note

△5: IICSn = 00000001B

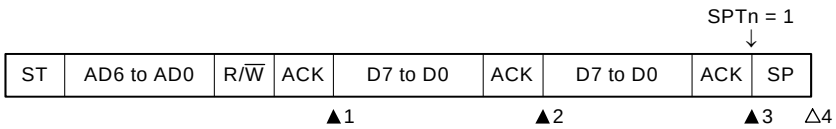
Note To generate a stop condition, set the WTIMn bit to 1 and change the timing for generating the INTIICAn interrupt request signal.

Remark ▲: Always generated

△: Generated only when SPIEn = 1

×: Don't care

(ii) When WTIMn = 1



▲1: IICSn = 1000×110B

▲2: IICSn = 1000×100B

▲3: IICSn = 1000××00B (Sets the SPTn bit to 1)

△4: IICSn = 00000001B

Remark ▲: Always generated

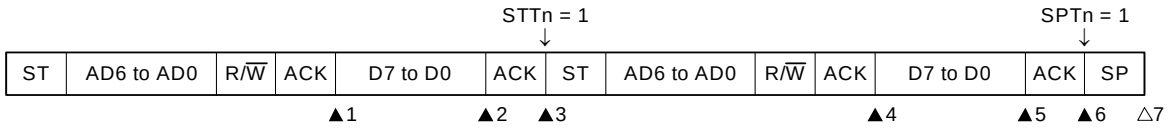
△: Generated only when SPIEn = 1

×: Don't care

Remark n = 0

(b) Start ~ Address ~ Data ~ Start ~ Address ~ Data ~ Stop (restart)

(i) When WTIMn = 0



▲1: IICSn = 1000×110B

▲2: IICSn = 1000×000B (Sets the WTIMn bit to 1) Note 1

▲3: IICSn = 1000××00B (Clears the WTIMn bit to 0 Note 2, sets the STTn bit to 1)

▲4: IICSn = 1000×110B

▲5: IICSn = 1000×000B (Sets the WTIMn bit to 1) Note 3

▲6: IICSn = 1000××00B (Sets the SPTn bit to 1)

△7: IICSn = 00000001B

Note 1. To generate a start condition, set the WTIMn bit to 1 and change the timing for generating the INTIICAn interrupt request signal.

Note 2. Clear the WTIMn bit to 0 to restore the original setting.

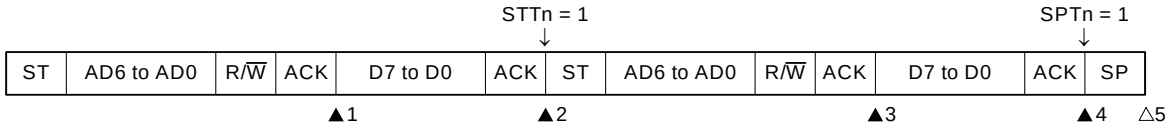
Note 3. To generate a stop condition, set the WTIMn bit to 1 and change the timing for generating the INTIICAn interrupt request signal.

Remark ▲: Always generated

△: Generated only when SPIEn = 1

×: Don't care

(ii) When WTIMn = 1



▲1: IICSn = 1000×110B

▲2: IICSn = 1000××00B (Sets the STTn bit to 1)

▲3: IICSn = 1000×110B

▲4: IICSn = 1000××00B (Sets the SPTn bit to 1)

△5: IICSn = 00000001B

Remark ▲: Always generated

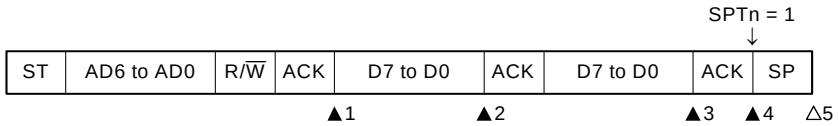
△: Generated only when SPIEn = 1

×: Don't care

Remark n = 0

(c) Start ~ Code ~ Data ~ Data ~ Stop (extension code transmission)

(i) When WTIMn = 0



▲1: IICSn = 1010×110B

▲2: IICSn = 1010×000B

▲3: IICSn = 1010×000B (Sets the WTIMn bit to 1) Note

▲4: IICSn = 1010××00B (Sets the SPTn bit to 1)

△5: IICSn = 00000001B

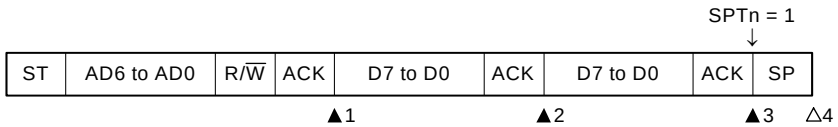
Note To generate a stop condition, set the WTIMn bit to 1 and change the timing for generating the INTIICAn interrupt request signal.

Remark ▲: Always generated

△: Generated only when SPIEn = 1

×: Don't care

(ii) When WTIMn = 1



▲1: IICSn = 1010×110B

▲2: IICSn = 1010×100B

▲3: IICSn = 1010××00B (Sets the SPTn bit to 1)

△4: IICSn = 00000001B

Remark ▲: Always generated

△: Generated only when SPIEn = 1

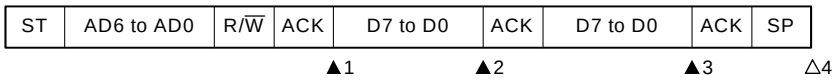
×: Don't care

Remark n = 0

(2) Slave device operation (slave address data reception)

(a) Start ~ Address ~ Data ~ Data ~ Stop

(i) When WTIMn = 0



▲1: IICSn = 0001×110B

▲2: IICSn = 0001×000B

▲3: IICSn = 0001×000B

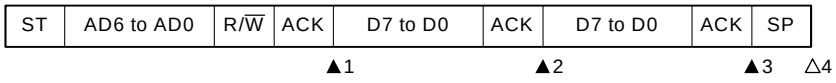
△4: IICSn = 00000001B

Remark ▲: Always generated

△: Generated only when SPIEn = 1

×: Don't care

(ii) When WTIMn = 1



▲1: IICSn = 0001×110B

▲2: IICSn = 0001×100B

▲3: IICSn = 0001××00B

△4: IICSn = 00000001B

Remark ▲: Always generated

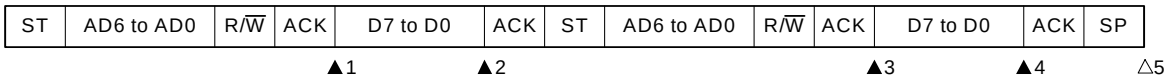
△: Generated only when SPIEn = 1

×: Don't care

Remark n = 0

(b) Start ~ Address ~ Data ~ Start ~ Address ~ Data ~ Stop

(i) When WTIMn = 0 (after restart, matches with SVAn)



▲1: IICSn = 0001×110B

▲2: IICSn = 0001×000B

▲3: IICSn = 0001×110B

▲4: IICSn = 0001×000B

△5: IICSn = 00000001B

Remark ▲: Always generated

△: Generated only when SPIEn = 1

×: Don't care

(ii) When WTIMn = 1 (after restart, matches with SVAn)

▲1: IICSn = 0001×110B

▲2: IICSn = 0001××00B

▲3: IICSn = 0001×110B

▲4: IICSn = 0001××00B

△5: IICSn = 00000001B

Remark ▲: Always generated

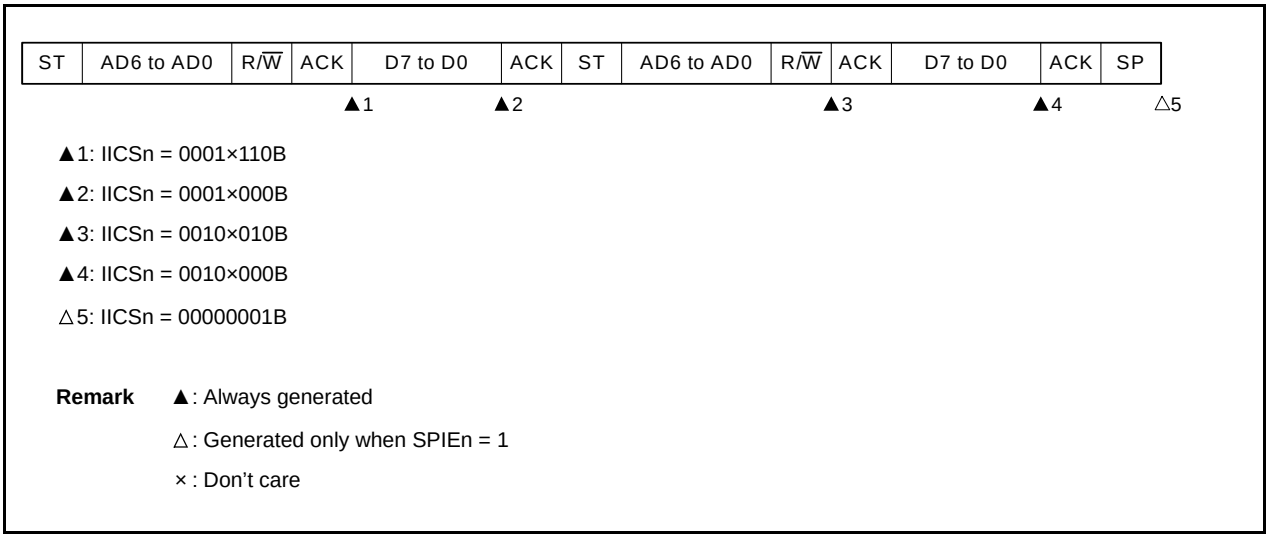
△: Generated only when SPIEn = 1

×: Don't care

Remark n = 0

(c) Start ~ Address ~ Data ~ Start ~ Code ~ Data ~ Stop

(i) When WTIMn = 0 (after restart, does not match address (= extension code))



▲1: IICSn = 0001×110B

▲2: IICSn = 0001×000B

▲3: IICSn = 0010×010B

▲4: IICSn = 0010×000B

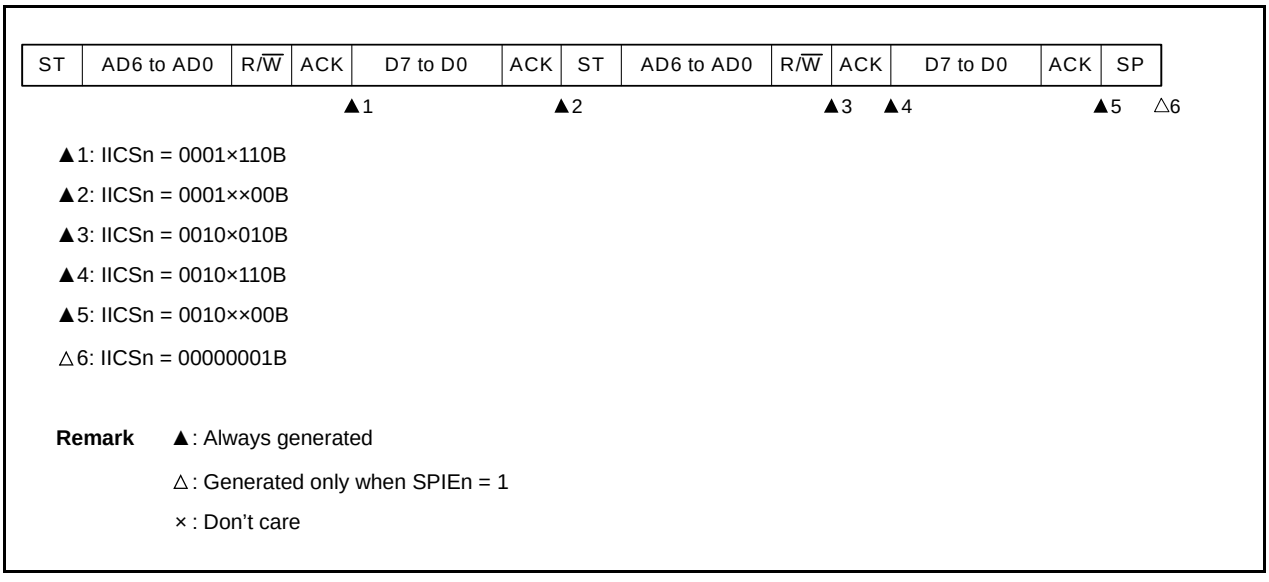
△5: IICSn = 00000001B

Remark ▲: Always generated

△: Generated only when SPIEn = 1

×: Don't care

(ii) When WTIMn = 1 (after restart, does not match address (= extension code))



▲1: IICSn = 0001×110B

▲2: IICSn = 0001××00B

▲3: IICSn = 0010×010B

▲4: IICSn = 0010×110B

▲5: IICSn = 0010××00B

△6: IICSn = 00000001B

Remark ▲: Always generated

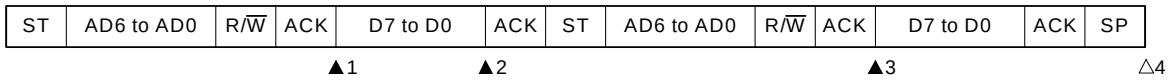
△: Generated only when SPIEn = 1

×: Don't care

Remark n = 0

(d) Start ~ Address ~ Data ~ Start ~ Address ~ Data ~ Stop

(i) When WTIMn = 0 (after restart, does not match address (= not extension code))



▲1: IICSn = 0001×110B

▲2: IICSn = 0001×000B

▲3: IICSn = 00000110B

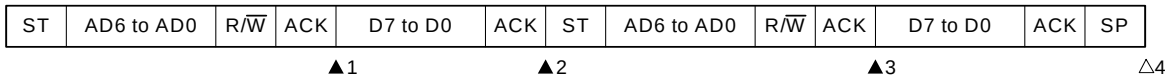
△4: IICSn = 00000001B

Remark ▲: Always generated

△: Generated only when SPIEn = 1

×: Don't care

(ii) When WTIMn = 1 (after restart, does not match address (= not extension code))



▲1: IICSn = 0001×110B

▲2: IICSn = 0001××00B

▲3: IICSn = 00000110B

△4: IICSn = 00000001B

Remark ▲: Always generated

△: Generated only when SPIEn = 1

×: Don't care

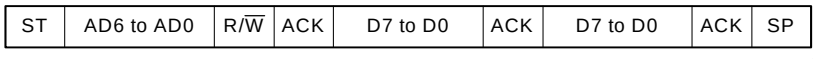
Remark n = 0

(3) Slave device operation (when receiving extension code)

The device is always participating in communication when it receives an extension code.

(a) Start ~ Code ~ Data ~ Data ~ Stop

(i) When WTIMn = 0



▲1: IICSn = 0010×010B

▲2: IICSn = 0010×000B

▲3: IICSn = 0010×000B

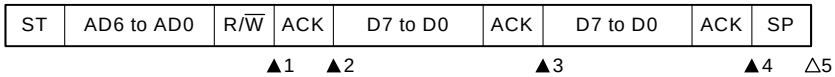
△4: IICSn = 00000001B

Remark ▲: Always generated

△: Generated only when SPIEn = 1

×: Don't care

(ii) When WTIMn = 1



▲1: IICSn = 0010×010B

▲2: IICSn = 0010×110B

▲3: IICSn = 0010×100B

▲4: IICSn = 0010××00B

△5: IICSn = 00000001B

Remark ▲: Always generated

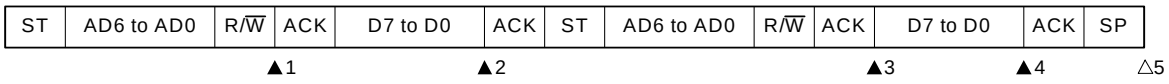
△: Generated only when SPIEn = 1

×: Don't care

Remark n = 0

(b) Start ~ Code ~ Data ~ Start ~ Address ~ Data ~ Stop

(i) When WTIMn = 0 (after restart, matches SVAn)



▲1: IICSn = 0010×010B

▲2: IICSn = 0010×000B

▲3: IICSn = 0001×110B

▲4: IICSn = 0001×000B

△5: IICSn = 00000001B

Remark ▲: Always generated

△: Generated only when SPIEn = 1

×: Don't care

(ii) When WTIMn = 1 (after restart, matches SVAn)

▲1: IICSn = 0010×010B

▲2: IICSn = 0010×110B

▲3: IICSn = 0010××00B

▲4: IICSn = 0001×110B

▲5: IICSn = 0001××00B

△6: IICSn = 00000001B

Remark ▲: Always generated

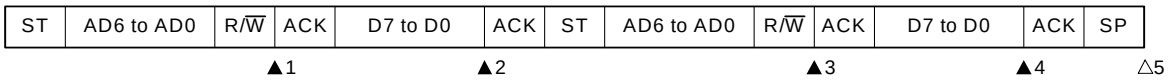
△: Generated only when SPIEn = 1

×: Don't care

Remark n = 0

(c) Start ~ Code ~ Data ~ Start ~ Code ~ Data ~ Stop

(i) When WTIMn = 0 (after restart, extension code reception)



▲1: IICSn = 0010×010B

▲2: IICSn = 0010×000B

▲3: IICSn = 0010×010B

▲4: IICSn = 0010×000B

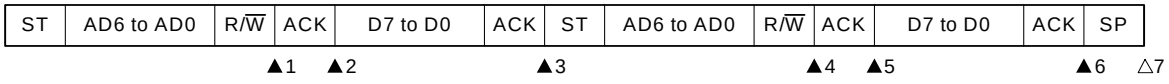
△5: IICSn = 00000001B

Remark ▲: Always generated

△: Generated only when SPIEn = 1

×: Don't care

(ii) When WTIMn = 1 (after restart, extension code reception)



▲1: IICSn = 0010×010B

▲2: IICSn = 0010×110B

▲3: IICSn = 0010××00B

▲4: IICSn = 0010×010B

▲5: IICSn = 0010×110B

▲6: IICSn = 0010××00B

△7: IICSn = 00000001B

Remark ▲: Always generated

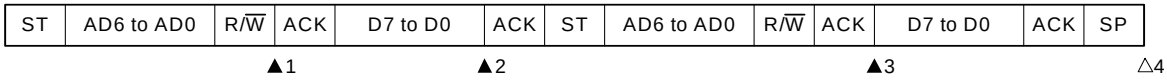
△: Generated only when SPIEn = 1

×: Don't care

Remark n = 0

(d) Start ~ Code ~ Data ~ Start ~ Address ~ Data ~ Stop

(i) When WTIMn = 0 (after restart, does not match address (= not extension code))



▲1: IICSn = 0010 × 010B

▲2: IICSn = 0010 × 000B

▲3: IICSn = 00000 × 10B

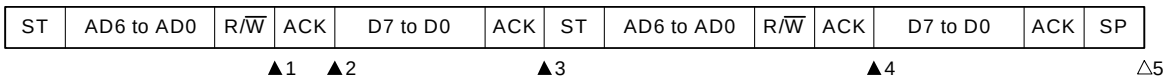
△4: IICSn = 00000001B

Remark ▲: Always generated

△: Generated only when SPIEn = 1

×: Don't care

(ii) When WTIMn = 1 (after restart, does not match address (= not extension code))



▲1: IICSn = 0010 × 010B

▲2: IICSn = 0010 × 110B

▲3: IICSn = 0010 × × 00B

▲4: IICSn = 00000 × 10B

△5: IICSn = 00000001B

Remark ▲: Always generated

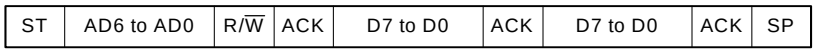
△: Generated only when SPIEn = 1

×: Don't care

Remark n = 0

(4) Operation without communication

(a) Start ~ Code ~ Data ~ Data ~ Stop



△1: IICSn = 00000001B

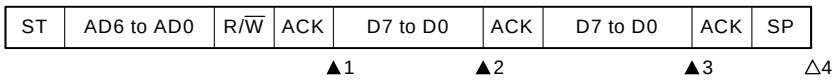
Remark △: Generated only when SPIEn = 1

(5) Arbitration loss operation (operation as slave after arbitration loss)

When the device is used as a master in a multi-master system, read the MSTSn bit each time interrupt request signal INTIICAn has occurred to check the arbitration result.

(a) When arbitration loss occurs during transmission of slave address data

(i) When WTIMn = 0



▲1: IICSn = 0101×110B

▲2: IICSn = 0001×000B

▲3: IICSn = 0001×000B

△4: IICSn = 00000001B

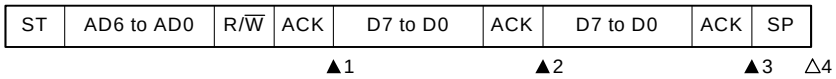
Remark ▲: Always generated

△: Generated only when SPIEn = 1

×: Don't care

Remark n = 0

(ii) When WTIMn = 1



▲1: IICSn = 0101×110B

▲2: IICSn = 0001×100B

▲3: IICSn = 0001××00B

△4: IICSn = 00000001B

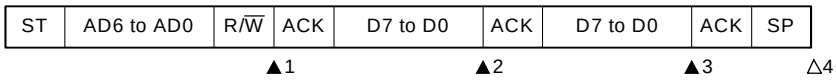
Remark ▲: Always generated

△: Generated only when SPIEn = 1

×: Don't care

(b) When arbitration loss occurs during transmission of extension code

(i) When WTIMn = 0



▲1: IICSn = 0110×010B

▲2: IICSn = 0010×000B

▲3: IICSn = 0010×000B

△4: IICSn = 00000001B

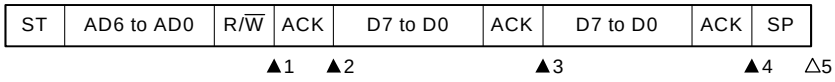
Remark ▲: Always generated

△: Generated only when SPIEn = 1

×: Don't care

Remark n = 0

(ii) When WTIMn = 1



▲1: IICSn = 0110×010B

▲2: IICSn = 0010×110B

▲3: IICSn = 0010×100B

▲4: IICSn = 0010××00B

△5: IICSn = 00000001B

Remark ▲: Always generated

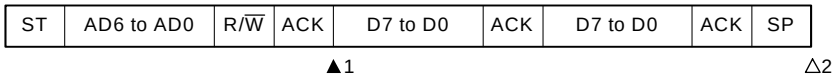
△: Generated only when SPIEn = 1

×: Don't care

(6) Operation when arbitration loss occurs (no communication after arbitration loss)

When the device is used as a master in a multi-master system, read the MSTSn bit each time interrupt request signal INTIICAn has occurred to check the arbitration result.

(a) When arbitration loss occurs during transmission of slave address data (when WTIMn = 1)



▲1: IICSn = 01000110B

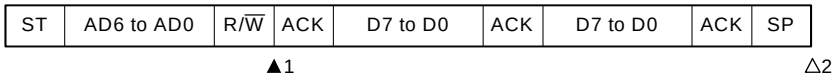
△2: IICSn = 00000001B

Remark ▲: Always generated

△: Generated only when SPIEn = 1

Remark n = 0

(b) When arbitration loss occurs during transmission of extension code



▲1 △2

▲1: IICSn = 0110×010B

Sets LRELn = 1 by software

△2: IICSn = 00000001B

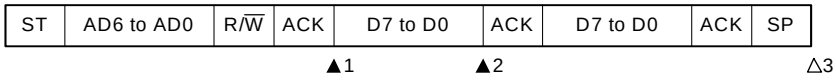
Remark ▲: Always generated

△: Generated only when SPIEn = 1

×: Don't care

(c) When arbitration loss occurs during transmission of data

(i) When WTIMn = 0



▲1 ▲2 △3

▲1: IICSn = 10001110B

▲2: IICSn = 01000000B

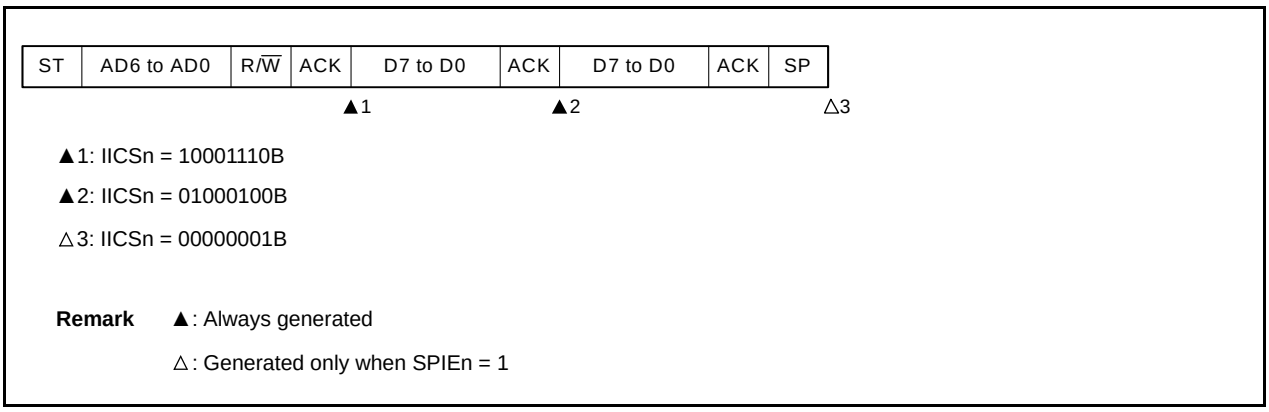
△3: IICSn = 00000001B

Remark ▲: Always generated

△: Generated only when SPIEn = 1

Remark n = 0

(ii) When WTIMn = 1



▲1: IICSn = 10001110B

▲2: IICSn = 01000100B

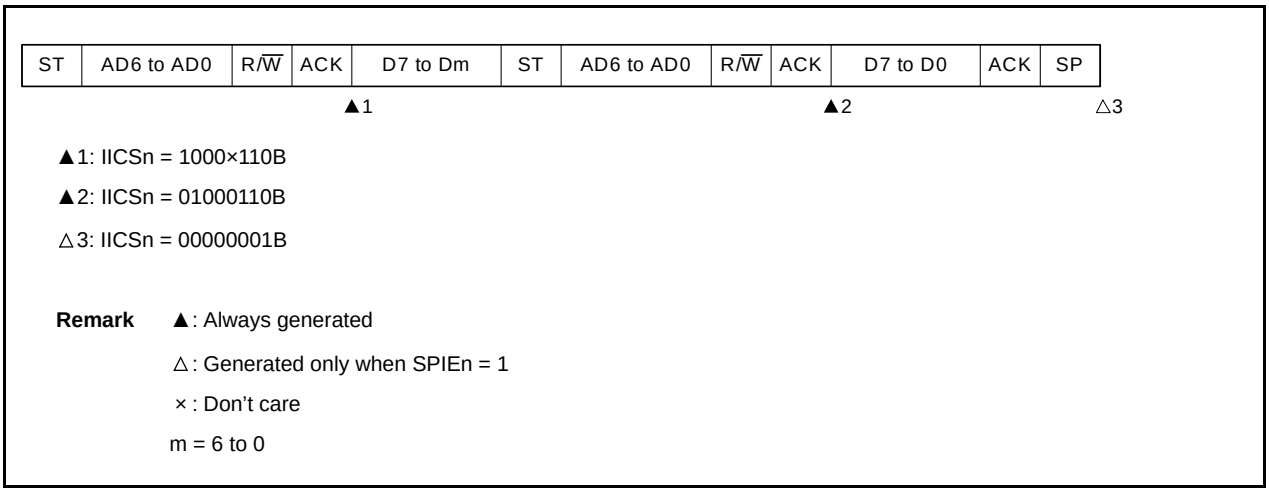
△3: IICSn = 00000001B

Remark ▲: Always generated

△: Generated only when SPIEn = 1

(d) When loss occurs due to restart condition during data transfer

(i) Not extension code (Example: unmatches with SVAn)



▲1: IICSn = 1000×110B

▲2: IICSn = 01000110B

△3: IICSn = 00000001B

Remark ▲: Always generated

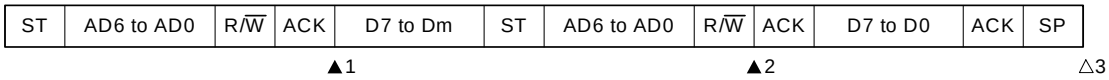
△: Generated only when SPIEn = 1

×: Don't care

m = 6 to 0

Remark n = 0

(ii) Extension code



▲1 ▲2 △3

▲1: IICSn = 1000×110B

▲2: IICSn = 01100010B

Sets LRELn = 1 by software

△3: IICSn = 00000001B

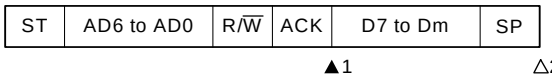
Remark ▲: Always generated

△: Generated only when SPIEn = 1

×: Don't care

m = 6 to 0

(e) When loss occurs due to stop condition during data transfer



▲1 △2

▲1: IICSn = 10000110B

△2: IICSn = 01000001B

Remark ▲: Always generated

△: Generated only when SPIEn = 1

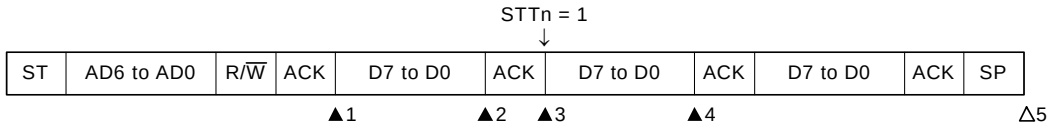
×: Don't care

m = 6 to 0

Remark n = 0

(f) When arbitration loss occurs due to low-level data when attempting to generate a restart condition

(i) When WTIMn = 0



▲1: IICSn = 1000×110B

▲2: IICSn = 1000×000B (Sets the WTIMn bit to 1)

▲3: IICSn = 1000×100B (Clears the WTIMn bit to 0)

▲4: IICSn = 01000000B

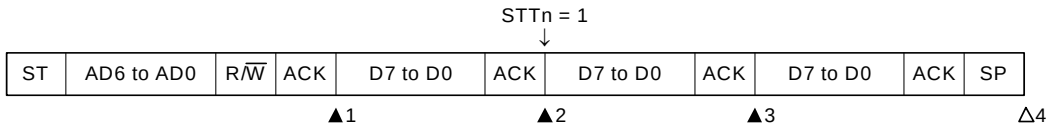
△5: IICSn = 00000001B

Remark ▲: Always generated

△: Generated only when SPIEn = 1

×: Don't care

(ii) When WTIMn = 1



▲1: IICSn = 1000×110B

▲2: IICSn = 1000×100B (Sets the STTn bit to 1)

▲3: IICSn = 01000100B

△4: IICSn = 00000001B

Remark ▲: Always generated

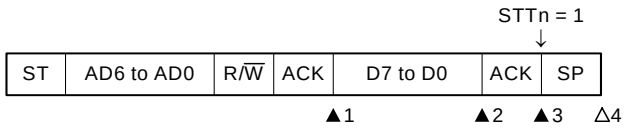
△: Generated only when SPIEn = 1

×: Don't care

Remark n = 0

(g) When arbitration loss occurs due to a stop condition when attempting to generate a restart condition

(i) When WTIMn = 0



▲1: IICSn = 1000×110B

▲2: IICSn = 1000×000B (Sets the WTIMn bit to 1)

▲3: IICSn = 1000××00B (Sets the STTn bit to 1)

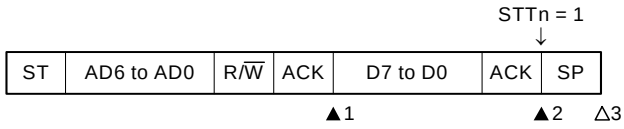
△4: IICSn = 01000001B

Remark ▲: Always generated

△: Generated only when SPIEn = 1

×: Don't care

(ii) When WTIMn = 1



▲1: IICSn = 1000×110B

▲2: IICSn = 1000××00B (Sets the STTn bit to 1)

△3: IICSn = 01000001B

Remark ▲: Always generated

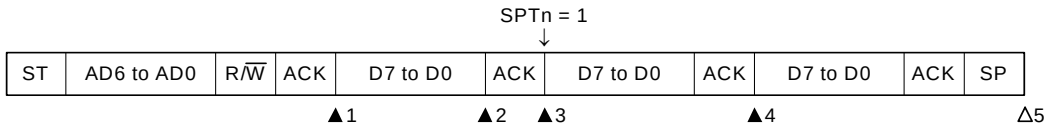
△: Generated only when SPIEn = 1

×: Don't care

Remark n = 0

(h) When arbitration loss occurs due to low-level data when attempting to generate a stop condition

(i) When WTIMn = 0



▲1: IICSn = 1000×110B

▲2: IICSn = 1000×000B (Sets the WTIMn bit to 1)

▲3: IICSn = 1000×100B (Clears the WTIMn bit to 0)

▲4: IICSn = 01000100B

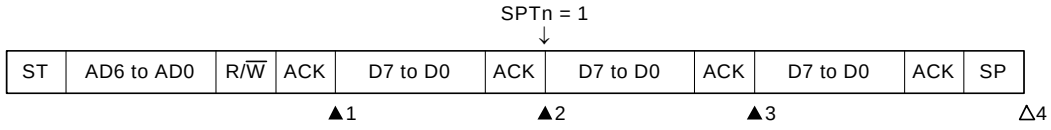
△5: IICSn = 00000001B

Remark ▲: Always generated

△: Generated only when SPIEn = 1

×: Don't care

(ii) When WTIMn = 1



▲1: IICSn = 1000×110B

▲2: IICSn = 1000×100B (Sets the SPTn bit to 1)

▲3: IICSn = 01000100B

△4: IICSn = 00000001B

Remark ▲: Always generated

△: Generated only when SPIEn = 1

×: Don't care

Remark n = 0

21.6 Timing Charts

When using the I^2C bus mode, the master device outputs an address via the serial bus to select one of several slave devices as its communication partner.

After outputting the slave address, the master device transmits the TRCn bit (bit 3 of the IICA status register n (IICSn)), which specifies the data transfer direction, and then starts serial communication with the slave device.

Figure 21 - 39 to **21 - 45** show timing charts of the data communication.

The IICA shift register n (IICAn)'s shift operation is synchronized with the falling edge of the serial clock (SCLAn). The transmit data is transferred to the SO latch and is output (MSB first) via the SDAAn pin.

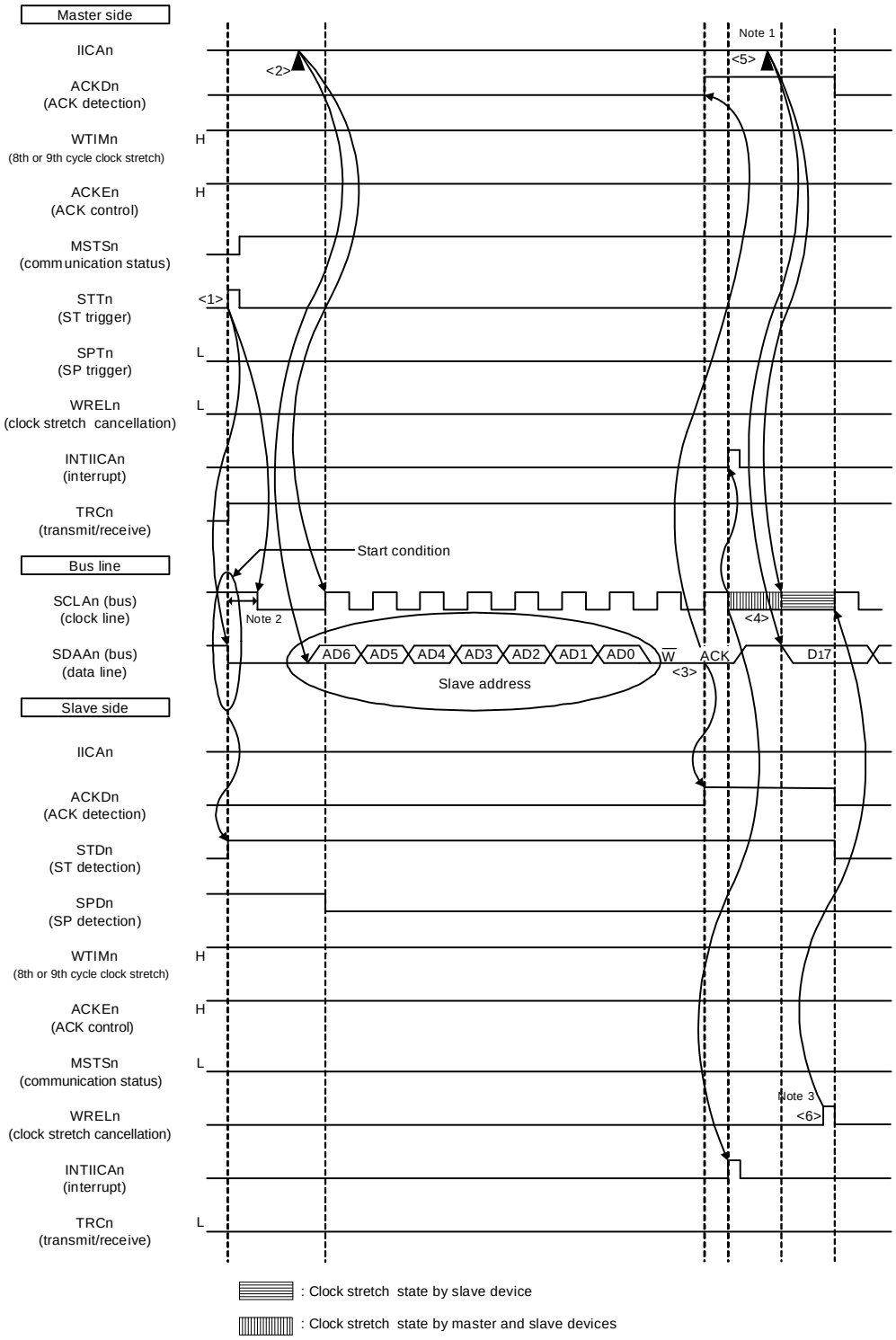
Data input via the SDAAn pin is captured into IICAn at the rising edge of SCLAn.

Remark n = 0

Figure 21 - 39 Example of Master to Slave Communication
(When 9th Cycle Clock Stretch Is Selected for Master, 9th Cycle Clock Stretch Is Selected for Slave) (1/4)

(1) Start condition ~ address ~ data

(1) Start condition ~ address ~ data



Note 1. Write data to IICAn, not setting the WRELn bit, in order to cancel a clock stretch state during transmission by a master device.

Note 2. Make sure that the time between the fall of the SDAAn pin signal and the fall of the SCLAn pin signal is at least 4.0 μs when specifying standard mode and at least 0.6 μs when specifying fast mode.

Note 3. For releasing clock stretch state during reception of a slave device, write “FFH” to IICAn or set the WRELn bit.

Remark n = 0

The meanings of <1> to <6> in (1) Start condition ~ address ~ data in **Figure 21 - 39** are explained below.

<1> The start condition trigger is set by the master device (STTn = 1) and a start condition (i.e. SCLAn = 1 changes SDAAn from 1 to 0) is generated once the bus data line goes low (SDAAn). When the start condition is subsequently detected, the master device enters the master device communication status (MSTSn = 1). The master device is ready to communicate once the bus clock line goes low (SCLAn = 0) after the hold time has elapsed.

<2> The master device writes the address + W (transmission) to the IICA shift register n (IICAn) and transmits the slave address.

<3> In the slave device if the address received matches the address (SVAn value) of a slave device Note, that slave device sends an ACK by hardware to the master device. The ACK is detected by the master device (ACKDn = 1) at the rising edge of the 9th clock.

<4> The master device issues an interrupt (INTIICAn: end of address transmission) at the falling edge of the 9th clock. The slave device whose address matched the transmitted slave address sets a clock stretch status (SCLAn = 0) and issues an interrupt (INTIICAn: address match) Note.

<5> The master device writes the data to transmit to the IICAn register and releases the clock stretch status that it set by the master device.

<6> If the slave device releases the clock stretch status (WRELn = 1), the master device starts transferring data to the slave device.

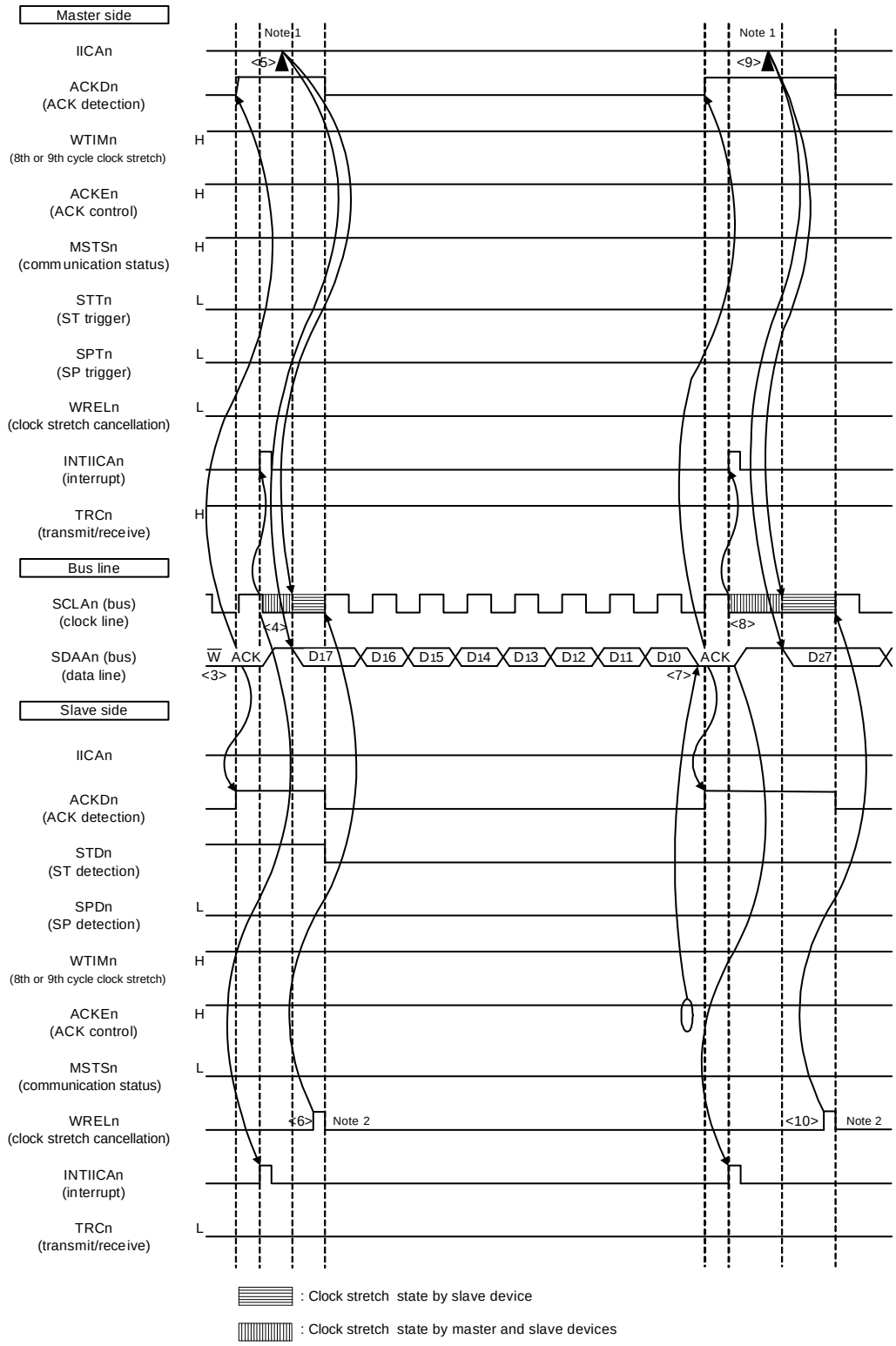
Note If the transmitted address does not match the address of the slave device, the slave device does not return an ACK to the master device (NACK: SDAAn = 1). The slave device also does not issue the INTIICAn interrupt (address match) and does not set a clock stretch status. The master device, however, issues the INTIICAn interrupt (end of address transmission) regardless of whether it receives an ACK or NACK.

Remark 1. <1> to <15> in **Figure 21 - 39** to **21 - 41** represent the entire procedure for communicating data using the I^2C bus. **Figure 21 - 39 (1) Start condition ~ address ~ data** shows the processing from <1> to <6>, **Figure 21 - 40 (2) Address ~ data ~ data** shows the processing from <3> to <10>, and **Figure 21 - 41 (3) Data ~ data ~ stop condition** shows the processing from <7> to <15>.

Remark 2. n = 0

Figure 21 - 40 Example of Master to Slave Communication
(When 9th Cycle Clock Stretch Is Selected for Master, 9th Cycle Clock Stretch Is Selected for Slave) (2/4)

(2) Address ~ data ~ data



Note 1. Write data to IICAn, not setting the WRELn bit, in order to cancel a clock stretch state during transmission by a master device.
Note 2. For releasing clock stretch state during reception of a slave device, write “FFH” to IICAn or set the WRELn bit.
Remark n = 0

The meanings of <3> to <10> in (2) Address ~ data ~ data in **Figure 21 - 40** are explained below.

<3> In the slave device if the address received matches the address (SVAn value) of a slave device Note, that slave device sends an ACK by hardware to the master device. The ACK is detected by the master device (ACKDn = 1) at the rising edge of the 9th clock.

<4> The master device issues an interrupt (INTIICAn: end of address transmission) at the falling edge of the 9th clock. The slave device whose address matched the transmitted slave address sets a clock stretch status (SCLAn = 0) and issues an interrupt (INTIICAn: address match) Note.

<5> The master device writes the data to transmit to the IICA shift register n (IICAn) and releases the clock stretch status that it set by the master device.

<6> If the slave device releases the clock stretch status (WRELn = 1), the master device starts transferring data to the slave device.

<7> After data transfer is completed, because of ACKEn = 1, the slave device sends an ACK by hardware to the master device. The ACK is detected by the master device (ACKDn = 1) at the rising edge of the 9th clock.

<8> The master device and slave device set a clock stretch status (SCLAn = 0) at the falling edge of the 9th clock, and both the master device and slave device issue an interrupt (INTIICAn: end of transfer).

<9> The master device writes the data to transmit to the IICAn register and releases the clock stretch status that it set by the master device.

<10>The slave device reads the received data and releases the clock stretch status (WRELn = 1). The master device then starts transferring data to the slave device.

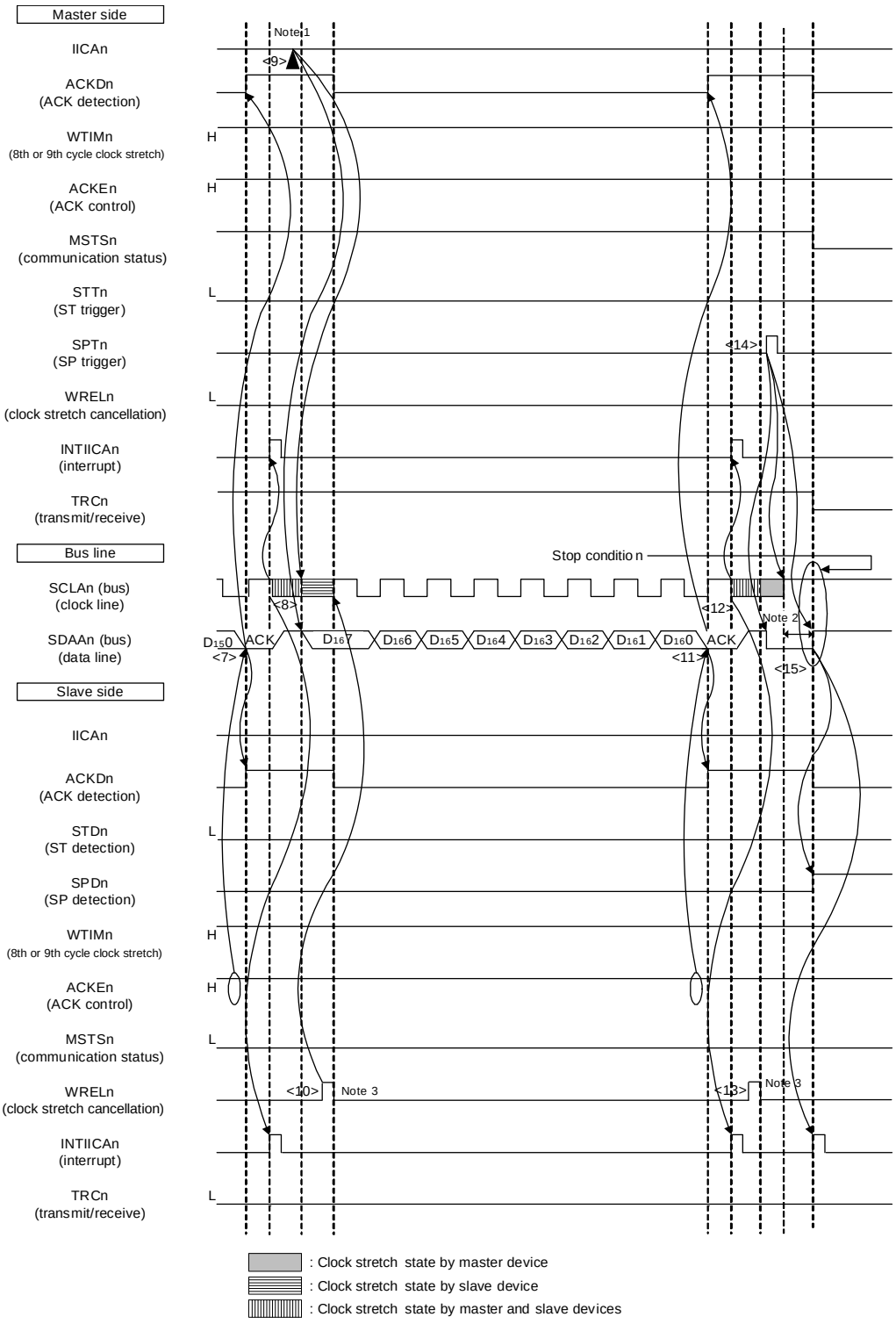
Note If the transmitted address does not match the address of the slave device, the slave device does not return an ACK to the master device (NACK: SDAAn = 1). The slave device also does not issue the INTIICAn interrupt (address match) and does not set a clock stretch status. The master device, however, issues the INTIICAn interrupt (end of address transmission) regardless of whether it receives an ACK or NACK.

Remark 1. <1> to <15> in **Figure 21 - 39** to **21 - 41** represent the entire procedure for communicating data using the I^2C bus. **Figure 21 - 39 (1) Start condition ~ address ~ data** shows the processing from <1> to <6>, **Figure 21 - 40 (2) Address ~ data ~ data** shows the processing from <3> to <10>, and **Figure 21 - 41 (3) Data ~ data ~ stop condition** shows the processing from <7> to <15>.

Remark 2. n = 0

Figure 21 - 41 Example of Master to Slave Communication
(When 9th Cycle Clock Stretch Is Selected for Master, 9th Cycle Clock Stretch Is Selected for Slave) (3/4)

(3) Data ~ data ~ stop condition



Note 1. Write data to IICAn, not setting the WRELn bit, in order to cancel a clock stretch state during transmission by a master device.

Note 2. Make sure that the time between the rise of the SCLAn pin signal and the generation of the stop condition after a stop condition has been issued is at least 4.0 µs when specifying standard mode and at least 0.6 µs when specifying fast mode.

Note 3. For releasing clock stretch state during reception of a slave device, write “FFH” to IICAn or set the WRELn bit.

Remark n = 0

The meanings of <7> to <15> in **(3) Data ~ data ~ stop condition** in **Figure 21 - 41** are explained below.

<7> After data transfer is completed, because of ACKEn = 1, the slave device sends an ACK by hardware to the master device. The ACK is detected by the master device (ACKDn = 1) at the rising edge of the 9th clock.

<8> The master device and slave device set a clock stretch status (SCLAn = 0) at the falling edge of the 9th clock, and both the master device and slave device issue an interrupt (INTIICAn: end of transfer).

<9> The master device writes the data to transmit to the IICA shift register n (IICAn) and releases the clock stretch status that it set by the master device.

<10>The slave device reads the received data and releases the clock stretch status (WRELn = 1). The master device then starts transferring data to the slave device.

<11>When data transfer is complete, the slave device (ACKEn =1) sends an ACK by hardware to the master device. The ACK is detected by the master device (ACKDn = 1) at the rising edge of the 9th clock.

<12>The master device and slave device set a clock stretch status (SCLAn = 0) at the falling edge of the 9th clock, and both the master device and slave device issue an interrupt (INTIICAn: end of transfer).

<13>The slave device reads the received data and releases the clock stretch status (WRELn = 1).

<14> By the master device setting a stop condition trigger (SPTn = 1), the bus data line is cleared (SDAAn = 0) and the bus clock line is set (SCLAn = 1). After the stop condition setup time has elapsed, by setting the bus data line (SDAAn = 1), the stop condition is then generated (i.e. SCLAn =1 changes SDAAn from 0 to 1).

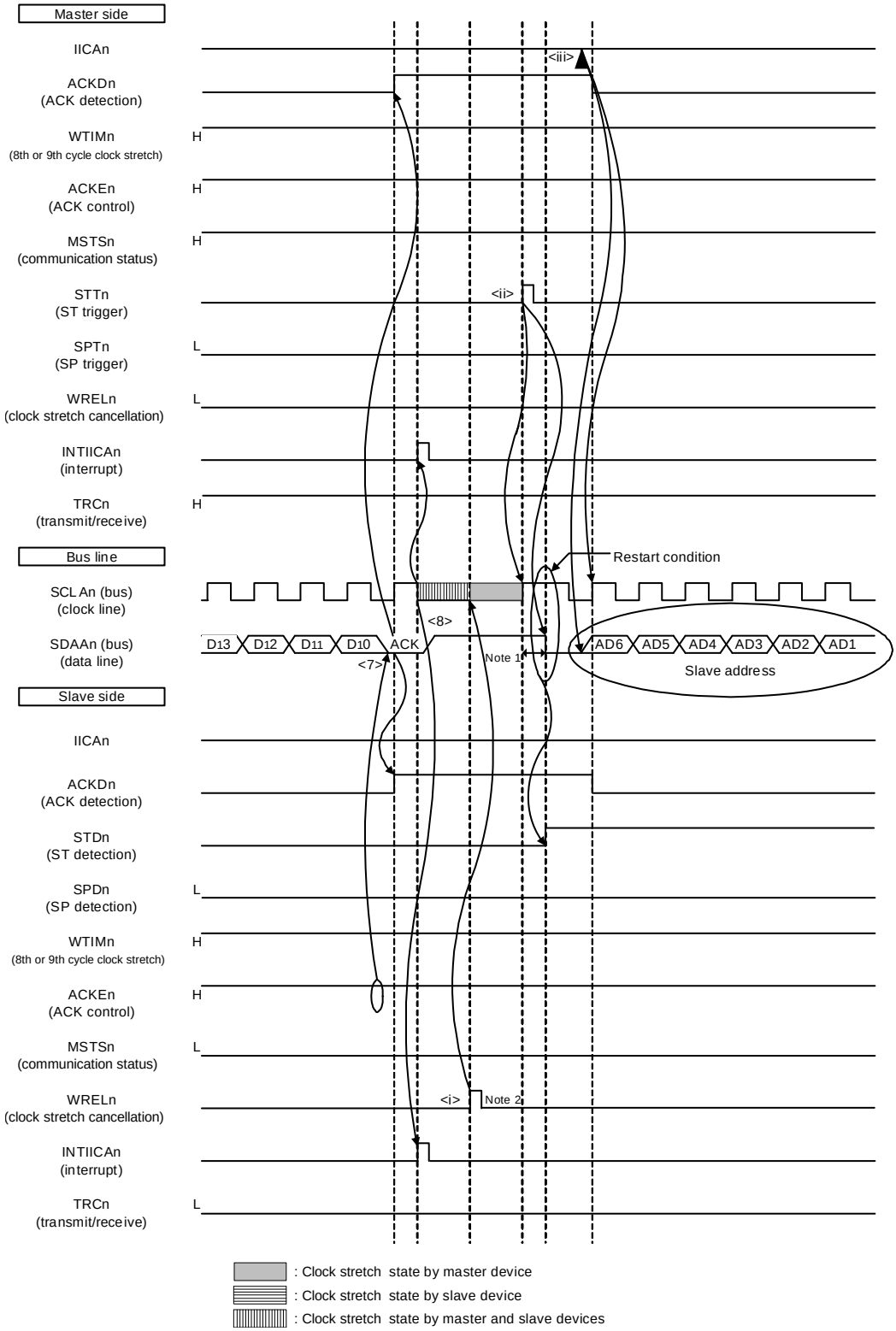
<15> When a stop condition is generated, the slave device detects the stop condition and issues an interrupt (INTIICAn: stop condition).

Remark 1. <1> to <15> in **Figure 21 - 39** to **21 - 41** represent the entire procedure for communicating data using the I^2C bus. **Figure 21 - 39 (1) Start condition ~ address ~ data** shows the processing from <1> to <6>, **Figure 21 - 40 (2) Address ~ data ~ data** shows the processing from <3> to <10>, and **Figure 21 - 41 (3) Data ~ data ~ stop condition** shows the processing from <7> to <15>.

Remark 2. n = 0

Figure 21 - 42 Example of Master to Slave Communication
(When 9th Cycle Clock Stretch Is Selected for Master, 9th Cycle Clock Stretch Is Selected for Slave) (4/4)

(4) Data ~ restart condition ~ address



Note 1. Make sure that the time between the rise of the SCLAn pin signal and the generation of the start condition after a restart condition has been issued is at least 4.7 µs when specifying standard mode and at least 0.6 µs when specifying fast mode.

Note 2. For releasing clock stretch state during reception of a slave device, write “FFH” to IICAn or set the WRELn bit.

Remark n = 0

The following describes the operations in **Figure 21 - 42 (4) Data ~ restart condition ~ address**. After the operations in steps <7> and <8>, the operations in steps <i> to <iii> are performed. These steps return the processing to step <iii>, the data transmission step.

<7> After data transfer is completed, because of ACKEn = 1, the slave device sends an ACK by hardware to the master device. The ACK is detected by the master device (ACKDn = 1) at the rising edge of the 9th clock.

<8> The master device and slave device set a clock stretch status (SCLAn = 0) at the falling edge of the 9th clock, and both the master device and slave device issue an interrupt (INTIICAn: end of transfer).

<i> The slave device reads the received data and releases the clock stretch status (WRELn = 1).

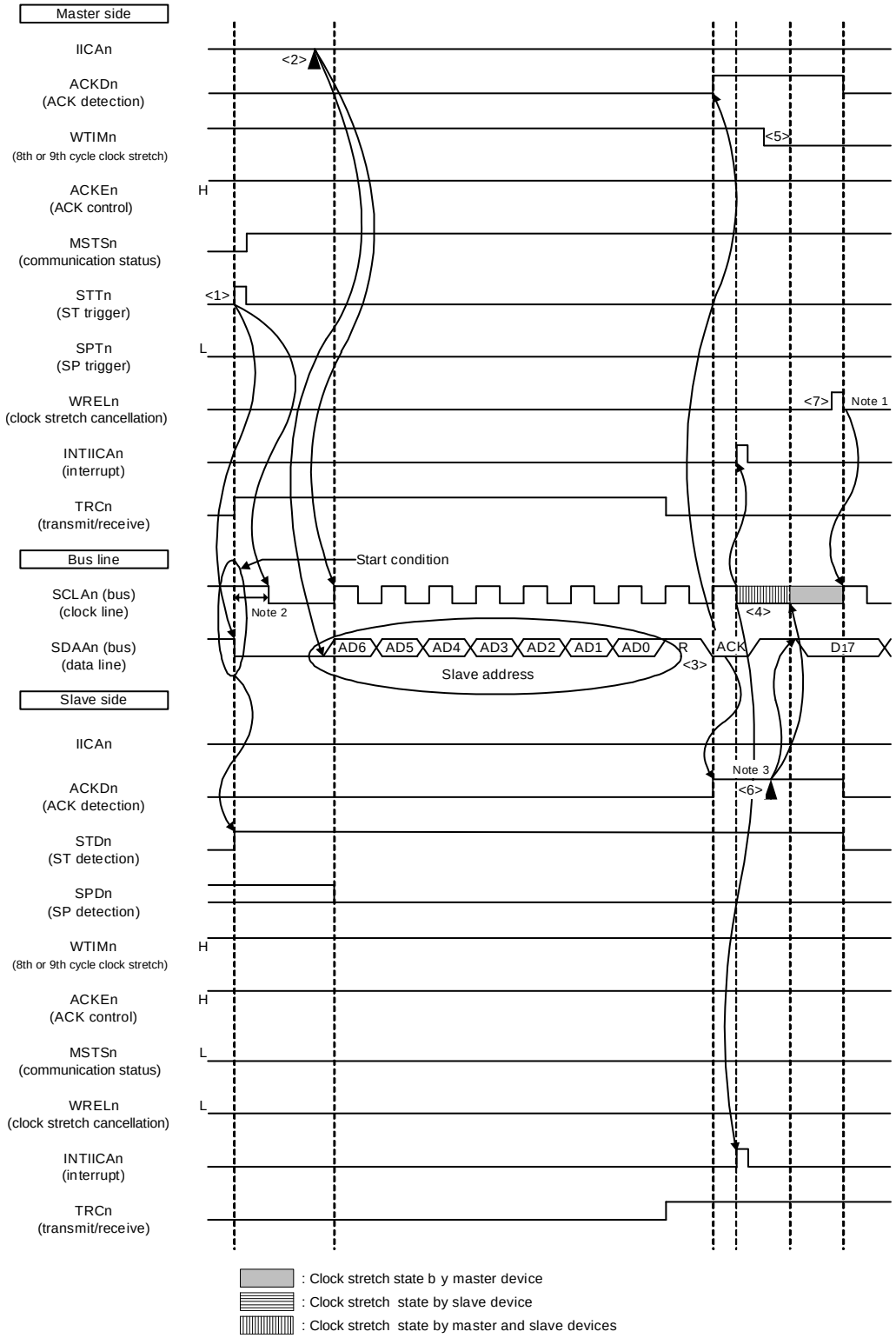
<ii> The start condition trigger is set again by the master device (STTn = 1) and a start condition (i.e. SCLAn =1 changes SDAAn from 1 to 0) is generated once the bus clock line goes high (SCLAn = 1) and the bus data line goes low (SDAAn = 0) after the restart condition setup time has elapsed. When the start condition is subsequently detected, the master device is ready to communicate once the bus clock line goes low (SCLAn = 0) after the hold time has elapsed.

<iii> The master device writing the address + R/W (transmission) to the IICA shift register (IICAn) enables the slave address to be transmitted.

Remark n = 0

Figure 21 - 43 Example of Slave to Master Communication
(When 8th Cycle Clock Stretch Is Selected for Master, 9th Cycle Clock Stretch Is Selected for Slave) (1/3)

(1) Start condition ~ address ~ data



Note 1. For releasing clock stretch state during reception of a master device, write “FFH” to IICAn or set the WRELn bit.
Note 2. Make sure that the time between the fall of the SDAAn pin signal and the fall of the SCLAn pin signal is at least 4.0 μs when specifying standard mode and at least 0.6 μs when specifying fast mode.
Note 3. Write data to IICAn, not setting the WRELn bit, in order to cancel a clock stretch state during transmission by a slave device.
Remark n = 0

The meanings of <1> to <7> in **(1) Start condition ~ address ~ data** in **Figure 21 - 43** are explained below.

<1> The start condition trigger is set by the master device (STTn = 1) and a start condition (i.e. SCLAn =1 changes SDAAn from 1 to 0) is generated once the bus data line goes low (SDAAn). When the start condition is subsequently detected, the master device enters the master device communication status (MSTSn = 1). The master device is ready to communicate once the bus clock line goes low (SCLAn = 0) after the hold time has elapsed.

<2> The master device writes the address + R (reception) to the IICA shift register n (IICAn) and transmits the slave address.

<3> In the slave device if the address received matches the address (SVAn value) of a slave device Note, that slave device sends an ACK by hardware to the master device. The ACK is detected by the master device (ACKDn = 1) at the rising edge of the 9th clock.

<4> The master device issues an interrupt (INTIICAn: end of address transmission) at the falling edge of the 9th clock. The slave device whose address matched the transmitted slave address sets a clock stretch status (SCLAn = 0) and issues an interrupt (INTIICAn: address match) Note.

<5> The timing at which the master device sets the clock stretch status changes to the 8th clock (WTIMn = 0).

<6> The slave device writes the data to transmit to the IICAn register and releases the clock stretch status that it set by the slave device.

<7> The master device releases the clock stretch status (WRELn = 1) and starts transferring data from the slave device to the master device.

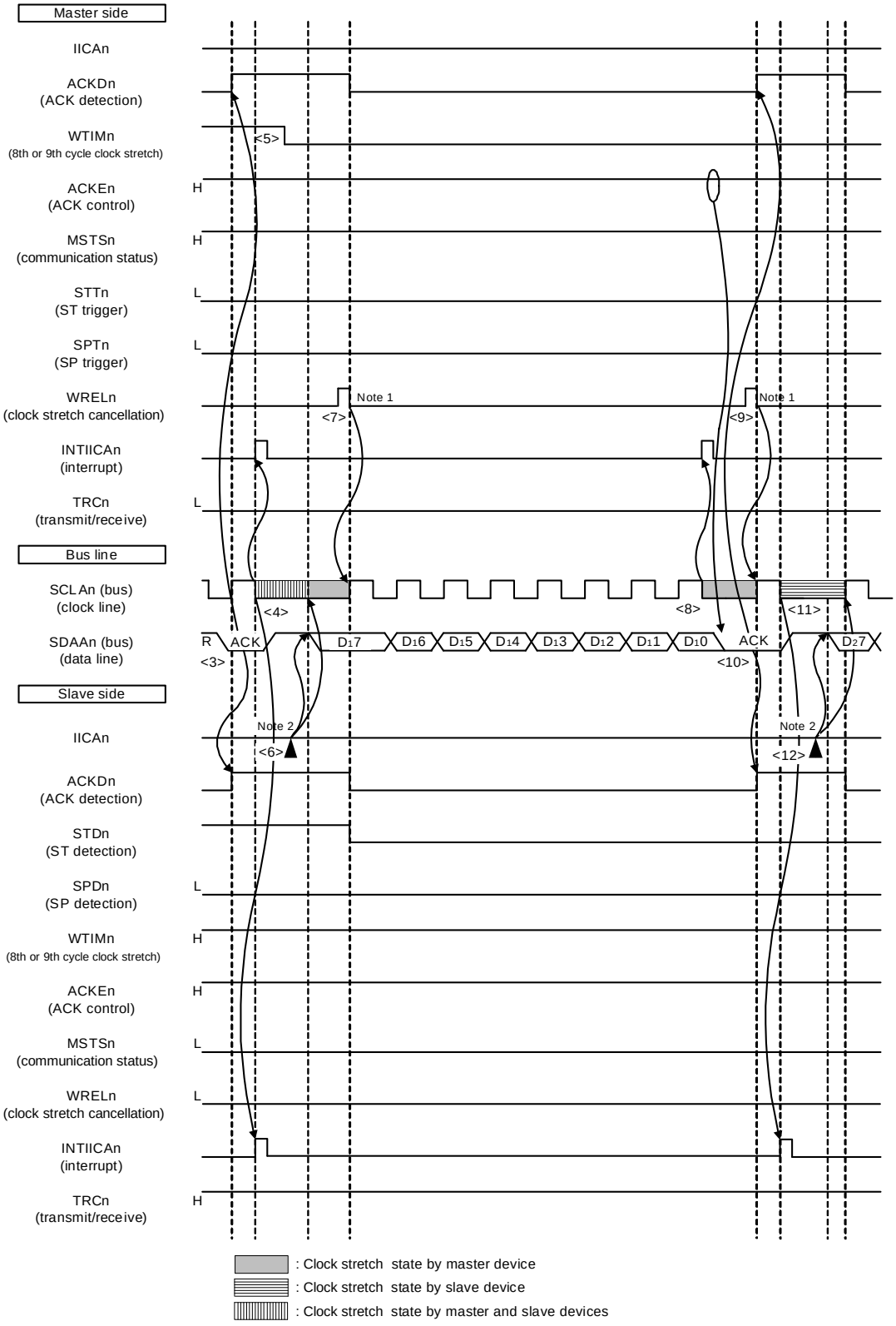
Note If the transmitted address does not match the address of the slave device, the slave device does not return an ACK to the master device (NACK: SDAAn = 1). The slave device also does not issue the INTIICAn interrupt (address match) and does not set a clock stretch status. The master device, however, issues the INTIICAn interrupt (end of address transmission) regardless of whether it receives an ACK or NACK.

Remark 1. <1> to <19> in **Figure 21 - 43** to **21 - 45** represent the entire procedure for communicating data using the I^2C bus. **Figure 21 - 43 (1) Start condition ~ address ~ data** shows the processing from <1> to <7>, **Figure 21 - 44 (2) Address ~ data ~ data** shows the processing from <3> to <12>, and **Figure 21 - 45 (3) Data ~ data ~ stop condition** shows the processing from <8> to <19>.

Remark 2. n = 0

Figure 21 - 44 Example of Slave to Master Communication
(When 8th Cycle Clock Stretch Is Selected for Master, 9th Cycle Clock Stretch Is Selected for Slave) (2/3)

(2) Address ~ data ~ data



Note 1. For releasing clock stretch state during reception of a master device, write “FFH” to IICAn or set the WRELn bit.
Note 2. Write data to IICAn, not setting the WRELn bit, in order to cancel a clock stretch state during transmission by a slave device.
Remark n = 0

The meanings of <3> to <12> in **(2) Address ~ data ~ data** in **Figure 21 - 44** are explained below.

<3> In the slave device if the address received matches the address (SVAn value) of a slave device Note, that slave device sends an ACK by hardware to the master device. The ACK is detected by the master device (ACKDn = 1) at the rising edge of the 9th clock.

<4> The master device issues an interrupt (INTIICAn: end of address transmission) at the falling edge of the 9th clock. The slave device whose address matched the transmitted slave address sets a clock stretch status (SCLAn = 0) and issues an interrupt (INTIICAn: address match) Note.

<5> The master device changes the timing of the clock stretch status to the 8th clock (WTIMn = 0).

<6> The slave device writes the data to transmit to the IICA shift register n (IICAn) and releases the clock stretch status that it set by the slave device.

<7> The master device releases the clock stretch status (WRELn = 1) and starts transferring data from the slave device to the master device.

<8> The master device sets a clock stretch status (SCLAn = 0) at the falling edge of the 8th clock, and issues an interrupt (INTIICAn: end of transfer). Because of ACKEn = 1 in the master device, the master device then sends an ACK by hardware to the slave device.

<9> The master device reads the received data and releases the clock stretch status (WRELn = 1).

<10>The ACK is detected by the slave device (ACKDn = 1) at the rising edge of the 9th clock.

<11>The slave device set a clock stretch status (SCLAn = 0) at the falling edge of the 9th clock, and the slave device issue an interrupt (INTIICAn: end of transfer).

<12>By the slave device writing the data to transmit to the IICAn register, the clock stretch status set by the slave device is released. The slave device then starts transferring data to the master device.

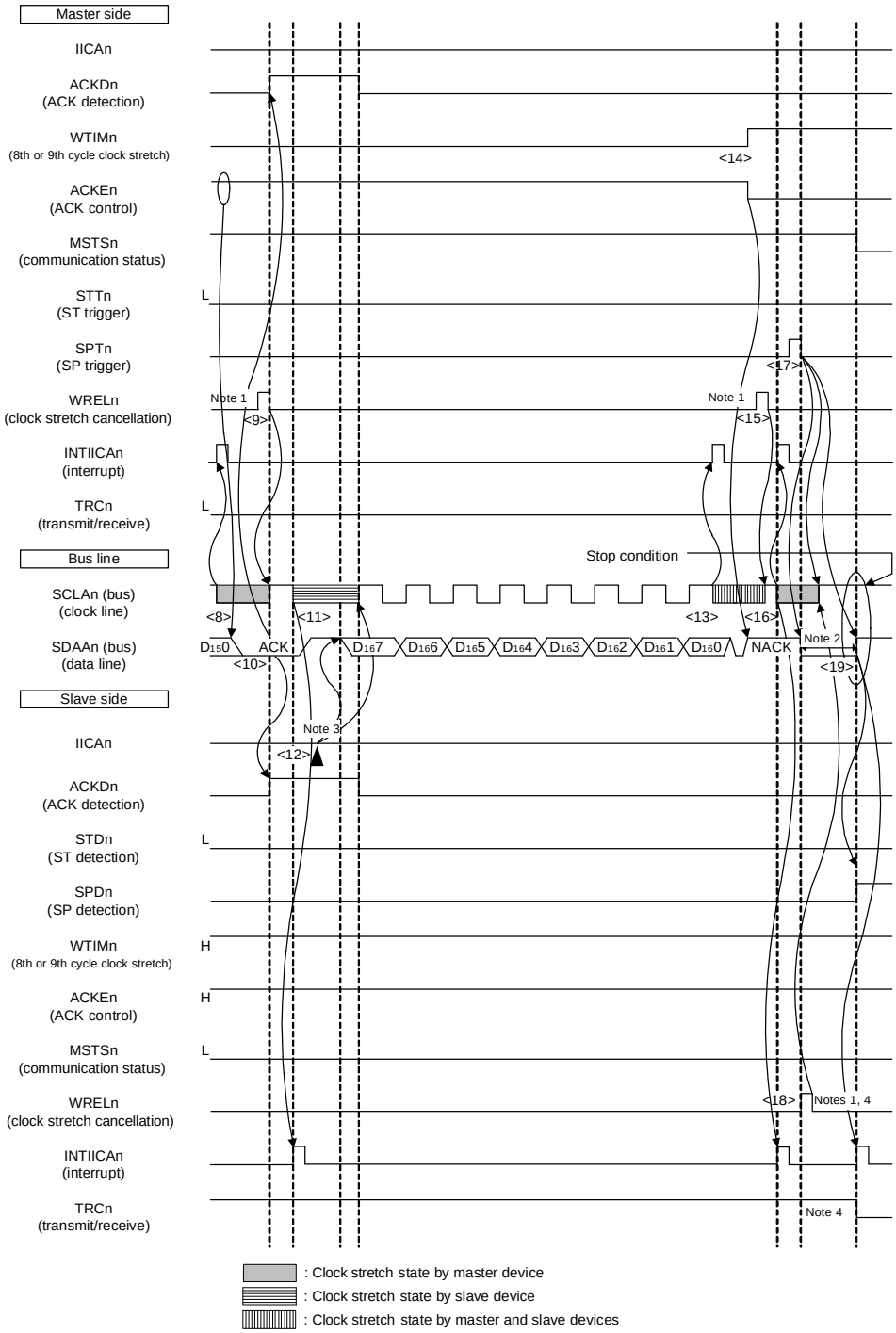
Note If the transmitted address does not match the address of the slave device, the slave device does not return an ACK to the master device (NACK: SDAAn = 1). The slave device also does not issue the INTIICAn interrupt (address match) and does not set a clock stretch status. The master device, however, issues the INTIICAn interrupt (end of address transmission) regardless of whether it receives an ACK or NACK.

Remark 1. <1> to <19> in **Figure 21 - 43** to **21 - 45** represent the entire procedure for communicating data using the I^2C bus. **Figure 21 - 43 (1) Start condition ~ address ~ data** shows the processing from <1> to <7>, **Figure 21 - 44 (2) Address ~ data ~ data** shows the processing from <3> to <12>, and **Figure 21 - 45 (3) Data ~ data ~ stop condition** shows the processing from <8> to <19>.

Remark 2. n = 0

Figure 21 - 45 Example of Slave to Master Communication
(8th Cycle Clock Stretch is Changed to 9th Cycle Clock Stretch for Master, 9th Cycle Clock Stretch is Selected for Slave)

(3) Data ~ data ~ stop condition



Note 1. To cancel a clock stretch state, write “FFH” to IICAn or set the WRELn bit.

Note 2. Make sure that the time between the rise of the SCLAn pin signal and the generation of the stop condition after a stop condition has been issued is at least 4.0 μs when specifying standard mode and at least 0.6 μs when specifying fast mode.

Note 3. Write data to IICAn, not setting the WRELn bit, in order to cancel a clock stretch state during transmission by a slave device.

Note 4. If a clock stretch state during transmission by a slave device is canceled by setting the WRELn bit, the TRCn bit will be cleared.

Remark n = 0

The meanings of <8> to <19> in **(3) Data ~ data ~ stop condition** in **Figure 21 - 45** are explained below.

<8> The master device sets a clock stretch status (SCLAn = 0) at the falling edge of the 8th clock, and issues an interrupt (INTIICAn: end of transfer). Because of ACKEn = 0 in the master device, the master device then sends an ACK by hardware to the slave device.

<9> The master device reads the received data and releases the clock stretch status (WRELn = 1).

<10>The ACK is detected by the slave device (ACKDn = 1) at the rising edge of the 9th clock.

<11>The slave device set a clock stretch status (SCLAn = 0) at the falling edge of the 9th clock, and the slave device issue an interrupt (INTIICAn: end of transfer).

<12>By the slave device writing the data to transmit to the IICA register, the clock stretch status set by the slave device is released. The slave device then starts transferring data to the master device.

<13>The master device issues an interrupt (INTIICAn: end of transfer) at the falling edge of the 8th clock, and sets a clock stretch status (SCLAn = 0). Because ACK control (ACKEn = 1) is performed, the bus data line is at the low level (SDAAn = 0) at this stage.

<14>The master device sets NACK as the response (ACKEn = 0) and changes the timing at which it sets the clock stretch status to the 9th clock (WTIMn = 1).

<15>If the master device releases the clock stretch status (WRELn = 1), the slave device detects the NACK (ACKDn = 0) at the rising edge of the 9th clock.

<16>The master device and slave device set a clock stretch status (SCLAn = 0) at the falling edge of the 9th clock, and both the master device and slave device issue an interrupt (INTIICAn: end of transfer).

<17> When the master device issues a stop condition (SPTn = 1), the bus data line is cleared (SDAAn = 0) and the master device releases the clock stretch status. The master device then clock stretch until the bus clock line is set (SCLAn = 1).

<18> The slave device acknowledges the NACK, halts transmission, and releases the clock stretch status (WRELn = 1) to end communication. Once the slave device releases the clock stretch status, the bus clock line is set (SCLAn = 1).

<19> Once the master device recognizes that the bus clock line is set (SCLAn = 1) and after the stop condition setup time has elapsed, the master device sets the bus data line (SDAAn = 1) and issues a stop condition (i.e. SCLAn =1 changes SDAAn from 0 to 1). The slave device detects the generated stop condition and slave device issue an interrupt (INTIICAn: stop condition).

Remark 1. <1> to <19> in **Figure 21 - 43** to **21 - 45** represent the entire procedure for communicating data using the I^2C bus. **Figure 21 - 43 (1) Start condition ~ address ~ data** shows the processing from <1> to <7>, **Figure 21 - 44 (2) Address ~ data ~ data** shows the processing from <3> to <12>, and **Figure 21 - 45 (3) Data ~ data ~ stop condition** shows the processing from <8> to <19>.

Remark 2. n = 0

CHAPTER 22 SERIAL INTERFACE UARTMG (R5F11R Only)

22.1 Overview

The serial interface (UARTMGn, n=0) supports the following two modes.

(1) Operation stop mode
This mode is used when serial communication is not executed; power consumption can be reduced.
(2) UART mode
This is a UART mode that supports continuous transmission.

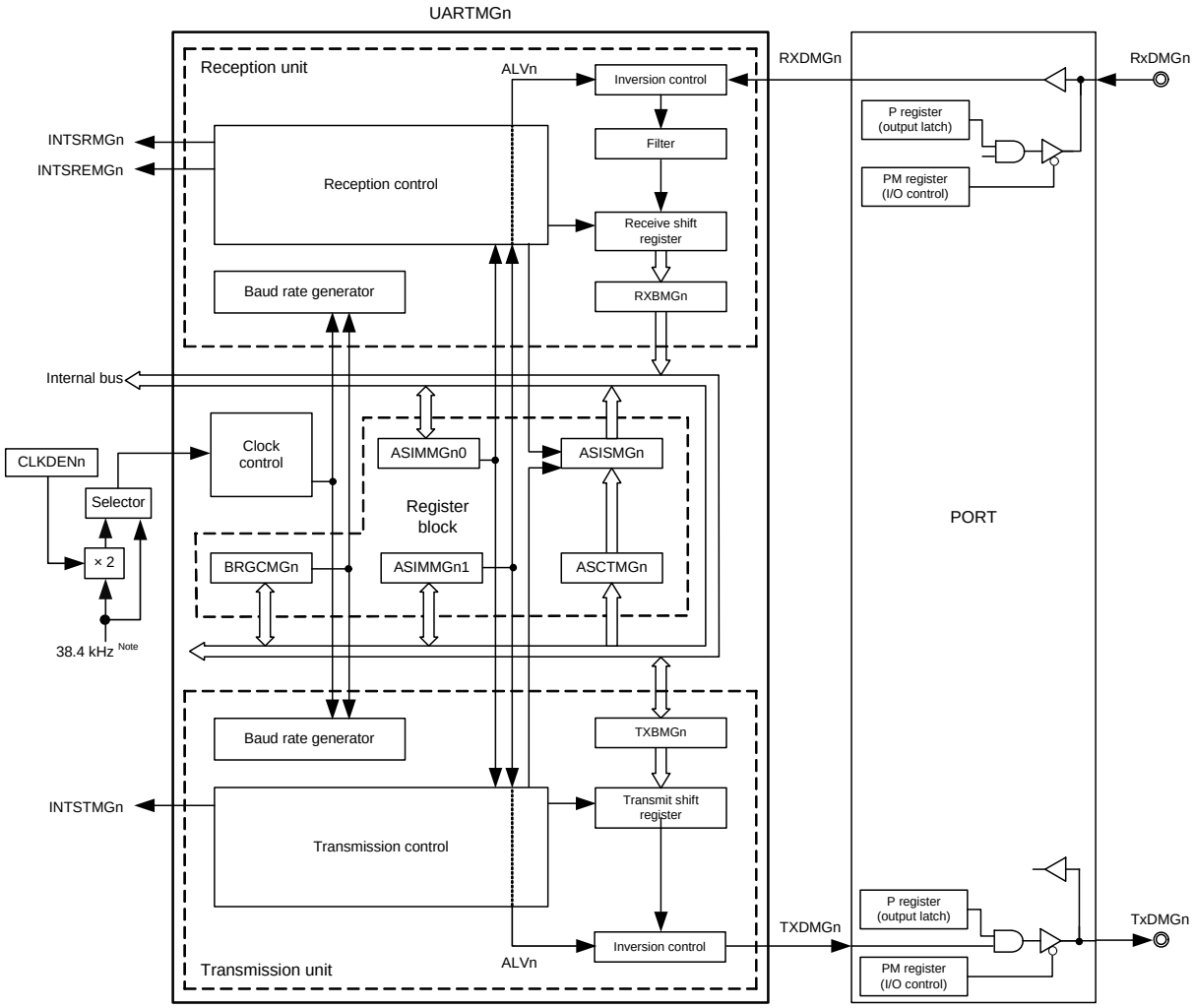
UARTMGn performs an asynchronous communication. It has the following functions.

- Maximum transfer rate: 9600 bps (19200 bps with a clock doubler used)
- Transmission and reception using two pins
  TxDMGn:Transmit data output pin
  RxDMGn:Receive data input pin
- Character length of transfer data selectable from 5, 7, and 8 bits
- Baud rate arbitrarily settable with the dedicated internal 8-bit baud rate generator
- Transmission and reception independent of each other (full-duplex communication)
- MSB or LSB first transfer selectable
- Inversion control of communication logic level provided

Remark n: unit number (n = 0)

Figure 22 - 1 shows a block diagram of UARTMGn and **Table 22 - 1** shows the pin configuration of UARTMGn.

Figure 22 - 1 Block Diagram of UARTMGn



Note Be sure to select the subsystem clock (WUTMMCK0 bit = 0).

Table 22 - 1 UARTMGn Pin Configuration (n = 0)

Pin Name	I/O	Function
RxDMGn	Input	Serial data input signal
TxDMGn	Output	Serial data output signal

22.2 Register Descriptions

Table 22 - 2 shows the registers used in UARTMGn.

Table 22 - 2 UARTMGn Registers

Register Name	Symbol	Value after Reset	Address	Access Size
Peripheral enable register 2	PER2	00H	F00FDH	8
Clock doubler control register	CLKDCTL	00H	F02CCH	8
Transmit buffer register 0	TXBMG0	FFH	F0280H	8
Receive buffer register 0	RXBMG0	FFH	F0281H	8
Operation mode setting register 00	ASIMMG00	01H	F0282H	8
Operation mode setting register 01	ASIMMG01	1AH	F0283H	8
Baud rate generator control register 0	BRGCMG0	FFH	F0284H	8
Status register 0	ASISMG0	00H	F0285H	8
Status clear trigger register 0	ASCTMG0	00H	F0286H	8

Remark UARTMGn uses the following registers, in addition to those listed above.
Port mode register (PM1) (See **CHAPTER 4 PORT FUNCTIONS**.)
Port register (P1) (See **CHAPTER 4 PORT FUNCTIONS**.)

22.2.1 Peripheral enable register 2 (PER2)

The PER2 register is used to enable or disable supplying the clock to the peripheral hardware. Clock supply to the hardware that is not used is also stopped so as to decrease the power consumption and noise.

When using UARTMG0, be sure to set bit 4 (UARTMG0EN) to 1.

The PER2 register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 22 - 2 Format of Peripheral Enable Register 2 (PER2)

Address: F00FDH After reset: 00H R/W

Symbol	7	6	5	<4>	<3>	<2>	<1>	<0>
PER2	0	0	0	UARTMG0EN	SMOTDEN	EXSDEN	TRJ1EN	TRJ0EN

UARTMGn EN	Control of input clock supply to serial interface UARTMGn (n = 0)
0	Stops supply of input clock. • SFR used by the serial interface UARTMGn cannot be written. • Operation of the serial interface UARTMGn is disabled.
1	Supplies input clock. • SFR used by the serial interface UARTMGn can be read and written. • Operation of the serial interface UARTMGn is enabled.

Caution 1. When setting UARTMG0, be sure to set the UARTMG0EN bit to 1 first. If UARTMG0EN = 0, writing to a control register of UARTMG0 is ignored, and all read values are default values (except for the port mode register 1 (PM1) and port register 1 (P1)).

Caution 2. Be sure to clear bits 5 through 7 to 0.

22.2.2 Clock Doubler Control Register (CLKDCTL)

The CLKDCTL register sets the the operating clock of the serial interface UARTMGn.

The CLKDCTL register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 22 - 3 Format of Clock Doubler Control Register (CLKDCTL)

Address: F02CCH After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	<0>
CLKDCTL	0	0	0	0	0	0	0	CLKDEN0

CLKDENn	Selection of operating clock for serial interface UARTMGn
0	f_{SUB}
1	$f_{SUB} \times 2$

Caution 1. The clock doubler starts operation when CLKDENn (n = 0) is set to 1.

Caution 2. Setting the CLKDENn bit during the UARTMGn operation is prohibited. Be sure to set the bit to 1 before UARTMGn starts communication.

22.2.3 Transmit Buffer Register (TXBMGn) (n = 0)

The TXBMGn register can be read and written by an 8-bit memory manipulation instruction.

Reset signal generation sets this register to FFH.

Figure 22 - 4 Format of Transmit Buffer Register (TXBMGn)

Address: F0280H (TXBMG0) After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
TXBMGn	—	—	—	—	—	—	—	—

Bits 7 to 0	Function
—	A buffer register for setting transmit data. Transmission starts by writing data for transmission to the TXBMGn register. When a character length of 8 bits is specified: • Data in bits 7 to 0 of TXBMGn are transferred. When a character length of 7 bits is specified: • Data in bits 6 to 0 of TXBMGn are transferred in either MSB- or LSB-first mode; bit 7 is invalid. When a character length of 5 bits is specified: • Data in bits 4 to 0 of TXBMGn are transferred in either MSB- or LSB-first mode; bits 7 to 5 are invalid.

Caution 1. When the TXBFMGn bit of the ASISMGn register is 1, writing to the TXBMGn register is prohibited.

Caution 2. After setting TXEMGn = 1, wait for at least one cycle of the base clock (f_{SUB}) before setting the first data for transmission in the TXBMGn register. Although the data for transmission can be set normally even when the first data for transmission is set in the TXBMGn register before one cycle of the base clock has elapsed, this delays the start of transmission.

Remark Transmit shift register:
Data is transferred from the TXBMGn register to this register, and is then transmitted as serial data through the TXDMGn pin. In the first transmission, data is transferred from the TXBMGn register to this register immediately after data is written to the TXBMGn register. In continuous transmission, data is transferred after transmission of one frame and just before generation of the transmission completion interrupt.
The transmit shift register cannot be manipulated directly by a program.

22.2.4 Receive Buffer Register (RXBMGn) (n = 0)

The RXBMGn register can be read by an 8-bit memory manipulation instruction. Writing to this register is disabled.

Reset signal generation sets this register to FFH.

Figure 22 - 5 Format of Receive Buffer Register (RXBMGn)

Address: F0281H (RXBMG0) After reset: FFH R

Symbol	7	6	5	4	3	2	1	0
RXBMGn	—	—	—	—	—	—	—	—

Bits 7 to 0	Function
—	This register stores the parallel data converted by the receive shift register. Every time one byte of data is received, the next receive data is transferred from the receive shift register[Note] to this register. When a character length of 8 bits is specified: • Receive data is transferred to bits 7 to 0 of this register. When a character length of 7 bits is specified: • Receive data is transferred to bits 6 to 0 of this register in either MSB- or LSB-first mode; bit 7 is always 0. When a character length of 5 bits is specified: • Receive data is transferred to bits 4 to 0 of this register in either MSB- or LSB-first mode; bits 7 to 5 are always 0.

Note The receive shift register converts the serial data that is input through the RXDMGn pin to parallel data. The receive shift register cannot be manipulated directly by a program.

Caution If an overrun error (OVEMGn) occurs, the data received at that time are not stored in the RXBMGn register.

22.2.5 Operation Mode Setting Register 0 (ASIMMGn0) (n = 0)

The ASIMMGn0 register is an 8-bit register that controls serial communication of the serial interface UARTMGn.

The ASIMMGn0 register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets this register to 01H.

Figure 22 - 6 Format of Operation Mode Setting Register 0 (ASIMMGn0)

Address: F0282H (ASIMMG00) After reset: 01H R/W

Symbol	<7>	<6>	<5>	4	3	2	<1>	<0>
ASIMMGn0	POWERMGn	TXEMGn	RXEMGn	—	—	—	ISSMMGn	ISRMMGn

POWERMGn Note 1	UART operation enable
0	Disables the UART operation clock (fixed to low level). Asynchronously resets the internal circuits. Note 2
1	Enables the UART operation clock.

TXEMGn	Transmission enable
0	Disables transmission. (Synchronously resets the transmission circuit.)
1	Enables transmission.

RXEMGn	Reception enable
0	Disables reception. (Synchronously resets the reception circuit.)
1	Enables reception.

ISSMMGn	Transmit interrupt mode select
0	The INTSTMGn interrupt is generated on completion of transmission.
1	The INTSTMGn interrupt is generated when the transmit buffer becomes empty. (for continuous transmission)

ISRMMGn	Receive interrupt mode select
0	The INTSREMGn interrupt is generated when a reception error occurs. (INTSRMGn is not generated.)
1	The INTSRMGn interrupt is generated when a reception error occurs. (INTSREMGn is not generated.)

(**Notes** and **Cautions** are listed on the next page.)

Note 1. When POWERMGn = 0, the level being output from the TXDMGn pin and the level being input from the RXDMGn pin are determined according to the setting of the ALVn bit as described below.
When ALVn = 0, output from the TXDMGn pin is high, and input from the RXDMGn pin is fixed to the high level.
When ALVn = 1, output from the TXDMGn pin is low, and input from the RXDMGn pin is fixed to the low level.

Note 2. The ASISMGn and RXBMGn registers are reset by clearing the POWERMGn bit to 0.

Caution 1. To start transmission, set the POWERMGn bit to 1 and then set the TXEMGn bit to 1. To stop transmission, clear the TXEMGn bit to 0 and then clear the POWERMGn bit to 0.

Caution 2. To start reception, set the POWERMGn bit to 1 and then set the RXEMGn bit to 1. To stop reception, clear the RXEMGn bit to 0 and then clear the POWERMGn bit to 0.

Caution 3. Follow the procedure below when setting the POWERMGn bit to 1 and then setting the RXEMGn bit to 1.
When ALVn = 0, the setting must be made while the level being input to the RXDMGn pin is high. Otherwise, reception is started at that point.
When ALVn = 1, the setting must be made while the level being input to the RXDMGn pin is low. Otherwise, reception is started at that point.

Caution 4. TXEMGn and RXEMGn are synchronized with the subsystem clock (f_{SUB}). To enable transmission or reception again, set the TXEMGn or RXEMGn bit to 1 at least two cycles of the subsystem clock after clearing the TXEMGn or RXEMGn bit to 0. If the bit is set to 1 within two cycles of the subsystem clock after the clearing, the transmission or reception circuit may not be able to be initialized.

Caution 5. After setting the TXEMGn bit to 1, wait at least one cycle of the subsystem clock before setting the transmit data in the TXBMGn register.

Caution 6. Clear the RXEMGn bit to 0 before modifying the ISRMMGn bit.

Caution 7. Be sure to clear bits 2, 3, and 4 to 0.

22.2.6 Operation Mode Setting Register 1 (ASIMMGn1) (n = 0)

The ASIMMGn1 register is an 8-bit register that controls serial communication of the serial interface UARTMGn.

The ASIMMGn1 register can be set by a 1-bit or 8-bit memory manipulation instruction.

The ASIMMGn1 register must be modified while TXEMGn = 0 and RXEMGn = 0.

Reset signal generation sets this register to 1AH.

Figure 22 - 7 Format of Operation Mode Setting Register 1 (ASIMMGn1)

Address: F0283H (ASIMMG01) After reset: 1AH R/W

Symbol	7	6	5	4	3	2	1	0
ASIMMGn1	—	PSn1	PSn0	CLn1	CLn0	SLn	DIRn	ALVn

PSn1 Note 1	PSn0 Note 1	Transmission/reception parity bit setting 1, 0	
		Transmission	Reception
0	0	No parity bit is output.	Data is received without parity.
0	1	0 parity is output.	Data is received with 0 parity. Note 4
1	0	Odd parity is output.	Check is made for odd parity.
1	1	Even parity is output.	Check is made for even parity.

CLn1 Note 3	CLn0 Note 3	Transmission/reception character length setting 1, 0
0	0	Character length of data = 5 bits
0	1	Character length of data = 5 bits
1	0	Character length of data = 7 bits
1	1	Character length of data = 8 bits

SLn Note 2	Transmission stop bit length setting
0	Stop bit length = 1 bit
1	Stop bit length = 2 bits

DIRn Note 1	Transmission/reception order setting
0	MSB first
1	LSB first

ALVn Note 1	Transmission/reception level setting Note 5
0	Positive logic (wait state = high level, start bit = low level, stop bit = high level)
1	Negative logic (wait state = low level, start bit = high level, stop bit = low level)

(**Notes** and **Cautions** are listed on the next page.)

Note 1. Modify the ALVn, DIRn, PSn0, and PSn1 bits while the TXEMGn and RXEMGn bits are 0 (in the transmission/reception stopped state).

Note 2. Modify the SLn bit while the TXEMGn bit is 0 (in the transmission stopped state).

Note 3. Modify the CLn0 and CLn1 bits while the TXEMGn and RXEMGn bits are 0 (in the transmission/reception stopped state). Otherwise, the character length of communication data is not guaranteed.

Note 4. When “Data is received with 0 parity” is set, parity check is not performed. Accordingly the PEMGn bit of the ASISMGn register is not set: no error interrupts are generated.

Note 5. Data level inversion is controlled in the “Inversion control” part in **Figure 22 - 1 Block Diagram of UARTMGn**.

Caution 1. Clear both the TXEMGn and RXEMGn bits to 0 before modifying the ASIMMGn1 register.

Caution 2. Reception is always handled as including 1 stop bit; the setting of the SLn bit does not affect reception.

Caution 3. Be sure to clear bit 7 to 0

22.2.7 Baud Rate Generator Control Register (BRGCMGn) (n = 0)

The BRGCMGn register sets the frequency divisor for the 8-bit counter in the serial interface UARTMGn.

The BRGCMGn register can be set by an 8-bit memory manipulation instruction.

Reset signal generation sets this register to FFH.

Figure 22 - 8 Format of Baud Rate Generator Control Register (BRGCMGn)

Address: F0284H (BRGCMG0) After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
BRGCMGn	—	—	—	—	—	—	—	—

Bits 7 to 0	Function
—	Controls the UART baud rate (serial transfer speed). For details on the settings, see **Table 22 - 3**.

Caution Modify the BRGCMGn bits while the TXEMGn and RXEMGn bits are 0 (in the transmission/reception stopped state).

Table 22 - 3 BRGCMGn Settings

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	k	Selection of 8-bit counter output clock
0	0	0	0	0	0	0	x	x	Setting prohibited
0	0	0	0	0	0	1	0	2	$f_{SUB}/2$
0	0	0	0	0	0	1	1	3	$f_{SUB}/3$
:	:	:	:	:	:	:	:	:	:
1	1	1	1	1	1	0	0	252	$f_{SUB}/252$
1	1	1	1	1	1	0	1	253	$f_{SUB}/253$
1	1	1	1	1	1	1	0	254	$f_{SUB}/254$
1	1	1	1	1	1	1	1	255	$f_{SUB}/255$

Caution The baud rate is one half the frequency of the output clock signal from the 8-bit counter.

Remark 1. k: The value set with the BRGCMGn bits (k = 2, 3, 4, 5, 6, …, 255)

Remark 2. X: Don't care.

For an example of the baud rate setting, see **22.3.4 (3) (c) Baud rate setting example**.

22.2.8 Status Register (ASISMGn) (n = 0)

The ASISMGn register indicates the error status and the transmission status on completion of reception by the serial interface UARTMGn. It consists of three error flag bits (PEMGn, FEMGn, and OVEMGn) and two transmission status flag bits (TXBFMGn and TXSFMGn).

The ASISMGn register is read-only and can be read by an 8-bit memory manipulation instruction.

Reset signal generation sets this register to 00H. The PEMGn, FEMGn, and OVEMGn bits are initialized by clearing the POWERMGn or RXEMGn bit to 0. These bits are also cleared by writing to the corresponding bit of the ASCTMGn register. The TXBFMGn and TXSFMGn bits are initialized by clearing the POWERMGn or TXEMGn bit to 0.

Figure 22 - 9 Format of Status Register (ASISMGn)

Address: F0285H (ASISMG0) After reset: 00H R

Symbol	7	6	5	4	3	2	1	0
ASISMGn	—	—	TXBFMGn	TXSFMGn	—	PEMGn	FEMGn	OVEMGn

TXBFMGn	Transmit buffer data flag
—	[Setting condition] • Data is written to the TXBMGn register. (Data exists in the TXBMGn register.) [Clearing conditions] • The POWERMGn or TXEMGn bit is cleared to 0. • Data is transferred to the transmit shift register.

TXSFMGn	Transmit shift register data flag
—	[Setting condition] • Data is transferred from the TXBMGn register. (Data is being transmitted.) [Clearing conditions] • The POWERMGn or TXEMGn bit is cleared to 0. • Data is transferred from the transmit shift register and then no subsequent data is transferred from the TXBMGn register.

PEMGn	Parity error flag
—	[Setting condition] • The parity of the received data does not match the parity bit. [Clearing conditions] • The POWERMGn or RXEMGn bit is cleared to 0. • 1 is written to the PECTMGn bit.

FEMGn	Framing error flag
—	[Setting condition] • A stop bit is not detected when receiving data. [Clearing conditions] • The POWERMGn or RXEMGn bit is cleared to 0. • 1 is written to the FECTMGn bit.

OVEMGn	Overrun error flag
—	[Setting condition] • The next reception is completed before the receive data in the RXBMGn register is read. [Clearing conditions] • The POWERMGn or RXEMGn bit is cleared to 0. • 1 is written to the OVECTMGn bit.

(**Cautions** are listed on the next page.)

Caution 1. For continuous transmission, be sure to check that the TXBFMGn flag is 0 after writing the the first transmit data (the first byte) to the TXBMGn register and then write the next transmit data (the second byte) to the TXBMGn register. Otherwise, the reliability of the transmit data is not guaranteed. However, the TXBFMGn flag need not be checked when continuous transmission is performed by using the transmit buffer empty interrupt (ISSMMGn bit = 1).

Caution 2. When initializing the transmission unit (TXEMGn = 0) after completion of continuous transmission, be sure to check that the TXSFMGn flag is 0 after the transmission completion interrupt is generated, and then initialize the unit. Otherwise, the reliability of the transmit data is not guaranteed.

Caution 3. The setting condition for the PEMGn bit depends on the setting of the PSn1 and PSn0 bits of the ASIMMGn1 register.

Caution 4. For the receive data, only the first 1 bit of the stop bits is checked regardless of the stop bit length.

Caution 5. When an overrun error occurs, the next receive data is not written to the RXBMGn register and discarded.

Caution 6. Be sure to clear bits 7, 6, and 3 to 0.

22.2.9 Status Clear Trigger Register (ASCTMGn) (n = 0)

The ASCTMGn register sets the trigger to clear the error status on completion of reception of the serial interface UARTMGn. It contains 3 bits of the error clear trigger flags (PECTMGn, FECTMGn, and OVECTMGn).

The ASCTMGn register can be written by an 8-bit or 1-bit memory manipulation instruction.

When the ASISMGn register is read, all bits are always read as 0.

Reset signal generation clears this register to 00H. Writing 1 to the PECTMGn, FECTMGn, and OVECTMGn bits clears the PEMGn, FEMGn, and OVEMGn bits of the ASISMGn register, respectively. When writing 0, the corresponding error flags are not cleared.

Figure 22 - 10 Format of Status Clear Trigger Register (ASCTMGn)

Address: F0286H (ASCTMG0) After reset: 00H R/W

Symbol	7	6	5	4	3	<2>	<1>	<0>
ASCTMGn	—	—	—	—	—	PECTMGn	ISSMMGn	ISRMMGn

PECTMGn	Parity error flag clear trigger
0	Does not clear the PEMGn flag. (The flag is retained.)
1	Clears the PEMGn flag.

FECTMGn	Framing error flag clear trigger
0	Does not clear the FEMGn flag. (The flag is retained.)
1	Clears the FEMGn flag.

OVECTMGn	Overrun error flag clear trigger
0	Does not clear the OVEMGn flag. (The flag is retained.)
1	Clears the OVEMGn flag.

Caution 1. When reading the ASCTMGn register, 0 is returned.

Caution 2. After writing 1 to the trigger bit, the corresponding error flag is cleared on the next rising edge of the operating clock (f_{SUB}). Accordingly, if reading the ASISMGn register immediately after writing 1 to the trigger bit, the corresponding error flag may not have been cleared yet.

22.3 Operation

UARTMGn operates in the following two modes.

- Operation stop mode
- UART mode

22.3.1 Operation Stop Mode

In the operation stop mode, serial communication is not performed, and thus the power consumption can be reduced. In addition, in this mode, the pins can be used as ordinary port pins. To set the operation stop mode, clear bits 7, 6, and 5 (POWERMGn, TXEMGn, RXEMGn) of the ASIMMGn0 register to 0.

The bus clock is not stopped by the above setting. To completely stop operation, clear the UARTMGnEN bit of the PER2 register to 0 after the above setting.

Remark n: unit number (n = 0)

22.3.2 UART Mode

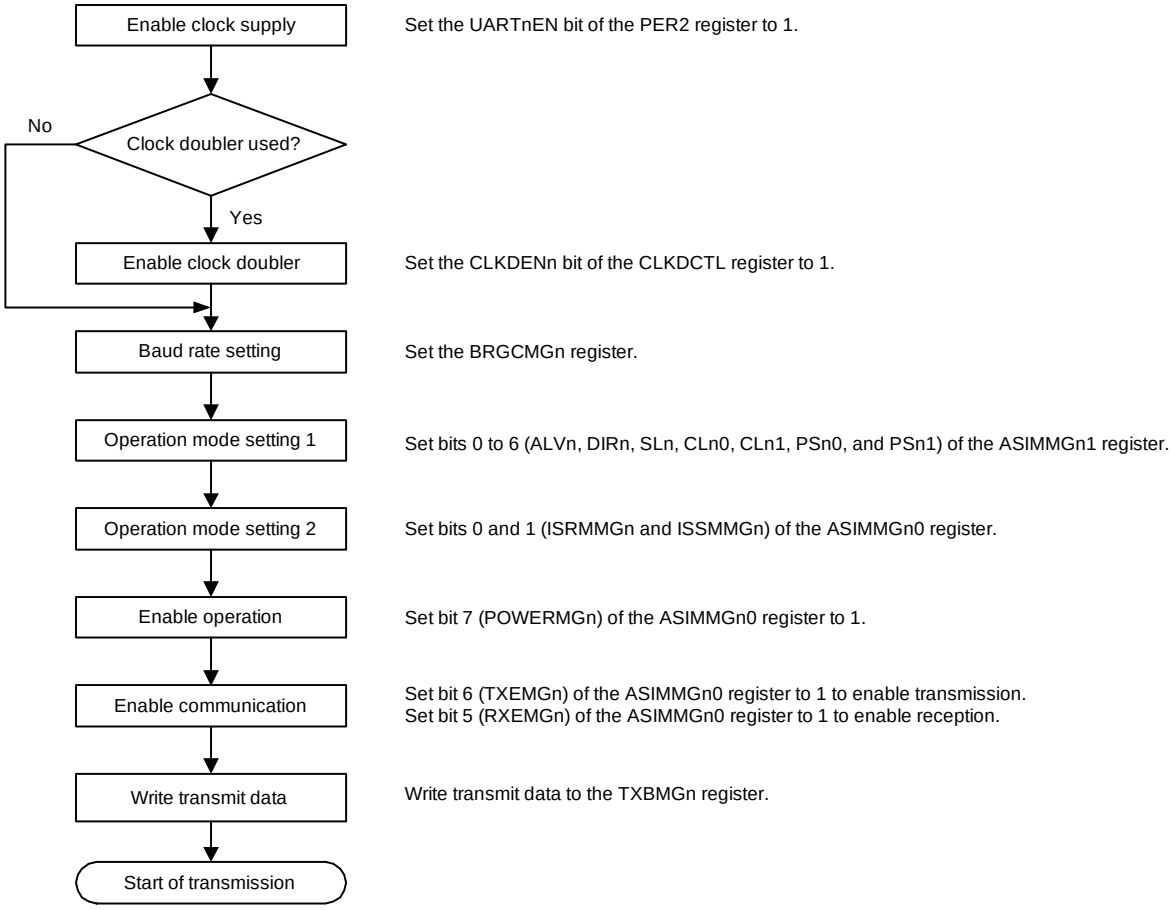
In this mode, one byte of data is transmitted and one byte is received following the start bit. That is, operation is full duplex.

A dedicated UART baud rate generator is incorporated, so that communication can be executed at a wide range of baud rates.

(1) Communication procedure

Figure 22 - 11 shows the flowchart of communication procedure.

Figure 22 - 11 Flowchart of Communication Procedure



Caution **When using the receiving function, set the port mode registers to input mode.**
When using the transmitting function, set the port mode registers to output mode, and set the port register to the high level.
Frequency-multiplied clock starts to be supplied with a delay of one cycle of the subsystem clock (f_{SUB}) after setting the CLKDCTL register.

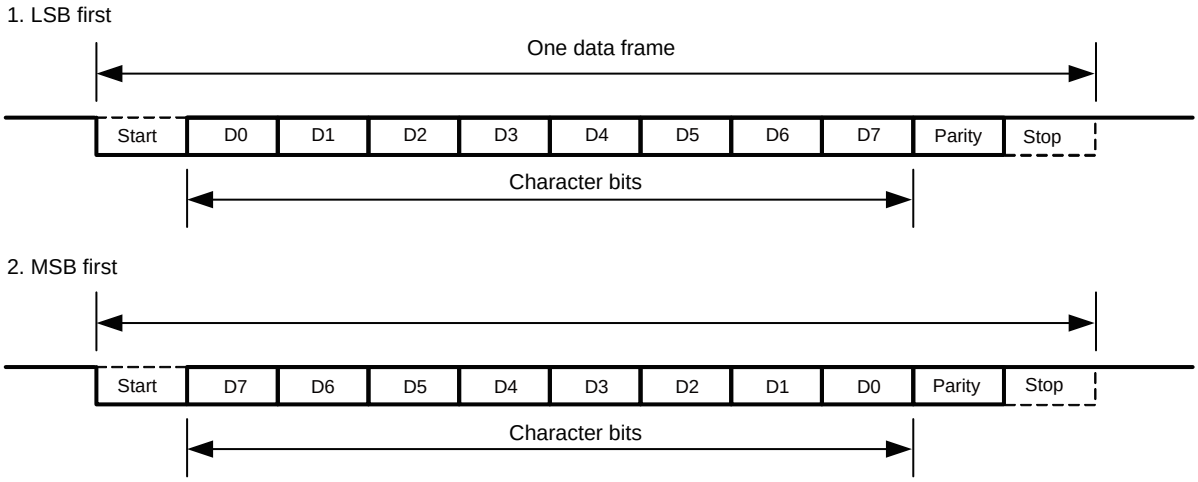
Remark n: unit number (n = 0)

(2) Format and waveform example of transmit/receive data

The following describes the communication data format of UARTMGn.

Figure 22 - 12 shows the data format.

Figure 22 - 12 Transmit/Receive Data Format



One data frame consists of the following bits.

- Start bit: 1 bit
- Character bits: 5, 7 or 8 bits
- Parity bit: Even parity, odd parity, 0 parity, or no parity
- Stop bit: 1 or 2 bits

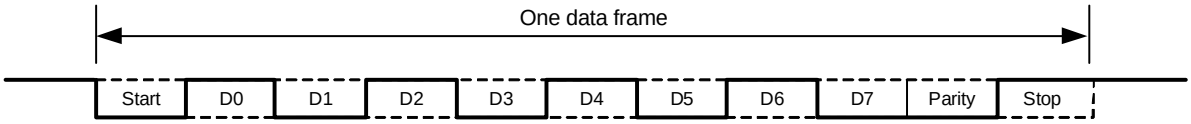
The character bit length, the parity, the stop bit length, the transfer direction (LSB/MSB first), and the TXDMGn pin output (direct/inverted) in one data frame are specified by the ASIMMGn1 register.

Remark n: unit number (n = 0)

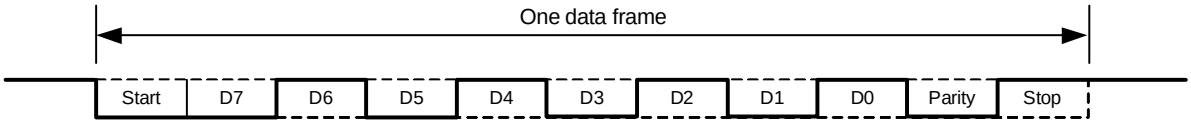
Figure 22 - 13 shows the examples of transmit/receive data waveforms.

Figure 22 - 13 Example of Transmit/Receive Data Waveform

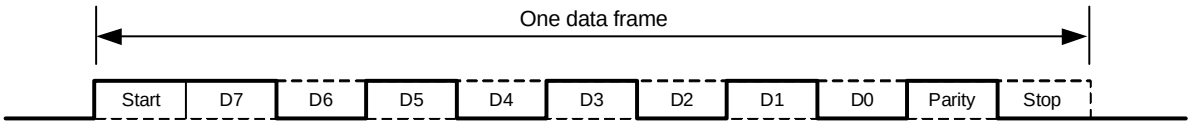
Character length: 8 bits, LSB first, Even parity, Stop bit: 1 bit, Transfer data: 55H



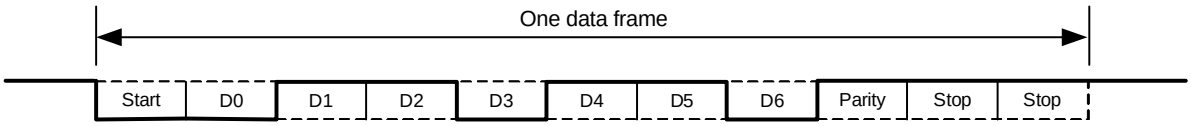
Character length: 8 bits, MSB first, Even parity, Stop bit: 1 bit, Transfer data: 55H



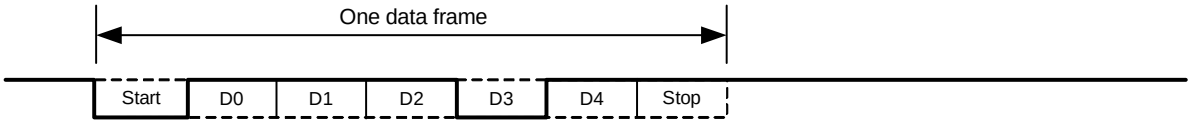
Character length: 8 bits, MSB first, Even parity, Stop bit: 1 bit, Transfer data: 55H, Transmit/receive data level inversion



Character length: 7 bits, LSB first, Odd parity, Stop bit: 2 bits, Transfer data: 36H



Character length: 5 bits, LSB first, No parity, Stop bit: 1 bit, Transfer data: 17H



(3) Parity types and operation

The parity bit is used to detect a bit error in communication data. Usually, the same type of parity bit is used on both the transmitting and reception sides. With even/odd parity, a 1-bit (odd number) error can be detected. With zero/no parity, an error cannot be detected.

(a) Even parity

- In transmission

  Data for transmission, including the parity bit, are controlled so that an even number of bits have the value “1”. The value of the parity bit is set as follows.

  If the data for transmission have an odd number of bits with the value “1”: 1

  If the data for transmission have an even number of bits with the value “1”: 0
- In reception

  In the data for reception, including the parity bit, the number of bits with the value "1" , is counted. If it is odd, a parity error occurs.

(b) Odd parity

- In transmission

  Unlike even parity, data for transmission, including the parity bit, are controlled so that an odd number of bits have the value “1”.

  If the data for transmission have an odd number of bits with the value “1”: 0

  If the data for transmission have an even number of bits with the value “1”: 1
- In reception

  In the data for reception, including the parity bit, the number of bits with the value "1" , is counted. If it is even, a parity error occurs.

(c) 0 parity

The parity bit is cleared to 0 when data is transmitted, regardless of the transmit data.

The parity bit is not detected when the data is received. Therefore, a parity error does not occur regardless of whether the parity bit is “0” or “1”.

(d) No parity

No parity bit is appended to the transmit data.

Reception is performed assuming that there is no parity bit. A parity error does not occur, because there is no parity bit.

(4) Normal transmission

Transmission is enabled by setting bit 7 (POWERMGn) of the operation mode register 0 (ASIMMGn0) to 1 and then setting bit 6 (TXEMGn) of ASIMMGn0 to 1. Transmission can be started by writing the data for transmission to the transmission buffer register (TXBMGn). The start bit, parity bit, and stop bit are automatically appended to the data.

When transmission is started, the data in the TXBMGn register is transferred to the transmit shift register. After that, the transmit data bits are sequentially output from the transmit shift register to the TXDMGn pin in the specified transfer direction. When transmission is completed, the parity and stop bits which are set by the ASIMMGn0 register are appended and a transmission completion interrupt request (INTSTMGn) is generated. Transmission is suspended until the next transmit data is written to the TXBMGn register.

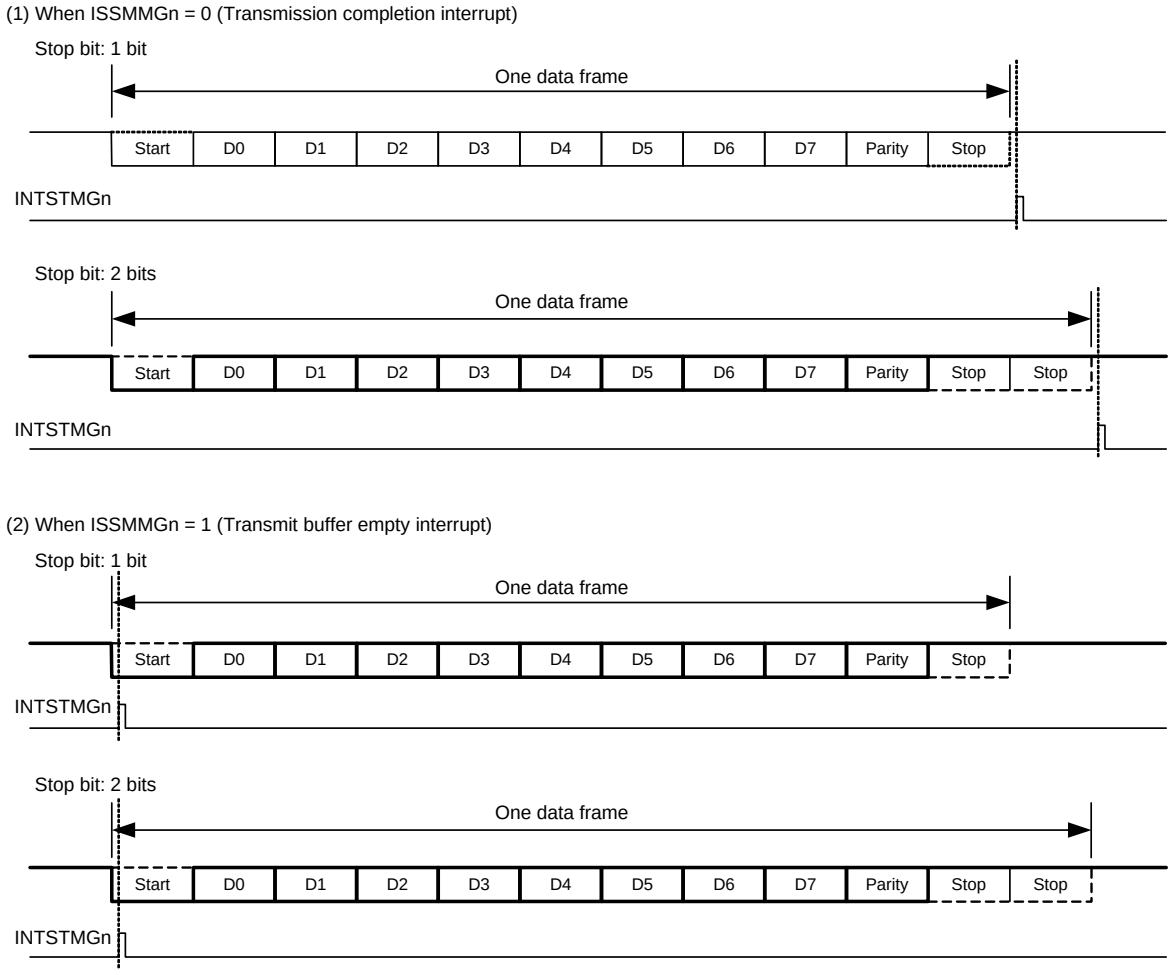
Figure 22 - 14 shows the timing of the transmission completion interrupt request (INTSTMGn). INTSTMGn is issued at the following timing.

(a) When ISSMMGn = 0 (INTSTMGn functions as a transmission completion interrupt.)
INTSTMGn is issued after the output of the last stop bit.

(b) ISSMMGn = 1 (INTSTMGn functions as a transfer buffer empty interrupt.)
INTSTMGn is issued when the start bit is output.

Remark n: unit number (n = 0)

Figure 22 - 14 Interrupt Output Timing



Remark n: unit number (n = 0)

(5) Continuous transmission

UARTMGn has two separate registers for continuous transmission: the transmit buffer register (TXBMGn) and the transmit shift register.

At the moment the transmit shift register starts a shift operation, the next transmit data can be written to the transmit buffer register (TXBMGn). This operation enables continuous transmission, thereby improving communication rate.

Continuous transmission is achieved by the following two methods.

(a) Continuous transfer by polling

Continuous transmission is achieved by polling the transmit buffer data flag (bit 5: TXBFMGn) and the transmit shift register data flag (bit 4: TXSFMGn) of the status register (ASISMGn).

When using this method, clear bit 1 (ISSMMGn) of the operation mode setting register 0 (ASIMMGn0) to 0.

• At the start of continuous transmission

At the start of continuous transmission, write the first byte of data to the TXBMGn register, check that the transmit buffer data flag (TXBFMGn) is 0, and then write the second byte of data.

TXBFMGn	Determination flag indicating that writing to TXBMGn is enabled or disabled at the start of continuous transmission
0	Writing is enabled.
1	Writing is disabled.

At the start of continuous transmission, only check this flag. The TXSFMGn flag must not be used for judgment in combination with this flag, as its value changes from 0 to 1.

• During continuous transmission

When continuous transmission is in progress, check the transmit shift register data flag after the transmission completion interrupt is generated to determine if the subsequent data can be written to the TXBMGn register.

When the flag is 1: Continuous transmission is in progress. One byte of data can be written.

When the flag is 0: Continuous transmission has been completed. Two bytes of data can be written according to the method used at the start of continuous transmission.

TXSFMGn	Determination flag for write processing during continuous transmission
0	Writing 2 bytes of data or transmission end processing is enabled.
1	Writing 1 byte of data is enabled.

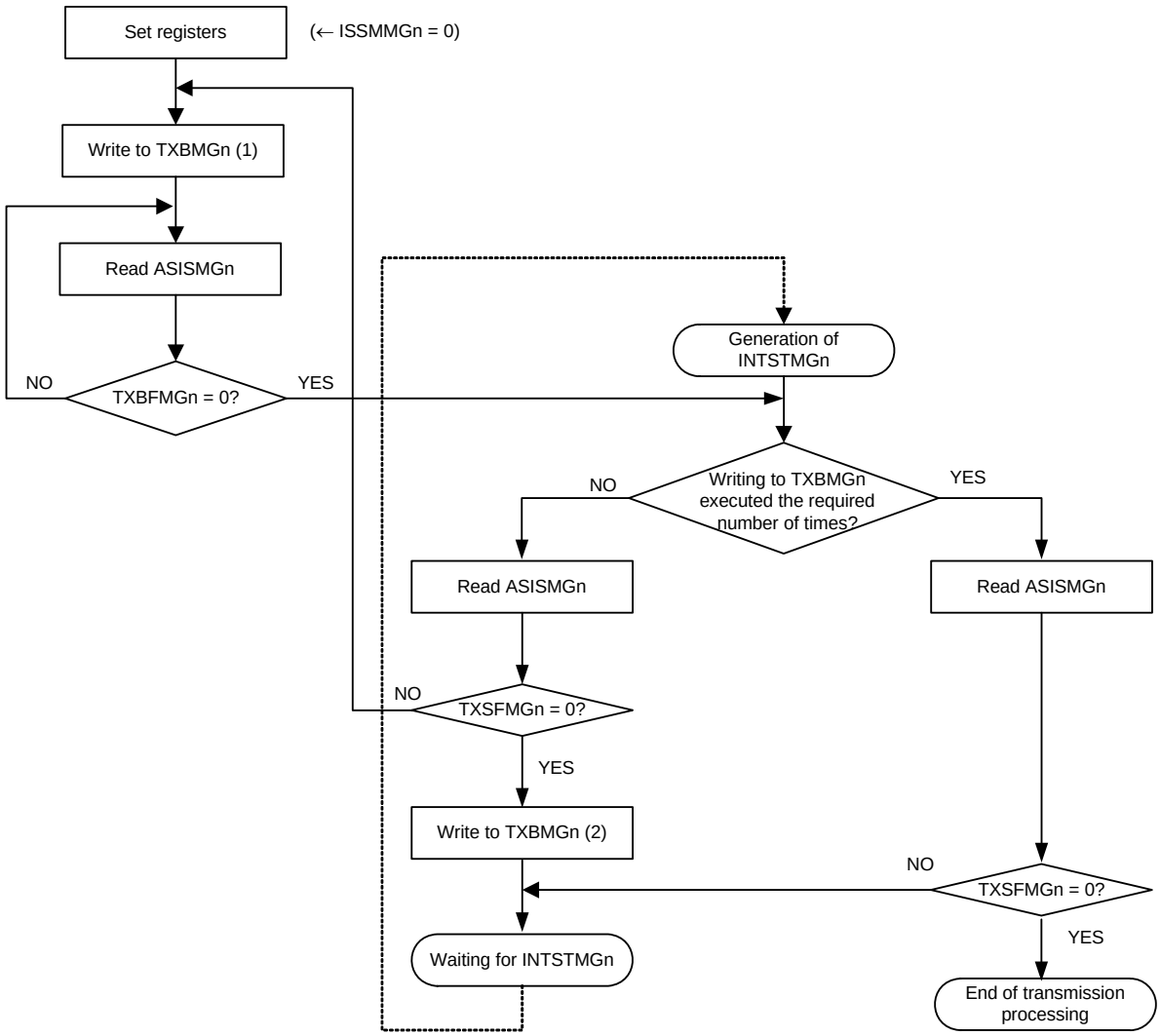
Caution 1. To execute initialization during continuous transmission, check before initialization that this flag has been cleared 0 after generation of a transmission completion interrupt. If initialization is executed while this flag is 1, the reliability of the transmit data is not guaranteed.

Caution 2. During continuous transmission, after transmission of one data frame, the subsequent transmission may be completed before execution of the INTSTMGn interrupt processing. This is called an overrun error. An overrun error can be detected by incorporating the program that counts the number of transmit data and by referencing the TXSFMGn flag.

Remark n: unit number (n = 0)

Figure 22 - 15 shows a flow example of continuous transmission processing by polling.

Figure 22 - 15 Flow Example of Continuous Transmission Processing by Polling



TXBFMGn
0: Writing to TXBMGn is enabled.
1: Writing to TXBMGn is disabled.

TXSFMGn
0: Writing 2 bytes of data or transmission end processing is enabled.
1: Writing 1 byte of data is enabled.

Remark n: unit number (n = 0)

(b) Continuous transfer by using an interrupt

Continuous transmission is achieved by using the interrupt (INTSTMGn).

The transfer completion interrupt can be switched to the transmit buffer register (TXBMGn) empty interrupt by setting bit 1 (ISSMMGn) to 1 in the operation mode setting register 0 (ASIMMGn0).

With this setting, data can be written to the TXBMGn register on occurrence of the INTSTMGn interrupt; thereby continuous transmission is enabled.

In addition, the transfer completion interrupt can be generated on completion of continuous transmission by clearing the ISSMMGn bit to 0 after writing the last transmit data to the TXBMGn register.

Note that continuous transmission is not achieved when writing to the TXBMGn register is not completed within the maximum number of clock cycles defined below from generation of the transmit buffer register (TXBMGn) empty interrupt.

Maximum number of clock cycles = Data transfer length × 2k - (2k + 3)

k: the value set with the BRGCMGn bits (k = 2, 3, 4, 5, 6, …, 255)

An example of calculating the maximum number of clock cycles is described below.

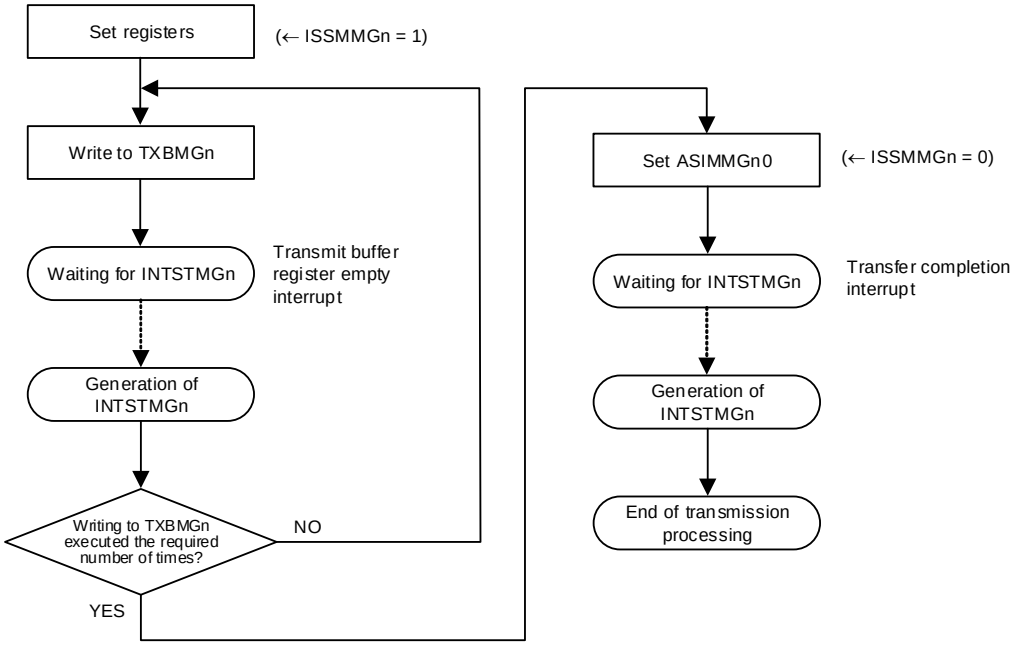
When the BRGCMGn register = 02H (k = 2), start bit = 1 bit, character length = 8 bits, parity used, and stop bit = 1 bit:

The maximum number of clock cycles = Transfer length × 2k - (2k + 3) = 11 × 2 × 2 - (2 × 2 + 3) = 37

(Writing must be completed within 37 clock cycles.)

Figure 22 - 16 shows a flow example of continuous transmission using interrupt.

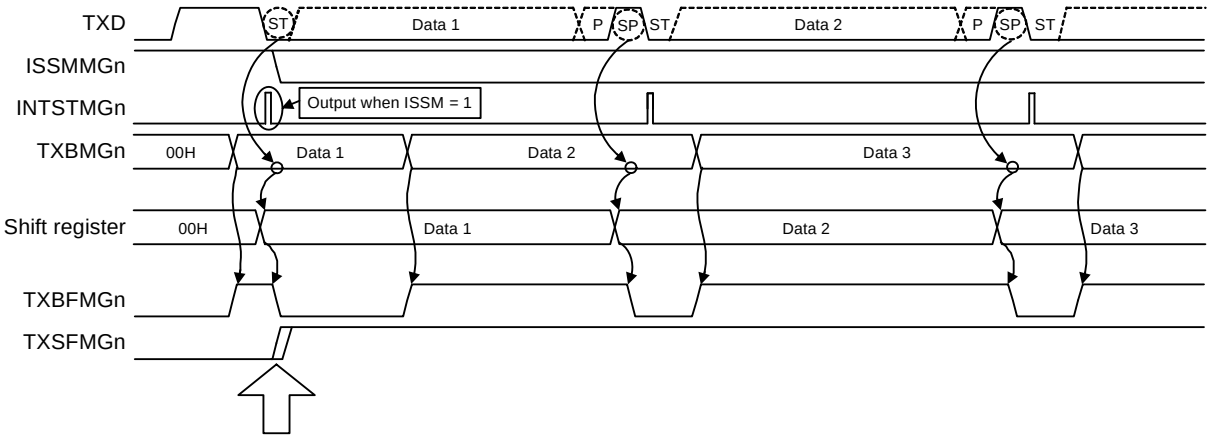
Figure 22 - 16 Flow Example of Continuous Transmission Using Interrupt



Remark n: unit number (n = 0)

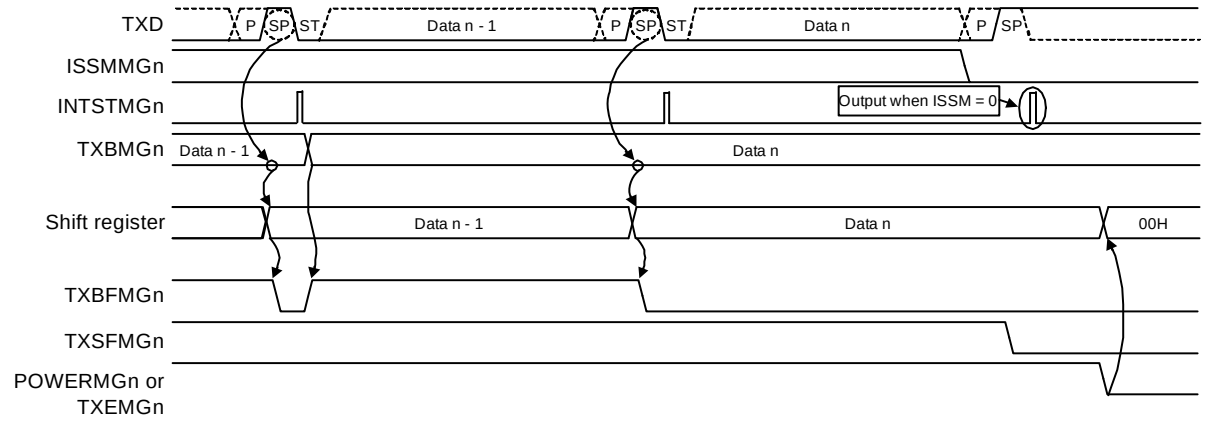
Figure 22 - 17 and **Figure 22 - 18** show the timing charts when the continuous transmission is started and completed, respectively.

Figure 22 - 17 Timing Chart When Continuous Transmission Is Started



Caution **When the ASISMGn register is read, both the TXBFMGn and TXSFMGn bits are read as 1 within this period. Accordingly, use only the TXBFMGn flag to determine if writing is enabled or disabled.**

Figure 22 - 18 Timing Chart When Continuous Transmission is Completed



Remark n: unit number (n = 0)

(6) Normal reception

When setting bit 7 (POWERMGn) of the operation mode register 0 (ASIMMGn0) to 1 and then setting bit 5 (RXEMGn) of the ASIMMGn0 register to 1, reception is enabled, and sampling of the input to the RXDMGn pin is performed.

When the ALVn bit is 0, the 8-bit counter of the baud rate generator starts counting on detection of the falling edge on the RXDMGn pin. When the counter reaches the set value of the baud rate generator control register (BRGCMGn), the input to the RXDMGn pin is sampled again (at the point indicated with ∇ in **Figure 22 - 19**). If the RXDMGn pin is low, it is regarded as a start bit.

When the ALVn bit is 1, the 8-bit counter of the baud rate generator starts counting on detection of the rising edge on the RXDMGn pin. When the counter reaches the set value of the baud rate generator control register (BRGCMGn), the input to the RXDMGn pin is sampled again (at the point indicated with ∇ in **Figure 22 - 19**). If the RXDMGn pin is high, it is regarded as a start bit.

Figure 22 - 19 shows the timing chart of receive operation.

On detection of a start bit, receive operation is started: serial data is sequentially stored in the receive shift register at a specified baud rate. On reception of a stop bit, the reception completion interrupt (INTSRMGn) is generated, and at the same time, the data in the receive shift register is written to the receive buffer register (RXBMGn).

Note that when an overrun error (OVEMGn) occurs, the data received on occurrence of the error is not written to the RXBMGn register.

When a parity error (PEMGn) or a framing error (FEMGn) occurs during reception, reception continues until a stop bit is received. After completion of the reception, the reception error interrupt (INTSRMGn/INTSREMGn) set in ISRMMGn is generated.

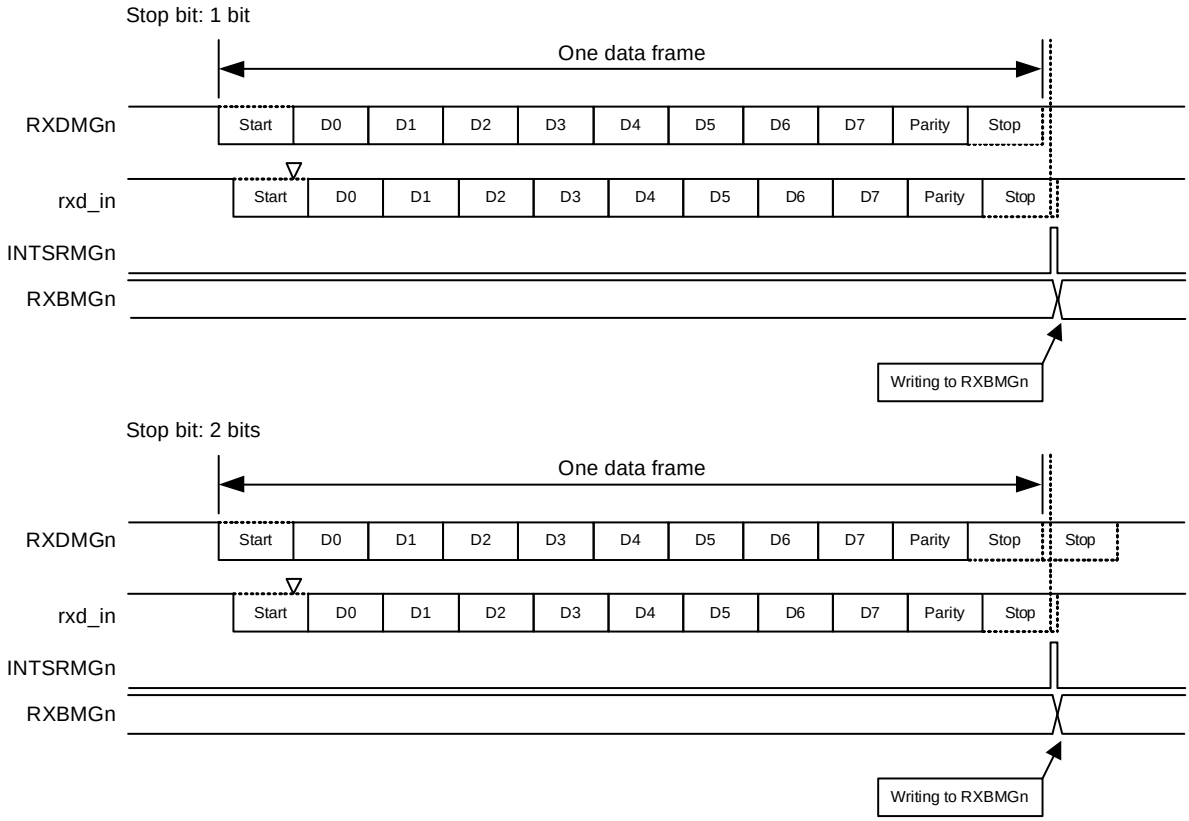
When a reception error occurs, read the status register (ASISMGn) and then read the receive buffer register (RXBMGn) to clear the error flag.

If the receive buffer register (RXBMGn) is not read, an overrun error will occur when the next data is received: the reception error state will continue.

Reception is always handled as including 1 stop bit. Accordingly, the second stop bit is ignored.

Remark n: unit number (n = 0)

Figure 22 - 19 Timing of UART Receive Operation



Remark 1. rxd_in: the internal signal generated by latching RXDMGn with a noise filter (rxd_in is delayed relative to RXDMGn by maximum of 3 cycles of the UART operation clock.)

Remark 2. The INTSRMGn output timing in the figure is just an example. The timing relative to RXDMGn varies according to the setting of the BRGCMGn register.

Remark 3. n: unit number (n = 0)

(7) Reception error

Three types of errors may occur during reception; parity error, framing error, and overrun error. When these errors occur, the corresponding error flag in the status register (ASISMGn) is set, and the reception error interrupt (INTSRMGn or INTSREMGn) is generated.

The type of the reception error can be identified by the reception error interrupt processing routine, which reads and checks the contents of the status register (ASISMGn).

The contents of the ASISMGn register is cleared to 0 by setting the corresponding bit of the status clear trigger register (ASCTMGn) to 1.

Table 22 - 4 shows the causes of the reception errors.

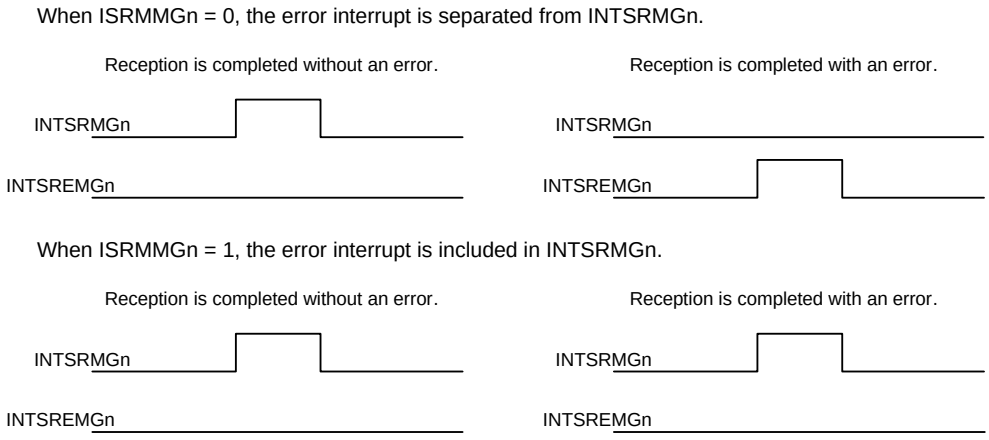
Table 22 - 4 Causes of Reception Errors

Error flag	Reception error	Cause
PEMGn	Parity error	The parity specified for reception does not match the parity of receive data.
FEMGn	Framing error	No stop bit is detected.
OVEMGn	Overrun error	Before the receive data is read from the receive buffer, the next data reception is completed.

Setting bit 0 (ISRMMGn) of the operation mode register 0 (ASIMMGn0) to 0 allows the reception error interrupt to be separated from the reception completion interrupt (INTSRMGn) and allows it to be generated as the error interrupt (INTSREMGn).

Figure 22 - 20 shows the interrupt output waveform which varies depending on the setting of ISRMMGn.

Figure 22 - 20 Various Interrupt Output Waveforms Depending on ISRMMGn Setting



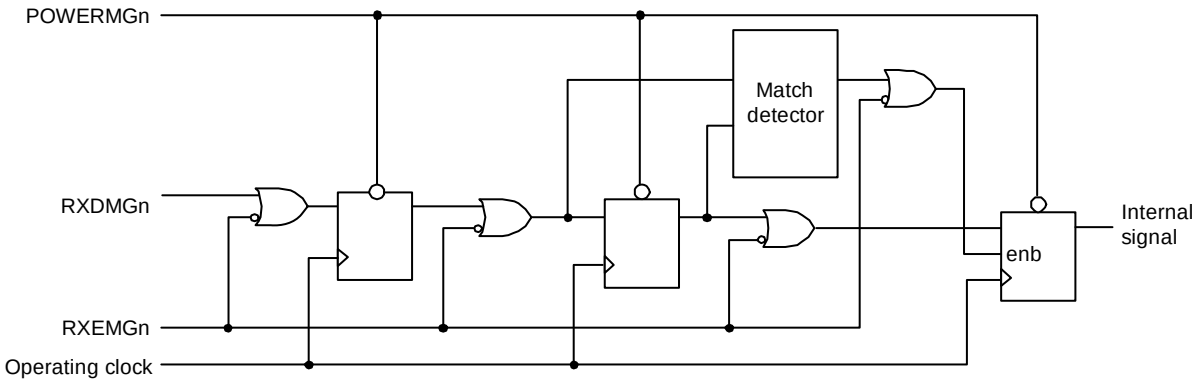
Remark n: unit number (n = 0)

22.3.3 Receive Data Noise Filter

This filter samples the receive data (RXDMGn), and determines the level when the same level is sampled twice. The receive data is delayed by maximum of three cycles of the operating clock because of the circuit configuration.

Figure 22 - 21 shows the noise filter circuit.

Figure 22 - 21 Noise Filter



Caution 1. When ALVn = 0 (wait state = high level; start bit = low level), the initial value of the receive data (RXDMGn) needs to be "high".

Caution 2. When ALVn = 1 (wait state = low level; start bit = high level), the initial value of the receive data (RXDMGn) needs to be "low".

Remark n: unit number (n = 0)

22.3.4 Baud Rate Generator

The baud rate generator consists of 8-bit programmable counters, and generates a serial clock for transmission/reception of UARTMGn.
An 8-bit counter is provided each for transmission and reception.

(1) Configuration of baud rate generator

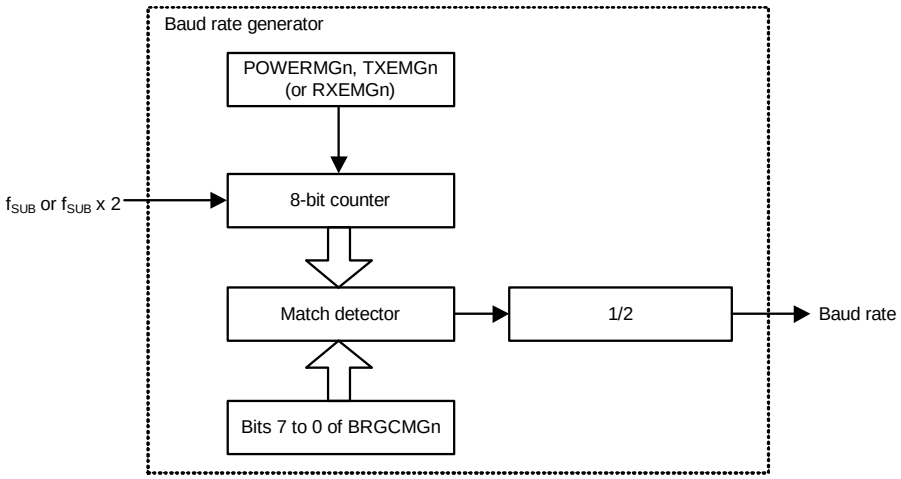
(a) Base clock
When bit 7 (POWERMGn) = 1 in the operation mode register 0 (ASIMMGn0), the operating clock (f_{SUB} or $f_{SUB} \times 2$) of UARTMGn is supplied to each module. This clock is called the base clock. When POWERMGn = 0, the base clock is fixed to low level.

(b) Transmission counter
This counter is cleared to 0 and stops when bit 7 (POWERMGn) = 0 or bit 6 (TXEMGn) = 0 in the operation mode register 0 (ASIMMGn0). It starts counting when POWERMGn = 1 and TXEMGn = 1.
The counter is cleared to 0 when the first transmit data is written to the transmit buffer register (TXBMGn). When continuous transmission is performed, the counter is cleared to 0 again when transmission of one frame of data has been completed. If there is no data to be transmitted next, the counter is not cleared to 0 and continues counting until the POWERMGn or TXEMGn bit is cleared to 0. When POWERMGn = 0 or TXEMGn =0 in the ASIMMGn0 register, the counter stops at 00H.

(c) Reception counter
This counter is cleared to 0 and stops when bit 7 (POWERMGn) = 0 or bit 5 (RXEMGn) = 0 in the operation mode register 0 (ASIMMGn0). It starts counting when the start bit is detected.
The counter stops operation after one frame has been received, until the next start bit is detected. When POWERMGn = 0 or RXEMGn = 0 in the ASIMMGn0 register, the counter stops at 00H.

Figure 22 - 22 shows the configuration of the baud rate generator.

Figure 22 - 22 Configuration of Baud Rate Generator



Remark n: Unit number (n = 0)

(2) Generation of serial clock

A serial clock to be generated can be specified by using the baud rate generator control register (BRGCMGn).

The frequency divisor for the 8-bit counter can be selected as a value in the range from $f_{SUB}/2$ to $f_{SUB}/255$ by the setting of bits 7 to 0 in BRGCMGn.

(3) Baud rate calculation

(a) Baud rate calculation expression

The baud rate can be calculated by the following expression.

Baud rate = $f_{SUB} \div (2 \times k)$ [bps]

f_{SUB}: Frequency of operating clock

k: Value set by bits 7 to 0 of the BRGCMGn register (k = 2, 3, 4, …, 255)

(b) Baud rate error

The baud rate error can be calculated by the following expression.

$$\text{Error} = \left(\frac{\text{Actual baud rate (baud rate with error)}}{\text{Desired baud rate (correct baud rate)}} - 1 \right) \times 100\ [\%]$$

Caution 1. Keep the baud rate error during transmission to within the permissible error range on the reception side.

Caution 2. Make sure that the baud rate error during reception satisfies the permissible baud rate error range during reception. Permissible baud rate error during reception is described in 22.3.4 (2) (d) Permissible baud rate range during reception.

Remark n: unit number (n = 0)

(c) Baud rate setting example

Table 22 - 5 Set Data of Baud Rate Generator

Desired baud rate	In operation with f_{SUB} = 38.4 kHz				In operation with f_{SUB} = 32.768 kHz	
	CLKDENn = 0		CLKDENn = 1		CLKDENn = 0	
	k	Error from the desired baud rate	k	Error from the desired baud rate	k	Error from the desired baud rate
200 bps	96	±0.00%	192	±0.00%	82	-0.10%
300 bps	64	±0.00%	128	±0.00%	55	-0.70%
1200 bps	16	±0.00%	32	±0.00%	14	-2.48%
2400 bps	8	±0.00%	16	±0.00%	7	-2.48%
4800 bps	4	±0.00%	8	±0.00%	Disabled	
9600 bps	2	±0.00%	4	±0.00%	Disabled	
19200 bps	Disabled		2	±0.00%	Disabled	

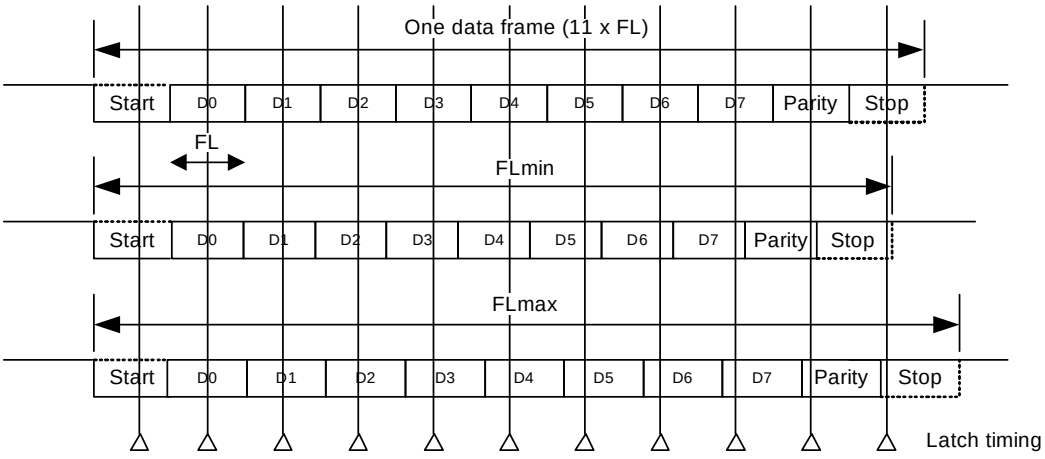
Remark k: Value set by bits 7 to 0 of the baud rate generator control register (BRGCMGn) (k = 2, 3, 4, …, 255)

(d) Permissible baud rate range during reception

Figure 22 - 23 shows the permissible error from the baud rate on the transmitting side during reception.

Figure 22 - 23 Permissible Baud Rate Range during Reception

Data length: 8 bits, with parity, stop bit: 1 bit



Caution Be sure to make settings so that the baud rate error during reception is within the permissible error range . Use the calculation expression below to check if the error is within the permissible range.

After the start bit is detected, the latch timing of receive data is determined by the counter specified with the baud rate generator control register (BRGCMGn). If the whole frame including the stop bit has been received before this latching, reception can proceed correctly. Assuming that 11 bits of data are received, the theoretical values can be calculated as follows.

Remark n: unit number (n = 0)

- The relation between 1-bit data length and baud rate
  FL = (Brate) - 1
  Brate: Baud rate of UART
  k: Set value of BRGCMGn
  FL: 1-bit data length
  Margin of latch timing: 1 clock

- Minimum permissible data frame length (FLmin)

$$FLmin = 11 \times FL - \frac{k - 1}{2k} \times FL = \frac{21k + 1}{2k} FL$$

- Maximum permissible baud rate for reception on the transmitting side (BRmax)

$$BRmax = (FLmin/11)^{-1} = \frac{22k}{21k + 1} Brate$$

- Maximum permissible data frame length (FLmax)

$$FLmax = \frac{21k + 1}{20k} FL \times 11$$

- Minimum permissible baud rate for reception on the transmitting side (BRmin)

$$BRmin = (FLmax/11)^{-1} = \frac{20k}{21k - 1} Brate$$

The permissible baud rate error between UART and the transmitting side can be calculated from the above minimum and maximum baud rate expressions, as follows.

Table 22 - 6 Maximum/Minimum Permissible Baud Rate Error

Division ratio (k)	Maximum permissible baud rate error	Minimum permissible baud rate error
2	+2.32%	-2.43%
4	+3.52%	-3.61%
8	+4.14%	-4.19%
20	+4.51%	-4.53%
50	+4.66%	-4.67%
100	+4.71%	-4.71%
255	+4.74%	-4.74%

Remark 1. The permissible error of reception depends on the number of bits in one frame, input clock frequency, and division ratio (k). The higher the input clock frequency and the division ratio (k), the higher the permissible error.

Remark 2. k: Set value of BRGCMGn

Remark 3. n: unit number (n = 0)

22.4 Usage Notes

22.4.1 Port Setting for RXDMGn Pin

When ALVn = 0 (wait state = high level, start bit = low level), the initial value of receive data (RXDMGn) must be high.

When ALVn = 1 (wait state = low level, start bit = high level), the initial value of receive data (RXDMGn) must be low.

Accordingly, port setting is required for the RXDMGn pin before setting POWERMGn = 1.

Remark n: unit number (n = 0)

CHAPTER 23 LCD CONTROLLER/DRIVER (R5F11NM, R5F11NL, and R5F11RM only)

The number of LCD display function pins of the RL78/H1D differs depending on the product. The following table shows the number of pins of each product.

Table 23 - 1 Number of LCD Display Function Pins of Each Product

Item		RL78/H1D																							
		R5F11NM								R5F11NL								R5F11RM							
Number of LCD output pins		Segment signal outputs: 36 (32) Note Common signal outputs: 8								Segment signal outputs: 27 (23) Note Common signal outputs: 8								Segment signal outputs: 36 (32) Note Common signal outputs: 8							
Multiplexed I/O port		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Segment	P0	SEG 28	SEG 27	SEG 26	SEG 25	SEG 24	SEG 23	SEG 22	—	SEG 28	SEG 27	SEG 26	—	SEG 24	—	—	—	SEG 28	SEG 27	SEG 26	SEG 25	SEG 24	SEG 23	SEG 22	—
	P1	—	SEG 35	SEG 34	SEG 33	SEG 32	SEG 31	SEG 30	SEG 29	—	—	SEG 34	SEG 33	SEG 32	SEG 31	SEG 30	SEG 29	—	SEG 35	SEG 34	SEG 33	SEG 32	SEG 31	SEG 30	SEG 29
	P3	SEG 21	SEG 20	SEG 19	—	—	SEG 18	SEG 17	SEG 16	SEG 21	SEG 20	SEG 19	—	—	SEG 18	SEG 17	SEG 16	SEG 21	SEG 20	SEG 19	—	—	SEG 18	SEG 17	SEG 16
	P5	—	—	—	—	SEG 4	SEG 5	SEG 6	SEG 7	—	—	—	—	—	SEG 5	SEG 6	SEG 7	—	—	—	—	SEG 4	SEG 5	SEG 6	SEG 7
	P7	SEG 15	SEG 14	SEG 13	SEG 12	SEG 11	SEG 10	SEG 9	SEG 8	SEG 15	SEG 14	—	—	—	—	SEG 9	SEG 8	SEG 15	SEG 14	SEG 13	SEG 12	SEG 11	SEG 10	SEG 9	SEG 8
Alternate relationship between COM signal output pins and I/O pots		—								—								—						
Alternate relationship between COM signal output pins and LCD display function pins	COM4	SEG0								SEG0								SEG0							
	COM5	SEG1								SEG1								SEG1							
	COM6	SEG2								SEG2								SEG2							
	COM7	SEG3								SEG3								SEG3							

Note ( ) indicates the number of signal output pins when 8 com is used.

23.1 Functions of LCD Controller/Driver

The functions of the LCD controller/driver in the RL78/H1D microcontrollers are as follows.

(1) Waveform A or B selectable
(2) The LCD driver voltage generator can switch internal voltage boosting method, capacitor split method, and external resistance division method.
(3) Automatic output of segment and common signals based on automatic display data register read
(4) The reference voltage to be generated when operating the voltage boost circuit can be selected from 16 steps (contrast adjustment).
(5) LCD blinking is available

Tables 23 - 2 to **23 - 4** list the maximum number of pixels that can be displayed in each display mode.

Table 23 - 2 Maximum Number of Pixels (R5F11NM)

Drive Waveform for LCD Driver	LCD Driver Voltage Generator	Bias Mode	Number of Time Slices	Maximum Number of Pixels
Waveform A	External resistance division	—	Static	36 (36 segment signals, 1 common signal)
		1/2	2	72 (36 segment signals, 2 common signals)
			3	108 (36 segment signals, 3 common signals)
		1/3	3	
			4	144 (36 segment signals, 4 common signals)
			6	204 (34 segment signals, 6 common signals)
			8	256 (32 segment signals, 8 common signals)
		1/4	8	
	Internal voltage boosting	1/3	3	108 (36 segment signals, 3 common signals)
			4	144 (36 segment signals, 4 common signals)
			6	204 (34 segment signals, 6 common signals)
			8	256 (32 segment signals, 8 common signals)
		1/4	6	204 (34 segment signals, 6 common signals)
			8	256 (32 segment signals, 8 common signals)
	Capacitor split	1/3	3	108 (36 segment signals, 3 common signals)
			4	144 (36 segment signals, 4 common signals)
			6	204 (34 segment signals, 6 common signals)
			8	256 (32 segment signals, 8 common signals)
Waveform B	External resistance division, internal voltage boosting	1/3	3	108 (36 segment signals, 3 common signals)
			4	144 (36 segment signals, 4 common signals)
			6	204 (34 segment signals, 6 common signals)
			8	256 (32 segment signals, 8 common signals)
		1/4	8	
	Capacitor split	1/3	3	108 (36 segment signals, 3 common signals)
			4	144 (36 segment signals, 4 common signals)
			6	204 (34 segment signals, 6 common signals)
			8	256 (32 segment signals, 8 common signals)

Table 23 - 3 Maximum Number of Pixels (R5F11NL)

Drive Waveform for LCD Driver	LCD Driver Voltage Generator	Bias Mode	Number of Time Slices	Maximum Number of Pixels
Waveform A	External resistance division	-	Static	27 (27 segment signals, 1 common signal)
		1/2	2	54 (27 segment signals, 2 common signals)
			3	81 (27 segment signals, 3 common signals)
		1/3	3	
			4	108 (27 segment signals, 4 common signals)
			6	150 (25 segment signals, 6 common signals)
			8	184 (23 segment signals, 8 common signals)
		1/4	8	
	Internal voltage boosting	1/3	3	81 (27 segment signals, 3 common signals)
			4	108 (27 segment signals, 4 common signals)
			6	150 (25 segment signals, 6 common signals)
			8	184 (23 segment signals, 8 common signals)
		1/4	6	150 (25 segment signals, 6 common signals)
			8	184 (23 segment signals, 8 common signals)
	Capacitor split	1/3	3	81 (27 segment signals, 3 common signals)
			4	108 (27 segment signals, 4 common signals)
			6	150 (25 segment signals, 6 common signals)
			8	184 (23 segment signals, 8 common signals)
Waveform B	External resistance division, internal voltage boosting	1/3	3	81 (27 segment signals, 3 common signals)
			4	108 (27 segment signals, 4 common signals)
			6	150 (25 segment signals, 6 common signals)
			8	184 (23 segment signals, 8 common signals)
		1/4	8	
	Capacitor split	1/3	3	81 (27 segment signals, 3 common signals)
			4	108 (27 segment signals, 4 common signals)
			6	150 (25 segment signals, 6 common signals)
			8	184 (23 segment signals, 8 common signals)

Table 23 - 4 Maximum Number of Pixels (R5F11RM)

Drive Waveform for LCD Driver	LCD Driver Voltage Generator	Bias Mode	Number of Time Slices	Maximum Number of Pixels
Waveform A	External resistance division	-	Static	36 (36 segment signals, 1 common signal)
		1/2	2	72 (36 segment signals, 2 common signals)
			3	108 (36 segment signals, 3 common signals)
		1/3	3	
			4	144 (36 segment signals, 4 common signals)
			6	204 (34 segment signals, 6 common signals)
			8	256 (32 segment signals, 8 common signals)
		1/4	8	
	Internal voltage boosting	1/3	3	108 (36 segment signals, 3 common signals)
			4	144 (36 segment signals, 4 common signals)
			6	204 (34 segment signals, 6 common signals)
			8	256 (32 segment signals, 8 common signals)
		1/4	6	204 (34 segment signals, 6 common signals)
			8	256 (32 segment signals, 8 common signals)
	Capacitor split	1/3	3	108 (36 segment signals, 3 common signals)
			4	144 (36 segment signals, 4 common signals)
			6	204 (34 segment signals, 6 common signals)
			8	256 (32 segment signals, 8 common signals)
Waveform B	External resistance division, internal voltage boosting	1/3	3	108 (36 segment signals, 3 common signals)
			4	144 (36 segment signals, 4 common signals)
			6	204 (34 segment signals, 6 common signals)
			8	256 (32 segment signals, 8 common signals)
		1/4	8	
	Capacitor split	1/3	3	108 (36 segment signals, 3 common signals)
			4	144 (36 segment signals, 4 common signals)
			6	204 (34 segment signals, 6 common signals)
			8	256 (32 segment signals, 8 common signals)

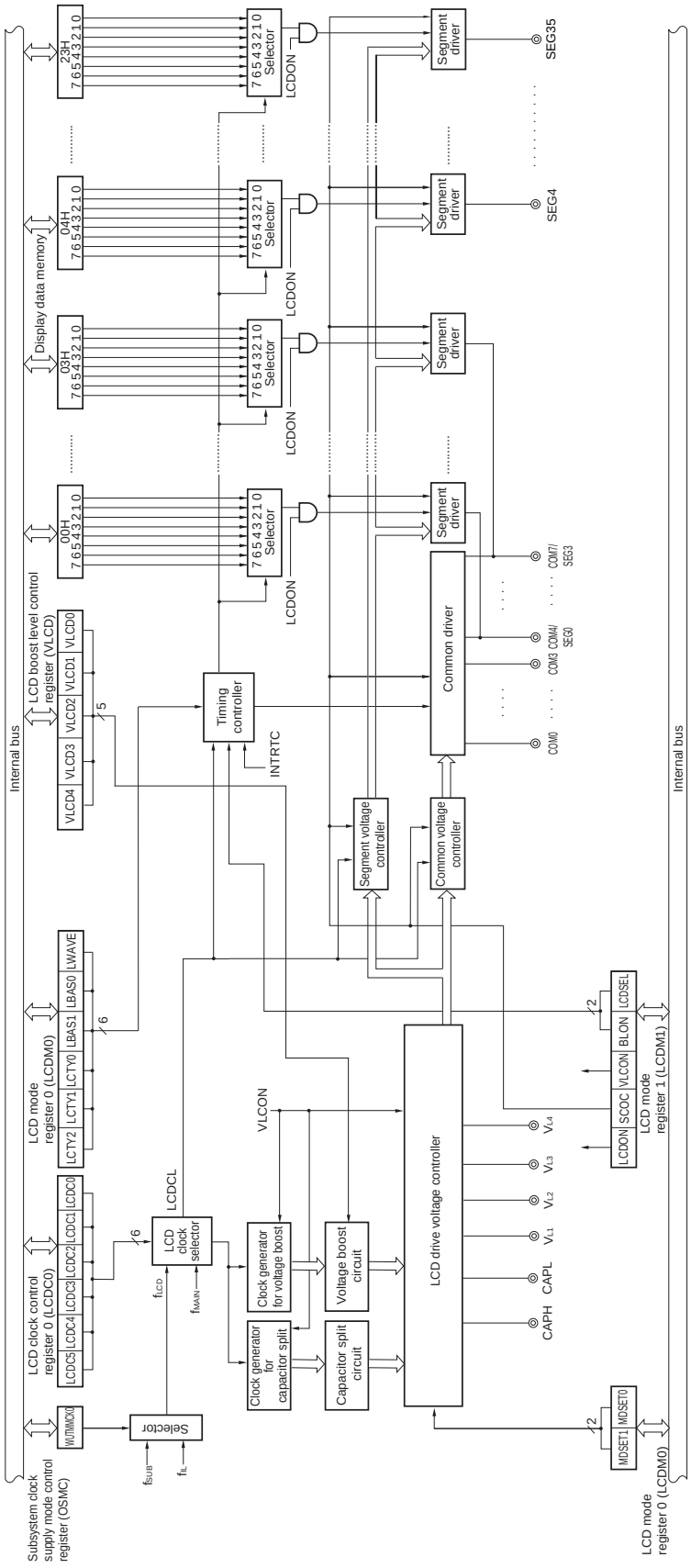
23.2 Configuration of LCD Controller/Driver

The LCD controller/driver consists of the following hardware.

Table 23 - 5 Configuration of LCD Controller/Driver

Item	Configuration
Control registers	LCD mode register 0 (LCDM0) LCD mode register 1 (LCDM1) Subsystem clock supply option control register (OSMC) LCD clock control register 0 (LCDC0) LCD boost level control register (VLCD) LCD input switch control register (ISCLCD) LCD port function registers 0 to 4 (PFSEG0 to PFSEG4) Port mode registers 0, 1, 3, 5, 7 (PM0, PM1, PM3, PM5, PM7) Port mode control registers 0, 1 (PMC0, PMC1)

Figure 23 - 1 Block Diagram of LCD Controller/Driver



23.3 Registers Controlling LCD Controller/Driver

The following nine registers are used to control the LCD controller/driver.

- LCD mode register 0 (LCDM0)
- LCD mode register 1 (LCDM1)
- Subsystem clock supply option control register (OSMC)
- LCD clock control register 0 (LCDC0)
- LCD boost level control register (VLCD)
- LCD input switch control register (ISCLCD)
- LCD port function registers 0 to 4 (PFSEG0 to PFSEG4)
- Port mode registers 0, 1, 3, 5, 7 (PM0, PM1, PM3, PM5, PM7)
- Port mode control registers 0, 1 (PMC0, PMC1)

23.3.1 LCD mode register 0 (LCDM0)

LCDM0 specifies the LCD operation.

This register is set by using an 8-bit memory manipulation instruction.

Reset signal generation sets LCDM0 to 00H.

Figure 23 - 2 Format of LCD Mode Register 0 (LCDM0)

Address: FFF40H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
LCDM0	MDSET1	MDSET0	LWAVE	LDTY2	LDTY1	LDTY0	LBAS1	LBAS0

MDSET1	MDSET0	LCD drive voltage generator selection
0	0	External resistance division method
0	1	Internal voltage boosting method
1	0	Capacitor split method
1	1	Setting prohibited

LWAVE	LCD display waveform selection
0	Waveform A
1	Waveform B

LDTY2	LDTY1	LDTY0	Selection of time slice of LCD display
0	0	0	Static
0	0	1	2-time slice
0	1	0	3-time slice
0	1	1	4-time slice
1	0	0	6-time slice
1	0	1	8-time slice
Other than above			Setting prohibited

LBAS1	LBAS0	LCD display bias mode selection
0	0	1/2 bias method
0	1	1/3 bias method
1	0	1/4 bias method
1	1	Setting prohibited

Caution 1. Do not rewrite the LCDM0 value while the SCOC bit of the LCDM1 register = 1.

Caution 2. When "Static" is selected (LDTY2 to LDTY0 bits = 000B), be sure to set the LBAS1 and LBAS0 bits to the default value (00B). Otherwise, the operation will not be guaranteed.

Caution 3. Only the combinations of display waveform, number of time slices, and bias method shown in Table 23 - 6 are supported.
Combinations of settings not shown in Table 23 - 6 are prohibited.

Table 23 - 6 Combinations of Display Waveform, Time Slices, Bias Method, and Frame Frequency

Display Mode			Set Value						Driving Voltage Generation Method		
Display Waveform	Number of Time Slices	Bias Mode	LWAVE	LDTY2	LDTY1	LDTY0	LBAS1	LBAS0	External Resistance Division	Internal Voltage Boosting	Capacitor Split
Waveform A	8	1/4	0	1	0	1	1	0	√ (24 to 128 Hz)	√ (24 to 64 Hz)	×
Waveform A	6	1/4	0	1	0	0	1	0	×	√ (32 to 86 Hz)	×
Waveform A	8	1/3	0	1	0	1	0	1	√ (32 to 128 Hz)	√ (32 to 64 Hz)	√ (32 to 128 Hz)
Waveform A	6	1/3	0	1	0	0	0	1	√ (32 to 128 Hz)	√ (32 to 86 Hz)	√ (32 to 128 Hz)
Waveform A	4	1/3	0	0	1	1	0	1	√ (24 to 128 Hz)	√ (24 to 128 Hz)	√ (24 to 128 Hz)
Waveform A	3	1/3	0	0	1	0	0	1	√ (32 to 128 Hz)	√ (32 to 128 Hz)	√ (32 to 128 Hz)
Waveform A	3	1/2	0	0	1	0	0	0	√ (32 to 128 Hz)	×	×
Waveform A	2	1/2	0	0	0	1	0	0	√ (24 to 128 Hz)	×	×
Waveform A	Static		0	0	0	0	0	0	√ (24 to 128 Hz)	×	×
Waveform B	8	1/4	1	1	0	1	1	0	√ (24 to 128 Hz)	√ (24 to 64 Hz)	×
Waveform B	8	1/3	1	1	0	1	0	1	√ (32 to 128 Hz)	v (32 to 64 Hz)	√ (32 to 128 Hz)
Waveform B	6	1/3	1	1	0	0	0	1	√ (32 to 128 Hz)	√ (32 to 86 Hz)	√ (32 to 128 Hz)
Waveform B	4	1/3	1	0	1	1	0	1	√ (24 to 128 Hz)	√ (24 to 128 Hz)	√ (24 to 128 Hz)
Waveform B	3	1/3	1	0	1	0	0	1	√ (32 to 128 Hz)	√ (32 to 128 Hz)	√ (32 to 128 Hz)

Remark √: Supported
×: Not supported

23.3.2 LCD mode register 1 (LCDM1)

LCDM1 enables or disables display operation, voltage boost circuit operation, and capacitor split circuit operation, and specifies the display data area and the low voltage mode.

LCDM1 is set using a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets LCDM1 to 00H.

Figure 23 - 3 Format of LCD Mode Register 1 (LCDM1) (1/2)

Address: FFF41H After reset: 00H R/W

Symbol	<7>	<6>	<5>	<4>	<3>	2	1	<0>
LCDM1	LCDON	SCOC	VLCON	BLON	LCDSEL	0	0	LCDVLM

SCOC	LCDON	LCD display enable/disable
0	0	Output ground level to segment/common pin
0	1	
1	0	Display off (all segment outputs are deselected.)
1	1	Display on

VLCON Note 1	Voltage boost circuit or capacitor split circuit operation enable/disable
0	Stops voltage boost circuit or capacitor split circuit operation
1	Enables voltage boost circuit or capacitor split circuit operation

BLON Note 2	LCDSEL	Display data area control
0	0	Displaying an A-pattern area data (lower four bits of LCD display data register)
0	1	Displaying a B-pattern area data (higher four bits of LCD display data register)
1	0	Alternately displaying A-pattern and B-pattern area data (blinking display corresponding to the constant-period interrupt (INTRTC) timing of the real-time clock 2 (RTC2))
1	1	

Note 1. Cannot be set during external resistance division mode.

Note 2. When f_{IL} is selected as the LCD source clock (f_{LCD}), be sure to set the BLON bit to “0”.

(**Cautions** are listed on the next page.)

Figure 23 - 3 Format of LCD Mode Register 1 (LCDM1) (2/2)

Address: FFF41H After reset: 00H R/W

Symbol	<7>	<6>	<5>	<4>	<3>	2	1	<0>
LCDM1	LCDON	SCOC	VLCON	BLON	LCDSEL	0	0	LCDVLM

LCDVLM Note	Control of default value of voltage boosting pin
0	Set when $V_{DD} \geq 2.7$ V
1	Set when $V_{DD} \leq 4.2$ V

Note This function is used to shorten the boost stabilization time by setting the V_{Lx} pin to the default status when the voltage boost circuit is used. If the V_{DD} voltage is 2.7 V or higher when boosting is started, set the LCDVLM bit to “0”; if the V_{DD} voltage is 4.2 V or less, set the LCDVLM bit to “1”. However, when 2.7 V ≤ V_{DD} ≤ 4.2 V, operation is possible with LCDVLM = 0 or LCDVLM = 1.

Caution 1. When the voltage boost circuit is used, set SCOC = 0 and VLCON = 0, and MDSET1, MDSET0 = 00 in order to reduce power consumption when the LCD is not used. When MDSET1, MDSET0 = 01, power is consumed by the internal reference voltage generator.

Caution 2. When the external resistance division method has been set (MDSET1 and MDSET0 of LCDM0 = 00B) or capacitor split method has been set (MDSET1 and MDSET0 = 10B), set the LCDVLM bit to 0.

Caution 3. Do not rewrite the VLCON and LCDVLM bits while SCOC = 1.

Caution 4. Set the BLON and LCDSEL bits to 0 when 8 has been selected as the number of time slices for the display mode.

Caution 5. To use the internal voltage boosting method, specify the reference voltage by using the VLCD register (select the internal boosting method (by setting the MDSET1 and MDSET0 bits of the LCDM0 register to 01B) if the default reference voltage is used), wait for the reference voltage setup time (5 ms (min.)), and then set the VLCON bit to 1.

23.3.3 Subsystem clock supply option control register (OSMC)

This register is used to reduce power consumption by stopping unnecessary clock functions.

If the RTCLPC bit is set to 1, power consumption can be reduced, because clock supply to the peripheral functions, except the real-time clock 2, 12-bit interval timer, 8-bit interval timer, clock output/buzzer output, LCD controller/driver, serial interface UARTMG0, external signal sampler, and sampling output timer detector is stopped in STOP mode or HALT mode while sub clock (f_{SUB}) is selected as CPU clock.

In addition, the OSMC register can be used to select the count clock of the real-time clock 2, 12-bit interval timer, and 8-bit interval timer, and the operation clock of the clock output/buzzer output, LCD controller/driver, serial interface UARTMG0, external signal sampler, sampling output timer detector, and timers RJ0 and RJ1.

The low-speed on-chip oscillator clock cannot be selected as the operation clock for the serial interface UARTMG0, external signal sampler, and sampling output timer detector. When the serial interface UARTMG0, external signal sampler, and sampling output timer detector are used, set the WUTMMCK0 bit to 0 and select the subsystem clock as the operation clock.

The OSMC register can be set by an 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 23 - 4 Format of Subsystem clock supply mode control register (OSMC)

Address: F00F3H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
OSMC	RTCLPC	0	0	WUTMMCK0	0	0	0	0

RTCLPC	Setting in STOP mode or HALT mode while subsystem clock is selected as CPU clock
0	Enables subsystem clock supply to peripheral functions. (See **Table 27 - 1** to **Table 27 - 3** for the peripheral functions whose operations are enabled.)
1	Stops subsystem clock supply to peripheral functions except real-time clock 2, 12-bit interval timer, 8-bit interval timer, clock output/buzzer output, LCD controller/driver, serial interface UARTMG0, external signal sampler, and sampling output timer detector.

WUTMMCK0 Note	Selection of operation clock for real-time clock 2, 12-bit interval timer, 8-bit interval timer, LCD controller/driver, and timers RJ0 and RJ1	Selection of clock output from PCLBUZn pin of clock output/buzzer output
0	Subsystem clock (f_{SUB}) • The subsystem clock is selected as the operation clock for the real-time clock 2, 12-bit interval timer, 8-bit interval timer, and LCD controller/driver. • The low-speed on-chip oscillator cannot be selected as the count source for timers RJ0 and RJ1.	Selecting the subsystem clock (f_{SUB}) is enabled.
1	Low-speed on-chip oscillator clock (f_{IL}) • The low-speed on-chip oscillator clock is selected as the operation clock for the real-time clock 2, 12-bit interval timer, 8-bit interval timer, and LCD controller/driver. • Either the low-speed on-chip oscillator or subsystem clock can be selected as the count source for timers RJ0 an RJ1.	Selecting the subsystem clock (f_{SUB}) is disabled.

Note Be sure to select the subsystem clock (WUTMMCK0 bit = 0) if the subsystem clock is oscillating.

Caution The subsystem clock and low-speed on-chip oscillator clock can only be switched by using the WUTMMCK0 bit if the real-time clock 2, 12-bit interval timer, 8-bit interval timer, and LCD controller/driver are all stopped.

23.3.4 LCD clock control register 0 (LCDC0)

LCDC0 specifies the LCD source clock and LCD clock.

The frame frequency is determined according to the LCD clock and the number of time slices.

This register is set by using an 8-bit memory manipulation instruction.

Reset signal generation sets LCDC0 to 00H.

Figure 23 - 5 Format of LCD Clock Control Register 0 (LCDC0)

Address: FFF42H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
LCDC0	0	0	LCDC05	LCDC04	LCDC03	LCDC02	LCDC01	LCDC00

LCDC05	LCDC04	LCDC03	LCDC02	LCDC01	LCDC00	LCD clock (LCDCL)
0	0	0	1	0	0	$f_{SUB}/2^5$ or $f_{IL}/2^5$
0	0	0	1	0	1	$f_{SUB}/2^6$ or $f_{IL}/2^6$
0	0	0	1	1	0	$f_{SUB}/2^7$ or $f_{IL}/2^7$
0	0	0	1	1	1	$f_{SUB}/2^8$ or $f_{IL}/2^8$
0	0	1	0	0	0	$f_{SUB}/2^9$ or $f_{IL}/2^9$
0	0	1	0	0	1	$f_{SUB}/2^{10}$
0	1	0	0	0	1	$f_{MAIN}/2^8$
0	1	0	0	1	0	$f_{MAIN}/2^9$
0	1	0	0	1	1	$f_{MAIN}/2^{10}$
0	1	0	1	0	0	$f_{MAIN}/2^{11}$
0	1	0	1	0	1	$f_{MAIN}/2^{12}$
0	1	0	1	1	0	$f_{MAIN}/2^{13}$
0	1	0	1	1	1	$f_{MAIN}/2^{14}$
0	1	1	0	0	0	$f_{MAIN}/2^{15}$
0	1	1	0	0	1	$f_{MAIN}/2^{16}$
0	1	1	0	1	0	$f_{MAIN}/2^{17}$
0	1	1	0	1	1	$f_{MAIN}/2^{18}$
1	0	1	0	1	1	$f_{MAIN}/2^{19}$
Other than above						Setting prohibited

Caution 1. Do not set LCDC0 when the SCOC bit of the LCDM1 register is 1.

Caution 2. Be sure to set bits 6 and 7 to "0".

Caution 3. When the internal boosting method or capacitance division method is set, set the LCD clock (LCDCL) as follows:

- **512 Hz or less when f_{SUB} is selected.**
- **235 Hz or less when f_{IL} is selected.**

For details, see Table 23 - 6 Combinations of Display Waveform, Time Slices, Bias Method, and Frame Frequency.

Remark f_{MAIN}: Main system clock frequency
f_{SUB}: Subsystem clock frequency
f_{IL}: Low-speed on-chip oscillator clock frequency

23.3.5 LCD boost level control register (VLCD)

VLCD selects the reference voltage that is to be generated when operating the voltage boost circuit (contrast adjustment). The reference voltage can be selected from 16 steps.

This register is set by using an 8-bit memory manipulation instruction.

Reset signal generation sets VLCD to 04H.

Figure 23 - 6 Format of LCD Boost Level Control Register (VLCD)

Address: FFF43H After reset: 04H R/W

Symbol	7	6	5	4	3	2	1	0
VLCD	0	0	0	VLCD4	VLCD3	VLCD2	VLCD1	VLCD0

VLCD4	VLCD3	VLCD2	VLCD1	VLCD0	Reference voltage selection (contrast adjustment)	V_{L4} voltage	
						1/3 bias method	1/4 bias method
0	0	1	0	0	1.00 V	3.00 V	4.00 V
0	0	1	0	1	1.05 V	3.15 V	4.20 V
0	0	1	1	0	1.10 V	3.30 V	4.40 V
0	0	1	1	1	1.15 V	3.45 V	4.60 V
0	1	0	0	0	1.20 V	3.60 V	4.80 V
0	1	0	0	1	1.25 V	3.75 V	5.00 V
0	1	0	1	0	1.30 V	3.90 V	5.20 V
0	1	0	1	1	1.35 V	4.05 V	Setting prohibited
0	1	1	0	0	1.40 V	4.20 V	Setting prohibited
0	1	1	0	1	1.45 V	4.35 V	Setting prohibited
0	1	1	1	0	1.50 V	4.50 V	Setting prohibited
0	1	1	1	1	1.55 V	4.65 V	Setting prohibited
1	0	0	0	0	1.60 V	4.80 V	Setting prohibited
1	0	0	0	1	1.65 V	4.95 V	Setting prohibited
1	0	0	1	0	1.70 V	5.10 V	Setting prohibited
1	0	0	1	1	1.75 V	5.25 V	Setting prohibited
Other than above					Setting prohibited		

(**Cautions** are listed on the next page.)

Caution 1. The VLCD setting is valid only when the voltage boost circuit is operating.

Caution 2. Be sure to set bits 5 to 7 to "0".

Caution 3. Be sure to change the VLCD value after having stopped the operation of the voltage boost circuit (VLCON = 0).

Caution 4. To use the internal voltage boosting method, specify the reference voltage by using the VLCD register (select the internal boosting method (by setting the MDSET1 and MDSET0 bits of the LCDM0 register to 01B) if the default reference voltage is used), wait for the reference voltage setup time (5 ms (min.)), and then set VLCON to 1.

Caution 5. To use the external resistance division method or capacitor split method, use the VLCD register with its initial value (04H).

23.3.6 LCD input switch control register (ISCLCD)

Input to the Schmitt trigger buffer must be disabled until the CAPL/P126, CAPH/P127, and V_{L3}/P125 pins are set to operate as LCD function pins in order to prevent through-current from entering.

This register is set by using a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets ISCLCD to 00H.

Figure 23 - 7 Format of LCD Input Switch Control Register (ISCLCD)

Address: F0308H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
ISCLCD	0	0	0	0	0	0	ISCVL3	ISCCAP

ISCVL3	V_{L3}/P125 pin Schmitt trigger buffer control
0	Input invalid
1	Input valid

ISCCAP	CAPL/P126, CAPH/P127 pins Schmitt trigger buffer control
0	Input invalid
1	Input valid

Caution 1. If ISCVL3 = 0, set the corresponding port registers as follows:
PU125 bit of PU12 register = 0, P125 bit of P12 register = 0

Caution 2. If ISCCAP = 0, set the corresponding port registers as follows:
PU126 bit of PU12 register = 0, P126 bit of P12 register = 0
PU127 bit of PU12 register = 0, P127 bit of P12 register = 0

(1) Operation of ports that alternately function as V_{L3}, CAPL, and CAPH pins

The functions of the V_{L3}/P125, CAPL/P126, and CAPH/P127 pins can be selected by using the LCD input switch control register (ISCLCD), LCD mode register 0 (LCDM0), and port mode register 12 (PM12).

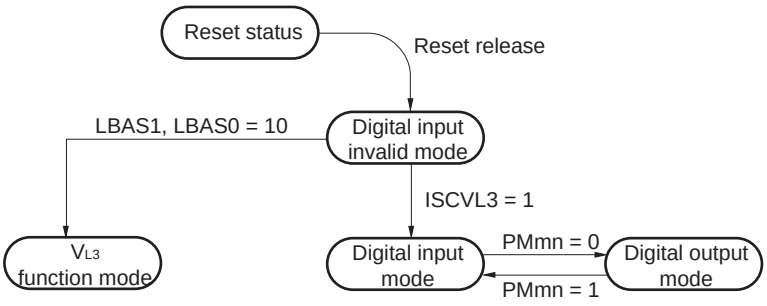
- **VL3/P125**

Table 23 - 7 Settings of V_{L3}/P125 Pin Function

Bias Setting (LBAS1 and LBAS0 Bits of LCDM0 Register)	ISCVL3 Bit of ISCLCD Register	PM125 Bit of PM12 Register	Pin Function	Initial Status
Other than 1/4 bias method (LBAS1, LBAS0 = 00 or 01)	0	1	Digital input invalid mode	√
	1	0	Digital output mode	—
	1	1	Digital input mode	—
1/4 bias method (LBAS1, LBAS0 = 10)	0	1	V_{L3} function mode	—
Other than above			Setting prohibited	

The following shows the V_{L3}/P125 pin function status transitions.

Figure 23 - 8 V_{L3}/P125 Pin Function Status Transitions



Caution Be sure to set the V_{L3} function mode before segment output starts (while SCOC bit of LCD mode register 1 (LCDM1) is 0).

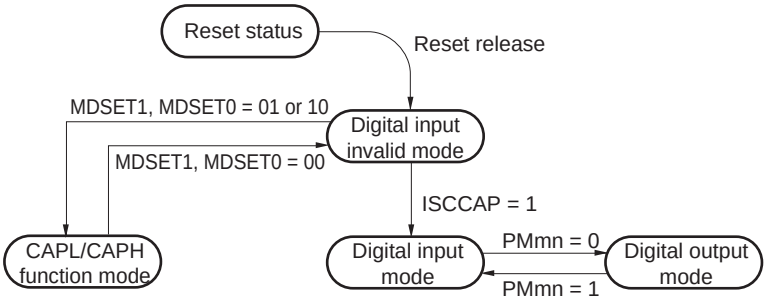
- **CAPL/P126 and CAPH/P127**

Table 23 - 8 Settings of CAPL/P126 and CAPH/P127 Pin Functions

LCD Drive Voltage Generator (MDSET1 and MDSET0 Bits of LCDM0 Register)	ISCCAP Bit of ISCLCD Register	PM126 and PM127 Bits of PM12 Register	Pin Function	Initial Status
External resistance division (MDSET1, MDSET0 = 00)	0	1	Digital input invalid mode	√
	1	0	Digital output mode	—
	1	1	Digital input mode	—
Internal voltage boosting or capacitor split (MDSET1, MDSET0 = 01 or 10)	0	1	CAPL/CAPH function mode	—
Other than above			Setting prohibited	

The following shows the CAPL/P126 and CAPH/P127 pin function status transitions.

Figure 23 - 9 CAPL/P126 and CAPH/P127 Pin Function Status Transitions



Caution Be sure to set the CAPL/CAPH function mode before segment output starts (while SCOC bit of LCD mode register 1 (LCDM1) is 0).

23.3.7 LCD port function registers 0 to 4 (PFSEG0 to PFSEG4)

These registers specify whether to use pins P01 to P07, P10 to P16, P30 to P32, P35 to P37, P50 to P53, and P70 to P77 as port pins (other than segment output pins) or segment output pins.
These registers are set by using a 1-bit or 8-bit memory manipulation instruction.
Reset signal generation sets these registers to FFH (PFSEG0 is F0H, PFSEG4 is 0FH).

Remark The correspondence between the segment output pins (SEGxx) and the PFSEG register (PFSEGxx bits) and the existence of SEGxx pins in each product are shown in Table 23 - 9 Segment Output Pins in Each Product and Correspondence with PFSEG Register (PFSEG Bits).

Figure 23 - 10 Format of LCD Port Function Registers 0 to 4 (R5F11NM)

Address: F0300H After reset: F0H R/W

Symbol	7	6	5	4	3	2	1	0
PFSEG0	PFSEG07	PFSEG06	PFSEG05	PFSEG04	0	0	0	0

Address: F0301H After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
PFSEG1	PFSEG15	PFSEG14	PFSEG13	PFSEG12	PFSEG11	PFSEG10	PFSEG09	PFSEG08

Address: F0302H After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
PFSEG2	PFSEG23	PFSEG22	PFSEG21	PFSEG20	PFSEG19	PFSEG18	PFSEG17	PFSEG16

Address: F0303H After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
PFSEG3	PFSEG31	PFSEG30	PFSEG29	PFSEG28	PFSEG27	PFSEG26	PFSEG25	PFSEG24

Address: F0304H After reset: 0FH R/W

Symbol	7	6	5	4	3	2	1	0
PFSEG4	0	0	0	0	PFSEG35	PFSEG34	PFSEG33	PFSEG32

PFSEGxx (xx = 04 to 35)	Port (other than segment output)/segment outputs specification of Pmn pins (mn = 01 to 07, 10 to 16, 30 to 32, 35 to 37, 50 to 53, 70 to 77)
0	Used as port (other than segment output)
1	Used as segment output

Caution To use the Pmn pins as segment output pins (PFSEGxx = 1), be sure to set the PUmn bit of the PUm register, POMmn bit of the POMm register, and PIMmn bit of the PIMm register to "0".

Table 23 - 9 Segment Output Pins in Each Product and Correspondence with PFSEG Register (PFSEG Bits)

Bit name of PFSEG register	Corresponding SEGxx pins	Alternate port	R5F11NM	R5F11NL	R5F11RM
PFSEG04	SEG4	P53	√	—	√
PFSEG05	SEG5	P52	√	√	√
PFSEG06	SEG6	P51	√	√	√
PFSEG07	SEG7	P50	√	√	√
PFSEG08	SEG8	P70	√	√	√
PFSEG09	SEG9	P71	√	√	√
PFSEG10	SEG10	P72	√	—	√
PFSEG11	SEG11	P73	√	—	√
PFSEG12	SEG12	P74	√	—	√
PFSEG13	SEG13	P75	√	—	√
PFSEG14	SEG14	P76	√	√	√
PFSEG15	SEG15	P77	√	√	√
PFSEG16	SEG16	P30	√	√	√
PFSEG17	SEG17	P31	√	√	√
PFSEG18	SEG18	P32	√	√	√
PFSEG19	SEG19	P35	√	√	√
PFSEG20	SEG20	P36	√	√	√
PFSEG21	SEG21	P37	√	√	√
PFSEG22	SEG22	P01	√	—	√
PFSEG23	SEG23	P02	√	—	√
PFSEG24	SEG24	P03	√	√	√
PFSEG25	SEG25	P04	√	—	√
PFSEG26	SEG26	P05	√	√	√
PFSEG27	SEG27	P06	√	√	√
PFSEG28	SEG28	P07	√	√	√
PFSEG29	SEG29	P10	√	√	√
PFSEG30	SEG30	P11	√	√	√
PFSEG31	SEG31	P12	√	√	√
PFSEG32	SEG32	P13	√	√	√
PFSEG33	SEG33	P14	√	√	√
PFSEG34	SEG34	P15	√	√	√
PFSEG35	SEG35	P16	√	—	√

(1) Operation of ports that alternately function as SEGxx pins

The functions of ports that also serve as segment output pins (SEGxx) can be selected by using the port mode register (PMxx), port mode control register (PMCxx) and LCD port function registers 0 to 4 (PFSEG0 to PFSEG4).

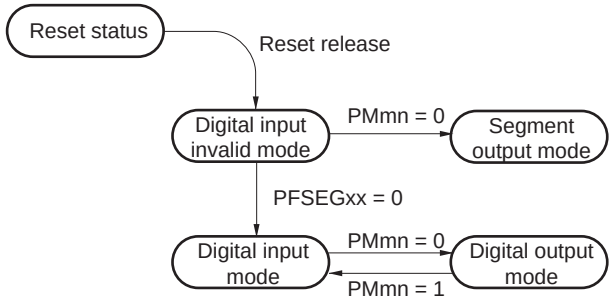
- **P01 to P07, P10 to P16, P30 to P32, P35 to P37, P50 to P53, P70 to P77 (ports that do not serve as analog input pins (ANIxx))**

Table 23 - 10 Settings of SEGxx/Port Pin Function

PFSEGxx Bit of PFSEG0 to PFSEG4 Registers	PMxx Bit of PMxx Register	Pin Function	Initial Status
1	1	Digital input invalid mode	√
0	0	Digital output mode	—
0	1	Digital input mode	—
1	0	Segment output mode	—

The following shows the SEGxx/Pxx pin function status transitions.

Figure 23 - 11 SEGxx/Pxx Pin Function Status Transitions



Caution Be sure to set the segment output mode before segment output starts (while SCOC bit of LCD mode register 1 (LCDM1) is 0).

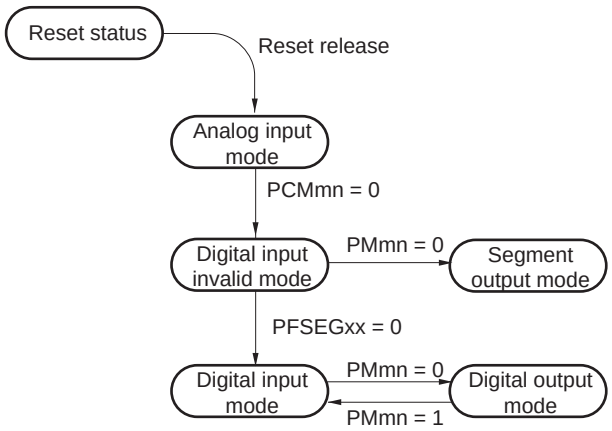
P03 to P05, P11 (ports that serves as analog input pins (ANIxx))

Table 23 - 11 Settings of ANIxx/SEGxx/Port Pin Function

PMCxx Bit of PMCxx Register	PFSEG3 Bit of PFSEGxx Register	PMxx Bit of PMxx Register	Pin Function	Initial Status
1	1	1	Analog input mode	√
0	0	0	Digital output mode	—
0	0	1	Digital input mode	—
0	1	0	Segment output mode	—
0	1	1	Digital input invalid mode	—
Other than above			Setting prohibited	

The following shows the ANIxx/SEGxx/Pxx pin function status transitions.

Figure 23 - 12 ANIxx/SEGxx/Pxx Pin Function Status Transitions



Caution Be sure to set the segment output mode before segment output starts (while SCOC bit of LCD mode register 1 (LCDM1) is 0).

23.3.8 Registers that control port functions of segment output pins

Using the segment output requires setting of the registers that control the port functions for the port pins with which the segment output pin functions for the target channel are multiplexed (port mode register (PMxx), port register (Pxx), and port mode control register (PMCxx)).
For details, see **4.4.1 Port mode registers (PMxx)**, **4.4.2 Port registers (Pxx)**, and **4.4.6 Port mode control registers (PMCxx)**.
The port mode register (PMxx), port register (Pxx), and port mode control register (PMCxx) to be set depend on the product. For details, see **4.6 Register Settings When Using Alternate Function**.

Using a port pin (e.g. P01/(INTP5)/SEG22) on which an analog input pin function (ANIxx) is not multiplexed but a segment output pin function is multiplexed for segment output requires setting the corresponding bits in the port mode control register (PMCxx), port mode register (PMxx), and port register (Pxx) to 0.

Example: When P01/(INTP5)/SEG22 is to be used for segment output
Set PM01 bit of port mode register 0 to 0.
Set P01 bit of port register 0 to 0.

Using a port pin (e.g. P03/ANI8/TO00/SEG24) on which both analog input pin (ANIxx) and segment output pin functions are multiplexed for segment output requires setting the corresponding bits in the port mode control register (PMCxx), port mode register (PMxx), and port register (Pxx) to 0.

Example: When P03/ANI8/TO00/SEG24 is to be used for segment output
Set PMC03 bit of port mode control register 0 to 0.
Set PM03 bit of port mode register 0 to 0.
Set P03 bit of port register 0 to 0.

23.4 LCD Display Data Registers

The LCD display data registers are mapped as shown in Table 23 - 12. The contents displayed on the LCD can be changed by changing the contents of the LCD display data registers.

Table 23 - 12 Relationship Between LCD Display Data Register Contents and Segment/Common Outputs (1/2)

(a) Other than 6-time slice and 8-time slice (static, 2-time slice, 3-time slice, and 4-time slice)

Register Name	Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	R5F11NM	R5F11NL	R5F11RM
		COM7	COM6	COM5	COM4	COM3	COM2	COM1	COM0			
SEG0	F0400H	SEG0 (B-pattern area)				SEG0 (A-pattern area)				√	√	√
SEG1	F0401H	SEG1 (B-pattern area)				SEG1 (A-pattern area)				√	√	√
SEG2	F0402H	SEG2 (B-pattern area)				SEG2 (A-pattern area)				√	√	√
SEG3	F0403H	SEG3 (B-pattern area)				SEG3 (A-pattern area)				√	√	√
SEG4	F0404H	SEG4 (B-pattern area)				SEG4 (A-pattern area)				√	—	√
SEG5	F0405H	SEG5 (B-pattern area)				SEG5 (A-pattern area)				√	√	√
SEG6	F0406H	SEG6 (B-pattern area)				SEG6 (A-pattern area)				√	√	√
SEG7	F0407H	SEG7 (B-pattern area)				SEG7 (A-pattern area)				√	√	√
SEG8	F0408H	SEG8 (B-pattern area)				SEG8 (A-pattern area)				√	√	√
SEG9	F0409H	SEG9 (B-pattern area)				SEG9 (A-pattern area)				√	√	√
SEG10	F040AH	SEG10 (B-pattern area)				SEG10 (A-pattern area)				√	—	√
SEG11	F040BH	SEG11 (B-pattern area)				SEG11 (A-pattern area)				√	—	√
SEG12	F040CH	SEG12 (B-pattern area)				SEG12 (A-pattern area)				√	—	√
SEG13	F040DH	SEG13 (B-pattern area)				SEG13 (A-pattern area)				√	—	√
SEG14	F040EH	SEG14 (B-pattern area)				SEG14 (A-pattern area)				√	√	√
SEG15	F040FH	SEG15 (B-pattern area)				SEG15 (A-pattern area)				√	√	√
SEG16	F0410H	SEG16 (B-pattern area)				SEG16 (A-pattern area)				√	√	√
SEG17	F0411H	SEG17 (B-pattern area)				SEG17 (A-pattern area)				√	√	√
SEG18	F0412H	SEG18 (B-pattern area)				SEG18 (A-pattern area)				√	√	√
SEG19	F0413H	SEG19 (B-pattern area)				SEG19 (A-pattern area)				√	√	√
SEG20	F0414H	SEG20 (B-pattern area)				SEG20 (A-pattern area)				√	√	√
SEG21	F0415H	SEG21 (B-pattern area)				SEG21 (A-pattern area)				√	√	√
SEG22	F0416H	SEG22 (B-pattern area)				SEG22 (A-pattern area)				√	—	√
SEG23	F0417H	SEG23 (B-pattern area)				SEG23 (A-pattern area)				√	—	√
SEG24	F0418H	SEG24 (B-pattern area)				SEG24 (A-pattern area)				√	√	√
SEG25	F0419H	SEG25 (B-pattern area)				SEG25 (A-pattern area)				√	—	√
SEG26	F041AH	SEG26 (B-pattern area)				SEG26 (A-pattern area)				√	√	√
SEG27	F041BH	SEG27 (B-pattern area)				SEG27 (A-pattern area)				√	√	√
SEG28	F041CH	SEG28 (B-pattern area)				SEG28 (A-pattern area)				√	√	√
SEG29	F041DH	SEG29 (B-pattern area)				SEG29 (A-pattern area)				√	√	√
SEG30	F041EH	SEG30 (B-pattern area)				SEG30 (A-pattern area)				√	√	√
SEG31	F041FH	SEG31 (B-pattern area)				SEG31 (A-pattern area)				√	√	√
SEG32	F0420H	SEG32 (B-pattern area)				SEG32 (A-pattern area)				√	√	√
SEG33	F0421H	SEG33 (B-pattern area)				SEG33 (A-pattern area)				√	√	√
SEG34	F0422H	SEG34 (B-pattern area)				SEG34 (A-pattern area)				√	√	√
SEG35	F0423H	SEG35 (B-pattern area)				SEG35 (A-pattern area)				√	—	√

Remark √: Supported, -: Not supported

Table 23 - 12 Relationship Between LCD Display Data Register Contents and Segment/Common Outputs (2/2)

(a) 6-time slice and 8-time slice

Register Name	Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	R5F11NM	R5F11NL	R5F11RM
		COM7	COM6	COM5	COM4	COM3	COM2	COM1	COM0			
SEG0	F0400H	SEG0 Note								√	√	√
SEG1	F0401H	SEG1 Note								√	√	√
SEG2	F0402H	SEG2 Note								√	√	√
SEG3	F0403H	SEG3 Note								√	√	√
SEG4	F0404H	SEG4								√	—	√
SEG5	F0405H	SEG5								√	√	√
SEG6	F0406H	SEG6								√	√	√
SEG7	F0407H	SEG7								√	√	√
SEG8	F0408H	SEG8								√	√	√
SEG9	F0409H	SEG9								√	√	√
SEG10	F040AH	SEG10								√	—	√
SEG11	F040BH	SEG11								√	—	√
SEG12	F040CH	SEG12								√	—	√
SEG13	F040DH	SEG13								√	—	√
SEG14	F040EH	SEG14								√	√	√
SEG15	F040FH	SEG15								√	√	√
SEG16	F0410H	SEG16								√	√	√
SEG17	F0411H	SEG17								√	√	√
SEG18	F0412H	SEG18								√	√	√
SEG19	F0413H	SEG19								√	√	√
SEG20	F0414H	SEG20								√	√	√
SEG21	F0415H	SEG21								√	√	√
SEG22	F0416H	SEG22								√	—	√
SEG23	F0417H	SEG23								√	—	√
SEG24	F0418H	SEG24								√	√	√
SEG25	F0419H	SEG25								√	—	√
SEG26	F041AH	SEG26								√	√	√
SEG27	F041BH	SEG27								√	√	√
SEG28	F041CH	SEG28								√	√	√
SEG29	F041DH	SEG29								√	√	√
SEG30	F041EH	SEG30								√	√	√
SEG31	F041FH	SEG31								√	√	√
SEG32	F0420H	SEG32								√	√	√
SEG33	F0421H	SEG33								√	√	√
SEG34	F0422H	SEG34								√	√	√
SEG35	F0423H	SEG35								√	—	√

Note The COM4 to COM7 pins and SEG0 to SEG3 pins are used alternatively.

Remark √: Supported, —: Not supported

To use the LCD display data register when the number of time slices is static, two, three, or four, the lower four bits and higher four bits of each address of the LCD display data register become an A-pattern area and a B-pattern area, respectively.

The correspondences between A-pattern area data and COM signals are as follows: bit 0 ↔ COM0, bit 1 ↔ COM1, bit 2 ↔ COM2, and bit 3 ↔ COM3.

The correspondences between B-pattern area data and COM signals are as follows: bit 4 ↔ COM0, bit 5 ↔ COM1, bit 6 ↔ COM2, and bit 7 ↔ COM3.

A-pattern area data will be displayed on the LCD panel when BLON = LCDSEL = 0 has been selected, and B-pattern area data will be displayed on the LCD panel when BLON = 0 and LCDSEL = 1 have been selected.

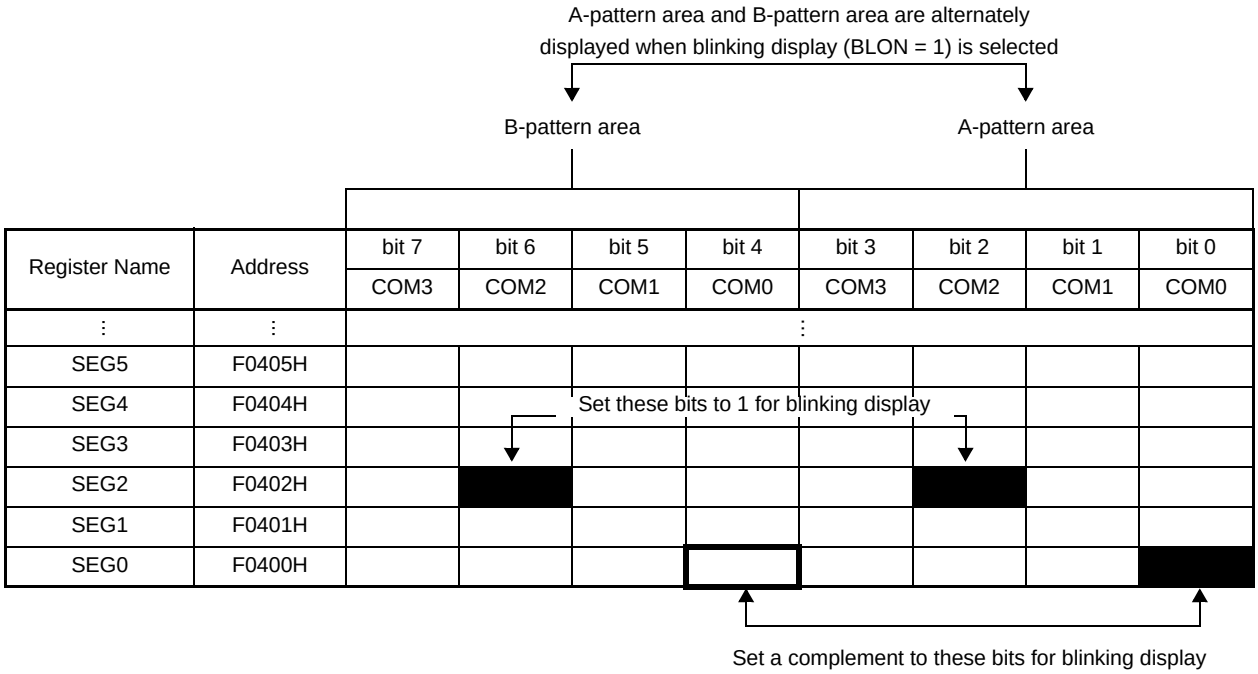
23.5 Selection of LCD Display Register

With RL78/H1D, to use the LCD display data registers when the number of time slices is static, two, three, or four, the LCD display data register can be selected from the following three types, according to the BLON and LCDSEL bit settings.

- Displaying an A-pattern area data (lower four bits of LCD display data register)
- Displaying a B-pattern area data (higher four bits of LCD display data register)
- Alternately displaying A-pattern and B-pattern area data (blinking display corresponding to the constant-period interrupt timing of the real-time clock 2 (RTC2))

Caution CautionWhen the number of time slices is six or eight, LCD display data registers (A-pattern, B-pattern, or blinking display) cannot be selected.

Figure 23 - 13 Example of Setting LCD Display Registers When Pattern Is Changed



23.5.1 A-pattern area and B-pattern area data display

When BLON = LCDSEL = 0, A-pattern area (lower four bits of the LCD display data register) data will be output as the LCD display register.

When BLON = 0, and LCDSEL = 1, B-pattern area (higher four bits of the LCD display data register) data will be output as the LCD display register.

See **23.4 LCD Display Data Registers** about the display area.

23.5.2 Blinking display (Alternately displaying A-pattern and B-pattern area data)

When BLON = 1 has been set, A-pattern and B-pattern area data will be alternately displayed, according to the constant-period interrupt (INTRTC) timing of the real-time clock 2 (RTC2). See **CHAPTER 8 REAL-TIME CLOCK 2** about the setting of the RTC2 constant-period interrupt (INTRTC, 0.5 s setting only) timing.

For blinking display of the LCD, set inverted values to the B-pattern area bits corresponding to the A-pattern area bits. (Example: Set 1 to bit 0 of F0400H, and set 0 to bit 4 of F0400H for blinking display.) When not setting blinking display of the LCD, set the same values. (Example: Set 1 to bit 2 of F0402H, and set 1 to bit 6 of F0402H for lighting display.)

See **23.4 LCD Display Data Registers** about the display area.

Next, the timing operation of display switching is shown.

Figure 23 - 14 Switching Operation from A-Pattern Display to Blinking Display

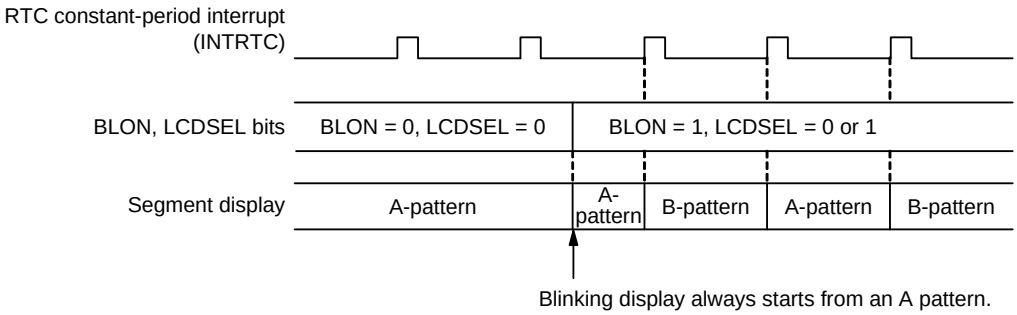
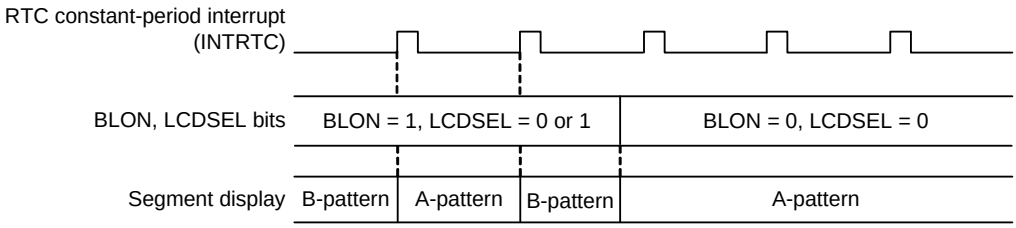


Figure 23 - 15 Switching Operation from Blinking Display to A-Pattern Display



23.6 Setting the LCD Controller/Driver

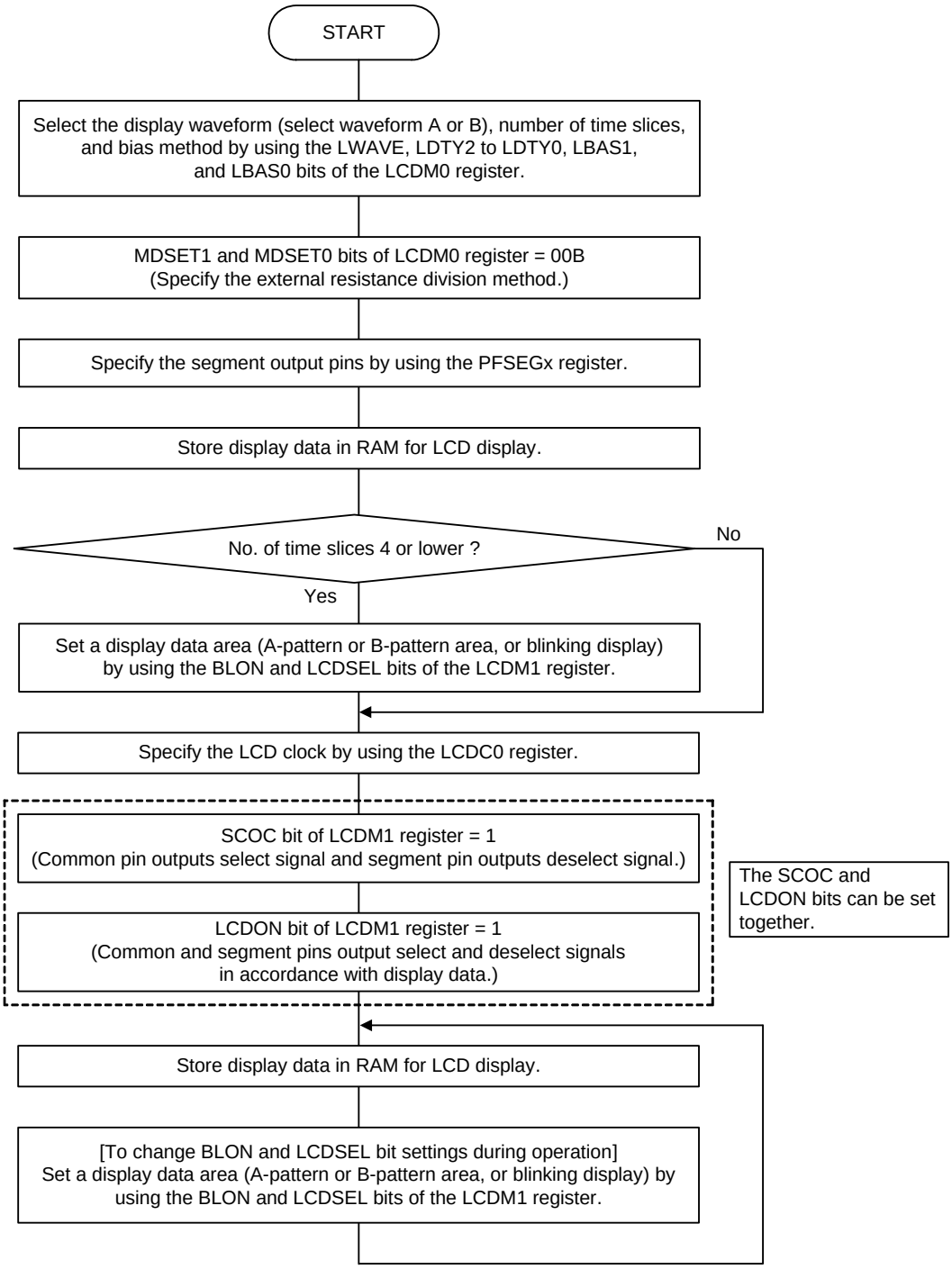
Set the LCD controller/driver using the following procedure.

Caution 1. To operate the LCD controller/driver, be sure to follow procedures (1) to (3). Unless these procedures are observed, the operation will not be guaranteed.

Caution 2. The steps shown in the flowcharts in (1) to (3) are performed by the CPU.

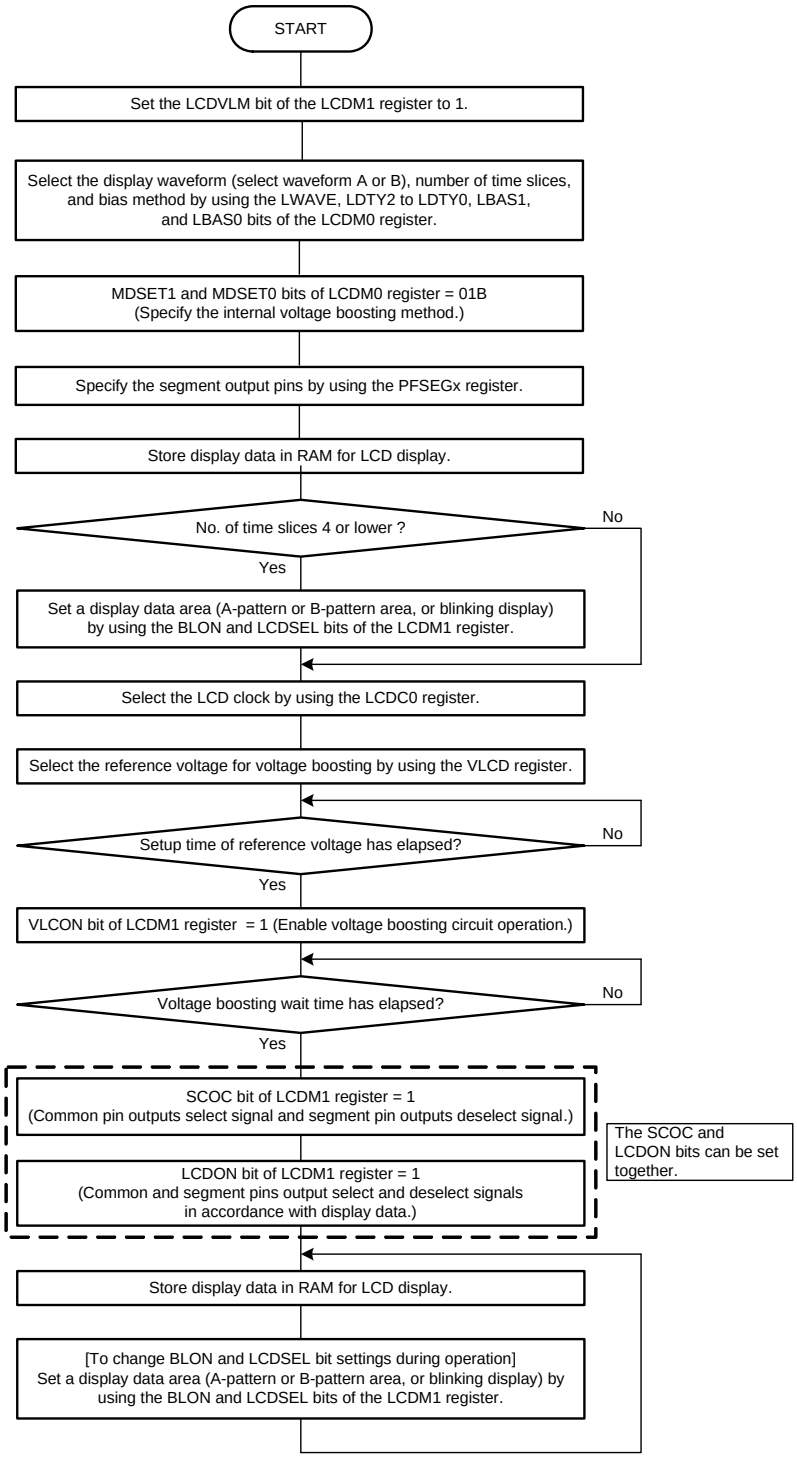
(1) External resistance division method

Figure 23 - 16 External Resistance Division Method Setting Procedure



(2) Internal voltage boosting method

Figure 23 - 17 Internal Voltage Boosting Method Setting Procedure

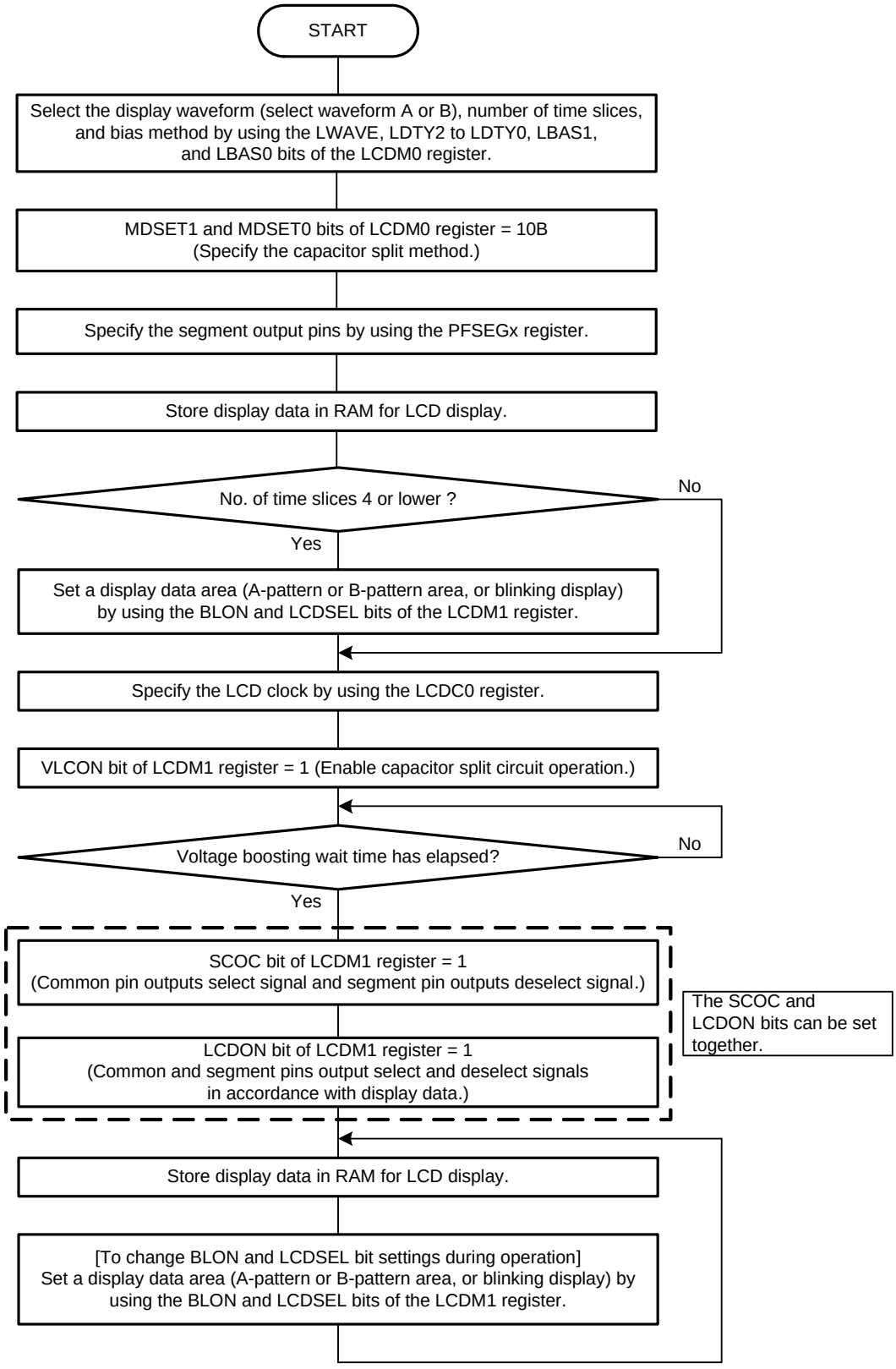


Caution 1. Wait until the setup time has elapsed even if not changing the setting of the VLCD register.

Caution 2. For the specifications of the reference voltage setup time and voltage boosting wait time, see CHAPTER 38 or CHAPTER 39 ELECTRICAL SPECIFICATIONS.

(3) Capacitor split method

Figure 23 - 18 Capacitor Split Method Setting Procedure



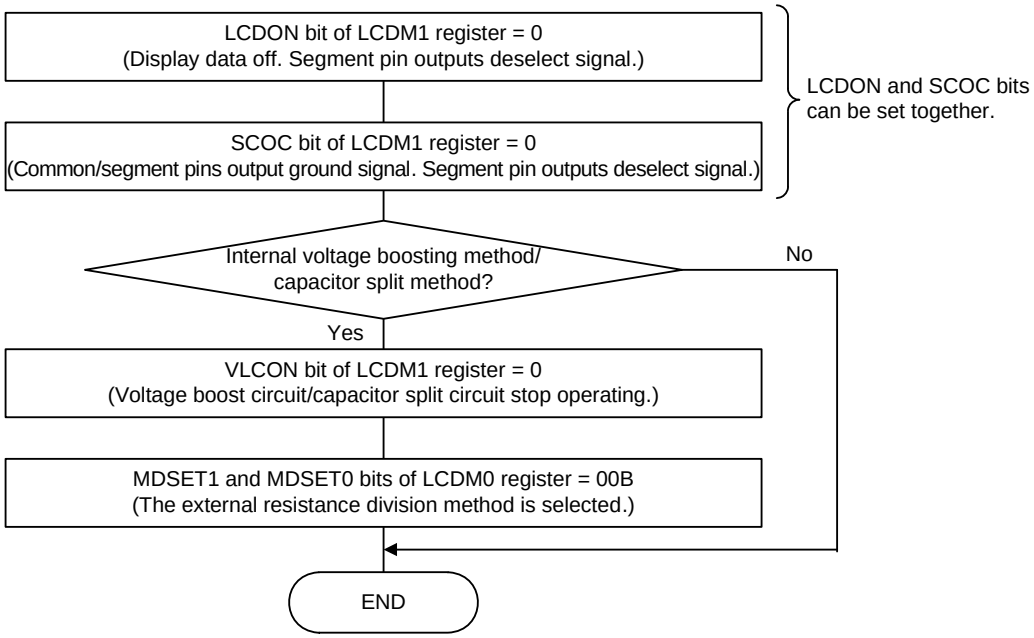
Caution For the specifications of the voltage boosting wait time, see CHAPTER 38 or CHAPTER 39 ELECTRICAL SPECIFICATIONS.

23.7 Operation Stop Procedure

To stop the operation of the LCD while it is displaying waveforms, follow the steps shown in the flowchart below.

The LCD stops operating when the LCDON bit of LCDM1 register and SCOC bit of the LCDM1 register are set to “0”.

Figure 23 - 19 Operation Stop Procedure



Caution **CautionStopping the voltage boost/capacitor split circuits is prohibited while the display is on (SCOC and LCDON bits of LCDM1 register = 11B). Otherwise, the operation will not be guaranteed. Be sure to turn off display (SCOC and LCDON bits of LCDM1 register = 00B) before stopping the voltage boost/capacitor split circuits (VLCON bit of LCDM1 register = 0).**

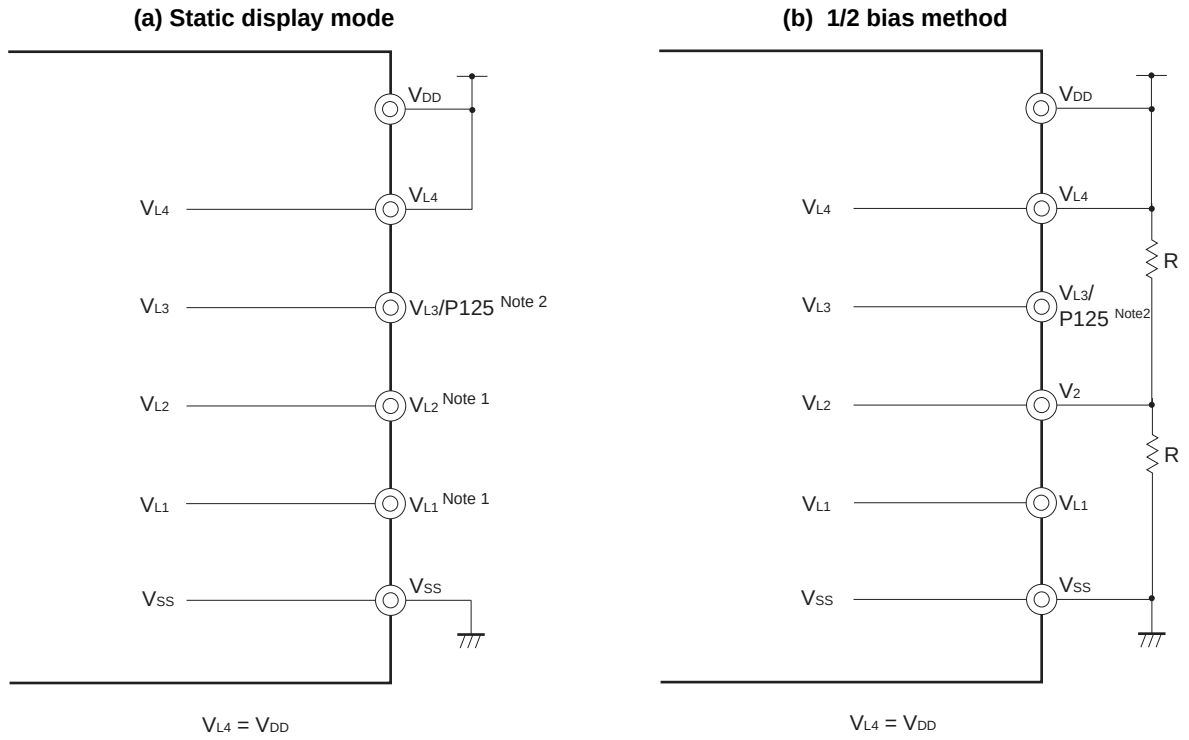
23.8 Supplying LCD Drive Voltages V_{L1}, V_{L2}, V_{L3}, and V_{L4}

The external resistance division method, internal voltage boosting method, and capacitor split method can be selected as LCD drive power generating method.

23.8.1 External resistance division method

Figure 23 - 20 shows examples of LCD drive voltage connection, corresponding to each bias method.

Figure 23 - 20 Examples of LCD Drive Power Connections (External Resistance Division Method) (1/2)

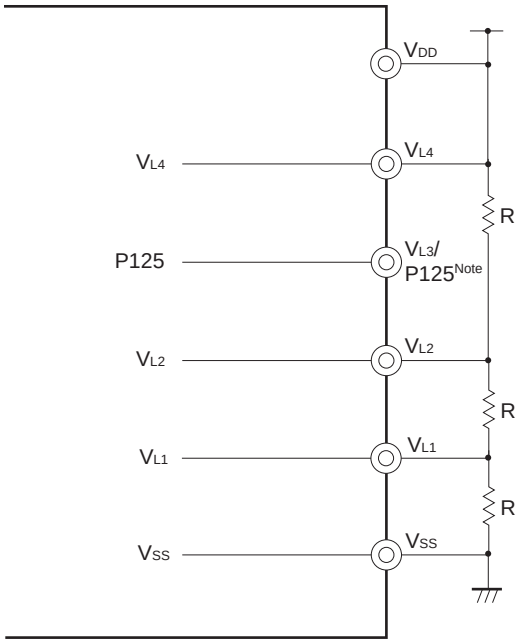


Note 1. Connect V_{L1} and V_{L2} to GND or leave open.

Note 2. V_{L3} can be used as port (P125).

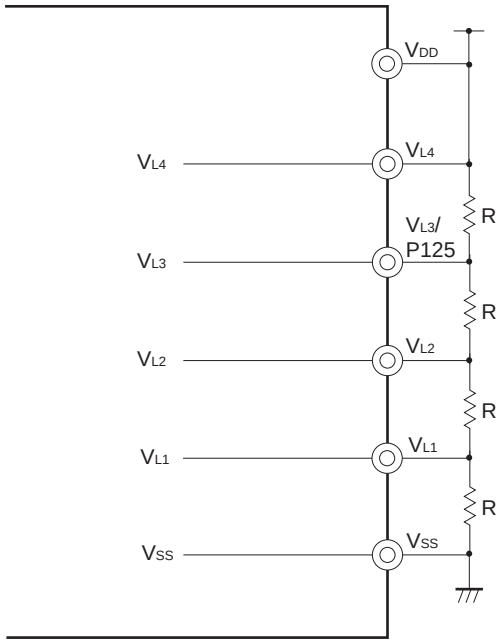
Figure 23 - 20 Examples of LCD Drive Power Connections (External Resistance Division Method) (2/2)

(c) 1/3 bias method



$V_{L4} = V_{DD}$

(d) 1/4 bias method



$V_{L4} = V_{DD}$

Note V_{L3} can be used as port (P125).

Caution The reference resistance "R" value for external resistance division is 10 kΩ to 1 MΩ. Also, to stabilize the potential of the V_{L1} to V_{L4} pins, connect a capacitor between each of pins V_{L1} to V_{L4} and the GND pin as needed. The reference capacitance is about 0.47 μF but it depends on the LCD panel used, the number of segment pins, the number of common pins, the frame frequency, and the operating environment. Thoroughly evaluate these values in accordance with your system and adjust and determine the capacitance.

23.8.2 Internal voltage boosting method

RL78/H1D contains an internal voltage boost circuit for generating LCD drive power supplies. The internal voltage boost circuit and external capacitors (0.47 μF±30%) are used to generate an LCD drive voltage. Only 1/3 bias mode or 1/4 bias mode can be set for the internal voltage boosting method.

The LCD drive voltage of the internal voltage boosting method can supply a constant voltage, regardless of changes in V_{DD}, because it is a power supply separate from the main unit.

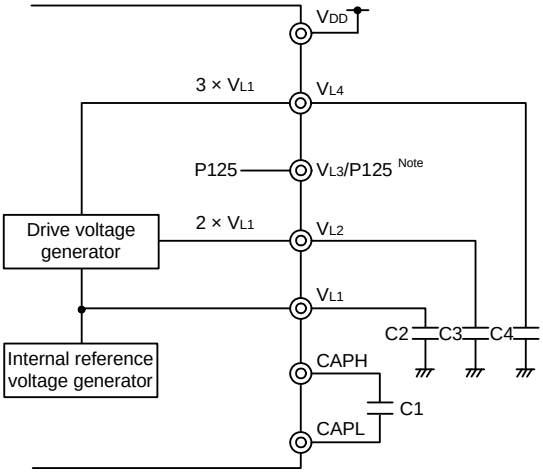
In addition, a contrast can be adjusted by using the LCD boost level control register (VLCD).

Table 23 - 13 LCD Drive Voltages (Internal Voltage Boosting Method)

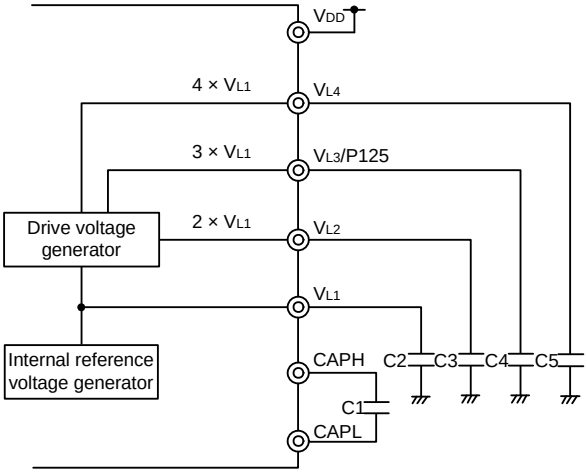
Bias Method / LCD Drive Voltage Pin	1/3 Bias Method	1/4 Bias Method
V_{L4}	3 × V_{L1}	4 × V_{L1}
V^{L3}	—	3 × V_{L1}
V_{L2}	2 × V_{L1}	2 × V_{L1}
V_{L1}	LCD reference voltage	LCD reference voltage

Figure 23 - 21 Examples of LCD Drive Power Connections (Internal Voltage Boosting Method)

(a) 1/3 bias method



(b) 1/4 bias method



Note V_{L3} can be used as port (P125).

Remark Use a capacitor with as little leakage as possible.
In addition, make C1 a nonpolar capacitor.

23.8.3 Capacitor split method

RL78/H1D contains an internal voltage reduction circuit for generating LCD drive power supplies. The internal voltage reduction circuit and external capacitors (0.47 μF±30%) are used to generate an LCD drive voltage. Only 1/3 bias mode can be set for the capacitor split method.

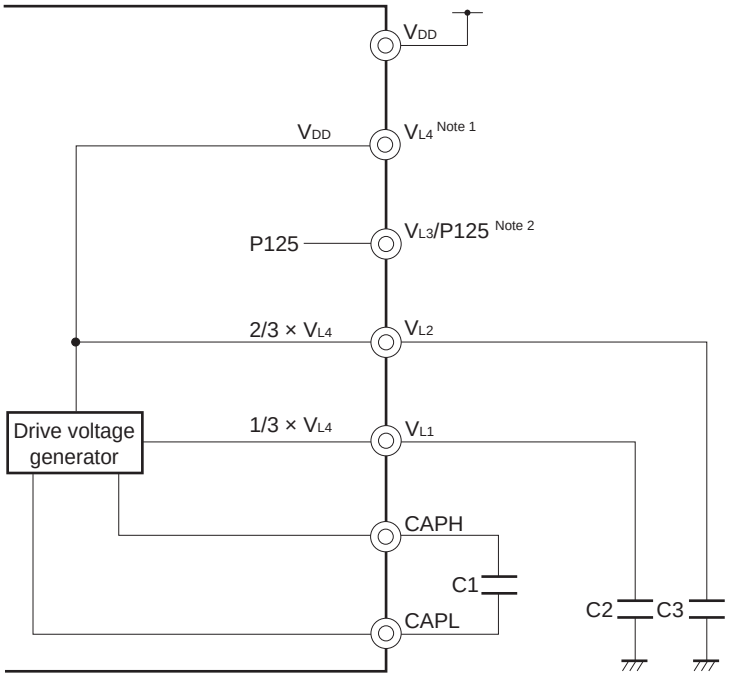
Different from the external resistance division method, there is always no current flowing with the capacitor split method, so current consumption can be reduced.

Table 23 - 14 LCD Drive Voltages (Capacitor Split Method)

Bias Method / LCD Drive Voltage Pin	1/3 Bias Method
V_{L4}	V_{DD}
V_{L3}	—
V_{L2}	2/3 × V_{L4}
V_{L1}	1/3 × V_{L4}

Figure 23 - 22 Examples of LCD Drive Power Connections (Capacitor Split Method)

• 1/3 bias method



Note 1. When switching to internal voltage boosting method, connect capacitor C4 as shown in Figure 23 - 21 Examples of LCD Drive Power Connections (Internal Voltage Boosting Method).

Note 2. V_{L3} can be used as port (P125).

Remark Use a capacitor with as little leakage as possible.
In addition, make C1 a nonpolar capacitor.

23.9 Common and Segment Signals

Each pixel of the LCD panel turns on when the potential difference between the corresponding common and segment signals becomes higher than a specific voltage (LCD drive voltage, V_{LCD}). The pixels turn off when the potential difference becomes lower than V_{LCD}.

Applying DC voltage to the common and segment signals of an LCD panel causes deterioration. To avoid this problem, this LCD panel is driven by AC voltage.

(1) Common signals

Each common signal is selected sequentially according to a specified number of time slices at the timing listed in Table 23 - 15. In the static display mode, the same signal is output to COM0 to COM3.

In the two-time-slice mode, leave the COM2 and COM3 pins open. In the three-time-slice mode, leave the COM3 pin open.

Use the COM4 to COM7 pins other than in the six-time-slice mode and eight-time-slice mode, and COM6, COM7 pins in the six-time-slice mode as open or segment pins.

Table 23 - 15 COM Signals

COM Signal / Number of Time Slices	COM0	COM1	COM2	COM3	COM4	COM5	COM6	COM7
Static display mode					Note	Note	Note	Note
Two-time-slice mode			Open	Open	Note	Note	Note	Note
Three-time-slice mode				Open	Note	Note	Note	Note
Four-time-slice mode					Note	Note	Note	Note
Six-time-slice mode							Note	Note
Eight-time-slice mode								

Note Use the pins as open or segment pins.

(2) Segment signals

The segment signals correspond to the LCD display data register (see **23.4 LCD Display Data Registers**).

When the number of time slices is eight, bits 0 to 7 of each display data register are read in synchronization with COM0 to COM7, respectively. If a bit is 1, it is converted to the select voltage, and if it is 0, it is converted to the deselect voltage. The conversion results are output to the segment pins (SEG4 to SEG35).

When the number of time slices is number other than eight, bits 0 to 3 of each byte in A-pattern area are read in synchronization with COM0 to COM3, and bits 4 to 7 of each byte in B-pattern area are read in synchronization with COM0 to COM3, respectively. If a bit is 1, it is converted to the select voltage, and if it is 0, it is converted to the deselect voltage. The conversion results are output to the segment pins (SEG0 to SEG35).

Check, with the information given above, what combination of front-surface electrodes (corresponding to the segment signals) and rear-surface electrodes (corresponding to the common signals) forms display patterns in the LCD display data register, and write the bit data that corresponds to the desired display pattern on a one-to-one basis.

Remark The mounted segment output pins vary depending on the product.

- R5F11NM, R5F11RM: SEG0 to SEG35
- R5F11NL: SEG0 to SEG3, SEG5 to SEG9, SEG14 to SEG21, SEG24, SEG26 to SEG34

(3) Output waveforms of common and segment signals

The voltages listed in Table 23 - 16 are output as common and segment signals.

When both common and segment signals are at the select voltage, a display on-voltage of ±V_{LCD} is obtained.

The other combinations of the signals correspond to the display off-voltage.

Table 23 - 16 LCD Drive Voltage

(a) Static display mode

Common Signal \ Segment Signal	Select Signal Level	Deselect Signal Level
	V_{SS}/V_{L4}	V_{L4}/V_{SS}
V_{L4}/V_{SS}	$-V_{LCD}/+V_{LCD}$	0 V/0 V

(b) 1/2 bias method

Common Signal \ Segment Signal		Select Signal Level	Deselect Signal Level
		V_{SS}/V_{L4}	V_{L4}/V_{SS}
Select signal level	V_{L4}/V_{SS}	$-V_{LCD}/+V_{LCD}$	0 V/0 V
Deselect signal level	V_{L2}	$-\frac{1}{2}V_{LCD}/+\frac{1}{2}V_{LCD}$	$+\frac{1}{2}V_{LCD}/-\frac{1}{2}V_{LCD}$

(c) 1/3 bias method (waveform A or B)

Common Signal \ Segment Signal		Select Signal Level	Deselect Signal Level
		V_{SS}/V_{L4}	V_{L2}/V_{L1}
Select signal level	V_{L4}/V_{SS}	$-V_{LCD}/+V_{LCD}$	$-\frac{1}{3}V_{LCD}/+\frac{1}{3}V_{LCD}$
Deselect signal level	V_{L1}/V_{L2}	$-\frac{1}{3}V_{LCD}/+\frac{1}{3}V_{LCD}$	$+\frac{1}{3}V_{LCD}/-\frac{1}{3}V_{LCD}$

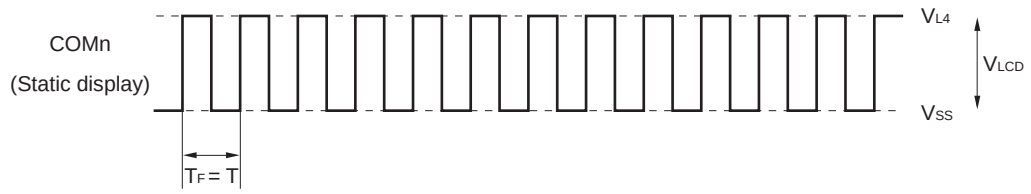
(d) 1/4 bias method (waveform A or B)

Common Signal \ Segment Signal		Select Signal Level	Deselect Signal Level
		V_{SS}/V_{L4}	V_{L2}
Select signal level	V_{L4}/V_{SS}	$-V_{LCD}/+V_{LCD}$	$-\frac{1}{2}V_{LCD}/+\frac{1}{2}V_{LCD}$
Deselect signal level	V_{L1}/V_{L3}	$-\frac{1}{4}V_{LCD}/+\frac{1}{4}V_{LCD}$	$+\frac{1}{4}V_{LCD}/-\frac{1}{4}V_{LCD}$

Figure 23 - 23 shows the common signal waveforms, and Figure 23 - 24 shows the voltages and phases of the common and segment signals.

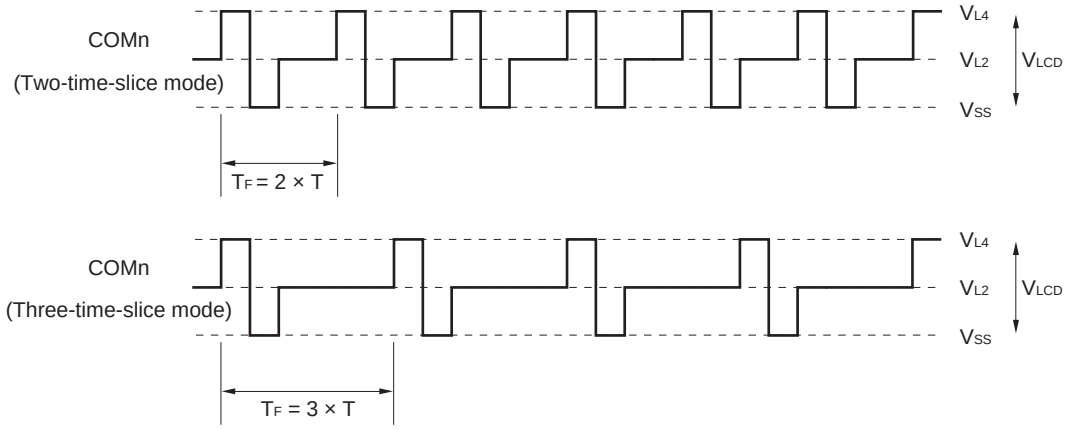
Figure 23 - 23 Common Signal Waveforms (1/3)

(a) Static display mode



T: One LCD clock period TF: Frame frequency

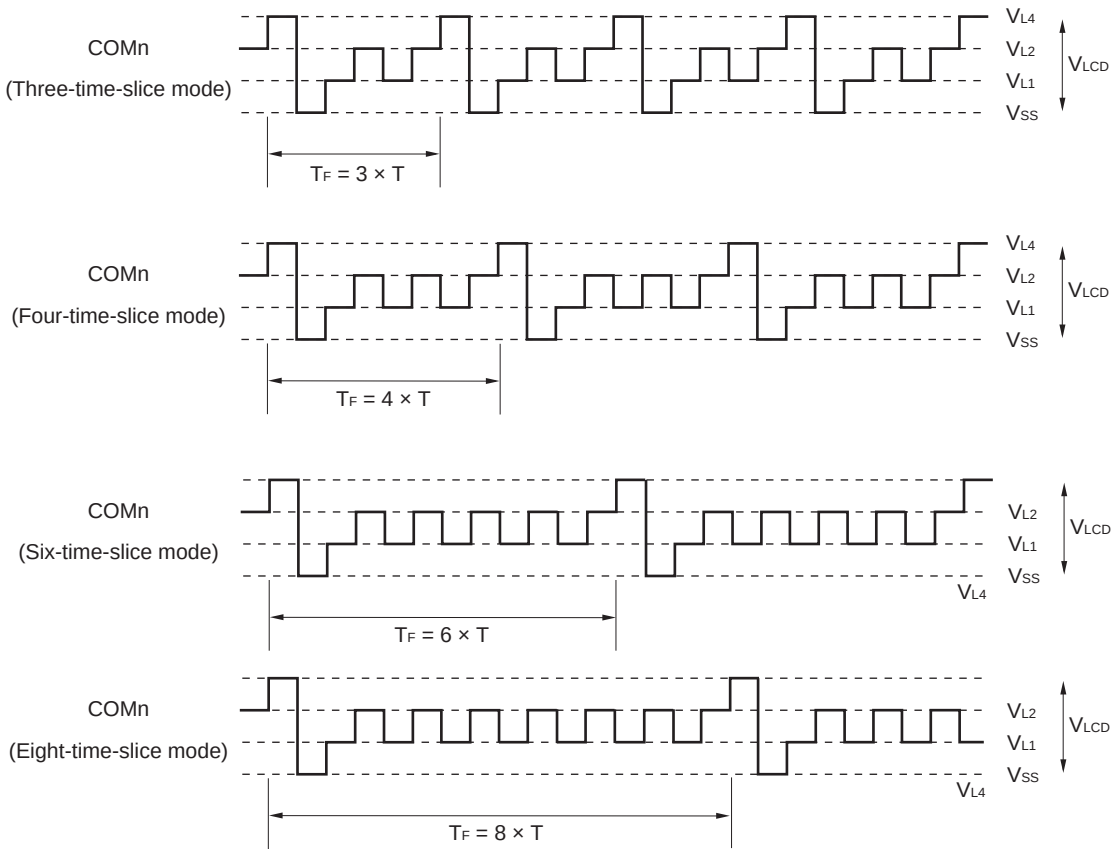
(b) 1/2 bias method



T: One LCD clock period TF: Frame frequency

Figure 23 - 23 Common Signal Waveforms (2/3)

(c) 1/3 bias method



T: One LCD clock period TF: Frame frequency

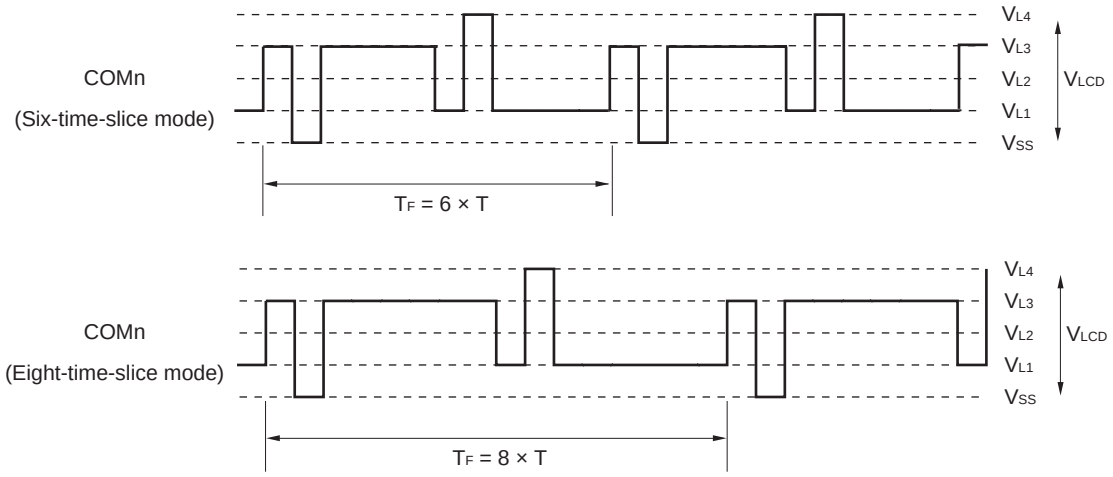
< Example of calculation of LCD frame frequency (When four-time-slice mode is used) >

LCD clock: $32768/2^7$ = 256 Hz (When setting to LCDC0 = 06H)

LCD frame frequency: 64 Hz

Figure 23 - 23 Common Signal Waveforms (3/3)

(d) 1/4 bias method



T: One LCD clock period TF: Frame frequency

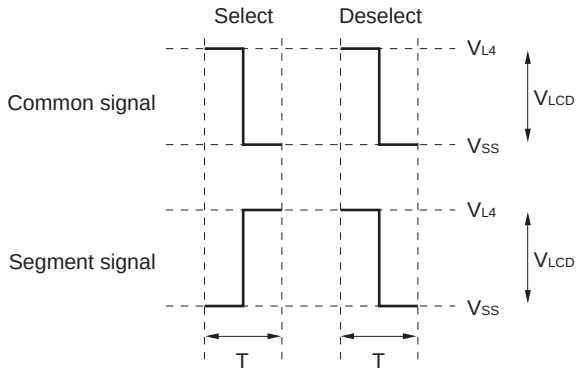
< Example of calculation of LCD frame frequency (When eight-time-slice mode is used) >

LCD clock: $32768/2^7$ = 256 Hz (When setting to LCDC0 = 06H)

LCD frame frequency: 32 Hz

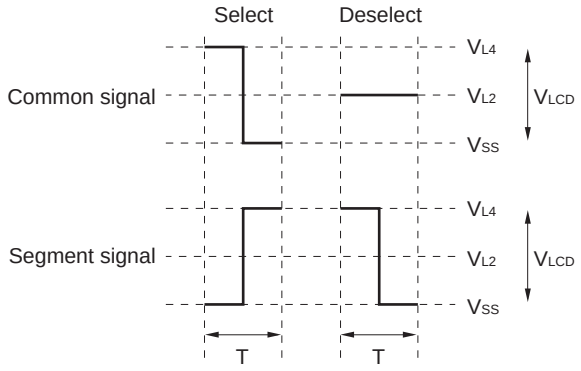
Figure 23 - 24 Voltages and Phases of Common and Segment Signals (1/3)

(a) Static display mode (waveform A)



T: One LCD clock period

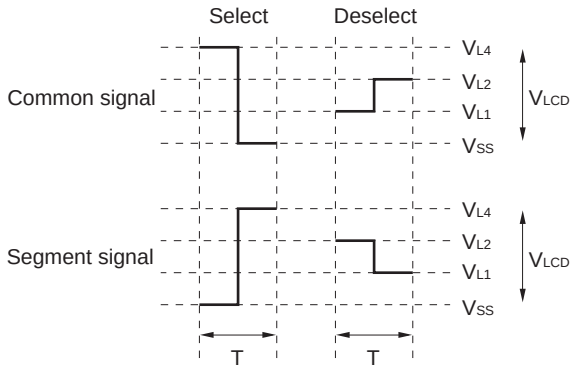
(b) 1/2 bias method (waveform A)



T: One LCD clock period

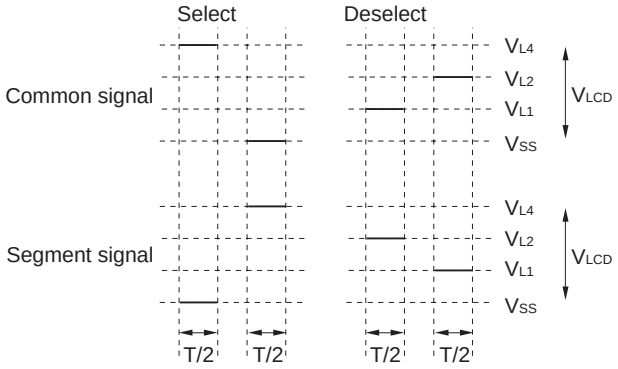
Figure 23 - 24 Voltages and Phases of Common and Segment Signals (2/3)

(c) 1/3 bias method (waveform A)



T: One LCD clock period

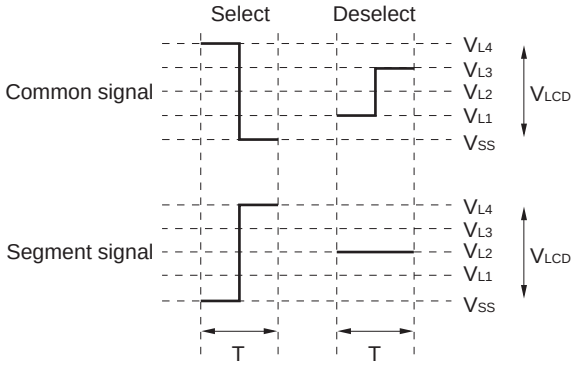
(d) 1/3 bias method (waveform B)



T: One LCD clock period

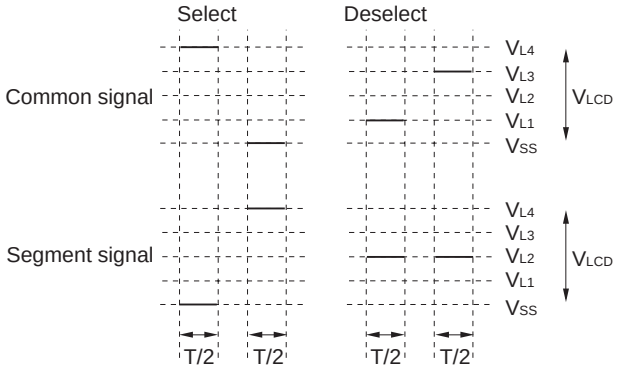
Figure 23 - 24 Voltages and Phases of Common and Segment Signals (3/3)

(e) 1/4 bias method (waveform A)



T: One LCD clock period

(f) 1/4 bias method (waveform B)



T: One LCD clock period

23.10 Display Modes

23.10.1 Static display example

Figure 23 - 26 shows how the three-digit LCD panel having the display pattern shown in Figure 23 - 25 is connected to the segment signals (SEG0 to SEG23) and the common signal (COM0). This example displays data “12.3” in the LCD panel. The contents of the display data register (F0400H to F0417H) correspond to this display.

The following description focuses on numeral “2.” (2.) displayed in the second digit. To display “2.” in the LCD panel, it is necessary to apply the select or deselect voltage to the SEG8 to SEG15 pins according to Table 23 - 17 at the timing of the common signal COM0; see **Figure 23 - 25** for the relationship between the segment signals and LCD segments.

Table 23 - 17 Select and Deselect Voltages (COM0)

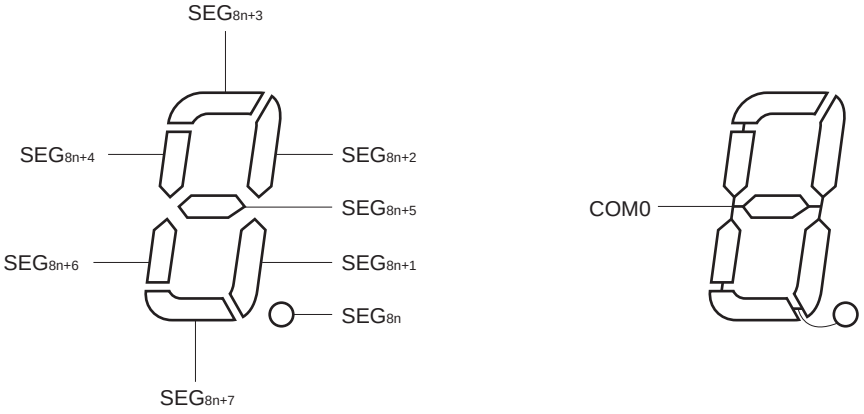
Segment / Common	SEG8	SEG9	SEG10	SEG11	SEG12	SEG13	SEG14	SEG15
COM0	Select	Deselect	Select	Select	Deselect	Select	Select	Select

According to Table 23 - 17, it is determined that the bit-0 pattern of the display data register locations (F0408H to F040FH) must be 10110111.

Figure 23 - 27 shows the LCD drive waveforms of SEG11 and SEG12, and COM0. When the select voltage is applied to SEG11 at the timing of COM0, an alternate rectangle waveform, +V_{LCD}/–V_{LCD}, is generated to turn on the corresponding LCD segment.

COM1 to COM3 are supplied with the same waveform as for COM0. So, COM0 to COM3 may be connected together to increase the driving capacity.

Figure 23 - 25 Static LCD Display Pattern and Electrode Connections



Remark R5F11NM: n = 0 to 3

Figure 23 - 26 Example of Connecting Static LCD Panel

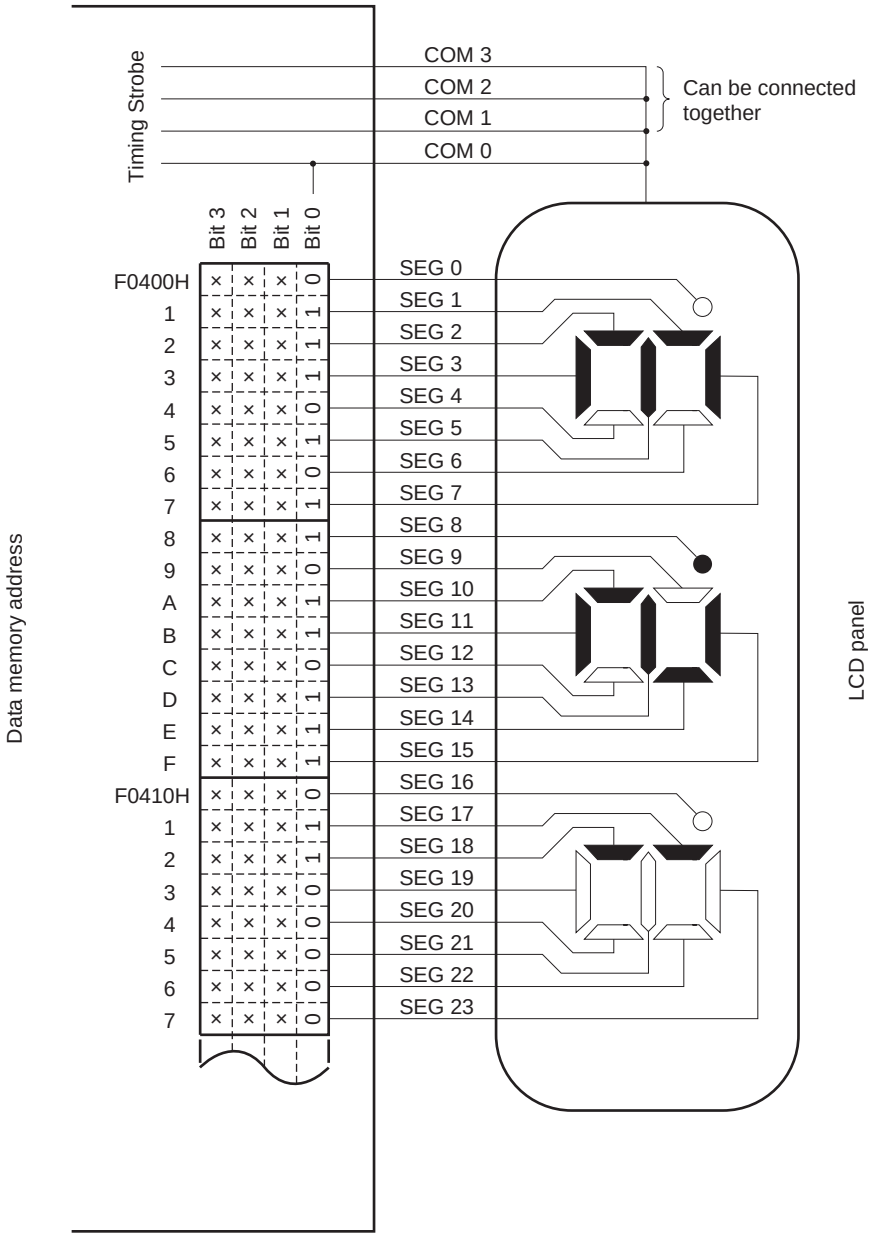
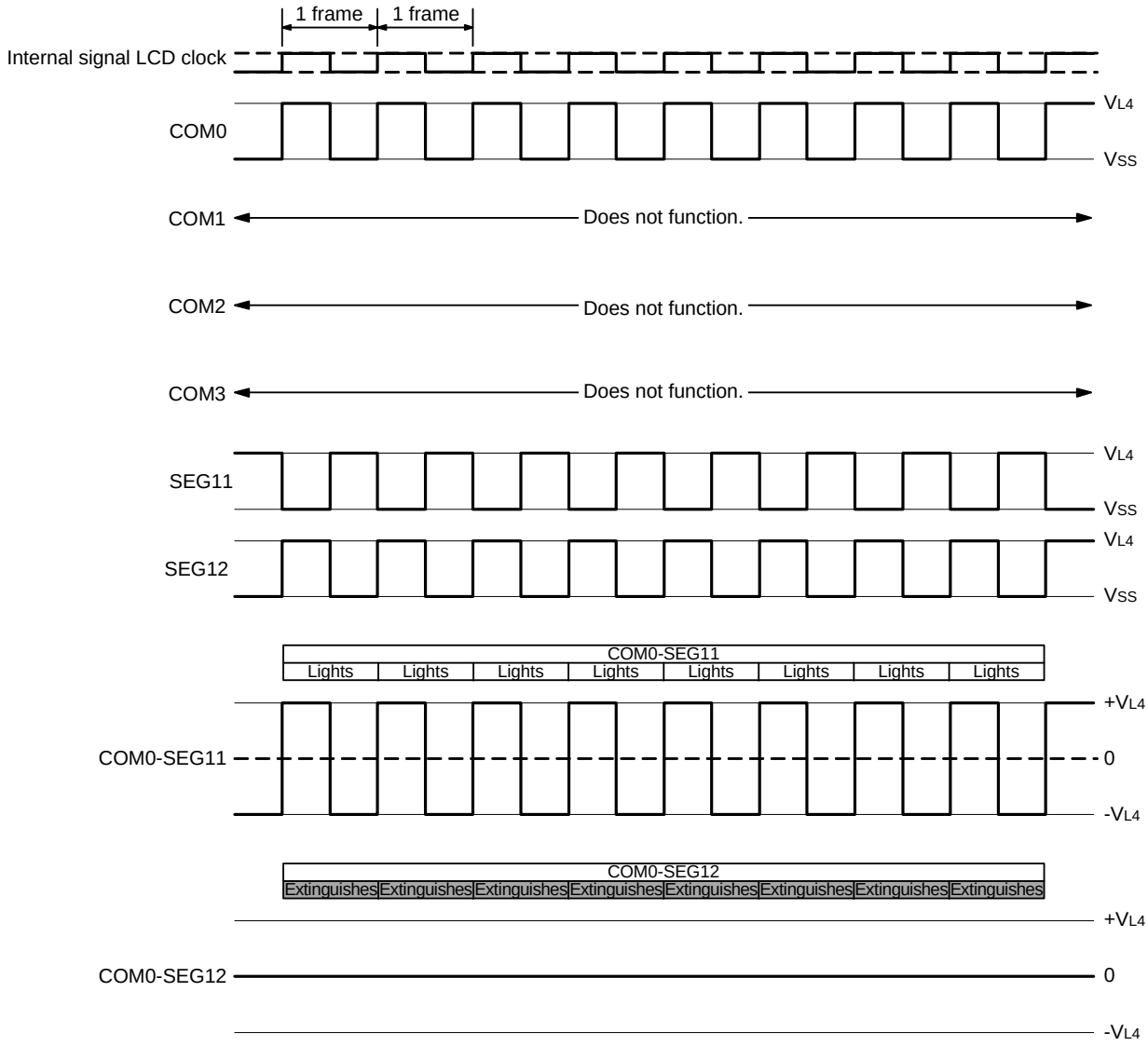


Figure 23 - 27 Static LCD Drive Waveform Examples for SEG11, SEG12, and COM0



23.10.2 Two-time-slice display example

Figure 23 - 29 shows how the 6-digit LCD panel having the display pattern shown in Figure 23 - 28 is connected to the segment signals (SEG0 to SEG23) and the common signals (COM0 and COM1). This example displays data “12345.6” in the LCD panel. The contents of the display data register (F0400H to F0417H) correspond to this display.

The following description focuses on numeral “3” (3) displayed in the fourth digit. To display “3” in the LCD panel, it is necessary to apply the select or deselect voltage to the SEG12 to SEG15 pins according to Table 23 - 18 at the timing of the common signals COM0 and COM1; see **Figure 23 - 28** for the relationship between the segment signals and LCD segments.

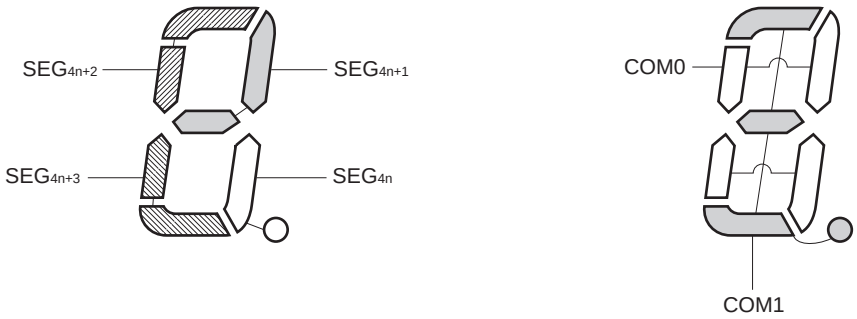
Table 23 - 18 Select and Deselect Voltages (COM0 and COM1)

Segment / Common	SEG12	SEG13	SEG14	SEG15
COM0	Select	Select	Deselect	Deselect
COM1	Deselect	Select	Select	Select

According to Table 23 - 18, it is determined that the display data register location (F040FH) that corresponds to SEG15 must contain xx10.

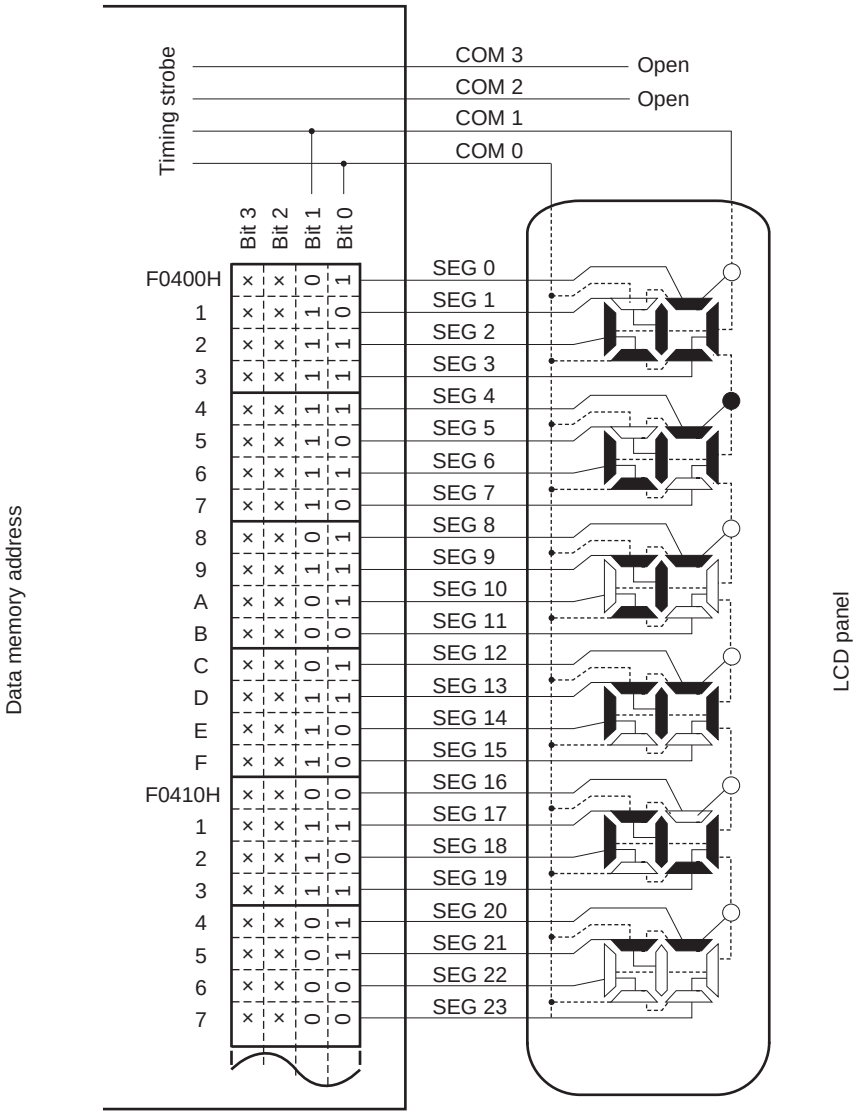
Figure 23 - 30 shows examples of LCD drive waveforms between the SEG15 signal and each common signal. When the select voltage is applied to SEG15 at the timing of COM1, an alternate rectangle waveform, $+V_{LCD}/-V_{LCD}$, is generated to turn on the corresponding LCD segment.

Figure 23 - 28 Two-Time-Slice LCD Display Pattern and Electrode Connections



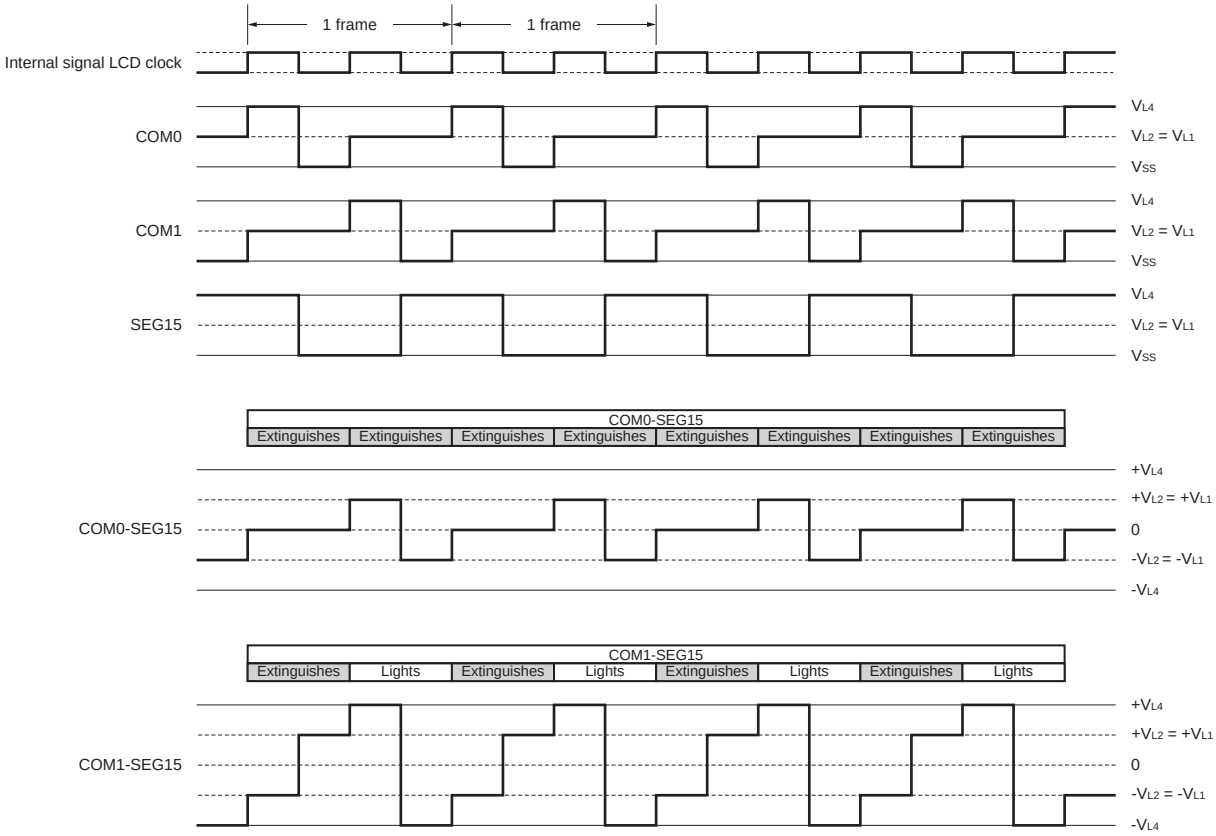
Remark R5F11NM: n = 0 to 8

Figure 23 - 29 Example of Connecting Two-Time-Slice LCD Panel



×: Can always be used to store any data because the two-time-slice mode is being used.

Figure 23 - 30 Two-Time-Slice LCD Drive Waveform Examples Between SEG15 and Each Common Signals (1/2 Bias Method)



23.10.3 Three-time-slice display example

Figure 23 - 32 shows how the 8-digit LCD panel having the display pattern shown in Figure 23 - 31 is connected to the segment signals (SEG0 to SEG23) and the common signals (COM0 to COM2). This example displays data “123456.78” in the LCD panel. The contents of the display data register (addresses F0400H to F0417H) correspond to this display.

The following description focuses on numeral “6.” (6.) displayed in the third digit. To display “6.” in the LCD panel, it is necessary to apply the select or deselect voltage to the SEG6 to SEG8 pins according to Table 23 - 19 at the timing of the common signals COM0 to COM2; see **Figure 23 - 31** for the relationship between the segment signals and LCD segments.

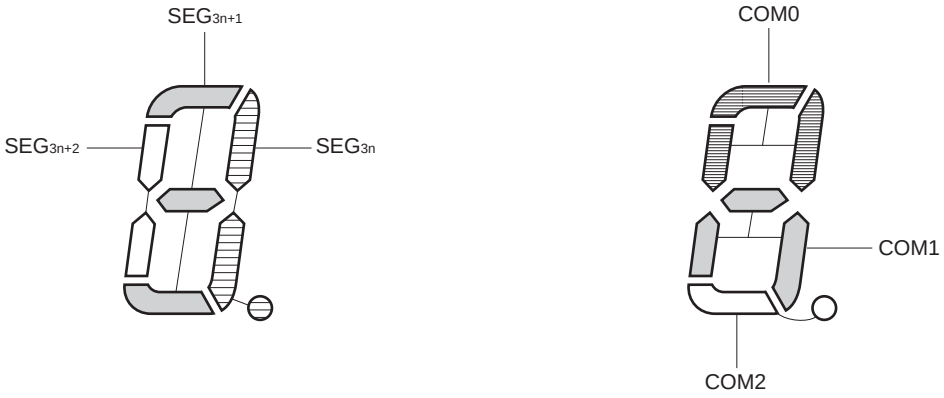
Table 23 - 19 Select and Deselect Voltages (COM0 to COM2)

Common \ Segment	SEG6	SEG7	SEG8
COM0	Deselect	Select	Select
COM1	Select	Select	Select
COM2	Select	Select	—

According to Table 23 - 19, it is determined that the display data register location (F0406H) that corresponds to SEG6 must contain x110.

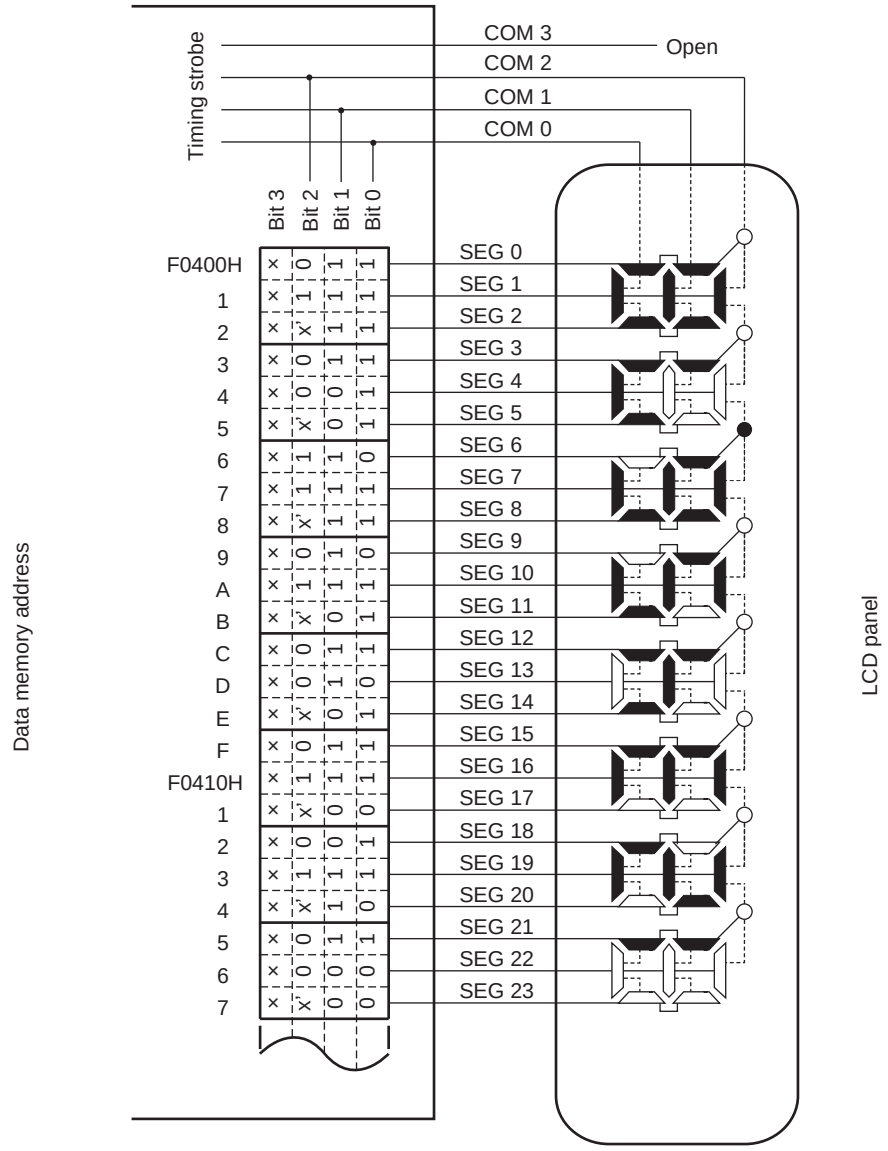
Figures 23 - 33 and 23 - 34 show examples of LCD drive waveforms between the SEG6 signal and each common signal in the 1/2 and 1/3 bias methods, respectively. When the select voltage is applied to SEG6 at the timing of COM1 or COM2, an alternate rectangle waveform, +V_{LCD}/–V_{LCD}, is generated to turn on the corresponding LCD segment.

Figure 23 - 31 Three-Time-Slice LCD Display Pattern and Electrode Connections



Remark R5F11NM: n = 0 to 11

Figure 23 - 32 Example of Connecting Three-Time-Slice LCD Panel



X': Can be used to store any data because there is no corresponding segment in the LCD panel.
×: Can always be used to store any data because the three-time-slice mode is being used.

Figure 23 - 33 Three-Time-Slice LCD Drive Waveform Examples Between SEG6 and Each Common Signals (1/2 Bias Method)

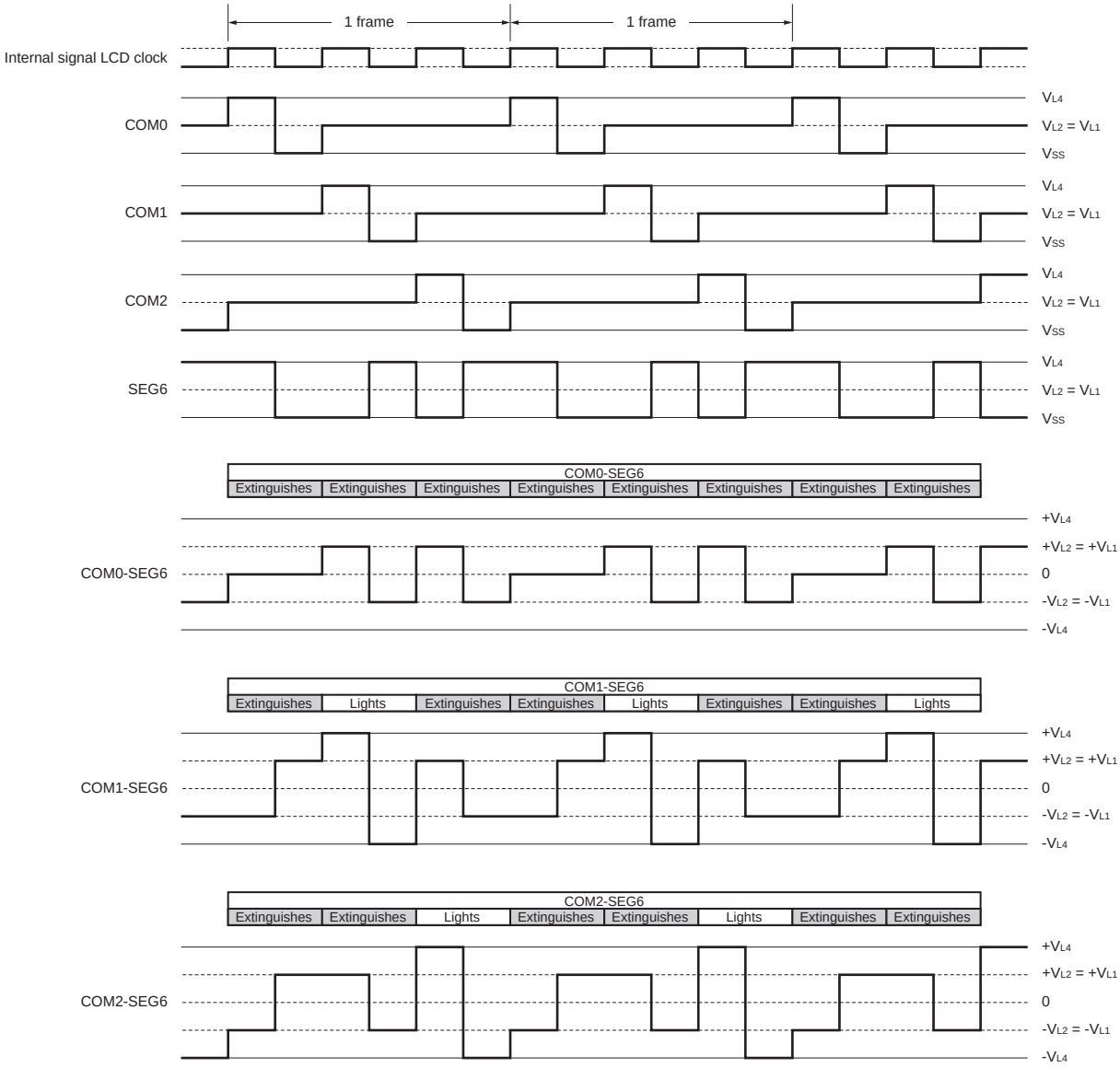
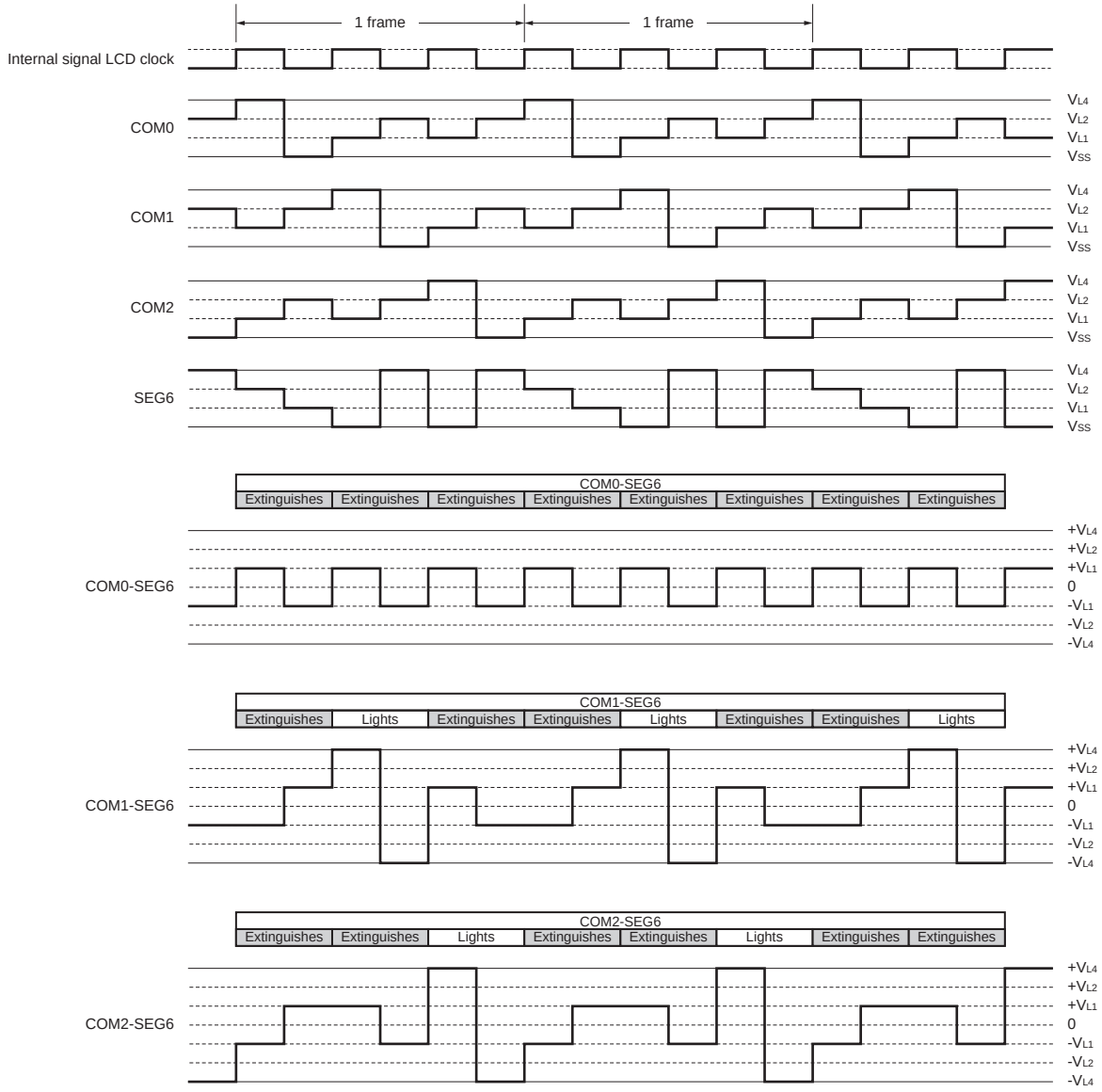


Figure 23 - 34 Three-Time-Slice LCD Drive Waveform Examples Between SEG6 and Each Common Signals (1/3 Bias Method)



23.10.4 Four-time-slice display example

Figure 23 - 36 shows how the 12-digit LCD panel having the display pattern shown in Figure 23 - 35 is connected to the segment signals (SEG0 to SEG23) and the common signals (COM0 to COM3). This example displays data “123456.789012” in the LCD panel. The contents of the display data register (addresses F0400H to F0417H) correspond to this display.

The following description focuses on numeral “6.” (6.) displayed in the seventh digit. To display “6.” in the LCD panel, it is necessary to apply the select or deselect voltage to the SEG12 and SEG13 pins according to Table 23 - 20 at the timing of the common signals COM0 to COM3; see **Figure 23 - 35** for the relationship between the segment signals and LCD segments.

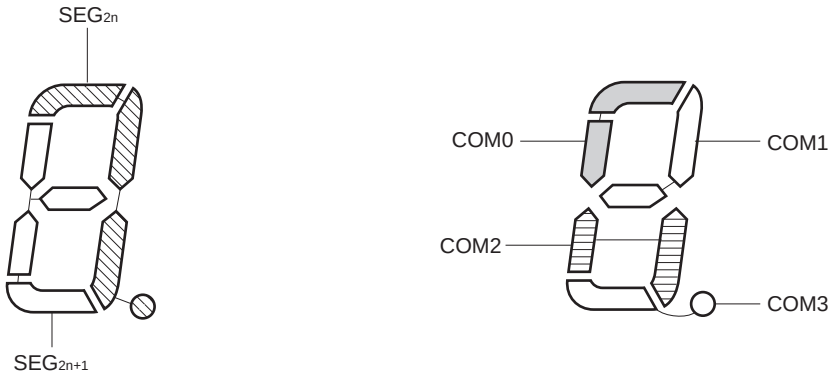
Table 23 - 20 Select and Deselect Voltages (COM0 to COM3)

Segment / Common	SEG12	SEG13
COM0	Select	Select
COM1	Deselect	Select
COM2	Select	Select
COM3	Select	Select

According to Table 23 - 20, it is determined that the display data register location (F040CH) that corresponds to SEG12 must contain 1101.

Figure 23 - 37 shows examples of LCD drive waveforms between the SEG12 signal and each common signal. When the select voltage is applied to SEG12 at the timing of COM0, an alternate rectangle waveform, $+V_{LCD}$/$-V_{LCD}$, is generated to turn on the corresponding LCD segment.

Figure 23 - 35 Four-Time-Slice LCD Display Pattern and Electrode Connections



Remark R5F11NM: n = 0 to 17

Figure 23 - 36 Example of Connecting Four-Time-Slice LCD Panel

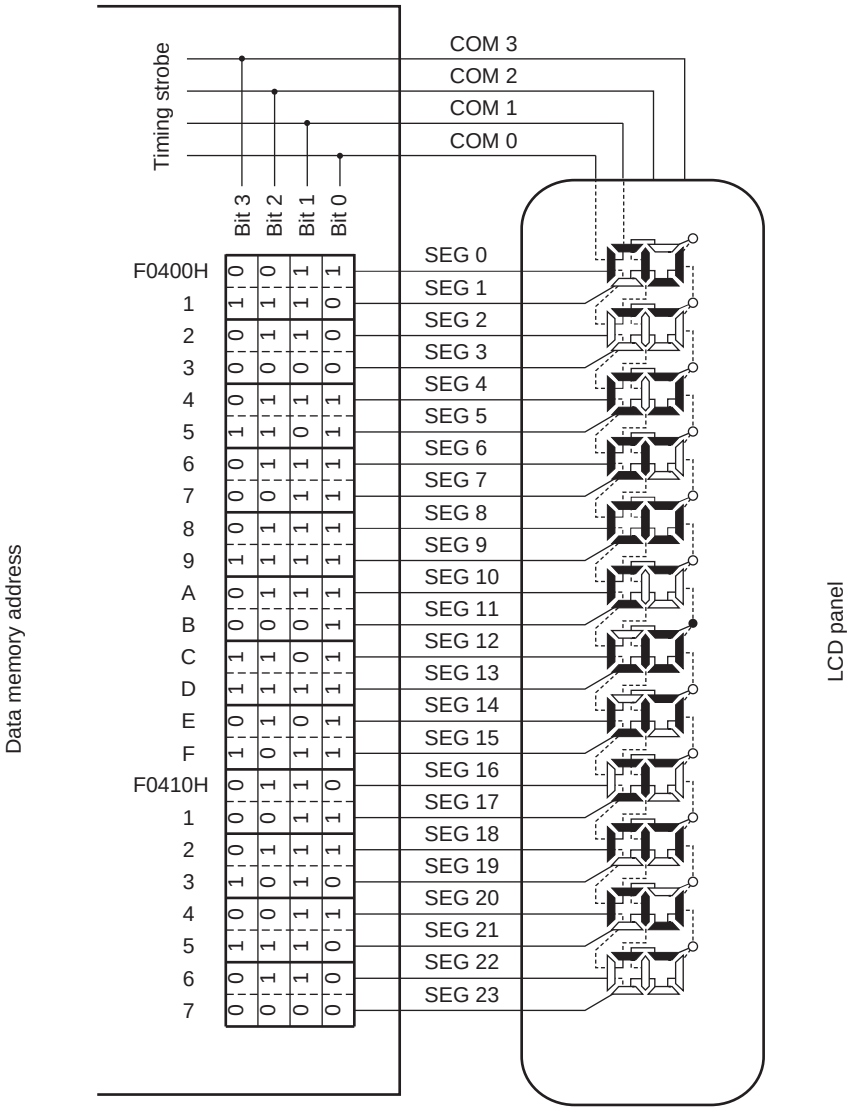


Figure 23 - 37 Four-Time-Slice LCD Drive Waveform Examples Between SEG12 and Each Common Signals (1/3 Bias Method) (1/2)

(a) Waveform A

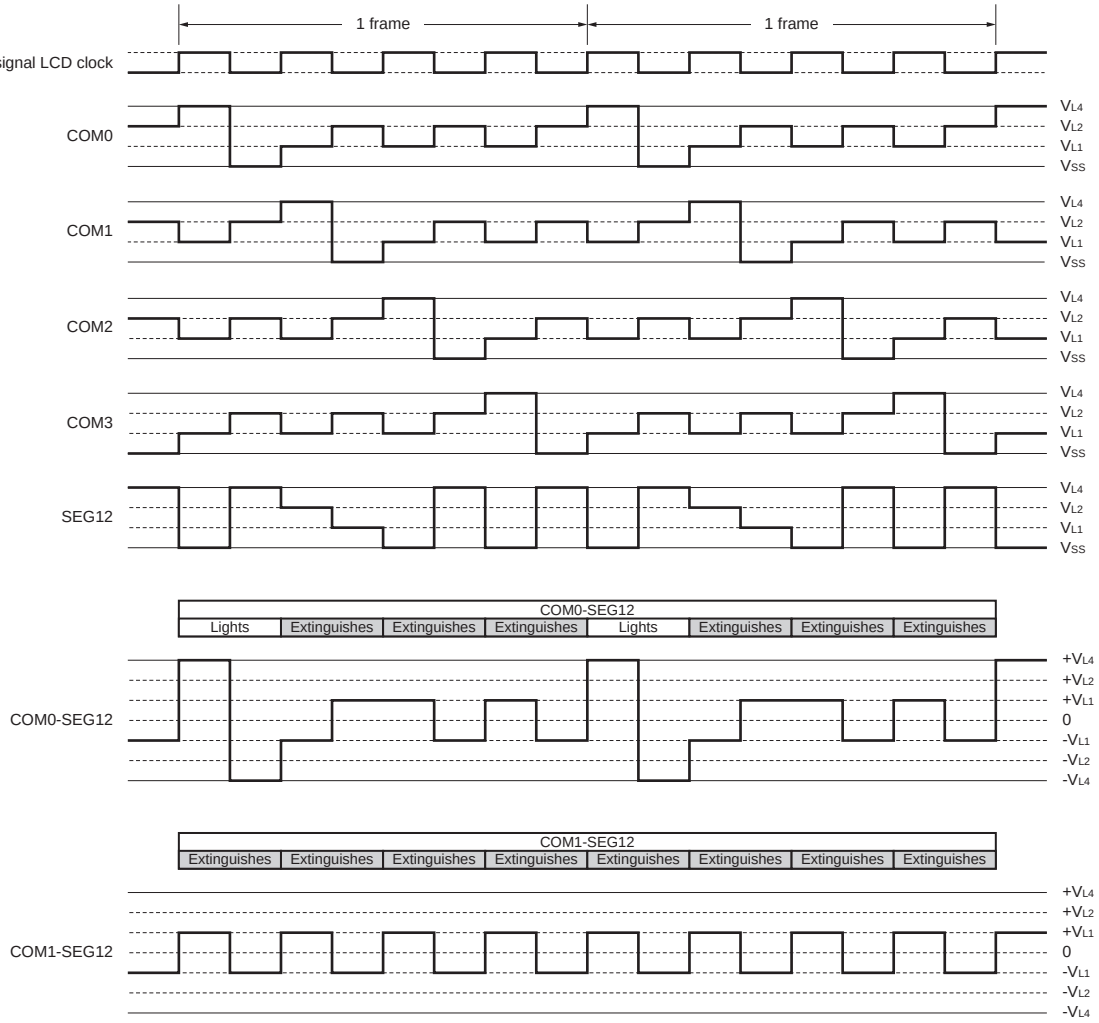
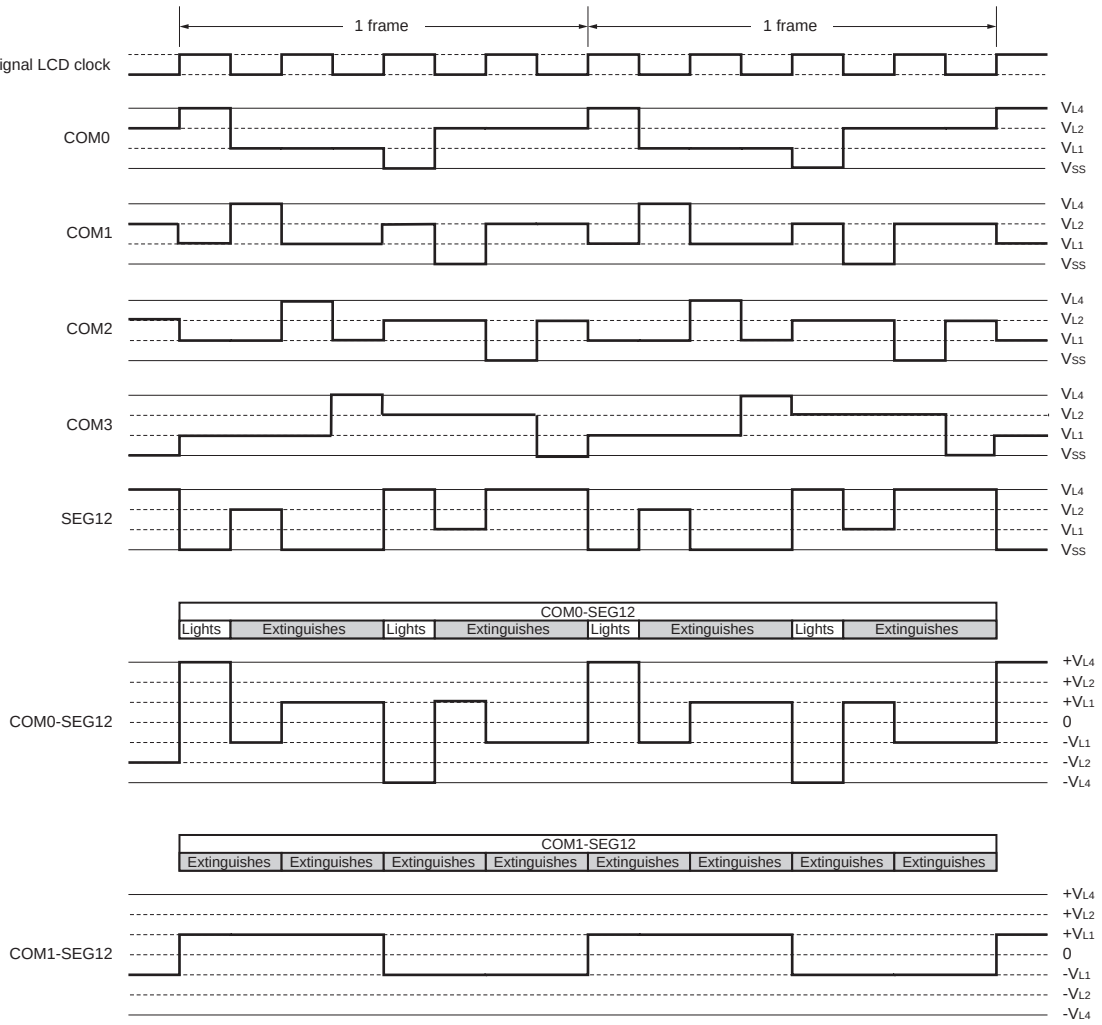


Figure 23 - 37 Four-Time-Slice LCD Drive Waveform Examples Between SEG12 and Each Common Signals (1/3 Bias Method) (2/2)

(b) Waveform B



23.10.5 Six-time-slice display example

Figure 23 - 39 shows how the 15x6 dot LCD panel having the display pattern shown in Figure 23 - 38 is connected to the segment signals (SEG2 to SEG16) and the common signals (COM0 to COM5). This example displays data “123” in the LCD panel. The contents of the display data register (addresses F0402H to F0410H) correspond to this display.

The following description focuses on numeral “3.” (3) displayed in the first digit. To display “3.” in the LCD panel, it is necessary to apply the select or deselect voltage to the SEG2 to SEG6 pins according to Table 23 - 21 at the timing of the common signals COM0 to COM5; see **Figure 23 - 38** for the relationship between the segment signals and LCD segments.

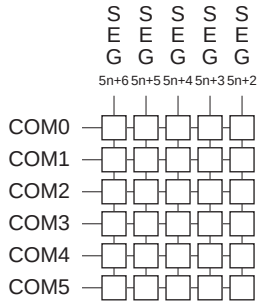
Table 23 - 21 Select and Deselect Voltages (COM0 to COM5)

Common \ Segment	SEG2	SEG3	SEG4	SEG5	SEG6
COM0	Select	Select	Select	Select	Select
COM1	Deselect	Select	Deselect	Deselect	Deselect
COM2	Deselect	Deselect	Select	Deselect	Deselect
COM3	Deselect	Select	Deselect	Deselect	Deselect
COM4	Select	Deselect	Deselect	Deselect	Select
COM5	Deselect	Select	Select	Select	Deselect

According to Table 23 - 21, it is determined that the display data register location (F0402H) that corresponds to SEG2 must contain 010001.

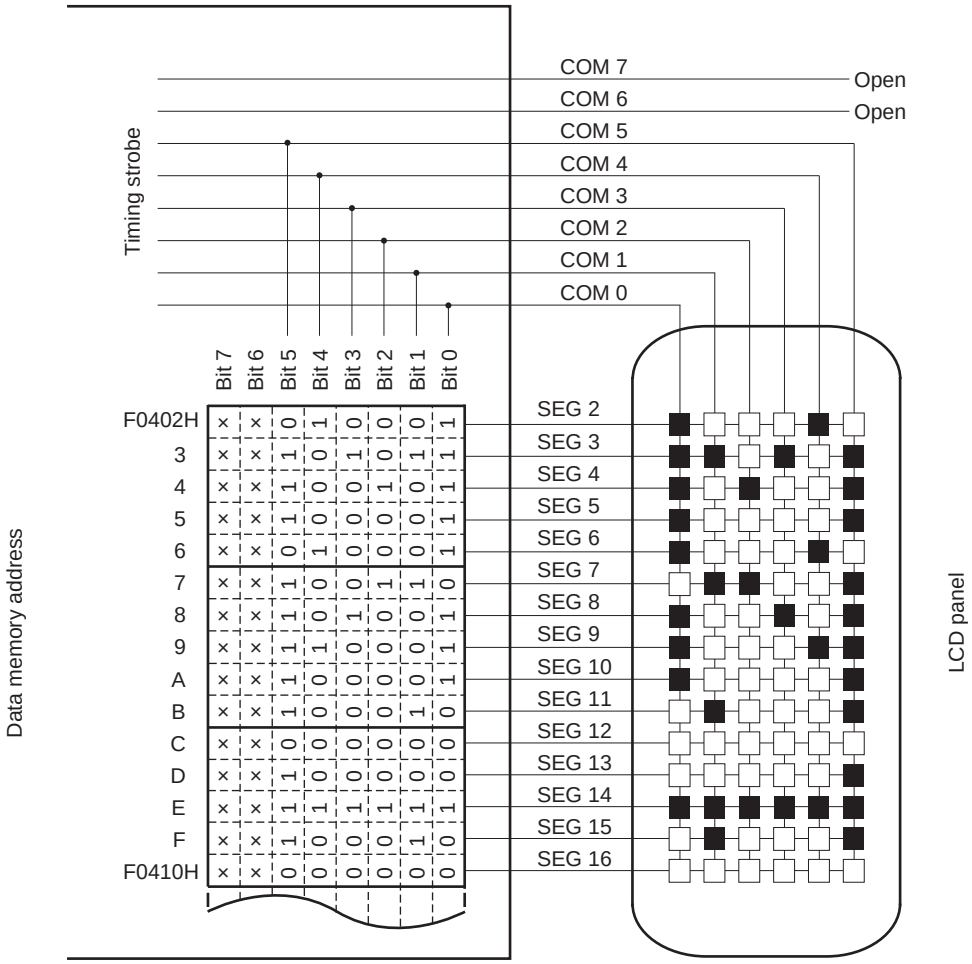
Figure 23 - 40 shows examples of LCD drive waveforms between the SEG2 signal and each common signal. When the select voltage is applied to SEG2 at the timing of COM0, a waveform is generated to turn on the corresponding LCD segment.

Figure 23 - 38 Six-Time-Slice LCD Display Pattern and Electrode Connections



Remark R5F11NM: n = 0 to 5

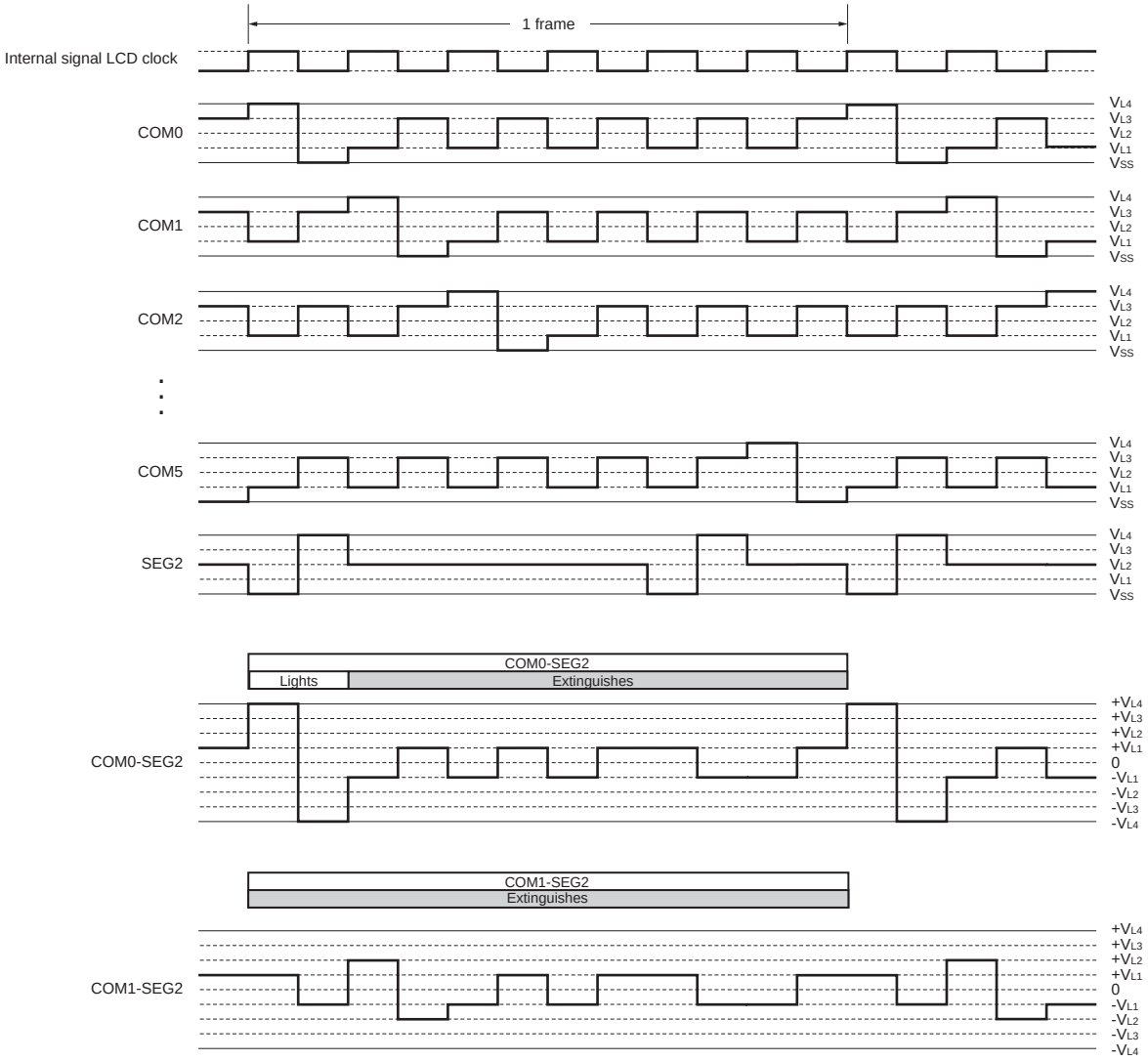
Figure 23 - 39 Example of Connecting Six-Time-Slice LCD Panel



×: Can always be used to store any data because the six-time-slice mode is being used.

Figure 23 - 40 Six-Time-Slice LCD Drive Waveform Examples Between SEG2 and Each Common Signals (1/4 Bias Method)

(a) Waveform A



23.10.6 Eight-time-slice display example

Figure 23 - 42 shows how the 15 × 8 dot LCD panel having the display pattern shown in Figure 23 - 41 is connected to the segment signals (SEG4 to SEG18) and the common signals (COM0 to COM7). This example displays data “123” in the LCD panel. The contents of the display data register (addresses F0404H to F0412H) correspond to this display.

The following description focuses on numeral “3” (3) displayed in the first digit. To display “3” in the LCD panel, it is necessary to apply the select or deselect voltage to the SEG4 to SEG8 pins according to Table 23 - 22 at the timing of the common signals COM0 to COM7; see **Figure 23 - 41** for the relationship between the segment signals and LCD segments.

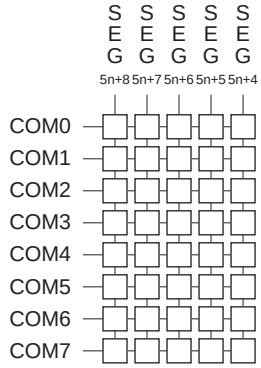
Table 23 - 22 Select and Deselect Voltages (COM0 to COM7)

Common \ Segment	SEG4	SEG5	SEG6	SEG7	SEG8
COM0	Select	Select	Select	Select	Select
COM1	Deselect	Select	Deselect	Deselect	Deselect
COM2	Deselect	Deselect	Select	Deselect	Deselect
COM3	Deselect	Select	Deselect	Deselect	Deselect
COM4	Select	Deselect	Deselect	Deselect	Deselect
COM5	Select	Deselect	Deselect	Deselect	Select
COM6	Deselect	Select	Select	Select	Deselect
COM7	Deselect	Deselect	Deselect	Deselect	Deselect

According to Table 23 - 22, it is determined that the display data register location (F0404H) that corresponds to SEG4 must contain 00110001.

Figure 23 - 43 shows examples of LCD drive waveforms between the SEG4 signal and each common signal. When the select voltage is applied to SEG4 at the timing of COM0, a waveform is generated to turn on the corresponding LCD segment.

Figure 23 - 41 Eight-Time-Slice LCD Display Pattern and Electrode Connections



Remark R5F11NM: n = 0 to 5

Figure 23 - 42 Example of Connecting Eight-Time-Slice LCD Panel

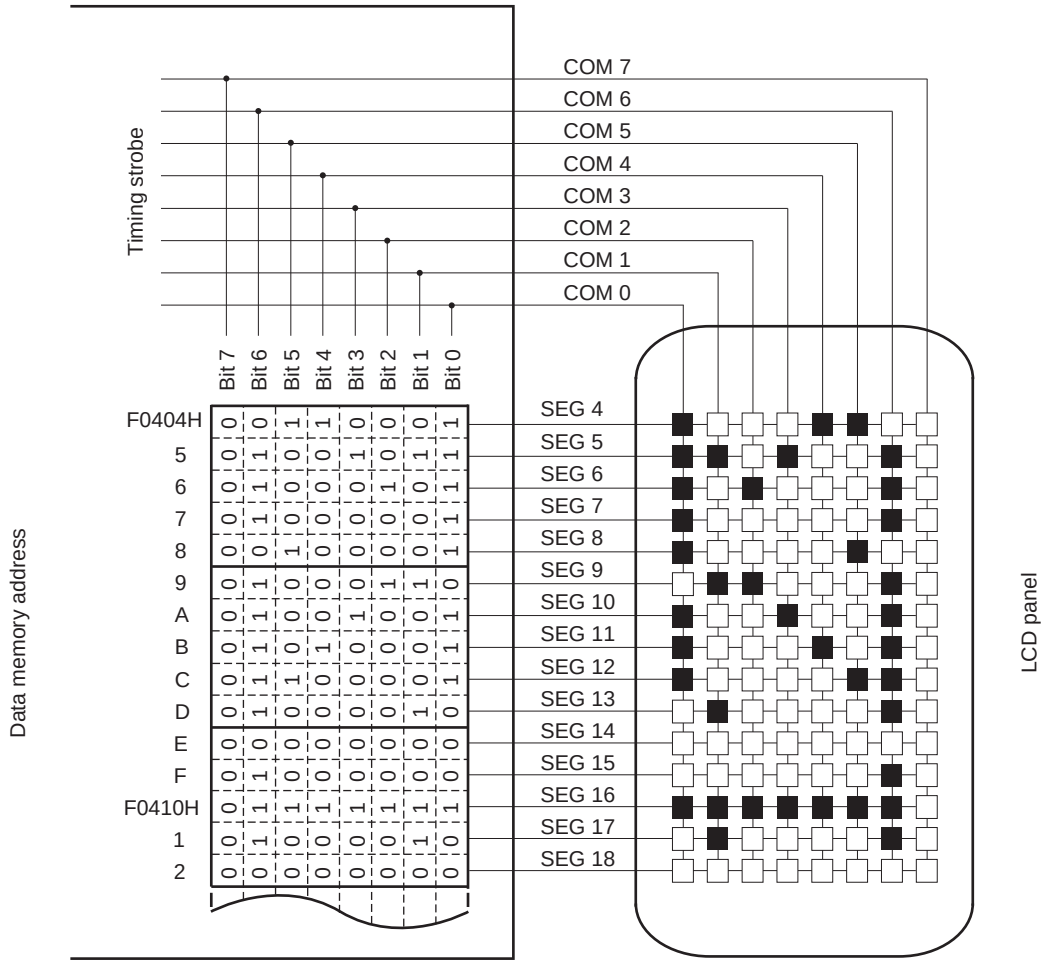


Figure 23 - 43 Eight-Time-Slice LCD Drive Waveform Examples Between SEG4 and Each Common Signals (1/4 Bias Method) (1/2)

(a) Waveform A

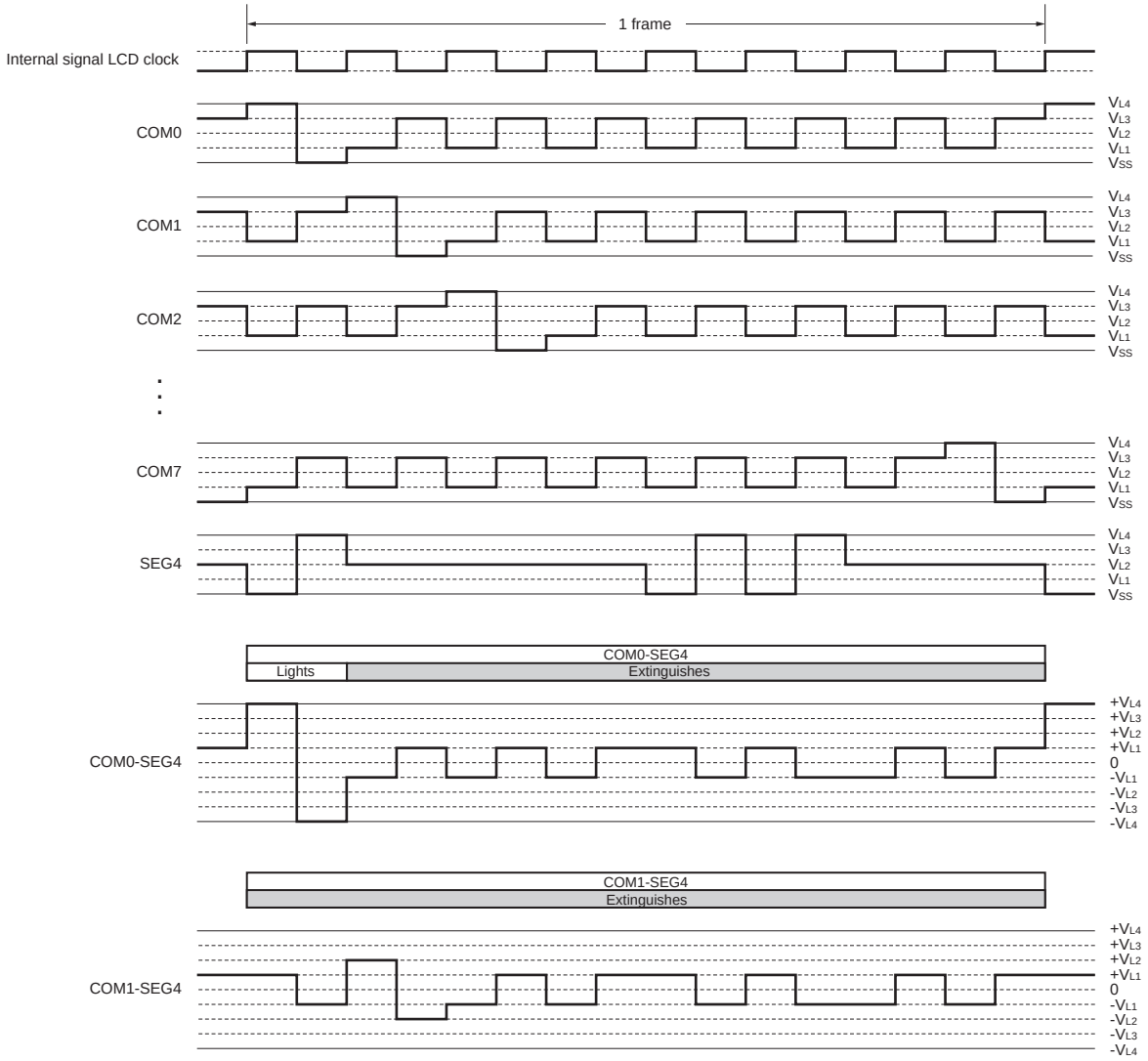
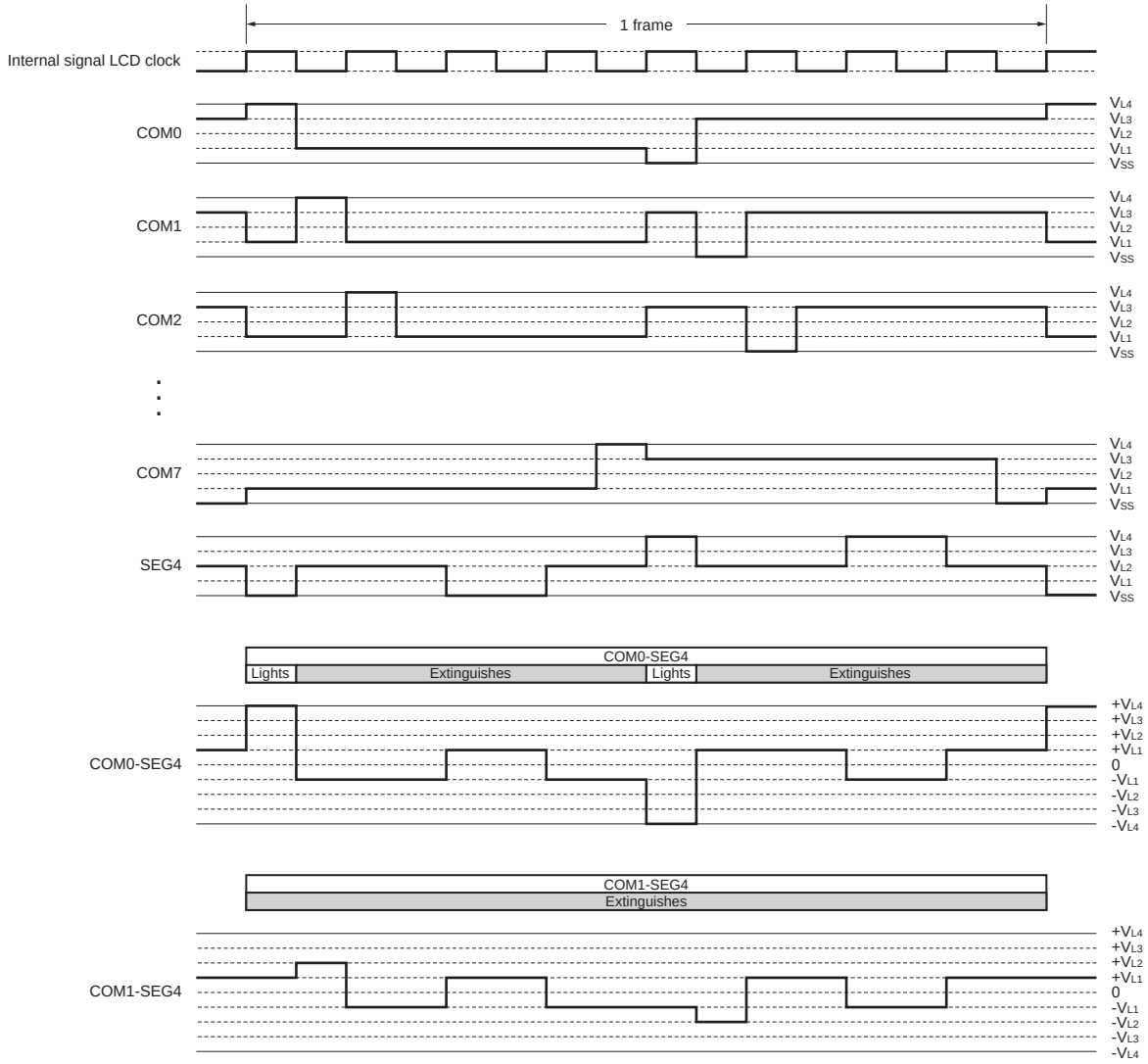


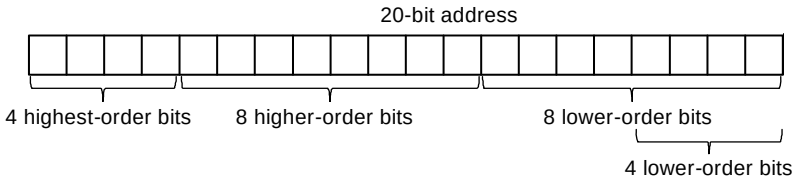
Figure 23 - 43 Eight-Time-Slice LCD Drive Waveform Examples Between SEG4 and Each Common Signals (1/4 Bias Method) (2/2)

(b) Waveform B



CHAPTER 24 DATA TRANSFER CONTROLLER (DTC)

The term “8 higher-order bits of the address” in this chapter indicates bits 15 to 8 of 20-bit address as shown below.



Unless otherwise specified, the 4 highest-order address bits all become 1 (values are of the form FxxxxH).

24.1 Functions of DTC

The data transfer controller (DTC) is a function that transfers data between memories without using the CPU. The DTC is activated by a peripheral function interrupt to perform data transfers. The DTC and CPU use the same bus, and the DTC takes priority over the CPU in using the bus.

Table 24 - 1 lists the DTC Specifications.

Table 24 - 1 DTC Specifications

Item		Specification
Activation sources		35 sources
Allocatable control data		24 sets
Address space which can be transferred	Address space	64 Kbytes (F0000H to FFFFFH), excluding general-purpose registers
	Sources	1st SFR area, RAM area (excluding general-purpose registers), mirror area Note, data flash memory area Note, 2nd SFR area
	Destinations	1st SFR area, RAM area (excluding general-purpose registers), 2nd SFR area
Maximum number of transfers	Normal mode	256 times
	Repeat mode	255 times
Maximum size of block to be transferred	Normal mode (8-bit transfer)	256 bytes
	Normal mode (16-bit transfer)	512 bytes
	Repeat mode	255 bytes
Unit of transfers		8 bits/16 bits
Transfer mode	Normal mode	Transfers end on completion of the transfer causing the DTCCTj register value to change from 1 to 0.
	Repeat mode	On completion of the transfer causing the DTCCTj register value to change from 1 to 0, the repeat area address is initialized and the DTRLDj register value is reloaded to the DTCCTj register to continue transfers.
Address control	Normal mode	Fixed or incremented
	Repeat mode	Addresses of the area not selected as the repeat area are fixed or incremented.
Priority of activation sources		Refer to **Table 24 - 5 DTC Activation Sources and Vector Addresses**.
Interrupt request	Normal mode	When the data transfer causing the DTCCTj register value to change from 1 to 0 is performed, the activation source interrupt request is generated for the CPU, and interrupt handling is performed on completion of the data transfer.
	Repeat mode	When the data transfer causing the DTCCTj register value to change from 1 to 0 is performed while the RPTINT bit in the DTCCRj register is 1 (interrupt generation enabled), the activation source interrupt request is generated for the CPU, and interrupt handling is performed on completion of the transfer.
Transfer start		When bits DTCENi0 to DTCENi7 in the DTCENi registers are 1 (activation enabled), data transfer is started each time the corresponding DTC activation sources are generated.

Table 24 - 1 DTC Specifications

Item		Specification
Transfer stop	Normal mode	• When bits DTCENi0 to DTCENi7 are set to 0 (activation disabled). • When the data transfer causing the DTCCTj register value to change from 1 to 0 is completed.
	Repeat mode	• When bits DTCENi0 to DTCENi7 are set to 0 (activation disabled). • When the data transfer causing the DTCCTj register value to change from 1 to 0 is completed while the RPTINT bit is 1 (interrupt generation enabled).
Operation in standby mode	HALT state	DTC operates
	SNOOZE state	DTC operates
	STOP state	DTC stops

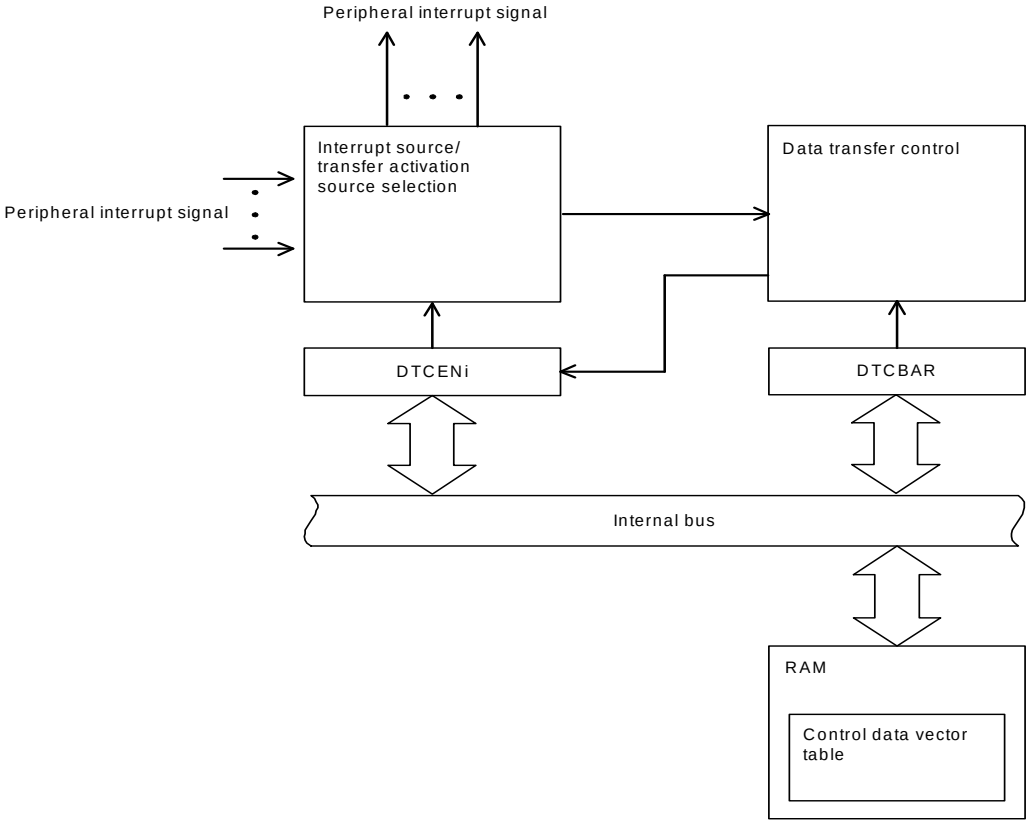
Note In the HALT mode and SNOOZE mode, these areas cannot be set as the sources for DTC transfer since the flash memory is stopped.

Remark i = 0 to 4, j = 0 to 23

24.2 Configuration of DTC

Figure 24 - 1 shows the DTC Block Diagram.

Figure 24 - 1 DTC Block Diagram



24.3 Registers Controlling DTC

Table 24 - 2 lists the Registers Controlling DTC.

Table 24 - 2 Registers Controlling DTC

Register Name	Symbol
Peripheral enable register 1	PER1
DTC activation enable register 0	DTCEN0
DTC activation enable register 1	DTCEN1
DTC activation enable register 2	DTCEN2
DTC activation enable register 3	DTCEN3
DTC activation enable register 4 Note	DTCEN4 Note
DTC base address register	DTCBAR

Note R5F11R only.

Table 24 - 3 lists DTC Control Data.

DTC control data is allocated in the DTC control data area in RAM.

The DTCBAR register is used to set the 256-byte area, including the DTC control data area and the DTC vector table area where the start address for control data is stored.

Table 24 - 3 DTC Control Data

Register Name	Symbol
DTC control register j	DTCCRj
DTC block size register j	DTBLSj
DTC transfer count register j	DTCCTj
DTC transfer count reload register j	DTRLDj
DTC source address register j	DTSARj
DTC destination address register j	DTDARj

Remark j = 0 to 23

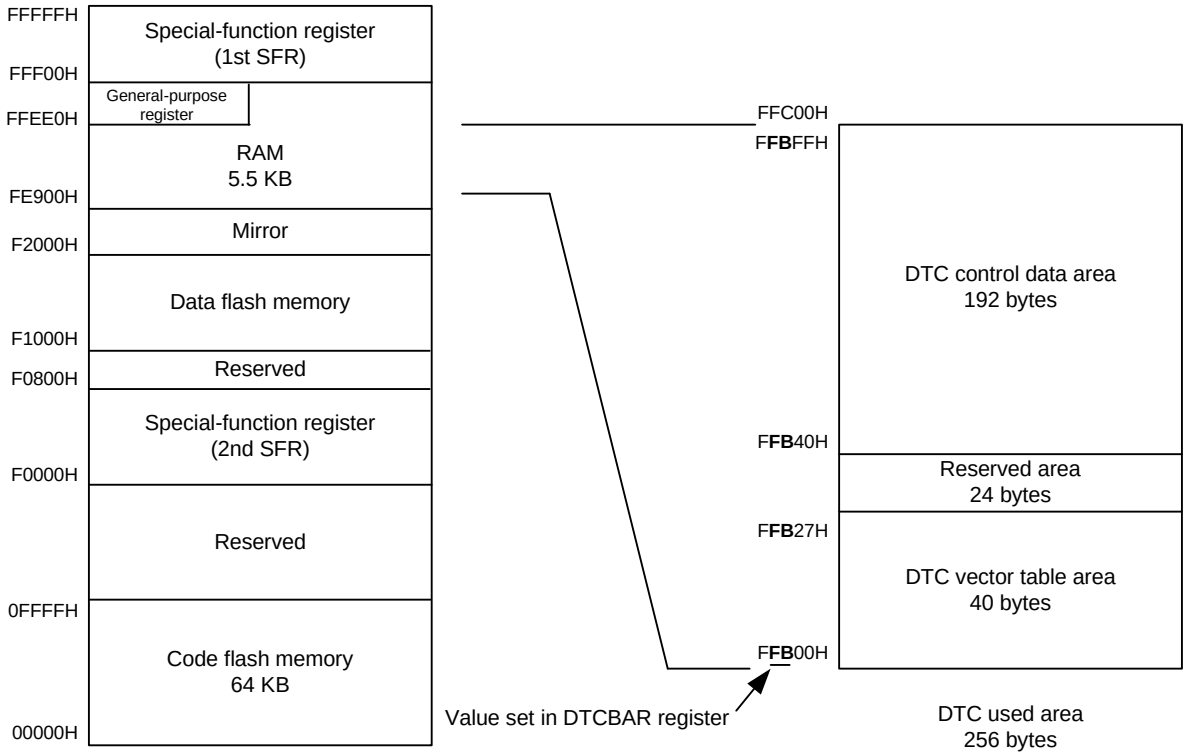
24.3.1 Allocation of DTC control data area and DTC vector table area

The DTCBAR register is used to set the 256-byte area where DTC control data and the vector table within the RAM area.

Figure 24 - 2 shows a Memory Map Example when DTCBAR Register is Set to FBH.

In the 192-byte DTC control data area, the space not used by the DTC can be used as RAM.

Figure 24 - 2 Memory Map Example when DTCBAR Register is Set to FBH



The areas where the DTC control data and vector table can be allocated differ depending on the product.

Caution 1. It is prohibited to use the general-purpose register (FFEE0H to FFEFFH) space as the DTC control data area or DTC vector table area.

Caution 2. Make sure the stack area, the DTC control data area, and the DTC vector table area do not overlap.

Caution 3. The internal RAM area in the following products cannot be used as the DTC control data area or DTC vector table area when using the self-programming and data-flash functions.
R5F11RMG: FDF00H to FE309H

Caution 4. The internal RAM area in the following products cannot be used as the DTC control data area or DTC vector table area when using the on-chip debugging trace function.
R5F11RMG: FE300H to FE6FFH

24.3.2 Control data allocation

Control data is allocated beginning with each start address in the order: Registers DTCCRj, DTBLSj, DTCCTj, DTRLDj, DTSARj, and DTDARj (j = 0 to 23).

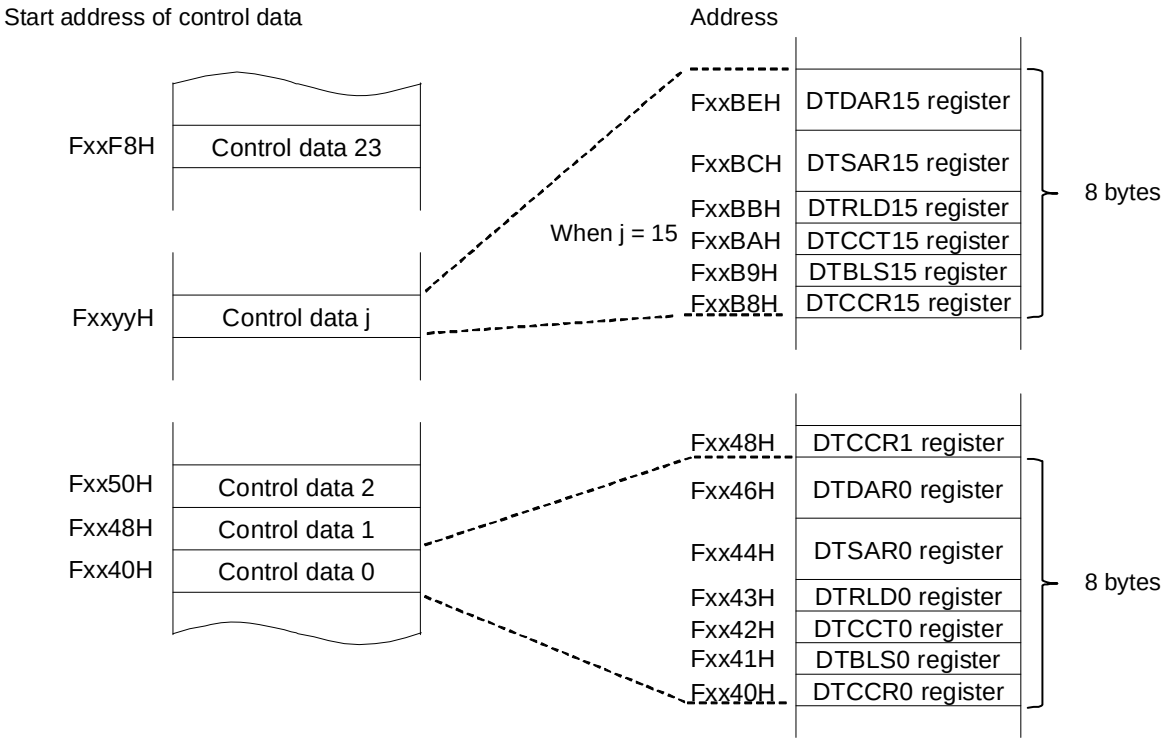
The higher 8 bits for start addresses 0 to 23 are set by the DTCBAR register, and the lower 8 bits are separately set according to the vector table assigned to each activation source.

Figure 24 - 3 shows Control Data Allocation.

Caution 1. Change the data in registers DTCCRj, DTBLSj, DTCCTj, DTRLDj, DTSARj, and DTDARj when the corresponding bit among bits DTCENi0 to DTCENi7 (i = 0 to 4) in the DTCENi register is set to 0 (DTC activation disabled).

Caution 2. Do not access DTCCRj, DTBLSj, DTCCTj, DTRLDj, DTSARj, or DTDARj using a DTC transfer.

Figure 24 - 3 Control Data Allocation



Remark xx: Value set in DTCBAR register

Table 24 - 4 Start Address of Control Data

j	Address	j	Address
11	Fxx98H	23	FxxF8H
10	Fxx90H	22	FxxF0H
9	Fxx88H	21	FxxE8H
8	Fxx80H	20	FxxE0H
7	Fxx78H	19	FxxD8H
6	Fxx70H	18	FxxD0H
5	Fxx68H	17	FxxC8H
4	Fxx60H	16	FxxC0H
3	Fxx58H	15	FxxB8H
2	Fxx50H	14	FxxB0H
1	Fxx48H	13	FxxA8H
0	Fxx40H	12	FxxA0H

Remark xx: Value set in DTCBAR register

24.3.3 Vector table

When the DTC is activated, one control data is selected according to the data read from the vector table which has been assigned to each activation source, and the selected control data is read from the DTC control data area.

Table 24 - 5 lists the DTC Activation Sources and Vector Addresses. A one byte of the DTC vector table is assigned to each activation source, and data from 40H to F8H is stored in each area to select one of the 24 control data sets. The higher 8 bits for the DTC vector address are set by the DTCBAR register, and 00H to 1EH are allocated to the lower 8 bits corresponding to the DTC activation source.

Caution Change the start address of the DTC control data area to be set in the vector table when the corresponding bit among bits DTCENi0 to DTCENi7 (i = 0 to 4) in the DTCENi register is set to 0 (activation disabled).

Table 24 - 5 DTC Activation Sources and Vector Addresses

DTC Activation Source (Interrupt Request Source)	Source No.	DTC Vector Address	Priority
Reserved	0	Address set in DTCBAR register +00H	Highest
INTP0	1	Address set in DTCBAR register +01H	
INTP1	2	Address set in DTCBAR register +02H	
INTP2	3	Address set in DTCBAR register +03H	
INTP3	4	Address set in DTCBAR register +04H	
INTP4	5	Address set in DTCBAR register +05H	
INTP5	6	Address set in DTCBAR register +06H	
INTP6 Note 1	7	Address set in DTCBAR register +07H	
INTP7 Note 2	8	Address set in DTCBAR register +08H	
Reserved	9	Address set in DTCBAR register +09H	
10-bit A/D conversion end	10	Address set in DTCBAR register +0AH	
UART0 reception transfer end	11	Address set in DTCBAR register +0BH	
UART0 transmission transfer end/CSI00 transfer end or buffer empty/IIC00 transfer end	12	Address set in DTCBAR register +0CH	
UART1 reception transfer end	13	Address set in DTCBAR register +0DH	
UART1 transmission transfer end/CSI10 transfer end or buffer empty/IIC10 transfer end	14	Address set in DTCBAR register +0EH	
UART2 reception transfer end	15	Address set in DTCBAR register +0FH	
UART2 transmission transfer end/CSI20 transfer end or buffer empty/IIC20 transfer end	16	Address set in DTCBAR register +10H	
UARTMG0 reception transfer end Note 3	17	Address set in DTCBAR register +11H	
UARTMG0 transmission transfer end or buffer empty Note 3	18	Address set in DTCBAR register +12H	
End of channel 0 of timer array unit 0 count or capture	19	Address set in DTCBAR register +13H	
End of channel 1 of timer array unit 0 count or capture	20	Address set in DTCBAR register +14H	
End of channel 2 of timer array unit 0 count or capture	21	Address set in DTCBAR register +15H	
End of channel 3 of timer array unit 0 count or capture	22	Address set in DTCBAR register +16H	
End of channel 4 of timer array unit 0 count or capture	23	Address set in DTCBAR register +17H	
End of channel 5 of timer array unit 0 count or capture	24	Address set in DTCBAR register +18H	
End of channel 6 of timer array unit 0 count or capture	25	Address set in DTCBAR register +19H	
End of channel 7 of timer array unit 0 count or capture	26	Address set in DTCBAR register +1AH	
Compare match of 12-bit interval timer	27	Address set in DTCBAR register +1BH	
Compare match of 8-bit interval timer channel 00 (at 8-bit or 16-bit timer operation)	28	Address set in DTCBAR register +1CH	
Compare match of 8-bit interval timer channel 01	29	Address set in DTCBAR register +1DH	
Compare match of 8-bit interval timer channel 10 (at 8-bit or 16-bit timer operation) Note 3	30	Address set in DTCBAR register +1EH	
Compare match of 8-bit interval timer channel 11 Note 3	31	Address set in DTCBAR register +1FH	
Compare match of 8-bit interval timer channel 20 (at 8-bit or 16-bit timer operation) Note 3	32	Address set in DTCBAR register +20H	
Compare match of 8-bit interval timer channel 21 Note 3	33	Address set in DTCBAR register +21H	
Timer RJ0 underflow Note 3	34	Address set in DTCBAR register +22H	
Timer RJ1 underflow Note 3	35	Address set in DTCBAR register +23H	
External signal sampler edge detection Note 3	36	Address set in DTCBAR register +24H	Lowest

(**Notes** are listed on the next page.)

Note 1. R5F11NM, R5F11PL, R5F11NG, and R5F11RM only.
Note 2. R5F11NM and R5F11RM only.
Note 3. R5F11RM only.

24.3.4 Peripheral enable register 1 (PER1)

The PER1 register is used to enable or disable supplying the clock to the peripheral hardware. Clock supply to the hardware that is not used is also stopped so as to decrease the power consumption and noise.
When using the DTC, be sure to set bit 3 (DTCEN) to 1.

The PER1 register can be set by a 1-bit or 8-bit memory manipulation instruction.
Reset signal generation clears this register to 00H.

Figure 24 - 4 Format of Peripheral enable register 1 (PER1)

Address: F007AH After reset: 00H R/W

Symbol	<7>	6	5	<4>	<3>	2	<1>	<0>
PER1	TMKAEN	0	0	AMPEN Note	DTCEN	PGAEN Note	AFEEN Note	DACEN Note

DTCEN	Control of DTC input clock supply
0	Stops input clock supply. • DTC cannot run.
1	Enables input clock supply. • DTC can run.

Note R5F11N and R5F11P only.

Caution **Be sure to set the following bits to 0.**
R5F11N, R5F11P: bits 5 and 6
R5F11R: bits 0 to 2, 4 to 6

24.3.5 DTC control register j (DTCCRj) (j = 0 to 23)

The DTCCRj register is used to control the DTC operating mode.

Figure 24 - 5 Format of DTC control register j (DTCCRj)

Address: Refer to **24.3.2 Control data allocation**. After reset: Undefined R/W

Symbol	7	6	5	4	3	2	1	0
DTCCRj	0	SZ	RPTINT	CHNE	DAMOD	SAMOD	RPTSEL	MODE

SZ	Data size selection
0	8 bits
1	16 bits

RPTINT	Enabling/disabling repeat mode interrupts
0	Interrupt generation disabled
1	Interrupt generation enabled
The setting of the RPTINT bit is invalid when the MODE bit is 0 (normal mode).	

CHNE	Enabling/disabling chain transfers
0	Chain transfers disabled
1	Chain transfers enabled
Set the CHNE bit in the DTCCR23 register to 0 (chain transfers disabled).	

DAMOD	Transfer destination address control
0	Fixed
1	Incremented
The setting of the DAMOD bit is invalid when the MODE bit is 1 (repeat mode) and the RPTSEL bit is 0 (transfer destination is the repeat area).	

SAMOD	Transfer source address control
0	Fixed
1	Incremented
The setting of the SAMOD bit is invalid when the MODE bit is 1 (repeat mode) and the RPTSEL bit is 1 (transfer source is the repeat area).	

RPTSEL	Repeat area selection
0	Transfer destination is the repeat area
1	Transfer source is the repeat area
The setting of the RPTSEL bit is invalid when the MODE bit is 0 (normal mode).	

MODE	Transfer mode selection
0	Normal mode
1	Repeat mode

Caution Do not access the DTCCRj register using a DTC transfer.

24.3.6 DTC block size register j (DTBLSj) (j = 0 to 23)

This register is used to set the block size of the data to be transferred by one activation.

Figure 24 - 6 Format of DTC block size register j (DTBLSj)

Address: Refer to **24.3.2 Control data allocation**. After reset: Undefined R/W

Symbol	7	6	5	4	3	2	1	0
DTBLSj	DTBLSj7	DTBLSj6	DTBLSj5	DTBLSj4	DTBLSj3	DTBLSj2	DTBLSj1	DTBLSj0

DTBLSj	Transfer Block Size	
	8-Bit Transfer	16-Bit Transfer
00H	256 bytes	512 bytes
01H	1 byte	2 bytes
02H	2 bytes	4 bytes
03H	3 bytes	6 bytes
• • •	• • •	• • •
FDH	253 bytes	506 bytes
FEH	254 bytes	508 bytes
FFH	255 bytes	510 bytes

Caution Do not access the DTBLSj register using a DTC transfer.

24.3.7 DTC transfer count register j (DTCCTj) (j = 0 to 23)

This register is used to set the number of DTC data transfers. The value is decremented by 1 each time DTC transfer is activated once.

Figure 24 - 7 Format of DTC transfer count register j (DTCCTj)

Address: Refer to **24.3.2 Control data allocation**. After reset: Undefined R/W

Symbol	7	6	5	4	3	2	1	0
DTCCTj	DTCCTj7	DTCCTj6	DTCCTj5	DTCCTj4	DTCCTj3	DTCCTj2	DTCCTj1	DTCCTj0

DTCCTj	Number of Transfers
00H	256 times
01H	Once
02H	2 times
03H	3 times
• • •	• • •
FDH	253 times
FEH	254 times
FFH	255 times

Caution Do not access the DTCCTj register using a DTC transfer.

24.3.8 DTC transfer count reload register j (DTRLDj) (j = 0 to 23)

This register is used to set the initial value of the transfer count register in repeat mode. Since the value of this register is reloaded to the DTCCT register in repeat mode, set the same value as the initial value of the DTCCT register.

Figure 24 - 8 Format of DTC transfer count reload register j (DTRLDj)

Address: Refer to **24.3.2 Control data allocation**. After reset: Undefined R/W

	7	6	5	4	3	2	1	0
DTRLDj	DTRLDj7	DTRLDj6	DTRLDj5	DTRLDj4	DTRLDj3	DTRLDj2	DTRLDj1	DTRLDj0

Caution Do not access the DTRLDj register using a DTC transfer.

24.3.9 DTC source address register j (DTSARj) (j = 0 to 23)

This register is used to specify the transfer source address for data transfer.

When the SZ bit in the DTCCRj register is set to 1 (16-bit transfer), the lowest bit is ignored and the address is handled as an even address.

Figure 24 - 9 Format of DTC source address register j (DTSARj)

Address: Refer to **24.3.2 Control data allocation**. After reset: Undefined R/W

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DTSARj	DTS ARj15	DTS ARj14	DTS ARj13	DTS ARj12	DTS ARj11	DTS ARj10	DTS ARj9	DTS ARj8	DTS ARj7	DTS ARj6	DTS ARj5	DTS ARj4	DTS ARj3	DTS ARj2	DTS ARj1	DTS ARj0

Caution 1. Do not set the general-purpose register (FFEE0H to FFEFFH) space to the transfer source address.
Caution 2. Do not access the DTSARj register using a DTC transfer.

24.3.10 DTC destination address register j (DTDARj) (j = 0 to 23)

This register is used to specify the transfer destination address for data transfer.

When the SZ bit in the DTCCRj register is set to 1 (16-bit transfer), the lowest bit is ignored and the address is handled as an even address.

Figure 24 - 10 Format of DTC destination address register j (DTDARj)

Address: Refer to **24.3.2 Control data allocation**. After reset: Undefined R/W

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DTDARj	DTD ARj15	DTD ARj14	DTD ARj13	DTD ARj12	DTD ARj11	DTD ARj10	DTD ARj9	DTD ARj8	DTD ARj7	DTD ARj6	DTD ARj5	DTD ARj4	DTD ARj3	DTD ARj2	DTD ARj1	DTD ARj0

Caution 1. Do not set the general-purpose register (FFEE0H to FFEFFH) space to the transfer source address.
Caution 2. Do not access the DTDARj register using a DTC transfer.

24.3.11 DTC activation enable register i (DTCENi) (i = 0 to 4)

This is an 8-bit register which enables or disables DTC activation by interrupt sources. **Table 24 - 6** lists the Correspondences between Interrupt Sources and Bits DTCENi0 to DTCENi7.

The DTCENi register can be set by an 8-bit memory manipulation instruction and a 1-bit memory manipulation instruction.

Caution 1. Modify bits DTCENi0 to DTCENi7 if an activation source corresponding to the bit has not been generated.

Caution 2. Do not access the DTCENi register using a DTC transfer.

Figure 24 - 11 Format of DTC activation enable register i (DTCENi) (i = 0 to 4) (1/2)

Address: F02E8H (DTCEN0), F02E9H (DTCEN1), F02EAH (DTCEN2), F02EBH (DTCEN3), F02ECH(DTCEN4) Note — After reset: 00H — R/W

Symbol	7	6	5	4	3	2	1	0
DTCENi	DTCENi7	DTCENi6	DTCENi5	DTCENi4	DTCENi3	DTCENi2	DTCENi1	DTCENi0

DTCENi7	DTC activation enable i7
0	Activation disabled
1	Activation enabled
The DTCENi7 bit is set to 0 (activation disabled) by a condition for generating a transfer end interrupt.	

DTCENi6	DTC activation enable i6
0	Activation disabled
1	Activation enabled
The DTCENi6 bit is set to 0 (activation disabled) by a condition for generating a transfer end interrupt.	

DTCENi5	DTC activation enable i5
0	Activation disabled
1	Activation enabled
The DTCENi5 bit is set to 0 (activation disabled) by a condition for generating a transfer end interrupt.	

DTCENi4	DTC activation enable i4
0	Activation disabled
1	Activation enabled
The DTCENi4 bit is set to 0 (activation disabled) by a condition for generating a transfer end interrupt.	

DTCENi3	DTC activation enable i3
0	Activation disabled
1	Activation enabled
The DTCENi3 bit is set to 0 (activation disabled) by a condition for generating a transfer end interrupt.	

Note R5F11R only.

Figure 24 - 11 Format of DTC activation enable register i (DTCENi) (i = 0 to 4) (2/2)

Address: F02E8H (DTCEN0), F02E9H (DTCEN1), F02EAH (DTCEN2), F02EBH (DTCEN3), F02ECH(DTCEN4) Note — After reset: 00H — R/W

Symbol	7	6	5	4	3	2	1	0
DTCENi	DTCENi7	DTCENi6	DTCENi5	DTCENi4	DTCENi3	DTCENi2	DTCENi1	DTCENi0

DTCENi2	DTC activation enable i2
0	Activation disabled
1	Activation enabled
The DTCENi2 bit is set to 0 (activation disabled) by a condition for generating a transfer end interrupt.	

DTCENi1	DTC activation enable i1
0	Activation disabled
1	Activation enabled
The DTCENi1 bit is set to 0 (activation disabled) by a condition for generating a transfer end interrupt.	

DTCENi0	DTC activation enable i0
0	Activation disabled
1	Activation enabled
The DTCENi0 bit is set to 0 (activation disabled) by a condition for generating a transfer end interrupt.	

Note R5F11R only.

Table 24 - 6 Correspondences between Interrupt Sources and Bits DTCENi0 to DTCENi7

Register	DTCENi7 Bit	DTCENi6 Bit	DTCENi5 Bit	DTCENi4 Bit	DTCENi3 Bit	DTCENi2 Bit	DTCENi1 Bit	DTCENi0 Bit
DTCEN0	Reserved	INTP0	INTP1	INTP2	INTP3	INTP4	INTP5	INTP6 Note 1
DTCEN1	INTP7 Note 2	Reserved	10-bit A/D conversion end	UART0 reception transfer end	UART0 transmission transfer end/CSI00 transfer end or buffer empty/IIC00 transfer end	UART1 reception transfer end	UART1 transmission transfer end/CSI10 transfer end or buffer empty/IIC10 transfer end	UART2 reception transfer end
DTCEN2	UART2 transmission transfer end/CSI20 transfer end or buffer empty/IIC20 transfer end	UARTMG0 transmission transfer end Note 3	UARTMG0 transmission transfer end or buffer empty Note 3	End of channel 0 of timer array unit 0 count or capture	End of channel 1 of timer array unit 0 count or capture	End of channel 2 of timer array unit 0 count or capture	End of channel 3 of timer array unit 0 count or capture	End of channel 4 of timer array unit 0 count or capture
DTCEN3	End of channel 5 of timer array unit 0 count or capture	End of channel 6 of timer array unit 0 count or capture	End of channel 7 of timer array unit 0 count or capture	Compare match of 12-bit interval timer	Compare match of 8-bit interval timer channel 00 (at 8-bit or 16-bit timer operation)	Compare match of 8-bit interval timer channel 01	Compare match of 8-bit interval timer channel 10 (at 8-bit or 16-bit timer operation) Note 3	Compare match of 8-bit interval timer channel 11 Note 3
DTCEN4	Compare match of 8-bit interval timer channel 20 (at 8-bit or 16-bit timer operation) Note 3	Compare match of 8-bit interval timer channel 21 Note 3	Timer RJ0 underflow Note 3	Timer RJ1 underflow Note 3	External signal sampler edge detection Note 3	Reserved	Reserved	Reserved

Note 1. R5F11NM, R5F11PL, R5F11NG, and R5F11RM only.
Note 2. R5F11NM and R5F11RM only.
Note 3. R5F11RM only.

Remark i = 0 to 4

24.3.12 DTC base address register (DTCBAR)

This is an 8-bit register used to set the following addresses: the vector address where the start address of the DTC control data area is stored and the address of the DTC control data area. The value of the DTCBAR register is handled as the higher 8 bits to generate a 16-bit address.

Caution 1. Change the DTCBAR register value with all DTC activation sources set to activation disabled.
Caution 2. Do not rewrite the DTCBAR register more than once.
Caution 3. Do not access the DTCBAR register using a DTC transfer.
Caution 4. For the allocation of the DTC control data area and the DTC vector table area, refer to the notes on 24.3.1 Allocation of DTC control data area and DTC vector table area.

Figure 24 - 12 Format of DTC base address register (DTCBAR)

Address: F02E0H After reset: FDH R/W

Symbol	7	6	5	4	3	2	1	0
DTCBAR	DTCBAR7	DTCBAR6	DTCBAR5	DTCBAR4	DTCBAR3	DTCBAR2	DTCBAR1	DTCBAR0

24.4 DTC Operation

When the DTC is activated, control data is read from the DTC control data area to perform data transfers and control data after data transfer is written back to the DTC control data area. Twenty-four sets of control data can be stored in the DTC control data area, which allows 24 types of data transfers to be performed.

There are two transfer modes (normal mode and repeat mode) and two transfer sizes (8-bit transfer and 16-bit transfer). When the CHNE bit in the DTCCRj (j = 0 to 23) register is set to 1 (chain transfers enabled), multiple control data is read and data transfers are continuously performed by one activation source (chain transfers).

A transfer source address is specified by the 16-bit register DTSARj, and a transfer destination address is specified by the 16-bit register DTDARj.

The values in registers DTSARj and DTDARj are separately incremented or fixed according to the control data after the data transfer.

24.4.1 Activation sources

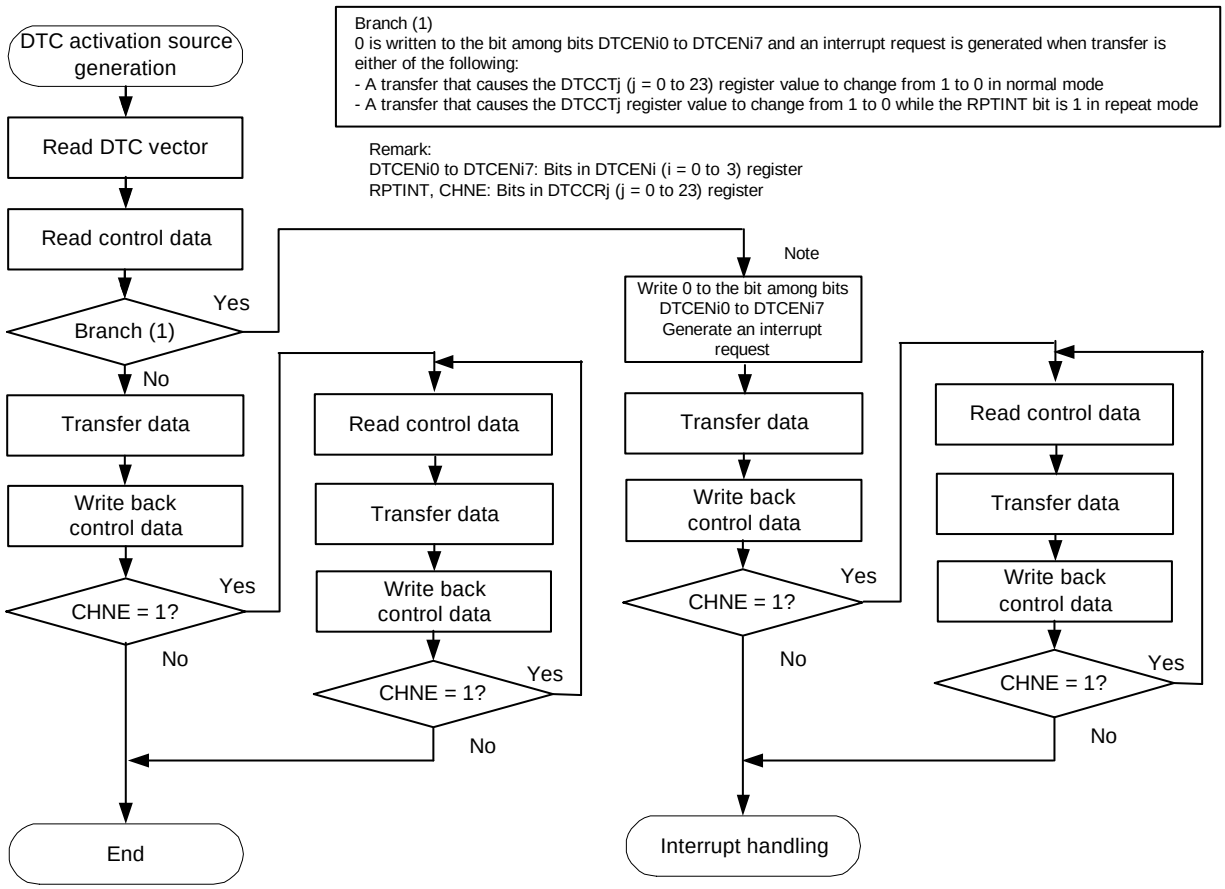
The DTC is activated by an interrupt signal from the peripheral functions. The interrupt signals to activate the DTC are selected with the DTCENi (i = 0 to 4) register.

The DTC sets the corresponding bit among bits DTCENi0 to DTCENi7 in the DTCENi register to 0 (activation disabled) during operation when the setting of data transfer (the first transfer in chain transfers) is either of the following:

- A transfer that causes the DTCCTj (j = 0 to 23) register value to change to 0 in normal mode
- A transfer that causes the DTCCTj register value to change to 0 while the RPTINT bit in the DTCCRj register is 1 (interrupt generation enabled) in repeat mode

Figure 24 - 13 shows the DTC Internal Operation Flowchart.

Figure 24 - 13 DTC Internal Operation Flowchart



Note 0 is not written to the bit among bits DTCENi0 to DTCENi7 for data transfers activated by the setting to enable chain transfers (the CHNE bit is 1). Also, no interrupt request is generated.

24.4.2 Normal mode

One to 256 bytes of data are transferred by one activation during 8-bit transfer and 2 to 512 bytes during 16-bit transfer. The number of transfers can be 1 to 256 times. When the data transfer causing the DTCCTj (j = 0 to 23) register value to change to 0 is performed, the DTC generates an interrupt request corresponding to the activation source to the interrupt controller during DTC operation, and sets the corresponding bit among bits DTCENi0 to DTCENi (i = 0 to 4) in the DTCENi register to 0 (activation disabled).

Table 24 - 7 lists Register Functions in Normal Mode. **Figure 24 - 14** shows Data Transfers in Normal Mode.

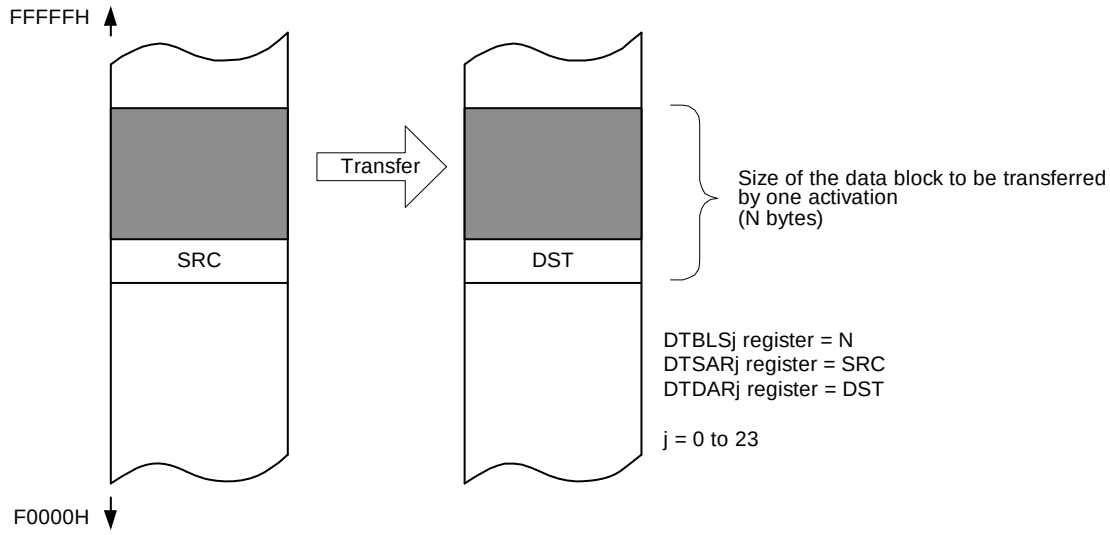
Table 24 - 7 Register Functions in Normal Mode

Register Name	Symbol	Function
DTC block size register j	DTBLSj	Size of the data block to be transferred by one activation
DTC transfer count register j	DTCCTj	Number of data transfers
DTC transfer count reload register j	DTRLDj	Not used Note
DTC source address register j	DTSARj	Data transfer source address
DTC destination address register j	DTDARj	Data transfer destination address

Note Initialize this register to 00H when parity error resets are enabled (RPERDIS = 0) using the RAM parity error detection function.

Remark j = 0 to 23

Figure 24 - 14 Data Transfers in Normal Mode



DTCCR Register Setting				Source Address Control	Destination Address Control	Source Address after Transfer	Destination Address after Transfer
DAMOD	SAMOD	RPTSEL	MODE				
0	0	X	0	Fixed	Fixed	SRC	DST
0	1	X	0	Incremented	Fixed	SRC + N	DST
1	0	X	0	Fixed	Incremented	SRC	DST + N
1	1	X	0	Incremented	Incremented	SRC + N	DST + N

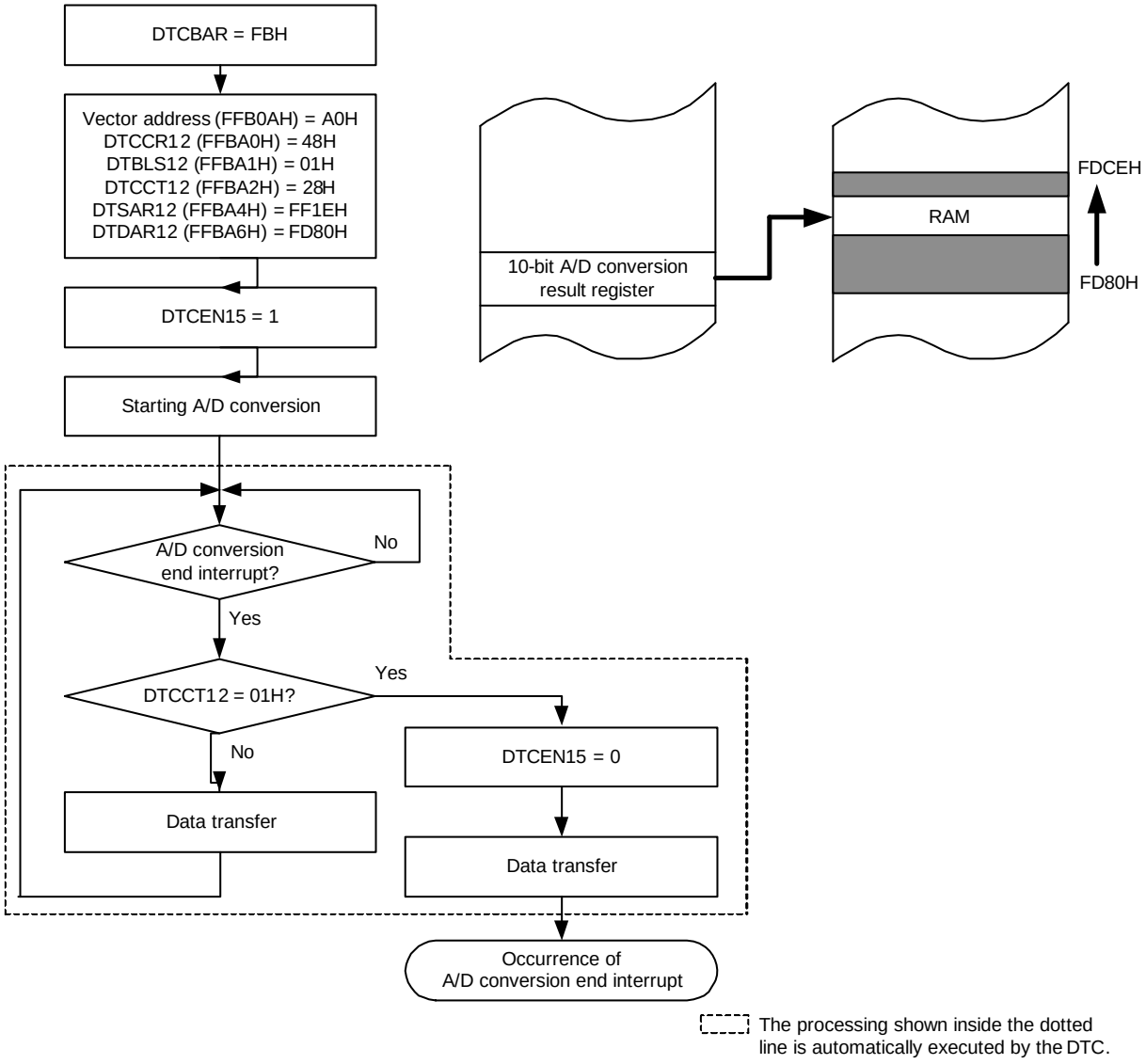
X: 0 or 1

(1) Example 1 of using normal mode: Consecutively capturing 10-bit A/D conversion results

The DTC is activated by an A/D conversion end interrupt and the value of the 10-bit A/D conversion result register is transferred to RAM.

- The vector address is FFB0AH and control data is allocated at FFBA0H to FFBA7H
- Transfers 2-byte data of the 10-bit A/D conversion results register (FFF1EH, FFF1FH) to 80 bytes of FFD80H to FFDCFH of RAM

Figure 24 - 15 Example 1 of using normal mode: Consecutively capturing 10-bit A/D conversion results



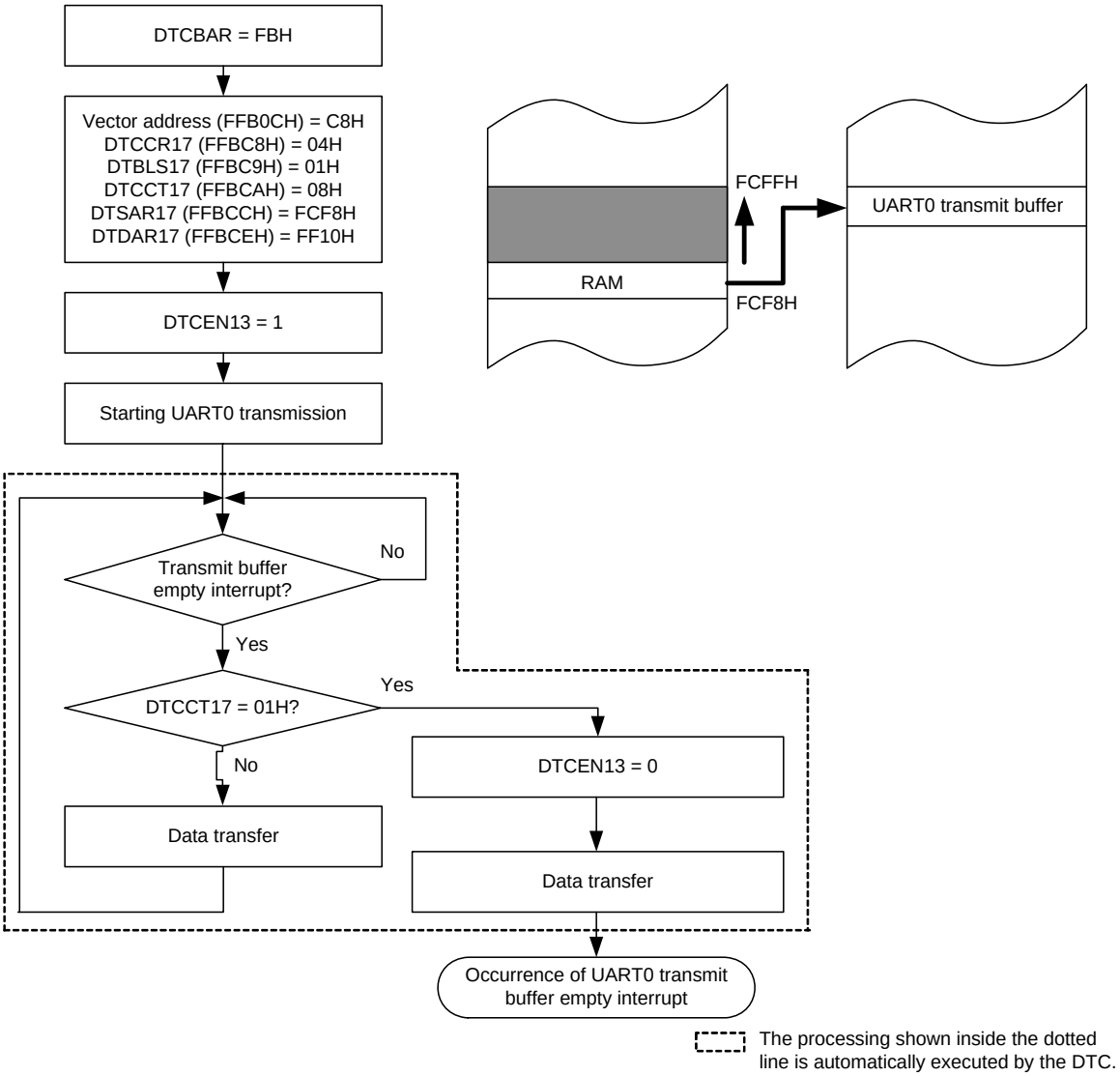
The value of the DTRLD12 register is not used because of normal mode, but initialize the register to 00H when parity error resets are enabled (RPERDIS = 0) using the RAM parity error detection function.

(2) Example 2 of using normal mode: UART consecutive transmission

The DTC is activated by a UART0 transmit buffer empty interrupt and the value of RAM is transferred to the UART0 transmit buffer.

- The vector address is FFB0CH and control data is allocated at FFBC8H to FFBCFH
- Transfers 8 bytes of FFCF8H to FFCFFH of RAM to the UART0 transmit buffer (FFF10H)

Figure 24 - 16 Example 2 of using normal mode: UART0 consecutive transmission



The value of the DTRLD17 register is not used because of normal mode, but initialize the register to 00H when parity error resets are enabled (RPERDIS = 0) using the RAM parity error detection function.

Start the first UART0 transmission by software. The second and subsequent transmissions are automatically sent when the DTC is activated by a transmit buffer empty interrupt.

24.4.3 Repeat mode

One to 255 bytes of data are transferred by one activation. Either of the transfer source or destination should be specified as the repeat area. The number of transfers can be 1 to 255 times. On completion of the specified number of transfers, the DTCCTj (j = 0 to 23) register and the address specified for the repeat area are initialized to continue transfers. When the data transfer causing the DTCCTj register value to change to 0 is performed while the RPTINT bit in the DTCCRj register is 1 (interrupt generation enabled), the DTC generates an interrupt request corresponding to the activation source to the interrupt controller during DTC operation, and sets the corresponding bit among bits DTCENi0 to DTCENi7 in the DTCENi (i = 0 to 4) register to 0 (activation disabled). When the RPTINT bit in the DTCCRj register is 0 (interrupt generation disabled), no interrupt request is generated even if the data transfer causing the DTCCTj register value to change to 0 is performed. Also, bits DTCENi0 to DTCENi7 are not set to 0.

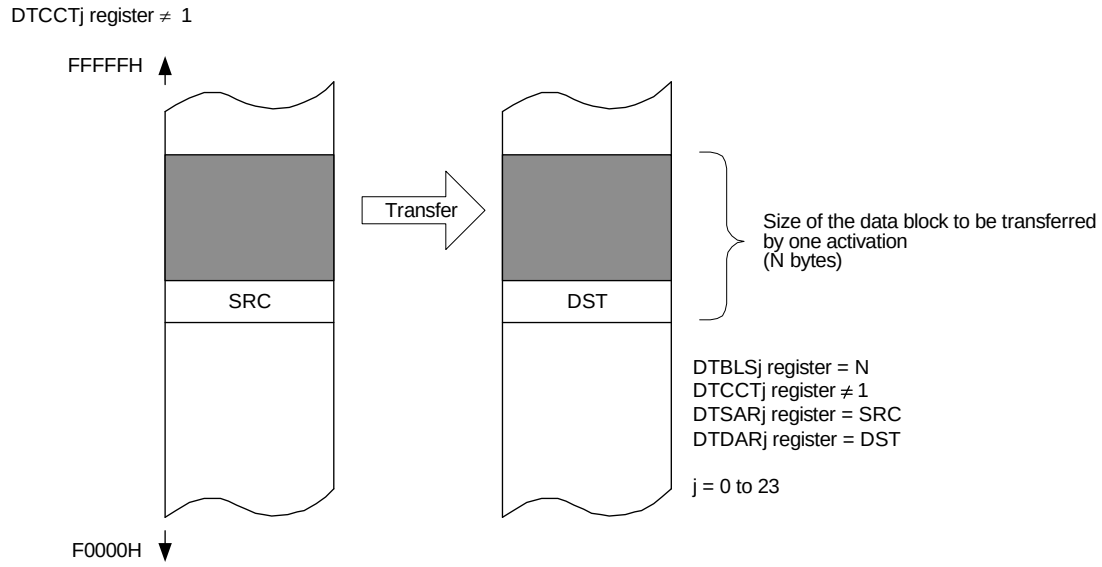
Table 24 - 8 lists Register Functions in Repeat Mode. **Figure 24 - 17** shows Data Transfers in Repeat Mode.

Table 24 - 8 Register Functions in Repeat Mode

Register Name	Symbol	Function
DTC block size register j	DTBLSj	Size of the data block to be transferred by one activation
DTC transfer count register j	DTCCTj	Number of data transfers
DTC transfer count reload register j	DTRLDj	This register value is reloaded to the DTCCT register (the number of transfers is initialized).
DTC source address register j	DTSARj	Data transfer source address
DTC destination address register j	DTDARj	Data transfer destination address

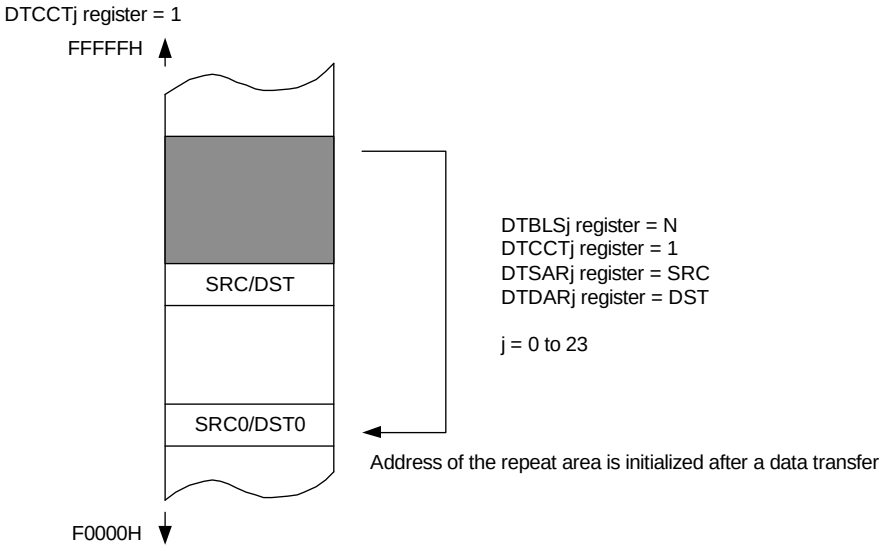
Remark j = 0 to 23

Figure 24 - 17 Data Transfers in Repeat Mode



DTCCR Register Setting				Source Address Control	Destination Address Control	Source Address after Transfer	Destination Address after Transfer
DAMOD	SAMOD	RPTSEL	MODE				
0	X	1	1	Repeat area	Fixed	SRC + N	DST
1	X	1	1	Repeat area	Incremented	SRC + N	DST + N
X	0	0	1	Fixed	Repeat area	SRC	DST + N
X	1	0	1	Incremented	Repeat area	SRC + N	DST + N

X: 0 or 1



DTCCR Register Setting				Source Address Control	Destination Address Control	Source Address after Transfer	Destination Address after Transfer
DAMOD	SAMOD	RPTSEL	MODE				
0	X	1	1	Repeat area	Fixed	SRC0	DST
1	X	1	1	Repeat area	Incremented	SRC0	DST + N
X	0	0	1	Fixed	Repeat area	SRC	DST0
X	1	0	1	Incremented	Repeat area	SRC + N	DST0

SRC0: Initial source address value
DST0: Initial destination address value
X: 0 or 1

Caution 1. When repeat mode is used, the lower 8 bits of the initial value for the repeat area address must be 00H.

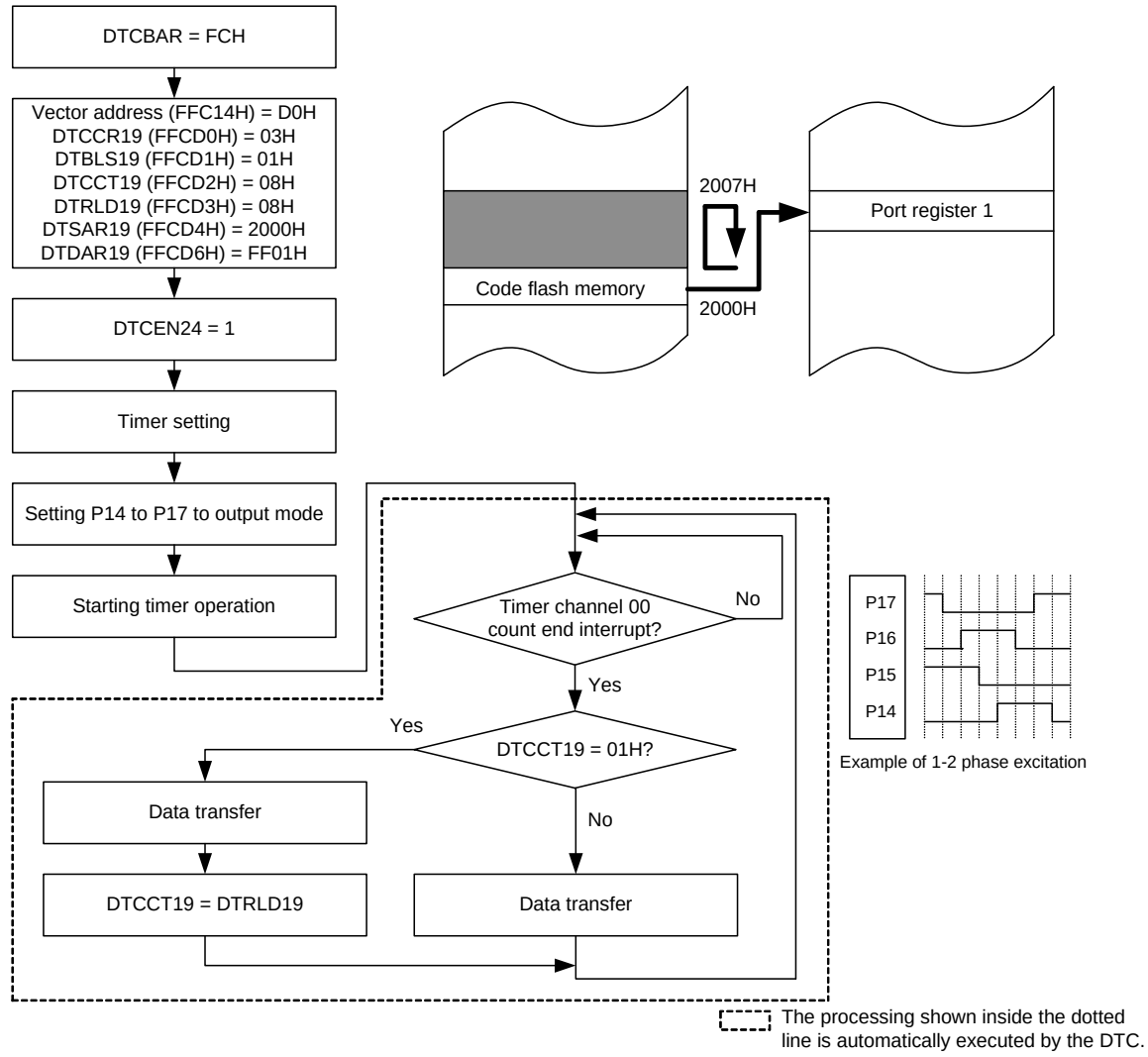
Caution 2. When repeat mode is used, the data size of the repeat area must be set to 255 bytes or less.

(1) Example 1 of using repeat mode: Outputting a stepping motor control pulse using ports

The DTC is activated using the interval timer function of channel 0 of timer array unit 0, and the pattern of the motor control pulse stored in the code flash memory is transferred to the general-purpose port.

- The vector address is FFC14H and control data is allocated at FFCD0H to FFCD7H
- Transfers 8-byte data of 02000H to 02007H of the code flash memory from the mirror space (F2000H to F2007H) to port register 1 (FFF01H)
- A repeat mode interrupt is disabled

Figure 24 - 18 Example 1 of using repeat mode: Outputting a stepping motor control pulse using ports



To stop the output, stop the timer first and then clear DTCEN24.

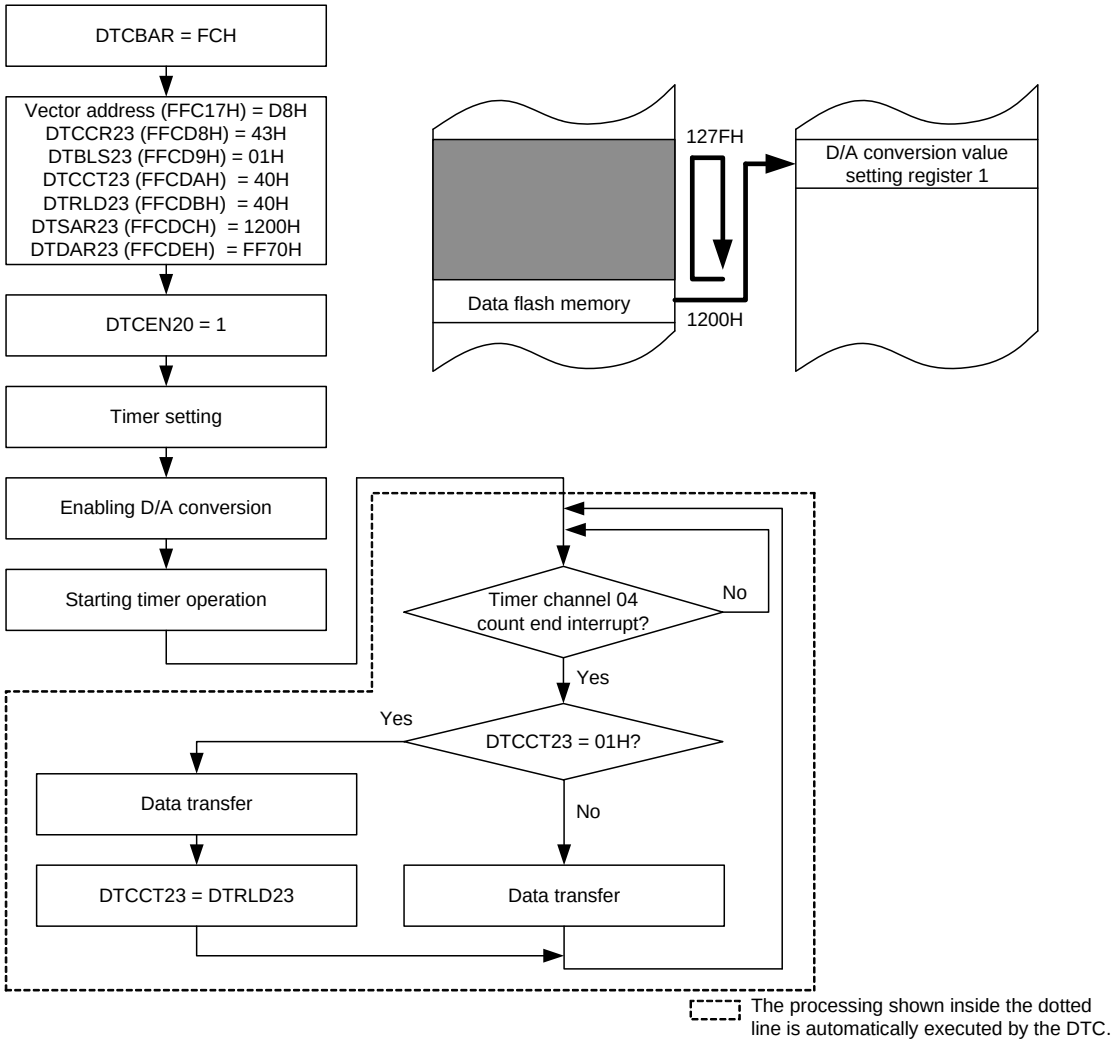
(2) Example 2 of using repeat mode: Outputting a sine wave using the 12-bit D/A converter

The DTC is activated using the interval timer function of channel 4 of timer array unit 0, and the table of the sine wave stored in the data flash memory is transferred to the D/A conversion value setting register 1 (F0482H).

The timer interval time is set to the D/A output setup time.

- The vector address is FFC17H and control data is allocated at FFCD8H to FFCDFH
- Transfers 128-byte data of F1200H to F127FH of the data flash memory to the D/A conversion value setting register 1 (F0482H)
- A repeat mode interrupt is disabled

Figure 24 - 19 Example 2 of using repeat mode: Outputting a sine wave using the 12-bit D/A converter



To stop the output, stop the timer first and then clear DTCEN20.

24.4.4 Chain transfers

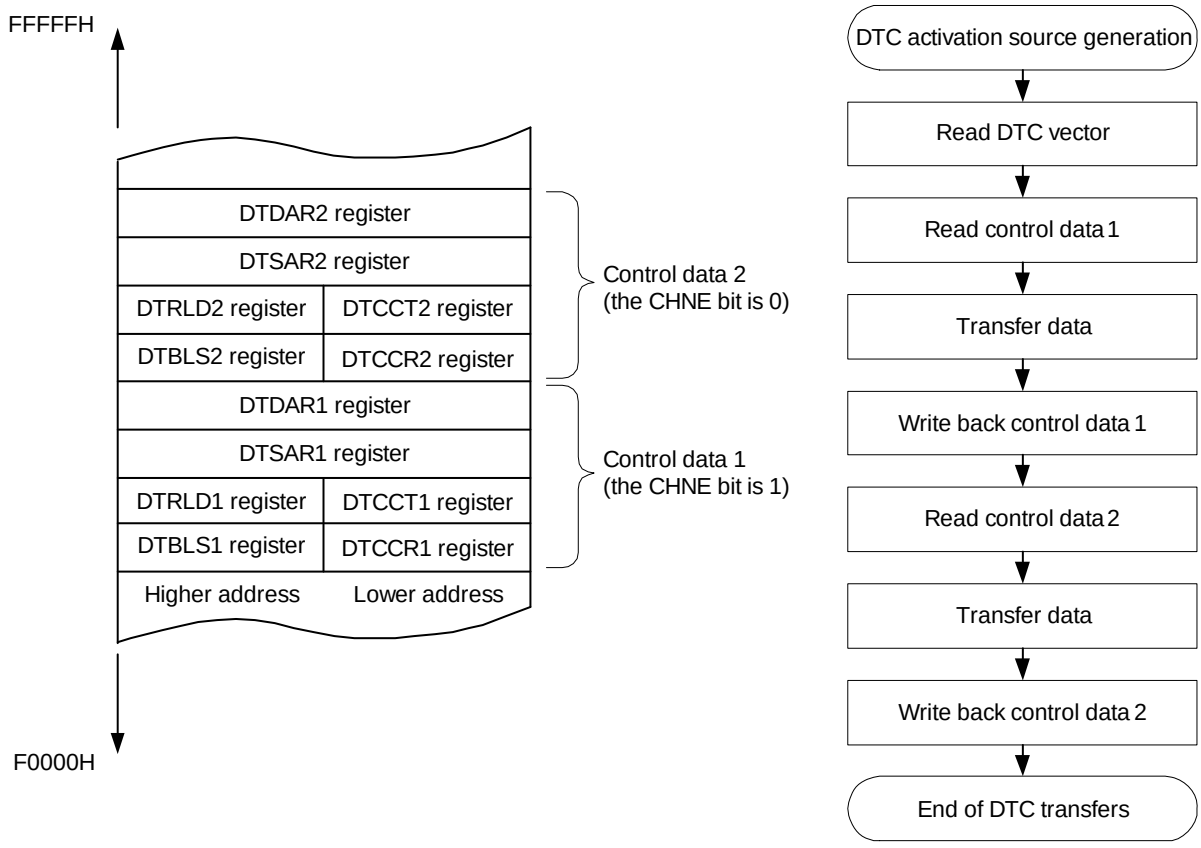
When the CHNE bit in the DTCCRj (j = 0 to 22) register is 1 (chain transfers enabled), multiple data transfers can be continuously performed by one activation source.

When the DTC is activated, one control data is selected according to the data read from the vector address corresponding to the activation source, and the selected control data is read from the DTC control data area. When the CHNE bit for the control data is 1 (chain transfers enabled), the next control data immediately following the current control data is read and transferred after the current transfer is completed. This operation is repeated until the data transfer with the control data for which the CHNE bit is 0 (chain transfers disabled) is completed.

When chain transfers are performed using multiple control data, the number of transfers set for the first control data is enabled, and the number of transfers set for the second and subsequent control data to be processed will be invalid.

Figure 24 - 20 shows Data Transfers during Chain Transfers.

Figure 24 - 20 Data Transfers during Chain Transfers



Caution 1. Set the CHNE bit in the DTCCR23 register to 0 (chain transfers disabled).

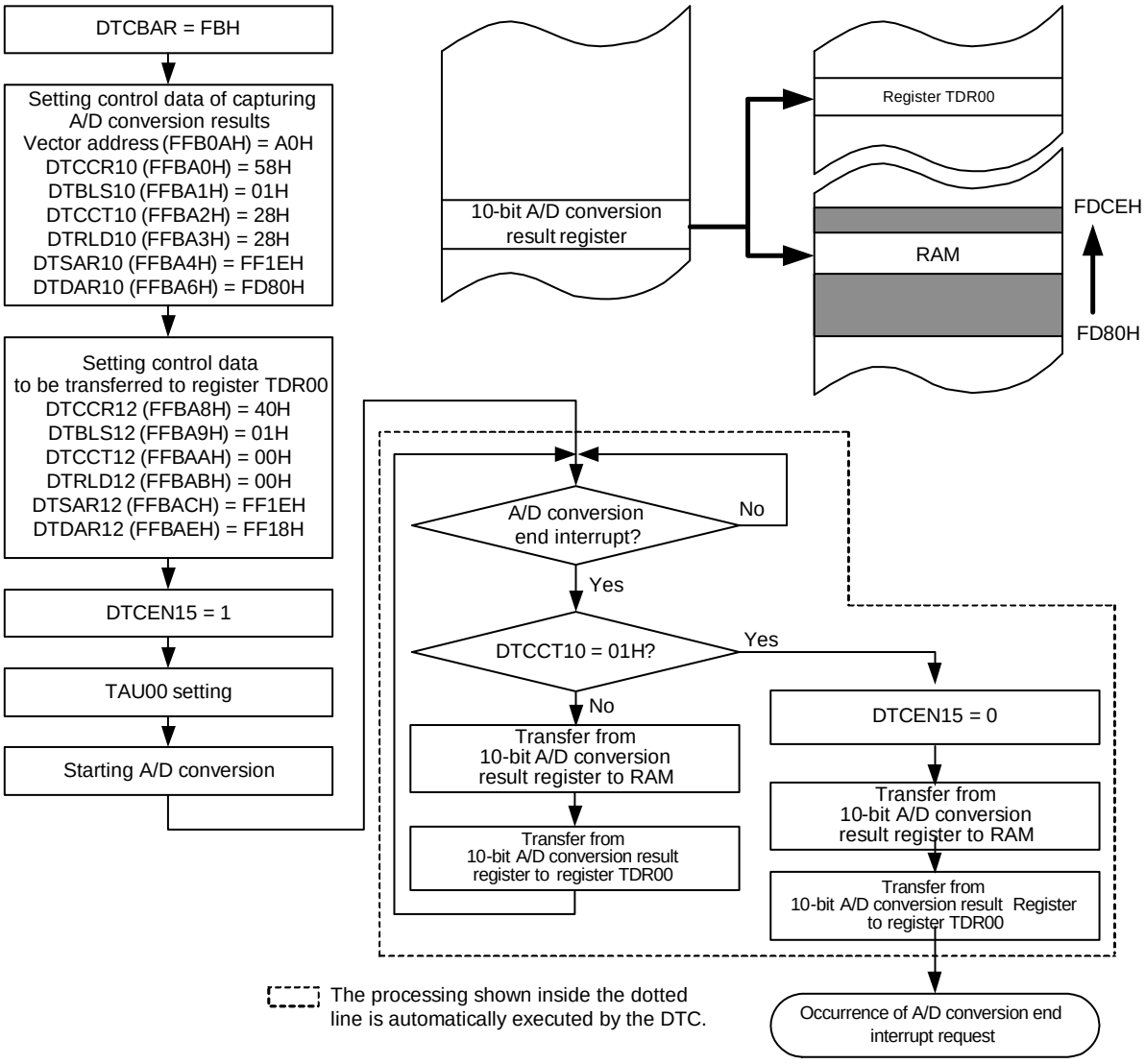
Caution 2. During chain transfers, bits DTCENi0 to DTCENi7 (i = 0 to 4) in the DTCENi register are not set to 0 (activation disabled) for the second and subsequent transfers. Also, no interrupt request is generated.

(1) Example of using chain transfers: Consecutively capturing 10-bit A/D conversion results and transferring to the timer data register 00 (TDR00)

The DTC is activated by an A/D conversion end interrupt and A/D conversion results are transferred to RAM, and then transferred to the register TDR00.

- The vector address is FFB0AH
- Control data of capturing A/D conversion results is allocated at FFBA0H to FFBA7H
- Control data to be transferred to the register TDR00 is allocated at FFBA8H at FFBAFH
- Transfers 2-byte data of the 10-bit A/D conversion result register (FFF1EH, FFF1FH) to FFD80H to FFDCFH of RAM, and transfers the data of the 10-bit A/D conversion result register (FFF1EH, FFF1FH) to the register TDR00 (FFF18H, FFF19H)

Figure 24 - 21 Example of using chain transfers: Consecutively capturing 10-bit A/D conversion results and transferring to TDR00



24.5 Notes on DTC

24.5.1 Setting DTC registers and vector table

- Do not access the DTC extended special function register (2nd SFR), the DTC control data area, the DTC vector table area, or the general-register (FFEE0H to FFEFFH) space using a DTC transfer.
- Modify the DTC base address register (DTCBAR) while all DTC activation sources are set to activation disabled.
- Do not rewrite the DTC base address register (DTCBAR) twice or more.
- Modify the data of the DTCCRj, DTBLSj, DTCCTj, DTRLDj, DTSARj, or DTDARj register when the corresponding bit among bits DTCENi0 to DTCENi7 in the DTCENi (i = 0 to 4) register is 0 (activation disabled).
- Modify the start address of the DTC control data area to be set in the vector table when the corresponding bit among bits DTCENi0 to DTCENi7 in the DTCENi (i = 0 to 4) register is 0 (activation disabled).
- Do not allocate RAM addresses which are used as a DTC transfer destination/transfer source to the area FFE20H to FFEDFH when performing self-programming and rewriting the data flash memory.

24.5.2 Allocation of DTC control data area and DTC vector table area

The areas where the DTC control data and vector table can be allocated differ, depending on the usage conditions.

- It is prohibited to use the general-purpose register (FFEE0H to FFEFFH) space as the DTC control data area or DTC vector table area.
- Make sure the stack area, the DTC control data area, and the DTC vector table area do not overlap.
- Initialize the DTRLD register to 00H even in normal mode when parity error resets are enabled (RPERDIS = 0) using the RAM parity error detection function.
- The internal RAM area in the following products cannot be used as the DTC control data area or DTC vector table area when using the self-programming and data-flash functions.
  R5F11RMG: FDF00H to FE309H
- The internal RAM area in the following products cannot be used as the DTC control data area or DTC vector table area when using the on-chip debugging trace function.
  R5F11RMG: FE300H to FE6FFH

24.5.3 DTC pending instruction

Even if a DTC transfer request is generated, DTC transfer is held pending immediately after the following instructions. Also, the DTC is not activated between PREFIX instruction code and the instruction immediately after that code.

- Call/return instruction
- Unconditional branch instruction
- Conditional branch instruction
- Read access instruction for code flash memory
- Bit manipulation instructions for IFxx, MKxx, PRxx, and PSW, and an 8-bit manipulation instruction that has the ES register as operand
- Instruction for accessing the data flash memory
- Instruction of Multiply, Divide, Multiply & Accumulate (excluding MULU)

Caution 1. When a DTC transfer request is acknowledged, all interrupt requests are held pending until DTC transfer is completed.

Caution 2. While the DTC is held pending by the DTC pending instruction, all interrupt requests are held pending.

24.5.4 Operation when accessing data flash memory space

Because DTC data transfer is suspended to access the data flash space, be sure to add the DTC pending instruction.

If the data flash space is accessed after an instruction execution from start of DTC data transfer, a 3-clock wait will be inserted to the next instruction.

```
Instruction 1
DTC data transfer
Instruction ←  The wait of three clock cycles occurs.
MOV A,         ! Data Flash space
```

24.5.5 Number of DTC execution clock cycles

Table 24 - 9 lists the Operations Following DTC Activation and Required Number of Cycles for each operation.

Table 24 - 9 Operations Following DTC Activation and Required Number of Cycles

Vector Read	Control Data		Data Read	Data Write
	Read	Write-back		
1	4	Note 1	Note 2	Note 2

Note 1. For the number of clock cycles required for control data write-back, refer to **Table 24 - 10 Number of Clock Cycles Required for Control Data Write-Back Operation**.

Note 2. For the number of clock cycles required for data read/write, refer to **Table 24 - 11 Number of Clock Cycles Required for One Data Read/Write Operation**.

Table 24 - 10 Number of Clock Cycles Required for Control Data Write-Back Operation

DTCCR Register Setting				Address Setting		Control Register to be Written Back				Number of Clock Cycles
DAMOD	SAMOD	RPTSEL	MODE	Source	Destination	DTCCTj Register	DTRLDj Register	DTSARj Register	DTDARj Register	
0	0	X	0	Fixed	Fixed	Written back	Written back	Not written back	Not written back	1
0	1	X	0	Incremented	Fixed	Written back	Written back	Written back	Not written back	2
1	0	X	0	Fixed	Incremented	Written back	Written back	Not written back	Written back	2
1	1	X	0	Incremented	Incremented	Written back	Written back	Written back	Written back	3
0	X	1	1	Repeat area	Fixed	Written back	Written back	Written back	Not written back	2
1	X	1	1		Incremented	Written back	Written back	Written back	Written back	3
X	0	0	1	Fixed	Repeat area	Written back	Written back	Not written back	Written back	2
X	1	0	1	Incremented		Written back	Written back	Written back	Written back	3

Remark j = 0 to 23; X: 0 or 1

Table 24 - 11 Number of Clock Cycles Required for One Data Read/Write Operation

Operation	RAM	Code Flash Memory	Data Flash Memory	Special function register (SFR)	Extended special function register (2nd SFR)	
					No Wait State	Wait States
Data read	1	2	4	1	1	1 + number of wait states Note
Data write	1	—	—	1	1	1 + number of wait states Note

Note The number of wait states differs depending on the specifications of the register allocated to the extended special function register (2nd SFR) to be accessed.

24.5.6 DTC response time

Table 24 - 12 lists the DTC Response Time. The DTC response time is the time from when the DTC activation source is detected until DTC transfer starts. It does not include the number of DTC execution clocks.

Table 24 - 12 DTC Response Time

	Minimum Time	Maximum Time
Response Time	3 clocks	19 clocks

Note that the response from the DTC may be further delayed under the following cases. The number of delayed clock cycles differs depending on the conditions.

- When executing an instruction from the internal RAM
  Maximum response time: 20 clocks
- When executing a DTC pending instruction (refer to **24.5.3 DTC pending instruction**)
  Maximum response time: Maximum response time for each condition + execution clock cycles for the instruction to be held pending under the condition.
- When accessing the 8-bit interval timer counter register n (TRTn) that a wait occurs
  Maximum response time: Maximum response time for each condition + 1 clock

Remark 1 clock: 1/f_{CLK} (f_{CLK}: CPU/peripheral hardware clock)

24.5.7 DTC activation sources

- After inputting a DTC activation source, do not input the same activation source again until DTC transfer is completed.
- While a DTC activation source is generated, do not manipulate the DTC activation enable bit corresponding to the source.
- When an 8-bit interval timer or the 12-bit interval timer is selected as a DTC activation source and DTC transfer is to proceed again following the completion of a previous DTC transfer activated by the same source, set the corresponding DTCENi0 to DTCENi7 bit in the DTCENi (i = 0 to 4) register to 1 (enabling activation) after one cycle of the operating clock for the timer.
- If DTC activation sources conflict, their priority levels are determined in order to select the source for activation when the CPU acknowledges the DTC transfer. For details on the priority levels of activation sources, refer to **24.3.3 Vector table**.

24.5.8 Operation in standby mode status

Status	DTC Operation
HALT mode	Operable (Operation is disabled while in the low power consumption RTC mode)
STOP mode	DTC activation sources can be accepted Note 2
SNOOZE mode	Operable Notes 1, 3, 4, 5

Note 1. The SNOOZE mode can only be specified when the high-speed on-chip oscillator clock is selected as f_{CLK}.

Note 2. In the STOP mode, detecting a DTC activation source enables transition to SNOOZE mode and DTC transfer. After completion of transfer, the system returns to the STOP mode. However, since the code flash memory and the data flash memory are stopped during the SNOOZE mode, the flash memory cannot be set as the transfer source.

Note 3. When a transfer end interrupt is set as a DTC activation source from the CSIp SNOOZE mode function, release the SNOOZE mode by the transfer end interrupt to start CPU processing after completion of DTC transfer, or use a chained transfer to set CSIp reception again (writing 1 to the STm0 bit, writing 0 to the SWCm bit, setting of the SSCm register, and writing 1 to the SSm0 bit).

Note 4. When a transfer end interrupt is set as a DTC activation source from the UARTq SNOOZE mode function, release the SNOOZE mode by the transfer end interrupt to start CPU processing after completion of DTC transfer, or use a chained transfer to set UARTq reception again (writing 1 to the STm1 bit, writing 0 to the SWCm bit, setting of the SSCm register, and writing 1 to the SSm1 bit).

Note 5. When an A/D conversion end interrupt is set as a DTC activation source from the A/D converter SNOOZE mode function, release the SNOOZE mode using the A/D conversion end interrupt to start CPU processing after completion of DTC transfer, or use a chain transfer to set the A/D converter SNOOZE mode function again (writing 0 to the AWC bit and then writing 1 to the AWC bit).

Remark p = 00, 20; q = 0, 2; m = 0, 1

CHAPTER 25 EVENT LINK CONTROLLER (ELC)

25.1 Functions of ELC

The event link controller (ELC) mutually connects (links) events output from each peripheral function. By linking events, it becomes possible to coordinate operation between peripheral functions directly without going through the CPU.

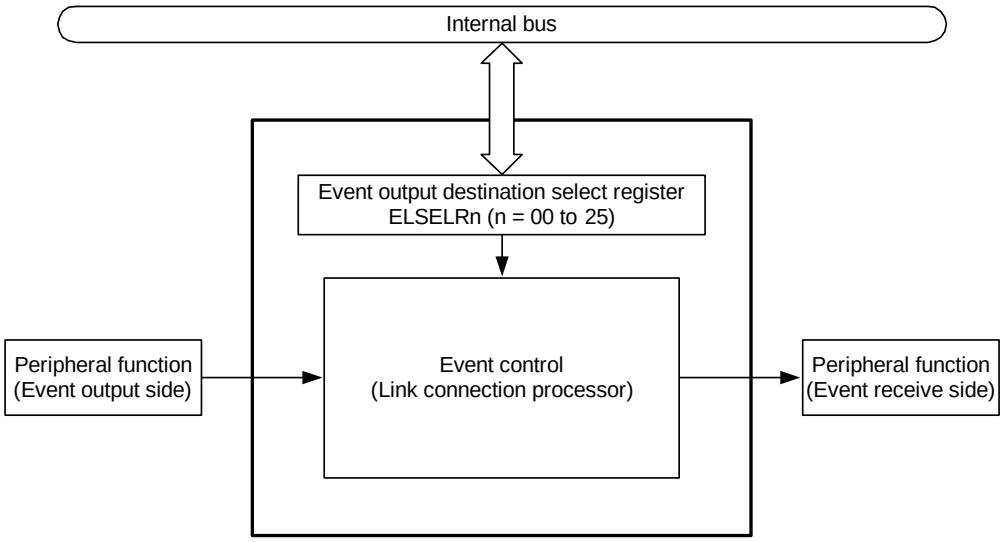
The ELC has the following functions.

- Capable of directly linking event signals from 18 to 26 types of peripheral functions to specified peripheral functions
- Event signals can be used as activation sources for operating any one of 5 to 10 types of peripheral functions

25.2 Configuration of ELC

Figure 25 - 1 shows the ELC Block Diagram.

Figure 25 - 1 ELC Block Diagram



25.3 Registers Controlling ELC

Table 25 - 1 lists the Registers Controlling ELC.

Table 25 - 1 Registers Controlling ELC

Register Name	Symbol
Event link setting register 00	ELSELR00
Event link setting register 01	ELSELR01
Event link setting register 02	ELSELR02
Event link setting register 03	ELSELR03
Event link setting register 04	ELSELR04
Event link setting register 05	ELSELR05
Event link setting register 06 Note 1	ELSELR06
Event link setting register 07 Note 2	ELSELR07
Event link setting register 08	ELSELR08
Event link setting register 09	ELSELR09
Event link setting register 10	ELSELR10
Event link setting register 11	ELSELR11
Event link setting register 12 Note 3	ELSELR12
Event link setting register 13 Note 3	ELSELR13
Event link setting register 14 Note 3	ELSELR14
Event link setting register 15 Note 3	ELSELR15
Event link setting register 16 Note 3	ELSELR16
Event link setting register 17 Note 3	ELSELR17
Event link setting register 18	ELSELR18
Event link setting register 19	ELSELR19
Event link setting register 20	ELSELR20
Event link setting register 21	ELSELR21
Event link setting register 22	ELSELR22
Event link setting register 23	ELSELR23
Event link setting register 24	ELSELR24
Event link setting register 25	ELSELR25

Note 1. R5F11NM, R5F11PL, R5F11NG, and R5F11RM only.

Note 2. R5F11NM and R5F11RM only.

Note 3. R5F11RM only.

25.3.1 Event output destination select register n (ELSELRn) (n = 00 to 25)

An ELSELRn register links each event signal to an operation of an event-receiving peripheral function (link destination peripheral function) after reception.

Do not set multiple event inputs to the same event output destination (event receive side). The operation of the event-receiving peripheral function will become undefined, and event signals may not be received correctly. In addition, do not set the event link generation source and the event link output destination to the same function.

Set an ELSELRn register during a period when no event output peripheral functions are generating event signals and the function of the event output destination (event receive side) is stopped.

Table 25 - 2 lists the Correspondence Between ELSELRn (n = 00 to 25) Registers and Peripheral Functions and Table 25 - 3 lists the Correspondence Between Values Set to ELSELRn (n = 00 to 25) Registers and Operation of Link Destination Peripheral Functions at Reception.

Figure 25 - 2 Format of Event output destination select register n (ELSELRn)

Address: F01C0H (ELSELR00) to F01D9H (ELSELR25) After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
ELSELRn	0	0	0	0	ELSELn3	ELSELn2	ELSELn1	ELSELn0

ELSELn3	ELSELn2	ELSELn1	ELSELn0	Event link selection
0	0	0	0	Event link disabled
0	0	0	1	Select operation of peripheral function 1 to link Note 1
0	0	1	0	Select operation of peripheral function 2 to link Note 1
0	0	1	1	Select operation of peripheral function 3 to link Note 1
0	1	0	0	Select operation of peripheral function 4 to link Notes 1, 2
0	1	0	1	Select operation of peripheral function 5 to link Notes 1, 2
0	1	1	0	Select operation of peripheral function 6 to link Notes 1, 3
0	1	1	1	Select operation of peripheral function 7 to link Notes 1, 2
1	0	0	0	Select operation of peripheral function 8 to link Notes 1, 3
1	0	0	1	Select operation of peripheral function 9 to link Notes 1, 2
1	0	1	0	Select operation of peripheral function 10 to link Notes 1, 4
1	0	1	1	Select operation of peripheral function 11 to link Notes 1, 4
1	1	0	0	Select operation of peripheral function 12 to link Notes 1, 3
Other than above				Setting prohibited

Note 1. See **Table 25 - 3 Correspondence Between Values Set to ELSELRn (n = 00 to 25) Registers and Operation of Link Destination Peripheral Functions at Reception**.

Note 2. R5F11NM, R5F11NL, R5F11PL, and R5F11NG only.

Note 3. R5F11NL, R5F11PL, and R5F11NG only.

Note 4. R5F11RM only.

Table 25 - 2 Correspondence Between ELSELRn (n = 00 to 25) Registers and Peripheral Functions

Register Name	Event Generator (Output Origin of Event Input n)	Event Description
ELSELR00	External interrupt edge detection 0	INTP0
ELSELR01	External interrupt edge detection 1	INTP1
ELSELR02	External interrupt edge detection 2	INTP2
ELSELR03	External interrupt edge detection 3	INTP3
ELSELR04	External interrupt edge detection 4	INTP4
ELSELR05	External interrupt edge detection 5	INTP5
ELSELR06	External interrupt edge detection 6 Note 1	INTP6
ELSELR07	External interrupt edge detection 7 Note 2	INTP7
ELSELR08	RTC fixed-cycle signal/Alarm match detection	INTRTC
ELSELR09	Compare match of 12-bit interval timer	INTIT
ELSELR10	Compare match of 8-bit interval timer channel 00 (at 8-bit or 16-bit timer operation)	INTIT00
ELSELR11	Compare match of 8-bit interval timer channel 01	INTIT01
ELSELR12	Compare match of 8-bit interval timer channel 10 (at 8-bit or 16-bit timer operation) Note 3	INTIT10
ELSELR13	Compare match of 8-bit interval timer channel 11 Note 3	INTIT11
ELSELR14	Compare match of 8-bit interval timer channel 20 (at 8-bit or 16-bit timer operation) Note 3	INTIT20
ELSELR15	Compare match of 8-bit interval timer channel 21 Note 3	INTIT21
ELSELR16	Timer RJ0 underflow Note 3	INTTRJ0
ELSELR17	Timer RJ1 underflow Note 3	INTTRJ1
ELSELR18	End of counting or capturing by channel 00 of the timer array unit	INTTM00
ELSELR19	End of counting or capturing by channel 01 of the timer array unit	INTTM01
ELSELR20	End of counting or capturing by channel 02 of the timer array unit	INTTM02
ELSELR21	End of counting or capturing by channel 03 of the timer array unit	INTTM03
ELSELR22	End of counting or capturing by channel 04 of the timer array unit	INTTM04
ELSELR23	End of counting or capturing by channel 05 of the timer array unit	INTTM05
ELSELR24	End of counting or capturing by channel 06 of the timer array unit	INTTM06
ELSELR25	End of counting or capturing by channel 07 of the timer array unit	INTTM07

Note 1. R5F11NM, R5F11PL, R5F11NG, and R5F11RM only.
Note 2. R5F11NM and R5F11RM only.
Note 3. R5F11RM only.

Table 25 - 3 Correspondence Between Values Set to ELSELRn (n = 00 to 25) Registers and Operation of Link Destination Peripheral Functions at Reception

Bits ELSELn3 to ELSELn0 in ELSELRn Register	Link Destination Number	Link Destination Peripheral Function	Link Destination Peripheral Function
0000B	—	Event link disabled	—
0001B	1	10-bit A/D converter	A/D conversion starts
0010B	2	Timer input of timer array unit 0 channel 0 Note 1	Delay counter, input pulse interval measurement, external event counter
0011B	3	Timer input of timer array unit 0 channel 1 Note 2	Delay counter, input pulse interval measurement, external event counter
0100B	4	Amplifier ELC trigger 0 Note 4	Operation starts
0101B	5	Amplifier ELC trigger 1 Note 4	Operation starts
0110B	6	Amplifier ELC trigger 2 Note 5	Operation starts
0111B	7	DA0 Notes 3, 4	Real-time output
1000B	8	DA1 Notes 3, 5	Real-time output
1001B	9	24-bit ΔΣ A/D converter Note 4	A/D conversion starts
1010B	10	Timer RJ0 Note 6	Count source
1011B	11	Timer RJ1 Note 6	Count source
1100B	12	Amplifier ELC trigger 3 Note 5	Operation starts
Other than above	—	Setting prohibited	—

Note 1. To select the timer input of timer array unit 0 channel 0 as the link destination peripheral function, set the operating clock for channel 0 to f_{CLK} using timer clock select register 0 (TPS0), set the noise filter of the TI00 pin to OFF (TNFEN00 = 0) using noise filter enable register 1 (NFEN1), and then set the timer output used for channel 0 to an event input signal from the ELC using timer input select register 0 (TIS0).

Note 2. To select the timer input of timer array unit 0 channel 1 as the link destination peripheral function, set the operating clock for channel 1 to f_{CLK} using timer clock select register 0 (TPS0), set the noise filter of the TI01 pin to OFF (TNFEN01 = 0) using noise filter enable register 1 (NFEN1), and then set the timer output used for channel 1 to an event input signal from the ELC using timer input select register 0 (TIS0).

Note 3. When entering the STOP mode while the real-time output event mode for D/A conversion is enabled, disable linking of ELC events before entering STOP mode.

Note 4. R5F11NM, R5F11NL, R5F11PL, and R5F11NG only.

Note 5. R5F11NL, R5F11PL, and R5F11NG only.

Note 6. R5F11RM only.

25.4 ELC Operation

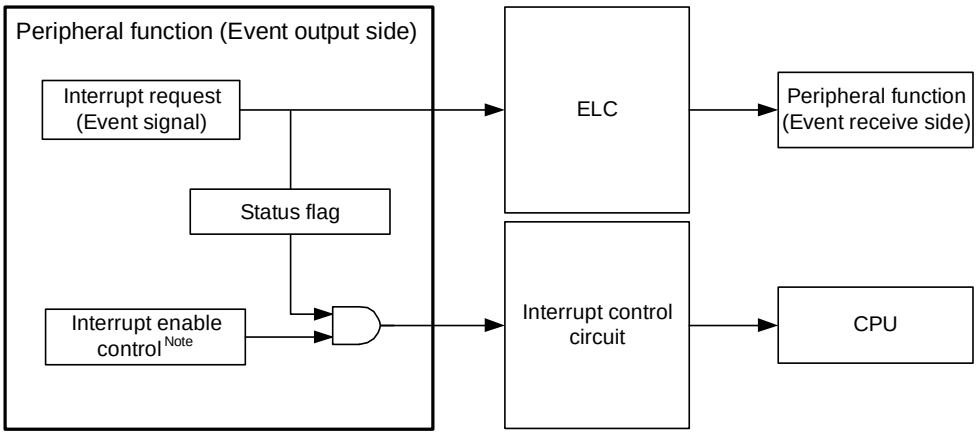
The path for using an event signal generated by a peripheral function as an interrupt request to the interrupt control circuit is independent from the path for using it as an ELC event. Therefore, each event signal can be used as an event signal for operation of an event-receiving peripheral function, regardless of interrupt control.

In addition, event link operation can be performed without being influenced by the presence or absence of a CPU clock supply. However, the operating clock of a peripheral function needs to be supplied and be in an operational state.

Figure 25 - 3 shows the Relationship Between Interrupt Handling and ELC. The figure show an example of an interrupt request status flag and a peripheral function possessing the enable bits that control enabling/disabling of such interrupts.

A peripheral function which receives an event from the ELC will perform the operation corresponding to the event-receiving peripheral function after reception of an event.

Figure 25 - 3 Relationship Between Interrupt Handling and ELC



Note Not available depending on the peripheral function.

Table 25 - 4 lists the Response of Peripheral Functions That Receive Events.

Table 25 - 4 Response of Peripheral Functions That Receive Events

Event Receiver No.	Event Link Destination Function	Operation after Event Reception	Response
1	10-bit A/D converter	A/D conversion	An event from the ELC is directly used as a hardware trigger of A/D conversion.
2	Timer array unit 0 Timer input of channel 0	Delay counter Input pulse width measurement External event counter	The edge is detected 3 or 4 cycles of f_{CLK} after an ELC event is generated.
3	Timer array unit 0 Timer input of channel 1		
4	Amplifier ELC trigger 0 Note 1	Amplifier unit activation	An event from the ELC is directly used as an activation trigger of amplifier unit.
5	Amplifier ELC trigger 1 Note 1	Amplifier unit activation	An event from the ELC is directly used as an activation trigger of amplifier unit.
6	Amplifier ELC trigger 2 Note 2	Amplifier unit activation	An event from the ELC is directly used as an activation trigger of amplifier unit.
7	Channel 0 of D/A converter Note 1	Real-time output (channel 0)	An event from the ELC is directly used as a trigger of D/A conversion of channel 0.
8	Channel 1 of D/A converter Note 2	Real-time output (channel 1)	An event from the ELC is directly used as a trigger of D/A conversion of channel 1.
9	24-bit ΔΣ A/D converter	A/D conversion	A hardware trigger of A/D conversion is generated after 2 or 3 cycles of f_{DSADCK} after an ELC event is generated.
10	Timer RJ0 Note 3	Count source	An event from the ELC is directly used as a sount source of timer RJ0.
11	Timer RJ1 Note 3	Count source	An event from the ELC is directly used as a sount source of timer RJ1.
12	Amplifier ELC trigger 3 Note 2	Amplifier unit activation	An event from the ELC is directly used as an activation trigger of operational amplifier.

Note 1. R5F11NM, R5F11NL, R5F11PL, and R5F11NG only.

Note 2. R5F11NL, R5F11PL, and R5F11NG only.

Note 3. R5F11RM only.

CHAPTER 26 INTERRUPT FUNCTIONS

The interrupt function switches the program execution to other processing. When the branch processing is finished, the program returns to the interrupted processing.
The number of interrupt sources depends on the products.

		R5F11NM	R5F11NL	R5F11PL, R5F11NG	R5F11RM
Maskable interrupts	External	8	6	7	8
	Internal	29	29	29	43

26.1 Interrupt Function Types

The following two types of interrupt functions are used.

(1) Maskable interrupts

These interrupts undergo mask control. Maskable interrupts can be divided into four priority groups by setting the priority specification flag registers (PR00L, PR00H, PR01L, PR01H, PR02L, PR02H, PR03L, PR10L, PR10H, PR11L, PR11H, PR12L, PR12H, PR13L).

Multiple interrupt servicing can be applied to low-priority interrupts when high-priority interrupts are generated. If two or more interrupt requests, each having the same priority, are simultaneously generated, then they are processed according to the default priority of vectored interrupt servicing. For the default priority, see **Table 26 - 1**.

A standby release signal is generated and STOP, HALT, and SNOOZE modes are released.

External interrupt requests and internal interrupt requests are provided as maskable interrupts.

(2) Software interrupt

This is a vectored interrupt generated by executing the BRK instruction. It is acknowledged even when interrupts are disabled. The software interrupt does not undergo interrupt priority control.

26.2 Interrupt Sources and Configuration

Interrupt sources include maskable interrupts and software interrupts. In addition, they also have up to five reset sources (see **Table 26 - 1**). The vector codes that store the program start address when branching due to the generation of a reset or various interrupt requests are two bytes each, so interrupts jump to a 64 K address of 00000H to 0FFFFH.

Table 26 - 1 Interrupt Source List (1/4)

Interrupt Type	Default Priority Note 1	Interrupt Source		Internal/ External	Vector Table Address	Basic Configuration Type Note 2	R5F11NM	R5F11NL	R5F11PL, R5F11NG	R5F11RM
		Name	Trigger							
Maskable	0	INTWDTI	Watchdog timer interval Note 3 (75% of overflow time + 1/2fIL)	Internal	00004H	(A)	√	√	√	√
	1	INTLVI	Voltage detection Note 4		00006H		√	√	√	√
	2	INTP0	Pin input edge detection	External	00008H	(B)	√	√	√	√
	3	INTP1			0000AH		√	√	√	√
	4	INTP2			0000CH		√	√	√	√
	5	INTP3			0000EH		√	√	√	√
	6	INTP4			00010H		√	√	√	√
	7	INTP5			00012H		√	√	√	√
	8	INTST2/ INTCSI20/ INTIIC20	UART2 transmission transfer end or buffer empty interrupt/CSI20 transfer end or buffer empty interrupt/IIC20 transfer end	Internal	00014H	(A)	√	√	√	√
	9	INTSR2	UART2 reception transfer end		00016H		√	√	√	√
	10	INTSRE2	UART2 reception communication error occurrence		00018H		√	√	√	√
	11	INTST0/ INTCSI00/ INTIIC00	UART0 transmission transfer end or buffer empty interrupt/CSI00 transfer end or buffer empty interrupt/IIC00 transfer end		0001EH		√	√	√	√
	12	INTTM00	End of counting or capturing by channel 0 of the timer array unit		00020H		√	√	√	√
	13	INTSR0	UART0 reception transfer end		00022H		√	√	√	√

Note 1. The default priority determines the sequence of interrupts if two or more maskable interrupts occur simultaneously. Zero indicates the highest priority and 50 indicates the lowest priority.

Note 2. Basic configuration types (A) to (C) correspond to (A) to (C) in **Figure 26 - 1**.

Note 3. When bit 7 (WDTINT) of the option byte (000C0H) is set to 1.

Note 4. When bit 7 (LVIMD) of the voltage detection level register (LVIS) is cleared to 0.

Table 26 - 1 Interrupt Source List (2/4)

Interrupt Type	Default Priority Note 1	Interrupt Source		Internal/ External	Vector Table Address	Basic Configuration Type Note 2	R5F11NM	R5F11NL	R5F11PL, R5F11NG	R5F11RM
		Name	Trigger							
Maskable	14	INTSRE0	UART0 reception communication error occurrence	Internal	00024H	(A)	√	√	√	√
		INTTM01H	End of counting or capturing by channel 1 of the timer array unit (at higher 8-bit timer operation)				√	√	√	√
	15	INTST1/ INTCSI10/ INTIIC10	UART1 transmission transfer end or buffer empty interrupt/CSI10 transfer end or buffer empty interrupt/IIC10 transfer end		00026H		√	√	√	√
	16	INTSR1	UART1 reception transfer end		00028H		√	√	√	√
	17	INTSRE1	UART1 reception communication error occurrence		0002AH		√	√	√	√
		INTTM03H	End of counting or capturing by channel 03 of the timer array unit				√	√	√	√
	18	INTIICA0	End of IICA0 communication		0002CH		√	√	√	√
	19	INTRTIT	RTC correction timing		0002EH		√	√	√	√
		INTSMP0	Sampling detector detection 0				—	—	—	√
	20	INTTM01	End of counting or capturing by channel 01 of the timer array unit (at 16-bit/lower 8-bit timer operation)		00032H		√	√	√	√
	21	INTTM02	End of counting or capturing by channel 02 of the timer array unit		00034H		√	√	√	√
	22	INTTM03	End of counting or capturing by channel 03 of the timer array unit (at 16-bit/lower 8-bit timer operation)		00036H		√	√	√	√
	23	INTAD	End of 10-bit A/D conversion		00038H		√	√	√	√
	24	INTRTC	Fixed-cycle signal of real-time clock 2/alarm match detection		0003AH		√	√	√	√
		INTSMP1	Sampling detector detection 1				—	—	—	√
	25	INTIT	Compare match of 12-bit interval timer		0003CH		√	√	√	√
	26	INTTRJ0	Timer RJ0 interrupt		0003EH		—	—	—	√
	27	INTTRJ1	Timer RJ1 interrupt		00040H		—	—	—	√

Note 1. The default priority determines the sequence of interrupts if two or more maskable interrupts occur simultaneously. Zero indicates the highest priority and 50 indicates the lowest priority.

Note 2. Basic configuration types (A) to (C) correspond to (A) to (C) in **Figure 26 - 1**.

Table 26 - 1 Interrupt Source List (3/4)

Interrupt Type	Default Priority Note 1	Interrupt Source		Internal/ External	Vector Table Address	Basic Configuration Type Note 2	R5F11NM	R5F11NL	R5F11PL, R5F11NG	R5F11RM
		Name	Trigger							
Maskable	28	INTTM04	End of counting or capturing by channel 04 of the timer array unit	Internal	00042H	(A)	√	√	√	√
	29	INTTM05	End of counting or capturing by channel 05 of the timer array unit		00044H		√	√	√	√
	30	INTP6	Pin input edge detection	External	00046H	(B)	√	—	√	√
	31	INTP7			00048H		√	—	—	√
	32	INTTM06	End of counting or capturing by channel 06 of the timer array unit	Internal	0004CH	(A)	√	√	√	√
	33	INTTM07	End of counting or capturing by channel 07 of the timer array unit		0004EH		√	√	√	√
	34	INTIT00	Compare match of 8-bit interval timer 00 (at 8-bit/16-bit timer operation)		00050H		√	√	√	√
	35	INTIT01	Compare match of 8-bit interval timer 00		00052H		√	√	√	√
	36	INTIT10	Compare match of 8-bit interval timer 10 (at 8-bit/16-bit timer operation)		00054H		—	—	—	√
	37	INTIT11	Compare match of 8-bit interval timer 11		00056H		—	—	—	√
	38	INTIT20	Compare match of 8-bit interval timer 20 (at 8-bit/16-bit timer operation)		00058H		—	—	—	√
	39	INTIT21	Compare match of 8-bit interval timer 21		0005AH		—	—	—	√
	40	INTDSAD	24-bit ΔΣ A/D conversion end		0005CH		√	√	√	—
		INTEXSD	External signal sampler edge detection				—	—	—	√
	41	INTDSADS	24-bit ΔΣ A/D scan end		00060H		√	√	√	—
		INTSMP2	Sampling detector detection 2				—	—	—	√
	42	INTFL	Reserved		00062H		√	√	√	√
	43	INTSMP3	Sampling detector detection 3		00064H		—	—	—	√
	44	INTSMP4	Sampling detector detection 4		00066H		—	—	—	√
	45	INTSMP5	Sampling detector detection 5		00068H		—	—	—	√
	46	INTSMOTA	Sampling output timer interval interrupt		0006AH		—	—	—	√
	47	INTSMOTB	Sampling output timer compare match interrupt		0006CH		—	—	—	√
	48	INTSTMG0	UARTMG0 transmission transfer end or buffer empty interrupt		0006EH		—	—	—	√
	49	INTSRMG0	UARTMG0 reception transfer end		00070H		—	—	—	√
	50	INTSREMG0	UARTMG0 reception transfer end communication error occurrence		00072H		—	—	—	√

Note 1. The default priority determines the sequence of interrupts if two or more maskable interrupts occur simultaneously. Zero indicates the highest priority and 50 indicates the lowest priority.

Note 2. Basic configuration types (A) to (C) correspond to (A) to (C) in **Figure 26 - 1**.

Table 26 - 1 Interrupt Source List (4/4)

Interrupt Type	Default Priority Note 1	Interrupt Source		Internal/ External	Vector Table Address	Basic Configuration Type Note 2	R5F11NM	R5F11NL	R5F11PL, R5F11NG	R5F11RM
		Name	Trigger							
Software	—	BRK	Execution of BRK instruction	—	0007EH	(C)	√	√	√	√
Reset	—	RESET	$\overline{\text{RESET}}$ pin input	—	00000H	—	√	√	√	√
		POR	Power-on-reset				√	√	√	√
		LVD	Voltage detection Note 3				√	√	√	√
		WDT	Overflow of watchdog timer				√	√	√	√
		TRAP	Execution of illegal instruction Note 4				√	√	√	√
		IAW	Illegal-memory access				√	√	√	√
		RPE	RAM parity error				√	√	√	√

Note 1. The default priority determines the sequence of interrupts if two or more maskable interrupts occur simultaneously. Zero indicates the highest priority and 50 indicates the lowest priority.

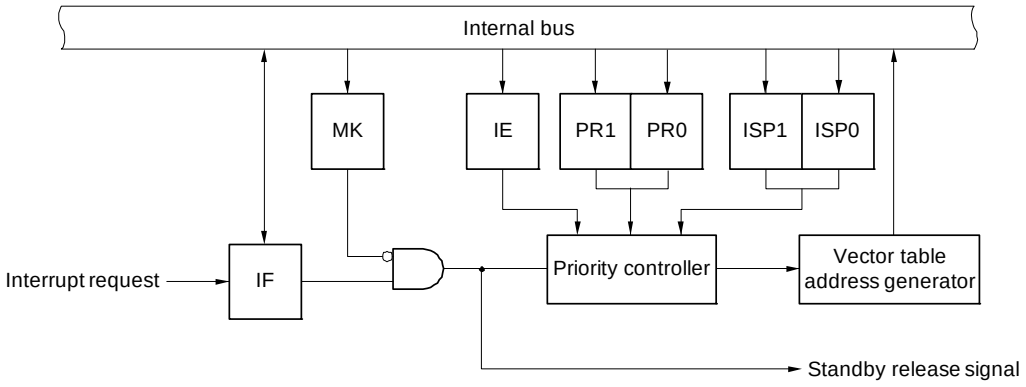
Note 2. Basic configuration types (A) to (C) correspond to (A) to (C) in **Figure 26 - 1**.

Note 3. When bit 7 (LVIMD) of the voltage detection level register (LVIS) is set to 1.

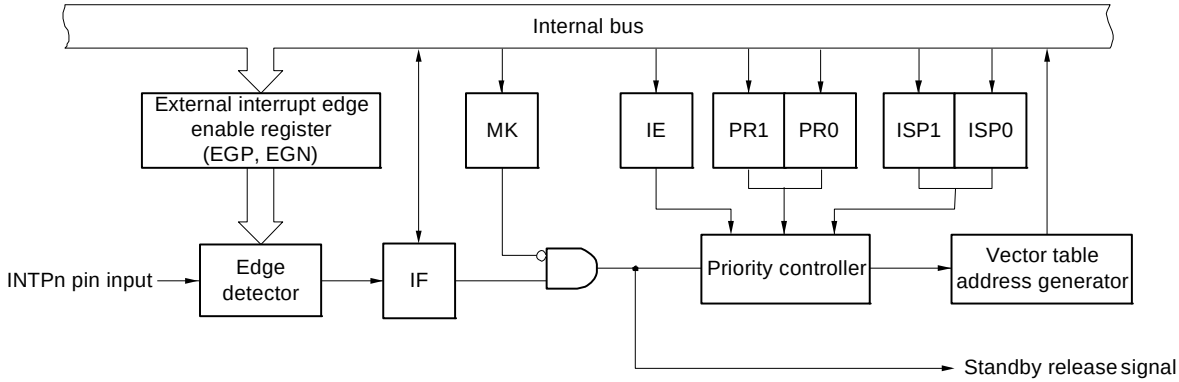
Note 4. When the instruction code in FFH is executed.
Reset by the illegal instruction execution not issued by emulation with the in-circuit emulator or on-chip debug emulator.

Figure 26 - 1 Basic Configuration of Interrupt Function

(A) Internal maskable interrupt



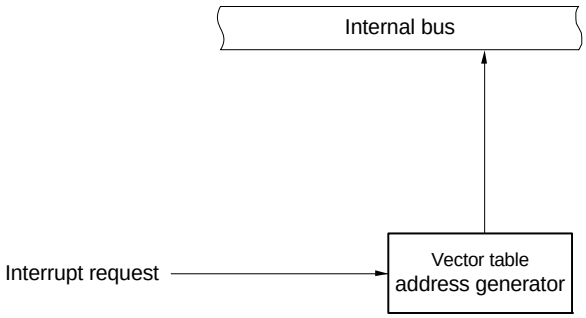
(B) External maskable interrupt (INTPn)



IF: Interrupt request flag
IE: Interrupt enable flag
ISP0: In-service priority flag 0
ISP1: In-service priority flag 1
MK: Interrupt mask flag
PR0: Priority specification flag 0
PR1: Priority specification flag 1

Remark n = 0 to 7

(C) Software interrupt



IF: Interrupt request flag
IE: Interrupt enable flag
ISP0: In-service priority flag 0
ISP1: In-service priority flag 1
MK: Interrupt mask flag
PR0: Priority specification flag 0
PR1: Priority specification flag 1

26.3 Registers Controlling Interrupt Functions

The following 6 types of registers are used to control the interrupt functions.

- Interrupt request flag registers (IF0L, IF0H, IF1L, IF1H, IF2L, IF2H, IF3L)
- Interrupt mask flag registers (MK0L, MK0H, MK1L, MK1H, MK2L, MK2H, MK3L)
- Priority specification flag registers (PR00L, PR00H, PR01L, PR01H, PR02L, PR02H, PR03L, PR10L, PR10H, PR11L, PR11H, PR12L, PR12H, PR13L)
- External interrupt rising edge enable registers (EGP0)
- External interrupt falling edge enable registers (EGN0)
- Program status word (PSW)

Table 26 - 2 show a list of interrupt request flags, interrupt mask flags, and priority specification flags corresponding to interrupt request sources.

Table 26 - 2 Flags Corresponding to Interrupt Request Sources (1/4)

Interrupt Source	Interrupt Request Flag		Interrupt Mask Flag		Priority Specification Flag		R5F11NM	R5F11NL	R5F11PL, R5F11NG	R5F11RM
		Register		Register		Register				
INTWDTI	WDTIIF	IF0L	WDTIMK	MK0L	WDTIPR0, WDTIPR1	PR00L, PR10L	√	√	√	√
INTLVI	LVIIF		LVIMK		LVIPR0, LVIPR1		√	√	√	√
INTP0	PIF0		PMK0		PPR00, PPR10		√	√	√	√
INTP1	PIF1		PMK1		PPR01, PPR11		√	√	√	√
INTP2	PIF2		PMK2		PPR02, PPR12		√	√	√	√
INTP3	PIF3		PMK3		PPR03, PPR13		√	√	√	√
INTP4	PIF4		PMK4		PPR04, PPR14		√	√	√	√
INTP5	PIF5		PMK5		PPR05, PPR15		√	√	√	√

Table 26 - 2 Flags Corresponding to Interrupt Request Sources (2/4)

Interrupt Source	Interrupt Request Flag	Register	Interrupt Mask Flag	Register	Priority Specification Flag	Register	R5F11NM	R5F11NL	R5F11PL, R5F11NG	R5F11RM
INTST2 Note 1	STIF2 Note 1	IF0H	STMK2 Note 1	MK0H	STPR02, STPR12 Note 1	PR00H, PR10H	√	√	√	√
INTCSI20 Note 1	CSIIF20 Note 1		CSIMK20 Note 1		CSIPR020, CSIPR120 Note 1		√	√	√	√
INTIIC20 Note 1	IICIF20 Note 1		IICMK20 Note 1		IICPR020, IICPR120 Note 1		√	√	√	√
INTSR2	SRIF2		SRMK2		SRPR02, SRPR12		√	√	√	√
INTSRE2	SREIF2		SREMK2		SREPR02, SREPR12		√	√	√	√
INTST0 Note 2	STIF0 Note 2		STMK0 Note 2		STPR00, STPR10 Note 2		√	√	√	√
INTCSI00 Note 2	CSIIF00 Note 2		CSIMK00 Note 2		CSIPR000, CSIPR100 Note 2		√	√	√	√
INTIIC00 Note 2	IICIF00 Note 2		IICMK00 Note 2		IICPR000, IICPR100 Note 2		√	√	√	√
INTTM00	TMIF00		TMMK00		TMPR000, TMPR100		√	√	√	√
INTSR0	SRIF0		SRMK0		SRPR00, SRPR10		√	√	√	√

Note 1. If one of the interrupt sources INTST2, INTCSI20, and INTIIC20 is generated, bit 0 of the IF0H register is set to 1. Bit 0 of the MK0H, PR00H, and PR10H registers supports these three interrupt sources.

Note 2. If one of the interrupt sources INTST0, INTCSI00, and INTIIC00 is generated, bit 5 of the IF0H register is set to 1. Bit 5 of the MK0H, PR00H, and PR10H registers supports these three interrupt sources.

Table 26 - 2 Flags Corresponding to Interrupt Request Sources (3/4)

Interrupt Source	Interrupt Request Flag	Register	Interrupt Mask Flag	Register	Priority Specification Flag	Register	R5F11NM	R5F11NL	R5F11PL, R5F11NG	R5F11RM
INTSRE0 Note 1	SREIF0 Note 1	IF1L	SREMK0 Note 1	MK1L	SREPR00, SREPR10 Note 1	PR01L, PR11L	√	√	√	√
INTTM01H Note 1	TMIF01H Note 1		TMMK01H Note 1		TMPR001H, TMPR101H Note 1		√	√	√	√
INTCSI10 Note 2	CSIIF10 Note 2		CSIMK10 Note 2		CSIPR010, CSIPR110 Note 2		√	√	√	√
INTIIC10 Note 2	IICIF10 Note 2		IICMK10 Note 2		IICPR010, IICPR110 Note 2		√	√	√	√
INTST1 Note 2	STIF1 Note 2		STMK1 Note 2		STPR01, STPR11 Note 2		√	√	√	√
INTSR1	SRIF1		SRMK1		SRPR01, SRPR11		√	√	√	√
INTSRE1 Note 3	SREIF1 Note 3		SREMK1 Note 3		SREPR01, SREPR11 Note 3		√	√	√	√
INTTM03H Note 3	TMIF03H Note 3		TMMK03H Note 3		TMPR003H, TMPR103H Note 3		√	√	√	√
INTIICA0	IICAIF0		IICAMK0		IICAPR00, IICAPR10		√	√	√	√
INTRTIT Note 4	RTITIF		RTITMK		RTITPR0, RTITPR1		√	√	√	√
INTSMP0 Note 4	SMPIF0		SMPMK0		SMPPR00, SMPPR10		—	—	—	√
INTTM01	TMIF01		TMMK01		TMPR001, TMPR101		√	√	√	√
INTTM02	TMIF02	IF1H	TMMK02	MK1H	TMPR002, TMPR102	PR01H, PR11H	√	√	√	√
INTTM03	TMIF03		TMMK03		TMPR003, TMPR103		√	√	√	√
INTAD	ADIF		ADMK		ADPR0, ADPR1		√	√	√	√
INTRTC Note 5	RTCIF		RTCMK		RTCPR0, RTCPR1		√	√	√	√
INTSMP1 Note 5	SMPIF1		SMPMK1		SMPPR01, SMPPR11		—	—	—	√
INTIT	TMKAIF		TMKAMK		TMKAPR0, TMKAPR1		√	√	√	√
INTTRJ0	TRJIF0		TRJMK0		TRJPR00, TRJPR10		—	—	—	√
INTTRJ1	TRJIF1		TRJMK1		TRJPR01, TRJPR11		—	—	—	√
INTTM04	TMIF04		TMMK04		TMPR004, TMPR104		√	√	√	√

Note 1. Do not use a UART0 reception error interrupt and an interrupt of channel 1 of TAU0 (at higher 8-bit timer operation) at the same time because they share flags for the interrupt request sources. If the UART0 reception error interrupt is not used (EOC01 = 0), UART0 and channel 1 of TAU0 (at higher 8-bit timer operation) can be used at the same time. If one of the interrupt sources INTSRE0 and INTTM01H is generated, bit 0 of the IF1L register is set to 1. Bit 0 of the MK1L, PR01L, and PR11L registers supports these two interrupt sources.

Note 2. If one of the interrupt sources INTST1, INTCSI10, and INTIIC10 is generated, bit 1 of the IF1L register is set to 1. Bit 1 of the MK1L, PR01L, and PR11L registers supports these three interrupt sources.

Note 3. Do not use a UART1 reception error interrupt and an interrupt of channel 3 of TAU0 (at higher 8-bit timer operation) at the same time because they share flags for the interrupt request sources. If the UART1 reception error interrupt is not used (EOC03 = 0), UART1 and channel 3 of TAU0 (at higher 8-bit timer operation) can be used at the same time. If one of the interrupt sources INTSRE1 and INTTM03H is generated, bit 3 of the IF1L register is set to 1. Bit 3 of the MK1L, PR01L, and PR11L registers supports these two interrupt sources.

Note 4. Do not use an RTC correction timing interrupt (INTRTIT) and a sampling detector detection 0 interrupt (INTSMP0) at the same time because they share flags for the interrupt request sources.

Note 5. Do not use a fixed-cycle signal of real-time clock 2/alarm match detection interrupt (INTRTC) and a sampling detector detection 1 interrupt (INTSMP1) at the same time because they share flags for the interrupt request sources.

Table 26 - 2 Flags Corresponding to Interrupt Request Sources (4/4)

Interrupt Source	Interrupt Request Flag	Register	Interrupt Mask Flag	Register	Priority Specification Flag	Register	R5F11NM	R5F11NL	R5F11PL, R5F11NG	R5F11RM
INTTM05	TMIF05	IF2L	TMMK05	MK2L	TMPR005, TMPR105	PR02L, PR12L	√	√	√	√
INTP6	PIF6		PMK6		PPR06, PPR16		√	—	√	√
INTP7	PIF7		PMK7		PPR07, PPR17		√	—	—	√
INTTM06	TMIF06		TMMK06		TMPR006, TMPR106		√	√	√	√
INTTM07	TMIF07		TMMK07		TMPR007, TMPR107		√	√	√	√
INTIT00	ITIF00		ITMK00		ITPR000, ITPR100		√	√	√	√
INTIT01	ITIF01		ITMK01		ITPR001, ITPR101		√	√	√	√
INTIT10	ITIF10	IF2H	ITMK10	MK2H	ITPR010, ITPR110	PR02H, PR12H	—	—	—	√
INTIT11	ITIF11		ITMK11		ITPR011, ITPR111		—	—	—	√
INTIT20	ITIF20		ITMK20		ITPR020, ITPR120		—	—	—	√
INTIT21	ITIF21		ITMK21		ITPR021, ITPR121		—	—	—	√
INTDSAD	DSADIF		DSADMK		DSADPR0, DSADPR1		√	√	√	—
INTEXSD	EXSDIF		EXSDMK		EXSDPR0, EXSDPR1		—	—	—	√
INTDSADS	DSADSIF		DSADSMK		DSADSPR0, DSADSPR1		√	√	√	—
INTSMP2	SMPIF2		SMPMK2		SMPPR02, SMPPR12		—	—	—	√
INTFL	FLIF		FLMK		FLPR0, FLPR1		√	√	√	√
INTSMP3	SMPIF3	IF3L	SMPMK3	MK3L	SMPPR03, SMPPR13	PR03L, PR13L	—	—	—	√
INTSMP4	SMPIF4		SMPMK4		SMPPR04, SMPPR14		—	—	—	√
INTSMP5	SMPIF5		SMPMK5		SMPPR05, SMPPR15		—	—	—	√
INTSMOTA	SMOTAIF		SMOTAMK		SMOTAPR0, SMOTAPR1		—	—	—	√
INTSMOTB	SMOTBIF		SMOTBMK		SMOTBPR0, SMOTBPR1		—	—	—	√
INTSTMG0	STMGIF0		STMGMK0		STMGPR00, STMGPR10		—	—	—	√
INTSRMG0	SRMGIF0		SRMGMK0		SRMGPR00, SRMGPR10		—	—	—	√
INTSREMG0	SREMGIF0		SREMGMK0		SREMGPR00, SREMGPR10		—	—	—	√

26.3.1 Interrupt request flag registers (IF0L, IF0H, IF1L, IF1H, IF2L, IF2H, IF3L)

The interrupt request flags are set to 1 when the corresponding interrupt request is generated or an instruction is executed. They are cleared to 0 when an instruction is executed upon acknowledgment of an interrupt request or upon reset signal generation.

When an interrupt is acknowledged, the interrupt request flag is automatically cleared and then the interrupt routine is entered.

The IF0L, IF0H, IF1L, IF1H, IF2L, IF2H, and IF3L registers can be set by a 1-bit or 8-bit memory manipulation instruction. When the IF0L and IF0H registers, the IF1L and IF1H registers, and the IF2L and IF2H registers are combined to form 16-bit registers IF0, IF1, and IF2, they can be set by a 16-bit memory manipulation instruction.

Reset signal generation clears these registers to 00H.

Remark If an instruction that writes data to this register is executed, the number of instruction execution clocks increases by 2 clocks.

Figure 26 - 2 Format of Interrupt Request Flag Registers (IF0L, IF0H, IF1L, IF1H, IF2L, IF2H, IF3L) (1/2)

Address: FFFE0H After reset: 00H R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
IF0L	PIF5	PIF4	PIF3	PIF2	PIF1	PIF0	LVIIF	WDTIIF

Address: FFFE1H After reset: 00H R/W

Symbol	<7>	<6>	<5>	4	3	<2>	<1>	<0>
IF0H	SRIF0	TMIF00	STIF0 CSIIF00 IICIF00	0	0	SREIF2	SRIF2	STIF2 CSIIF20 IICIF20

Address: FFFE2H After reset: 00H R/W

Symbol	<7>	6	<5>	<4>	<3>	<2>	<1>	<0>
IF1L	TMIF01	0	RTITIF SMPIF0	IICAIF0	SREIF1 TMIF03H	SRIF1	CSIIF10 IICIF10 STIF1	SREIF0 TMIF01H

Address: FFFE3H After reset: 00H R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
IF1H	TMIF04	TRJIF1	TRJIF0	TMKAIF	RTCIF SMPIF1	ADIF	TMIF03	TMIF02

Address: FFFD0H After reset: 00H R/W

Symbol	<7>	<6>	<5>	<4>	3	<2>	<1>	<0>
IF2L	ITIF01	ITIF00	TMIF07	TMIF06	0	PIF7	PIF6	TMIF05

Figure 26 - 2 Format of Interrupt Request Flag Registers (IF0L, IF0H, IF1L, IF1H, IF2L, IF2H, IF3L) (2/2)

Address: FFFD1H After reset: 00H R/W

Symbol	<7>	<6>	5	<4>	<3>	<2>	<1>	<0>
IF2H	FLIF	DSADSIF SMPIF2	0	DSADIF EXSDIF	ITIF21	ITIF20	ITIF11	ITIF10

Address: FFFD2H After reset: 00H R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
IF3L	SREMGIF0	SRMGIF0	STMGIF0	SMOTBIF	SMOTAIF	SMPIF5	SMPIF4	SMPIF3

XXIFX	Interrupt request flag
0	No interrupt request signal is generated
1	Interrupt request is generated, interrupt request status

Caution 1. The available registers and bits differ depending on the product. For details about the registers and bits available for each product, see Table 26 - 2. Be sure to set bits that are not available to the initial value.

Caution 2. When manipulating a flag of the interrupt request flag register, use a 1-bit memory manipulation instruction (CLR1). When describing in C language, use a bit manipulation instruction such as "IF0L.0 = 0;" or "_asm ("clr1 IF0L.0");" because the compiled assembler must be a 1-bit memory manipulation instruction (CLR1).

If a program is described in C language using an 8-bit memory manipulation instruction such as "IF0L & = 0xfe;" and compiled, it becomes the assembler of three instructions.

```
mov a, IF0L
and a, #0FEH
mov IF0L, a
```

In this case, even if the request flag of the another bit of the same interrupt request flag register (IF0L) is set to 1 at the timing between "mov a, IF0L" and "mov IF0L, a", the flag is cleared to 0 at "mov IF0L, a". Therefore, care must be exercised when using an 8-bit memory manipulation instruction in C language.

26.3.2 Interrupt mask flag registers (MK0L, MK0H, MK1L, MK1H, MK2L, MK2H, MK3L)

The interrupt mask flags are used to enable/disable the corresponding maskable interrupt.

The MK0L, MK0H, MK1L, MK1H, MK2L, MK2H, and MK3L registers can be set by a 1-bit or 8-bit memory manipulation instruction. When the MK0L and MK0H registers, the MK1L and MK1H registers, and the MK2L and MK2H registers are combined to form 16-bit registers MK0, MK1, and MK2, they can be set by a 16-bit memory manipulation instruction.

Reset signal generation sets these registers to FFH.

Remark If an instruction that writes data to this register is executed, the number of instruction execution clocks increases by 2 clocks.

Figure 26 - 3 Format of Interrupt Mask Flag Registers (MK0L, MK0H, MK1L, MK1H, MK2L, MK2H, MK3L) (1/2)

Address: FFFE4H After reset: FFH R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
MK0L	PMK5	PMK4	PMK3	PMK2	PMK1	PMK0	LVIMK	WDTIMK

Address: FFFE5H After reset: FFH R/W

Symbol	<7>	<6>	<5>	4	3	<2>	<1>	<0>
MK0H	SRMK0	TMMK00	STMK0 CSIMK00 IICMK00	1	1	SREMK2	SRMK2	STMK2 CSIMK20 IICMK20

Address: FFFE6H After reset: FFH R/W

Symbol	<7>	6	<5>	<4>	<3>	<2>	<1>	<0>
MK1L	TMMK01	1	RTITMK SMPMK0	IICAMK0	SREMK1 TMMK03H	SRMK1	CSIMK10 IICMK10 STMK1	SREMK0 TMMK01H

Address: FFFE7H After reset: FFH R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
MK1H	TMMK04	TRJMK1	TRJMK0	TMKAMK	RTCMK SMPMK1	ADMK	TMMK03	TMMK02

Address: FFFD4H After reset: FFH R/W

Symbol	<7>	<6>	<5>	<4>	3	<2>	<1>	<0>
MK2L	ITMK01	ITMK00	TMMK07	TMMK06	1	PMK7	PMK6	TMMK05

Figure 26 - 3 Format of Interrupt Mask Flag Registers (MK0L, MK0H, MK1L, MK1H, MK2L, MK2H, MK3L) (2/2)

Address: FFFD5H After reset: FFH R/W

Symbol	<7>	<6>	5	<4>	<3>	<2>	<1>	<0>
MK2H	FLMK	DSADSMK SMPMK2	1	DSADMK EXSDMK	ITMK21	ITMK20	ITMK11	ITMK10

Address: FFFD6H After reset: FFH R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
MK3L	SREMGMK0	SRMGMK0	STMGMK0	SMOTBMK	SMOTAMK	SMPMK5	SMPMK4	SMPMK3

XXMKX	Interrupt servicing control
0	Interrupt servicing enabled
1	Interrupt servicing disabled

Caution The available registers and bits differ depending on the product. For details about the registers and bits available for each product, see Table 26 - 2. Be sure to set bits that are not available to the initial value.

26.3.3 Priority specification flag registers (PR00L, PR00H, PR01L, PR01H, PR02L, PR02H, PR03L, PR10L, PR10H, PR11L, PR11H, PR12L, PR12H, PR13L)

The priority specification flag registers are used to set the corresponding maskable interrupt priority level.
A priority level is set by using the PR0xy and PR1xy registers in combination (xy = 0L, 0H, 1L, 1H, 2L, 2H, or 3L).
The PR00L, PR00H, PR01L, PR01H, PR02L, PR02H, PR03L, PR10L, PR10H, PR11L, PR11H, PR12L, PR12H, and PR13L registers can be set by a 1-bit or 8-bit memory manipulation instruction. If the PR00L and PR00H registers, the PR01L and PR01H registers, the PR02L and PR02H registers, the PR10L and PR10H registers, the PR11L and PR11H registers, and the PR12L and PR12H registers are combined to form 16-bit registers PR00, PR01, PR02, PR10, PR11, and PR12, they can be set by a 16-bit memory manipulation instruction.
Reset signal generation sets these registers to FFH.

Remark If an instruction that writes data to this register is executed, the number of instruction execution clocks increases by 2 clocks.

Figure 26 - 4 Format of Priority specification flag registers (PR00L, PR00H, PR01L, PR01H, PR02L, PR02H, PR03L, PR10L, PR10H, PR11L, PR11H, PR12L, PR12H, PR13L) (1/2)

Address: FFFE8H After reset: FFH R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
PR00L	PPR05	PPR04	PPR03	PPR02	PPR01	PPR00	LVIPR0	WDTIPR0

Address: FFFECH After reset: FFH R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
PR10L	PPR15	PPR14	PPR13	PPR12	PPR11	PPR10	LVIPR1	WDTIPR1

Address: FFFE9H After reset:FFH R/W

Symbol	<7>	<6>	<5>	4	3	<2>	<1>	<0>
PR00H	SRPR00	TMPR000	STPR00 CSIPR000 IICPR000	1	1	SREPR02	SRPR02	STPR02 CSIPR020 IICPR020

Address: FFFEDH After reset: FFH R/W

Symbol	<7>	<6>	<5>	4	3	<2>	<1>	<0>
PR10H	SRPR10	TMPR100	STPR10 CSIPR100 IICPR100	1	1	SREPR12	SRPR12	STPR12 CSIPR120 IICPR120

Address: FFFEAH After reset: FFH R/W

Symbol	<7>	6	<5>	<4>	<3>	<2>	<1>	<0>
PR01L	TMPR001	1	RTITPR0 SMPPR00	IICAPR00	SREPR01 TMPR003H	SRPR01	CSIPR010 IICPR010 STPR01	SREPR00 TMPR001H

Address: FFFEEH After reset: FFH R/W

Symbol	<7>	6	<5>	<4>	<3>	<2>	<1>	<0>
PR11L	TMPR101	1	RTITPR1 SMPPR10	IICAPR10	SREPR11 TMPR103H	SRPR11	CSIPR110 IICPR110 STPR11	SREPR10 TMPR101H

Address: FFFEBH After reset: FFH R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
PR01H	TMPR004	TRJRP01	TRJPR00	TMKAPR0	RTCPR0 SMPPR01	ADPR0	TMPR003	TMPR002

Address: FFFEFH After reset: FFH R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
PR11H	TMPR104	TRJRP11	TRJPR10	TMKAPR1	RTCPR1 SMPPR11	ADPR1	TMPR103	TMPR102

Figure 26 - 4 Format of Priority specification flag registers (PR00L, PR00H, PR01L, PR01H, PR02L, PR02H, PR03L, PR10L, PR10H, PR11L, PR11H, PR12L, PR12H, PR13L) (2/2)

Address: FFFD8H After reset: FFH R/W

Symbol	<7>	<6>	<5>	<4>	3	<2>	<1>	<0>
PR02L	ITPR001	ITPR000	TMPR007	TMPR006	1	PPR07	PPR06	TMPR005

Address: FFFDCH After reset: FFH R/W

Symbol	<7>	<6>	<5>	<4>	3	<2>	<1>	<0>
PR12L	ITPR101	ITPR100	TMPR107	TMPR106	1	PPR17	PPR16	TMPR105

Address: FFFD9H After reset: FFH R/W

Symbol	<7>	<6>	5	<4>	<3>	<2>	<1>	<0>
PR02H	FLPR0	DSADSPR0 SMPPR02	1	DSADPR0 EXSDPR0	ITPR021	ITPR020	ITPR011	ITPR010

Address: FFFDDH After reset: FFH R/W

Symbol	<7>	<6>	5	<4>	<3>	<2>	<1>	<0>
PR12H	FLPR1	DSADSPR1 SMPPR12	1	DSADPR1 EXSDPR1	ITPR121	ITPR120	ITPR111	ITPR110

Address: FFFDAH After reset: FFH R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
PR03L	SREMGPR00	SRMGPR00	STMGPR00	SMOTBPR0	SMOTAPR0	SMPPR05	SMPPR04	SMPPR03

Address: FFFDEH After reset: FFH R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
PR13L	SREMGPR10	SRMGPR10	STMGPR10	SMOTBPR1	SMOTAPR1	SMPPR15	SMPPR14	SMPPR13

XXPR1X	XXPR0X	Priority level selection
0	0	Specify level 0 (high priority level)
0	1	Specify level 1
1	0	Specify level 2
1	1	Specify level 3 (low priority level)

Caution The available registers and bits differ depending on the product. For details about the registers and bits available for each product, see Table 26 - 2. Be sure to set bits that are not available to the initial value.

26.3.4 External interrupt rising edge enable registers (EGP0), external interrupt falling edge enable registers (EGN0)

These registers specify the valid edge for INTP0 to INTP7.

The EGP0 and EGN0 registers can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears these registers to 00H.

Figure 26 - 5 Format of External Interrupt Rising Edge Enable Registers (EGP0) and External Interrupt Falling Edge Enable Registers (EGN0)

Address: FFF38H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
EGP0	EGP7	EGP6	EGP5	EGP4	EGP3	EGP2	EGP1	EGP0

Address: FFF39H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
EGN0	EGN7	EGN6	EGN5	EGN4	EGN3	EGN2	EGN1	EGN0

EGPn	EGNn	INTPn pin valid edge selection (n = 0 to 7)
0	0	Edge detection disabled
0	1	Falling edge
1	0	Rising edge
1	1	Both rising and falling edges

Table 26 - 3 shows the Ports Corresponding to EGPn and EGNn Bits.

Table 26 - 3 Ports Corresponding to EGPn and EGNn Bits

Detection Enable Bit		Interrupt Request Signal
EGP0	EGN0	INTP0
EGP1	EGN1	INTP1
EGP2	EGN2	INTP2
EGP3	EGN3	INTP3
EGP4	EGN4	INTP4
EGP5	EGN5	INTP5
EGP6	EGN6	INTP6
EGP7	EGN7	INTP7

Caution When the input port pins used for the external interrupt functions are switched to the output mode, the INTPn interrupt might be generated upon detection of a valid edge.
When switching the input port pins to the output mode, set the port mode register (PMxx) to 0 after disabling the edge detection (by setting EGPn and EGNn to 0).

Remark 1. For edge detection port, see **2.1 Port Function**.

Remark 2. n = 0 to 7

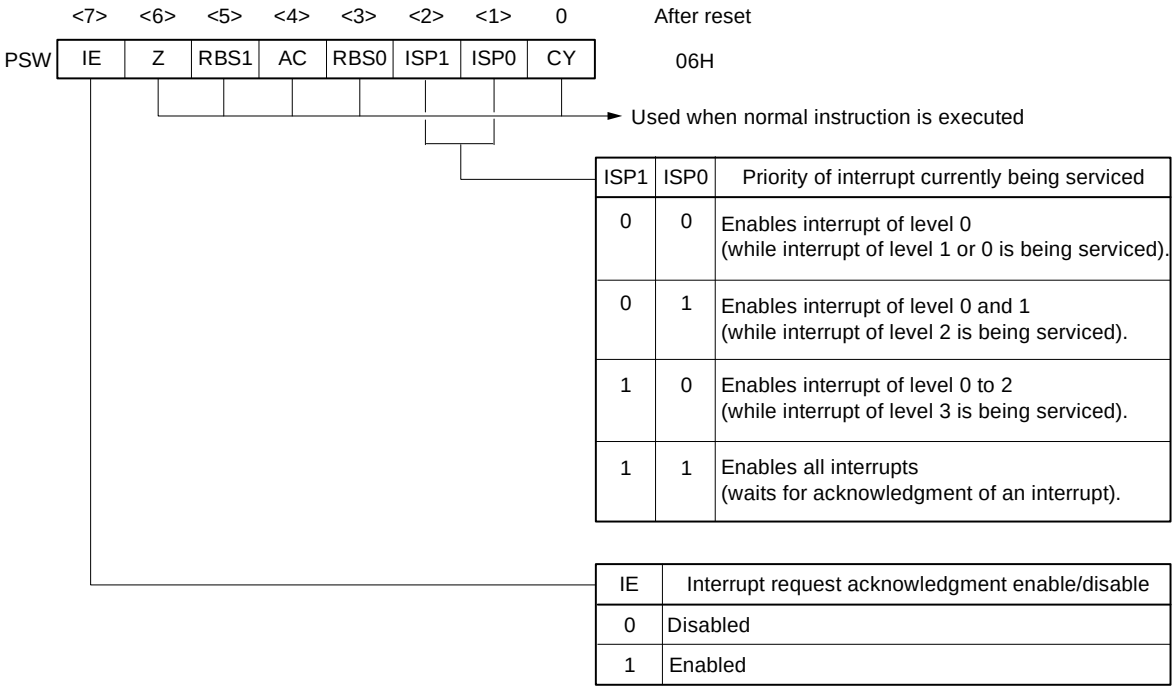
26.3.5 Program status word (PSW)

The program status word is a register used to hold the instruction execution result and the current status for an interrupt request. The IE flag that sets maskable interrupt enable/disable and the ISP0 and ISP1 flags that controls multiple interrupt servicing are mapped to the PSW.

Besides 8-bit read/write, this register can carry out operations using bit manipulation instructions and dedicated instructions (EI and DI). When a vectored interrupt request is acknowledged, if the BRK instruction is executed, the contents of the PSW are automatically saved into a stack and the IE flag is reset to 0. Upon acknowledgment of a maskable interrupt request, if the value of the priority specification flag register of the acknowledged interrupt is not 00, its value minus 1 is transferred to the ISP0 and ISP1 flags. The PSW contents are also saved into the stack with the PUSH PSW instruction. They are restored from the stack with the RETI, RETB, and POP PSW instructions.

Reset signal generation sets PSW to 06H.

Figure 26 - 6 Configuration of Program Status Word



ISP1	ISP0	Priority of interrupt currently being serviced
0	0	Enables interrupt of level 0 (while interrupt of level 1 or 0 is being serviced).
0	1	Enables interrupt of level 0 and 1 (while interrupt of level 2 is being serviced).
1	0	Enables interrupt of level 0 to 2 (while interrupt of level 3 is being serviced).
1	1	Enables all interrupts (waits for acknowledgment of an interrupt).

IE	Interrupt request acknowledgment enable/disable
0	Disabled
1	Enabled

26.4 Interrupt Servicing Operations

26.4.1 Maskable interrupt request acknowledgment

A maskable interrupt request becomes acknowledgeable when the interrupt request flag is set to 1 and the mask (MK) flag corresponding to that interrupt request is cleared to 0. A vectored interrupt request is acknowledged if interrupts are in the interrupt enabled state (when the IE flag is set to 1). However, a low-priority interrupt request is not acknowledged during servicing of a higher priority interrupt request.

The times from generation of a maskable interrupt request until vectored interrupt servicing is performed are listed in **Table 26 - 4** below.

For the interrupt request acknowledgment timing, see **Figures 26 - 8** and **26 - 9**.

Table 26 - 4 Time from Generation of Maskable Interrupt Until Servicing

	Minimum Time	Maximum Time Note
Servicing time	9 clocks	16 clocks

Note Maximum time does not apply when an instruction from the internal RAM area is executed.

Remark 1 clock: 1/f_{CLK} (f_{CLK}: CPU clock)

If two or more maskable interrupt requests are generated simultaneously, the request with a higher priority level specified in the priority specification flag is acknowledged first. If two or more interrupts requests have the same priority level, the request with the highest default priority is acknowledged first.

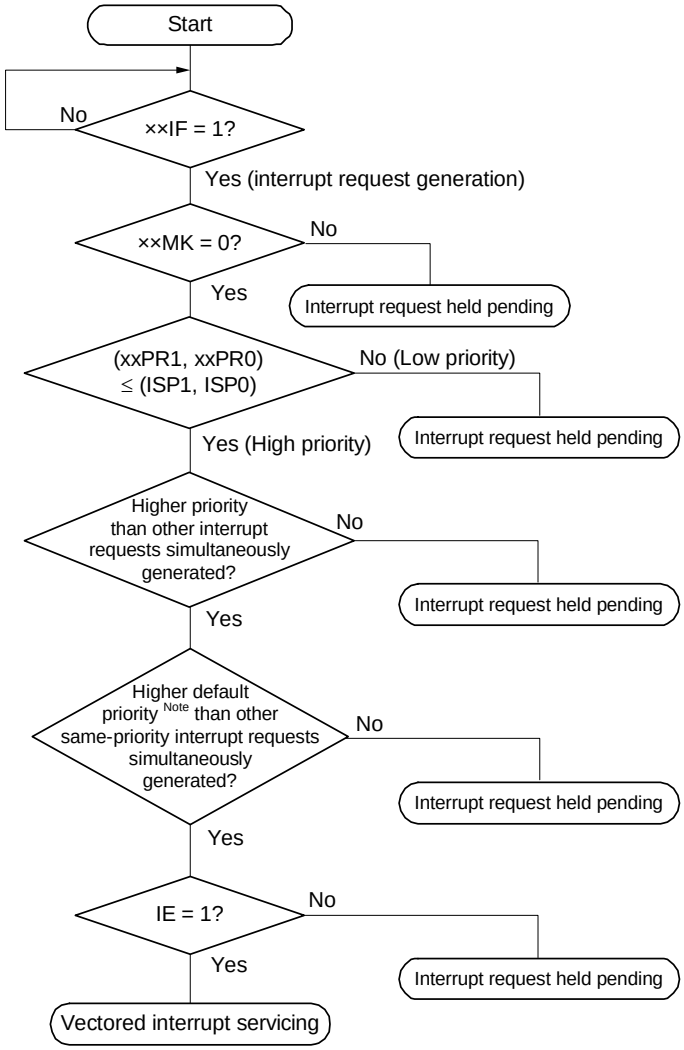
An interrupt request that is held pending is acknowledged when it becomes acknowledgeable.

Figure 26 - 7 shows the Interrupt Request Acknowledgment Processing Algorithm.

If a maskable interrupt request is acknowledged, the contents are saved into the stacks in the order of PSW, then PC, the IE flag is reset (0), and the contents of the priority specification flag corresponding to the acknowledged interrupt are transferred to the ISP1 and ISP0 flags. The vector table data determined for each interrupt request is the loaded into the PC and branched.

Restoring from an interrupt is possible by using the RETI instruction.

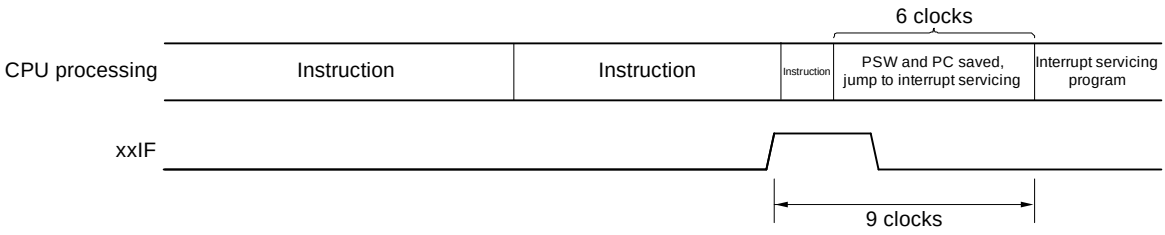
Figure 26 - 7 Interrupt Request Acknowledgment Processing Algorithm



xxIF: Interrupt request flag
xxMK: Interrupt mask flag
xxPR0: Priority specification flag 0
xxPR1: Priority specification flag 1
IE: Flag that controls acknowledgment of maskable interrupt request (1 = Enable, 0 = Disable)
ISP0, ISP1: Flag that indicates the priority level of the interrupt currently being serviced (see **Figure 26 - 6**)

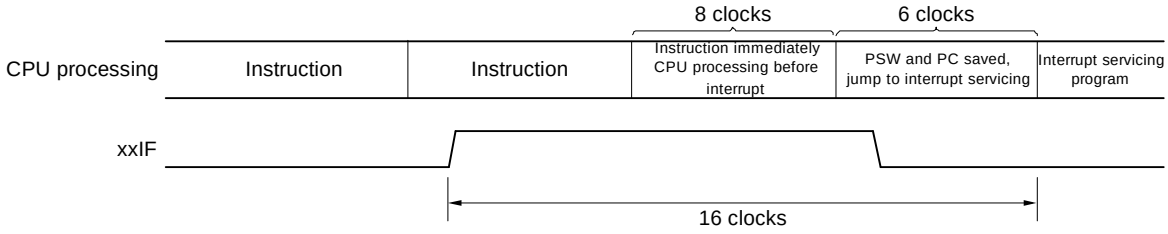
Note For the default priority, refer to **Table 26 - 1 Interrupt Source List**.

Figure 26 - 8 Interrupt Request Acknowledgment Timing (Minimum Time)



Remark 1 clock: 1/f_{CLK} (f_{CLK}: CPU clock)

Figure 26 - 9 Interrupt Request Acknowledgment Timing (Maximum Time)



Remark 1 clock: 1/f_{CLK} (f_{CLK}: CPU clock)

26.4.2 Software interrupt request acknowledgment

A software interrupt request is acknowledged by BRK instruction execution. Software interrupts cannot be disabled.

If a software interrupt request is acknowledged, the contents are saved into the stacks in the order of the program status word (PSW), then program counter (PC), the IE flag is reset (0), and the contents of the vector table (0007EH, 0007FH) are loaded into the PC and branched.

Restoring from a software interrupt is possible by using the RETB instruction.

Caution The RETI instruction cannot be used for restoring from the software interrupt.

26.4.3 Multiple interrupt servicing

Multiple interrupt servicing occurs when another interrupt request is acknowledged during execution of an interrupt.

Multiple interrupt servicing does not occur unless the interrupt request acknowledgment enabled state is selected (IE = 1). When an interrupt request is acknowledged, interrupt request acknowledgment becomes disabled (IE = 0). Therefore, to enable multiple interrupt servicing, it is necessary to set (1) the IE flag with the EI instruction during interrupt servicing to enable interrupt acknowledgment.

Moreover, even if interrupts are enabled, multiple interrupt servicing may not be enabled, this being subject to interrupt priority control. Two types of priority control are available: default priority control and programmable priority control. Programmable priority control is used for multiple interrupt servicing.

In the interrupt enabled state, if an interrupt request with a priority equal to or higher than that of the interrupt currently being serviced is generated, it is acknowledged for multiple interrupt servicing. If an interrupt with a priority equal to or lower than that of the interrupt currently being serviced is generated during interrupt servicing, it is not acknowledged for multiple interrupt servicing. However, when setting the IE flag to 1 during the interruption at level 0, other level 0 interruptions can be allowed.

Interrupt requests that are not enabled because interrupts are in the interrupt disabled state or because they have a lower priority are held pending. When servicing of the current interrupt ends, the pending interrupt request is acknowledged following execution of at least one main processing instruction execution.

Table 26 - 5 shows Relationship Between Interrupt Requests Enabled for Multiple Interrupt Servicing During Interrupt Servicing and **Figure 26 - 10** and **26 - 10** show multiple interrupt servicing examples.

Table 26 - 5 Relationship Between Interrupt Requests Enabled for Multiple Interrupt Servicing During Interrupt Servicing

Multiple Interrupt Request / Interrupt Being Serviced		Maskable Interrupt Request								Software Interrupt Request
		Priority Level 0 (PR = 00)		Priority Level 1 (PR = 01)		Priority Level 2 (PR = 10)		Priority Level 3 (PR = 11)		
		IE = 1	IE = 0	IE = 1	IE = 0	IE = 1	IE = 0	IE = 1	IE = 0	
Maskable interrupt	ISP1 = 0, ISP0 = 0	√	×	×	×	×	×	×	×	√
	ISP1 = 0, ISP0 = 1	√	×	√	×	×	×	×	×	√
	ISP1 = 1, ISP0 = 0	√	×	√	×	√	×	×	×	√
	ISP1 = 1, ISP0 = 1	√	×	√	×	√	×	√	×	√
Software interrupt		√	×	√	×	√	×	√	×	√

Remark 1. √: Multiple interrupt servicing enabled

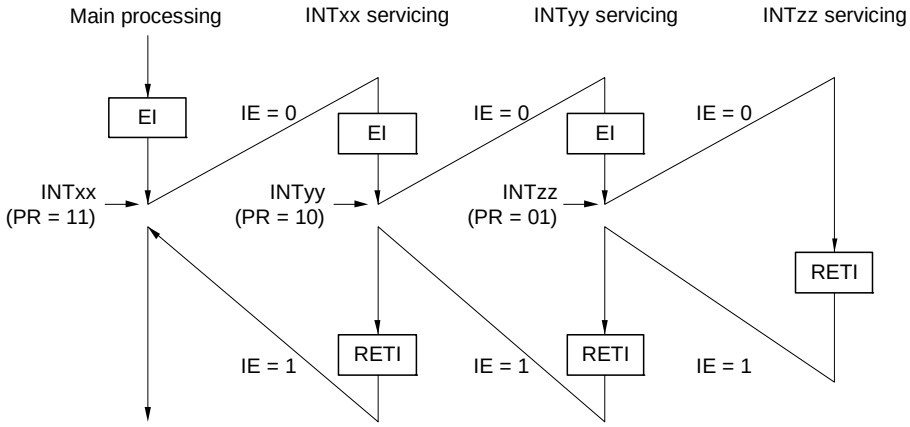
Remark 2. ×: Multiple interrupt servicing disabled

Remark 3. ISP0, ISP1, and IE are flags contained in the PSW.
ISP1 = 0, ISP0 = 0: An interrupt of level 1 or level 0 is being serviced.
ISP1 = 0, ISP0 = 1: An interrupt of level 2 is being serviced.
ISP1 = 1, ISP0 = 0: An interrupt of level 3 is being serviced.
ISP1 = 1, ISP0 = 1: Wait for An interrupt acknowledgment (all interrupts are enabled).
IE = 0: Interrupt request acknowledgment is disabled.
IE = 1: Interrupt request acknowledgment is enabled.

Remark 4. PR is a flag contained in the PR00L, PR00H, PR01L, PR01H, PR02L, PR02H, PR03L, PR10L, PR10H, PR11L, PR11H, PR12L, PR12H, and PR13L registers.
PR = 00: Specify level 0 with ××PR1× = 0, ××PR0× = 0 (higher priority level)
PR = 01: Specify level 1 with ××PR1× = 0, ××PR0× = 1
PR = 10: Specify level 2 with ××PR1× = 1, ××PR0× = 0
PR = 11: Specify level 3 with ××PR1× = 1, ××PR0× = 1 (lower priority level)

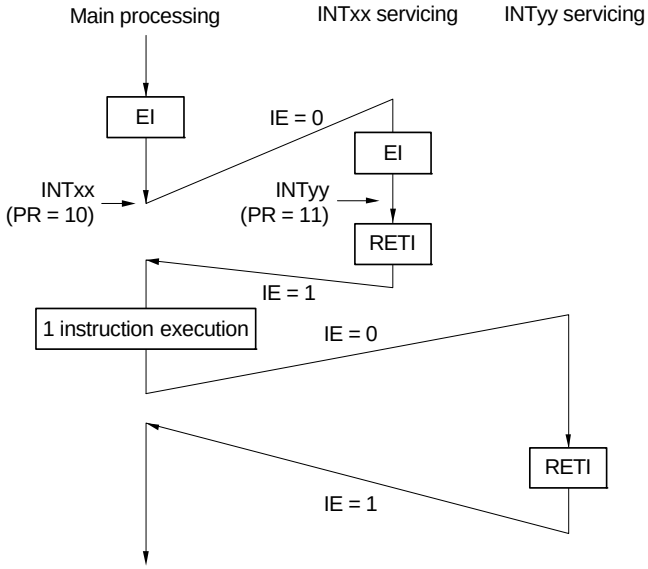
Figure 26 - 10 Examples of Multiple Interrupt Servicing (1/2)

Example 1. Multiple interrupt servicing occurs twice



During servicing of interrupt INTxx, two interrupt requests, INTyy and INTzz, are acknowledged, and multiple interrupt servicing takes place. Before each interrupt request is acknowledged, the EI instruction must always be issued to enable interrupt request acknowledgment.

Example 2. Multiple interrupt servicing does not occur due to priority control

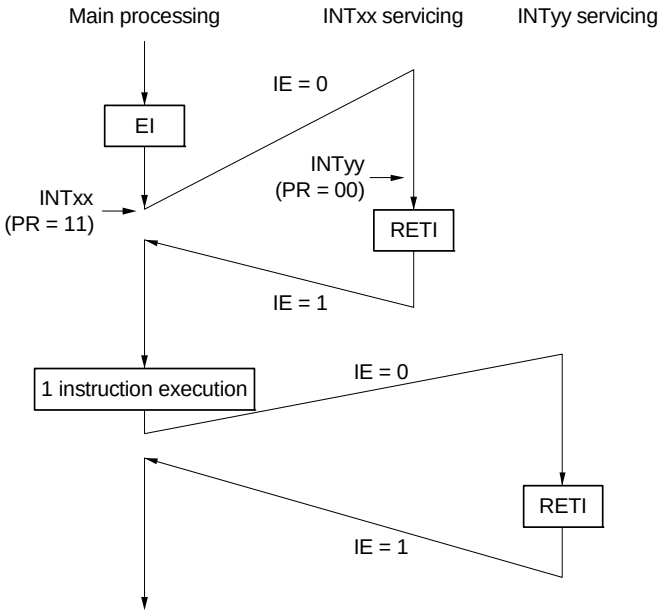


Interrupt request INTyy issued during servicing of interrupt INTxx is not acknowledged because its priority is lower than that of INTxx, and multiple interrupt servicing does not take place. The INTyy interrupt request is held pending, and is acknowledged following execution of one main processing instruction.

PR = 00: Specify level 0 with xxPR1x = 0, xxPR0x = 0 (higher priority level)
PR = 01: Specify level 1 with xxPR1x = 0, xxPR0x = 1
PR = 10: Specify level 2 with xxPR1x = 1, xxPR0x = 0
PR = 11: Specify level 3 with xxPR1x = 1, xxPR0x = 1 (lower priority level)
IE = 0: Interrupt request acknowledgment is disabled
IE = 1: Interrupt request acknowledgment is enabled.

Figure 26 - 10 Examples of Multiple Interrupt Servicing (2/2)

Example 3. Multiple interrupt servicing does not occur because interrupts are not enabled



Interrupts are not enabled during servicing of interrupt INTxx (EI instruction is not issued), therefore, interrupt request INTyy is not acknowledged and multiple interrupt servicing does not take place. The INTyy interrupt request is held pending, and is acknowledged following execution of one main processing instruction.

PR = 00: Specify level 0 with xxPR1x = 0, xxPR0x = 0 (higher priority level)
PR = 01: Specify level 1 with xxPR1x = 0, xxPR0x = 1
PR = 10: Specify level 2 with xxPR1x = 1, xxPR0x = 0
PR = 11: Specify level 3 with xxPR1x = 1, xxPR0x = 1 (lower priority level)
IE = 0: Interrupt request acknowledgment is disabled
IE = 1: Interrupt request acknowledgment is enabled.

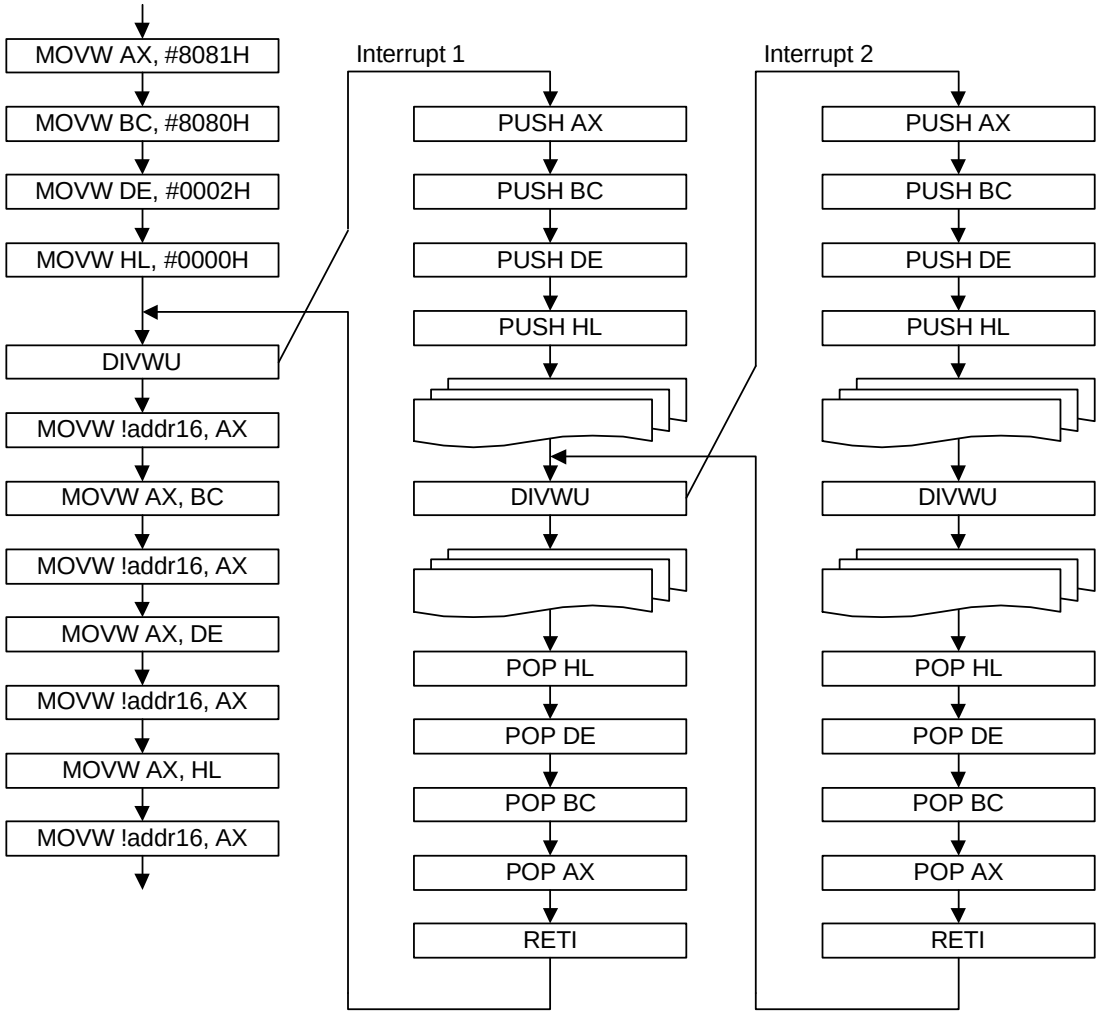
26.4.4 Interrupt servicing during division instruction

The RL78/H1D handles interrupts during the DIVHU/DIVWU instruction in order to enhance the interrupt response when a division instruction is executed.

- When an interrupt is generated while the DIVHU/DIVWU instruction is executed, the instruction is suspended
- After the instruction is suspended, the PC indicates the next instruction after DIVHU/DIVWU
- An interrupt is generated by the next instruction
- PC-3 is stacked to execute the DIVHU/DIVWU instruction again

Normal interrupt	Interrupts while Executing DIVHU/DIVWU Instruction
(SP-1) ← PSW	(SP-1) ← PSW
(SP-2) ← $(PC)_S$	(SP-2) ← $(PC-3)_S$
(SP-3) ← $(PC)_H$	(SP-3) ← $(PC-3)_H$
(SP-4) ← $(PC)_L$	(SP-4) ← $(PC-3)_L$
PC_S ← 0000	PC_S ← 0000
PC_H ← (Vector)	PC_H ← (Vector)
PC_L ← (Vector)	PC_L ← (Vector)
SP ← SP-4	SP ← SP-4
IE ← 0	IE ← 0

The AX, BC, DE, and HL registers are used for DIVHU/DIVWU. Use these registers by stacking them for interrupt servicing.



Caution Disable interrupts when executing the DIVHU or DIVWU instruction in an interrupt servicing routine. Alternatively, unless they are executed in the RAM area, note that execution of a DIVHU or DIVWU instruction is possible even with interrupts enabled as long as a NOP instruction is added immediately after the DIVHU or DIVWU instruction in the assembly language source code. The following compilers automatically add a NOP instruction immediately after any DIVHU or DIVWU instruction output during the build process.

- V. 1.71 and later versions of the CA78K0R (Renesas Electronics compiler), for both C and assembly language source code

- Service pack 1.40.3 and later versions of the EWRL78 (IAR compiler), for C language source code

- GNURL78 (KPIT compiler), for C language source code

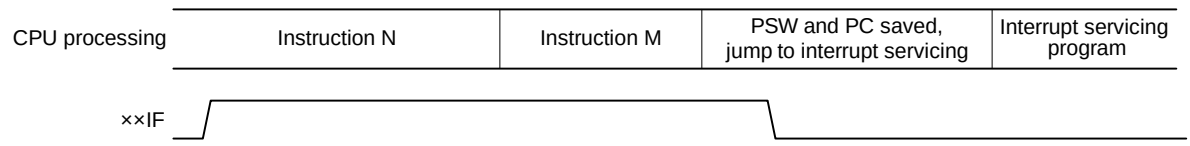
26.4.5 Interrupt request hold

There are instructions where, even if an interrupt request is issued while the instructions are being executed, interrupt request acknowledgment is held pending until the end of execution of the next instruction. These instructions (interrupt request hold instructions) are listed below.

- MOV PSW, #byte
- MOV PSW, A
- MOV1 PSW. bit, CY
- SET1 PSW. bit
- CLR1 PSW. bit
- RETB
- RETI
- POP PSW
- BTCLR PSW. bit, $addr20
- EI
- DI
- SKC
- SKNC
- SKZ
- SKNZ
- SKH
- SKNH
- MULHU
- MULH
- MACHU
- MACH
- Write instructions for the IF0L, IF0H, IF1L, IF1H, IF2L, IF3L, IF2H, MK0L, MK0H, MK1L, MK1H, MK2L, MK2H, MK3L, PR00L, PR00H, PR01L, PR01H, PR02L, PR02H, PR03L, PR10L, PR10H, PR11L, PR11H, PR12L, PR12H, and PR13L registers

Figure 26 - 11 shows the timing at which interrupt requests are held pending.

Figure 26 - 11 Interrupt Request Hold



Remark 1. Instruction N: Interrupt request hold instruction
Remark 2. Instruction M: Instruction other than interrupt request hold instruction

CHAPTER 27 STANDBY FUNCTION

27.1 Standby function

The standby function reduces the operating current of the system, and the following three modes are available.

(1) HALT mode

HALT instruction execution sets the HALT mode. In the HALT mode, the CPU operation clock is stopped. If the high-speed system clock oscillator, high-speed on-chip oscillator, or subsystem clock oscillator is operating before the HALT mode is set, oscillation of each clock continues. In this mode, the operating current is not decreased as much as in the STOP mode, but the HALT mode is effective for restarting operation immediately upon interrupt request generation and carrying out intermittent operations frequently.

(2) STOP mode

STOP instruction execution sets the STOP mode. In the STOP mode, the high-speed system clock oscillator and high-speed on-chip oscillator stop, stopping the whole system, thereby considerably reducing the CPU operating current.

Because this mode can be cleared by an interrupt request, it enables intermittent operations to be carried out. However, because a wait time is required to secure the oscillation stabilization time after the STOP mode is released when the X1 clock is selected, select the HALT mode if it is necessary to start processing immediately upon interrupt request generation.

(3) SNOOZE mode

When reception of data through CSIp or UARTq, a request for A/D conversion by the 10-bit A/D converter issued by a trigger signal from a timer (interrupt request signal (INTRTC/INTIT) or event trigger from the ELC), or activation of the DTC leads to release from STOP mode, reception of data through CSIp or UARTq, A/D conversion by the 10-bit A/D converter, or activation of the DTC proceeds without CPU operations. This mode is only available when the high-speed on-chip oscillator is selected as the CPU/peripheral hardware clock (f_{CLK}).

In either of these two modes, all the contents of registers, flags and data memory just before the standby mode is set are held. The I/O port output latches and output buffer statuses are also held.

Caution 1. The STOP mode can be used only when the CPU is operating on the main system clock. The STOP mode cannot be set while the CPU operates with the subsystem clock. The HALT mode can be used when the CPU is operating on either the main system clock or the subsystem clock.

Caution 2. When shifting to the STOP mode, be sure to stop the peripheral hardware operation operating with main system clock before executing STOP instruction (except SNOOZE mode setting unit).

Caution 3. When using CSIp, UARTq, or 10-bit A/D converter in the SNOOZE mode, set up serial standby control register m (SSCm) and A/D converter mode register 2 (ADM2) before switching to the STOP mode. For details, see 20.3 Registers Controlling Serial Array Unit and 19.3 Registers controlling A/D converter.

Caution 4. The following sequence is recommended for operating current reduction of the 10-bit A/D converter when the standby function is used: First clear bit 7 (ADCS) and bit 0 (ADCE) of A/D converter mode register 0 (ADM0) to 0 to stop the A/D conversion operation, and then execute the STOP instruction.

Caution 5. Whether to continue oscillating or stop the low-speed on-chip oscillator in the HALT or STOP mode can be selected by using the option byte. For details, see CHAPTER 33 OPTION BYTE.

Remark m: Unit number (m = 0, 1), p: CSI number (p = 00, 20), q: UART number (q = 0, 2)

27.2 Registers controlling standby function

The registers which control the standby function are described below.

- Subsystem clock supply mode control register (OSMC)
- Oscillation stabilization time counter status register (OSTC)
- Oscillation stabilization time select register (OSTS)

Remark For details of registers described above, see **CHAPTER 5 CLOCK GENERATOR**. For registers which control the SNOOZE mode, see **CHAPTER 20 SERIAL ARRAY UNIT**.

27.3 Standby Function Operation

27.3.1 HALT mode

(1) HALT mode

The HALT mode is set by executing the HALT instruction. HALT mode can be set regardless of whether the CPU clock before the setting was the high-speed system clock, high-speed on-chip oscillator clock, or subsystem clock.

The operating statuses in the HALT mode are shown below.

Caution Because the interrupt request signal is used to clear the HALT mode, if the interrupt mask flag is 0 (the interrupt processing is enabled) and the interrupt request flag is 1 (the interrupt request signal is generated), the HALT mode is not entered even if the HALT instruction is executed in such a situation.

Table 27 - 1 Operating Statuses in HALT Mode (1/2)

Item \ HALT Mode Setting			When HALT Instruction is Executed While CPU is Operating on Main System Clock		
			When CPU is Operating on High-speed On-chip Oscillator Clock (f_{IH})	When CPU is Operating on X1 Clock (f_X)	When CPU is Operating on External Main System Clock (f_{EX})
System clock			Clock supply to the CPU is stopped		
	Main system clock	f_{IH}	Operation continues (cannot be stopped)	Operation disabled	
		f_X	Operation disabled	Operation continues (cannot be stopped)	Cannot operate
		f_{EX}		Cannot operate	Operation continues (cannot be stopped)
	Subsystem clock	f_{XT}	Status before HALT mode was set is retained		
		f_{EXT}			
	f_{IL}		Set by bits 0 (WDSTBYON) and 4 (WDTON) of option byte (000C0H), and WUTMMCK0 bit of subsystem clock supply mode control register (OSMC) • WUTMMCK0 = 1: Oscillates • WUTMMCK0 = 0 and WDTON = 0: Stops • WUTMMCK0 = 0, WDTON = 1, and WDSTBYON = 1: Oscillates • WUTMMCK0 = 0, WDTON = 1, and WDSTBYON = 0: Stops		
CPU			Operation stopped		
Code flash memory			Operation stopped		
Data flash memory					
RAM			Operation stopped (Operable while in the DTC is executed)		
Port (latch)			Status before HALT mode was set is retained		
Timer array unit			Operable		
8-bit interval timer					
Real-time clock 2					
12-bit Interval timer					
Sampling output timer detector Note 1			Operable		
External signal sampler Note 1			Operable only when the external signal sampler is operating on the subsystem clock.		
Timer RJ Note 1			Operable		
Watchdog timer			See **CHAPTER 14 WATCHDOG TIMER**.		
Clock output/buzzer output			Operable		
10-bit A/D converter					
Analog front-end power supply circuit Note 2					
24-bit ΔΣ A/D converter with programmable gain instrumentation amplifier Note 2					
D/A converter		8 bits Note 2			
		12 bits Note 3			
Amplifier unit Note 2					
Serial array unit (SAU)					
Serial interface (IICA)					
Serial interface UARTMG Note 1					
LCD controller/driver			Operable (However, this depends on the status of the clock selected as the LCD source clock: operation is possible if the selected clock is operating, but operation will stop if the selected clock is stopped.)		
DTC			Operable		
ELC			Operable function blocks can be linked		
Power-on-reset function			Operable		
Voltage detection function					
External interrupt					
Key interrupt function					
CRC operation function		High-speed CRC			
		General-purpose CRC	Operation stopped (capable of operation in response to access by the DTC to obtain data for calculations from the RAM area)		
RAM parity error detection function			Operation stopped (Operable while in the DTC is executed)		
RAM guard function					
SFR guard function					
Illegal-memory access detection function					

(**Notes** and **Remark** are listed on the next page.)

Note 1. R5F11RM only.
Note 2. R5F11NM, R5F11NL, R5F11PL, and R5F11NG only.
Note 3. R5F11NL, R5F11PL, and R5F11NG only.

Remark Operation stopped: Operation is automatically stopped before switching to the HALT mode.
Operation disabled: Operation is stopped before switching to the HALT mode.
f_{IH}: High-speed on-chip oscillator clock
f_{IL}: Low-speed on-chip oscillator clock
f_X: X1 clock
f_{EX}: External main system clock
f_{XT}: XT1 clock
f_{EXT}: External subsystem clock

Table 27 - 1 Operating Statuses in HALT Mode (2/2)

Item \ HALT Mode Setting		When HALT Instruction is Executed While CPU is Operating on Subsystem Clock	
		When CPU is Operating on XT1 Clock (f_{XT})	When CPU is Operating on External Subsystem Clock (f_{EXT})
System clock		Clock supply to the CPU is stopped	
Main system clock	f_{IH}	Operation disabled	
	f_X		
	f_{EX}		
Subsystem clock	f_{XT}	Operation continues (cannot be stopped)	Cannot operate
	f_{EXT}	Cannot operate	Operation continues (cannot be stopped)
f_{IL}		Set by bits 0 (WDSTBYON) and 4 (WDTON) of option byte (000C0H), and WUTMMCK0 bit of subsystem clock supply mode control register (OSMC) • WUTMMCK0 = 1: Oscillates • WUTMMCK0 = 0 and WDTON = 0: Stops • WUTMMCK0 = 0, WDTON = 1, and WDSTBYON = 1: Oscillates • WUTMMCK0 = 0, WDTON = 1, and WDSTBYON = 0: Stops	
CPU		Operation stopped	
Code flash memory			
Data flash memory			
RAM		Operation stopped (Operable while in the DTC is executed)	
Port (latch)		Status before HALT mode was set is retained	
Timer array unit		Operable (Operation is disabled while in the low consumption RTC mode (when the RTCLPC bit of the OSMC register is 1))	
8-bit interval timer		Operable	
Real-time clock 2			
12-bit Interval timer			
Sampling output timer detector Note 1		Operable	
External signal sampler Note 1		Operable	
Timer RJ Note 1		Operable (Operation is disabled while in the low consumption RTC mode (when the RTCLPC bit of the OSMC register is 1))	
Watchdog timer		See **CHAPTER 14 WATCHDOG TIMER**.	
Clock output/buzzer output		Operable (Operation is disabled while in the low consumption RTC mode (when the RTCLPC bit of the OSMC register is 1))	
10-bit A/D converter		Operation disabled	
Analog front-end power supply circuit Note 2		Status before HALT mode was set is retained	
24-bit ΔΣ A/D converter with programmable gain instrumentation amplifier Note 2		Operable (Operation is disabled while in the low consumption RTC mode (when the RTCLPC bit of the OSMC register is 1))	
D/A converter	8 bits Note 2		
	12 bits Note 3		
Amplifier unit Note 2			
Serial array unit (SAU)			
Serial interface (IICA)		Operation disabled	
Serial interface UARTMG Note 1		Operable	
LCD controller/driver		Operable (However, this depends on the status of the clock selected as the LCD source clock: operation is possible if the selected clock is operating, but operation will stop if the selected clock is stopped.)	
DTC		Operable (Operation is disabled while in the low consumption RTC mode (when the RTCLPC bit of the OSMC register is 1))	
ELC		Operable function blocks can be linked	
Power-on-reset function		Operable	
Voltage detection function			
External interrupt			
Key interrupt function			
CRC operation function	High-speed CRC	Operation disabled	
	General-purpose CRC	Operation stopped (capable of operation in response to access by the DTC to obtain data for calculations from the RAM area)	
RAM parity error detection function		Operation stopped (Operable while in the DTC is executed)	
RAM guard function			
SFR guard function			
Illegal-memory access detection function			

(**Notes** and **Remark** are listed on the next page.)

Note 1. R5F11RM only.
Note 2. R5F11NM, R5F11NL, R5F11PL, and R5F11NG only.
Note 3. R5F11NL, R5F11PL, and R5F11NG only.

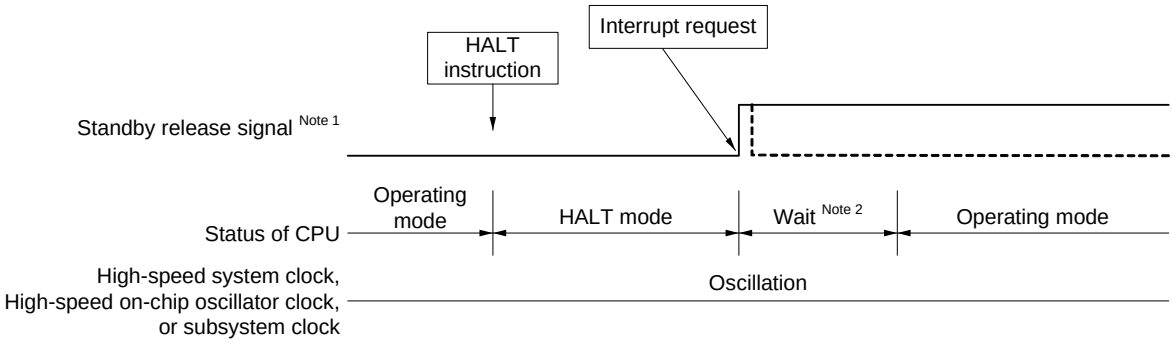
Remark Operation stopped: Operation is automatically stopped before switching to the HALT mode.
Operation disabled: Operation is stopped before switching to the HALT mode.
f_{IH}: High-speed on-chip oscillator clock
f_{IL}: Low-speed on-chip oscillator clock
f_X: X1 clock
f_{EX}: External main system clock
f_{XT}: XT1 clock
f_{EXT}: External subsystem clock

(2) The HALT mode can be released by the following two sources.

(a) Release by unmasked interrupt request

When an unmasked interrupt request is generated, the HALT mode is released. If interrupt acknowledgment is enabled, vectored interrupt servicing is carried out. If interrupt acknowledgment is disabled, the next address instruction is executed.

Figure 27 - 1 HALT Mode Release by Interrupt Request Generation



Note 1. For details of the standby release signal, see **Figure 26 - 1**.
Note 2. Wait time for HALT mode release
- When vectored interrupt servicing is carried out
  Main system clock: 15 to 16 clocks
  Subsystem clock (RTCLPC = 0): 10 to 11 clocks
  Subsystem clock (RTCLPC = 1): 11 to 12 clocks
- When vectored interrupt servicing is not carried out
  Main system clock: 9 to 10 clocks
  Subsystem clock (RTCLPC = 0): 4 to 5 clocks
  Subsystem clock (RTCLPC = 1): 5 to 6 clocks

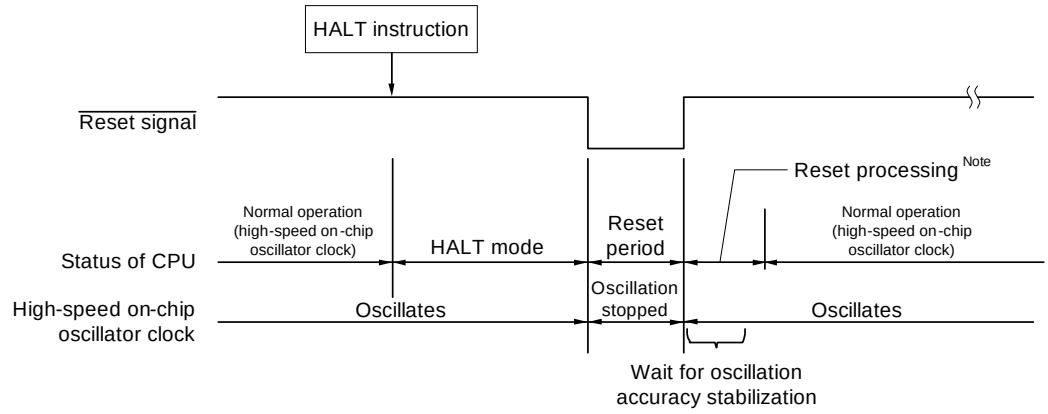
Remark The broken lines indicate the case when the interrupt request which has released the standby mode is acknowledged.

(b) Release by reset signal generation

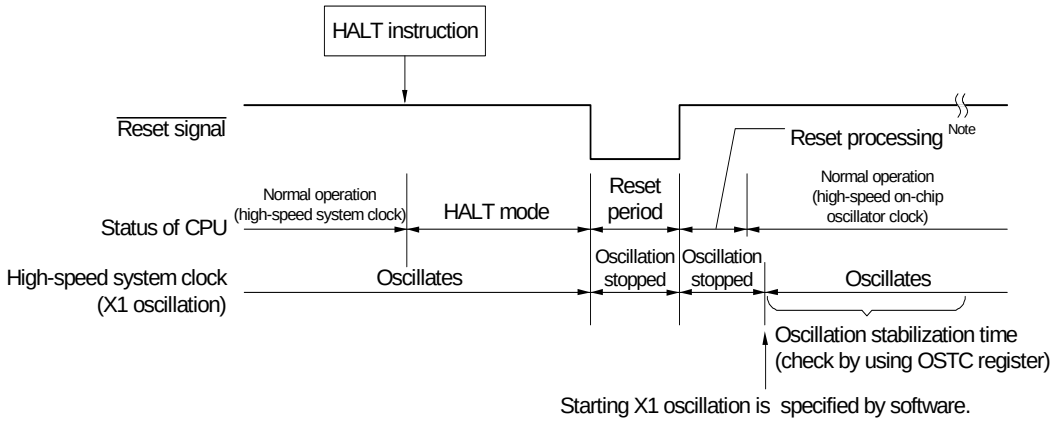
When the reset signal is generated, HALT mode is released, and then, as in the case with a normal reset operation, the program is executed after branching to the reset vector address.

Figure 27 - 2 HALT Mode Release by Reset (1/2)

(1) When high-speed on-chip oscillator clock is used as CPU clock



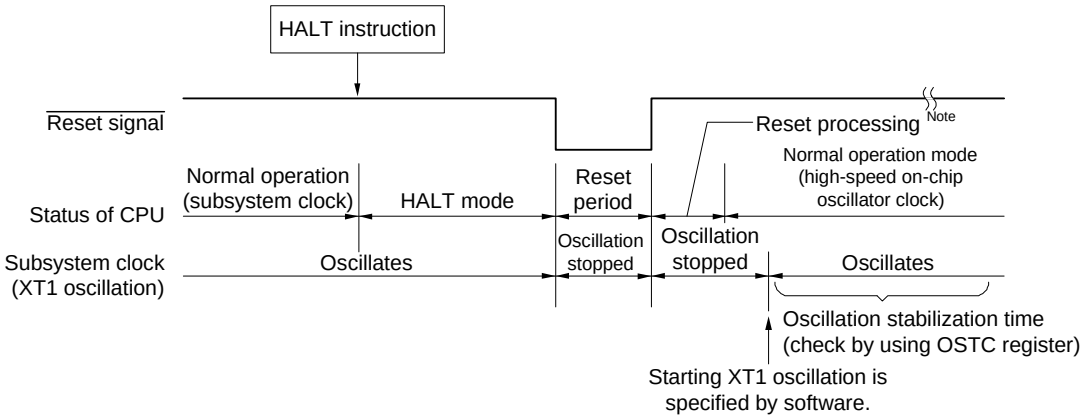
(2) When high-speed system clock is used as CPU clock



Note For the reset processing time, see **CHAPTER 28 RESET FUNCTION**. For the reset processing time of the power-on-reset circuit (POR) and voltage detector (LVD), see **CHAPTER 29 POWER-ON-RESET CIRCUIT**.

Figure 27 - 2 HALT Mode Release by Reset (2/2)

(3) When subsystem clock is used as CPU clock



Note For the reset processing time, see **CHAPTER 28 RESET FUNCTION**. For the reset processing time of the power-on-reset circuit (POR) and voltage detector (LVD), see **CHAPTER 29 POWER-ON-RESET CIRCUIT**.

27.3.2 STOP mode

(1) STOP mode setting and operating statuses

The STOP mode is set by executing the STOP instruction, and it can be set only when the CPU clock before the setting was the high-speed on-chip oscillator clock, X1 clock, or external main system clock.

Caution Because the interrupt request signal is used to clear the STOP mode, if the interrupt mask flag is 0 (the interrupt processing is enabled) and the interrupt request flag is 1 (the interrupt request signal is generated), the STOP mode is immediately cleared if set when the STOP instruction is executed in such a situation.
Accordingly, once the STOP instruction is executed, the system returns to its normal operating mode after the elapse of release time from the STOP mode.

The operating statuses in the STOP mode are shown below.

Table 27 - 2 Operating Statuses in STOP Mode (1/2)

Item \ STOP Mode Setting	When STOP Instruction is Executed While CPU is Operating on Main System Clock		
	When CPU is Operating on High-speed On-chip Oscillator Clock (f_{IH})	When CPU is Operating on X1 Clock (f_X)	When CPU is Operating on External Main System Clock (f_{EX})
System clock	Clock supply to the CPU is stopped		
Main system clock: f_{IH}	Stopped		
Main system clock: f_X			
Main system clock: f_{EX}			
Subsystem clock: f_{XT}	Status before STOP mode was set is retained		
Subsystem clock: f_{EXT}			
f_{IL}	Set by bits 0 (WDSTBYON) and 4 (WDTON) of option byte (000C0H), and WUTMMCK0 bit of subsystem clock supply mode control register (OSMC) • WUTMMCK0 = 1: Oscillates • WUTMMCK0 = 0 and WDTON = 0: Stops • WUTMMCK0 = 0, WDTON = 1, and WDSTBYON = 1: Oscillates • WUTMMCK0 = 0, WDTON = 1, and WDSTBYON = 0: Stops		
CPU	Operation stopped		
Code flash memory			
Data flash memory	Operation stopped		
RAM	Operation stopped		
Port (latch)	Status before STOP mode was set is retained		
Timer array unit	Operation disabled		
8-bit interval timer	Operable		
Real-time clock 2			
12-bit Interval timer			
Sampling output timer detector Note 1	Operable		
External signal sampler Note 1	Operable: Note, however, that the external signal sampler edge detection interrupt signal (INTEXSD) is not generated, and the EXSDD01, EXSDD00, and PRTY0 bits in external signal sampler control register 0 (EXSDM0) are not updated.		
Timer RJ Note 1	• Operable in event count mode when TRJIO input with no filer is selected • Operable when the subsystem clock is selected as the count source and RTCLPC in the OSMC register is 0 • Operable when the low-speed on-chip oscillator is selected as the count source • Operation is disabled under any conditions other than the above		
Watchdog timer	See **CHAPTER 14 WATCHDOG TIMER**.		
Clock output/buzzer output	Operable only when subsystem clock is selected as the count clock (when low-consumption RTC mode (set RTCLPC bit of OSMC register to 1), operation disabled)		
10-bit A/D converter	Wakeup operation is enabled (switching to SNOOZE mode)		
Analog front-end power supply circuit Note 2	Operable		
24-bit ΔΣ A/D converter with programmable gain instrumentation amplifier Note 2	Operation disabled		
D/A converter: 8 bits Note 2	Operable (status before STOP mode was set is retained)		
D/A converter: 12 bits Note 3			
Amplifier unit Note 2	Operation disabled		
Serial array unit (SAU)	Wakeup operation is enabled only for CSIp and UARTq (switching to the SNOOZE mode) Operation is disabled for anything other than CSIp and UARTq		
Serial interface (IICA)	Wakeup by address match operable		
Serial interface UARTMG Note 1	Operable		
LCD controller/driver	Operable (However, this depends on the status of the clock selected as the LCD source clock: operation is possible if the selected clock is operating, but operation will stop if the selected clock is stopped.)		
DTC	DTC activation source receiving operation enabled (switching to SNOOZE mode)		
ELC	Operable function blocks can be linked		
Power-on-reset function	Operable		
Voltage detection function			
External interrupt			

Table 27 - 2 Operating Statuses in STOP Mode (2/2)

STOP Mode Setting / Item		When STOP Instruction is Executed While CPU is Operating on Main System Clock		
		When CPU is Operating on High-speed On-chip Oscillator Clock (f_{IH})	When CPU is Operating on X1 Clock (f_X)	When CPU is Operating on External Main System Clock (f_{EX})
CRC operation function	High-speed CRC	Operation stopped		
	General-purpose CRC			
RAM parity error detection function				
RAM guard function				
SFR guard function				
Illegal-memory access detection function				

Note 1. R5F11RM only.

Note 2. R5F11NM, R5F11NL, R5F11PL, and R5F11NG only.

Note 3. R5F11NL, R5F11PL, and R5F11NG only.

Caution To use the peripheral hardware that stops operation in the STOP mode, and the peripheral hardware for which the clock that stops oscillating in the STOP mode after the STOP mode is released, restart the peripheral hardware.

Remark 1. Operation stopped: Operation is automatically stopped before switching to the HALT mode.
Operation disabled: Operation is stopped before switching to the HALT mode.
f_{IH}: High-speed on-chip oscillator clock
f_{IL}: Low-speed on-chip oscillator clock
f_X: X1 clock
f_{EX}: External main system clock
f_{XT}: XT1 clock
f_{EXT}: External subsystem clock

Remark 2. p = 00, 20; q = 0, 2

(2) STOP mode release

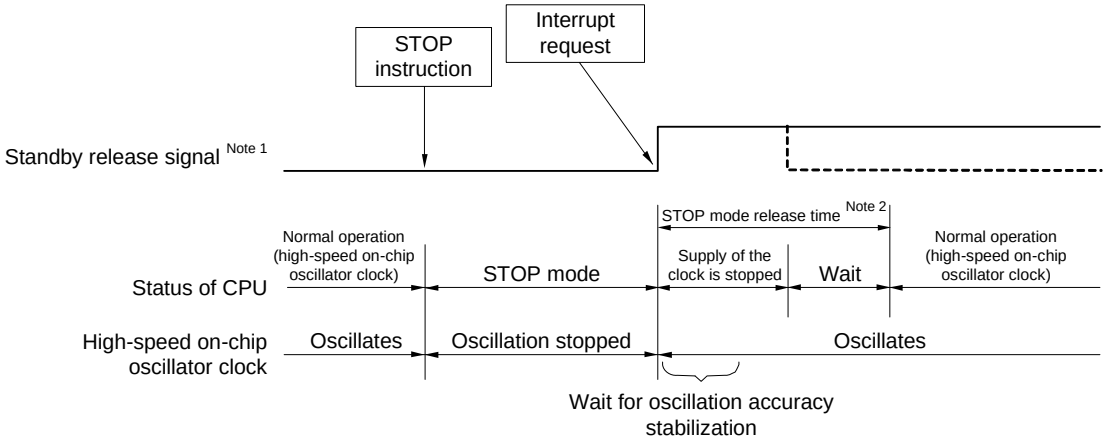
The STOP mode can be released by the following two sources.

(a) Release by unmasked interrupt request

When an unmasked interrupt request is generated, the STOP mode is released. After the oscillation stabilization time has elapsed, if interrupt acknowledgment is enabled, vectored interrupt servicing is carried out. If interrupt acknowledgment is disabled, the next address instruction is executed.

Figure 27 - 3 STOP Mode Release by Interrupt Request Generation (1/2)

(1) When high-speed on-chip oscillator clock is used as CPU clock



Note 1. For details of the standby release signal, see **Figure 26 - 1**.

Note 2. STOP mode release time

Supply of the clock is stopped: 18 μs to 65 μs

Wait:

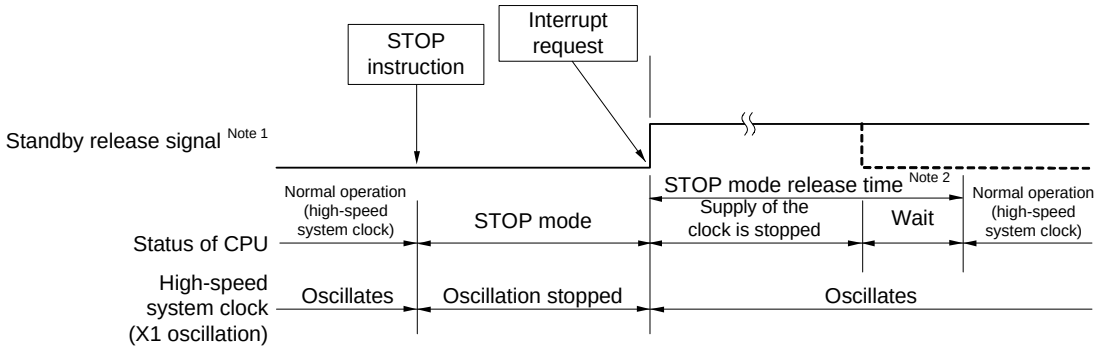
- When vectored interrupt servicing is carried out: 7 clocks
- When vectored interrupt servicing is not carried out: 1 clock

Remark 1. The clock supply stop time varies depending on the temperature conditions and STOP mode period.

Remark 2. The broken lines indicate the case when the interrupt request that has released the standby mode is acknowledged.

Figure 27 - 3 STOP Mode Release by Interrupt Request Generation (2/2)

(2) When high-speed system clock (X1 oscillation) is used as CPU clock



Note 1. For details of the standby release signal, see **Figure 26 - 1**.

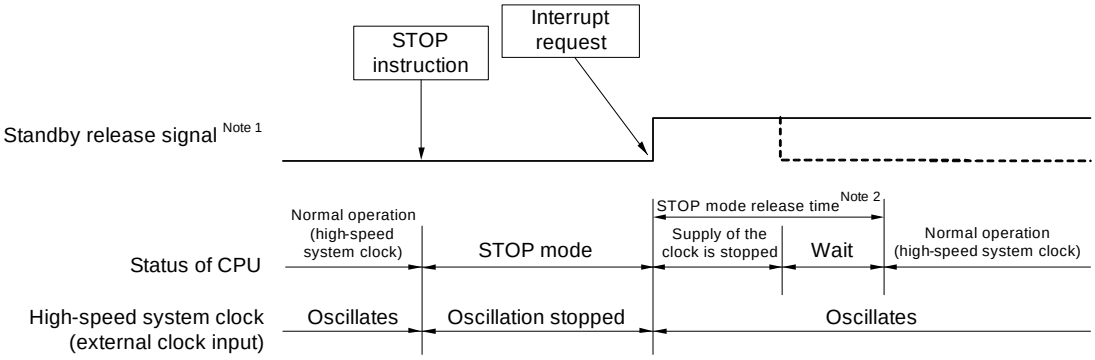
Note 2. STOP mode release time

Supply of the clock is stopped: 18 μs to “whichever is longer 65 μs or the oscillation stabilization time (set by OSTS)”

Wait:

- When vectored interrupt servicing is carried out: 10 to 11 clocks
- When vectored interrupt servicing is not carried out: 4 to 5 clocks

(3) When high-speed system clock (external clock input) is used as CPU clock



Note 1. For details of the standby release signal, see **Figure 26 - 1**.

Note 2. STOP mode release time

Supply of the clock is stopped: 18 μs to 65 μs

Wait:

- When vectored interrupt servicing is carried out: 7 clocks
- When vectored interrupt servicing is not carried out: 1 clock

Caution To reduce the oscillation stabilization time after release from the STOP mode while CPU operates based on the high-speed system clock (X1 oscillation), switch the clock to the high-speed on-chip oscillator clock temporarily before executing the STOP instruction.

Remark 1. The clock supply stop time varies depending on the temperature conditions and STOP mode period.

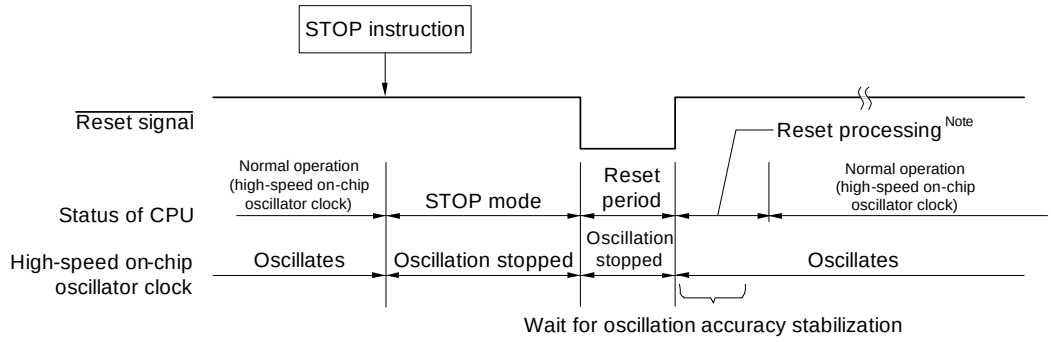
Remark 2. The broken lines indicate the case when the interrupt request that has released the standby mode is acknowledged.

(b) Release by reset signal generation

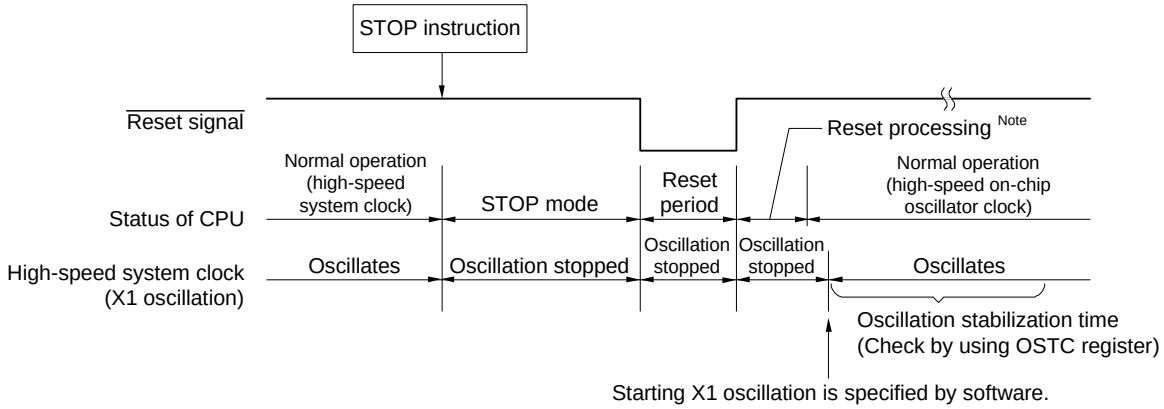
When the reset signal is generated, STOP mode is released, and then, as in the case with a normal reset operation, the program is executed after branching to the reset vector address.

Figure 27 - 4 STOP Mode Release by Reset

(1) When high-speed on-chip oscillator clock is used as CPU clock



(2) When high-speed system clock is used as CPU clock



Note For the reset processing time, see **CHAPTER 28 RESET FUNCTION**. For the reset processing time of the power-on-reset circuit (POR) and voltage detector (LVD), see **CHAPTER 29 POWER-ON-RESET CIRCUIT**.

27.3.3 SNOOZE mode

(1) SNOOZE mode setting and operating statuses

The CSIp, UARTq, A/D converter, and DTC can be placed in SNOOZE mode. Note that this mode can only be specified if the CPU clock is the high-speed on-chip oscillator clock.

When using CSIp or UARTq in the SNOOZE mode, set up serial standby control register m (SSCm) before switching to the STOP mode. For details, see **20.3 Registers Controlling Serial Array Unit**.

When using the A/D converter in the SNOOZE mode, set up A/D converter mode register 2 (ADM2) before switching to the STOP mode. For details, see **19.3 Registers Controlling A/D Converter**.

When DTC transfer is used in SNOOZE mode, before switching to the STOP mode, allow DTC activation by interrupt to be used. During STOP mode, detecting DTC activation by interrupt enables DTC transit to SNOOZE mode, automatically. For details, see **24.3 Registers Controlling DTC**.

Remark m: Unit number (m = 0, 1), p: CSI number (p = 00, 20), q: UART number (q = 0, 2)

In SNOOZE mode transition, wait status to be only following time.

Transition time from STOP mode to SNOOZE mode: 18 µs to 65 µs

Remark Transition time from STOP mode to SNOOZE mode varies depending on the temperature conditions and the STOP mode period.

Transition time from SNOOZE mode to normal operation:

- When vectored interrupt servicing is carried out:
  HS (High-speed main) mode: “4.99 µs to 9.44 µs” + 7 clocks
  LS (Low-speed main) mode: “1.10 µs to 5.08 µs” + 7 clocks

- When vectored interrupt servicing is not carried out:
  HS (High-speed main) mode: “4.99 µs to 9.44 µs” + 1 clock
  LS (Low-speed main) mode: “1.10 µs to 5.08 µs” + 1 clock

The operating statuses in the SNOOZE mode are shown next.

Table 27 - 3 Operating Statuses in SNOOZE Mode (1/2)

Item \ STOP Mode Setting			During STOP mode, reception of data through CSIp or UARTq, input of a trigger signal from a timer to the A/D converter, or activation of the DTC by an interrupt
			When CPU is Operating on High-speed On-chip Oscillator Clock (f_{IH})
System clock			Clock supply to the CPU is stopped
	Main system clock	f_{IH}	Operation started
		f_X	Stopped
		f_{EX}	
	Subsystem clock	f_{XT}	Use of the status while in the STOP mode continues
		f_{EXT}	
	f_{IL}		Set by bits 0 (WDSTBYON) and 4 (WDTON) of option byte (000C0H), and WUTMMCK0 bit of subsystem clock supply mode control register (OSMC) • WUTMMCK0 = 1: Oscillates • WUTMMCK0 = 0 and WDTON = 0: Stops • WUTMMCK0 = 0, WDTON = 1, and WDSTBYON = 1: Oscillates • WUTMMCK0 = 0, WDTON = 1, and WDSTBYON = 0: Stops
CPU			Operation stopped
Code flash memory			
Data flash memory			
RAM			Operation stopped (Operable while in the DTC is executed)
Port (latch)			Use of the status while in the STOP mode continues
Timer array unit			Operation disabled
8-bit interval timer			Operable
Real-time clock 2			
12-bit interval timer			
Sampling output timer detector Note 1			Operable when the subsystem clock is selected as the count source and RTCLPC in the OSMC register is 0.
External signal sampler Note 1			
Timer RJ Note 1			• Operable in event count mode when TRJIO input with no filer is selected • Operable when the subsystem clock is selected as the count source and RTCLPC in the OSMC register is 0 • Operable when the low-speed on-chip oscillator is selected as the count source • Operation is disabled under any conditions other than the above
Watchdog timer			See **CHAPTER 14 WATCHDOG TIMER**.
Clock output/buzzer output			Operable only when subsystem clock is selected as the count clock (when low-consumption RTC mode (set RTCLPC bit of OSMC register to 1), operation disabled)
10-bit A/D converter			Operable
Analog front-end power supply circuit Note 2			Operable
24-bit ΔΣ A/D converter with programmable gain instrumentation amplifier Note 2			Operation disabled
D/A converter		8 bits Note 2	Operable (Status before transitioning to SNOOZE is retained)
		12 bits Note 3	
Amplifier unit Note 2			Operation disabled
Serial array unit (SAU)			Operation is enabled only for CSIp and UARTq. Operation is disabled for other than CSIp and UARTq.
Serial interface (IICA)			Operation disabled
Serial interface UARTMG Note 1			Operable
LCD controller/driver			Operable (However, this depends on the status of the clock selected as the LCD source clock: operation is possible if the selected clock is operating, but operation will stop if the selected clock is stopped.)
DTC			Operable
ELC			Operable function blocks can be linked
Power-on-reset function			Operable
Voltage detection function			
External interrupt			
CRC operation function		High-speed CRC	Operation stopped
		General-purpose CRC	Operation disabled

(**Notes** and **Remarks** are listed on the next page.)

Table 27 - 3 Operating Statuses in SNOOZE Mode (2/2)

STOP Mode Setting / Item	During STOP mode, reception of data through CSIp or UARTq, input of a trigger signal from a timer to the A/D converter, or activation of the DTC by an interrupt
	When CPU is Operating on High-speed On-chip Oscillator Clock (f_{IH})
RAM parity error detection function	Operable while in the DTC is executed
RAM guard function	
SFR guard function	
Illegal-memory access detection function	

Note 1. R5F11RM only.

Note 2. R5F11NM, R5F11NL, R5F11PL, and R5F11NG only.

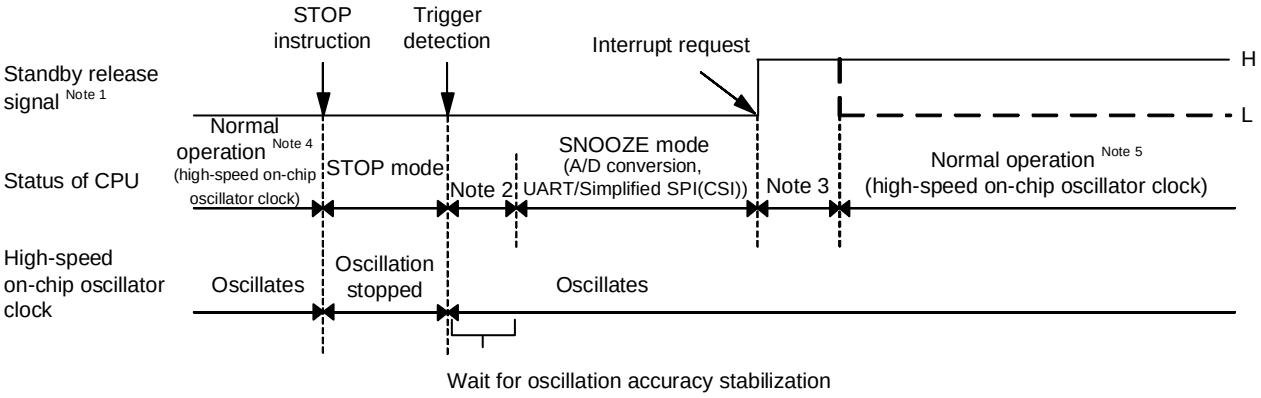
Note 3. R5F11NL, R5F11PL, and R5F11NG only.

Remark 1. Operation stopped: Operation is automatically stopped before switching to the HALT mode.
Operation disabled: Operation is stopped before switching to the HALT mode.
f_{IH}: High-speed on-chip oscillator clock
f_{IL}: Low-speed on-chip oscillator clock
f_X: X1 clock
f_{EX}: External main system clock
f_{XT}: XT1 clock
f_{EXT}: External subsystem clock

Remark 2. p: CSI number (p = 00, 20), q: UART number (q = 0, 2)

(2) Timing diagram when the interrupt request signal is generated in the SNOOZE mode

Figure 27 - 5 When the Interrupt Request Signal is Generated in the SNOOZE Mode



Note 1. For details of the standby release signal, see **Figure 26 - 1**.

Note 2. Transition time from STOP mode to SNOOZE mode

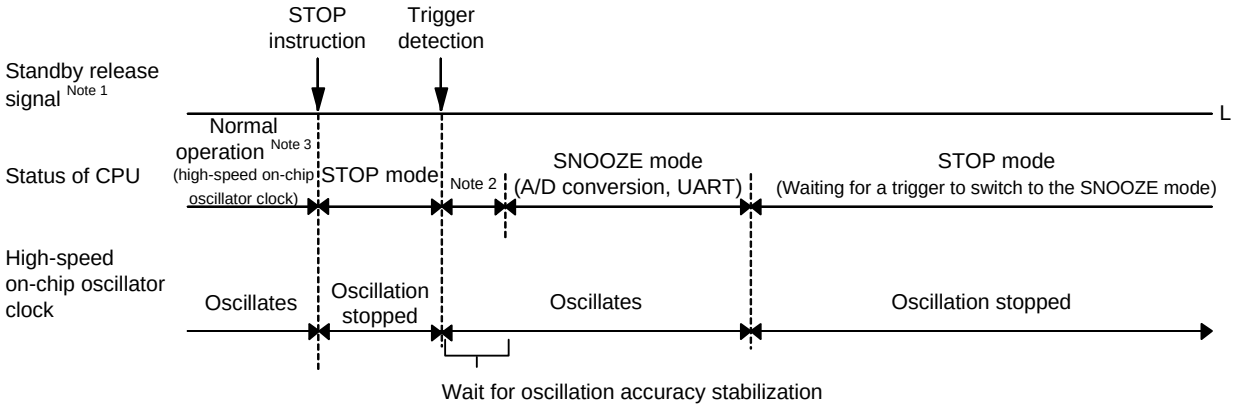
Note 3. Transition time from SNOOZE mode to normal operation

Note 4. Enable the SNOOZE mode (SWC = 1) immediately before switching to the STOP mode.

Note 5. Be sure to release the SNOOZE mode (SWC = 0) immediately after return to the normal operation.

(3) Timing diagram when the interrupt request signal is not generated in the SNOOZE mode

Figure 27 - 6 When the Interrupt Request Signal is not Generated in the SNOOZE Mode



Note 1. For details of the standby release signal, see **Figure 26 - 1**.

Note 2. Transition time from STOP mode to SNOOZE mode

Note 3. Enable the SNOOZE mode (SWC = 1) immediately before switching to the STOP mode.

Remark For details of the SNOOZE mode function, see **CHAPTER 19 A/D CONVERTER** and **CHAPTER 20 SERIAL ARRAY UNIT**.

CHAPTER 28 RESET FUNCTION

The following seven operations are available to generate a reset signal.

(1) External reset input via $\overline{\text{RESET}}$ pin
(2) Internal reset by watchdog timer program loop detection
(3) Internal reset by comparison of supply voltage and detection voltage of power-on-reset (POR) circuit
(4) Internal reset by comparison of supply voltage of the voltage detector (LVD) and detection voltage
(5) Internal reset by execution of illegal instruction Note
(6) Internal reset by RAM parity error
(7) Internal reset by illegal-memory access

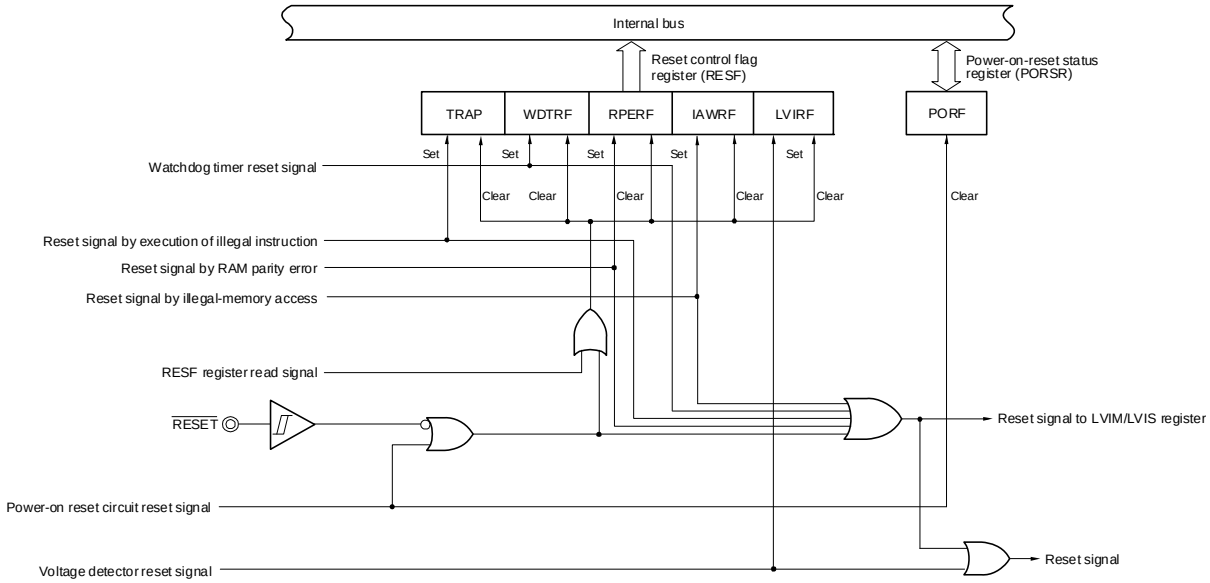
External and internal resets start program execution from the address at 00000H and 00001H when the reset signal is generated.
A reset is effected when a low level is input to the $\overline{\text{RESET}}$ pin, the watchdog timer overflows, or by POR and LVD circuit voltage detection, execution of illegal instruction Note, RAM parity error or illegal-memory access, and each item of hardware is set to the status shown in Table 28 - 1.

Note The illegal instruction is generated when instruction code FFH is executed.
Reset by the illegal instruction execution not issued by emulation with the in-circuit emulator or on-chip debug emulator.

Caution 1. For an external reset, input a low level for 10 μs or more to the $\overline{\text{RESET}}$ pin.
To perform an external reset upon power application, input a low level to the $\overline{\text{RESET}}$ pin, turn power on, continue to input a low level to the pin for 10 μs or more within the operating voltage range shown in 38.4 or 39.4 AC Characteristics, and then input a high level to the pin.
Caution 2. During reset input, the X1 clock, XT1 clock, high-speed on-chip oscillator clock, and low-speed on-chip oscillator clock oscillating. External main system clock input and external subsystem clock input become invalid.
Caution 3. The port pins become the following state because each SFR and 2nd SFR are initialized after reset.
- **P40: High-impedance during the external reset period or reset period by the POR. High level during other types of reset or after receiving a reset signal (connected to the internal pull-up resistance).**
- **Ports other than P40: High-impedance during the reset period or after receiving a reset signal.**

Remark V_{POR}: POR power supply rise detection voltage
V_{LVD}: LVD detection voltage

Figure 28 - 1 Block Diagram of Reset Function



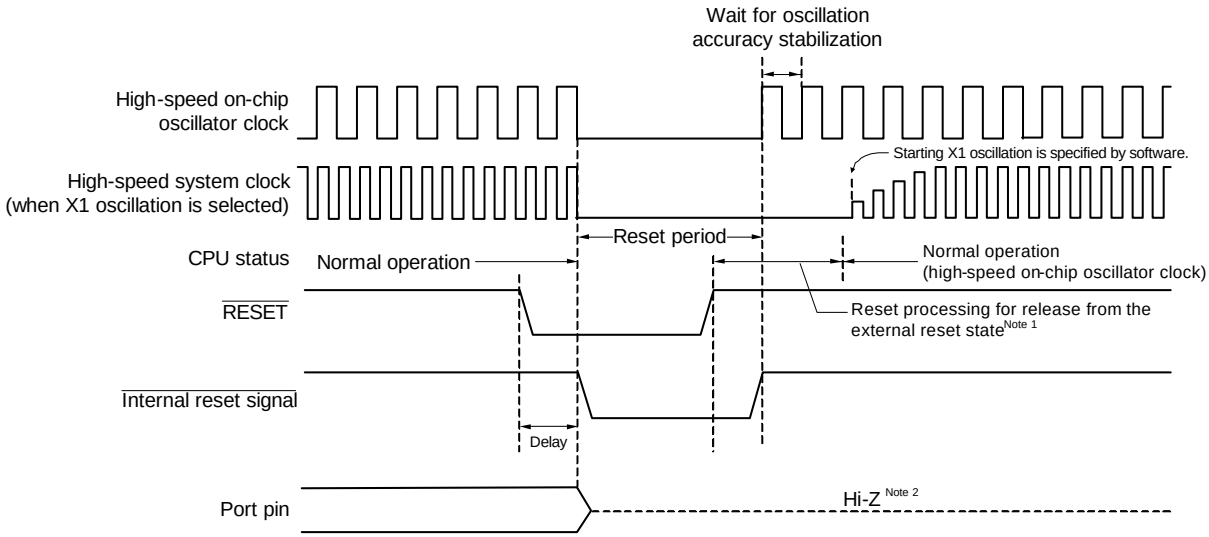
Caution An LVD circuit internal reset does not reset the LVD circuit.

Remark 1. LVIM: Voltage detection register
Remark 2. LVIS: Voltage detection level register

28.1 Timing of Reset Operation

This LSI is reset by input of the low level on the $\overline{\text{RESET}}$ pin and released from the reset state by input of the high level on the $\overline{\text{RESET}}$ pin. After reset processing, execution of the program with the high-speed on-chip oscillator clock as the operating clock starts.

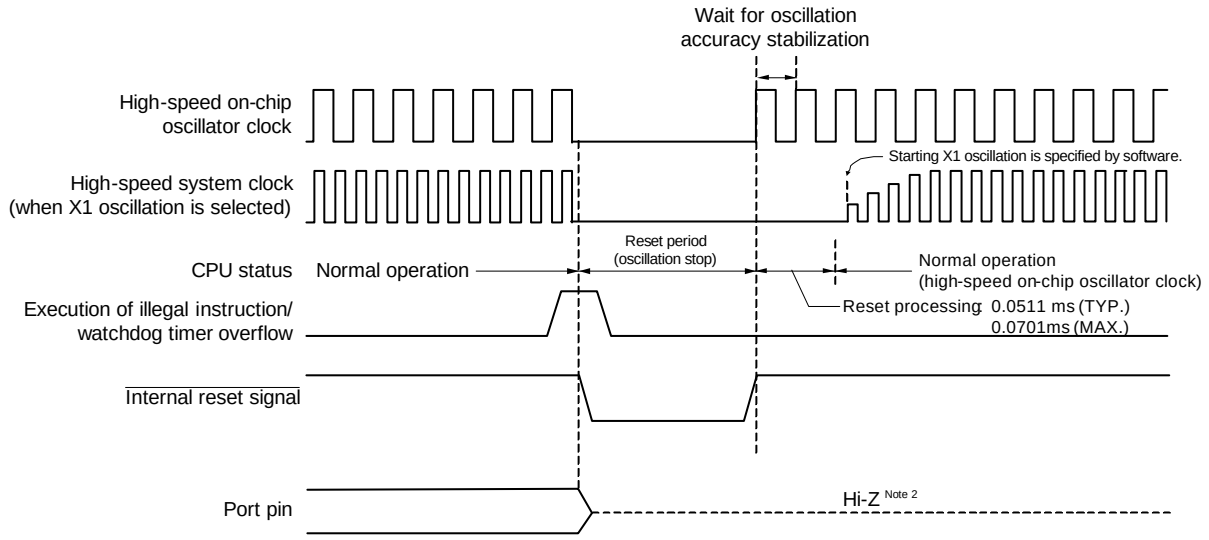
Figure 28 - 2 Timing of Reset by $\overline{\text{RESET}}$ Input



(**Notes** and **Caution** are listed on the next page.)

Release from the reset state is automatic in the case of a reset due to a watchdog timer overflow, execution of an illegal instruction, detection of a RAM parity error, or detection of illegal memory access. After reset processing, execution of the program with the high-speed on-chip oscillator clock as the operating clock starts.

Figure 28 - 3 Timing of Reset Due to Watchdog Timer Overflow, Execution of Illegal Instruction, Detection of RAM Parity Error, or Detection of Illegal Memory Access



(**Notes** and **Caution** are listed on the next page.)

Note 1. Reset times (times for release from the external reset state)

After the first release of the POR:	0.672 ms (typ.), 0.832 ms (max.) when the LVD is in use.
	0.399 ms (typ.), 0.519 ms (max.) when the LVD is off.
After the second release of the POR:	0.531 ms (typ.), 0.675 ms (max.) when the LVD is in use.
	0.259 ms (typ.), 0.362 ms (max.) when the LVD is off.

After power is supplied, a voltage stabilization waiting time of about 0.99 ms (typ.) and up to 2.30 ms (max.) is required before reset processing starts after release of the external reset.

Note 2. The state of P40 is as follows.

- High-impedance during the external reset period or reset period by the POR.
- High level during other types of reset or after receiving a reset signal (connected to the internal pull-up resistance).

Reset by POR and LVD circuit supply voltage detection is automatically released when internal $V_{DD} \geq V_{POR}$ or internal $V_{DD} \geq V_{LVD}$ after the reset. After reset processing, execution of the program with the high-speed on-chip oscillator clock as the operating clock starts.

For details, see **CHAPTER 29 POWER-ON-RESET CIRCUIT** or **CHAPTER 30 VOLTAGE DETECTOR**

Remark V_{POR}: POR power supply rise detection voltage
V_{LVD}: LVD detection voltage

28.2 States of Operation During Reset Periods

Table 28 - 1 shows the states of operation during reset periods. **Table 28 - 2** shows the states of the hardware after receiving a reset signal.

Table 28 - 1 Operation Statuses During Reset Period

Item			During Reset Period
System clock			Clock supply to the CPU is stopped.
	Main system clock	f_{IH}	Operation stopped
		f_X	Operation stopped (the X1 and X2 pins are input port mode)
		f_{EX}	Clock input invalid (the pin is input port mode)
	Subsystem clock	f_{XT}	During a reset other than the POR reset: Operation possible During a POR reset: Operation stopped (the X1 and X2 pins are input port mode)
		f_{EXT}	During a reset other than the POR reset: Operation possible During a POR reset: Clock input invalid (the pin is input port mode)
	f_{IL}		Operation stopped
CPU			Operation stopped
Code flash memory			
Data flash memory			
RAM			
Port (latch)			High impedance Note 1
Timer array unit			Operation stopped
8-bit interval timer			
Real-time clock 2			During a reset other than the POR reset: Operation possible During a POR reset: Calendar operation possible; operation of the RTCC0, RTCC1, and SUBCUD registers stops.
12-bit Interval timer			Operation stopped
Watchdog timer			
Clock output/buzzer output			
Sampling output timer detector Note 2			
External signal sampler Note 2			
Timer RJ Note 2			
10-bit A/D converter			
Analog front-end power supply circuit Note 3			
24-bit ΔΣ A/D converter with programmable gain instrumentation amplifier Note 3			
D/A converter		8 bits Note 3	
		12 bits Note 4	
Amplifier unit Note 3			
Serial array unit (SAU)			
Serial interface (IICA)			
Serial interface UARTMG Note 2			
LCD controller/driver			Operation stopped (COM only pin, COM/SEG alternate pin: GND output, SEG/general-purpose port alternate pin: high-impedance output, VL1 to VL4 pins: high-impedance output, CAPH/P127 pin, CAPL/P126 pin: high-impedance output)
DTC			Operation stopped
ELC			
Power-on-reset function			Detection operation possible
Voltage detection function			Operation is possible in the case of an LVD reset and stopped in the case of other types of reset.
External interrupt			Operation stopped
CRC operation function		High-speed CRC	
		General-purpose CRC	
RAM parity error detection function			
RAM guard function			
SFR guard function			
Illegal-memory access detection function			

(**Notes** and **Remark** are listed on the next page.)

Note 1. P40 becomes the following state.
- High-impedance during the external reset period or reset period by the POR. High level during other types of reset (connected to the on-chip pull-up resistance).

Note 2. R5F11R only.

Note 3. R5F11NM, R5F11NL, R5F11PL, and R5F11NG only.

Note 4. R5F11NL, R5F11PL, and R5F11NG only.

Remark f_{IH}: High-speed on-chip oscillator clock
f_X: X1 oscillation clock
f_{EX}: External main system clock
f_{XT}: XT1 oscillation clock
f_{EXT}: External subsystem clock
f_{IL}: Low-speed on-chip oscillator clock

Table 28 - 2 State of Hardware After Receiving a Reset Signal

Hardware		After Reset Acknowledgment Note
Program counter (PC)		The contents of the reset vector table (00000H, 00001H) are set.
Stack pointer (SP)		Undefined
Program status word (PSW)		06H
RAM	Data memory	Undefined
	General-purpose registers	Undefined

Note During reset signal generation or oscillation stabilization time wait, only the PC contents among the hardware statuses become undefined. All other hardware statuses remain unchanged after reset.

Remark For the state of the special function register (SFR) after receiving a reset signal, see **3.2.4 Special function register (SFR) area** and **3.2.5 Extended special function register (2nd SFR: 2nd Special Function Register) area**.

28.3 Register for Confirming Reset Source

28.3.1 Reset control flag register (RESF)

Many internal reset generation sources exist in the RL78 microcontroller. The reset control flag register (RESF) is used to store which source has generated the reset request.

The RESF register can be read by an 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input, reset by power-on-reset (POR) circuit, and reading the RESF register clear TRAP, WDTRF, RPERF, IAWRF, and LVIRF flags.

Figure 28 - 4 Format of Reset control flag register (RESF)

Address: FFFA8H After reset: Undefined Note 1 R

Symbol	7	6	5	4	3	2	1	0
RESF	TRAP	0	0	WDTRF	0	RPERF	IAWRF	LVIRF

TRAP	Internal reset request by execution of illegal instruction Note 2
0	Internal reset request is not generated, or the RESF register is cleared.
1	Internal reset request is generated.

WDTRF	Internal reset request by watchdog timer (WDT)
0	Internal reset request is not generated, or the RESF register is cleared.
1	Internal reset request is generated.

RPERF	Internal reset request t by RAM parity
0	Internal reset request is not generated, or the RESF register is cleared.
1	Internal reset request is generated.

IAWRF	Internal reset request t by illegal-memory access
0	Internal reset request is not generated, or the RESF register is cleared.
1	Internal reset request is generated.

LVIRF	Internal reset request by voltage detector (LVD)
0	Internal reset request is not generated, or the RESF register is cleared.
1	Internal reset request is generated.

Note 1. The value after reset varies depending on the reset source. See **Table 28 - 3**.

Note 2. The illegal instruction is generated when instruction code FFH is executed.
Reset by the illegal instruction execution not issued by emulation with the in-circuit emulator or on-chip debug emulator.

Caution 1. Do not read data by a 1-bit memory manipulation instruction.

Caution 2. An instruction code fetched from RAM is not subject to parity error detection while it is being executed. However, the data read by the instruction is subject to parity error detection.

Caution 3. Because the RL78's CPU executes look ahead due to the pipeline operation, the CPU might read an uninitialized RAM area that is allocated beyond the RAM used, which causes a RAM parity error. Therefore, when enabling RAM parity error resets (RPERDIS = 0), be sure to initialize the used RAM area + 10 bytes.

The status of the RESF register when a reset request is generated is shown in **Table 28 - 3**.

Table 28 - 3 RESF Register Status When Reset Request Is Generated

Reset Source / Flag	$\overline{\text{RESET}}$ Input	Reset by POR	Reset by Execution of Illegal Instruction	Reset by WDT	Reset by RAM parity error	Reset by illegal-memory access	Reset by LVD
TRAP bit	Cleared (0)	Cleared (0)	Set (1)	Held	Held	Held	Held
WDTRF bit			Held	Set (1)			
RPERF bit				Held	Set (1)		
IAWRF bit					Held	Set (1)	
LVIRF bit						Held	Set (1)

The RESF register is automatically cleared when it is read by an 8-bit memory manipulation instruction.

28.3.2 Power-on-reset status register (PORSR)

The PORSR register is used to check the occurrence of a power-on reset.

Writing 1 to bit 0 (PORF) of the PORSR register enables this function. Writing 0 disables this function.

Write 1 to the PORF bit in advance to enable checking of the occurrence of a power-on reset.

The PORSR register can be set by an 8-bit memory manipulation instruction.

Power-on reset signal generation clears this register to 00H.

Caution 1. The PORSR register is reset only by a power-on reset; it retains the value when a reset caused by another factor occurs.

Caution 2. If the PORF bit is set to 1, it guarantees that no power-on reset has occurred, but it does not guarantee that the RAM value is retained.

Figure 28 - 5 Format of Power-on-reset status register (PORSR)

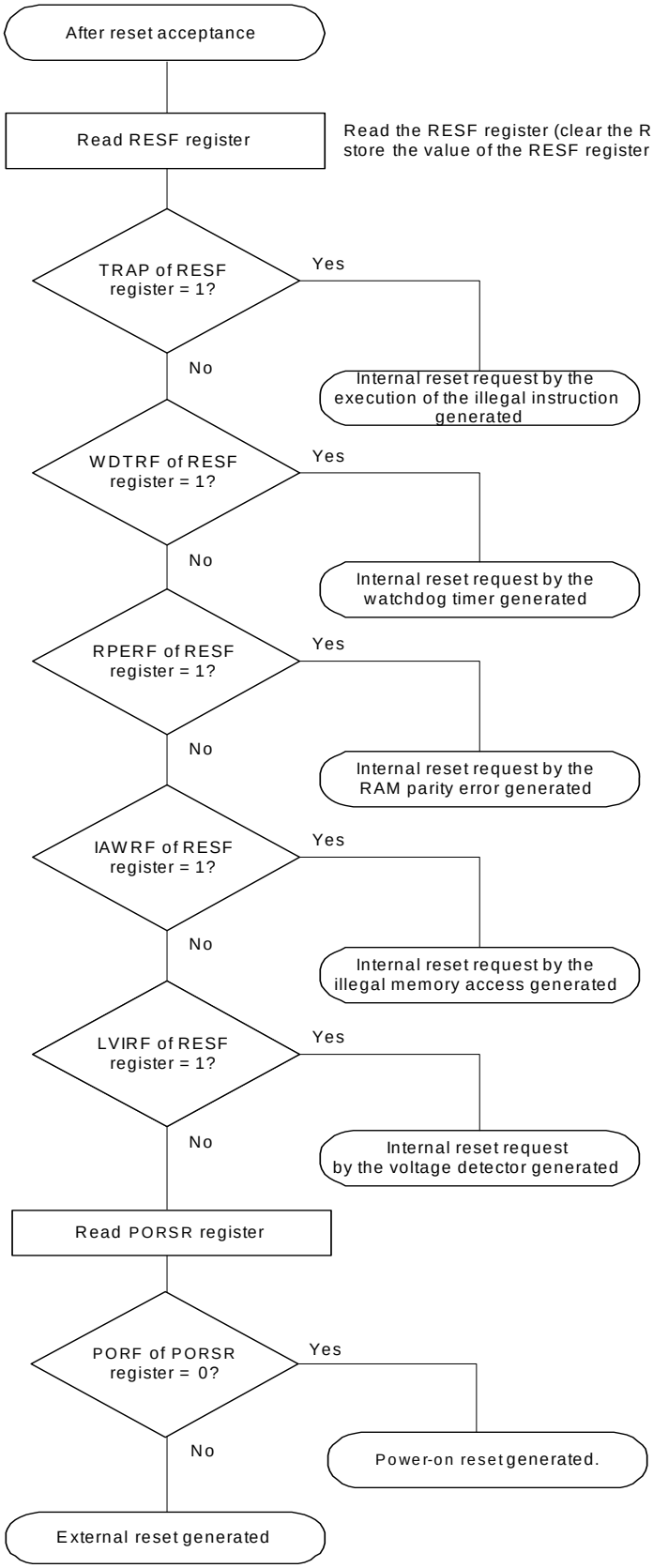
Address: F00F9H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
PORSR	0	0	0	0	0	0	0	PORF

PORF	Checking occurrence of power-on reset
0	A value 1 has not been written, or a power-on reset has occurred.
1	No power-on reset has occurred.

Figure 28 - 6 shows the example of procedure for checking a reset source.

Figure 28 - 6 Example of Procedure for Checking Reset Source



Caution Write 1 to bit 0 (PORF) of the PORSR register before receiving a reset signal.

CHAPTER 29 POWER-ON-RESET CIRCUIT

29.1 Functions of Power-on-reset Circuit

The power-on-reset circuit (POR) has the following functions.

- Generates internal reset signal at power on.
  The reset signal is released when the supply voltage (V_{DD}) exceeds the detection voltage (V_{POR}). Note that the reset state must be retained until the operating voltage becomes in the range defined in **38.4** or **39.4 AC Characteristics**.
  This is done by utilizing the voltage detection circuit or controlling the externally input reset signal.

- Compares supply voltage (V_{DD}) and detection voltage (V_{PDR}), generates internal reset signal when $V_{DD} < V_{PDR}$.
  Note that, after power is supplied, this LSI should be placed in the STOP mode, or in the reset state by utilizing the voltage detection circuit or externally input reset signal, before the operation voltage falls below the range defined in **38.4** or **39.4 AC Characteristics**. When restarting the operation, make sure that the operation voltage has returned within the range of operation.

Caution **If an internal reset signal is generated in the power-on-reset circuit, the reset control flag register (RESF) and the power-on-reset status register (PORSR) are cleared (00H).**

Remark 1. The RL78 microcontroller incorporates multiple hardware functions that generate an internal reset signal. A flag that indicates the reset source is located in the reset control flag register (RESF) for when an internal reset signal is generated by the watchdog timer (WDT), voltage-detector (LVD), illegal instruction execution, RAM parity error, or illegal-memory access. The RESF register is not cleared to 00H and the flag is set to 1 when an internal reset signal is generated by the watchdog timer (WDT), voltage-detector (LVD), illegal instruction execution, RAM parity error, or illegal-memory access.
For details of the RESF register, see **CHAPTER 28 RESET FUNCTION**.

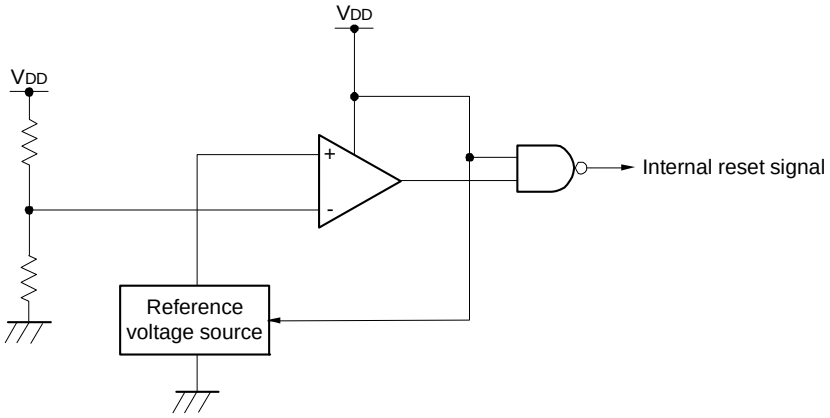
Remark 2. The occurrence of an internal reset in the power-on-reset circuit can be checked by the power-on reset status register (PORSR). For details on the PORSR register, refer to **CHAPTER 28 RESET FUNCTION**.

Remark 3. V_{POR}: POR power supply rise detection voltage
V_{PDR}: POR power supply fall detection voltage
For details, see **38.6.3** or **39.6.3 POR circuit characteristics**.

29.2 Configuration of Power-on-reset Circuit

The block diagram of the power-on-reset circuit is shown in Figure 29 - 1.

Figure 29 - 1 Block Diagram of Power-on-reset Circuit

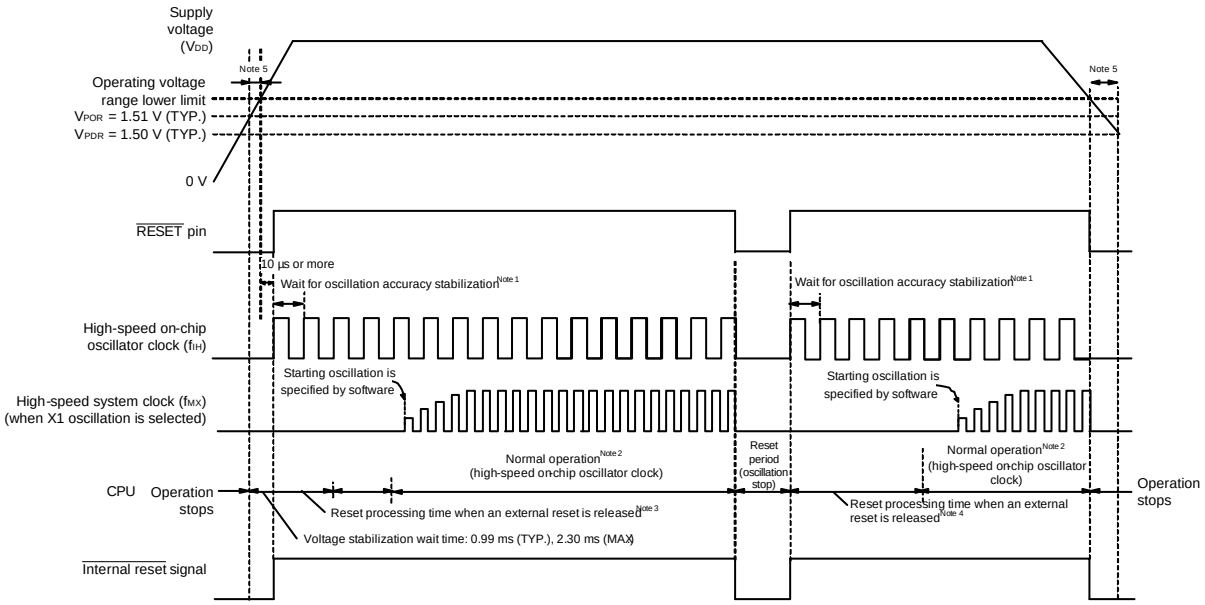


29.3 Operation of Power-on-reset Circuit

The timing of generation of the internal reset signal by the power-on-reset circuit and voltage detector is shown next.

Figure 29 - 2 Timing of Generation of Internal Reset Signal by Power-on-reset Circuit and Voltage Detector (1/3)

(1) When the externally input reset signal on the $\overline{\text{RESET}}$ pin is used



Note 1. The internal reset processing time includes the oscillation accuracy stabilization time of the high-speed on-chip oscillator clock.

Note 2. The high-speed on-chip oscillator clock and a high-speed system clock or subsystem clock can be selected as the CPU clock. To use the X1 clock, use the oscillation stabilization time counter status register (OSTC) to confirm the lapse of the oscillation stabilization time. To use the XT1 clock, use the timer function for confirmation of the lapse of the stabilization time.

Note 3. The time until normal operation starts includes the following reset processing time when the external reset is released (release from the first external reset following release from the POR state) after the $\overline{\text{RESET}}$ signal is driven high (1) as well as the voltage stabilization wait time after V_{POR} (1.51 V, typ.) is reached.

With the LVD circuit in use: 0.672 ms (typ.), 0.832 ms (max.)

With the LVD circuit not in use: 0.399 ms (typ.), 0.519 ms (max.)

Note 4. The reset processing times in the case of the second or subsequent external reset following release from the POR state are listed below.

With the LVD circuit in use: 0.531 ms (typ.), 0.675 ms (max.)

With the LVD circuit not in use: 0.259 ms (typ.), 0.362 ms (max.)

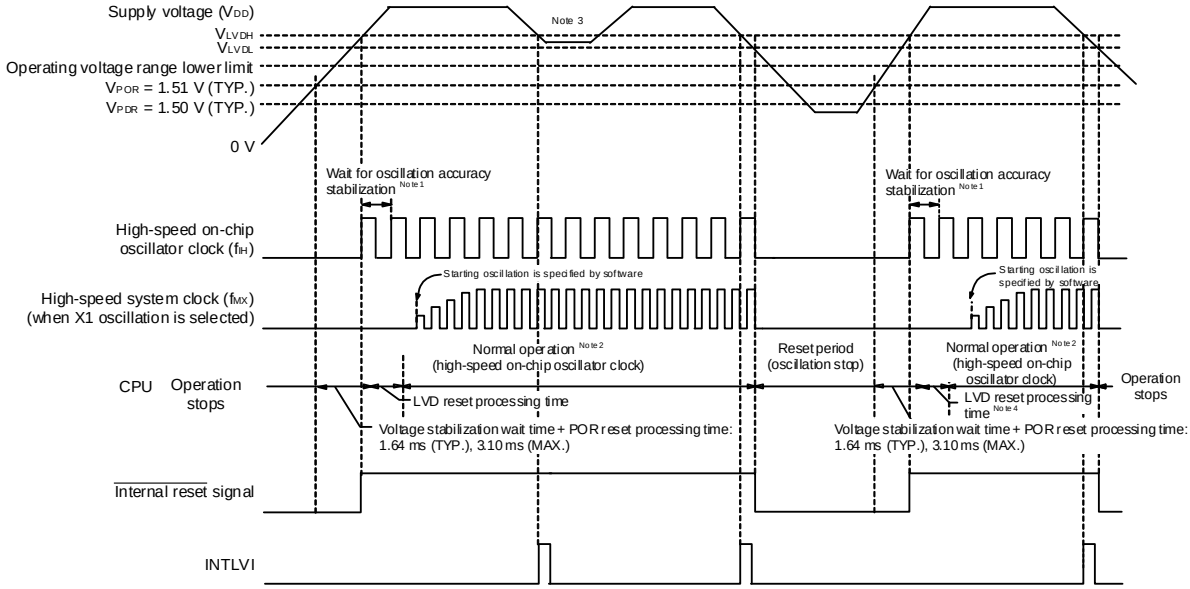
Note 5. After power is supplied, the reset state must be retained until the operating voltage becomes in the range defined in **38.4** or **39.4 AC Characteristics**. This is done by controlling the externally input reset signal.
After power supply is turned off, this LSI should be placed in the STOP mode, or in the reset state by utilizing the voltage detection circuit or externally input reset signal, before the voltage falls below the operating range. When restarting the operation, make sure that the operation voltage has returned within the range of operation.

Caution For power-on reset, be sure to use the externally input reset signal on the $\overline{\text{RESET}}$ pin when the LVD is off. For details, see CHAPTER 30 VOLTAGE DETECTOR.

Remark V_{POR}: POR power supply rise detection voltage
V_{PDR}: POR power supply fall detection voltage

Figure 29 - 3 Timing of Generation of Internal Reset Signal by Power-on-reset Circuit and Voltage Detector (2/3)

(2) When LVD interrupt & reset mode (option byte 000C1: LVIMDS1, LVIMDS0 = 1, 0)



Note 1. The internal reset processing time includes the oscillation accuracy stabilization time of the high-speed on-chip oscillator clock.

Note 2. The high-speed on-chip oscillator clock and a high-speed system clock or subsystem clock can be selected as the CPU clock. To use the X1 clock, use the oscillation stabilization time counter status register (OSTC) to confirm the lapse of the oscillation stabilization time. To use the XT1 clock, use the timer function for confirmation of the lapse of the stabilization time.

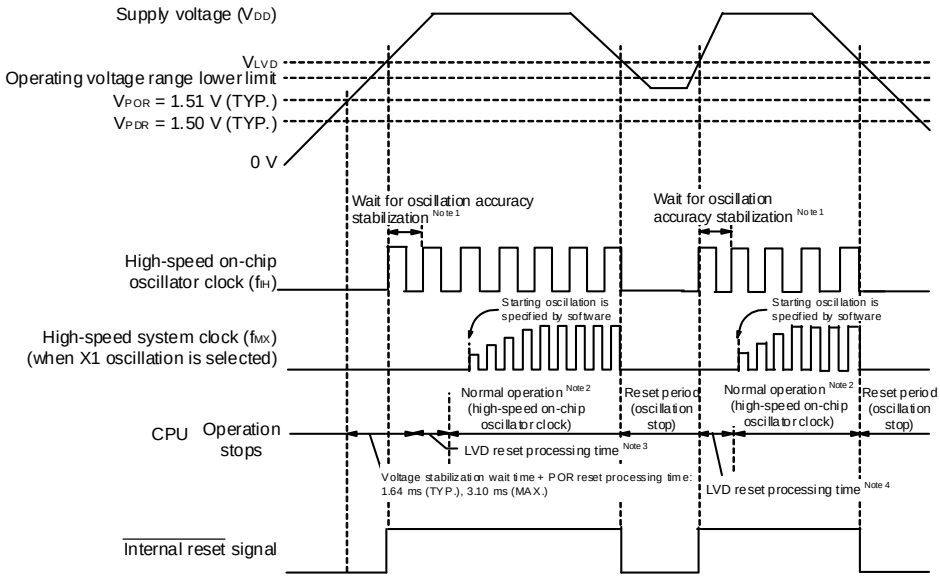
Note 3. After the interrupt request signal (INTLVI) is generated, the LVILV and LVIMD bits of the voltage detection level register (LVIS) are automatically set to 1. After INTLVI is generated, appropriate settings should be made according to **Figure 30 - 7 Processing Procedure After an Interrupt Is Generated** and **Figure 30 - 8 Initial Setting of Interrupt and Reset Mode**, taking into consideration that the supply voltage might return to the high voltage detection level (V_{LVDH}) or higher without falling below the low voltage detection level (V_{LVDL}).

Note 4. The time until normal operation starts includes the following LVD reset processing time after the LVD detection level (V_{LVDH}) is reached as well as the voltage stabilization wait + POR reset processing time after the V_{POR} (1.51 V, TYP.) is reached.
LVD reset processing time: 0 ms to 0.0701 ms (MAX.)

Remark V_{LVDH}, V_{LVDL}: LVD detection voltage
V_{POR}: POR power supply rise detection voltage
V_{PDR}: POR power supply fall detection voltage

Figure 29 - 4 Timing of Generation of Internal Reset Signal by Power-on-reset Circuit and Voltage Detector (3/3)

(3) LVD reset mode (option byte 000C1H: LVIMDS1, LVIMDS0 = 1, 1)



Note 1. The internal reset processing time includes the oscillation accuracy stabilization time of the high-speed on-chip oscillator clock.

Note 2. The high-speed on-chip oscillator clock and a high-speed system clock or subsystem clock can be selected as the CPU clock. To use the X1 clock, use the oscillation stabilization time counter status register (OSTC) to confirm the lapse of the oscillation stabilization time. To use the XT1 clock, use the timer function for confirmation of the lapse of the stabilization time.

Note 3. The time until normal operation starts includes the following LVD reset processing time after the LVD detection level (V_{LVD}) is reached as well as the voltage stabilization wait + POR reset processing time after the V_{POR} (1.51 V, TYP.) is reached.
LVD reset processing time: 0 ms to 0.0701 ms (MAX.)

Note 4. When the power supply voltage is below the lower limit for operation and the power supply voltage is then restored after an internal reset is generated only by the voltage detector (LVD), the following LVD reset processing time is required after the LVD detection level (V_{LVD}) is reached.
LVD reset processing time: 0.0511 ms (TYP.), 0.0701 ms (MAX.)

Remark 1. V_{LVDH}, V_{LVDL}: LVD detection voltage
V_{POR}: POR power supply rise detection voltage
V_{PDR}: POR power supply fall detection voltage

Remark 2. When the LVD interrupt mode is selected (option byte 000C1H: LVIMD1 = 0, LVIMD0 = 1), the time until normal operation starts after power is turned on is the same as the time specified in Note 3 of **Figure 29 - 4 (3)**.

CHAPTER 30 VOLTAGE DETECTOR

30.1 Functions of Voltage Detector

The operation mode and detection voltages (V_{LVDH}, V_{LVDL}, V_{LVD}) for the voltage detector is set by using the option byte (000C1H). The voltage detector (LVD) has the following functions.

- The LVD circuit compares the supply voltage (V_{DD}) with the detection voltage (V_{LVDH}, V_{LVDL}, V_{LVD}), and generates an internal reset or internal interrupt signal.
- The option byte can be used to select the detection levels for the power supply voltage (V_{LVDH}, V_{LVDL}) as one of 9 sets of levels[Note 1], and for the power supply voltage (V_{LVD}) as one of 12 sets of levels[Note 2]. (For details, see **CHAPTER 33 OPTION BYTE**.)
- Operable in STOP mode.
- After power is supplied, the reset state must be retained until the operating voltage becomes in the range defined in **38.4** or **39.4 AC Characteristics**. This is done by utilizing the voltage detection circuit or controlling the externally input reset signal. After the power supply is turned off, this LSI should be placed in the STOP mode, or placed in the reset state by utilizing the voltage detection circuit or controlling the externally input reset signal before the voltage falls below the operating range. The range of operating voltage varies with the setting of the user option byte (000C2H or 010C2H).

(a) Interrupt & reset mode (option byte LVIMDS1, LVIMDS0 = 1, 0)
The two detection voltages (V_{LVDH}, V_{LVDL}) are selected by the option byte 000C1H. The high-voltage detection level (V_{LVDH}) is used for releasing resets and generating interrupts. The low-voltage detection level (V_{LVDL}) is used for generating resets.

(b) Reset mode (option byte LVIMDS1, LVIMDS0 = 1, 1)
The detection voltage (V_{LVD}) selected by the option byte 000C1H is used for triggering and ending resets.

(c) Interrupt mode (option byte LVIMDS1, LVIMDS0 = 0, 1)
The detection voltage (V_{LVD}) selected by the option byte 000C1H is used for releasing resets/generating interrupts.

Note 1. This is the case for the R5F11R. Six sets of levels are selectable in the case of the R5F11N and R5F11P.

Note 2. This is the case for the R5F11R. Nine sets of levels are selectable in the case of the R5F11N and R5F11P.

The reset and internal interrupt signals are generated in each mode as follows.

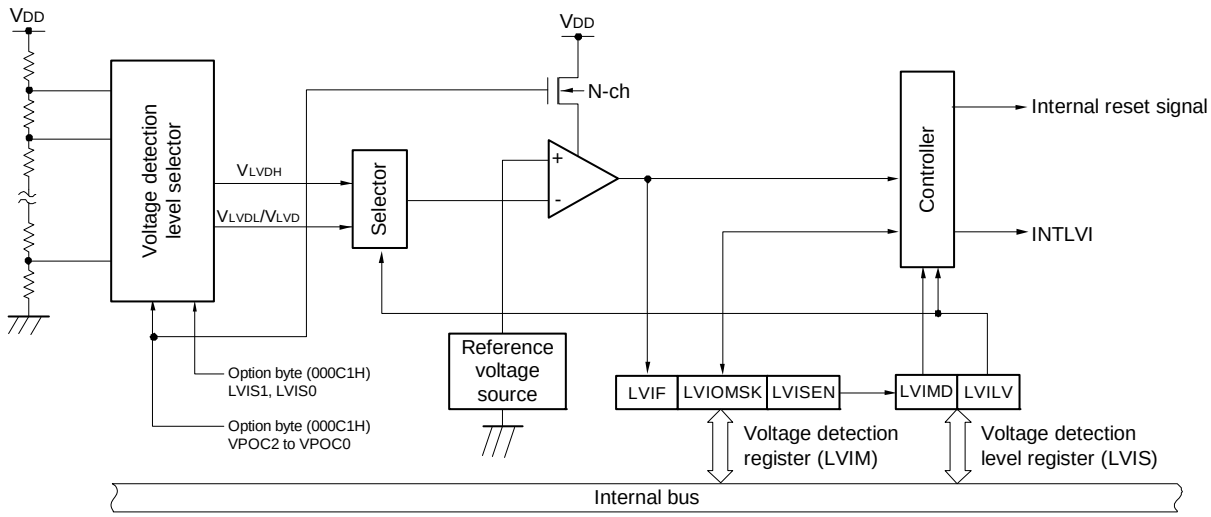
Interrupt & reset mode (LVIMDS1, LVIMDS0 = 1, 0)	Reset mode (LVIMDS1, LVIMDS0 = 1, 1)	Interrupt mode (LVIMDS1, LVIMDS0 = 0, 1)
Generates an interrupt request signal by detecting $V_{DD} < V_{LVDH}$ when the operating voltage falls, and an internal reset by detecting $V_{DD} < V_{LVDL}$. Releases an internal reset by detecting $V_{DD} \geq V_{LVDH}$.	Releases an internal reset by detecting $V_{DD} \geq V_{LVD}$. Generates an internal request signal by detecting $V_{DD} < V_{LVD}$.	Releases an internal reset by detecting $V_{DD} \geq V_{LVD}$ at power on after the first release of the POR. Generates an interrupt request signal by detecting $V_{DD} < V_{LVD}$ or $V_{DD} \geq V_{LVD}$ at power on after the second release of the POR.

While the voltage detector is operating, whether the supply voltage is more than or less than the detection level can be checked by reading the voltage detection flag (LVIF: bit 0 of the voltage detection register (LVIM)).
Bit 0 (LVIRF) of the reset control flag register (RESF) is set to 1 if reset occurs. For details of the RESF register, see **CHAPTER 28 RESET FUNCTION**.

30.2 Configuration of Voltage Detector

The block diagram of the voltage detector is shown in **Figure 30 - 1**.

Figure 30 - 1 Block Diagram of Voltage Detector



30.3 Registers Controlling Voltage Detector

The voltage detector is controlled by the following registers.

- Voltage detection register (LVIM)
- Voltage detection level register (LVIS)

30.3.1 Voltage detection register (LVIM)

This register is used to specify whether to enable or disable rewriting the voltage detection level register (LVIS), as well as to check the LVD output mask status.

This register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 30 - 2 Format of Voltage detection register (LVIM)

Address: FFFA9H After reset: 00H Note 1 R/W Note 2

Symbol	<7>	6	5	4	3	2	<1>	<0>
LVIM	LVISEN Note 3	0	0	0	0	0	LVIOMSK	LVIF

LVISEN Note 3	Specification of whether to enable or disable rewriting the voltage detection level register (LVIS)
0	Disabling of rewriting the LVIS register (LVIOMSK = 0 (Mask of LVD output is invalid))
1	Enabling of rewriting the LVIS register (LVIOMSK = 1 (Mask of LVD output is valid))

LVIOMSK	Mask status flag of LVD output
0	Mask of LVD output is invalid
1	Mask of LVD output is valid Note 4

LVIF	Voltage detection flag
0	Supply voltage (V_{DD}) ≥ detection voltage (V_{LVD}), or when LVD is off
1	Supply voltage (V_{DD}) < detection voltage (V_{LVD})

Note 1. The reset value changes depending on the reset source.
If the LVIS register is reset by LVD, it is not reset but holds the current value. The value of this register is reset to “00H” if a reset other than by LVD is effected.

Note 2. Bits 0 and 1 are read-only.

Note 3. Can only be set in the interrupt & reset mode (option byte LVIMDS1, LVIMDS0 = 1, 0). Do not change the initial value in other modes.

Note 4. LVIOMSK bit is only automatically set to “1” when the interrupt & reset mode is selected (option byte LVIMDS1, LVIMDS0 = 1, 0) and reset or interrupt by LVD is masked.
- Period during LVISEN = 1
- Waiting period from the time when LVD interrupt is generated until LVD detection voltage becomes stable
- Waiting period from the time when the value of LVILV bit changes until LVD detection voltage becomes stable

30.3.2 Voltage detection level register (LVIS)

This register selects the voltage detection level.

This register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation input sets this register to 00H/01H/81H Note 1.

Figure 30 - 3 Format of Voltage detection level register (LVIS)

Address: FFFAAH After reset:00H/01H/81H Note 1 R/W

Symbol	<7>	6	5	4	3	2	1	<0>
LVIS	LVIMD Note 2	0	0	0	0	0	0	LVILV Note 2

LVIMD Note 2	Operation mode of voltage detection
0	Interrupt mode
1	Reset mode

LVILV Note 2	LVD detection level
0	High-voltage detection level (V_{LVDH})
1	Low-voltage detection level (V_{LVDL} or V_{LVD})

Note 1. The reset value changes depending on the reset source and the setting of the option byte.
This register is not cleared (00H) by LVD reset.
The generation of reset signal other than an LVD reset sets as follows.
- When option byte LVIMDS1, LVIMDS0 = 1, 0: 00H
- When option byte LVIMDS1, LVIMDS0 = 1, 1: 81H
- When option byte LVIMDS1, LVIMDS0 = 0, 1: 01H

Note 2. Writing “0” can only be allowed in the interrupt & reset mode (option byte LVIMDS1, LVIMDS0 = 1, 0). Do not set LVIMD and LVILV in other cases. The value is switched automatically when reset or interrupt is generated in the interrupt & reset mode.

Caution 1. Rewrite the value of the LVIS register according to Figures 30 - 6 and 30 - 7.

Caution 2. Specify the LVD operation mode and detection voltage (V_{LVDH}, V_{LVDL}, V_{LVD}) of each mode by using the option byte 000C1H. Table 30 - 1 shows the format of the user option byte (000C1H/010C1H). For details about the option byte, see CHAPTER 33 OPTION BYTE.

Table 30 - 1 Format of User Option Byte (000C1H/010C1H) (1/2)

Address: 000C1H/010C1H Note 1

7	6	5	4	3	2	1	0
VPOC2	VPOC1	VPOC0	1	LVIS1	LVIS0	LVIMDS1	LVIMDS0

• LVD setting (interrupt & reset mode)

Detection voltage			Option byte Setting Value						
V_{LVDH}		V_{LVDL}	VPOC2	VPOC1	VPOC0	LVIS1	LVIS0	Mode setting	
Rising edge	Falling edge	Falling edge						LVIMDS1	LVIMDS0
1.98 V Note 2	1.94 V Note 2	1.84 V Note 2	0	0	1	1	0	1	0
2.09 V Note 2	2.04 V Note 2					0	1		
3.13 V Note 2	3.06 V Note 2					0	0		
2.61 V	2.55 V	2.45 V		1	0	1	0		
2.71 V	2.65 V					0	1		
3.75 V	3.67 V					0	0		
2.92 V	2.86 V	2.75 V		1	1	1	0		
3.02 V	2.96 V					0	1		
4.06 V	3.98 V					0	0		
—			Setting of values other than above is prohibited						

• LVD setting (reset mode)

Detection voltage		Option byte Setting Value						
V_{LVD}		VPOC2	VPOC1	VPOC0	LVIS1	LVIS0	Mode setting	
Rising edge	Falling edge						LVIMDS1	LVIMDS0
1.88 V Note 2	1.84 V Note 2	0	0	1	1	1	1	1
1.98 V Note 2	1.94 V Note 2		0	1	1	0		
2.09 V Note 2	2.04 V Note 2		0	1	0	1		
2.50 V	2.45 V		1	0	1	1		
2.61 V	2.55 V		1	0	1	0		
2.71 V	2.65 V		1	0	0	1		
2.81 V	2.75 V		1	1	1	1		
2.92 V	2.86 V		1	1	1	0		
3.02 V	2.96 V		1	1	0	1		
3.13 V	3.06 V		0	1	0	0		
3.75 V	3.67 V		1	0	0	0		
4.06 V	3.98 V		1	1	0	0		
—		Setting of values other than above is prohibited						

Note 1. Set the same value as 000C1H to 010C1H when the boot swap operation is used because 000C1H is replaced by 010C1H.

Note 2. R5F11R only. Setting is prohibited for R5F11N and R5F11P.

Remark The detection voltage is a TYP. value. For details, see **38.6.4** or **39.6.4 LVD circuit characteristics**.

(**Cautions** are listed on the next page.)

Table 30 - 1 Format of User Option Byte (000C1H/010C1H) (2/2)

Address: 000C1H/010C1H Note 1

7	6	5	4	3	2	1	0
VPOC2	VPOC1	VPOC0	1	LVIS1	LVIS0	LVIMDS1	LVIMDS0

• LVD setting (interrupt mode)

Detection voltage		Option byte Setting Value						
V_{LVD}		VPOC2	VPOC1	VPOC0	LVIS1	LVIS0	Mode setting	
Rising edge	Falling edge						LVIMDS1	LVIMDS0
1.88 V Note 2	1.84 V Note 2	0	0	1	1	1	0	1
1.98 V Note 2	1.94 V Note 2		0	1	1	0		
2.09 V Note 2	2.04 V Note 2		0	1	0	1		
2.50 V	2.45 V		1	0	1	1		
2.61 V	2.55 V		1	0	1	0		
2.71 V	2.65 V		1	0	0	1		
2.81 V	2.75 V		1	1	1	1		
2.92 V	2.86 V		1	1	1	0		
3.02 V	2.96 V		1	1	0	1		
3.13 V	3.06 V		0	1	0	0		
3.75 V	3.67 V		1	0	0	0		
4.06 V	3.98 V		1	1	0	0		
—		Setting of values other than above is prohibited						

• LVD off (use of external reset input via $\overline{\text{RESET}}$ pin)

Detection voltage		Option byte Setting Value						
V_{LVD}		VPOC2	VPOC1	VPOC0	LVIS1	LVIS0	Mode setting	
Rising edge	Falling edge						LVIMDS1	LVIMDS0
—	—	1	×	×	×	×	×	1
—		Setting of values other than above is prohibited						

Note 1. Set the same value as 000C1H to 010C1H when the boot swap operation is used because 000C1H is replaced by 010C1H.

Note 2. R5F11R only. Setting is prohibited for R5F11N and R5F11P.

Caution 1. Set bit 4 to 1.

Caution 2. After power is supplied, the reset state must be retained until the operating voltage becomes in the range defined in 38.4 or 39.4 AC Characteristics. This is done by utilizing the voltage detection circuit or controlling the externally input reset signal. After the power supply is turned off, this LSI should be placed in the STOP mode, or placed in the reset state by utilizing the voltage detection circuit or controlling the externally input reset signal, before the voltage falls below the operating range. The range of operating voltage varies with the setting of the user option byte (000C2H or 010C2H).

Remark 1. ×: don't care

Remark 2. The detection voltage is a TYP. value. For details, see **38.6.4** or **39.6.4 LVD circuit characteristics**.

30.4 Operation of Voltage Detector

30.4.1 When used as reset mode

Specify the operation mode (the reset mode (LVIMDS1, LVIMDS0 = 1, 1)) and the detection voltage (V_{LVD}) by using the option byte 000C1H.

The operation is started in the following initial setting state when the reset mode is set.

- Bit 7 (LVISEN) of the voltage detection register (LVIM) is set to 0 (disable rewriting of voltage detection level register (LVIS))
- The initial value of the voltage detection level select register (LVIS) is set to 81H.
  Bit 7 (LVIMD) is 1 (reset mode).
  Bit 0 (LVILV) is 1 (low-voltage detection level: V_{LVD}).

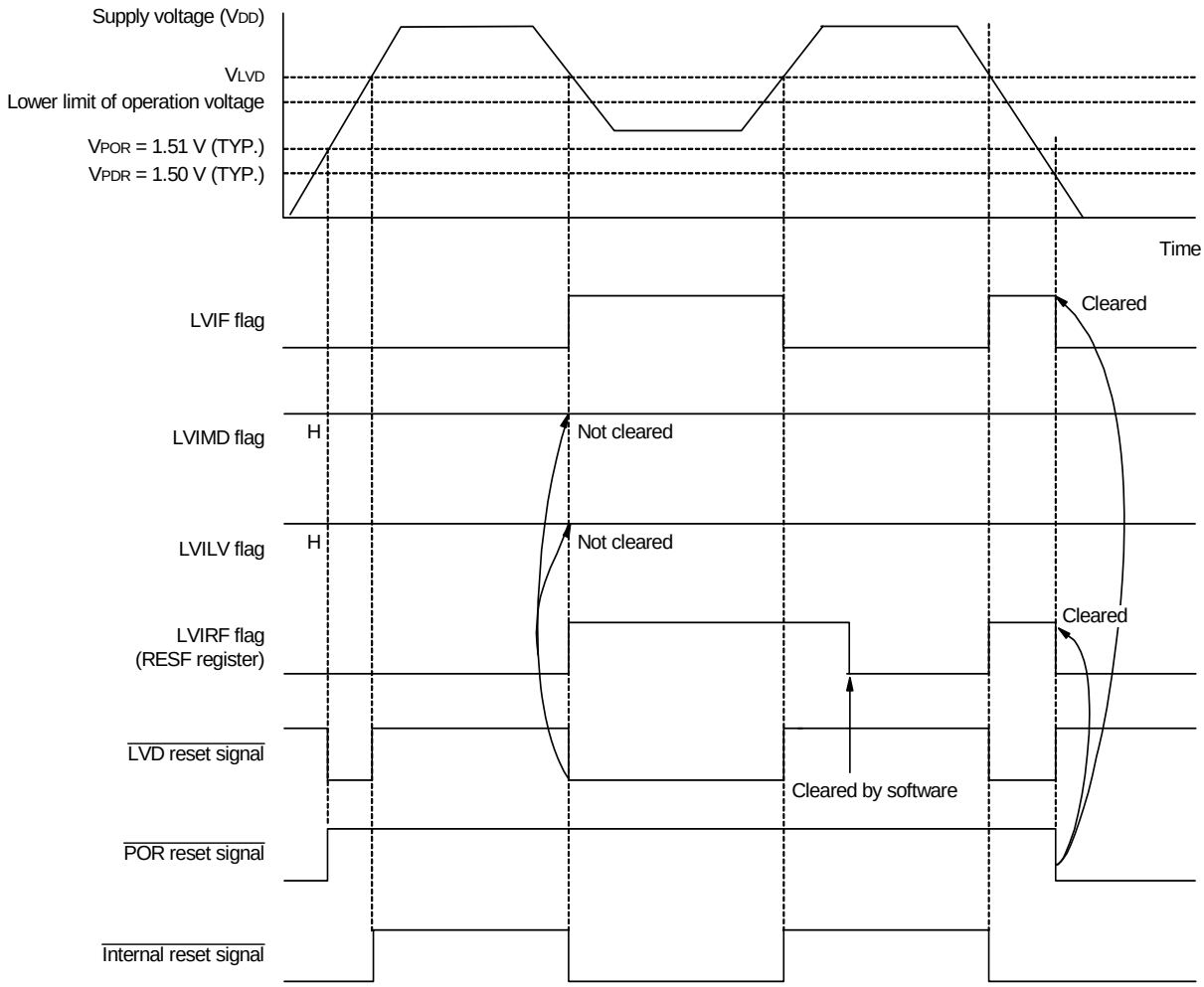
• Operation in LVD reset mode

In the reset mode (option byte LVIMDS1, LVIMDS0 = 1, 1), the state of an internal reset by LVD is retained until the supply voltage (V_{DD}) exceeds the voltage detection level (V_{LVD}) after power is supplied. The internal reset is released when the supply voltage (V_{DD}) exceeds the voltage detection level (V_{LVD}).

At the fall of the operating voltage, an internal reset by LVD is generated when the supply voltage (V_{DD}) falls below the voltage detection level (V_{LVD}).

Figure 30 - 4 shows the timing of the internal reset signal generated in the LVD reset mode.

Figure 30 - 4 Timing of Voltage Detector Internal Reset Signal Generation (Option Byte LVIMDS1, LVIMDS0 = 1, 1)



Remark VPOR: POR power supply rise detection voltage
VPDR: POR power supply fall detection voltage

30.4.2 When used as interrupt mode

Specify the operation mode (the interrupt mode (LVIMDS1, LVIMDS0 = 0, 1)) and the detection voltage (V_{LVD}) by using the option byte 000C1H.

The operation is started in the following initial setting state when the interrupt mode is set.

- Bit 7 (LVISEN) of the voltage detection register (LVIM) is set to 0 (disable rewriting of voltage detection level register (LVIS))
- The initial value of the voltage detection level select register (LVIS) is set to 01H.
  Bit 7 (LVIMD) is 0 (interrupt mode).
  Bit 0 (LVILV) is 1 (low-voltage detection level: V_{LVD}).

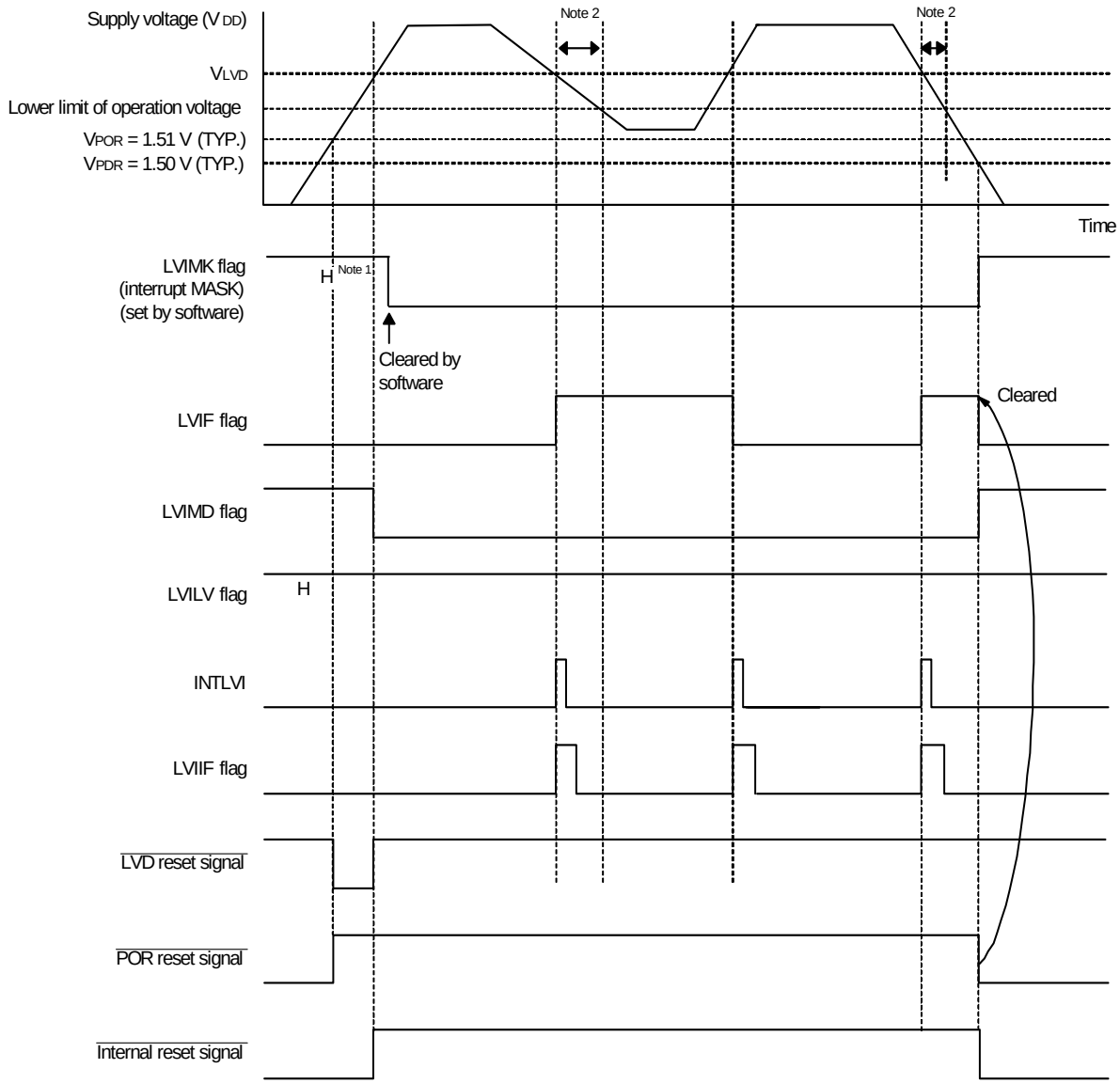
• Operation in LVD interrupt mode

In the interrupt mode (option byte LVIMDS1, LVIMDS0 = 0, 1), the state of an internal reset by LVD is retained until the supply voltage (V_{DD}) exceeds the voltage detection level (V_{LVD}) after power is supplied (after the first release of the POR). The internal reset is released when the supply voltage (V_{DD}) exceeds the voltage detection level (V_{LVD}).

An interrupt request signal by LVD (INTLVI) is generated, when the supply voltage (V_{DD}) falls below the voltage detection level (V_{LVD}) or when the supply voltage (V_{DD}) exceeds the voltage detection level (V_{LVD}) after the second release of the POR. When the voltage falls, this LSI should be placed in the STOP mode, or placed in the reset state by controlling the externally input reset signal, before the voltage falls below the operating voltage range defined in **38.4** or **39.4 AC Characteristics**. When restarting the operation, make sure that the operation voltage has returned within the range of operation.

Figure 30 - 5 shows the timing of the interrupt request signal generated in the LVD interrupt mode.

Figure 30 - 5 Timing of Voltage Detector Internal Interrupt Signal Generation (Option Byte LVIMDS1, LVIMDS0 = 0, 1)



Note 1. The LVIMK flag is set to “1” by reset signal generation.

Note 2. When the voltage falls, this LSI should be placed in the STOP mode, or placed in the reset state by controlling the externally input reset signal, before the voltage falls below the operating voltage range defined in **38.4** or **39.4 AC Characteristics**. When restarting the operation, make sure that the operation voltage has returned within the range of operation.

Remark VPOR: POR power supply rise detection voltage
VPDR: POR power supply fall detection voltage

30.4.3 When used as interrupt and reset mode

Specify the operation mode (the interrupt & reset (LVIMDS1, LVIMDS0 = 1, 0)) and the detection voltage (V_{LVDH}, V_{LVDL}) by using the option byte 000C1H.

The operation is started in the following initial setting state when the interrupt & reset mode is set.

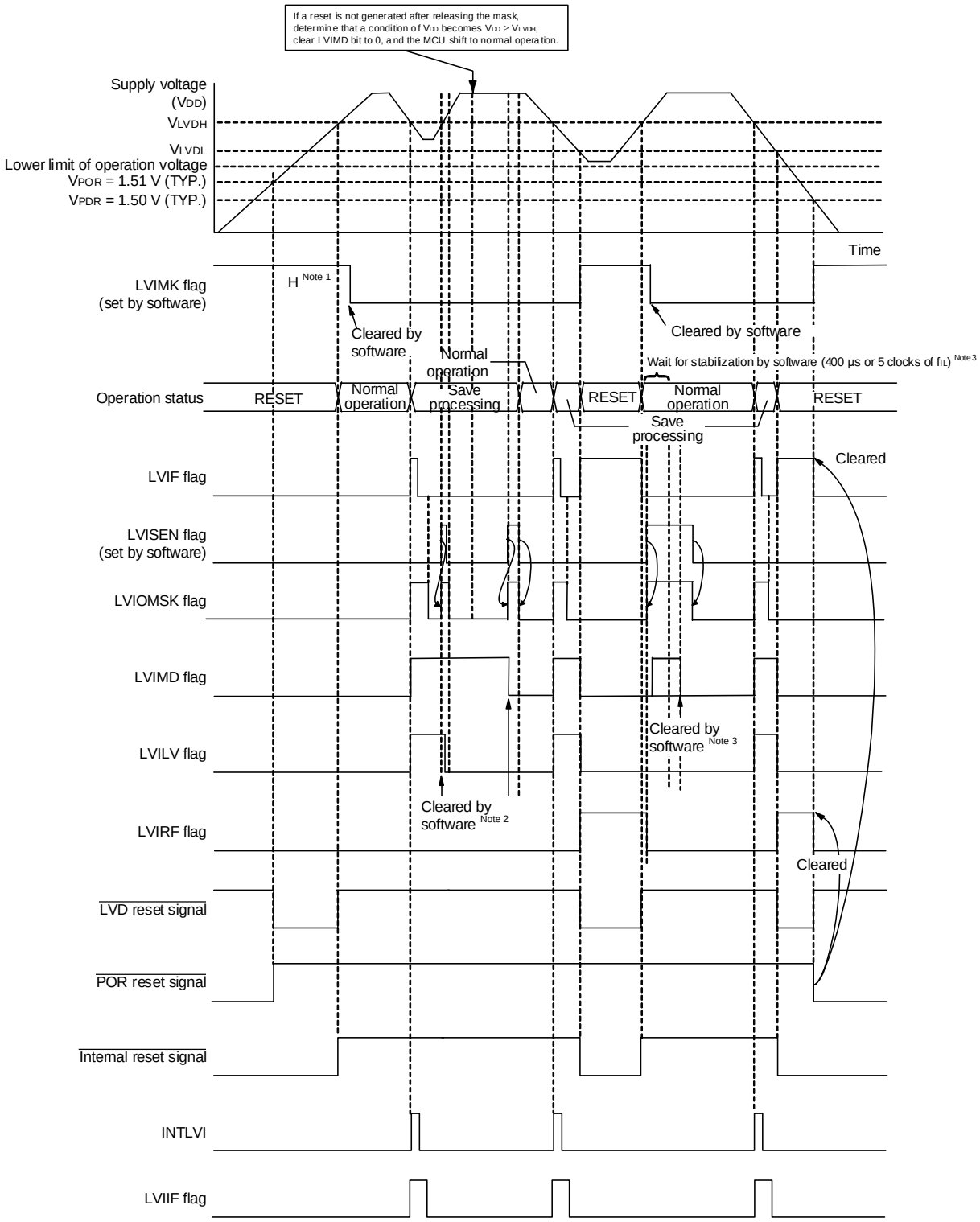
- Bit 7 (LVISEN) of the voltage detection register (LVIM) is set to 0 (disable rewriting of voltage detection level register (LVIS))
- The initial value of the voltage detection level select register (LVIS) is set to 00H.
  Bit 7 (LVIMD) is 0 (interrupt mode).
  Bit 0 (LVILV) is 0 (high-voltage detection level: V_{LVDH}).

• Operation in LVD interrupt & reset mode

In the interrupt & reset mode (option byte LVIMDS1, LVIMDS0 = 1, 0), the state of an internal reset by LVD is retained until the supply voltage (V_{DD}) exceeds the high-voltage detection level (V_{LVDH}) after power is supplied. The internal reset is released when the supply voltage (V_{DD}) exceeds the high-voltage detection level (V_{LVDH}). An interrupt request signal by LVD (INTLVI) is generated and arbitrary save processing is performed when the supply voltage (V_{DD}) falls below the high-voltage detection level (V_{LVDH}). After that, an internal reset by LVD is generated when the supply voltage (V_{DD}) falls below the low-voltage detection level (V_{LVDL}). After INTLVI is generated, an interrupt request signal is not generated even if the supply voltage becomes equal to or higher than the high-voltage detection voltage (V_{LVDH}) without falling below the low-voltage detection voltage (V_{LVDL}). To use the LVD reset & interrupt mode, perform the processing according to **Figure 30 - 7 Processing Procedure After an Interrupt Is Generated** and **Figure 30 - 8 Initial Setting of Interrupt and Reset Mode**.

Figure 30 - 6 show the timing of the internal reset signal and interrupt signal generated in the LVD interrupt & reset mode.

Figure 30 - 6 Timing of Voltage Detector Reset Signal and Interrupt Signal Generation (Option Byte LVIMDS1, LVIMDS0 = 1, 0) (1/2)



(**Notes** and **Remark** are listed on the next page.)

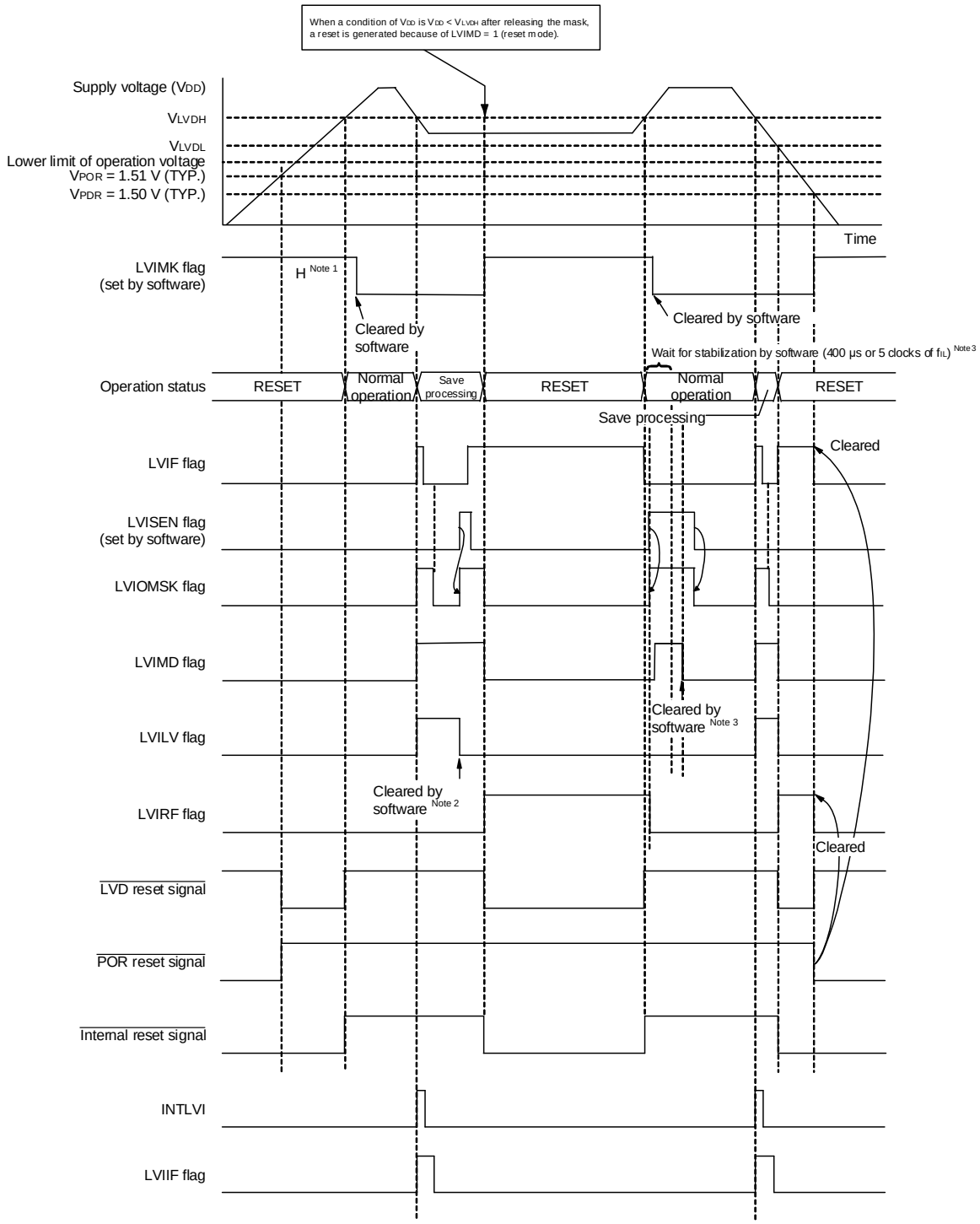
Note 1. The LVIMK flag is set to “1” by reset signal generation.

Note 2. After an interrupt is generated, perform the processing according to **Figure 30 - 7** in interrupt and reset mode.

Note 3. After a reset is released, perform the processing according to **Figure 30 - 8 Initial Setting of Interrupt and Reset Mode** in interrupt and reset mode.

Remark V_{POR}: POR power supply rise detection voltage
V_{POR}: POR power supply fall detection voltage

Figure 30 - 6 Timing of Voltage Detector Reset Signal and Interrupt Signal Generation (Option Byte LVIMDS1, LVIMDS0 = 1, 0) (2/2)



(**Notes** and **Remark** are listed on the next page.)

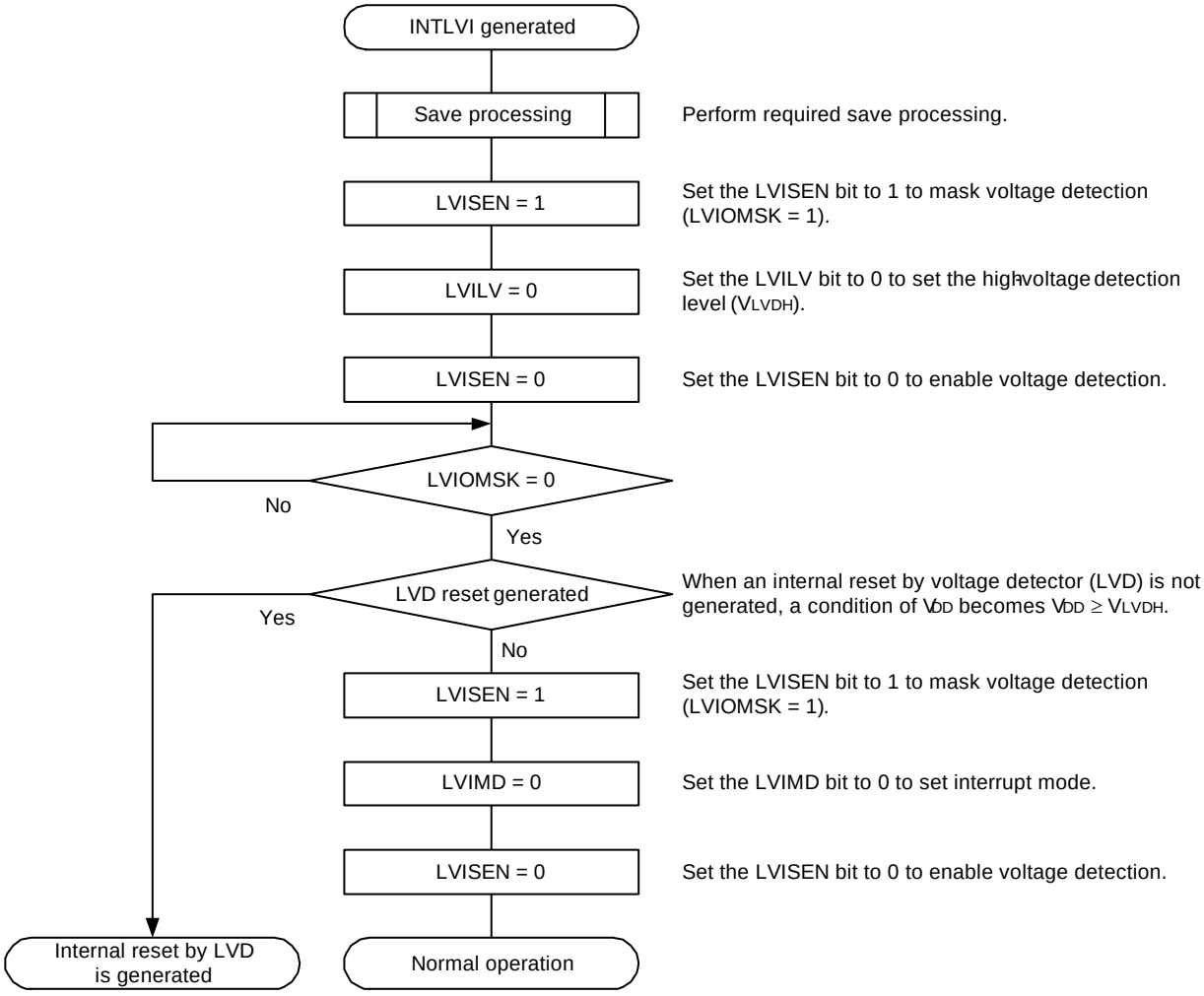
Note 1. The LVIMK flag is set to “1” by reset signal generation.

Note 2. After an interrupt is generated, perform the processing according to **Figure 30 - 7 Processing Procedure After an Interrupt Is Generated** in interrupt and reset mode.

Note 3. After a reset is released, perform the processing according to Figure 30 - 8 Initial Setting of Interrupt and Reset Mode in interrupt and reset mode.

Remark V_{POR}: POR power supply rise detection voltage
V_{PDR}: POR power supply fall detection voltage

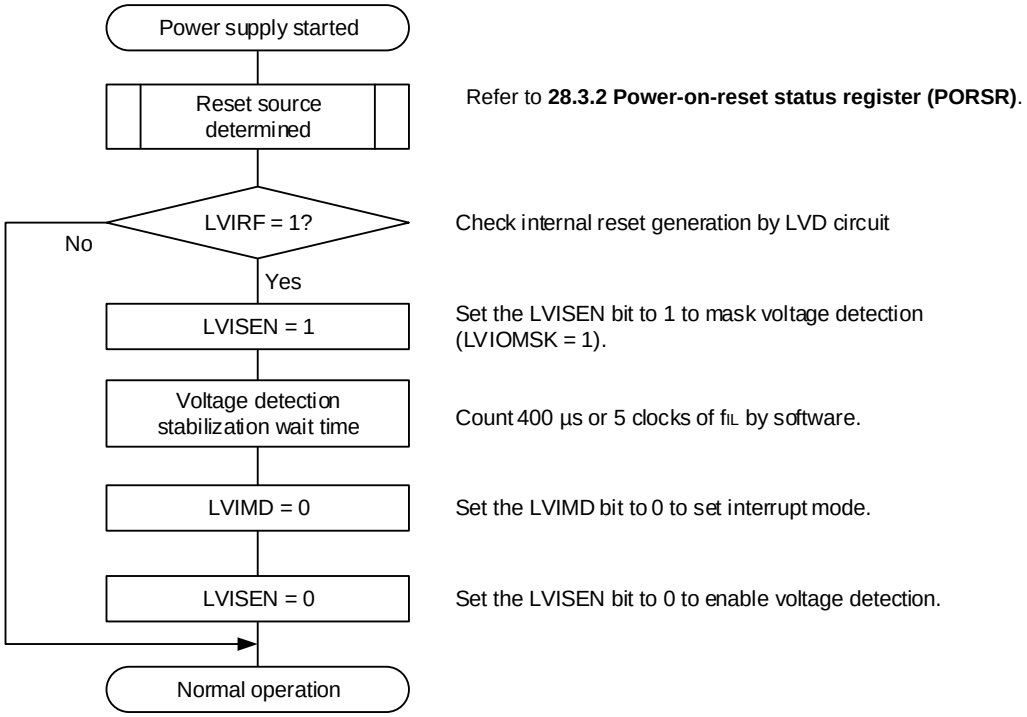
Figure 30 - 7 Processing Procedure After an Interrupt Is Generated



When setting an interrupt and reset mode (LVIMDS1, LVIMDS0 = 1, 0), voltage detection stabilization wait time for 400 µs or 5 clocks of f_{IL} is necessary after LVD reset is released (LVIRF = 1). After waiting until voltage detection stabilizes, (0) clear the LVIMD bit for initialization. While voltage detection stabilization wait time is being counted and when the LVIMD bit is rewritten, set LVISEN to 1 to mask a reset or interrupt generation by LVD.

Figure 30 - 8 shows the procedure for Initial Setting of Interrupt and Reset Mode.

Figure 30 - 8 Initial Setting of Interrupt and Reset Mode



Remark f_{IL}: Low-speed on-chip oscillator clock frequency

30.5 Cautions for Voltage Detector

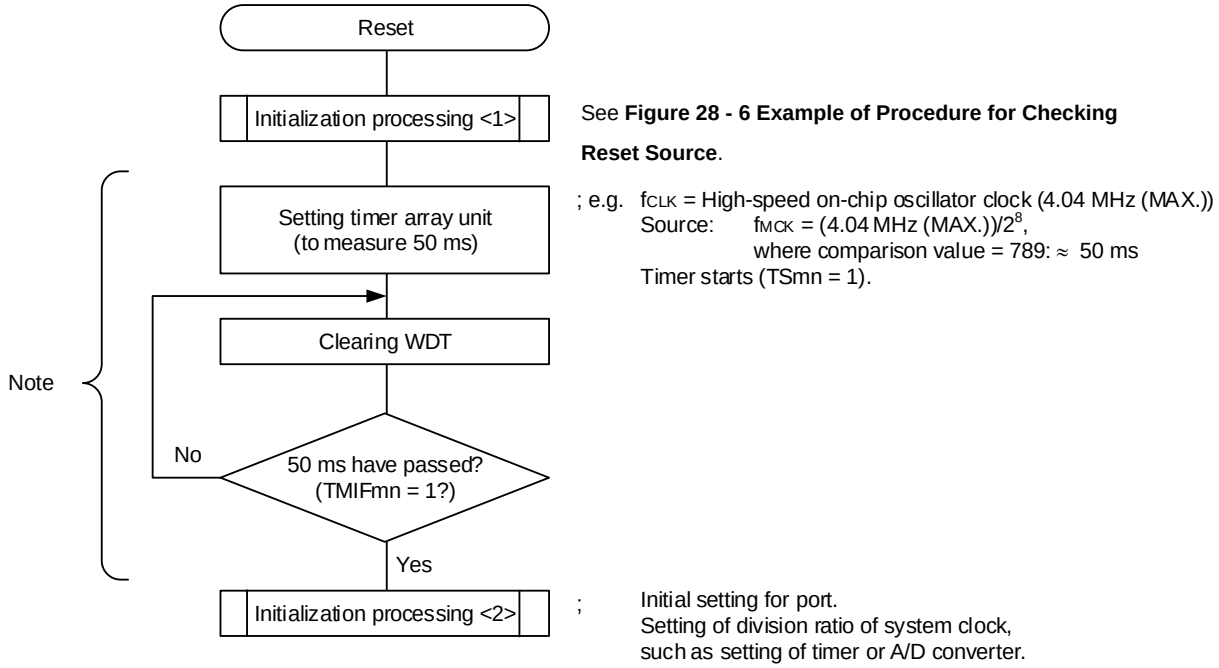
(1) Voltage fluctuation when power is supplied

In a system where the supply voltage (V_{DD}) fluctuates for a certain period in the vicinity of the LVD detection voltage, the system may be repeatedly reset and released from the reset status. In this case, the time from release of reset to the start of the operation of the microcontroller can be arbitrarily set by taking the following action.

<Action>

After releasing the reset signal, wait for the supply voltage fluctuation period of each system by means of a software counter that uses a timer, and then initialize the ports.

Figure 30 - 9 Example of Software Processing If Supply Voltage Fluctuation is 50 ms or Less in Vicinity of LVD Detection Voltage



Note If reset is generated again during this period, initialization processing <2> is not started.

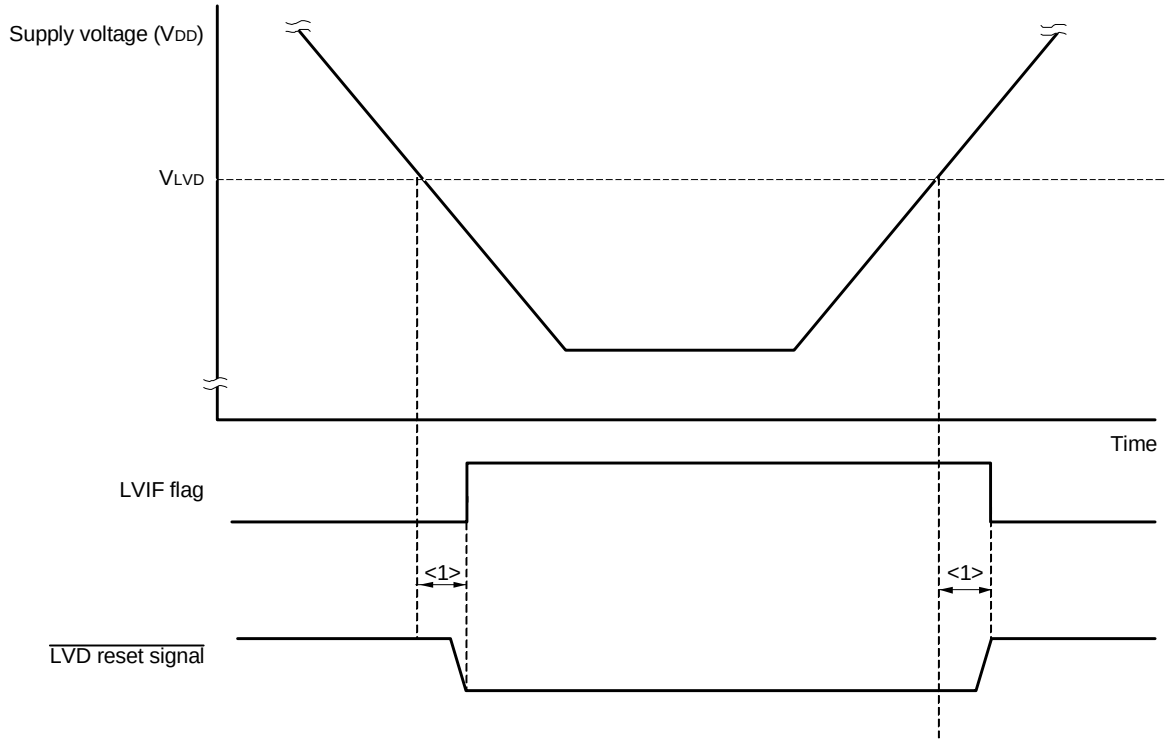
Remark m = 0, n = 0 to 7

(2) Delay from the time LVD reset source is generated until the time LVD reset has been generated or released

There is some delay from the time supply voltage (V_{DD}) < LVD detection voltage (V_{LVD}) until the time LVD reset has been generated.

In the same way, there is also some delay from the time LVD detection voltage (V_{LVD}) ≤ supply voltage (V_{DD}) until the time LVD reset has been released (see **Figure 30 - 10**).

Figure 30 - 10 Delay from the time LVD reset source is generated until the time LVD reset has been generated or released



<1>: Detection delay (300 μs (MAX.))

(3) Power on when LVD is off

Use the external rest input via the $\overline{\text{RESET}}$ pin when the LVD is off.

For an external reset, input a low level for 10 μs or more to the $\overline{\text{RESET}}$ pin. To perform an external reset upon power application, input a low level to the $\overline{\text{RESET}}$ pin, turn power on, continue to input a low level to the pin for 10 μs or more within the operating voltage range shown in **38.4** or **39.4 AC Characteristics**, and then input a high level to the pin.

(4) Operating voltage fall when LVD is off or LVD interrupt mode is selected

When the operating voltage falls with the LVD is off or with the LVD interrupt mode is selected, this LSI should be placed in the STOP mode, or placed in the reset state by controlling the externally input reset signal, before the voltage falls below the operating voltage range defined in **38.4** or **39.4 AC Characteristics**. When restarting the operation, make sure that the operation voltage has returned within the range of operation.

CHAPTER 31 SAFETY FUNCTIONS

31.1 Overview of Safety Functions

<R> The following safety functions are provided in the RL78/H1D to comply with the IEC60730 safety standard. These functions enable the microcontroller to self-diagnose abnormalities and stop operating if an abnormality is detected.

(1) Flash memory CRC operation function (high-speed CRC, general-purpose CRC)
This detects data errors in the flash memory by performing CRC operations.
Two CRC functions are provided in the RL78/H1D that can be used according to the application or purpose of use.
- High-speed CRC: The CPU can be stopped and a high-speed check executed on its entire code flash memory area during the initialization routine.
- General CRC: This can be used for checking various data in addition to the code flash memory area while the CPU is running.

(2) RAM parity error detection function
This detects parity errors when the RAM is read as data.

(3) RAM guard function
This prevents RAM data from being rewritten when the CPU freezes.

(4) SFR guard function
This prevents SFRs from being rewritten when the CPU freezes.

(5) Invalid memory access detection function
This detects illegal accesses to invalid memory areas (such as areas where no memory is allocated and areas to which access is restricted).

(6) Frequency detection function
This function allows a self-check of the CPU/peripheral hardware clock frequencies using the timer array unit.

(7) A/D test function
This is used to perform a self-check of A/D converter by performing A/D conversion on the positive reference voltage, negative reference voltage, analog input channel (ANI), temperature sensor output, and internal reference voltage.

(8) Digital output signal level detection function for I/O ports
When the I/O ports are output mode in which PMm bit of the port mode register (PMm) is 0, the output level of the pin can be read.

Remark 1. m = 0 to 8, 12, 15; n = 0 to 7

Remark 2. For usage examples of the safety functions complying with the IEC60730 safety standards, refer to the RL78 MCU series IEC60730/60335 application notes (R01AN1062, R01AN1296).

31.2 Registers Used by Safety Functions

The safety functions use the following registers:

Register	Each Function of Safety Function
• Flash memory CRC control register (CRC0CTL) • Flash memory CRC operation result register (PGCRCL)	Flash memory CRC operation function (high-speed CRC)
• CRC input register (CRCIN) • CRC data register (CRCD)	CRC operation function (general-purpose CRC)
• RAM parity error control register (RPECTL)	RAM parity error detection function
• Invalid memory access detection control register (IAWCTL)	RAM guard function
	SFR guard function
	Invalid memory access detection function
• Timer input select register 0 (TIS0)	Frequency detection function
• A/D test register (ADTES)	A/D test function
• Port mode select register (PMS)	Digital output signal level detection function for I/O ports

The content of each register is described in **31.3 Operation of Safety Functions**.

31.3 Operation of Safety Functions

31.3.1 Flash memory CRC operation function (high-speed CRC)

The IEC60730 standard mandates the checking of data in the flash memory, and recommends using CRC to do it. The high-speed CRC provided in the RL78/H1D can be used to check the entire code flash memory area during the initialization routine. The high-speed CRC can be executed only when the program is allocated on the RAM and in the HALT mode of the main system clock.

The high-speed CRC performs an operation by reading 32-bit data per clock from the flash memory while stopping the CPU. This function therefore can finish a check in a shorter time (for example, 341 µs@24 MHz with 32 KB flash memory).

The CRC generator polynomial used complies with “$X^{16} + X^{12} + X^5 + 1$” of CRC-16-CCITT.
The high-speed CRC operates in MSB first order from bit 31 to bit 0.

Caution The CRC operation result might differ during on-chip debugging because the monitor program is allocated.

Remark The operation result is different between the high-speed CRC and the general CRC, because the general CRC operates in LSB first order.

31.3.1.1 Flash memory CRC control register (CRC0CTL)

This register is used to control the operation of the high-speed CRC ALU, as well as to specify the operation range.

The CRC0CTL register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 31 - 1 Format of Flash memory CRC control register (CRC0CTL)

Address: F02F0H After reset:00H R/W

Symbol	<7>	6	5	4	3	2	1	0
CRC0CTL	CRC0EN	0	0	0	0	FEA2	FEA1	FEA0

CRC0EN	Control of high-speed CRC ALU operation
0	Stop the operation.
1	Start the operation according to HALT instruction execution.

FEA2	FEA1	FEA0	High-speed CRC operation range
0	0	0	00000H to 03FFBH (16 K - 4 bytes)
0	0	1	00000H to 07FFBH (32 K - 4 bytes)
0	1	0	00000H to 0BFFBH (48 K - 4 bytes)
0	1	1	00000H to 0FFFBH (64 K - 4 bytes)
1	0	0	00000H to 13FFBH (80 K - 4 bytes) Note 1
1	0	1	00000H to 17FFBH (96 K - 4 bytes) Note 1
1	1	0	00000H to 1BFFBH (112 K - 4 bytes) Note 2
1	1	1	00000H to 1FFFBH (128 K - 4 bytes) Note 2
Other than the above			Setting prohibited

Note 1. R5F11RMG, R5F11xG (x = NG, NL, NM, PL), and R5F11xF (x = NG, NL, NM, PL) only.

Note 2. R5F11RMG and R5F11xG (x = NG, NL, NM, PL) only.

Remark Input the expected CRC operation result value to be used for comparison in the lowest 4 bytes of the flash memory. Note that the operation range will thereby be reduced by 4 bytes.

31.3.1.2 Flash memory CRC operation result register (PGCRCL)

This register is used to store the high-speed CRC operation results.

The PGCRCL register can be set by a 16-bit memory manipulation instruction.

Reset signal generation clears this register to 0000H.

Figure 31 - 2 Format of Flash memory CRC operation result register (PGCRCL)

Address: F02F2H After reset: 0000H R/W

Symbol	15	14	13	12	11	10	9	8
PGCRCL	PGCRC15	PGCRC14	PGCRC13	PGCRC12	PGCRC11	PGCRC10	PGCRC9	PGCRC8

7	6	5	4	3	2	1	0
PGCRC7	PGCRC6	PGCRC5	PGCRC4	PGCRC3	PGCRC2	PGCRC1	PGCRC0

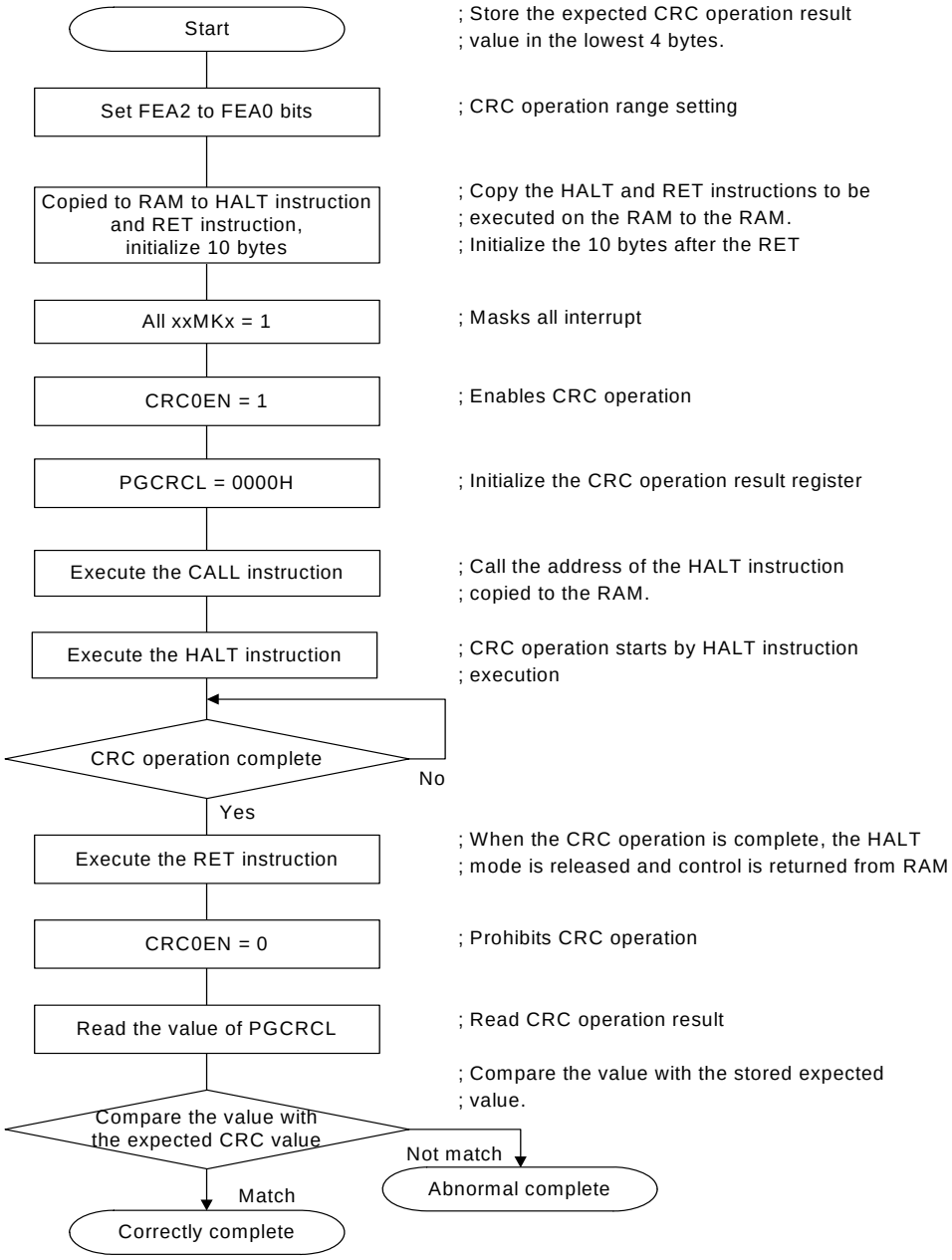
PGCRC15 to 0	High-speed CRC operation results
0000H to FFFFH	Store the high-speed CRC operation results.

Caution The PGCRCL register can only be written if CRC0EN (bit 7 of the CRC0CTL register) = 1.

Figure 31 - 3 shows the Flowchart of Flash Memory CRC Operation Function (High-speed CRC).

<Operation flow>

Figure 31 - 3 Flowchart of Flash Memory CRC Operation Function (High-speed CRC)



Caution 1. The CRC operation is executed only on the code flash.
Caution 2. Store the expected CRC operation value in the area below the operation range in the code flash.
Caution 3. The CRC operation is enabled by executing the HALT instruction in the RAM area.
Be sure to execute the HALT instruction in RAM area.

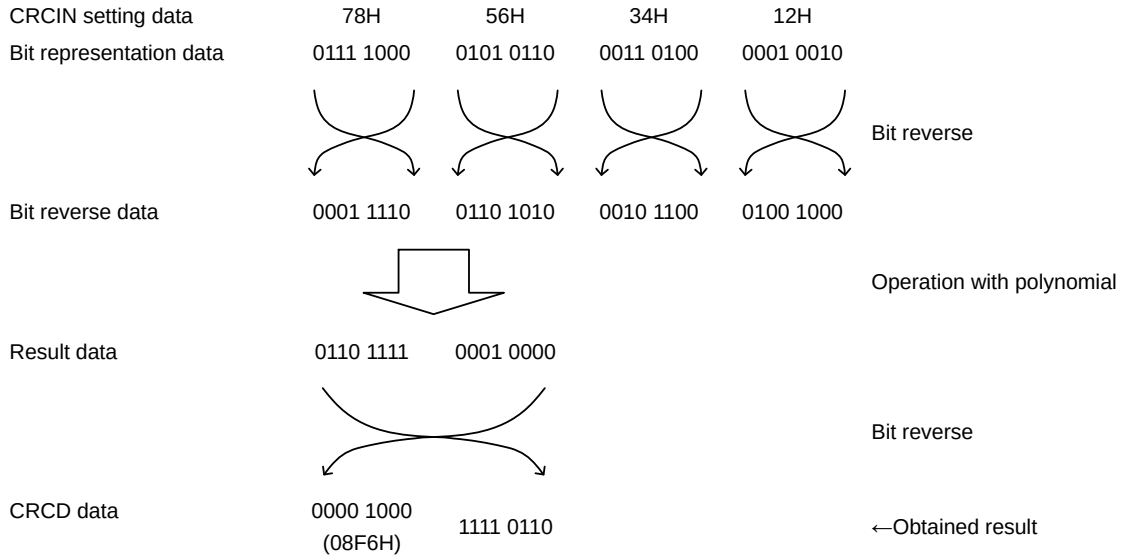
The expected CRC value can be calculated by using the Integrated Development Environment CubeSuite+. See **Integrated Development Environment CubeSuite+ user's manual** for details.

31.3.2 CRC operation function (general-purpose CRC)

<R> In the RL78/H1D, a general CRC operation can be executed as a peripheral function while the CPU is operating. The general CRC can be used for checking various data in addition to the code flash memory area. The data to be checked can be specified by using software (a user-created program). CRC calculation function in the HALT mode can be used only during the DTC transmission.

The general CRC operation can be executed in the main system clock operation mode as well as the subsystem clock operation mode.

The CRC generator polynomial used is "$X^{16} + X^{12} + X^5 + 1$" of CRC-16-CCITT. The data to be input is inverted in bit order and then calculated to allow for LSB-first communication. For example, if the data 12345678H is sent from the LSB, values are written to the CRCIN register in the order of 78H, 56H, 34H, and 12H, enabling a value of 08F6H to be obtained from the CRCD register. This is the result obtained by executing a CRC operation on the bit rows shown below, which consist of the data 12345678H inverted in bit order.



Caution Because the debugger rewrites the software break setting line to a break instruction during program execution, the CRC operation result differs if a software break is set in the CRC operation target area.

31.3.2.1 CRC input register (CRCIN)

CRCIN register is an 8-bit register that is used to set the CRC operation data of general-purpose CRC.

The possible setting range is 00H to FFH.

The CRCIN register can be set by an 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 31 - 4 Format of CRC input register (CRCIN)

Address:FFFACH After reset:00H R/W

Symbol	7	6	5	4	3	2	1	0
CRCIN								

Bits 7 to 0	Function
00H to FFH	Data input.

31.3.2.2 CRC data register (CRCD)

This register is used to store the CRC operation result of the general-purpose CRC.

The possible setting range is 0000H to FFFFH.

After 1 clock of CPU/peripheral hardware clock (f_{CLK}) has elapsed from the time CRCIN register is written, the CRC operation result is stored to the CRCD register.

The CRCD register can be set by a 16-bit memory manipulation instruction.

Reset signal generation clears this register to 0000H.

Figure 31 - 5 Format of CRC data register (CRCD)

Address: F02FAH After reset: 0000H R/W

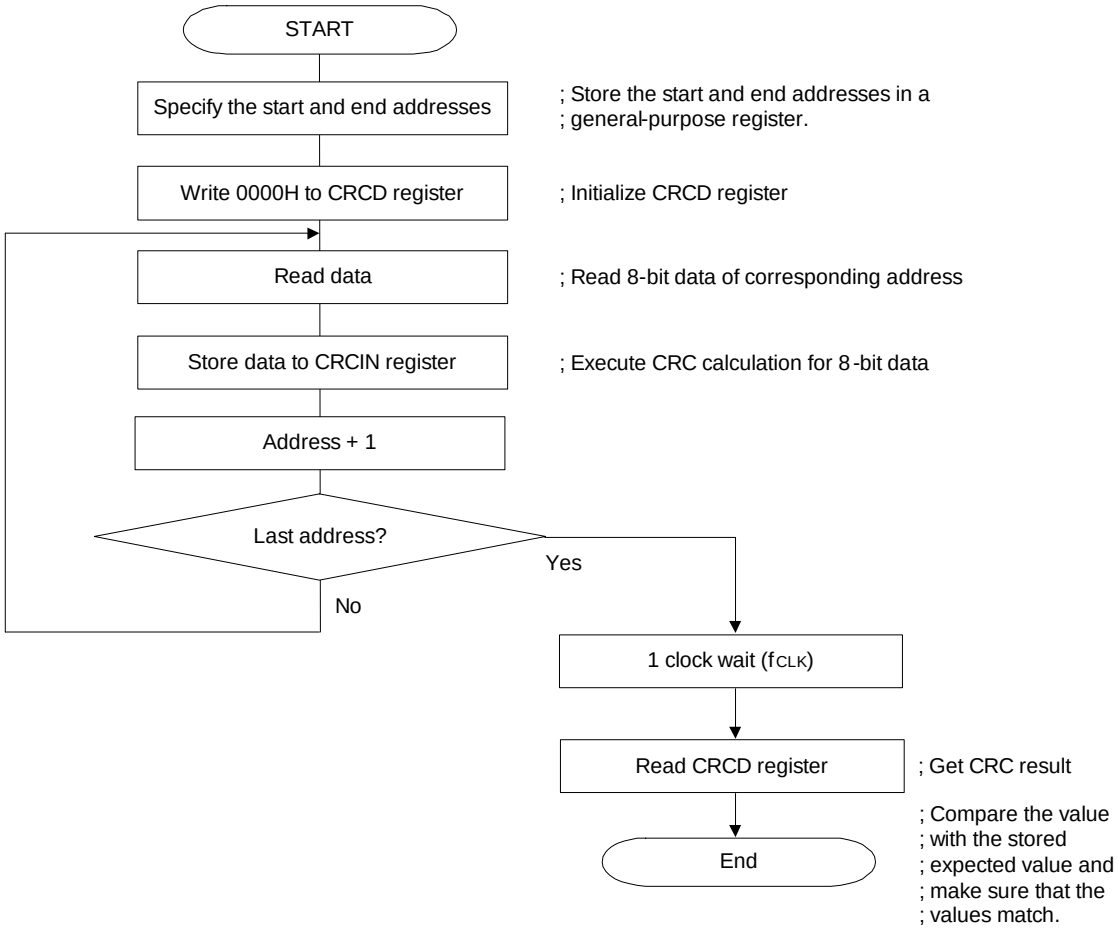
Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CRCD																

Caution 1. Read the value written to CRCD register before writing to CRCIN register.

Caution 2. If writing and storing operation result to CRCD register conflict, the writing is ignored.

<Operation flow>

Figure 31 - 6 CRC Operation Function (General-Purpose CRC)



31.3.3 RAM parity error detection function

The IEC60730 standard mandates the checking of RAM data. A single-bit parity bit is therefore added to all 8-bit data in the RL78/H1D's RAM. By using this RAM parity error detection function, the parity bit is appended when data is written, and the parity is checked when the data is read. This function can also be used to trigger a reset when a parity error occurs.

31.3.3.1 RAM parity error control register (RPECTL)

This register is used to control parity error generation check bit and reset generation due to parity errors.
The RPECTL register can be set by a 1-bit or 8-bit memory manipulation instruction.
Reset signal generation clears this register to 00H.

Figure 31 - 7 Format of RAM parity error control register (RPECTL)

Address: F00F5H After reset: 00H R/W

Symbol	<7>	6	5	4	3	2	1	<0>
RPECTL	RPERDIS	0	0	0	0	0	0	RPEF

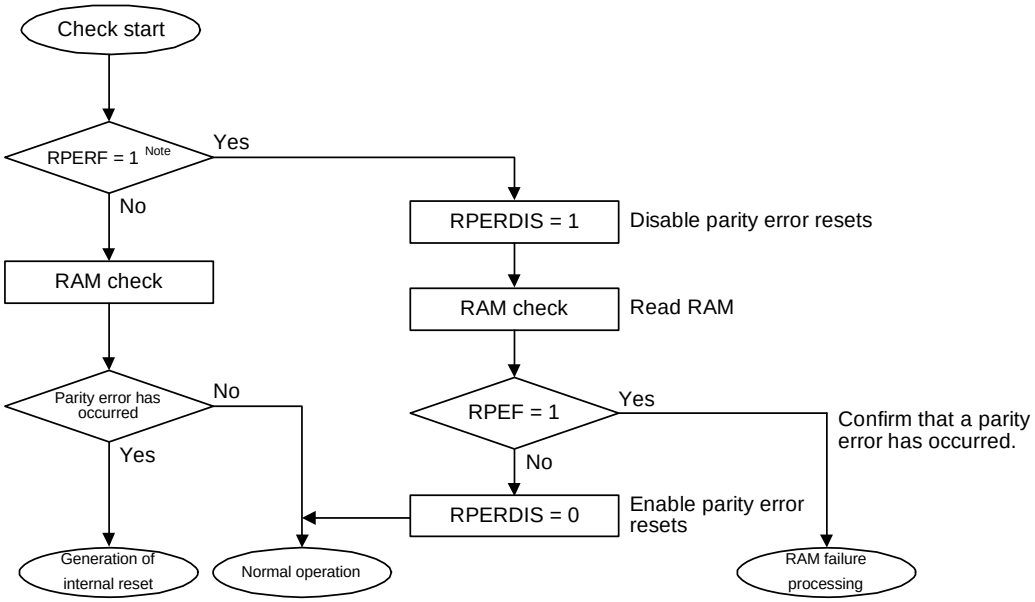
RPERDIS	Parity error reset mask flag
0	Enable parity error resets.
1	Disable parity error resets.

RPEF	Parity error status flag
0	No parity error has occurred.
1	A parity error has occurred.

Caution The parity bit is appended when data is written, and the parity is checked when the data is read. Therefore, while RAM parity error resets are enabled (RPERDIS = 0), be sure to initialize RAM areas where data access is to proceed before reading data.
The RL78's CPU executes look-ahead due to the pipeline operation, the CPU might read an uninitialized RAM area that is allocated beyond the RAM used, which causes a RAM parity error. Therefore, while RAM parity error resets are enabled (RPERDIS = 0), be sure to initialize the RAM area + 10 bytes when instructions are fetched from RAM areas. When using the self-programming function while RAM parity error resets are enabled (RPERDIS = 0), be sure to initialize the RAM area to overwrite + 10 bytes before overwriting.

Remark 1. The parity error reset is enabled by default (RPERDIS = 0).
Remark 2. Even if the parity error reset is disabled (RPERDIS = 1), the RPEF flag will be set (1) if a parity error occurs. If parity error resets are enabled (RPERDIS = 0) with RPEF set to 1, a parity error reset is generated when the RPERDIS bit is cleared to 0.
Remark 3. The RPEF flag in the RPECTL register is set (1) when the RAM parity error occurs and cleared (0) by writing 0 to it or by any reset source. When RPEF = 1, the value is retained even if RAM for which no parity error has occurred is read.
Remark 4. The general registers are not included for RAM parity error detection.

Figure 31 - 8 RAM Parity Error Check Flow



Note See **CHAPTER 28 RESET FUNCTION** for details on how to confirm internal resets due to RAM parity errors.

31.3.4 RAM guard function

<R> This RAM guard function is used to protect data in the specified memory space.
If the RAM guard function is specified, writing to the specified RAM space is disabled, but reading from the space can be carried out as usual.

31.3.4.1 Invalid memory access detection control register (IAWCTL)

This register is used to control the detection of invalid memory access and RAM/SFR guard function.
GRAM1 and GRAM0 bits are used in RAM guard function.
The IAWCTL register can be set by an 8-bit memory manipulation instruction.
Reset signal generation clears this register to 00H.

Figure 31 - 9 Format of Invalid memory access detection control register (IAWCTL)

Address: F0078H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
IAWCTL	IAWEN	0	GRAM1	GRAM0	0	GPORT	GINT	GCSC

GRAM1	GRAM0	RAM guard space Note
0	0	Disabled. RAM can be written to.
0	1	The 128 bytes of space starting at the start address in the RAM
1	0	The 256 bytes of space starting at the start address in the RAM
1	1	The 512 bytes of space starting at the start address in the RAM

Note The RAM start address differs depending on the size of the RAM provided with the product.

31.3.5 SFR guard function

<R> This SFR guard function is used to protect data in the control registers used by the port function, interrupt function, clock control function, voltage detection function, and RAM parity error detection function.
If the SFR guard function is specified, writing to the specified SFRs is disabled, but reading from the SFRs can be carried out as usual.

31.3.5.1 Invalid memory access detection control register (IAWCTL)

This register is used to control the detection of invalid memory access and RAM/SFR guard function.
GPORT, GINT and GCSC bits are used in SFR guard function.
The IAWCTL register can be set by an 8-bit memory manipulation instruction.
Reset signal generation clears this register to 00H.

Figure 31 - 10 Format of Invalid memory access detection control register (IAWCTL)

Address: F0078H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
IAWCTL	IAWEN	0	GRAM1	GRAM0	0	GPORT	GINT	GCSC

GPORT	Control registers of port function guard
0	Disabled. Control registers of port function can be read or written to.
1	Enabled. Writing to control registers of port function is disabled. Reading is enabled. [Guarded SFR] PMxx, PUxx, PIMxx, POMxx, PMCxx, PIORx, PFSEGxx, ISCLCD Note

GINT	Registers of interrupt function guard
0	Disabled. Registers of interrupt function can be read or written to.
1	Enabled. Writing to registers of interrupt function is disabled. Reading is enabled. [Guarded SFR] IFxx, MKxx, PRxx, EGPx, EGNx

GCSC	Control registers of clock control function, voltage detector and RAM parity error detection function guard
0	Disabled. Control registers of clock control function, voltage detector and RAM parity error detection function can be read or written to.
1	Enabled. Writing to control registers of clock control function, voltage detector and RAM parity error detection function is disabled. Reading is enabled. [Guarded SFR] CMC, CSC, OSTS, CKC, PERx, OSMC, CLKDCTL, LVIM, LVIS, RPECTL

Note Pxx (Port register) is not guarded.

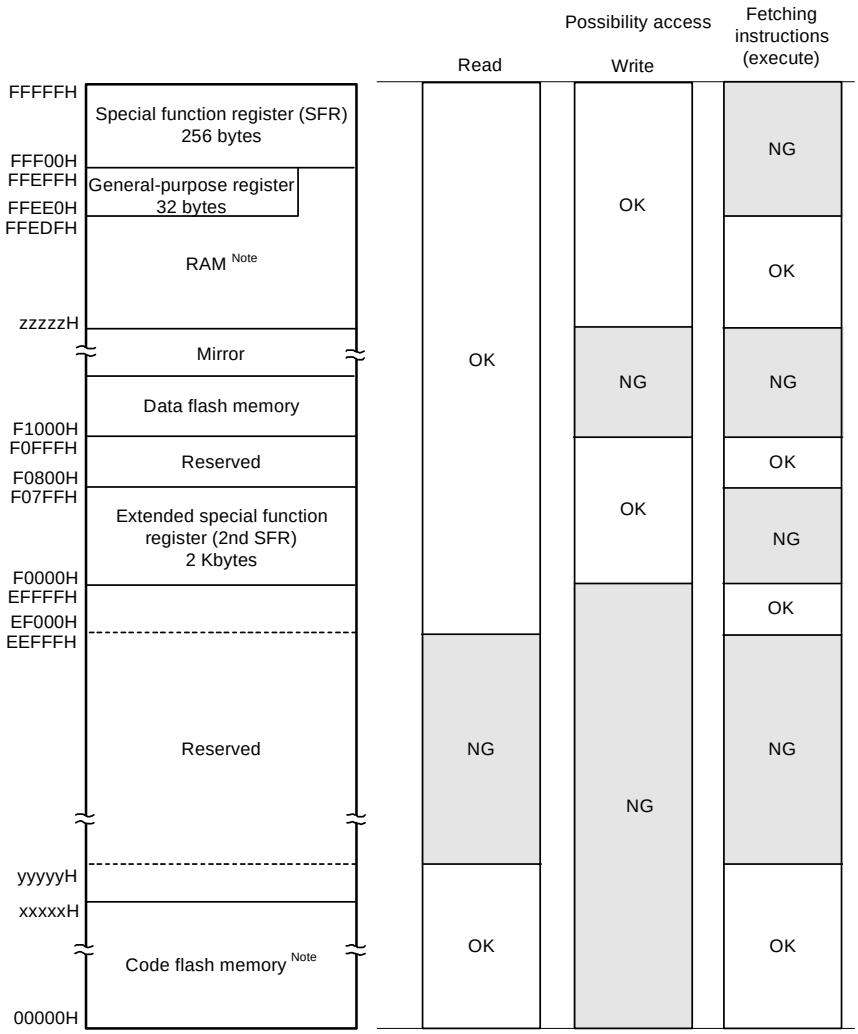
31.3.6 Invalid memory access detection function

The IEC60730 standard mandates checking that the CPU and interrupts are operating correctly.

The illegal memory access detection function triggers a reset if a memory space specified as access-prohibited is accessed.

The illegal memory access detection function applies to the areas indicated by NG in **Figure 31 - 11**.

Figure 31 - 11 Invalid access detection area



Note The following table lists the code flash memory, RAM, and lowest detection address for each product:

Products	Code flash memory (00000H to xxxxxH)	RAM (zzzzzH to FFEFFH)	Detected lowest address for read/instruction fetch (execution) (yyyyyH)
R5F11RMG	131072 × 8 bits (00000H to 1FFFFH)	8192 × 8 bits (FDF00H to FFEFFH)	20000H
R5F11xG (x = NG, NL, NM, PL)	131072 × 8 bits (00000H to 1FFFFH)	5632 × 8 bits (FE900H to FFEFFH)	20000H
R5F11xF (x = NG, NL, NM, PL)	98304 × 8 bits (00000H to 17FFFH)	5632 × 8 bits (FE900H to FFEFFH)	20000H
R5F11NME	65536 × 8 bits (00000H to 0FFFFH)	5632 × 8 bits (FE900H to FFEFFH)	10000H

31.3.6.1 Invalid memory access detection control register (IAWCTL)

This register is used to control the detection of invalid memory access and RAM/SFR guard function.

IAWEN bit is used in invalid memory access detection function.

The IAWCTL register can be set by an 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 31 - 12 Format of Invalid memory access detection control register (IAWCTL)

Address: F0078H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
IAWCTL	IAWEN Note	0	GRAM1	GRAM0	0	GPORT	GINT	GCSC

IAWEN Note	Control of invalid memory access detection
0	Disable the detection of invalid memory access.
1	Enable the detection of invalid memory access.

Note Only writing 1 to the IAWEN bit is enabled, not writing 0 to it after setting it to 1.

Remark By specifying WDTON = 1 (watchdog timer operation enabled) in the option byte (000C0H), the invalid memory access detection function is enabled even IAWEN = 0.

31.3.7 Frequency detection function

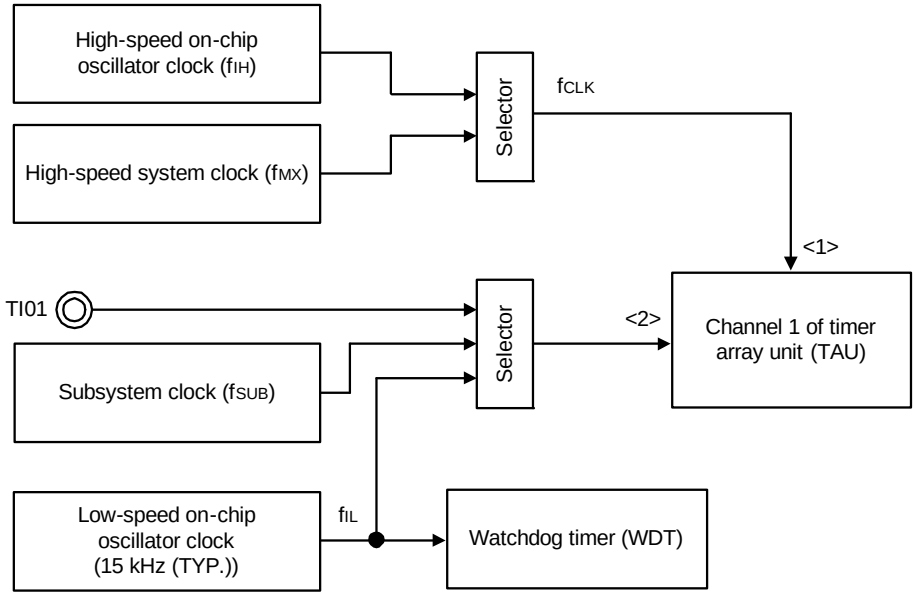
The IEC60730 standard mandates checking that the oscillation frequency is correct.
By using the CPU/peripheral hardware clock frequency (f_{CLK}) and measuring the pulse width of the input signal to channel 1 of the timer array unit (TAU), whether the proportional relationship between the two clock frequencies is correct can be determined. Note that, however, if one or both clock operations are completely stopped, the proportional relationship between the clocks cannot be determined.

<Clocks to be compared>

<1> CPU/peripheral hardware clock frequency (f_{CLK}):
- High-speed on-chip oscillator clock (f_{IH})
- High-speed system clock (f_{MX})

<2> Input to channel 1 of the timer array unit
- Timer input to channel 1 (TI01)
- Low-speed on-chip oscillator clock (f_{IL}: 15 kHz (TYP.))
- Subsystem clock (f_{SUB})

Figure 31 - 13 Configuration of Frequency Detection Function



If pulse interval measurement results in an abnormal value, it can be concluded that the clock frequency is abnormal.
For how to execute pulse interval measurement, see **6.8.3 Operation as input pulse interval measurement**.

31.3.7.1 Timer input select register 0 (TIS0)

This register is used to select the timer input of channels 0, 1.

By selecting the low-speed on-chip oscillator clock for the timer input, its pulse width can be measured to determine whether the proportional relationship between the low-speed on-chip oscillator clock and the timer operation clock is correct.

The TIS0 register can be set by an 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 31 - 14 Format of Timer input select register 0 (TIS0)

Address: F0074H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
TIS0	0	0	0	TIS04	0	TIS02	TIS01	TIS00

TIS04	Selection of timer input used with channel 0
0	Input signal of timer input pin (TI00)
1	Event input signal from ELC

TIS02	TIS01	TIS00	Selection of timer input used with channel 1
0	0	0	Input signal of timer input pin (TI01)
0	1	0	
0	1	1	
0	0	1	Event input signal from ELC
1	0	0	Low-speed on-chip oscillator clock (f_{IL})
1	0	1	Subsystem clock (f_{SUB})
Other than above			Setting prohibited

31.3.8 A/D test function

The IEC60730 standard mandates testing the A/D converter. The A/D test function is used to check whether the A/D converter is operating normally by executing A/D conversions of the positive reference voltage and negative reference voltage of the A/D converter, analog input channel (ANI), temperature sensor output voltage, and internal reference voltage. For details on the checking method, refer to the safety function (A/D test) application note (R01AN0955).

The analog multiplexer can be checked using the following procedure.

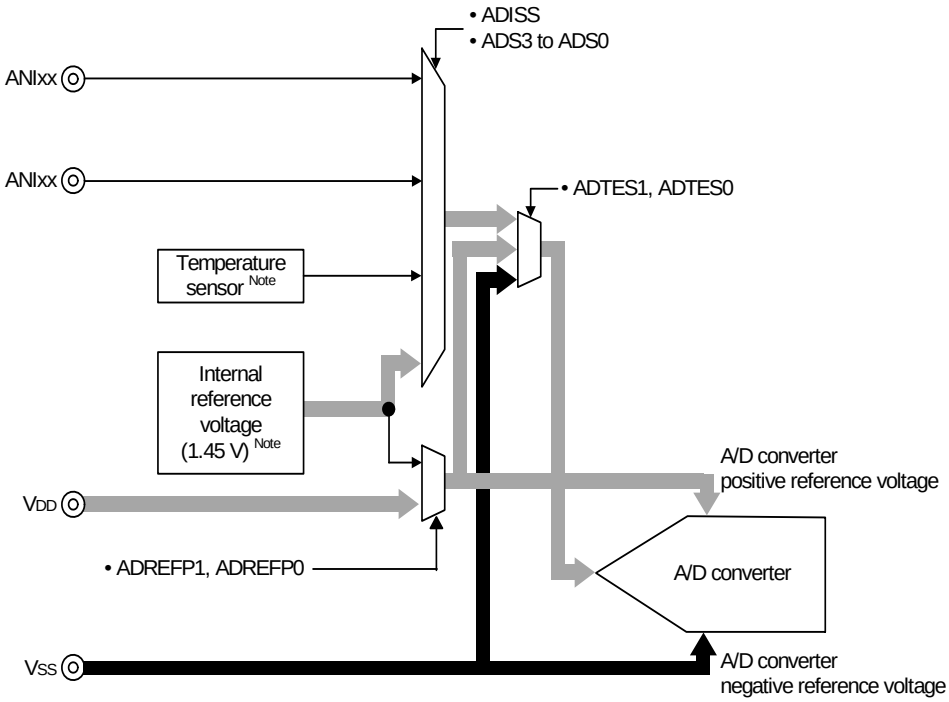
(1) Select the ANIx pin as the target for A/D conversion by setting the ADTES register (ADTES1, ADTES0 = 0, 0).
(2) Perform A/D conversion for the ANIx pin (conversion result 1-1).
(3) Select the negative reference voltage of the A/D converter as the target for A/D conversion by setting the ADTES register (ADTES1, ADTES0 = 1, 0).
(4) Perform A/D conversion of the negative reference voltage of the A/D converter (conversion result 2-1).
(5) Select the ANIx pin as the target for A/D conversion by setting the ADTES register (ADTES1, ADTES0 = 0, 0).
(6) Perform A/D conversion for the ANIx pin (conversion result 1-2).
(7) Select the positive reference voltage of the A/D converter as the target for A/D conversion by setting the ADTES register (ADTES1, ADTES0 = 1, 1).
(8) Perform A/D conversion of the positive reference voltage of the A/D converter (conversion result 2-2).
(9) Select the ANIx pin as the target for A/D conversion by setting the ADTES register (ADTES1, ADTES0 = 0, 0).
(10) Perform A/D conversion for the ANIx pin (conversion result 1-3).
(11) Make sure that “conversion result 1-1” = “conversion result 1-2” = “conversion result 1-3”.
(12) Make sure that the A/D conversion results of “conversion result 2-1” are all 0 and those of “conversion result 2-2” are all 1.

Using the procedure above can confirm that the analog multiplexer is selected and all wiring is connected.

Remark 1. If the analog input voltage is variable during conversion in steps (1) to (10) above, use another method to check the analog multiplexer.

Remark 2. The conversion results might contain an error. Consider an appropriate level of error when comparing the conversion results.

Figure 31 - 15 Configuration of Frequency Detection Function



Note Selectable only in HS (high-speed main) mode.

31.3.8.1 A/D test register (ADTES)

This register is used to select the positive reference voltage and negative reference voltage of the A/D converter, analog input channel (ANIxx), temperature sensor output voltage, or internal reference voltage (1.45 V) as the target of A/D conversion.

When using the A/D test function, specify the following settings:

- Select the negative reference voltage as the target of A/D conversion when measuring the zero-scale.
- Select the positive reference voltage as the target of A/D conversion when measuring the full-scale.

The ADTES register can be set by an 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 31 - 16 Format of A/D test register (ADTES)

Address: F0013H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
ADTES	0	0	0	0	0	0	ADTES1	ADTES0

ADTES1	ADTES0	A/D conversion target
0	0	Set by the analog input channel specification register (ADS).
0	1	Setting prohibited
1	0	Negative reference voltage (Vss)
1	1	Positive reference voltage (selected by the ADREFP1 and ADREFP0 bits in the A/D converter mode register 2 (ADM2))

Caution Be sure to clear bits 2 to 7 to "0".

31.3.8.2 Analog input channel specification register (ADS)

This register specifies the input channel of the analog voltage to be A/D converted.

Set A/D test register (ADTES) to 00H when measuring the ANIxx/temperature sensor output/internal reference voltage (1.45 V).

The ADS register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 31 - 17 Format of Analog input channel specification register (ADS)

Address: FFF31H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
ADS	ADISS	0	0	0	ADS3	ADS2	ADS1	ADS0

ADISS	ADS3	ADS2	ADS1	ADS0	Analog input channel	Input source
0	1	0	0	0	ANI8	P03/ANI8 pin Note 1
0	1	0	0	1	ANI9	P04/ANI9 pin Note 2
0	1	0	1	0	ANI10	P05/ANI10 pin Note 1
0	1	0	1	1	ANI11	P11/ANI11 pin Note 3
0	1	1	0	0	ANI12	ANI12 pin Note 4
0	1	1	0	1	ANI13	ANI13 pin Note 4
0	1	1	1	0	ANI14	ANI14 pin Note 4
1	0	0	0	0	—	Temperature sensor output voltage Note 5
1	0	0	0	1	—	Internal reference voltage (1.45 V) Note 5
Other than above					Setting prohibited	

Note 1. R5F11NL, R5F11PL, R5F11NG, and R5F11RM only.

Note 2. R5F11PL, R5F11NG, and R5F11RM only.

Note 3. R5F11NL only.

Note 4. R5F11NM only.

Note 5. This setting can be used only in HS (high-speed main) mode.

Caution 1. Be sure to clear bits 4 to 6 to 0.

Caution 2. For ports that set to analog input using the port mode control registers 0, 1 (PMC0, PMC1), select input mode using port mode registers 0, 1 (PM0, PM1).

Caution 3. Do not use the ADS register to set ports that to be set as digital I/O using the PMC0 and PMC1 registers.

Caution 4. Only rewrite the value of the ADISS bit while conversion is stopped (ADCS = 0, ADCE = 0).

Caution 5. If ADISS is set to 1, the internal reference voltage (1.45 V) cannot be used for the positive reference voltage. Also, the first conversion result cannot be used after ADISS is set to 1. For details on the setup flow, see 19.7.4 Setup when temperature sensor output voltage/internal reference voltage is selected (example for software trigger mode and one-shot conversion mode).

Caution 6. Do not set ADISS to 1 when entering HALT mode while in STOP mode or while the CPU operates on the subsystem clock. With ADISS = 1, the current value of the A/D converter internal reference voltage current (I_{ADREF}) listed in 38.3.2 or 39.3.2 Supply current characteristics is added.

31.3.9 Digital output signal level detection function for I/O ports

In the IEC60730, it is required to check that the I/O function correctly operates.

By using the digital output signal level detection function for I/O ports, the digital output level of the pin can be read when the port is set to output mode (the PMmn bit in the port mode register (PMm) is 0).

31.3.9.1 Port mode select register (PMS)

This register is used to select the output level from output latch level or pin output level when the port is output mode in which PMm bit of port mode register (PMm) is 0.

This register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears these registers to 00H.

Figure 31 - 18 Format of Port mode select register (PMS)

Address: F007BH After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
PMS	0	0	0	0	0	0	0	PMS0

PMS0	Method for selecting output level to be read when the port is output mode (PMmn = 0)
0	Pmn register value is read.
1	Digital output level of the pin is read.

Caution 1. When setting the PMS0 bit to 1 and rewriting the port register (Pm register), use an 8-bit memory manipulation instruction only.

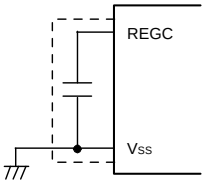
Caution 2. When using P60 and P61 as general-purpose ports, the output level of these pins cannot be read by setting PMS0 (However, only when the IICA0EN bit in the PER0 register is set to 1, the output level of P60 and P61 can be read by setting the PMS0 bit).

Remark m = 0 to 8, 12, 15
n = 0 to 7

CHAPTER 32 REGULATOR

32.1 Regulator Overview

The RL78/H1D contains a circuit for operating the device with a constant voltage. At this time, in order to stabilize the regulator output voltage, connect the REGC pin to Vss via a capacitor (0.47 to 1 µF). Also, use a capacitor with good characteristics, since it is used to stabilize internal voltage.



Caution Keep the wiring length as short as possible for the broken-line part in the above figure.

Table 32 - 1 Regulator Output Voltage Conditions

Mode	Output Voltage	Condition
LS (low-speed main) mode Note 1	1.8 V	—
HS (high-speed main) mode	1.8 V	In STOP mode
		When both the high-speed system clock (fMX) and the high-speed on-chip oscillator clock (fIH) are stopped during CPU operation with the subsystem clock (fSUB)
		When both the high-speed system clock (fMX) and the high-speed on-chip oscillator clock (fIH) are stopped during the HALT mode when the CPU operation with the subsystem clock (fSUB) has been set
	2.1 V	Other than above (include during OCD mode) Note 2

Note 1. R5F11R only.

Note 2. When it shifts to the subsystem clock operation or STOP mode during the on-chip debugging, the regulator output voltage is kept at 2.1 V (not decline to 1.8 V).

CHAPTER 33 OPTION BYTE

33.1 Functions of Option Bytes

Addresses 000C0H to 000C3H of the flash memory of the RL78/H1D form an option byte area.
Option bytes consist of user option byte (000C0H to 000C2H) and on-chip debug option byte (000C3H).
Upon power application or resetting and starting, an option byte is automatically referenced and a specified function is set. When using the product, be sure to set the following functions by using the option bytes.
For the bits to which no function is allocated, do not change their initial values.
To use the boot swap operation during self programming, 000C0H to 000C3H are replaced by 010C0H to 010C3H. Therefore, set the same values as 000C0H to 000C3H to 010C0H to 010C3H.

Remark The option bytes should always be set regardless of whether each function is used.

33.1.1 User option byte (000C0H to 000C2H/010C0H to 010C2H)

(1) 000C0H/010C0H

- ○ Operation of watchdog timer
  - • Enabling or disabling of counter operation
  - • Enabling or disabling of counter operation in the HALT or STOP mode
- ○ Setting of interval time of watchdog timer
- ○ Setting of window open period of watchdog timer
- ○ Setting of interval interrupt of watchdog timer
  - • Whether or not to use the interval interrupt is selectable

Caution Set the same value as 000C0H to 010C0H when the boot swap operation is used because 000C0H is replaced by 010C0H.

(2) 000C1H/010C1H

○ Setting of LVD operation mode
- Interrupt & reset mode
- Reset mode
- Interrupt mode
- LVD off (by controlling the externally input reset signal on the $\overline{\text{RESET}}$ pin)

○ Setting of LVD detection level (V_{LVDH}, V_{LVDL}, V_{LVD})

Caution 1. After power is supplied, the reset state must be retained until the operating voltage becomes in the range defined in 38.4 or 39.4 AC Characteristics. This is done by utilizing the voltage detection circuit or controlling the externally input reset signal. After the power supply is turned off, this LSI should be placed in the STOP mode, or placed in the reset state by utilizing the voltage detection circuit or controlling the externally input reset signal, before the voltage falls below the operating range. The range of operating voltage varies with the setting of the user option byte (000C2H or 010C2H).

Caution 2. Set the same value as 000C1H to 010C1H when the boot swap operation is used because 000C1H is replaced by 010C1H.

(3) 000C2H/010C2H

○ Setting of flash operation mode
- LS (low speed main) mode
- HS (high speed main) mode

○ Setting of the frequency of the high-speed on-chip oscillator
- Select from 24 MHz, 16 MHz, 12 MHz, 8 MHz, 6 MHz, 4 MHz, 3 MHz, 2 MHz, and 1 MHz (TYP).

Caution Set the same value as 000C2H to 010C2H when the boot swap operation is used because 000C2H is replaced by 010C2H.

33.1.2 On-chip debug option byte (000C3H/ 010C3H)

○ Control of on-chip debug operation
- On-chip debug operation is disabled or enabled.

○ Handling of data of flash memory in case of failure in on-chip debug security ID authentication
- Data of flash memory is erased or not erased in case of failure in on-chip debug security ID authentication.

Caution Set the same value as 000C3H to 010C3H when the boot swap operation is used because 000C3H is replaced by 010C3H.

33.2 Format of User Option Byte

The format of user option byte is shown below.

Figure 33 - 1 Format of User Option Byte (000C0H/010C0H)

Address: 000C0H/010C0H Note 1

7	6	5	4	3	2	1	0
WDTINT	WINDOW1	WINDOW0	WDTON	WDCS2	WDCS1	WDCS0	WDSTBYON

WDTINT	Use of interval interrupt of watchdog timer
0	Interval interrupt is not used.
1	Interval interrupt is generated when 75% of the overflow time + 1/2fIL is reached.Note 3

WINDOW1	WINDOW0	Watchdog timer window open period Note 2
0	1	50%
1	1	100%
Other than above		Setting prohibited

WDTON	Operation control of watchdog timer counter
0	Counter operation disabled (counting stopped after reset)
1	Counter operation enabled (counting started after reset)

WDCS2	WDCS1	WDCS0	Watchdog timer overflow time (fIL = 17.25 kHz (MAX.))
0	0	0	2^6/fIL (3.71 ms)
0	0	1	2^7/fIL (7.42 ms)
0	1	0	2^8/fIL (14.84 ms)
0	1	1	2^9/fIL (29.68 ms)
1	0	0	2^{11}/fIL (118.72 ms)
1	0	1	2^{13}/fIL (474.89 ms)
1	1	0	2^{14}/fIL (949.79 ms)
1	1	1	2^{16}/fIL (3799.18 ms)

WDSTBYON	Operation control of watchdog timer counter (HALT/STOP mode)
0	Counter operation stopped in HALT/STOP mode Note 2
1	Counter operation enabled in HALT/STOP mode

Note 1. Set the same value as 000C0H to 010C0H when the boot swap operation is used because 000C0H is replaced by 010C0H.

Note 2. The window open period is 100% when WDSTBYON = 0, regardless the value of the WINDOW1 and WINDOW0 bits.

Note 3. When the interval interrupt of the watchdog timer is in use, clear the counter of the watchdog timer by following the procedure under **14.4.5 Cautions on the watchdog timer**.

Remark fIL: Low-speed on-chip oscillator clock frequency

Figure 33 - 2 Format of User Option Byte (000C1H/010C1H) (1/2)

Address: 000C1H/010C1H Note 1

7	6	5	4	3	2	1	0
VPOC2	VPOC1	VPOC0	1	LVIS1	LVIS0	LVIMDS1	LVIMDS0

• LVD setting (interrupt & reset mode)

Detection voltage			Option byte Setting Value						
V_{LVDH}		V_{LVDL}	VPOC2	VPOC1	VPOC0	LVIS1	LVIS0	Mode setting	
Rising edge	Falling edge	Falling edge						LVIMDS1	LVIMDS0
1.98 V Note 2	1.94 V Note 2	1.84 V Note 2	0	0	1	1	0	1	0
2.09 V Note 2	2.04 V Note 2					0	1		
3.13 V Note 2	3.06 V Note 2					0	0		
2.61 V	2.55 V	2.45 V		1	0	1	0		
2.71 V	2.65 V					0	1		
3.75 V	3.67 V					0	0		
2.92 V	2.86 V	2.75 V		1	1	1	0		
3.02 V	2.96 V					0	1		
4.06 V	3.98 V					0	0		
—			Setting of values other than above is prohibited						

• LVD setting (reset mode)

Detection voltage		Option byte Setting Value						
V_{LVD}		VPOC2	VPOC1	VPOC0	LVIS1	LVIS0	Mode setting	
Rising edge	Falling edge						LVIMDS1	LVIMDS0
1.88 V Note 2	1.84 V Note 2	0	0	1	1	1	1	1
1.98 V Note 2	1.94 V Note 2				1	0		
2.09 V Note 2	2.04 V Note 2				0	1		
2.50 V	2.45 V		1	0	1	1		
2.61 V	2.55 V				1	0		
2.71 V	2.65 V				0	1		
2.81 V	2.75 V		1	1	1	1		
2.92 V	2.86 V				1	0		
3.02 V	2.96 V				0	1		
3.13 V	3.06 V		0	1	0	0		
3.75 V	3.67 V		1	0	0	0		
4.06 V	3.98 V		1	1	0	0		
—		Setting of values other than above is prohibited						

Note 1. Set the same value as 000C1H to 010C1H when the boot swap operation is used because 000C1H is replaced by 010C1H.

Note 2. R5F11R only. Setting is prohibited for R5F11N and R5F11P.

Remark 1. For details on the LVD circuit, see **CHAPTER 30 VOLTAGE DETECTOR**.

Remark 2. The detection voltage is a typical value. For details, see **38.6.4** or **39.6.4 LVD circuit characteristics**.

(**Cautions** are listed on the next page.)

Figure 33 - 2 Format of User Option Byte (000C1H/010C1H) (2/2)

Address: 000C1H/010C1H Note 1

7	6	5	4	3	2	1	0
VPOC2	VPOC1	VPOC0	1	LVIS1	LVIS0	LVIMDS1	LVIMDS0

• LVD setting (interrupt mode)

Detection voltage		Option byte Setting Value						
V_{LVD}		VPOC2	VPOC1	VPOC0	LVIS1	LVIS0	Mode setting	
Rising edge	Falling edge						LVIMDS1	LVIMDS0
1.88 V Note 2	1.84 V Note 2	0	0	1	1	1	0	1
1.98 V Note 2	1.94 V Note 2				1	0		
2.09 V Note 2	2.04 V Note 2				0	1		
2.50 V	2.45 V		1	0	1	1		
2.61 V	2.55 V				1	0		
2.71 V	2.65 V				0	1		
2.81 V	2.75 V		1	1	1	1		
2.92 V	2.86 V				1	0		
3.02 V	2.96 V				0	1		
3.13 V	3.06 V		0	1	0	0		
3.75 V	3.67 V		1	0	0	0		
4.06 V	3.98 V		1	1	0	0		
—		Setting of values other than above is prohibited						

• LVD off (by controlling the externally input reset signal on the $\overline{\text{RESET}}$ pin)

Detection voltage		Option byte Setting Value						
V_{LVD}		VPOC2	VPOC1	VPOC0	LVIS1	LVIS0	Mode setting	
Rising edge	Falling edge						LVIMDS1	LVIMDS0
—	—	1	×	×	×	×	×	1
—		Setting of values other than above is prohibited						

Note 1. Set the same value as 000C1H to 010C1H when the boot swap operation is used because 000C1H is replaced by 010C1H.

Note 2. R5F11R only. Setting is prohibited for R5F11N and R5F11P.

Caution 1. Be sure to set bit 4 to "1".

Caution 2. After power is supplied, the reset state must be retained until the operating voltage becomes in the range defined in 38.4 or 39.4 AC Characteristics. This is done by utilizing the voltage detection circuit or controlling the externally input reset signal. After the power supply is turned off, this LSI should be placed in the STOP mode, or placed in the reset state by utilizing the voltage detection circuit or controlling the externally input reset signal, before the voltage falls below the operating range. The range of operating voltage varies with the setting of the user option byte (000C2H or 010C2H).

Remark 1. ×: don't care

Remark 2. For details on the LVD circuit, see **CHAPTER 30 VOLTAGE DETECTOR**.

Remark 3. The detection voltage is a typical value. For details, see **38.6.4** or **39.6.4 LVD circuit characteristics**.

Figure 33 - 3 Format of User Option Byte (000C2H/010C2H)

Address: 000C2H/010C2H Note 1

7	6	5	4	3	2	1	0
CMODE1	CMODE0	1	0	FRQSEL3	FRQSEL2	FRQSEL1	FRQSEL0

CMODE1	CMODE0	Setting of flash operation mode		
			Operating Frequency Range (f_{MAIN})	Operating Voltage Range (V_{DD})
1	0	LS (low speed main) mode Note 2	1 to 8 MHz	1.8 to 5.5 V
1	1	HS (high speed main) mode	1 to 16 MHz	2.4 to 5.5 V
			1 to 24 MHz	2.7 to 5.5 V
Other than above		Setting prohibited		

FRQSEL3	FRQSEL2	FRQSEL1	FRQSEL0	Frequency of the high-speed on-chip oscillator clock (f_{IH})
0	0	0	0	24 MHz
1	0	0	1	16 MHz
0	0	0	1	12 MHz
1	0	1	0	8 MHz
0	0	1	0	6 MHz
1	0	1	1	4 MHz
0	0	1	1	3 MHz
1	1	0	0	2 MHz
1	1	0	1	1 MHz
Other than above				Setting prohibited

Note 1. Set the same value as 000C2H to 010C2H when the boot swap operation is used because 000C2H is replaced by 010C2H.

Note 2. R5F11R only.

Caution 1. Be sure to set bits 5 and 4 to 10B.

Caution 2. The ranges of operation frequency and operation voltage vary depending on the flash operation mode. For details, see 38.4 or 39.4 AC Characteristics.

33.3 Format of On-chip Debug Option Byte

The format of on-chip debug option byte is shown below.

Figure 33 - 4 Format of On-chip Debug Option Byte (000C3H/010C3H)

Address: 000C3H/010C3H Note

7	6	5	4	3	2	1	0
OCDENSET	0	0	0	0	1	0	OCDERSD

OCDENSET	OCDERSD	Control of on-chip debug operation
0	0	Disables on-chip debug operation.
0	1	Setting prohibited
1	0	Enables on-chip debugging. Erases data of flash memory in case of failures in authenticating on-chip debug security ID.
1	1	Enables on-chip debugging. Does not erases data of flash memory in case of failures in authenticating on-chip debug security ID.

Note Set the same value as 000C3H to 010C3H when the boot swap operation is used because 000C3H is replaced by 010C3H.

Caution **Bits 7 and 0 (OCDENSET and OCDERSD) can only be specified a value.**
Be sure to write 000010B to bits 6 to 1.

Remark The value on bits 3 to 1 will be written over when the on-chip debug function is in use and thus it will become unstable after the setting.
However, be sure to set the default values (0, 1, and 0) to bits 3 to 1 at setting.

33.4 Setting of Option Byte

The user option byte and on-chip debug option byte can be set using the link option, in addition to describing to the source. When doing so, the contents set by using the link option take precedence, even if descriptions exist in the source, as mentioned below.

A software description example of the option byte setting is shown below.

```
OPT     CSEG    OPT_BYTE
        DB      36H     ; Does not use interval interrupt of watchdog timer,
                        ; Enables watchdog timer operation,
                        ; Window open period of watchdog timer is 50%,
                        ; Overflow time of watchdog timer is 2^9/fIL,
                        ; Stops watchdog timer operation during HALT/STOP mode
        DB      5AH     ; Select 2.45 V for VLVDL
                        ; Select rising edge 2.61 V, falling edge 2.55 V for VLVDH
                        ; Select the interrupt & reset mode as the LVD operation mode
        DB      ADH     ; Select the LS (low speed main) mode as the flash operation mode
                          and 1 MHz as the frequency of the high-speed on-chip oscillator clock
        DB      85H     ; Enables on-chip debug operation, does not erase flash memory
                          data when security ID authorization fails
```

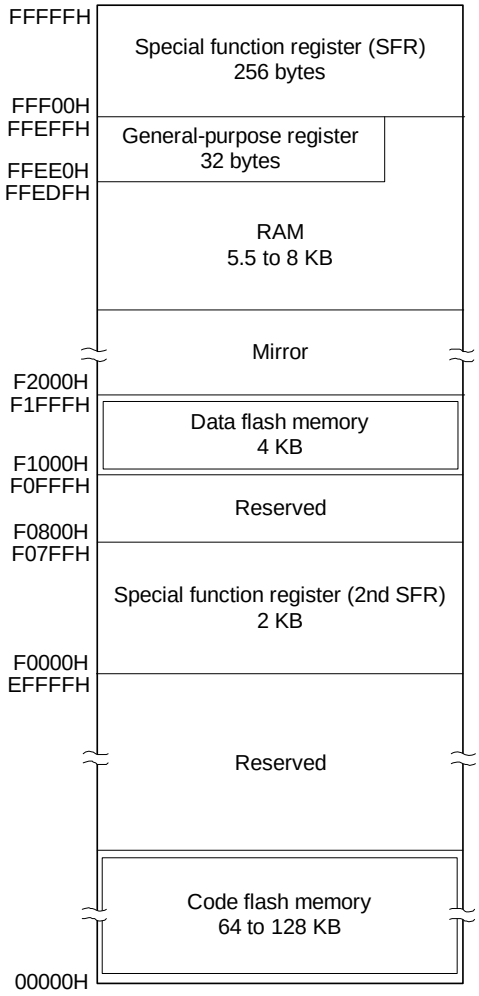
When the boot swap function is used during self programming, 000C0H to 000C3H is switched to 010C0H to 010C3H. Describe to 010C0H to 010C3H, therefore, the same values as 000C0H to 000C3H as follows.

```
OPT2    CSEG    AT      010C0H
        DB      36H     ; Does not use interval interrupt of watchdog timer,
                        ; Enables watchdog timer operation,
                        ; Window open period of watchdog timer is 50%,
                        ; Overflow time of watchdog timer is 2^9/fIL,
                        ; Stops watchdog timer operation during HALT/STOP mode
        DB      5AH     ; Select 2.45 V for VLVDL
                        ; Select rising edge 2.61 V, falling edge 2.55 V for VLVDH
                        ; Select the interrupt & reset mode as the LVD operation mode
        DB      ADH     ; Select the LS (low speed main) mode as the flash operation mode
                          and 1 MHz as the frequency of the high-speed on-chip oscillator clock
        DB      85H     ; Enables on-chip debug operation, does not erase flash memory
                          data when security ID authorization fails
```

Caution To specify the option byte by using assembly language, use OPT_BYTE as the relocation attribute name of the CSEG pseudo instruction. To specify the option byte to 010C0H to 010C3H in order to use the boot swap function, use the relocation attribute AT to specify an absolute address.

CHAPTER 34 FLASH MEMORY

The RL78 microcontroller incorporates the flash memory to which a program can be written, erased, and overwritten while mounted on the board. The flash memory includes the “code flash memory”, in which programs can be executed, and the “data flash memory”, an area for storing data.



The following methods for programming the flash memory are available.
The code flash memory can be rewritten to through serial programming using a flash memory programmer or an external device (UART communication), or through self-programming.

- Serial programming using flash memory programmer (see **34.4**)
  Data can be written to the flash memory on-board or off-board by using a dedicated flash memory programmer.

- Serial programming using external device (UART communication) (see **34.2**)
  Data can be written to the flash memory on-board through UART communication with an external device (microcontroller or ASIC).

- Self-programming (see **34.6**)
  The user application can execute self-programming of the code flash memory by using the flash self-programming library.

The data flash memory can be rewritten to by using the data flash library during user program execution (background operation). For access and writing to the data flash memory, see **34.8 Data Flash**.

34.1 Serial Programming Using Flash Memory Programmer

The following dedicated flash memory programmer can be used to write data to the internal flash memory of the RL78 microcontroller.

- PG-FP6, FL-PR6
- E1, E2, E2 Lite, E20 on-chip debugging emulator

Data can be written to the flash memory on-board or off-board, by using a dedicated flash memory programmer.

(1) On-board programming

The contents of the flash memory can be rewritten after the RL78 microcontroller has been mounted on the target system. The connectors that connect the dedicated flash memory programmer must be mounted on the target system.

(2) Off-board programming

Data can be written to the flash memory with a dedicated program adapter (FA series) before the RL78 microcontroller is mounted on the target system.

Remark FL-PR6 and FA series are products of Naito Densei Machida Mfg. Co., Ltd.

Table 34 - 1 Wiring Between RL78/H1D and Dedicated Flash Memory Programmer

Pin Configuration of Dedicated Flash Memory Programmer				Pin Name	Pin No.				
					48-pin	64-pin		80-pin	
Signal Name		I/O	Pin Function		LQFP (7 × 7)	TFBGA (4 × 4)	LQFP (10 × 10)	LQFP (12 × 12)	
PG-FP6, FL-PR6	E1, E2, E2 Lite, E20 on-chip debugging emulator				R5F11NG	R5F11PL	R5F11NL	R5F11NM	R5F11RM
—	TOOL0	I/O	Transmit/receive signal	TOOL0/ P40	4	F5	5	9	
SI/RxD	—	I/O	Transmit/receive signal						
—	$\overline{\text{RESET}}$	Output	Reset signal	$\overline{\text{RESET}}$	5	F6	6	10	
/RESET	—	Output							
V_{DD}		I/O	V_{DD} voltage generation/ power monitoring	V_{DD}	13	G8	14	18	
GND		—	Ground	V_{SS}	12	H8	13	17	
				REGC Note	11	G6	12	16	
FLMD1	EMV_{DD}	—	Driving power for TOOL pin	V_{DD}	13	G8	14	18	

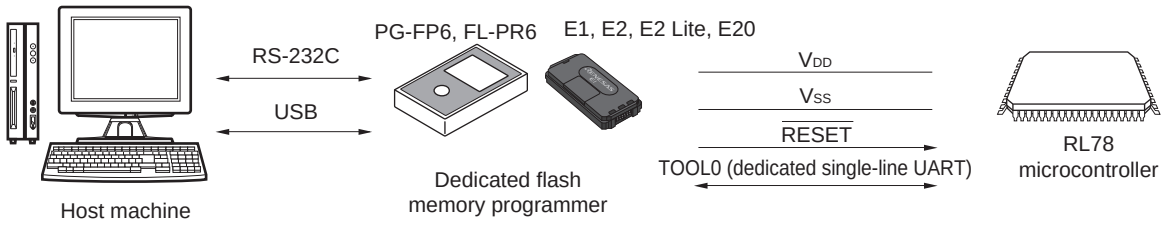
Note Connect REGC pin to ground via a capacitor (0.47 to 1 µF).

Remark Pins that are not indicated in the above table can be left open when using the flash memory programmer for flash programming.

34.1.1 Programming Environment

The environment required for writing a program to the flash memory of the RL78 microcontroller is illustrated below.

Figure 34 - 1 Environment for Writing Program to Flash Memory



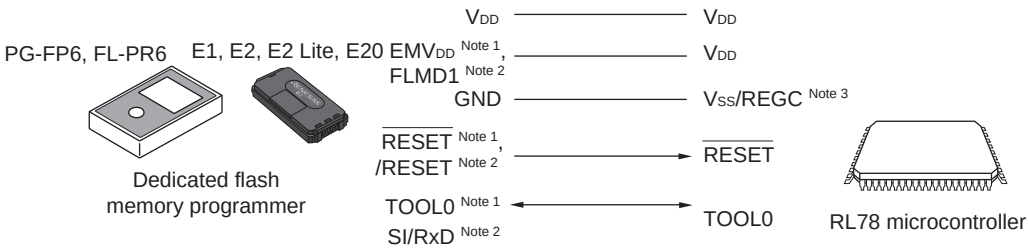
A host machine that controls the dedicated flash memory programmer is necessary.
To interface between the dedicated flash memory programmer and the RL78 microcontroller, the TOOL0 pin is used for manipulation such as writing and erasing via a dedicated single-line UART.

34.1.2 Communication Mode

Communication between the dedicated flash memory programmer and the RL78 microcontroller is established by serial communication using the TOOL0 pin via a dedicated single-line UART of the RL78 microcontroller.

Transfer rate: 1 M, 500 k, 250 k, 115.2 kbps

Figure 34 - 2 Communication with Dedicated Flash Memory Programmer



Note 1. When using E1, E2, E2 Lite, E20 on-chip debugging emulator.
Note 2. When using PG-FP6 or FL-PR6.
Note 3. Connect REGC pin to ground via a capacitor (0.47 to 1 µF).

The dedicated flash memory programmer generates the following signals for the RL78 microcontroller. See each manual of PG-FP6, FL-PR6, or E1, E2, E2 Lite, E20 on-chip debugging emulator for details.

Table 34 - 2 Pin Connection

Dedicated Flash Memory Programmer				RL78 microcontroller
Signal Name		I/O	Pin Function	Pin Name Note 2
PG-FP6, FL-PR6	E1, E2, E2 Lite, E20 on-chip debugging emulator			
V_{DD}		I/O	V_{DD} voltage generation/power monitoring	V_{DD}
GND		—	Ground	V_{SS}, REGC Note 1
FLMD1	EMV_{DD}	—	Driving power for TOOL0 pin	V_{DD}
/RESET	—	Output	Reset signal	$\overline{\text{RESET}}$
—	$\overline{\text{RESET}}$	Output		
—	TOOL0	I/O	Transmit/receive signal	TOOL0
SI/RxD	—	I/O	Transmit/receive signal	

Note 1. Connect REGC pin to ground via a capacitor (0.47 to 1 µF).

Note 2. Pins to be connected differ with the product. For details, see **Table 34 - 1**.

34.2 Serial Programming Using External Device (that Incorporates UART)

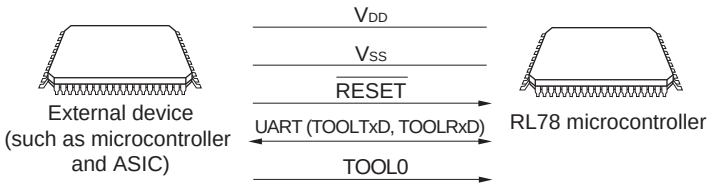
On-board data writing to the internal flash memory is possible by using the RL78 microcontroller and an external device (a microcontroller or ASIC) connected to a UART.

On the development of flash memory programmer by user, refer to **RL78 microcontrollers (RL78 Protocol A) Programmer Edition Application Note (R01AN0815)**.

34.2.1 Programming Environment

The environment required for writing a program to the flash memory of the RL78 microcontroller is illustrated below.

Figure 34 - 3 Environment for Writing Program to Flash Memory



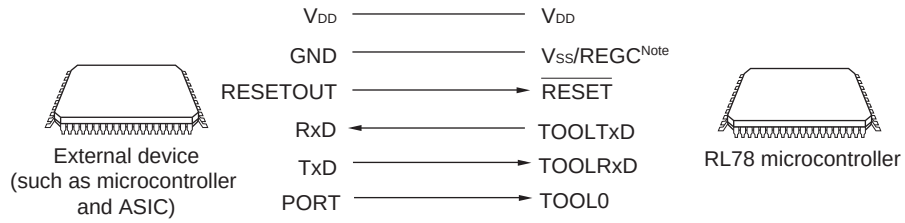
Processing to write data to or delete data from the RL78 microcontroller by using an external device is performed on-board. Off-board writing is not possible.

34.2.2 Communication Mode

Communication between the external device and the RL78 microcontroller is established by serial communication using the TOOLTxD and TOOLRxD pins via the dedicated UART of the RL78 microcontroller.

Transfer rate: 1 M, 500 k, 250 k, 115.2 kbps

Figure 34 - 4 Communication with External Device



Note Connect REGC pin to ground via a capacitor (0.47 to 1 µF).

The external device generates the following signals for the RL78 microcontroller.

Table 34 - 3 Pin Connection

External Device			RL78 microcontroller
Signal Name	I/O	Pin Function	Pin Name
VDD	I/O	VDD voltage generation/power monitoring	VDD
GND	—	Ground	VSS, REGC Note
RESETOUT	Output	Reset signal output	$\overline{\text{RESET}}$
RxD	Input	Receive signal	TOOLTxD
TxD	Output	Transmit signal	TOOLRxD
PORT	Output	Mode signal	TOOL0

Note Connect REGC pin to ground via a capacitor (0.47 to 1 µF).

34.3 Connection of Pins on Board

To write the flash memory on-board by using the flash memory programmer, connectors that connect the dedicated flash memory programmer must be provided on the target system. First provide a function that selects the normal operation mode or flash memory programming mode on the board.

When the flash memory programming mode is set, all the pins not used for programming the flash memory are in the same status as immediately after reset. Therefore, if the external device does not recognize the state immediately after reset, the pins must be handled as described below.

Remark For flash programming mode, see **34.4.2 Flash memory programming mode**.

34.3.1 P40/TOOL0 pin

In the flash memory programming mode, connect this pin to the dedicated flash memory programmer via an external 1 kΩ pull-up resistor.

When this pin is used as the port pin, use that by the following method.

When used as an input pin:	Input of low-level is prohibited for t_{HD} period after external reset release. However, when this pin is used via pull-down resistors, use the 500 kΩ or more resistors.
When used as an output pin:	When this pin is used via pull-down resistors, use the 500 kΩ or more resistors.

Remark 1. t_{HD}: How long to keep the TOOL0 pin at the low level from when the external and internal resets end for setting of the flash memory programming mode. See **38.12** or **39.12 Timing of Entry to Flash Memory Programming Modes**.

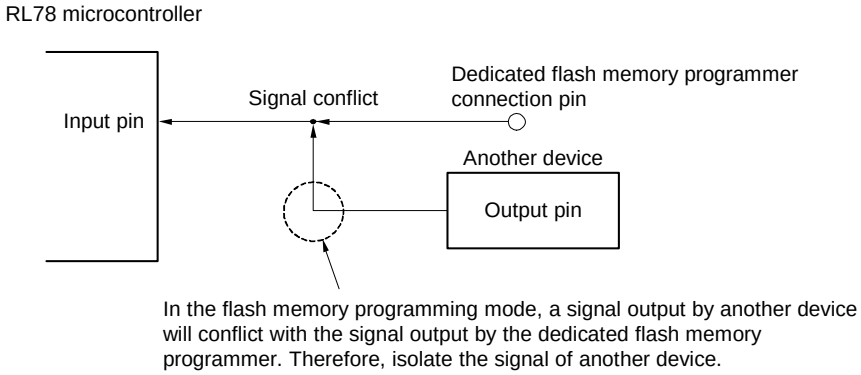
Remark 2. The SAU and IICA pins are not used for communication between the RL78 microcontroller and dedicated flash memory programmer, because single-line UART (TOOL0 pin) is used.

34.3.2 $\overline{\text{RESET}}$ pin

Signal conflict will occur if the reset signal of the dedicated flash memory programmer and external device are connected to the $\overline{\text{RESET}}$ pin that is connected to the reset signal generator on the board. To prevent this conflict, isolate the connection with the reset signal generator.

The flash memory will not be correctly programmed if the reset signal is input from the user system while the flash memory programming mode is set. Do not input any signal other than the reset signal of the dedicated flash memory programmer and external device.

Figure 34 - 5 Signal Conflict ($\overline{\text{RESET}}$ Pin)



34.3.3 Port pins

When the flash memory programming mode is set, all the pins not used for flash memory programming enter the same status as that immediately after reset. If external devices connected to the ports do not recognize the port status immediately after reset, the port pin must be connected to either to V_{DD}, or V_{SS}, via a resistor.

34.3.4 REGC pin

Connect the REGC pin to GND via a capacitor having excellent characteristics (0.47 to 1 µF) in the same manner as during normal operation. Also, use a capacitor with good characteristics, since it is used to stabilize internal voltage.

34.3.5 X1 and X2 pins

Connect X1 and X2 in the same status as in the normal operation mode.

Remark In the flash memory programming mode, the high-speed on-chip oscillator clock (f_{IH}) is used.

34.3.6 Power supply

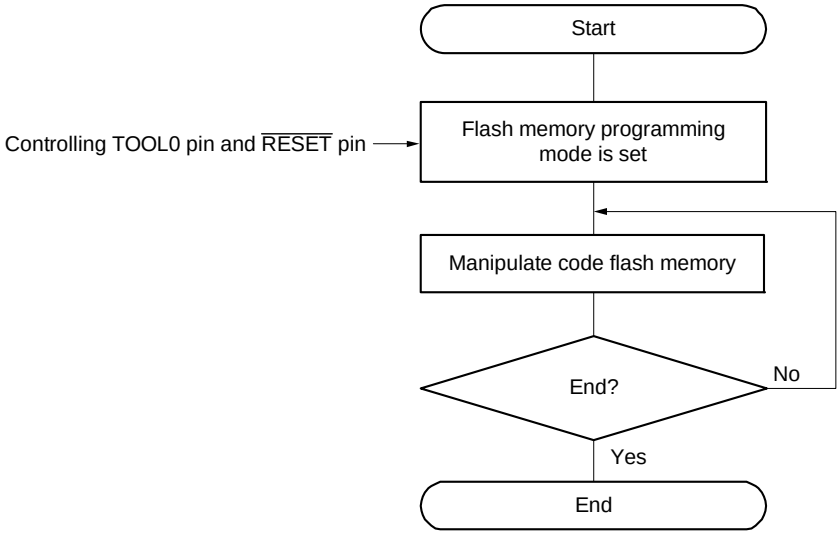
To use the supply voltage output of the flash memory programmer, connect the V_{DD} pin to V_{DD} of the flash memory programmer, and the V_{SS} pin to GND of the flash memory programmer.
To use the on-board supply voltage, connect in compliance with the normal operation mode.
However, when writing to the flash memory by using the flash memory programmer and using the on-board supply voltage, be sure to connect the V_{DD} and V_{SS} pins to V_{DD} and GND of the flash memory programmer to use the power monitor function with the flash memory programmer.

34.4 Serial Programming Method

34.4.1 Serial programming procedure

The following figure illustrates a flow for rewriting the code flash memory through serial programming.

Figure 34 - 6 Code Flash Memory Manipulation Procedure



34.4.2 Flash memory programming mode

To rewrite the contents of the code flash memory through serial programming, specify the flash memory programming mode. To enter the mode, set as follows.

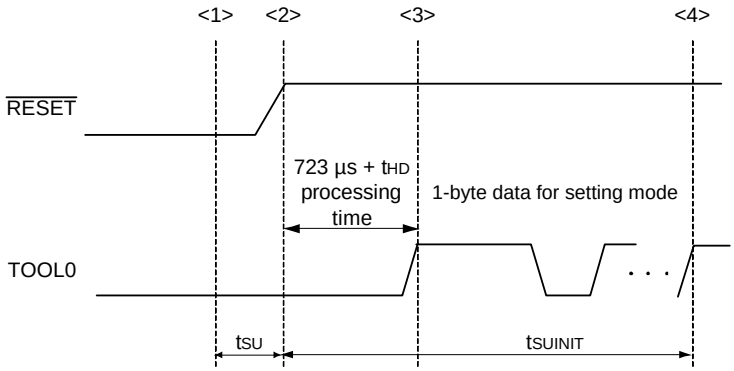
<Serial programming using the dedicated flash memory programmer>
Connect the RL78 microcontroller to a dedicated flash memory programmer. Communication from the dedicated flash memory programmer is performed to automatically switch to the flash memory programming mode.

<Serial programming using an external device (UART communication)>
Set the TOOL0 pin to the low level, and then cancel the reset (see **Table 34 - 4**). After that, enter flash memory programming mode according to the procedures <1> to <4> shown in **Figure 34 - 7**. For details, refer to **RL78 Microcontrollers (RL78 Protocol A) Programmer Edition Application Note (R01AN0815).**

Table 34 - 4 Relationship Between TOOL0 Pin and Operation Mode After Reset Release

TOOL0	Operation Mode
V_{DD}	Normal operation mode
0 V	Flash memory programming mode

Figure 34 - 7 Setting of Flash Memory Programming Mode



<1> The low level is input to the TOOL0 pin.
<2> The external reset ends (POR and LVD reset must end before the pin reset ends.).
<3> The TOOL0 pin is set to the high level.
<4> Baud rate setting by UART reception is completed.

Remark t_{SUINIT}: The segment shows that it is necessary to finish specifying the initial communication settings within 100 ms from when the external resets end.
t_{SU}: How long from when the TOOL0 pin is placed at the low level until a external reset ends
t_{HD}: How long to keep the TOOL0 pin at the low level from when the external reset end (the flash firmware processing time is excluded)

For details, see **38.12** or **39.12 Timing of Entry to Flash Memory Programming Modes**.
There are two flash memory programming modes: wide voltage mode and full speed mode. The supply voltage value applied to the microcontroller during write operations and the setting information of the user option byte for setting of the flash memory programming mode determine which mode is selected.
When a dedicated flash memory programmer is used for serial programming, setting the voltage on GUI selects the mode automatically.

Table 34 - 5 Programming Modes and Voltages at Which Data Can Be Written, Erased, or Verified

Power Supply Voltage (V_{DD})	User Option Byte Setting for Switching to Flash Memory Programming Mode		Flash Programming Mode
	Flash Operation Mode	Operating Frequency	
2.7 V ≤ V_{DD} ≤ 5.5 V	Blank state		Full speed mode
	HS (high speed main) mode	1 MHz to 24 MHz	Full speed mode
	LS (low speed main) mode Note	1 MHz to 8 MHz	Wide voltage mode
2.4 V ≤ V_{DD} < 2.7 V	Blank state		Full speed mode
	HS (high speed main) mode	1 MHz to 16 MHz	Full speed mode
	LS (low speed main) mode Note	1 MHz to 8 MHz	Wide voltage mode
1.8 V ≤ V_{DD} < 2.4 V Note	Blank state		Wide voltage mode
	LS (low speed main) mode Note	1 MHz to 8 MHz	Wide voltage mode

Note R5F11R only.

Remark 1. Using both the wide voltage mode and full speed mode imposes no restrictions on writing, deletion, or verification.

Remark 2. For details about communication commands, see **34.4.4 Communication commands**.

34.4.3 Selecting communication mode

Communication mode of the RL78 microcontroller as follows.

Table 34 - 6 Communication Modes

Communication Mode	Standard Setting Note 1				Pins Used
	Port	Speed Note 2	Frequency	Multiply Rate	
1-line mode (when flash memory programmer is used, or when external device is used)	UART	115200 bps, 250000 bps, 500000 bps, 1 Mbps	—	—	TOOL0
Dedicated UART (when external device is used)	UART	115200 bps, 250000 bps, 500000 bps, 1 Mbps	—	—	TOOLTxD, TOOLRxD

Note 1. Selection items for Standard settings on GUI of the flash memory programmer.

Note 2. Because factors other than the baud rate error, such as the signal waveform slew, also affect UART communication, thoroughly evaluate the slew as well as the baud rate error.

34.4.4 Communication commands

The RL78 microcontroller executes serial programming through the commands listed in **Table 34 - 7**.

The signals sent from the dedicated flash memory programmer or external device to the RL78 microcontroller are called commands, and programming functions corresponding to the commands are executed. For details, refer to **RL78 Microcontrollers (RL78 Protocol A) Programmer Edition Application Note (R01AN0815)**.

Table 34 - 7 Flash Memory Control Commands

Classification	Command Name	Function
Verify	Verify	Compares the contents of a specified area of the flash memory with data transmitted from the programmer.
Erase	Block Erase	Erases a specified area in the flash memory.
Blank check	Block Blank Check	Checks if a specified block in the flash memory has been correctly erased
Write	Programming	Writes data to a specified area in the flash memory.
Getting information	Silicon Signature	Gets the RL78 microcontroller information (such as the part number, flash memory configuration, and programming firmware version).
	Checksum	Gets the checksum data for a specified area.
Security	Security Set	Sets security information.
	Security Get	Gets security information.
	Security Release	Release setting of prohibition of writing.
Others	Reset	Used to detect synchronization status of communication.
	Baud Rate Set	Sets baud rate when UART communication mode is selected.

Caution Confirm that no data has been written to the write area. Because data cannot be erased after block erase is prohibited, do not write data if the data has not been erased.

Remark Product information (such as product name and firmware version) can be obtained by executing the “Silicon Signature” command.

Tables 34 - 8 and **34 - 9** show signature data list and example of signature data list.

Table 34 - 8 Signature Data List

Field name	Description	Number of transmit data
Device code	The serial number assigned to the device	3 bytes
Device name	Device name (ASCII code)	10 bytes
Code flash memory area last address	Last address of code flash memory area (Sent from lower address. Example. 00000H to 0FFFFH (64 KB) → FFH, FFH, 00H)	3 bytes
Data flash memory area last address	Last address of data flash memory area (Sent from lower address. Example. F1000H to F1FFFH (4 KB) → FFH, 1FH, 0FH)	3 bytes
Firmware version	Version information of firmware for programming (Sent from upper address. Example. From Ver. 1.23 → 01H, 02H, 03H)	3 bytes

Table 34 - 9 Signature Data List

Field name	Description	Number of transmit data	Data (hexadecimal)
Device code	RL78 protocol A	3 bytes	10 00 06
Device name	R5F11NME	10 bytes	52 = “R” 35 = “5” 46 = “F” 31 = “1” 31 = “1” 4E = “N” 4D = “M” 45 = “E” 20 = “ ” 20 = “ ”
Code flash memory area last address	Code flash memory area 00000H to FFFFH (64 KB)	3 bytes	FF FF 00
Data flash memory area last address	Data flash memory area F1000H to F1FFFH (4 KB)	3 bytes	FF 1F 0F
Firmware version	Ver.1.23	3 bytes	01 02 03

34.5 Processing Time for Each Command When PG-FP6 Is in Use (Reference Value)

The following shows the processing time for each command (reference value) when PG-FP6 is used as a dedicated flash memory programmer.

Table 34 - 10 Processing Time for Each Command When PG-FP6 Is in Use (Reference Value)

PG-FP6 Command	Code Flash		
	64 Kbytes	96 Kbytes	128 Kbytes
Erasing	1.5 s	1.5 s	2 s
Writing	2.3 s	2.7 s	3.2 s
Verification	2 s	3 s	3.5 s
Writing after erasing	3 s	4 s	4.5 s

Remark The command processing times (reference values) shown in the table are typical values under the following conditions.
Port: TOOL0 (single-line UART)
Speed: 1,000,000 bps
Mode: Full speed mode (flash operation mode: HS (high speed main) mode)

34.6 Self-Programming

The RL78 microcontroller supports a self-programming function that can be used to rewrite the code flash memory via a user program. Because this function allows a user application to rewrite the code flash memory by using the flash self-programming library, it can be used to upgrade the program in the field.

Caution 1. The self-programming function cannot be used when the CPU operates with the subsystem clock.

Caution 2. To prohibit an interrupt during self-programming, in the same way as in the normal operation mode, execute the flash self-programming library in the state where the IE flag is cleared (0) by the DI instruction. To enable an interrupt, clear (0) the interrupt mask flag to accept in the state where the IE flag is set (1) by the EI instruction, and then execute the self-programming library.

Caution 3. The high-speed on-chip oscillator should be kept operating during self-programming. If it is kept stopping, it should be operated (HIOSTOP = 0). The flash self-programming library should be executed after 30 μs have elapsed.

Remark 1. For details of the self-programming function, refer to **RL78 Microcontroller Self-Programming Library Type01 User's Manual (R01US0050)**.

Remark 2. For details of the time required to execute self-programming, see the notes on use that accompany the flash self-programming library tool.

The self-programming function has two flash memory programming modes; wide voltage mode and full speed mode. Specify the mode that corresponds to the flash operation mode specified in bits CMODE1 and CMODE0 in option byte 000C2H.

Specify the full speed mode when the HS (high speed main) mode is specified. Specify the wide voltage mode when the LS (low speed main) mode is specified.

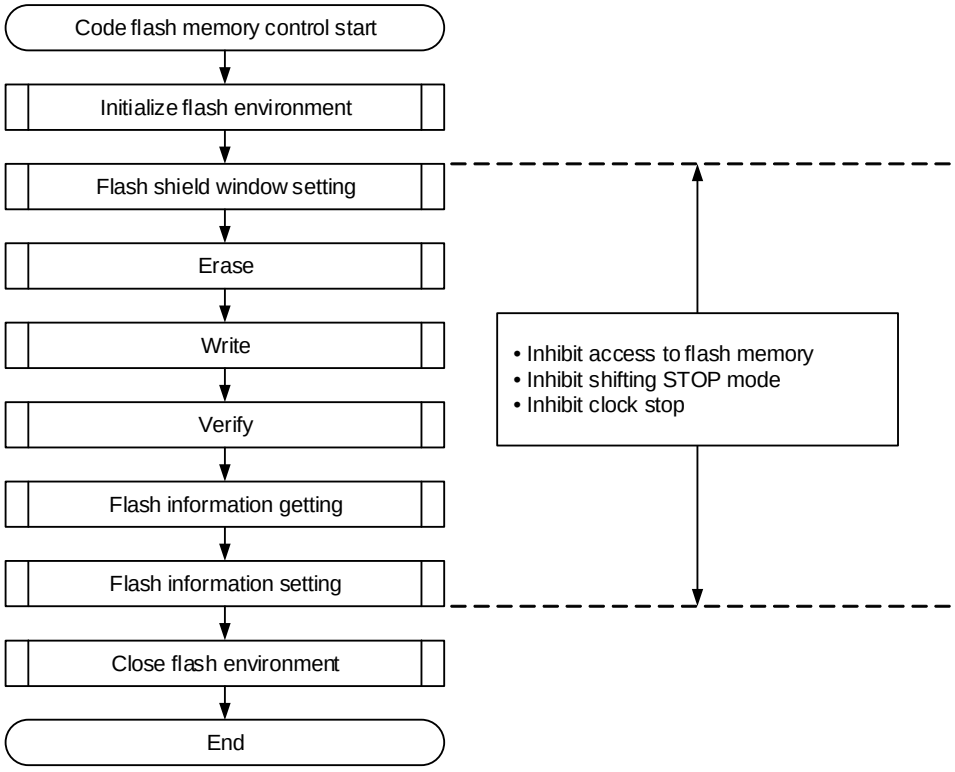
If the argument fsl_flash_voltage_u08 is 00H when the FSL_Init function of the flash self-programming library provided by Renesas Electronics is executed, full speed mode is specified. If the argument is other than 00H, the wide voltage mode is specified.

Remark Using both the wide voltage mode and full speed mode imposes no restrictions on writing, deletion, or verification.

34.6.1 Self-programming procedure

The following figure illustrates a flow for rewriting the code flash memory by using a flash self-programming library.

Figure 34 - 8 Flow of Self-Programming (Rewriting Flash Memory)



34.6.2 Boot swap function

If rewriting the boot area failed by temporary power failure or other reasons, restarting a program by resetting or overwriting is disabled due to data destruction in the boot area.

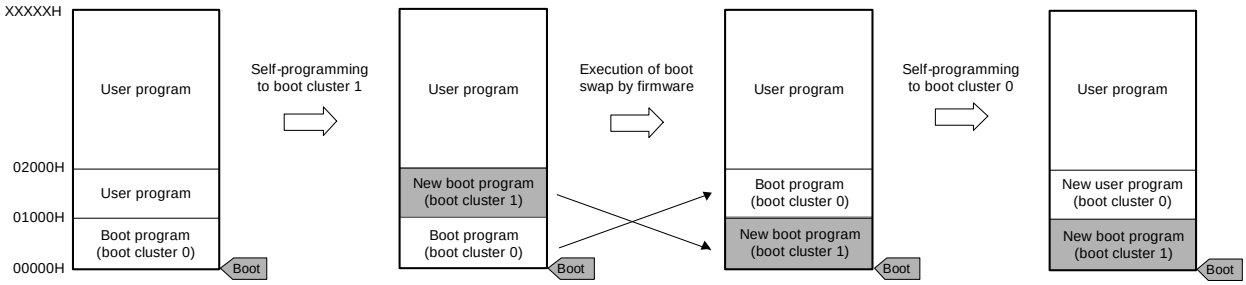
The boot swap function is used to avoid this problem.

Before erasing boot cluster 0 Note, which is a boot area, by self-programming, write a new boot program to boot cluster 1 in advance. When the program has been correctly written to boot cluster 1, swap this boot cluster 1 and boot cluster 0 by using the set information function of the firmware of the RL78 microcontroller, so that boot cluster 1 is used as a boot area. After that, erase or write the original boot program area, boot cluster 0.

As a result, even if a power failure occurs while the boot programming area is being rewritten, the program is executed correctly because it is booted from boot cluster 1 to be swapped when the program is reset and started next.

Note A boot cluster is a 4 KB area and boot clusters 0 and 1 are swapped by the boot swap function.

Figure 34 - 9 Boot Swap Function

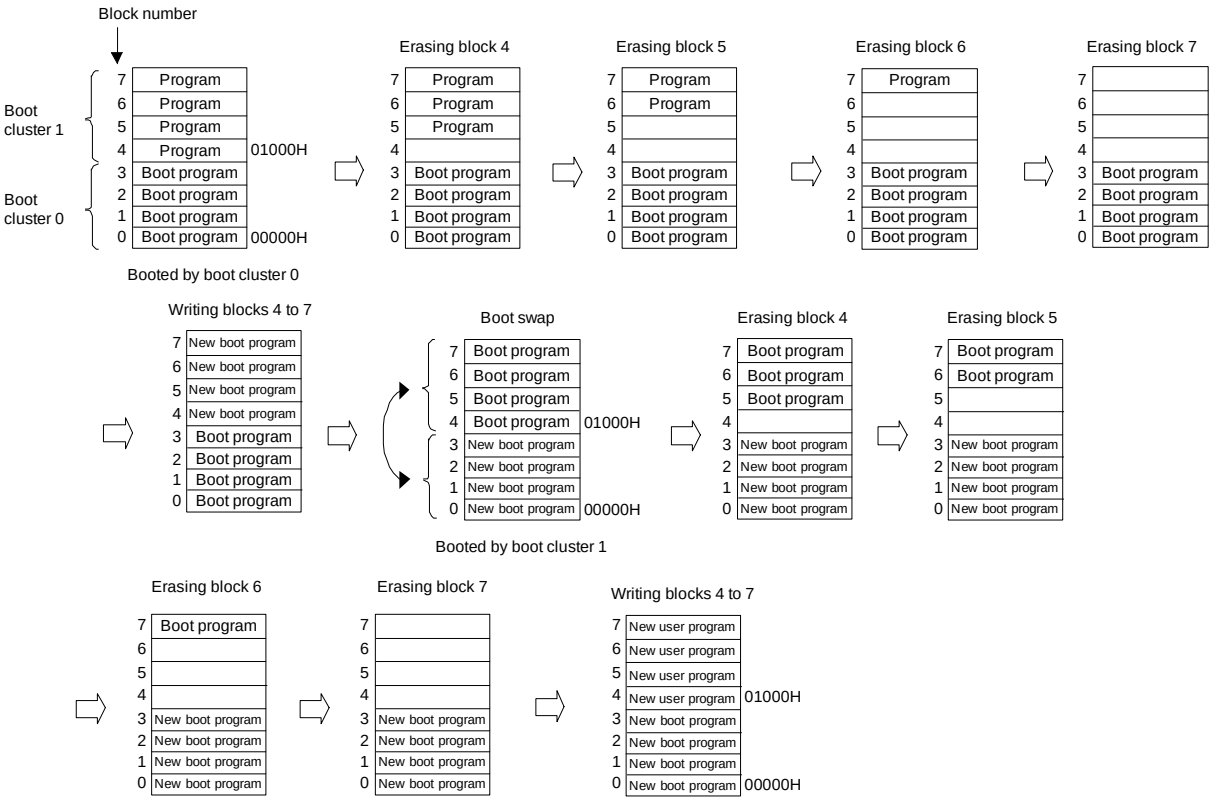


In an example of above figure, it is as follows.

Boot cluster 0: Boot area before boot swap

Boot cluster 1: Boot area after boot swap

Figure 34 - 10 Example of Executing Boot Swapping



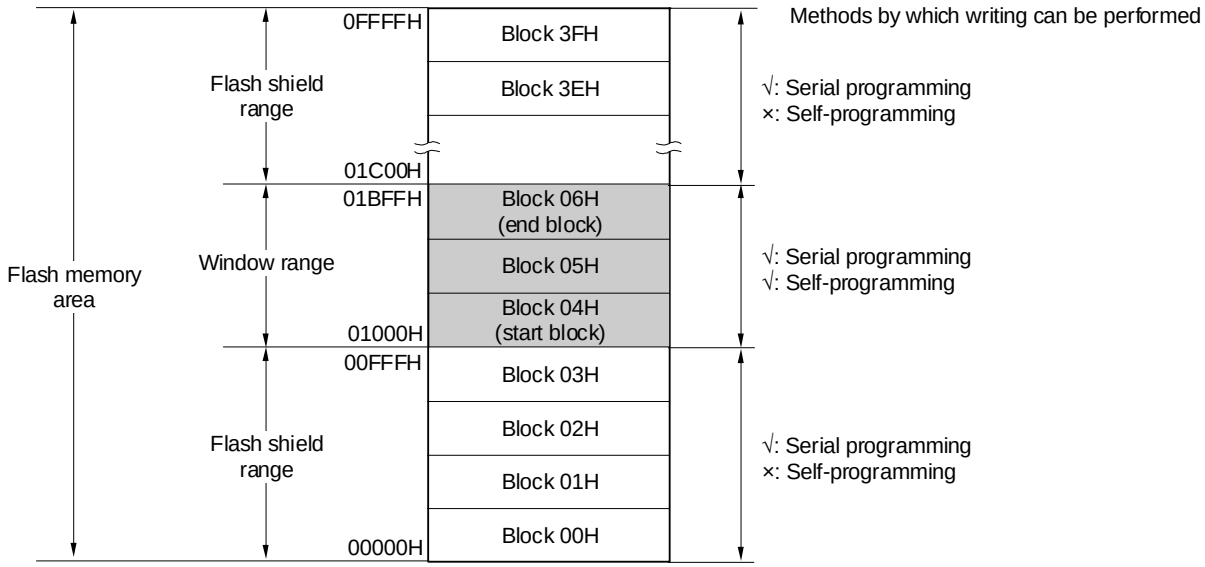
34.6.3 Flash shield window function

The flash shield window function is provided as one of the security functions for self-programming. It disables writing to and erasing areas outside the range specified as a window only during self-programming.

The window range can be set by specifying the start and end blocks. The window range can be set or changed during both serial programming and self-programming.

Writing to and erasing areas outside the window range are disabled during self-programming. During serial programming, however, areas outside the range specified as a window can be written and erased.

Figure 34 - 11 Flash Shield Window Setting Example
(Target Devices: R5F11NME, Start Block: 04H, End Block: 06H)



Caution 1. If the rewrite-prohibited area of the boot cluster 0 overlaps with the flash shield window range, prohibition to rewrite the boot cluster 0 takes priority.

Caution 2. The flash shield window can only be used for the code flash memory (and is not supported for the data flash memory).

Table 34 - 11 Relationship between Flash Shield Window Function Setting/Change Methods and Commands

Programming conditions	Window Range Setting/ Change Methods	Execution Commands	
		Block erase	Write
Self-programming	Specify the starting and ending blocks by the flash self-programming library.	Block erasing is enabled only within the window range.	Writing is enabled only within the range of window range.
Serial programming	Specify the starting and ending blocks on GUI of dedicated flash memory programmer, etc.	Block erasing is enabled also outside the window range.	Writing is enabled also outside the window range.

Remark See **34.7 Security Settings** to prohibit writing/erasing during serial programming.

34.7 Security Settings

The RL78 microcontroller supports a security function that prohibits rewriting the user program written to the internal flash memory, so that the program cannot be changed by an unauthorized person.
The operations shown below can be performed using the Security Set command.

- Disabling block erase
  Execution of the block erase command for a specific block in the flash memory is prohibited during serial programming. However, blocks can be erased by means of self-programming.

- Disabling write
  Execution of the write command for entire blocks in the code flash memory is prohibited during serial programming. However, blocks can be written by means of self-programming.
  After the setting of prohibition of writing is specified, releasing the setting by the Security Release command is enabled by a reset.

- Disabling rewriting boot cluster 0
  Execution of the block erase command and write command on boot cluster 0 (00000H to 00FFFH) in the code flash memory is prohibited by this setting.

The block erase, write commands, and rewriting boot cluster 0 are enabled by the default setting when the flash memory is shipped. Security can be set by serial programming and self-programming. Each security setting can be used in combination.
Table 34 - 12 shows the relationship between the erase and write commands when the RL78 microcontroller security function is enabled.

Caution The security function of the dedicated flash programmer does not support self-programming.

Remark To prohibit writing and erasing during self-programming, use the flash shield window function (see **34.6.3** for detail).

Table 34 - 12 Relationship Between Enabling Security Function and Command

(1) During serial programming

Valid Security	Executed Command	
	Block Erase	Write
Prohibition of block erase	Blocks cannot be erased.	Can be performed. Note
Prohibition of writing	Blocks can be erased.	Cannot be performed.
Prohibition of rewriting boot cluster 0	Boot cluster 0 cannot be erased.	Boot cluster 0 cannot be written.

Note Confirm that no data has been written to the write area. Because data cannot be erased after block erase is prohibited, do not write data if the data has not been erased.

(2) During self-programming

Valid Security	Executed Command	
	Block Erase	Write
Prohibition of block erase	Blocks can be erased.	Can be performed.
Prohibition of writing		
Prohibition of rewriting boot cluster 0	Boot cluster 0 cannot be erased.	Boot cluster 0 cannot be written.

Remark To prohibit writing and erasing during self-programming, use the flash shield window function (see **34.6.3** for detail).

Table 34 - 13 Setting Security in Each Programming Mode

(1) During serial programming

Security	Security Setting	How to Disable Security Setting
Prohibition of block erase	Set via GUI of dedicated flash memory programmer, etc.	Cannot be disabled after set.
Prohibition of writing		Set via GUI of dedicated flash memory programmer, etc.
Prohibition of rewriting boot cluster 0		Cannot be disabled after set.

Caution Releasing the setting of prohibition of writing is enabled only when the security is not set as the block erase prohibition and the boot cluster 0 rewrite prohibition with code flash memory area and data flash memory area being blanks.

(2) Self-programming

Security	Security Setting	How to Disable Security Setting
Prohibition of block erase	Set by using flash self-programming library.	Cannot be disabled after set.
Prohibition of writing		Cannot be disabled during self-programming (set via GUI of dedicated flash memory programmer, etc. during serial programming).
Prohibition of rewriting boot cluster 0		Cannot be disabled after set.

34.8 Data Flash

34.8.1 Data flash overview

An overview of the data flash memory is provided below.

- The user program can rewrite the data flash memory by using the flash data library. For details, refer to **RL78 Family Data Flash Library User's Manual**.
- The data flash memory can also be rewritten to through serial programming using the dedicated flash memory programmer or an external device.
- The data flash can be erased in 1-block (1-Kbyte) units.
- The data flash can be accessed only in 8-bit units.
- The data flash can be directly read by CPU instructions.
- Instructions can be executed from the code flash memory while rewriting the data flash memory (that is, background operation (BGO) is supported).
- Because the data flash memory is an area exclusively used for data, it cannot be used to execute instructions.
- Accessing the data flash memory is not possible while rewriting the code flash memory (during self-programming).
- Manipulating the DFLCTL register is not possible while rewriting the data flash memory.
- Transition to the STOP mode is not possible while rewriting the data flash memory.

Caution 1. The data flash memory is stopped after a reset is canceled. The data flash control register (DFLCTL) must be set up in order to use the data flash memory.

Caution 2. The high-speed on-chip oscillator should be kept operating during data flash rewrite. If it is kept stopping, the high-speed on-chip oscillator clock should be operated (HIOSTOP = 0). The data flash library should be executed after 30 μs have elapsed.

Remark For rewriting the code flash memory via a user program, see **34.6 Self-Programming**.

34.8.2 Register controlling data flash memory

34.8.2.1 Data flash control register (DFLCTL)

This register is used to enable or disable accessing to the data flash.

The DFLCTL register is set by a 1-bit or 8-bit memory manipulation instruction.

Reset input sets this register to 00H.

Figure 34 - 12 Format of Data flash control register (DFLCTL)

Address: F0090H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	<0>
DFLCTL	0	0	0	0	0	0	0	DFLEN

DFLEN	Data flash access control
0	Disables data flash access
1	Enables data flash access

Caution Manipulating the DFLCTL register is not possible while rewriting the data flash memory.

34.8.3 Procedure for accessing data flash memory

The data flash memory is stopped after release from the reset state and is inaccessible (neither readable nor programmable) at that time. To access the data flash, make initial settings according to the following procedure. After initial setting, the data flash can be read through CPU instructions and can be read or rewritten to by using the data flash library.

<1> Write 1 to bit 0 (DFLEN) of the data flash control register (DFLCTL).

<2> Wait for the setup to finish for software timer, etc.

The time setup takes differs for each flash operation mode for the main clock.

<Setup time for each flash operation mode>

- HS (High-speed main): 5 µs
- LS (Low-speed main): 720 ns

<3> After the wait, the data flash memory can be accessed.

Caution 1. Accessing the data flash memory is not possible during the setup time.

Caution 2. Transition to the STOP mode is not possible during the setup time. To enter the STOP mode during the setup time, clear DFLEN to 0 and then execute the STOP instruction.

Caution 3. The high-speed on-chip oscillator should be kept operating during data flash rewrite. If it is kept stopping, the high-speed on-chip oscillator clock should be operated (HIOSTOP = 0). The data flash library should be executed after 30 µs have elapsed.

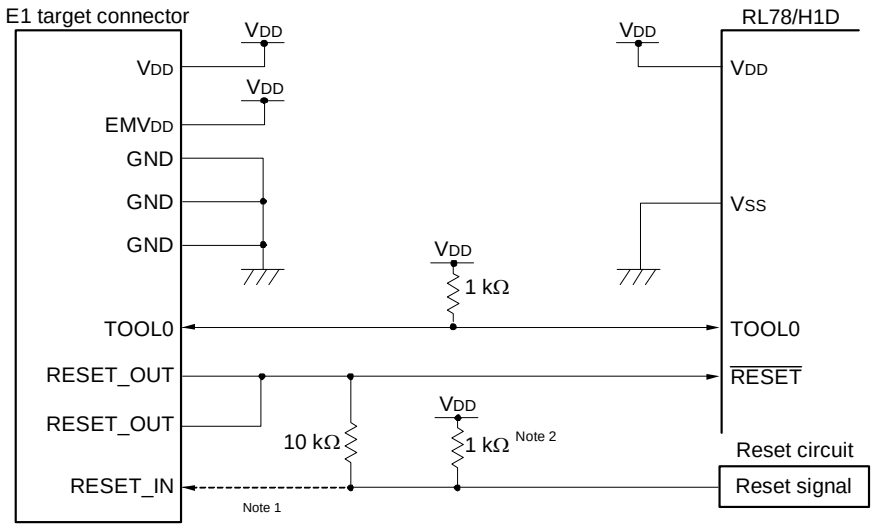
CHAPTER 35 ON-CHIP DEBUG FUNCTION

35.1 Connecting E1 On-chip Debugging Emulator

The RL78 microcontroller uses the V_{DD}, $\overline{RESET}$, TOOL0, and V_{SS} pins to communicate with the host machine via an E1 on-chip debugging emulator. Serial communication is performed by using a single-line UART that uses the TOOL0 pin.

Caution The RL78 microcontroller has an on-chip debug function, which is provided for development and evaluation. Do not use the on-chip debug function in products designated for mass production, because the guaranteed number of rewritable times of the flash memory may be exceeded when this function is used, and product reliability therefore cannot be guaranteed. Renesas Electronics is not liable for problems occurring when the on-chip debug function is used.

Figure 35 - 1 Connection Example of E1 On-chip Debugging Emulator



Note 1. Connecting the dotted line is not necessary during serial programming.

Note 2. If the reset circuit on the target system does not have a buffer and generates a reset signal only with resistors and capacitors, this pull-up resistor is not necessary.

Caution This circuit diagram is assumed that the reset signal outputs from an N-ch O.D. buffer (output resistor: 100 Ω or less)

35.2 On-Chip Debug Security ID

The RL78 microcontroller has an on-chip debug operation control bit in the flash memory at 000C3H (see **CHAPTER 33 OPTION BYTE**) and an on-chip debug security ID setting area at 000C4H to 000CDH, to prevent third parties from reading memory content.

When the boot swap function is used, also set a value that is the same as that of 010C3H and 010C4H to 010CDH in advance, because 000C3H, 000C4H to 000CDH and 010C3H, and 010C4H to 010CDH are switched.

Table 35 - 1 On-Chip Debug Security ID

Address	On-Chip Debug Security ID
000C4H to 000CDH	Any ID code of 10 bytes Note (excluding all FFH)
010C4H to 010CDH	

Note The setting FFFFFFFFFFFFFFFFFFFFH for the ID code is not possible.

35.3 Securing of User Resources

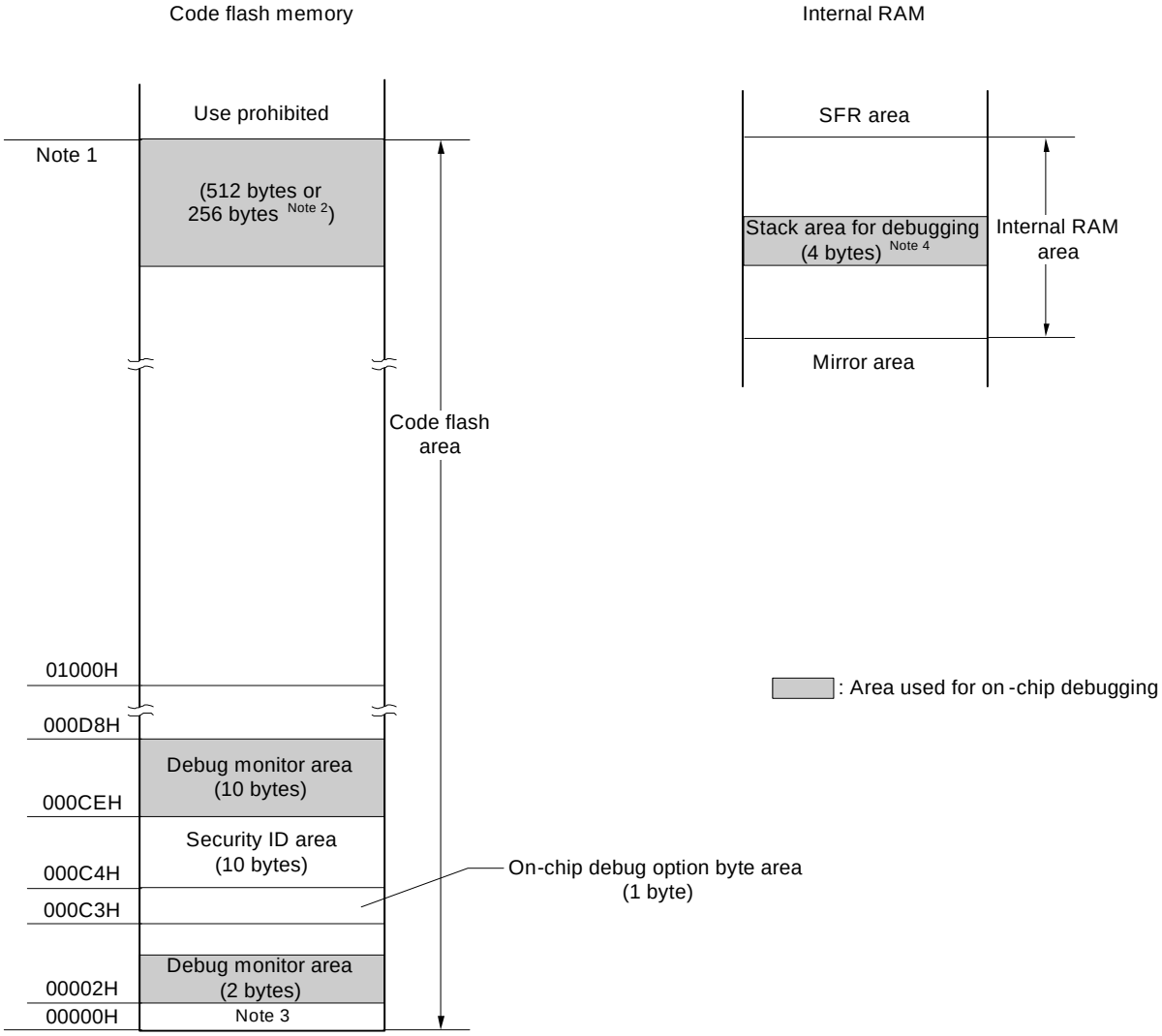
To perform communication between the RL78 microcontroller and E1 on-chip debugging emulator, as well as each debug function, the securing of memory space must be done beforehand.

If Renesas Electronics assembler or compiler is used, the items can be set by using link options.

(1) Securement of memory space

The shaded portions in **Figure 35 - 2** are the areas reserved for placing the debug monitor program, so user programs or data cannot be allocated in these spaces. When using the on-chip debug function, these spaces must be secured so as not to be used by the user program. Moreover, this area must not be rewritten by the user program.

Figure 35 - 2 Memory Spaces Where Debug Monitor Programs Are Allocated



Note 1. Address differs depending on products as follows.

Products (code flash memory capacity)	Address of **Note 1.**
R5F11NME	0FFFFH
R5F11xF (x = NG, NL, NM, PL)	17FFFH
R5F11xG (x = NG, NL, NM, PL), R5F11RMG	1FFFFH

Note 2. When real-time RAM monitor (RRM) function and dynamic memory modification (DMM) function are not used, it is 256 bytes.

Note 3. In debugging, reset vector is rewritten to address allocated to a monitor program.

Note 4. Since this area is allocated immediately before the stack area, the address of this area varies depending on the stack increase and decrease. That is, 4 extra bytes are consumed for the stack area used.
When using self-programming, 12 extra bytes are consumed for the stack area used.

CHAPTER 36 BCD CORRECTION CIRCUIT

36.1 BCD Correction Circuit Function

The result of addition/subtraction of the BCD (binary-coded decimal) code and BCD code can be obtained as BCD code with this circuit.

The decimal correction operation result is obtained by performing addition/subtraction having the A register as the operand and then adding/ subtracting the BCD correction result register (BCDADJ).

36.2 Registers Used by BCD Correction Circuit

The BCD correction circuit uses the following registers.

- BCD correction result register (BCDADJ)

36.2.1 BCD correction result register (BCDADJ)

The BCDADJ register stores correction values for obtaining the add/subtract result as BCD code through add/subtract instructions using the A register as the operand.

The value read from the BCDADJ register varies depending on the value of the A register when it is read and those of the CY and AC flags.

The BCDADJ register is read by an 8-bit memory manipulation instruction.

Reset input sets this register to undefined.

Figure 36 - 1 Format of BCD correction result register (BCDADJ)

Address: F00FEH After reset: Undefined R

Symbol	7	6	5	4	3	2	1	0
BCDADJ								

36.3 BCD Correction Circuit Operation

The basic operation of the BCD correction circuit is as follows.

(1) Addition: Calculating the result of adding a BCD code value and another BCD code value by using a BCD code value

<1> The BCD code value to which addition is performed is stored in the A register.

<2> By adding the value of the A register and the second operand (value of one more BCD code to be added) as are in binary, the binary operation result is stored in the A register and the correction value is stored in the BCD correction result register (BCDADJ).

<3> Decimal correction is performed by adding in binary the value of the A register (addition result in binary) and the BCDADJ register (correction value), and the correction result is stored in the A register and CY flag.

Caution The value read from the BCDADJ register varies depending on the value of the A register when it is read and those of the CY and AC flags. Therefore, execute the instruction <3> after the instruction <2> instead of executing any other instructions. To perform BCD correction in the interrupt enabled state, saving and restoring the A register is required within the interrupt function. PSW (CY flag and AC flag) is restored by the RETI instruction.

An example is shown below.

Examples 1: 99 + 89 = 188

Instruction			A Register	CY Flag	AC Flag	BCDADJ Register
MOV	A, #99H	; <1>	99H	—	—	—
ADD	A, #89H	; <2>	22H	1	1	66H
ADD	A, !BCDADJ	; <3>	88H	1	0	—

Examples 2: 85 + 15 = 100

Instruction			A Register	CY Flag	AC Flag	BCDADJ Register
MOV	A, #85H	; <1>	85H	—	—	—
ADD	A, #15H	; <2>	9AH	0	0	66H
ADD	A, !BCDADJ	; <3>	00H	1	1	—

Examples 3: 80 + 80 = 160

Instruction			A Register	CY Flag	AC Flag	BCDADJ Register
MOV	A, #80H	; <1>	80H	—	—	—
ADD	A, #80H	; <2>	00H	1	0	60H
ADD	A, !BCDADJ	; <3>	60H	1	0	—

(2) Subtraction: Calculating the result of subtracting a BCD code value from another BCD code value by using a BCD code value

<1> The BCD code value from which subtraction is performed is stored in the A register.

<2> By subtracting the value of the second operand (value of BCD code to be subtracted) from the A register as is in binary, the calculation result in binary is stored in the A register, and the correction value is stored in the BCD correction result register (BCDADJ).

<3> Decimal correction is performed by subtracting the value of the BCDADJ register (correction value) from the A register (subtraction result in binary) in binary, and the correction result is stored in the A register and CY flag.

Caution The value read from the BCDADJ register varies depending on the value of the A register when it is read and those of the CY and AC flags. Therefore, execute the instruction <3> after the instruction <2> instead of executing any other instructions. To perform BCD correction in the interrupt enabled state, saving and restoring the A register is required within the interrupt function. PSW (CY flag and AC flag) is restored by the RETI instruction.

An example is shown below.

Example: 91 ─ 52 = 39

Instruction			A Register	CY Flag	AC Flag	BCDADJ Register
MOV	A, #91H	; <1>	91H	—	—	—
SUB	A, #52H	; <2>	3FH	0	1	06H
SUB	A, !BCDADJ	; <3>	39H	0	0	—

CHAPTER 37 INSTRUCTION SET

This chapter lists the instructions in the RL78 microcontroller instruction set. For details of each operation and operation code, refer to the separate document **RL78 Family User's Manual Software (R01US0015)**.

37.1 Conventions Used in Operation List

37.1.1 Operand identifiers and specification methods

Operands are described in the “Operand” column of each instruction in accordance with the description method of the instruction operand identifier (refer to the assembler specifications for details). When there are two or more description methods, select one of them. Alphabetic letters in capitals and the symbols, #, !, !!, $, $!, [ ], and ES: are keywords and are described as they are. Each symbol has the following meaning.

- #: Immediate data specification
- !: 16-bit absolute address specification
- !!: 20-bit absolute address specification
- $: 8-bit relative address specification
- $!: 16-bit relative address specification
- [ ]: Indirect address specification
- ES:: Extension address specification

In the case of immediate data, describe an appropriate numeric value or a label. When using a label, be sure to describe the #, !, !!, $, $!, [ ], and ES: symbols.
For operand register identifiers, r and rp, either function names (X, A, C, etc.) or absolute names (names in parentheses in the table below, R0, R1, R2, etc.) can be used for description.

Table 37 - 1 Operand Identifiers and Specification Methods

Identifier	Description Method
r rp sfr sfrp	X (R0), A (R1), C (R2), B (R3), E (R4), D (R5), L (R6), H (R7) AX (RP0), BC (RP1), DE (RP2), HL (RP3) Special-function register symbol (SFR symbol) FFF00H to FFFFFH Special-function register symbols (16-bit manipulatable SFR symbol. Even addresses only Note) FFF00H to FFFFFH
saddr saddrp	FFE20H to FFF1FH Immediate data or labels FFE20H to FFF1FH Immediate data or labels (even addresses only Note)
addr20 addr16 addr5	00000H to FFFFFH Immediate data or labels 0000H to FFFFH Immediate data or labels (only even addresses for 16-bit data transfer instructions Note) 0080H to 00BFH Immediate data or labels (even addresses only)
word byte bit	16-bit immediate data or label 8-bit immediate data or label 3-bit immediate data or label
RBn	RB0 to RB3

Note Bit 0 = 0 when an odd address is specified.

Remark The special function registers can be described to operand sfr as symbols. See **Table 3 - 5 SFR List** for the symbols of the special function registers. The extended special function registers can be described to operand !addr16 as symbols. See **Table 3 - 6 Extended SFR (2nd SFR) List** for the symbols of the extended special function registers.

37.1.2 Description of operation column

The operation when the instruction is executed is shown in the “Operation” column using the following symbols.

Table 37 - 2 Symbols in “Operation” Column

Symbol	Function
A	A register; 8-bit accumulator
X	X register
B	B register
C	C register
D	D register
E	E register
H	H register
L	L register
ES	ES register
CS	CS register
AX	AX register pair; 16-bit accumulator
BC	BC register pair
DE	DE register pair
HL	HL register pair
PC	Program counter
SP	Stack pointer
PSW	Program status word
CY	Carry flag
AC	Auxiliary carry flag
Z	Zero flag
RBS	Register bank select flag
IE	Interrupt request enable flag
()	Memory contents indicated by address or register contents in parentheses
X_H, X_L X_S, X_H, X_L	16-bit registers: X_H = higher 8 bits, X_L = lower 8 bits 20-bit registers: X_S = (bits 19 to 16), X_H = (bits 15 to 8), X_L = (bits 7 to 0)
∧	Logical product (AND)
∨	Logical sum (OR)
∨̲	Exclusive logical sum (exclusive OR)
—	Inverted data
addr5	16-bit immediate data (even addresses only in 0080H to 00BFH)
addr16	16-bit immediate data
addr20	20-bit immediate data
jdisp8	Signed 8-bit data (displacement value)
jdisp16	Signed 16-bit data (displacement value)

37.1.3 Description of flag operation column

The change of the flag value when the instruction is executed is shown in the “Flag” column using the following symbols.

Table 37 - 3 Symbols in “Flag” Column

Symbol	Change of Flag Value
(Blank)	Unchanged
0	Cleared to 0
1	Set to 1
×	Set/cleared according to the result
R	Previously saved value is restored

37.1.4 PREFIX instruction

Instructions with “ES:” have a PREFIX operation code as a prefix to extend the accessible data area to the 1 MB space (00000H to FFFFFH), by adding the ES register value to the 64 KB space from F0000H to FFFFFH. When a PREFIX operation code is attached as a prefix to the target instruction, only one instruction immediately after the PREFIX operation code is executed as the addresses with the ES register value added.

A interrupt and DTC transfer are not acknowledged between a PREFIX instruction code and the instruction immediately after.

Table 37 - 4 Use Example of PREFIX Operation Code

Instruction	Opcode				
	1	2	3	4	5
MOV !addr16, #byte	CFH	!addr16		#byte	—
MOV ES:!addr16, #byte	11H	CFH	!addr16		#byte
MOV A, [HL]	8BH	—	—	—	—
MOV A, ES: [HL]	11H	8BH	—	—	—

Caution Set the ES register value with MOV ES, A, etc., before executing the PREFIX instruction.

37.2 Operation List

Table 37 - 5 Operation List (1/18)

Instruction Group	Mnemonic	Operands	Bytes	Clocks		Clocks	Flag		
				Note 1	Note 2		Z	AC	CY
8-bit data transfer	MOV	r, #byte	2	1	—	r ← byte			
		PSW, #byte	3	3	—	PSW ← byte	×	×	×
		CS, #byte	3	1	—	CS ← byte			
		ES, #byte	2	1	—	ES ← byte			
		!addr16, #byte	4	1	—	(addr16) ← byte			
		ES:!addr16, #byte	5	2	—	(ES, addr16) ← byte			
		saddr, #byte	3	1	—	(saddr) ← byte			
		sfr, #byte	3	1	—	sfr ← byte			
		[DE+byte], #byte	3	1	—	(DE + byte) ← byte			
		ES:[DE+byte], #byte	4	2	—	((ES, DE) + byte) ← byte			
		[HL+byte], #byte	3	1	—	(HL + byte) ← byte			
		ES:[HL+byte], #byte	4	2	—	((ES, HL) + byte) ← byte			
		[SP+byte], #byte	3	1	—	(SP + byte) ← byte			
		word[B], #byte	4	1	—	(B + word) ← byte			
		ES:word[B], #byte	5	2	—	((ES, B) + word) ← byte			
		word[C], #byte	4	1	—	(C+word) ← byte			
		ES:word[C], #byte	5	2	—	((ES, C) + word) ← byte			
		word[BC], #byte	4	1	—	(BC+word) ← byte			
		ES:word[BC], #byte	5	2	—	((ES, BC) + word) ← byte			
		A, r Note 3	1	1	—	A ← r			
		r, A Note 3	1	1	—	r ← A			
		A, PSW	2	1	—	A ← PSW			
		PSW, A	2	3	—	PSW ← A	×	×	×
		A, CS	2	1	—	A ← CS			
		CS, A	2	1	—	CS ← A			
		A, ES	2	1	—	A ← ES			
		ES, A	2	1	—	ES ← A			
		A, !addr16	3	1	4	A ← (addr16)			
		A, ES:!addr16	4	2	5	A ← (ES, addr16)			
		!addr16, A	3	1	—	(addr16) ← A			
		ES:!addr16, A	4	2	—	(ES, addr16) ← A			
		A, saddr	2	1	—	A ← (saddr)			
		saddr, A	2	1	—	(saddr) ← A			

Note 1. Number of CPU clocks (f_{CLK}) when the internal RAM area, SFR area, or extended SFR area is accessed, or when no data is accessed.

Note 2. Number of CPU clocks (f_{CLK}) when the code flash memory is accessed, or when the data flash memory is accessed by an 8-bit instruction.

Note 3. Except r = A

Remark Number of clock is when program exists in the internal ROM (flash memory) area. If fetching the instruction from the internal RAM area, the number becomes double number plus 3 clocks at a maximum.

Table 37 - 6 Operation List (2/18)

Instruction Group	Mnemonic	Operands	Bytes	Clocks		Clocks	Flag		
				Note 1	Note 2		Z	AC	CY
8-bit data transfer	MOV	A, sfr	2	1	—	A ← sfr			
		sfr, A	2	1	—	sfr ← A			
		A, [DE]	1	1	4	A ← (DE)			
		[DE], A	1	1	—	(DE) ← A			
		A, ES:[DE]	2	2	5	A ← (ES, DE)			
		ES:[DE], A	2	2	—	(ES, DE) ← A			
		A, [HL]	1	1	4	A ← (HL)			
		[HL], A	1	1	—	(HL) ← A			
		A, ES:[HL]	2	2	5	A ← (ES, HL)			
		ES:[HL], A	2	2	—	(ES, HL) ← A			
		A, [DE+byte]	2	1	4	A ← (DE + byte)			
		[DE+byte], A	2	1	—	(DE + byte) ← A			
		A, ES:[DE+byte]	3	2	5	A ← ((ES, DE) + byte)			
		ES:[DE+byte], A	3	2	—	((ES, DE) + byte ← A			
		A, [HL+byte]	2	1	4	A ← (HL + byte)			
		[HL+byte], A	2	1	—	(HL + byte) ← A			
		A, ES:[HL+byte]	3	2	5	A ← ((ES, HL) + byte)			
		ES:[HL+byte], A	3	2	—	((ES, HL) + byte) ← A			
		A, [SP+byte]	2	1	—	A ← (SP + byte)			
		[SP+byte], A	2	1	—	(SP + byte) ← A			
		A, word[B]	3	1	4	A ← (B + word)			
		word[B], A	3	1	—	(B + word) ← A			
		A, ES:word[B]	4	2	5	A ← ((ES, B) + word)			
		ES:word[B], A	4	2	—	((ES, B) + word) ← A			
		A, word[C]	3	1	4	A ← (C + word)			
		word[C], A	3	1	—	(C + word) ← A			
		A, ES:word[C]	4	2	5	A ← ((ES, C) + word)			
		ES:word[C], A	4	2	—	((ES, C) + word) ← A			
		A, word[BC]	3	1	4	A ← (BC + word)			
		word[BC], A	3	1	—	(BC + word) ← A			
		A, ES:word[BC]	4	2	5	A ← ((ES, BC) + word)			
		ES:word[BC], A	4	2	—	((ES, BC) + word) ← A			

Note 1. Number of CPU clocks (f_{CLK}) when the internal RAM area, SFR area, or extended SFR area is accessed, or when no data is accessed.

Note 2. Number of CPU clocks (f_{CLK}) when the code flash memory is accessed, or when the data flash memory is accessed by an 8-bit instruction.

Remark Number of clock is when program exists in the internal ROM (flash memory) area. If fetching the instruction from the internal RAM area, the number becomes double number plus 3 clocks at a maximum.

Table 37 - 7 Operation List (3/18)

Instruction Group	Mnemonic	Operands	Bytes	Clocks		Clocks	Flag		
				Note 1	Note 2		Z	AC	CY
8-bit data transfer	MOV	A, [HL+B]	2	1	4	A ← (HL + B)			
		[HL+B], A	2	1	—	(HL + B) ← A			
		A, ES:[HL+B]	3	2	5	A ← ((ES, HL) + B)			
		ES:[HL+B], A	3	2	—	((ES, HL) + B) ← A			
		A, [HL+C]	2	1	4	A ← (HL + C)			
		[HL+C], A	2	1	—	(HL + C) ← A			
		A, ES:[HL+C]	3	2	5	A ← ((ES, HL) + C)			
		ES:[HL+C], A	3	2	—	((ES, HL) + C) ← A			
		X, !addr16	3	1	4	X ← (addr16)			
		X, ES:!addr16	4	2	5	X ← (ES, addr16)			
		X, saddr	2	1	—	X ← (saddr)			
		B, !addr16	3	1	4	B ← (addr16)			
		B, ES:!addr16	4	2	5	B ← (ES, addr16)			
		B, saddr	2	1	—	B ← (saddr)			
		C, !addr16	3	1	4	C ← (addr16)			
		C, ES:!addr16	4	2	5	C ← (ES, addr16)			
		C, saddr	2	1	—	C ← (saddr)			
		ES, saddr	3	1	—	ES ← (saddr)			
	XCH	A, r Note 3	1 (r = X) 2 (other than r = X)	1	—	A ←→ r			
		A, !addr16	4	2	—	A ←→ (addr16)			
		A, ES:!addr16	5	3	—	A ←→ (ES, addr16)			
		A, saddr	3	2	—	A ←→ (saddr)			
		A, sfr	3	2	—	A ←→ sfr			
		A, [DE]	2	2	—	A ←→ (DE)			
		A, ES:[DE]	3	3	—	A ←→ (ES, DE)			
		A, [HL]	2	2	—	A ←→ (HL)			
		A, ES:[HL]	3	3	—	A ←→ (ES, HL)			
		A, [DE+byte]	3	2	—	A ←→ (DE + byte)			
		A, ES:[DE+byte]	4	3	—	A ←→ ((ES, DE) + byte)			
		A, [HL+byte]	3	2	—	A ←→ (HL + byte)			
		A, ES:[HL+byte]	4	3	—	A ←→ ((ES, HL) + byte)			

Note 1. Number of CPU clocks (f_{CLK}) when the internal RAM area, SFR area, or extended SFR area is accessed, or when no data is accessed.

Note 2. Number of CPU clocks (f_{CLK}) when the code flash memory is accessed, or when the data flash memory is accessed by an 8-bit instruction.

Note 3. Except r = A

Remark Number of clock is when program exists in the internal ROM (flash memory) area. If fetching the instruction from the internal RAM area, the number becomes double number plus 3 clocks at a maximum.

Table 37 - 8 Operation List (4/18)

Instruction Group	Mnemonic	Operands	Bytes	Clocks		Clocks	Flag		
				Note 1	Note 2		Z	AC	CY
8-bit data transfer	XCH	A, [HL+B]	2	2	—	A ←→ (HL + B)			
		A, ES:[HL+B]	3	3	—	A ←→ ((ES, HL) + B)			
		A, [HL+C]	2	2	—	A ←→ (HL + C)			
		A, ES:[HL+C]	3	3	—	A ←→ ((ES, HL) + C)			
	ONEB	A	1	1	—	A ← 01H			
		X	1	1	—	X ← 01H			
		B	1	1	—	B ← 01H			
		C	1	1	—	C ← 01H			
		!addr16	3	1	—	(addr16) ← 01H			
		ES:!addr16	4	2	—	(ES, addr16) ← 01H			
		saddr	2	1	—	(saddr) ← 01H			
	CLRB	A	1	1	—	A ← 00H			
		X	1	1	—	X ← 00H			
		B	1	1	—	B ← 00H			
		C	1	1	—	C ← 00H			
		!addr16	3	1	—	(addr16) ← 00H			
		ES:!addr16	4	2	—	(ES,addr16) ← 00H			
		saddr	2	1	—	(saddr) ← 00H			
	MOVS	[HL+byte], X	3	1	—	(HL + byte) ← X	×		×
		ES:[HL+byte], X	4	2	—	(ES, HL + byte) ← X	×		×
16-bit data transfer	MOVW	rp, #word	3	1	—	rp ← word			
		saddrp, #word	4	1	—	(saddrp) ← word			
		sfrp, #word	4	1	—	sfrp ← word			
		AX, rp Note 3	1	1	—	AX ← rp			
		rp, AX Note 3	1	1	—	rp ← AX			
		AX, !addr16	3	1	4	AX ← (addr16)			
		!addr16, AX	3	1	—	(addr16) ← AX			
		AX, ES:!addr16	4	2	5	AX ← (ES, addr16)			
		ES:!addr16, AX	4	2	—	(ES, addr16) ← AX			
		AX, saddrp	2	1	—	AX ← (saddrp)			
		saddrp, AX	2	1	—	(saddrp) ← AX			
		AX, sfrp	2	1	—	AX ← sfrp			
		sfrp, AX	2	1	—	sfrp ← AX			

Note 1. Number of CPU clocks (f_{CLK}) when the internal RAM area, SFR area, or extended SFR area is accessed, or when no data is accessed.

Note 2. Number of CPU clocks (f_{CLK}) when the code flash memory is accessed, or when the data flash memory is accessed by an 8-bit instruction.

Note 3. Except rp = AX

Remark Number of clock is when program exists in the internal ROM (flash memory) area. If fetching the instruction from the internal RAM area, the number becomes double number plus 3 clocks at a maximum.

Table 37 - 9 Operation List (5/18)

Instruction Group	Mnemonic	Operands	Bytes	Clocks		Clocks	Flag		
				Note 1	Note 2		Z	AC	CY
16-bit data transfer	MOVW	AX, [DE]	1	1	4	AX ← (DE)			
		[DE], AX	1	1	—	(DE) ← AX			
		AX, ES:[DE]	2	2	5	AX ← (ES, DE)			
		ES:[DE], AX	2	2	—	(ES, DE) ← AX			
		AX, [HL]	1	1	4	AX ← (HL)			
		[HL], AX	1	1	—	(HL) ← AX			
		AX, ES:[HL]	2	2	5	AX ← (ES, HL)			
		ES:[HL], AX	2	2	—	(ES, HL) ← AX			
		AX, [DE+byte]	2	1	4	AX ← (DE + byte)			
		[DE+byte], AX	2	1	—	(DE + byte) ← AX			
		AX, ES:[DE+byte]	3	2	5	AX ← ((ES, DE) + byte)			
		ES:[DE+byte], AX	3	2	—	((ES, DE) + byte) ← AX			
		AX, [HL+byte]	2	1	4	AX ← (HL + byte)			
		[HL+byte], AX	2	1	—	(HL + byte) ← AX			
		AX, ES:[HL+byte]	3	2	5	AX ← ((ES, HL) + byte)			
		ES:[HL+byte], AX	3	2	—	((ES, HL) + byte) ← AX			
		AX, [SP+byte]	2	1	—	AX ← (SP + byte)			
		[SP+byte], AX	2	1	—	(SP + byte) ← AX			
		AX, word[B]	3	1	4	AX ← (B + word)			
		word[B], AX	3	1	—	(B + word) ← AX			
		AX, ES:word[B]	4	2	5	AX ← ((ES, B) + word)			
		ES:word[B], AX	4	2	—	((ES, B) + word) ← AX			
		AX, word[C]	3	1	4	AX ← (C + word)			
		word[C], AX	3	1	—	(C + word) ← AX			
		AX, ES:word[C]	4	2	5	AX ← ((ES, C) + word)			
		ES:word[C], AX	4	2	—	((ES, C) + word) ← AX			
		AX, word[BC]	3	1	4	AX ← (BC + word)			
		word[BC], AX	3	1	—	(BC + word) ← AX			
		AX, ES:word[BC]	4	2	5	AX ← ((ES, BC) + word)			
		ES:word[BC], AX	4	2	—	((ES, BC) + word) ← AX			

Note 1. Number of CPU clocks (f_{CLK}) when the internal RAM area, SFR area, or extended SFR area is accessed, or when no data is accessed.

Note 2. Number of CPU clocks (f_{CLK}) when the code flash memory is accessed, or when the data flash memory is accessed by an 8-bit instruction.

Remark Number of clock is when program exists in the internal ROM (flash memory) area. If fetching the instruction from the internal RAM area, the number becomes double number plus 3 clocks at a maximum.

Table 37 - 10 Operation List (6/18)

Instruction Group	Mnemonic	Operands	Bytes	Clocks		Clocks	Flag		
				Note 1	Note 2		Z	AC	CY
16-bit data transfer	MOVW	BC, !addr16	3	1	4	BC ← (addr16)			
		BC, ES:!addr16	4	2	5	BC ← (ES, addr16)			
		DE, !addr16	3	1	4	DE ← (addr16)			
		DE, ES:!addr16	4	2	5	DE ← (ES, addr16)			
		HL, !addr16	3	1	4	HL ← (addr16)			
		HL, ES:!addr16	4	2	5	HL ← (ES, addr16)			
		BC, saddrp	2	1	—	BC ← (saddrp)			
		DE, saddrp	2	1	—	DE ← (saddrp)			
		HL, saddrp	2	1	—	HL ← (saddrp)			
	XCHW	AX, rp Note 3	1	1	—	AX ←→ rp			
	ONEW	AX	1	1	—	AX ← 0001H			
		BC	1	1	—	BC ← 0001H			
	CLRW	AX	1	1	—	AX ← 0000H			
		BC	1	1	—	BC ← 0000H			
8-bit operation	ADD	A, #byte	2	1	—	A, CY← A + byte	×	×	×
		saddr, #byte	3	2	—	(saddr), CY ← (saddr) + byte	×	×	×
		A, r Note 4	2	1	—	A, CY ← A + r	×	×	×
		r, A	2	1	—	r, CY ← r + A	×	×	×
		A, !addr16	3	1	4	A, CY ← A + (addr16)	×	×	×
		A, ES:!addr16	4	2	5	A, CY ← A + (ES, addr16)	×	×	×
		A, saddr	2	1	—	A, C ← A + (saddr)	×	×	×
		A, [HL]	1	1	4	A, CY ← A + (HL)	×	×	×
		A, ES:[HL]	2	2	5	A,CY ← A + (ES, HL)	×	×	×
		A, [HL+byte]	2	1	4	A, CY ← A + (HL + byte)	×	×	×
		A, ES:[HL+byte]	3	2	5	A,CY ← A + ((ES, HL) + byte)	×	×	×
		A, [HL+B]	2	1	4	A, CY ← A + (HL + B)	×	×	×
		A, ES:[HL+B]	3	2	5	A,CY ← A + ((ES, HL) + B)	×	×	×
		A, [HL+C]	2	1	4	A, CY ← A + (HL + C)	×	×	×
		A, ES:[HL+C]	3	2	5	A,CY ← A + ((ES, HL) + C)	×	×	×

Note 1. Number of CPU clocks (f_{CLK}) when the internal RAM area, SFR area, or extended SFR area is accessed, or when no data is accessed.

Note 2. Number of CPU clocks (f_{CLK}) when the code flash memory is accessed, or when the data flash memory is accessed by an 8-bit instruction.

Note 3. Except rp = AX

Note 4. Except r = A

Remark Number of clock is when program exists in the internal ROM (flash memory) area. If fetching the instruction from the internal RAM area, the number becomes double number plus 3 clocks at a maximum.

Table 37 - 11 Operation List (7/18)

Instruction Group	Mnemonic	Operands	Bytes	Clocks		Clocks	Flag		
				Note 1	Note 2		Z	AC	CY
8-bit operation	ADDC	A, #byte	2	1	—	A, CY ← A + byte + CY	×	×	×
		saddr, #byte	3	2	—	(saddr), CY ← (saddr) + byte + CY	×	×	×
		A, rv Note 3	2	1	—	A, CY ← A + r + CY	×	×	×
		r, A	2	1	—	r, CY ← r + A + CY	×	×	×
		A, !addr16	3	1	4	A, CY ← A + (addr16) + CY	×	×	×
		A, ES:!addr16	4	2	5	A, CY ← A + (ES, addr16) + CY	×	×	×
		A, saddr	2	1	—	A, CY ← A + (saddr) + CY	×	×	×
		A, [HL]	1	1	4	A, CY ← A + (HL) + CY	×	×	×
		A, ES:[HL]	2	2	5	A,CY ← A + (ES, HL) + CY	×	×	×
		A, [HL+byte]	2	1	4	A, CY ← A + (HL + byte) + CY	×	×	×
		A, ES:[HL+byte]	3	2	5	A,CY ← A + ((ES, HL) + byte) + CY	×	×	×
		A, [HL+B]	2	1	4	A, CY ← A + (HL + B) + CY	×	×	×
		A, ES:[HL+B]	3	2	5	A,CY ← A + ((ES, HL) + B) + CY	×	×	×
		A, [HL+C]	2	1	4	A, CY ← A + (HL + C) + CY	×	×	×
		A, ES:[HL+C]	3	2	5	A,CY ← A + ((ES, HL) + C) + CY	×	×	×
	SUB	A, #byte	2	1	—	A, CY ← A - byte	×	×	×
		saddr, #byte	3	2	—	(saddr), CY ← (saddr) - byte	×	×	×
		A, r Note 3	2	1	—	A, CY ← A - r	×	×	×
		r, A	2	1	—	r, CY ← r - A	×	×	×
		A, !addr16	3	1	4	A, CY ← A - (addr16)	×	×	×
		A, ES:!addr16	4	2	5	A, CY ← A - (ES, addr16)	×	×	×
		A, saddr	2	1	—	A, CY ← A - (saddr)	×	×	×
		A, [HL]	1	1	4	A, CY ← A - (HL)	×	×	×
		A, ES:[HL]	2	2	5	A,CY ← A - (ES, HL)	×	×	×
		A, [HL+byte]	2	1	4	A, CY ← A - (HL + byte)	×	×	×
		A, ES:[HL+byte]	3	2	5	A,CY ← A - ((ES, HL) + byte)	×	×	×
		A, [HL+B]	2	1	4	A, CY ← A - (HL + B)	×	×	×
		A, ES:[HL+B]	3	2	5	A,CY ← A - ((ES, HL) + B)	×	×	×
		A, [HL+C]	2	1	4	A, CY ← A - (HL + C)	×	×	×
		A, ES:[HL+C]	3	2	5	A,CY ← A - ((ES, HL) + C)	×	×	×

Note 1. Number of CPU clocks (f_{CLK}) when the internal RAM area, SFR area, or extended SFR area is accessed, or when no data is accessed.

Note 2. Number of CPU clocks (f_{CLK}) when the code flash memory is accessed, or when the data flash memory is accessed by an 8-bit instruction.

Note 3. Except r = A

Remark Number of clock is when program exists in the internal ROM (flash memory) area. If fetching the instruction from the internal RAM area, the number becomes double number plus 3 clocks at a maximum.

Table 37 - 12 Operation List (8/18)

Instruction Group	Mnemonic	Operands	Bytes	Clocks		Clocks	Flag		
				Note 1	Note 2		Z	AC	CY
8-bit operation	SUBC	A, #byte	2	1	—	A, CY ← A - byte - CY	×	×	×
		saddr, #byte	3	2	—	(saddr), CY ← (saddr) - byte - CY	×	×	×
		A, r Note 3	2	1	—	A, CY ← A - r - CY	×	×	×
		r, A	2	1	—	r, CY ← r - A - CY	×	×	×
		A, !addr16	3	1	4	A, CY ← A - (addr16) - CY	×	×	×
		A, ES:!addr16	4	2	5	A, CY ← A - (ES, addr16) - CY	×	×	×
		A, saddr	2	1	—	A, CY ← A - (saddr) - CY	×	×	×
		A, [HL]	1	1	4	A, CY ← A - (HL) - CY	×	×	×
		A, ES:[HL]	2	2	5	A,CY ← A - (ES, HL) - CY	×	×	×
		A, [HL+byte]	2	1	4	A, CY ← A - (HL + byte) - CY	×	×	×
		A, ES:[HL+byte]	3	2	5	A,CY ← A - ((ES, HL) + byte) - CY	×	×	×
		A, [HL+B]	2	1	4	A, CY ← A - (HL + B) - CY	×	×	×
		A, ES:[HL+B]	3	2	5	A,CY ← A - ((ES, HL) + B) - CY	×	×	×
		A, [HL+C]	2	1	4	A, CY ← A - (HL + C) - CY	×	×	×
		A, ES:[HL+C]	3	2	5	A, CY ← A - ((ES:HL) + C) - CY	×	×	×
	AND	A, #byte	2	1	—	A ← A ∧ byte	×		
		saddr, #byte	3	2	—	(saddr) ← (saddr) ∧ byte	×		
		A, r Note 3	2	1	—	A ← A ∧ r	×		
		r, A	2	1	—	R ← r ∧ A	×		
		A, !addr16	3	1	4	A ← A ∧ (addr16)	×		
		A, ES:!addr16	4	2	5	A ← A ∧ (ES:addr16)	×		
		A, saddr	2	1	—	A ← A ∧ (saddr)	×		
		A, [HL]	1	1	4	A ← A ∧ (HL)	×		
		A, ES:[HL]	2	2	5	A ← A ∧ (ES:HL)	×		
		A, [HL+byte]	2	1	4	A ← A ∧ (HL + byte)	×		
		A, ES:[HL+byte]	3	2	5	A ← A ∧ ((ES:HL) + byte)	×		
		A, [HL+B]	2	1	4	A ← A ∧ (HL + B)	×		
		A, ES:[HL+B]	3	2	5	A ← A ∧ ((ES:HL) + B)	×		
		A, [HL+C]	2	1	4	A ← A ∧ (HL + C)	×		
		A, ES:[HL+C]	3	2	5	A ← A ∧ ((ES:HL) + C)	×		

Note 1. Number of CPU clocks (f_{CLK}) when the internal RAM area, SFR area, or extended SFR area is accessed, or when no data is accessed.

Note 2. Number of CPU clocks (f_{CLK}) when the code flash memory is accessed, or when the data flash memory is accessed by an 8-bit instruction.

Note 3. Except r = A

Remark Number of clock is when program exists in the internal ROM (flash memory) area. If fetching the instruction from the internal RAM area, the number becomes double number plus 3 clocks at a maximum.

Table 37 - 13 Operation List (9/18)

Instruction Group	Mnemonic	Operands	Bytes	Clocks		Clocks	Flag		
				Note 1	Note 2		Z	AC	CY
8-bit operation	OR	A, #byte	2	1	—	A ← A ∨ byte	×		
		saddr, #byte	3	2	—	(saddr) ← (saddr) ∨ byte	×		
		A, r Note 3	2	1	—	A ← A ∨ r	×		
		r, A	2	1	—	r ← r ∨ A	×		
		A, !addr16	3	1	4	A ← A ∨ (addr16)	×		
		A, ES:!addr16	4	2	5	A ← A ∨ (ES:addr16)	×		
		A, saddr	2	1	—	A ← A ∨ (saddr)	×		
		A, [HL]	1	1	4	A ← A ∨ (HL)	×		
		A, ES:[HL]	2	2	5	A ← A ∨ (ES:HL)	×		
		A, [HL+byte]	2	1	4	A ← A ∨ (HL + byte)	×		
		A, ES:[HL+byte]	3	2	5	A ← A ∨ ((ES:HL) + byte)	×		
		A, [HL+B]	2	1	4	A ← A ∨ (HL + B)	×		
		A, ES:[HL+B]	3	2	5	A ← A ∨ ((ES:HL) + B)	×		
		A, [HL+C]	2	1	4	A ← A ∨ (HL + C)	×		
		A, ES:[HL+C]	3	2	5	A ← A ∨ ((ES:HL) + C)	×		
	XOR	A, #byte	2	1	—	A ← A ⩛ byte	×		
		saddr, #byte	3	2	—	(saddr) ← (saddr) ⩛ byte	×		
		A, r Note 3	2	1	—	A ← A ⩛ r	×		
		r, A	2	1	—	r ← r ⩛ A	×		
		A, !addr16	3	1	4	A ← A ⩛ (addr16)	×		
		A, ES:!addr16	4	2	5	A ← A ⩛ (ES:addr16)	×		
		A, saddr	2	1	—	A ← A ⩛ (saddr)	×		
		A, [HL]	1	1	4	A ← A ⩛ (HL)	×		
		A, ES:[HL]	2	2	5	A ← A ⩛ (ES:HL)	×		
		A, [HL+byte]	2	1	4	A ← A ⩛ (HL + byte)	×		
		A, ES:[HL+byte]	3	2	5	A ← A ⩛ ((ES:HL) + byte)	×		
		A, [HL+B]	2	1	4	A ← A ⩛ (HL + B)	×		
		A, ES:[HL+B]	3	2	5	A ← A ⩛ ((ES:HL) + B)	×		
		A, [HL+C]	2	1	4	A ← A ⩛ (HL + C)	×		
		A, ES:[HL+C]	3	2	5	A ← A ⩛ ((ES:HL) + C)	×		

Note 1. Number of CPU clocks (f_{CLK}) when the internal RAM area, SFR area, or extended SFR area is accessed, or when no data is accessed.

Note 2. Number of CPU clocks (f_{CLK}) when the code flash memory is accessed, or when the data flash memory is accessed by an 8-bit instruction.

Note 3. Except r = A

Remark Number of clock is when program exists in the internal ROM (flash memory) area. If fetching the instruction from the internal RAM area, the number becomes double number plus 3 clocks at a maximum.

Table 37 - 14 Operation List (10/18)

Instruction Group	Mnemonic	Operands	Bytes	Clocks		Clocks	Flag		
				Note 1	Note 2		Z	AC	CY
8-bit operation	CMP	A, #byte	2	1	—	A - byte	×	×	×
		!addr16, #byte	4	1	4	(addr16) - byte	×	×	×
		ES:!addr16, #byte	5	2	5	(ES:addr16) - byte	×	×	×
		saddr, #byte	3	1	—	(saddr) - byte	×	×	×
		A, r Note 3	2	1	—	A - r	×	×	×
		r, A	2	1	—	r - A	×	×	×
		A, !addr16	3	1	4	A - (addr16)	×	×	×
		A, ES:!addr16	4	2	5	A - (ES:addr16)	×	×	×
		A, saddr	2	1	—	A - (saddr)	×	×	×
		A, [HL]	1	1	4	A - (HL)	×	×	×
		A, ES:[HL]	2	2	5	A - (ES:HL)	×	×	×
		A, [HL+byte]	2	1	4	A - (HL + byte)	×	×	×
		A, ES:[HL+byte]	3	2	5	A - ((ES:HL) + byte)	×	×	×
		A, [HL+B]	2	1	4	A - (HL + B)	×	×	×
		A, ES:[HL+B]	3	2	5	A - ((ES:HL) + B)	×	×	×
		A, [HL+C]	2	1	4	A - (HL + C)	×	×	×
		A, ES:[HL+C]	3	2	5	A - ((ES:HL) + C)	×	×	×
	CMP0	A	1	1	—	A - 00H	×	0	0
		X	1	1	—	X - 00H	×	0	0
		B	1	1	—	B - 00H	×	0	0
		C	1	1	—	C - 00H	×	0	0
		!addr16	3	1	4	(addr16) - 00H	×	0	0
		ES:!addr16	4	2	5	(ES:addr16) - 00H	×	0	0
		saddr	2	1	—	(saddr) - 00H	×	0	0
	CMPS	X, [HL+byte]	3	1	4	X - (HL + byte)	×	×	×
		X, ES:[HL+byte]	4	2	5	X - ((ES:HL) + byte)	×	×	×

Note 1. Number of CPU clocks (f_{CLK}) when the internal RAM area, SFR area, or extended SFR area is accessed, or when no data is accessed.

Note 2. Number of CPU clocks (f_{CLK}) when the code flash memory is accessed, or when the data flash memory is accessed by an 8-bit instruction.

Note 3. Except r = A

Remark Number of clock is when program exists in the internal ROM (flash memory) area. If fetching the instruction from the internal RAM area, the number becomes double number plus 3 clocks at a maximum.

Table 37 - 15 Operation List (11/18)

Instruction Group	Mnemonic	Operands	Bytes	Clocks		Clocks	Flag		
				Note 1	Note 2		Z	AC	CY
16-bit operation	ADDW	AX, #word	3	1	—	AX, CY ← AX + word	×	×	×
		AX, AX	1	1	—	AX, CY ← AX + AX	×	×	×
		AX, BC	1	1	—	AX, CY ← AX + BC	×	×	×
		AX, DE	1	1	—	AX, CY ← AX + DE	×	×	×
		AX, HL	1	1	—	AX, CY ← AX + HL	×	×	×
		AX, !addr16	3	1	4	AX, CY ← AX + (addr16)	×	×	×
		AX, ES:!addr16	4	2	5	AX, CY ← AX + (ES:addr16)	×	×	×
		AX, saddrp	2	1	—	AX, CY ← AX + (saddrp)	×	×	×
		AX, [HL+byte]	3	1	4	AX, CY ← AX + (HL + byte)	×	×	×
		AX, ES: [HL+byte]	4	2	5	AX, CY ← AX + ((ES:HL) + byte)	×	×	×
	SUBW	AX, #word	3	1	—	AX, CY ← AX - word	×	×	×
		AX, BC	1	1	—	AX, CY ← AX - BC	×	×	×
		AX, DE	1	1	—	AX, CY ← AX - DE	×	×	×
		AX, HL	1	1	—	AX, CY ← AX - HL	×	×	×
		AX, !addr16	3	1	4	AX, CY ← AX - (addr16)	×	×	×
		AX, ES:!addr16	4	2	5	AX, CY ← AX - (ES:addr16)	×	×	×
		AX, saddrp	2	1	—	AX, CY ← AX - (saddrp)	×	×	×
		AX, [HL+byte]	3	1	4	AX, CY ← AX - (HL + byte)	×	×	×
		AX, ES: [HL+byte]	4	2	5	AX, CY ← AX - ((ES:HL) + byte)	×	×	×
	CMPW	AX, #word	3	1	—	AX - word	×	×	×
		AX, BC	1	1	—	AX - BC	×	×	×
		AX, DE	1	1	—	AX - DE	×	×	×
		AX, HL	1	1	—	AX - HL	×	×	×
		AX, !addr16	3	1	4	AX - (addr16)	×	×	×
		AX, ES:!addr16	4	2	5	AX - (ES:addr16)	×	×	×
		AX, saddrp	2	1	—	AX - (saddrp)	×	×	×
		AX, [HL+byte]	3	1	4	AX - (HL + byte)	×	×	×
		AX, ES: [HL+byte]	4	2	5	AX - ((ES:HL) + byte)	×	×	×

Note 1. Number of CPU clocks (f_{CLK}) when the internal RAM area, SFR area, or extended SFR area is accessed, or when no data is accessed.

Note 2. Number of CPU clocks (f_{CLK}) when the code flash memory is accessed, or when the data flash memory is accessed by an 8-bit instruction.

Remark Number of clock is when program exists in the internal ROM (flash memory) area. If fetching the instruction from the internal RAM area, the number becomes double number plus 3 clocks at a maximum.

Table 37 - 16 Operation List (12/18)

Instruction Group	Mnemonic	Operands	Bytes	Clocks		Clocks	Flag		
				Note 1	Note 2		Z	AC	CY
Multiply, Divide, Multiply & accumulate	MULU	X	1	1	—	AX ← A × X			
	MULHU		3	2	—	BCAX ← AX × BC (unsigned)			
	MULH		3	2	—	BCAX ← AX × BC (signed)			
	DIVHU		3	9	—	AX (quotient), DE (remainder) ← AX ÷ DE (unsigned)			
	DIVWU		3	17	—	BCAX (quotient), HLDE (remainder) ← BCAX ÷ HLDE (unsigned)			
	MACHU		3	3	—	MACR ← MACR + AX × BC (unsigned)		×	×
	MACH		3	3	—	MACR ← MACR + AX × BC(signed)		×	×

Note 1. Number of CPU clocks (f_{CLK}) when the internal RAM area, SFR area, or extended SFR area is accessed, or when no data is accessed.

Note 2. Number of CPU clocks (f_{CLK}) when the code flash memory is accessed, or when the data flash memory is accessed by an 8-bit instruction.

Caution Disable interrupts when executing the DIVHU or DIVWU instruction in an interrupt servicing routine. Alternatively, unless they are executed in the RAM area, note that execution of a DIVHU or DIVWU instruction is possible even with interrupts enabled as long as a NOP instruction is added immediately after the DIVHU or DIVWU instruction in the assembly language source code. The following compilers automatically add a NOP instruction immediately after any DIVHU or DIVWU instruction output during the build process.

- V. 1.71 and later versions of the CA78K0R (Renesas Electronics compiler), for both C and assembly language source code

- Service pack 1.40.6 and later versions of the EWRL78 (IAR compiler), for C language source code

- GNURL78 (KPIT compiler), for C language source code

Remark 1. Number of clock is when program exists in the internal ROM (flash memory) area. If fetching the instruction from the internal RAM area, the number becomes double number plus 3 clocks at a maximum.

Remark 2. MACR indicates the multiplication and accumulation register (MACRH, MACRL).

Table 37 - 17 Operation List (13/18)

Instruction Group	Mnemonic	Operands	Bytes	Clocks		Clocks	Flag		
				Note 1	Note 2		Z	AC	CY
Increment/ decrement	INC	r	1	1	—	r ← r + 1	×	×	
		!addr16	3	2	—	(addr16) ← (addr16) + 1	×	×	
		ES:!addr16	4	3	—	(ES, addr16) ← (ES, addr16) + 1	×	×	
		saddr	2	2	—	(saddr) ← (saddr) + 1	×	×	
		[HL+byte]	3	2	—	(HL + byte) ← (HL + byte) + 1	×	×	
		ES: [HL+byte]	4	3	—	((ES:HL) + byte) ← ((ES:HL) + byte) + 1	×	×	
	DEC	r	1	1	—	r ← r - 1	×	×	
		!addr16	3	2	—	(addr16) ← (addr16) - 1	×	×	
		ES:!addr16	4	3	—	(ES, addr16) ← (ES, addr16) - 1	×	×	
		saddr	2	2	—	(saddr) ← (saddr) - 1	×	×	
		[HL+byte]	3	2	—	(HL + byte) ← (HL + byte) - 1	×	×	
		ES: [HL+byte]	4	3	—	((ES:HL) + byte) ← ((ES:HL) + byte) - 1	×	×	
	INCW	rp	1	1	—	rp ← rp + 1			
		!addr16	3	2	—	(addr16) ← (addr16) + 1			
		ES:!addr16	4	3	—	(ES, addr16) ← (ES, addr16) + 1			
		saddrp	2	2	—	(saddrp) ← (saddrp) + 1			
		[HL+byte]	3	2	—	(HL + byte) ← (HL + byte) + 1			
		ES: [HL+byte]	4	3	—	((ES:HL) + byte) ← ((ES:HL) + byte) + 1			
	DECW	rp	1	1	—	rp ← rp - 1			
		!addr16	3	2	—	(addr16) ← (addr16) - 1			
		ES:!addr16	4	3	—	(ES, addr16) ← (ES, addr16) - 1			
		saddrp	2	2	—	(saddrp) ← (saddrp) - 1			
		[HL+byte]	3	2	—	(HL + byte) ← (HL + byte) - 1			
		ES: [HL+byte]	4	3	—	((ES:HL) + byte) ← ((ES:HL) + byte) - 1			
Shift	SHR	A, cnt	2	1	—	(CY ← A_0, A_{m-1} ← A_m, A_7 ← 0) × cnt			×
	SHRW	AX, cnt	2	1	—	(CY ← AX_0, AX_{m-1} ← AX_m, AX_{15} ← 0) × cnt			×
	SHL	A, cnt	2	1	—	(CY ← A_7, A_m ← A_{m-1}, A_0 ← 0) ×cnt			×
		B, cnt	2	1	—	(CY ← B_7, B_m ← B_{m-1}, B_0 ← 0) × cnt			×
		C, cnt	2	1	—	(CY ← C_7, C_m ← C_{m-1}, C_0 ← 0) × cnt			×
	SHLW	AX, cnt	2	1	—	(CY ← AX_{15}, AX_m ← AX_{m-1}, AX_0 ← 0) × cnt			×
		BC, cnt	2	1	—	(CY ← BC_{15}, BC_m ← BC_{m-1}, BC_0 ← 0) × cnt			×
	SAR	A, cnt	2	1	—	(CY ← A_0, A_{m-1} ← A_m, A_7 ← A_7) × cnt			×
	SARW	AX, cnt	2	1	—	(CY ← AX_0, AX_{m-1} ← AX_m, AX_{15} ← AX_{15}) × cnt			×

Note 1. Number of CPU clocks (f_{CLK}) when the internal RAM area, SFR area, or extended SFR area is accessed, or when no data is accessed.

Note 2. Number of CPU clocks (f_{CLK}) when the code flash memory is accessed, or when the data flash memory is accessed by an 8-bit instruction.

Remark 1. Number of clock is when program exists in the internal ROM (flash memory) area. If fetching the instruction from the internal RAM area, the number becomes double number plus 3 clocks at a maximum.

Remark 2. cnt indicates the bit shift count.

Table 37 - 18 Operation List (14/18)

Instruction Group	Mnemonic	Operands	Bytes	Clocks		Clocks	Flag		
				Note 1	Note 2		Z	AC	CY
Rotate	ROR	A, 1	2	1	—	(CY, $A_7 \leftarrow A_0$, $A_{m-1} \leftarrow A_m$) × 1			×
	ROL	A, 1	2	1	—	(CY, $A_0 \leftarrow A_7$, $A_{m+1} \leftarrow A_m$) × 1			×
	RORC	A, 1	2	1	—	(CY $\leftarrow A_0$, $A_7 \leftarrow$ CY, $A_{m-1} \leftarrow A_m$) × 1			×
	ROLC	A, 1	2	1	—	(CY $\leftarrow A_7$, $A_0 \leftarrow$ CY, $A_{m+1} \leftarrow A_m$) × 1			×
	ROLWC	AX,1	2	1	—	(CY $\leftarrow AX_{15}$, $AX_0 \leftarrow$ CY, $AX_{m+1} \leftarrow AX_m$) × 1			×
		BC,1	2	1	—	(CY $\leftarrow BC_{15}$, $BC_0 \leftarrow$ CY, $BC_{m+1} \leftarrow BC_m$) × 1			×
Bit manipulate	MOV1	CY, A.bit	2	1	—	CY ← A.bit			×
		A.bit, CY	2	1	—	A.bit ← CY			
		CY, PSW.bit	3	1	—	CY ← PSW.bit			×
		PSW.bit, CY	3	4	—	PSW.bit ← CY	×	×	
		CY, saddr.bit	3	1	—	CY ← (saddr).bit			×
		saddr.bit, CY	3	2	—	(saddr).bit ← CY			
		CY, sfr.bit	3	1	—	CY ← sfr.bit			×
		sfr.bit, CY	3	2	—	sfr.bit ← CY			
		CY,[HL].bit	2	1	4	CY ← (HL).bit			×
		[HL].bit, CY	2	2	—	(HL).bit ← CY			
		CY, ES:[HL].bit	3	2	5	CY ← (ES, HL).bit			×
		ES:[HL].bit, CY	3	3	—	(ES, HL).bit ← CY			
	AND1	CY, A.bit	2	1	—	CY ← CY ∧ A.bit			×
		CY, PSW.bit	3	1	—	CY ← CY ∧ PSW.bit			×
		CY, saddr.bit	3	1	—	CY ← CY ∧ (saddr).bit			×
		CY, sfr.bit	3	1	—	CY ← CY ∧ sfr.bit			×
		CY,[HL].bit	2	1	4	CY ← CY ∧ (HL).bit			×
		CY, ES:[HL].bit	3	2	5	CY ← CY ∧ (ES, HL).bit			×
	OR1	CY, A.bit	2	1	—	CY ← CY ∨ A.bit			×
		CY, PSW.bit	3	1	—	CY ← CY ∨ PSW.bit			×
		CY, saddr.bit	3	1	—	CY ← CY ∨ (saddr).bit			×
		CY, sfr.bit	3	1	—	CY ← CY ∨ sfr.bit			×
		CY, [HL].bit	2	1	4	CY ← CY ∨ (HL).bit			×
		CY, ES:[HL].bit	3	2	5	CY ← CY ∨ (ES, HL).bit			×

Note 1. Number of CPU clocks (f_{CLK}) when the internal RAM area, SFR area, or extended SFR area is accessed, or when no data is accessed.

Note 2. Number of CPU clocks (f_{CLK}) when the code flash memory is accessed, or when the data flash memory is accessed by an 8-bit instruction.

Remark Number of clock is when program exists in the internal ROM (flash memory) area. If fetching the instruction from the internal RAM area, the number becomes double number plus 3 clocks at a maximum.

Table 37 - 19 Operation List (15/18)

Instruction Group	Mnemonic	Operands	Bytes	Clocks		Clocks	Flag		
				Note 1	Note 2		Z	AC	CY
Bit manipulate	XOR1	CY, A.bit	2	1	—	CY ← CY ⨯ bit			×
		CY, PSW.bit	3	1	—	CY ← CY ⨯ PSW.bit			×
		CY, saddr.bit	3	1	—	CY ← CY ⨯ (saddr).bit			×
		CY, sfr.bit	3	1	—	CY ← CY ⨯ sfr.bit			×
		CY, [HL].bit	2	1	4	CY ← CY ⨯ (HL).bit			×
		CY, ES:[HL].bit	3	2	5	CY ← CY ⨯ (ES, HL).bit			×
	SET1	A.bit	2	1	—	A.bit ← 1			
		PSW.bit	3	4	—	PSW.bit ← 1	×	×	×
		!addr16.bit	4	2	—	(addr16).bit ← 1			
		ES:!addr16.bit	5	3	—	(ES, addr16).bit ← 1			
		saddr.bit	3	2	—	(saddr).bit ← 1			
		sfr.bit	3	2	—	sfr.bit ← 1			
		[HL].bit	2	2	—	(HL).bit ← 1			
		ES:[HL].bit	3	3	—	(ES, HL).bit ← 1			
	CLR1	A.bit	2	1	—	A.bit ← 0			
		PSW.bit	3	4	—	PSW.bit ← 0	×	×	×
		!addr16.bit	4	2	—	(addr16).bit ← 0			
		ES:!addr16.bit	5	3	—	(ES, addr16).bit ← 0			
		saddr.bit	3	2	—	(saddr.bit) ← 0			
		sfr.bit	3	2	—	sfr.bit ← 0			
		[HL].bit	2	2	—	(HL).bit ← 0			
		ES:[HL].bit	3	3	—	(ES, HL).bit ← 0			
	SET1	CY	2	1	—	CY ← 1			1
	CLR1	CY	2	1	—	CY ← 0			0
	NOT1	CY	2	1	—	CY ← $\overline{CY}$			×

Note 1. Number of CPU clocks (f_{CLK}) when the internal RAM area, SFR area, or extended SFR area is accessed, or when no data is accessed

Note 2. Number of CPU clocks (f_{CLK}) when the code flash memory is accessed, or when the data flash memory is accessed by an 8-bit instruction.

Remark Number of clock is when program exists in the internal ROM (flash memory) area. If fetching the instruction from the internal RAM area, the number becomes double number plus 3 clocks at a maximum.

Table 37 - 20 Operation List (16/18)

Instruction Group	Mnemonic	Operands	Bytes	Clocks		Clocks	Flag		
				Note 1	Note 2		Z	AC	CY
Call/return	CALL	rp	2	3	—	(SP - 2) ← (PC + 2)S, (SP - 3) ← (PC + 2)H, (SP - 4) ← (PC + 2)L, PC ← CS, rp, SP ← SP - 4			
		$!addr20	3	3	—	(SP - 2) ← (PC + 3)S, (SP - 3) ← (PC + 3)H, (SP - 4) ← (PC + 3)L, PC ← PC + 3 + jdisp16, SP ← SP - 4			
		!addr16	3	3	—	(SP - 2) ← (PC + 3)S, (SP - 3) ← (PC + 3)H, (SP - 4) ← (PC + 3)L, PC ← 0000, addr16, SP ← SP - 4			
		!!addr20	4	3	—	(SP - 2) ← (PC + 4)S, (SP - 3) ← (PC + 4)H, (SP - 4) ← (PC + 4)L, PC ← addr20, SP ← SP - 4			
	CALLT	[addr5]	2	5	—	(SP - 2) ← (PC + 2)S, (SP - 3) ← (PC + 2)H, (SP - 4) ← (PC + 2)L, PCS ← 0000, PCH ← (0000, addr5 + 1), PCL ← (0000, addr5), SP ← SP - 4			
	BRK	—	2	5	—	(SP - 1) ← PSW, (SP - 2) ← (PC + 2)S, (SP - 3) ← (PC + 2)H, (SP - 4) ← (PC + 2)L, PCS ← 0000, PCH ← (0007FH), PCL ← (0007EH), SP ← SP - 4, IE ← 0			
	RET	—	1	6	—	PCL ← (SP), PCH ← (SP + 1), PCS ← (SP + 2), SP ← SP + 4			
	RETI	—	2	6	—	PCL ← (SP), PCH ← (SP + 1), PCS ← (SP + 2), PSW ← (SP + 3), SP ← SP + 4	R	R	R
	RETB	—	2	6	—	PCL ← (SP), PCH ← (SP + 1), PCS ← (SP + 2), PSW ← (SP + 3), SP ← SP + 4	R	R	R

Note 1. Number of CPU clocks (fCLK) when the internal RAM area, SFR area, or extended SFR area is accessed, or when no data is accessed.

Note 2. Number of CPU clocks (fCLK) when the code flash memory is accessed, or when the data flash memory is accessed by an 8-bit instruction.

Remark Number of clock is when program exists in the internal ROM (flash memory) area. If fetching the instruction from the internal RAM area, the number becomes double number plus 3 clocks at a maximum.

Table 37 - 21 Operation List (17/18)

Instruction Group	Mnemonic	Operands	Bytes	Clocks		Clocks	Flag		
				Note 1	Note 2		Z	AC	CY
Stack manipulate	PUSH	PSW	2	1	—	(SP - 1) ← PSW, (SP - 2) ← 00H, SP ← SP - 2			
		rp	1	1	—	(SP - 1) ← rp_H, (SP - 2) ← rp_L, SP ← SP - 2			
	POP	PSW	2	3	—	PSW ← (SP + 1), SP ← SP + 2	R	R	R
		rp	1	1	—	rp_L ← (SP), rp_H ← (SP + 1), SP ← SP + 2			
	MOVW	SP, #word	4	1	—	SP ← word			
		SP, AX	2	1	—	SP ← AX			
		AX, SP	2	1	—	AX ← SP			
		HL, SP	3	1	—	HL ← SP			
		BC, SP	3	1	—	BC ← SP			
		DE, SP	3	1	—	DE ← SP			
	ADDW	SP, #byte	2	1	—	SP ← SP + byte			
	SUBW	SP, #byte	2	1	—	SP ← SP - byte			
Unconditional branch	BR	AX	2	3	—	PC ← CS, AX			
		$addr20	2	3	—	PC ← PC + 2 + jdisp8			
		$!addr20	3	3	—	PC ← PC + 3 + jdisp16			
		!addr16	3	3	—	PC ← 0000, addr16			
		!!addr20	4	3	—	PC ← addr20			
Conditional branch	BC	$addr20	2	2/4 Note 3	—	PC ← PC + 2 + jdisp8 if CY = 1			
	BNC	$addr20	2	2/4 Note 3	—	PC ← PC + 2 + jdisp8 if CY = 0			
	BZ	$addr20	2	2/4 Note 3	—	PC ← PC + 2 + jdisp8 if Z = 1			
	BNZ	$addr20	2	2/4 Note 3	—	PC ← PC + 2 + jdisp8 if Z = 0			
	BH	$addr20	3	2/4 Note 3	—	PC ← PC + 3 + jdisp8 if (Z ∨ CY) = 0			
	BNH	$addr20	3	2/4 Note 3	—	PC ← PC + 3 + jdisp8 if (Z ∨ CY) = 1			
	BT	saddr.bit, $addr20	4	3/5 Note 3	—	PC ← PC + 4 + jdisp8 if (saddr).bit = 1			
		sfr.bit, $addr20	4	3/5 Note 3	—	PC ← PC + 4 + jdisp8 if sfr.bit = 1			
		A.bit, $addr20	3	3/5 Note 3	—	PC ← PC + 3 + jdisp8 if A.bit = 1			
		PSW.bit, $addr20	4	3/5 Note 3	—	PC ← PC + 4 + jdisp8 if PSW.bit = 1			
		[HL].bit, $addr20	3	3/5 Note 3	6/7	PC ← PC + 3 + jdisp8 if (HL).bit = 1			
		ES:[HL].bit, $addr20	4	4/6 Note 3	7/8	PC ← PC + 4 + jdisp8 if (ES, HL).bit = 1			

Note 1. Number of CPU clocks (f_{CLK}) when the internal RAM area, SFR area, or extended SFR area is accessed, or when no data is accessed.

Note 2. Number of CPU clocks (f_{CLK}) when the code flash memory is accessed, or when the data flash memory is accessed by an 8-bit instruction.

Note 3. This indicates the number of clocks “when condition is not met/when condition is met”.

Remark Number of clock is when program exists in the internal ROM (flash memory) area. If fetching the instruction from the internal RAM area, the number becomes double number plus 3 clocks at a maximum.

Table 37 - 22 Operation List (18/18)

Instruction Group	Mnemonic	Operands	Bytes	Clocks		Clocks	Flag		
				Note 1	Note 2		Z	AC	CY
Conditional branch	BF	saddr.bit, $addr20	4	3/5 Note 3	—	PC ← PC + 4 + jdisp8 if (saddr).bit = 0			
		sfr.bit, $addr20	4	3/5 Note 3	—	PC ← PC + 4 + jdisp8 if sfr.bit = 0			
		A.bit, $addr20	3	3/5 Note 3	—	PC ← PC + 3 + jdisp8 if A.bit = 0			
		PSW.bit, $addr20	4	3/5 Note 3	—	PC ← PC + 4 + jdisp8 if PSW.bit = 0			
		[HL].bit, $addr20	3	3/5 Note 3	6/7	PC ← PC + 3 + jdisp8 if (HL).bit = 0			
		ES:[HL].bit, $addr20	4	4/6 Note 3	7/8	PC ← PC + 4 + jdisp8 if (ES, HL).bit = 0			
	BTCLR	saddr.bit, $addr20	4	3/5 Note 3	—	PC ← PC + 4 + jdisp8 if (saddr).bit = 1 then reset (saddr).bit			
		sfr.bit, $addr20	4	3/5 Note 3	—	PC ← PC + 4 + jdisp8 if sfr.bit = 1 then reset sfr.bit			
		A.bit, $addr20	3	3/5 Note 3	—	PC ← PC + 3 + jdisp8 if A.bit = 1 then reset A.bit			
		PSW.bit, $addr20	4	3/5 Note 3	—	PC ← PC + 4 + jdisp8 if PSW.bit = 1 then reset PSW.bit	×	×	×
		[HL].bit, $addr20	3	3/5 Note 3	—	PC ← PC + 3 + jdisp8 if (HL).bit = 1 then reset (HL).bit			
		ES:[HL].bit, $addr20	4	4/6 Note 3	—	PC ← PC + 4 + jdisp8 if (ES, HL).bit = 1 then reset (ES, HL).bit			
Conditional skip	SKC	—	2	1	—	Next instruction skip if CY = 1			
	SKNC	—	2	1	—	Next instruction skip if CY = 0			
	SKZ	—	2	1	—	Next instruction skip if Z = 1			
	SKNZ	—	2	1	—	Next instruction skip if Z = 0			
	SKH	—	2	1	—	Next instruction skip if (Z ∨ CY) = 0			
	SKNH	—	2	1	—	Next instruction skip if (Z ∨ CY) = 1			
CPU control	SEL Note 4	RBn	2	1	—	RBS[1:0] ← n			
	NOP	—	1	1	—	No Operation			
	EI	—	3	4	—	IE ← 1 (Enable Interrupt)			
	DI	—	3	4	—	IE ← 0 (Disable Interrupt)			
	HALT	—	2	3	—	Set HALT Mode			
	STOP	—	2	3	—	Set STOP Mode			

Note 1. Number of CPU clocks (f_{CLK}) when the internal RAM area, SFR area, or extended SFR area is accessed, or when no data is accessed.

Note 2. Number of CPU clocks (f_{CLK}) when the code flash memory is accessed, or when the data flash memory is accessed by an 8-bit instruction.

Note 3. This indicates the number of clocks “when condition is not met/when condition is met”.

Note 4. n indicates the number of register banks (n = 0 to 3)

Remark Number of clock is when program exists in the internal ROM (flash memory) area. If fetching the instruction from the internal RAM area, the number becomes double number plus 3 clocks at a maximum.

CHAPTER 38 ELECTRICAL SPECIFICATIONS (R5F11N, R5F11P) (A: TA = -40 to +85°C)

This chapter describes the electrical specifications for the products A: Consumer applications (TA = -40 to +85°C).

Caution 1. The RL78 microcontroller has an on-chip debug function, which is provided for development and evaluation. Do not use the on-chip debug function in products designated for mass production, because the guaranteed number of rewritable times of the flash memory may be exceeded when this function is used, and product reliability therefore cannot be guaranteed. Renesas Electronics is not liable for problems occurring when the on-chip debug function is used.

Caution 2. The pins mounted depend on the product. Refer to 2.1 Port Function to 2.2 Functions other than port pins in the User's Manual: Hardware.

38.1 Absolute Maximum Ratings

Absolute Maximum Ratings **(1/3)**

Parameter	Symbols	Conditions	Ratings	Unit
Supply voltage	V_{DD}		-0.5 to +6.5	V
	AV_{DD}	AV_{DD} = V_{DD}	-0.5 to +6.5	V
	AV_{SS}	AV_{SS} = V_{SS}	-0.5 to +0.3	V
REGC pin input voltage	V_{IREGC}	REGC	-0.3 to +2.8 and -0.3 to V_{DD} + 0.3 Note 1	V
REGA pin input voltage	V_{IREGA}	REGA	-0.3 to +2.8 and -0.3 to AV_{DD} + 0.3 Note 2	V
Input voltage	V_{I1}	P01 to P07, P10 to P17, P30 to P32, P35 to P37, P40, P43, P44, P50 to P53, P70 to P77, P80 to P86, P121 to P124, P125 to P127, P137, EXCLK, EXCLKS, $\overline{\text{RESET}}$	-0.3 to V_{DD} + 0.3 Note 3	V
	V_{I2}	P60, P61 (N-ch open-drain)	-0.3 to +6.5	V
Output voltage	V_{O1}	P01 to P07, P10 to P17, P30 to P32, P35 to P37, P40, P43, P44, P50 to P53, P60, P61, P70 to P77, P80 to P86, P125 to P127	-0.3 to V_{DD} + 0.3 Note 3	V
Analog input voltage	V_{AI1}	ANI8 to ANI11	-0.3 to V_{DD} + 0.3 Note 3	V
	V_{AI2}	ANI12 to ANI14 PGA00P, PGA01P, PGA10P, PGA11P, PGA00N, PGA01N, PGA10N, PGA11N, AMP0P to AMP2P, AMP0N to AMP2N	-0.3 to AV_{DD} + 0.3 Note 3	V
Analog output voltage	V_{OA}	SBIAS, PGA1O, AMP0O to AMP2O	-0.3 to AV_{DD} + 0.3 Note 3	V

Note 1. Connect the REGC pin to V_{SS} via a capacitor (0.47 to 1 µF). This value regulates the absolute maximum rating of the REGC pin. Do not use this pin with voltage applied to it.

Note 2. Connect the REGA pin to AV_{SS} via a capacitor (0.22 µF). This value regulates the absolute maximum rating of the REGA pin. Do not use this pin with voltage applied to it.

Note 3. Must be 6.5 V or lower.

Caution **Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.**

Remark 1. Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

Remark 2. The reference voltage is V_{SS} (for the V_{DD} systems) = AV_{SS} (for the AV_{DD} systems)

Absolute Maximum Ratings **(2/3)**

Parameter	Symbols	Conditions		Ratings	Unit
LCD voltage	V_{LI1}	V_{L1} input voltage Note 1		-0.3 to +2.8	V
	V_{LI2}	V_{L2} input voltage Note 1		-0.3 to +6.5	V
	V_{LI3}	V_{L3} input voltage Note 1		-0.3 to +6.5	V
	V_{LI4}	V_{L4} input voltage Note 1		-0.3 to +6.5	V
	V_{LI5}	CAPL, CAPH input voltage Note 1		-0.3 to +6.5	V
	V_{LO1}	V_{L1} output voltage		-0.3 to +2.8	V
	V_{LO2}	V_{L2} output voltage		-0.3 to +6.5	V
	V_{LO3}	V_{L3} output voltage		-0.3 to +6.5	V
	V_{LO4}	V_{L4} output voltage		-0.3 to +6.5	V
	V_{LO5}	CAPL, CAPH output voltage		-0.3 to +6.5	V
	V_{LO6}	COM0 to COM7 SEG0 to SEG35 output voltage	External resistance division method	-0.3 to V_{DD} + 0.3 Note 2	V
			Capacitor split method	-0.3 to V_{DD} + 0.3 Note 2	V
			Internal voltage boosting method	-0.3 to V_{LI4} + 0.3 Note 2	V

Note 1. This value only indicates the absolute maximum ratings when applying voltage to the V_{L1}, V_{L2}, V_{L3}, and V_{L4} pins; it does not mean that applying voltage to these pins is recommended. When using the internal voltage boosting method or capacitance split method, connect these pins to V_{SS} via a capacitor (0.47 µF ± 30%) and connect a capacitor (0.47 µF ± 30%) between the CAPL and CAPH pins.

Note 2. Must be 6.5 V or lower.

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Absolute Maximum Ratings **(3/3)**

Parameter	Symbols	Conditions		Ratings	Unit
Output current, high	I_{OH1}	Per pin		-40	mA
		Total of all pins -170 mA	P40, P43, P44, P80 to P83	-70	mA
			P01 to P07, P10 to P17, P30 to P32, P35 to P37, P50 to P53, P70 to P77, P84 to P86, P125 to P127	-100	mA
Output current, low	I_{OL1}	Per pin		40	mA
		Total of all pins 170 mA	P40, P43, P44, P80 to P83	70	mA
			P01 to P07, P10 to P17, P30 to P32, P35 to P37, P50 to P53, P60, P61, P70 to P77, P84 to P86, P125 to P127	100	mA
Operating ambient temperature	T_A	In normal operation mode		-40 to +85	°C
		In flash memory programming mode			
Storage temperature	T_{stg}			-65 to +150	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

38.2 Oscillator Characteristics

38.2.1 X1 and XT1 oscillator characteristics

(T_A = -40 to +85°C, 2.4 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Resonator	Conditions	MIN.	TYP.	MAX.	Unit
X1 clock oscillation frequency (f_X) Note	Ceramic resonator/crystal resonator	2.7 V ≤ V_{DD} ≤ 5.5 V	1.0		20.0	MHz
		2.4 V ≤ V_{DD} < 2.7 V	1.0		16.0	
XT1 clock oscillation frequency (f_{XT}) Note	Crystal resonator		32	32.768	35	kHz

Note Indicates only permissible oscillator frequency ranges. Refer to **AC Characteristics** for instruction execution time. Request evaluation by the manufacturer of the oscillator circuit mounted on a board to check the oscillator characteristics.

Caution **Since the CPU is started by the high-speed on-chip oscillator clock after a reset release, check the X1 clock oscillation stabilization time using the oscillation stabilization time counter status register (OSTC) by the user. Determine the oscillation stabilization time of the OSTC register and the oscillation stabilization time select register (OSTS) after sufficiently evaluating the oscillation stabilization time with the resonator to be used.**

Remark When using the X1 and XT1 oscillator, refer to **5.4 System Clock Oscillator** in the User's Manual: Hardware.

38.2.2 On-chip oscillator characteristics

(T_A = -40 to +85°C, 2.4 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V)

Oscillators	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
High-speed on-chip oscillator clock frequency Notes 1, 2	f_{IH}	2.7 V ≤ V_{DD} ≤ 5.5 V		1		24	MHz
		2.4 V ≤ V_{DD} < 2.7 V		1		16	MHz
High-speed on-chip oscillator clock frequency accuracy		-20 to +85°C	2.4 V ≤ V_{DD} ≤ 5.5 V	-1.0		+1.0	%
		-40 to +85°C	2.4 V ≤ V_{DD} ≤ 5.5 V	-1.5		+1.5	%
Low-speed on-chip oscillator clock frequency	f_{IL}				15		kHz
Low-speed on-chip oscillator clock frequency accuracy				-15		+15	%

Note 1. High-speed on-chip oscillator frequency is selected with bits 0 to 4 of the option byte (000C2H/010C2H) and bits 0 to 2 of the HOCODIV register.

Note 2. This only indicates the oscillator characteristics. Refer to **AC Characteristics** for instruction execution time.

38.3 DC Characteristics

38.3.1 Pin characteristics

(T_A = -40 to +85°C, 2.4 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V)

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output current, high Note 1	I_{OH1}	Per pin for P01 to P07, P10 to P17, P30 to P32, P35 to P37, P40, P43, P44, P50 to P53, P70 to P77, P80 to P86, P125 to P127				-10.0 Note 2	mA
		Total of P40, P43, P44, P80 to P83 (When duty ≤ 70% Note 3)	4.0 V ≤ V_{DD} ≤ 5.5 V			-55	mA
			2.7 V ≤ V_{DD} < 4.0 V			-10	mA
			2.4 V ≤ V_{DD} < 2.7 V			-5	mA
		Total of P01 to P07, P10 to P17, P30 to P32, P35 to P37, P50 to P53, P70 to P77, P84 to P86, P125 to P127 (When duty ≤ 70% Note 3)	4.0 V ≤ V_{DD} ≤ 5.5 V			-69	mA
			2.7 V ≤ V_{DD} < 4.0 V			-23	mA
			2.4 V ≤ V_{DD} < 2.7 V			-12	mA
		Total of all pins (When duty ≤ 70% Note 3)	2.4 V ≤ V_{DD} ≤ 5.5 V			-124	mA

Note 1. Value of current at which the device operation is guaranteed even if the current flows from the V_{DD} pin (I_{OH1}) to an output pin.

Note 2. However, do not exceed the total current value.

Note 3. Specification under conditions where the duty factor ≤ 70%.
The output current value that has changed to the duty factor > 70% the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

- Total output current of pins = (I_{OH} × 0.7)/(n × 0.01)

<Example> Where n = 80% and I_{OH} = –10.0 mA
Total output current of pins = (–10.0 × 0.7)/(80 × 0.01) ≅ –8.7 mA

However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

Caution P02 to P04, P06, P07, P10, P35 to P37, P40, P43, P44, P50 to P52, and P80 to P82 do not output high level in N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(T_A = -40 to +85°C, 2.4 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V)

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output current, low Note 1	I_{OL1}	Per pin for P01 to P07, P10 to P17, P30 to P32, P35 to P37, P40, P43, P44, P50 to P53, P70 to P77, P80 to P86, P125 to P127				20.0 Note 2	mA
		Per pin for P60 and P61				15.0 Note 2	mA
		Total of P40, P43, P44, P80 to P83 (When duty ≤ 70% Note 3)	4.0 V ≤ V_{DD} ≤ 5.5 V			70	mA
			2.7 V ≤ V_{DD} < 4.0 V			15	mA
			2.4 V ≤ V_{DD} < 2.7 V			9	mA
		P01 to P07, P10 to P17, P30 to P32, P35 to P37, P50 to P53, P60, P61, P70 to P77, P84 to P86, P125 to P127 (When duty ≤ 70% Note 3)	4.0 V ≤ V_{DD} ≤ 5.5 V			90	mA
			2.7 V ≤ V_{DD} < 4.0 V			35	mA
			2.4 V ≤ V_{DD} < 2.7 V			20	mA
		Total of all pins (When duty ≤ 70% Note 3)				160	mA

Note 1. Value of current at which the device operation is guaranteed even if the current flows from an output pin to the V_{SS} pin (I_{OL1}).

Note 2. However, do not exceed the total current value.

Note 3. Specification under conditions where the duty factor ≤ 70%.
The output current value that has changed to the duty factor > 70% the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

- Total output current of pins = (I_{OL} × 0.7)/(n × 0.01)

<Example> Where n = 80% and I_{OL} = 10.0 mA
Total output current of pins = (10.0 × 0.7)/(80 × 0.01) ≅ 8.7 mA

However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(T_A = -40 to +85°C, 2.4 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V)

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input voltage, high	V_{IH1}	P01 to P07, P10 to P17, P30 to P32, P35 to P37, P40, P43, P44, P50 to P53, P70 to P77, P80 to P86, P125 to P127	Normal input buffer	0.8 V_{DD}		V_{DD}	V
	V_{IH2}	For TTL mode supported ports	TTL input buffer 4.0 V ≤ V_{DD} ≤ 5.5 V	2.2		V_{DD}	V
			TTL input buffer 3.3 V ≤ V_{DD} < 4.0 V	2.0		V_{DD}	V
			TTL input buffer 2.4 V ≤ V_{DD} < 3.3 V	1.50		V_{DD}	V
	V_{IH4}	P60, P61		0.7 V_{DD}		6.0	V
	V_{IH5}	P121 to P124, P137, EXCLK, EXCLKS, $\overline{\text{RESET}}$		0.8 V_{DD}		V_{DD}	V
Input voltage, low	V_{IL1}	P01 to P07, P10 to P17, P30 to P32, P35 to P37, P40, P43, P44, P50 to P53, P60, P61, P70 to P77, P80 to P86, P125 to P127	Normal input buffer	0		0.2 V_{DD}	V
	V_{IL2}	For TTL mode supported ports	TTL input buffer 4.0 V ≤ V_{DD} ≤ 5.5 V	0		0.8	V
			TTL input buffer 3.3 V ≤ V_{DD} < 4.0 V	0		0.5	V
			TTL input buffer 2.4 V ≤ V_{DD} < 3.3 V	0		0.32	V
	V_{IL4}	P60, P61		0		0.3 V_{DD}	V
	V_{IL5}	P121 to P124, P137, EXCLK, EXCLKS, $\overline{\text{RESET}}$		0		0.2 V_{DD}	V

Caution The maximum value of V_{IH} of pins P02 to P04, P06, P07, P10, P35 to P37, P40, P43, P44, P50 to P52, and P80 to P82 is V_{DD}, even in the N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(T_A = -40 to +85°C, 2.4 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V)

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output voltage, high	V_{OH1}	P01 to P07, P10 to P17, P30 to P32, P35 to P37, P40, P43, P44, P50 to P53, P70 to P77, P80 to P86, P125 to P127	4.0 V ≤ V_{DD} ≤ 5.5 V, I_{OH} = -10.0 mA	V_{DD} - 1.5			V
			4.0 V ≤ V_{DD} ≤ 5.5 V, I_{OH} = -3.0 mA	V_{DD} - 0.7			V
			2.7 V ≤ V_{DD} ≤ 5.5 V, I_{OH} = -2.0 mA	V_{DD} - 0.6			V
			2.4 V ≤ V_{DD} ≤ 5.5 V, I_{OH} = -1.5 mA	V_{DD} - 0.5			V
Output voltage, low	V_{OL1}	P01 to P07, P10 to P17, P30 to P32, P35 to P37, P40, P43, P44, P50 to P53, P70 to P77, P80 to P86, P125 to P127	4.0 V ≤ V_{DD} ≤ 5.5 V, I_{OL} = 20.0 mA			1.3	V
			4.0 V ≤ V_{DD} ≤ 5.5 V, I_{OL} = 8.5 mA			0.7	V
			2.7 V ≤ V_{DD} ≤ 5.5 V, I_{OL} = 3.0 mA			0.6	V
			2.7 V ≤ V_{DD} ≤ 5.5 V, I_{OL} = 1.5 mA			0.4	V
			2.4 V ≤ V_{DD} ≤ 5.5 V, I_{OL} = 0.6 mA			0.4	V
	V_{OL3}	P60, P61	4.0 V ≤ V_{DD} ≤ 5.5 V, I_{OL} = 15.0 mA			2.0	V
			4.0 V ≤ V_{DD} ≤ 5.5 V, I_{OL} = 5.0 mA			0.4	V
			2.7 V ≤ V_{DD} ≤ 5.5 V, I_{OL} = 3.0 mA			0.4	V
			2.4 V ≤ V_{DD} ≤ 5.5 V, I_{OL} = 2.0 mA			0.4	V

Caution **P02 to P04, P06, P07, P10, P35 to P37, P40, P43, P44, P50 to P52, and P80 to P82 do not output high level in N-ch open-drain mode.**

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(T_A = -40 to +85°C, 2.4 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V)

Items	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Input leakage current, high	I_{LIH1}	P01 to P07, P10 to P17, P30 to P32, P35 to P37, P40, P43, P44, P50 to P53, P60, P61, P70 to P77, P80 to P86, P125 to P127, P137, $\overline{\text{RESET}}$	V_I = V_{DD}				1	μA
	I_{LIH3}	P121 to P124 (X1, X2, EXCLK, XT1, XT2, EXCLKS)	V_I = V_{DD}	In input port or external clock input			1	μA
				In resonator connection			10	μA
Input leakage current, low	I_{LIL1}	P01 to P07, P10 to P17, P30 to P32, P35 to P37, P40, P43, P44, P50 to P53, P60, P61, P70 to P77, P80 to P86, P125 to P127, P137, $\overline{\text{RESET}}$	V_I = V_{SS}				-1	μA
	I_{LIL3}	P121 to P124 (X1, X2, EXCLK, XT1, XT2, EXCLKS)	V_I = V_{SS}	In input port or external clock input			-1	μA
				In resonator connection			-10	μA
On-chip pull-up resistance	R_{U1}	P01 to P07, P10 to P17, P30 to P32, P35 to P37, P40, P43, P44, P50 to P53, P70 to P77, P80 to P86, P125 to P127	V_I = V_{SS} or In input port		10	20	100	kΩ

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

38.3.2 Supply current characteristics

(T_A = -40 to +85°C, 2.4 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V) (1/2)

Parameter	Symbol	Conditions					MIN.	TYP.	MAX.	Unit
Supply current Notes 1, Note 6	I_{DD1}	Operating mode	HS (high-speed main) mode Note 5	f_{IH} = 24 MHz Note 3	Basic operation	V_{DD} = 5.0 V		1.7		mA
						V_{DD} = 3.0 V		1.7		
					Normal operation	V_{DD} = 5.0 V		3.7	6.2	
						V_{DD} = 3.0 V		3.7	6.2	
				f_{IH} = 16 MHz Note 3	Normal operation	V_{DD} = 5.0 V		2.8	4.8	
						V_{DD} = 3.0 V		2.8	4.8	
			HS (high-speed main) mode Note 5	f_{MX} = 20 MHz Note 2, V_{DD} = 5.0 V	Normal operation	Square wave input		3.1	5.2	mA
						Resonator connection		3.3	5.3	
				f_{MX} = 20 MHz Note 2, V_{DD} = 3.0 V	Normal operation	Square wave input		3.0	5.2	
						Resonator connection		3.3	5.3	
				f_{MX} = 16 MHz Note 2, V_{DD} = 5.0 V	Normal operation	Square wave input		2.6	4.5	
						Resonator connection		2.8	4.6	
				f_{MX} = 16 MHz Note 2, V_{DD} = 3.0 V	Normal operation	Square wave input		2.6	4.5	
						Resonator connection		2.8	4.6	
				f_{MX} = 10 MHz Note 2, V_{DD} = 5.0 V	Normal operation	Square wave input		1.9	3.0	
						Resonator connection		1.9	3.0	
				f_{MX} = 10 MHz Note 2, V_{DD} = 3.0 V	Normal operation	Square wave input		1.9	3.0	
						Resonator connection		1.9	3.0	
			Subsystem clock operation	f_{SUB} = 32.768 kHz Note 4 T_A = -40°C	Normal operation	Square wave input		4.3	5.8	µA
						Resonator connection		4.6	5.8	
				f_{SUB} = 32.768 kHz Note 4 T_A = +25°C	Normal operation	Square wave input		4.3	5.8	
						Resonator connection		4.6	5.8	
				f_{SUB} = 32.768 kHz Note 4 T_A = +50°C	Normal operation	Square wave input		4.5	7.6	
						Resonator connection		4.5	7.6	
				f_{SUB} = 32.768 kHz Note 4 T_A = +70°C	Normal operation	Square wave input		4.7	9.2	
						Resonator connection		5.1	9.2	
				f_{SUB} = 32.768 kHz Note 4 T_A = +85°C	Normal operation	Square wave input		5.2	12.6	
						Resonator connection		5.7	12.6	

Note 1. Total current flowing into V_{DD}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD} or V_{SS}. The following points apply in the HS (high-speed main) mode.

- The currents in the "TYP." column do not include the operating currents of the peripheral modules.
- The currents in the "MAX." column include the operating currents of the peripheral modules, except for those flowing into the LCD controller/driver, A/D converter, LVD, I/O port, and on-chip pull-up/pull-down resistors, and those flowing while the data flash memory is being rewritten.

In the subsystem clock operation, the currents in both the "TYP." and "MAX." columns do not include the operating currents of the peripheral modules. However, in HALT mode, including the current flowing into the real-time clock 2.The current flowing into AFE is not included.

Note 2. When high-speed on-chip oscillator and subsystem clock are stopped.

Note 3. When high-speed system clock and subsystem clock are stopped.

Note 4. When high-speed on-chip oscillator and high-speed system clock are stopped. When AMPHS1 = 1 (Ultra-low power consumption oscillation).

Note 5. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.
HS (high-speed main) mode: 2.7 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 24 MHz
2.4 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 16 MHz

Note 6. I_{DD1} do not include the current flowing to the AFE.
The current value of the RL78 microcontrollers is the sum of I_{DD1}, I_{DD2}, or I_{DD3} and AFE current (AV_{DD} systems) when the AFE operates in the operating mode, HALT mode, or STOP mode.

Remark 1. f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

Remark 2. f_{IH}: High-speed on-chip oscillator clock frequency

Remark 3. f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)

Remark 4. Except subsystem clock operation, temperature condition of the TYP. value is T_A = 25°C.

(T_A = -40 to +85°C, 2.4 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V) **(2/2)**

Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit
Supply current Notes 1, Note 8	I_{DD2} Note 2	HALT mode	HS (high-speed main) mode Note 6	f_{IH} = 24 MHz Note 4	V_{DD} = 5.0 V		0.42	1.83	mA
					V_{DD} = 3.0 V		0.42	1.83	
				f_{IH} = 16 MHz Note 4	V_{DD} = 5.0 V		0.39	1.38	
					V_{DD} = 3.0 V		0.39	1.38	
			HS (high-speed main) mode Note 6	f_{MX} = 20 MHz Note 3, V_{DD} = 5.0 V	Square wave input		0.26	1.55	mA
					Resonator connection		0.40	1.68	
				f_{MX} = 20 MHz Note 3, V_{DD} = 3.0 V	Square wave input		0.25	1.55	
					Resonator connection		0.40	1.68	
				f_{MX} = 16 MHz Note 3, V_{DD} = 5.0 V	Square wave input		0.23	1.22	
					Resonator connection		0.36	1.39	
				f_{MX} = 16 MHz Note 3, V_{DD} = 3.0 V	Square wave input		0.22	1.22	
					Resonator connection		0.35	1.39	
				f_{MX} = 10 MHz Note 3, V_{DD} = 5.0 V	Square wave input		0.19	0.82	
					Resonator connection		0.29	0.90	
				f_{MX} = 10 MHz Note 3, V_{DD} = 3.0 V	Square wave input		0.18	0.82	
					Resonator connection		0.28	0.90	
			Subsystem clock operation	f_{SUB} = 32.768 kHz Note 5 T_A = -40°C	Square wave input		0.32	0.69	µA
					Resonator connection		0.51	0.89	
				f_{SUB} = 32.768 kHz Note 5 T_A = +25°C	Square wave input		0.41	0.82	
					Resonator connection		0.62	1.00	
				f_{SUB} = 32.768 kHz Note 5 T_A = +50°C	Square wave input		0.52	1.40	
					Resonator connection		0.75	1.60	
				f_{SUB} = 32.768 kHz Note 5 T_A = +70°C	Square wave input		0.82	2.70	
					Resonator connection		1.08	2.90	
				f_{SUB} = 32.768 kHz Note 5 T_A = +85°C	Square wave input		1.38	4.95	
					Resonator connection		1.62	5.15	
	I_{DD3}	STOP mode Note 7	T_A = -40°C				0.20	0.59	µA
			T_A = +25°C				0.26	0.72	
			T_A = +50°C				0.33	1.30	
			T_A = +70°C				0.53	2.60	
			T_A = +85°C				0.93	4.85	

(**Notes** and **Remarks** are listed on the next page.)

Note 1. Total current flowing into V_{DD}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD} or V_{SS}.The following points apply in the HS (high-speed main) mode.

- The currents in the “TYP.” column do not include the operating currents of the peripheral modules.
- The currents in the “MAX.” column include the operating currents of the peripheral modules, except for those flowing into the LCD controller/driver, A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors, and those flowing while the data flash memory is being rewritten.

In the subsystem clock operation, the currents in both the “TYP.” and “MAX.” columns do not include the operating currents of the peripheral modules. However, in HALT mode, including the current flowing into the real-time clock 2.

In the STOP mode, the currents in both the “TYP.” and “MAX.” columns do not include the operating currents of the peripheral modules.The current flowing into AFE is not included.

Note 2. During HALT instruction execution by flash memory.

Note 3. When high-speed on-chip oscillator and subsystem clock are stopped.

Note 4. When high-speed system clock and subsystem clock are stopped.

Note 5. When high-speed on-chip oscillator and high-speed system clock are stopped. When RTCLPC = 1 and setting ultra-low current consumption (AMPHS1 = 1).

Note 6. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (high-speed main) mode: 2.7 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 24 MHz
2.4 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 16 MHz

Note 7. Regarding the value for current to operate the subsystem clock in STOP mode, refer to that in HALT mode.

Note 8. I_{DD2} and I_{DD3} do not include the current flowing to the AFE.

The current value of the RL78 microcontrollers is the sum of I_{DD1}, I_{DD2}, or I_{DD3} and AFE current (AV_{DD} systems) when the AFE operates in the operating mode, HALT mode, or STOP mode.

Remark 1. f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

Remark 2. f_{IH}: High-speed on-chip oscillator clock frequency

Remark 3. f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)

Remark 4. Except subsystem clock operation, temperature condition of the TYP. value is T_A = 25°C.

• Peripheral functions

(T_A = -40 to +85°C, 2.4 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit
Low-speed on-chip oscillator operating current	I_{FIL} Note 1						0.20		μA
RTC2 operating current	I_{RTC} Notes 1, 3	f_{SUB} = 32.768 kHz					0.02		μA
12-bit interval timer operating current	I_{TMKA} Notes 1, 2, 4	f_{SUB} = 32.768 kHz, f_{MAIN} stopped					0.02		μA
8-bit interval timer operating current	I_{TMRT} Notes 1, 14	f_{SUB} = 32.768 kHz, f_{MAIN} stopped, per unit		8-bit counter mode × 2-channel operation			0.12		μA
				16-bit counter mode operation			0.10		μA
Watchdog timer operating current	I_{WDT} Notes 1, 5	f_{IL} = 15 kHz					0.22		μA
A/D converter operating current	I_{ADC} Notes 1, 6	When conversion at maximum speed		Normal mode, V_{DD} = 5.0 V			1.3	1.7	mA
				Low-voltage mode, V_{DD} = 3.0 V			0.5	0.7	mA
Internal reference voltage (1.45 V) current	I_{ADREF} Notes 1, 7						85		μA
Temperature sensor operating current	I_{TMPS} Note 1						85		μA
LVD operating current	I_{LVI} Notes 1, 8						0.06		μA
Self-programming operating current	I_{FSP} Notes 1, 9						2.0	12.2	mA
BGO operating current	I_{BGO} Notes 1, 10						2.0	12.2	mA
SNOOZE operating current	I_{SNOZ} Notes 1, 11	A/D converter operation		The mode is performed			0.50	0.60	mA
				During A/D conversion, low-voltage mode, V_{DD} = 3.0 V			1.20	1.44	
		Simplified SPI(CSI)/UART operation					0.70	0.84	mA
		DTC operation					3.1		mA
LCD operating current	I_{LCD1} Notes 12, 13	External resistance division method	f_{LCD} = f_{SUB} LCD clock = 128 Hz	1/3 bias 4-time slice	V_{DD} = 5.0 V, V_{L4} = 5.0 V		0.04	0.20	μA
	I_{LCD2} Note 12	Internal voltage boosting method	f_{LCD} = f_{SUB} LCD clock = 128 Hz	1/3 bias 4-time slice	V_{DD} = 3.0 V, V_{L4} = 3.0 V (VLCD = 04H)		0.85	2.20	μA
					V_{DD} = 5.0 V, V_{L4} = 5.1 V (VLCD = 04H)		1.55	3.70	μA
	I_{LCD3} Note 12	Capacitor split method	f_{LCD} = f_{SUB} LCD clock = 128 Hz	1/3 bias 4-time slice	V_{DD} = 3.0 V, V_{L4} = 3.0 V		0.20	0.50	μA

(**Notes** and **Remarks** are listed on the next page.)

Note 1. Current flowing to V_{DD}.

Note 2. When high speed on-chip oscillator and high-speed system clock are stopped.

Note 3. Current flowing only to the real-time clock 2 (excluding the operating current of the low-speed on-chip oscillator and the XT1 oscillator). The supply current of the RL78 microcontrollers is the sum of the values of either I_{DD1} or I_{DD2}, and I_{RTC}, when the real-time clock 2 operates in the operating mode or HALT mode. When the low-speed on-chip oscillator is selected, I_{FIL} should be added. I_{DD2} subsystem clock operation includes the operational current of the real-time clock 2.

Note 4. Current flowing only to the 12-bit interval timer (excluding the operating current of the low-speed on-chip oscillator and the XT1 oscillator). The supply current of the RL78 microcontrollers is the sum of the values of either I_{DD1} or I_{DD2}, and I_{TMKA}, when the 12-bit interval timer operates in the operating mode or HALT mode. When the low-speed on-chip oscillator is selected, I_{FIL} should be added. I_{DD2} subsystem clock operation includes the operational current of the 12-bit interval timer.

Note 5. Current flowing only to the watchdog timer (including the operating current of the low-speed on-chip oscillator). The current value of the RL78 microcontrollers is the sum of I_{DD1}, I_{DD2}, or I_{DD3} and I_{WDT} when the watchdog timer operates in STOP mode.

Note 6. Current flowing only to the A/D converter. The supply current of the RL78 microcontrollers is the sum of I_{DD1} or I_{DD2} and I_{ADC}, I_{ADREF} when the A/D converter operates in the operating mode or the HALT mode.

Note 7. Operation current flowing to the internal reference voltage.

Note 8. Current flowing only to the LVD circuit. The current value of the RL78 microcontrollers is the sum of I_{DD1}, I_{DD2}, or I_{DD3} and I_{LVI} when the LVD circuit operates in the operating mode, HALT mode, or STOP mode.

Note 9. Current flowing only during self-programming.

Note 10. Current flowing only during data flash rewrite.

Note 11. For shift time to the SNOOZE mode, see **27.3.3 SNOOZE mode** in the User's Manual: Hardware.

Note 12. Current flowing only to the LCD controller/driver (V_{DD} pin). The current value of the RL78 microcontrollers is the sum of the LCD operating current (I_{LCD1}, I_{LCD2}, or I_{LCD3}) and the supply current (I_{DD1} or I_{DD2}) when the LCD controller/driver operates in the operating mode or HALT mode. Not including the current that flows through the LCD panel.

Note 13. Not including the current that flows through the external divider resistor.

Note 14. Current flowing only to the 8-bit interval timer (excluding the operating current of the low-speed on-chip oscillator and the XT1 oscillator). The supply current of the RL78 microcontrollers is the sum of the values of either I_{DD1} or I_{DD2}, and I_{IT}, when the 8-bit interval timer operates in the operating mode or HALT mode. When the low-speed on-chip oscillator is selected, I_{FIL} should be added.

Remark 1. f_{IL}: Low-speed on-chip oscillator clock frequency

Remark 2. f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)

Remark 3. f_{CLK}: CPU/peripheral hardware clock frequency

Remark 4. Temperature condition of the TYP. value is T_A = 25°C

• AFE functions

(T_A = -40 to +85°C, 2.7 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
24-bit ΔΣ A/D converter operating current	I_{DSAD}	Normal mode Notes 1, 2 Circuits that operate: ABGR, REGA, SBIAS, VREFAMP, PGA0, 24-bit ΔΣ A/D converter, and digital filter Differential input mode, OSR = 256, SBIAS I_{OUT} = 0 mA		0.94	1.46	mA
		Low power mode Notes 1, 2 Circuits that operate: ABGR, REGA, SBIAS, VREFAMP, PGA0, 24-bit ΔΣ A/D converter, and digital filter Differential input mode, OSR = 256, SBIAS I_{OUT} = 0 mA		0.60	0.91	mA
Amplifier operating current	I_{PGA1}	Low power mode Notes 1, 2 Circuits that operate: ABGR, PGA1, and DAC1 I_L = 0 mA		0.60	1.10	mA
		High-speed mode Notes 1, 2 Circuits that operate: ABGR, PGA1, and DAC1 I_L = 0 mA		1.10	1.80	mA
	I_{AMP0}	Low power mode Notes 1, 2 Circuits that operate: ABGR and AMP0 I_L = 0 mA		0.10	0.15	mA
		High-speed mode Notes 1, 2 Circuits that operate: ABGR and AMP0 I_L = 0 mA		0.30	0.48	mA
	I_{AMP1}, I_{AMP2}	Low power mode Notes 1, 2 Circuits that operate: ABGR and AMP1 or AMP2 I_L = 0 mA		0.10	0.14	mA
		High-speed mode Notes 1, 2 Circuits that operate: ABGR and AMP1 or AMP2 I_L = 0 mA		0.23	0.35	mA
8-bit D/A converter operating current	I_{DAC0}	SBIAS normal mode Notes 1, 2 Circuits that operate: ABGR, REGA, SBIAS, and DAC0 Note 3 I_L = 0 mA, SBIAS I_{OUT} = 0 mA		1.00	1.50	mA
		SBIAS low-power mode Notes 1, 2 Circuits that operate: ABGR, REGA, SBIAS, and DAC0 Note 3 I_L = 0 mA, SBIAS I_{OUT} = 0 mA		0.85	1.30	mA
12-bit D/A converter operating current	I_{DAC1}	When AV_{DD} is selected as the reference voltage Notes 1, 2 Circuits that operate: ABGR and DAC1 I_L = 0 mA		0.61	0.97	mA
		When SBIAS (normal mode) is selected as the reference voltage Notes 1, 2 Circuits that operate: ABGR, REGA, SBIAS, and DAC1 Note 3 I_L = 0 mA, SBIAS I_{OUT} = 0 mA		1.06	1.62	mA
		When SBIAS (low-power mode) is selected as the reference voltage Notes 1, 2 Circuits that operate: ABGR, REGA, SBIAS, and DAC1 Note 3 I_L = 0 mA, SBIAS I_{OUT} = 0 mA		0.91	1.42	mA

Note 1. Current flowing to AV_{DD}. The typical conditions are the conditions when T_A = 25°C and AV_{DD} = 3.3 V.

Note 2. Current flowing only into the operating circuit indicated in the column for conditions.

Note 3. Including the static current of VREFAMP, PGA0, and 24-bit ΔΣ A/D converter.

Remark Values in parentheses are target design values (i.e. not guaranteed) and therefore are not tested for shipment.

38.4 AC Characteristics

38.4.1 Basic operation

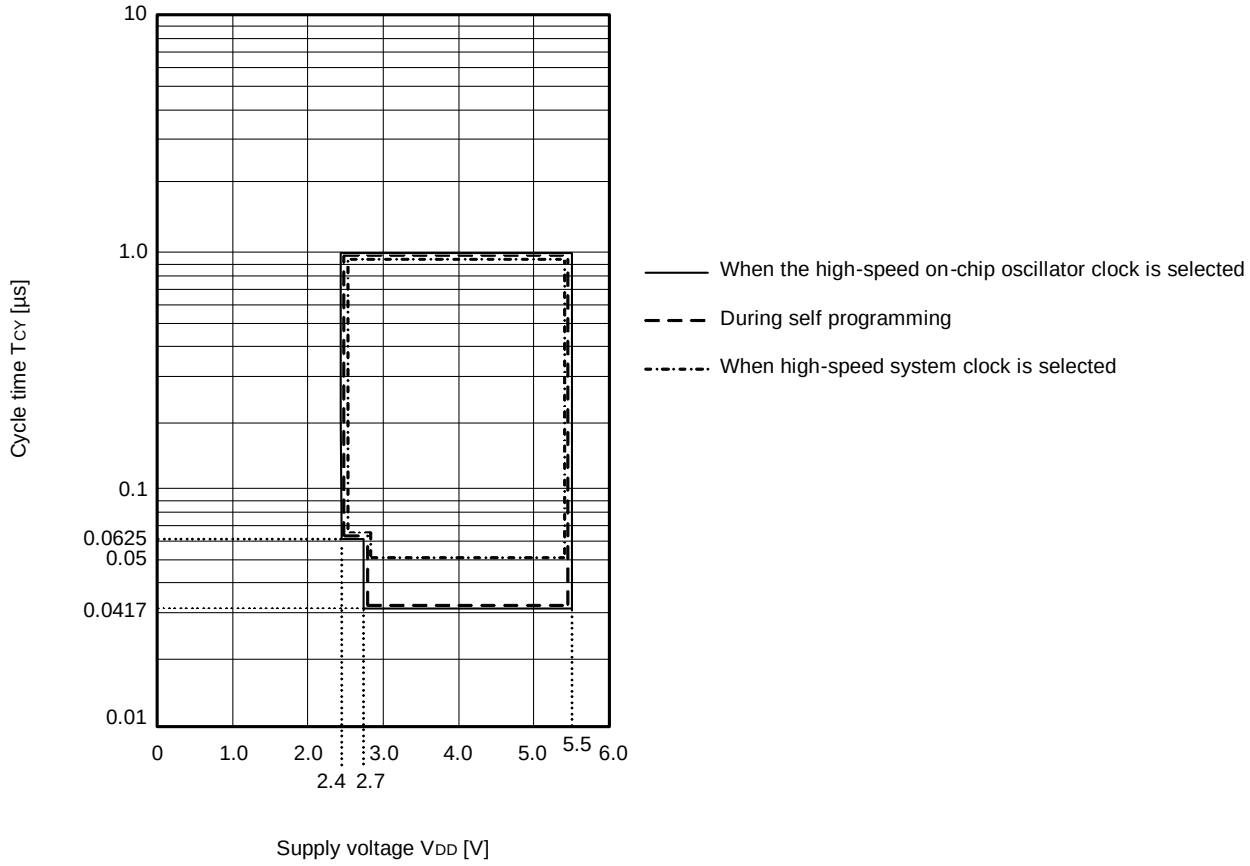
(T_A = -40 to +85°C, 2.4 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V)

Items	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Instruction cycle (minimum instruction execution time)	T_{CY}	Main system clock (f_{MAIN}) operation	HS (high-speed main) mode	2.7 V ≤ V_{DD} ≤ 5.5 V	0.0417		1	μs
				2.4 V ≤ V_{DD} < 2.7 V	0.0625		1	μs
		Subsystem clock (f_{SUB}) operation	f_{XT} =32.768 kHz	2.4 V ≤ V_{DD} ≤ 5.5 V	28.5	30.5	31.3	μs
		In the self-programming mode	HS (high-speed main) mode	2.7 V ≤ V_{DD} ≤ 5.5 V	0.0417		1	μs
				2.4 V ≤ V_{DD} < 2.7 V	0.0625		1	μs
External main system clock frequency	f_{EX}	EXCLK		2.7 V ≤ V_{DD} ≤ 5.5 V	1.0		20.0	MHz
				2.4 V ≤ V_{DD} < 2.7 V	1.0		16.0	MHz
	f_{EXT}	EXCLKS			32		35	kHz
External main system clock input high-level width, low-level width	t_{EXH}, t_{EXL}	EXCLK		2.7 V ≤ V_{DD} ≤ 5.5 V	24			ns
				2.4 V ≤ V_{DD} < 2.7 V	30			ns
	t_{EXHS}, t_{EXLS}	EXCLKS			13.7			μs
Timer input high-level width, low-level width	t_{TIH}, t_{TIL}	TI00 to TI07			1/f_{MCK} + 10			ns
Timer output frequency	f_{TO}	TO00 to TO07	HS (high-speed main) mode	4.0 V ≤ V_{DD} ≤ 5.5 V			12	MHz
				2.7 V ≤ V_{DD} < 4.0 V			8	MHz
				2.4 V ≤ V_{DD} < 2.7 V			4	MHz
Buzzer output frequency	f_{PCL}	PCLBUZ0, PCLBUZ1	HS (high-speed main) mode	4.0 V ≤ V_{DD} ≤ 5.5 V			12	MHz
				2.7 V ≤ V_{DD} < 4.0 V			8	MHz
				2.4 V ≤ V_{DD} < 2.7 V			4	MHz
Interrupt input high-level width, low-level width	t_{INTH}, t_{INTL}	INTP0 to INTP7		2.4 V ≤ V_{DD} ≤ 5.5 V	1			μs
$\overline{\text{RESET}}$ low-level width	t_{RSL}				10			μs

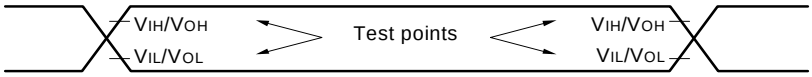
Remark f_{MCK}: Timer array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of timer mode register mn (TMRmn). m: Unit number (m = 0), n: Channel number (n = 0 to 7))

Minimum Instruction Execution Time during Main System Clock Operation

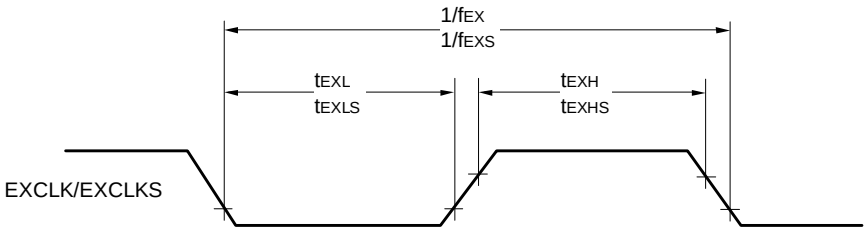
TCY vs VDD (HS (high-speed main) mode)



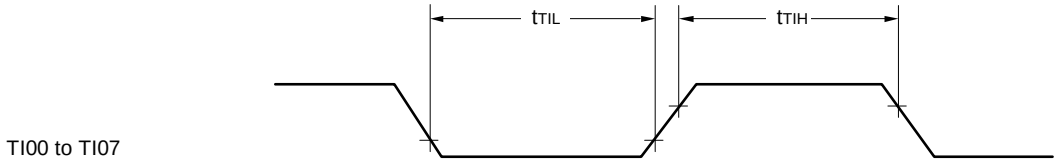
AC Timing Test Points

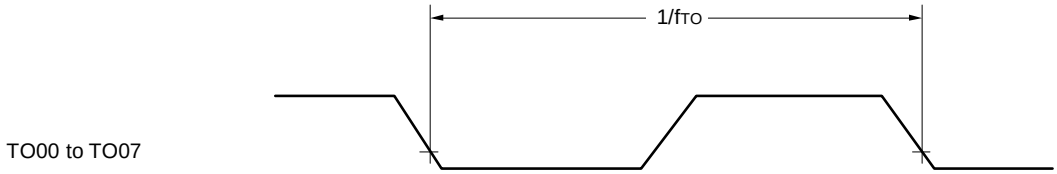


External System Clock Timing

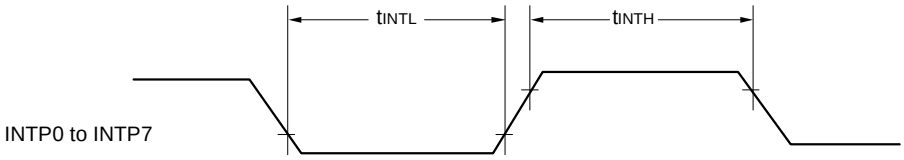


TI/TO Timing

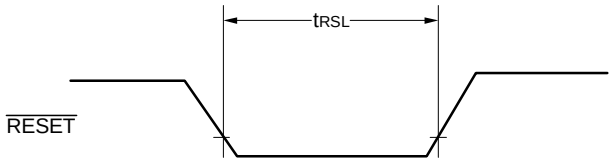




Interrupt Request Input Timing



$\overline{\text{RESET}}$ Input Timing



38.5 Peripheral Functions Characteristics

38.5.1 Serial array unit

(1) During communication at same potential (UART mode)

(T_A = -40 to +85°C, 2.4 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		Unit
			MIN.	MAX.	
Transfer rate Note 1		2.4 V ≤ V_{DD} ≤ 5.5 V		f_{MCK}/6 Note 2	bps
		Theoretical value of the maximum transfer rate f_{MCK} = f_{CLK} Note 3		4.0	Mbps

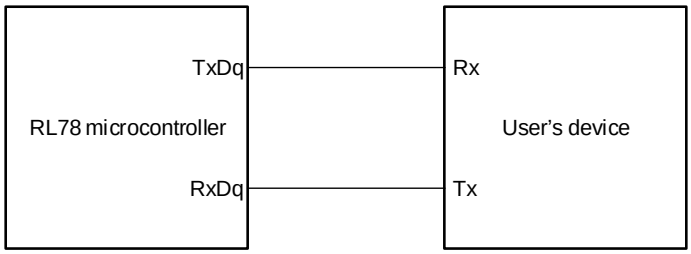
Note 1. Transfer rate in the SNOOZE mode is 4800 bps only.

Note 2. The following conditions are required for low voltage interface.
2.4 V ≤ V_{DD} < 2.7 V: MAX. 2.6 Mbps

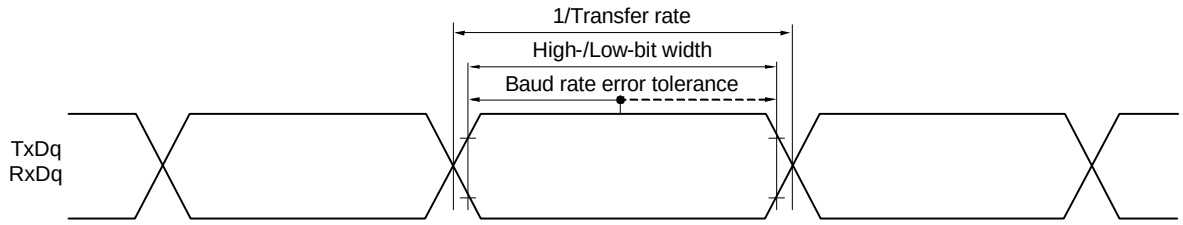
Note 3. The maximum operating frequencies of the CPU/peripheral hardware clock (f_{CLK}) are:
HS (high-speed main) mode: 24 MHz (2.7 V ≤ V_{DD} ≤ 5.5 V)
16 MHz (2.4 V ≤ V_{DD} ≤ 5.5 V)

Caution Select the normal input buffer for the RxDq pin and the normal output mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg).

UART mode connection diagram (during communication at same potential)



UART mode bit width (during communication at same potential) (reference)



Remark 1. q: UART number (q = 0 to 2), g: PIM and POM number (g = 0, 1, 3, 4, 5, 8)

Remark 2. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03, 10, 11))

(2) During communication at same potential (Simplified SPI(CSI) mode) (master mode, SCKp... internal clock output)

(T_A = -40 to +85°C, 2.4 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		Unit
				MIN.	MAX.	
SCKp cycle time	t_{KCY1}	t_{KCY1} ≥ f_{CLK}/4	2.7 V ≤ V_{DD} ≤ 5.5 V	167		ns
			2.4 V ≤ V_{DD} ≤ 5.5 V	250		ns
SCKp high-/low-level width	t_{KH1}, t_{KL1}	4.0 V ≤ V_{DD} ≤ 5.5 V		t_{KCY1}/2 - 12		ns
		2.7 V ≤ V_{DD} ≤ 5.5 V		t_{KCY1}/2 - 18		ns
		2.4 V ≤ V_{DD} ≤ 5.5 V		t_{KCY1}/2 - 38		ns
SIp setup time (to SCKp↑) Note 1	t_{SIK1}	4.0 V ≤ V_{DD} ≤ 5.5 V		44		ns
		2.7 V ≤ V_{DD} ≤ 5.5 V		44		ns
		2.4 V ≤ V_{DD} ≤ 5.5 V		75		ns
SIp hold time (from SCKp↑) Note 2	t_{KSI1}	2.4 V ≤ V_{DD} ≤ 5.5 V		19		ns
Delay time from SCKp↓ to SOp output Note 3	t_{KSO1}	C = 20 pF Note 4	2.7 V ≤ V_{DD} ≤ 5.5 V		25	ns
			2.4 V ≤ V_{DD} ≤ 5.5 V		25	ns

Note 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes “to SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes “from SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes “from SCKp↑” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 4. C is the load capacitance of the SCKp and SOp output lines.

Caution Select the normal input buffer for the SIp pin and the normal output mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remark 1. p: CSI number (p = 00, 10, 20), m: Unit number (m = 0, 1), n: Channel number (n = 0, 2), g: PIM and POM number (g = 0, 1, 3, 4, 5, 8)

Remark 2. f_{MCK}: Serial array unit operation clock frequency (Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00, 02, 10))

(3) During communication at same potential (Simplified SPI(CSI) mode) (slave mode, SCKp... external clock output) (1/2)

(T_A = -40 to +85°C, 2.4 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		Unit
				MIN.	MAX.	
SCKp cycle time Note 5	t_{KCY2}	4.0 V ≤ V_{DD} ≤ 5.5 V	20 MHz < f_{MCK}	8/f_{MCK}		ns
			f_{MCK} ≤ 20 MHz	8/f_{MCK}		ns
		2.7 V ≤ V_{DD} ≤ 5.5 V	f_{MCK} > 16 MHz	8/f_{MCK}		ns
			f_{MCK} ≤ 16 MHz	6/f_{MCK}		ns
		2.4 V ≤ V_{DD} ≤ 5.5 V		6/f_{MCK} and 500		ns
SCKp high-/low-level width	t_{KH2}, t_{KL2}	4.0 V ≤ V_{DD} ≤ 5.5 V		t_{KCY2}/2 - 7		ns
		2.7 V ≤ V_{DD} ≤ 5.5 V		t_{KCY2}/2 - 8		ns
		2.4 V ≤ V_{DD} ≤ 5.5 V		t_{KCY2}/2 - 18		ns
SIp setup time (to SCKp↑) Note 1	t_{SIK2}	2.7 V ≤ V_{DD} ≤ 5.5 V		1/f_{MCK} + 20		ns
		2.4 V ≤ V_{DD} ≤ 5.5 V		1/f_{MCK} + 30		ns
SIp hold time (from SCKp↑) Note 2	t_{KSI2}	2.4 V ≤ V_{DD} ≤ 5.5 V		1/f_{MCK} + 31		ns
Delay time from SCKp↓ to SOp output Note 3	t_{KSO2}	C = 30 pF Note 4	2.7 V ≤ V_{DD} ≤ 5.5 V		2/f_{MCK} + 44	ns
			2.4 V ≤ V_{DD} ≤ 5.5 V		2/f_{MCK} + 75	ns

Note 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes “to SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes “from SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes “from SCKp↑” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 4. C is the load capacitance of the SCKp and SOp output lines.

Note 5. The maximum transfer rate when using the SNOOZE mode is 1 Mbps.

Caution Select the normal input buffer for the SIp pin and the normal output mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remark 1. p: CSI number (p = 00, 10, 20), m: Unit number (m = 0, 1), n: Channel number (n = 0, 2), g: PIM and POM number (g = 0, 1, 3, 4, 5, 8)

Remark 2. f_{MCK}: Serial array unit operation clock frequency (Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00, 02, 10))

(3) During communication at same potential (Simplified SPI(CSI) mode) (slave mode, SCKp... external clock output) (2/2)

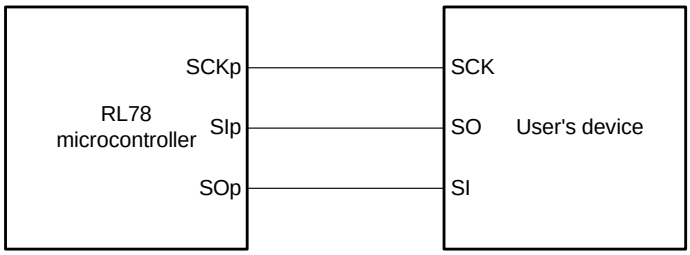
(T_A = -40 to +85°C, 2.4 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		Unit
				MIN.	MAX.	
$\overline{SSI00}$ setup time	t_{SSIK}	DAPmn = 0	2.7 V ≤ V_{DD} ≤ 5.5 V	120		ns
			2.4 V ≤ V_{DD} ≤ 5.5 V	200		ns
		DAPmn = 1	2.7 V ≤ V_{DD} ≤ 5.5 V	1/f_{MCK} + 120		ns
			2.4 V ≤ V_{DD} ≤ 5.5 V	1/f_{MCK} + 200		ns
$\overline{SSI00}$ hold time	t_{KSSI}	DAPmn = 0	2.7 V ≤ V_{DD} ≤ 5.5 V	1/f_{MCK} + 120		ns
			2.4 V ≤ V_{DD} ≤ 5.5 V	1/f_{MCK} + 200		ns
		DAPmn = 1	2.7 V ≤ V_{DD} ≤ 5.5 V	120		ns
			2.4 V ≤ V_{DD} ≤ 5.5 V	200		ns

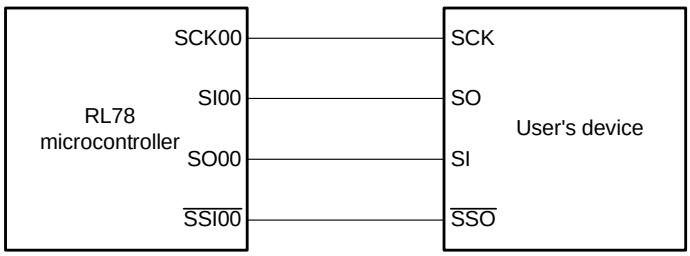
Caution **Select the normal input buffer for the SIp pin and SCKp pin and the normal output mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg).**

Remark p: CSI number (p = 00), m: Unit number (m = 0), n: Channel number (n = 0), g: PIM and POM number (g = 3, 4)

Simplified SPI(CSI) mode connection diagram (during communication at same potential)

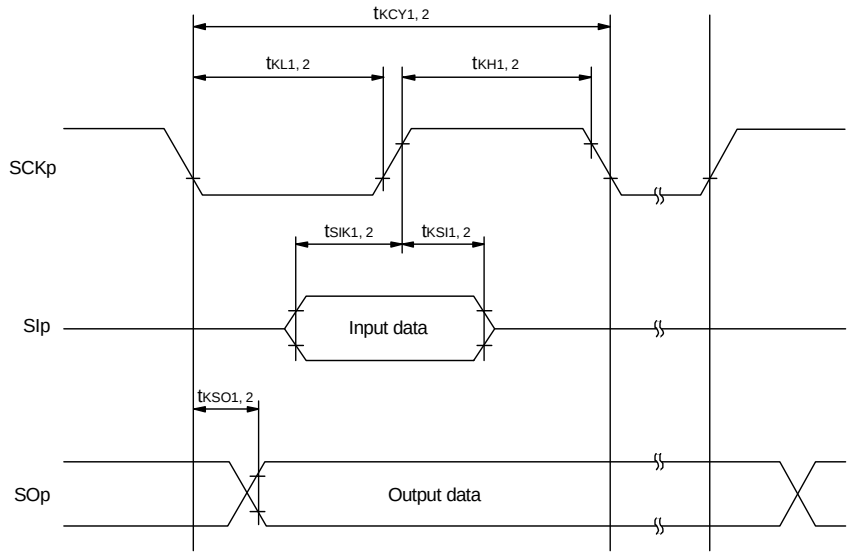


Simplified SPI(CSI) mode connection diagram (during communication at same potential)
(Slave Transmission of slave select input function (CSI00))

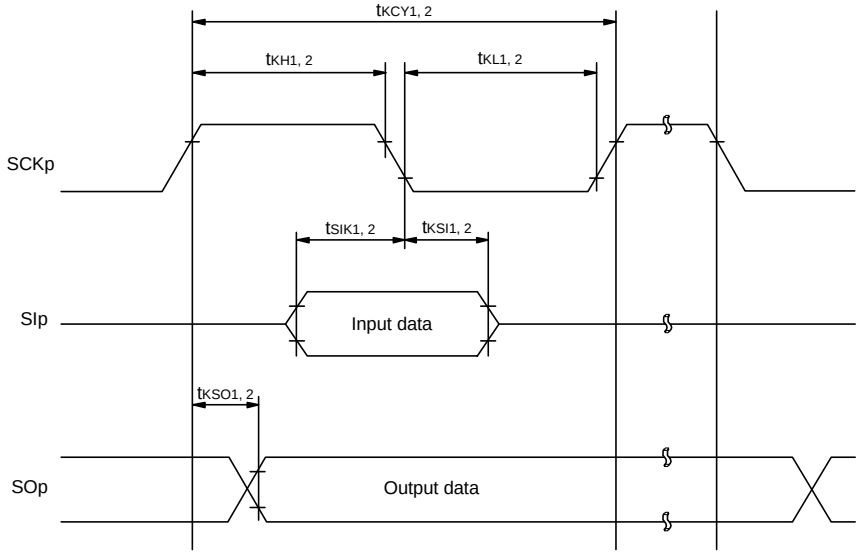


Remark p: CSI number (p = 00, 10, 20), m: Unit number (m = 0, 1), n: Channel number (n = 0, 2)

Simplified SPI(CSI) mode serial transfer timing (during communication at same potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)



Simplified SPI(CSI) mode serial transfer timing (during communication at same potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)



Remark p: CSI number (p = 00, 10, 20), m: Unit number (m = 0, 1), n: Channel number (n = 0, 2)

(4) During communication at same potential (simplified I²C mode)

(T_A = -40 to +85°C, 2.4 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V)

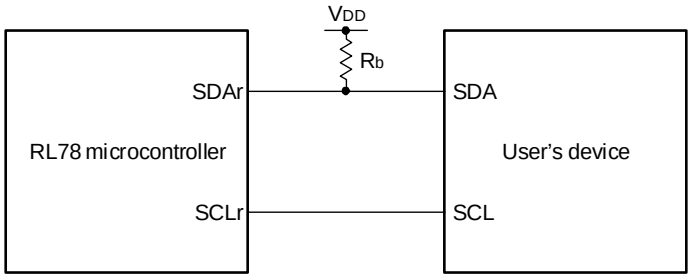
Parameter	Symbol	Conditions	HS (high-speed main) Mode		Unit
			MIN.	MAX.	
SCLr clock frequency	f_{SCL}	2.7 V ≤ V_{DD} ≤ 5.5 V, C_b = 50 pF, R_b = 2.7 kΩ		1000 Note 1	kHz
		2.4 V ≤ V_{DD} ≤ 5.5 V, C_b = 100 pF, R_b = 3 kΩ		400 Note 1	kHz
		2.4 V ≤ V_{DD} < 2.7 V, C_b = 100 pF, R_b = 5 kΩ		300 Note 1	kHz
Hold time when SCLr = “L”	t_{LOW}	2.7 V ≤ V_{DD} ≤ 5.5 V, C_b = 50 pF, R_b = 2.7 kΩ	475		ns
		2.4 V ≤ V_{DD} ≤ 5.5 V, C_b = 100 pF, R_b = 3 kΩ	1150		ns
		2.4 V ≤ V_{DD} < 2.7 V, C_b = 100 pF, R_b = 5 kΩ	1550		ns
Hold time when SCLr = “H”	t_{HIGH}	2.7 V ≤ V_{DD} ≤ 5.5 V, C_b = 50 pF, R_b = 2.7 kΩ	475		ns
		2.4 V ≤ V_{DD} ≤ 5.5 V, C_b = 100 pF, R_b = 3 kΩ	1150		ns
		2.4 V ≤ V_{DD} < 2.7 V, C_b = 100 pF, R_b = 5 kΩ	1550		ns
Data setup time (reception)	$t_{SU: DAT}$	2.7 V ≤ V_{DD} ≤ 5.5 V, C_b = 50 pF, R_b = 2.7 kΩ	1/f_{MCK} + 85 Note 2		ns
		2.4 V ≤ V_{DD} ≤ 5.5 V, C_b = 100 pF, R_b = 3 kΩ	1/f_{MCK} + 145 Note 2		ns
		2.4 V ≤ V_{DD} < 2.7 V, C_b = 100 pF, R_b = 5 kΩ	1/f_{MCK} + 230 Note 2		ns
Data hold time (transmission)	$t_{HD: DAT}$	2.7 V ≤ V_{DD} ≤ 5.5 V, C_b = 50 pF, R_b = 2.7 kΩ	0	305	ns
		2.4 V ≤ V_{DD} ≤ 5.5 V, C_b = 100 pF, R_b = 3 kΩ	0	355	ns
		2.4 V ≤ V_{DD} < 2.7 V, C_b = 100 pF, R_b = 5 kΩ	0	405	ns

Note 1. The value must be equal to or less than f_{MCK}/4.

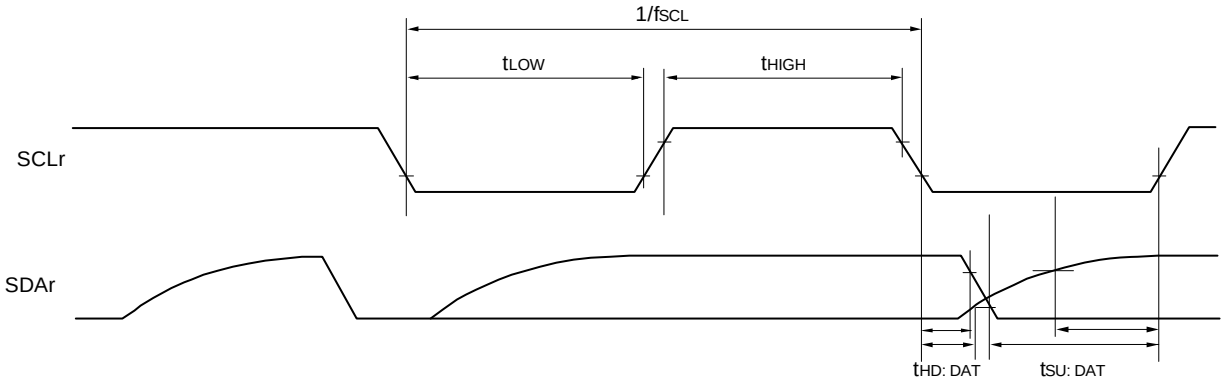
Note 2. Set the f_{MCK} value to keep the hold time of SCLr = “L” and SCLr = “H”.

Caution Select the normal input buffer and the N-ch open drain output (V_{DD} tolerance) mode for the SDAr pin and the normal output mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register h (POMh).

Simplified I²C mode connection diagram (during communication at same potential)



Simplified I²C mode serial transfer timing (during communication at same potential)



Remark 1. R_b[Ω]: Communication line (SDAr) pull-up resistance, C_b[F]: Communication line (SCLr, SDAr) load capacitance

Remark 2. r: IIC number (r = 00, 10, 20), g: PIM number (g = 0, 1, 3, 4, 5, 8),

Remark 3. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number (m = 0, 1), n: Channel number (n = 0, 2), mn = 00, 02, 10)

(5) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode) (1/2)

(T_A = -40 to +85°C, 2.4 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		Unit
				MIN.	MAX.	
Transfer rate		reception	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V		f_{MCK}/6 Note 1	bps
			Theoretical value of the maximum transfer rate f_{MCK} = f_{CLK} Note 4		4.0	Mbps
			2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V		f_{MCK}/6 Note 1	bps
			Theoretical value of the maximum transfer rate f_{MCK} = f_{CLK} Note 4		4.0	Mbps
			2.4 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V		f_{MCK}/6 Notes 1, 2, 3	bps
			Theoretical value of the maximum transfer rate f_{MCK} = f_{CLK} Note 4		4.0	Mbps

Note 1. Transfer rate in the SNOOZE mode is 4,800 bps only.

Note 2. Use it with V_{DD} ≥ V_b.

Note 3. The following conditions are required for low voltage interface.
2.4 V ≤ V_{DD} < 2.7 V: MAX. 2.6 Mbps

Note 4. The maximum operating frequencies of the CPU/peripheral hardware clock (f_{CLK}) are:
HS (high-speed main) mode: 24 MHz (2.7 V ≤ V_{DD} ≤ 5.5 V)
16 MHz (2.4 V ≤ V_{DD} ≤ 5.5 V)

Caution Select the TTL input buffer for the RxDq pin and the N-ch open drain output (V_{DD} tolerance) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

Remark 1. V_b[V]: Communication line voltage

Remark 2. q: UART number (q = 0 to 2), g: PIM and POM number (g = 0, 1, 3, 4, 5, 8)

Remark 3. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03, 10, 11))

(5) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode) (2/2)

(T_A = -40 to +85°C, 2.4 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		Unit
				MIN.	MAX.	
Transfer rate		transmission	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V		Note 1	bps
			Theoretical value of the maximum transfer rate C_b = 50 pF, R_b = 1.4 kΩ, V_b = 2.7 V		2.8 Note 2	Mbps
			2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V		Note 3	bps
			Theoretical value of the maximum transfer rate C_b = 50 pF, R_b = 2.7 kΩ, V_b = 2.3 V		1.2 Note 4	Mbps
			2.4 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V		Notes 5, 6	bps
			Theoretical value of the maximum transfer rate C_b = 50 pF, R_b = 5.5 kΩ, V_b = 1.6 V		0.43 Note 7	Mbps

Note 1. The smaller maximum transfer rate derived by using f_{MCK}/6 or the following expression is the valid maximum transfer rate.
Expression for calculating the transfer rate when 4.0 V ≤ V_{DD} ≤ 5.5 V and 2.7 V ≤ V_b ≤ 4.0 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.2}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.2}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [\%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

Note 2. This value as an example is calculated when the conditions described in the “Conditions” column are met.
Refer to Note 1 above to calculate the maximum transfer rate under conditions of the customer.

Note 3. The smaller maximum transfer rate derived by using f_{MCK}/6 or the following expression is the valid maximum transfer rate.
Expression for calculating the transfer rate when 2.7 V ≤ V_{DD} ≤ 4.0 V and 2.3 V ≤ V_b ≤ 2.7 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [\%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

Note 4. This value as an example is calculated when the conditions described in the “Conditions” column are met.
Refer to Note 3 above to calculate the maximum transfer rate under conditions of the customer.

Note 5. Use it with V_{DD} ≥ V_b.

Note 6. The smaller maximum transfer rate derived by using f_{MCK}/6 or the following expression is the valid maximum transfer rate.
Expression for calculating the transfer rate when 2.4 V ≤ V_{DD} < 3.3 V and 1.6 V ≤ V_b ≤ 2.0 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\} \times 3} \text{ [bps]}$$

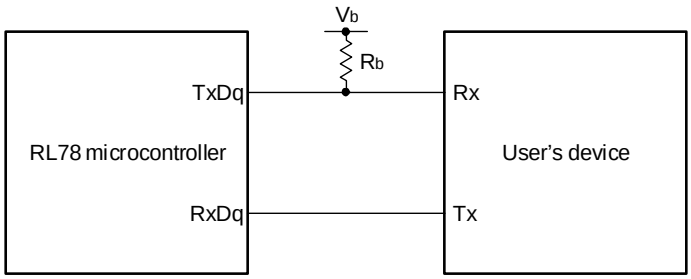
$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [\%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

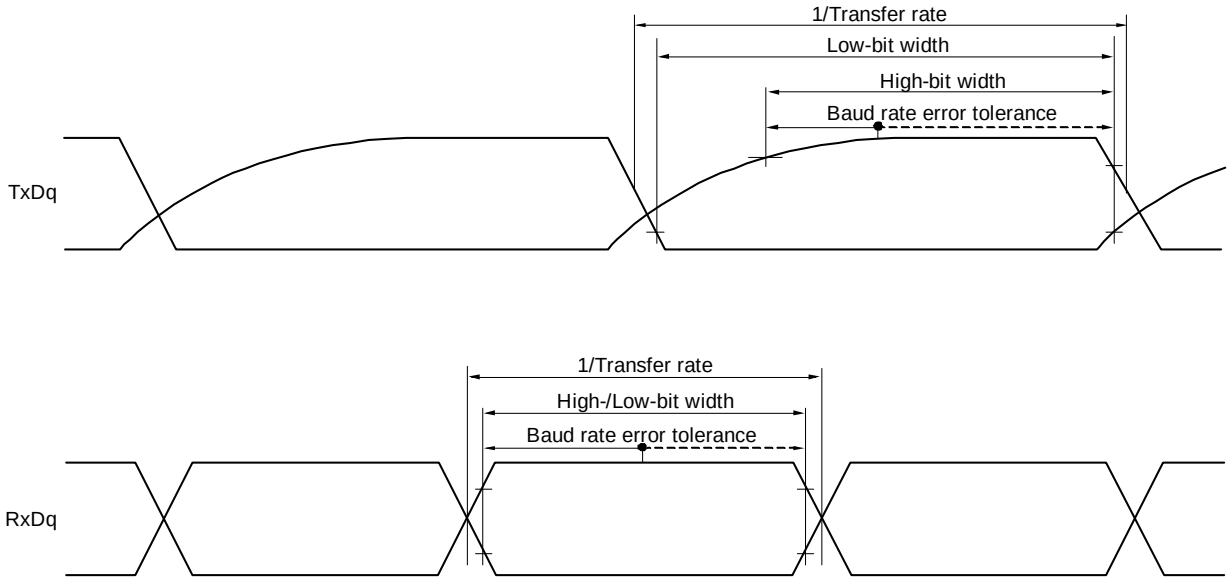
Note 7. This value as an example is calculated when the conditions described in the “Conditions” column are met.
Refer to Note 6 above to calculate the maximum transfer rate under conditions of the customer.

Caution Select the TTL input buffer for the RxDq pin and the N-ch open drain output (V_{DD} tolerance) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

UART mode connection diagram (during communication at different potential)



UART mode bit width (during communication at different potential) (reference)



Remark 1. R_b[Ω]: Communication line (TxDq) pull-up resistance, C_b[F]: Communication line (TxDq) load capacitance, V_b[V]: Communication line voltage

Remark 2. q: UART number (q = 0 to 2), g: PIM and POM number (g = 0, 1, 3, 4, 5, 8)

Remark 3. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03, 10, 11))

(6) Communication at different potential (1.8 V, 2.5 V, 3 V) (Simplified SPI(CSI) mode) (master mode, SCKp... internal clock output) (1/2)

(T_A = -40 to +85°C, 2.4 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		Unit
				MIN.	MAX.	
SCKp cycle time	t_{KCY1}	t_{KCY1} ≥ 4/f_{CLK}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ	300		ns
			2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	500 Note		ns
			2.4 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V, C_b = 30 pF, R_b = 5.5 kΩ	1150 Note		ns
SCKp high-level width	t_{KH1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ		t_{KCY1}/2 - 75		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ		t_{KCY1}/2 - 170		ns
		2.4 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V, C_b = 30 pF, R_b = 5.5 kΩ		t_{KCY1}/2 - 458		ns
SCKp low-level width	t_{KL1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ		t_{KCY1}/2 - 12		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ		t_{KCY1}/2 - 18		ns
		2.4 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V, C_b = 30 pF, R_b = 5.5 kΩ		t_{KCY1}/2 - 50		ns

Note Use it with V_{DD} ≥ V_b.

Caution Select the TTL input buffer for the SIp pin and the N-ch open drain output (V_{DD} tolerance) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

(**Remarks** are listed on the page after the next page.)

(6) Communication at different potential (1.8 V, 2.5 V, 3 V) (Simplified SPI(CSI) mode) (master mode, SCKp... internal clock output) (2/2)

(T_A = -40 to +85°C, 2.4 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		Unit
			MIN.	MAX.	
SIp setup time (to SCKp↑) Note 1	t_{SIK1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ	81		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	177		ns
		2.4 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 3, C_b = 30 pF, R_b = 5.5 kΩ	479		ns
SIp hold time (from SCKp↑) Note 1	t_{KSI1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ	19		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	19		ns
		2.4 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 3, C_b = 30 pF, R_b = 5.5 kΩ	19		ns
Delay time from SCKp↓ to SOp output Note 1	t_{KSO1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ		100	ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ		195	ns
		2.4 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 3, C_b = 30 pF, R_b = 5.5 kΩ		483	ns
SIp setup time (to SCKp↓) Note 2	t_{SIK1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ	44		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	44		ns
		2.4 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 3, C_b = 30 pF, R_b = 5.5 kΩ	110		ns
SIp hold time (from SCKp↓) Note 2	t_{KSI1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ	19		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	19		ns
		2.4 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 3, C_b = 30 pF, R_b = 5.5 kΩ	19		ns
Delay time from SCKp↑ to SOp output Note 2	t_{KSO1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ		25	ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ		25	ns
		2.4 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 3, C_b = 30 pF, R_b = 5.5 kΩ		25	ns

Note 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.

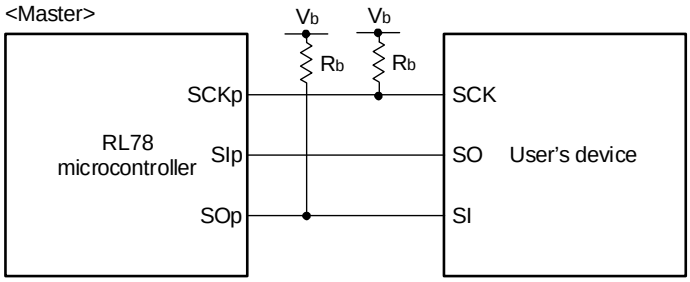
Note 2. When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 3. Use it with V_{DD} ≥ V_b.

Caution Select the TTL input buffer for the SIp pin and the N-ch open drain output (V_{DD} tolerance) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

(**Remarks** are listed on the next page.)

Simplified SPI(CSI) mode connection diagram (during communication at different potential)

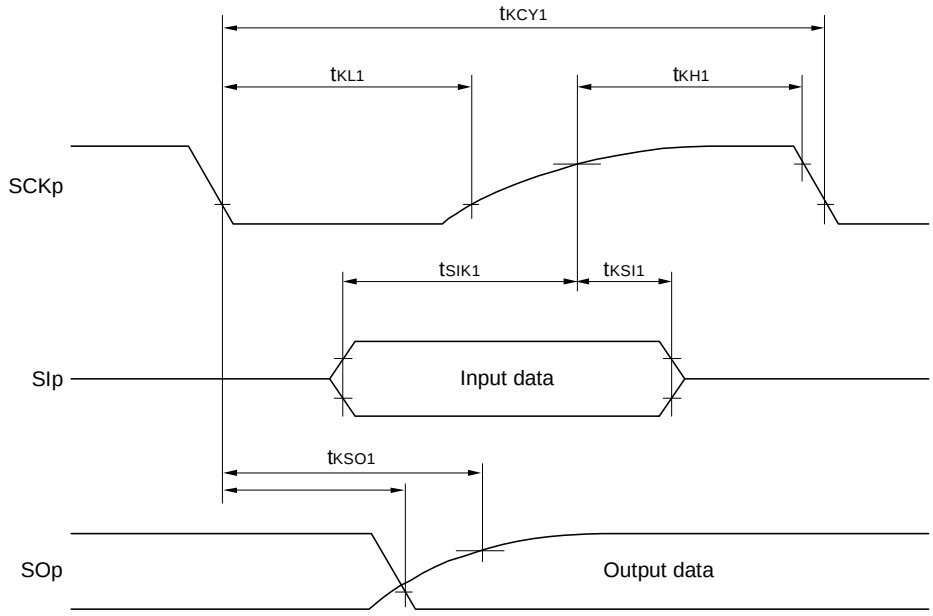


Remark 1. R_b[Ω]: Communication line (SCKp, SOp) pull-up resistance, C_b[F]: Communication line (SCKp, SOp) load capacitance, V_b[V]: Communication line voltage

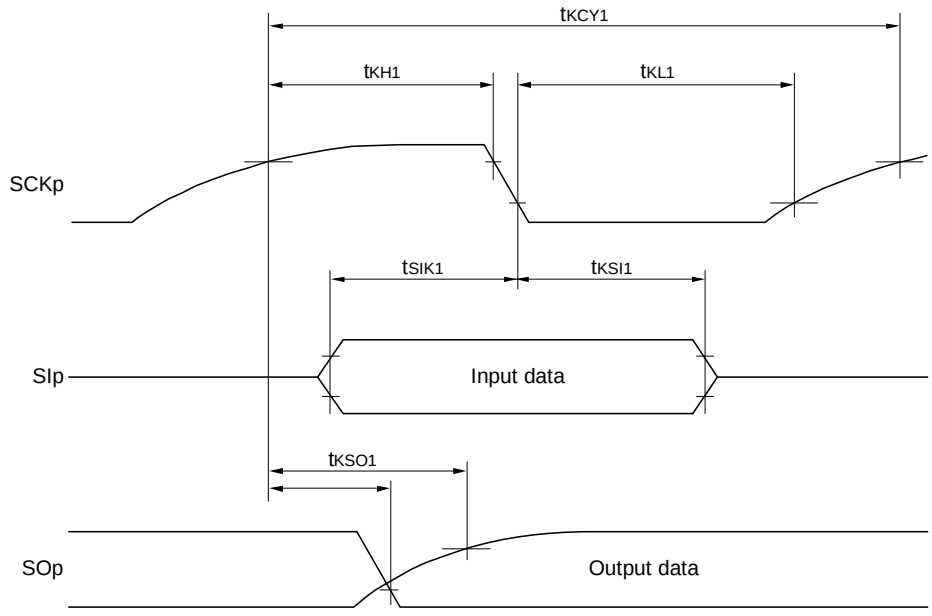
Remark 2. p: CSI number (p = 00, 10, 20), m: Unit number (m = 0, 1), n: Channel number (n = 0, 2), g: PIM and POM number (g = 0, 1, 3, 4, 5, 8)

Remark 3. f_{MCK}: Serial array unit operation clock frequency (Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00, 02, 10))

Simplified SPI(CSI) mode serial transfer timing (master mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)



Simplified SPI(CSI) mode serial transfer timing (master mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)



Remark p: CSI number (p = 00, 10, 20), m: Unit number (m = 0, 1), n: Channel number (n = 0, 2),
g: PIM and POM number (g = 0, 1, 3, 4, 5, 8)

(7) Communication at different potential (1.8 V, 2.5 V, 3 V) (Simplified SPI(CSI) mode) (slave mode, SCKp... external clock input)

(T_A = -40 to +85°C, 2.4 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		Unit
				MIN.	MAX.	
SCKp cycle time Note 1	t_{KCY2}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V	20 MHz < f_{MCK}	12/f_{MCK}		ns
			8 MHz < f_{MCK} ≤ 20 MHz	10/f_{MCK}		ns
			4 MHz < f_{MCK} ≤ 8 MHz	8/f_{MCK}		ns
			f_{MCK} ≤ 4 MHz	6/f_{MCK}		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V	20 MHz < f_{MCK}	16/f_{MCK}		ns
			16 MHz < f_{MCK} ≤ 20 MHz	14/f_{MCK}		ns
			8 MHz < f_{MCK} ≤ 16 MHz	12/f_{MCK}		ns
			4 MHz < f_{MCK} ≤ 8 MHz	8/f_{MCK}		ns
			f_{MCK} ≤ 4 MHz	6/f_{MCK}		ns
		2.4 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 2	20 MHz < f_{MCK}	36/f_{MCK}		ns
			16 MHz < f_{MCK} ≤ 20 MHz	32/f_{MCK}		ns
			8 MHz < f_{MCK} ≤ 16 MHz	26/f_{MCK}		ns
			4 MHz < f_{MCK} ≤ 8 MHz	16/f_{MCK}		ns
			f_{MCK} ≤ 4 MHz	10/f_{MCK}		ns
SCKp high-/low-level width	t_{KH2}, t_{KL2}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V		t_{KCY2}/2 - 12		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V		t_{KCY2}/2 - 18		ns
		2.4 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 2		t_{KCY2}/2 - 50		ns
SIp setup time (to SCKp↑) Note 3	t_{SIK2}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V		1/f_{MCK} + 20		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V		1/f_{MCK} + 20		ns
		2.4 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 2		1/f_{MCK} + 30		ns
SIp hold time (from SCKp↑) Note 4	t_{KSI2}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V		1/f_{MCK} + 31		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V		1/f_{MCK} + 31		ns
		2.4 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 2		1/f_{MCK} + 31		ns
Delay time from SCKp↓ to SOp output Note 5	t_{KSO2}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V C_b = 30 pF, R_b = 1.4 kΩ			2/f_{MCK} + 120	ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V C_b = 30 pF, R_b = 2.7 kΩ			2/f_{MCK} + 214	ns
		2.4 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 2 C_b = 30 pF, R_b = 5.5 kΩ			2/f_{MCK} + 573	ns

Note 1. Transfer rate in the SNOOZE mode: MAX. 1 Mbps

Note 2. Use it with V_{DD} ≥ V_b.

Note 3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes “to SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

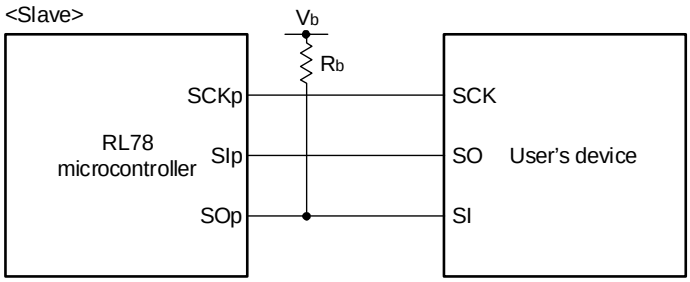
Note 4. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes “from SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 5. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes “from SCKp↑” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Caution Select the TTL input buffer for the SIp pin and SCKp pin and the N-ch open drain output (V_{DD} tolerance) mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

(**Remarks** are listed on the next page.)

Simplified SPI(CSI) mode connection diagram (during communication at different potential)

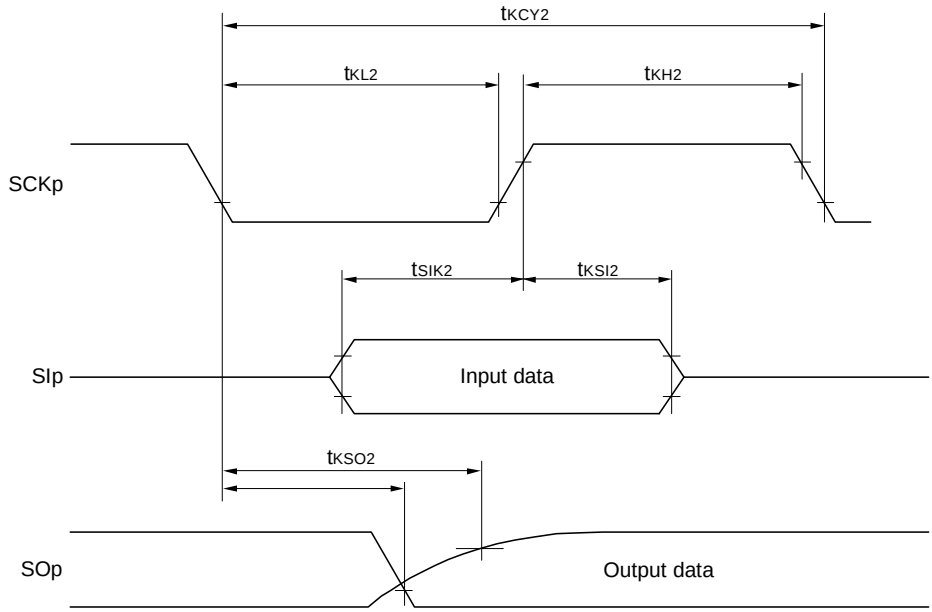


Remark 1. R_b[Ω]: Communication line (SOp) pull-up resistance, C_b[F]: Communication line (SOp) load capacitance, V_b[V]: Communication line voltage

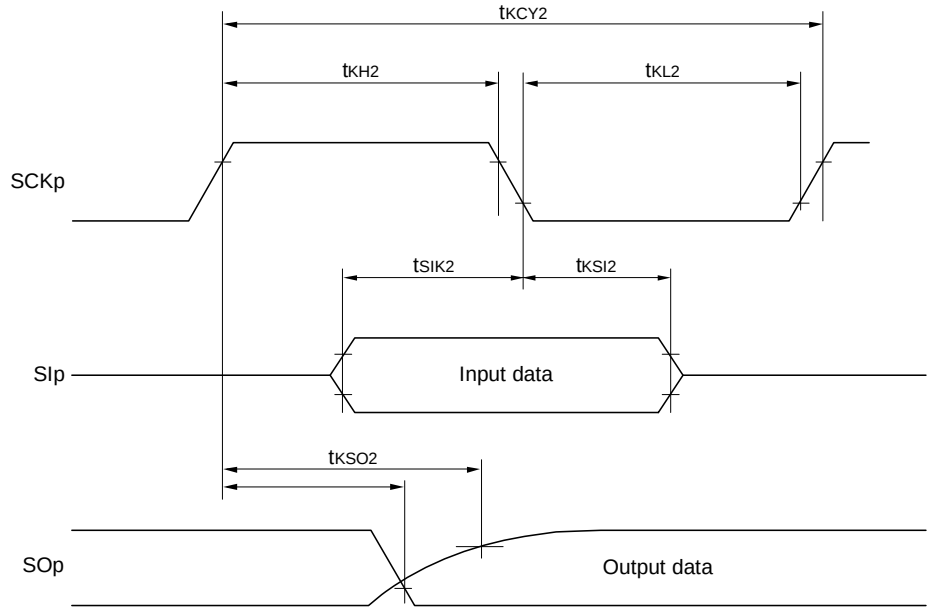
Remark 2. p: CSI number (p = 00, 10, 20), m: Unit number (m = 0, 1), n: Channel number (n = 0, 2), g: PIM and POM number (g = 0, 1, 3, 4, 5, 8)

Remark 3. f_{MCK}: Serial array unit operation clock frequency (Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00, 02, 10))

Simplified SPI(CSI) mode serial transfer timing (slave mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)



Simplified SPI(CSI) mode serial transfer timing (slave mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)



Remark p: CSI number (p = 00, 10, 20), m: Unit number (m = 0, 1),
n: Channel number (n = 0, 2), g: PIM and POM number (g = 0, 1, 3, 4, 5, 8)

(8) Communication at different potential (1.8 V, 2.5 V, 3 V) (simplified I^2C mode)

(T_A = -40 to +85°C, 2.4 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		Unit
			MIN.	MAX.	
SCLr clock frequency	f_{SCL}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 50 pF, R_b = 2.7 kΩ		1000 Note 1	kHz
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 50 pF, R_b = 2.7 kΩ		1000 Note 1	kHz
		4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 100 pF, R_b = 2.8 kΩ		400 Note 1	kHz
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 100 pF, R_b = 2.7 kΩ		400 Note 1	kHz
		2.4 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 2, C_b = 100 pF, R_b = 5.5 kΩ		400 Note 1	kHz
Hold time when SCLr = “L”	t_{LOW}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 50 pF, R_b = 2.7 kΩ	475		ns
		2.7 V ≤ V_{DD} ≤ 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 50 pF, R_b = 2.7 kΩ	475		ns
		4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 100 pF, R_b = 2.8 kΩ	1150		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 100 pF, R_b = 2.7 kΩ	1150		ns
		2.4 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 2, C_b = 100 pF, R_b = 5.5 kΩ	1550		ns
Hold time when SCLr = “H”	t_{HIGH}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 50 pF, R_b = 2.7 kΩ	245		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 50 pF, R_b = 2.7 kΩ	200		ns
		4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 100 pF, R_b = 2.8 kΩ	675		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 100 pF, R_b = 2.7 kΩ	600		ns
		2.4 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 2, C_b = 100 pF, R_b = 5.5 kΩ	610		ns
Data setup time (reception)	$t_{SU:DAT}$	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 50 pF, R_b = 2.7 kΩ	1/f_{MCK} + 135 Note 3		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 50 pF, R_b = 2.7 kΩ	1/f_{MCK} + 135 Note 3		ns
		4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 100 pF, R_b = 2.8 kΩ	1/f_{MCK} + 190 Note 3		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 100 pF, R_b = 2.7 kΩ	1/f_{MCK} + 190 Note 3		ns
		2.4 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 2, C_b = 100 pF, R_b = 5.5 kΩ	1/f_{MCK} + 190 Note 3		ns
Data hold time (transmission)	$t_{HD:DAT}$	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 50 pF, R_b = 2.7 kΩ	0	305	ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 50 pF, R_b = 2.7 kΩ	0	305	ns
		4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 100 pF, R_b = 2.8 kΩ	0	355	ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 100 pF, R_b = 2.7 kΩ	0	355	ns
		2.4 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 2, C_b = 100 pF, R_b = 5.5 kΩ	0	405	ns

Note 1. The value must also be equal to or less than f_{MCK}/4.

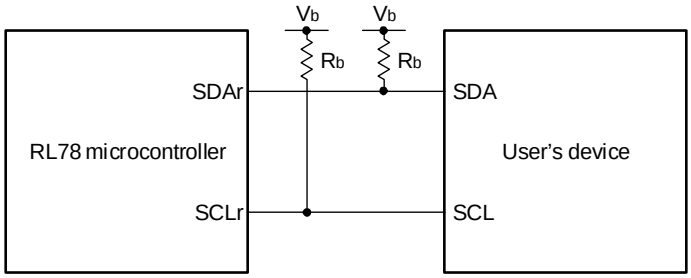
Note 2. Use it with V_{DD} ≥ V_b.

Note 3. Set the f_{MCK} value to keep the hold time of SCLr = “L” and SCLr = “H”.

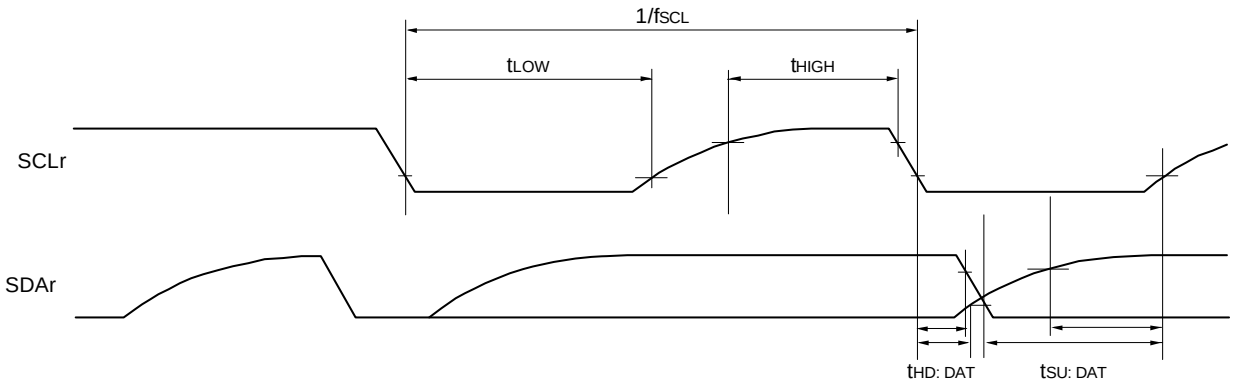
Caution Select the TTL input buffer and the N-ch open drain output (V_{DD} tolerance) mode for the SDAr pin and the N-ch open drain output (V_{DD} tolerance) mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

(**Remarks** are listed on the next page.)

Simplified I²C mode connection diagram (during communication at different potential)



Simplified I²C mode serial transfer timing (during communication at different potential)



Remark 1. R_b[Ω]: Communication line (SDAr, SCLr) pull-up resistance, C_b[F]: Communication line (SDAr, SCLr) load capacitance, V_b[V]: Communication line voltage

Remark 2. r: IIC number (r = 00, 10, 20), g: PIM, POM number (g = 0, 1, 3, 4, 5, 8)

Remark 3. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number (m = 0, 1), n: Channel number (n = 0, 2), mn = 00, 02, 10)

38.5.2 Serial interface IICA

(1) I^2C standard mode

(T_A = -40 to +85°C, 2.4 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		Unit
				MIN.	MAX.	
SCLA0 clock frequency	f_{SCL}	Standard mode: f_{CLK} ≥ 1 MHz	2.7 V ≤ V_{DD} ≤ 5.5 V	0	100	kHz
			2.4 V ≤ V_{DD} ≤ 5.5 V	0	100	kHz
Setup time of restart condition	$t_{SU:STA}$	2.7 V ≤ V_{DD} ≤ 5.5 V		4.7		µs
		2.4 V ≤ V_{DD} ≤ 5.5 V		4.7		µs
Hold time Note 1	$t_{HD:STA}$	2.7 V ≤ V_{DD} ≤ 5.5 V		4.0		µs
		2.4 V ≤ V_{DD} ≤ 5.5 V		4.0		µs
Hold time when SCLA0 = “L”	t_{LOW}	2.7 V ≤ V_{DD} ≤ 5.5 V		4.7		µs
		2.4 V ≤ V_{DD} ≤ 5.5 V		4.7		µs
Hold time when SCLA0 = “H”	t_{HIGH}	2.7 V ≤ V_{DD} ≤ 5.5 V		4.0		µs
		2.4 V ≤ V_{DD} ≤ 5.5 V		4.0		µs
Data setup time (reception)	$t_{SU:DAT}$	2.7 V ≤ V_{DD} ≤ 5.5 V		250		ns
		2.4 V ≤ V_{DD} ≤ 5.5 V		250		ns
Data hold time (transmission) Note 2	$t_{HD:DAT}$	2.7 V ≤ V_{DD} ≤ 5.5 V		0	3.45	µs
		2.4 V ≤ V_{DD} ≤ 5.5 V		0		µs
Setup time of stop condition	$t_{SU:STO}$	2.7 V ≤ V_{DD} ≤ 5.5 V		4.0		µs
		2.4 V ≤ V_{DD} ≤ 5.5 V		4.0		µs
Bus-free time	t_{BUF}	2.7 V ≤ V_{DD} ≤ 5.5 V		4.7		µs
		2.4 V ≤ V_{DD} ≤ 5.5 V		4.7		µs

Note 1. The first clock pulse is generated after this period when the start/restart condition is detected.

Note 2. The maximum value (MAX.) of $t_{HD:DAT}$ is during normal transfer and a clock stretch state is inserted in the ACK (acknowledge) timing.

Remark The maximum value of C_b (communication line capacitance) and the value of R_b (communication line pull-up resistor) at that time in each mode are as follows.
Standard mode: C_b = 400 pF, R_b = 2.7 kΩ

(2) I^2C fast mode

(T_A = -40 to +85°C, 2.4 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		Unit
				MIN.	MAX.	
SCLA0 clock frequency	f_{SCL}	Fast mode: f_{CLK} ≥ 3.5 MHz	2.7 V ≤ V_{DD} ≤ 5.5 V	0	400	kHz
			2.4 V ≤ V_{DD} ≤ 5.5 V	0	400	kHz
Setup time of restart condition	$t_{SU: STA}$	2.7 V ≤ V_{DD} ≤ 5.5 V		0.6		µs
		2.4 V ≤ V_{DD} ≤ 5.5 V		0.6		µs
Hold time Note 1	$t_{HD: STA}$	2.7 V ≤ V_{DD} ≤ 5.5 V		0.6		µs
		2.4 V ≤ V_{DD} ≤ 5.5 V		0.6		µs
Hold time when SCLA0 = “L”	t_{LOW}	2.7 V ≤ V_{DD} ≤ 5.5 V		1.3		µs
		2.4 V ≤ V_{DD} ≤ 5.5 V		1.3		µs
Hold time when SCLA0 = “H”	t_{HIGH}	2.7 V ≤ V_{DD} ≤ 5.5 V		0.6		µs
		2.4 V ≤ V_{DD} ≤ 5.5 V		0.6		µs
Data setup time (reception)	$t_{SU: DAT}$	2.7 V ≤ V_{DD} ≤ 5.5 V		100		ns
		2.4 V ≤ V_{DD} ≤ 5.5 V		100		ns
Data hold time (transmission) Note 2	$t_{HD: DAT}$	2.7 V ≤ V_{DD} ≤ 5.5 V		0	0.9	µs
		2.4 V ≤ V_{DD} ≤ 5.5 V		0		µs
Setup time of stop condition	$t_{SU: STO}$	2.7 V ≤ V_{DD} ≤ 5.5 V		0.6		µs
		2.4 V ≤ V_{DD} ≤ 5.5 V		0.6		µs
Bus-free time	t_{BUF}	2.7 V ≤ V_{DD} ≤ 5.5 V		1.3		µs
		2.4 V ≤ V_{DD} ≤ 5.5 V		1.3		µs

Note 1. The first clock pulse is generated after this period when the start/restart condition is detected.

Note 2. The maximum value (MAX.) of $t_{HD: DAT}$ is during normal transfer and a clock stretch state is inserted in the ACK (acknowledge) timing.

Remark The maximum value of C_b (communication line capacitance) and the value of R_b (communication line pull-up resistor) at that time in each mode are as follows.
Fast mode: C_b = 320 pF, R_b = 1.1 kΩ

(3) I^2C fast mode plus

(T_A = -40 to +85°C, 2.4 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V)

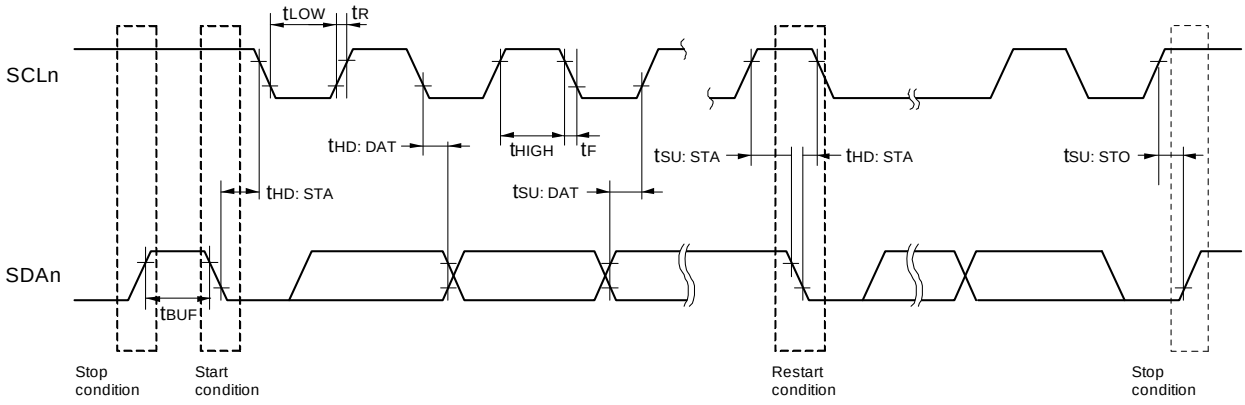
Parameter	Symbol	Conditions		HS (high-speed main) Mode		Unit
				MIN.	MAX.	
SCLA0 clock frequency	f_{SCL}	Fast mode plus: f_{CLK} ≥ 10 MHz	2.7 V ≤ V_{DD} ≤ 5.5 V	0	1000	kHz
Setup time of restart condition	$t_{SU: STA}$	2.7 V ≤ V_{DD} ≤ 5.5 V		0.26		µs
Hold time Note 1	$t_{HD: STA}$	2.7 V ≤ V_{DD} ≤ 5.5 V		0.26		µs
Hold time when SCLA0 = “L”	t_{LOW}	2.7 V ≤ V_{DD} ≤ 5.5 V		0.5		µs
Hold time when SCLA0 = “H”	t_{HIGH}	2.7 V ≤ V_{DD} ≤ 5.5 V		0.26		µs
Data setup time (reception)	$t_{SU: DAT}$	2.7 V ≤ V_{DD} ≤ 5.5 V		50		ns
Data hold time (transmission) Note 2	$t_{HD: DAT}$	2.7 V ≤ V_{DD} ≤ 5.5 V		0	0.45	µs
Setup time of stop condition	$t_{SU: STO}$	2.7 V ≤ V_{DD} ≤ 5.5 V		0.26		µs
Bus-free time	t_{BUF}	2.7 V ≤ V_{DD} ≤ 5.5 V		0.5		µs

Note 1. The first clock pulse is generated after this period when the start/restart condition is detected.

Note 2. The maximum value (MAX.) of $t_{HD: DAT}$ is during normal transfer and a clock stretch state is inserted in the ACK (acknowledge) timing.

Remark The maximum value of C_b (communication line capacitance) and the value of R_b (communication line pull-up resistor) at that time in each mode are as follows.
Fast mode plus: C_b = 120 pF, R_b = 1.1 kΩ

IICA serial transfer timing



38.6 Analog Characteristics

38.6.1 A/D converter characteristics

(1) When reference voltage (+) = V_{DD} (ADREFP1 = 0, ADREFP0 = 0), reference voltage (-) = V_{SS} (ADREFM = 0), target pin: ANI8 to ANI14, internal reference voltage, and temperature sensor output voltage

(T_A = –40 to +85°C, 2.4 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V, reference voltage (+) = V_{DD}, reference voltage (–) = V_{SS})

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8		10	bit
Overall error Note 1	AINL	10-bit resolution	2.4 V ≤ V_{DD} ≤ 5.5 V		1.2	±7.0	LSB
Conversion time	tCONV	10-bit resolution Target pin: ANI8 to ANI14	3.6 V ≤ V_{DD} ≤ 5.5 V	2.125		39	μs
			2.7 V ≤ V_{DD} ≤ 5.5 V	3.1875		39	μs
			2.4 V ≤ V_{DD} ≤ 5.5 V	17		39	μs
		10-bit resolution Target pin: internal reference voltage and temperature sensor output voltage (HS (high-speed main) mode)	3.6 V ≤ V_{DD} ≤ 5.5 V	2.375		39	μs
			2.7 V ≤ V_{DD} ≤ 5.5 V	3.5626		39	μs
			2.4 V ≤ V_{DD} ≤ 5.5 V	17		39	μs
Zero-scale error Notes 1, 2	EZS	10-bit resolution	2.4 V ≤ V_{DD} ≤ 5.5 V			±0.60	%FSR
Full-scale error Notes 1, 2	EFS	10-bit resolution	2.4 V ≤ V_{DD} ≤ 5.5 V			±0.60	%FSR
Integral linearity error Note 1	ILE	10-bit resolution	2.4 V ≤ V_{DD} ≤ 5.5 V			±4.0	LSB
Differential linearity error Note 1	DLE	10-bit resolution	2.4 V ≤ V_{DD} ≤ 5.5 V			±2.0	LSB
Analog input voltage	VAIN	ANI8 to ANI11		0		V_{DD}	V
		ANI12 to ANI14		0		AV_{DD}	V
		Internal reference voltage (2.4 V ≤ V_{DD} ≤ 5.5 V, HS (high-speed main) mode)		V_{BGR} Note 3			V
		Temperature sensor output voltage (2.4 V ≤ V_{DD} ≤ 5.5 V, HS (high-speed main) mode)		V_{TMPS25} Note 3			V

Note 1. Excludes quantization error (±1/2 LSB).

Note 2. This value is indicated as a ratio (%FSR) to the full-scale value.

Note 3. Refer to **38.6.2 Temperature sensor/internal reference voltage output characteristics**.

(2) When reference voltage (+) = Internal reference voltage (ADREFP1 = 1, ADREFP0 = 0), reference voltage (-) = V_{SS} (ADREFM = 0), target pin: ANI8 to ANI11, ANI12 to ANI14

(T_A = -40 to +85°C, 2.4 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V, reference voltage (+) = V_{BGR} Note 3, reference voltage (–) = V_{SS} = 0 V, HS (high-speed main) mode)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8			bit
Conversion time	t_{CONV}	8-bit resolution	2.4 V ≤ V_{DD} ≤ 5.5 V	17		39	µs
Zero-scale error Notes 1, 2	E_{ZS}	8-bit resolution	2.4 V ≤ V_{DD} ≤ 5.5 V			±(0.60 + 0.35)	%FSR
Integral linearity error Note 1	ILE	8-bit resolution	2.4 V ≤ V_{DD} ≤ 5.5 V			±(2.0 + 0.5)	LSB
Differential linearity error Note 1	DLE	8-bit resolution	2.4 V ≤ V_{DD} ≤ 5.5 V			±(1.0 + 0.2)	LSB
Analog input voltage	V_{AIN}			0		V_{BGR} Note 3	V

Note 1. Excludes quantization error (±1/2 LSB).
Note 2. This value is indicated as a ratio (%FSR) to the full-scale value.
Note 3. Refer to **38.6.2 Temperature sensor/internal reference voltage output characteristics**.

38.6.2 Temperature sensor/internal reference voltage output characteristics

(T_A = -40 to +85°C, 2.4 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V, HS (high-speed main) mode)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Temperature sensor output voltage	V_{TMPS25}	T_A = +25°C		1.05		V
Internal reference voltage	V_{BGR}		1.38	1.45	1.5	V
Temperature coefficient	F_{VTMPS}	Temperature sensor output voltage that depends on the temperature		-3.6		mV/°C
Operation stabilization wait time	t_{AMP}	2.4 V ≤ V_{DD} ≤ 5.5 V	5			µs

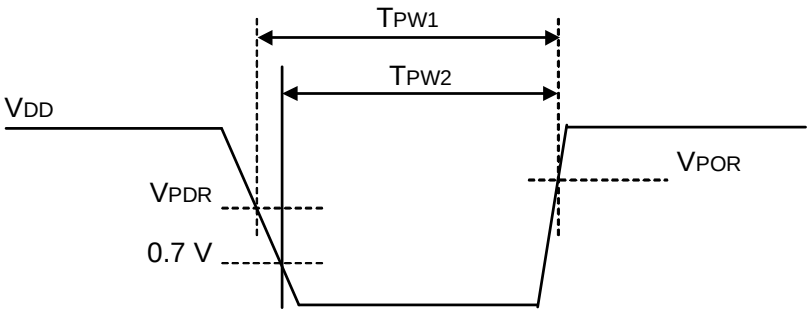
38.6.3 POR circuit characteristics

(T_A = -40 to +85°C, Vss = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	V_{POR}	Power supply rise time	1.47	1.51	1.55	V
	V_{PDR}	Power supply fall time Note 1	1.46	1.50	1.54	V
Minimum pulse width Note 2	T_{PW1}	Other than STOP/SUB HALT/SUB RUN	300			µs
	T_{PW2}	STOP/SUB HALT/SUB RUN	300			µs

Note 1. If the power supply voltage falls while the voltage detector is off, be sure to either shift to STOP mode or execute a reset by using the voltage detector or external reset pin before the power supply voltage falls below the minimum operating voltage specified in 38.4 AC Characteristics.

Note 2. Minimum time required for a POR reset when V_{DD} falls below V_{PDR}. This is also the minimum time required for a POR reset from when V_{DD} exceeds below 0.7 V to when V_{DD} exceeds V_{POR} while STOP mode is entered or the main system clock is stopped through setting bit 0 (HIOSTOP) and bit 7 (MSTOP) in the clock operation status control register (CSC).



38.6.4 LVD circuit characteristics

(1) LVD Detection Voltage of Reset Mode and Interrupt Mode

(T_A = -40 to +85°C, $V_{PDR} \leq AV_{DD} = V_{DD} \leq 5.5$ V, $AV_{SS} = V_{SS}$ = 0 V)

Parameter		Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	Supply voltage level	V_{LVD0}	Power supply rise time	3.98	4.06	4.14	V
			Power supply fall time	3.90	3.98	4.06	V
		V_{LVD1}	Power supply rise time	3.68	3.75	3.82	V
			Power supply fall time	3.60	3.67	3.74	V
		V_{LVD2}	Power supply rise time	3.07	3.13	3.19	V
			Power supply fall time	3.00	3.06	3.12	V
		V_{LVD3}	Power supply rise time	2.96	3.02	3.08	V
			Power supply fall time	2.90	2.96	3.02	V
		V_{LVD4}	Power supply rise time	2.86	2.92	2.97	V
			Power supply fall time	2.80	2.86	2.91	V
		V_{LVD5}	Power supply rise time	2.76	2.81	2.87	V
			Power supply fall time	2.70	2.75	2.81	V
		V_{LVD6}	Power supply rise time	2.66	2.71	2.76	V
			Power supply fall time	2.60	2.65	2.70	V
		V_{LVD7}	Power supply rise time	2.56	2.61	2.66	V
			Power supply fall time	2.50	2.55	2.60	V
		V_{LVD8}	Power supply rise time	2.45	2.50	2.55	V
			Power supply fall time	2.40	2.45	2.50	V
Minimum pulse width		t_{LW}		300			µs
Detection delay time						300	µs

Caution Set the detection voltage (V_{LVD}) to be within the operating voltage range. The operating voltage range depends on the setting of the user option byte (000C2H/010C2H). The following shows the operating voltage range.
HS (high-speed main) mode: V_{DD} = 2.7 to 5.5 V @ 1 MHz to 24 MHz
V_{DD} = 2.4 to 5.5 V @ 1 MHz to 16 MHz

(2) LVD Detection Voltage of Interrupt & Reset Mode

(T_A = -40 to +85°C, $V_{PDR} \leq AV_{DD} = V_{DD} \leq 5.5$ V, $AV_{SS} = V_{SS}$ = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Interrupt and reset mode	V_{LVDC0}	V_{POC2}, V_{POC1}, V_{POC0} = 0, 1, 0, falling reset voltage: 2.4 V		2.40	2.45	2.50	V
	V_{LVDC1}	LVIS1, LVIS0 = 1, 0	Rising release reset voltage	2.56	2.61	2.66	V
			Falling interrupt voltage	2.50	2.55	2.60	V
	V_{LVDC2}	LVIS1, LVIS0 = 0, 1	Rising release reset voltage	2.66	2.71	2.76	V
			Falling interrupt voltage	2.60	2.65	2.70	V
	V_{LVDC3}	LVIS1, LVIS0 = 0, 0	Rising release reset voltage	3.68	3.75	3.82	V
			Falling interrupt voltage	3.60	3.67	3.74	V
	V_{LVDD0}	V_{POC2}, V_{POC1}, V_{POC0} = 0, 1, 1, falling reset voltage: 2.7 V		2.70	2.75	2.81	V
	V_{LVDD1}	LVIS1, LVIS0 = 1, 0	Rising release reset voltage	2.86	2.92	2.97	V
			Falling interrupt voltage	2.80	2.86	2.91	V
	V_{LVDD2}	LVIS1, LVIS0 = 0, 1	Rising release reset voltage	2.96	3.02	3.08	V
			Falling interrupt voltage	2.90	2.96	3.02	V
	V_{LVDD3}	LVIS1, LVIS0 = 0, 0	Rising release reset voltage	3.98	4.06	4.14	V
			Falling interrupt voltage	3.90	3.98	4.06	V

38.6.5 Programmable gain instrumentation amplifier and 24-bit ΔΣ A/D converter

(1) Analog input in differential input mode

(T_A = -40 to +85°C, 2.7 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V, normal mode: fs1 = 1 MHz, FDATA1 = 3.90625 ksps, low-power mode: fs2 = 0.125 MHz, FDATA2 = 488.28125 sps, SBIAS = 2.1 V, d_{OFR} = 0 mV, V_{COM} = 1.0 V, external clock input used)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Full-scale differential input voltage range	V_{ID}	V_{ID} = (PGA0xP - PGA0xN) (x = 0, 1)	—	±800 /G_{TOTAL0}	—	mV
Input voltage range	V_I		0.2	—	1.8	V
Common mode input voltage range	V_{COM}	d_{OFR} = 0 mV	0.2+(|V_{ID}|x G_{SET01})/2	—	1.8-(|V_{ID}|x G_{SET01})/2	V
Input bias current	I_{IN}	V_I = 1.0 V			±50	nA
Input offset current	I_{INO}	V_I = 1.0 V			±20	nA

(2) Analog input in single-ended input mode

(T_A = -40 to +85°C, 2.7 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V, normal mode: fs1 = 1 MHz, FDATA1 = 3.90625 ksps, low-power mode: fs2 = 0.125 MHz, FDATA2 = 488.28125 sps, SBIAS = 2.1 V, d_{OFR} = 0 mV, V_{COM} = 1.0 V, external clock input used)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input voltage range	V_I		0.2	—	1.8	V
Input bias current	I_{IN}	V_I = 1.0 V			±50	nA

(3) Programmable gain instrumentation amplifier and 24-bit ΔΣ A/D converter

(T_A = -40 to +85°C, 2.7 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V, normal mode: fs1 = 1 MHz, FDATA1 = 3.90625 ksps, low-power mode: fs2 = 0.125 MHz, FDATA2 = 488.28125 sps, SBIAS = 2.1 V, d_{OFR} = 0 mV, V_{COM} = 1.0 V, external clock input used, in differential input mode) (1/2)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution	RES				24	bit
Sampling frequency	fs1	Normal mode		1		MHz
	fs2	Low-power mode		0.125		MHz
Output data rate	f_{DATA1}	Normal mode	0.488		15.625	ksps
	f_{DATA2}	Low-power mode	61.035		1953.125	sps
Gain setting range	G_{TOTAL0}	G_{TOTAL0} = G_{SET01} x G_{SET02}	1		64	V/V
1st gain setting range	G_{SET01}			1, 2, 3, 4, 8		V/V
2nd gain setting range	G_{SET02}			1, 2, 4, 8		V/V
Offset adjustment bit range	d_{OFFB}			5		bit
Offset adjustment range	d_{OFR}	Referred to input	- 164/G_{SET01}		+ 164/G_{SET01}	mV
Offset adjustment steps	d_{OFS}	Referred to input		11/G_{SET01}		mV

(T_A = -40 to +85°C, 2.7 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V, normal mode: fs1 = 1 MHz, FDATA1 = 3.90625 ksps, low-power mode: fs2 = 0.125 MHz, FDATA2 = 488.28125 sps, SBIAS = 2.1 V, d_{OFR} = 0 mV, V_{COM} = 1.0 V, external clock input used, in differential input mode) (2/2)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Gain error	E_{G0}	T_A = 25°C G_{SET01} = 1, G_{SET02} = 1 Excluding SBIAS error		±0.2	±2.7	%
		T_A = 25°C G_{SET01} = 8, G_{SET02} = 4 Excluding SBIAS error		±0.1		%
Gain drift Note	dE_{G0}	G_{SET01} = 1, G_{SET02} = 1 Excluding SBIAS drift		(5.6)	(22.0)	ppm/°C
		G_{SET01} = 8, G_{SET02} = 4 Excluding SBIAS drift		(9.1)		ppm/°C
Offset error	E_{OS0}	T_A = 25°C G_{SET01} = 1, G_{SET02} = 1 Referred to input		±0.32	±2.90	mV
		T_A = 25°C G_{SET01} = 8, G_{SET02} = 4 Referred to input		±0.03		mV
Offset drift Note	dE_{OS}	G_{SET01} = 1, G_{SET02} = 1 Referred to input		(±0.02)	(±6.00)	µV/°C
		G_{SET01} = 8, G_{SET02} = 4 Referred to input		(±0.02)		µV/°C
SND ratio	SNDR	G_{SET01} = 1, G_{SET02} = 1, fin = 50 Hz Normal mode, Pin = -1 dBFS	(82)	(85)		dB
		G_{SET01} = 8, G_{SET02} = 4, fin = 50 Hz Normal mode, Pin = -1 dBFS	(73)	(80)		dB
Noise	Vn	G_{SET01} = 1, G_{SET02} = 1, OSR = 2048		(13)		µVRms
		G_{SET01} = 8, G_{SET02} = 4, OSR = 2048		(0.6)		µVRms
Integral non-linearity error	INL	G_{SET01} = 1, G_{SET02} = 1, OSR = 2048		(±10)		ppmFS
Common mode rejection ratio	CMRR0	V_{COM} = 1.0±0.8 V, fin = 50 Hz G_{SET01} = 1, G_{SET02} = 1	(72)	(90)		dB
Power supply rejection ratio	PSRR0	AV_{DD} = 2.7 to 5.5 V, G_{SET01} = 1, G_{SET02} = 1	(60)	(85)		dB
ΔΣ A/D converter input clock frequency	f_{ADC}		3.8	4.0	4.2	MHz

Note Calculate the gain drift and offset drift by using the following expression (for 85°C products):
For gain drift: (MAX(EG(T(-40) to T(85))) - MIN(EG(T(-40) to T(85)))) / (85°C -(-40°C))
For offset drift: (MAX(EOS(T(-40) to T(85))) - MIN(EOS(T(-40) to T(85)))) / (85°C -(-40°C))
MAX(EG(T(-40) to T(85))): The maximum value of gain error when the temperature range is -40°C to 85°C
MIN(EG(T(-40) to T(85))): The minimum value of gain error when the temperature range is -40°C to 85°C
MAX(EOS(T(-40) to T(85))): The maximum value of offset error when the temperature range is -40°C to 85°C
MIN(EOS(T(-40) to T(85))):The minimum value of offset error when the temperature range is -40°C to 85°C

Remark 1. Values in parentheses are target design values (i.e. not guaranteed) and therefore are not tested for shipment.
Remark 2. The typical conditions are the conditions when T_A = 25°C and AV_{DD} = 3.3 V.

38.6.6 Sensor power supply (SBIAS)

(T_A = -40 to +85°C, 2.7 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V, C_{OUT} = 0.22 µF, V_{OUT} = 1.0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Output voltage range	V_{OUT}		0.5		2.2	V
Output voltage adjustment steps	V_{STEP}			0.1		V
Output voltage precision	V_A	I_{OUT} = 1 mA	(- 3)		(+ 3)	%
Maximum output current	I_{OUT}		5			mA
Short circuit current	I_{SHORT}	V_{OUT} = 0 V		40	65	mA
Load regulation	L_R	1 mA ≤ I_{OUT} ≤ 5 mA			(15)	mV
Power supply rejection ratio	PSRR	AV_{DD} = 5.0 V + 0.1 Vpp ripple f = 100 Hz, I_{OUT} = 2.5 mA, V_{OUT} = 2.1 V	(45)	(70)		dB

Remark 1. Values in parentheses are target design values (i.e. not guaranteed) and therefore are not tested for shipment.
Remark 2. The typical conditions are the conditions when T_A = 25°C and AV_{DD} = 3.3 V.

38.6.7 Internal BIAS power supply

(T_A = -40 to +85°C, 2.7 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Output voltage	V_{BIAS}		0.95	1.00	1.05	V

Remark The typical conditions are the conditions when T_A = 25°C and AV_{DD} = 3.3 V.

38.6.8 Programmable gain instrumentation amplifier (PGA1)

(T_A = -40 to +85°C, 2.7 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V) **(1/2)**

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Differential input voltage range	V_{ID}	V_{ID} = (PGA1xP - PGA1xN) (x = 0, 1)		±800 /G_{TOTAL1}		mV
Input voltage range	V_{IN}		0.3		AV_{DD} - 0.6	V
Common mode input voltage range	V_{COM}		0.3+ (($\|V_{ID}\|$+$\|E_{OS}\|$) ×G_{SET11})/2		AV_{DD}-0.6+ (($\|V_{ID}\|$+$\|E_{OS}\|$) ×G_{SET11})/2	V
Output voltage range	V_{OUT}		0.1		AV_{DD} - 0.1	V
Maximum output current	I_{OUT}		-0.1		+0.1	mA
Input bias current	I_{IN}				±50	nA
Input bias offset current	I_{OS}				±20	nA
Gain setting range	G_{TOTAL1}			G_{SET11} × G_{SET12}		V/V
1st gain setting range	G_{SET11}			12, 16, 20, 24		V/V
2nd gain setting range	G_{SET12}			Note		V/V
Gain error	E_{G1}	T_A = 25°C G_{SET11} = 24, G_{SET12} = 1			±2.7	%
Gain drift	dE_{G1}	G_{SET11} = 24, G_{SET12} = 1		(5.6)	(22.0)	ppm/°C
Offset error	E_{OS1}	T_A = 25°C G_{SET11} = 24, G_{SET12} = 1 Referred to input	-10		+10	mV
Bandwidth	BW11	Low-power mode G_{SET11} = 24, G_{SET12} = 1		(1.5)		kHz
	BW12	High-speed mode G_{SET11} = 24, G_{SET12} = 1		(67)		kHz
Slew rate	SR11	Low-power mode		(6)		mV/µs
	SR12	High-speed mode		(220)		mV/µs
Peak-to-peak voltage noise	Enb11	0.1 Hz to 10 Hz Low-power mode		(3.0)		µVrms
	Enb12	0.1 Hz to 10 Hz High-speed mode		(2.6)		µVrms

Note See the setting of PGA1GC3 to PGA1GC0.

(T_A = -40 to +85°C, 2.7 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V) **(2/2)**

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input-referred noise	En11	f = 1 kHz Low-power mode		(210)		nV/√Hz
	En12	f = 1 kHz High-speed mode		(110)		nV/√Hz
	En13	f = 10 Hz Low-power mode		(460)		nV/√Hz
	En14	f = 10 Hz High-speed mode		(410)		nV/√Hz
Common mode rejection ratio	CMRR1	G_{SET11} = 24, G_{SET12} = 1 f = 50 Hz		(100)		dB
Power supply rejection ratio	PSRR1	2.7 V ≤ AV_{DD} ≤ 5.5 V f = 50 Hz When SBIAS is selected as the reference voltage of the 12-bit D/A converter.		(80)		dB

Remark 1. Values in parentheses are target design values (i.e. not guaranteed) and therefore are not tested for shipment.

Remark 2. The typical conditions are the conditions when T_A = 25°C and AV_{DD} = 3.3 V.

Remark 3. Unless otherwise specified, values are for operation in high-speed mode.

38.6.9 Operational amplifier 0 (AMP0)

(T_A = -40 to +85°C, 2.7 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Common mode input voltage range	V_{CM}		0.1		AV_{DD} - 0.1	V
Output voltage range	V_{OUT}	I_{OUT}= ±1 mA	0.07		AV_{DD} - 0.15	V
Maximum output current	I_{OUT}		(-2)		(+2)	mA
Input bias current	I_{IN}				±50	nA
Input offset voltage	V_{OS1}	Low-power mode	-10		+10	mV
	V_{OS2}	High-speed mode	-7		+7	mV
Slew rate	SR1	Low-power mode		(0.04)		V/µs
	SR2	High-speed mode		(0.7)		V/µs
Gain bandwidth	GBW1	Low-power mode		(0.06)		MHz
	GBW2	High-speed mode		(1)		MHz
Phase margin	PM1	Low-power mode		(70)		deg
	PM2	High-speed mode		(60)		deg
Settling time	Tset1	Low-power mode CL = 50 pF, RL = 10 kΩ			(300)	µs
	Tset2	High-speed mode CL = 50 pF, RL = 10 kΩ			(14)	µs
Stabilization wait time	Tstaw1	AMPEn = 0 → 1, Low-power mode CL = 50 pF, RL = 10 kΩ			(300)	µs
	Tstaw2	AMPEn = 0 → 1, High-speed mode CL = 50 pF, RL = 10 kΩ			(14)	µs
Input-referred noise	En1	f = 1 kHz Low-power mode		(200)		nV/√Hz
	En2	f = 1 kHz High-speed mode		(80)		nV/√Hz
Common mode rejection ratio	CMRR	DC		(70)		dB
Power supply rejection ratio	PSRR	DC		(90)		dB

Remark 1. Values in parentheses are target design values (i.e. not guaranteed) and therefore are not tested for shipment.

Remark 2. The typical conditions are the conditions when T_A = 25°C and AV_{DD} = 3.3 V.

Remark 3. Unless otherwise specified, values are for operation in high-speed mode.

38.6.10 Operational amplifiers 1 and 2 (AMP1, AMP2)

(T_A = -40 to +85°C, 2.7 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Common mode input voltage range	V_{CM1}	Low-power mode	0.2		AV_{DD} - 0.5	V
	V_{CM2}	High-speed mode	0.3		AV_{DD} - 0.6	V
Output voltage range	V_{OUT}		0.1		AV_{DD} - 0.1	V
Maximum output current	I_{OUT}	2.7 V ≤ AV_{DD} ≤ 5.5 V	-100		+100	μA
Input bias current	I_{IN}				±50	nA
Input offset voltage	V_{OS1}	Low-power mode	-10		+10	mV
	V_{OS2}	High-speed mode	-10		+10	mV
Slew rate	SR1	Low-power mode		(0.02)		V/μs
	SR2	High-speed mode		(1.1)		V/μs
Gain bandwidth	GBW1	Low-power mode		(0.04)		MHz
	GBW2	High-speed mode		(1.7)		MHz
Phase margin	PM1	Low-power mode		(70)		deg
	PM2	High-speed mode		(60)		deg
Settling time	Tset1	Low-power mode CL = 50 pF, RL = 10 kΩ			(750)	μs
	Tset2	High-speed mode CL = 50 pF, RL = 10 kΩ			(13)	μs
Stabilization wait time	Tstaw1	AMPEn = 0 → 1, Low-power mode CL = 50 pF, RL = 10 kΩ			(800)	μs
	Tstaw2	AMPEn = 0 → 1, High-speed mode CL = 50 pF, RL = 10 kΩ			(13)	μs
Input-referred noise	En1	f = 1 kHz Low-power mode		(230)		nV/√Hz
	En2	f = 1 kHz High-speed mode		(90)		nV/√Hz
Common mode rejection ratio	CMRR	DC		(90)		dB
Power supply rejection ratio	PSRR	DC		(90)		dB

Remark 1. Values in parentheses are target design values (i.e. not guaranteed) and therefore are not tested for shipment.

Remark 2. The typical conditions are the conditions when T_A = 25°C and AV_{DD} = 3.3 V.

Remark 3. Unless otherwise specified, values are for operation in high-speed mode.

38.6.11 8-bit D/A converter (DAC0)

(T_A = -40 to +85°C, 2.7 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V, reference voltage (+) = 2.1 V (SBIAS))

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution	DARES0				8	bit
Absolute accuracy	LE	Note			±2.5	LSB
Differential non-linearity error	DADLE0				±2.0	LSB
Settling time	DAtset0	CL = 50 pF, RL = 10 kΩ			(6)	μs

Note Errors of the SBIAS output voltage are not included.

Remark 1. Values in parentheses are target design values (i.e. not guaranteed) and therefore are not tested for shipment.
Remark 2. The 8-bit D/A converter characteristics are the values obtained with the amplifier unit connected.

38.6.12 12-bit D/A converter (DAC1)

(1) When reference voltage (+) = 2.1 V (SBIAS)

(T_A = -40 to +85°C, 2.7 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V, reference voltage (+) = 2.1 V (SBIAS))

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution	DARES1				(12)	bit
Output voltage range	DAOUT	12-bit resolution	0.35		SBIAS	V
Integral non-linearity error	DAILE	12-bit resolution			±4.0	LSB
Differential non-linearity error	DADLE1	12-bit resolution			±1.0	LSB
Offset error	DAErr	12-bit resolution			±30	mV
Gain error	DAEG	12-bit resolution Note			±20	mV
Settling time	DAtset1	12-bit resolution CL = 50 pF, RL = 10 kΩ			(60)	μs

Note Errors of the SBIAS output voltage are not included.

Remark 1. Values in parentheses are target design values (i.e. not guaranteed) and therefore are not tested for shipment.
Remark 2. The 12-bit D/A converter characteristics are the values obtained with the amplifier unit connected.

(2) When reference voltage (+) = AV_{DD}

(T_A = -40 to +85°C, 2.7 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V, reference voltage (+) = AV_{DD})

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution	DARES1				(12)	bit
Output voltage range	DAOUT	12-bit resolution	0.35		AV_{DD} - 0.47	V
Integral non-linearity error	DAILE	12-bit resolution			±4.0	LSB
Differential non-linearity error	DADLE1	12-bit resolution			±1.0	LSB
Offset error	DAErr	12-bit resolution			±30	mV
Gain error	DAEG	12-bit resolution			±20	mV
Settling time	DAtset1	12-bit resolution CL = 50 pF, RL = 10 kΩ			(60)	μs

Remark 1. Values in parentheses are target design values (i.e. not guaranteed) and therefore are not tested for shipment.
Remark 2. The 12-bit D/A converter characteristics are the values obtained with the amplifier unit connected.

38.7 Power supply voltage rising slope characteristics

(T_A = -40 to +85°C, V_{SS} = 0 V)

Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Power supply voltage rising slope	SV_{DD}			54	V/ms

Caution Make sure to keep the internal reset state by the LVD circuit or an external reset until V_{DD} reaches the operating voltage range shown in 38.4 AC Characteristics.

38.8 LCD Characteristics

38.8.1 Resistance division method

(1) Static display mode

(T_A = -40 to +85°C, V_{L4} (MIN.) ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
LCD drive voltage	V_{L4}		2.0		V_{DD}	V

(2) 1/2 bias method, 1/4 bias method

(T_A = -40 to +85°C, V_{L4} (MIN.) ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
LCD drive voltage	V_{L4}		2.7		V_{DD}	V

(3) 1/3 bias method

(T_A = -40 to +85°C, V_{L4} (MIN.) ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
LCD drive voltage	V_{L4}		2.5		V_{DD}	V

38.8.2 Internal voltage boosting method

(1) 1/3 bias method

(T_A = -40 to +85°C, 2.4 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
LCD output voltage variation range	V_{L1}	C1 to C4 Note 1 = 0.47 µF Note 2	VLCD = 04H	0.90	1.00	1.08	V
			VLCD = 05H	0.95	1.05	1.13	V
			VLCD = 06H	1.00	1.10	1.18	V
			VLCD = 07H	1.05	1.15	1.23	V
			VLCD = 08H	1.10	1.20	1.28	V
			VLCD = 09H	1.15	1.25	1.33	V
			VLCD = 0AH	1.20	1.30	1.38	V
			VLCD = 0BH	1.25	1.35	1.43	V
			VLCD = 0CH	1.30	1.40	1.48	V
			VLCD = 0DH	1.35	1.45	1.53	V
			VLCD = 0EH	1.40	1.50	1.58	V
			VLCD = 0FH	1.45	1.55	1.63	V
			VLCD = 10H	1.50	1.60	1.68	V
			VLCD = 11H	1.55	1.65	1.73	V
			VLCD = 12H	1.60	1.70	1.78	V
			VLCD = 13H	1.65	1.75	1.83	V
Doubler output voltage	V_{L2}	C1 to C4 Note 1 = 0.47 µF		2 V_{L1} - 0.1	2 V_{L1}	2 V_{L1}	V
Tripler output voltage	V_{L4}	C1 to C4 Note 1 = 0.47 µF		3 V_{L1}- 0.15	3 V_{L1}	3 V_{L1}	V
Reference voltage setup time Note 2	t_{VWAIT1}			5			ms
Voltage boost wait time Note 3	t_{VWAIT2}	C1 to C4 Note 1 = 0.47 µF		500			ms

Note 1. This is a capacitor that is connected between voltage pins used to drive the LCD.
C1: A capacitor connected between CAPH and CAPL
C2: A capacitor connected between V_{L1} and GND
C3: A capacitor connected between V_{L2} and GND
C4: A capacitor connected between V_{L4} and GND
C1 = C2 = C3 = C4 = 0.47 µF±30%

Note 2. This is the time required to wait from when the reference voltage is specified by using the VLCD register (or when the internal voltage boosting method is selected (by setting the MDSET1 and MDSET0 bits of the LCDM0 register to 01B) if the default value reference voltage is used) until voltage boosting starts (VLCON = 1).

Note 3. This is the wait time from when voltage boosting is started (VLCON = 1) until display is enabled (LCDON = 1).

(2) 1/4 bias method

(T_A = -40 to +85°C, 2.4 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
LCD output voltage variation range	V_{L1}	C1 to C5 Note 1 = 0.47 µF Note 2	VLCD = 04H	0.90	1.00	1.08	V
			VLCD = 05H	0.95	1.05	1.13	V
			VLCD = 06H	1.00	1.10	1.18	V
			VLCD = 07H	1.05	1.15	1.23	V
			VLCD = 08H	1.10	1.20	1.28	V
			VLCD = 09H	1.15	1.25	1.33	V
			VLCD = 0AH	1.20	1.30	1.38	V
Doubler output voltage	V_{L2}	C1 to C5 Note 1 = 0.47 µF		2 V_{L1} - 0.08	2 V_{L1}	2 V_{L1}	V
Tripler output voltage	V_{L3}	C1 to C5 Note 1 = 0.47 µF		3 V_{L1} - 0.12	3 V_{L1}	3 V_{L1}	V
Quadruply output voltage	V_{L4}	C1 to C5 Note 1 = 0.47 µF		4 V_{L1} - 0.16	4 V_{L1}	4 V_{L1}	V
Reference voltage setup time Note 2	t_{VWAIT1}			5			ms
Voltage boost wait time Note 3	t_{VWAIT2}	C1 to C5 Note 1 = 0.47µF		500			ms

Note 1. This is a capacitor that is connected between voltage pins used to drive the LCD.
C1: A capacitor connected between CAPH and CAPL
C2: A capacitor connected between V_{L1} and GND
C3: A capacitor connected between V_{L2} and GND
C4: A capacitor connected between V_{L3} and GND
C5: A capacitor connected between V_{L4} and GND
C1 = C2 = C3 = C4 = C5 = 0.47 µF±30%

Note 2. This is the time required to wait from when the reference voltage is specified by using the VLCD register (or when the internal voltage boosting method is selected (by setting the MDSET1 and MDSET0 bits of the LCDM0 register to 01B) if the default value reference voltage is used) until voltage boosting starts (VLCON = 1).

Note 3. This is the wait time from when voltage boosting is started (VLCON = 1) until display is enabled (LCDON = 1).

38.8.3 Capacitor split method

(1) 1/3 bias method

(T_A = -40 to +85°C, 2.4 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
V_{L4} voltage	V_{L4}	C1 to C4 = 0.47 µF Note 2		V_{DD}		V
V_{L2} voltage	V_{L2}	C1 to C4 = 0.47 µF Note 2	2/3 V_{L4} - 0.1	2/3 V_{L4}	2/3 V_{L4} + 0.1	V
V_{L1} voltage	V_{L1}	C1 to C4 = 0.47 µF Note 2	1/3 V_{L4} - 0.1	1/3 V_{L4}	1/3 V_{L4} + 0.1	V
Capacitor split wait time Note 1	tVWAIT		100			ms

Note 1. This is the wait time from when voltage bucking is started (VLCON = 1) until display is enabled (LCDON = 1).

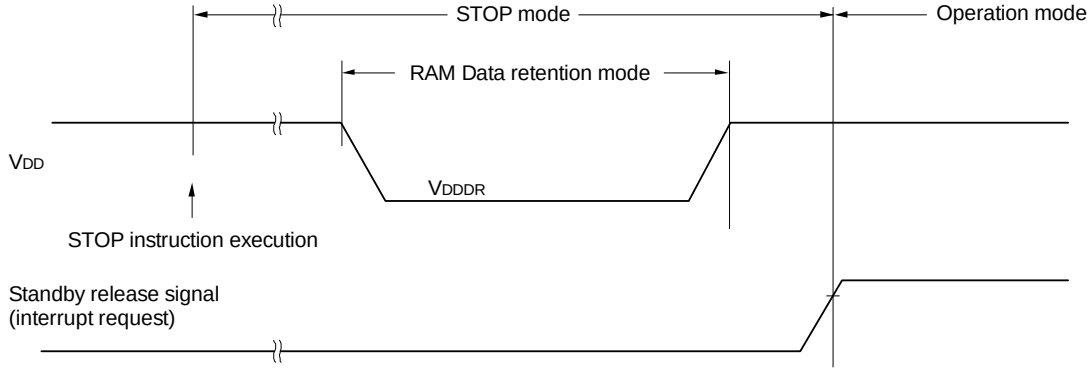
Note 2. This is a capacitor that is connected between voltage pins used to drive the LCD.
C1: A capacitor connected between CAPH and CAPL
C2: A capacitor connected between V_{L1} and GND
C3: A capacitor connected between V_{L2} and GND
C4: A capacitor connected between V_{L4} and GND
C1 = C2 = C3 = C4 = 0.47 µF±30%

38.9 RAM data retention characteristics

(T_A = -40 to +85°C, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{DDDR}		1.46 Note		5.5	V

Note The value depends on the POR detection voltage. When the voltage drops, the RAM data is retained before a POR reset is effected, but RAM data is not retained when a POR reset is effected.



38.10 Flash Memory Programming Characteristics

(T_A = -40 to +85°C, 2.4 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
System clock frequency	f_{CLK}	2.4 V ≤ V_{DD} ≤ 5.5 V		1		24	MHz
Number of code flash rewrites Notes 1, 2, 3	C_{erwr}	Retained for 20 years	T_A = 85°C	1,000			Times
Number of data flash rewrites Notes 1, 2, 3		Retained for 1 year	T_A = 25°C		1,000,000		
		Retained for 5 years	T_A = 85°C	100,000			
		Retained for 20 years	T_A = 85°C	10,000			

Note 1. 1 erase + 1 write after the erase is regarded as 1 rewrite. The retaining years are until next rewrite after the rewrite.

Note 2. When using flash memory programmer and Renesas Electronics self programming library

Note 3. These are the characteristics of the flash memory and the results obtained from reliability testing by Renesas Electronics Corporation.

38.11 Dedicated Flash Memory Programmer Communication (UART)

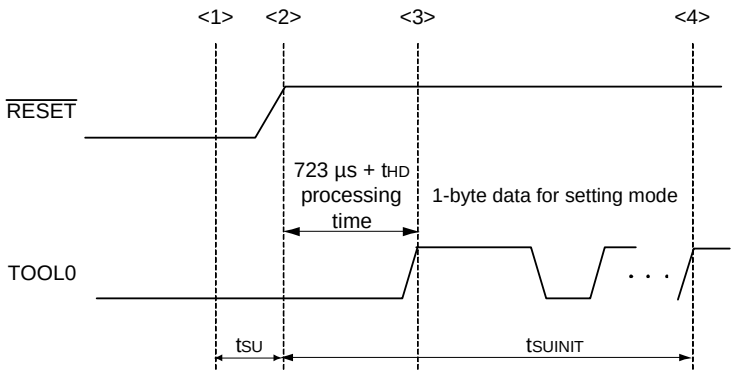
(T_A = -40 to +85°C, 2.4 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate		During serial programming	115,200		1,000,000	bps

38.12 Timing of Entry to Flash Memory Programming Modes

(T_A = -40 to +85°C, 2.4 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
How long from when an external reset ends until the initial communication settings are specified	t_{SUINIT}	POR and LVD reset must end before the external reset ends.			100	ms
How long from when the TOOL0 pin is placed at the low level until an external reset ends	t_{SU}	POR and LVD reset must end before the external reset ends.	10			μs
Time to hold the TOOL0 pin at the low level after an external reset is released (excluding the processing time of the firmware to control the flash memory)	t_{HD}	POR and LVD reset must end before the external reset ends.	1			ms



<1> The low level is input to the TOOL0 pin.
<2> The external reset ends (POR and LVD reset must end before the external reset ends.).
<3> The TOOL0 pin is set to the high level.
<4> Setting of the flash memory programming mode by UART reception and complete the baud rate setting.

Remark t_{SUINIT}: The segment shows that it is necessary to finish specifying the initial communication settings within 100 ms from when the resets end.
t_{SU}: How long from when the TOOL0 pin is placed at the low level until an external reset ends
t_{HD}: Time to hold the TOOL0 pin at the low level after an external reset is released (excluding the processing time of the firmware to control the flash memory)

CHAPTER 39 ELECTRICAL SPECIFICATIONS (R5F11R) (D: T_A = -40 to +85°C)

This chapter describes the electrical specifications for the products “D: Industrial applications (T_A = -40 to +85°C)”.

Caution 1. The RL78 microcontrollers have an on-chip debug function, which is provided for development and evaluation. Do not use the on-chip debug function in products designated for mass production, because the guaranteed number of rewritable times of the flash memory may be exceeded when this function is used, and product reliability therefore cannot be guaranteed. Renesas Electronics is not liable for problems occurring when the on-chip debug function is used.

Caution 2. The pins mounted depend on the product. Refer to 2.1 Port Function to 2.2 Functions other than port pins.

39.1 Absolute Maximum Ratings

Absolute Maximum Ratings **(1/3)**

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{DD}		-0.5 to +6.5	V
	AV_{DD}	$AV_{DD} = V_{DD}$	-0.5 to +6.5	V
	AV_{SS}	$AV_{SS} = V_{SS}$	-0.5 to +0.3	V
REGC pin input voltage	V_{IREGC}	REGC	-0.3 to +2.8 and -0.3 to V_{DD} + 0.3 Note 1	V
Input voltage	V_{I1}	P01 to P07, P10 to P17, P30 to P32, P35 to P37, P40, P43, P44, P50 to P53, P70 to P77, P80 to P86, P121 to P124, P125 to P127, P137, EXCLK, EXCLKS, $\overline{\text{RESET}}$	-0.3 to V_{DD} +0.3 Note 2	V
	V_{I2}	P60, P61 (N-ch open-drain)	-0.3 to +6.5	V
	V_{I3}	P20 to P27, P150, P151	-0.3 to AV_{DD} + 0.3 Note 2	V
Output voltage	V_{O1}	P01 to P07, P10 to P17, P30 to P32, P35 to P37, P40, P43, P44, P50 to P53, P60, P61, P70 to P77, P80 to P86, P125 to P127	-0.3 to V_{DD} + 0.3 Note 2	V
	V_{O2}	P20 to P27, P150, P151	-0.3 to AV_{DD} + 0.3 Note 2	V
Analog input voltage	V_{AI1}	ANI8 to ANI10	-0.3 to V_{DD} + 0.3 Note 2	V

Note 1. Connect the REGC pin to V_{SS} via a capacitor (0.47 to 1 µF). This value regulates the absolute maximum rating of the REGC pin. Do not use this pin with voltage applied to it.

Note 2. Must be 6.5 V or lower.

Caution **Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.**

Remark 1. Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

Remark 2. The reference voltage is V_{SS} (for the V_{DD} systems) = AV_{SS} (for the AV_{DD} systems).

Absolute Maximum Ratings **(2/3)**

Parameter	Symbol	Conditions		Ratings	Unit
LCD voltage	V_{LI1}	V_{L1} input voltage Note 1		-0.3 to +2.8	V
	V_{LI2}	V_{L2} input voltage Note 1		-0.3 to +6.5	V
	V_{LI3}	V_{L3} input voltage Note 1		-0.3 to +6.5	V
	V_{LI4}	V_{L4} input voltage Note 1		-0.3 to +6.5	V
	V_{LI5}	CAPL, CAPH input voltage Note 1		-0.3 to +6.5	V
	V_{LO1}	V_{L1} output voltage		-0.3 to +2.8	V
	V_{LO2}	V_{L2} output voltage		-0.3 to +6.5	V
	V_{LO3}	V_{L3} output voltage		-0.3 to +6.5	V
	V_{LO4}	V_{L4} output voltage		-0.3 to +6.5	V
	V_{LO5}	CAPL, CAPH output voltage		-0.3 to +6.5	V
	V_{LO6}	COM0 to COM7 SEG0 to SEG35 output voltage	External resistance division method	-0.3 to V_{DD} + 0.3 Note 2	V
			Capacitor split method	-0.3 to V_{DD} + 0.3 Note 2	V
			Internal voltage boosting method	-0.3 to V_{LI4} + 0.3 Note 2	V

Note 1. This value only indicates the absolute maximum ratings when applying voltage to the V_{L1}, V_{L2}, V_{L3}, and V_{L4} pins; it does not mean that applying voltage to these pins is recommended. When using the internal voltage boosting method or capacitance split method, connect these pins to V_{SS} via a capacitor (0.47 µF ± 30%) and connect a capacitor (0.47 µF ± 30%) between the CAPL and CAPH pins.

Note 2. Must be 6.5 V or lower.

Caution **Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.**

Absolute Maximum Ratings **(3/3)**

Parameter	Symbol	Conditions		Ratings	Unit
Output current, high	I_{OH1}	Per pin		-40	mA
		Total of all pins -170 mA	P40, P43, P44, P80 to P83	-70	mA
			P01 to P07, P10 to P17, P30 to P32, P35 to P37, P50 to P53, P70 to P77, P84 to P86, P125 to P127	-100	mA
	I_{OH2}	Per pin		-40	mA
		Total of all pins -140 mA	P21 to P27	-70	mA
			P20, P150, P151	-70	mA
Output current, low	I_{OL1}	Per pin		40	mA
		Total of all pins 170 mA	P40, P43, P44, P80 to P83	70	mA
			P01 to P07, P10 to P17, P30 to P32, P35 to P37, P50 to P53, P60, P61, P70 to P77, P84 to P86, P125 to P127	100	mA
	I_{OL2}	Per pin		40	mA
		Total of all pins 140 mA	P21 to P27	70	mA
			P20, P150, P151	70	mA
Operating ambient temperature	T_A	In normal operation mode		-40 to +85	°C
		In flash memory programming mode			
Storage temperature	T_{stg}			-65 to +150	°C

Caution **Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.**

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

39.2 Oscillator Characteristics

39.2.1 X1 and XT1 characteristics

(T_A = -40 to +85°C, 1.8 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Resonator	Conditions	MIN.	TYP.	MAX.	Unit
X1 clock oscillation frequency (f_X) Note	Ceramic resonator/ crystal resonator	2.7 V ≤ V_{DD} ≤ 5.5 V	1.0		20.0	MHz
		2.4 V ≤ V_{DD} < 2.7 V	1.0		16.0	
		1.8 V ≤ V_{DD} < 2.4 V	1.0		8.0	
X1 clock oscillation frequency (f_{XT}) Note	Crystal resonator		32	32.768	35	kHz
			31	38.4	39	

Note Indicates only permissible oscillator frequency ranges. Refer to **AC Characteristics** for instruction execution time. Request evaluation by the manufacturer of the oscillator circuit mounted on a board to check the oscillator characteristics.

Caution Since the CPU is started by the high-speed on-chip oscillator clock after a reset release, check the X1 clock oscillation stabilization time using the oscillation stabilization time counter status register (OSTC) by the user. Determine the oscillation stabilization time of the OSTC register and the oscillation stabilization time select register (OSTS) after sufficiently evaluating the oscillation stabilization time with the resonator to be used.

Remark When using the X1 and XT1 oscillator, refer to **5.4 System Clock Oscillator**.

39.2.2 On-chip oscillator characteristics

(T_A = -40 to +85°C, 1.8 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
High-speed on-chip oscillator clock frequency Notes 1, 2	f_{IH}	2.7 V ≤ V_{DD} ≤ 5.5 V		1		24	MHz
		2.4 V ≤ V_{DD} < 2.7 V		1		16	MHz
		1.8 V ≤ V_{DD} < 2.4 V		1		8	MHz
High-speed on-chip oscillator clock frequency accuracy		-20 to +85°C	1.8 V ≤ V_{DD} ≤ 5.5 V	-1.0		+1.0	%
		-40 to -20°C	1.8 V ≤ V_{DD} ≤ 5.5 V	-1.5		+1.5	%
Low-speed on-chip oscillator clock frequency	f_{IL}				15		kHz
Low-speed on-chip oscillator clock frequency accuracy				-15		+15	%

Note 1. High-speed on-chip oscillator frequency is selected with bits 0 to 4 of the option byte (000C2H/010C2H) and bits 0 to 2 of the HOCODIV register.

Note 2. This only indicates the oscillator characteristics. Refer to **AC Characteristics** for instruction execution time.

39.3 DC Characteristics

39.3.1 Pin characteristics

(T_A = -40 to +85°C, 1.8 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V) **(1/5)**

Item	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output current, high Note 1	I_{OH1}	Per pin for P01 to P07, P10 to P17, P30 to P32, P35 to P37, P40, P43, P44, P50 to P53, P70 to P77, P80 to P86, P125 to P127				-10.0 Note 2	mA
		Total of P40, P43, P44, P80 to P83 (When duty ≤ 70% Note 3)	4.0 V ≤ V_{DD} ≤ 5.5 V			-55	mA
			2.7 V ≤ V_{DD} < 4.0 V			-10	mA
			1.8 V ≤ V_{DD} < 2.7 V			-5	mA
		Total of P01 to P07, P10 to P17, P30 to P32, P35 to P37, P50 to P53, P70 to P77, P84 to P86, P125 to P127 (When duty ≤ 70% Note 3)	4.0 V ≤ V_{DD} ≤ 5.5 V			-69	mA
			2.7 V ≤ V_{DD} < 4.0 V			-23	mA
			1.8 V ≤ V_{DD} < 2.7 V			-12	mA
		Total of all pins (When duty ≤ 70% Note 3)	1.8 V ≤ V_{DD} ≤ 5.5 V			-124	mA
	I_{OH2}	Per pin for P20 to P27, P150, P151	1.8 V ≤ AV_{DD} ≤ 5.5 V			-10.0 Note 2	mA
		Total of P21 to P27 (When duty ≤ 70% Note 3)	4.0 V ≤ AV_{DD} ≤ 5.5 V			-50	mA
			2.7 V ≤ AV_{DD} < 4.0 V			-10	mA
			1.8 V ≤ AV_{DD} < 2.7 V			-5	mA
		Total of P20, P150, P151 (When duty ≤ 70% Note 3)	4.0 V ≤ AV_{DD} ≤ 5.5 V			-21	mA
			2.7 V ≤ AV_{DD} < 4.0 V			-5	mA
			1.8 V ≤ AV_{DD} < 2.7 V			-3	mA
		Total of all pins (When duty ≤ 70% Note 3)	1.8 V ≤ AV_{DD} ≤ 5.5 V			-71	mA

Note 1. Value of current at which the device operation is guaranteed even if the current flows from the V_{DD} pin (I_{OH1}) and AV_{DD} pin (I_{OH2}) to an output pin.

Note 2. Do not exceed the total current value.

Note 3. Specification under conditions where the duty factor ≤ 70%.
The output current value that has changed to the duty factor > 70% the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).
- Total output current of pins = (I_{OH} × 0.7)/(n × 0.01)

<Example> Where n = 80% and I_{OH} = −10.0 mA
Total output current of pins = (−10.0 × 0.7)/(80 × 0.01) ≅ −8.7 mA

However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

Caution **P02 to P04, P06, P07, P10, P12, P35 to P37, P40, P43, P44, P50 to P52, and P80 to P82 do not output high level in N-ch open-drain mode.**

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(T_A = -40 to +85°C, 1.8 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V) **(2/5)**

Item	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output current, low Note 1	I_{OL1}	Per pin for P01 to P07, P10 to P17, P30 to P32, P35 to P37, P40, P43, P44, P50 to P53, P70 to P77, P80 to P86, P121 to P127				20.0 Note 2	mA
		Per pin for P60, P61				15.0 Note 2	mA
		Total of P40, P43, P44, P80 to P83 (When duty ≤ 70% Note 3)	4.0 V ≤ V_{DD} ≤ 5.5 V			70	mA
			2.7 V ≤ V_{DD} < 4.0 V			15	mA
			1.8 V ≤ V_{DD} < 2.7 V			9	mA
		Total of P01 to P07, P10 to P17, P30 to P32, P35 to P37, P50 to P53, P60, P61, P70 to P77, P84 to P86, P125 to P127 (When duty ≤ 70% Note 3)	4.0 V ≤ V_{DD} ≤ 5.5 V			90	mA
			2.7 V ≤ V_{DD} < 4.0 V			35	mA
			1.8 V ≤ V_{DD} < 2.7 V			20	mA
		Total of all pins (When duty ≤ 70% Note 3)	1.8 V ≤ V_{DD} ≤ 5.5 V			160	mA
	I_{OL2}	Per pin for P20 to P27, P150, P151	1.8 V ≤ AV_{DD} ≤ 5.5 V			20	mA
		Total of P21 to P27 (When duty ≤ 70% Note 3)	4.0 V ≤ AV_{DD} ≤ 5.5 V			60	mA
			2.7 V ≤ AV_{DD} < 4.0 V			10	mA
			1.8 V ≤ AV_{DD} < 2.7 V			5	mA
		Total of P20, P150, P151 (When duty ≤ 70% Note 3)	4.0 V ≤ AV_{DD} ≤ 5.5 V			25	mA
			2.7 V ≤ AV_{DD} < 4.0 V			8	mA
			1.8 V ≤ AV_{DD} < 2.7 V			5	mA
		Total of all pins (When duty ≤ 70% Note 3)	1.8 V ≤ AV_{DD} ≤ 5.5 V			85	mA

Note 1. Value of current at which the device operation is guaranteed even if the current flows from the V_{SS} pin (I_{OL1}) and AV_{SS} pin (I_{OL2}) to an output pin.

Note 2. Do not exceed the total current value.

Note 3. Specification under conditions where the duty factor ≤ 70%.
The output current value that has changed to the duty factor > 70% the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

- Total output current of pins = (I_{OL} × 0.7)/(n × 0.01)

<Example> Where n = 80% and I_{OL} = 10.0 mA
Total output current of pins = (10.0 × 0.7)/(80 × 0.01) ≅ 8.7 mA

However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(T_A = -40 to +85°C, 1.8 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V) (3/5)

Item	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input voltage, high	V_{IH1}	P01 to P07, P10 to P17, P30 to P32, P35 to P37, P40, P43, P44, P50 to P53, P70 to P77, P80 to P86, P125 to P127	Normal input buffer	0.8 V_{DD}		V_{DD}	V
	V_{IH2}	For TTL mode supported ports	TTL input buffer, 4.0 V ≤ V_{DD} ≤ 5.5 V	2.2		V_{DD}	V
			TTL input buffer, 3.3 V ≤ V_{DD} < 4.0 V	2.0		V_{DD}	V
			TTL input buffer, 1.8 V ≤ V_{DD} < 3.3 V	1.5		V_{DD}	V
	V_{IH3}	P20 to P27, P150, P151		0.8 AV_{DD}		AV_{DD}	V
	V_{IH4}	P60, P61		0.7 V_{DD}		6.0	V
	V_{IH5}	P121 to P124, P137, EXCLK, EXCLKS, $\overline{\text{RESET}}$		0.8 V_{DD}		V_{DD}	V
Input voltage, low	V_{IL1}	P01 to P07, P10 to P17, P30 to P32, P35 to P37, P40, P43, P44, P50 to P53, P70 to P77, P80 to P86, P125 to P127	Normal input buffer	0		0.2 V_{DD}	V
	V_{IL2}	For TTL mode supported ports	TTL input buffer, 4.0 V ≤ V_{DD} ≤ 5.5 V	0		0.8	V
			TTL input buffer, 3.3 V ≤ V_{DD} < 4.0 V	0		0.5	V
			TTL input buffer, 1.8 V ≤ V_{DD} < 3.3 V	0		0.32	V
	V_{IL3}	P20 to P27, P150, P151		0		0.2 AV_{DD}	V
	V_{IL4}	P60, P61		0		0.3 V_{DD}	V
	V_{IL5}	P121 to P124, P137, EXCLK, EXCLKS, $\overline{\text{RESET}}$		0		0.2 V_{DD}	V

Caution The maximum V_{IH} value on P02 to P04, P06, P07, P10, P12, P35 to P37, P40, P43, P44, P50 to P52, and P80 to P82 is V_{DD}, even in the N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(T_A = -40 to +85°C, 1.8 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V) (4/5)

Item	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output voltage, high	V_{OH1}	P01 to P07, P10 to P17, P30 to P32, P35 to P37, P40, P43, P44, P50 to P53, P70 to P77, P80 to P86, P125 to P127	4.0 V ≤ V_{DD} ≤ 5.5 V, I_{OH} = -10.0 mA	V_{DD} - 1.5			V
			4.0 V ≤ V_{DD} ≤ 5.5 V, I_{OH} = -3.0 mA	V_{DD} - 0.7			V
			2.7 V ≤ V_{DD} ≤ 5.5 V, I_{OH} = -2.0 mA	V_{DD} - 0.6			V
			1.8 V ≤ V_{DD} ≤ 5.5 V, I_{OH} = -1.5 mA	V_{DD} - 0.5			V
	V_{OH2}	P20 to P27, P150, P151	4.0 V ≤ AV_{DD} ≤ 5.5 V, I_{OH} = -10.0 mA	AV_{DD} - 1.5			V
			4.0 V ≤ AV_{DD} ≤ 5.5 V, I_{OH} = -3.0 mA	AV_{DD} - 0.7			V
			2.7 V ≤ AV_{DD} ≤ 5.5 V, I_{OH} = -2.0 mA	AV_{DD} - 0.6			V
			1.8 V ≤ AV_{DD} ≤ 5.5 V, I_{OH} = -1.5 mA	AV_{DD} - 0.5			V
Output voltage, low	V_{OL1}	P01 to P07, P10 to P17, P30 to P32, P35 to P37, P40, P43, P44, P50 to P53, P70 to P77, P80 to P86, P125 to P127	4.0 V ≤ V_{DD} ≤ 5.5 V, I_{OL} = 20.0 mA			1.3	V
			4.0 V ≤ V_{DD} ≤ 5.5 V, I_{OL} = 8.5 mA			0.7	V
			2.7 V ≤ V_{DD} ≤ 5.5 V, I_{OL} = 3.0 mA			0.6	V
			2.7 V ≤ V_{DD} ≤ 5.5 V, I_{OL} = 1.5 mA			0.4	V
			1.8 V ≤ V_{DD} ≤ 5.5 V, I_{OL} = 0.6 mA			0.4	V
	V_{OL2}	P20 to P27, P150, P151	4.0 V ≤ AV_{DD} ≤ 5.5 V, I_{OL} = 20.0 mA			1.3	V
			4.0 V ≤ AV_{DD} ≤ 5.5 V, I_{OL} = 8.5 mA			0.7	V
			2.7 V ≤ AV_{DD} ≤ 5.5 V, I_{OL} = 3.0 mA			0.6	V
			2.7 V ≤ AV_{DD} ≤ 5.5 V, I_{OL} = 1.5 mA			0.4	V
			1.8 V ≤ AV_{DD} ≤ 5.5 V, I_{OL} = 0.6 mA			0.4	V
	V_{OL3}	P60, P61	4.0 V ≤ V_{DD} ≤ 5.5 V, I_{OL} = 15.0 mA			2.0	V
			4.0 V ≤ V_{DD} ≤ 5.5 V, I_{OL} = 5.0 mA			0.4	V
			2.7 V ≤ V_{DD} ≤ 5.5 V, I_{OL} = 3.0 mA			0.4	V
			1.8 V ≤ V_{DD} ≤ 5.5 V, I_{OL} = 2.0 mA			0.4	V

Caution The maximum V_{IH} value on P02 to P04, P06, P07, P10, P12, P35 to P37, P40, P43, P44, P50 to P52, and P80 to P82 is V_{DD}, even in the N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(T_A = -40 to +85°C, 1.8 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V) **(5/5)**

Item	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Input leakage current, high	I_{LIH1}	P01 to P07, P10 to P17, P30 to P32, P35 to P37, P40, P43, P44, P50 to P53, P60, P61, P70 to P77, P80 to P86, P125 to P127, P137, $\overline{\text{RESET}}$	$V_I = V_{DD}$				1	μA
	I_{LIH2}	P20 to P27, P150, P151	$V_I = AV_{DD}$				1	μA
	I_{LIH3}	P121 to P124 (X1, X2, EXCLK, XT1, XT2, EXCLKS)	$V_I = V_{DD}$	In input port mode or when using external clock input			1	μA
				When a resonator is connected			10	μA
Input leakage current, low	I_{LIL1}	P01 to P07, P10 to P17, P30 to P32, P35 to P37, P40, P43, P44, P50 to P53, P60, P61, P70 to P77, P80 to P86, P125 to P127, P137, $\overline{\text{RESET}}$	$V_I = V_{SS}$				-1	μA
	I_{LIL2}	P20 to P27, P150, P151	$V_I = AV_{SS}$				-1	μA
	I_{LIL3}	P121 to P124 (X1, X2, EXCLK, XT1, XT2, EXCLKS)	$V_I = V_{SS}$	In input port mode or when using external clock input			-1	μA
				When a resonator is connected			-10	μA
On-chip pull-up resistance	R_{U1}	P01 to P07, P10 to P16, P30 to P32, P35 to P37, P50 to P53, P70 to P77, P125 to P127	$V_I = V_{SS}$, in input port mode	2.4 V ≤ V_{DD} ≤ 5.5 V	10	20	100	kΩ
				1.8 V ≤ V_{DD} < 2.4 V	10	30	100	kΩ
	R_{U2}	P17, P40, P43, P44, P80 to P86,	$V_I = V_{SS}$, in input port mode		10	20	100	kΩ
	R_{U3}	P20 to P27, P150 and P151	$V_I = AV_{SS}$, in input port mode		10	20	100	kΩ

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

39.3.2 Supply current characteristics

(T_A = -40 to +85°C, 1.8 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V) (1/2)

Parameter	Symbol	Conditions					MIN.	TYP.	MAX.	Unit
Supply current Note 1	I_{DD1}	Operating mode	HS (high-speed main) Mode Note 5	f_{IH} = 24 MHz Note 3	Basic operation	V_{DD} = 5.0 V		1.7		mA
						V_{DD} = 3.0 V		1.7		
					Normal operation	V_{DD} = 5.0 V		3.7	6.4	
						V_{DD} = 3.0 V		3.7	6.4	
				f_{IH} = 16 MHz Note 3	Normal operation	V_{DD} = 5.0 V		2.8	5.0	
						V_{DD} = 3.0 V		2.8	5.0	
			LS (low-speed main) Mode Note 5	f_{IH} = 8 MHz Note 3	Normal operation	V_{DD} = 3.0 V		1.2	2.1	mA
						V_{DD} = 2.0 V		1.2	2.1	
			HS (high-speed main) Mode Note 5	f_{MX} = 20 MHz Note 2, V_{DD} = 5.0 V	Normal operation	Square wave input		3.1	5.4	mA
						Resonator connection		3.3	5.5	
				f_{MX} = 20 MHz Note 2, V_{DD} = 3.0 V	Normal operation	Square wave input		3.0	5.4	
						Resonator connection		3.3	5.5	
				f_{MX} = 16 MHz Note 2, V_{DD} = 5.0 V	Normal operation	Square wave input		2.6	4.7	
						Resonator connection		2.8	4.8	
				f_{MX} = 16 MHz Note 2, V_{DD} = 3.0 V	Normal operation	Square wave input		2.6	4.7	
						Resonator connection		2.8	4.8	
				f_{MX} = 10 MHz Note 2, V_{DD} = 5.0 V	Normal operation	Square wave input		1.9	3.1	
						Resonator connection		1.9	3.1	
				f_{MX} = 10 MHz Note 2, V_{DD} = 3.0 V	Normal operation	Square wave input		1.9	3.1	
						Resonator connection		1.9	3.1	
			LS (low-speed main) Mode Note 5	f_{MX} = 8 MHz Note 2, V_{DD} = 3.0 V	Normal operation	Square wave input		1.1	2.1	mA
						Resonator connection		1.1	2.1	
				f_{MX} = 8 MH Note 2, V_{DD} = 2.0 V	Normal operation	Square wave input		1.1	2.1	
						Resonator connection		1.1	2.1	
			Subsystem clock operation	f_{SUB} = 32.768 kHz Note 4 T_A = -40°C	Normal operation	Square wave input		4.3	5.8	µA
						Resonator connection		4.6	5.8	
				f_{SUB} = 32.768 kHz Note 4 T_A = +25°C	Normal operation	Square wave input		4.3	5.8	
						Resonator connection		4.6	5.8	
				f_{SUB} = 32.768 kHz Note 4 T_A = +50°C	Normal operation	Square wave input		4.5	7.6	
						Resonator connection		4.5	7.6	
				f_{SUB} = 32.768 kHz Note 4 T_A = +70°C	Normal operation	Square wave input		4.7	9.2	
						Resonator connection		5.1	9.2	
				f_{SUB} = 32.768 kHz Note 4 T_A = +85°C	Normal operation	Square wave input		5.2	12.6	
						Resonator connection		5.7	12.6	
				f_{SUB} = 38.4 kHz Note 4 T_A = -40°C	Normal operation	Square wave input		5.0	6.8	µA
						Resonator connection		5.4	6.8	
				f_{SUB} = 38.4 kHz Note 4 T_A = +25°C	Normal operation	Square wave input		5.0	6.8	
						Resonator connection		5.4	6.8	
				f_{SUB} = 38.4 kHz Note 4 T_A = +50°C	Normal operation	Square wave input		5.3	8.9	
						Resonator connection		5.3	8.9	
				f_{SUB} = 38.4 kHz Note 4 T_A = +70°C	Normal operation	Square wave input		5.5	10.8	
						Resonator connection		6.0	10.8	
				f_{SUB} = 38.4 kHz Note 4 T_A = +85°C	Normal operation	Square wave input		6.1	14.8	
						Resonator connection		6.7	14.8	

(**Notes** and **Remarks** are listed on the next page.)

Note 1. Total current flowing into V_{DD} and AV_{DD}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD} or V_{SS}. The following points apply in the HS (high-speed main), and LS (low-speed main) modes.

- The currents in the "TYP." column do not include the operating currents of the peripheral modules.
- The currents in the "MAX." column include the operating currents of the peripheral modules, except for those flowing into the LCD controller/driver, A/D converter, LVD, I/O port, and on-chip pull-up/pull-down resistors, and those flowing while the data flash memory is being rewritten.

In the subsystem clock operation, the currents in both the "TYP." and "MAX." columns do not include the operating currents of the peripheral modules. However, in HALT mode, including the current flowing into the real-time Clock 2. The current flowing into AFE is not included.

Note 2. When high-speed on-chip oscillator and subsystem clock are stopped.

Note 3. When high-speed system clock and subsystem clock are stopped.

Note 4. When high-speed on-chip oscillator and high-speed system clock are stopped. When AMPHS1 = 1 (Ultra-low power consumption oscillation).

Note 5. Relationship between operation voltage width, operation frequency of CPU, and operation mode is as below.

HS (high-speed main) mode: 2.7 V ≤ V_{DD} ≤ 5.5 V @ 1 MHz to 24 MHz
2.4 V ≤ V_{DD} ≤ 5.5 V @ 1 MHz to 16 MHz
LS (low-speed main) mode: 1.8 V ≤ V_{DD} ≤ 5.5 V @ 1 MHz to 8 MHz

Remark 1. f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

Remark 2. f_{IH}: High-speed on-chip oscillator clock frequency

Remark 3. f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)

Remark 4. Except subsystem clock operation, temperature condition for the TYP. value is T_A = 25°C.

(T_A = -40 to +85°C, 1.8 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V) **(2/2)**

Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit
Supply current Note 1	I_{DD2} Note 2	HALT mode	HS (high-speed main) Mode Note 6	f_{IH} = 24 MHz Note 4	V_{DD} = 5.0 V		0.42	2.03	mA
					V_{DD} = 3.0 V		0.42	2.03	
				f_{IH} = 16 MHz Note 4	V_{DD} = 5.0 V		0.39	1.58	
					V_{DD} = 3.0 V		0.39	1.58	
			LS (low-speed main) Mode Note 6	f_{IH} = 8 MHz Note 4	V_{DD} = 3.0 V		0.25	0.81	mA
					V_{DD} = 2.0 V		0.25	0.81	
			HS (high-speed main) Mode Note 6	f_{MX} = 20 MHz Note 3 V_{DD} = 5.0 V	Square wave input		0.26	1.75	mA
					Resonator connection		0.40	1.88	
				f_{MX} = 20 MHz Note 3 V_{DD} = 3.0 V	Square wave input		0.25	1.75	
					Resonator connection		0.40	1.88	
				f_{MX} = 16 MHz Note 3 V_{DD} = 5.0 V	Square wave input		0.23	1.42	
					Resonator connection		0.36	1.59	
				f_{MX} = 16 MHz Note 3 V_{DD} = 3.0 V	Square wave input		0.22	1.42	
					Resonator connection		0.35	1.59	
				f_{MX} = 10 MHz Note 3 V_{DD} = 5.0 V	Square wave input		0.19	0.92	
					Resonator connection		0.29	1.00	
				f_{MX} = 10 MHz Note 3 V_{DD} = 3.0 V	Square wave input		0.18	0.92	
					Resonator connection		0.28	1.00	
			LS (low-speed main) Mode Note 6	f_{MX} = 8 MHz Note 3 V_{DD} = 3.0 V	Square wave input		0.09	0.61	mA
					Resonator connection		0.15	0.66	
				f_{MX} = 8 MHz Note 3 V_{DD} = 2.0 V	Square wave input		0.10	0.62	
					Resonator connection		0.15	0.67	
			Subsystem clock operation	f_{SUB} = 32.768 kHz Note 5 T_A = -40°C	Square wave input		0.32	0.69	µA
					Resonator connection		0.51	0.89	
				f_{SUB} = 32.768 kHz Note 5 T_A = +25°C	Square wave input		0.41	0.82	
					Resonator connection		0.62	1.00	
				f_{SUB} = 32.768 kHz Note 5 T_A = +50°C	Square wave input		0.52	1.40	
					Resonator connection		0.75	1.60	
				$_{SUB}$ = 32.768 kHz Note 5 T_A = +70°C	Square wave input		0.82	2.70	
					Resonator connection		1.08	2.90	
				f_{SUB} = 32.768 kHz Note 5 T_A = +85°C	Square wave input		1.38	4.95	
					Resonator connection		1.62	5.15	
				f_{SUB} = 38.4 kHz Note 5 T_A = -40°C	Square wave input		0.38	0.81	µA
					Resonator connection		0.60	1.04	
				f_{SUB} = 38.4 kHz Note 5 T_A = +25°C	Square wave input		0.48	0.96	
					Resonator connection		0.73	1.17	
				f_{SUB} = 38.4 kHz Note 5 T_A = +50°C	Square wave input		0.61	1.64	
					Resonator connection		0.88	1.88	
				$_{SUB}$ = 38.4 kHz Note 5 T_A = +70°C	Square wave input		0.96	3.16	
					Resonator connection		1.27	3.40	
				f_{SUB} = 38.4 kHz Note 5 T_A = +85°C	Square wave input		1.62	5.80	
					Resonator connection		1.90	6.04	
	I_{DD3}	STOP mode Note 7	T_A = -40°C				0.20	0.59	µA
			T_A = +25°C				0.26	0.72	
			T_A = +50°C				0.33	1.30	
			T_A = +70°C				0.53	2.60	
			T_A = +85°C				0.93	4.85	

(**Notes** and **Remarks** are listed on the next page.)

Note 1. Total current flowing into V_{DD} and AV_{DD}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD} or V_{SS}. The following points apply in the HS (high-speed main), and LS (low-speed main) modes.

- The currents in the "TYP." column do not include the operating currents of the peripheral modules.
- The currents in the "MAX." column include the operating currents of the peripheral modules, except for those flowing into the LCD controller/driver, A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors, and those flowing while the data flash memory is being rewritten.

In the subsystem clock operation, the currents in both the "TYP." and "MAX." columns do not include the operating currents of the peripheral modules. However, in HALT mode, including the current flowing into the real-time Clock 2.

In the STOP mode, the currents in both the "TYP." and "MAX." columns do not include the operating currents of the peripheral modules. The current flowing into AFE is not included.

Note 2. During HALT instruction execution from flash memory

Note 3. When the high-speed on-chip oscillator and the subsystem clock are stopped

Note 4. When the high-speed system clock and the subsystem clock are stopped

Note 5. When high-speed on-chip oscillator and high-speed system clock are stopped. When RTCLPC = 1 and setting ultra-low current consumption (AMPHS1 = 1).

Note 6. Relationship between operation voltage width, operation frequency of CPU, and operation mode is as below.

HS (high-speed main) Mode: 2.7 V ≤ V_{DD} ≤ 5.5 V @ 1 MHz to 24 MHz
2.4 V ≤ V_{DD} ≤ 5.5 V @ 1 MHz to 16 MHz
LS (low-speed main) Mode: 1.8 V ≤ V_{DD} ≤ 5.5 V @ 1 MHz to 8 MHz

Note 7. Regarding the value for current to operate the subsystem clock in STOP mode, refer to that in HALT mode.

Remark 1. f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

Remark 2. f_{IH}: High-speed on-chip oscillator clock frequency

Remark 3. f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)

Remark 4. Except subsystem clock operation, temperature condition of the TYP. value is T_A = 25°C.

• Peripheral functions

(T_A = -40 to +85°C, 1.8 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V) **(1/2)**

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Low-speed on-chip oscillator operating current	I_{FIL} Note 1				0.20		μA
RTC2 operating current	I_{RTC} Notes 1, 3	f_{SUB} = 32.768 kHz			0.02		μA
12-bit Interval timer operating current	I_{TMKA} Notes 1, 2, 4	f_{SUB} = 38.4 kHz, f_{MAIN} stopped			0.02		μA
		f_{SUB} = 32.768 kHz, f_{MAIN} stopped			0.02		μA
8-bit Interval timer operating current	I_{TMRT} Notes 1, 14	f_{SUB} = 38.4 kHz, f_{MAIN} stopped, per unit	8-bit counter mode × 2-channel operation		0.14		μA
			16-bit counter mode operation		0.12		μA
		f_{SUB} = 32.768 kHz, f_{MAIN} stopped, per unit	8-bit counter mode × 2-channel operation		0.12		μA
			16-bit counter mode operation		0.10		μA
Watchdog timer operating current	I_{WDT} Notes 1, 5	f_{IL} = 15 kHz			0.22		μA
10-bit A/D converter operating current	I_{ADC} Notes 1, 6	When conversion at maximum speed	Normal mode, V_{DD} = 5.0 V		1.3	1.7	mA
			Low-voltage mode, V_{DD} = 3.0 V		0.5	0.7	mA
Internal reference voltage (1.45 V) current	I_{ADREF} Notes 1, 7				85		μA
Temperature sensor operating current	I_{TMPS} Note 1				85		μA
LVD operating current	I_{LVI} Notes 1, 8				0.06		μA
Self-programming operating current	I_{FSP} Notes 1, 9				2.0	12.2	mA
BGO operating current	I_{BGO} Notes 1, 10				2.0	12.2	mA
SNOOZE operating current	I_{SNOZ} Notes 1, 11	A/D converter operation	The mode is performed		0.50	0.60	mA
			During A/D conversion, low-voltage mode, V_{DD} = 3.0 V		1.20	1.44	
		Simplified SPI(CSI)/UART operation			0.70	0.84	
		DTC operation			3.1		

(**Notes** and **Remarks** are listed on the page after the next page.)

(T_A = -40 to +85°C, 1.8 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V) **(2/2)**

Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit
LCD operating current	I_{LCD1} Notes 12, 13	External resistance division method	f_{LCD} = f_{SUB} (32.768 kHz) LCD clock = 128 Hz	1/3 bias 4-time slice	V_{DD} = 5.0 V V_{L4} = 5.0 V		0.04	0.20	µA
			f_{LCD} = f_{SUB} (38.4 kHz) LCD clock = 75 Hz				0.08	0.40	
	I_{LCD2} Note 12	Internal voltage boosting method	f_{LCD} = f_{SUB} (32.768 kHz) LCD clock = 128 Hz	1/3 bias 4-time slice	V_{DD} = 3.0 V V_{L4} = 3.0 V (VLCD = 04H)		0.85	2.20	µA
			f_{LCD} = f_{SUB} (38.4 kHz) LCD clock = 75 Hz				0.50	2.20	
			f_{LCD} = f_{SUB} (32.768 kHz) LCD clock = 128 Hz		V_{DD} = 5.0 V V_{L4} = 5.1 V (VLCD = 12H)		1.55	3.70	µA
			f_{LCD} = f_{SUB} (38.4 kHz) LCD clock = 75 Hz				0.91	3.70	
	I_{LCD3} Note 12	Capacitor split method	f_{LCD} = f_{SUB} (32.768 kHz) LCD clock = 128 Hz	1/3 bias 4-time slice	V_{DD} = 3.0 V V_{L4} = 3.0 V		0.20	0.50	µA
			f_{LCD} = f_{SUB} (38.4 kHz) LCD clock = 75 Hz				0.13	0.50	
Operating currents of the meter-dedicated macro	I_{TMRJ} Note 15	f_{SUB} = 38.4 kHz, f_{MAIN} stopped, per unit					0.10		µA
	I_{UARTMG} Note 15	f_{SUB} = 38.4 kHz, f_{MAIN} stopped					0.12		µA
	I_{SMOTD} Note 15	f_{SUB} = 38.4 kHz, f_{MAIN} stopped					0.10		µA
	I_{EXSD} Note 15	f_{SUB} = 38.4 kHz, f_{MAIN} stopped					0.02		µA

(**Notes** and **Remarks** are listed on the next page.)

Note 1. Current flowing to V_{DD}.

Note 2. When the high-speed on-chip oscillator and high-speed system clock are stopped.

Note 3. Current flowing only to the real-time clock 2 (excluding the operating current of the low-speed on-chip oscillator and the XT1 oscillator). The supply current of the RL78 microcontrollers is the sum of the values of either I_{DD1} or I_{DD2}, and I_{RTC}, when the real-time clock 2 is operating in operation mode or HALT mode. When the low-speed on-chip oscillator is selected, I_{FIL} should be added. I_{DD2} subsystem clock operation includes the operational current of the real-time clock 2.

Note 4. Current flowing only to the 12-bit interval timer (excluding the operating current of the low-speed on-chip oscillator and the XT1 oscillator). The supply current of the RL78 microcontrollers is the sum of the values of either I_{DD1} or I_{DD2}, and I_{TMKA}, when the 12-bit interval timer operates in the operating mode or HALT mode. When the low-speed on-chip oscillator is selected, I_{FIL} should be added. I_{DD2} subsystem clock operation includes the operational current of the 12-bit interval timer.

Note 5. Current flowing only to the watchdog timer (including the operating current of the low-speed on-chip oscillator). The supply current of the RL78 microcontrollers is the sum of I_{DD1}, I_{DD2} or I_{DD3} and I_{WDT} when the watchdog timer is operating.

Note 6. Current flowing only to the A/D converter. The supply current of the RL78 microcontrollers is the sum of I_{DD1} or I_{DD2}, I_{ADC}, and I_{ADREF} when the A/D converter operates in the operating mode or the HALT mode.

Note 7. Operation current flowing to the internal reference voltage.

Note 8. Current flowing only to the LVD circuit. The supply current of the RL78 microcontrollers is the sum of I_{DD1}, I_{DD2}, or I_{DD3} and ILVI when the LVD circuit operates in the operating mode, HALT mode, or STOP mode.

Note 9. Current flowing during self-programming

Note 10. Current flowing during writing to the data flash

Note 11. For time required to shift to the SNOOZE mode, see **27.3.3 SNOOZE mode**.

Note 12. Current flowing only to the LCD controller/driver (V_{DD} pin). The current value of the RL78 microcontrollers is the sum of the LCD operating current (I_{LCD1}, I_{LCD2}, or I_{LCD3}) and the supply current (I_{DD1} or I_{DD2}) when the LCD controller/driver operates in the operating mode or HALT mode. Not including the current that flows through the LCD panel.

Note 13. Not including the current that flows through the external divider resistor.

Note 14. Current flowing only to the 8-bit interval timer (excluding the operating current of the low-speed on-chip oscillator and the XT1 oscillator). The supply current of the RL78 microcontrollers is the sum of the values of either I_{DD1} or I_{DD2}, and IIT, when the 8-bit interval timer operates in the operating mode or HALT mode. When the low-speed on-chip oscillator is selected, I_{FIL} should be added.

Note 15. The current value of the RL78 microcontrollers is the sum of I_{DD2} or I_{DD3} and I_{TMRJ}, I_{UARTMG}, I_{SMOTD}, or I_{EXSD} when each module operates in the sub-HALT mode or STOP mode.

Remark 1. f_{IL}: Low-speed on-chip oscillator clock frequency

Remark 2. f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)

Remark 3. f_{CLK}: CPU/peripheral hardware clock frequency

Remark 4. The temperature condition for the TYP. value is T_A = 25°C.

39.4 AC Characteristics

(T_A = -40 to +85°C, 1.8 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V) **(1/2)**

Items	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Instruction cycle (minimum instruction execution time)	T_{CY}	Main system clock (f_{MAIN}) operation	HS (high-speed main) Mode	2.7 V ≤ V_{DD} ≤ 5.5 V	0.0417		1	µs
				2.4 V ≤ V_{DD} < 2.7 V	0.0625		1	µs
			LS (low-speed main) Mode	1.8 V ≤ V_{DD} ≤ 5.5 V	0.125		1	µs
		Subsystem clock (f_{SUB}) operation	f_{XT} = 38.4 kHz	1.8 V ≤ V_{DD} ≤ 5.5 V		26.04		µs
			f_{XT} = 32.768 kHz	1.8 V ≤ V_{DD} ≤ 5.5 V	28.5	30.5	31.3	µs
		In the self-programming mode	HS (high-speed main) Mode	2.7 V ≤ V_{DD} ≤ 5.5 V	0.0417		1	µs
				2.4 V ≤ V_{DD} < 2.7 V	0.0625		1	µs
			LS (low-speed main) Mode	1.8 V ≤ V_{DD} ≤ 5.5 V	0.125		1	µs
External system clock frequency	f_{EX}	EXCLK		2.7 V ≤ V_{DD} ≤ 5.5 V	1.0		20.0	MHz
				2.4 V ≤ V_{DD} < 2.7 V	1.0		16.0	MHz
				1.8 V ≤ V_{DD} < 2.4 V	1.0		8.0	MHz
	f_{EXT}	EXCLKS			32		35	kHz
External system clock input high-level width, low-level width	t_{EXH}, t_{EXL}	EXCLK		2.7 V ≤ V_{DD} ≤ 5.5 V	24			ns
				2.4 V ≤ V_{DD} < 2.7 V	30			ns
				1.8 V ≤ V_{DD} < 2.4 V	60			ns
	t_{EXHS}, t_{EXLS}	EXCLKS			13.7			µs
Timer input high-level width, low-level width	t_{TIH}, t_{TIL}	TI00 to TI07			1/f_{MCK} + 10			ns
Timer RJ input cycle	t_C	TRJIO0, TRJIO1		2.7 V ≤ V_{DD} ≤ 5.5 V	100			ns
				1.8 V ≤ V_{DD} < 2.7 V	300			ns
Timer RJ input high-level width, low-level width	t_{TJIH}, t_{TJIL}	TRJIO0, TRJIO1		2.7 V ≤ V_{DD} ≤ 5.5 V	40			ns
				1.8 V ≤ V_{DD} < 2.7 V	120			ns
Timer output frequency	f_{TO}	TO00 to TO07 TRJIO0, TRJIO1, TRJO0, TRJO1	HS (high-speed main) Mode	4.0 V ≤ V_{DD} ≤ 5.5 V			12	MHz
				2.7 V ≤ V_{DD} < 4.0 V			8	MHz
				2.4 V ≤ V_{DD} < 2.7 V			4	MHz
			LS (low-speed main) Mode	1.8 V ≤ V_{DD} ≤ 5.5 V			4	MHz
Buzzer output frequency	f_{PCL}	PCLBUZ0, PCLBUZ1	HS (high-speed main) Mode	4.0 V ≤ V_{DD} ≤ 5.5 V			12	MHz
				2.7 V ≤ V_{DD} < 4.0 V			8	MHz
				2.4 V ≤ V_{DD} < 2.7 V			4	MHz
			LS (low-speed main) Mode	1.8 V ≤ V_{DD} ≤ 5.5 V			4	MHz

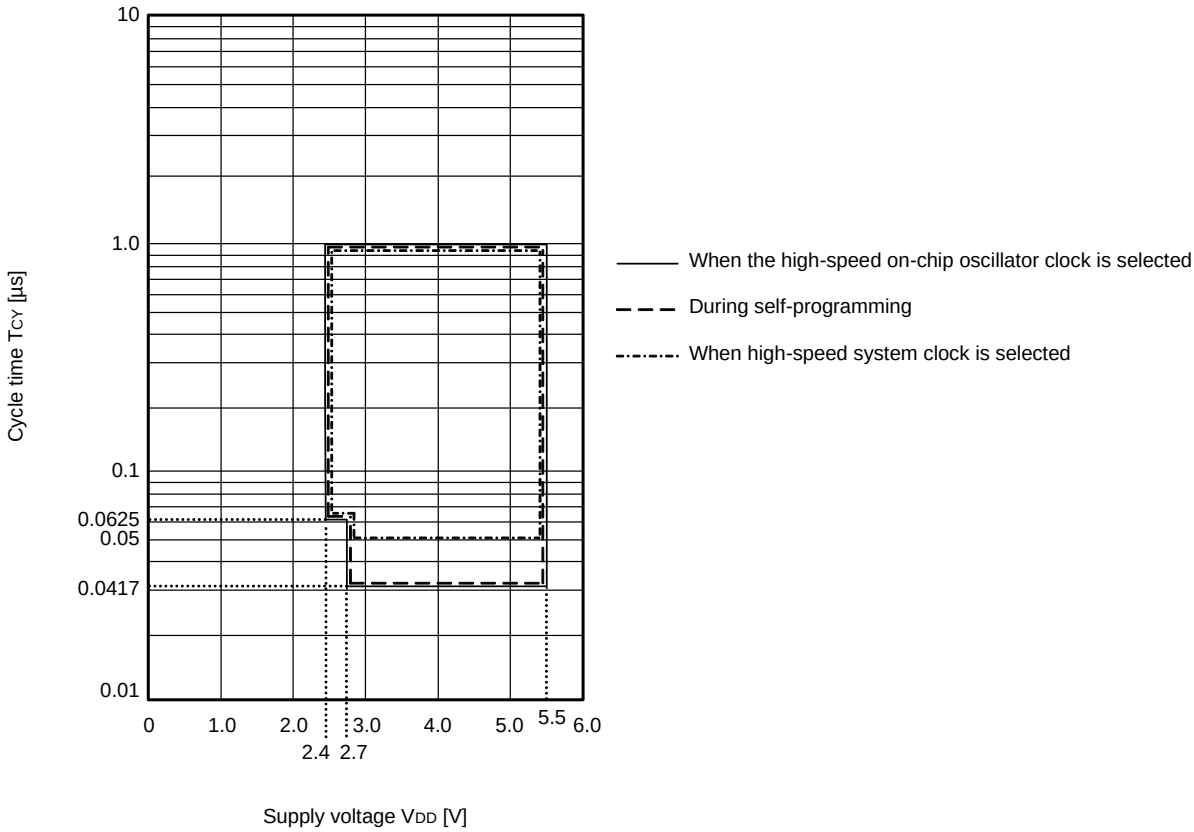
(T_A = -40 to +85°C, 1.8 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V) **(2/2)**

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Interrupt input high-level width, low-level width	t_{INTH}, t_{INTL}	INTP0 to INTP7 (when the pin on which the function is in use is multiplexed with pin functions other than P27 to P22)	1.8 V ≤ V_{DD} ≤ 5.5 V	1			µs
		INTP2 to INTP7 (when the pin on which the function is in use is multiplexed with a pin function from among P27 to P22)	1.8 V ≤ AV_{DD} ≤ 5.5 V	1			µs
$\overline{\text{RESET}}$ low-level width	t_{RSL}			10			µs

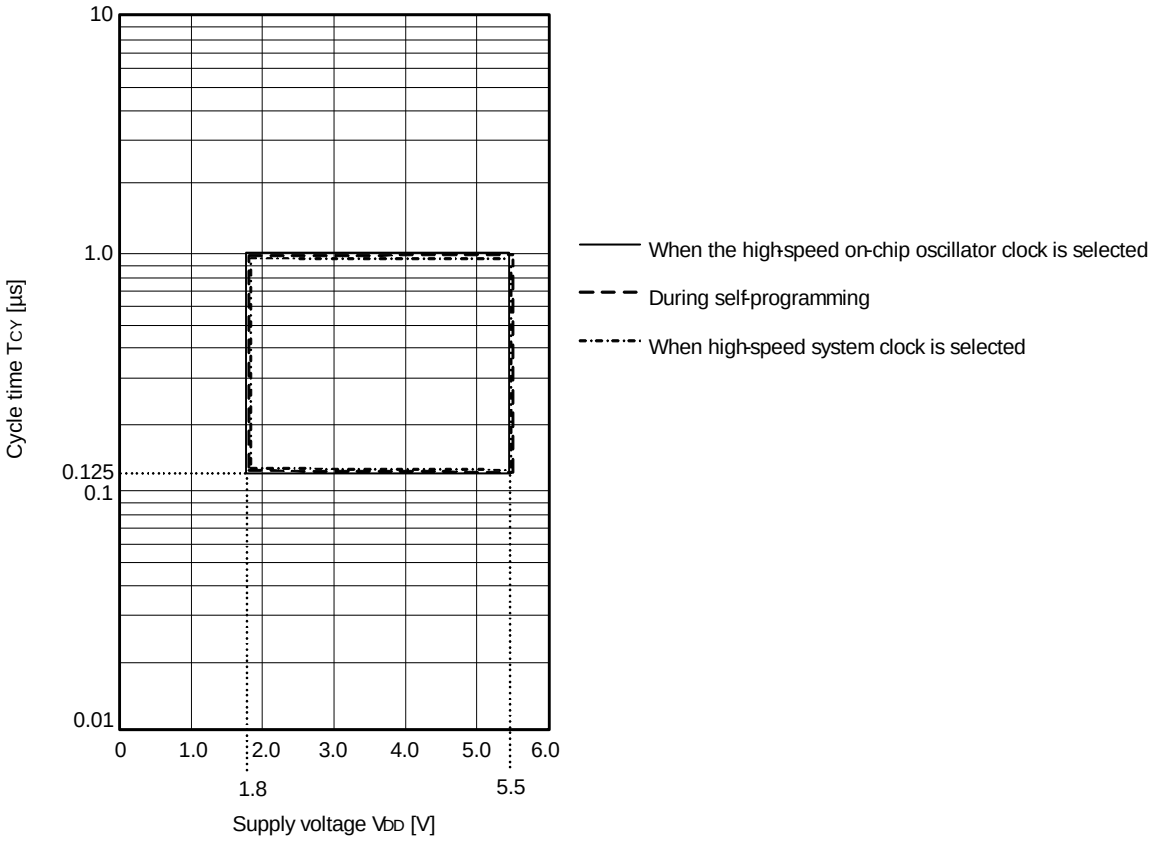
Remark f_{MCK}: Timer array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of timer mode register mn (TMRmn). m: Unit number (m = 0), n: Channel number (n = 0 to 7))

Minimum Instruction Execution Time During Main System Clock Operation

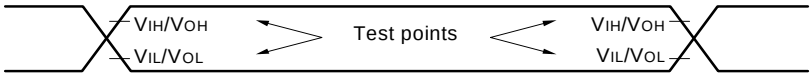
TCY vs VDD (HS (high-speed main) mode)



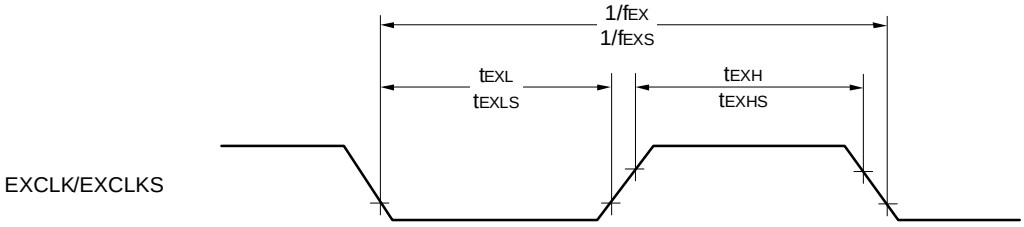
T_{CY} vs V_{DD} (LS (low-speed main) mode)



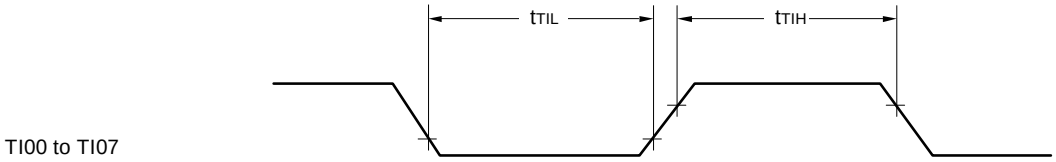
AC Timing Test Points

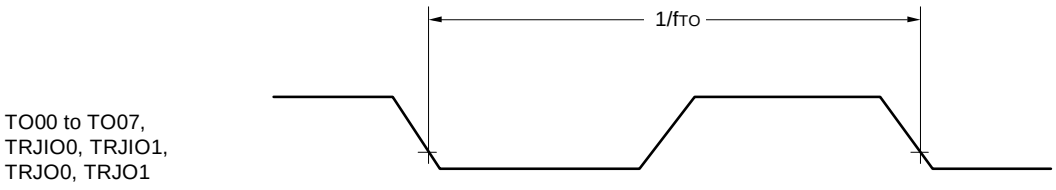


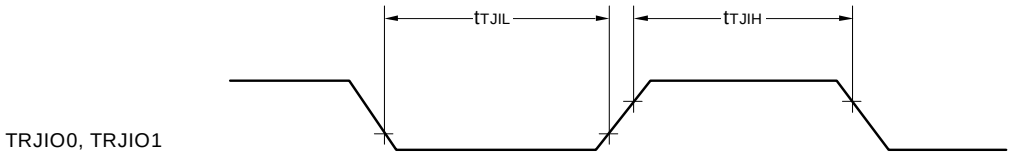
External System Clock Timing



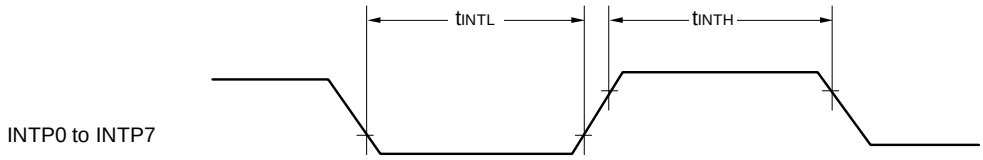
TI/TO Timing



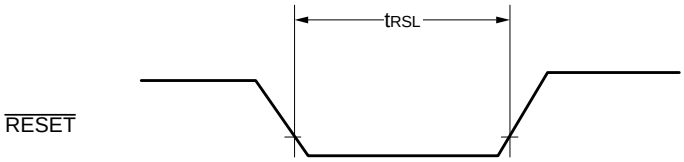




Interrupt Request Input Timing



$\overline{\text{RESET}}$ Input Timing



39.5 Peripheral Functions Characteristics

39.5.1 Serial array unit

(1) During communication at same potential (UART mode)

(T_A = -40 to +85°C, 1.8 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	
Transfer rate Note 1		2.4 V ≤ V_{DD} ≤ 5.5 V		f_{MCK}/6 Note 2		f_{MCK}/6 Note 2	bps
		Theoretical value of the maximum transfer rate f_{MCK} = f_{CLK} Note 3		4.0		1.3	Mbps
		1.8 V ≤ V_{DD} ≤ 5.5 V	—			f_{MCK}/6	bps
		Theoretical value of the maximum transfer rate f_{MCK} = f_{CLK} Note 3	—			1.3	Mbps

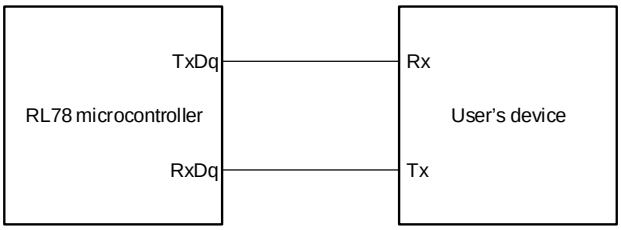
Note 1. Transfer rate in the SNOOZE mode is 4800 bps only.

Note 2. The following conditions are required for low voltage interface.
2.4 V ≤ V_{DD} < 2.7 V: MAX. 2.6 Mbps
1.8 V ≤ V_{DD} < 2.4 V: MAX. 1.3 Mbps

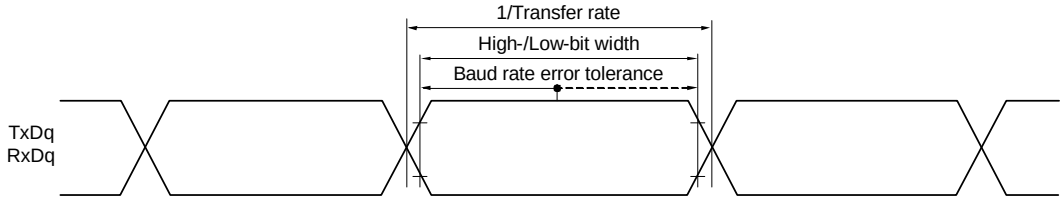
Note 3. The maximum operating frequencies of the CPU/peripheral hardware clock (f_{CLK}) are:
HS (high-speed main) mode: 24 MHz (2.7 V ≤ V_{DD} ≤ 5.5 V)
16 MHz (2.4 V ≤ V_{DD} ≤ 5.5 V)
LS (low-speed main) mode: 8 MHz (1.8 V ≤ V_{DD} ≤ 5.5 V)

Caution Select the normal input buffer for the RxDq pin and the normal output mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg).

UART mode connection diagram (during communication at same potential)



UART mode bit width (during communication at same potential) (reference)



Remark 1. q: UART number (q = 0 to 2), g: PIM or POM number (g = 0, 1, 3, 4, 5, 8)

Remark 2. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03, 10, 11))

(2) During communication at same potential (Simplified SPI(CSI) mode) (master mode, SCKp... internal clock output)

(T_A = -40 to +85°C, 1.8 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	
SCKp cycle time	t_{KCY1}	t_{KCY1} ≥ 4/f_{CLK}	2.7 V ≤ V_{DD} ≤ 5.5 V	167		500		ns
			2.4 V ≤ V_{DD} ≤ 5.5 V	250		500		ns
			1.8 V ≤ V_{DD} ≤ 5.5 V	—		500		ns
SCKp high-/low-level width	t_{KH1}, t_{KL1}	4.0 V ≤ V_{DD} ≤ 5.5 V		t_{KCY1}/2 - 12		t_{KCY1}/2 - 50		ns
		2.7 V ≤ V_{DD} ≤ 5.5 V		t_{KCY1}/2 - 18		t_{KCY1}/2 - 50		ns
		2.4 V ≤ V_{DD} ≤ 5.5 V		t_{KCY1}/2 - 38		t_{KCY1}/2 - 50		ns
		1.8 V ≤ V_{DD} ≤ 5.5 V		—		t_{KCY1}/2 - 50		ns
SIp setup time (to SCKp↑) Note 1	t_{SIK1}	4.0 V ≤ V_{DD} ≤ 5.5 V		44		110		ns
		2.7 V ≤ V_{DD} ≤ 5.5 V		44		110		ns
		2.4 V ≤ V_{DD} ≤ 5.5 V		75		110		ns
		1.8 V ≤ V_{DD} ≤ 5.5 V		—		110		ns
SIp hold time (from SCKp↑) Note 2	t_{KSI1}	2.4 V ≤ V_{DD} ≤ 5.5 V		19		19		ns
		1.8 V ≤ V_{DD} ≤ 5.5 V		—		19		ns
Delay time from SCKp↓ to SOp output Note 3	t_{KSO1}	C = 30 pF Note 4	2.7 V ≤ V_{DD} ≤ 5.5 V		25		50	ns
			2.4 V ≤ V_{DD} ≤ 5.5 V		25		50	ns
			1.8 V ≤ V_{DD} ≤ 5.5 V		—		50	ns

Note 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes “to SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes “from SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes “from SCKp↑” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 4. C is the load capacitance of the SCKp and SOp output lines.

Caution Select the normal input buffer for the SIp pin and the normal output mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remark 1. p: CSI number (p = 00, 10, 20), m: Unit number (m = 0, 1), n: Channel number (n = 0, 2), g: PIMand POM number (g = 0, 1, 3, 4, 5, 8)

Remark 2. f_{MCK}: Serial array unit operation clock frequency (Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00, 02, 10))

(3) During communication at same potential (Simplified SPI(CSI) mode) (slave mode, SCKp... external clock input)

(T_A = -40 to +85°C, 1.8 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V) (1/2)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	
SCKp cycle time Note 5	t_{KCY2}	4.0 V ≤ V_{DD} ≤ 5.5 V	20 MHz < f_{MCK}	8/f_{MCK}		—		ns
			f_{MCK} ≤ 20 MHz	8/f_{MCK}		6/f_{MCK}		ns
		2.7 V ≤ V_{DD} ≤ 5.5 V	16 MHz > f_{MCK}	8/f_{MCK}		—		ns
			f_{MCK} ≤ 16 MHz	6/f_{MCK}		6/f_{MCK}		ns
		2.4 V ≤ V_{DD} ≤ 5.5 V		6/f_{MCK} and 500		6/f_{MCK} and 500		ns
		1.8 V ≤ V_{DD} ≤ 5.5 V		—		6/f_{MCK} and 750		ns
SCKp high-/low-level width	t_{KH2}, t_{KL2}	4.0 V ≤ V_{DD} ≤ 5.5 V		t_{KCY2}/2 - 7		t_{KCY2}/2 - 7		ns
		2.7 V ≤ V_{DD} ≤ 5.5 V		t_{KCY2}/2 - 8		t_{KCY2}/2 - 8		ns
		2.4 V ≤ V_{DD} ≤ 5.5 V		t_{KCY2}/2 - 18		t_{KCY2}/2 - 18		ns
		1.8 V ≤ V_{DD} ≤ 5.5 V		—		t_{KCY2}/2 - 18		ns
SIp setup time (to SCKp↑) Note 1	t_{SIK2}	2.7 V ≤ V_{DD} ≤ 5.5 V		1/f_{MCK} + 20		1/f_{MCK} + 30		ns
		2.4 V ≤ V_{DD} ≤ 5.5 V		1/f_{MCK} + 30		1/f_{MCK} + 30		ns
		1.8 V ≤ V_{DD} ≤ 5.5 V		—		1/f_{MCK} + 30		ns
SIp hold time (from SCKp↑) Note 2	t_{KSI2}	2.4 V ≤ V_{DD} ≤ 5.5 V		1/f_{MCK} + 31		1/f_{MCK} + 31		ns
		1.8 V ≤ V_{DD} ≤ 5.5 V		—		1/f_{MCK} + 31		ns
Delay time from SCKp↓ to SOp output Note 3	t_{KSO2}	C = 30 pF Note 4	2.7 V ≤ V_{DD} ≤ 5.5 V		2/f_{MCK} + 44		2/f_{MCK} + 110	ns
			2.4 V ≤ V_{DD} ≤ 5.5 V		2/f_{MCK} + 75		2/f_{MCK} + 110	ns
			1.8 V ≤ V_{DD} ≤ 5.5 V		—		2/f_{MCK} + 110	ns

Note 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes "to SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes "from SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 4. C is the load capacitance of the SOp output lines.

Note 5. The maximum transfer rate when using the SNOOZE mode is 1 Mbps.

Caution Select the normal input buffer for the SIp and SCKp pins and the normal output mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remark 1. p: CSI number (p = 00, 10, 20), m: Unit number (m = 0, 1), n: Channel number (n = 0, 2), g: PIM number (g = 0, 1, 3, 4, 5, 8)

Remark 2. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00, 02, 10))

(3) During communication at same potential (Simplified SPI(CSI) mode) (slave mode, SCKp... external clock input)

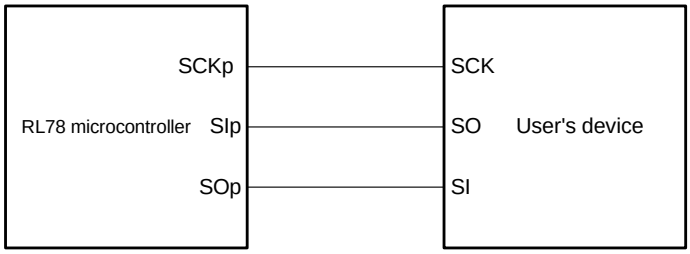
(T_A = -40 to +85°C, 1.8 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V) **(2/2)**

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	
$\overline{SSI00}$ setup time	t_{SSIK}	DAPmn = 0	2.7 V ≤ V_{DD} ≤ 5.5 V	120		120		ns
			2.4 V ≤ V_{DD} ≤ 5.5 V	200		200		ns
			1.8 V ≤ V_{DD} ≤ 5.5 V	—		200		ns
		DAPmn = 1	2.7 V ≤ V_{DD} ≤ 5.5 V	1/f_{MCK} + 120		1/f_{MCK} + 120		ns
			2.4 V ≤ V_{DD} ≤ 5.5 V	1/f_{MCK} + 200		1/f_{MCK} + 200		ns
			1.8 V ≤ V_{DD} ≤ 5.5 V	—		1/f_{MCK} + 200		ns
$\overline{SSI00}$ hold time	t_{KSSI}	DAPmn = 0	2.7 V ≤ V_{DD} ≤ 5.5 V	1/f_{MCK} + 120		1/f_{MCK} + 120		ns
			2.4 V ≤ V_{DD} ≤ 5.5 V	1/f_{MCK} + 200		1/f_{MCK} + 200		ns
			1.8 V ≤ V_{DD} ≤ 5.5 V	—		1/f_{MCK} + 200		ns
		DAPmn = 1	2.7 V ≤ V_{DD} ≤ 5.5 V	120		120		ns
			2.4 V ≤ V_{DD} ≤ 5.5 V	200		200		ns
			1.8 V ≤ V_{DD} ≤ 5.5 V	—		200		ns

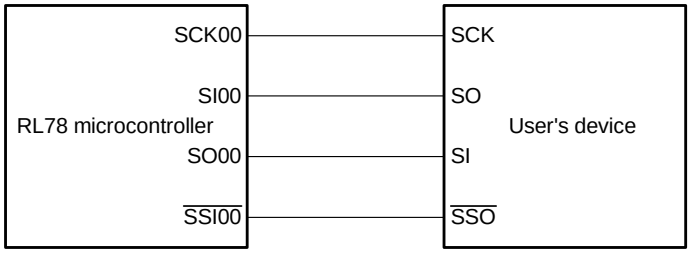
Caution **Select the normal input buffer for the SIp and SCKp pins and the normal output mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg).**

Remark p: CSI number (p = 00), m: Unit number (m = 0), n: Channel number (n = 0), g: PIM number (g = 3, 4)

Simplified SPI(CSI) mode connection diagram (during communication at same potential)

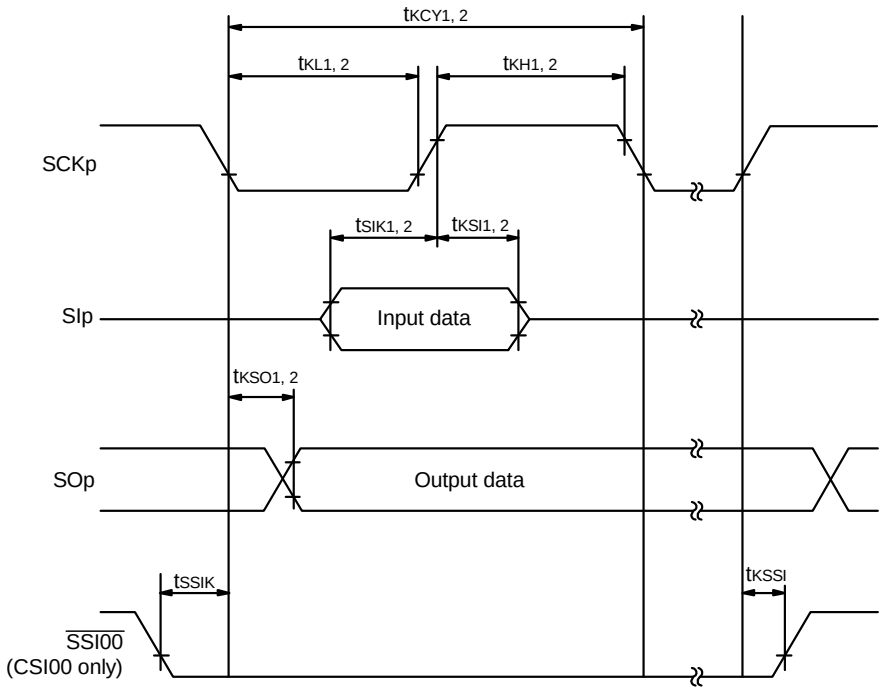


Simplified SPI(CSI) mode connection diagram (during communication at same potential)
(Slave transmission of slave select input function (CSI00))

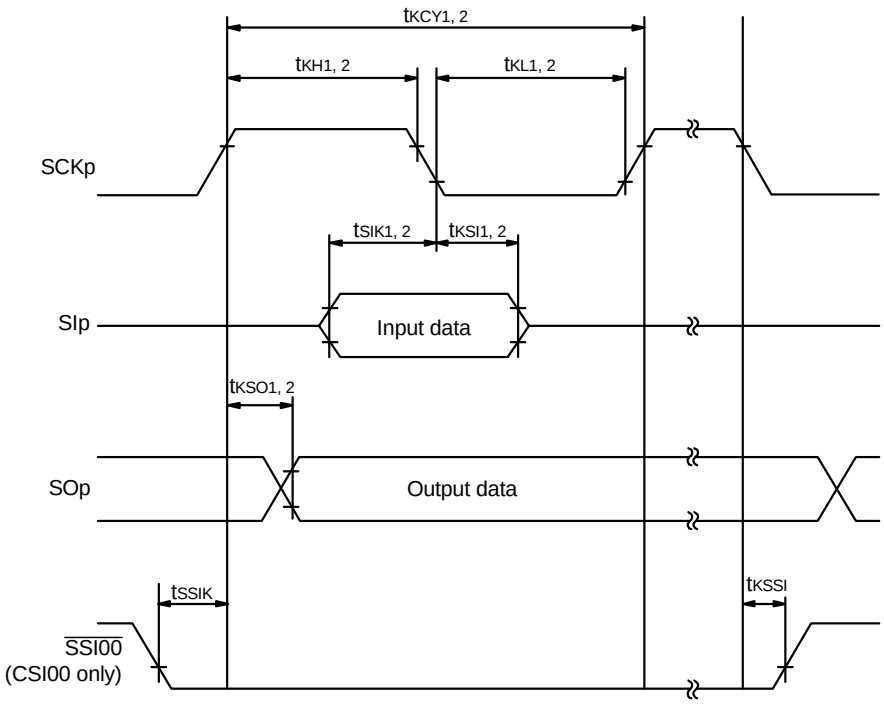


Remark p: CSI number (p = 00, 10, 20), m: Unit number (m = 0, 1), n: Channel number (n = 0, 2)

Simplified SPI(CSI) mode serial transfer timing (during communication at same potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)



Simplified SPI(CSI) mode serial transfer timing (during communication at same potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)



Remark p: CSI number (p = 00, 10, 20), m: Unit number (m = 0, 1), n: Channel number (n = 0, 2)

(4) During communication at same potential (simplified I²C mode)

(T_A = -40 to +85°C, 1.8 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	
SCLr clock frequency	f_{SCL}	2.7 V ≤ V_{DD} ≤ 5.5 V, C_b = 50 pF, R_b = 2.7 kΩ		1000 Note 1		400 Note 1	kHz
		1.8 V (2.4 V Note 3) ≤ V_{DD} ≤ 5.5 V, C_b = 100 pF, R_b = 3 kΩ		400 Note 1		400 Note 1	kHz
		1.8 V (2.4 V Note 3) ≤ V_{DD} < 2.7 V, C_b = 100 pF, R_b = 5 kΩ		300 Note 1		300 Note 1	kHz
Hold time when SCLr = “L”	t_{LOW}	2.7 V ≤ V_{DD} ≤ 5.5 V, C_b = 50 pF, R_b = 2.7 kΩ	475		1150		ns
		1.8 V (2.4 V Note 3) ≤ V_{DD} ≤ 5.5 V, C_b = 100 pF, R_b = 3 kΩ	1150		1150		ns
		1.8 V (2.4 V Note 3) ≤ V_{DD} < 2.7 V, C_b = 100 pF, R_b = 5 kΩ	1550		1550		ns
Hold time when SCLr = “H”	t_{HIGH}	2.7 V ≤ V_{DD} ≤ 5.5 V, C_b = 50 pF, R_b = 2.7 kΩ	475		1150		ns
		1.8 V (2.4 V Note 3) ≤ V_{DD} ≤ 5.5 V, C_b = 100 pF, R_b = 3 kΩ	1150		1150		ns
		1.8 V (2.4 V Note 3) ≤ V_{DD} < 2.7 V, C_b = 100 pF, R_b = 5 kΩ	1550		1550		ns
Data setup time (reception)	$t_{SU:DAT}$	2.7 V ≤ V_{DD} ≤ 5.5 V, C_b = 50 pF, R_b = 2.7 kΩ	1/f_{MCK} + 85 Note 2		1/f_{MCK} + 145 Note 2		ns
		1.8 V (2.4 V Note 3) ≤ V_{DD} ≤ 5.5 V, C_b = 100 pF, R_b = 3 kΩ	1/f_{MCK} + 145 Note 2		1/f_{MCK} + 145 Note 2		ns
		1.8 V (2.4 V Note 3) ≤ V_{DD} < 2.7 V, C_b = 100 pF, R_b = 5 kΩ	1/f_{MCK} + 230 Note 2		1/f_{MCK} + 230 Note 2		ns
Data hold time (transmission)	$t_{HD:DAT}$	2.7 V ≤ V_{DD} ≤ 5.5 V, C_b = 50 pF, R_b = 2.7 kΩ	0	305	0	305	ns
		1.8 V (2.4 V Note 3) ≤ V_{DD} ≤ 5.5 V, C_b = 100 pF, R_b = 3 kΩ	0	355	0	355	ns
		1.8 V (2.4 V Note 3) ≤ V_{DD} < 2.7 V, C_b = 100 pF, R_b = 5 kΩ	0	405	0	405	ns

Note 1. The value must be equal to or less than f_{MCK}/4.

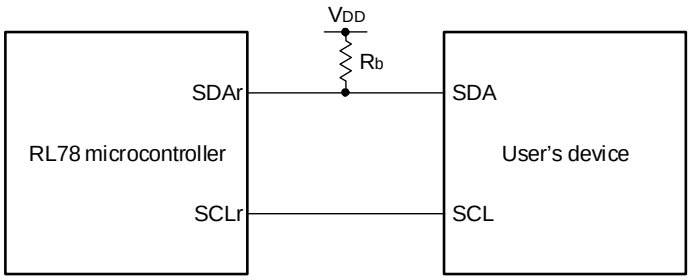
Note 2. Set the f_{MCK} value to keep the hold time of SCLr = “L” and SCLr = “H”.

Note 3. Condition in the HS (high-speed main) mode

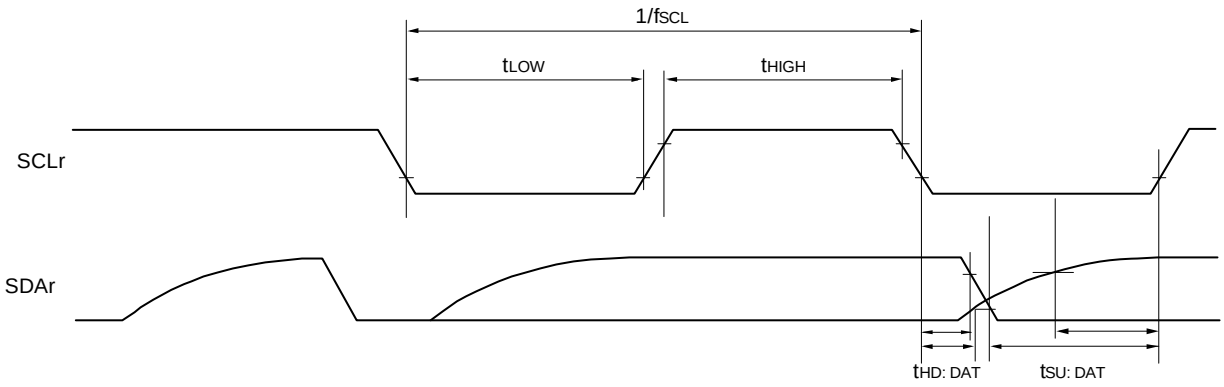
Caution Select the normal input buffer and the N-ch open drain output (V_{DD} tolerance) mode for the SDAr pin and the normal output mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register h (POMh).

(**Remarks** are listed on the next page.)

Simplified I²C mode connection diagram (during communication at same potential)



Simplified I²C mode serial transfer timing (during communication at same potential)



Remark 1. R_b [Ω]: Communication line (SDAr) pull-up resistance, C_b [F]: Communication line (SDAr, SCLr) load capacitance

Remark 2. r: IIC number (r = 00, 10, 20), g: PIM number (g = 0, 1, 3, 4, 5, 8)

Remark 3. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number (m = 0, 1), n: Channel number (n = 0, 2), mn = 00, 02, 10)

(5) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode)

(T_A = -40 to +85°C, 1.8 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V) (1/2)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	
Transfer rate		Reception	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V		f_{MCK}/6 Note 1		f_{MCK}/6 Note 1	bps
			Theoretical value of the maximum transfer rate f_{MCK} = f_{CLK} Note 4		4.0		1.3	Mbps
			2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V		f_{MCK}/6 Note 1		f_{MCK}/6 Note 1	bps
			Theoretical value of the maximum transfer rate f_{MCK} = f_{CLK} Note 4		4.0		1.3	Mbps
			1.8 V (2.4 V Note 5) ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V		f_{MCK}/6 Notes 1, 2, 3		f_{MCK}/6 Notes 1, 2, 3	bps
			Theoretical value of the maximum transfer rate f_{MCK} = f_{CLK} Note 4		4.0		1.3	Mbps

Note 1. Transfer rate in the SNOOZE mode is 4800 bps only.

Note 2. Use it with $V_{DD} \geq V_b$

Note 3. The following conditions are required for low voltage interface.
2.4 V ≤ V_{DD} < 2.7 V: MAX. 2.6 Mbps
1.8 V ≤ V_{DD} < 2.4 V: MAX. 1.3 Mbps

Note 4. The maximum operating frequencies of the CPU/peripheral hardware clock (f_{CLK}) are:
HS (high-speed main) Mode: 24 MHz (2.7 V ≤ V_{DD} ≤ 5.5 V)
16 MHz (2.4 V ≤ V_{DD} ≤ 5.5 V)
LS (low-speed main) Mode: 8 MHz (1.8 V ≤ V_{DD} ≤ 5.5 V)

Note 5. Condition in the HS (high-speed main) mode

Caution Select the TTL input buffer for the RxDq pin and the N-ch open drain output (V_{DD} tolerance) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

Remark 1. V_b [V]: Communication line voltage

Remark 2. q: UART number (q = 0 to 2), g: PIM or POM number (g = 0, 1, 3, 4, 5, 8)

Remark 3. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03, 10, 11))

(5) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode)

(T_A = -40 to +85°C, 1.8 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V) (2/2)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	
Transfer rate		Transmission	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V		Note 1		Note 1	bps
			Theoretical value of the maximum transfer rate C_b = 50 pF, R_b = 1.4 kΩ, V_b = 2.7 V		2.8 Note 2		2.8 Note 2	Mbps
			2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V		Note 3		Note 3	bps
			Theoretical value of the maximum transfer rate C_b = 50 pF, R_b = 2.7 kΩ, V_b = 2.3 V		1.2 Note 4		1.2 Note 4	Mbps
			1.8 V (2.4 V Note 8) ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V		Notes 5, 6		Notes 5, 6	bps
			Theoretical value of the maximum transfer rate C_b = 50 pF, R_b = 5.5 kΩ, V_b = 1.6 V		0.43 Note 7		0.43 Note 7	Mbps

Note 1. The smaller maximum transfer rate derived by using f_{MCK}/12 or the following expression is the valid maximum transfer rate.
Expression for calculating the transfer rate when 4.0 V ≤ V_{DD} ≤ 5.5 V and 2.7 V ≤ V_b ≤ 4.0 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.2}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.2}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [\%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

Note 2. This value as an example is calculated when the conditions described in the “Conditions” column are met.
Refer to **Note 1** above to calculate the maximum transfer rate under conditions of the customer.

Note 3. The smaller maximum transfer rate derived by using f_{MCK}/6 or the following expression is the valid maximum transfer rate.
Expression for calculating the transfer rate when 2.7 V ≤ V_{DD} < 4.0 V and 2.3 V ≤ V_b ≤ 2.7 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [\%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

Note 4. This value as an example is calculated when the conditions described in the “Conditions” column are met.
Refer to **Note 3** above to calculate the maximum transfer rate under conditions of the customer.

Note 5. Use it with V_{DD} ≥ V_b

Note 6. The smaller maximum transfer rate derived by using f_{MCK}/6 or the following expression is the valid maximum transfer rate.
Expression for calculating the transfer rate when 1.8 V ≤ V_{DD} < 3.3 V and 1.6 V ≤ V_b ≤ 2.0 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [\%]}$$

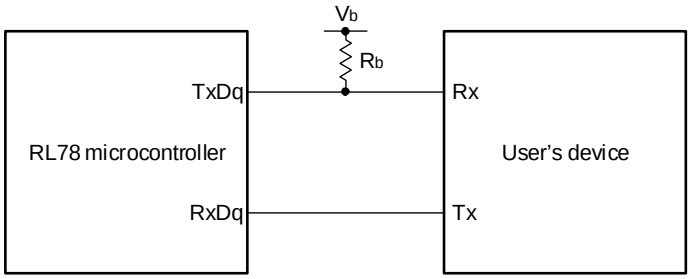
* This value is the theoretical value of the relative difference between the transmission and reception sides.

Note 7. This value as an example is calculated when the conditions described in the “Conditions” column are met.
Refer to **Note 6** above to calculate the maximum transfer rate under conditions of the customer.

Note 8. Condition in the HS (high-speed main) mode

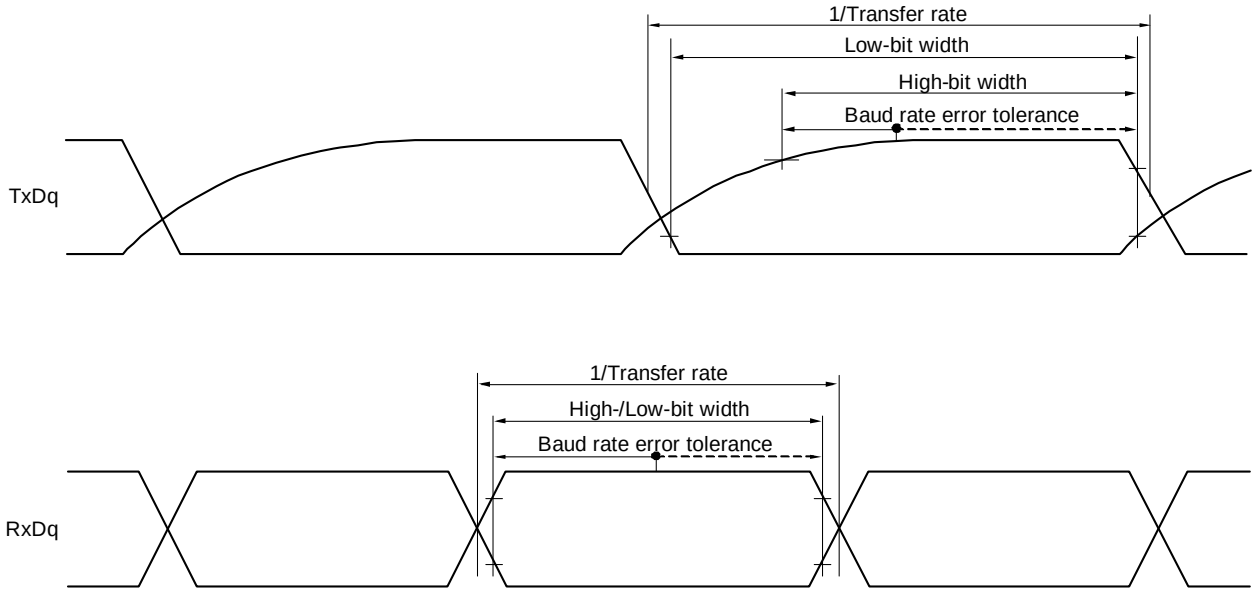
Caution Select the TTL input buffer for the RxDq pin and the N-ch open drain output (V_{DD} tolerance) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

UART mode connection diagram (during communication at different potential)



(**Remarks** are listed on the next page.)

UART mode bit width (during communication at different potential) (reference)



Remark 1. R_b [Ω]: Communication line (TxDq) pull-up resistance,
C_b [F]: Communication line (TxDq) load capacitance, V_b [V]: Communication line voltage

Remark 2. q: UART number (q = 0 to 2), g: PIM or POM number (g = 0, 1, 3, 4, 5, 8)

Remark 3. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).
m: Unit number, n: Channel number (mn = 00 to 03, 10, 11))

(6) Communication at different potential (1.8 V, 2.5 V, 3 V) (Simplified SPI(CSI) mode) (master mode, SCKp... internal clock output)

(T_A = -40 to +85°C, 1.8 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V) **(1/2)**

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	
SCKp cycle time	t_{KCY1}	t_{KCY1} ≥ 4/f_{CLK}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ	300		1150		ns
			2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	500 Note 1		1150		ns
			1.8 V (2.4 V Note 2) ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V, C_b = 30 pF, R_b = 5.5 kΩ	1150 Note 1		1150		ns
SCKp high-level width	t_{KH1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ		t_{KCY1}/2 - 75		t_{KCY1}/2 - 75		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ		t_{KCY1}/2 - 170		t_{KCY1}/2 - 170		ns
		1.8 V (2.4 V Note 2) ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V, C_b = 30 pF, R_b = 5.5 kΩ		t_{KCY1}/2 - 458		t_{KCY1}/2 - 458		ns
SCKp low-level width	t_{KL1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ		t_{KCY1}/2 - 12		t_{KCY1}/2 - 50		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ		t_{KCY1}/2 - 18		t_{KCY1}/2 - 50		ns
		1.8 V (2.4 V Note 2) ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V, C_b = 30 pF, R_b = 5.5 kΩ		t_{KCY1}/2 - 50		t_{KCY1}/2 - 50		ns

Note 1. Use it with V_{DD} ≥ V_b

Note 2. Condition in the HS (high-speed main) mode

Caution Select the TTL input buffer for the SIp pin and the N-ch open drain output (V_{DD} tolerance) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

(**Remarks** are listed two pages after the next page.)

(6) Communication at different potential (1.8 V, 2.5 V, 3 V) (Simplified SPI(CSI) mode) (master mode, SCKp... internal clock output)

(T_A = -40 to +85°C, 1.8 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V) (2/2)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	
SIp setup time (to SCKp↓) Note 1	t_{SIK1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ	81		479		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	177		479		ns
		1.8 V (2.4 V Note 4) ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 3, C_b = 30 pF, R_b = 5.5 kΩ	479		479		ns
SIp hold time (from SCKp↓) Note 1	t_{KSI1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ	19		19		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	19		19		ns
		1.8 V (2.4 V Note 4) ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 3, C_b = 30 pF, R_b = 5.5 kΩ	19		19		ns
Delay time from SCKp↑ to SOp output Note 1	t_{KSO1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ		100		100	ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ		195		195	ns
		1.8 V (2.4 V Note 4) ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 3, C_b = 30 pF, R_b = 5.5 kΩ		483		483	ns
SIp setup time (to SCKp↓) Note 2	t_{SIK1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ	44		110		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	44		110		ns
		1.8 V (2.4 V Note 4) ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 3, C_b = 30 pF, R_b = 5.5 kΩ	110		110		ns
SIp hold time (from SCKp↓) Note 2	t_{KSI1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ	19		19		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	19		19		ns
		1.8 V (2.4 V Note 4) ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 3, C_b = 30 pF, R_b = 5.5 kΩ	19		19		ns
Delay time from SCKp↑ to SOp output Note 2	t_{KSO1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ		25		25	ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ		25		25	ns
		1.8 V (2.4 V Note 4) ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 3, C_b = 30 pF, R_b = 5.5 kΩ		25		25	ns

Note 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.

Note 2. When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

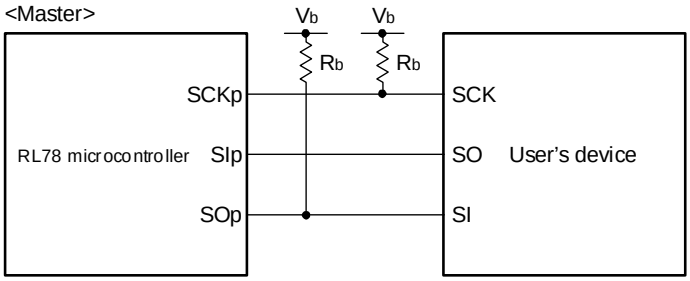
Note 3. Use it with V_{DD} ≥ V_b

Note 4. Condition in the HS (high-speed main) mode

(**Caution** and remarks are listed on the next page.)

Caution Select the TTL input buffer for the SIp pin and the N-ch open drain output (V_{DD} tolerance) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

Simplified SPI(CSI) mode connection diagram (during communication at different potential)

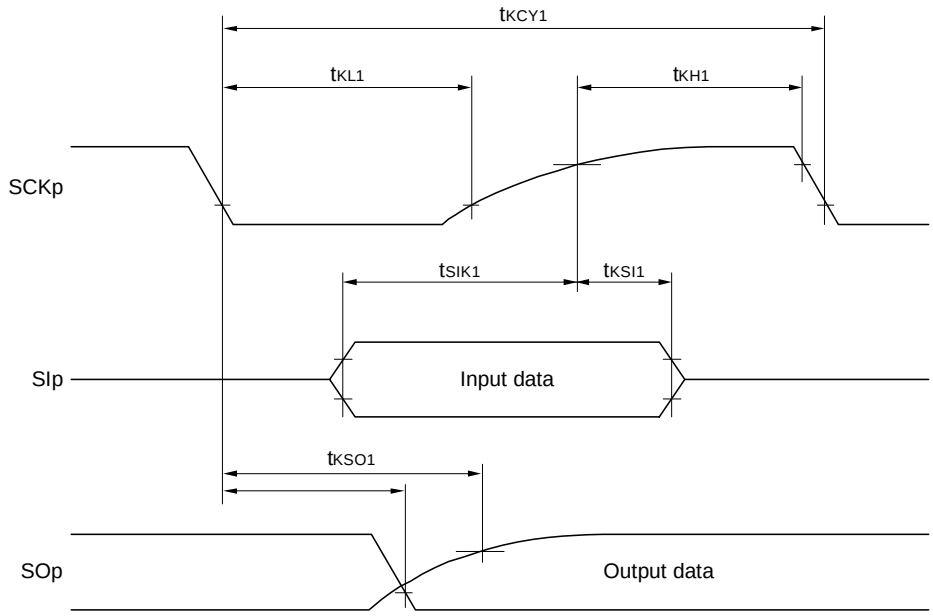


Remark 1. R_b [Ω]: Communication line (SCKp, SOp) pull-up resistance, C_b [F]: Communication line (SCKp, SOp) load capacitance, V_b [V]: Communication line voltage

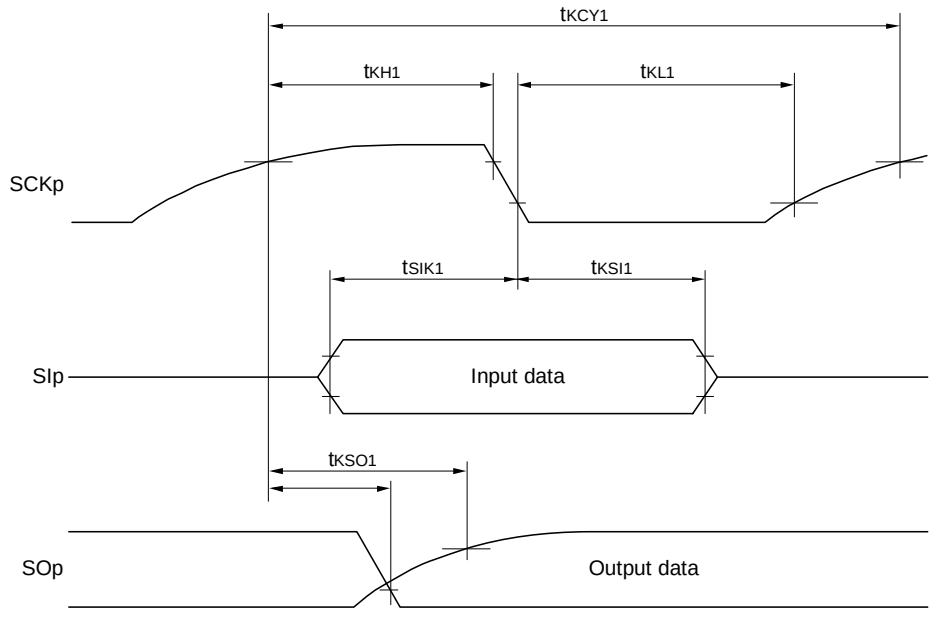
Remark 2. p: CSI number (p = 00, 10, 20), m: Unit number (m = 0, 1), n: Channel number (n = 0, 2), g: PIM or POM number (g = 0, 1, 3, 4, 5, 8)

Remark 3. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00, 02, 10))

Simplified SPI(CSI) mode serial transfer timing (master mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)



Simplified SPI(CSI) mode serial transfer timing (master mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)



Remark p: CSI number (p = 00, 10, 20), m: Unit number (m = 0, 1), n: Channel number (n = 0, 2),
g: PIM or POM number (g = 0, 1, 3, 4, 5, 8)

(7) Communication at different potential (1.8 V, 2.5 V, 3 V) (Simplified SPI(CSI) mode) (slave mode, SCKp... external clock input)

(T_A = -40 to +85°C, 1.8 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	
SCKp cycle time Note 1	t_{KCY2}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V	20 MHz < f_{MCK}	12/f_{MCK}		—		ns
			8 MHz < f_{MCK} ≤ 20 MHz	10/f_{MCK}		—		ns
			4 MHz < f_{MCK} ≤ 8 MHz	8/f_{MCK}		—		ns
			f_{MCK} ≤ 4 MHz	6/f_{MCK}		—		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V	20 MHz < f_{MCK}	16/f_{MCK}		—		ns
			16 MHz < f_{MCK} ≤ 20 MHz	14/f_{MCK}		—		ns
			8 MHz < f_{MCK} ≤ 16 MHz	12/f_{MCK}		—		ns
			4 MHz < f_{MCK} ≤ 8 MHz	8/f_{MCK}		16/f_{MCK}		ns
			f_{MCK} ≤ 4 MHz	6/f_{MCK}		10/f_{MCK}		ns
		1.8 V (2.4 V Note 6) ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 2	20 MHz < f_{MCK}	36/f_{MCK}		—		ns
			16 MHz < f_{MCK} ≤ 20 MHz	32/f_{MCK}		—		ns
			8 MHz < f_{MCK} ≤ 16 MHz	26/f_{MCK}		—		ns
			4 MHz < f_{MCK} ≤ 8 MHz	16/f_{MCK}		16/f_{MCK}		ns
			f_{MCK} ≤ 4 MHz	10/f_{MCK}		10/f_{MCK}		ns
SCKp high-/low-level width	t_{KH2}, t_{KL2}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V		t_{KCY2}/2 - 12		t_{KCY2}/2 - 50		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V		t_{KCY2}/2 - 18		t_{KCY2}/2 - 50		ns
		1.8 V (2.4 V Note 6) ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 2		t_{KCY2}/2 - 50		t_{KCY2}/2 - 50		ns
SIp setup time (to SCKp↑) Note 3	t_{SIK2}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V		1/f_{MCK} + 20		1/f_{MCK} + 30		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V		1/f_{MCK} + 20		1/f_{MCK} + 30		ns
		1.8 V (2.4 V Note 6) ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 2		1/f_{MCK} + 30		1/f_{MCK} + 30		ns
SIp hold time (from SCKp↑) Note 4	t_{KSI2}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V		1/f_{MCK} + 31		1/f_{MCK} + 31		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V		1/f_{MCK} + 31		1/f_{MCK} + 31		ns
		1.8 V (2.4 V Note 6) ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 2		1/f_{MCK} + 31		1/f_{MCK} + 31		ns
Delay time from SCKp↓ to SOp output Note 5	t_{KSO2}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ			2/f_{MCK} + 120		2/f_{MCK} + 573	ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ			2/f_{MCK} + 214		2/f_{MCK} + 573	ns
		1.8 V (2.4 V Note 6) ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 2, C_b = 30 pF, R_b = 5.5 kΩ			2/f_{MCK} + 573		2/f_{MCK} + 573	ns

(**Notes**, **Cautions**, and **Remarks** are listed on the next page.)

Note 1. Transfer rate in the SNOOZE mode: MAX. 1 Mbps

Note 2. Use it with $V_{DD} \geq V_b$.

Note 3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes “to SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

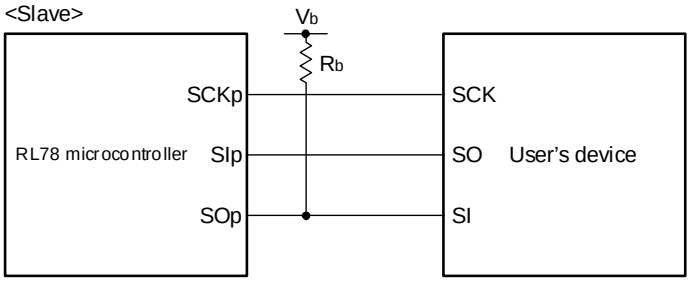
Note 4. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes “from SCKp↓” when DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 0.

Note 5. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes “from SCKp↑” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 6. Condition in the HS (high-speed main) mode

Caution Select the TTL input buffer for the SIp and SCKp pins, and the N-ch open drain output (V_{DD} tolerance) mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

Simplified SPI(CSI) mode connection diagram (during communication at different potential)

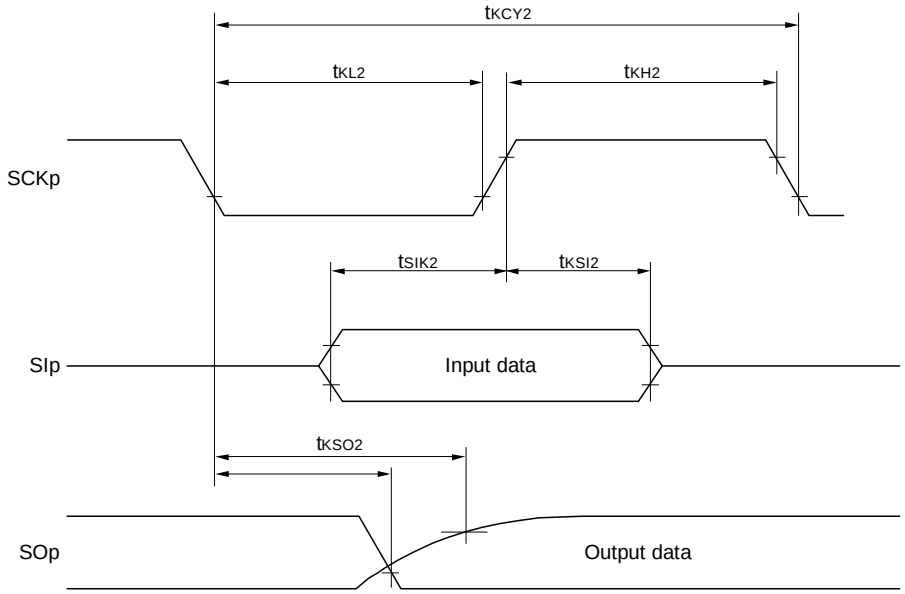


Remark 1. R_b [Ω]: Communication line (SOp) pull-up resistance, C_b [F]: Communication line (SOp) load capacitance, V_b [V]: Communication line voltage

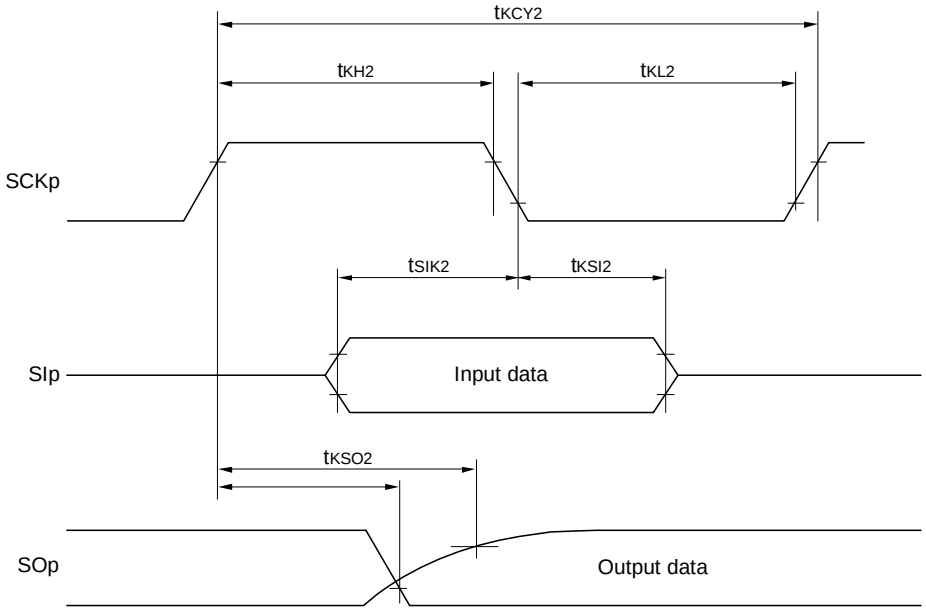
Remark 2. p: CSI number (p = 00, 10, 20), m: Unit number (m = 0, 1), n: Channel number (n = 0 , 2), g: PIM or POM number (g = 0, 1, 3, 4, 5, 8)

Remark 3. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).
m: Unit number, n: Channel number (mn = 00, 02, 10))

Simplified SPI(CSI) mode serial transfer timing (slave mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)



Simplified SPI(CSI) mode serial transfer timing (slave mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)



Remark p: CSI number (p = 00, 10, 20), m: Unit number (m = 0, 1), n: Channel number (n = 0, 2),
g: PIM or POM number (g = 0, 1, 3, 4, 5, 8)

(8) Communication at different potential (1.8 V, 2.5 V, 3 V) (simplified I^2C mode)

(T_A = -40 to +85°C, 1.8 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V) **(1/2)**

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	
SCLr clock frequency	f_{SCL}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 50 pF, R_b = 2.7 kΩ		1000 Note 1		300 Note 1	kHz
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 50 pF, R_b = 2.7 kΩ		1000 Note 1		300 Note 1	kHz
		4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 100 pF, R_b = 2.8 kΩ		400 Note 1		300 Note 1	kHz
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 100 pF, R_b = 2.7 kΩ		400 Note 1		300 Note 1	kHz
		1.8 V (2.4 V Note 4) ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 2, C_b = 100 pF, R_b = 5.5 kΩ		400 Note 1		300 Note 1	kHz
Hold time when SCLr = “L”	t_{LOW}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 50 pF, R_b = 2.7 kΩ	475		1550		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 50 pF, R_b = 2.7 kΩ	475		1550		ns
		4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 100 pF, R_b = 2.8 kΩ	1150		1550		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 100 pF, R_b = 2.7 kΩ	1150		1550		ns
		1.8 V (2.4 V Note 4) ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 2, C_b = 100 pF, R_b = 5.5 kΩ	1550		1550		ns
Hold time when SCLr = “H”	t_{HIGH}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 50 pF, R_b = 2.7 kΩ	245		610		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 50 pF, R_b = 2.7 kΩ	200		610		ns
		4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 100 pF, R_b = 2.8 kΩ	675		610		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 100 pF, R_b = 2.7 kΩ	600		610		ns
		1.8 V (2.4 V Note 4) ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 2, C_b = 100 pF, R_b = 5.5 kΩ	610		610		ns

(8) Communication at different potential (1.8 V, 2.5 V, 3 V) (simplified I^2C mode)

(T_A = -40 to +85°C, 1.8 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V) (2/2)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	
Data setup time (reception)	$t_{SU:DAT}$	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 50 pF, R_b = 2.7 kΩ	1/f_{MCK} + 135 Note 3		1/f_{MCK} + 190 Note 2		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 50 pF, R_b = 2.7 kΩ	1/f_{MCK} + 135 Note 3		1/f_{MCK} + 190 Note 2		ns
		4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 100 pF, R_b = 2.8 kΩ	1/f_{MCK} + 190 Note 3		1/f_{MCK} + 190 Note 3		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 100 pF, R_b = 2.7 kΩ	1/f_{MCK} + 190 Note 3		1/f_{MCK} + 190 Note 3		ns
		1.8 V (2.4 V Note 4) ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 2, C_b = 100 pF, R_b = 5.5 kΩ	1/f_{MCK} + 190 Note 3		1/f_{MCK} + 190 Note 3		ns
Data hold time (transmission)	$t_{HD:DAT}$	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 50 pF, R_b = 2.7 kΩ	0	305	0	305	ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 50 pF, R_b = 2.7 kΩ	0	305	0	305	ns
		4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 100 pF, R_b = 2.8 kΩ	0	355	0	355	ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 100 pF, R_b = 2.7 kΩ	0	355	0	355	ns
		1.8 V (2.4 V Note 4) ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 2, C_b = 100 pF, R_b = 5.5 kΩ	0	405	0	405	ns

Note 1. The value must be equal to or less than f_{MCK}/4.

Note 2. Use it with V_{DD} ≥ V_b

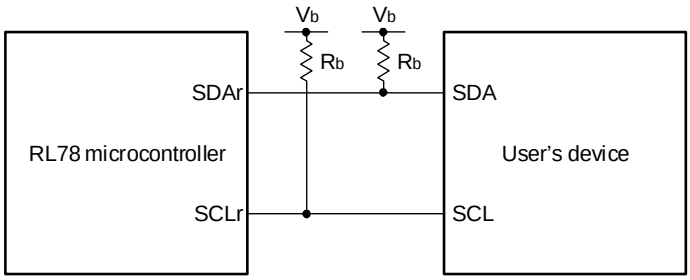
Note 3. Set the f_{MCK} value to keep the hold time of SCLr = “L” and SCLr = “H”.

Note 4. Condition in the HS (high-speed main) mode

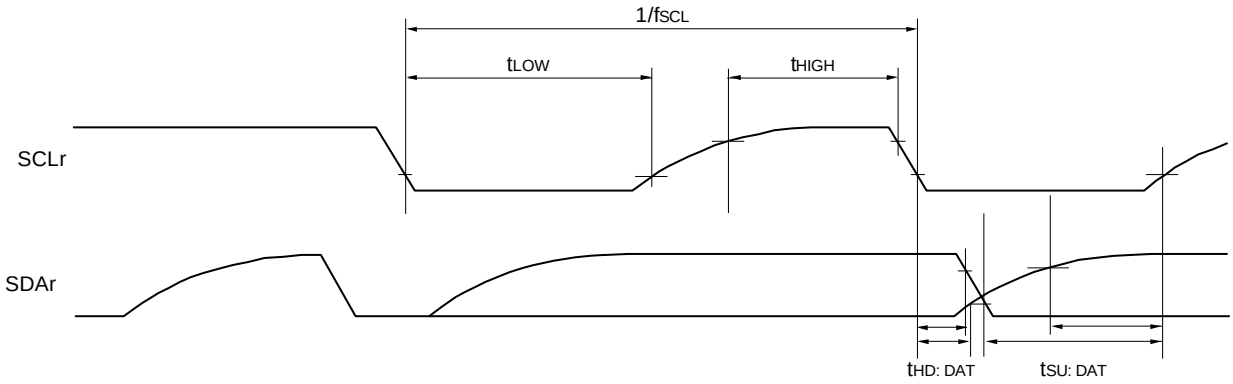
Caution Select the TTL input buffer and the N-ch open drain output (V_{DD} tolerance) mode for the SDAr pin and the N-ch open drain output (V_{DD} tolerance) mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

(**Remarks** are listed on the next page.)

Simplified I²C mode connection diagram (during communication at different potential)



Simplified I²C mode serial transfer timing (during communication at different potential)



Remark 1. Rb [Ω]: Communication line (SDAr, SCLr) pull-up resistance, Cb [F]: Communication line (SDAr, SCLr) load capacitance, Vb [V]: Communication line voltage

Remark 2. r: IIC number (r = 00, 10, 20), g: PIM, POM number (g = 0, 1, 3, 4, 5, 8)

Remark 3. fMCK: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number (m = 0), n: Channel number (n = 0, 2), mn = 00, 02, 10)

39.5.2 Serial Interface UARTMG

(TA = -40 to +85°C, 1.8 V ≤ AVDD = VDD ≤ 5.5 V, AVSS = VSS = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate		fSUB = 38.4 kHz	200		9600	bps
		fSUB = 38.4 kHz (when the clock doubler is in use)	200		19200	bps

39.5.3 Serial interface IICA

(1) I^2C standard mode

(T_A = -40 to +85°C, 1.8 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	
SCLA0 clock frequency	f_{SCL}	Standard mode: f_{CLK} ≥ 1 MHz	2.7 V ≤ V_{DD} ≤ 5.5 V	0	100	0	100	kHz
			1.8 V (2.4 V Note 3) ≤ V_{DD} ≤ 5.5 V	0	100	0	100	kHz
Setup time of restart condition	$t_{SU:STA}$	2.7 V ≤ V_{DD} ≤ 5.5 V		4.7		4.7		µs
		1.8 V (2.4 V Note 3) ≤ V_{DD} ≤ 5.5 V		4.7		4.7		µs
Hold time Note 1	$t_{HD:STA}$	2.7 V ≤ V_{DD} ≤ 5.5 V		4.0		4.0		µs
		1.8 V (2.4 V Note 3) ≤ V_{DD} ≤ 5.5 V		4.0		4.0		µs
Hold time when SCLA0 = “L”	t_{LOW}	2.7 V ≤ V_{DD} ≤ 5.5 V		4.7		4.7		µs
		1.8 V (2.4 V Note 3) ≤ V_{DD} ≤ 5.5 V		4.7		4.7		µs
Hold time when SCLA0 = “H”	t_{HIGH}	2.7 V ≤ V_{DD} ≤ 5.5 V		4.0		4.0		µs
		1.8 V (2.4 V Note 3) ≤ V_{DD} ≤ 5.5 V		4.0		4.0		µs
Data setup time (reception)	$t_{SU:DAT}$	2.7 V ≤ V_{DD} ≤ 5.5 V		250		250		ns
		1.8 V (2.4 V Note 3) ≤ V_{DD} ≤ 5.5 V		250		250		ns
Data hold time (transmission) Note 2	$t_{HD:DAT}$	2.7 V ≤ V_{DD} ≤ 5.5 V		0	3.45	0	3.45	µs
		1.8 V (2.4 V Note 3) ≤ V_{DD} ≤ 5.5 V		0		0	3.45	µs
Setup time of stop condition	$t_{SU:STO}$	2.7 V ≤ V_{DD} ≤ 5.5 V		4.0		4.0		µs
		1.8 V (2.4 V Note 3) ≤ V_{DD} ≤ 5.5 V		4.0		4.0		µs
Bus-free time	t_{BUF}	2.7 V ≤ V_{DD} ≤ 5.5 V		4.7		4.7		µs
		1.8 V (2.4 V Note 3) ≤ V_{DD} ≤ 5.5 V		4.7		4.7		µs

Note 1. The first clock pulse is generated after this period when the start/restart condition is detected.

Note 2. The maximum value (MAX.) of $t_{HD:DAT}$ is during normal transfer and a clock stretch state is inserted in the ACK (acknowledge) timing.

Note 3. Condition in the HS (high-speed main) mode

Remark The maximum value of C_b (communication line capacitance) and the value of R_b (communication line pull-up resistor) at that time in each mode are as follows.
Standard mode: C_b = 400 pF, R_b = 2.7 kΩ

(2) I^2C fast mode

(T_A = -40 to +85°C, 1.8 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	
SCLA0 clock frequency	f_{SCL}	Fast mode: f_{CLK} ≥ 3.5 MHz	2.7 V ≤ V_{DD} ≤ 5.5 V	0	400	0	400	kHz
			1.8 V (2.4 V Note 3) ≤ V_{DD} ≤ 5.5 V	0	400	0	400	kHz
Setup time of restart condition	$t_{SU: STA}$	2.7 V ≤ V_{DD} ≤ 5.5 V		0.6		0.6		µs
		1.8 V (2.4 V Note 3) ≤ V_{DD} ≤ 5.5 V		0.6		0.6		µs
Hold time Note 1	$t_{HD: STA}$	2.7 V ≤ V_{DD} ≤ 5.5 V		0.6		0.6		µs
		1.8 V (2.4 V Note 3) ≤ V_{DD} ≤ 5.5 V		0.6		0.6		µs
Hold time when SCLA0 = “L”	t_{LOW}	2.7 V ≤ V_{DD} ≤ 5.5 V		1.3		1.3		µs
		1.8 V (2.4 V Note 3) ≤ V_{DD} ≤ 5.5 V		1.3		1.3		µs
Hold time when SCLA0 = “H”	t_{HIGH}	2.7 V ≤ V_{DD} ≤ 5.5 V		0.6		0.6		µs
		1.8 V (2.4 V Note 3) ≤ V_{DD} ≤ 5.5 V		0.6		0.6		µs
Data setup time (reception)	$t_{SU: DAT}$	2.7 V ≤ V_{DD} ≤ 5.5 V		100		100		ns
		1.8 V (2.4 V Note 3) ≤ V_{DD} ≤ 5.5 V		100		100		ns
Data hold time (transmission) Note 2	$t_{HD: DAT}$	2.7 V ≤ V_{DD} ≤ 5.5 V		0	0.9	0	0.9	µs
		1.8 V (2.4 V Note 3) ≤ V_{DD} ≤ 5.5 V		0		0	0.9	µs
Setup time of stop condition	$t_{SU: STO}$	2.7 V ≤ V_{DD} ≤ 5.5 V		0.6		0.6		µs
		1.8 V (2.4 V Note 3) ≤ V_{DD} ≤ 5.5 V		0.6		0.6		µs
Bus-free time	t_{BUF}	2.7 V ≤ V_{DD} ≤ 5.5 V		1.3		1.3		µs
		1.8 V (2.4 V Note 3) ≤ V_{DD} ≤ 5.5 V		1.3		1.3		µs

Note 1. The first clock pulse is generated after this period when the start/restart condition is detected.

Note 2. The maximum value (MAX.) of $t_{HD: DAT}$ is during normal transfer and a clock stretch state is inserted in the ACK (acknowledge) timing.

Note 3. Condition in the HS (high-speed main) mode

Remark The maximum value of C_b (communication line capacitance) and the value of R_b (communication line pull-up resistor) at that time in each mode are as follows.
Fast mode: C_b = 320 pF, R_b = 1.1 kΩ

(3) I^2C fast mode plus

(T_A = -40 to +85°C, 1.8 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V)

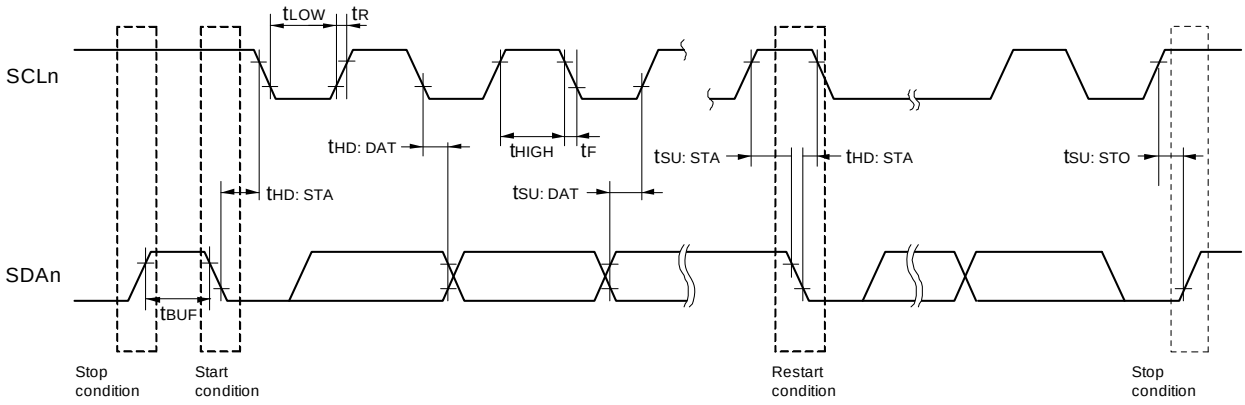
Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	
SCLA0 clock frequency	f_{SCL}	Fast mode plus: f_{CLK} ≥ 10 MHz	2.7 V ≤ V_{DD} ≤ 5.5 V	0	1000	—		kHz
Setup time of restart condition	$t_{SU: STA}$	2.7 V ≤ V_{DD} ≤ 5.5 V		0.26		—		µs
Hold time Note 1	$t_{HD: STA}$	2.7 V ≤ V_{DD} ≤ 5.5 V		0.26		—		µs
Hold time when SCLA0 = “L”	t_{LOW}	2.7 V ≤ V_{DD} ≤ 5.5 V		0.5		—		µs
Hold time when SCLA0 = “H”	t_{HIGH}	2.7 V ≤ V_{DD} ≤ 5.5 V		0.26		—		µs
Data setup time (reception)	$t_{SU: DAT}$	2.7 V ≤ V_{DD} ≤ 5.5 V		50		—		ns
Data hold time (transmission) Note 2	$t_{HD: DAT}$	2.7 V ≤ V_{DD} ≤ 5.5 V		0	0.45	—		µs
Setup time of stop condition	$t_{SU: STO}$	2.7 V ≤ V_{DD} ≤ 5.5 V		0.26		—		µs
Bus-free time	t_{BUF}	2.7 V ≤ V_{DD} ≤ 5.5 V		0.5		—		µs

Note 1. The first clock pulse is generated after this period when the start/restart condition is detected.

Note 2. The maximum value (MAX.) of $t_{HD: DAT}$ is during normal transfer and a clock stretch state is inserted in the ACK (acknowledge) timing.

Remark The maximum value of C_b (communication line capacitance) and the value of R_b (communication line pull-up resistor) at that time in each mode are as follows.
Fast mode plus: C_b = 120 pF, R_b = 1.1 kΩ

IICA serial transfer timing



39.6 Analog Characteristics

39.6.1 A/D converter Characteristics

(1) When reference voltage (+) = V_{DD} (ADREFP1 = 0, ADREFP0 = 0), reference voltage (-) = V_{SS} (ADREFM = 0), target pin: ANI8 to ANI10, internal reference voltage, and temperature sensor output voltage

(T_A = -40 to +85°C, 1.8 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V, reference voltage (+) = V_{DD}, reference voltage (–) = V_{SS})

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8		10	bit
Overall error Note 1	AINL	10-bit resolution	1.8 V ≤ V_{DD} ≤ 5.5 V		1.2	±7.0	LSB
Conversion time	t_{CONV}	10-bit resolution Target pin: ANI8 to ANI10	3.6 V ≤ V_{DD} ≤ 5.5 V	2.125		39	μs
			2.7 V ≤ V_{DD} ≤ 5.5 V	3.1875		39	μs
			1.8 V ≤ V_{DD} ≤ 5.5 V	17		39	μs
		10-bit resolution Target pin: internal reference voltage and temperature sensor output voltage (HS (high-speed main) mode)	3.6 V ≤ V_{DD} ≤ 5.5 V	2.375		39	μs
			2.7 V ≤ V_{DD} ≤ 5.5 V	3.5626		39	μs
			1.8 V ≤ V_{DD} ≤ 5.5 V	17		39	μs
Zero-scale error Notes 1, 2	E_{ZS}	10-bit resolution	1.8 V ≤ V_{DD} ≤ 5.5 V			±0.60	%FSR
Full-scale error Notes 1, 2	E_{FS}	10-bit resolution	1.8 V ≤ V_{DD} ≤ 5.5 V			±0.60	%FSR
Integral linearity error Note 1	ILE	10-bit resolution	1.8 V ≤ V_{DD} ≤ 5.5 V			±4.0	LSB
Differential linearity error Note 1	DLE	10-bit resolution	1.8 V ≤ V_{DD} ≤ 5.5 V			±2.0	LSB
Analog input voltage	V_{AIN}	ANI8 to ANI10		0		V_{DD}	V
		Internal reference voltage (2.4 V ≤ V_{DD} ≤ 5.5 V, HS (high-speed main) mode)		V_{BGR} Note 3			V
		Temperature sensor output voltage (2.4 V ≤ V_{DD} ≤ 5.5 V, HS (high-speed main) mode)		V_{TMPS25} Note 3			V

Note 1. Excludes quantization error (±1/2 LSB).

Note 2. This value is indicated as a ratio (%FSR) to the full-scale value.

Note 3. Refer to **39.6.2 Temperature sensor/internal reference voltage output characteristics**.

(2) When reference voltage (+) = Internal reference voltage (ADREFP1 = 1, ADREFP0 = 0), reference voltage (-) = V_{SS} (ADREFM = 0), target pin: ANI8 to ANI10

(T_A = -40 to +85°C, 2.4 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V, reference voltage (+) = V_{BGR} Note 3, reference voltage (–) = V_{SS} = 0 V, HS (high-speed main) mode)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8			bit
Conversion time	t_{CONV}	8-bit resolution	2.4 V ≤ V_{DD} ≤ 5.5 V	17		39	µs
Zero-scale error Notes 1, 2,	E_{ZS}	8-bit resolution	2.4 V ≤ V_{DD} ≤ 5.5 V			±(0.60+0.35)	%FSR
Integral linearity error Note 1	ILE	8-bit resolution	2.4 V ≤ V_{DD} ≤ 5.5 V			±(2.0+0.5)	LSB
Differential linearity error Note 1	DLE	8-bit resolution	2.4 V ≤ V_{DD} ≤ 5.5 V			±(1.0+0.2)	LSB
Analog input voltage	V_{AIN}			0		V_{BGR} Note 3	V

Note 1. Excludes quantization error (±1/2 LSB).

Note 2. This value is indicated as a ratio (%FSR) to the full-scale value.

Note 3. Refer to **39.6.2 Temperature sensor/internal reference voltage output characteristics**.

39.6.2 Temperature sensor/internal reference voltage output characteristics

(T_A = -40 to +85°C, 2.4 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V, HS (high-speed main) Mode)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Temperature sensor output voltage	V_{TEMP}	T_A = +25°C		1.05		V
Internal reference voltage	V_{BGR}		1.38	1.45	1.5	V
Temperature coefficient	F_{VTMPS}	Temperature sensor output voltage that depends on the temperature		-3.6		mV/°C
Operation stabilization wait time	t_{AMP}	2.4 V ≤ V_{DD} ≤ 5.5 V	5			µs

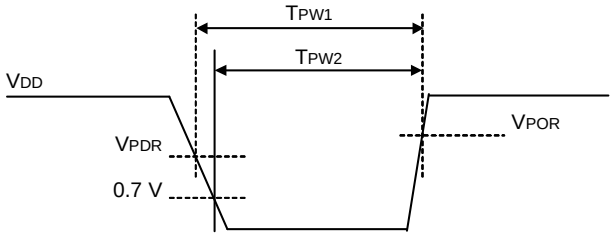
39.6.3 POR circuit characteristics

(T_A = -40 to +85°C, Vss = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	V_{POR}	Power supply rise time	1.47	1.51	1.55	V
	V_{PDR}	Power supply fall time Note 1	1.46	1.50	1.54	V
Minimum pulse width Note 2	T_{PW1}	Other than STOP/SUB HALT/SUB RUN	300			µs
	T_{PW2}	STOP/SUB HALT/SUB RUN	300			µs

Note 1. If the power supply voltage falls while the voltage detector is off, be sure to either shift to STOP mode or execute a reset by using the voltage detector or external reset pin before the power supply voltage falls below the minimum operating voltage specified in **39.4 AC Characteristics**.

Note 2. Minimum time required for a POR reset when V_{DD} falls below V_{PDR}. This is also the minimum time required for a POR reset from when V_{DD} exceeds below 0.7 V to when V_{DD} exceeds V_{POR} while STOP mode is entered or the main system clock is stopped through setting bit 0 (HIOSTOP) and bit 7 (MSTOP) in the clock operation status control register (CSC).



39.6.4 LVD circuit characteristics

(1) LVD detection voltage in reset mode and interrupt mode

(T_A = -40 to +85°C, $V_{PDR} \le AV_{DD} = V_{DD} \le 5.5$ V, $AV_{SS} = V_{SS}$ = 0 V)

Parameter		Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	Supply voltage level	V_{LVD0}	Rising edge	3.98	4.06	4.14	V
			Falling edge	3.90	3.98	4.06	V
		V_{LVD1}	Rising edge	3.68	3.75	3.82	V
			Falling edge	3.60	3.67	3.74	V
		V_{LVD2}	Rising edge	3.07	3.13	3.19	V
			Falling edge	3.00	3.06	3.12	V
		V_{LVD3}	Rising edge	2.96	3.02	3.08	V
			Falling edge	2.90	2.96	3.02	V
		V_{LVD4}	Rising edge	2.86	2.92	2.97	V
			Falling edge	2.80	2.86	2.91	V
		V_{LVD5}	Rising edge	2.76	2.81	2.87	V
			Falling edge	2.70	2.75	2.81	V
		V_{LVD6}	Rising edge	2.66	2.71	2.76	V
			Falling edge	2.60	2.65	2.70	V
		V_{LVD7}	Rising edge	2.56	2.61	2.66	V
			Falling edge	2.50	2.55	2.60	V
		V_{LVD8}	Rising edge	2.45	2.50	2.55	V
			Falling edge	2.40	2.45	2.50	V
		V_{LVD9}	Rising edge	2.05	2.09	2.13	V
			Falling edge	2.00	2.04	2.08	V
		V_{LVD10}	Rising edge	1.94	1.98	2.02	V
			Falling edge	1.90	1.94	1.98	V
		V_{LVD11}	Rising edge	1.84	1.88	1.91	V
			Falling edge	1.80	1.84	1.87	V
Minimum pulse width		t_{LW}		300			µs
Detection delay time						300	µs

Caution Set the detection voltage (V_{LVD}) to be within the operating voltage range. The operating voltage range depends on the setting of the user option byte (000C2H/010C2H). The following shows the operating voltage range.

HS (high-speed main) mode: V_{DD} = 2.7 to 5.5 V @ 1 MHz to 24 MHz

V_{DD} = 2.4 to 5.5 V @ 1 MHz to 16 MHz

LS (low-speed main) mode: V_{DD} = 1.8 to 5.5 V @ 1 MHz to 8 MHz

(2) LVD Detection Voltage of Interrupt & Reset Mode

(T_A = -40 to +85°C, $V_{PDR} \leq AV_{DD} = V_{DD} \leq 5.5$ V, $AV_{SS} = V_{SS}$ = 0 V)

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Interrupt and reset mode	V_{LVDB0}	V_{POC2}, V_{POC1}, V_{POC0} = 0, 0, 1, falling reset voltage: 1.8 V			1.80	1.84	1.87	V
	V_{LVDB1}	LVIS1, LVIS0 = 1, 0		Rising release reset voltage	1.94	1.98	2.02	V
				Falling interrupt voltage	1.90	1.94	1.98	V
	V_{LVDB2}	LVIS1, LVIS0 = 0, 1		Rising release reset voltage	2.05	2.09	2.13	V
				Falling interrupt voltage	2.00	2.04	2.08	V
	V_{LVDB3}	LVIS1, LVIS0 = 0, 0		Rising release reset voltage	3.07	3.13	3.19	V
				Falling interrupt voltage	3.00	3.06	3.12	V
	V_{LVDC0}	V_{POC2}, V_{POC1}, V_{POC0} = 0, 1, 0, falling reset voltage: 2.4 V			2.40	2.45	2.50	V
	V_{LVDC1}	LVIS1, LVIS0 = 1, 0		Rising release reset voltage	2.56	2.61	2.66	V
				Falling interrupt voltage	2.50	2.55	2.60	V
	V_{LVDC2}	LVIS1, LVIS0 = 0, 1		Rising release reset voltage	2.66	2.71	2.76	V
				Falling interrupt voltage	2.60	2.65	2.70	V
	V_{LVDC3}	LVIS1, LVIS0 = 0, 0		Rising release reset voltage	3.68	3.75	3.82	V
				Falling interrupt voltage	3.60	3.67	3.74	V
	V_{LVDD0}	V_{POC2}, V_{POC1}, V_{POC0} = 0, 1, 1, falling reset voltage: 2.7 V			2.70	2.75	2.81	V
	V_{LVDD1}	LVIS1, LVIS0 = 1, 0		Rising release reset voltage	2.86	2.92	2.97	V
				Falling interrupt voltage	2.80	2.86	2.91	V
	V_{LVDD2}	LVIS1, LVIS0 = 0, 1		Rising release reset voltage	2.96	3.02	3.08	V
				Falling interrupt voltage	2.90	2.96	3.02	V
	V_{LVDC3}	LVIS1, LVIS0 = 0, 0		Rising release reset voltage	3.98	4.06	4.14	V
				Falling interrupt voltage	3.90	3.98	4.06	V

39.7 Power supply voltage rising slope characteristics

(T_A = -40 to +85°C, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Power supply voltage rising slope	SV_{DD}				54	V/ms

Caution Make sure to keep the internal reset state by the LVD circuit or an external reset until V_{DD} reaches the operating voltage range shown in 39.4 AC Characteristics.

39.8 LCD Characteristics

39.8.1 Resistance division method

(1) Static display mode

(T_A = -40 to +85°C, V_{L4} (MIN.) ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
LCD drive voltage	V_{L4}		2.0		V_{DD}	V

(2) 1/2 bias method, 1/4 bias method

(T_A = -40 to +85°C, V_{L4} (MIN.) ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
LCD drive voltage	V_{L4}		2.7		V_{DD}	V

(3) 1/3 bias method

(T_A = -40 to +85°C, V_{L4} (MIN.) ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
LCD drive voltage	V_{L4}		2.5		V_{DD}	V

39.8.2 Internal voltage boosting method

(1) 1/3 bias method

(T_A = -40 to +85°C, 1.8 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
LCD output voltage variation range	V_{L1}	C1 to C4 Note 1 = 0.47 µF Note 2	VLCD = 04H	0.90	1.00	1.08	V
			VLCD = 05H	0.95	1.05	1.13	V
			VLCD = 06H	1.00	1.10	1.18	V
			VLCD = 07H	1.05	1.15	1.23	V
			VLCD = 08H	1.10	1.20	1.28	V
			VLCD = 09H	1.15	1.25	1.33	V
			VLCD = 0AH	1.20	1.30	1.38	V
			VLCD = 0BH	1.25	1.35	1.43	V
			VLCD = 0CH	1.30	1.40	1.48	V
			VLCD = 0DH	1.35	1.45	1.53	V
			VLCD = 0EH	1.40	1.50	1.58	V
			VLCD = 0FH	1.45	1.55	1.63	V
			VLCD = 10H	1.50	1.60	1.68	V
			VLCD = 11H	1.55	1.65	1.73	V
			VLCD = 12H	1.60	1.70	1.78	V
			VLCD = 13H	1.65	1.75	1.83	V
Doubler output voltage	V_{L2}	C1 to C4 Note 1 = 0.47 µF		2 V_{L1} - 0.1	2 V_{L1}	2 V_{L1}	V
Tripler output voltage	V_{L4}	C1 to C4 Note 1 = 0.47 µF		3 V_{L1}- 0.15	3 V_{L1}	3 V_{L1}	V
Reference voltage setup time Note 2	t_{VWAIT1}			5			ms
Voltage boost wait time Note 3	t_{VWAIT2}	C1 to C4 Note 1 = 0.47µF		500			ms

Note 1. This is a capacitor that is connected between voltage pins used to drive the LCD.
C1: A capacitor connected between CAPH and CAPL
C2: A capacitor connected between V_{L1} and GND
C3: A capacitor connected between V_{L2} and GND
C4: A capacitor connected between V_{L4} and GND
C1 = C2 = C3 = C4 = 0.47 µF±30%

Note 2. This is the time required to wait from when the reference voltage is specified by using the VLCD register (or when the internal voltage boosting method is selected (by setting the MDSET1 and MDSET0 bits of the LCDM0 register to 01B) if the default value reference voltage is used) until voltage boosting starts (VLCON = 1).

Note 3. This is the wait time from when voltage boosting is started (VLCON = 1) until display is enabled (LCDON = 1).

(2) 1/4 bias method

(T_A = -40 to +85°C, 1.8 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
LCD output voltage variation range	V_{L1}	C1 to C5 Note 1 = 0.47 µF Note 2	VLCD = 04H	0.90	1.00	1.08	V
			VLCD = 05H	0.95	1.05	1.13	V
			VLCD = 06H	1.00	1.10	1.18	V
			VLCD = 07H	1.05	1.15	1.23	V
			VLCD = 08H	1.10	1.20	1.28	V
			VLCD = 09H	1.15	1.25	1.33	V
			VLCD = 0AH	1.20	1.30	1.38	V
Doubler output voltage	V_{L2}	C1 to C5 Note 1 = 0.47 µF		2 V_{L1} - 0.08	2 V_{L1}	2 V_{L1}	V
Tripler output voltage	V_{L3}	C1 to C5 Note 1 = 0.47 µF		3 V_{L1} - 0.12	3 V_{L1}	3 V_{L1}	V
Quadruply output voltage	V_{L4}	C1 to C5 Note 1 = 0.47 µF		4 V_{L1} - 0.16	4 V_{L1}	4 V_{L1}	V
Reference voltage setup time Note 2	t_{VWAIT1}			5			ms
Voltage boost wait time Note 3	t_{VWAIT2}	C1 to C5 Note 1 = 0.47µF		500			ms

Note 1. This is a capacitor that is connected between voltage pins used to drive the LCD.
C1: A capacitor connected between CAPH and CAPL
C2: A capacitor connected between V_{L1} and GND
C3: A capacitor connected between V_{L2} and GND
C4: A capacitor connected between V_{L3} and GND
C5: A capacitor connected between V_{L4} and GND
C1 = C2 = C3 = C4 = C5 = 0.47 µF±30%

Note 2. This is the time required to wait from when the reference voltage is specified by using the VLCD register (or when the internal voltage boosting method is selected (by setting the MDSET1 and MDSET0 bits of the LCDM0 register to 01B) if the default value reference voltage is used) until voltage boosting starts (VLCON = 1).

Note 3. This is the wait time from when voltage boosting is started (VLCON = 1) until display is enabled (LCDON = 1).

39.8.3 Capacitor split method

(1) 1/3 bias method

(T_A = -40 to +85°C, 2.2 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
V_{L4} voltage	V_{L4}	C1 to C4 = 0.47 µF Note 2		V_{DD}		V
V_{L2} voltage	V_{L2}	C1 to C4 = 0.47 µF Note 2	2/3 V_{L4} - 0.1	2/3 V_{L4}	2/3 V_{L4} + 0.1	V
V_{L1} voltage	V_{L1}	C1 to C4 = 0.47 µF Note 2	1/3 V_{L4} - 0.1	1/3 V_{L4}	1/3 V_{L4} + 0.1	V
Capacitor split wait time Note 1	t_{VWAIT}		100			ms

Note 1. This is the wait time from when voltage bucking is started (VLCON = 1) until display is enabled (LCDON = 1).

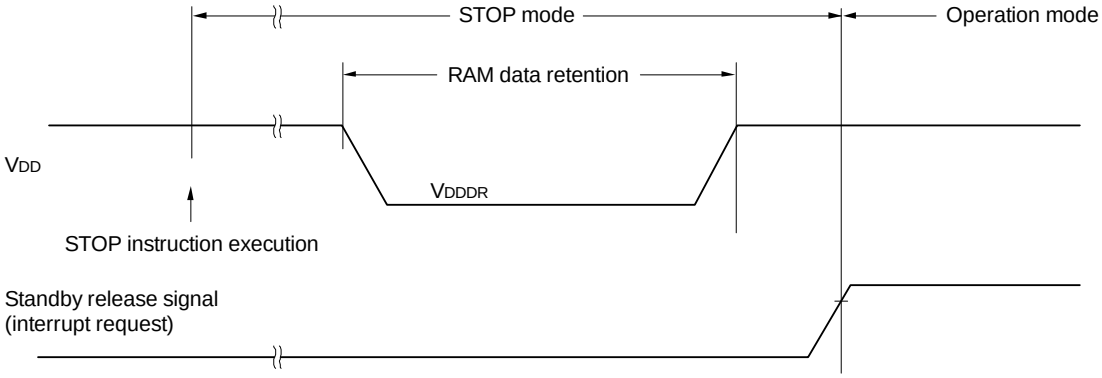
Note 2. This is a capacitor that is connected between voltage pins used to drive the LCD.
C1: A capacitor connected between CAPH and CAPL
C2: A capacitor connected between V_{L1} and GND
C3: A capacitor connected between V_{L2} and GND
C4: A capacitor connected between V_{L4} and GND
C1 = C2 = C3 = C4 = 0.47 µF±30%

39.9 RAM Data Retention Characteristics

(TA = -40 to +85°C, VSS = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	VDDDR		1.46 Note		5.5	V

Note The value depends on the POR detection voltage. When the voltage drops, the RAM data is retained before a POR reset is effected, but RAM data is not retained when a POR reset is effected.



39.10 Flash Memory Programming Characteristics

(TA = -40 to +85°C, 1.8 V ≤ AVDD = VDD ≤ 5.5 V, AVSS = VSS = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
System clock frequency	fCLK	1.8 V ≤ VDD ≤ 5.5 V		1		24	MHz
Number of code flash rewrites Notes 1, 2, 3	Cerwr	Retained for 20 years	TA = 85°C	1,000			Times
Number of data flash rewrites Notes 1, 2, 3		Retained for 1 year	TA = 25°C		1,000,000		
		Retained for 5 years	TA = 85°C	100,000			
		Retained for 20 years	TA = 85°C	10,000			

Note 1. 1 erase + 1 write after the erase is regarded as 1 rewrite. The retaining years are until next rewrite after the rewrite.

Note 2. When using flash memory programmer and Renesas Electronics self-programming library

Note 3. These are the characteristics of the flash memory and the results obtained from reliability testing by Renesas Electronics Corporation.

39.11 Dedicated Flash Memory Programmer Communication (UART)

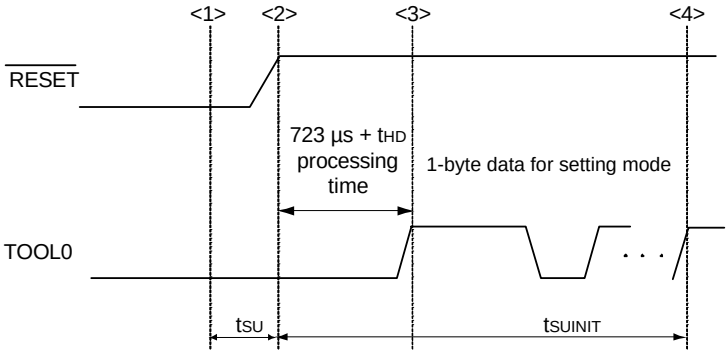
(TA = -40 to +85°C, 1.8 V ≤ AVDD = VDD ≤ 5.5 V, AVSS = VSS = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate		During serial programming	115,200		1,000,000	bps

39.12 Timing of Entry to Flash Memory Programming Modes

(T_A = -40 to +85°C, 1.8 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
How long from when an external reset ends until the initial communication settings are specified	t_{SUINIT}	POR and LVD reset must end before the external reset ends.			100	ms
How long from when the TOOL0 pin is placed at the low level until an external reset ends	t_{SU}	POR and LVD reset must end before the external reset ends.	10			μs
How long the TOOL0 pin must be kept at the low level after an external reset ends (excluding the processing time of the firmware to control the flash memory)	t_{HD}	POR and LVD reset must end before the external reset ends.	1			ms



<1> The low level is input to the TOOL0 pin.
<2> The external reset ends (POR and LVD reset must end before the external reset ends).
<3> The TOOL0 pin is set to the high level.
<4> Setting of the flash memory programming mode by UART reception and complete the baud rate setting.

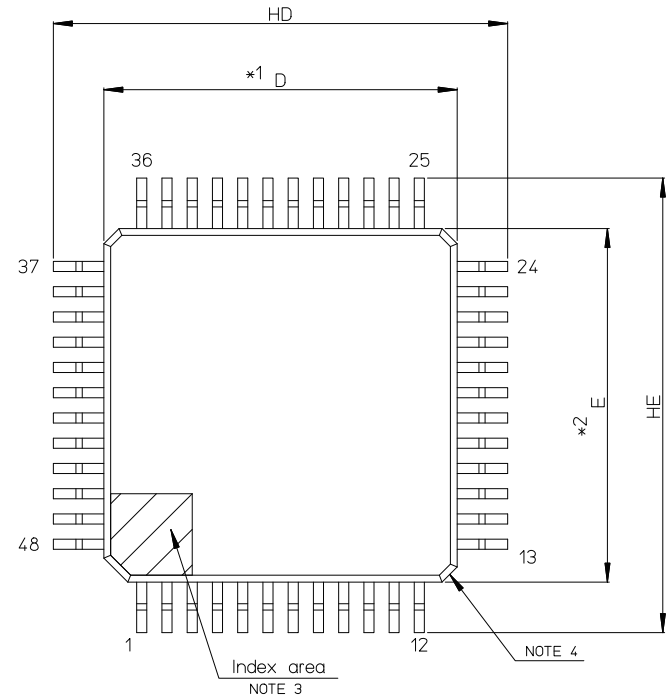
Remark t_{SUINIT}: The segment shows that it is necessary to finish specifying the initial communication settings within 100 ms from when the external resets end.
t_{SU}: How long from when the TOOL0 pin is placed at the low level until a pin reset ends
t_{HD}: How long to keep the TOOL0 pin at the low level from when the external resets end (excluding the processing time of the firmware to control the flash memory)

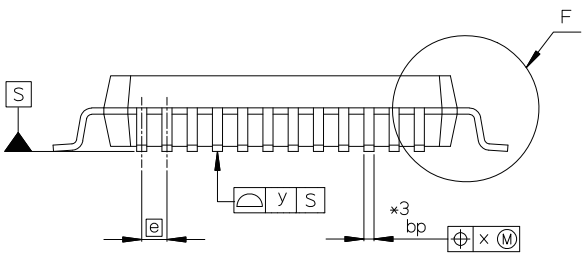
CHAPTER 40 PACKAGE DRAWINGS

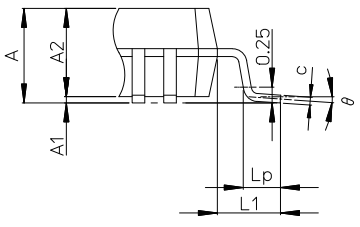
40.1 48-pin products

R5F11NGGAFB, R5F11NGFAFB

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LFQFP48-7x7-0.50	PLQP0048KB-B	——	0.2g







Detail F

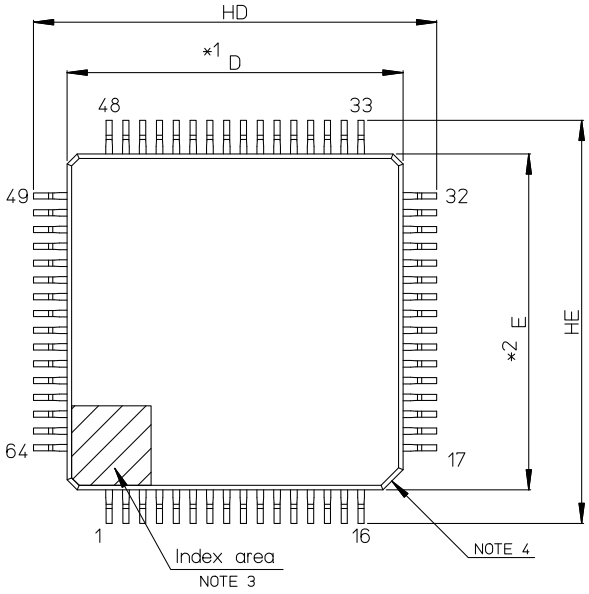
NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.
3. PIN 1 VISUAL INDEX FEATURE MAY VARY, BUT MUST BE LOCATED WITHIN THE HATCHED AREA.
4. CHAMFERS AT CORNERS ARE OPTIONAL, SIZE MAY VARY.

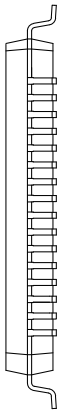
Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	6.9	7.0	7.1
E	6.9	7.0	7.1
A2	——	1.4	——
HD	8.8	9.0	9.2
HE	8.8	9.0	9.2
A	——	——	1.7
A1	0.05	——	0.15
bp	0.17	0.20	0.27
c	0.09	——	0.20
θ	0°	3.5°	8°
e	——	0.5	——
x	——	——	0.08
y	——	——	0.08
Lp	0.45	0.6	0.75
L1	——	1.0	——

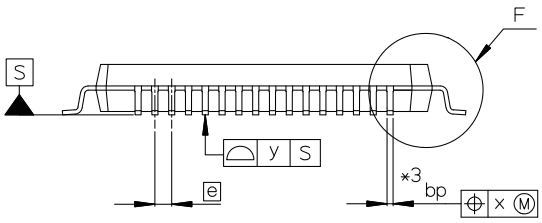
40.2 64-pin products

R5F11NLGAFB, R5F11NLFAFB

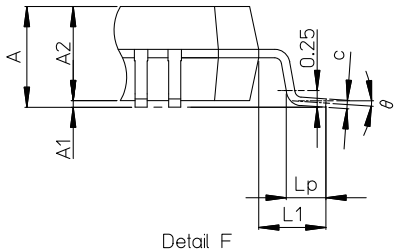
JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LFQFP64-10x10-0.50	PLQP0064KB-C	——	0.3g







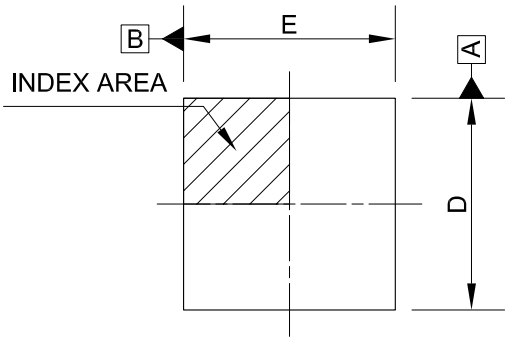
NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.
3. PIN 1 VISUAL INDEX FEATURE MAY VARY, BUT MUST BE LOCATED WITHIN THE HATCHED AREA.
4. CHAMFERS AT CORNERS ARE OPTIONAL; SIZE MAY VARY.

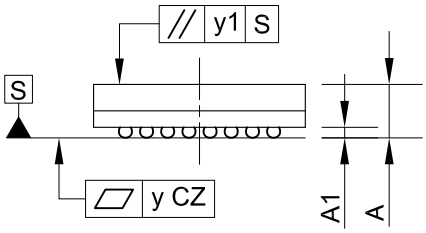


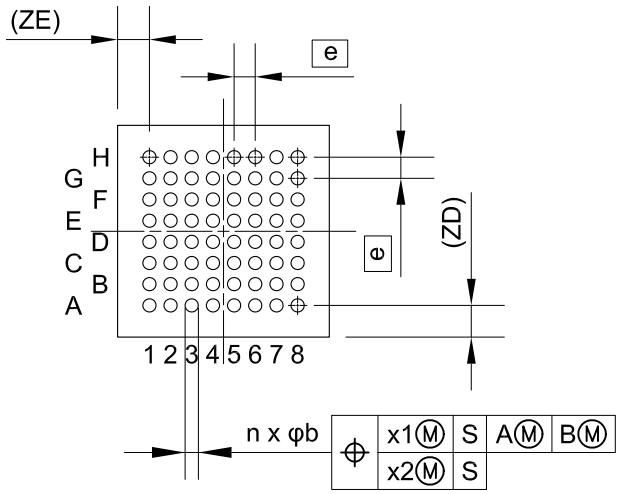
Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	9.9	10.0	10.1
E	9.9	10.0	10.1
A2	——	1.4	——
HD	11.8	12.0	12.2
HE	11.8	12.0	12.2
A	——	——	1.7
A1	0.05	——	0.15
bp	0.15	0.20	0.27
c	0.09	——	0.20
θ	0°	3.5°	8°
e	——	0.5	——
x	——	——	0.08
y	——	——	0.08
Lp	0.45	0.6	0.75
L1	——	1.0	——

R5F11PLGABG, R5F11PLFABG

JEITA Package code	RENESAS code	MASS(TYP.)[g]
P-TFBGA64-4x4-0.40	PTBG0064LA-A	0.03







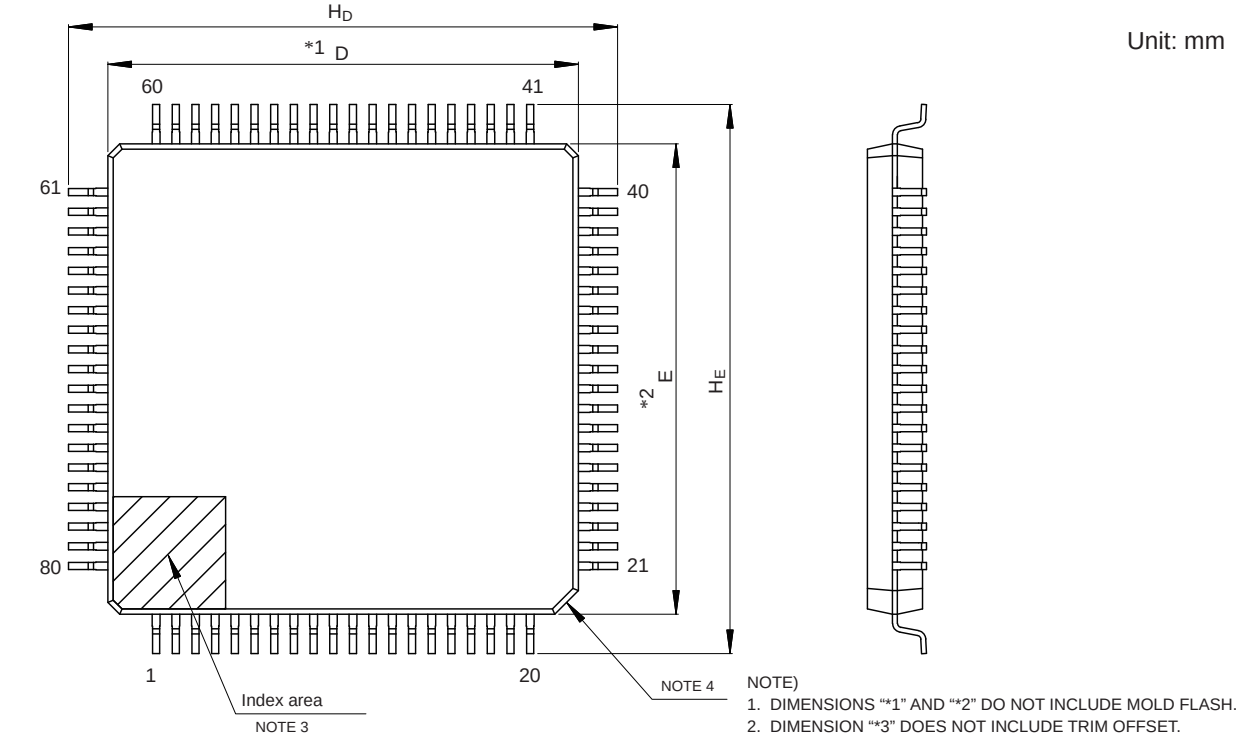
Reference Symbol	Dimension in Millimeters		
	Min.	Nom.	Max.
D	3.9	4.0	4.1
E	3.9	4.0	4.1
A	—	—	1.10
A1	0.15	0.20	0.25
b	0.20	0.25	0.30
e	—	0.40	—
x1	—	—	0.15
x2	—	—	0.05
y	—	—	0.08
y1	—	—	0.20
n	—	64	—
ZD	—	0.60	—
ZE	—	0.60	—

40.3 80-pin products

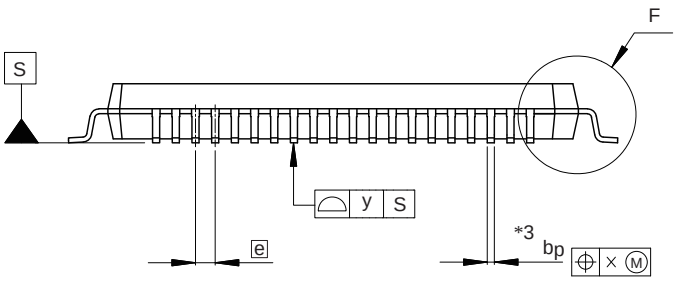
R5F11NMGAFB, R5F11NMFAFB, R5F11NMEAFB
R5F11RMGDFB

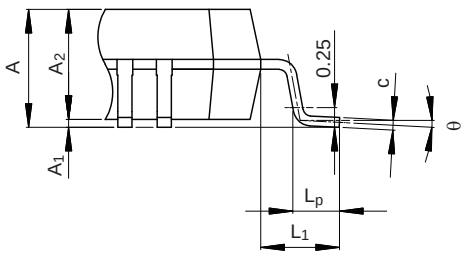
JEITA Package Code	RENESAS Code	Previous Code	MASS (Typ) [g]
P-LFQFP80-12x12-0.50	PLQP0080KB-B	—	0.5

Unit: mm



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.
3. PIN 1 VISUAL INDEX FEATURE MAY VARY, BUT MUST BE LOCATED WITHIN THE HATCHED AREA.
4. CHAMFERS AT CORNERS ARE OPTIONAL, SIZE MAY VARY.





Detail F

Reference Symbol	Dimensions in millimeters		
	Min	Nom	Max
D	11.9	12.0	12.1
E	11.9	12.0	12.1
A_2	—	1.4	—
H_D	13.8	14.0	14.2
H_E	13.8	14.0	14.2
A	—	—	1.7
A_1	0.05	—	0.15
b_p	0.15	0.20	0.27
c	0.09	—	0.20
θ	0°	3.5°	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
L_p	0.45	0.6	0.75
L_1	—	1.0	—

APPENDIX A REVISION HISTORY

A.1 Major Revisions in This Edition

(1/1)

Page	Description	Classification
CHAPTER 1 OUTLINE		
p.5	Modification of table in **1.2 Ordering Information**	(d)
p.6	Modification of **Figure 1-1 Part Number, Memory Size, and Package of RL78/H1D**	(d)
CHAPTER 31 SAFETY FUNCTIONS		
p.1066	Modification of description in **31.1 Overview of Safety Functions**	(c)
p.1071	Modification of description in **31.3.2 CRC operation function (general-purpose CRC)**	(c)
p.1074	Modification of description in **31.3.4 RAM guard function**	(c)
p.1075	Modification of description in **31.3.5 SFR guard function**	(c)

Remark “Classification” in the above table classifies revisions as follows.
(a): Error correction, (b): Addition/change of specifications, (c): Addition/change of description or note,
(d): Addition/change of package, part number, or management division, (e): Addition/change of related documents

A.2 Revision History of Preceding Editions

Here is the revision history of the preceding editions. Chapter indicates the chapter of each edition.

(1/4)

Edition	Description	Chapter
Rev.0.50	First Edition issued	All
Rev.0.80	PG-FP5 has been modified to PG-FP6, FL-PR5 has been modified to FL-PR6, and description of E2, E2 Lite, and E20 has been added.	All
	Modification of orderable part number in **1.2 Ordering Information**	CHAPTER 1 OUTLINE
	Modification of note 1 in **Figure 3 - 1 Memory Map (R5F11NME)**	CHAPTER 3 CPU ARCHITECTURE
	Modification of note 1 in **Figure 3 - 2 Memory Map (R5F11xF (x = NG, NL, NM, PL))**	
	Modification of note 1 in **Figure 3 - 3 Memory Map (R5F11xG (x = NG, NL, NM, PL))**	
	Modification of note 1 in **Figure 3 - 4 Memory Map (R5F11RMG)**	
	Modification of description in **5.4.4 Low-speed on-chip oscillator**	CHAPTER 5 CLOCK GENERATOR
	Addition of note in **Table 14 - 5 Setting of Watchdog Timer Interval Interrupt**	CHAPTER 14 WATCHDOG TIMER
	Addition of **14.4.5 Cautions on the watchdog timer**	
	Modification of description in **15.1 Functions of Analog Front-End Power Supply Circuit**	CHAPTER 15 ANALOG FRONT-END POWER SUPPLY CIRCUIT (R5F11N and R5F11P only)
	Modification of description in **15.4.1 Overview of AFE internal reference voltage generator**	
	Modification of figure and note in **Figure 16 - 1 Block Diagram of 24-bit ΔΣ A/D Converter with Programmable Gain Instrumentation Amplifier**	CHAPTER 16 24-BIT ΔΣ A/D CONVERTER WITH PROGRAMMABLE GAIN INSTRUMENTATION AMPLIFIER (R5F11N and R5F11P only)
	Modification of description in **16.4.1 Overview of programmable gain instrumentation amplifier (PGA0)**	
	Modification of **Figure 16 - 7 Transition of the Differential Input Voltage Level in the Programmable Gain Instrumentation Amplifier**	
	Modification of description in **16.4.4 Input voltage range in differential input mode**	
	Modification of description and addition of caution 2 in **Figure 16 - 19 Format of ΔΣ A/D Converter Control Register (DSADCTL)**	
	Addition of description in **17.3.4 Amplifier trigger mode control register (AMPTRM)**	CHAPTER 17 AMPLIFIER UNIT (R5F11N and R5F11P only)
	Modification of **Figure 17 - 13 Format of Amplifier Unit 0 Gain Setting Register (PGA1GC)**	
	Modification of description and note 2 in **17.4.3 Software trigger mode**	
	Modification of note 3 in **17.4.5 ELC and A/D Trigger Mode**	
	Modification of description in **17.5 Usage Notes on Amplifier Unit**	
	Modification of **Figure 19 - 11 Format of Analog input channel specification register (ADS)**	CHAPTER 19 A/D CONVERTER
	Modification of **Figure 20 - 123 Transmission Operation of LIN**	CHAPTER 20 SERIAL ARRAY UNIT
	Modification of **Figure 20 - 124 Flowchart for LIN Transmission**	
	Modification of **Figure 20 - 125 Reception Operation of LIN**	
	Modification of **Figure 20 - 126 Flowchart of LIN Reception**	
	Modification of description in **22.3.4 (2) Generation of serial clock**	CHAPTER 22 SERIAL INTERFACE UARTMG (R5F11R Only)
	Modification of figure and note in **Figure 23 - 3 Format of LCD Mode Register 1 (LCDM1) (2/2)**	CHAPTER 23 LCD CONTROLLER/DRIVER (R5F11NM, R5F11NL, and R5F11RM only)

(2/4)

Edition	Description	Chapter
Rev.0.80	Addition of remark 2 in **31.1 Overview of Safety Functions**	CHAPTER 31 SAFETY FUNCTIONS
	Addition of note 3 in **Figure 33 - 1 Format of User Option Byte (000C0H/010C0H)**	CHAPTER 33 OPTION BYTE
	Modification of **Figure 34 - 7 Setting of Flash Memory Programming Mode**	CHAPTER 34 FLASH MEMORY
	Modification of **38.3.1 Pin characteristics**	CHAPTER 38 ELECTRICAL SPECIFICATIONS (R5F11N, R5F11P) (A: T_A = -40 to +85°C)
	Modification of **38.3.2 Supply current characteristics**	
	Modification of note 1 in **38.3.2 Supply current characteristics**	
	Modification of remark 1, and deletion of remark 2 in **38.5.1 (3) During communication at same potential (CSI mode) (slave mode, SCKp... external clock output) (2/2)**	
	Modification of **38.6.5 (3) Programmable gain instrumentation amplifier and 24-bit ΔΣ A/D converter**	
	Addition of remark 2 in **38.6.5 (3) Programmable gain instrumentation amplifier and 24-bit ΔΣ A/D converter**	
	Modification of table and addition of remark 2 in **38.6.6 Sensor power supply (SBIAS)**	
	Modification of table and addition of remark 2 in **38.6.7 Internal BIAS power supply**	
	Modification of **38.6.8 Programmable gain instrumentation amplifier (PGA1)**	
	Modification of **38.6.9 Operational amplifier 0 (AMP0)**	
	Modification of **38.6.10 Operational amplifiers 1 and 2 (AMP1, AMP2)**	
	Modification of **38.6.11 8-bit D/A converter (DAC0)**	
	Modification of **38.6.12 12-bit D/A converter (DAC1)**	
	Modification of **38.12 Timing of Entry to Flash Memory Programming Modes**	
	Modification of **39.1 Absolute Maximum Ratings**	CHAPTER 39 ELECTRICAL SPECIFICATIONS (R5F11R) (D: T_A = -40 to +85°C)
	Modification of **39.3.1 Pin characteristics**	
	Modification of **39.3.2 Supply current characteristics**	
	Modification of remark 1, and deletion of remark 2 in **39.5.1 (3) During communication at same potential (CSI mode) (slave mode, SCKp... external clock input) (T_A = -40 to +85°C, 1.8 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V)**	
	Modification of **39.12 Timing of Entry to Flash Memory Programming Modes**	
	Addition of figure in **40.2 64-pin products**	CHAPTER 40 PACKAGE DRAWINGS

(3/4)

Edition	Description	Chapter
Rev.1.00	Package name "VFBGA" has been modified to "TFBGA".	All
	Modification of title and description in **3.4.4 Register indirect addressing**	CHAPTER 3 CPU ARCHITECTURE
	Modification of title in **Figure 3 - 17 Outline of Register Indirect Addressing**	
	Modification of **Figure 3 - 37 Example of CALL, CALLT**	
	Modification of description in **7.4.2 Timer operation**	CHAPTER 7 8-BIT INTERVAL TIMER
	Addition of **7.4.5 Procedure for Setting the 8-bit Interval Timer**	
	Modification of figure and addition of remark in **Figure 12 - 1 Block Diagram of External Signal Sampler**	CHAPTER 12 EXTERNAL SIGNAL SAMPLER (R5F11R only)
	Addition of description in **12.6 Cautions**	
	Modification of figure and note 1 in **Figure 13 - 2 Format of Clock output select registers n (CKSn)**	CHAPTER 13 CLOCK OUTPUT/BUZZER OUTPUT CONTROLLER
	Modification of note 2 in **Figure 20 - 109 Example of Contents of Registers for UART Reception of UART (UART0 to UART2) (1/2)**	CHAPTER 20 SERIAL ARRAY UNIT
	Modification of description in **21.5.17 Timing of I^2C interrupt request (INTIICAn) occurrence (1) Master device operation (c) Start ~ Code ~ Data ~ Data ~ Stop (extension code transmission) (ii) When WTIMn = 1**	CHAPTER 21 SERIAL INTERFACE IICA
	Addition of description in **24.5.7 DTC activation sources**	CHAPTER 24 DATA TRANSFER CONTROLLER (DTC)
	Modification of description in **25.3.1 Event output destination select register n (ELSELRn) (n = 00 to 25)**	CHAPTER 25 EVENT LINK CONTROLLER (ELC)
	Modification of **Table 27 - 2 Operating Statuses in STOP Mode (1/2)**	CHAPTER 27 STANDBY FUNCTION
	Modification of **Figure 27 - 5 When the Interrupt Request Signal is Generated in the SNOOZE Mode**	
	Modification of **Figure 27 - 6 When the Interrupt Request Signal is not Generated in the SNOOZE Mode**	
	Modification of figure, and notes 3 and 4 in **Figure 29 - 2 Timing of Generation of Internal Reset Signal by Power-on-reset Circuit and Voltage Detector (1/3)**	CHAPTER 29 POWER-ON-RESET CIRCUIT
	Modification of figure in **40.2 64-pin products**	CHAPTER 40 PACKAGE DRAWINGS

(4/4)

Edition	Description	Chapter
Rev.1.10	The module name for 3-wire serial I/O and 3-wire serial were changed to simplified SPI.	All
	The module name for CSI was changed to simplified SPI.	
	“Wait” was modified to “clock stretch”.	
	Modification from Note to Notes 3 **1.1 Features**	CHAPTER 1 OUTLINE
	Modification of **1.2 Ordering Information**	
	Modification of **Figure 1-1 Part Number, Memory Size, and Package of RL78/H1D**	
	Modification from Note to Note 1 in **4.5.4 Handling different potential (1.8 V Note, 2.5 V, 3 V) by using I/O buffers**	CHAPTER 4 PORT FUNCTIONS
	Addition of Note 2 in **4.5.4 Handling different potential (1.8 V Note, 2.5 V, 3 V) by using I/O buffers**	
	Modification of **Figure 8-7 Format of Real-time clock control register 1 (RTCC1) (3/3)**	CHAPTER 8 REAL-TIME CLOCK 2
	Modification of Note 2 in **Figure 8-21 Procedure for Reading Real-time Clock 2**	
	Modification of Caution in **Figure 8-21 Procedure for Reading Real-time Clock 2**	
	Modification of Note 2 in **Figure 8-22 Procedure for Writing Real-time Clock 2**	
	Modification of Caution 1 in **Figure 8-22 Procedure for Writing Real-time Clock 2**	
	Addition of Note in **CHAPTER 20 SERIAL ARRAY UNIT**	CHAPTER 20 SERIAL ARRAY UNIT
	Modification of title in **Figure 21 - 25 Clock stretch (1/2)**	CHAPTER 21 SERIAL INTERFACE IICA
	Modification of title in **Figure 21 - 25 Clock stretch (2/2)**	
	Modification of title in **Figure 21-45 Example of Slave to Master Communication (8th Cycle Clock Stretch is Changed to 9th Cycle Clock Stretch for Master, 9th Cycle Clock Stretch is Selected for Slave)**	
	Modification of Note 1, and 4 in **38.3.2 Supply current characteristics**	CHAPTER 38 ELECTRICAL SPECIFICATIONS (R5F11N, R5F11P) (A: T_A = -40 to +85°C)
	Modification of Note 1, and 5 and delete Note 6 in **38.3.2 Supply current characteristics**	
	Modification of Note 1, and 4 in **39.3.2 Supply current characteristics**	CHAPTER 39 ELECTRICAL SPECIFICATIONS (R5F11R) (D: T_A = -40 to +85°C)
	Modification of Note 1, and 5 and delete Note 6 in **39.3.2 Supply current characteristics**	
	Modification of package drawing in **40.1 48-pin products (PLQP0048KB-B)**	CHAPTER 40 PACKAGE DRAWINGS
	Modification of package drawing in **40.2 64-pin products (PLQP0064KB-C)**	
	Modification of package drawing in **40.3 80-pin products (PLQP0080KB-B)**	

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