User's Manual

R-IN32M3 Series

User's Manual

R-IN32M3-EC

MC-10287BF1-HN4-A

MC-10287BF1-HN4-M1-A

Renesas Electronics

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General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products
   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

How to Use This Manual

1. Purpose and Target Readers

This manual is intended for users who wish to understand the functions of industrial Ethernet network ASSP (application specific standard product) "R-IN32M3-EC" (MC-10287BF1-HN4-A, MC-10287BF1-HN4-M1-A) for designing application of it.
It is assumed that the reader of this manual has general knowledge in the fields of electrical engineering, logic circuits, and microcontrollers.

Particular attention should be paid to the precautionary notes when using the manual. These notes occur within the body of the text, at the end of each section, and in the Usage Notes section.

The revision history summarizes the locations of revisions and additions. It does not list all revisions. Refer to the text of the manual for details.

Literature

Literature may be preliminary versions. Note, however, that the following descriptions do not indicate "Preliminary". Some documents on cores were created when they were planned or still under development. So, they may be directed to specific customers. Last four digits of document number (described as ****) indicate version information of each document. Please download the latest document from our web site and refer to it.

The document related to R-IN32M3-EC

Document Name	Document Number
R-IN32M3 Series Datasheet	R18DS0008EJ****
R-IN32M3-CL User's Manual	R18UZ0005EJ****
R-IN32M3 Series User's Manual (Peripheral Modules)	R18UZ0007EJ****
R-IN32M3 Series Programming Manual (Driver edition)	R18UZ0009EJ****
R-IN32M3 Series Programming Manual (OS edition)	R18UZ0011EJ****
R-IN32M3 Series User's Manual (Board design edition)	R18UZ0021EJ****
R-IN32M3-EC User's Manual	This manual

2. Notation of Numbers and Symbols

Weight in data notation: Left is high-order column, right is low-order column

Active low notation:

xxxZ (capital letter Z after pin name or signal name)

or xxx_N (capital letter _N after pin name or signal name)

or xxnx (pin name or signal name contains small letter n)

Note:

Explanation of (Note) in the text

Caution:

Item deserving extra attention

Remark:

Supplementary explanation to the text

Numeric notation:

Binary ⋯ xxxx , xxxxB or n'bxxxx (n bits)

Decimal ⋯ xxxx

Hexadecimal ⋯ xxxxH or n'hxxxx (n bits)

Prefixes representing powers of 2 (address space, memory capacity):

K (kilo)⋯ $2^{10} = 1024$

M (mega)⋯ $2^{20} = 1024^2$

G (giga)⋯ $2^{30} = 1024^3$

Data Type:

Word ⋯ 32 bits

Halfword ⋯ 16 bits

Byte ⋯ 8 bits

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1. Overview

1.1 Introduction

Ethernet communication continues to spread rapidly in the field of industrial automation as manufacturers seek to improve the capability, efficiency, and flexibility of their organizations. Modern industrial Ethernet applications require high-speed real-time response, low power consumption, and high performance. These requirements are not necessarily met by traditional methods such as hard-wired Ethernet processors or dedicated high-speed CPUs.

Renesas R-IN32M3-EC of large-scale integrated circuits (LSI) are specifically tailored to meet the demands of industrial Ethernet applications. Key features include:

- Integrated Arm® Cortex®-MY core for flexibility
- Integrated real-time OS accelerator with support for citrons version 4.0
- Integrated 10/100 Mbps EtherPHY
- Dedicated DMA controller and buffer for the network processor
- Multiple timers, serial interfaces, general purpose I/O (GPIO), external memory interfaces
- High-speed, real-time, deterministic, low-latency, low-jitter response for real-time applications
- High performance with low CPU usage by offloading functions to real-time OS accelerator
- Low power consumption

1.2 Overview

Table 1.1 Overview of R-IN32M3-EC

(1/2)

Item \ Product	R-IN32M3-EC
CPU cores	Arm Cortex-M3 32-bit RISC CPU + Real-Time OS Accelerator (Hardware Real-Time OS, HW-RTOS)
Operating frequency	100 MHz
Instruction set	Thumb®-2 instruction Arm v7-M architecture
Instruction RAM	768 Kbytes (RAM with ECC)
Data RAM	512 Kbytes (RAM with ECC)
Buffer RAM	64 Kbytes (RAM with ECC)
Internal system bus	- 32-bit system bus at 100 MHz - 128-bit communication bus at 100 MHz
DMA bus (system bus side)	- 4 channels + 1 channel (for real-time port) - Supports software and various interrupt-triggered DMA
Boot options	- Serial flash ROM boot - External memory boot - External MCU boot
External memory support	- 16-bit or 32-bit bus interface - Page ROM / ROM / SRAM interface - Synchronous burst memory interface - Four chip selects for external SRAM - 256-Mbyte (max) external memory space - Programmable wait function
External MCU interface	- 16-bit or 32-bit bus interface - General-purpose interface for static memory - Address space: 2 Mbytes (instruction RAM, data RAM, register area)
Serial flash ROM memory controller	- Support serial interface compatible with SPI of the companies - Support direct boot from serial memory device - Support Fast Read, Fast Read Dual Output, Fast Read Dual I/O mode - Direct layout in memory space
Interrupt	- 29 external interrupt pins
Internal peripheral circuit	
I/O ports	CMOS I/O: 96 pins (max.)
Timers (three systems)	- Internal timer of Hardware RTOS
	- Internal timer of CPU
	- 4-channel timer array - 32-bit counter & 32-bit data register - Counter by external signal

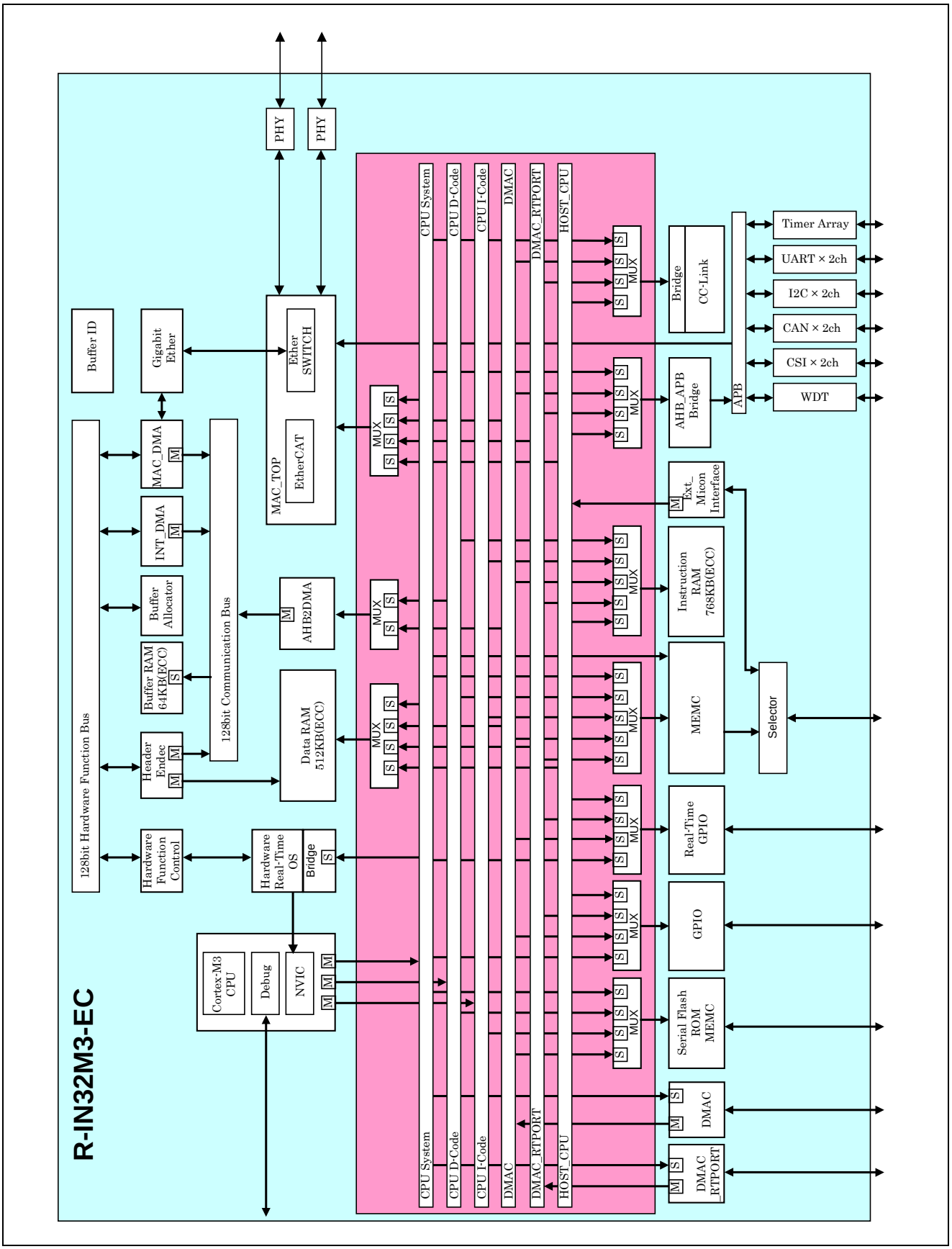
(2/2)

Item \ Product	R-IN32M3-EC
Internal peripheral circuit	
Watchdog timer	- 1 channel - Software-triggered start mode - Selectable operations in response to errors: - Generation of a non-maskable interrupt (NMIZ) - Generation of a reset
Asynchronous serial interface	- 2 channels - Full duplex - FIFOs: 10 bits x 16 receive and 8 bits x 16 transmit - Support output of receive errors and status - Character length: 7 or 8 bits - Parity bit options: Odd, even, 0, none - Transmit stop bits: 1 or 2 bits
I2C serial interface	- 2 channels - Operating modes: Normal or high-speed - Transfer modes: Single-transfer mode or continuous-transfer mode - Transmission data length: 8 bits
CAN controller	- 2 channels - Conforming to ISO11898 - Support to transfer and receive normal frame and expand frame - Transmission speed: 1 Mbps (max)
Clock synchronous serial interface	- 2 channels - Synchronized serial data transmission by three-wire system - Selectable master mode or slave mode - Built-in baud-rate generator - Transmission data length: 7 bits to 16 bits
CC-Link	- Intelligent device station Note1 - Remote device station
10/100-Mbps EtherPHY Note2	- 2 ports - Support 10BaseT and 100Base TX/FX
EtherCAT	EtherCAT® slave controller
On-chip debug function	- Select serial wire or JTAG - Support Full Trace (Built-in ETM)
Internal PLL	Generates various clocks from 25-MHz input clock
Power supply voltage	I/O: VDD33 = 3.3±0.3 V Internal circuit: VDD10 = 1.0±0.1 V On-chip PHY: VDD15 = 1.5±0.15 V (on-chip regulator is available.)

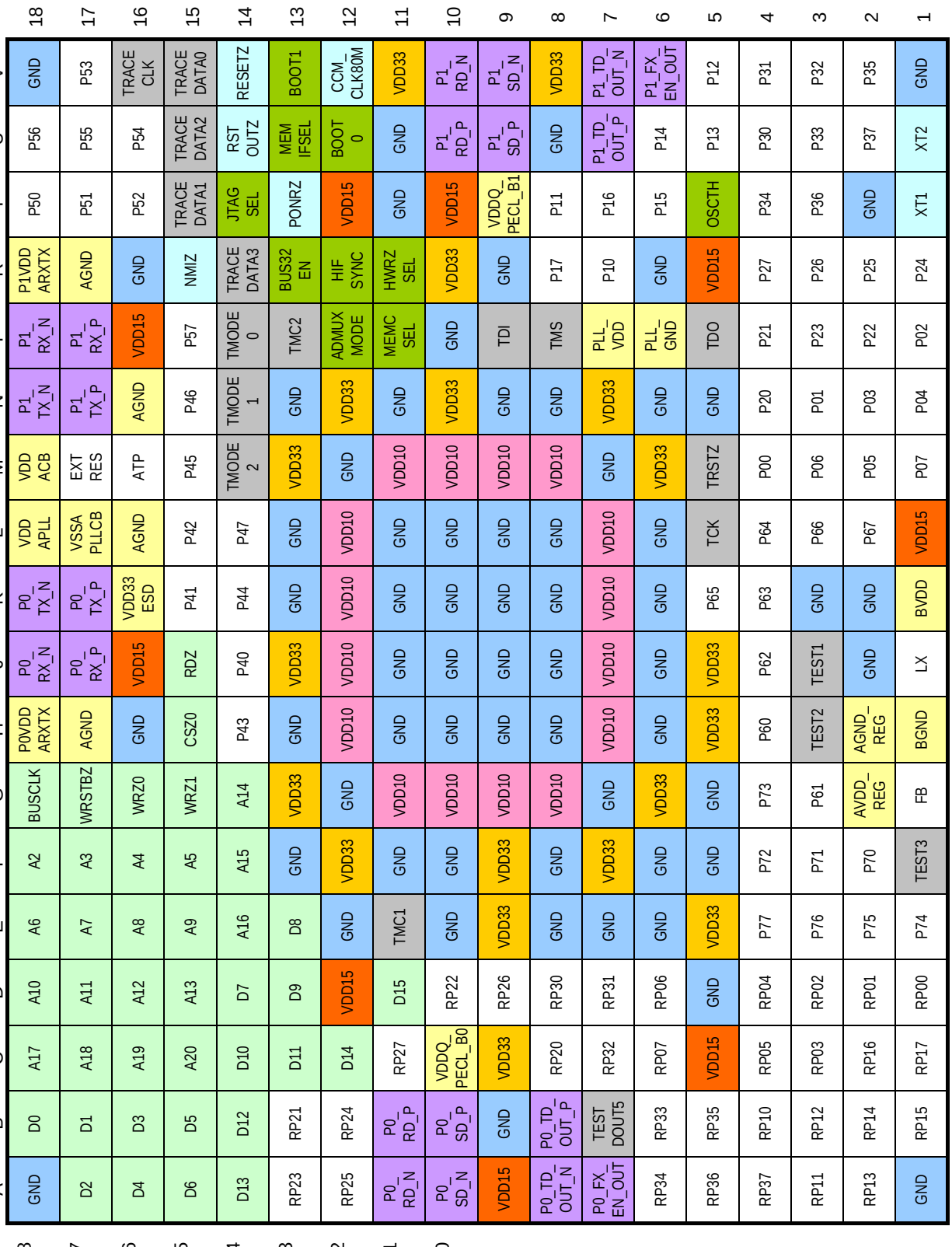
Note 1. Please contact our sales representative for details.

2. EtherCAT P is not supported.

1.3 Internal Block Diagram



1.4 Pin Assignments (Top View)



1.5 Base Addresses of the System Registers Area

The addresses of registers given in the subsequent sections are relative to the base addresses. In access to the registers via the external MCU interface, the base address is D_0000H. In access by the internal CPU or DMA controller, the base address is 4001_0000H.

- In access by the CPU or DMA controller
  BASE = 4001_0000H
- In access via the external microcontroller interface
  BASE = D_0000H

2. Pin Functions

The meanings of the symbols and abbreviations used in this document are given below.

Table 2.1 Meanings of the Items in the List of Pins

Item	Meaning
Pin name	Name of the pin shown in section 1.4, Pin Assignments (Top View).
I/O	I/O direction of the given pin
Function	Summary of the given pin function
Active	Active level of the given pin
Level during reset Level after reset	"Level during reset" indicates the pin state while RSTOUTZ = low, and "Level after reset" indicates the pin state directly after the transition to RSTOUTZ = high. For details on the reset specifications, see the R-IN32M3 Series User's Manual (Peripheral Modules).

Table 2.2 Meanings of the Symbols and Abbreviations in the List of Pins

Target	Symbol and Abbreviation	Meaning
Pin name	- (hyphen)	Indicates that the pin is a dedicated pin and is not multiplexed with a port-pin function.
I/O	- (hyphen)	Indicates that the pin is a pin such as a power supply or ground pin and so does not have an I/O direction.
Active	- (hyphen)	Indicates that there is no active level (clock signals, data bus, and address bus).
	High	The active level is high.
	Low	The active level is low.
Level during reset Level after reset	- (hyphen)	Indicates an input-dedicated pin that has no initial level or state following a reset.
	High	The pin state during a reset is high.
	Low	The pin state during a reset is low.
	Hi-Z (high)	The pin state during a reset is Hi-Z (high) with the internal pull-up resistor pulling it to the high level.
	Hi-Z (low)	The pin state during a reset is Hi-Z (low) with the internal pull-up resistor pulling it to the low level.

2.1 List of Pins

2.1.1 Ethernet Pins

(1) Media Interface Pins

Pin Name	I/O	Function	Active	Level during & after Reset
P0_RX_P	I	PHY0 receive data input (+)	-	-
P0_RX_N	I	PHY0 receive data input (-)	-	-
P1_RX_P	I	PHY1 receive data input (+)	-	-
P1_RX_N	I	PHY1 receive data input (-)	-	-
P0_TX_P	O	PHY0 transmit data output (+)	-	-
P0_TX_N	O	PHY0 transmit data output (-)	-	-
P1_TX_P	O	PHY1 transmit data output (+)	-	-
P1_TX_N	O	PHY1 transmit data output (-)	-	-
P0_SD_P	I	PHY0 100BASE-FX signal detect (+)	High	-
P0_SD_N	I	PHY0 100BASE-FX signal detect (-)	Low	-
P1_SD_P	I	PHY1 100BASE-FX signal detect (+)	High	-
P1_SD_N	I	PHY1 100BASE-FX signal detect (-)	Low	-
P0_RD_P	I	PHY0 100BASE-FX receive data input (+)	-	-
P0_RD_N	I	PHY0 100BASE-FX receive data input (-)	-	-
P1_RD_P	I	PHY1 100BASE-FX receive data input (+)	-	-
P1_RD_N	I	PHY1 100BASE-FX receive data input (-)	-	-
P0_TD_OUT_P	O	PHY0 100BASE-FX transmit data output (+)	-	-
P0_TD_OUT_N	O	PHY0 100BASE-FX transmit data output (-)	-	-
P1_TD_OUT_P	O	PHY1 100BASE-FX transmit data output (+)	-	-
P1_TD_OUT_N	O	PHY1 100BASE-FX Transmit data output (-)	-	-
P0_FX_EN_OUT	O	PHY0 100BASE-FX FX enable indication output 1: 100BASE-FX mode	High	-
P1_FX_EN_OUT	O	PHY1 100BASE-FX FX enable indication output 1: 100BASE-FX mode	High	-

Remark: In MDI-X mode but not in 100BASE-FX mode, the input and output attributes of RXP/RXN and TXP/TXN are reversed.

(2) Other Pins

Pin Name	I/O	Function	Shared Port	Active	Level during & after Reset
P0LINKLEDZ	O	On-chip PHY0 link status LED output	P06	Low	Hi-Z
P1LINKLEDZ	O	On-chip PHY1 link status LED output	P07	Low	
ETHSWSECOUT	O	EtherSwitch event output per second	P24	High	
P0DUPLEXLEDZ	O	On-chip PHY0 half-duplex transfer status LED output 0: Full-duplex 1: Half-duplex	P70	-	
P0SPEED100LEDZ	O	On-chip PHY0 100-BASE status LED output	P72	Low	
P0SPEED10LEDZ	O	On-chip PHY0 10-BASE status LED output	P73	Low	
P1DUPLEXLEDZ	O	On-chip PHY1 half-duplex transfer status LED output 0: Full-duplex 1: Half-duplex	P74	-	
P1SPEED100LEDZ	O	On-chip PHY1 100-BASE status LED output	P76	Low	
P1SPEED10LEDZ	O	On-chip PHY1 10-BASE status LED output	P77	Low	
P0ACTLEDZ	O	On-chip PHY0 ACT LED output	RP02	Low	Hi-Z (High)
P1ACTLEDZ	O	On-chip PHY1 ACT LED output	RP04	Low	

2.1.2 EtherCAT Slave Controller Pins

Pin Name	I/O	Function	Shared Port	Active	Level during & after Reset
CATLEDRUN	O	EtherCAT RUN LED output	P00	High	Hi-Z
CATIRQ	O	EtherCAT IRQ output	P01	High	
CATLEDSTER	O	EtherCAT dual-color state LED output	P02	High	
CATLEDERR	O	EtherCAT error LED output	P03	High	
CATLINKACT0, CATLINKACT1	O	EtherCAT link / activity LED output	P04-P05	High	
CATSYNC1	O	EtherCAT SYNC1 output	P10	High	Hi-Z (High)
CATSYNC0	O	EtherCAT SYNC0 output	P11	High	Hi-Z (Low)
CATLATCH1	I	EtherCAT LATCH1 input	P10	High	Hi-Z (High)
CATLATCH0	I	EtherCAT LATCH0 input	P11	High	Hi-Z (Low)
CATI2CCLK	O	EtherCAT EEPROM I2C clock output	P22	-	Hi-Z
CATI2CDATA	I/O	EtherCAT EEPROM I2C data	P23	-	
CATRESTOUT	O	EtherCAT PHY RESETOUT	P56	High	Hi-Z (High)

2.1.3 External Memory Interface Pins

Pin Name	I/O	Function	Shared Pin	Shared Port	Active	Level during Reset	Level after Reset
BUSCLK	O	Bus clock output	-	-	-	Clock output	
CSZ0	O	Chip select signal output	HCSZ	-	Low	Hi-Z (High)	High
CSZ1	O		HPGCSZ	P44			Hi-Z (High)
CSZ2	O		-	P51			
CSZ3	O		-	P50			
A1/MA0 Note4	O	Address output	HA1	P40	-		Low
A2-A20/MA1-MA19 Note4	O		HA2-HA20	-		Hi-Z (Low)	
A21-A27/MA20-MA26 Note4	O		-	RP21-RP27			Hi-Z (Low)
D0-D15/MD0-MD15 Note1 Note4	I/O	Data bus	HD0-HD15	-			
D16-D31/MD16-MD31 Note1 Note4	I/O		HD16-HD31	RP30-RP37 RP10-RP17	-	Hi-Z (High)	
RDZ	O	Read strobe output	HRDZ	-	Low	Hi-Z (High)	High
WRSTBZ	O	Write strobe output	HWRSTBZ	-	Low		
WRZ0, WRZ1/ BENZ0, BENZ1	O	Valid byte lane strobe output	HWRZ0, HWRZ1/ HBENZ0, HBENZ1	-	Low		
WRZ2, WRZ3/ BENZ2, BENZ3	O		HWRZ2, HWRZ3/ HBENZ2, HBENZ3	RP06, RP07			Hi-Z (High)
WAITZ	I	Wait signal input	HWAITZ	P41	Low	Hi-Z (High)	
WAITZ1-WAITZ3 Note2	I	Wait signal input	-	P45-P47	Low		
BCYSTZ / ADVZ Note3	O	Address valid output	HBCYSTZ	RP20	Low		

Remark: **Pins of the external memory interface pins other than BUSCLK are input pins while the internal reset signal (HRESETZ) is at its active level.**

Notes 1. **While the synchronous burst access memory controller is in use, these signals are multiplexed with the address signals if the ADMUXMODE pin is driven high.**
ADMUXMODE = 0: MD0-MD31 (Separate address and data lines)
ADMUXMODE = 1: MD0-MD31/MA0-MA31 (Multiplexed address and data lines)

2. **These pins are only available when the synchronous burst access memory controller is in use.**
3. **This pin functions as BCYSTZ when the asynchronous SRAM memory controller is in use and as ADVZ when the synchronous burst access memory controller is in use.**
4. **This pin functions as A1-A27 and D0-D31 functions when the asynchronous SRAM memory controller is in use and as MA0-MA26 and MD0-MD31 functions when the synchronous burst access memory controller is in use.**

2.1.4 External MCU Interface Pins

Pin Name	I/O	Function	Shared Pin	Shared Port	Active	Level during & after Reset
HBUSCLK	I	Bus clock input for host	INTPZ11	P43	-	Hi-Z (High)
HCSZ	I	Chip select signal input	CSZ0	-	Low	
HPGCSZ	I	Page POM mode chip select input	CSZ1	P44	Low	
HWAITZ	O	Wait signal output	WAITZ	P41	Low	
HA1	I	Address signal input	A1	P40	-	
HA2-HA20	I		A2-A20	-		Hi-Z (Low)
HD0-HD15	I/O	Data bus	D0-D15	-	-	Hi-Z (Low)
HD16-HD31	I/O		D16-D31	RP30-RP37 RP10-RP17		Hi-Z (High)
HRDZ	I	Read strobe input	RDZ	-	Low	
HWRSTBZ	I	Write strobe input	WRSTBZ	-	Low	
HWRZ0, HWRZ1/ HBENZ0, HBENZ1	I	Valid byte lane strobe input	WRZ0, WRZ1/ BENZ0, BENZ1	-	Low	
HWRZ2, HWRZ3/ HBENZ2, HBENZ3	I		WRZ2, WRZ3/ BENZ2, BENZ3	RP06, RP07		
HERROUTZ	O	Error interrupt output	SLEEPING	P42	Low	High
HBCYSTZ	I	Bus cycle input	BCYSTZ / ADVZ	RP20	Low	Hi-Z (High)

Caution: Input the low level to the HBUSCLK pin while asynchronous mode is in use.

Remark: The external MCU interface pins continue to operate during a reset.

2.1.5 Port Pins and Real-Time Port Pins

The ports and pins are configured as 12 sets of 8-bit ports.
They are accessible in 32-bit units by grouping sets of 4 ports; i.e. ports 0 to 3, ports 4 to 7, and real-time ports 0 to 3.

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	Pin Name	Mode 1	Mode 2	Mode 3	Mode 4	Level during & after Reset
P0	P00	INTPZ0	CATLEDRUN	-	-	Hi-Z
	P01	INTPZ1	CATIRQ	-	-	
	P02	INTPZ2	CATLEDSTER	-	-	
	P03	INTPZ3	CATLEDERR	-	CCS_MON5	
	P04	INTPZ4	CATLINKACT0	-	CCS_MON6	
	P05	INTPZ5	CATLINKACT1	-	CCS_MON7	
	P06	-	P0LINKLEDZ	-	CCS_MON0	
	P07	-	P1LINKLEDZ	-	CCS_RESOUT	
P1	P10	CATLATCH1	CATSYNC1	-	CCS_REFSTB	Hi-Z (High)
	P11	CATLATCH0	CATSYNC0	-	CCS_MON4	Hi-Z (Low)
	P12	INTPZ6	-	-	-	Hi-Z (High)
	P13	INTPZ7	-	CCS_WDTZ / CCM_WDTENZ	-	
	P14	SMSCK	-	-	-	
	P15	SMSI	-	-	-	
	P16	SMSO	-	-	-	
	P17	SMCSZ	-	-	-	
P2	P20	RXD0	−	CCM_LINKERRZ	-	Hi-Z
	P21	TXD0	−	CCM_ERRZ	-	
	P22	INTPZ8	CATI2CCLK	CCS_IOTENSU	-	
	P23	INTPZ9	CATI2CDATA	CCS_SENYU0	-	
	P24	INTPZ10	ETHSWSECOUT	CCS_SENYU1	-	
	P25	WDTOUTZ	−	CCS_ERRZ	-	
	P26	TIN1	TOUT1	CCM_RUNZ / CCS_RUNZ	-	
	P27	TIN0	TOUT0	-	-	

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	Pin Name	Mode 1	Mode 2	Mode 3	Mode 4	Level during & after Reset
P3	P30	RXD1	-	-	-	Hi-Z (high)
	P31	TXD1	-	-	-	
	P32	DMAREQZ1	-	-	CCS_MON1	
	P33	DMAACKZ1	-	-	CCS_MON2	
	P34	DMATCZ1	-	-	CCS_MON3	
	P35	CSISCK1	INTPZ22	CCM_IRLZ	-	
	P36	CSISI1	INTPZ23	CCS_FUSEZ	-	
	P37	CSISO1	INTPZ24	CCM_MSTZ	-	
P4	P40	A1/MA0	HA1	-	-	
	P41	WAITZ	HWAITZ	-	-	
	P42	SLEEPING	HERROUTZ	CCM_SDGCZ	-	
	P43	INTPZ11	HBUSCLK	-	-	
	P44	CSZ1	HPGCSZ	-	-	
	P45	CSISCK0	WAITZ1	-	-	
	P46	CSISI0	WAITZ2	-	-	
	P47	CSISO0	WAITZ3	-	-	
P5	P50	CSZ3	-	CCM_LNKRUNZ / CCS_LNKRUNZ	-	
	P51	CSZ2	-	CCM_RDLEDZ / CCS_RDLEDZ	-	
	P52	TIN3	TOUT3	CCS_SDGATEON	-	Hi-Z (Low)
	P53	CRXD0	CCS_RD	CCM_RD	-	Hi-Z (high)
	P54	CTXD0	CCS_SD	CCM_SD	-	
	P55	CRXD1	-	-	-	
	P56	CTXD1	CATRESTOUT	-	-	
	P57	TIN2	TOUT2	-	-	

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	Pin Name	Mode 1	Mode 2	Mode 3	Mode 4	Level during & after Reset
P6	P60	SCL0	-	-	-	Hi-Z
	P61	SDA0	-	-	-	
	P62	RTDMAREQZ	-	CCM_MDIN0	-	
	P63	RTDMAACKZ	-	CCM_MDIN1	-	
	P64	RTDMATCZ	-	CCM_MDIN2	-	
	P65	DMAREQZ0	-	CCM_MDIN3	-	
	P66	DMAACKZ0	-	-	-	
	P67	DMATCZ0	-	-	-	
P7	P70	CSICS00	P0DUPLEXLEDZ	CCS_STATION_NO_0 / CCM_SNIN0	-	
	P71	CSICS01	-	CCS_STATION_NO_1 / CCM_SNIN1	-	
	P72	CSICS10	P0SPEED100LEDZ	CCS_STATION_NO_2 / CCM_SNIN2	-	
	P73	CSICS11	P0SPEED10LEDZ	CCS_STATION_NO_3 / CCM_SNIN3	-	
	P74	INTPZ12	P1DUPLEXLEDZ	CCS_STATION_NO_4 / CCM_SNIN4	-	
	P75	INTPZ13	-	CCS_STATION_NO_5 / CCM_SNIN5	-	
	P76	INTPZ14	P1SPEED100LEDZ	CCS_STATION_NO_6 / CCM_SNIN6	-	
	P77	INTPZ15	P1SPEED10LEDZ	CCS_STATION_NO_7 / CCM_SNIN7	-	

RP0x to RP3x function as real-time ports which can transfer data via a dedicated DMA controller. They are able to input and output data in 32-bit units in synchronization with the DMA transfer trigger.

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	Pin Name	Mode 1	Mode 2	Mode 3	Mode 4	Level during & after Reset
RP0	RP00	INTPZ16	SCL1	CCM_SDLEDZ / CCS_SDLEDZ	-	Hi-Z (High)
	RP01	INTPZ17	SDA1	CCM_SMSTZ	-	
	RP02	INTPZ18	P0ACTLEDZ	CCS_BS1	-	
	RP03	INTPZ19	-	CCS_BS2	-	
	RP04	INTPZ20	P1ACTLEDZ	CCS_BS4	-	
	RP05	INTPZ21	-	CCS_BS8	-	
	RP06	WRZ2/BENZ2	HWRZ2/HBENZ2	-	-	
	RP07	WRZ3/BENZ3	HWRZ3/HBENZ3	-	-	
RP1	RP10	D24/MD24/HD24	-	-	-	
	RP11	D25/MD25/HD25	-	-	-	
	RP12	D26/MD26/HD26	-	-	-	
	RP13	D27/MD27/HD27	-	-	-	
	RP14	D28/MD28/HD28	-	-	-	
	RP15	D29/MD29/HD29	-	-	-	
	RP16	D30/MD30/HD30	-	-	-	
	RP17	D31/MD31/HD31	-	-	-	
RP2	RP20	BCYSTZ/ADVZ	HBCYSTZ	-	-	
	RP21	A21/MA20	-	-	-	Hi-Z (Low)
	RP22	A22/MA21	-	-	-	
	RP23	A23/MA22	-	-	-	
	RP24	A24/MA23	INTPZ25	-	-	
	RP25	A25/MA24	INTPZ26	-	-	
	RP26	A26/MA25	INTPZ27	-	-	
	RP27	A27/MA26	INTPZ28	-	-	
RP3	RP30	D16/MD16/HD16	-	-	-	Hi-Z (High)
	RP31	D17/MD17/HD17	-	-	-	
	RP32	D18/MD18/HD18	-	-	-	
	RP33	D19/MD19/HD19	-	-	-	
	RP34	D20/MD20/HD20	-	-	-	
	RP35	D21/MD21/HD21	-	-	-	
	RP36	D22/MD22/HD22	-	-	-	
	RP37	D23/MD23/HD23	-	-	-	

2.1.6 Serial Flash ROM Interface Pins

The serial flash ROM interface pins are pins of the serial flash ROM memory controller.
They support the fast read, fast read dual output, and fast read dual I/O modes.

Pin Name	I/O	Function	Shared Port	Active	Level during & after Reset
SMSCK	O	Serial clock output signal for serial flash ROM	P14	-	Hi-Z (High)
SMSI	I/O	Serial data I/O signal for serial flash ROM (connected to the SO pin of serial flash ROM)	P15	High	
SMSO	I/O	Serial data I/O signal for serial flash ROM (connected to the SI pin of serial flash ROM)	P16	High	
SMCSZ	O	Chip select output signal for serial flash ROM	P17	Low	

2.1.7 DMA Interface Pins

The DMA interface pins are external interface pins of the DMA controllers for the internal AHB bus.
As the external DMA interface, they control two types of DMA controllers incorporated in the R-IN32M3-EC; a general DMA controller for channel 0 and channel 1, and a DMA controller for real-time ports.

Pin Name	I/O	Function	Shared Port	Active	Level during & after Reset
RTDMAREQZ	I	RTDMAC DMA transfer request input	P62	Low	Hi-Z
RTDMAACKZ	O	RTDMAC DMA acknowledge output	P63	Low	
RTDMATCZ	O	RTDMAC terminal count output	P64	Low	
DMAREQZ0	I	DMA transfer request input 0	P65	Low	
DMAACKZ0	O	DMA acknowledge output 0	P66	Low	
DMATCZ0	O	Terminal count output 0	P67	Low	
DMAREQZ1	I	DMA transfer request input 1	P32	Low	Hi-Z (High)
DMAACKZ1	O	DMA acknowledge output 1	P33	Low	
DMATCZ1	O	Terminal count output port 1	P34	Low	

Caution: The DMA interface pin is fixed to the specific channel of the DMA controller, and not assigned to any other DMA controller or channel. For details, see section 13, DMA Controllers, in the R-IN32M3 Series User's Manual: Peripheral Modules.

2.1.8 External Interrupt Input Pins

The chip has one non-maskable interrupt and 29 maskable interrupt input pins.

Pin Name	I/O	Function	Shared Port	Active	Level during & after Reset
NMIZ	I	Non-maskable external interrupt input	-	Low	Hi-Z (High)
INTPZ0-INTPZ5	I	External interrupt input	P00-P05	Low	Hi-Z
INTPZ6, INTPZ7			P12, P13	Low	Hi-Z (High)
INTPZ8-INTPZ10			P22-P24	Low	Hi-Z
INTPZ11			P43	Low	Hi-Z (High)
INTPZ12-INTPZ15			P74-P77	Low	Hi-Z
INTPZ16-INTPZ21			RP00-RP05	Low	Hi-Z (High)
INTPZ22-INTPZ24			P35-P37		
INTPZ25-INTPZ28			RP24-RP27		Hi-Z (Low)

2.1.9 Timer I/O Pins

Pin Name	I/O	Function	Shared Port	Active	Level during & after Reset
TIN0 / TOUT0	I/O	Timer TAUJ0 I/O pin	P27	-	Hi-Z
TIN1 / TOUT1	I/O	Timer TAUJ1 I/O pin	P26	-	
TIN2 / TOUT2	I/O	Timer TAUJ2 I/O pin	P57	-	Hi-Z (High)
TIN3 / TOUT3	I/O	Timer TAUJ3 I/O pin	P52	-	Hi-Z (Low)

2.1.10 Watchdog Timer Output Pin

Pin Name	I/O	Function	Shared Port	Active	Level during & after Reset
WDTOUTZ	O	Watchdog timer output pin	P25	Low	Hi-Z

2.1.11 Trace Pins

Pin Name	I/O	Function	Active	Level during & after Reset
TRACECLK	O	Trace port clock output	-	Clock output
TRACEDATA3-TRACEDATA0	O	Trace port data output	-	Low

2.1.12 CPU Power Control Pin

Pin Name	I/O	Function	Shared Port	Active	Level during & after Reset
SLEEPING	O	CPU SLEEP mode output	P42	High	Hi-Z (High)

2.1.13 Serial Interface Pins

Pin Name	I/O	Function	Shared Port	Active	Level during & after Reset
TXD0	O	UART0 serial data output	P21	-	Hi-Z
RXD0	I	UART0 serial data input	P20	-	
TXD1	O	UART1 serial data output	P31	-	Hi-Z (High)
RXD1	I	UART1 serial data input	P30	-	
CSISCK0	I/O	CSI0 serial clock I/O	P45	-	
CSISI0	I	CSI0 serial data input	P46	-	
CSISO0	O	CSI0 serial data output	P47	-	
CSICS00, CSICS01	O	CSI0 chip select output 0, 1	P70, P71	Low	Hi-Z
CSISCK1	I/O	CSI1 serial clock I/O	P35	-	Hi-Z (High)
CSISI1	I	CSI1 serial data input	P36	-	
CSISO1	O	CSI1 serial data output	P37	-	
CSICS10, CSICS11	O	CSI1 chip select 0, 1	P72, P73	Low	Hi-Z
SCL0	I/O	I2C0 serial clock	P60	-	
SDA0	I/O	I2C0 serial data	P61	-	
SCL1	I/O	I2C1 serial clock	RP00	-	Hi-Z (High)
SDA1	I/O	I2C1 serial data	RP01	-	
CRXD0	I	CAN0 receive data input (5V-Tolerant buffer)	P53	-	
CTXD0	O	CAN0 transmit data output	P54	-	
CRXD1	I	CAN1 receive data input (5V-Tolerant buffer)	P55	-	
CTXD1	O	CAN1 transmit data output	P56	-	

2.1.14 CC-Link Pins (Intelligent Device Station)

Pin Name	I/O	Function	Shared Port	Active	Level during & after Reset
CCM_LINKERRZ	O	Link error LED control output	P20	Low	Hi-Z
CCM_ERRZ	O	Not used	P21	Low	
CCM_RUNZ	O	Run LED control output	P26	Low	
CCM_MDIN0-CCM_MDIN3	I	Transfer rate setting input	P62-P65	-	
CCM_SNIN0-CCM_SNIN7	I	Station no. setting switch input	P70-P77	-	
CCM_LNKRUNZ	O	Link run LED control output	P50	Low	Hi-Z (High)
CCM_RDLEDZ	O	Receive data LED control output	P51	Low	
CCM_SDLEDZ	O	Transmit data LED control output	RP00	Low	
CCM_IRLZ	O	Interrupt signal output from communications circuit	P35	Low	
CCM_WDTENZ	I	Watchdog timer error input	P13	Low	
CCM_MSTZ	O	Not used	P37	Low	
CCM_SMSTZ	O	Not used	RP01	Low	
CCM_RD	I	Communications circuit data reception pin	P53	-	
CCM_SD	O	Communications circuit data transmission pin	P54	-	
CCM_SDGCZ	O	Communications circuit transmit data & gate control pin	P42	Low	
CCM_CLK80M	I	CC-Link clock input (80 MHz)	-	-	-

2.1.15 CC-Link Pins (Remote Device Station)

Caution: To use a remote device station, it is necessary to connect a CCS_REFSTB (P10) pin to a port pin with the external interrupt function (INTPZ).

Pin Name	I/O	Function	Shared Port	Active	Level during & after Reset
CCS_MON0	O	Monitor signal	P06	-	Hi-Z
CCS_MON1-CCS_MON3	O	Monitor signal	P32-P34	-	Hi-Z (High)
CCS_MON4	O	Monitor signal	P11	-	Hi-Z (Low)
CCS_MON5-CCS_MON7	O	Monitor signal	P03-P05	-	Hi-Z
CCS_RESOUT	O	Reset output signal	P07	High	
CCS_IOTENSU	I	Initial setting pin	P22	-	
CCS_SENYU0	I	Initial setting pin	P23	-	
CCS_SENYU1	I	Initial setting pin	P24	-	
CCS_ERRZ	O	Operation check LED	P25	Low	
CCS_RUNZ	O	Operation check LED	P26	Low	
CCS_STATION_NO_0-CCS_STATION_NO_7	I	Station no. setting switch input	P70-P77	-	
CCS_LNKRUNZ	O	Link run LED control output	P50	Low	Hi-Z (High)
CCS_REFSTB	O	Interrupt signal	P10	High	
CCS_WDTZ	I	Watchdog timer input	P13	Low	
CCS_RDLEDZ	O	Receive data LED control output	P51	Low	
CCS_RD	I	Communications circuit data reception pin	P53	-	
CCS_SD	O	Communications circuit data transmission pin	P54	-	
CCS_SDLEDZ	O	Operation check LED	RP00	Low	
CCS_SDGATEON	O	Communications circuit transmit data & gate control pin	P52	High	Hi-Z (Low)
CCS_BS1	I	Baud rate setting switch input pin	RP02	-	Hi-Z (High)
CCS_BS2	I	Baud rate setting switch input pin	RP03	-	
CCS_BS4	I	Baud rate setting switch input pin	RP04	-	
CCS_BS8	I	Baud rate setting switch input pin	RP05	-	
CCS_FUSEZ	I	Fuse cutting input signal	P36	Low	
CCM_CLK80M Note	I	CC-Link clock input (80 MHz)	-	-	-

Note: This pin is shared with CC-Link (intelligent device station).

2.1.16 System Pins

Pin Name	I/O	Function	Active	Level during & after Reset
XT1	I	Clock input pins	-	-
XT2	I/O	OSCTH = 1: Oscillator is in use. XT1 and XT2 are respectively connected to GND and oscillator. OSCTH = 0: Resonator is in use. XT1 and XT2 are connected to resonator	-	-
RESETZ	I	Reset input	Low	-
PONRZ	I	Power on reset input	Low	-
OSCTH	I	External clock input mode setting 0: Resonator using mode 1: External clock input mode	High	-
JTAGSEL	I	JTAG pin operating mode setting 0: Cortex-M3 JTAG mode 1: B-SCAN JTAG mode	-	-
RSTOUTZ	O	External reset output	Low	Low (after reset: High)
PLL_VDD	-	PLL power supply (1.0 V)	-	-
PLL_GND	-	PLL ground level (GND)	-	-
VDD33	-	I/O power supply (3.3 V)	-	-
VDD10	-	Internal power supply (1.0 V)	-	-
GND	-	Ground level (GND)	-	-
LX	O	1.5-V output for on-chip regulator	-	-
EXTRES	-	Reference resistor connecting pin for on-chip PHY	-	-
P0VDDARXTX	-	Analog power supply for Rx/Tx pin (1.5 V) - port 0	-	-
P1VDDARXTX	-	Analog power supply for Rx/Tx pin (1.5 V) - port 1	-	-
VDDACB	-	Analog power supply for on-chip PHY (3.3 V)	-	-
AGND	-	Analog ground level for on-chip PHY (GND)	-	-
VDD15	-	I/O power supply for on-chip PHY (1.5 V)	-	-
VDDAPLL	-	Analog core power supply for on-chip PHY (1.5V)	-	-
VSSAPLLCB	-	Analog core ground level for on-chip PHY (GND)	-	-
VDD33ESD	-	Analog test power supply for on-chip PHY (3.3 V)	-	-
AVDD_REG	-	Analog power supply for on-chip regulator (3.3 V)	-	-
AGND_REG	-	Analog ground level for on-chip regulator (GND)	-	-
BVDD	-	Power supply for on-chip regulator (3.3 V)	-	-
BGND	-	Ground level for on-chip regulator (GND)	-	-
FB	I	Feedback input for on-chip regulator	-	-
VDDQ_PECL_B0	-	PECL buffer power supply (3.3 V)	-	-
VDDQ_PECL_B1	-	PECL buffer power supply (3.3 V)	-	-

2.1.17 Test Pins

Pin Name	I/O	Function	Active	Level during & after Reset
TMODE0-TMODE2	I	Test mode select pin	-	-
TMS	I/O	Mode select signal	-	-
TDI	I	Serial data input	-	-
TDO	O	Serial data output	-	-
TRSTZ	I	Reset signal	Low	-
TCK	I	Clock signal (JTAG clock)	-	-
TMC1	I	Renesas test pins	-	-
TMC2	I		-	-
ATP	I			
TEST1	I		-	-
TEST2	I		-	-
TEST3	I		-	-
TESTOUT5	O		-	-

2.1.18 Operating Mode Setting Pins

Pin Name	I/O	Function	Active	Level during & after Reset
BOOT1-BOOT0	I	Boot mode select 00: External memory boot 01: External serial flash ROM boot 10: External MPU boot 11: Instruction RAM boot (only available for debugging)	-	-
MEMIFSEL	I	External memory interface select 0: Slave memory interface 1: External MCU interface	-	-
BUS32EN	I	External memory interface bus width select 0: 16-bit bus 1: 32-bit bus	-	-
HIFSYNC	I	External MCU interface operating mode 0: Asynchronous SRAM interface 1: Synchronous SRAM interface	-	-
HWRZSEL	I	External MCU interface HWRZ/HBENZ select 0: Used as HBENZ 1: Used as HWRZ	-	-
MEMCSEL	I	Internal memory controller select 0: Asynchronous SRAM MEMC 1: Synchronous burst access MEMC	-	-
ADMUXMODE	I	Multiplexing of address and data lines 0: Separate address and data lines 1: Multiplexed address and data lines	-	-

The combinations of available operating mode setting pins in this product are as follows.

Boot Mode	External Memory Boot				External MCU Boot				External Serial Flash ROM Boot							
External Memory Interface	Slave Memory Interface				External MCU Interface				Slave Memory Interface				External MCU Interface			
MEMC Type	Asynchronous		Synchronous		Asynchronous		Synchronous		Asynchronous		Synchronous		Asynchronous		Synchronous	
External Bus Width	16-bit	32-bit	16-bit	32-bit	16-bit	32-bit	16-bit	32-bit	16-bit	32-bit	16-bit	32-bit	16-bit	32-bit	16-bit	32-bit
BOOT1-0	00	00	00	00	10	10	10	10	01	01	01	01	01	01	01	01
MEMIFSEL	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
MEMCSEL	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
BUS32EN	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
HIFSYNC	0	0	0	0	Note1	Note1	1	1	0	0	0	0	Note1	Note1	1	1
HWRZSEL	0	0	0	0	Note2	Note2	0	0	0	0	0	0	Note2	Note2	0	0
ADMUXMODE	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1

Caution: Any combination of operating mode setting pins other than the above is prohibited.

Notes 1. The mode of the external MCU interface is selectable by the level on the HIFSYNC pin.
HIFSYNC = 0: Asynchronous SRAM interface mode
HIFSYNC = 1: Synchronous SRAM interface mode
For details, see section 11, External MCU Interface, in the R-IN32M3 Series User's Manual (Peripheral Modules).
2. The external MCU interface HWRZ or HBENZ is selectable by the level on the HWRZSEL pin.
For details, see section 2.1.3.1, External MCU Interface Pins.

Remarks 1. The combination of operating-mode setting pins used to select booting for instruction RAM (BOOT1-0 = 11) is the same as that for booting from external memory (BOOT1-0 = 00).
2. Asynchronous: Asynchronous SRAM memory controller (MEMCSEL = 0)
Synchronous: Synchronous burst access memory controller (MEMCSEL = 1)

2.2 Pin States

The initial state of the port functions after release from the reset state differs depending on the state of the operating mode setting pins. For the state of the operating mode setting pins in each boot mode and the supported combinations, see section 2.1.18, Operating Mode Setting Pins.

Remarks 1. Entries in cells shaded in light green indicate multiplexed pin functions that are enabled in the initial state.

2. The initial state of booting for instruction RAM is the same as that for booting from external memory.

2.2.1 Pin States when Booting is from External Memory

Pin Name	External Memory Boot (BOOT1-0 = 00)			
	Slave Memory Interface (MEMIFSEL = 0)			
	Asynchronous SRAM Memory Controller (MEMCSEL = 0)		Synchronous Burst Access Memory Controller (MEMCSEL = 1)	
	16-bit (BUS32EN = 0)	32-bit (BUS32EN = 1)	16-bit (BUS32EN = 0)	32-bit (BUS32EN = 1)
P00	P00	P00	P00	P00
P01	P01	P01	P01	P01
P02	P02	P02	P02	P02
P03	P03	P03	P03	P03
P04	P04	P04	P04	P04
P05	P05	P05	P05	P05
P06	P06	P06	P06	P06
P07	P07	P07	P07	P07
P10	P10	P10	P10	P10
P11	P11	P11	P11	P11
P12	P12	P12	P12	P12
P13	P13	P13	P13	P13
P14	P14	P14	P14	P14
P15	P15	P15	P15	P15
P16	P16	P16	P16	P16
P17	P17	P17	P17	P17
P20	P20	P20	P20	P20
P21	P21	P21	P21	P21
P22	P22	P22	P22	P22
P23	P23	P23	P23	P23
P24	P24	P24	P24	P24
P25	P25	P25	P25	P25
P26	P26	P26	P26	P26
P27	P27	P27	P27	P27
P30	P30	P30	P30	P30
P31	P31	P31	P31	P31
P32	P32	P32	P32	P32
P33	P33	P33	P33	P33
P34	P34	P34	P34	P34
P35	P35	P35	P35	P35
P36	P36	P36	P36	P36
P37	P37	P37	P37	P37

Pin Name	External Memory Boot (BOOT1-0 = 00)			
	Slave Memory Interface (MEMIFSEL = 0)			
	Asynchronous SRAM Memory Controller (MEMCSEL = 0)		Synchronous Burst Access Memory Controller (MEMCSEL = 1)	
	16-bit (BUS32EN = 0)	32-bit (BUS32EN = 1)	16-bit (BUS32EN = 0)	32-bit (BUS32EN = 1)
P40	A1	P40	MA0	MA0
P41	P41	P41	P41	P41
P42	P42	P42	P42	P42
P43	P43	P43	P43	P43
P44	P44	P44	P44	P44
P45	P45	P45	P45	P45
P46	P46	P46	P46	P46
P47	P47	P47	P47	P47
P50	P50	P50	P50	P50
P51	P51	P51	P51	P51
P52	P52	P52	P52	P52
P53	P53	P53	P53	P53
P54	P54	P54	P54	P54
P55	P55	P55	P55	P55
P56	P56	P56	P56	P56
P57	P57	P57	P57	P57
P60	P60	P60	P60	P60
P61	P61	P61	P61	P61
P62	P62	P62	P62	P62
P63	P63	P63	P63	P63
P64	P64	P64	P64	P64
P65	P65	P65	P65	P65
P66	P66	P66	P66	P66
P67	P67	P67	P67	P67
P70	P70	P70	P70	P70
P71	P71	P71	P71	P71
P72	P72	P72	P72	P72
P73	P73	P73	P73	P73
P74	P74	P74	P74	P74
P75	P75	P75	P75	P75
P76	P76	P76	P76	P76
P77	P77	P77	P77	P77

Pin Name	External Memory Boot (BOOT1-0 = 00)			
	Slave Memory Interface (MEMIFSEL = 0)			
	Asynchronous SRAM Memory Controller (MEMCSEL = 0)		Synchronous Burst Access Memory Controller (MEMCSEL = 1)	
	16-bit (BUS32EN = 0)	32-bit (BUS32EN = 1)	16-bit (BUS32EN = 0)	32-bit (BUS32EN = 1)
RP00	RP00	RP00	RP00	RP00
RP01	RP01	RP01	RP01	RP01
RP02	RP02	RP02	RP02	RP02
RP03	RP03	RP03	RP03	RP03
RP04	RP04	RP04	RP04	RP04
RP05	RP05	RP05	RP05	RP05
RP06	RP06	WRZ2	RP06	WRZ2
RP07	RP07	WRZ3	RP07	WRZ3
RP10	RP10	D24	RP10	MD24
RP11	RP11	D25	RP11	MD25
RP12	RP12	D26	RP12	MD26
RP13	RP13	D27	RP13	MD27
RP14	RP14	D28	RP14	MD28
RP15	RP15	D29	RP15	MD29
RP16	RP16	D30	RP16	MD30
RP17	RP17	D31	RP17	MD31
RP20	RP20	RP20	RP20	RP20
RP21	RP21	RP21	RP21	RP21
RP22	RP22	RP22	RP22	RP22
RP23	RP23	RP23	RP23	RP23
RP24	RP24	RP24	RP24	RP24
RP25	RP25	RP25	RP25	RP25
RP26	RP26	RP26	RP26	RP26
RP27	RP27	RP27	RP27	RP27
RP30	RP30	D16	RP30	MD16
RP31	RP31	D17	RP31	MD17
RP32	RP32	D18	RP32	MD18
RP33	RP33	D19	RP33	MD19
RP34	RP34	D20	RP34	MD20
RP35	RP35	D21	RP35	MD21
RP36	RP36	D22	RP36	MD22
RP37	RP37	D23	RP37	MD23

2.2.2 Pin States when Booting is from External Serial Flash ROM

Remarks 1. Asynchronous type: Asynchronous SRAM memory controller (MEMCSEL = 0)
Synchronous type: Synchronous burst access memory controller (MEMCSEL = 1)
2. 16-bit: 16-bit bus width of the external memory interface (BUS32EN = 0)
32-bit: 32-bit bus width of the external memory interface (BUS32EN = 1)

	External Serial Flash ROM Boot (BOOT1-0 = 01)							
	Slave Memory Interface (MEMIFSEL = 0)				External MCU Interface (MEMIFSEL = 1)			
	Asynchronous Type		Synchronous Type		Asynchronous Type		Synchronous type	
Pin Name	16-bit	32-bit	16-bit	32-bit	16-bit	32-bit	16-bit	32-bit
P00	P00	P00	P00	P00	P00	P00	P00	P00
P01	P01	P01	P01	P01	P01	P01	P01	P01
P02	P02	P02	P02	P02	P02	P02	P02	P02
P03	P03	P03	P03	P03	P03	P03	P03	P03
P04	P04	P04	P04	P04	P04	P04	P04	P04
P05	P05	P05	P05	P05	P05	P05	P05	P05
P06	P06	P06	P06	P06	P06	P06	P06	P06
P07	P07	P07	P07	P07	P07	P07	P07	P07
P10	P10	P10	P10	P10	P10	P10	P10	P10
P11	P11	P11	P11	P11	P11	P11	P11	P11
P12	P12	P12	P12	P12	P12	P12	P12	P12
P13	P13	P13	P13	P13	P13	P13	P13	P13
P14	SMSCK	SMSCK	SMSCK	SMSCK	SMSCK	SMSCK	SMSCK	SMSCK
P15	SMSI	SMSI	SMSI	SMSI	SMSI	SMSI	SMSI	SMSI
P16	SMSO	SMSO	SMSO	SMSO	SMSO	SMSO	SMSO	SMSO
P17	SMCSZ	SMCSZ	SMCSZ	SMCSZ	SMCSZ	SMCSZ	SMCSZ	SMCSZ
P20	P20	P20	P20	P20	P20	P20	P20	P20
P21	P21	P21	P21	P21	P21	P21	P21	P21
P22	P22	P22	P22	P22	P22	P22	P22	P22
P23	P23	P23	P23	P23	P23	P23	P23	P23
P24	P24	P24	P24	P24	P24	P24	P24	P24
P25	P25	P25	P25	P25	P25	P25	P25	P25
P26	P26	P26	P26	P26	P26	P26	P26	P26
P27	P27	P27	P27	P27	P27	P27	P27	P27
P30	P30	P30	P30	P30	P30	P30	P30	P30
P31	P31	P31	P31	P31	P31	P31	P31	P31
P32	P32	P32	P32	P32	P32	P32	P32	P32
P33	P33	P33	P33	P33	P33	P33	P33	P33
P34	P34	P34	P34	P34	P34	P34	P34	P34
P35	P35	P35	P35	P35	P35	P35	P35	P35
P36	P36	P36	P36	P36	P36	P36	P36	P36
P37	P37	P37	P37	P37	P37	P37	P37	P37

Pin Name	External Serial Flash ROM Boot (BOOT1-0 = 01)							
	Slave Memory Interface (MEMIFSEL = 0)				External MCU Interface (MEMIFSEL = 1)			
	Asynchronous Type		Synchronous Type		Asynchronous Type		Synchronous type	
	16-bit	32-bit	16-bit	32-bit	16-bit	32-bit	16-bit	32-bit
P40	A1	P40	MA0	MA0	HA1	P40	HA1	HA1
P41	P41	P41	P41	P41	HWAITZ	HWAITZ	HWAITZ	HWAITZ
P42	P42	P42	P42	P42	HERROUTZ	HERROUTZ	HERROUTZ	HERROUTZ
P43	P43	P43	P43	P43	HBUSCLK	HBUSCLK	HBUSCLK	HBUSCLK
P44	P44	P44	P44	P44	HPGCSZ	HPGCSZ	HPGCSZ	HPGCSZ
P45	P45	P45	P45	P45	P45	P45	P45	P45
P46	P46	P46	P46	P46	P46	P46	P46	P46
P47	P47	P47	P47	P47	P47	P47	P47	P47
P50	P50	P50	P50	P50	P50	P50	P50	P50
P51	P51	P51	P51	P51	P51	P51	P51	P51
P52	P52	P52	P52	P52	P52	P52	P52	P52
P53	P53	P53	P53	P53	P53	P53	P53	P53
P54	P54	P54	P54	P54	P54	P54	P54	P54
P55	P55	P55	P55	P55	P55	P55	P55	P55
P56	P56	P56	P56	P56	P56	P56	P56	P56
P57	P57	P57	P57	P57	P57	P57	P57	P57
P60	P60	P60	P60	P60	P60	P60	P60	P60
P61	P61	P61	P61	P61	P61	P61	P61	P61
P62	P62	P62	P62	P62	P62	P62	P62	P62
P63	P63	P63	P63	P63	P63	P63	P63	P63
P64	P64	P64	P64	P64	P64	P64	P64	P64
P65	P65	P65	P65	P65	P65	P65	P65	P65
P66	P66	P66	P66	P66	P66	P66	P66	P66
P67	P67	P67	P67	P67	P67	P67	P67	P67
P70	P70	P70	P70	P70	P70	P70	P70	P70
P71	P71	P71	P71	P71	P71	P71	P71	P71
P72	P72	P72	P72	P72	P72	P72	P72	P72
P73	P73	P73	P73	P73	P73	P73	P73	P73
P74	P74	P74	P74	P74	P74	P74	P74	P74
P75	P75	P75	P75	P75	P75	P75	P75	P75
P76	P76	P76	P76	P76	P76	P76	P76	P76
P77	P77	P77	P77	P77	P77	P77	P77	P77

Pin Name	External Serial Flash ROM Boot (BOOT1-0 = 01)							
	Slave Memory Interface (MEMIFSEL = 0)				External MCU Interface (MEMIFSEL = 1)			
	Asynchronous Type		Synchronous Type		Asynchronous Type		Synchronous type	
	16-bit	32-bit	16-bit	32-bit	16-bit	32-bit	16-bit	32-bit
RP00	RP00	RP00	RP00	RP00	RP00	RP00	RP00	RP00
RP01	RP01	RP01	RP01	RP01	RP01	RP01	RP01	RP01
RP02	RP02	RP02	RP02	RP02	RP02	RP02	RP02	RP02
RP03	RP03	RP03	RP03	RP03	RP03	RP03	RP03	RP03
RP04	RP04	RP04	RP04	RP04	RP04	RP04	RP04	RP04
RP05	RP05	RP05	RP05	RP05	RP05	RP05	RP05	RP05
RP06	RP06	WRZ2	RP06	WRZ2	RP06	HWRZ2	RP06	HWRZ2
RP07	RP07	WRZ3	RP07	WRZ3	RP07	HWRZ3	RP07	HWRZ3
RP10	RP10	D24	RP10	MD24	RP10	HD24	RP10	HD24
RP11	RP11	D25	RP11	MD25	RP11	HD25	RP11	HD25
RP12	RP12	D26	RP12	MD26	RP12	HD26	RP12	HD26
RP13	RP13	D27	RP13	MD27	RP13	HD27	RP13	HD27
RP14	RP14	D28	RP14	MD28	RP14	HD28	RP14	HD28
RP15	RP15	D29	RP15	MD29	RP15	HD29	RP15	HD29
RP16	RP16	D30	RP16	MD30	RP16	HD30	RP16	HD30
RP17	RP17	D31	RP17	MD31	RP17	HD31	RP17	HD31
RP20	RP20	RP20	ADVZ	ADVZ	HBCYSTZ	HBCYSTZ	HBCYSTZ	HBCYSTZ
RP21	RP21	RP21	RP21	RP21	RP21	RP21	RP21	RP21
RP22	RP22	RP22	RP22	RP22	RP22	RP22	RP22	RP22
RP23	RP23	RP23	RP23	RP23	RP23	RP23	RP23	RP23
RP24	RP24	RP24	RP24	RP24	RP24	RP24	RP24	RP24
RP25	RP25	RP25	RP25	RP25	RP25	RP25	RP25	RP25
RP26	RP26	RP26	RP26	RP26	RP26	RP26	RP26	RP26
RP27	RP27	RP27	RP27	RP27	RP27	RP27	RP27	RP27
RP30	RP30	D16	RP30	MD16	RP30	HD16	RP30	HD16
RP31	RP31	D17	RP31	MD17	RP31	HD17	RP31	HD17
RP32	RP32	D18	RP32	MD18	RP32	HD18	RP32	HD18
RP33	RP33	D19	RP33	MD19	RP33	HD19	RP33	HD19
RP34	RP34	D20	RP34	MD20	RP34	HD20	RP34	HD20
RP35	RP35	D21	RP35	MD21	RP35	HD21	RP35	HD21
RP36	RP36	D22	RP36	MD22	RP36	HD22	RP36	HD22
RP37	RP37	D23	RP37	MD23	RP37	HD23	RP37	HD23

2.2.3 Pin States when Booting is for External MCU

Pin Name	External MCU Boot (BOOT1-0 = 10)			
	External MCU Interface (MEMIFSEL = 1)			
	Asynchronous SRAM memory controller (MEMCSEL = 0)		Synchronous burst access memory controller (MEMCSEL = 1)	
	16-bit (BUS32EN = 0)	32-bit (BUS32EN = 1)	16-bit (BUS32EN = 0)	32-bit (BUS32EN = 1)
P00	P00	P00	P00	P00
P01	P01	P01	P01	P01
P02	P02	P02	P02	P02
P03	P03	P03	P03	P03
P04	P04	P04	P04	P04
P05	P05	P05	P05	P05
P06	P06	P06	P06	P06
P07	P07	P07	P07	P07
P10	P10	P10	P10	P10
P11	P11	P11	P11	P11
P12	P12	P12	P12	P12
P13	P13	P13	P13	P13
P14	P14	P14	P14	P14
P15	P15	P15	P15	P15
P16	P16	P16	P16	P16
P17	P17	P17	P17	P17
P20	P20	P20	P20	P20
P21	P21	P21	P21	P21
P22	P22	P22	P22	P22
P23	P23	P23	P23	P23
P24	P24	P24	P24	P24
P25	P25	P25	P25	P25
P26	P26	P26	P26	P26
P27	P27	P27	P27	P27
P30	P30	P30	P30	P30
P31	P31	P31	P31	P31
P32	P32	P32	P32	P32
P33	P33	P33	P33	P33
P34	P34	P34	P34	P34
P35	P35	P35	P35	P35
P36	P36	P36	P36	P36
P37	P37	P37	P37	P37

Pin Name	External MCU Boot (BOOT1-0 = 10)			
	External MCU Interface (MEMIFSEL = 1)			
	Asynchronous SRAM memory controller (MEMCSEL = 0)		Synchronous burst access memory controller (MEMCSEL = 1)	
	16-bit (BUS32EN = 0)	32-bit (BUS32EN = 1)	16-bit (BUS32EN = 0)	32-bit (BUS32EN = 1)
P40	HA1	P40	HA1	HA1
P41	HWAITZ	HWAITZ	HWAITZ	HWAITZ
P42	HERROUTZ	HERROUTZ	HERROUTZ	HERROUTZ
P43	HBUSCLK	HBUSCLK	HBUSCLK	HBUSCLK
P44	HPGCSZ	HPGCSZ	HPGCSZ	HPGCSZ
P45	P45	P45	P45	P45
P46	P46	P46	P46	P46
P47	P47	P47	P47	P47
P50	P50	P50	P50	P50
P51	P51	P51	P51	P51
P52	P52	P52	P52	P52
P53	P53	P53	P53	P53
P54	P54	P54	P54	P54
P55	P55	P55	P55	P55
P56	P56	P56	P56	P56
P57	P57	P57	P57	P57
P60	P60	P60	P60	P60
P61	P61	P61	P61	P61
P62	P62	P62	P62	P62
P63	P63	P63	P63	P63
P64	P64	P64	P64	P64
P65	P65	P65	P65	P65
P66	P66	P66	P66	P66
P67	P67	P67	P67	P67
P70	P70	P70	P70	P70
P71	P71	P71	P71	P71
P72	P72	P72	P72	P72
P73	P73	P73	P73	P73
P74	P74	P74	P74	P74
P75	P75	P75	P75	P75
P76	P76	P76	P76	P76
P77	P77	P77	P77	P77

Pin Name	External MCU Boot (BOOT1-0 = 10) External MCU Interface (MEMIFSEL = 1) Asynchronous SRAM memory controller (MEMCSEL = 0) 16-bit (BUS32EN = 0)	External MCU Boot (BOOT1-0 = 10) External MCU Interface (MEMIFSEL = 1) Asynchronous SRAM memory controller (MEMCSEL = 0) 32-bit (BUS32EN = 1)	External MCU Boot (BOOT1-0 = 10) External MCU Interface (MEMIFSEL = 1) Synchronous burst access memory controller (MEMCSEL = 1) 16-bit (BUS32EN = 0)	External MCU Boot (BOOT1-0 = 10) External MCU Interface (MEMIFSEL = 1) Synchronous burst access memory controller (MEMCSEL = 1) 32-bit (BUS32EN = 1)
RP00	RP00	RP00	RP00	RP00
RP01	RP01	RP01	RP01	RP01
RP02	RP02	RP02	RP02	RP02
RP03	RP03	RP03	RP03	RP03
RP04	RP04	RP04	RP04	RP04
RP05	RP05	RP05	RP05	RP05
RP06	RP06	HWRZ2	RP06	HWRZ2
RP07	RP07	HWRZ3	RP07	HWRZ3
RP10	RP10	HD24	RP10	HD24
RP11	RP11	HD25	RP11	HD25
RP12	RP12	HD26	RP12	HD26
RP13	RP13	HD27	RP13	HD27
RP14	RP14	HD28	RP14	HD28
RP15	RP15	HD29	RP15	HD29
RP16	RP16	HD30	RP16	HD30
RP17	RP17	HD31	RP17	HD31
RP20	HBCYSTZ	HBCYSTZ	HBCYSTZ	HBCYSTZ
RP21	RP21	RP21	RP21	RP21
RP22	RP22	RP22	RP22	RP22
RP23	RP23	RP23	RP23	RP23
RP24	RP24	RP24	RP24	RP24
RP25	RP25	RP25	RP25	RP25
RP26	RP26	RP26	RP26	RP26
RP27	RP27	RP27	RP27	RP27
RP30	RP30	HD16	RP30	HD16
RP31	RP31	HD17	RP31	HD17
RP32	RP32	HD18	RP32	HD18
RP33	RP33	HD19	RP33	HD19
RP34	RP34	HD20	RP34	HD20
RP35	RP35	HD21	RP35	HD21
RP36	RP36	HD22	RP36	HD22
RP37	RP37	HD23	RP37	HD23

2.3 Buffer Types and Handling of Unused Pins

2.3.1 Ethernet Pins

(1) Media Interface Pins

Pin Name	I/O	Interface	Recommended Connection when Not in Use
P0_RX_P	I	3.3-V analog input buffer	Open
P0_RX_N	I		
P1_RX_P	I		
P1_RX_N	I		
P0_TX_P	O	3.3-V analog output buffer	Open
P0_TX_N	O		
P1_TX_P	O		
P1_TXN	O		
P0_SD_P	I	3.3-V PECL input buffer	Connect to GND
P0_SD_N	I		
P1_SD_P	I		
P1_SD_N	I		
P0_RD_P	I		
P0_RD_N	I		
P1_RD_P	I		
P1_RD_N	I		
P0_TD_OUT_P	O	3.3-V PECL output buffer	Open
P0_TD_OUT_N	O		
P1_TD_OUT_P	O		
P1_TD_OUT_N	O		
P0_FX_EN_OUT	O	Output buffer (3.3 V) 12 mA	Open
P1_FX_EN_OUT	O		

2.3.2 External Memory/MCU Interface Pins

Pin Name	I/O	Interface	Recommended Connection when Not in Use
BUSCLK	O	Output buffer (3.3 V) 9 mA	Open
CSZ0 / HCSZ	I/O	I/O buffer (3.3 V) 6 mA 50kΩ pull-up	Open
A2-A20 / HA2-HA20	I/O	I/O buffer (3.3 V) 6 mA 50kΩ pull-down	Open
D0-D15 / HD0-HD15			
RDZ / HRDZ	I/O	I/O buffer (3.3 V) 6 mA 50kΩ pull-up	Open
WRSTBZ / HWRSTBZ			
WRZ0, WRZ1 / BENZ0, BENZ1 / HWRZ0, HWRZ1			

2.3.3 External Interrupt Input Pins

Pin Name	I/O	Interface	Recommended Connection when Not in Use
NMIZ	I	Input buffer (3.3 V) Schmitt in, 50kΩ pull-up	Connect to VDD33 (3.3 V)

2.3.4 System Pins

Pin Name	I/O	Interface	Recommended Connection when Not in Use
XT1	I	Oscillator with EN	Note
XT2	I/O		Note
RSTOUTZ	O	Output buffer (3.3 V) 6 mA	Open
RESETZ	I	Input buffer (3.3 V) Schmitt in	Connect a reset signal since these pins are always used
PONRZ			
OSCTH	I	Input buffer (3.3 V) Schmitt in, 50kΩ pull-down	Set these pins according to the operating mode
JTAGSEL			

Note: The pin connection differs depending on the setting of the OSCTH pin.
For details, see the R-IN32M3 Series User's Manual (Board design edition).

2.3.5 Test Pins

Pin Name	I/O	Interface	Required Connection when Not in Use
TMODE0-TMODE2	I	Input buffer (3.3 V) Schmitt in, 50kΩ pull-down	Connect to GND
TMS	I/O	I/O buffer (3.3 V) 6 mA 50kΩ pull-up	Open
TDI	I	Input buffer (3.3 V), 50kΩ pull-up	Open
TDO	O	3-state output buffer (3.3 V) 6 mA	Open
TRSTZ	I	Input buffer (3.3 V) Schmitt in, 50kΩ pull-up	Open
TCK	I	Input buffer (3.3 V), 50kΩ pull-down	Open
TMC1	I	(TMC1) input buffer (3.3 V) for TMC terminal	Connect to GND
TMC2	I	(TMC2) input buffer (3.3 V) for TMC terminal	Connect to GND
ATP	I	Input buffer (3.3 V)	Open
TEST1	I	Input buffer (3.3 V)	Note
TEST2	I	Input buffer (3.3 V)	
TEST3	I	Input buffer (3.3 V)	
TESTDOUT5	O	Output buffer (3.3 V)	Open

Note: The procedure differs depending on whether the regulator in R-IN32M3-EC is used or not. For details, refer to Section 5 Built-in Regulator Pin (R-IN32M3-EC only in the R-IN32M3 Series User's Manual: Board design edition.

2.3.6 Port Pins

Pin Name	I/O	Interface	Recommended connection when Not in Use
P00-P07	I/O	I/O buffer (3.3 V) (6 mA)	Connect to GND
P10	I/O	Programmable I/O buffer (3.3 V) (6 mA) Resistor select function (50kΩ pull-up or 50kΩ pull-down or less)	Open
P11-P17	I/O	Programmable I/O buffer (3.3 V) (6 mA) Resistor select function (50kΩ pull-up or 50kΩ pull-down or less)	
P20-P27	I/O	I/O buffer (3.3 V) (6 mA)	Connect to GND
P30-P36	I/O	Programmable I/O buffer (3.3 V) (6 mA) Resistor select function (50kΩ pull-up or 50kΩ pull-down or less)	Open
P37	I/O	Programmable I/O buffer (3.3 V) Load drive select function (6 mA, 12 mA) Resistor select function (50kΩ pull-up or 50kΩ pull-down or less)	
P40-P47	I/O	Programmable I/O buffer (3.3 V) (6 mA) Resistor select function (50kΩ pull-up or 50kΩ pull-down or less)	
P50, P51	I/O	Programmable I/O buffer (3.3 V) Load drive select function (6 mA, 12 mA) Resistor select function (50kΩ pull-up or 50kΩ pull-down or less)	
P52	I/O	Programmable I/O buffer (3.3 V) (6 mA) Resistor select function (50kΩ pull-up or 50kΩ pull-down or less)	
P53-P56	I/O	5V-tolerant I/O buffer 4 mA 50kΩ pull-up	Open
P57	I/O	Programmable I/O buffer (3.3 V) (6 mA) Resistor select function (50kΩ pull-up or 50kΩ pull-down or less)	Open
P60-P67	I/O	I/O buffer (3.3 V) (6 mA)	Connect to GND
P70-P77	I/O	I/O buffer (3.3 V) (6 mA)	Connect to GND
RP00-RP07	I/O	Programmable I/O buffer (3.3 V) Load drive select function (6 mA, 12 mA) Resistor select function (50kΩ pull-up or 50kΩ pull-down or less)	Open
RP10-RP17			
RP20-RP27			
RP30-RP37			

2.3.7 Operation Mode Setting Pins

Pin Name	I/O	Interface	Recommended Connection when not in Use
BOOT0, BOOT1	I	Input buffer (3.3 V) Schmitt in	Set these pins according to the operating mode
MEMIFSEL			
BUS32EN			
HIFSYNC			
HWRZSEL			
MEMCSEL			
ADMUXMODE			

2.3.8 CC-Link Pin (Intelligent Device Station, Remote Device Station)

Pin Name	I/O	Interface	Recommended Connection when Not in Use
CCM_CLK80M	I	Input buffer (3.3 V)	Connect to GND

2.3.9 Trace Pins

Pin Name	I/O	Interface	Recommended Connection when Not in Use
TRACECLK	O	Output buffer (3.3 V) 6 mA	Open
TRACEDATA0-3			

3. Memory Maps

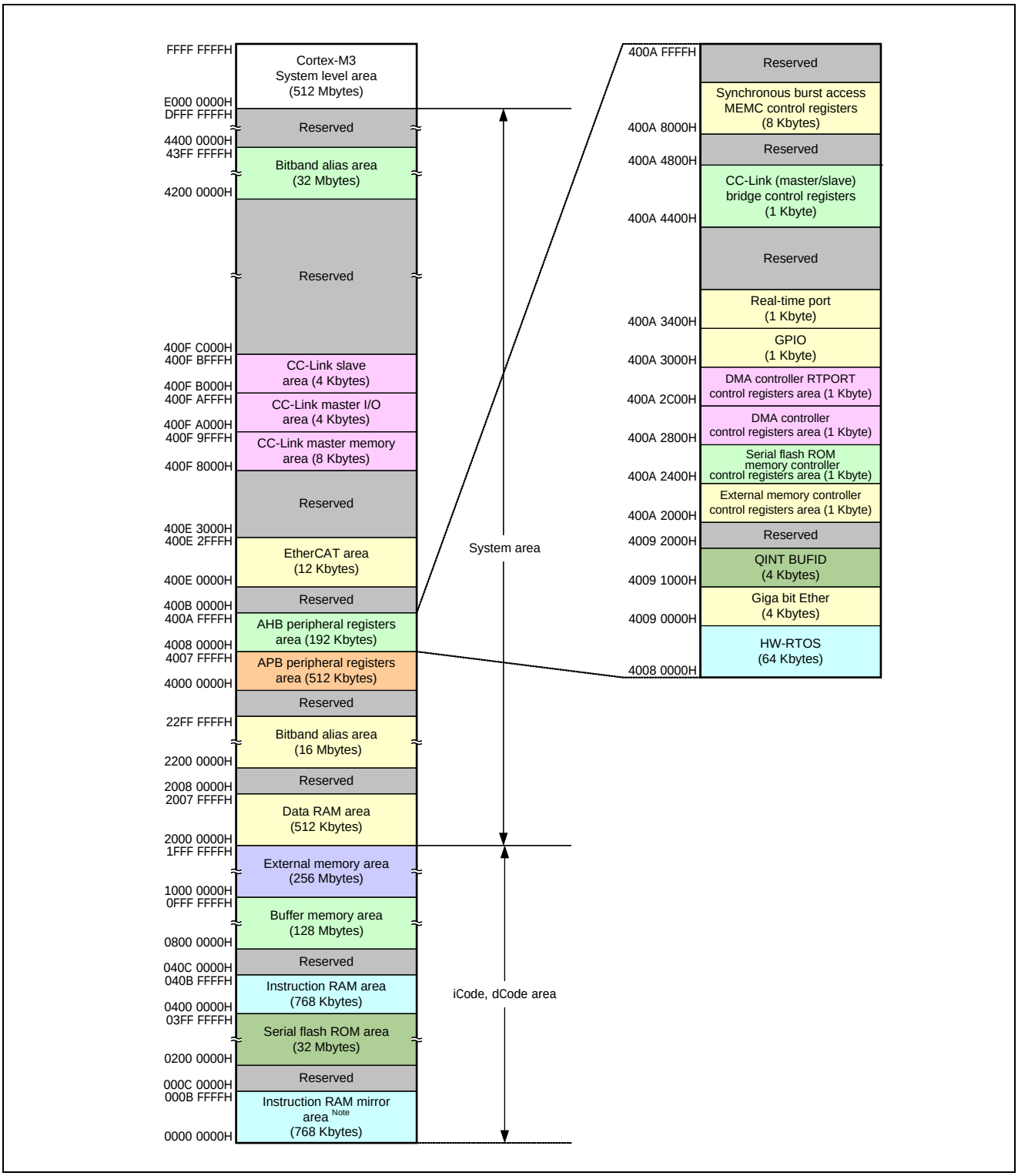

Figure 3.1 Memory Map (All)

Note: The addresses of the instruction RAM mirror area (768 Kbytes) where access actually occurs will change according to the selected boot mode. For details, see section 5.3, Memory MAP in Each Boot Mode, in the R-IN32M3 Series User's Manual: Peripheral Modules.

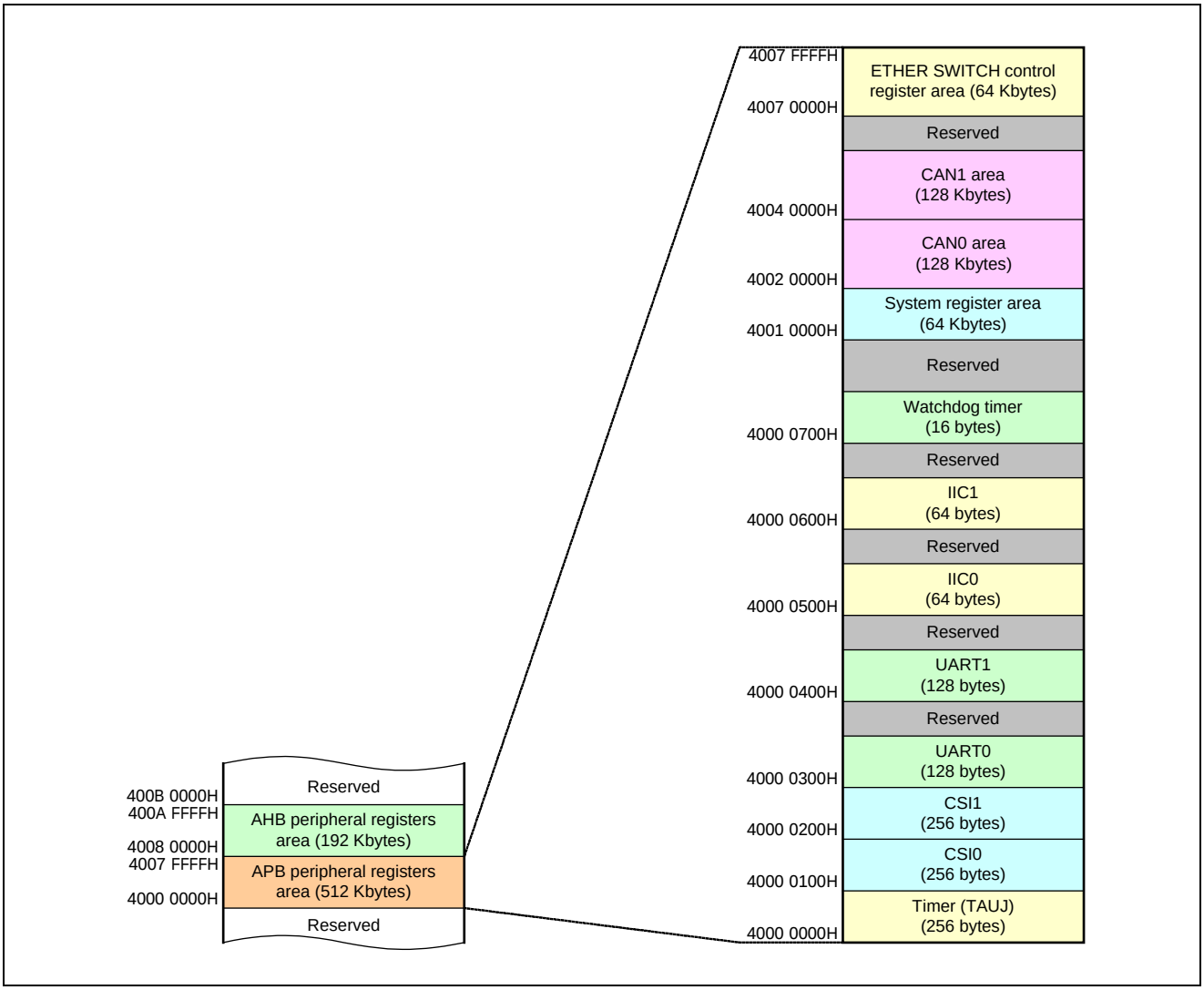

Figure 3.2 Memory Map (APB Peripheral Registers Area)

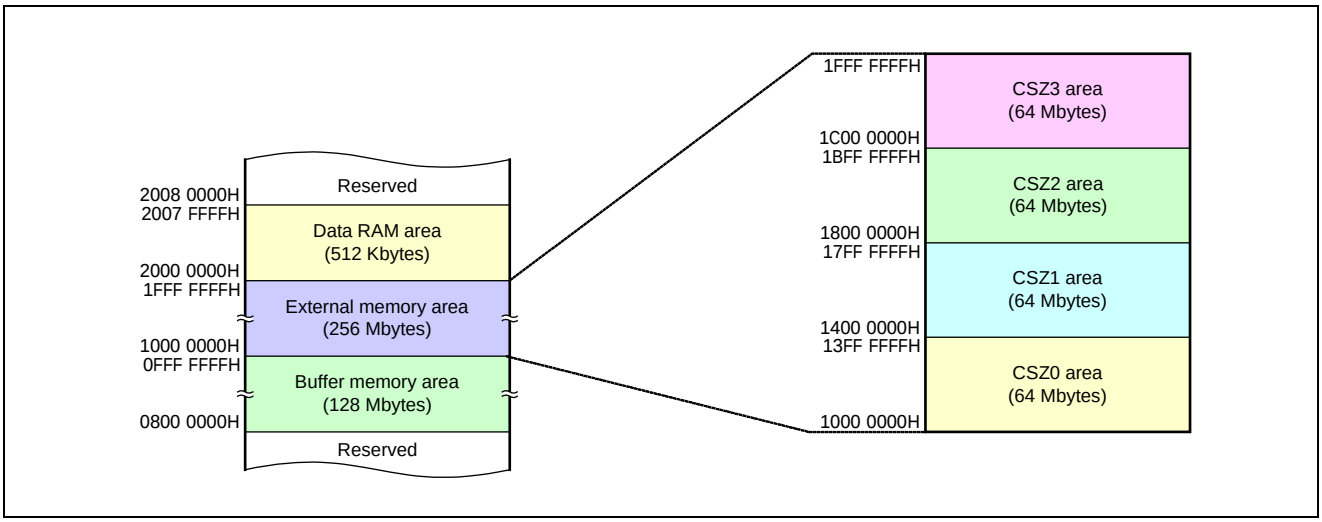

Figure 3.3 Memory Map (External Memory Area)

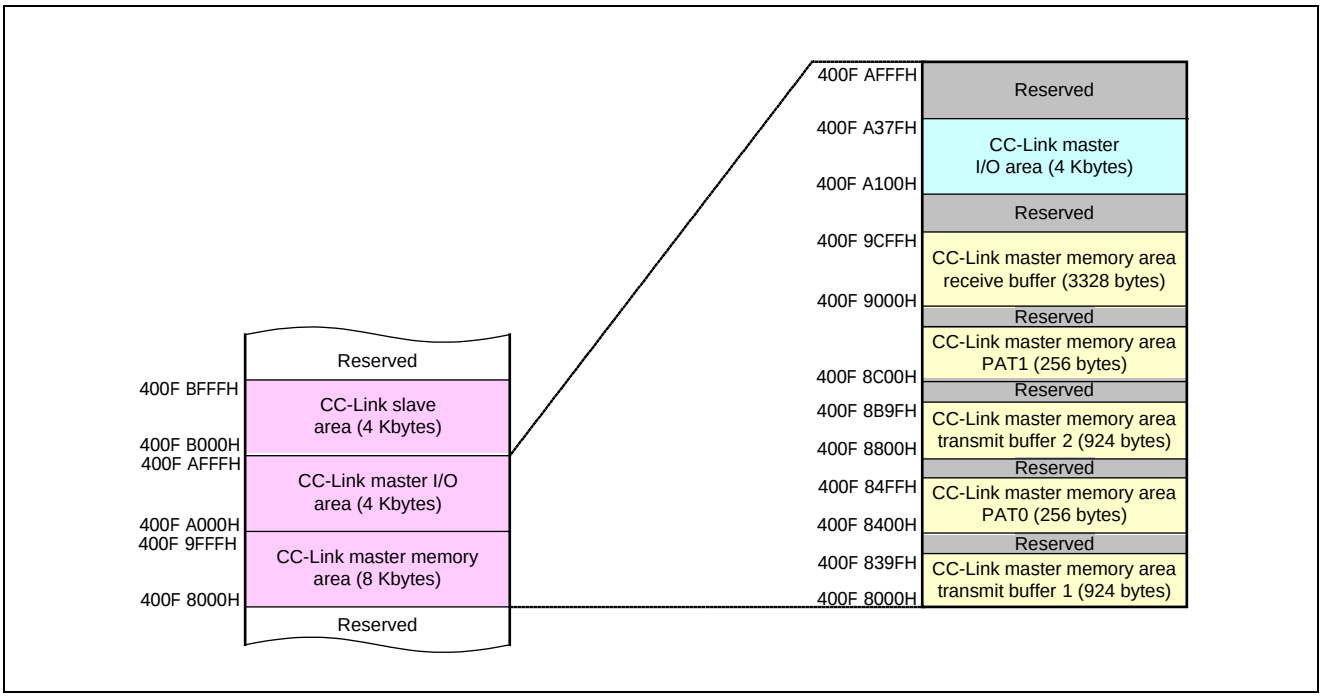

Figure 3.4 Memory Map (CC-Link Master Area)

Cautions 1. The CC-Link master shows a function block of intelligent device station.

2. The CC-Link slave shows a function block of remote device station.

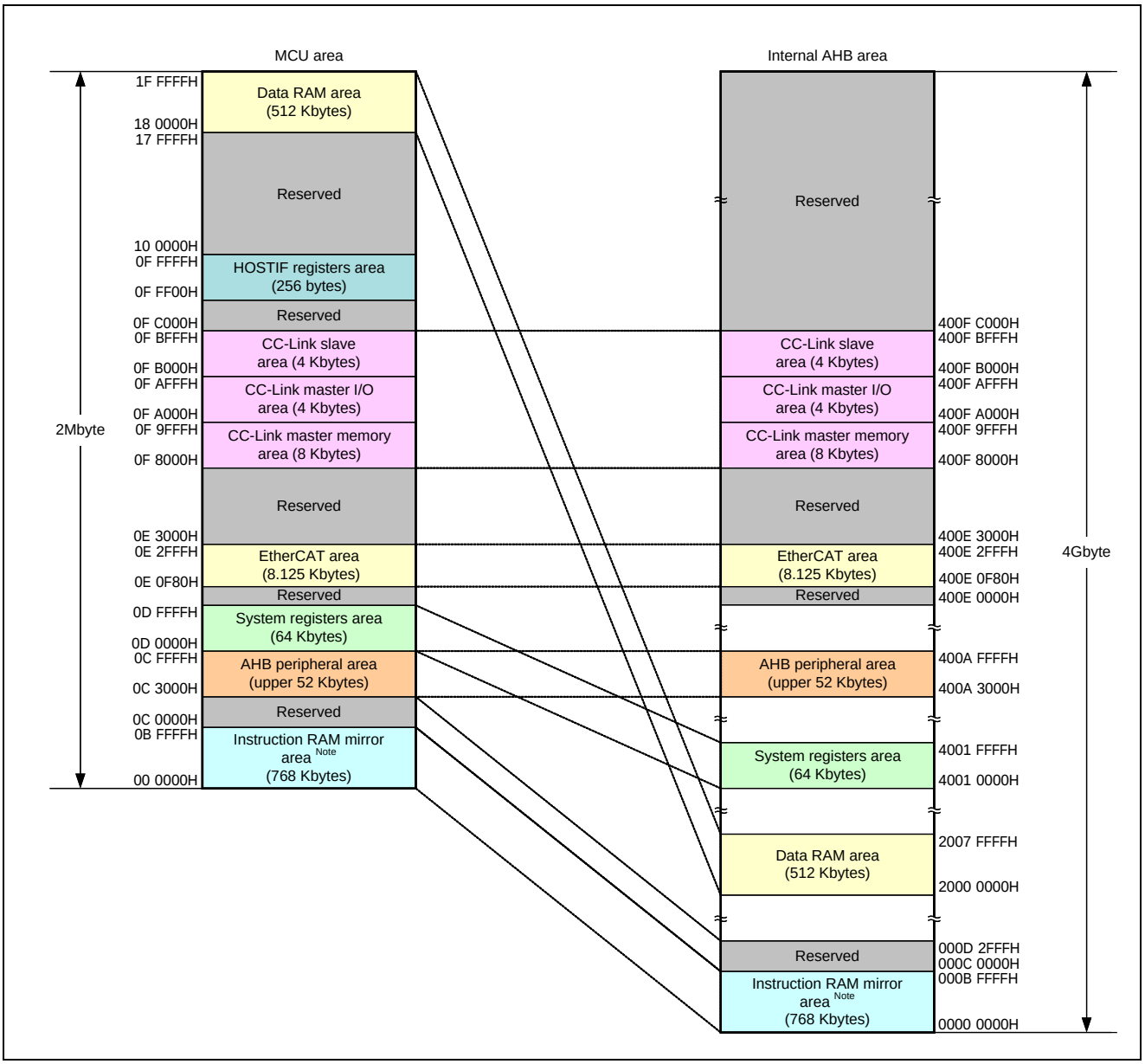

Figure 3.5 External MCU Interface Area

Note: The addresses of the instruction RAM mirror area (768 Kbytes) where access actually occurs will change according to the selected boot mode, as shown in the table below. For details, see section 5.3, Memory MAP in Each Boot Mode, and section 4, Bus Architecture, in the R-IN32M3 Series User's Manual: Peripheral Modules.

BOOT1	BOOT0	Boot Mode	Access Destination Area	Remarks
0	0	External memory boot	—	External MCU interface is disabled
0	1	External serial flash ROM boot	Reserved	Access disabled
1	0	External MCU boot	Instruction RAM area	—
1	1	Instruction RAM boot	Instruction RAM area	Enabled only for debugging

4. Exception Handling

The R-IN32M3 uses the interrupt controller of Cortex-M3.
Refer to the following URL of Arm for the exceptions handling operation of Cortex-M3.
http://infocenter.arm.com/help/topic/com.arm.doc.set.cortexm/index.html

4.1 Exceptions List

Exception numbers 1 to 15 are system exceptions of the Cortex-M3 CPU. Interrupts from the internal hardware of the R-IN32M3 and external pins are assigned to exception number 16 and higher exception numbers

Exception No.	Exception Type	Priority	Remark
1	Reset	-3 (highest)	- Input on the reset pin (RESETZ or PONRZ) - Reset by the watchdog timer - Set the SYSRESETREQ bit in NVIC of the Cortex-M3 CPU to 1 - Reset by the SYSRESET register
2	NMI	-2	- Input on the NMI pin - Generation of NMI by the watchdog timer
3	Hard fault	-1	All classes of exceptions that no other exception handler can handle. Used to call up a response to a fault.
4	Memory manage fault	Programmable	Exception from the MPU
5	Bus fault	Programmable	Bus error in access through the bus to the area outside the scope of management by the MPU
6	Use fault	Programmable	Error in instruction execution, including the execution of an undefined instruction
7 to 10	Reserved	-	-
11	SVCall	Programmable	System service call by an SVC instruction
12	Debug monitor	Programmable	Debug monitor
13	Reserved	-	-
14	PendSV	Programmable	Request for system service that can be kept pending
15	SysTick	Programmable	Indication from the system timer
16 and higher	R-IN32M3 specific Interrupt	Programmable	Interrupt from the internal hardware of the R-IN32M3 and external pins

4.2 List of Interrupts

The interrupts below are the exceptions (interrupts) with exception numbers 16 and higher, which are assigned to the NVIC of the Cortex-M3 CPU.
In the R-IN32M3, interrupts from the internal hardware and external pins are connected not only to the NVIC of the Cortex-M3 but also to the internal hardware real-time OS (HW-RTOS), trigger for starting the internal DMA controllers (common to both the general-purpose DMAC and real-time port DMAC), real-time ports, and timers.
The R-IN32M3 supports the following interrupts.

Table 4.1 List of Interrupts

(1/4)

Exception No.	Name	Interrupt Source	Connected to				
			NVIC	HW-RTOS	DMAC	Real-Time Port	Timer
16	INTTAUJ2I0	Timer array TAUJ2 channel 0 interrupt	○	○	○	○	○
17	INTTAUJ2I1	Timer array TAUJ2 channel 1 interrupt	○	○	○	○	○
18	INTTAUJ2I2	Timer array TAUJ2 channel 2 interrupt	○	○	○	○	○
19	INTTAUJ2I3	Timer array TAUJ2 channel 3 interrupt	○	○	○	○	○
20	INTUAJ0TIT	UARTJ0 transmission interrupt	○	○	○	○	○
21	INTUAJ0TIR	UARTJ0 reception interrupt	○	○	○	○	○
22	INTUAJ1TIT	UARTJ1 transmission interrupt	○	○	○	○	○
23	INTUAJ1TIR	UARTJ1 reception interrupt	○	○	○	○	○
24	INTCSIH0IC	CSIH0 communication status interrupt	○	○	○	○	○
25	INTCSIH0IR	CSIH0 reception status interrupt	○	○	○	○	○
26	INTCSIH0IJC	CSIH0 end of job interrupt	○	○	○	○	○
27	INTCSIH1IC	CSIH1 communication status interrupt	○	○	○	○	○
28	INTCSIH1IR	CSIH1 reception status interrupt	○	○	○	○	○
29	INTCSIH1IJC	CSIH1 end of job interrupt	○	○	○	○	○
30	INTIICB0TIA	IICB0 transmission/reception interrupt request	○	○	○	○	○
31	INTIICB1TIA	IICB1 transmission/reception interrupt request	○	○	○	○	○
32	INTFCN0REC	FCN0 reception completion	○	○	○	○	○
33	INTFCN0TRX	FCN0 transmission completion	○	○	○	○	○
34	INTFCN0WUP	FCN0 sleep and wakeup/transmission suspension	○	○	○	○	○
35	INTFCN1REC	FCN1 reception completion	○	○	○	○	○
36	INTFCN1TRX	FCN1 transmission completion	○	○	○	○	○
37	INTFCN1WUP	FCN1 sleep and wakeup/transmission suspension	○	○	○	○	○
38	INTDMA00	DMAC channel 0 transfer completion interrupt	○	○	○	○	○
39	INTDMA01	DMAC channel 1 transfer completion interrupt	○	○	○	○	○
40	INTDMA02	DMAC channel 2 transfer completion interrupt	○	○	○	○	○
41	INTDMA03	DMAC channel 3 transfer completion interrupt	○	○	○	○	○
42	INTRTDMA	RTDMAC transfer completion interrupt	○	○	○	○	○
43	INTCATSYNC0	EtherCAT Sync0 interrupt	○	○	○	○	-
44	INTCATSYNC1	EtherCAT Sync1 interrupt	○	○	○	○	-
45	INTCAT	EtherCAT interrupt	○	○	○	○	○

○: Connectable -: Not used

(2/4)

Exception No.	Name	Interrupt Source	Connected to				
			NVIC	HW-RTOS	DMAC	Real-Time Port	Timer
46	INTCATSOF	EtherCAT SOF interrupt	○	○	○	○	○
47	INTCATEOF	EtherCAT EOF interrupt	○	○	○	○	○
48	INTBUFDMA	Inter-Buffer DMA transfer completion	○	○	○	○	○
49	INTPHY0	Ether PHY interrupt 0	○	○	○	○	○
50	INTPHY1	Ether PHY interrupt 1	○	○	○	○	○
51	INTETHMII	Ether MII management access completion interrupt	○	○	○	○	○
52	INTETHPAUSE	Ether pause packet transmission completion	○	○	○	○	○
53	INTETHTX	Ether transmission completion interrupt	○	○	○	○	○
54	INTETHSW	Ether SWITCH Timer interrupt	○	○	○	○	○
55	INTETHSWDLR	Ether SWITCH DLR interrupt	○	○	○	○	○
56	INTETHSWSEC	Ether SWITCH SEC interrupt	○	○	○	○	○
57	INTETHRXFIFO	RX FIFO overflow	○	○	-	-	-
58	INTETHTXFIFO	TX FIFO underflow	○	○	-	-	-
59	INTETHRXDMA	Ether MACDMA reception completion	○	○	○	○	○
60	INTETHTXDMA	Ether MACDMA transmission completion	○	○	○	○	○
61	INTMACDMARXFRM	Receive frame successfully interrupt	○	○	○	○	○
62	INTHOSTIF	External MPU I/F interrupt	○	○	○	○	○
63	INTPZ0	INTPZ0 input	○	○	○	○	○
64	INTPZ1	INTPZ1 input	○	○	○	○	○
65	INTPZ2	INTPZ2 input	○	○	○	○	○
66	INTPZ3	INTPZ3 input	○	○	○	○	○
67	INTPZ4	INTPZ4 input	○	○	○	○	○
68	INTPZ5	INTPZ5 input	○	○	○	○	○
69	INTPZ6	INTPZ6 input	○	○	○	○	○
70	INTPZ7	INTPZ7 input	○	○	○	○	○
71	INTPZ8	INTPZ8 input	○	○	○	○	○
72	INTPZ9	INTPZ9 input	○	○	○	○	○
73	INTPZ10	INTPZ10 input	○	○	○	○	○
74	INTPZ11	INTPZ11 input	○	○	○	○	○
75	INTPZ12	INTPZ12 input	○	○	○	○	○
76	INTPZ13	INTPZ13 input	○	○	○	○	○
77	INTPZ14	INTPZ14 input	○	○	○	○	○
78	INTPZ15	INTPZ15 input	○	○	○	○	○
79	INTPZ16	INTPZ16 input	○	○	○	○	○
80	INTPZ17	INTPZ17 input	○	○	○	○	○
81	INTPZ18	INTPZ18 input	○	○	○	○	○
82	INTPZ19	INTPZ19 input	○	○	○	○	○

○: Connectable -: Not used

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Exception No.	Name	Interrupt Source	Connected to				
			NVIC	HW-RTOS	DMAC	Real-Time Port	Timer
83	INTPZ20	INTPZ20 input	○	○	○	○	○
84	INTPZ21	INTPZ21 input	○	○	○	○	○
85	INTPZ22	INTPZ22 input	○	○	○	○	○
86	INTPZ23	INTPZ23 input	○	○	○	○	○
87	INTPZ24	INTPZ24 input	○	○	○	○	○
88	INTPZ25	INTPZ25 input	○	○	○	○	○
89	INTPZ26	INTPZ26 input	○	○	○	○	○
90	INTPZ27	INTPZ27 input	○	○	○	○	○
91	INTPZ28	INTPZ28 input	○	○	○	○	○
92	INTHWRTOS	HW-RTOS interrupt	○	-	-	-	-
93	INTBRAMERR	Buffer RAM area access error	○	○	-	-	-
94	INTIICB0TIS	I2C0 status interrupt	○	○	-	-	-
95	INTIICB1TIS	I2C1 status interrupt	○	○	-	-	-
96	-	Reserved	-	-	-	-	-
97	INTSFLASH	Serial flash ROM controller error interrupt	○	○	-	-	-
98	INTUAJ0TIS	UARTJ0 status interrupt	○	○	-	-	-
99	INTUAJ1TIS	UARTJ1 status interrupt	○	○	-	-	-
100	INTCSIH0IRE	CSIH0 communication error interrupt	○	○	-	-	-
101	INTCSIH1IRE	CSIH1 communication error interrupt	○	○	-	-	-
102	INTFCN0ERR	FCN0 error detection	○	○	-	-	-
103	INTFCN1ERR	FCN1 error detection	○	○	-	-	-
104	INTDERR0	General DMAC error response interrupt	○	○	-	-	-
105	INTDERR1	Real-time port DMAC error response interrupt	○	○	-	-	-
106	INTETHTXFIFOERR	TX-FIFO error interrupt	○	○	-	-	-
107	INTETHRXERR	Ether receive flame error	○	○	-	-	-
108	INTETHRXDERR	MACDMA reception error interrupt	○	○	-	-	-
109	INTETHTXDERR	MACDMA transmission error interrupt	○	○	-	-	-
110	INTBUFDMAERR	Internal buffer DMA error	○	○	-	-	-
111	-	Reserved	-	-	-	-	-
112	INTECATRST	EtherCAT RESET interrupt	○	○	-	-	-
113	-	Reserved	-	-	-	-	-
114	-	Reserved	-	-	-	-	-
115	IRAMECCSEC	Internal instruction RAM 1-bit ECC error correction interrupt	○	-	-	-	-
116	DRAMECCSEC	Data RAM 1-bit ECC error correction interrupt	○	-	-	-	-
117	BRAMECCSEC	Buffer RAM 1-bit ECC error correction interrupt	○	-	-	-	-
118	IRAMECCDED	Internal instruction RAM 2-bit ECC error detection interrupt	○	-	-	-	-
119	DRAMECCDED	Data RAM 2-bit ECC error detection interrupt	○	-	-	-	-

○: Connectable -: Not used

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Exception No.	Name	Interrupt Source	Connected to				
			NVIC	HW-RTOS	DMAC	Real-Time Port	Timer
120	BRAMECCDED	Buffer RAM 2-bit ECC error detection interrupt	○	-	-	-	-
121	-	Reserved	-	-	-	-	-
122	-	Reserved	-	-	-	-	-
123	-	Reserved	-	-	-	-	-
124	-	Reserved	-	-	-	-	-
125	-	Reserved	-	-	-	-	-
126	-	Reserved	-	-	-	-	-
127	-	Reserved	-	-	-	-	-
128	-	Reserved	-	-	-	-	-
129	-	Reserved	-	-	-	-	-
130	-	Reserved	-	-	-	-	-
131	INTCCMRQ	CC-Link INTRQ interrupt	○	○	○	○	○
132	INTCCSRFSTB	CC-Link RFSTB interrupt Note	○	○	○	○	○
133	INTCCSMON3	CC-Link MON3 interrupt	○	○	○	○	○

○: Connectable -: Not used

Note: To use the CC-Link remote device station, connect the CCS_REFSTB (multiplexed with P10) pin to a pin with an external interrupt function (INTPZ) so as to generate an interrupt. In addition, select "both edges" as the mode for the interrupt trigger.

5. Peripheral Modules

For details of the following peripheral modules, refer to the R-IN32M3 Series User's Manual (Peripheral Modules).

- Clock function/Reset function
- CPU/Internal RAM
- Bus structure
- Hardware real-time OS
- Gigabit Ethernet interface
- Asynchronous SRAM memory controller
- Synchronous burst access memory controller
- External MCU interface
- Serial flash ROM memory controller
- DMA function
- Timer array unit J (TAUJ2)
- Window watchdog timer A (WDTA)
- Asynchronous serial interface J (UARTJ)
- Clocked serial interface H (CSIH)
- I^2C BUS (IICB)
- CAN controller (FCN)
- CC-Link (Intelligent device station, Remote device station)
- System registers (APB peripheral register area)
- Debug function

6. EtherCAT Slave Controller Function

6.1 Features

The EtherCAT slave controller (ESC) uses the EtherCAT slave controller IP core made by Beckhoff Automation GmbH, Germany.
The ESC processes EtherCAT communications and acts as the interface between the EtherCAT field bus and slave applications.

Table 6.1 Features of EtherCAT Slave Controller (ESC)

Features	R-IN32M3-EC	ET1100
Ports	2	2 to 4
FMMUs	8	8
SyncManagers	8	8
Process data RAM [Kbytes]	8	8
Distributed clocks	64 bits	64 bits
EBus	Not available	Available (0 to 4)
Process data interfaces		
Digital I/O	Not available	Available
SPI slave	Not available	Available
Host CPU interface	On-chip bus (external MCU interface)	8 bits/16 bits, synchronous/asynchronous

Caution: The register area (0E_0000H-0E_0F7FH) cannot be accessed from the external MCU interface (host CPU interface).

6.2 Configuration of EtherCAT Slave Controller

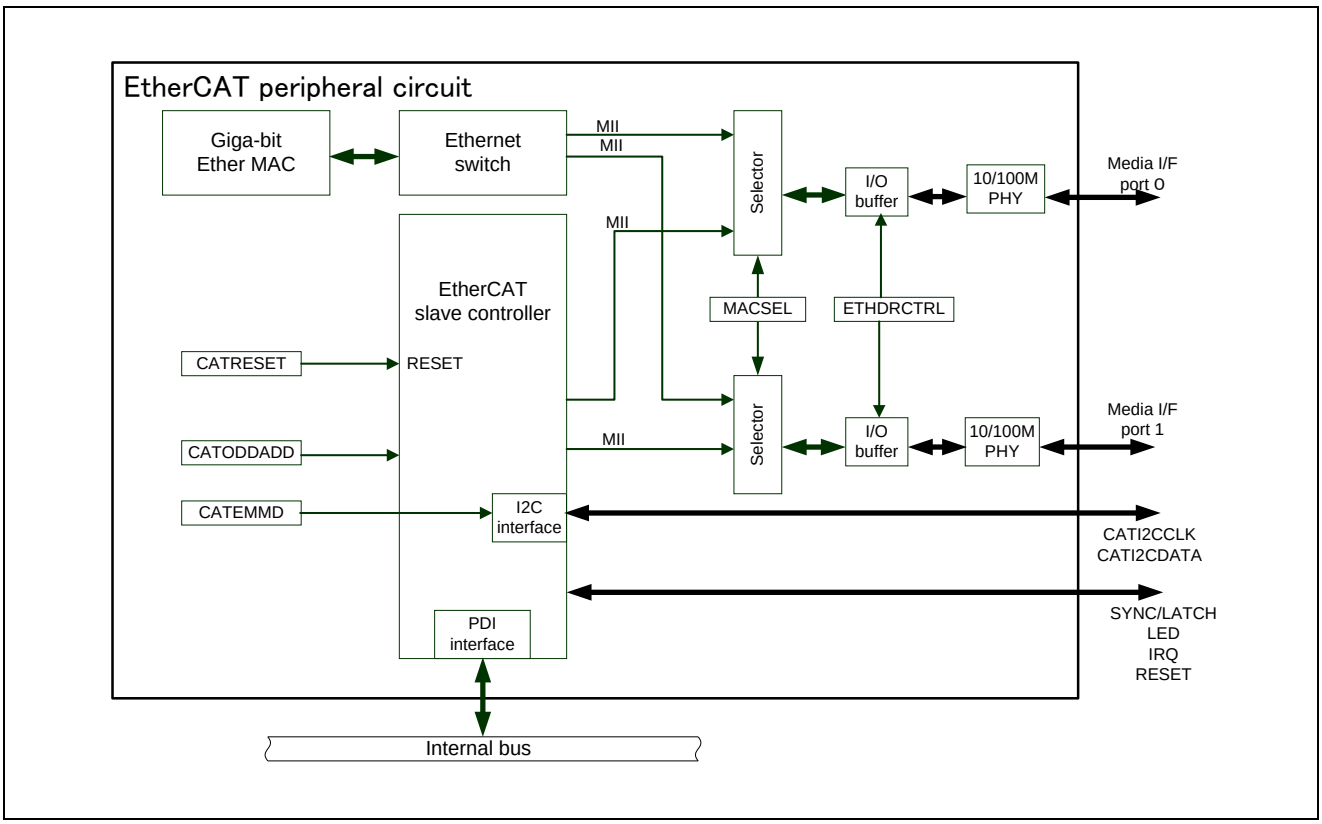


Figure 6.1 Peripheral Circuit of EtherCAT Slave Controller

6.3 Interrupt and I/O Signals

Table 6.2 Interrupt Signals of EtherCAT Slave Controller

Exception No.	Interrupt Signal	Function	Connected to				
			NVIC	HW-RTOS	DMAC	Real-Time Port	Timer
43	INTCATSYNC0	EtherCAT sync0 interrupt	○	○	○	○	-
44	INTCATSYNC1	EtherCAT sync1 interrupt	○	○	○	○	-
45	INTCAT	EtherCAT interrupt	○	○	○	○	○
46	INTCATSOF	EtherCAT SOF interrupt	○	○	○	○	○
47	INTCATEOF	EtherCAT EOF interrupt	○	○	○	○	○
112	INTECATRST	EtherCAT RESET interrupt	○	○	-	-	-

Table 6.3 I/O Signals of EtherCAT Slave Controller (Excluding PHY MDI Pins)

Pin Name	I/O	Function	Shared Port	Active
CATLEDRUN	O	EtherCAT RUN LED output	P00	High
CATIRQ	O	EtherCAT IRQ output	P01	High
CATLEDSTER	O	EtherCAT dual-color state LED output	P02	High
CATLEDERR	O	EtherCAT error LED output	P03	High
CATLINKACT0	O	EtherCAT Link/Activity LED output (port 0)	P04	High
CATLINKACT1	O	EtherCAT Link/Activity LED output (port 1)	P05	High
CATSYNC0	O	EtherCAT SYNC0 output	P11	High
CATSYNC1	O	EtherCAT SYNC1 output	P10	High
CATLATCH0	I	EtherCAT LATCH0 input	P11	High
CATLATCH1	I	EtherCAT LATCH1 input	P10	High
CATI2CCLK	O	EtherCAT EEPROM I2C clock output	P22	-
CATI2CDATA	I/O	EtherCAT EEPROM I2C data	P23	-
CATRESTOUT	O	EtherCAT PHY reset output	P56	High

6.4 Functional Overview

Typical functions of EtherCAT slave controller (ESC) and supported functions by R-IN32M3-EC are shown below. Regarding the detailed specifications of EtherCAT and ESC, refer to the documentation (e.g. ETG.1000 EtherCAT Specification) provided by EtherCAT Technology Group (ETG) and the EtherCAT Slave Controller IP Core (v2.04) datasheet provided by Beckhoff Automation GmbH.

Table 6.4 Typical Functions of EtherCAT Slave Controller and Supported Functions by R-IN32M3-EC

(1/3)

Features	Functions	Supported
EtherCAT protocol	Handling the following frames: ・Ethernet frames with Ether type 0x88A4 ・EtherCAT frames encapsulated in UDP/IP ・EtherCAT frames with VLAN tag ・Normal Ethernet frames	✓
Addressing modes	Device addressing ・Auto increment address ・Configured station address ・Broadcast address	✓
	Logical addressing	✓
Working counter	Counting the number of read/write from/to the device	✓
EtherCAT command types	Processing the command that master requests slaves to address each addressing mode	✓
Loop control	Loop control and loop state in the ESC	✓
Shadow buffers	Shadow buffers function when reading or writing registers	✓
Circulating frames	Processing of circulating frames during the failure	✓
Link detection	Link MII signal (PHY link signal)	✓
	MI link detection and configuration (PHY register monitor via the management interface)	✓
	Enhanced link detection (Communication state monitoring by the RX error monitor of MII)	✓
FIFO size reduction	RX FIFO size reduction to reduce the propagation delay	✓
Ethernet physical layer	MII	-
	MDI (100BASE-TX)	✓ NOTE 1
	MDI (100BASE-FX)	-
	EBUS	-
	Back-to-back MII connection	-
	MII management interface	✓
	Read/write of the PHY register via the MII management interface	✓
	PHY address offset	✓
	Manual TX clock shift compensation	-
	Automatic TX clock shift compensation	✓
FMMU	Mapping between logical address and physical address	✓

(2/3)

Features	Functions	Supported
SyncManager	Buffered mode	✓
	Mailbox mode	✓
	Interrupt and latch event generation when a buffer was completely and successfully written or read	✓
	Repeating mailbox communication	✓
	SyncManager deactivation by the PDI	✓
Distributed clocks	Clock synchronization considering propagation delay and drift compensation	✓
	Generation of synchronous output signals (SYNC0/1 signals) ・Cyclic mode ・Single shot mode ・Cyclic acknowledge mode ・Single shot acknowledge mode	✓
	Precise time stamping of input events (LATCH0/1 signals) ・Single event mode ・Continuous mode ・SyncManager event mode (for debugging)	✓
	Generation of synchronous interrupts	✓
	Synchronous digital output update / input sampling	-
	ECAT or PDI exclusive control over SYNC signals / LATCH signals	✓
	System time PDI controlled	-
	Communication timing ・Free run ・Synchronized to output event ・Synchronized to SYNC signal	✓
EtherCAT state machine	Control of EtherCAT state machine / Indication of the status and error code	✓
	Device emulation	-
SII EEPROM	SII EEPROM commands	✓
	SII EEPROM error indication	✓
	SII EEPROM access interface	✓
	EEPROM size selection	✓
	EEPROM emulation	-
Interrupt	AL event request (PDI interrupt)	✓
	ECAT event request (ECAT interrupt)	✓
Watchdog	Process data watchdog	✓
	PDI watchdog	✓
Error counters	Port error counters	✓
	Forwarded RX error counter	✓
	ECAT processing unit error counter	✓
	PDI error counter	✓
	Lost link counter	✓
	Watchdog counter: process data	✓
	Watchdog counter: PDI	✓

(3/3)

Features	Functions	Supported
LED signals	RUN LED signal	✓
	ERR LED signal	✓
	STATE LED and STATE_RUN LED signal	✓
	LINK/ACT LED signals	✓
	Port error LED signal	-
	RUN/ERR LED override	✓
Process data interface (PDI)	Digital I/O	-
	SPI	-
	8-/16-bit synchronous/asynchronous MCU interface	-
	On-chip bus	✓
	General purpose I/O	-
Write protection	Register write protection (0x0000-0x0FFF)	✓
	Write protection over the area including user RAM and process data RAM (0x0000-0x2FFF)	✓
ESC reset	ESC reset from master or PDI	✓

Notes 1. EtherCAT P is not supported.

6.5 List of EtherCAT Registers

(1) Peripheral Function Registers

Register Name	Symbol	Bits	Address Note
EtherCAT PHY offset address setting	CATOFFADD	32	BASE + 0620H
EtherCAT operation mode setting	CATEMMD	32	BASE + 0624H
EtherCAT reset	CATRESET	32	BASE + 0628H

(2) ESC Information Registers

Register Name	Symbol	Bits	Address
Type	TYPE	8	400E 0000H
Revision	REVISION	8	400E 0001H
Build	BUILD	16	400E 0002H
FMMUs supported	FMMU_NUM	8	400E 0004H
SyncManagers supported	SYNC_MANAGER	8	400E 0005H
RAM size	RAM_SIZE	8	400E 0006H
Port descriptor	PORT_DESC	8	400E 0007H
ESC features supported	FEATURE	16	400E 0008H

(3) Station Address Registers

Register Name	Symbol	Bits	Address
Configured station address	STATION_ADR	16	400E 0010H
Configured station alias	STATION_ALIAS	16	400E 0012H

(4) Write Protection Registers

Register Name	Symbol	Bits	Address
Write register enable	WR_REG_ENABLE	8	400E 0020H
Write register protection	WR_REG_PROTECT	8	400E 0021H
ESC write enable	ESC_WR_ENABLE	8	400E 0030H
ESC write protection	ESC_WR_PROTECT	8	400E 0031H

(5) Data Link Layer Registers

Register Name	Symbol	Bits	Address
ESC reset ECAT	ESC_RESET_ECAT	8	400E 0040H
ESC reset PDI	ESC_RESET_PDI	8	400E 0041H
ESC DL control	ESC_DL_CONTROL	32	400E 0100H
Physical read/Write offset	PHYSICAL_RW_OFFSET	16	400E 0108H
ESC DL status	ESC_DL_STATUS	16	400E 0110H

(6) Application Layer Registers

Register Name	Symbol	Bits	Address
AL control	AL_CONTROL	16	400E 0120H
AL status	AL_STATUS	16	400E 0130H
AL status code	AL_STATUS_CODE	16	400E 0134H
RUN LED override	RUN_LED_OVERRIDE	8	400E 0138H
ERR LED override	ERR_LED_OVERRIDE	8	400E 0139H

(7) PDI Registers

Register Name	Symbol	Bits	Address
PDI control	PDI_CONTROL	8	400E 0140H
ESC configuration	ESC_CONFIG	8	400E 0141H
PDI configuration	PDI_CONFIG	8	400E 0150H
SYNC/LATCH PDI configuration	SYNC_LATCH_CONFIG	8	400E 0151H
Extended PDI configuration	EXT_PDI_CONFIG	16	400E 0152H

(8) Interrupts Registers

Register Name	Symbol	bits	Address
ECAT event mask	ECAT_EVENT_MASK	16	400E 0200H
AL event mask	AL_EVENT_MASK	32	400E 0204H
ECAT event request	ECAT_EVENT_REQ	16	400E 0210H
AL event request	AL_EVENT_REQ	32	400E 0220H

(9) Error Counters Registers (n = 0, 1)

Register Name	Symbol	Bits	Address
Rx error counter n	RX_ERR_COUNTn	16	400E 0300H + 0002H*n
Forwarded Rx error counter n	FWD_RX_ERR_COUNTn	8	400E 0308H + 0001H*n
ECAT processing unit error counter	ECAT_PROC_ERR_COUNT	8	400E 030CH
PDI error counter	PDI_ERR_COUNT	8	400E 030DH
Lost link counter n	LOST_LINK_COUNTn	8	400E 0310H + 0001H*n

(10) Watchdog Registers

Register Name	Symbol	Bits	Address
Watchdog divider	WD_DIVIDE	16	400E 0400H
Watchdog time PDI	WDT_PDI	16	400E 0410H
Watchdog time process data	WDT_DATA	16	400E 0420H
Watchdog status process data	WDS_DATA	16	400E 0440H
Watchdog counter process data	WDC_DATA	8	400E 0442H
Watchdog counter PDI	WDC_PDI	8	400E 0443H

(11) SII EEPROM Interface Registers

Register Name	Symbol	Bits	Address
EEPROM configuration	EEP_CONF	8	400E 0500H
EEPROM PDI access state	EEP_STATE	8	400E 0501H
EEPROM control/status	EEP_CONT_STAT	16	400E 0502H
EEPROM address	EEP_ADR	32	400E 0504H
EEPROM data	EEP_DATA	32	400E 0508H

(12) MII Management Interface Registers (n = 0, 1)

Register Name	Symbol	Bits	Address
MII management control/status	MII_CONT_STAT	16	400E 0510H
PHY address	PHY_ADR	8	400E 0512H
PHY register address	PHY_REG_ADR	8	400E 0513H
PHY data	PHY_DATA	16	400E 0514H
MII management ECAT access state	MII_ECAT_ACS_STAT	8	400E 0516H
MII management PDI access state	MII_PDI_ACS_STAT	8	400E 0517H
PHY port status n	PHY_STATUSn	8	400E 0518H + 0001H*n

(13) FMMU Registers (m = 0 to 7)

Register Name	Symbol	Bits	Address
FMMU logical start address m	FMMUm.L_START_ADR	32	400E 0600H + 0010H*m
FMMU length m	FMMUm.LEN	16	400E 0604H + 0010H*m
FMMU logical start bit m	FMMUm.L_START_BIT	8	400E 0606H + 0010H*m
FMMU logical stop bit m	FMMUm.L_STOP_BIT	8	400E 0607H + 0010H*m
FMMU physical start address m	FMMUm.P_START_ADR	16	400E 0608H + 0010H*m
FMMU physical start bit m	FMMUm.P_START_BIT	8	400E 060AH + 0010H*m
FMMU type m	FMMUm.TYPE	8	400E 060BH + 0010H*m
FMMU activate m	FMMUm.ACT	8	400E 060CH + 0010H*m

(14) SyncManager Registers (m = 0 to 7)

Register Name	Symbol	Bits	Address
SyncManager physical start address m	SMm.P_START_ADR	16	400E 0800H + 0008H*m
SyncManager length m	SMm.LEN	16	400E 0802H + 0008H*m
SyncManager control m	SMm.CONTROL	8	400E 0804H + 0008H*m
SyncManager status m	SMm.STATUS	8	400E 0805H + 0008H*m
SyncManager activate m	SMm.ACT	8	400E 0806H + 0008H*m
SyncManager PDI control m	SMm.PDI_CONT	8	400E 0807H + 0008H*m

(15) Distributed Clocks Registers

Register Name	Symbol	Bits	Address
DC – Receive Time Registers			
Receive time port 0	DC_RCV_TIME_PORT0	32	400E 0900H
Receive time port 1	DC_RCV_TIME_PORT1	32	400E 0904H
DC – Time Loop Control Unit Registers			
System time	DC_SYS_TIME	64	400E 0910H
Receive time ECAT processing unit	DC_RCV_TIME_UNIT	64	400E 0918H
System time offset	DC_SYS_TIME_OFFSET	64	400E 0920H
System time delay	DC_SYS_TIME_DELAY	32	400E 0928H
System time difference	DC_SYS_TIME_DIFF	32	400E 092CH
Speed counter start	DC_SPEED_COUNT_START	16	400E 0930H
Speed counter difference	DC_SPEED_COUNT_DIFF	16	400E 0932H
System time difference filter depth	DC_SYS_TIME_DIFF_FIL_DEPTH	8	400E 0934H
Speed counter filter depth	DC_SPEED_COUNT_FIL_DEPTH	8	400E 0935H
DC – Cyclic Unit Control Registers			
Cyclic unit control	DC_CYC_CONT	8	400E 0980H
DC – SYNC Output Unit Registers			
Activation	DC_ACT	8	400E 0981H
Pulse length of Sync signals	DC_PULSE_LEN	16	400E 0982H
Activation status	DC_ACT_STAT	8	400E 0984H
SYNC0 status	DC_SYNC0_STAT	8	400E 098EH
SYNC1 status	DC_SYNC1_STAT	8	400E 098FH
Start time cyclic operation / next SYNC0 pulse	DC_CYC_START_TIME	64	400E 0990H
Next SYNC1 pulse	DC_NEXT_SYNC1_PULSE	64	400E 0998H
SYNC0 cycle time	DC_SYNC0_CYC_TIME	32	400E 09A0H
SYNC1 cycle time	DC_SYNC1_CYC_TIME	32	400E 09A4H
DC – Latch Input Unit Registers			
Latch0 control	DC_LATCH0_CONT	8	400E 09A8H
Latch1 control	DC_LATCH1_CONT	8	400E 09A9H
Latch0 status	DC_LATCH0_STAT	8	400E 09AEH
Latch1 status	DC_LATCH1_STAT	8	400E 09AFH
Latch0 time positive edge	DC_LATCH0_TIME_POS	64	400E 09B0H
Latch0 time negative edge	DC_LATCH0_TIME_NEG	64	400E 09B8H
Latch1 time positive edge	DC_LATCH1_TIME_POS	64	400E 09C0H
Latch1 time negative edge	DC_LATCH1_TIME_NEG	64	400E 09C8H
DC – SyncManager Event Times Registers			
EtherCAT buffer change event time	DC_ECAT_CNG_EV_TIME	32	400E 09F0H
PDI buffer start event time	DC_PDI_START_EV_TIME	32	400E 09F8H
PDI buffer change event time	DC_PDI_CNG_EV_TIME	32	400E 09FCH

(16) ETC Registers

Register Name	Symbol	Byte	Address
Product ID	PRODUCT_ID	8	400E 0E00H
Vender ID	VENDOR_ID	8	400E 0E08H
User RAM	USER_RAM	128	400E 0F80H - 400E 0FFFH
Process data RAM	DATA_RAM	8K	400E 1000H - 400E 2FFFH

Cautions 1. When accessing "(1) Peripheral Function Registers" via the external MCU interface, the base address is different from the one when accessing from the Cortex-M3 or DMA.
- When accessing from the CPU or DMA controller
BASE = 4001_0000H
- When accessing via the external MCU interface
BASE = D_0000H
2. When accessing via the external MCU interface, only user RAM and process data RAM (400E 0F80H – 400E 2FFF) can be accessed in the whole ESC memory area (400E 0000H – 400E 2FFFH).

Remark: Registers listed in this section are accessible from the EtherCAT master and CPU. An accessible state of respective registers is indicated by the following symbols.
ECAT: Access from the EtherCAT master
R/W, PDI: Access from the CPU

6.6 Peripheral Function Registers

6.6.1 EtherCAT PHY Offset Address Setting Register (CATOFFADD)

CATOFFADD sets the offset address of PHY when using EtherCAT.

This register can be read/written in 32-bit or 16bit units.

Caution: This register can be written only when releasing protection by the specific sequence with the system protect command register (SYSPCMD). Refer to the system protect command register (SYSPCMD) for protection releasing procedure. In addition, the special sequence is not necessary for reading the value from this register. For details on the system protect command register (SYSPCMD), see the R-IN32M3 Series User's Manual (Peripheral Modules).

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
CATOFFADD	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	OADD4	OADD3	OADD2	OADD1	OADD0	BASE + 0620H
																																	Initial Value
R/W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R/W	R/W	R/W	R/W	R/W	0000 0000H

Bit Position	Bit Name	Description
4 to 0	OADD4 to OADD0	Set the PHY offset address for EtherCAT.

6.6.2 EtherCAT Operation Mode Setting Register (CATEMMD)

CATEMMD sets the operating mode when using EtherCAT.

This register can be read/written in 32-bit or 16bit units.

Caution: This register can be written only when releasing protection by the specific sequence with the system protect command register (SYSPCMD). Refer to the system protect command register (SYSPCMD) for protection releasing procedure. In addition, the special sequence is not necessary for reading the value from this register. For details on the system protect command register (SYSPCMD), see the R-IN32M3 Series User's Manual (Peripheral Modules).

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
CATEMMD	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	I2CSIZE	BASE + 0624H
																																	Initial Value
R/W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R/W	0000 0000H

Bit Position	Bit Name	Description
0	I2CSIZE	Sets the I2C memory size for EtherCAT. 0: 16 Kbits or less 1: 32 Kbits to 4 Mbits

6.6.3 EtherCAT Reset Register (CATRESET)

CATRESET controls the reset operation of EtherCAT. EtherCAT is at the reset state when the R-IN32M3 is started. Release the reset by this register after the completion of shared port setting for EtherCAT. In addition, reset EtherCAT again by this register when the reset interrupt occurs from EtherCAT.

This register can be read/written in 32-bit or 16bit units.

Cautions 1. This register can be written only when releasing protection by the specific sequence with the system protect command register (SYSPCMD). Refer to the system protect command register (SYSPCMD) for protection releasing procedure. In addition, the special sequence is not necessary for reading the value from this register. For details on the system protect command register (SYSPCMD), see the R-IN32M3 Series User's Manual (Peripheral Modules).

2. Control this register after securing the time to satisfy reset width to EtherPHY by software in case of resetting EtherCAT. For detail, see section 6.22, Reset Circuit .

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
CATRESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	CATRST	BASE + 0628H
																																	Initial Value
R/W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R/W	0000 0000H

Bit Position	Bit Name	Description
0	CATRST	Resets EtherCAT. 0: During reset 1: Release reset

6.7 ESC Information Register

6.7.1 Type Register (TYPE)

TYPE indicates the type of the EtherCAT slave controller.

	7	6	5	4	3	2	1	0	Address	Initial Value
TYPE	TYPE								400E 0000H	A0H
ECAT	R	R	R	R	R	R	R	R		
PDI	R	R	R	R	R	R	R	R		

Bit Position	Bit Name	Description
7 to 0	TYPE	Type of the EtherCAT slave controller

6.7.2 Revision Register (REVISION)

REVISION indicates the revision of the EtherCAT slave controller.

	7	6	5	4	3	2	1	0	Address	Initial Value
REVISION	REV								400E 0001H	01H
ECAT	R	R	R	R	R	R	R	R		
PDI	R	R	R	R	R	R	R	R		

Bit Position	Bit Name	Description
7 to 0	REV	Revision of the EtherCAT slave controller

6.7.3 Build Register (BUILD)

BUILD indicates the build number of the EtherCAT slave controller.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	Initial Value
BUILD	BUILD																400E 0002H	0000H
ECAT	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R		
PDI	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R		

Bit Position	Bit Name	Description
15 to 0	BUILD	Build number of the EtherCAT slave controller

6.7.4 FMMUs Supported Register (FMMU_NUM)

FMMU_NUM indicates the number of supported FMMU channels (or entities) of the EtherCAT slave controller.

	7	6	5	4	3	2	1	0	Address	Initial Value
FMMU_NUM	NUMFMMU								400E 0004H	08H
ECAT	R	R	R	R	R	R	R	R		
PDI	R	R	R	R	R	R	R	R		

Bit Position	Bit Name	Description
7 to 0	NUMFMMU	Number of supported FMMU channels (or entities) of the EtherCAT slave controller

6.7.5 SyncManagers Supported Register (SYNC_MANAGER)

SYNC_MANAGER indicates the number of supported SyncManager channels (or entities) of the EtherCAT slave controller.

	7	6	5	4	3	2	1	0	Address	Initial Value
SYNC_ MANAGER	NUMSYNC								400E 0005H	08H
ECAT	R	R	R	R	R	R	R	R		
PDI	R	R	R	R	R	R	R	R		

Bit Position	Bit Name	Description
7 to 0	NUMSYNC	Number of supported SyncManager channels (or entities) of the EtherCAT slave controller

6.7.6 RAM Size Register (RAM_SIZE)

RAM_SIZE indicates the process data RAM size supported by the EtherCAT slave controller in Kbytes.

	7	6	5	4	3	2	1	0	Address	Initial Value
RAM_SIZE	RAMSIZE								400E 0006H	08H
ECAT	R	R	R	R	R	R	R	R		
PDI	R	R	R	R	R	R	R	R		

Bit Position	Bit Name	Description
7 to 0	RAMSIZE	Process data RAM size supported by the EtherCAT slave controller in Kbytes

6.7.7 Port Descriptor Register (PORT_DESC)

PORT_DESC indicates the port configuration.

	7	6	5	4	3	2	1	0	Address	Initial Value
PORT_DESC	P3		P2		P1		P0		400E 0007H	0FH
ECAT	R	R	R	R	R	R	R	R		
PDI	R	R	R	R	R	R	R	R		

Bit Position	Bit Name	Description
7, 6	P3	Port 3 configuration: This LSI doesn't implement port 3. 00: Not implemented 01: Not configured (SII EEPROM) 10: EBUS 11: MII
5, 4	P2	Port 2 configuration: This LSI doesn't implement port 2. 00: Not implemented 01: Not configured (SII EEPROM) 10: EBUS 11: MII
3, 2	P1	Port 1 configuration: This LSI provides the MII connection. 00: Not implemented 01: Not configured (SII EEPROM) 10: EBUS 11: MII
1, 0	P0	Port 0 configuration: This LSI provides the MII connection. 00: Not implemented 01: Not configured (SII EEPROM) 10: EBUS 11: MII

6.7.8 ESC Features Supported Register (FEATURE)

FEATURE indicates the features supported by the EtherCAT slave controller.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	Initial Value
FEATURE	0	0	0	0	FSCONFIG	RWSUPP	LRW	DCSYNC	FCS	LINKDECMII	0	0	DCWID	DC	0	FMMU	400E 0008H	01CCH
ECAT	0	0	0	0	R	R	R	R	R	R	0	0	R	R	0	R		
PDI	0	0	0	0	R	R	R	R	R	R	0	0	R	R	0	R		

Bit Position	Bit Name	Description
11	FSCONFIG	Fixed FMMU/SyncManager Configuration 0: Variable configuration 1: Fixed configuration
10	RWSUPP	EtherCAT Read/Write Command Support (BRW, APRW, FPRW) 0: Supported 1: Not supported
9	LRW	EtherCAT LRW Command Support 0: Supported 1: Not supported
8	DCSYNC	Enhanced DC SYNC Activation 0: Not available 1: Available
7	FCS	Separate Handling of FCS Errors 0: Not supported 1: Supported. Frames with wrong FCS and additional nibble will be counted separately in forwarded RX error counter.
6	LINKDECMII	Enhanced Link Detection in MII 0: Not available 1: Available
3	DCWID	Distributed Clocks (Width) 0: 32 bits 1: 64 bits
2	DC	Distributed Clocks 0: Not available 1: Available
0	FMMU	FMMU Operation 0: Bit oriented 1: Byte oriented

6.8 Station Address Registers

6.8.1 Configured Station Address Register (STATION_ADR)

STATION_ADR indicates the address used for node addressing.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	Initial Value
STATION_ADR	NODADDR																400E 0010H	0000H
ECAT	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		
PDI	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R		

Bit Position	Bit Name	Description
15 to 0	NODADDR	Address used for node addressing (FPxx commands)

6.8.2 Configured Station Alias Register (STATION_ALIAS)

STATION_ALIAS indicates the alias address used for node addressing (FPxx commands).

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	Initial Value
STATION_ALIAS	NODALIADDR																400E 0012H	0000H[Note]
ECAT	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R		
PDI	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		

Bit Position	Bit Name	Description
15 to 0	NODALIADDR	Alias Address Used for Node Addressing (FPxx Commands) The use of this alias is activated by setting 1 to bit 8 in the extended ESC DL control register (ESC_EX_DL_CONTROL: 0x0102).

Note: The initial value is 0 until the EEPROM is loaded, then changes to the value stored at 0x0004 in the EEPROM. The EEPROM value is only taken over at first EEPROM load after power-on or reset.

6.9 Write Protection Registers

6.9.1 Write Register Enable Register (WR_REG_ENABLE)

WR_REG_ENABLE is used to release the write protection temporarily when the write register protection is enabled.

	7	6	5	4	3	2	1	0	Address	Initial Value
WR_REG_ENABLE	0	0	0	0	0	0	0	ENABLE	400E 0020H	00H
ECAT	0	0	0	0	0	0	0	R/W		
PDI	0	0	0	0	0	0	0	R		

Bit Position	Bit Name	Description
0	ENABLE	When the write register protection is enabled (1 is set to bit 0 in the write register protection register (WR_REG_PROTECT: 0x0021)), this register has to be written in the same Ethernet frame (value does not care) before other writes to this station are allowed. Write protection is still active after this frame (if the write register protection register is not changed).

6.9.2 Write Register Protection Register (WR_REG_PROTECT)

WR_REG_PROTECT is used to protect from writing register. The registers at 400E 0000H to 400E 0FFFH are write protected (excluding the WR_REG_ENABLE register (0x0020) and the ESC_WR_ENABLE register (0x0030)).

	7	6	5	4	3	2	1	0	Address	Initial Value
WR_REG_PROTECT	0	0	0	0	0	0	0	PROTECT	400E 0021H	00H
ECAT	0	0	0	0	0	0	0	R/W		
PDI	0	0	0	0	0	0	0	R		

Bit Position	Bit Name	Description
0	PROTECT	Write Register Protection 0: Protection disabled 1: Protection enabled

6.9.3 ESC Write Enable Register (ESC_WR_ENABLE)

ESC_WR_ENABLE is used to release the write protection temporarily when the ESC write protection is enabled.

	7	6	5	4	3	2	1	0	Address	Initial Value
ESC_WR_ENABLE	0	0	0	0	0	0	0	ENABLE	400E 0030H	00H
ECAT	0	0	0	0	0	0	0	R/W		
PDI	0	0	0	0	0	0	0	R		

Bit Position	Bit Name	Description
0	ENABLE	If the ESC write protection is enabled (1 is set to bit 0 in the ESC write protection register (ESC_WR_PROTECT: 0x0021)), this register has to be written in the same Ethernet frame (value does not care) before other writes to this station are allowed. ESC write protection is still active after this frame (if the ESC write protection register is not changed).

6.9.4 ESC Write Protection Register (ESC_WR_PROTECT)

ESC_WR_PROTECT is used to protect from writing register and process data RAM. The registers and memory at 400E 0000H to 400E 2FFFH including the process data RAM are write protected (excluding the WR_REG_ENABLE register (0x0020) and the ESC_WR_ENABLE register (0x0030)).

	7	6	5	4	3	2	1	0	Address	Initial Value
ESC_WR_PROTECT	0	0	0	0	0	0	0	PROTECT	400E 0031H	00H
ECAT	0	0	0	0	0	0	0	R/W		
PDI	0	0	0	0	0	0	0	R		

Bit Position	Bit Name	Description
0	PROTECT	Protection from Writing Register and Process Memory 0: Protection disabled 1: Protection enabled

6.10 Data Link Layer Registers

6.10.1 ESC Reset ECAT Register (ESC_RESET_ECAT)

ESC_RESET_ECAT is used to reset the EtherCAT slave controller from ECAT (master) by software.

Write:

	7	6	5	4	3	2	1	0	Address	Initial Value
ESC_RESET_ECAT	RESET_ECAT								400E 0040H	00H
ECAT	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		
PDI	R	R	R	R	R	R	R	R		

Bit Position	Bit Name	Description
7 to 0	RESET_ECAT	A reset is asserted after writing 0x52 ("R"), 0x45 ("E"), and 0x53 ("S") to this register with 3 consecutive frames.

Read:

	7	6	5	4	3	2	1	0	Address	Initial Value
ESC_RESET_ECAT	0	0	0	0	0	0	RESET_ECAT		400E 0040H	00H
ECAT	0	0	0	0	0	0	R/W	R/W		
PDI	0	0	0	0	0	0	R	R		

Bit Position	Bit Name	Description
1, 0	RESET_ECAT	Progress of the Reset Procedure 01: After writing 0x52 10: After writing 0x45 (if 0x52 was written before) 00: Others

6.10.2 ESC Reset PDI Register (ESC_RESET_PDI)

ESC_RESET_PDI is used to reset the EtherCAT slave controller from PDI by software.

Write:

	7	6	5	4	3	2	1	0	Address	Initial Value
ESC_RESET_PDI	RESET_PDI								400E 0041H	00H
ECAT	R	R	R	R	R	R	R	R		
PDI	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		

Bit Position	Bit Name	Description
7 to 0	RESET_PDI	A reset is asserted after writing 0x52 ("R"), 0x45 ("E"), and 0x53 ("S") to this register with 3 consecutive frames.

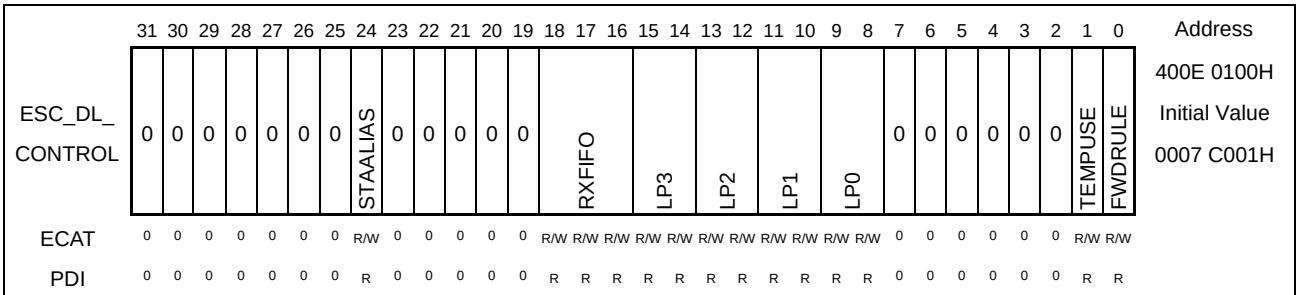
Read:

	7	6	5	4	3	2	1	0	Address	Initial Value
ESC_RESET_PDI	0	0	0	0	0	0	RESET_PDI		400E 0041H	00H
ECAT	0	0	0	0	0	0	R	R		
PDI	0	0	0	0	0	0	R/W	R/W		

Bit Position	Bit Name	Description
1, 0	RESET_PDI	Progress of the Reset Procedure 01: After writing 0x52 10: After writing 0x45 (if 0x52 was written before) 00: Others

6.10.3 ESC DL Control Register (ESC_DL_CONTROL)

ESC_DL_CONTROL is used to control loop and configure RX FIFO size and station alias in the EtherCAT slave controller.



Bit Position	Bit Name	Description
24	STAALIAS	Station Alias 0: Ignores the station alias 1: Alias can be used for all configured address command types (FPRD, FPWR, …)
18 to 16	RXFIFO	Specify the RX FIFO size. Reducing the size of FIFO shortens the transfer time. 0 to 3: -40 ns 4 to 6: No change 7: Default
15, 14	LP3	Loop Port 3 (Port 3 is not available on this LSI.) 00: Auto 01: Auto close 10: Open 11: Closed
13, 12	LP2	Loop Port 2 (Port 2 is not available on this LSI.) 00: Auto 01: Auto close 10: Open 11: Closed
11, 10	LP1	Loop Port 1 00: Auto 01: Auto close 10: Open 11: Closed
9, 8	LP0	Loop Port 0 00: Auto 01: Auto close 10: Open 11: Closed
1	TEMPUSE	Temporary Use of Settings in Bits 15 to 8 0: Always used 1: Used for about 1 second, then revert to previous settings

Bit Position	Bit Name	Description
0	FWDRULE	Forwarding Rule 0: EtherCAT frames are processed. Non-EtherCAT frames are forwarded without processing. 1: EtherCAT frames are processed. Non-EtherCAT frames are destroyed. The source MAC address is changed for every frame (SOURCE_MAC[1] is set to 1 (locally administered address)) regardless of the forwarding rule.

Notes 1. Loop configuration changes are delayed until the end of a currently received or transmitted frame at the port.

2. The possibility of RX FIFO size reduction depends on the clock source accuracy of every connected EtherCAT devices (master, slave, etc.). The RX FIFO size as default is sufficient for 100 ppm accuracy, but the FIFO size of 0 to 3 is possible with 25 ppm accuracy.

6.10.4 Physical Read/Write Offset Register (PHYSICAL_RW_OFFSET)

PHYSICAL_RW_OFFSET is used to set offset size between the read address and the write address in the R/W command.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	Initial Value
PHYSICAL_RW_OFFSET	RWOFFSET																400E 0108H	0000H
ECAT	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		
PDI	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R		

Bit Position	Bit Name	Description
15 to 0	RWOFFSET	Offset of R/W Commands (FPRW, APRW) between Read address and Write address RD_ADR = ADR WR_ADR = ADR + R/W-offset

6.10.5 ESC DL Status Register (ESC_DL_STATUS)

ESC_DL_STATUS indicates the EtherCAT slave controller status.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	Initial Value
ESC_DL_STATUS	COMP3	LP3	COMP2	LP2	COMP1	LP1	COMP0	LP0	PHYP3	PHYP2	PHYP1	PHYP0	0	ENHLINKD	PDIWDST	PDIOPE	400E 0110H	0004H
ECAT	R (ack)	R (ack)	R (ack)	R (ack)	R (ack)	R (ack)	R (ack)	R (ack)	R (ack)	R (ack)	R (ack)	R (ack)	0	R (ack)	R (ack)	R (ack)		
PDI	R	R	R	R	R	R	R	R	R	R	R	R	0	R	R	R		

Bit Position	Bit Name	Description
15	COMP3	Communication on Port 3 (Port 3 is not available on this LSI.) 0: No stable communication 1: Communication established
14	LP3	Loop Port 3 (Port 3 is not available on this LSI.) 0: Open 1: Closed
13	COMP2	Communication on Port 2 (Port 2 is not available on this LSI.) 0: No stable communication 1: Communication established
12	LP2	Loop Port 2 (Port 2 is not available on this LSI.) 0: Open 1: Closed
11	COMP1	Communication on Port 1 0: No stable communication 1: Communication established
10	LP1	Loop Port 1 0: Open 1: Closed
9	COMP0	Communication on Port 0 0: No stable communication 1: Communication established
8	LP0	Loop Port 0 0: Open 1: Closed
7	PHYP3	Physical Link on Port 3 (Port 3 is not available on this LSI.) 0: No link 1: Link detected
6	PHYP2	Physical Link on Port 2 (Port 2 is not available on this LSI.) 0: No link 1: Link detected
5	PHYP1	Physical Link on Port 1 0: No link 1: Link detected

Bit Position	Bit Name	Description
4	PHYP0	Physical Link on Port 0 0: No link 1: Link detected
2	ENHLINKD	Enhanced Link Detection 0: Deactivated for all ports 1: Activated for at least one port Note: The value of bit 9 at 0x0000 in the EEPROM is set. The EEPROM value is only taken over at first EEPROM load after power-on or reset.
1	PDIWDST	PDI Watchdog Status 0: The watchdog is expired 1: The watchdog is reloaded
0	PDIOPE	PDI Operation/EEPROM Loaded State 0: EEPROM is not loaded, and PDI is not operational (no access to the process data RAM) 1: EEPROM is loaded correctly, and PDI is operational (access to the process data RAM)

Note: Reading this register from ECAT clears bit 2 in the ECAT event request register (ECAT_EVENT_REQ: 0x0210).

6.11 Application Layer Registers

6.11.1 AL Control Register (AL_CONTROL)

AL_CONTROL indicates the state transition of the device state machine according to the request from the master. In addition, this register acknowledges an error indication from the slave.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	Initial Value
AL_CONTROL	0	0	0	0	0	0	0	0	0	0	DEVICEID	ERRINDACK	INISTATE				400E 0120H	0001H
ECAT	0	0	0	0	0	0	0	0	0	0	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)		
PDI	0	0	0	0	0	0	0	0	0	0	R/ (clear)	R/ (clear)	R/ (clear)	R/ (clear)	R/ (clear)	R/ (clear)		

Bit Position	Bit Name	Description
5	DEVICEID	Device Identification Request 0: No request 1: Device Identification request
4	ERRINDACK	Error Indication Acknowledge 0: Error indication from the AL status register is not acknowledged. 1: Error indication from the AL status register is acknowledged.
3 to 0	INISTATE	These bits indicate the state transition of the device state machine. 1: Init state request 3: Bootstrap state request 2: Pre-operational state request 4: Safe-operational state request 8: Operational state request

Note: The PDI has to read the AL control register after ECAT has written it. Otherwise, ECAT cannot write the AL control register again. Reading this register from PDI clears bit 0 in the AL event request register (AL_EVENT_REQ: 0x0220).

6.11.2 AL Status Register (AL_STATUS)

AL_STATUS indicates the slave application status.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	Initial Value
AL_STATUS	0	0	0	0	0	0	0	0	0	0	DEVICEID	ERR	ACTSTATE				400E 0130H	0001H
ECAT	0	0	0	0	0	0	0	0	0	0	R	R	R	R	R	R		
PDI	0	0	0	0	0	0	0	0	0	0	R/W	R/W	R/W	R/W	R/W	R/W		

Bit Position	Bit Name	Description
5	DEVICEID	Device Identification Status 0: Device Identification not valid 1: Device Identification loaded
4	ERR	Error Indicator 0: The device is in the state as requested or the flag is cleared by command. 1: The device has not entered the requested state or the state has changed as a result of a local action.
3 to 0	ACTSTATE	Actual State of the Device State Machine 1: Init state 3: Request bootstrap state 2: Pre-operational state 4: Safe-operational state 8: Operational state

Note: Reading this register from ECAT clears bit 3 in the ECAT event request register (ECAT_EVENT_REQ: 0x0210).

6.11.3 AL Status Code Register (AL_STATUS_CODE)

AL_STATUS_CODE indicates the error code from slave application.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	Initial Value
AL_STATUS_CODE	STATUSCODE																400E 0134H	0000H
ECAT	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R		
PDI	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		

Bit Position	Bit Name	Description
15 to 0	STATUSCODE	AL Status Code

6.11.4 RUN LED Override Register (RUN_LED_OVERRIDE)

RUN_LED_OVERRIDE is used to override RUN LED control.

	7	6	5	4	3	2	1	0	Address	Initial Value
RUN_LED_OVERRIDE	0	0	0	OVERRIDEEN	LEDCODE				400E 0138H	00H
ECAT	0	0	0	R/W	R/W	R/W	R/W	R/W		
PDI	0	0	0	R/W	R/W	R/W	R/W	R/W		

Bit Position	Bit Name	Description
4	OVERRIDEEN	Override Enable 0: Override is disabled 1: Override is enabled
3 to 0	LEDCODE	LED Code: 0x0: Off (1-Init) 0x1-0xC: Flash 1x – 12x (4-SafeOp 1x) 0xD: Blinking (2-PreOp) 0xE: Flickering (3-Bootrap) 0xF: On (8-Op)

Note: Bit 4 (override enable) is cleared when the AL status register is changed to valid values. In general, RUN LED is automatically controlled by the AL status register (AL_STATUS: 0x0130). It is not necessary to override RUN LED in order to indicate the status of general state machine.
For instance, it is available to use this register to indicate the specific slave position by blinking.

6.11.5 ERR LED Override Register (ERR_LED_OVERRIDE)

ERR_LED_OVERRIDE is used to override ERR LED control.

	7	6	5	4	3	2	1	0	Address	Initial Value
ERR_LED_OVERRIDE	0	0	0	OVERRIDEEN	LEDCODE				400E 0139H	00H
ECAT	0	0	0	R/W	R/W	R/W	R/W	R/W		
PDI	0	0	0	R/W	R/W	R/W	R/W	R/W		

Bit Position	Bit Name	Description
4	OVERRIDEEN	Override Enable 0: Override is disabled 1: Override is enabled
3 to 0	LEDCODE	LED Code: 0x0: Off 0x1-0xC: Flash 1x – 12x 0xD: Blinking 0xE: Flickering 0xF: On

Note: Bit 4 (override enable) is cleared when a new error is generated.
ESC automatically controls ERR LED in the conditions below:
• SII EEPROM load error
• PDI watchdog timeout
Regarding other errors, ERR LED should be controlled by application using this register.

6.12 PDI Registers

6.12.1 PDI Control Register (PDI_CONTROL)

PDI_CONTROL indicates the type of PDI.

	7	6	5	4	3	2	1	0	Address	Initial Value
PDI_CONTROL	PDI								400E 0140H	80H
ECAT	R	R	R	R	R	R	R	R		
PDI	R	R	R	R	R	R	R	R		

Bit Position	Bit Name	Description
7 to 0	PDI	Process Data Interface This LSI indicates the value below. 0x80: On-chip bus

6.12.2 ESC Configuration Register (ESC_CONFIG)

ESC_CONFIG indicates the configuration of EtherCAT slave controller.

	7	6	5	4	3	2	1	0	Address	Initial Value
ESC_CONFIG	ENLP3	ENLP2	ENLP1	ENLP0	DCLATCH	DCSYNC	ENLALLP	DEVEMU	400E 0141H	0CH Note
ECAT	R	R	R	R	R	R	R	R		
PDI	R	R	R	R	R	R	R	R		

Bit Position	Bit Name	Description
7	ENLP3	Enhanced Link Detection of Port 3 (Port 3 is not available on this LSI.) 0: Disabled (if bit 9 at address 0 in the EEPROM is 0) 1: Enabled
6	ENLP2	Enhanced Link Detection of Port 2 (Port 2 is not available on this LSI.) 0: Disabled (if bit 9 at address 0 in the EEPROM is 0) 1: Enabled
5	ENLP1	Enhanced Link Detection of Port 1 0: Disabled (if bit 9 at address 0 in the EEPROM is 0) 1: Enabled
4	ENLP0	Enhanced Link Detection of Port 0 0: Disabled (if bit 9 at address 0 in the EEPROM is 0) 1: Enabled
3	DCLATCH	Distributed Clocks Latch Input Unit This bit is fixed to 1 in this LSI. 0: Disabled (power saving) 1: Enabled
2	DCSYNC	Distributed Clocks SYNC Output Unit This bit is fixed to 1 in this LSI. 0: Disabled (power saving) 1: Enabled
1	ENLALLP	Enhanced Link Detection for All Ports 0: Disabled (if bits 15 to 12 at address 0 in the EEPROM is 0) 1: Enabled for all ports
0	DEVEMU	Device Emulation (Control of AL Status) 0: The AL status register is set by PDI. 1: The AL status register will automatically be set to the value written to the AL control register. This bit is fixed to 0 in this LSI.

Note: This indicates the initial value until the EEPROM is loaded. After that, bits 7 to 4 and 1 change depending on the value stored at address 0x0001 in the EEPROM.
The EEPROM value is only taken over at first EEPROM load after power-on or reset.

6.12.3 PDI Configuration Register (PDI_CONFIG)

PDI_CONFIG indicates the PDI configuration.

	7	6	5	4	3	2	1	0	Address	Initial Value
PDI_CONFIG	ONCHIPBUS			ONCHIPBUSCLK					400E 0150H	44H
ECAT	R	R	R	R	R	R	R	R		
PDI	R	R	R	R	R	R	R	R		

Bit Position	Bit Name	Description
7 to 5	ONCHIPBUS	These bits indicate the type of on-chip bus. These bits always indicate 010 in this LSI.
4 to 0	ONCHIPBUSCLK	These bits indicate the on-chip bus clock. These bits always indicate 4 (100 MHz) in this LSI.

6.12.4 SYNC/LATCH PDI Configuration Register (SYNC_LATCH_CONFIG)

SYNC_LATCH_CONFIG indicates the settings of SYNC output and LATCH input.

	7	6	5	4	3	2	1	0	Address	Initial Value
SYNC_LATCH_CONFIG	SYNC1MAP	SYNCLAT1	SYNC1OUT		SYNC0MAP	SYNCLAT0	SYNC0OUT		400E 0151H	EEH Note 1
ECAT	R	R	R	R	R	R	R	R		
PDI	R	R	R	R	R	R	R	R		

Bit Position	Bit Name	Description
7	SYNC1MAP	SYNC1 Mapped to Bit 3 in AL Event Request Register (AL_EVENT_REQ: 0x0220) This bit always indicates 1 (enabled) in this LSI. 0: Disabled 1: Enabled
6	SYNCLAT1	SYNC1/LATCH1 Configuration This bit always indicates 1 in this LSI. Note 2 0: LATCH1 input 1: SYNC1 output
5, 4	SYNC1OUT	SYNC1 Output Driver/Polarity These bits always indicate 10 (push-pull active high) in this LSI.
3	SYNC0MAP	SYNC0 Mapped to Bit 2 in AL Event Request Register (AL_EVENT_REQ: 0x0220) This bit always indicates 1 (enabled) in this LSI. 0: Disabled 1: Enabled
2	SYNCLAT0	SYNC0/LATCH0 Configuration This bit always indicates 1 in this LSI. Note 2 0: LATCH0 input 1: SYNC0 output
1, 0	SYNC0OUT	SYNC0 Output Driver/Polarity These bits always indicate 10 (push-pull active high) in this LSI.

Notes 1. This indicates the initial value until the EEPROM is loaded. After that, bits 7 and 3 change depending on the value stored at address 0x0003 in the EEPROM.
The EEPROM value is only taken over at first EEPROM load after power-on or reset.
2. Though the bit always indicates SYNC output, Latch input is available. Use the chip level pin multiplex function in order to switch SYNC output to LATCH input, and vice versa.

6.12.5 Extended PDI Configuration Register (EXT_PDI_CONFIG)

EXT_PDI_CONFIG indicates the configuration of extended PDI.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	Initial Value
EXT_PDI_CONFIG	0	0	0	0	0	0	0	0	0	0	0	0	0	0	DATABUSWID		400E 0152H	00H
ECAT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R	R		
PDI	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R	R		

Bit Position	Bit Name	Description
1, 0	DATABUSWID	These bits indicate the data bus width of PDI. These bits always indicate 0 (4 bytes) in This LSI. 00: 4 bytes 01: 1 byte 10: 2 bytes 11: Reserved

6.13 Interrupts Registers

6.13.1 ECAT Event Mask Register (ECAT_EVENT_MASK)

The ECAT event request (ECAT interrupt) is used to transmit the slave event to EtherCAT master. This register is used to set mask to each event of ECAT event request register (ECAT_EVENT_REQ: 0x0210). This register and ECAT event request register are ANDed and it is used as an interrupt.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	Initial Value
ECAT_EVENT_MASK	ECATEVMASK																400E 0200H	0000H
ECAT	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		
PDI	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R		

Bit Position	Bit Name	Description
15 to 0	ECATEVMASK	0: The bit corresponding to the ECAT event request register (ECAT_EVENT_REQ: 0x0210) is not mapped. 1: The bit corresponding to the ECAT event request register is mapped.

6.13.2 AL Event Mask Register (AL_EVENT_MASK)

The AL event request (PDI interrupt) is used to transmit the ESC interrupt to the slave application. This register is used to set mask to each event of AL event request register (AL_EVENT_REQ: 0x0220). This register and AL event request register are ANDed and it is used as an interrupt.

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
AL_EVENT_MASK	ALEVMASK																																400E 0204H Initial Value 00FF FF0FH
ECAT	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	
PDI	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

Bit Position	Bit Name	Description
31 to 0	ALEVMASK	0: The bit corresponding to the AL event request register (AL_EVENT_REQ: 0x0220) is not mapped. 1: The bit corresponding to the AL event request register is mapped.

6.13.3 ECAT Event Request Register (ECAT_EVENT_REQ)

ECAT_EVENT_REQ indicates events of ECAT event request (ECAT interrupt).

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	Initial Value
ECAT_EVENT_REQ	0	0	0	0	SMSTA7	SMSTA6	SMSTA5	SMSTA4	SMSTA3	SMSTA2	SMSTA1	SMSTA0	ALSTA	DLSTA	0	DCLATCH	400E 0210H	0000H
ECAT	0	0	0	0	R	R	R	R	R	R	R	R	R	R	0	R		
PDI	0	0	0	0	R	R	R	R	R	R	R	R	R	R	0	R		

Bit Position	Bit Name	Description
11	SMSTA7	Mirror Value of SyncManager7 Status 0: No Sync Channel 7 event 1: Sync Channel 7 event pending
10	SMSTA6	Mirror Value of SyncManager6 Status 0: No Sync Channel 6 event 1: Sync Channel 6 event pending
9	SMSTA5	Mirror Value of SyncManager5 Status 0: No Sync Channel 5 event 1: Sync Channel 5 event pending
8	SMSTA4	Mirror Value of SyncManager4 Status 0: No Sync Channel 4 event 1: Sync Channel 4 event pending
7	SMSTA3	Mirror Value of SyncManager3 Status 0: No Sync Channel 3 event 1: Sync Channel 3 event pending
6	SMSTA2	Mirror Value of SyncManager2 Status 0: No Sync Channel 2 event 1: Sync Channel 2 event pending
5	SMSTA1	Mirror Value of SyncManager1 Status 0: No Sync Channel 1 event 1: Sync Channel 1 event pending
4	SMSTA0	Mirror Value of SyncManager0 Status 0: No Sync Channel 0 event 1: Sync Channel 0 event pending
3	ALSTA	AL Status Event 0: No change in the AL status 1: The AL status changes This bit is cleared by reading the AL status register (AL_STATUS: 0x0130:0x0131) from ECAT.
2	DLSTA	DL Status Event 0: No change in the DL status 1: The DL status changes This bit is cleared by reading the DL status register (ESC_DL_STATUS: 0x0110:0x0111) from ECAT.

Bit Position	Bit Name	Description
0	DCLATCH	DC Latch Event 0: No change on DC latch inputs 1: At least one change on DC latch inputs This bit is cleared by reading the DC latch event times from ECAT for the ECAT controlled latch units, so that the latch 0/1 status register (DC_LATCH_STAT0/1: 0x09AE:0x09AF) indicates no event.

6.13.4 AL Event Request Register (AL_EVENT_REQ)

AL_EVENT_REQ indicates events of AL event request (PDI interrupt).

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
AL_EVENT_REQ	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	SMINT7	SMNT6	SMINT5	SMINT4	SMINT3	SMINT2	SMINT1	SMINT0	0	WDPD	0	SYNCACT	DCSYNC1STA	DCSYNC0STA	DCLATCH	ALCTRL	400E 0220H
																																	Initial Value
ECAT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R	R	R	R	R	R	R	R	0	R	R	R	R	R	R	R	0000 0000H
PDI	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R	R	R	R	R	R	R	R	0	R	R	R	R	R	R	R	

Bit Position	Bit Name	Description
15	SMINT7	SyncManager 7 Interrupt (bit 0 or 1 in SyncManager status register (0x083D)) 0: No SyncManager 7 interrupt 1: SyncManager 7 interrupt pending
14	SMINT6	SyncManager 6 Interrupt (bit 0 or 1 in SyncManager status register (0x0835)) 0: No SyncManager 6 interrupt 1: SyncManager 6 interrupt pending
13	SMINT5	SyncManager 5 Interrupt (bit 0 or 1 in SyncManager status register (0x082D)) 0: No SyncManager 5 interrupt 1: SyncManager 5 interrupt pending
12	SMINT4	SyncManager 4 Interrupt (bit 0 or 1 in SyncManager status register (0x0825)) 0: No SyncManager 4 interrupt 1: SyncManager 4 interrupt pending
11	SMINT3	SyncManager 3 Interrupt (bit 0 or 1 in SyncManager status register (0x081D)) 0: No SyncManager 3 interrupt 1: SyncManager 3 interrupt pending
10	SMINT2	SyncManager 2 Interrupt (bit 0 or 1 in SyncManager status register (0x0815)) 0: No SyncManager 2 interrupt 1: SyncManager 2 interrupt pending
9	SMINT1	SyncManager 1 Interrupt (bit 0 or 1 in SyncManager status register (0x080D)) 0: No SyncManager 1 interrupt 1: SyncManager 1 interrupt pending
8	SMINT0	SyncManager 0 Interrupt (bit 0 or 1 in SyncManager status register (0x0805)) 0: No SyncManager 0 interrupt 1: SyncManager 0 interrupt pending
6	WDPD	Watchdog Process Data 0: Has not expired 1: Has expired This bit is cleared by reading the watchdog status process data register (WDS_DATA: 0x0440) from PDI.
4	SYNCACT	SyncManager Activation Register (SMm.ACT: 0x0806+8H*m) Changed 0: No change in any SyncManager 1: At least one SyncManager changed This bit is cleared by reading the SyncManager activation register (SMm.ACT) from PDI.
3	DCSYNC1STA	State of DC SYNC1 This bit is cleared by reading the SYNC1 status register (DC_SYNC_STAT1: 0x098F) from PDI.
2	DCSYNC0STA	State of DC SYNC0 This bit is cleared by reading the SYNC0 status register (DC_SYNC_STAT0: 0x098E) from PDI.

Bit Position	Bit Name	Description
1	DCLATCH	DC Latch Event 0: No change on DC latch inputs 1: At least one change on DC latch inputs This bit is cleared by reading the DC latch event times from PDI for the PDI controlled latch units, so that the latch 0/1 status register (DC_LATCH_STAT0/1: 0x09AE:0x09AF) indicates no event.
0	ALCTRL	AL Control Event 0: No change in the AL control register 1: The AL control register has been written This bit is cleared by reading the AL control register (AL_CONTROL: 0x0120:0x0121) from PDI.

6.14 Error Counters Registers

6.14.1 Rx Error Counter n Register (RX_ERR_COUNTn)

RX_ERR_COUNTn counts the number of receive frame errors.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	Initial Value
RX_ERR_COUNTn	RXERRCNT								INVFRMCNT								400E 0300H + 0002H*n	0000H
ECAT	R/W (clr)	R/W (clr)	R/W (clr)	R/W (clr)	R/W (clr)	R/W (clr)	R/W (clr)	R/W (clr)	R/W (clr)	R/W (clr)	R/W (clr)	R/W (clr)	R/W (clr)	R/W (clr)	R/W (clr)	R/W (clr)		
PDI	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R		

Bit Position	Bit Name	Description
15 to 8	RXERRCNT	Receive Error Counter of Port n (Counting is stopped when 0xFF is reached.) These bits count the number of receive errors for the MII interface. These bits are cleared if one of the RX error counters (RX_ERR_COUNTn, FWD_RX_ERR_COUNTn) is written to.
7 to 0	INVFRMCNT	Invalid Frame Counter of Port n (Counting is stopped when 0xFF is reached.) These bits are cleared if one of the RX error counters (RX_ERR_COUNTn, FWD_RX_ERR_COUNTn) is written to.

Remark: n = 0-1
n = 0: Port 0, n = 1: Port 1

6.14.2 Forwarded Rx Error Counter n Register (FWD_RX_ERR_COUNTn)

FWD_RX_ERR_COUNTn counts the number of forwarded frame errors.

	7	6	5	4	3	2	1	0	Address	Initial Value
FWD_RX_ERR_COUNTn	FWDERRCNT								400E 0308H + 0001H*n	00H
ECAT	R/W(clr)	R/W(clr)	R/W(clr)	R/W(clr)	R/W(clr)	R/W(clr)	R/W(clr)	R/W(clr)		
PDI	R	R	R	R	R	R	R	R		

Bit Position	Bit Name	Description
7 to 0	FWDERRCNT	Forwarded Error Counter of Port n (Counting is stopped when 0xFF is reached.) These bits are cleared if one of the RX error counters (RX_ERR_COUNTn, FWD_RX_ERR_COUNTn) is written to.

Remark: n = 0-1
n = 0: Port 0, n = 1: Port 1

6.14.3 ECAT Processing Unit Error Counter Register (ECAT_PROC_ERR_COUNT)

ECAT_PROC_ERR_COUNT counts the number of frame errors passing the ECAT processing unit.

	7	6	5	4	3	2	1	0	Address	Initial Value
ECAT_PROC_ERR_COUNT	EPUERRCNT								400E 030CH	00H
ECAT	R/W(clr)	R/W(clr)	R/W(clr)	R/W(clr)	R/W(clr)	R/W(clr)	R/W(clr)	R/W(clr)		
PDI	R	R	R	R	R	R	R	R		

Bit Position	Bit Name	Description
7 to 0	EPUERRCNT	ECAT Processing Unit Error Counter (Counting is stopped when 0xFF is reached.) These bits count the number of frame errors passing the processing unit. This register is cleared after written.

6.14.4 PDI Error Counter Register (PDI_ERR_COUNT)

PDI_ERR_COUNT counts the number of PDI access errors.

	7	6	5	4	3	2	1	0	Address	Initial Value
PDI_ERR_COUNT	PDIERRCNT								400E 030DH	00H
ECAT	R/W(clr)	R/W(clr)	R/W(clr)	R/W(clr)	R/W(clr)	R/W(clr)	R/W(clr)	R/W(clr)		
PDI	R	R	R	R	R	R	R	R		

Bit Position	Bit Name	Description
7 to 0	PDIERRCNT	PDI Error Counter (Counting is stopped when 0xFF is reached.) These bits count the number of interface errors generated at PDI access. This register is cleared after written.

6.14.5 Lost Link Counter n Register (LOST_LINK_COUNTn)

LOST_LINK_COUNTn counts the number of lost links at port n.

	7	6	5	4	3	2	1	0	Address	Initial Value
LOST_LINK_COUNTn	LOSTLINKCNT								400E 0310H + 0001H*n	00H
ECAT	R/W(clr)	R/W(clr)	R/W(clr)	R/W(clr)	R/W(clr)	R/W(clr)	R/W(clr)	R/W(clr)		
PDI	R	R	R	R	R	R	R	R		

Bit Position	Bit Name	Description
7 to 0	LOSTLINKCNT	Lost Link Counter of Port n (Counting is stopped when 0xff is reached.) These bits count the number of lost links only when a port loop is at "Auto" or "Auto-Close" state, and only lost links at open ports are counted. This register is cleared if one of the lost link counter registers is written to.

Remark: n = 0-1
n = 0: Port 0, n = 1: Port 1

6.15 Watchdogs Registers

6.15.1 Watchdog Divider Register (WD_DIVIDE)

WD_DIVIDE is used to set the divider ratio for 25 MHz as the basic watchdog increment.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	Initial Value
WD_DIVIDE	WDDIV																400E 0400H	09C2H
ECAT	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		
PDI	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R		

Bit Position	Bit Name	Description
15 to 0	WDDIV	These bits set the divider ratio of watchdog clocks for 25 MHz. The clock cycles divided by the "setting value + 2" represent the basic watchdog increment. The default value is 100 µs = 2498.

6.15.2 Watchdog Time PDI Register (WDT_PDI)

WDT_PDI is used to set the overflow time of PDI watchdog.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	Initial Value
WDT_PDI	WDTIMPDI																400E 0410H	03E8H
ECAT	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		
PDI	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R		

Bit Position	Bit Name	Description
15 to 0	WDTIMPDI	These bits set the overflow time of PDI watchdog as the number of basic watchdog increments. The default value with watchdog divider 100 µs means 100 µs x 1000 = 100 ms watchdog. The watchdog is disabled if these bits are set to 0. The watchdog is restarted with every PDI access.

6.15.3 Watchdog Time Process Data Register (WDT_DATA)

WDT_DATA is used to set the overflow time of process data watchdog.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	Initial Value
WDT_DATA	WDTIMPD																400E 0420H	03E8H
ECAT	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		
PDI	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R		

Bit Position	Bit Name	Description
15 to 0	WDTIMPD	These bits set the overflow time of the process data watchdog as the number of basic watchdog increments. The default value with watchdog divider 100 µs means 100 µs x 1000 = 100 ms watchdog. There is one watchdog for all SyncManagers. The watchdog is disabled if these bits are set to 0. The watchdog is restarted with every write access to SyncManagers with the watchdog trigger enable bit set.

6.15.4 Watchdog Status Process Data Register (WDS_DATA)

WDS_DATA indicates the status of process data watchdog.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	Initial Value
WDS_DATA	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	WDSTAPD	400E 0440H	0000H
ECAT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R		
PDI	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R (ack)		

Bit Position	Bit Name	Description
0	WDSTAPD	This bit indicates the status of process data watchdog triggered by SyncManagers. 0: The process data watchdog is expired. 1: The process data watchdog is active or disabled. Reading this register clears bit 6 in the AL event request register (AL_EVENT_REQ: 0x0220).

6.15.5 Watchdog Counter Process Data Register (WDC_DATA)

WDC_DATA indicates the number of timeout counts of process data watchdog.

	7	6	5	4	3	2	1	0	Address	Initial Value
WDC_DATA	WDCNTPD								400E 0442H	00H
ECAT	R/W(clr)	R/W(clr)	R/W(clr)	R/W(clr)	R/W(clr)	R/W(clr)	R/W(clr)	R/W(clr)		
PDI	R	R	R	R	R	R	R	R		

Bit Position	Bit Name	Description
7 to 0	WDCNTPD	These bits indicate the number of timeout counts of process data watchdog. (Counting is stopped when 0xFF is reached). Counting starts if the process data watchdog expires. The counter is cleared if one of the watchdog counter registers (WDC_DATA, WDC_PDI: 0x0442:0x0443) is written to.

6.15.6 Watchdog Counter PDI Register (WDC_PDI)

WDC_PDI indicates the number of timeout counts of PDI watchdog.

	7	6	5	4	3	2	1	0	Address	Initial Value
WDC_PDI	WDCNTPDI								400E 0443H	00H
ECAT	R/W(clr)	R/W(clr)	R/W(clr)	R/W(clr)	R/W(clr)	R/W(clr)	R/W(clr)	R/W(clr)		
PDI	R	R	R	R	R	R	R	R		

Bit Position	Bit Name	Description
7 to 0	WDCNTPDI	These bits indicate the number of timeout counts of PDI watchdog. (Counting is stopped when 0xFF is reached.) The counter is cleared if one of the watchdog counter registers (WDC_DATA, WDC_PDI: 0x0442:0x0443) is written to.

6.16 SII EEPROM Interface Registers

EtherCAT controls the SII EEPROM interface if bit 0 in the EEPROM configuration register (EEP_CONF: 0x0500) is 0 and bit 0 in the EEPROM PDI access state register (EEP_PDI_ACCESS: 0x0501) is 0. Otherwise PDI controls the EEPROM interface.

6.16.1 EEPROM Configuration Register (EEP_CONF)

EEP_CONF is used to configure the EEPROM access.

	7	6	5	4	3	2	1	0	Address	Initial Value
EEP_CONF	0	0	0	0	0	0	FORCEECAT	CTRLPDI	400E 0500H	00H
ECAT	0	0	0	0	0	0	R/W	R/W		
PDI	0	0	0	0	0	0	R	R		

Bit Position	Bit Name	Description
1	FORCEECAT	Changes forcibly to the access from ECAT. 0: Unchanged from the current state 1: Bit 0 in the EEPROM PDI access state register (EEP_PDI_ACCESS: 0x0501) is reset to 0. That is, the EEPROM access control from PDI is released.
0	CTRLPDI	Specifies whether the EEPROM control is offered to PDI. 0: PDI does not have the EEPROM control 1: PDI has the EEPROM control

6.16.2 EEPROM PDI Access State Register (EEP_STATE)

EEP_STATE is used to configure the EEPROM access from PDI.

	7	6	5	4	3	2	1	0	Address	Initial Value
EEP_STATE	0	0	0	0	0	0	0	PDIACCESS	400E 0501H	00H
ECAT	0	0	0	0	0	0	0	R		
PDI	0	0	0	0	0	0	0	R/(W)		

Bit Position	Bit Name	Description
0	PDIACCEES	Specifies the access control to EEPROM. 0: PDI releases the EEPROM access. 1: PDI has the EEPROM control. Writing from PDI is only enabled when bits 0 and 1 in the EEPROM configuration register (EEP_CONF: 0x0500) are set to 1 and 0, respectively.

6.16.3 EEPROM Control/Status Register (EEP_CONT_STAT)

EEP_CONT_STAT is used to control the EEPROM access and indicate the status.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	Initial Value
EEP_CONT_STAT	BUSY	WRENERR	ACKCMDERR	LOADSTA	CKSUMERR	COMMAND			PROMSIZE	READBYTE	0	0	0	0	0	ECATWREN	400E 0502H	0000H
ECAT	R	R	R	R	R	R/(W)	R/(W)	R/(W)	R	R	0	0	0	0	0	R/(W)		
PDI	R	R	R	R	R	R/(W)	R/(W)	R/(W)	R	R	0	0	0	0	0	R		

Bit Position	Bit Name	Description
15	BUSY	Indicates the busy state of the EEPROM interface 0: The EEPROM interface is idle 1: The EEPROM interface is busy
14	WRENERR	Indicates the write enable error[Note1] 0: No error 1: Write command without write enable
13	ACKCMDERR	Indicates the acknowledge/command error[Note1] 0: No error 1: Missing EEPROM acknowledge or invalid command
12	LOADSTA	Indicates the EEPROM loading status 0: EEPROM loaded, device information has no error 1: EEPROM not loaded, device information not available (EEPROM loading in progress or finished with a failure)
11	CKSUMERR	Indicates the checksum error in the ESC configuration area 0: Checksum has no error 1: Checksum error
10 to 8	COMMAND	Command[Note2] Write: Initiates the command below Read: Indicates the currently executed command Commands: 000: No command/EEPROM idle (clear error bits) 001: Read 010: Write 100: Reload Others: Reserved/invalid commands (do not issue)
7	PROMSIZE	Indicates the selected EEPROM algorithm 0: 1 address byte (1 Kbit – 16 Kbit EEPROMs) 1: 2 address bytes (32 Kbit – 4 Mbit EEPROMs)
6	READBYTE	Indicates the supported number of EEPROM read bytes 0: 4 bytes 1: 8 bytes
0	ECATWREN	ECAT Write Enable[Note2] 0: Write requests are disabled 1: Write requests are enabled This bit is always 1 if PDI has EEPROM control.

Remark: Write access depends on the assignment of the EEPROM interface (ECAT/PDI). Write access is generally blocked if the EEPROM interface is busy (bit 15 = 1).

Notes 1. The error bits are cleared by writing "000" (or any valid command) to command bits 10 to 8.

2. The ECAT write enable bit 0 is self-cleared at the SOF of the next frame, and command bits 10 to 8 are also self-cleared after the command is executed (after the EEPROM busy ends). Writing "000" to command bits 10 to 8 will clear the error bits 14 and 13. Command bits 10 to 8 are ignored, if the acknowledge/command error bit 13 is 1.

6.16.4 EEPROM Address Register (EEP_ADR)

EEP_ADR is used to set the EEPROM address to be accessed.

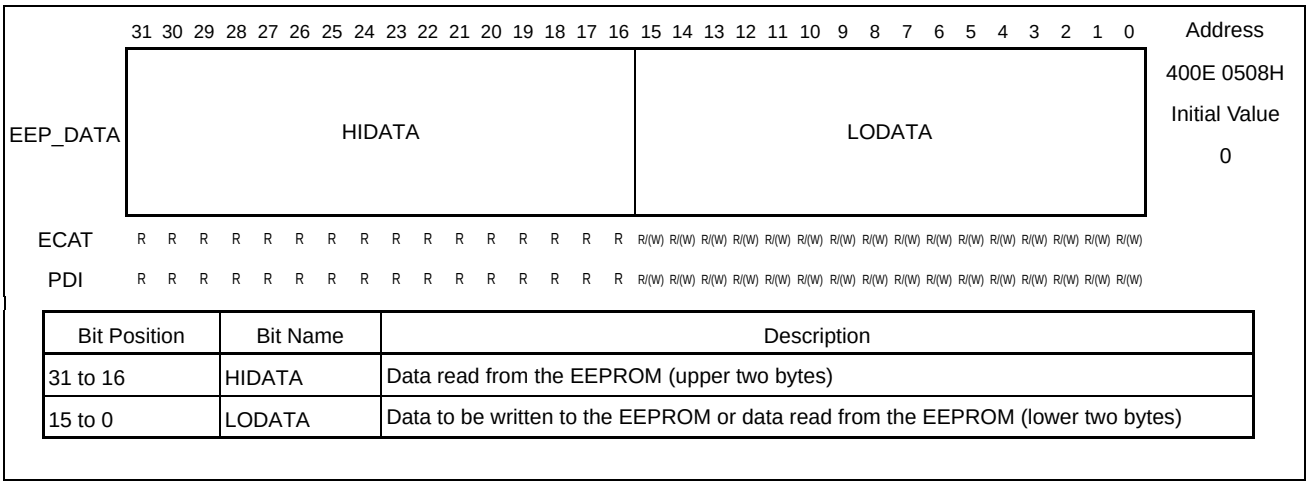
	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
EEP_ADR	ADDRESS																																400E 0504H
Initial Value	0000 0000H																																
ECAT	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	
PDI	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	

Bit Position	Bit Name	Description
31 to 0	ADDRESS	EEPROM Address 0: First word (= 16 bits) 1: Second word ... Actually used EEPROM address bits: [9:0]: EEPROM size up to 16 Kbits [17:0]: 32 Kbit – 4 Mbit EEPROM size

Remark: Write access depends on the assignment of the EEPROM interface (ECAT/PDI). Write access is generally blocked if the EEPROM interface is busy (bit 15 in the EEPROM control/status register (EEP_CONT_STAT: 0x0502) is 1).

6.16.5 EEPROM Data Register (EEP_DATA)

EEP_DATA is used to set write data to the EEPROM or indicates read data from the EEPROM. This register can be written in one word and read in two words.



Bit Position	Bit Name	Description
31 to 16	HIDATA	Data read from the EEPROM (upper two bytes)
15 to 0	LODATA	Data to be written to the EEPROM or data read from the EEPROM (lower two bytes)

Remark: Write access depends on the assignment of the EEPROM interface (ECAT/PDI). Write access is generally blocked if the EEPROM interface is busy (bit 15 in the EEPROM control/status register (EEP_CONT_STAT: 0x0502) is 1).

6.17 MII Management Interface Registers

6.17.1 MII Management Control/Status Register (MII_CONT_STAT)

MII_CONT_STAT is used to control the MII management interface and to indicate the status.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	Initial Value
MII_CONT_STAT	BUSY	CMDERR	READERR	0	0	0	COMMAND		PHYOFFSET					MILINK	PDICTRL	WREN	400E 0510H	0006H
ECAT	R	R	R/(W)	0	0	0	R/(W)	R/(W)	R	R	R	R	R	R	R	R/(W)		
PDI	R	R	R/(W)	0	0	0	R/(W)	R/(W)	R	R	R	R	R	R	R	R		

Bit Position	Bit Name	Description
15	BUSY	Indicates that the MII management interface is busy. 0: The MII management interface is idle 1: The MII management interface is busy
14	CMDERR	Indicates the generation of a command error. 0: The last command was successful 1: Invalid command or write command without write enable This bit is cleared with a valid command or by writing "00" to command bits 9 and 8.
13	READERR	Indicates the generation of a read error. 0: No read error 1: Read error occurred (PHY or register not available) This bit is cleared by writing to this register.
9, 8	COMMAND	Command Write: Initiates the command below Read: Indicates the currently executed command Commands: 00: No command/MI idle (clear error bits) 01: Read 10: Write Others: Reserved/invalid commands (do not issue)
7 to 3	PHYOFFSET	Indicates the PHY address offset.
2	MILINK	Indicates whether the MI link detection can be used. 0: Not available 1: Available
1	PDICTRL	Indicates that whether the MII management interface control is offered to PDI. 0: ECAT only has the control 1: PDI also has the control This bit is controlled by the MII management ECAT access state register (MII_ECAT_ACS_STAT: 0x0516) and the MII management PDI access state register (MII_PDI_ACS_STAT: 0x0517).
0	WREN	Write Enable 0: Write disabled 1: Write enabled This bit is always 1 if PDI has the MII management interface control.

Remark: Write access depends on the assignment of the management interface (ECAT/PDI). Write access is generally blocked if the management interface is busy (bit 15 in this register is 1).

Note: The write enable bit 0 is self-cleared at the SOF of the next frame (or at the end of the PDI access), and command bits 9 and 8 are also self-cleared after the command is executed (after the busy ends).
Writing "00" to command bits will clear the error bits 14 and 13. The command bits are cleared after the command is executed.

6.17.2 PHY Address Register (PHY_ADR)

PHY_ADR is used to set the PHY address.

	7	6	5	4	3	2	1	0	Address	Initial Value
PHY_ADR	0	0	0	PHYADDR					400E 0512H	00H
ECAT	0	0	0	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)		
PDI	0	0	0	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)		

Bit Position	Bit Name	Description
4 to 0	PHYADDR	PHY Address

Remark: Write access depends on the assignment of the management interface (ECAT/PDI). Write access is generally blocked if the management interface is busy (bit 15 in the MII management control/status register (MII_CONT_STAT: 0x0510) is 1).

6.17.3 PHY Register Address Register (PHY_REG_ADR)

PHY_REG_ADR is used to set the PHY register address.

	7	6	5	4	3	2	1	0	Address	Initial Value
PHY_REG_ADR	0	0	0	PHYREGADDR					400E 0513H	00H
ECAT	0	0	0	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)		
PDI	0	0	0	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)		

Bit Position	Bit Name	Description
4 to 0	PHYREGADDR	Address of the PHY register

Remark: Write access depends on the assignment of the management interface (ECAT/PDI). Write access is generally blocked if the management interface is busy (bit 15 in the MII management control/status register (MII_CONT_STAT: 0x0510) is 1).

6.17.4 PHY Data Register (PHY_DATA)

PHY_DATA is used to set data to write to the PHY register or to indicate read data from the PHY register.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	Initial Value
PHY_DATA	PHYREGDATA																400E 0514H	0000H
ECAT	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)		
PDI	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)		

Bit Position	Bit Name	Description
15 to 0	PHYREGDATA	PHY Read/Write Data

Remark: Write access depends on the assignment of the management interface (ECAT/PDI). Write access is generally blocked if the management interface is busy (bit 15 in the MII management control/status register (MII_CONT_STAT: 0x0510) is 1).

6.17.5 MII Management ECAT Access State Register (MII_ECAT_ACS_STAT)

MII_ECAT_ACS_STAT is used to set the access state of MII management interface.

	7	6	5	4	3	2	1	0	Address	Initial Value
MII_ECAT_ACS_STAT	0	0	0	0	0	0	0	ACSMII	400E 0516H	00H
ECAT	0	0	0	0	0	0	0	R/(W)		
PDI	0	0	0	0	0	0	0	R		

Bit Position	Bit Name	Description
0	ACSMII	Access to MII Management Interface 0: ECAT enables the PDI access to the MII management interface 1: ECAT claims the exclusive access to the MII management interface

Remark: Write access is only enabled when bit 0 in the MII management PDI access state register (MII_PDI_ACS_STAT: 0x0517) is 0.

6.17.6 MII Management PDI Access State Register (MII_PDI_ACS_STAT)

MII_PDI_ACS_STAT is used to set the access state of MII management interface.

	7	6	5	4	3	2	1	0	Address	Initial Value
MII_PDI_ACS_STAT	0	0	0	0	0	0	FORPDI	ACSMII	400E 0517H	00H
ECAT	0	0	0	0	0	0	R/W	R		
PDI	0	0	0	0	0	0	R	R/(W)		

Bit Position	Bit Name	Description
1	FORPDI	Forced Change of PDI Access State (Change Bit 0 Forcibly) 0: Do not change bit 0 1: Reset bit 0 to 0 (changed to ECAT access)
0	ACSMII	Access to MII Management Interface 0: ECAT has access to MII management interface 1: PDI has access to MII management interface

Remark: Write access to bit 0 from the PDI is only possible when the following two conditions are satisfied.
- **Bit 0 in the MII management ECAT access state register (MII_ECAT_ACS_STAT: 0x0516) and**
- **bit 1 in the MII management PDI access state register (MII_PDI_ACS_STAT: 0x0517) are 0.**

6.17.7 PHY Port Status n Register (PHY_STATUSn)

PHY_STATUSn indicates the PHY port status for each port.

	7	6	5	4	3	2	1	0	Address	Initial Value
PHY_ STATUSn	0	0	PHYCONFIG	LINKPARTERR	READERR	LINKSTAERR	LINKSTA	PHYLINKSTA	400E 0518H + 0001H*n	00H
ECAT	0	0	R/(W/clr)	R	R/(W/clr)	R	R	R		
PDI	0	0	R/(W/clr)	R	R/(W/clr)	R	R	R		

Bit Position	Bit Name	Description
5	PHYCONFIG	PHY Configuration Updated 0: Not updated 1: PHY configuration was updated This bit is cleared by writing any value to at least one of the PHY port status n registers (PHY_STATUSn) (n = 0, 1).
4	LINKPARTERR	Link Partner Error 0: No error detected 1: Link partner error
3	READERR	Read Error 0: No read error occurred 1: A read error has occurred This bit is cleared by writing any value to at least one of the PHY port status n registers (PHY_STATUSn) (n = 0, 1).
2	LINKSTAERR	Link Status Error 0: No error 1: Link error, or link inhibited state
1	LINKSTA	Link Status for 100 Mbit/s, Full Duplex, and Auto-negotiation 0: No link under the corresponding condition 1: Link detected under the corresponding condition
0	PHYLINKSTA	Physical Link Status (Bit 2 in PHY Register 1 (Status Register)) 0: No physical link 1: Physical link detected

Remarks 1. n = 0, 1
n = 0: Port 0, n = 1: Port 1
2. Write access depends on the assignment of the management interface (ECAT/PDI).

6.18 FMMU Registers

6.18.1 FMMU Logical Start Address Register m (FMMUm.L_START_ADR)

FMMUm.L_START_ADR is used to set the logical start address within the EtherCAT address space for FMMU.

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
FMMUm.L_START_ADR	LSTAADR																																400E 0600H + 0010H*m Initial Value 0000 0000H
ECAT	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
PDI	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	

Bit Position	Bit Name	Description
31 to 0	LSTAADR	These bits indicate the logical start address within the EtherCAT address space.

Remark: m = 0 to 7

6.18.2 FMMU Length Register m (FMMUm.LEN)

FMMUm.LEN is used to set the length for FMMU area in bytes.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	Initial Value
FMMUm.LEN	FMMULEN																400E 0604H + 0010H*m	0000H
ECAT	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		
PDI	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R		

Bit Position	Bit Name	Description
15 to 0	FMMULEN	These bits specify the length for the area in bytes. Logical end address specified by FMMU – Logical start address specified by FMMU + 1

Remark: m = 0 to 7

6.18.3 FMMU Logical Start Bit Register m (FMMUm.L_START_BIT)

FMMUm.L_START_BIT is used to set the start bit in the logical start address for FMMU.

	7	6	5	4	3	2	1	0	Address	Initial Value
FMMUm.L_START_BIT	0	0	0	0	0	LSTABIT			400E 0606H + 0010H*m	00H
ECAT	0	0	0	0	0	R/W	R/W	R/W		
PDI	0	0	0	0	0	R	R	R		

Bit Position	Bit Name	Description
2 to 0	LSTABIT	These bits specify the start bit in the logical start address for FMMU.

Remark: m = 0 to 7

6.18.4 FMMU Logical Stop Bit Register m (FMMUm.L_STOP_BIT)

FMMUm.L_STOP_BIT is used to set the end bit in the logical end address for FMMU.

	7	6	5	4	3	2	1	0	Address	Initial Value
FMMUm.L_STOP_BIT	0	0	0	0	0	LSTPBIT			400E 0607H + 0010H*m	00H
ECAT	0	0	0	0	0	R/W	R/W	R/W		
PDI	0	0	0	0	0	R	R	R		

Bit Position	Bit Name	Description
2 to 0	LSTPBIT	These bits specify the end bit in the logical end address for FMMU.

Remark: m = 0 to 7

6.18.5 FMMU Physical Start Address Register m (FMMUm.P_START_ADR)

FMMUm.P_START_ADR is used to set the physical start address of the ESC that is mapped to the logical start address for FMMU.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	Initial Value
FMMUm.P_START_ADR	PHYSTAADR																400E 0608H + 0010H*m	0000H
ECAT	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		
PDI	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R		

Bit Position	Bit Name	Description
15 to 0	PHYSTAADR	These bits specify the physical start address that is mapped to the logical start address. The address is specified by the offset to the base address (400E 0000H).

Remark: m = 0 to 7

6.18.6 FMMU Physical Start Bit Register m (FMMUm.P_START_BIT)

FMMUm.P_START_BIT is used to set the start bit of the physical start address of the ESC that is mapped to the start bit of the logical start address for FMMU.

	7	6	5	4	3	2	1	0	Address	Initial Value
FMMUm.P_START_BIT	0	0	0	0	0	PHYSTABIT			400E 060AH + 0010H*m	00H
ECAT	0	0	0	0	0	R/W	R/W	R/W		
PDI	0	0	0	0	0	R	R	R		

Bit Position	Bit Name	Description
2 to 0	PHYSTABIT	These bits specify the start bit of the physical start address that is mapped to the start bit of the logical start address.

Remark: m = 0 to 7

6.18.7 FMMU Type Register m (FMMUm.TYPE)

FMMUm.TYPE is used to set the FMMU access type.

	7	6	5	4	3	2	1	0	Address	Initial Value
FMMUm.TYPE	0	0	0	0	0	0	WRITE	READ	400E 060BH + 0010H*m	00H
ECAT	0	0	0	0	0	0	R/W	R/W		
PDI	0	0	0	0	0	0	R	R		

Bit Position	Bit Name	Description
1	WRITE	Specifies the write access mapping. 0: Ignores the mapping for write accesses 1: Use the mapping for write accesses
0	READ	Specifies the read access mapping. 0: Ignores the mapping for read accesses 1: Use the mapping for read accesses

Remark: m = 0 to 7

6.18.8 FMMU Activate Register m (FMMUm.ACT)

FMMUm.ACT is used to activate the FMMU.

	7	6	5	4	3	2	1	0	Address	Initial Value
FMMUm.ACT	0	0	0	0	0	0	0	ACTIVATE	400E 060CH + 0010H*m	00H
ECAT	0	0	0	0	0	0	0	R/W		
PDI	0	0	0	0	0	0	0	R		

Bit Position	Bit Name	Description
0	ACTIVATE	Activates the FMMU. 0: FMMU deactivated 1: FMMU activated

Remark: m = 0 to 7

6.19 SyncManager Registers

6.19.1 SyncManager Physical Start Address Register m (SMm.P_START_ADR)

SMm.P_START_ADR is used to set the physical start address of area assigned to SyncManager.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	Initial Value
SMm. P_START_ADR	SMSTAADDR																400E 0800H + 0008H*m	0000H
ECAT	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)		
PDI	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R		

Bit Position	Bit Name	Description
15 to 0	SMSTAADDR	These bits specify the physical start address of area assigned for SyncManager.

Remarks 1. m = 0 to 7

2. This register can be written to only when SyncManager is disabled (bit 0 in the SyncManager activate register m (SMm.ACT: 0x0806+8*m) is 0).

6.19.2 SyncManager Length Register m (SMm.LEN)

SMm.LEN is used to set the length for SyncManager area in bytes.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	Initial Value
SMm. LEN	SMLEN																400E 0802H + 0008H*m	0000H
ECAT	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)		
PDI	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R		

Bit Position	Bit Name	Description
15 to 0	SMLEN	These bits specify the number of bytes assigned to SyncManager. The number shall be greater than 1, otherwise SyncManager is not activated.

Remarks 1. m = 0 to 7

2. This register can be written to only when SyncManager is disabled (bit 0 in the SyncManager activate register m (SMm.ACT: 0x0806+8*m) is 0).

6.19.3 SyncManager Control Register m (SMm.CONTROL)

SMm.CONTROL is used to control the operation of SyncManager.

	7	6	5	4	3	2	1	0	Address	Initial Value
SMm. CONTROL	0	WDTRGEN	IRQPDI	IRQECAT	DIR		OPEMODE		400E 0804H + 0008H*m	00H
ECAT	0	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)		
PDI	0	R	R	R	R	R	R	R		

Bit Position	Bit Name	Description
6	WDTRGEN	Watchdog Trigger Enable 0: Disabled 1: Enabled
5	IRQPDI	Interrupt (PDI Interrupt) Setting by the AL Event Request Register (AL_EVENT_REQ: 0x0220) 0: Disabled 1: Enabled
4	IRQECAT	Interrupt (ECAT Interrupt) Setting by the ECAT Event Request Register (ECAT_EVENT_REQ: 0x0210) 0: Disabled 1: Enabled
3, 2	DIR	Transfer Direction 00: Read (ECAT: Read access, PDI: Write access) 01: Write (ECAT: Write access, PDI: Read access) Others: Reserved
1, 0	OPEMODE	Operating Mode 00: Buffer mode (3 buffer mode) 10: Mailbox mode (Single buffer mode) Others: Reserved

Remarks 1. m = 0 to 7

2. This register can be written to only when SyncManager is disabled (bit 0 in the SyncManager activate register m (SMm.ACT: 0x0806+8*m) is 0).

6.19.4 SyncManager Status Register m (SMm.STATUS)

SMm.STATUS indicates the status of SyncManager.

	7	6	5	4	3	2	1	0	Address	Initial Value
SMm. STATUS	WRBUF	RDBUF	BUFFERED		MAILBOX	0	INTRD	INTWR	400E 0805H + 0008H*m	30H
ECAT	R	R	R	R	R	0	R	R		
PDI	R	R	R	R	R	0	R	R		

Bit Position	Bit Name	Description
7	WRBUF	Indicates that the buffer is being written.
6	RDBUF	Indicates that the buffer is being read.
5, 4	BUFFERED	These bits indicate the state of buffer in buffer mode. (The last written buffer is indicated.) 00: First buffer 01: Second buffer 10: Third buffer 11: No buffer is written These bits are not used in mailbox mode.
3	MAILBOX	Indicates the state of mailbox in mailbox mode. 0: Mailbox is empty 1: Mailbox is full This bit is not used in buffer mode.
1	INTRD	Indicates the read completion interrupt. 0: First byte of the buffer was written (interrupt is cleared) 1: Buffer reading is completed without any errors.
0	INTWR	Indicates the write completion interrupt. 0: First byte of the buffer was read (interrupt is cleared) 1: Buffer writing is completed without any errors.

Remark: m = 0 to 7

6.19.5 SyncManager Activate Register m (SMm.ACT)

SMm.ACT is used to activate the operation of SyncManager.

	7	6	5	4	3	2	1	0	Address	Initial Value
SMm.ACT	LATCHPDI	LATCHECAT	0	0	0	0	REPEATREQ	SMEN	400E 0806H + 0008H*m	00H
ECAT	R/W	R/W	0	0	0	0	R/W	R/W		
PDI	R(ack)	R(ack)	0	0	0	0	R(ack)	R(ack)		

Bit Position	Bit Name	Description
7	LATCHPDI	Latch Event in PDI 0: None 1: Latch events are generated if the PDI issues a buffer exchange or accesses the buffer start address
6	LATCHECAT	Latch Event in ECAT 0: None 1: Latch events are generated if the EtherCAT master issues a buffer exchange
1	REPEATREQ	Repeat Request A toggle of the repeat request means that a mailbox retry is needed (primarily used in conjunction with the ECAT read mailbox)
0	SMEN	SyncManager Enable/Disable 0: Disabled: Memory is accessed without SyncManager control 1: Enabled: SyncManager is active and controls the memory area set in configuration

Remarks 1. m = 0 to 7

2. Reading this register from the PDI in all SyncManagers which have changed activation clears bit 4 in the AL event request register (AL_EVENT_REQ: 0x0220).

6.19.6 SyncManager PDI Control Register m (SMm.PDI_CONT)

SMm.PDI_CONT is used to control SyncManager from the PDI.

	7	6	5	4	3	2	1	0	Address	Initial Value
SMm. PDI_CONT	0	0	0	0	0	0	REPEATACK	DEACTIVE	400E 0807H + 0008H*m	00H
ECAT	0	0	0	0	0	0	R	R		
PDI	0	0	0	0	0	0	R/W	R/W		

Bit Position	Bit Name	Description
1	REPEATACK	Repeat Acknowledge If this bit is set to the same value as bit 1 (repeat request) in the SyncManager activate register (SMm.ACT: 0x0806+8*m), the PDI acknowledges the repeat request.
0	DEACTIVE	Deactivates SyncManager. Read: 0: Normal operation, SyncManager is activated. 1: SyncManager is deactivated and reset. SyncManager locks access to the memory area. Write: 0: SyncManager is activated. 1: SyncManager is deactivated.[Note]

Remark: m = 0 to 7

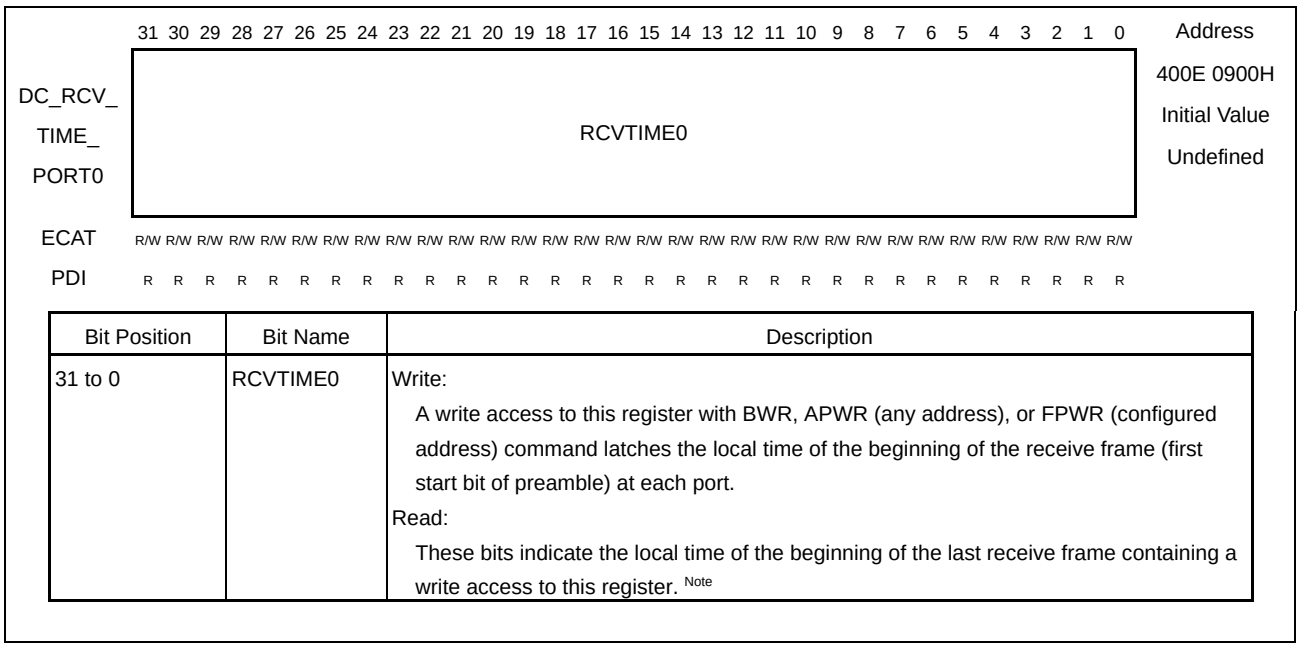
Note: Writing 1 is delayed until the end of a frame which is currently processed.

6.20 Distributed Clocks Registers

6.20.1 DC Receive Time Registers

6.20.1.1 Receive Time Port 0 Register (DC_RCV_TIME_PORT0)

DC_RCV_TIME_PORT0 is used to latch receive time of the frame at all ports if this register is written to, and to indicate the receive time latched at port 0 if this register is read.

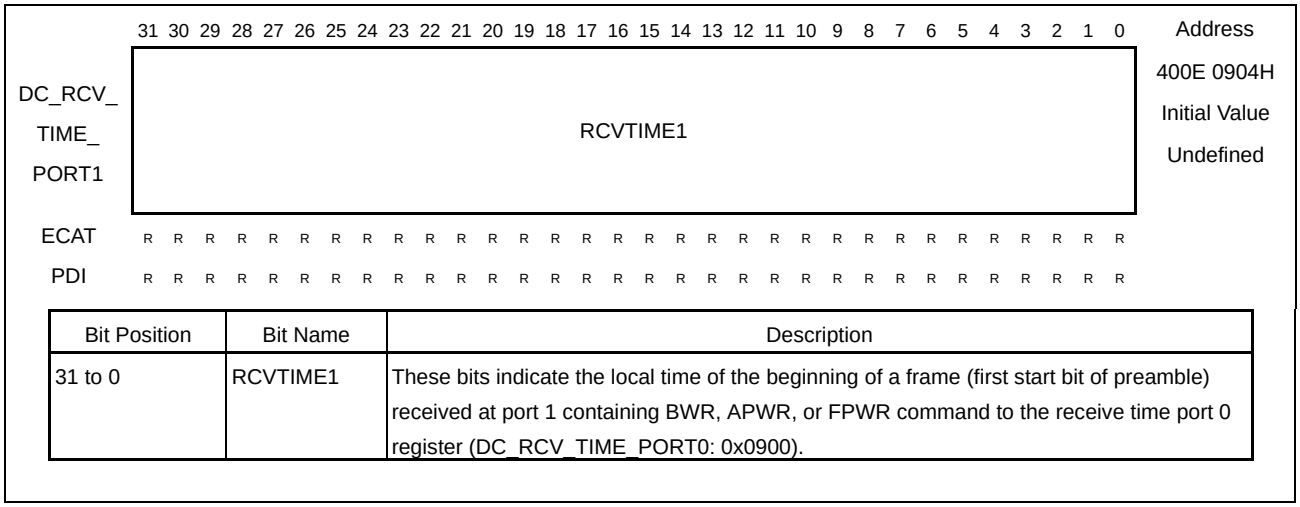


Bit Position	Bit Name	Description
31 to 0	RCVTIME0	Write: A write access to this register with BWR, APWR (any address), or FPWR (configured address) command latches the local time of the beginning of the receive frame (first start bit of preamble) at each port. Read: These bits indicate the local time of the beginning of the last receive frame containing a write access to this register. Note

Note: The time stamps cannot be read in the same frame in which this register was written.

6.20.1.2 Receive Time Port 1 Register (DC_RCV_TIME_PORT1)

DC_RCV_TIME_PORT1 indicates received time of the frame latched at port 1.



Bit Position	Bit Name	Description
31 to 0	RCVTIME1	These bits indicate the local time of the beginning of a frame (first start bit of preamble) received at port 1 containing BWR, APWR, or FPWR command to the receive time port 0 register (DC_RCV_TIME_PORT0: 0x0900).

6.20.2 DC Time Loop Control Unit Registers

6.20.2.1 System Time Register (DC_SYS_TIME)

DC_SYS_TIME indicates the local copy of the system time.

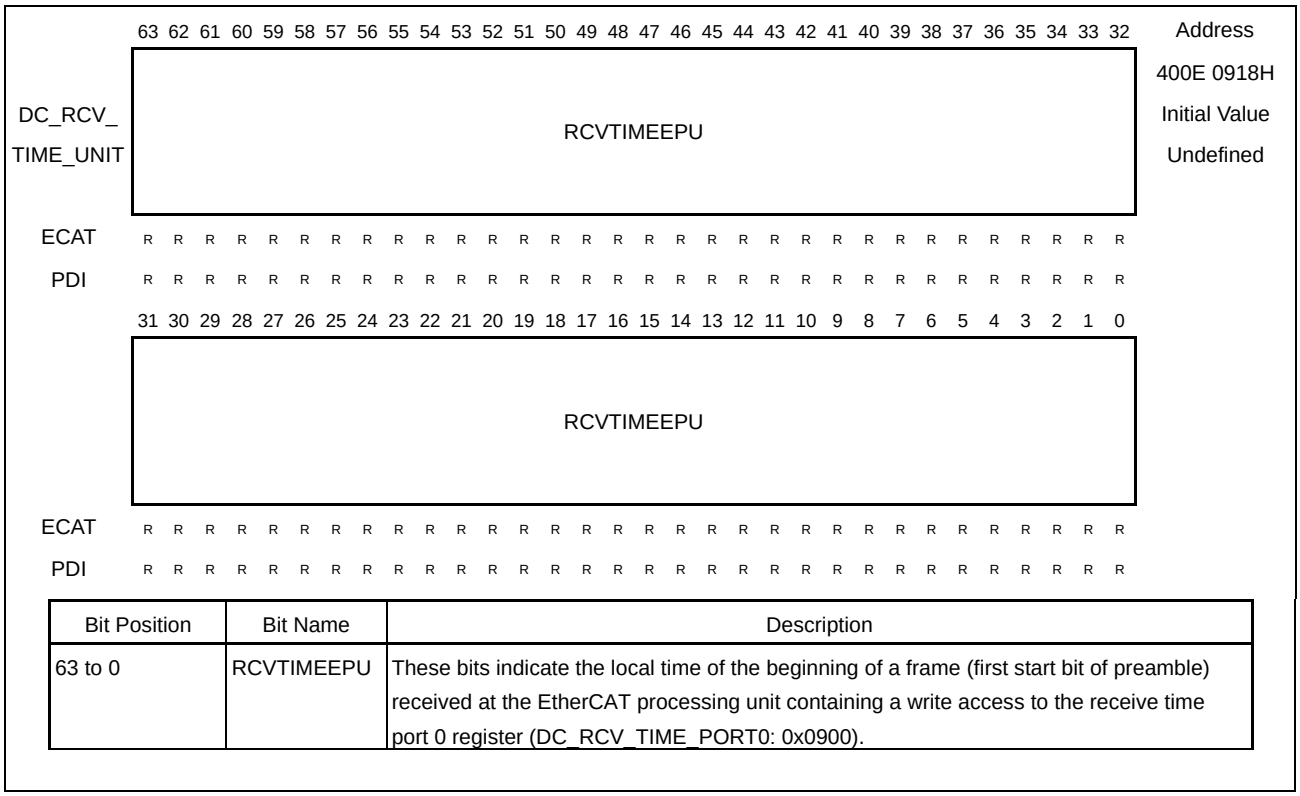
	63 62 61 60 59 58 57 56 55 54 53 52 51 50 49 48 47 46 45 44 43 42 41 40 39 38 37 36 35 34 33 32	Address
DC_SYS_TIME	SYSTIME	400E 0910H
		Initial Value
		0000 0000
		0000 0000H
ECAT	R R R R R R R R R R R R R R R R R R R R R R R R R R R R	
PDI	R R R R R R R R R R R R R R R R R R R R R R R R R R R R	

	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	SYSTIME
ECAT	R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W
PDI	R R R R R R R R R R R R R R R R R R R R R R R R R R R R

Bit Position	Bit Name	Description
63 to 0	SYSTIME	Access from the ECAT Read: These bits indicate the local copy of the system time, including the system time delay, when the frame passed the reference clock. The time latched at beginning of the frame (SOF) is indicated. Write: The written value will be compared with the local copy of the system time. The result is input to the time control loop unit.
		Access from the PDI Read: These bits indicate the local copy of the system time. The time latched when the first byte of this register is read is indicated.

6.20.2.2 Receive Time ECAT Processing Unit Register (DC_RCV_TIME_UNIT)

DC_RCV_TIME_UNIT indicates received time of the frame latched at the EtherCAT processing unit.

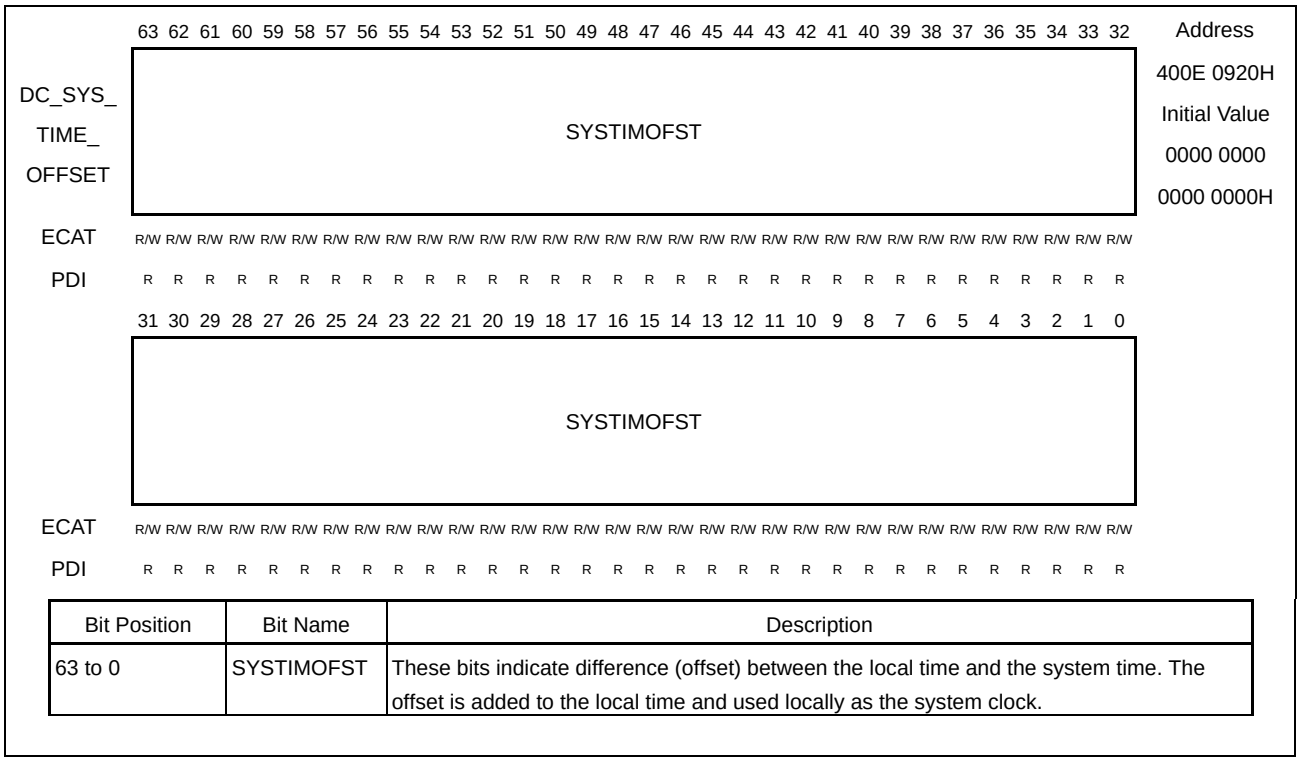


Bit Position	Bit Name	Description
63 to 0	RCVTIMEEPU	These bits indicate the local time of the beginning of a frame (first start bit of preamble) received at the EtherCAT processing unit containing a write access to the receive time port 0 register (DC_RCV_TIME_PORT0: 0x0900).

Remark: If port 0 is open, this register reflects the receive time port 0 register (DC_RCV_TIME_PORT0: 0x0900) in 64 bits.

6.20.2.3 System Time Offset Register (DC_SYS_TIME_OFFSET)

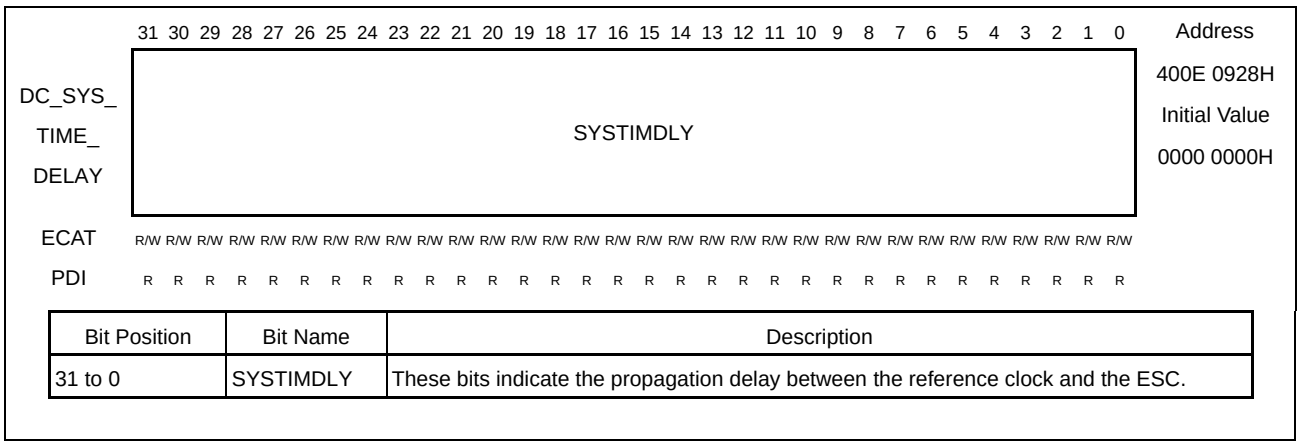
DC_SYS_TIME_OFFSET is used to indicate difference (offset) between the local time and the system time.



Bit Position	Bit Name	Description
63 to 0	SYSTIMOFST	These bits indicate difference (offset) between the local time and the system time. The offset is added to the local time and used locally as the system clock.

6.20.2.4 System Time Delay Register (DC_SYS_TIME_DELAY)

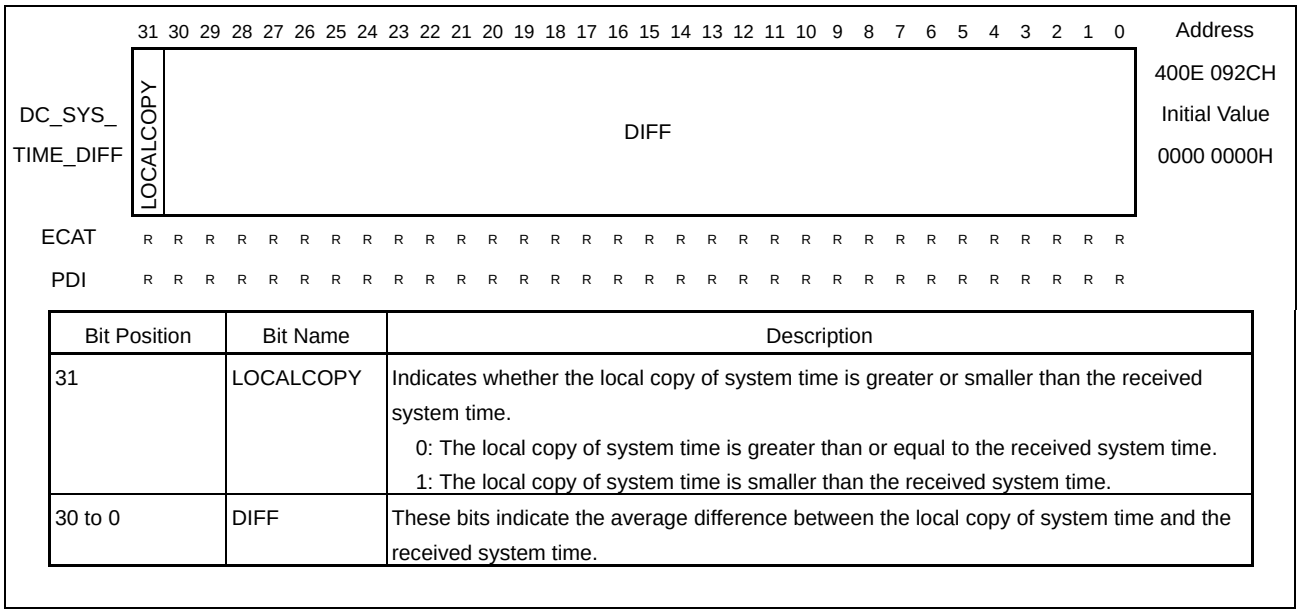
DC_SYS_TIME_DELAY indicates the propagation delay between the reference clock and the slave (ESC).



Bit Position	Bit Name	Description
31 to 0	SYSTIMDLY	These bits indicate the propagation delay between the reference clock and the ESC.

6.20.2.5 System Time Difference Register (DC_SYS_TIME_DIFF)

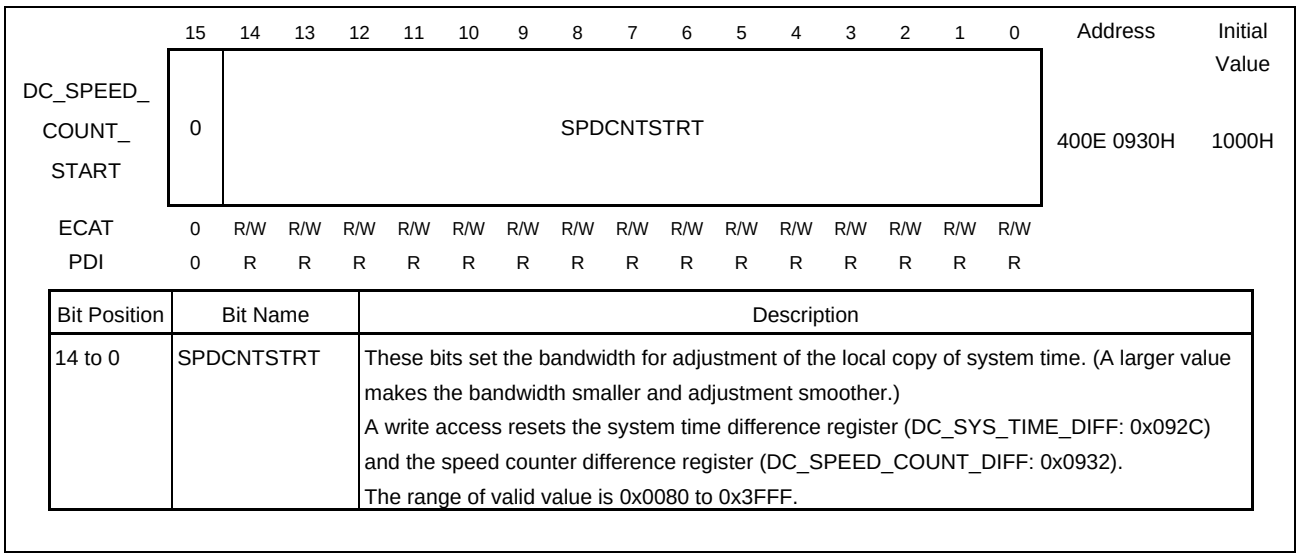
DC_SYS_TIME_DIFF indicates the average difference between the local copy of system time and the received system time.



Bit Position	Bit Name	Description
31	LOCALCOPY	Indicates whether the local copy of system time is greater or smaller than the received system time. 0: The local copy of system time is greater than or equal to the received system time. 1: The local copy of system time is smaller than the received system time.
30 to 0	DIFF	These bits indicate the average difference between the local copy of system time and the received system time.

6.20.2.6 Speed Counter Start Register (DC_SPEED_COUNT_START)

DC_SPEED_COUNT_START is used to set the bandwidth for adjustment of the local copy of system time.



Bit Position	Bit Name	Description
14 to 0	SPDCNTSTRT	These bits set the bandwidth for adjustment of the local copy of system time. (A larger value makes the bandwidth smaller and adjustment smoother.) A write access resets the system time difference register (DC_SYS_TIME_DIFF: 0x092C) and the speed counter difference register (DC_SPEED_COUNT_DIFF: 0x0932). The range of valid value is 0x0080 to 0x3FFF.

6.20.2.7 Speed Counter Difference Register (DC_SPEED_COUNT_DIFF)

DC_SPEED_COUNT_DIFF indicates the deviation between the local clock period and the clock period of reference clock.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	Initial Value
DC_SPEED_COUNT_DIFF	SPDCNTDIFF																400E 0932H	0000H
ECAT	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R		
PDI	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R		

Bit Position	Bit Name	Description
15 to 0	SPDCNTDIFF	These bits indicate the deviation between the local clock period and the clock period of reference clock. It is represented as two's complement. Range: ±(Value of the speed counter start – 0x7F)

6.20.2.8 System Time Difference Filter Depth Register (DC_SYS_TIME_DIFF_FIL_DEPTH)

DC_SYS_TIME_DIFF_FIL_DEPTH is used to set the filter depth for averaging the received system time deviation.

	7	6	5	4	3	2	1	0	Address	Initial Value
DC_SYS_TIME_DIFF_FIL_DEPTH	0	0	0	0	SYSTIMDEP				400E 0934H	04H
ECAT	0	0	0	0	R/W	R/W	R/W	R/W		
PDI	0	0	0	0	R	R	R	R		

Bit Position	Bit Name	Description
3-0	SYSTIMDEP	These bits set the filter depth for averaging the received system time deviation. A write access resets the system time difference register (DC_SYS_TIME_DIFF: 0x092C).

6.20.2.9 Speed Counter Filter Depth register (DC_SPEED_COUNT_FIL_DEPTH)

DC_SPEED_COUNT_FIL_DEPTH is used to set the filter depth for averaging the clock period deviation.

	7	6	5	4	3	2	1	0	Address	Initial Value
DC_SPEED_COUNT_FIL_DEPTH	0	0	0	0	CLKPERDEP				400E 0935H	0CH
ECAT	0	0	0	0	R/W	R/W	R/W	R/W		
PDI	0	0	0	0	R	R	R	R		

Bit Position	Bit Name	Description
3 to 0	CLKPERDEP	These bits set the filter depth for averaging the clock period deviation. A write access resets the internal speed counter filter.

6.20.3 Cyclic Unit Control Registers

6.20.3.1 Cyclic Unit Control Register (DC_CYC_CONT)

DC_CYC_CONT is used to specify whether the SYNC or latch unit is controlled by the ECAT/PDI.

	7	6	5	4	3	2	1	0	Address	Initial Value
DC_CYC_CONT	0	0	LATCH1	LATCH0	0	0	0	SYNCOUT	400E 0980H	00H
ECAT	0	0	R/W	R/W	0	0	0	R/W		
PDI	0	0	R	R	0	0	0	R		

Bit Position	Bit Name	Description
5	LATCH1	Specifies the control of latch input unit 1. 0: ECAT control 1: PDI control Note: Latch interrupt is routed to the ECAT/PDI depending on this setting.
4	LATCH0	Specifies the control of latch input unit 0. 0: ECAT control 1: PDI control Note: Latch interrupt is routed to the ECAT/PDI depending on this setting.
0	SYNCOUT	Specifies the control of SYNC output unit. 0: ECAT control 1: PDI control

6.20.4 SYNC Output Unit Registers

6.20.4.1 Activation Register (DC_ACT)

DC_ACT is used to activate the SYNC output unit.

	7	6	5	4	3	2	1	0	Address	Initial Value
DC_ACT	DBGPULSE	NEARFUTURE	STARTTIME	EXTSTARTTIME	AUTOACT	SYNC1	SYNC0	SYNCACT	400E 0981H	00H
ECAT	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)		
PDI	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)		

Bit Position	Bit Name	Description
7	DBGPULSE	Generates the SYNC signal debug pulse. 0: Invalid 1: A single debug ping is immediately generated on SYNC0 and SYNC1 pins according to the setting of bits 2 and 1 in this register. This bit is self-clearing, and always read as 0.
6	NEARFUTURE	Specifies the range of near future. 0: 2^{63} ns range (1/2 of DC bit width) 1: 2^{31} ns range (about 2.1 sec.)
5	STARTTIME	Checks the verification of start time. 0: Invalid. Sync signals are generated if the start time is reached. 1: Sync signals are immediately generated if the start time is out of the near future.
4	EXTSTARTTIME	Extends the start time cyclic operation. 0: No extension 1: The start time written in 32 bits is extended to 64 bits.
3	AUTOACT	Enables the SYNC output unit automatically by writing the start time cyclic operation register (DC_CYC_START_TIME: 0x0990). 0: Disabled 1: Enabled. After the start time was written, 1 is set automatically to bit 0 in this register.
2	SYNC1	Specifies the use of SYNC1 output. 0: Not used 1: SYNC1 pulse output is generated
1	SYNC0	Specifies the use of SYNC0 output. 0: Not used 1: SYNC0 pulse output is generated
0	SYNCACT	Specifies the activation of Sync output unit. 0: Deactivated 1: Activated Note: Write 1 after the start time was written.

Remark: Writing to this register depends on the setting of bit 0 in the cyclic unit control register (DC_CYC_CONT: 0x0980).

6.20.4.2 Pulse Length of Sync Signals Register (DC_PULSE_LEN)

DC_PULSE_LEN indicates the pulse length of Sync signals.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	Initial Value
DC_PULSE_LEN	PULSELEN																400E 0982H	0000H Note
ECAT	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R		
PDI	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R		

Bit Position	Bit Name	Description
15 to 0	PULSELEN	These bits indicate the pulse length of Sync signals (in 10-ns units). 0: Acknowledge mode. Sync signals will be cleared by reading the SYNC0/SYNC1 status register (DC_SYNC0/1_STAT: 0x098E:0x098F) in acknowledge mode.

Note: This is the initial value until the EEPROM was loaded. After that, the value is changed to the one stored at address 0x0002 in the EEPROM. The value is captured only when the EEPROM is loaded for the first time after the power on or reset.

6.20.4.3 Activation Status Register (DC_ACT_STAT)

DC_ACT_STAT indicates the activation status of Sync output signals.

	7	6	5	4	3	2	1	0	Address	Initial Value
DC_ACT_STAT	0	0	0	0	0	STARTTIME	SYNC1ACT	SYNC0ACT	400E 0984H	00H
ECAT	0	0	0	0	0	R	R	R		
PDI	0	0	0	0	0	R	R	R		

Bit Position	Bit Name	Description
2	STARTTIME	Checks the verification of the start time cyclic operation register (DC_CYC_START_TIME: 0x0990) when the Sync output unit was activated. 0: The start time is within the near future. 1: The start time is out of the near future.
1	SYNC1ACT	Indicates the SYNC1 activation state. 0: First SYNC1 pulse is not pending 1: First SYNC1 pulse is pending
0	SYNC0ACT	Indicates the SYNC0 activation state. 0: First SYNC0 pulse is not pending 1: First SYNC0 pulse is pending

6.20.4.4 SYNC0 Status Register (DC_SYNC0_STAT)

DC_SYNC0_STAT indicates the status of SYNC0 output. This register is only used in acknowledge mode.

	7	6	5	4	3	2	1	0	Address	Initial Value
DC_SYNC0_STAT	0	0	0	0	0	0	0	SYNC0STA	400E 098EH	00H
ECAT	0	0	0	0	0	0	0	R		
PDI	0	0	0	0	0	0	0	R(ack)		

Bit Position	Bit Name	Description
0	SYNC0STA	Indicates the SYNC0 state for acknowledge mode. SYNC0 in acknowledge mode is cleared by reading this register from the PDI. This bit is used only in acknowledge mode.

6.20.4.5 SYNC1 Status Register (DC_SYNC1_STAT)

DC_SYNC1_STAT indicates the status of SYNC1 output. This register is only used in acknowledge mode.

	7	6	5	4	3	2	1	0	Address	Initial Value
DC_SYNC1_STAT	0	0	0	0	0	0	0	SYNC1STA	400E 098FH	00H
ECAT	0	0	0	0	0	0	0	R		
PDI	0	0	0	0	0	0	0	R(ack)		

Bit Position	Bit Name	Description
0	SYNC1STA	Indicates the SYNC1 state for acknowledge mode. SYNC1 in acknowledge mode is cleared by reading this register from the PDI. This bit is used only in acknowledge mode.

6.20.4.6 Start Time Cyclic Operation/Next SYNC0 Pulse Register (DC_CYC_START_TIME)

DC_CYC_START_TIME sets the start time of cyclic operation when written, and indicates the system time of next SYNC0 pulse when read.

DC_CYC_START_TIME

Address: 400E 0990H

Initial Value: 0000 0000 0000 0000H

	63–32
DC_CYC_START_TIME	STATIM
ECAT	R/(W) (each bit 63 to 32)
PDI	R/(W) (each bit 63 to 32)

	31–0
	STATIM
ECAT	R/(W) (each bit 31 to 0)
PDI	R/(W) (each bit 31 to 0)

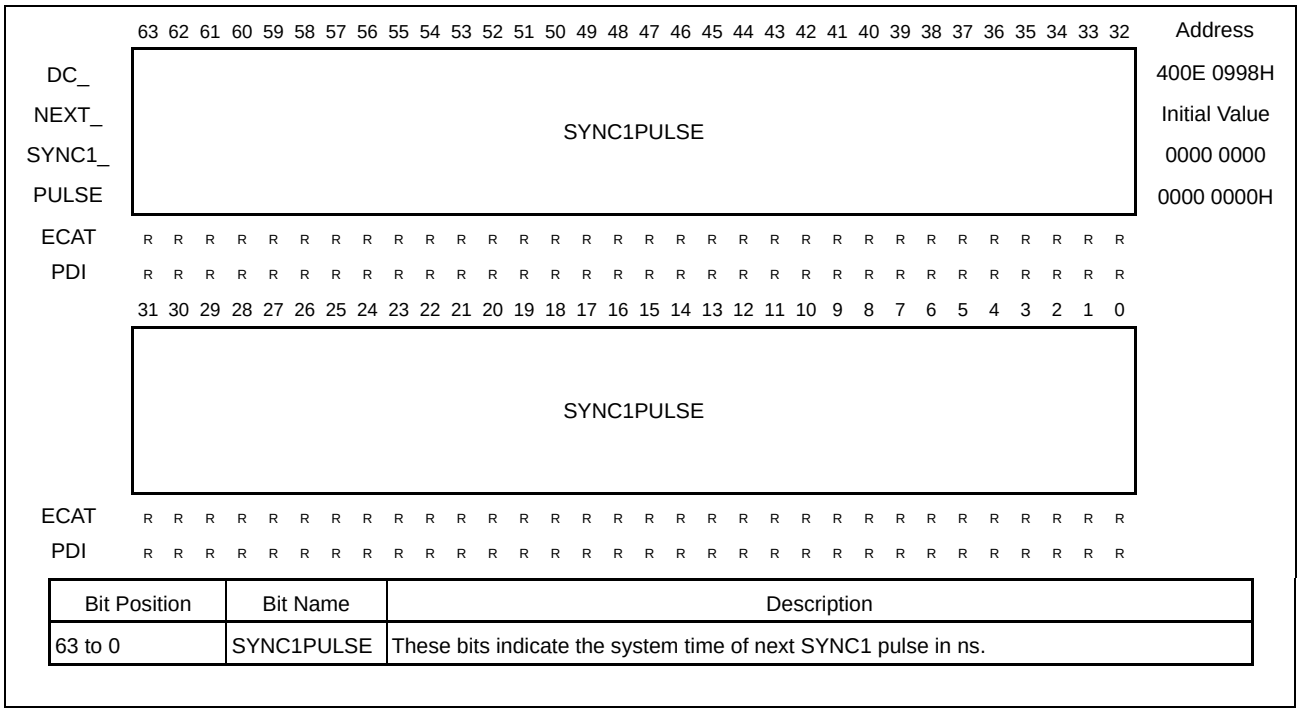
Bit Position	Bit Name	Description
63 to 0	STATIM	Write: The start time (system time) of cyclic operation is set in ns. Read: The system time of next SYNC0 pulse is indicated in ns.

Remarks 1. Writing to this register depends on the setting of bit 0 in the cyclic unit control register (DC_CYC_CONT: 0x0980). Writing is enabled only when bit 0 in the SYNC activation register (DC_ACT: 0x0981) is 0.

2. While the auto-activation is enabled, if only lower 32 bits are written within one frame, upper 32 bits are automatically extended.

6.20.4.7 Next SYNC1 Pulse Register (DC_NEXT_SYNC1_PULSE)

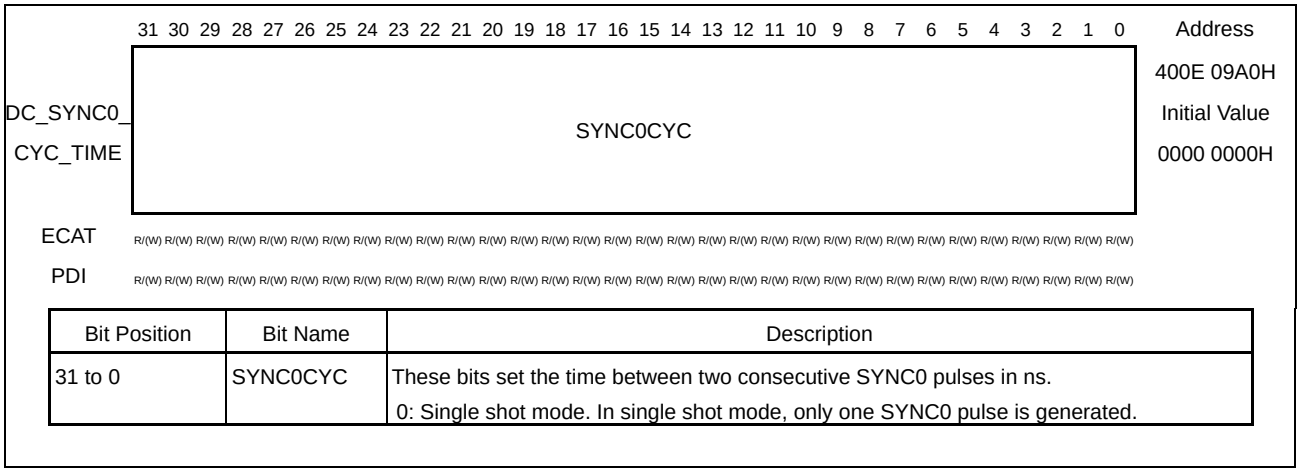
DC_NEXT_SYNC1_PULSE indicates the system time of next SYNC1 pulse.



Bit Position	Bit Name	Description
63 to 0	SYNC1PULSE	These bits indicate the system time of next SYNC1 pulse in ns.

6.20.4.8 SYNC0 Cycle Time Register (DC_SYNC0_CYC_TIME)

DC_SYNC0_CYC_TIME is used to set the time between two consecutive SYNC0 pulses.



Bit Position	Bit Name	Description
31 to 0	SYNC0CYC	These bits set the time between two consecutive SYNC0 pulses in ns. 0: Single shot mode. In single shot mode, only one SYNC0 pulse is generated.

Remark: Writing to this register depends on the setting of bit 0 in the cyclic unit control register (DC_CYC_CONT: 0x0980).

6.20.4.9 SYNC1 Cycle Time Register (DC_SYNC1_CYC_TIME)

DC_SYNC1_CYC_TIME is used to set the time between SYNC1 pulse and SYNC0 pulse.

	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	Address
DC_SYNC1_CYC_TIME	SYNC1CYC	400E 09A4H
		Initial Value
		0000 0000H
ECAT	R/(W) R/(W)	
PDI	R/(W) R/(W)	

Bit Position	Bit Name	Description
31 to 0	SYNC1CYC	These bits set the time between SYNC1 pulse and SYNC0 pulse in ns.

Remark: Writing to this register depends on the setting of bit 0 in the cyclic unit control register (DC_CYC_CONT: 0x0980).

6.20.5 Latch Input Unit Registers

6.20.5.1 Latch0 Control register (DC_LATCH0_CONT)

DC_LATCH0_CONT is used to control the edge function of Latch0 input signal.

	7	6	5	4	3	2	1	0	Address	Initial Value
DC_LATCH0_CONT	0	0	0	0	0	0	NEGEDGE	POSEDGE	400E 09A8H	00H
ECAT	0	0	0	0	0	0	R/(W)	R/(W)		
PDI	0	0	0	0	0	0	R/(W)	R/(W)		

Bit Position	Bit Name	Description
1	NEGEDGE	Indicates the function of Latch0 negative edge. 0: Continuous latch active 1: Single event (only first event is active)
0	POSEDGE	Indicates the function of Latch0 positive edge. 0: Continuous latch active 1: Single event (only first event is active)

Remark: Writing to this register depends on the setting of bit 4 in the cyclic unit control register (DC_CYC_CONT: 0x0980).

6.20.5.2 Latch1 Control Register (DC_LATCH1_CONT)

DC_LATCH1_CONT is used to control the edge function of Latch1 input signal.

	7	6	5	4	3	2	1	0	Address	Initial Value
DC_LATCH1_CONT	0	0	0	0	0	0	NEGEDGE	POSEDGE	400E 09A9H	00H
ECAT	0	0	0	0	0	0	R/(W)	R/(W)		
PDI	0	0	0	0	0	0	R/(W)	R/(W)		

Bit Position	Bit Name	Description
1	NEGEDGE	Indicates the function of Latch1 negative edge. 0: Continuous latch active 1: Single event (only first event is active)
0	POSEDGE	Indicates the function of Latch1 positive edge. 0: Continuous latch active 1: Single event (only first event is active)

Remark: Writing to this register depends on the setting of bit 5 in the cyclic unit control register (DC_CYC_CONT: 0x0980).

6.20.5.3 Latch0 Status Register (DC_LATCH0_STAT)

DC_LATCH0_STAT indicates the status of Latch0 input signal.

	7	6	5	4	3	2	1	0	Address	Initial Value
DC_LATCH0_STAT	0	0	0	0	0	PINSTATE	EVENTNEG	EVENTPOS	400E 09AEH	00H
ECAT	0	0	0	0	0	R	R	R		
PDI	0	0	0	0	0	R	R	R		

Bit Position	Bit Name	Description
2	PINSTATE	Indicates the status of Latch0 input pin.
1	EVENTNEG	Indicates the event of Latch0 input negative edge. 0: Negative edge is not detected or in continuous mode 1: Negative edge is detected in single event mode only. The flag is cleared by reading the Latch0 time negative edge register (DC_LATCH0_TIME_NEG: 0x09B8).
0	EVENTPOS	Indicates the event of Latch0 input positive edge. 0: Positive edge is not detected or in continuous mode 1: Positive edge is detected in single event mode only. The flag is cleared by reading the Latch0 time positive edge register (DC_LATCH0_TIME_POS: 0x09B0).

6.20.5.4 Latch1 Status Register (DC_LATCH1_STAT)

DC_LATCH1_STAT indicates the status of Latch1 input signal.

	7	6	5	4	3	2	1	0	Address	Initial Value
DC_LATCH1_STAT	0	0	0	0	0	PINSTATE	EVENTNEG	EVENTPOS	400E 09AFH	00H
ECAT	0	0	0	0	0	R	R	R		
PDI	0	0	0	0	0	R	R	R		

Bit Position	Bit Name	Description
2	PINSTATE	Indicates the status of Latch1 input pin.
1	EVENTNEG	Indicates the event of Latch1 input negative edge. 0: Negative edge is not detected or in continuous mode 1: Negative edge is detected in single event mode only. The flag is cleared by reading the Latch1 time negative edge register (DC_LATCH1_TIME_NEG: 0x09C8).
0	EVENTPOS	Indicates the event of Latch1 input positive edge. 0: Positive edge is not detected or in continuous mode 1: Positive edge is detected in single event mode only. The flag is cleared by reading the Latch1 time positive edge register (DC_LATCH1_TIME_POS: 0x09C0).

6.20.5.5 Latch0 Time Positive Edge Register (DC_LATCH0_TIME_POS)

DC_LATCH0_TIME_POS indicates the system time at the positive edge of Latch0 input signal.

	63 62 61 60 59 58 57 56 55 54 53 52 51 50 49 48 47 46 45 44 43 42 41 40 39 38 37 36 35 34 33 32	Address
DC_ LATCH0_ TIME_POS	SYSTIME	400E 09B0H Initial Value 0000 0000 0000 0000H
ECAT PDI	R(ack) R(ack)	
	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
	SYSTIME	
ECAT PDI	R(ack) R(ack)	

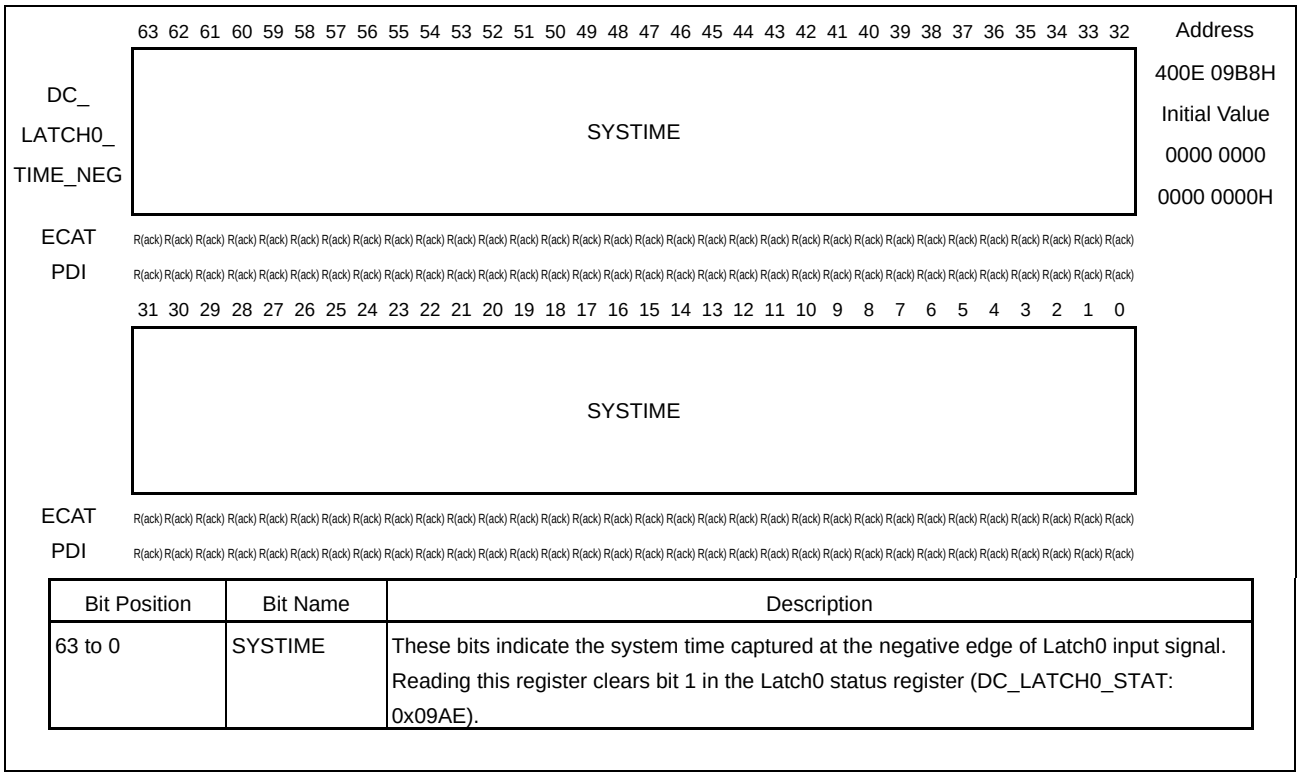
Bit Position	Bit Name	Description
63 to 0	SYSTIME	These bits indicate the system time captured at the positive edge of Latch0 input signal. Reading this register clears bit 0 in the Latch0 status register (DC_LATCH0_STAT: 0x09AE).

Remarks 1. Bits 63to 8 are internally latched (ECAT/PDI independently) when bits 7 to 0 are read, which guarantees reading a consistent value.

2. Clearing the Latch0 status flag function depends on the setting of bit 4 in the cyclic unit control register (DC_CYC_CONT: 0x0980).

6.20.5.6 Latch0 Time Negative Edge Register (DC_LATCH0_TIME_NEG)

DC_LATCH0_TIME_NEG indicates the system time at the negative edge of Latch0 input signal.



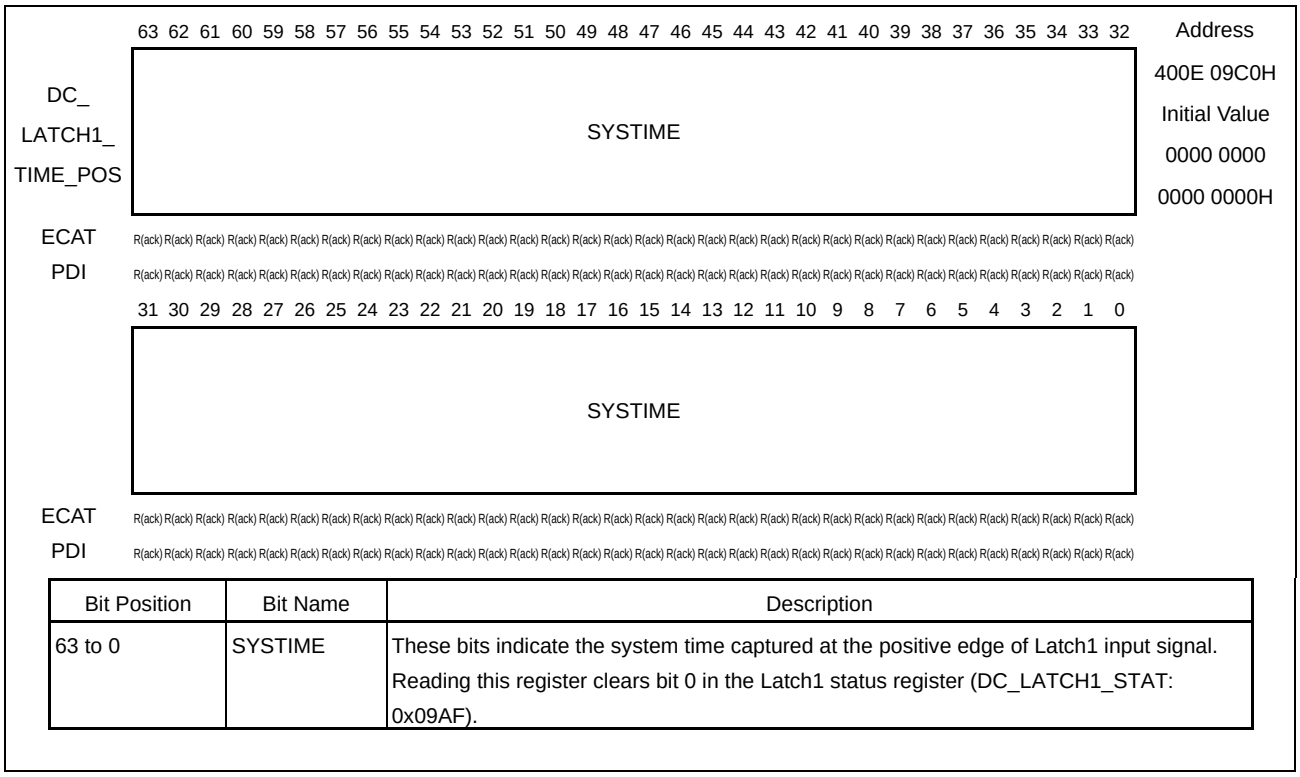
Bit Position	Bit Name	Description
63 to 0	SYSTIME	These bits indicate the system time captured at the negative edge of Latch0 input signal. Reading this register clears bit 1 in the Latch0 status register (DC_LATCH0_STAT: 0x09AE).

Remarks 1. Bits 63to 8 are internally latched (ECAT/PDI independently) when bits 7 to 0 are read, which guarantees reading a consistent value.

2. Clearing the Latch0 status flag function depends on the setting of bit 4 in the cyclic unit control register (DC_CYC_CONT: 0x0980).

6.20.5.7 Latch1 Time Positive Edge Register (DC_LATCH1_TIME_POS)

DC_LATCH1_TIME_POS indicates the system time at the positive edge of Latch1 input signal.



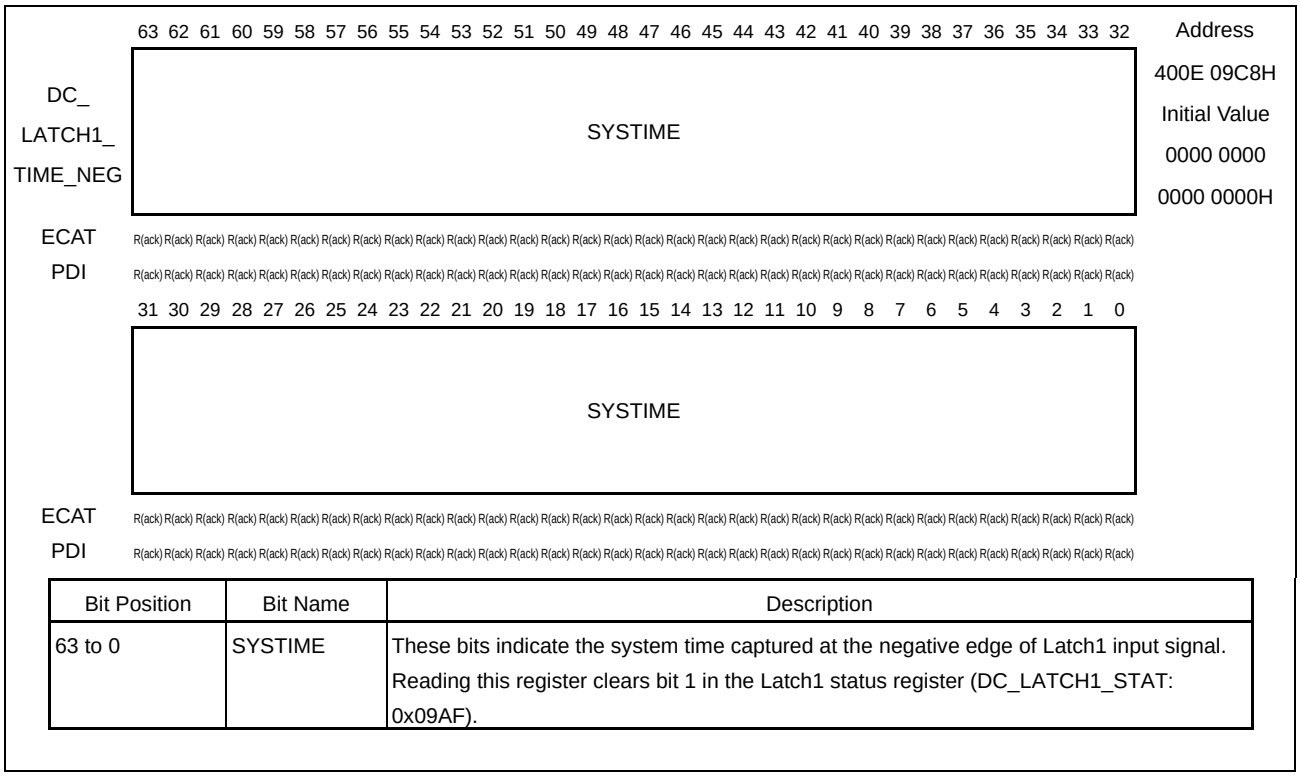
Bit Position	Bit Name	Description
63 to 0	SYSTIME	These bits indicate the system time captured at the positive edge of Latch1 input signal. Reading this register clears bit 0 in the Latch1 status register (DC_LATCH1_STAT: 0x09AF).

Remarks 1. Bits 63to 8 are internally latched (ECAT/PDI independently) when bits 7 to 0 are read, which guarantees reading a consistent value.

2. Clearing the Latch1 status flag function depends on the setting of bit 5 in the cyclic unit control register (DC_CYC_CONT: 0x0980).

6.20.5.8 Latch1 Time Negative Edge Register (DC_LATCH1_TIME_NEG)

DC_LATCH1_TIME_NEG indicates the system time at the negative edge of Latch1 input signal.



Bit Position	Bit Name	Description
63 to 0	SYSTIME	These bits indicate the system time captured at the negative edge of Latch1 input signal. Reading this register clears bit 1 in the Latch1 status register (DC_LATCH1_STAT: 0x09AF).

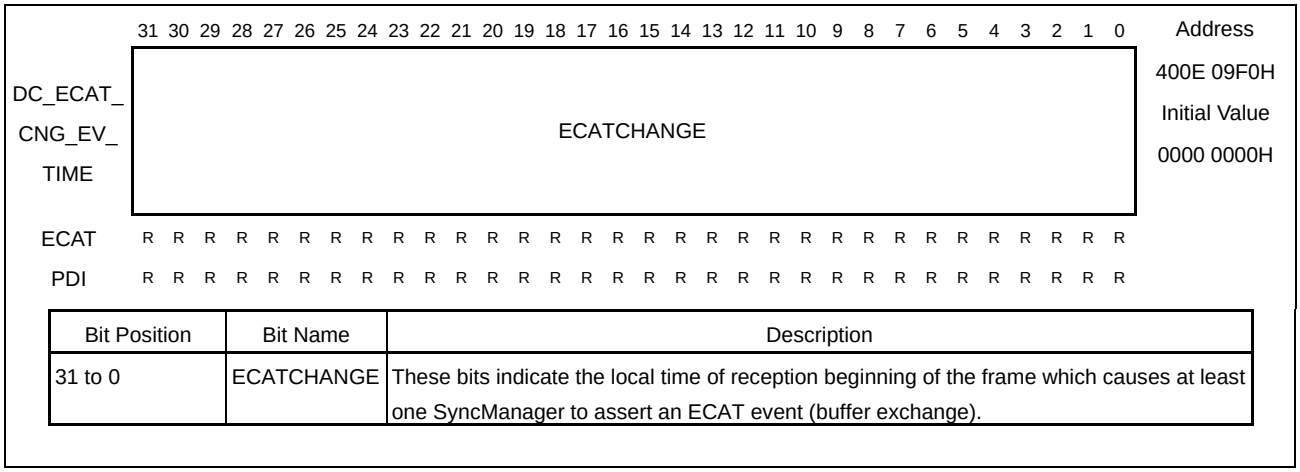
Remarks 1. Bits 63to 8 are internally latched (ECAT/PDI independently) when bits 7 to 0 are read, which guarantees reading a consistent value.

2. Clearing the Latch1 status flag function depends on the setting of bit 5 in the cyclic unit control register (DC_CYC_CONT: 0x0980).

6.20.6 SyncManager Event Times Registers

6.20.6.1 EtherCAT Buffer Change Event Time Register (DC_ECAT_CNG_EV_TIME)

DC_ECAT_CNG_EV_TIME indicates the local time of reception beginning of the frame which causes at least one SyncManager to assert an ECAT event (buffer exchange).

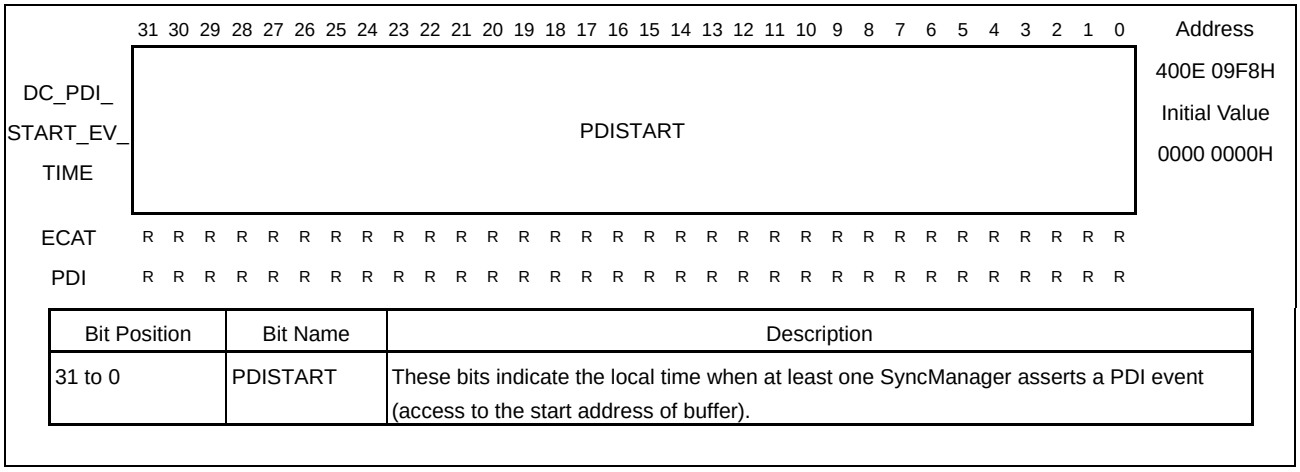


Bit Position	Bit Name	Description
31 to 0	ECATCHANGE	These bits indicate the local time of reception beginning of the frame which causes at least one SyncManager to assert an ECAT event (buffer exchange).

Remark: Bits 31 to 8 are internally latched (ECAT/PDI independently) when bits 7 to 0 are read, which guarantees reading a consistent value.

6.20.6.2 PDI Buffer Start Event Time Register (DC_PDI_START_EV_TIME)

DC_PDI_START_EV_TIME indicates the local time when at least one SyncManager asserts a PDI event (access to the start address of buffer).



Bit Position	Bit Name	Description
31 to 0	PDISTART	These bits indicate the local time when at least one SyncManager asserts a PDI event (access to the start address of buffer).

Remark: Bits 31 to 8 are internally latched (ECAT/PDI independently) when bits 7 to 0 are read, which guarantees reading a consistent value.

6.20.6.3 PDI Buffer Change Event Time Register (DC_PDI_CNG_EV_TIME)

DC_PDI_CNG_EV_TIME indicates the local time when at least one SyncManager asserts a PDI event (buffer exchange).

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
DC_PDI_CNG_EV_TIME	PDICHANGE																																400E 09FCH Initial Value 0000 0000H
ECAT	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	
PDI	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	

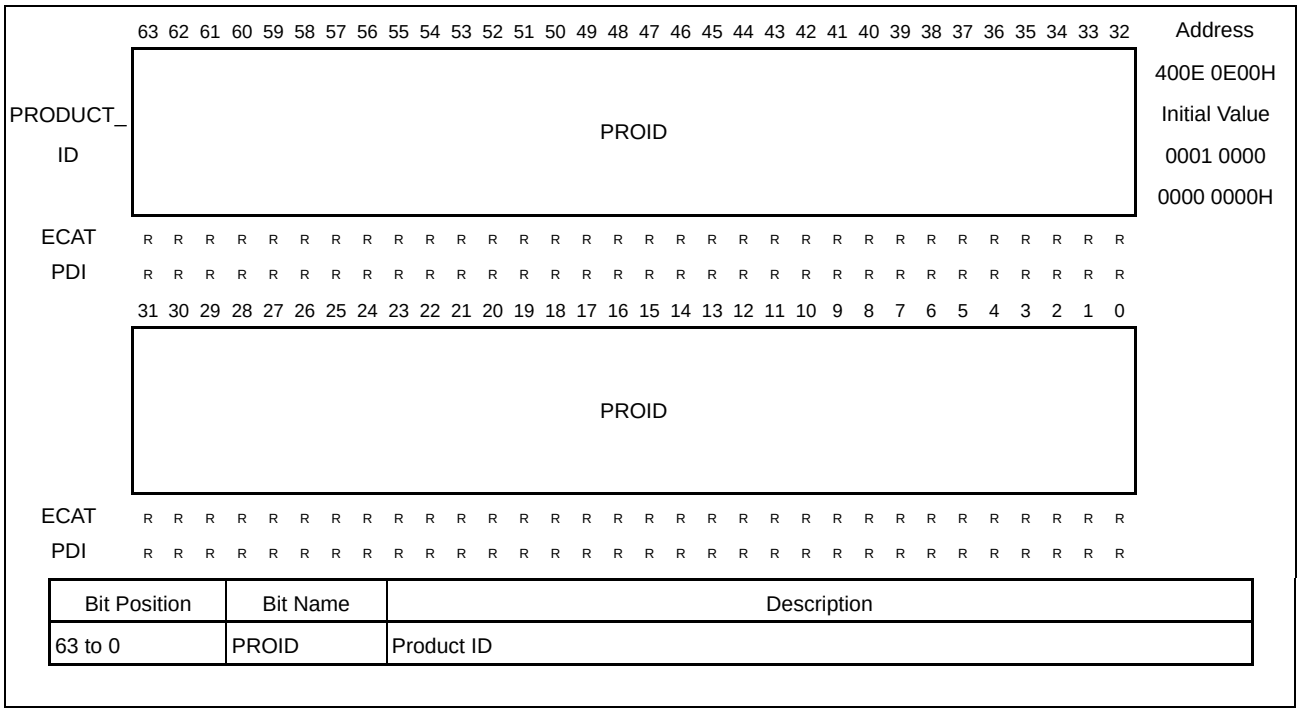
Bit Position	Bit Name	Description
31 to 0	PDICHANGE	These bits indicate the local time when at least one SyncManager asserts a PDI event (buffer exchange).

Remark: Bits 31 to 8 are internally latched (ECAT/PDI independently) when bits 7 to 0 are read, which guarantees reading a consistent value.

6.21 ETC Registers

6.21.1 Product ID Register (PRODUCT_ID)

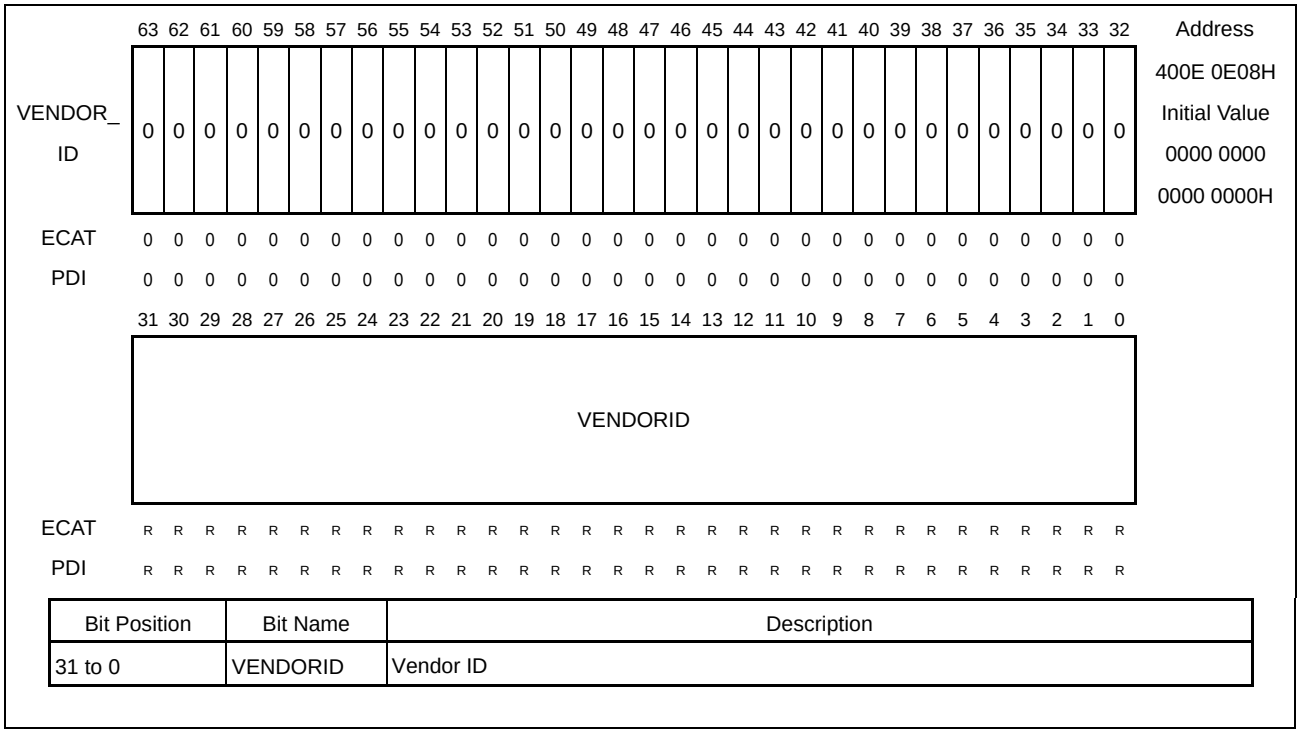
PRODUCT_ID indicates the product ID.



Bit Position	Bit Name	Description
63 to 0	PROID	Product ID

6.21.2 Vender ID Register (VENDOR_ID)

VENDOR_ID indicates the vendor ID.



Bit Position	Bit Name	Description
31 to 0	VENDORID	Vendor ID

6.21.3 User RAM (USER_RAM)

USER_RAM indicates the supported features dependent on the IP core configuration. The area is 128 bytes from 400E 0F80H to 400E 0FFFH. The value "1" of initial value means supported features. However, bits 7 to 0 indicate the number of bits defined in the user RAM, and the value in the R-IN32M3-EC is 33H.

Bit Position	Description	Initial Value
7 to 0	Number of extended feature bits. This LSI indicates 51 bits (33H).	33H
8	Extended DL control register (0x0102:0x0103)	1
9	AL status code register (0x0134:0x0135)	1
10	ECAT event mask (0x0200:0x0201)	1
11	Configured station alias (0x0012:0x0013)	1
12	General purpose input (0x0F18:0x0F1F)	0
13	General purpose output (0x0F10:0x0F17)	0
14	AL event mask (0x0204:0x0207)	1
15	Physical read/write offset (0x0108:0x0109)	1
16	Watchdog divider writeable (0x0400:0x04001) and Watchdog PDI (0x0410:0x0f11)	1
17	Watchdog counter (0x0442:0x0443)	1
18	Write protection (0x0020:0x0031)	1
19	Reset (0x0040:0x0041)	1
20	Reserved	0
21	DC SyncManager event time (0x09F0:0x09FF)	1
22	ECAT processing unit/PDI error counter (0x030C:0x030D)	1
23	EEPROM size configurable (0x0502.7) 0: EEPROM size fixed to up to 16 Kbits 1: EEPROM size configurable	1
26 to 24	Reserved	0
27	Lost link counter (0x0310:0x0313)	1
28	MII management interface (0x0510:0x0515)	1
29	Enhanced link detection MII	1
30	Enhanced link detection EBUS	0
31	Run LED	1
32	Link/Activity LED	1
33	Reserved	0
35, 34	Reserved	1
36	Reserved	0
37	Reserved	1
38	DC time loop control assigned to PDI	0
39	Link detection and configuration by MI (MI link detection and configuration)	1
40	MI control by PDI	1
41	Automatic TX shift	1
42	EEPROM emulation	0
49 to 43	Reserved	0
50	ERR LED, RUN/ERR LED override	1
Others	Reserved	Reserved

6.21.4 Process Data RAM (DATA_RAM)

DATA_RAM is used for process data and mailbox. The area is 8 Kbytes from 400E 1000H to 400E 2FFFH.

The process data RAM is only accessible when the EEPROM was correctly loaded (when bit 0 in the ESC DL status register (ESC_DL_STATUS: 0x0110) is 1).

6.22 Reset Circuit

Figure 6.2 shows the reset circuit of EtherCAT Slave Controller. When reset request by ECAT (0x0040) or PDI (0x0041) is received, ESC stops and reset output from ESC becomes 1. Integrated Ethernet PHY is also reset by reset output from ESC automatically (Hardware Power-down mode). At the same time, INTECATRST interrupt is generated and CATRESETOUT pin outputs High.
To release reset state of ESC, CATRST bit of CATRESET register must be changed 1→0→1 after INTECATRST interrupt is detected. When reset input to ESC changes 1 to 0, reset output from ESC change 1 to 0 and reset input to Ethernet PHY is cleared. Adjust clear timing of CATRESET register so that reset input width to Ethernet PHY is more than 100us as shown in Figure 6.3.
It is possible to reset ESC by not reset request by ECAT/PDI (0x0040/0x0041) but CATRESET register only. In that case, Ethernet PHY is not reset automatically. Since Ethernet PHY is needed to be in reset state when ESC is in reset state, change Ethernet PHY to hardware power-down mode by PxPHYEN bit of PHYMD register before ESC is reset by CATRESET register as shown in Figure 6.4.

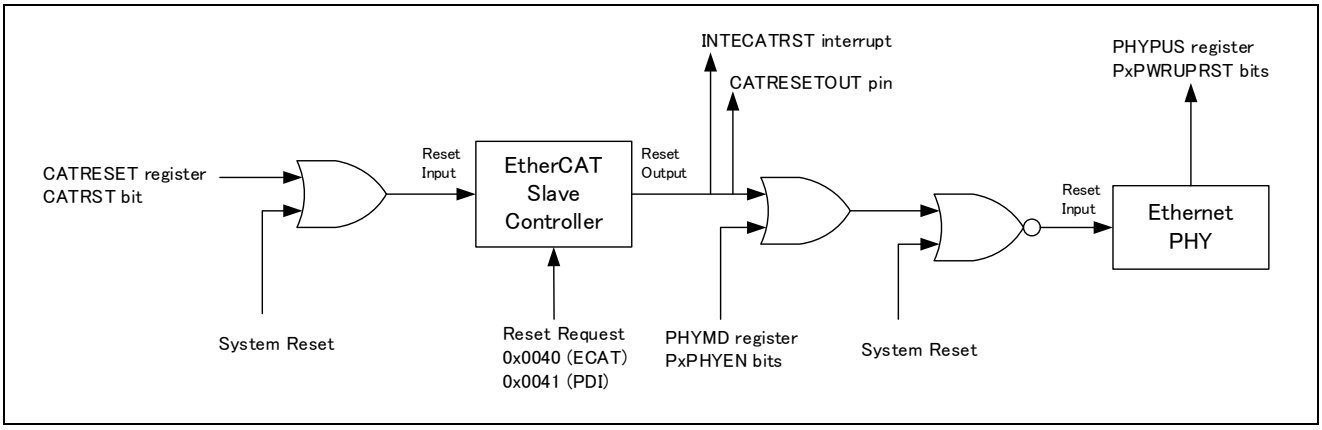


Figure 6.2 Reset Circuit of EtherCAT Slave Controller

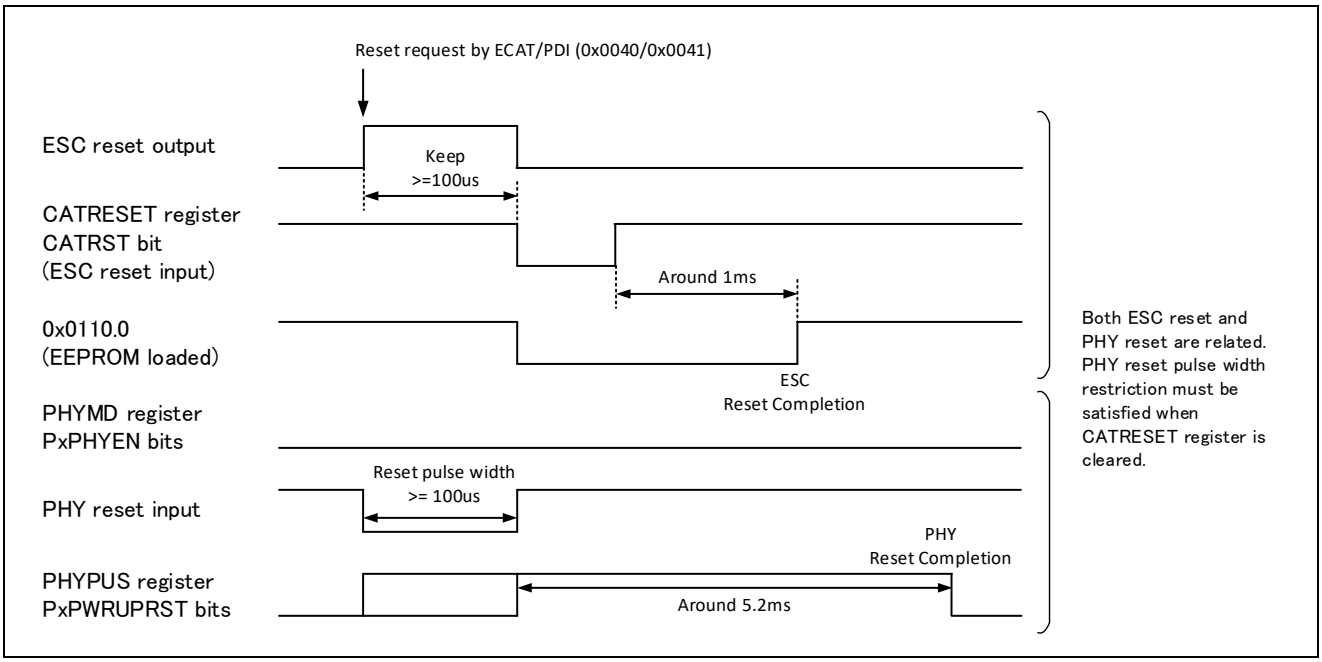


Figure 6.3 Reset Timing of EtherCAT Slave Controller (In case of reset request by ECAT/PDI)

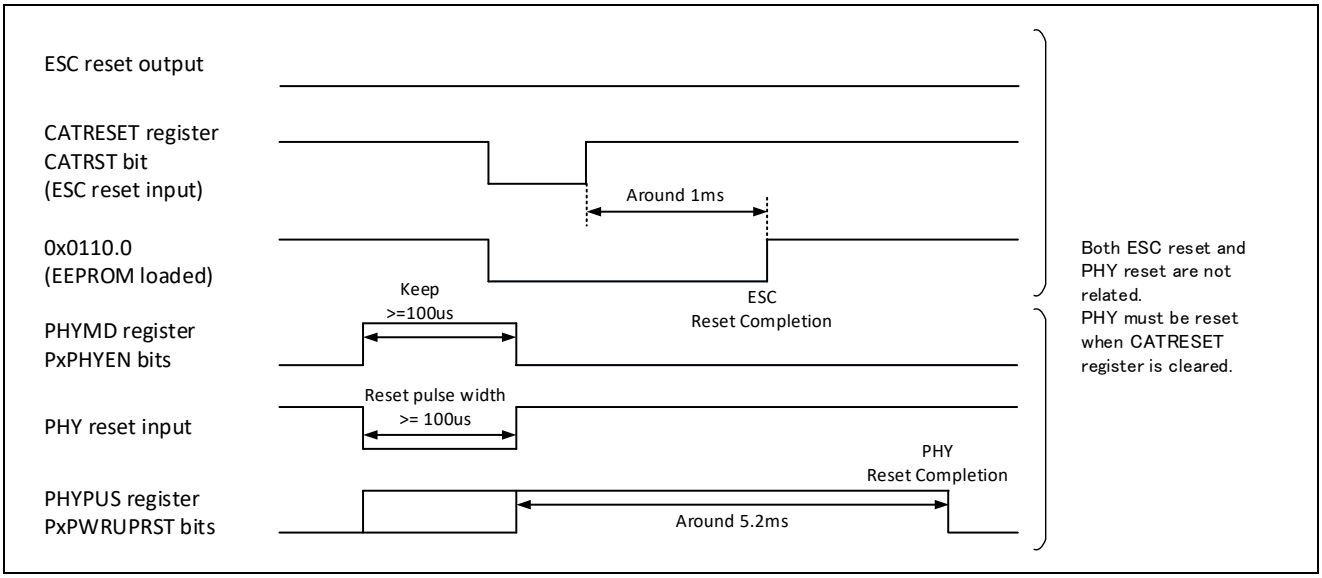


Figure 6.4 Reset Timing of EtherCAT Slave Controller (In case of reset by CATRESET register)

7. Ethernet PHY Function

7.1 Features

The R-IN32M3-EC supports 10BASE-T, 100BASE-TX/FX, and integrated IEEE802.3 dual-port Ethernet physical layer (PHY). It is possible to connect twisted-pair (UTP) cable by the external pulse transformer or connect optical fiber by the optical transceiver. It also supports Daisy chain structure and ring structure used by industry network.

- 10BASE-T, 100BASE-TX, and 100BASE-FX of based upon IEEE802.3
- 2 ports
- Auto-negotiation
- Full-duplex transmission and a half-duplex transmission
- Automatic MDI/MDI-X
- Serial management interface (MDC/MDIO)
- Low latency function
- Quick auto-negotiation
- Cable diagnosis function
- Fast link-loss detection function (BER monitor, FEQ monitor)

Caution 1: When using the EtherCAT slave controller, use 100BASE-TX because it doesn't support 100BASE-FX.
2: EtherCAT P is not supported.

7.2 Special Functions

7.2.1 Low Latency Function

It is possible to shorten the latency time for the Ethernet frame passing through PHY from the LINE interface to the MII interface (low latency mode). Ethernet frame starts from preamble while this preamble starts from symbol 11000 (J) and 10001 (K) of symbol (5B) of LINE. In the devices generally based on Ethernet, it is recognized as start preamble by detecting symbol J and K. In low latency mode, it is recognized as start preamble by detecting symbol J only. This means that the RX_DV signal is asserted at this moment and it becomes possible to shorten the latency 40 ns. If symbol J is incorrectly detected by a bit error, the RX_ER signal is asserted and the receiver will continue when symbol K in the following is not received.

The low latency mode becomes effective by setting bit 1 (RX_DV_J2T bit) in register 31 to 1.

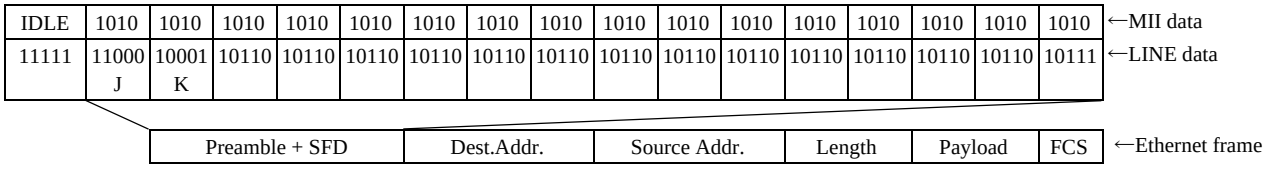


Figure 7.1 Preamble of Ethernet Frames

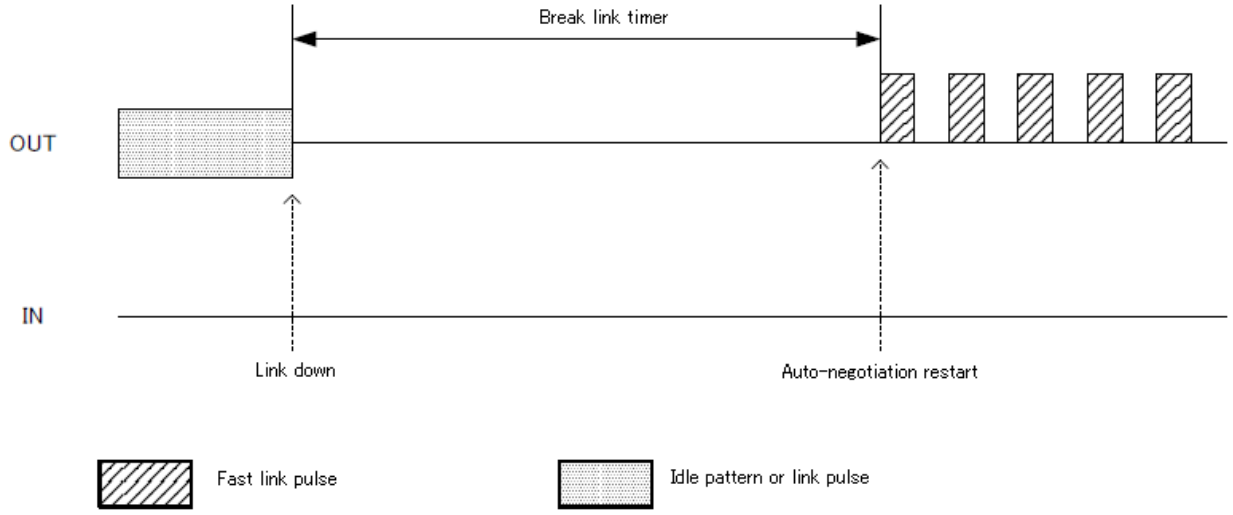
7.2.2 Quick Auto-Negotiation Function

R-IN32M3-EC supports the quick auto-negotiation function which means completing auto negotiation in less time than the specific time of IEEE802.3 and link up.

If the PHY is corresponding to the quick auto negotiation, auto negotiation can be complete in a shorter time than normal by reducing the timer time of the three elements described below among the auto negotiation state machine.

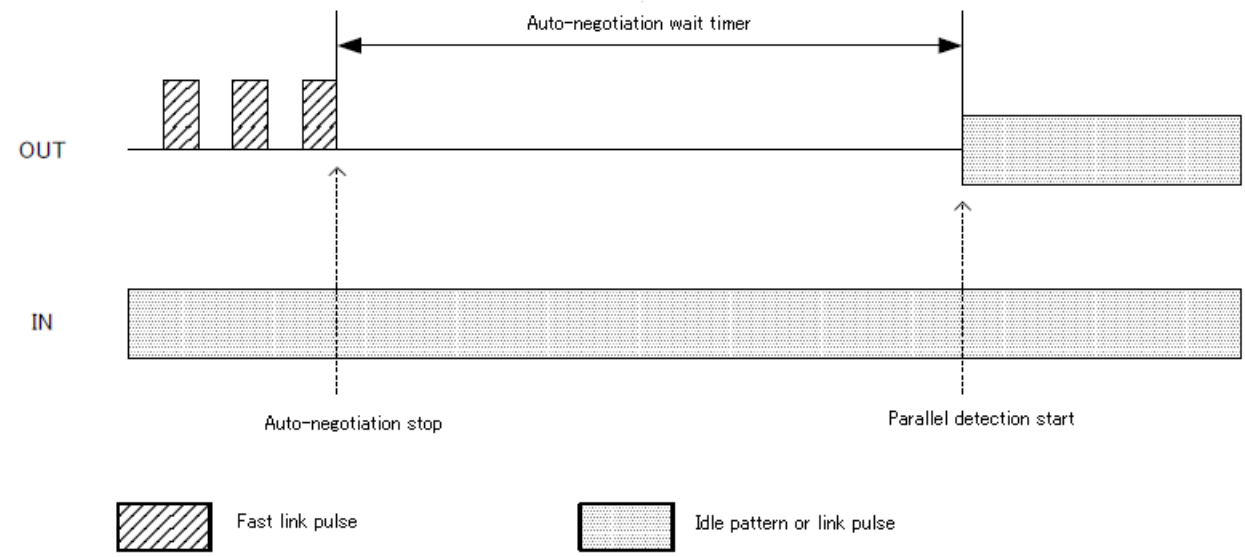
- Break Link Timer

The break link timer is defined as the time from PHY links down to auto-negotiation restarts and it is usually 1250 ms.



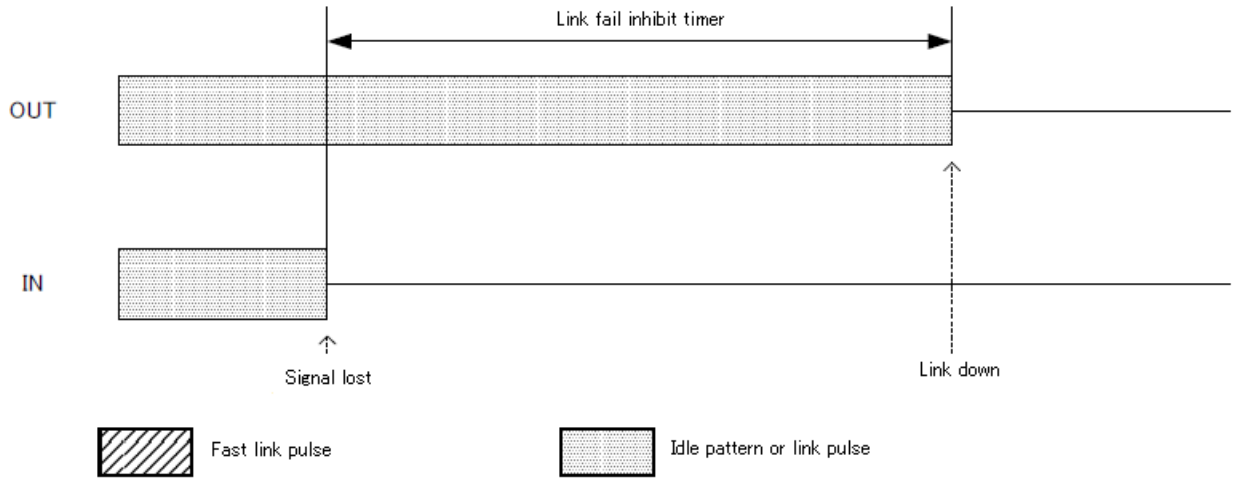
- Auto-Negotiation Wait Timer

The auto-negotiation wait timer is defined as the waiting time from auto-negotiation stops to parallel detection starts and it is usually 850 ms.



- Link Fail Inhibit Timer

The link fail inhibit timer is defined as the waiting time from signal loss or becomes abnormal to link down and it is usually 850 ms.



These three timers can be set by setting bits 8 to 5 in register 18 (PHY_MODE[3:0] bits). When PHY_MODE[3] is 0, the value of PHY_MODE[1:0] cannot be reflected. Set PHY_MODE[3] to 1 when using this function.

PHY_MODE[3]	PHY_MODE[1:0]	Break Link Timer	Auto-Negotiation Wait Timer	Link Fail Inhibit Timer
0	XX	1250 ms	850 ms	850 ms
1	00	80 ms	35 ms	50 ms
1	01	120 ms	50 ms	75 ms
1	10	240 ms	100 ms	150 ms
1	11	1250 ms	850 ms	850 ms

7.2.3 Cable Diagnostic Function (TDR Function)

The cable diagnostic function (TDR function) is a diagnostic function for detecting the type and location of abnormality when disconnection or short occurs in the Ethernet cable. This function outputs the pulse to the Ethernet cable and measures the time of pulse waveform reflected by the cable. This delay time is used to determine the distance of abnormal and the polarity is used to determine whether it is due to the short or open circuit.

The mechanism is as follows. In the following figures, (1) is the test pulse and (2) is the threshold for detecting the reflected pulse, and that can be set by the register. When the cable is disconnected (cable end open), the sent pulse will get back attenuated in the same polarity as shown in Figure 7.2. When the cable is short-circuited (cable end closed), the sent pulse will get back attenuated in opposite phase as shown in Figure 7.3.

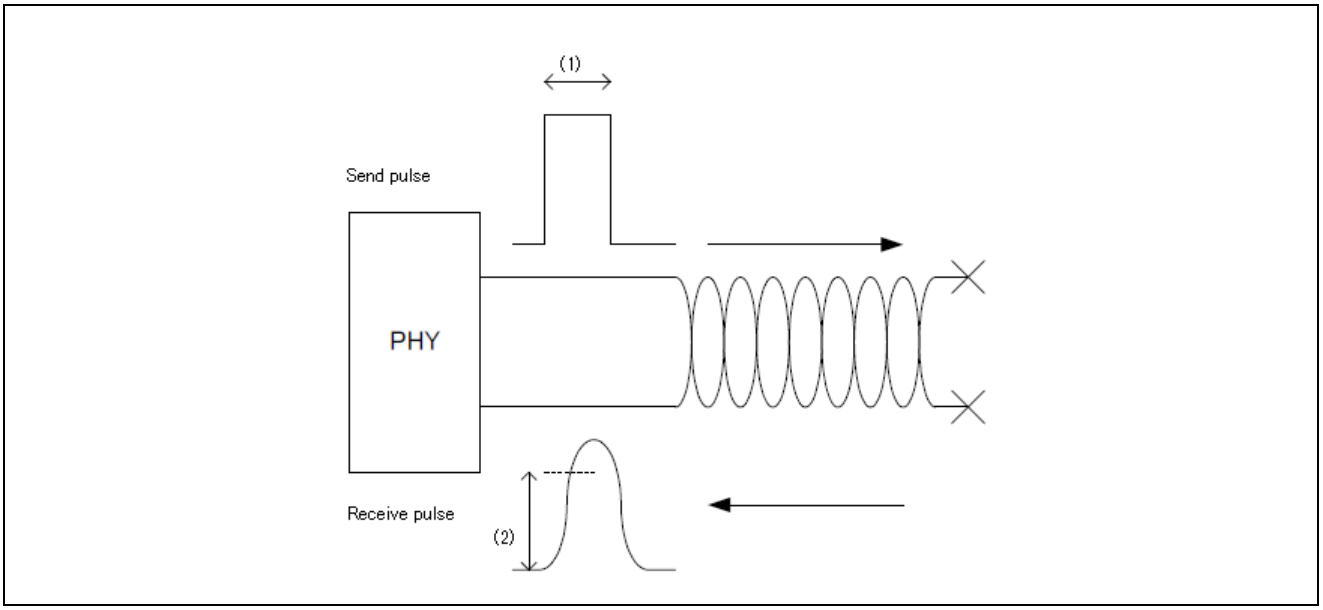


Figure 7.2 Operation when Cable is Disconnected

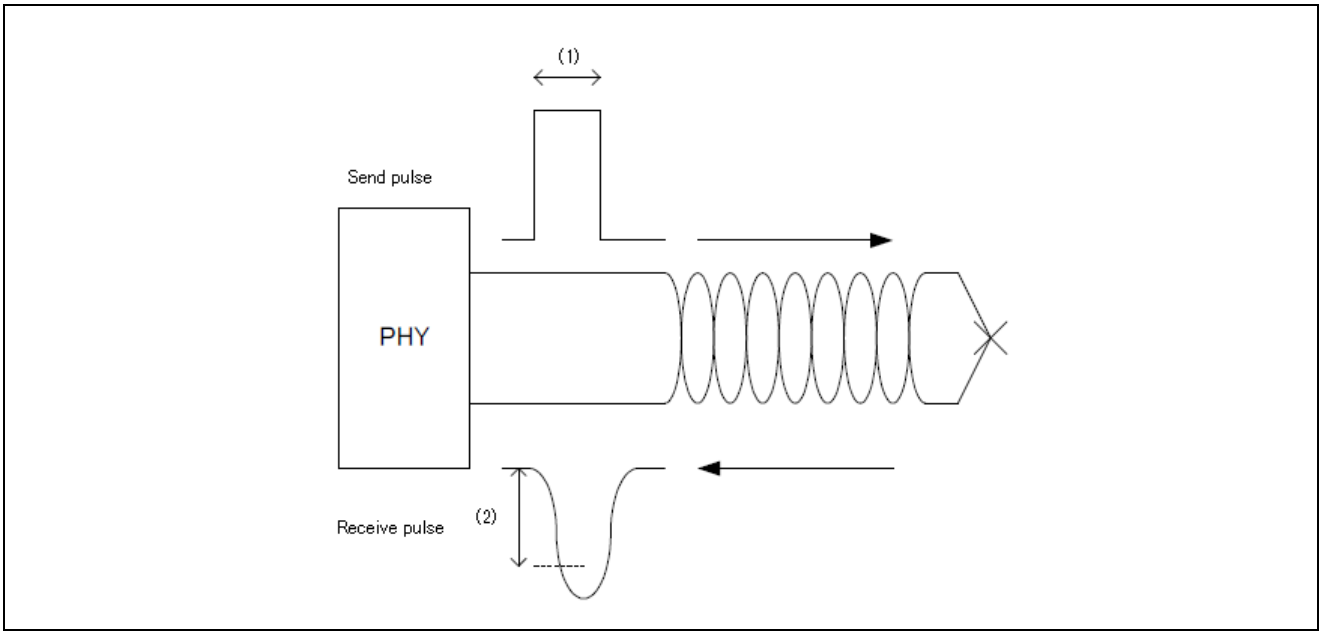


Figure 7.3 Operation when Cable is Short-Circuited

The operation of TDR function is performed by using register 25 and register 26 as follows.

Disable the auto-negotiation and auto-crossover and set to 100Base-Half Duplex at first, otherwise measuring cannot be performed correctly. Then, set the register with parameters relating to transmission pulse and pulse detection whether the TX line or RX line is measured. Pulse is sent by writing 1 to the DIAG_INIT bit and the measurement is started after the configuration is complete. When the measurement is completed, the DIAG_DONE bit is set to 1. The value of counter when pulse is detected is saved in the DIAGCNT register and the information about open or short is saved in the DIAG_POL register at this time.

The following shows an example of setting the parameters when measuring. However, it is necessary to adjust some parameters depending on the configuration of hardware and the installation environment.

No.	Cable Length	ADC_TRIGGER	CNT_WINDOW	PW_DIAG	Conditions of Counter Value
1	Below 20m	10	15	2	DIAGCNT ≠ 255 and DIAGCNT ≤ 42
2	20m to 40m	10	30	8	DIAGCNT ≠ 255 and 32 ≤ DIAGCNT ≤ 68
3	40m to 60m	8	50	8	DIAGCNT ≠ 255 and 56 ≤ DIAGCNT ≤ 88
4	60m to 80m	8	60	12	DIAGCNT ≠ 255 and 78 ≤ DIAGCNT ≤ 114
5	More than 80m	8	75	12	DIAGCNT ≠ 255 and 106 ≤ DIAGCNT

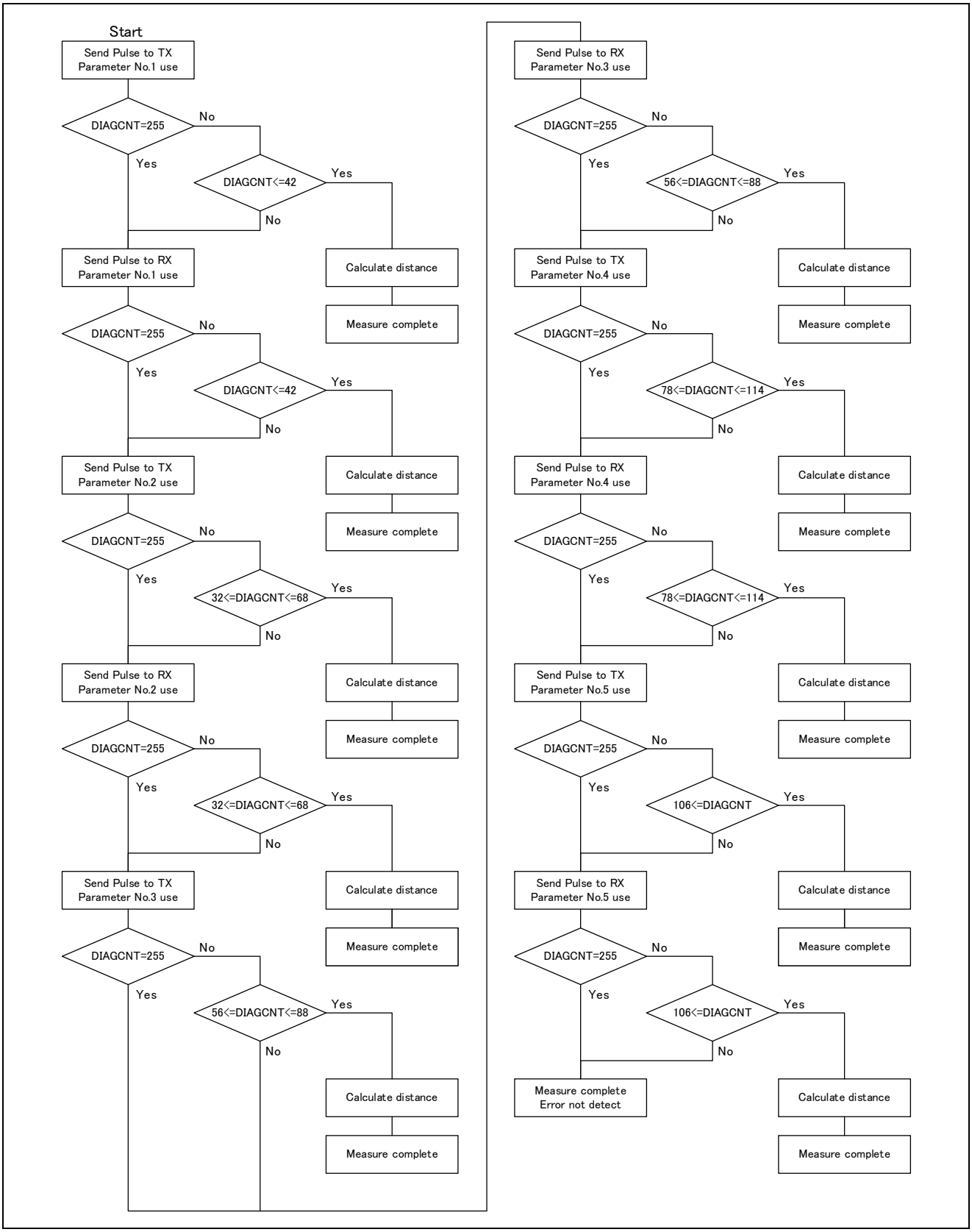


Figure 7.4 Cable Diagnostic Process Flow

7.2.4 Fast Link-Loss Detection Function

It is possible to generate the interrupt as soon as possible or bring down the link by monitoring the state of the communication when the communication is poor. Two functions with BER monitor and FEQ monitor are available.

(1) BER Monitor

The bit error rate (BER) monitor function can be used to measure the bit error of specific time, count the number of errors and notify. When the threshold is exceeded, it can link down as a trigger and inform the CPU by generating an interrupt signal. Element to be an error is different in the IDLE state and data communication as follows.

- In the IDLE state when communication is not performed, count the error judged as bit error when received symbol is other than IDLE symbol or J symbol which means the start of frame. Error count is only one when continuous error symbols without normal symbols are received.
- When the communication is performed, count the error judged as bit error when received symbol is other than data code group, IDLE code group or control code group in 32 kinds of symbols. Error count is up whenever error symbol is received.

The operation of the BER monitor function is done by register 23 and as shown below.

The first step is to check whether the port is in the link state by reading BER_LNK_OK. Note that the port does not work properly in the link-down state. Set the BER_CNT_LNK_EN, BER_CNT_TRIG, and BER_WINDOW parameters once the link state is verified. The error detection function starts to operate by writing 0 to BER_WINDOW. An interrupt is generated when the number of errors exceeding the threshold is detected within the specified time in the BER_WINDOW. When using the interrupt, release the interrupt mask by writing 1 to bit 10 in register 30 before setting the said parameters. To end the operation of BER function, write 0 to BER_WINDOW. When an interrupt was used, mask the interrupt by writing 0 to bit 10 in register 30.

(2) FEQ Monitor

To stably receive the incoming data, optimization is done by filtering the incoming signal by DSP in the PHY. FEQ is the coefficients of this filter and the value fluctuates greatly when the amplitude of the signal being received is changed. It can output the interrupt when detecting variation that exceeds the threshold set in advance or link down by monitoring the variation.

The operation of the FEQ monitor function is done by register 24 and as shown below.

Firstly, set the variation to be detected in FEQ_DELTA. The reference value at the time of writing can be referred by writing 0xfffe to FEQ_DELTA and reading FEQ_VAL. FEQ monitor function will begin to work when the threshold of variable of FEQ_DELTA is set. Current value of FEQ monitor can be detected by reading FEQ_VAL. An interrupt is generated when the value of FEQ_VAL exceeds the threshold. When using the interrupt, release the interrupt mask by writing 1 to bit 9 in register 30 before setting the said parameters. To end the operation of FEQ function, write 0xFFFF to FEQ_DELTA. When an interrupt was used, mask the interrupt by writing 0 to bit 9 in register 30.

7.3 Power-Down Mode

The hardware power-down mode, software power-down mode, and energy detection power-mode are available, and each of the power-down modes is described as follows.

7.3.1 Hardware Power-Down Mode

The operation is shifted to hardware power-down mode by setting 1 to bit 2 (P0PHYEN) or bit 5（P1PHYEN) in the Ethernet PHY operation mode control register (PHYMD). The Ethernet PHY does not work at all in hardware power-down mode and MII management registers cannot be accessed. The power consumption of the port will be almost 0. To wake up from the hardware power-down mode, set 0 to bit 2 (P0PHYEN) or bit 5 (P1PHYEN) in the Ethernet PHY operation mode control register (PHYMD). When returning from the hardware power-down mode, both analog and digital circuits are initialized by the Ethernet PHY and so are MII management registers. Hardware power-down mode must be kept for more than 100us.

7.3.2 Software Power-Down Mode

The operation is shifted to software power-down mode by setting 1 to bit 11 (POWERDOWN) in MII management register 0 with the Ethernet PHY. The IDLE signal is not output in the transition to software power-down mode and in software power-down mode. However, MII management registers can be accessed and the Ethernet PHY can be controlled in software power-down mode. To wake up from the software power-down mode, set 0 to bit 11 (POWERDOWN) in MII management register 0. The digital circuits are initialized automatically by the Ethernet PHY at the end of software power-down mode. However, note that some bits in MII management registers are not initialized. This applies to the bit described as "NASR" in Section 7.4, MII Management Registers in Ethernet PHY.

7.3.3 Energy Detection Power-Down Mode

The operation is shifted to energy detection power-down mode by setting 1 to bit 13 (EDPWRDOWN) in MII management register 17 with the Ethernet PHY. Note that the operation does not shift to the energy detection power-down mode when auto-negotiation is enabled. In this mode, the Ethernet PHY will not output anything except for several modules such as the serial management interface when there is no input of link pulse or packet signal to the Ethernet PHY. The Ethernet PHY will be reset automatically to the speed before becoming energy detection power-down mode, when link pulse or packet signal is input to the Ethernet PHY in this state. At that time, receiving the first and the next signals may be failed because of the detection of link pulse and packet signal.

Set 0 to bit 13 (EDPWRDOWN) in MII management register 17 to end the energy detection power-down mode and return to the normal mode.

7.4 MII Management Registers in Ethernet PHY

The MII management registers are included in the Ethernet PHY. These registers specify various settings of the Ethernet PHY and capture the state of the Ethernet PHY. These registers can be accessed via the serial management interface from each MAC, by accessing the MIIM register of on-chip Ethernet MAC or the MII management interface register of EtherCAT slave controller.

Caution: Registers 8 to 15 are mirror registers of registers 24 to 31 and there are no actual registers 8 to 15. Access to registers 8 to 15 is prohibited.

Table 7.1 List of PHY MII Management Registers

Register Address	Register Name	Type
0	Control register	Basic
1	Status register	Basic
2	PHY identifier	Extension
3	PHY identifier	Extension
4	Auto-negotiation advertisement register	Extension
5	Auto-negotiation link partner ability register	Extension
6	Auto-negotiation expansion register	Extension
7	Auto-negotiation next page transmit register	Extension
8	Unsupported (Access prohibited for the mirror of register 24)	-
9	Unsupported (Access prohibited for the mirror of register 25)	-
10	Unsupported (Access prohibited for the mirror of register 26)	-
11	Unsupported (Access prohibited for the mirror of register 27)	-
12	Unsupported (Access prohibited for the mirror of register 28)	-
13	Unsupported (Access prohibited for the mirror of register 29)	-
14	Unsupported (Access prohibited for the mirror of register 30)	-
15	Unsupported (Access prohibited for the mirror of register 31)	-
16	Silicon revision register	Vendor-specific
17	Mode control/status register	Vendor-specific
18	Special mode register	Vendor-specific
19	Reserved	Vendor-specific
20	Reserved	Vendor-specific
21	Reserved	Vendor-specific
22	Reserved	Vendor-specific
23	BER counter register	Vendor-specific
24	FEQ monitor register	Vendor-specific
25	Diagnostic control/status register	Vendor-specific
26	Diagnostic counter register	Vendor-specific
27	Special control/status indication register	Vendor-specific
28	Reserved	Vendor-specific
29	Interrupt factor register	Vendor-specific
30	Interrupt factor mask register	Vendor-specific
31	PHY special control/status register	Vendor-specific

Symbols except R and W below bit names in each register section mean the following.

SC : Self clearing after process completion
LL : Latching low level, clear on read of register
LH : Latching high level, clear on read of register
NASR : Not initialized by software power-down mode

7.4.1 Register 0 - Control Register

Register 0 makes the basic settings of Ethernet PHY.

MR0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET	LOOPBACK	SPEED_ SELECTION	AUTO-NEGOTIATION_ENABLE	POWERDOWN	ISOLATE	RESTART_AUTO-NEGOTIATION	DUPLEX_MODE	COLLISION_TEST	(RESERVED)						
RW/ SC	RW	RW	RW	RW	RW	RW/ SC	RW	RW	R	R	R	R	R	R	R

Register Address 00H

Initial Value 1000H

Bit Position	Bit Name	Description
15	RESET	Resets the Ethernet PHY. Settings of other bits in this register should not be changed when resetting. 0: Normal operation 1: Software reset
14	LOOPBACK	Enables/Disables the internal loop-back mode 0: Disabled 1: Enabled
13	SPEED_SELCTION	Sets the link speed 0: 10 Mb/s 1: 100 Mb/s
12	AUTO-NEGOTIATION_ ENABLE	Enables/Disables the auto-negotiation 0: Disabled 1: Enabled
11	POWERDOWN	Sets the power-down mode 0: Normal operation 1: Power-down mode
10	ISOLATE	Sets isolation 0: Normal operation 1: Electrically disconnected from the MII
9	RESTART_ AUTO-NEGOTIATION	Restarts the auto-negotiation process 0: Normal operation 1: Restarts the auto-negotiation process
8	DUPLEX_MODE	Sets the duplex mode. This setting is invalid when bit 12 is 1. 0: Half duplex 1: Full duplex
7	COLLISION_TEST	Enables/Disables the collision signal test 0: Disabled 1: Enabled
6 to 0	(RESERVED)	Reserved (Write 0 and ignore reading)

7.4.2 Register 1 - Status Register

Register 1 shows the status of Ethernet PHY.

MR1

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
100BASE-T4	100BASE-TX_ FULL_DUPLEX	100BASE-TX_ HALF_DUPLEX	10M_FULL_ DUPLEX	10M_HALF_ DUPLEX	(RESERVED)					AUTO-NEGOTIOATIO N_COMPLETE	REMOTE_FAULT	AUTO-NEGOTIOATIO N_ABILITY	LINK_STATUS	JABBER_DETECT	EXTENDED_ CAPABILITY
R	R	R	R	R	R	R	R	R	R	R	R/LH	R	R/LL	R/LH	R

Register Address 01H

Initial Value 7809H

Bit Position	Bit Name	Description
15	100BASE-T4	Enables/Disables 100BASE-T4 communication 0: Disabled 1: Enabled
14	100BASE-TX_ FULL_DUPLEX	Enables/Disables 100BASE-TX full-duplex communication 0: Disabled 1: Enabled
13	100BASE-TX_ HALF_DUPLEX	Enables/Disables 100BASE-TX half-duplex communication 0: Disabled 1: Enabled
12	10M_FULL_DUPLEX	Enables/Disables 10 Mb/s full-duplex communication 0: Disabled 1: Enabled
11	10M_HALF_DUPLEX	Enables/Disables 10 Mb/s half-duplex communication 0: Disabled 1: Enabled
10 to 6	(RESERVED)	Reserved (Write 0 and ignore reading)
5	AUTO-NEGOTIATION_ COMPLETE	Notice of Auto-Negotiation Completion 0: Not completed 1: Completed
4	REMOTE_FAULT	Indicates the detection result of failure in remote side. 0: Failure not detected 1: Failure detected
3	AUTO-NEGOTIATION_ ABILIT	Enables/Disables auto-negotiation communication 0: Disabled 1: Enabled
2	LINK_STATUS	Shows the status of link 0: Link down 1: Link up
1	JABBER_DETECT	Shows the detection result of jabber state 0: Jabber not detected 1: Jabber detected
0	EXTENDED_ CAPABILITY	Shows whether the extended register is used 0: Only basic register set is used 1: Extended register set is used

7.4.3 Registers 2, 3 - PHY Identifier

Registers 2, 3 show the identification number of PHY in a total of 32 bits.

MR2

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHY_ID_NUMBER															
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Register Address: 02H
Initial Value: 0033H

Bit Position	Bit Name	Description
15 to 0	PHY_ID_NUMBER	3rd to 18th bits of OUI

MR3

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHY_ID_NUMBER						MODEL_NUMBER						REVISION_NUMBER			
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Register Address: 03H
Initial Value: 2002H

Bit Position	Bit Name	Description
15 to 10	PHY_ID_NUMBER	19th to 24th bits of OUI
9 to 4	MODEL_NUMBER	Manufacturer model number
3 to 0	REVISION_NUMBER	Manufacturer revision number

7.4.4 Register 4 - Auto-Negotiation Advertisement Register

Register 4 indicates the information to be sent to the partner in auto-negotiation mode.

MR4

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NEXT_PAGE	(RESERVED)	REMOTE_FAULT	(RESERVED)	PAUSE_OPERATION		100BASE-T4	100BASE-TX_FULL_DUPLEX	100BASE-TX	10BASE-T_FULL_DUPLEX	10BASE-T	SELECTOR_FIELD				
RW	R	RW	RW	RW	RW	R	RW	RW	RW	RW	RW	RW	RW	RW	RW

Register Address: 04H
Initial Value: 01E1H

Bit Position	Bit Name	Description
15	NEXT_PAGE	Support of Next Page Function 0: Not supported 1: Supported
14	(RESERVED)	Reserved (Write 0 and ignore reading)
13	REMOTE_FAULT	Sets the state of local device with the remote fault detection function 0: Fault not detected 1: Fault detected
12	(RESERVED)	Reserved (Write 0 and ignore reading)
11, 10	PAUSE_OPERATION	Set the pause operation 00: No pause operation 01: Symmetric pause operation 10: Asymmetric pause operation to the link partner 11: Asymmetric pause operation to symmetric pause and local device
9	100BASE-T4	100BASE-T4 Support (Fixed to 0 in this LSI) 0: Not supported 1: Supported
8	100BASE-TX_ FULL_DUPLEX	100BASE-TX Full-Duplex Support 0: Not supported 1: Supported
7	100BASE-TX	100BASE-TX Support 0: Not supported 1: Supported
6	10BASE-T_ FULL_DUPLEX	10BASE-T Full-Duplex Support 0: Not supported 1: Supported
5	10BASE-T	10BASE-T Support 0: Not supported 1: Supported
4 to 0	SELECTOR_FIELD	00001: IEEE std 802.3

7.4.5 Register 5 - Auto-Negotiation Link Partner Ability (Base Page) Register

Register 5 shows the base page of the information received from the partner when using auto negotiation.

MR5 (Base Page)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NEXT_PAGE	ACKNOWLEDGE	REMOTE_FAULT	(RESERVED)		PAUSE_OPERATION	100BASE-T4	100BASE-TX_FULL_DUPLEX	100BASE-TX	10BASE-T_FULL_DUPLEX	10BASE-T	SELECTOR_FIELD				
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Register Address: 05H
Initial Value: 0001H

Bit Position	Bit Name	Description
15	NEXT_PAGE	Indicates whether there are additional next pages 0: Last page 1: Additional next pages
14	ACKNOWLEDGE	Result of Link Signal Received from the Link Partner 0: Failed 1: Successfully completed
13	REMOTE_FAULT	Fault Condition of the Link Partner 0: Without any fault 1: With a fault
12, 11	(RESERVED)	Reserved (Write 0 and ignore reading)
10	PAUSE_OPERATION	Pause Operation of MAC in the Remote Device Side 0: Not supported 1: Supported
9	100BASE-T4	100BASE-T4 Support (Fixed to 0 in this LSI) 0: Not supported 1: Supported
8	100BASE-TX_FULL_DUPLEX	100BASE-TX Full-Duplex Support 0: Not supported 1: Supported
7	100BASE-TX	100BASE-TX Support 0: Not supported 1: Supported
6	10BASE-T_FULL_DUPLEX	10BASE-T Full-Duplex Support 0: Not supported 1: Supported
5	10BASE-T	10BASE-T Support 0: Not supported 1: Supported
4 to 0	SELECTOR_FIELD	00001: IEEE std 802.3

7.4.6 Register 5 - Auto-Negotiation Link Partner Ability (Next Page) Register

Register 5 shows the next page of the information received from the partner when using auto negotiation.

MR5 (Next Page)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NEXT_PAGE	ACKNOWLEDGE	MESSAGE_PAGE	ACKNOWLEDGE2	TOGGLE	MESSAGE_UNFORMATTED_CODE_FIELD										
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

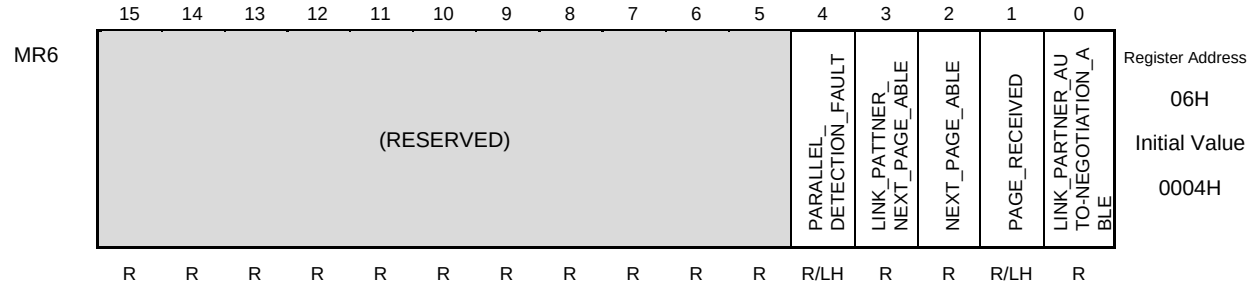
Register Address: 05H

Initial Value: 0000H

Bit Position	Bit Name	Description
15	NEXT_PAGE	Indicates whether there are additional next pages 0: Last page 1: Additional next pages
14	ACKNOWLEDGE	Result of Link Signal Received from the Link Partner 0: Failed 1: Successfully completed
13	MESSAGE_PAGE	Encoding Method of Code Filed for Bits 10 to 0 0: Unformatted page 1: Message page
12	ACKNOWLEDGE2	Shows correspondence to the message 0: Not supported 1: Supported
11	TOGGLE	Used for synchronization with the link partner at the replacement of the next page. 0: Sent link code word is 1 1: Sent link code word is 0
10 to 0	MESSAGE_UNFORMATTED_CODE_FIELD	11-Bit Code Word Received from the Link Partner

7.4.7 Register 6 - Auto-Negotiation Expansion Register

Register 6 shows the information when using auto negotiation.



Bit Position	Bit Name	Description
15 to 5	(RESERVED)	Reserved (Write 0 and ignore reading)
4	PARALLEL_ DETECTION_FAULT	Shows whether the failure was detected in parallel detection function. This bit is set to 0 when reading register 6. 0: Not detected 1: Detected
3	LINK_PATNER_ NEXT_PAGE_ABLE	Next Page Function of Link Partner Support 0: Not supported 1: Supported
2	NEXT_PAGE_ABLE	Next Page Function of Local Device Support 0: Not supported 1: Supported
1	PAGE_RECEIVED	Indicates that a new link code word is received and stored in register 5. This bit is cleared to 0 when reading register 6. 0: New page is not received 1: New page is received
0	LINK_PATNER_ AUTO-NEGOTIATION_ ABLE	Auto-Negotiation with Link Partner Support 0: Not supported 1: Supported

7.4.8 Register 7 - Auto-Negotiation Next Page Transmit Register

Register 7 shows the next page of the information to be transmitted to the partner when using auto negotiation.

MR7

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NEXT_PAGE	(RESERVED)	MESSAGE_PAGE	ACKNOWLEDGE2	TOGGLE	MESSAGE_UNFORMATTED_CODE_FIELD										
RW	R	RW	RW	R	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Register Address 07H

Initial Value 2001H

Bit Position	Bit Name	Description
15	NEXT_PAG	Indicates whether there are additional next pages 0: Last page 1: Additional next pages
14	(RESERVED)	Reserved (Write 0 and ignore reading)
13	MESSAGE_PAGE	Encoding Method of Code Filed for Bits 10 to 0 0: Unformatted page 1: Message page
12	ACKNOWLEDGE2	Shows correspondence to the message 0: Not supported 1: Supported
11	TOGGLE	Used for synchronization with the link partner at the replacement of the next page. 0: Sent link code word is 1 1: Sent link code word is 0
10 to 0	MESSAGE_UNFORMATTED_CODE_FIELD	11-Bit Code Word to be Transmitted to the Link Partner

7.4.9 Register 16 - Silicon Revision Register

Register 16 shows the silicon revision.

MR16

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
(RESERVED)						SILICON_REVISION				(RESERVED)					
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Register Address: 10H

Initial Value: 0040H

Bit Position	Bit Name	Description
15 to 10	(RESERVED)	Reserved (Write 0 and ignore reading)
9 to 6	SILICON_REVISION	These bits show the silicon revision.
5 to 0	(RESERVED)	Reserved (Write 0 and ignore reading)

7.4.10 Register 17 - Mode Control/Status Register

Register 17 specifies the operating mode of Ethernet PHY.

(1/2)

MR17

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
(RESERVED)	FASTRIP	EDPWRDOWN	(RESERVED)	LOWSQEN	(RESERVED)	FARLOOPBACK	FASTEST	AUTOMDIX_EN	MDI_MODE	(RESERVED)	DCD_PAT_GEN	(RESERVED)	FORCE_GOOD_LINK_STATUS	ENERGYON	(RESERVED)
RW	RW, NASR	RW	RW	RW	RW	RW	RW	RW	RW	R	RW	RW	RW	R	RW

Register Address 11H

Initial Value 0080H

Bit Position	Bit Name	Description
15	(RESERVED)	Reserved (Write 0 and ignore reading)
14	FASTRIP	Sets the 10BASE-T fast mode. This bit can only be used for simulation. 0: Normal operation 1: PHYT_10 test mode
13	EDPWRDOWN	Enables/Disables the energy detection power-down mode. 0: Disabled 1: Enabled
12	(RESERVED)	Reserved (Write 0 and ignore reading)
11	LOWSQEN	Low squelch setting 0: Normal operation 1: Low down the threshold (Increase the sensitivity of signal)
10	(RESERVED)	Reserved (Write 0 and ignore reading)
9	FARLOOPBACK	Enables/Disables the remote loopback mode. When enabled, all the received packets are sent back simultaneously. This bit supports only the 100BASE-TX/FX mode. 0: Disabled 1: Enabled
8	FASTEST	Enables/Disables the test mode of auto negotiation. This bit can only be used for simulation. It also shortens the time for software reset. 0: Disabled 1: Enabled
7	AUTOMDIX_EN	Enables/Disables the auto-MDIX function 0: Disabled (Set manually by bit 6 in register 17) 1: Enabled
6	MDI_MODE	When bit 7 in register 17 is 0, this bit sets the MDI/MDI-X mode manually. When bit 7 in register 17 is 1, this bit indicates the status of mode. Writing to the register is disabled at this time. 0: MDI mode 1: MDI-X mode
5	(RESERVED)	Reserved (Write 0 and ignore reading)

(2/2)

Bit Position	Bit Name	Description
4	DCD_PAT_GEN	Enables/Disables the pattern generation for DCD measurement in test mode. 0: Disabled 1: Enabled
3	(RESERVED)	Reserved (Write 0 and ignore reading)
2	FORCE_GOOD_LINK_STATUS	Shifts the operation to the link status forcibly. This bit is used only for testing. 0: Normal operation 1: Link status of 100BASE-X
1	ENERGYON	Shows the energy detection state of line. 0: Energy from the line within 256 ms is not detected. 1: Energy from the line is detected.
0	(RESERVED)	Reserved (Write 0 and ignore reading)

7.4.11 Register 18 - Special Mode Register

Register 18 specifies the mode setting of Ethernet PHY.

MR18

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
(RESERVED)					FX_MODE	(RESERVED)	PHY_MODE[3:0]				PHY_ADD[4:0]				
RW	R	R	RW	RW	RW NASR	RW	RW NASR	RW NASR	RW NASR	RW NASR	RW NASR	RW NASR	RW NASR	RW NASR	RW NASR

Register Address 12H

Initial Value 00E0H

Bit Position	Bit Name	Description
15to 11	(RESERVED)	Reserved (Write 0 and ignore reading)
10	FX_MODE	Enables/Disables the 100BASE-FX mode. When enabling the 100BASE-FX mode, PHY_MODE (bits 8 to 5 in register 18) must be 0011 or 0010. 0: Disabled (10BASE-T/100BASE-TX mode) 1: Enabled
9	(RESERVED)	Reserved (Write 0 and ignore reading)
8 to 5	PHY_MODE[3:0]	These bits set the PHY operating mode.
4to 0	PHY_ADD[4:0]	These bits specify the PHY address. Setting of PHY_ADD[0] is ignored and 0 is assigned to port 0 while 1 to port 1.

PHY_MODE [3:0]	Speed	Duplex	Auto negotiation
0000	10BASE-T	Half-duplex	Invalid
0001	10BASE-T	Full-duplex	Invalid
0010	100BASE-TX/FX	Half-duplex	Invalid. Enable CRS of sending and receiving.
0011	100BASE-TX/FX	Full-duplex	Invalid. Enable CRS of sending.
0100	100BASE-T	Half-duplex	Valid. Enable CRS of sending and receiving.
0101	100BASE-T repeater mode	Half-duplex	Valid. Enable CRS of receiving.
0110	Power-down mode (For testing)	-	-
0111	All	Both sides	Valid
1000	All	Full-duplex force by parallel detection	Enable quick auto negotiation. Select timing by bit 1 and bit 0[Note 1].
1001			
1010			
1011			
1100		Half-duplex by parallel detection(standard)	
1101			
1110			
1111	Loopback/Isolate	-	- (Internal loop-back mode)

Note 1. The timing of auto-negotiation can be changed in order to reduce the auto-negotiation time between 2 PHYs. It is possible to adjust the timing by changing the settings when link problem appears.

PHY_MODE[3]	PHY_MODE[1:0]	Break Link Timer	Auto-Negotiation Wait Timer	Link Fail Inhibit Timer
0	XX	1250 ms	850 ms	850 ms
1	00	80 ms	35 ms	50 ms
1	01	120 ms	50 ms	75 ms
1	10	240 ms	100 ms	150 ms
1	11 (IEEE compliant)	1250 ms	850 ms	850 ms

7.4.12 Register 19 - Reserved

MR19

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
(RESERVED)															
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Register Address 13H

Initial Value 0000H

Bit Position	Bit Name	Description
15 to 0	(RESERVED)	Reserved (Write 0 and ignore reading)

7.4.13 Register 20 - Reserved

MR20

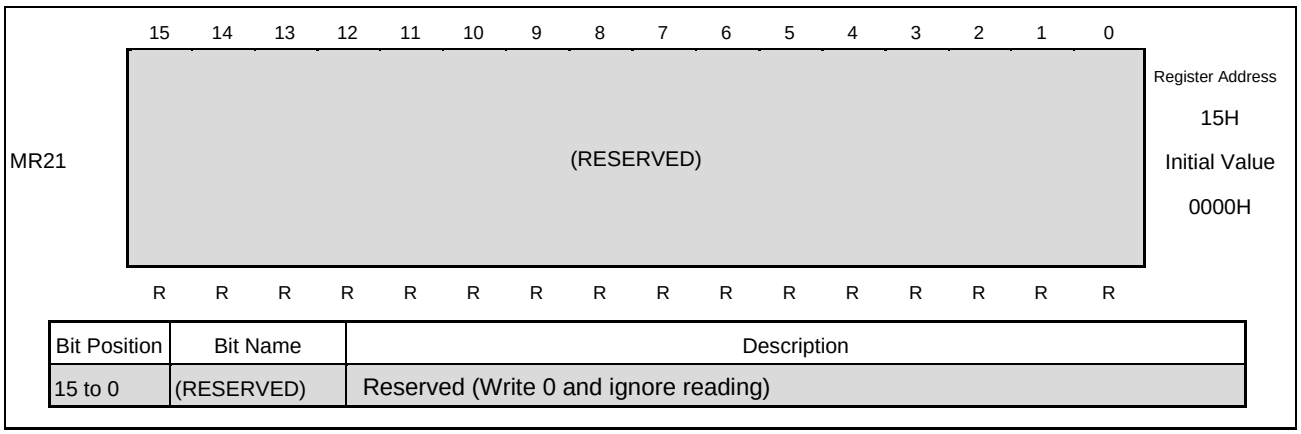
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
(RESERVED)															
RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Register Address 14H

Initial Value 0000H

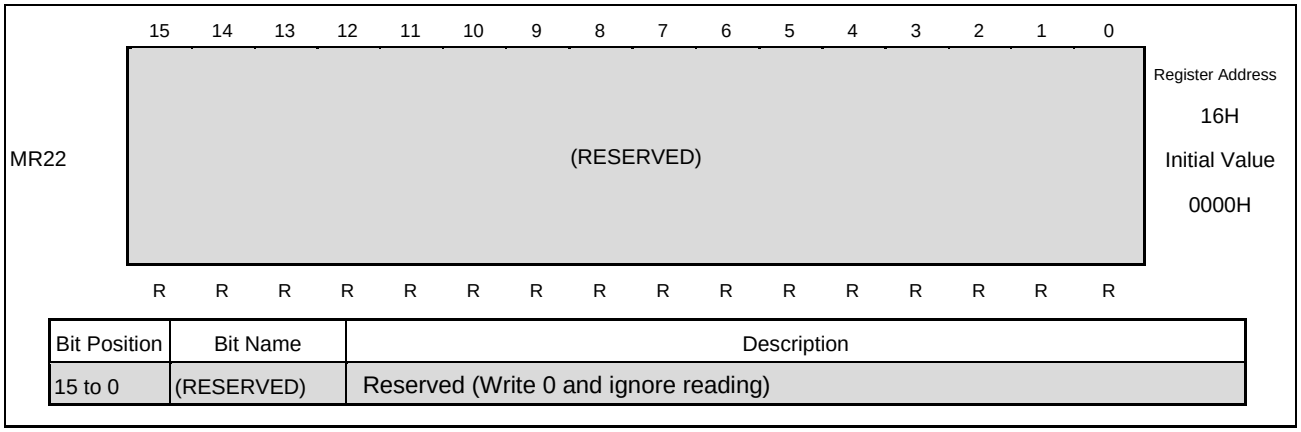
Bit Position	Bit Name	Description
15 to 0	(RESERVED)	Reserved (Write 0 and ignore reading)

7.4.14 Register 21 - Reserved



Bit Position	Bit Name	Description
15 to 0	(RESERVED)	Reserved (Write 0 and ignore reading)

7.4.15 Register 22 - Reserved



Bit Position	Bit Name	Description
15 to 0	(RESERVED)	Reserved (Write 0 and ignore reading)

7.4.16 Register 23 - BER Counter Register

Register 23 sets the BER counter function of Ethernet PHY and shows the BER results.

MR23

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BER_LNK_OK	BER_CNT_LNK_EN	BER_CNT_TRIG			BER_WINDOW				BER_COUNT						
R	RW	RW	RW	RW	RW	RW	RW	RW	R	R	R	R	R	R	R

Register Address 17H

Initial Value 5080H

Bit Position	Bit Name	Description
15	BER_LNK_OK	Shows the quality status of the link. It turns to 1 if the value of BER counter is below the threshold after startup. It is used to detect the reliable links after startup. 0: Not linked or the state of the link is not good. 1: The state of the link is good.
14	BER_CNT_LNK_EN	Operation when the count value of BER and FEQ monitor exceeds the threshold 0: Only BER_LNK_OK becomes 0 without bringing down the link. 1: Bring down the link.
13 to 11	BER_CNT_TRIG	These bits set the condition to determine the link down or interrupt occurrence by the value of BER counter. 0: 1 or more 1: More than 1 (2 or more) 2: More than 2 (3 or more) 3: More than 4 (5 or more) 4: More than 8 (9 or more) 5: More than 16 (17 or more) 6: More than 32 (33 or more) 7: More than 64 (65 or more)
10 to 7	BER_WINDOW	These bits set the width of the window of BER counter. 1: 0.2 ms 2: 0.4 ms 3: 0.8 ms … 15: 3.2 sec
6 to 0	BER_COUNT	Count value of bit errors in the window time before current.

7.4.17 Register 24 - FEQ Monitor Register

Register 24 sets the FEQ monitor function of Ethernet PHY and shows the FEQ results.

MR24

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FEQ_DELTA / FEQ_VAL															
RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Register Address: 18H

Initial Value: 0000H

Bit Position	Bit Name	Description
15 to 0	FEQ_DELTA (Write)	These bits set the amount of change in FEQ2 factor allowed for the value of the reference that has been latched. When the BER_CNT_LINK_EN bit in register 23 is 1, if the value of FEQ2 exceeds this value, FEQ interrupt is generated and the link is down. FFFF: Disable FEQ monitor function and continue to latch on the FEQ2 factor ongoing. FFFE: The current reference value can be read from this register. The value of FEQ_DELTA does not change. Others: Set the threshold of amount of change. FEQ monitor function starts to work with setting this value.
	FEQ_VAL (Read)	These bits show bits 17 to 2 of FEQ2 coefficient latched as a reference when write FFFE to FEQ_DELTA. Others: Current FEQ2 coefficient.

7.4.18 Register 25 - Diagnostic Control/Status Register

Register 25 sets the diagnostic function of Ethernet PHY and shows the results.

MR25

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
(RESERVED)	DIAG_INIT	ADC_MAX_VALUE / ADC_TRIGGER						DIAG_DONE	DIAG_POL	DIAG_SEL_LINE	PW_DIAG				
RW	RW/SC	RW	RW	RW	RW	RW	RW	R	R	RW	RW	RW	RW	RW	RW

Register Address: 19H
Initial Value: 0000H

Bit Position	Bit Name	Description
15	(RESERVED)	Reserved (Write 0 and ignore reading)
14	DIAG_INIT	Starts TDR test and generates a single cycle pulse. 0: Normal operation 1: Pulse generation (Turns to 0 after pulse generation)
13 to 8	ADC_MAX_VALUE (Read)	These bits show the maximum/minimum signed value of the reflected wave. When the TDR test starts, PHY sends out a trigger pulse and waits for the reflected wave for 255 cycles (2040 ns) of 8-ns clock. The DIAG_DONE bit is set after the time. These bits indicate the maximum value of the received wave if it is a positive value and the minimum value if negative.
	ADC_TRIGGER (Write)	These bits set the threshold voltage for detecting the reflected wave from 000111(0.5 V) to 001111 (1.5 V). This setting cannot be read.
7	DIAG_DONE	Shows that the counter is stopped. 0: Running or TDR untested 1: Stop (set to 0 after reading)
6	DIAG_POL	Shows the polarity of the reflected wave detected. 0: Positive logic 1: Negative logic
5	DIAG_SEL_LINE	Selects the line to implement the TDR test. 0: RX line 1: TX line
4 to 0	PW_DIAG	These bits set the width of the pulse send out at TDR test in the range of 8 ns to 248 ns for each 8 ns. 0: Normal operation Other than 0: Setting x 8 ns

7.4.19 Register 26 - Diagnostic Counter Register

Register 26 sets the diagnostic counter of Ethernet PHY and shows the results.

MR26

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CNT_WINDOW								DIAGCNT							
RW	RW	RW	RW	RW	RW	RW	RW	R	R	R	R	R	R	R	R

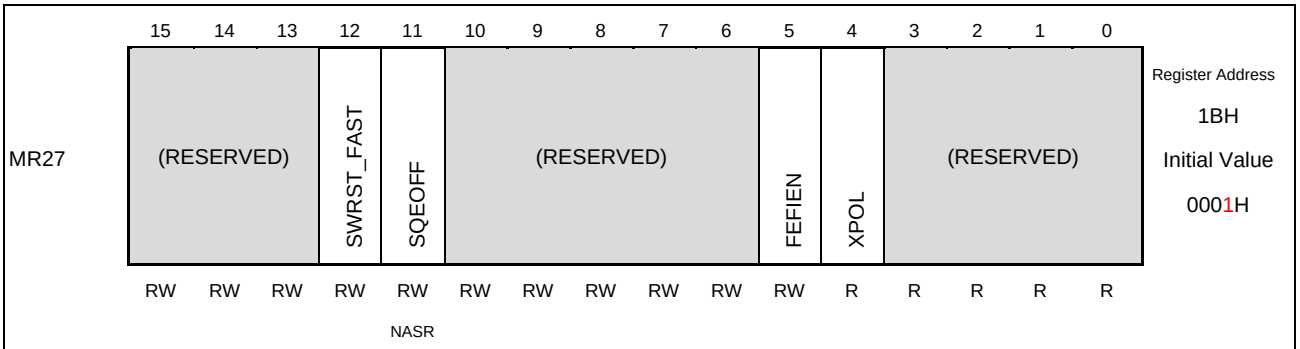
Register Address: 1AH

Initial Value: 0000H

Bit Position	Bit Name	Description
15 to 8	CNT_WINDOW	These bits set the time to mask as invalid detection result from the start of delivery of the pulse. This setting is to avoid the false detection of the sent pulse itself and the influence of noise immediately after the pulse is sent. It will be about 0.8 m per 1 count.
7 to 0	DIAGCNT	These bits show the value of the counter when the reflected wave is detected. They turn to 0x00 immediately after sending a pulse while DIAG_INIT is set to 1, and 0xFF when the reflected wave is not detected. They become 0x01 if the cable is not connected.

7.4.20 Register 27 - Special Control/Status Instruction Register

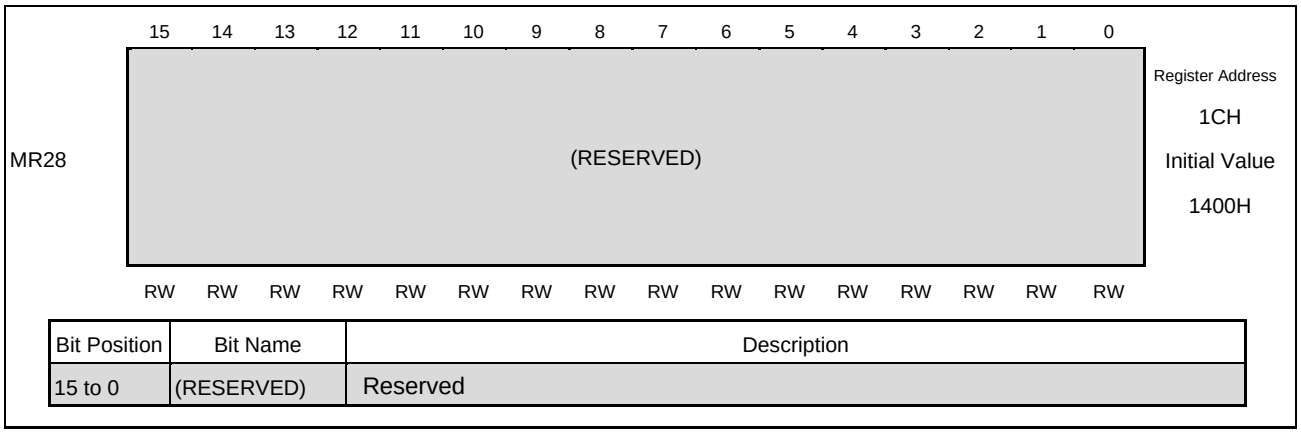
Register 27 sets the PHY mode of Ethernet PHY and shows the results.



Bit Position	Bit Name	Description
15 to 13	(RESERVED)	Reserved (Write 0 and ignore reading)
12	SWRST_FAST	Test the software reset counter 0: Normal operation 1: Shorten the software reset counter from 256 us to 10 us (for production test)
11	SQEOFF	Valid/Invalid the SQE test 0: Valid 1: Invalid
10 to 6	(RESERVED)	Reserved (Write 0 and ignore reading)
5	FEFIEN	Valid/Invalid the setting of Far End Fault Indication in 100BASE-FX 0: Invalid 1: Valid
4	XPOL	Automatic polarity detection result of 10BASE-T 0: Normal 1: Reversal
3 to 0	(RESERVED)	Reserved (Write 0 and ignore reading)

7.4.21 Register 28 - Reserved

Register 28 is used for testing. Please don't read from or write to this register.



Bit Position	Bit Name	Description
15 to 0	(RESERVED)	Reserved

7.4.22 Register 29 - Interrupt Factor Register

Register 29 indicates the source of interrupt when the interrupt output of Ethernet PHY is active. Bit 1 points to the cause of the interrupt. Interrupt output is cleared by reading.

MR29

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
(RESERVED)			INT12	INT11	INT10	INT9	(RESERVED)	INT7	INT6	INT5	INT4	INT3	INT2	INT1	(RESERVED)
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Register Address
1DH
Initial Value
0000H

Bit Position	Bit Name	Description
15 to 13	(RESERVED)	Reserved (Write 0 and ignore reading)
12	INT12	Clipping
11	INT11	Maxlvl
10	INT10	BER counter trigger
9	INT9	FEQ trigger
8	(RESERVED)	Reserved (Write 0 and ignore reading)
7	INT7	Energy detection of the line
6	INT6	Auto-negotiation is complete
5	INT5	Remote fault detection
4	INT4	Link down
3	INT3	Auto-negotiation is complete and receive the last FLP
2	INT2	Parallel detection failure
1	INT1	Auto-negotiation shifts to the complete acknowledge state.
0	(RESERVED)	Reserved (Write 0 and ignore reading)

7.4.23 Register 30 - Interrupt Factor Mask Register

Register 30 enables/disables interrupt factors of Ethernet PHY. "0" is invalid (mask), while "1" is valid.

MR30

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
(RESERVED)			INT12_MASK	INT11_MASK	INT10_MASK	INT9_MASK	(RESERVED)	INT7_MASK	INT6_MASK	INT5_MASK	INT4_MASK	INT3_MASK	INT2_MASK	INT1_MASK	(RESERVED)
R	R	R	RW	RW	RW	RW	R	RW	RW	RW	RW	RW	RW	RW	R

Register Address: 1EH

Initial Value: 0000H

Bit Position	Bit Name	Description
15 to 13	(RESERVED)	Reserved (Write 0 and ignore reading)
12	INT12_MASK	Clipping
11	INT11_MASK	Maxlvl
10	INT10_MASK	BER counter trigger
9	INT9_MASK	FEQ trigger
8	(RESERVED)	Reserved (Write 0 and ignore reading)
7	INT7_MASK	Energy detection of the line
6	INT6_MASK	Auto-negotiation is complete
5	INT5_MASK	Remote fault detection
4	INT4_MASK	Link down
3	INT3_MASK	Auto-negotiation is complete and receive the last FLP
2	INT2_MASK	Parallel detection failure
1	INT1_MASK	Auto-negotiation shifts to the complete acknowledge state.
0	(RESERVED)	Reserved (Write 0 and ignore reading)

7.4.24 Register 31 - PHY Special Control/Status Register

Register 31 does the configuration and status of the special features of Ethernet PHY.

MR31

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
(RESERVED)			AUTODONE	(RESERVED)					ENABLE_4B5B	(RESERVED)	SPEED_ INDICATION			RX_DV_J2T	SCRAMBLE_ DISABLE
RW	RW	RW	R	RW	RW	RW	RW	RW	RW	RW	R	R	R	RW	RW

Register Address: 1FH

Initial Value: 0040H

Bit Position	Bit Name	Description
15 to 13	(RESERVED)	Reserved (Write 0 and ignore reading)
12	AUTODONE	Completion notice of auto negotiation 0: Incomplete or auto negotiation not set 1: Completion
11 to 7	(RESERVED)	Reserved (Write 0 and ignore reading)
6	ENABLE_4B5B	Enables/disables settings in 4B/5B encoding/decoding 0: Invalid (Bypass 4B/5B encoding/decoding) 1: Valid
5	(RESERVED)	Reserved (Write 0 and ignore reading)
4 to 2	SPEED_ INDICATION	These bits show the speed 001: 10 Mbps half-duplex 101: 10 Mbps duplex 010: 100 Mbps half-duplex 110: 100 Mbps duplex
1	RX_DV_J2T	Sets the delimiter to identify the beginning and the end of the frame. 0: RX_DV rises by JK delimiter and falls down by TR delimiter. 1: RX_DV rises by J delimiter and falls down by T delimiter.
0	SCRAMBLE_ DISABLE	Valid/Invalid settings of data scrambling 0: Valid 1: Invalid

7.5 Ethernet PHY Function Setting Register

This register is used to change the operation that cannot be controlled by the MII management register of built-in Ethernet PHY without going through the serial management interface.

7.5.1 List of Registers

Register Name	Symbol	Address
Ethernet PHY operation mode control register	PHYMD	4001 06A0H
Ethernet PHY power-up status register	PHYPUS	4001 06A4H

7.5.2 Ethernet PHY Operation Mode Control Register (PHYMD)

PHYMD sets the operating mode of Ethernet PHY. It is a read/write accessible register in 32/16-bit units.

Caution: This register can be written only in case of releasing protection by specific sequence using the system protect command register (SYSPCMD). Refer to the system protect command register (SYSPCMD) for protection releasing procedure. In addition, the special sequence is not necessary in case of reading the value of this register.

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
PHYMD	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	P1PHYEN	P1FXMODE	P1ATMDIXEN	P0PHYEN	P0FXMODE	P0ATMDIXEN	4001 06A0H
																																	Initial Value
R/W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R/W	R/W	R/W	R/W	R/W	R/W	0000 003FH

Bit Position	Bit Name	Description
5	P1PHYEN	Valid/Invalid PHY of port 1 0: Valid 1: Invalid (initial value)
4	P1FXMODE	Valid/Invalid FX mode of port 1 (including the input/output pin control) 0: Valid 1: Invalid (initial value)
3	P1ATMDIXEN	Valid/Invalid MDIX automatic recognition of port 1 0: Invalid 1: Valid (initial value)
2	P0PHYEN	Valid/Invalid PHY of port 0 0: Valid 1: Invalid (initial value)
1	P0FXMODE	Valid/Invalid FX mode of port 0 (including the input/output pin control) 0: Valid 1: Invalid (initial value)
0	P0ATMDIXEN	Valid/Invalid MDIX automatic recognition of port 0 0: Invalid 1: Valid (initial value)

7.5.3 Ethernet PHY Power-Up Status Register (PHYPUS)

PHYPUS is used to confirm the power-up state of the built-in Ethernet PHY. This register is readable only in 32 bits. When hardware power-down mode is released, bit1 and/or bit0 are cleared around 5.2ms later.

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
PHYPUS	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	P1PWRUPRST	P0PWRUPRST	BASE + 06A4H
																																	Initial Value
																																	0000 0000H
R/W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R	R	

Bit Position	Bit Name	Description
1, 0	P1PWRUPRST, P0PWRUPRST	These bits inform the completion of the power-up of the built-in Ethernet PHY. 1: Power-up and reset 0: Power-up is complete

7.6 LED signal

Output pins showing internal PHY status. External LED can be connected.

Pin name	Function	Active
P0LINKLEDZ P1LINKLEDZ	Link Status 0: Linked 1: Unlinked	Low
P0DUPLEXLEDZ P1DUPLEXLEDZ	Duplex Status 0: Full duplex 1: Half duplex	―
P0SPEED100LEDZ P1SPEED100LEDZ	100Mbps Link Status 0: 100Mbps Linked 1: 100Mbps not Linked	Low
P0SPEED10LEDZ P1SPEED10LEDZ	10Mbps Link Status 0: 10Mbps Linked 1: Not 10Mbps Linked	Low
P0ACTLEDZ P1ACTLEDZ	Activity Status 0: Active on RX or TX 1: IDLE on both RX and TX When both RX and TX turn to IDLE, status 0 is extended by 128ms and then signal is inactive	Low

8. Port Function

8.1 Features

- Number of I/O ports: 96
- Can function alternately as the I/O pins of other peripheral functions.
- Input or output can be specified by bit unit.

Cautions 1. Switching from a signal for a peripheral module that is multiplexed with a port pin to port mode by changing the PMCn register setting might lead to a spike, depending on the state of the pin at the time.
The following general countermeasure for spikes should therefore be implemented in software.
- **Switch the pin function while the peripheral function is stopped.**
- **If the multiplexed pin function in use is an interrupt signal, clear the interrupt request flag and then remove masking of the interrupt.**
- **Only switch the mode after the output value is fixed.**

2. Do not externally apply an intermediate voltage to input buffers because these buffers do not implement through-current countermeasures.

8.2 Port Configuration

The R-IN32M3-EC incorporates eight 3-state I/O ports and four real-time control ports. Input or output mode can be specified for ports in 1-bit units. The basic structure of ports is the 8-bit unit, but ports 0 to 3 can also be grouped to enable reading and writing in 32-bit units. The real-time port pins (RP00 to RP37) can be used for input and output in synchronization with interrupt signals.

Each port has the registers shown below, which are used to make the I/O settings and to select and specify the multiplexed functions of the port pins. Figure 8.1 shows the basic circuit configuration of port registers and port pin.

Register Name	Application and Operation	
	Read	Write
Port registers (Pn, RPm)	Used to read the value of the output latch.	Used to set a value to the output latch.
Port mode registers (PMn, RPMm)	Used to read whether the port is in input or output mode.	Used to set the port to input or output mode.
Port mode control registers (PMCn, RPMCm)	Used to read whether the port pins are selected as port pins or as multiplexed function pins.	Used to select whether the port pins are used as port pins or as multiplexed function pins.
Port function control registers (PFCn, RPFCm)	Used to read which function is selected for the multiplexed pin.	Used to select the function of the multiplexed pin.
Port function control expansion registers (PFCEn, RPFCEm)		
Port pin input registers (PINn, RPINm)	Used to read the input level of the port pin.	Cannot be written.

Caution: Operation is not guaranteed if an unsupported function is allocated to the multiplexed pin. For example, if multiplexed function 4 is allocated to the P00 pin, which does not support multiplexed function 4, operation does not proceed correctly. For the allocation of multiplexed pins, see section 8.4, List of Selectable Multiplexed Functions.

Remark: n = 0 to 7, m = 0 to 3

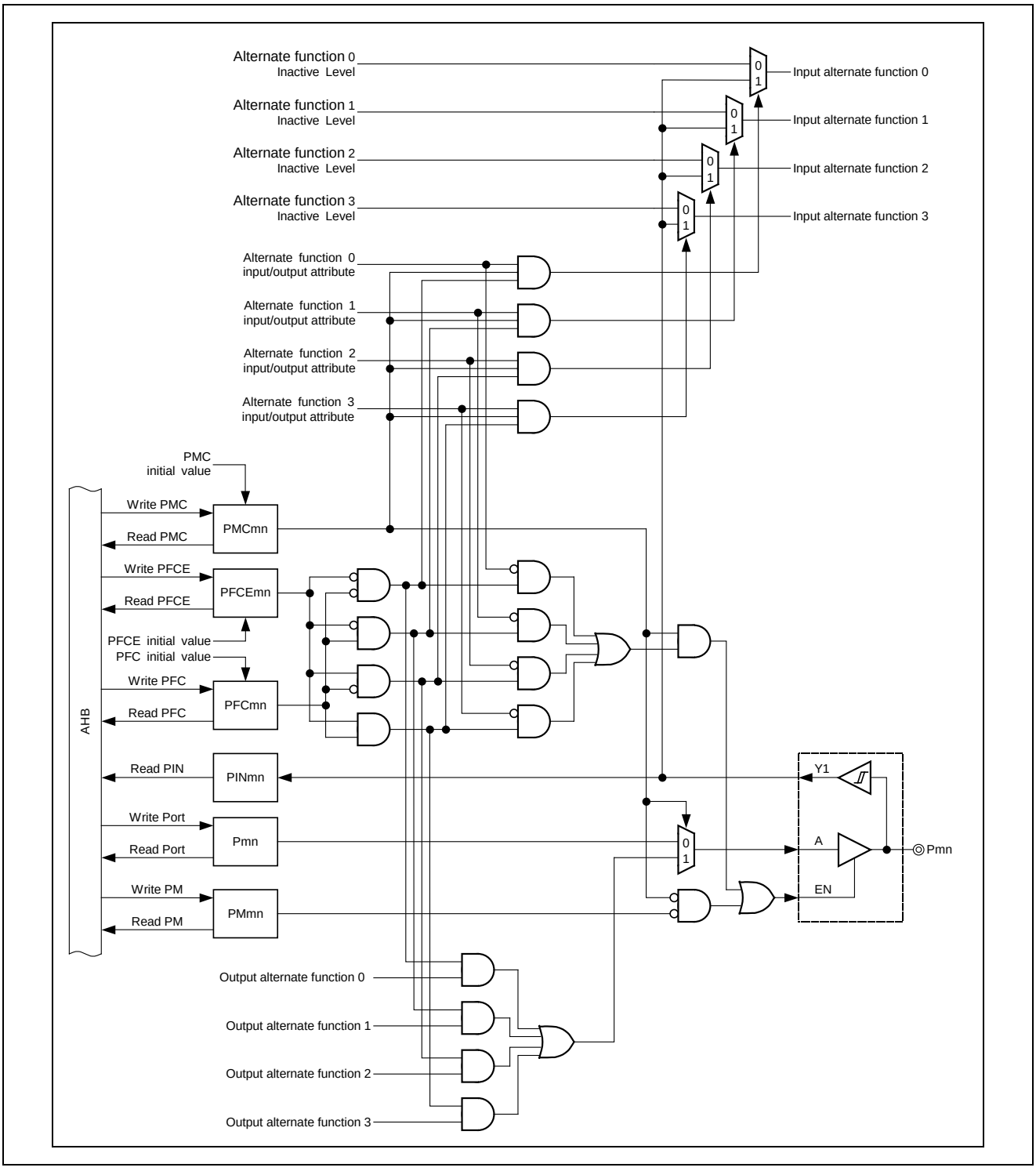


Figure 8.1 Basic Circuit Configuration of Ports

8.3 List of Registers

(1/6)

Register Name	Symbol	Address
Port register 0 (8 bits)	P0B	400A 3000H
Port register 1 (8 bits)	P1B	400A 3001H
Port register 2 (8 bits)	P2B	400A 3002H
Port register 3 (8 bits)	P3B	400A 3003H
Port register 4 (8 bits)	P4B	400A 3004H
Port register 5 (8 bits)	P5B	400A 3005H
Port register 6 (8 bits)	P6B	400A 3006H
Port register 7 (8 bits)	P7B	400A 3007H
Port register 0 (16 bits)	P0H	400A 3000H
Port register 2 (16 bits)	P2H	400A 3002H
Port register 4 (16 bits)	P4H	400A 3004H
Port register 6 (16 bits)	P6H	400A 3006H
Port register 0 (32 bits)	P0W	400A 3000H
Port register 4 (32 bits)	P4W	400A 3004H
Port mode register 0 (8 bits)	PM0B	400A 3010H
Port mode register 1 (8 bits)	PM1B	400A 3011H
Port mode register 2 (8 bits)	PM2B	400A 3012H
Port mode register 3 (8 bits)	PM3B	400A 3013H
Port mode register 4 (8 bits)	PM4B	400A 3014H
Port mode register 5 (8 bits)	PM5B	400A 3015H
Port mode register 6 (8 bits)	PM6B	400A 3016H
Port mode register 7 (8 bits)	PM7B	400A 3017H
Port mode register 0 (16 bits)	PM0H	400A 3010H
Port mode register 2 (16 bits)	PM2H	400A 3012H
Port mode register 4 (16 bits)	PM4H	400A 3014H
Port mode register 6 (16 bits)	PM6H	400A 3016H
Port mode register 0 (32 bits)	PM0W	400A 3010H
Port mode register 4 (32 bits)	PM4W	400A 3014H

(2/6)

Register Name	Symbol	Address
Port mode control register 0 (8 bits)	PMC0B	400A 3020H
Port mode control register 1 (8 bits)	PMC1B	400A 3021H
Port mode control register 2 (8 bits)	PMC2B	400A 3022H
Port mode control register 3 (8 bits)	PMC3B	400A 3023H
Port mode control register 4 (8 bits)	PMC4B	400A 3024H
Port mode control register 5 (8 bits)	PMC5B	400A 3025H
Port mode control register 6 (8 bits)	PMC6B	400A 3026H
Port mode control register 7 (8 bits)	PMC7B	400A 3027H
Port mode control register 0 (16 bits)	PMC0H	400A 3020H
Port mode control register 2 (16 bits)	PMC2H	400A 3022H
Port mode control register 4 (16 bits)	PMC4H	400A 3024H
Port mode control register 6 (16 bits)	PMC6H	400A 3026H
Port mode control register 0 (32 bits)	PMC0W	400A 3020H
Port mode control register 4 (32 bits)	PMC4W	400A 3024H
Port function control register 0 (8 bits)	PFC0B	400A 3030H
Port function control register 1 (8 bits)	PFC1B	400A 3031H
Port function control register 2 (8 bits)	PFC2B	400A 3032H
Port function control register 3 (8 bits)	PFC3B	400A 3033H
Port function control register 4 (8 bits)	PFC4B	400A 3034H
Port function control register 5 (8 bits)	PFC5B	400A 3035H
Port function control register 6 (8 bits)	PFC6B	400A 3036H
Port function control register 7 (8 bits)	PFC7B	400A 3037H
Port function control register 0 (16 bits)	PFC0H	400A 3030H
Port function control register 2 (16 bits)	PFC2H	400A 3032H
Port function control register 4 (16 bits)	PFC4H	400A 3034H
Port function control register 6 (16 bits)	PFC6H	400A 3036H
Port function control register 0 (32 bits)	PFC0W	400A 3030H
Port function control register 4 (32 bits)	PFC4W	400A 3034H

(3/6)

Register Name	Symbol	Address
Port function control expansion register 0 (8 bits)	PFCE0B	400A 3040H
Port function control expansion register 1 (8 bits)	PFCE1B	400A 3041H
Port function control expansion register 2 (8 bits)	PFCE2B	400A 3042H
Port function control expansion register 3 (8 bits)	PFCE3B	400A 3043H
Port function control expansion register 4 (8 bits)	PFCE4B	400A 3044H
Port function control expansion register 5 (8 bits)	PFCE5B	400A 3045H
Port function control expansion register 6 (8 bits)	PFCE6B	400A 3046H
Port function control expansion register 7 (8 bits)	PFCE7B	400A 3047H
Port function control expansion register 0 (16 bits)	PFCE0H	400A 3040H
Port function control expansion register 2 (16 bits)	PFCE2H	400A 3042H
Port function control expansion register 4 (16 bits)	PFCE4H	400A 3044H
Port function control expansion register 6 (16 bits)	PFCE6H	400A 3046H
Port function control expansion register 0 (32 bits)	PFCE0W	400A 3040H
Port function control expansion register 4 (32 bits)	PFCE4W	400A 3044H
Port pin input register 0 (8 bits)	PIN0B	400A 3050H
Port pin input register 1 (8 bits)	PIN1B	400A 3051H
Port pin input register 2 (8 bits)	PIN2B	400A 3052H
Port pin input register 3 (8 bits)	PIN3B	400A 3053H
Port pin input register 4 (8 bits)	PIN4B	400A 3054H
Port pin input register 5 (8 bits)	PIN5B	400A 3055H
Port pin input register 6 (8 bits)	PIN6B	400A 3056H
Port pin input register 7 (8 bits)	PIN7B	400A 3057H
Port pin input register 0 (16 bits)	PIN0H	400A 3050H
Port pin input register 2 (16 bits)	PIN2H	400A 3052H
Port pin input register 4 (16 bits)	PIN4H	400A 3054H
Port pin input register 6 (16 bits)	PIN6H	400A 3056H
Port pin input register 0 (32 bits)	PIN0W	400A 3050H
Port pin input register 4 (32 bits)	PIN4W	400A 3054H

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Register Name	Symbol	Address
RT port register 0 (8 bits)	RP0B	400A 3400H
RT port register 1 (8 bits)	RP1B	400A 3401H
RT port register 2 (8 bits)	RP2B	400A 3402H
RT port register 3 (8 bits)	RP3B	400A 3403H
RT port register 0 (16 bits)	RP0H	400A 3400H
RT port register 2 (16 bits)	RP2H	400A 3402H
RT port register 0 (32 bits)	RP0W	400A 3400H
RT port mode register 0 (8 bits)	RPM0B	400A 3410H
RT port mode register 1 (8 bits)	RPM1B	400A 3411H
RT port mode register 2 (8 bits)	RPM2B	400A 3412H
RT port mode register 3 (8 bits)	RPM3B	400A 3413H
RT port mode register 0 (16 bits)	RPM0H	400A 3410H
RT port mode register 2 (16 bits)	RPM2H	400A 3412H
RT port mode register 0 (32 bits)	RPM0W	400A 3410H
RT port mode control register 0 (8 bits)	RPMC0B	400A 3420H
RT port mode control register 1 (8 bits)	RPMC1B	400A 3421H
RT port mode control register 2 (8 bits)	RPMC2B	400A 3422H
RT port mode control register 3 (8 bits)	RPMC3B	400A 3423H
RT port mode control register 0 (16 bits)	RPMC0H	400A 3420H
RT port mode control register 2 (16 bits)	RPMC2H	400A 3422H
RT port mode control register 0 (32 bits)	RPMC0W	400A 3420H
RT port function control register 0 (8 bits)	RPFC0B	400A 3430H
RT port function control register 1 (8 bits)	RPFC1B	400A 3431H
RT port function control register 2 (8 bits)	RPFC2B	400A 3432H
RT port function control register 3 (8 bits)	RPFC3B	400A 3433H
RT port function control register 0 (16 bits)	RPFC0H	400A 3430H
RT port function control register 2 (16 bits)	RPFC2H	400A 3432H
RT port function control register 0 (32 bits)	RPFC0W	400A 3430H

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Register Name	Symbol	Address
RT port function control expansion register 0 (8 bits)	RPFCE0B	400A 3440H
RT port function control expansion register 1 (8 bits)	RPFCE1B	400A 3441H
RT port function control expansion register 2 (8 bits)	RPFCE2B	400A 3442H
RT port function control expansion register 3 (8 bits)	RPFCE3B	400A 3443H
RT port function control expansion register 0 (16 bits)	RPFCE0H	400A 3440H
RT port function control expansion register 2 (16 bits)	RPFCE2H	400A 3442H
RT port function control expansion register 0 (32 bits)	RPFCE0W	400A 3440H
RT port pin input register 0 (8 bits)	RPIN0B	400A 3450H
RT port pin input register 1 (8 bits)	RPIN1B	400A 3451H
RT port pin input register 2 (8 bits)	RPIN2B	400A 3452H
RT port pin input register 3 (8 bits)	RPIN3B	400A 3453H
RT port pin input register 0 (16 bits)	RPIN0H	400A 3450H
RT port pin input register 2 (16 bits)	RPIN2H	400A 3452H
RT port pin input register 0 (32 bits)	RPIN0W	400A 3450H

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Register Name	Symbol	Address
Buffer function change register P1L	DRCTLP1L	4001 0228H
Buffer function change register P1H	DRCTLP1H	4001 022CH
Buffer function change register P3L	DRCTLP3L	4001 0238H
Buffer function change register P3H	DRCTLP3H	4001 023CH
Buffer function change register P4L	DRCTLP4L	4001 0240H
Buffer function change register P4H	DRCTLP4H	4001 0244H
Buffer function change register P5L	DRCTLP5L	4001 0248H
Buffer function change register P5H	DRCTLP5H	4001 024CH
Buffer function change register RP0L	DRCTLRP0L	4001 0260H
Buffer function change register RP0H	DRCTLRP0H	4001 0264H
Buffer function change register RP1L	DRCTLRP1L	4001 0268H
Buffer function change register RP1H	DRCTLRP1H	4001 026CH
Buffer function change register RP2L	DRCTLRP2L	4001 0270H
Buffer function change register RP2H	DRCTLRP2H	4001 0274H
Buffer function change register RP3L	DRCTLRP3L	4001 0278H
Buffer function change register RP3H	DRCTLRP3H	4001 027CH

8.3.1 Port Registers (P, RP)

The R-IN32M3-EC incorporates twelve 3-state I/O ports. Input or output can be specified in 1-bit units. The port registers are used for writing the output levels for output port pins. When read, the value of the given port register is read. The PIN and RPIN registers are used to read the levels on input pins.

	7	6	5	4	3	2	1	0	Address	Initial Value
P0B	P07	P06	P05	P04	P03	P02	P01	P00	400A 3000H	00H
P1B	P17	P16	P15	P14	P13	P12	P11	P10	400A 3001H	00H
P2B	P27	P26	P25	P24	P23	P22	P21	P20	400A 3002H	00H
P3B	P37	P36	P35	P34	P33	P32	P31	P30	400A 3003H	00H
P4B	P47	P46	P45	P44	P43	P42	P41	P40	400A 3004H	00H
P5B	P57	P56	P55	P54	P53	P52	P51	P50	400A 3005H	00H
P6B	P67	P66	P65	P64	P63	P62	P61	P60	400A 3006H	00H
P7B	P77	P76	P75	P74	P73	P72	P71	P70	400A 3007H	00H
RP0B	RP07	RP06	RP05	RP04	RP03	RP02	RP01	RP00	400A 3400H	00H
RP1B	RP17	RP16	RP15	RP14	RP13	RP12	RP11	RP10	400A 3401H	00H
RP2B	RP27	RP26	RP25	RP24	RP23	RP22	RP21	RP20	400A 3402H	00H
RP3B	RP37	RP36	RP35	RP34	RP33	RP32	RP31	RP30	400A 3403H	00H

Bit Position	Bit Name	Description
7 to 0	Pmn/RPln	These bits set the value of the output latch when the port is used in output mode. If read, the value of the output latch is read.

Figure 8.2 Port Registers (in 8-Bit Notation)

Remark: l = 0 to 3, m = 0 to 7, n = 0 to 7

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
P0H	P17	P16	P15	P14	P13	P12	P11	P10	P07	P06	P05	P04	P03	P02	P01	P00	400A 3000H
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Initial Value 0000H

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
P2H	P37	P36	P35	P34	P33	P32	P31	P30	P27	P26	P25	P24	P23	P22	P21	P20	400A 3002H
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Initial Value 0000H

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
P4H	P57	P56	P55	P54	P53	P52	P51	P50	P47	P46	P45	P44	P43	P42	P41	P40	400A 3004H
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Initial Value 0000H

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
P6H	P77	P76	P75	P74	P73	P72	P71	P70	P67	P66	P65	P64	P63	P62	P61	P60	400A 3006H
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Initial Value 0000H

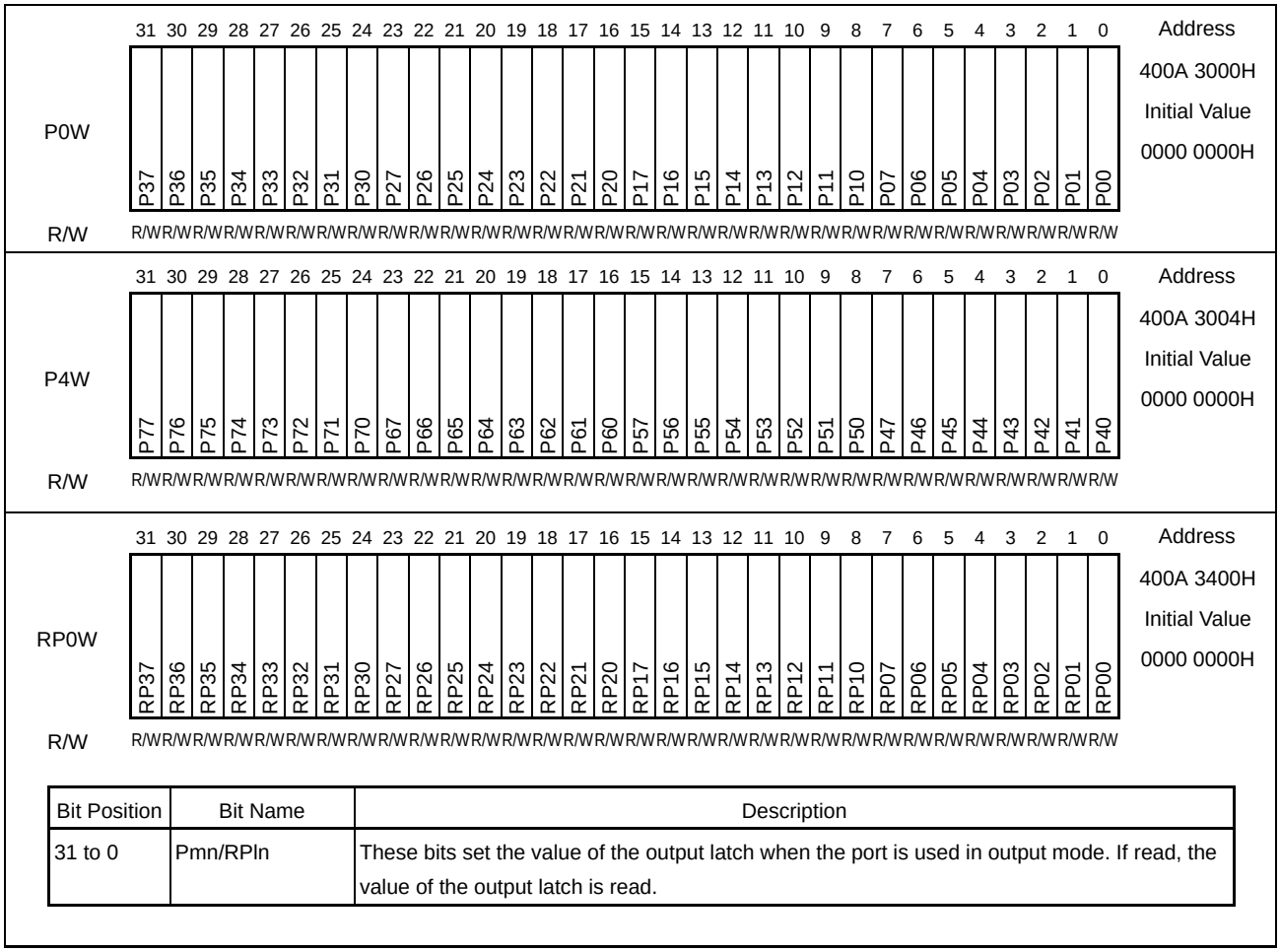
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
RP0H	RP17	RP16	RP15	RP14	RP13	RP12	RP11	RP10	RP07	RP06	RP05	RP04	RP03	RP02	RP01	RP00	400A 3400H
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Initial Value 0000H

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
RP2H	RP37	RP36	RP35	RP34	RP33	RP32	RP31	RP30	RP27	RP26	RP25	RP24	RP23	RP22	RP21	RP20	400A 3402H
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Initial Value 0000H

Bit Position	Bit Name	Description
15 to 0	Pmn/RPln	These bits set the value of the output latch when the port is used in output mode. If read, the value of the output latch is read.

Figure 8.3 Port Registers (in 16-Bit Notation)

Remark: l = 0 to 3, m = 0 to 7, n = 0 to 7



Bit Position	Bit Name	Description
31 to 0	Pmn/RPln	These bits set the value of the output latch when the port is used in output mode. If read, the value of the output latch is read.

Figure 8.4 Port Registers (in 32-Bit Notation)

Remark: l = 0 to 3, m = 0 to 7, n = 0 to 7

8.3.2 Port Mode Registers (PM, RPM)

These registers are used to set a port to input or output mode.

	7	6	5	4	3	2	1	0	Address	Initial Value
PM0B	PM07	PM06	PM05	PM04	PM03	PM02	PM01	PM00	400A 3010H	FFH
PM1B	PM17	PM16	PM15	PM14	PM13	PM12	PM11	PM10	400A 3011H	FFH
PM2B	PM27	PM26	PM25	PM24	PM23	PM22	PM21	PM20	400A 3012H	FFH
PM3B	PM37	PM36	PM35	PM34	PM33	PM32	PM31	PM30	400A 3013H	FFH
PM4B	PM47	PM46	PM45	PM44	PM43	PM42	PM41	PM40	400A 3014H	FFH
PM5B	PM57	PM56	PM55	PM54	PM53	PM52	PM51	PM50	400A 3015H	FFH
PM6B	PM67	PM66	PM65	PM64	PM63	PM62	PM61	PM60	400A 3016H	FFH
PM7B	PM77	PM76	PM75	PM74	PM73	PM72	PM71	PM70	400A 3017H	FFH
RPM0B	RPM07	RPM06	RPM05	RPM04	RPM03	RPM02	RPM01	RPM00	400A 3410H	FFH
RPM1B	RPM17	RPM16	RPM15	RPM14	RPM13	RPM12	RPM11	RPM10	400A 3411H	FFH
RPM2B	RPM27	RPM26	RPM25	RPM24	RPM23	RPM22	RPM21	RPM20	400A 3412H	FFH
RPM3B	RPM37	RPM36	RPM35	RPM34	RPM33	RPM32	RPM31	RPM30	400A 3413H	FFH

Bit Position	Bit Name	Description
7 to 0	PMmn/ RPMln	These bits set the port to input or output mode. 0: Output mode (output buffer is on) 1: Input mode (output buffer is off) (initial value)

Figure 8.5 Port Mode Registers (in 8-Bit Notation):

Remark: l = 0 to 3, m = 0 to 7, n = 0 to 7

PM0H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
PM17	PM16	PM15	PM14	PM13	PM12	PM11	PM10	PM07	PM06	PM05	PM04	PM03	PM02	PM01	PM00	400A 3010H
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Initial Value
																FFFFH

PM2H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
PM37	PM36	PM35	PM34	PM33	PM32	PM31	PM30	PM27	PM26	PM25	PM24	PM23	PM22	PM21	PM20	400A 3012H
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Initial Value
																FFFFH

PM4H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
PM57	PM56	PM55	PM54	PM53	PM52	PM51	PM50	PM47	PM46	PM45	PM44	PM43	PM42	PM41	PM40	400A 3014H
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Initial Value
																FFFFH

PM6H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
PM77	PM76	PM75	PM74	PM73	PM72	PM71	PM70	PM67	PM66	PM65	PM64	PM63	PM62	PM61	PM60	400A 3016H
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Initial Value
																FFFFH

RPM0H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
RPM 17	RPM 16	RPM 15	RPM 14	RPM 13	RPM 12	RPM 11	RPM 10	RPM 07	RPM 06	RPM 05	RPM 04	RPM 03	RPM 02	RPM 01	RPM 00	400A 3410H
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Initial Value
																FFFFH

RPM2H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
RPM 37	RPM 36	RPM 35	RPM 34	RPM 33	RPM 32	RPM 31	RPM 30	RPM 27	RPM 26	RPM 25	RPM 24	RPM 23	RPM 22	RPM 21	RPM 20	400A 3412H
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Initial Value
																FFFFH

Bit Position	Bit Name	Description
15 to 0	PMmn/ RPMln	These bits set the port to input or output mode. 0: Output mode (output buffer is on) 1: Input mode (output buffer is off) (initial value)

Figure 8.6 Port Mode Registers (in 16-Bit Notation)

Remark: l = 0 to 3, m = 0 to 7, n = 0 to 7

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
PM0W	PM37	PM36	PM35	PM34	PM33	PM32	PM31	PM30	PM27	PM26	PM25	PM24	PM23	PM22	PM21	PM20	PM17	PM16	PM15	PM14	PM13	PM12	PM11	PM10	PM07	PM06	PM05	PM04	PM03	PM02	PM01	PM00	400A 3010H
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Initial Value: FFFF FFFFH

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
PM4W	PM77	PM76	PM75	PM74	PM73	PM72	PM71	PM70	PM67	PM66	PM65	PM64	PM63	PM62	PM61	PM60	PM57	PM56	PM55	PM54	PM53	PM52	PM51	PM50	PM47	PM46	PM45	PM44	PM43	PM42	PM41	PM40	400A 3014H
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Initial Value: FFFF FFFFH

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
RPM0W	RPM37	RPM36	RPM35	RPM34	RPM33	RPM32	RPM31	RPM30	RPM27	RPM26	RPM25	RPM24	RPM23	RPM22	RPM21	RPM20	RPM17	RPM16	RPM15	RPM14	RPM13	RPM12	RPM11	RPM10	RPM07	RPM06	RPM05	RPM04	RPM03	RPM02	RPM01	RPM00	400A 3410H
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Initial Value: FFFF FFFFH

Bit Position	Bit Name	Description
31 to 0	PMmn/RPMln	These bits set the port to input or output mode. 0: Output mode (output buffer is on) 1: Input mode (output buffer is off) (initial value)

Figure 8.7 Port Mode Registers (in 32-Bit Notation)

Remark: l = 0 to 3, m = 0 to 7, n = 0 to 7

8.3.3 Port Mode Control Register (PMC, RPMC)

These registers are used to select whether to use a port as a port or for its alternate function.

	7	6	5	4	3	2	1	0	Address	Initial Value
PMC0B	PMC07	PMC06	PMC05	PMC04	PMC03	PMC02	PMC01	PMC00	400A 3020H	00H
PMC1B	PMC17	PMC16	PMC15	PMC14	PMC13	PMC12	PMC11	PMC10	400A 3021H	00H Note 1
PMC2B	PMC27	PMC26	PMC25	PMC24	PMC23	PMC22	PMC21	PMC20	400A 3022H	00H Note 1
PMC3B	PMC37	PMC36	PMC35	PMC34	PMC33	PMC32	PMC31	PMC30	400A 3023H	00H Note 1
PMC4B	PMC47	PMC46	PMC45	PMC44	PMC43	PMC42	PMC41	PMC40	400A 3024H	00H Note 1
PMC5B	PMC57	PMC56	PMC55	PMC54	PMC53	PMC52	PMC51	PMC50	400A 3025H	00H Note 1
PMC6B	PMC67	PMC66	PMC65	PMC64	PMC63	PMC62	PMC61	PMC60	400A 3026H	00H Note 1
PMC7B	PMC77	PMC76	PMC75	PMC74	PMC73	PMC72	PMC71	PMC70	400A 3027H	00H
RPMC0B	RPMC07	RPMC06	RPMC05	RPMC04	RPMC03	RPMC02	RPMC01	RPMC00	400A 3420H	00H Note 1
RPMC1B	RPMC17	RPMC16	RPMC15	RPMC14	RPMC13	RPMC12	RPMC11	RPMC10	400A 3421H	00H Note 1
RPMC2B	RPMC27	RPMC26	RPMC25	RPMC24	RPMC23	RPMC22	RPMC21	RPMC20	400A 3422H	00H Note 1
RPMC3B	RPMC37	RPMC36	RPMC35	RPMC34	RPMC33	RPMC32	RPMC31	RPMC30	400A 3423H	00H Note 1

Bit Position	Bit Name	Description
7 to 0	PMCmn/ RPMCln	These bits select whether the port pins are used as port pins or as multiplexed function pins. Note 2 0: Port mode (the inactive level is input for multiplexed input pin functions.) 1: Multiplexed function (control mode)

Figure 8.8 Port Mode Control Registers (in 8-Bit Notation)

Notes 1. The initial value depends on the state of the pins. For details, see section 2.2, Pin States.

2. The multiplexed function is selected by the port mode control register, port function control register, and the port function control expansion register. For details, see section 8.4, List of Selectable Multiplexed Functions.

Remark: l = 0 to 3, m = 0 to 7, n = 0 to 7

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
PMC0H	PMC17	PMC16	PMC15	PMC14	PMC13	PMC12	PMC11	PMC10	PMC07	PMC06	PMC05	PMC04	PMC03	PMC02	PMC01	PMC00	400A 3020H
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Initial Value
																	0000H Note 1

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
PMC2H	PMC37	PMC36	PMC35	PMC34	PMC33	PMC32	PMC31	PMC30	PMC27	PMC26	PMC25	PMC24	PMC23	PMC22	PMC21	PMC20	400A 3022H
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Initial Value
																	0000H Note 1

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
PMC4H	PMC57	PMC56	PMC55	PMC54	PMC53	PMC52	PMC51	PMC50	PMC47	PMC46	PMC45	PMC44	PMC43	PMC42	PMC41	PMC40	400A 3024H
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Initial Value
																	0000H Note 1

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
PMC6H	PMC77	PMC76	PMC75	PMC74	PMC73	PMC72	PMC71	PMC70	PMC67	PMC66	PMC65	PMC64	PMC63	PMC62	PMC61	PMC60	400A 3026H
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Initial Value
																	0000H Note 1

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
RPMC0H	RPMC17	RPMC16	RPMC15	RPMC14	RPMC13	RPMC12	RPMC11	RPMC10	RPMC07	RPMC06	RPMC05	RPMC04	RPMC03	RPMC02	RPMC01	RPMC00	400A 3420H
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Initial Value
																	0000H Note 1

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
RPMC2H	RPMC37	RPMC36	RPMC35	RPMC34	RPMC33	RPMC32	RPMC31	RPMC30	RPMC27	RPMC26	RPMC25	RPMC24	RPMC23	RPMC22	RPMC21	RPMC20	400A 3422H
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Initial Value
																	0000H Note 1

Bit Position	Bit Name	Description
15 to 0	PMCmn/ RPMCln	These bits select whether the port pins are used as port pins or as multiplexed function pins. Note 2 0: Port mode (the inactive level is input for multiplexed input pin functions.) 1: Multiplexed function (control mode)

Figure 8.9 Port Mode Control Registers (in 16-Bit Notation)

Notes 1. The initial value depends on the state of the pins. For details, see section 2.2, Pin States.

2. The multiplexed function is selected by the port mode control register, port function control register, and the port function control expansion register. For details, see section 8.4, List of Selectable Multiplexed Functions.

Remark: l = 0 to 3, m = 0 to 7, n = 0 to 7

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
PMC0W	PMC37	PMC36	PMC35	PMC34	PMC33	PMC32	PMC31	PMC30	PMC27	PMC26	PMC25	PMC24	PMC23	PMC22	PMC21	PMC20	PMC17	PMC16	PMC15	PMC14	PMC13	PMC12	PMC11	PMC10	PMC07	PMC06	PMC05	PMC04	PMC03	PMC02	PMC01	PMC00	400A 3020H Initial Value 0000 0000H Note 1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
PMC4W	PMC77	PMC76	PMC75	PMC74	PMC73	PMC72	PMC71	PMC70	PMC67	PMC66	PMC65	PMC64	PMC63	PMC62	PMC61	PMC60	PMC57	PMC56	PMC55	PMC54	PMC53	PMC52	PMC51	PMC50	PMC47	PMC46	PMC45	PMC44	PMC43	PMC42	PMC41	PMC40	400A 3024H Initial Value 0000 0000H Note 1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
RPMC0W	RPMC37	RPMC36	RPMC35	RPMC34	RPMC33	RPMC32	RPMC31	RPMC30	RPMC27	RPMC26	RPMC25	RPMC24	RPMC23	RPMC22	RPMC21	RPMC20	RPMC17	RPMC16	RPMC15	RPMC14	RPMC13	RPMC12	RPMC11	RPMC10	RPMC07	RPMC06	RPMC05	RPMC04	RPMC03	RPMC02	RPMC01	RPMC00	400A 3420H Initial Value 0000 0000H Note 1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

Bit Position	Bit Name	Description
31 to 0	PMCmn/RPMCln	These bits select whether the port pins are used as port pins or as multiplexed function pins. Note 2 0: Port mode (the inactive level is input for multiplexed input pin functions.) 1: Multiplexed function (control mode)

Figure 8.10 Port Mode Control Registers (in 32-Bit Notation)

Notes 1. The initial value depends on the state of the pins. For details, see section 2.2, Pin States.

2. The multiplexed function is selected by the port mode control register, port function control register, and the port function control expansion register. For details, see section 8.4, List of Selectable Multiplexed Functions.

Remark: l = 0 to 3, m = 0 to 7, n = 0 to 7

8.3.4 Port Function Control Registers (PFC, RPFC)

These registers are used to specify which multiplexed function is to be used. These registers can be set in 1-bit units.

	7	6	5	4	3	2	1	0	Address	Initial Value
PFC0B	1	PFC06	PFC05	PFC04	PFC03	PFC02	PFC01	PFC00	400A 3030H	00H
PFC1B	0	0	0	0	0	PFC12	PFC11	PFC10	400A 3031H	00H
PFC2B	PFC27	PFC26	0	PFC24	PFC23	PFC22	0	0	400A 3032H	00H Note 1
PFC3B	PFC37	PFC36	PFC35	PFC34	PFC33	PFC32	0	0	400A 3033H	00H Note 1
PFC4B	PFC47	PFC46	PFC45	PFC44	PFC43	PFC42	PFC41	PFC40	400A 3034H	00H Note 1
PFC5B	PFC57	PFC56	0	PFC54	PFC53	PFC52	0	0	400A 3035H	00H Note 1
PFC6B	0	0	0	0	0	0	0	0	400A 3036H	00H Note 1
PFC7B	PFC77	PFC76	0	PFC74	PFC73	PFC72	0	PFC70	400A 3037H	00H
RPFC0B	RPFC07	RPFC06	0	RPFC04	0	RPFC02	RPFC01	RPFC00	400A 3430H	00H
RPFC1B	0	0	0	0	0	0	0	0	400A 3431H	00H
RPFC2B	RPFC27	RPFC26	RPFC25	RPFC24	0	0	0	RPFC20	400A 3432H	00H
RPFC3B	0	0	0	0	0	0	0	0	400A 3433H	00H

Bit Position	Bit Name	Description
7 to 0	PFCmn/ RPFCmn	These bits select the multiplexed function. Note 2 0: Multiplexed function 1 or multiplexed function 3 1: Multiplexed function 2 or multiplexed function 4

Figure 8.11 Port Function Control Registers (in 8-Bit Notation)

Notes 1. The initial value depends on the state of the pins. For details, see section 2.2, Pin States.

2. The multiplexed function is selected by the port mode control register, port function control register, and the port function control expansion register. For details, see section 8.4, List of Selectable Multiplexed Functions.

Remark: l = 0 to 3, m = 0 to 7, n = 0 to 7

PFC0H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
0	0	0	0	0	PFC12	PFC11	PFC10	1	PFC06	PFC05	PFC04	PFC03	PFC02	PFC01	PFC00	400A 3030H
0	0	0	0	0	R/W	R/W	R/W	1	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Initial Value 0000H

PFC2H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
PFC37	PFC36	PFC35	PFC34	PFC33	PFC32	0	0	PFC27	PFC26	PFC25	PFC24	PFC23	PFC22	0	0	400A 3032H
R/W	R/W	R/W	R/W	R/W	R/W	0	0	R/W	R/W	R/W	R/W	R/W	R/W	0	0	Initial Value 0000H Note 1

PFC4H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
PFC57	PFC56	0	PFC54	PFC53	PFC52	0	0	PFC47	PFC46	PFC45	PFC44	PFC43	PFC42	PFC41	PFC40	400A 3034H
R/W	R/W	0	R/W	R/W	R/W	0	0	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Initial Value 0000H Note 1

PFC6H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
PFC77	PFC76	0	PFC74	PFC73	PFC72	0	PFC70	0	0	0	0	0	0	0	0	400A 3036H
R/W	R/W	0	R/W	R/W	R/W	0	R/W	0	0	0	0	0	0	0	0	Initial Value 0000H Note 1

RPFC0H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
0	0	0	0	0	0	0	0	RPFC07	RPFC06	0	RPFC04	0	RPFC02	RPFC01	RPFC00	400A 3430H
0	0	0	0	0	0	0	0	R/W	R/W	0	R/W	0	R/W	R/W	R/W	Initial Value 0000H

RPFC2H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
0	0	0	0	0	0	0	0	RPFC27	RPFC26	RPFC25	RPFC24	0	0	0	RPFC20	400A 3432H
0	0	0	0	0	0	0	0	R/W	R/W	R/W	R/W	0	0	0	R/W	Initial Value 0000H

Bit Position	Bit Name	Description
15 to 0	PFCmn/ RPFCln	These bits select the multiplexed function. Note 2 0: Multiplexed function 1 or multiplexed function 3 1: Multiplexed function 2 or multiplexed function 4

Figure 8.12 Port Function Control Registers (in 16-Bit Notation)

Notes 1. The initial value depends on the state of the pins. For details, see section 2.2, Pin States.

2. The multiplexed function is selected by the port mode control register, port function control register, and the port function control expansion register. For details, see section 8.4, List of Selectable Multiplexed Functions.

Remark: l = 0 to 3, m = 0 to 7, n = 0 to 7

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
PFC0W	PFC37	PFC36	PFC35	PFC34	PFC33	PFC32	0	0	PFC27	PFC26	0	PFC24	PFC23	PFC22	0	0	0	0	0	0	0	PFC12	PFC11	PFC10	1	PFC06	PFC05	PFC04	PFC03	PFC02	PFC01	PFC00	400A 3030H
R/W	R/W	R/W	R/W	R/W	R/W	R/W	0	0	R/W	R/W	0	R/W	R/W	R/W	0	0	0	0	0	0	0	R/W	R/W	R/W	1	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Initial Value
																																	0000 0000H[Note 1]

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
PFC4W	PFC77	PFC76	0	PFC74	PFC73	PFC72	0	PFC70	0	0	0	0	0	0	0	0	PFC57	PFC56	0	PFC54	PFC53	PFC52	0	0	PFC47	PFC46	PFC45	PFC44	PFC43	PFC42	PFC41	PFC40	400A 3034H
R/W	R/W	R/W	0	R/W	R/W	R/W	0	R/W	0	0	0	0	0	0	0	0	R/W	R/W	0	R/W	R/W	R/W	0	0	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Initial Value
																																	0000 0000H[Note 1]

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
RPFC0W	0	0	0	0	0	0	0	0	RPFC27	RPFC26	RPFC25	RPFC24	0	0	0	RPFC20	0	0	0	0	0	0	0	0	RPFC07	RPFC06	0	RPFC04	0	RPFC02	RPFC01	RPFC00	400A 3430H
R/W	0	0	0	0	0	0	0	0	R/W	R/W	R/W	R/W	0	0	0	R/W	0	0	0	0	0	0	0	0	R/W	R/W	0	R/W	0	R/W	R/W	R/W	Initial Value
																																	0000 0000H[Note 1]

Bit Position	Bit Name	Description
31 to 0	PFCmn/ RPFCln	These bits select the multiplexed function.[Note 2] 0: Multiplexed function 1 or multiplexed function 3 1: Multiplexed function 2 or multiplexed function 4

Figure 8.13 Port Function Control Registers (in 32-Bit Notation)

Notes 1. The initial value depends on the state of the pins. For details, see section 2.2, Pin States.

2. The multiplexed function is selected by the port mode control register, port function control register, and the port function control expansion register. For details, see section 8.4, List of Selectable Multiplexed Functions.

Remark: l = 0 to 3, m = 0 to 7, n = 0 to 7

8.3.5 Port Function Control Expansion Registers (PFCE, RPFCE)

These registers are used to specify which multiplexed extended function is to be used. These registers can be set in 1-bit units.

	7	6	5	4	3	2	1	0	Address	Initial Value
PFCE0B	PFCE07	PFCE06	PFCE05	PFCE04	PFCE03	PFCE02	0	0	400A 3040H	00H
PFCE1B	0	0	0	0	PFCE13	PFCE12	PFCE11	PFCE10	400A 3041H	00H
PFCE2B	0	PFCE26	PFCE25	PFCE24	PFCE23	PFCE22	PFCE21	PFCE20	400A 3042H	00H
PFCE3B	PFCE37	PFCE36	PFCE35	PFCE34	PFCE33	PFCE32	0	0	400A 3043H	00H Note 1
PFCE4B	0	0	0	0	0	PFCE42	0	0	400A 3044H	00H Note 1
PFCE5B	0	0	0	PFCE54	PFCE53	PFCE52	PFCE51	PFCE50	400A 3045H	00H Note 1
PFCE6B	0	0	PFCE65	PFCE64	PFCE63	PFCE62	0	0	400A 3046H	00H Note 1
PFCE7B	PFCE77	PFCE76	PFCE75	PFCE74	PFCE73	PFCE72	PFCE71	PFCE70	400A 3047H	00H
RPFCE0B	0	0	RPFCE05	RPFCE04	RPFCE03	RPFCE02	RPFCE01	RPFCE00	400A 3440H	00H Note 1
RPFCE1B	0	0	0	0	0	0	0	0	400A 3441H	00H Note 1
RPFCE2B	0	0	0	0	0	0	0	0	400A 3442H	00H Note 1
RPFCE3B	0	0	0	0	0	0	0	0	400A 3443H	00H Note 1

Bit Position	Bit Name	Description
7 to 0	PFCEmn/ RPFCEln	These bits select the multiplexed function. Note 2 0: Multiplexed function 1 or multiplexed function 2 1: Multiplexed function 3 or multiplexed function 4

Figure 8.14 Port Function Control Expansion Registers (in 8-Bit Notation)

Notes 1. The initial value depends on the state of the pins. For details, see section 2.2, Pin States.

2. The multiplexed function is selected by the port mode control register, port function control register, and the port function control expansion register. For details, see section 8.4, List of Selectable Multiplexed Functions.

Remark: l = 0 to 3, m = 0 to 7, n = 0 to 7

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
PFCE0H	0	0	0	0	PFCE13	PFCE12	PFCE11	PFCE10	PFCE07	PFCE06	PFCE05	PFCE04	PFCE03	PFCE02	0	0	400A 3040H
	0	0	0	0	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	0	0	Initial Value 0000H

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
PFCE2H	PFCE37	PFCE36	PFCE35	PFCE34	PFCE33	PFCE32	0	0	0	PFCE26	PFCE25	PFCE24	PFCE23	PFCE22	PFCE21	PFCE20	400A 3042H
	R/W	R/W	R/W	R/W	R/W	R/W	0	0	0	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Initial Value 0000H[Note 1]

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
PFCE4H	0	0	0	PFCE54	PFCE53	PFCE52	PFCE51	PFCE50	0	0	0	0	0	PFCE42	0	0	400A 3044H
	0	0	0	R/W	R/W	R/W	R/W	R/W	0	0	0	0	0	R/W	0	0	Initial Value 0000H[Note 1]

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
PFCE6H	PFCE77	PFCE76	PFCE75	PFCE74	PFCE73	PFCE72	PFCE71	PFCE70	0	0	PFCE65	PFCE64	PFCE63	PFCE62	0	0	400A 3046H
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	0	0	R/W	R/W	R/W	R/W	0	0	Initial Value 0000H[Note 1]

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
RPFCE0H	0	0	0	0	0	0	0	0	0	0	RPFCE05	RPFCE04	RPFCE03	RPFCE02	RPFCE01	RPFCE00	400A 3440H
	0	0	0	0	0	0	0	0	0	0	R/W	R/W	R/W	R/W	R/W	R/W	Initial Value 0000H[Note 1]

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
RPFCE2H	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	400A 3442H
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Initial Value 0000H[Note 1]

Bit Position	Bit Name	Description
15 to 0	PFCEmn/ RPFCEln	These bits select the multiplexed function. [Note 2] 0: Multiplexed function 1 or multiplexed function 2 1: Multiplexed function 3 or multiplexed function 4

Figure 8.15 Port Function Control Expansion Registers (in 16-Bit Notation)

Notes 1. The initial value depends on the state of the pins. For details, see section 2.2, Pin States.

2. The multiplexed function is selected by the port mode control register, port function control register, and the port function control expansion register. For details, see section 8.4, List of Selectable Multiplexed Functions.

Remark: l = 0 to 3, m = 0 to 7, n = 0 to 7

PFCE0W

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PFCE37	PFCE36	PFCE35	PFCE34	PFCE33	PFCE32	0	0	0	PFCE26	PFCE25	PFCE24	PFCE23	PFCE22	PFCE21	PFCE20	0	0	0	0	PFCE13	PFCE12	PFCE11	PFCE10	PFCE07	PFCE06	PFCE05	PFCE04	PFCE03	PFCE02	0	0
R/W	R/W	R/W	R/W	R/W	R/W	0	0	0	R/W	R/W	R/W	R/W	R/W	R/W	R/W	0	0	0	0	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	0	0

Address: 400A 3040H
Initial Value: 0000 0000H Note 1

PFCE4W

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PFCE77	PFCE76	PFCE75	PFCE74	PFCE73	PFCE72	PFCE71	PFCE70	0	0	PFCE65	PFCE64	PFCE63	PFCE62	0	0	0	0	0	PFCE54	PFCE53	PFCE52	PFCE51	PFCE50	0	0	0	0	0	PFCE42	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	0	0	R/W	R/W	R/W	R/W	0	0	0	0	0	R/W	R/W	R/W	R/W	R/W	0	0	0	0	0	R/W	0	0

Address: 400A 3044H
Initial Value: 0000 0000H Note 1

RPFCE0W

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	RPFCE05	RPFCE04	RPFCE03	RPFCE02	RPFCE01	RPFCE00
R/W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R/W	R/W	R/W	R/W	R/W	R/W

Address: 400A 3440H
Initial Value: 0000 0000H Note 1

Bit Position	Bit Name	Description
31 to 0	PFCEmn/ RPFCEln	These bits select the multiplexed function. Note 2 0: Multiplexed function 1 or multiplexed function 2 1: Multiplexed function 3 or multiplexed function 4

Figure 8.16 Port Function Control Expansion Registers (in 32-Bit Notation)

Notes 1. The initial value depends on the state of the pins. For details, see section 2.2, Pin States.

2. The multiplexed function is selected by the port mode control register, port function control register, and the port function control expansion register. For details, see section 8.4, List of Selectable Multiplexed Functions.

Remark: l = 0 to 3, m = 0 to 7, n = 0 to 7

8.3.6 Port Pin Input Registers (PIN, RPIN)

These are read-only registers for reading the input level of port pins.

	7	6	5	4	3	2	1	0	Address	Initial Value
PIN0B	PIN07	PIN06	PIN05	PIN04	PIN03	PIN02	PIN01	PIN00	400A 3050H	Pin Level
PIN1B	PIN17	PIN16	PIN15	PIN14	PIN13	PIN12	PIN11	PIN10	400A 3051H	Pin Level
PIN2B	PIN27	PIN26	PIN25	PIN24	PIN23	PIN22	PIN21	PIN20	400A 3052H	Pin Level
PIN3B	PIN37	PIN36	PIN35	PIN34	PIN33	PIN32	PIN31	PIN30	400A 3053H	Pin Level
PIN4B	PIN47	PIN46	PIN45	PIN44	PIN43	PIN42	PIN41	PIN40	400A 3054H	Pin Level
PIN5B	PIN57	PIN56	PIN55	PIN54	PIN53	PIN52	PIN51	PIN50	400A 3055H	Pin Level
PIN6B	PIN67	PIN66	PIN65	PIN64	PIN63	PIN62	PIN61	PIN60	400A 3056H	Pin Level
PIN7B	PIN77	PIN76	PIN75	PIN74	PIN73	PIN72	PIN71	PIN70	400A 3057H	Pin Level
RPIN0B	RPIN07	RPIN06	RPIN05	RPIN04	RPIN03	RPIN02	RPIN01	RPIN00	400A 3450H	Pin Level
RPIN1B	RPIN17	RPIN16	RPIN15	RPIN14	RPIN13	RPIN12	RPIN11	RPIN10	400A 3451H	Pin Level
RPIN2B	RPIN27	RPIN26	RPIN25	RPIN24	RPIN23	RPIN22	RPIN21	RPIN20	400A 3452H	Pin Level
RPIN3B	RPIN37	RPIN36	RPIN35	RPIN34	RPIN33	RPIN32	RPIN31	RPIN30	400A 3453H	Pin Level

Bit Position	Bit Name	Description
7 to 0	PINmn/ RPINln	Use to read the input level of the port pin.

Figure 8.17 Port Pin Input Registers (in 8-Bit Notation)

Remark: l = 0 to 3, m = 0 to 7, n = 0 to 7

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
PIN0H	PIN 17	PIN 16	PIN 15	PIN 14	PIN 13	PIN 12	PIN 11	PIN 10	PIN 07	PIN 06	PIN 05	PIN 04	PIN 03	PIN 02	PIN 01	PIN 00	Address: 400A 3050H
	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	Initial Value
																	Pin Level
PIN2H	PIN 37	PIN 36	PIN 35	PIN 34	PIN 33	PIN 32	PIN 31	PIN 30	PIN 27	PIN 26	PIN 25	PIN 24	PIN 23	PIN 22	PIN 21	PIN 20	Address: 400A 3052H
	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	Initial Value
																	Pin Level
PIN4H	PIN 57	PIN 56	PIN 55	PIN 54	PIN 53	PIN 52	PIN 51	PIN 50	PIN 47	PIN 46	PIN 45	PIN 44	PIN 43	PIN 42	PIN 41	PIN 40	Address: 400A 3054H
	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	Initial Value
																	Pin Level
PIN6H	PIN 77	PIN 76	PIN 75	PIN 74	PIN 73	PIN 72	PIN 71	PIN 70	PIN 67	PIN 66	PIN 65	PIN 64	PIN 63	PIN 62	PIN 61	PIN 60	Address: 400A 3056H
	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	Initial Value
																	Pin Level
RPIN0H	RPIN17	RPIN 16	RPIN 15	RPIN 14	RPIN 13	RPIN 12	RPIN 11	RPIN 10	RPIN 07	RPIN 06	RPIN 05	RPIN 04	RPIN 03	RPIN 02	RPIN 01	RPIN00	Address: 400A 3450H
	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	Initial Value
																	Pin Level
RPIN2H	RPIN37	RPIN 36	RPIN 35	RPIN 34	RPIN 33	RPIN 32	RPIN 31	RPIN 30	RPIN 27	RPIN 26	RPIN 25	RPIN 24	RPIN 23	RPIN 22	RPIN 21	RPIN20	Address: 400A 3452H
	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	Initial Value
																	Pin Level

Bit Position	Bit Name	Description
15 to 0	PINmn/ RPINln	These bits are for reading the input level of the port pins.

Figure 8.18 Port Pin Input Registers (in 16-Bit Notation)

Remark: l = 0 to 3, m = 0 to 7, n = 0 to 7

PIN0W

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
PIN37	PIN36	PIN35	PIN34	PIN33	PIN32	PIN31	PIN30	PIN27	PIN26	PIN25	PIN24	PIN23	PIN22	PIN21	PIN20	PIN17	PIN16	PIN15	PIN14	PIN13	PIN12	PIN11	PIN10	PIN07	PIN06	PIN05	PIN04	PIN03	PIN02	PIN01	PIN00	400A 3050H
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	Initial Value
R/W																																Pin Level

PIN4W

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
PIN77	PIN76	PIN75	PIN74	PIN73	PIN72	PIN71	PIN70	PIN67	PIN66	PIN65	PIN64	PIN63	PIN62	PIN61	PIN60	PIN57	PIN56	PIN55	PIN54	PIN53	PIN52	PIN51	PIN50	PIN47	PIN46	PIN45	PIN44	PIN43	PIN42	PIN41	PIN40	400A 3054H
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	Initial Value
R/W																																Pin Level

RPIN0W

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
RPIN37	RPIN36	RPIN35	RPIN34	RPIN33	RPIN32	RPIN31	RPIN30	RPIN27	RPIN26	RPIN25	RPIN24	RPIN23	RPIN22	RPIN21	RPIN20	RPIN17	RPIN16	RPIN15	RPIN14	RPIN13	RPIN12	RPIN11	RPIN10	RPIN07	RPIN06	RPIN05	RPIN04	RPIN03	RPIN02	RPIN01	RPIN00	400A 3450H
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	Initial Value
R/W																																Pin Level

Bit Position	Bit Name	Description
31 to 0	PINmn/ RPINln	These bits are for reading the input level of the port pins.

Remark: l = 0 to 3, m = 0 to 7, n = 0 to 7

8.4 List of Selectable Multiplexed Functions

The table below lists the combinations of multiplexed functions that can be specified by using the port-related registers.

(1) Ports (P00 to P77)

(1/3)

Pin Name	PMCmn = 0 (Port Mode)		PMCmn = 1 (Control Mode)			
			PFCEmn = 0		PFCEmn = 1	
	PMmn = 0 (Output Port)	PMmn = 1 (Input Port)	PFCmn = 0 (Multiplexed Function 1)	PFCmn = 1 (Multiplexed Function 2)	PFCmn = 0 (Multiplexed Function 3)	PFCmn = 1 (Multiplexed Function 4)
P00	P00 (output mode)	P00 (input mode)	INTPZ0	CATLEDRUN	-	-
P01	P01 (output mode)	P01 (input mode)	INTPZ1	CATIRQ	-	-
P02	P02 (output mode)	P02 (input mode)	INTPZ2	CATLEDSTER	-	-
P03	P03 (output mode)	P03 (input mode)	INTPZ3	CATLEDERR	-	CCS_MON5
P04	P04 (output mode)	P04 (input mode)	INTPZ4	CATLINKACT0	-	CCS_MON6
P05	P05 (output mode)	P05 (input mode)	INTPZ5	CATLINKACT1	-	CCS_MON7
P06	P06 (output mode)	P06 (input mode)	-	P0LINKLEDZ	-	CCS_MON0
P07	P07 (output mode)	P07 (input mode)	-	P1LINKLEDZ	-	CCS_RESOUT
P10	P10 (output mode)	P10 (input mode)	CATLATCH1	CATSYNC1	-	CCS_REFSTB
P11	P11 (output mode)	P11 (input mode)	CATLATCH0	CATSYNC0	-	CCS_MON4
P12	P12 (output mode)	P12 (input mode)	INTPZ6	-	-	-
P13	P13 (output mode)	P13 (input mode)	INTPZ7	-	CCS_WDTZ / CCM_WDTENZ	-
P14	P14 (output mode)	P14 (input mode)	SMSCK	-	-	-
P15	P15 (output mode)	P15 (input mode)	SMSI	-	-	-
P16	P16 (output mode)	P16 (input mode)	SMSO	-	-	-
P17	P17 (output mode)	P17 (input mode)	SMCSZ	-	-	-
P20	P20 (output mode)	P20 (input mode)	RXD0	–	CCM_LINKERRZ	-
P21	P21 (output mode)	P21 (input mode)	TXD0	–	CCM_ERRZ	-
P22	P22 (output mode)	P22 (input mode)	INTPZ8	CATI2CCLK	CCS_IOTENSU	-
P23	P23 (output mode)	P23 (input mode)	INTPZ9	CATI2CDATA	CCS_SENYU0	-
P24	P24 (output mode)	P24 (input mode)	INTPZ10	ETHSWSECOUT	CCS_SENYU1	-
P25	P25 (output mode)	P25 (input mode)	WDTOUTZ	–	CCS_ERRZ	-
P26	P26 (output mode)	P26 (input mode)	TIN1	TOUT1	CCM_RUNZ / CCS_RUNZ	-
P27	P27 (output mode)	P27 (input mode)	TIN0	TOUT0	-	-

Remark: m = 0 to 7, n = 0 to 7

(2/3)

Pin Name	PMCmn = 0 (Port Mode)		PMCmn = 1 (Control Mode)			
			PFCEmn = 0		PFCEmn = 1	
	PMmn = 0 (Output Port)	PMmn = 1 (Input Port)	PFCmn = 0 (Multiplexed Function 1)	PFCmn = 1 (Multiplexed Function 2)	PFCmn = 0 (Multiplexed Function 3)	PFCmn = 1 (Multiplexed Function 4)
P30	P30 (output mode)	P30 (input mode)	RXD1	-	-	-
P31	P31 (output mode)	P31 (input mode)	TXD1	-	-	-
P32	P32 (output mode)	P32 (input mode)	DMAREQZ1	-	-	CCS_MON1
P33	P33 (output mode)	P33 (input mode)	DMAACKZ1	-	-	CCS_MON2
P34	P34 (output mode)	P34 (input mode)	DMATCZ1	-	-	CCS_MON3
P35	P35 (output mode)	P35 (input mode)	CSISCK1	INTPZ22	CCM_IRLZ	-
P36	P36 (output mode)	P36 (input mode)	CSISI1	INTPZ23	CCS_FUSEZ	-
P37	P37 (output mode)	P37 (input mode)	CSISO1	INTPZ24	CCM_MSTZ	-
P40	P40 (output mode)	P40 (input mode)	A1	HA1	-	-
P41	P41 (output mode)	P41 (input mode)	WAITZ	HWAITZ	-	-
P42	P42 (output mode)	P42 (input mode)	SLEEPING	HERROUTZ	CCM_SDGCZ	-
P43	P43 (output mode)	P43 (input mode)	INTPZ11	HBUSCLK	-	-
P44	P44 (output mode)	P44 (input mode)	CSZ1	HPGCSZ	-	-
P45	P45 (output mode)	P45 (input mode)	CSISCK0	WAITZ1	-	-
P46	P46 (output mode)	P46 (input mode)	CSISI0	WAITZ2	-	-
P47	P47 (output mode)	P47 (input mode)	CSISO0	WAITZ3	-	-
P50	P50 (output mode)	P50 (input mode)	CSZ3	-	CCM_LNKRUNZ / CCS_LNKRUNZ	-
P51	P51 (output mode)	P51 (input mode)	CSZ2	-	CCM_RDLEDZ / CCS_RDLEDZ	-
P52	P52 (output mode)	P52 (input mode)	TIN3	TOUT3	CCS_SDGATEON	-
P53	P53 (output mode)	P53 (input mode)	CRXD0	CCS_RD	CCM_RD	-
P54	P54 (output mode)	P54 (input mode)	CTXD0	CCS_SD	CCM_SD	-
P55	P55 (output mode)	P55 (input mode)	CRXD1	–	–	-
P56	P56 (output mode)	P56 (input mode)	CTXD1	CATRESTOUT	-	-
P57	P57 (output mode)	P57 (input mode)	TIN2	TOUT2	-	-

Remark: m = 0 to 7, n = 0 to 7

(3/3)

Pin Name	PMCmn = 0 (Port Mode)		PMCmn = 1 (Control Mode)			
			PFCEmn = 0		PFCEmn = 1	
	PMmn = 0 (Output Port)	PMmn = 1 (Input Port)	PFCmn = 0 (Multiplexed Function 1)	PFCmn = 1 (Multiplexed Function 2)	PFCmn = 0 (Multiplexed Function 3)	PFCmn = 1 (Multiplexed Function 4)
P60	P60 (output mode)	P60 (input mode)	SCL0	–	–	–
P61	P61 (output mode)	P61 (input mode)	SDA0	–	–	–
P62	P62 (output mode)	P62 (input mode)	RTDMAREQZ	–	CCM_MDIN0	–
P63	P63 (output mode)	P63 (input mode)	RTDMAACKZ	–	CCM_MDIN1	–
P64	P64 (output mode)	P64 (input mode)	RTDMATCZ	–	CCM_MDIN2	–
P65	P65 (output mode)	P65 (input mode)	DMAREQZ0	–	CCM_MDIN3	–
P66	P66 (output mode)	P66 (input mode)	DMAACKZ0	–	–	–
P67	P67 (output mode)	P67 (input mode)	DMATCZ0	–	–	–
P70	P70 (output mode)	P70 (input mode)	CSICS00	P0DUPLEXLEDZ	CCS_STATION_NO_0 / CCM_SNIN0	–
P71	P71 (output mode)	P71 (input mode)	CSICS01	-	CCS_STATION_NO_1 / CCM_SNIN1	–
P72	P72 (output mode)	P72 (input mode)	CSICS10	P0SPEED100LEDZ	CCS_STATION_NO_2 / CCM_SNIN2	–
P73	P73 (output mode)	P73 (input mode)	CSICS11	P0SPEED10LEDZ	CCS_STATION_NO_3 / CCM_SNIN3	–
P74	P74 (output mode)	P74 (input mode)	INTPZ12	P1DUPLEXLEDZ	CCS_STATION_NO_4 / CCM_SNIN4	–
P75	P75 (output mode)	P75 (input mode)	INTPZ13	-	CCS_STATION_NO_5 / CCM_SNIN5	–
P76	P76 (output mode)	P76 (input mode)	INTPZ14	P1SPEED100LEDZ	CCS_STATION_NO_6 / CCM_SNIN6	–
P77	P77 (output mode)	P77 (input mode)	INTPZ15	P1SPEED10LEDZ	CCS_STATION_NO_7 / CCM_SNIN7	–

Remark: m = 0 to 7, n = 0 to 7

(2) Real-time control ports (RP00 to RP37)

Pin Name	PMCmn = 0 (Port Mode)		PMCmn = 1 (Control Mode)			
			RPFCEmn = 0		RPFCEmn = 1	
	PMmn = 0 (Output Port)	PMmn = 1 (Input Port)	PFCmn = 0 (Multiplexed Function 1)	PFCmn = 1 (Multiplexed Function 2)	PFCmn = 0 (Multiplexed Function 3)	PFCmn = 1 (Multiplexed Function 4)
RP00	RP00 (output mode)	RP00 (input mode)	INTPZ16	SCL1	CCM_SDLEDZ / CCS_SDLEDZ	-
RP01	RP01 (output mode)	RP01 (input mode)	INTPZ17	SDA1	CCM_SMSTZ	-
RP02	RP02 (output mode)	RP02 (input mode)	INTPZ18	P0ACTLEDZ	CCS_BS1	-
RP03	RP03 (output mode)	RP03 (input mode)	INTPZ19	–	CCS_BS2	-
RP04	RP04 (output mode)	RP04 (input mode)	INTPZ20	P1ACTLEDZ	CCS_BS4	-
RP05	RP05 (output mode)	RP05 (input mode)	INTPZ21	–	CCS_BS8	-
RP06	RP06 (output mode)	RP06 (input mode)	WRZ2/ BENZ2	HWRZ2/ HBENZ2	-	–
RP07	RP07 (output mode)	RP07 (input mode)	WRZ3/ BENZ3	HWRZ3/ HBENZ3	-	–
RP10	RP10 (output mode)	RP10 (input mode)	D24/HD24	–	-	–
RP11	RP11 (output mode)	RP11 (input mode)	D25/HD25	–	-	–
RP12	RP12 (output mode)	RP12 (input mode)	D26/HD26	–	-	–
RP13	RP13 (output mode)	RP13 (input mode)	D27/HD27	–	-	–
RP14	RP14 (output mode)	RP14 (input mode)	D28/HD28	–	-	–
RP15	RP15 (output mode)	RP15 (input mode)	D29/HD29	–	-	–
RP16	RP16 (output mode)	RP16 (input mode)	D30/HD30	–	-	–
RP17	RP17 (output mode)	RP17 (input mode)	D31/HD31	–	-	-
RP20	RP20 (output mode)	RP20 (input mode)	BCYSTZ	HBCYSTZ	-	-
RP21	RP21 (output mode)	RP21 (input mode)	A21	–	-	-
RP22	RP22 (output mode)	RP22 (input mode)	A22	–	–	-
RP23	RP23 (output mode)	RP23 (input mode)	A23	–	–	-
RP24	RP24 (output mode)	RP24 (input mode)	A24	INTPZ25	–	-
RP25	RP25 (output mode)	RP25 (input mode)	A25	INTPZ26	–	-
RP26	RP26 (output mode)	RP26 (input mode)	A26	INTPZ27	–	-
RP27	RP27 (output mode)	RP27 (input mode)	A27	INTPZ28	–	-
RP30	RP30 (output mode)	RP30 (input mode)	D16/HD16	-	–	-
RP31	RP31 (output mode)	RP31 (input mode)	D17/HD17	-	–	-
RP32	RP32 (output mode)	RP32 (input mode)	D18/HD18	-	–	-
RP33	RP33 (output mode)	RP33 (input mode)	D19/HD19	-	–	-
RP34	RP34 (output mode)	RP34 (input mode)	D20/HD20	-	–	-
RP35	RP35 (output mode)	RP35 (input mode)	D21/HD21	-	–	-
RP36	RP36 (output mode)	RP36 (input mode)	D22/HD22	-	–	-
RP37	RP37 (output mode)	RP37 (input mode)	D23/HD23	-	–	-

Remark: m = 0 to 3, n = 0 to 7

8.5 Buffer Switching Registers (DRCTL)

For some port pins, the driving ability and the connection or disconnection of a pull-up or pull-down resistor is programmable.

Set up the DRCTL registers during initialization after release from the reset state. After that, change the setting of a given DRCTL register only while the buffer functions for the corresponding pins are not in use. For example, change the setting while only internal access is proceeding.

The settings of the DRCTL registers are effective for output pins regardless of their operating mode (port mode, or control mode, in which a multiplexed function is used).

- Access These registers can be read and written in 32-bit or 16-bit units.

Cautions 1. These registers are only writable after protection has been released by a special sequence of writing to the system protection command register (SYSPCMD). For how to release protection, see the description of the system protection command register (SYSPCMD). No special sequence is required for reading the register.

2. Take special care with pins in the high-impedance state, since changing the settings for the pull-up and pull-down resistors will affect levels on the pins.

8.5.1 Port 1 Buffer Function Change Registers (DRCTLP1L, DRCTLP1H)

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
DRCTLP1L	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	PUIOP13	PDIOP13	0	1	PUIOP12	PDIOP12	0	1	PUIOP11	PDIOP11	0	1	PUIOP10	PDIOP10	IOLP101	IOLP100	BASE + 0228H
																																	Initial Value
R/W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R/W	R/W	0	1	R/W	R/W	0	1	R/W	R/W	0	1	R/W	R/W	R/W	R/W	0000 9959H

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
DRCTLP1H	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	PUIOP17	PDIOP17	0	1	PUIOP16	PDIOP16	0	1	PUIOP15	PDIOP15	0	1	PUIOP14	PDIOP14	0	1	BASE + 022CH
																																	Initial Value
R/W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R/W	R/W	0	1	R/W	R/W	0	1	R/W	R/W	0	1	R/W	R/W	0	1	0000 9999H

Bit Position	Bit Name	Description
31 to 16	–	Reserved. (Be sure to write 0 to these bits. If read, 0 is returned.)
15, 14, 11, 10, 7, 6, 3. 2	PUIOP1n, PDIOP1n	These bits specify whether to connect a pull-up or pull-down resistor to the P17 to P10 pins.

PUIO	PDIO	Connection of a Pull-Up or Pull-Down Resistor to the P17 to P10 Pins
0	0	Do not connect a pull-up or pull-down resistor.
0	1	Connect a pull-down resistor.
1	0	Connect a pull-up resistor.
1	1	Setting prohibited

1, 0	IOLP101, IOLP100	These bits specify the driving ability of the P10 pin.

IOL1	IOL0	Driving Ability of the P10 Pin
0	1	6 mA (recommended)
1	1	12 mA
Other than above		Setting prohibited

Remark: n = 7 to 0

8.5.2 Port 3 Buffer Function Change Registers (DRCTLP3L, DRCTLP3H)

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
DRCTLP3L	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	PUIOP33	PDIOP33	0	1	PUIOP32	PDIOP32	0	1	PUIOP31	PDIOP31	0	1	PUIOP30	PDIOP30	0	1	BASE + 0238H
																																	Initial Value
R/W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R/W	R/W	0	1	R/W	R/W	0	1	R/W	R/W	0	1	R/W	R/W	0	1	0000 9999H

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
DRCTLP3H	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	PUIOP37	PDIOP37	IOLP371	IOLP370	PUIOP36	PDIOP36	0	1	PUIOP35	PDIOP35	0	1	PUIOP34	PDIOP34	0	1	BASE + 023CH
																																	Initial Value
R/W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R/W	R/W	R/W	R/W	R/W	R/W	0	1	R/W	R/W	0	1	R/W	R/W	0	1	0000 9999H

Bit Position	Bit Name	Description
31 to 16	–	Reserved. (Be sure to write 0 to these bits. If read, 0 is returned.)
15, 14, 11, 10, 7, 6, 3, 2	PUIOP3n, PDIOP3n	These bits specify whether to connect a pull-up or pull-down resistor to the P37 to P30 pins.

PUIO	PDIO	Connection of a Pull-Up or Pull-Down Resistor to the P37 to P30 Pins
0	0	Do not connect a pull-up or pull-down resistor.
0	1	Connect a pull-down resistor.
1	0	Connect a pull-up resistor.
1	1	Setting prohibited

13, 12	IOLP371, IOLP370	These bits specify the driving ability of the P37 pin.

IOL1	IOL0	Driving Ability of the P37 Pin
0	1	6 mA (recommended)
1	1	12 mA
Other than above		Setting prohibited

Remark n = 7 to 0

8.5.3 Port 4 Buffer Function Change Registers (DRCTLP4L, DRCTLP4H)

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
DRCTLP4L	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	PUIOP43	PDIOP43	0	1	PUIOP42	PDIOP42	0	1	PUIOP41	PDIOP41	0	1	PUIOP40	PDIOP40	0	1	BASE + 0240H
																																	Initial Value
R/W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R/W	R/W	0	1	R/W	R/W	0	1	R/W	R/W	0	1	R/W	R/W	0	1	0000 9999H

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
DRCTLP4H	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	PUIOP47	PDIOP47	0	1	PUIOP46	PDIOP46	0	1	PUIOP45	PDIOP45	0	1	PUIOP44	PDIOP44	0	1	BASE + 0244H
																																	Initial Value
R/W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R/W	R/W	0	1	R/W	R/W	0	1	R/W	R/W	0	1	R/W	R/W	0	1	0000 9999H

Bit Position	Bit Name	Description
31 to 16	–	Reserved. (Be sure to write 0 to these bits. If read, 0 is returned.)
15, 14, 11, 10, 7, 6, 3, 2	PUIOP4n, PDIOP4n	These bits specify whether to connect a pull-up or pull-down resistor to the P47 to P40 pins.

PUIO	PDIO	Connection of a Pull-Up or Pull-Down Resistor to the P47 to P40 Pins
0	0	Do not connect a pull-up or pull-down resistor.
0	1	Connect a pull-down resistor.
1	0	Connect a pull-up resistor.
1	1	Setting prohibited

Remark: n = 7 to 0

8.5.4 Port 5 Buffer Function Change Registers (DRCTLP5L, DRCTLP5H)

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
DRCTLP5L	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	PUIOP52	PDIOP52	0	1	PUIOP51	PDIOP51	IOLP511	IOLP510	PUIOP50	PDIOP50	IOLP501	IOLP500	BASE + 0248H
																																	Initial Value
																																	0000 0599H
R/W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
DRCTLP5H	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	PUIOP57	PDIOP57	0	1	0	0	0	0	0	0	0	0	0	0	0	0	BASE + 024CH
																																	Initial Value
																																	0000 9000H
R/W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R/W	R/W	0	1	0	0	0	0	0	0	0	0	0	0	0	0	

Bit Position	Bit Name	Description
31 to 16	–	Reserved. (Be sure to write 0 to these bits. If read, 0 is returned.)
15, 14, 11, 10, 7, 6, 3, 2	PUIOP5n, PDIOP5n	These bits specify whether to connect a pull-up or pull-down resistor to the P57 and P52 to P50 pins.

PUIO	PDIO	Connection of a Pull-Up or Pull-Down Resistor to the P57 and P52 to P50 Pins
0	0	Do not connect a pull-up or pull-down resistor.
0	1	Connect a pull-down resistor.
1	0	Connect a pull-up resistor.
1	1	Setting prohibited

5, 4, 1, 0	IOLP5n1, IOLP5n0	These bits specify the driving ability of the P51 and P50 pins.

IOL1	IOL0	Driving Ability of the P51 and P50 Pins
0	1	6 mA (recommended)
1	1	12 mA
Other than above		Setting prohibited

Remark: n = 7 to 0

8.5.5 Real-Time Port 0 Buffer Function Change Registers (DRCTLRP0L, DRCTLRP0H)

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
DRCTLRP0L	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	PUIORP03	PDIORP03	IOLRP031	IOLRP030	PUIORP02	PDIORP02	IOLRP021	IOLRP020	PUIORP01	PDIORP01	IOLRP011	IOLRP010	PUIORP00	PDIORP00	IOLRP001	IOLRP000	BASE + 0260H
																																	Initial Value
																																	0000 9999H
R/W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
DRCTLRP0H	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	PUIORP07	PDIORP07	IOLRP071	IOLRP070	PUIORP06	PDIORP06	IOLRP061	IOLRP060	PUIORP05	PDIORP05	IOLRP051	IOLRP050	PUIORP04	PDIORP04	IOLRP041	IOLRP040	BASE + 0264H
																																	Initial Value
																																	0000 9999H
R/W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

Bit Position	Bit Name	Description
31 to 16	–	Reserved. (Be sure to write 0 to these bits. If read, 0 is returned.)
15, 14, 11, 10, 7, 6, 3, 2	PUIORP0n, PDIORP0n	These bits specify whether to connect a pull-up or pull-down resistor to the RP07 to RP00 pins.
13, 12, 9, 8, 5, 4, 1, 0	IOLRP0n1, IOLRP0n0	These bits specify the driving ability of the RP07 to RP00 pins.

PUIO	PDIO	Connection of a Pull-Up or Pull-Down Resistor to the RP07 to RP00 Pins
0	0	Do not connect a pull-up or pull-down resistor.
0	1	Connect a pull-down resistor.
1	0	Connect a pull-up resistor.
1	1	Setting prohibited

IOL1	IOL0	Driving Ability of the RP07 to RP00 Pins
0	1	6 mA (recommended)
1	1	12 mA
Other than above		Setting prohibited

Remark: n = 7 to 0

8.5.6 Real-Time Port 1 Buffer Function Change Registers (DRCTLRP1L, DRCTLRP1H)

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
DRCTLRP1L	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	PUIORP13	PDIORP13	IOLRP131	IOLRP130	PUIORP12	PDIORP12	IOLRP121	IOLRP120	PUIORP11	PDIORP11	IOLRP111	IOLRP110	PUIORP10	PDIORP10	IOLRP101	IOLRP100	BASE + 0268H
																																	Initial Value
																																	0000 9999H
R/W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
DRCTLRP1H	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	PUIORP17	PDIORP17	IOLRP171	IOLRP170	PUIORP16	PDIORP16	IOLRP161	IOLRP160	PUIORP15	PDIORP15	IOLRP151	IOLRP150	PUIORP14	PDIORP14	IOLRP141	IOLRP140	BASE + 026CH
																																	Initial Value
																																	0000 9999H
R/W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

Bit Position	Bit Name	Description
31 to 16	–	Reserved. (Be sure to write 0 to these bits. If read, 0 is returned.)
15, 14, 11, 10, 7, 6, 3, 2	PUIORP1n, PDIORP1n	These bits specify whether to connect a pull-up or pull-down resistor to the RP17 to RP10 pins.

PUIO	PDIO	Connection of a Pull-Up or Pull-Down Resistor to the RP17 to RP10 Pins
0	0	Do not connect a pull-up or pull-down resistor.
0	1	Connect a pull-down resistor.
1	0	Connect a pull-up resistor.
1	1	Setting prohibited

13, 12, 9, 8, 5, 4, 1, 0	IOLRP1n1, IOLRP1n0	These bits specify the driving ability of the RP17 to RP10 pins.

IOL1	IOL0	Driving Ability of the RP17 to RP10 Pins
0	1	6 mA (recommended)
1	1	12 mA
Other than above		Setting prohibited

Remark: n = 7 to 0

8.5.7 Real-Time Port 2 Buffer Function Change Registers (DRCTLRP2L, DRCTLRP2H)

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
DRCTLRP2L	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	PUIORP23	PDIORP23	IOLRP231	IOLRP230	PUIORP22	PDIORP22	IOLRP221	IOLRP220	PUIORP21	PDIORP21	IOLRP211	IOLRP210	PUIORP20	PDIORP20	IOLRP201	IOLRP200	BASE + 0270H
																																	Initial Value
																																	0000 5559H
R/W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
DRCTLRP2H	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	PUIORP27	PDIORP27	IOLRP271	IOLRP270	PUIORP26	PDIORP26	IOLRP261	IOLRP260	PUIORP25	PDIORP25	IOLRP251	IOLRP250	PUIORP24	PDIORP24	IOLRP241	IOLRP240	BASE + 0274H
																																	Initial Value
																																	0000 5555H
R/W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

Bit Position	Bit Name	Description
31 to 16	–	Reserved. (Be sure to write 0 to these bits. If read, 0 is returned.)
15, 14, 11, 10, 7, 6, 3, 2	PUIORP2n, PDIORP2n	These bits specify whether to connect a pull-up or pull-down resistor to the RP27 to RP20 pins.
13, 12, 9, 8, 5, 4, 1, 0	IOLRP2n1, IOLRP2n0	These bits specify the driving ability of the RP27 to RP20 pins.

PUIO	PDIO	Connection of a Pull-Up or Pull-Down Resistor to the RP27 to RP20 Pins
0	0	Do not connect a pull-up or pull-down resistor.
0	1	Connect a pull-down resistor.
1	0	Connect a pull-up resistor.
1	1	Setting prohibited

IOL1	IOL0	Driving Ability of the RP27 to RP20 Pins
0	1	6 mA (recommended)
1	1	12 mA
Other than above		Setting prohibited

Remark: n = 7 to 0

8.5.8 Real-Time Port 3 Buffer Function Change Registers (DRCTLRP3L, DRCTLRP3H)

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
DRCTLRP3L	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	PUIORP33	PDIORP33	IOLRP331	IOLRP330	PUIORP32	PDIORP32	IOLRP321	IOLRP320	PUIORP31	PDIORP31	IOLRP311	IOLRP310	PUIORP30	PDIORP30	IOLRP301	IOLRP300	BASE + 0278H
																																	Initial Value
																																	0000 9999H
R/W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
DRCTLRP3H	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	PUIORP37	PDIORP37	IOLRP371	IOLRP370	PUIORP36	PDIORP36	IOLRP361	IOLRP360	PUIORP35	PDIORP35	IOLRP351	IOLRP350	PUIORP34	PDIORP34	IOLRP341	IOLRP340	BASE + 027CH
																																	Initial Value
																																	0000 9999H
R/W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

Bit Position	Bit Name	Description
31 to 16	–	Reserved. (Be sure to write 0 to these bits. If read, 0 is returned.)
15, 14, 11, 10, 7, 6, 3, 2	PUIORP3n, PDIORP3n	These bits specify whether to connect a pull-up or pull-down resistor to the RP37 to RP30 pins.
13, 12, 9, 8, 5, 4, 1, 0	IOLRP3n1, IOLRP3n0	These bits specify the driving ability of the RP37 to RP30 pins.

PUIO	PDIO	Connection of a Pull-Up or Pull-Down Resistor to the RP37 to RP30 Pins
0	0	Do not connect a pull-up or pull-down resistor.
0	1	Connect a pull-down resistor.
1	0	Connect a pull-up resistor.
1	1	Setting prohibited

IOL1	IOL0	Driving Ability of the RP37 to RP30 Pins
0	1	6 mA (recommended)
1	1	12 mA
Other than above		Setting prohibited

Remark: n = 7 to 0

8.6 Operation of Port Functions

Operation of the ports differs depending on the I/O mode setting as described below.

8.6.1 Reading and Writing via I/O Ports

(1) In Output Mode

If a value is written to port register n (Pn or RPn), the value is written to that port's output latch (Pn or RPn). The value of the output latch is output from the pin.

The value written to the output latch is held until another value is written.

The value of the output latch (Pn or RPn) can be read by reading port register n (Pn or RPn).

To directly read the pin level, read port pin input register n (PINn or RPINn).

(2) In Input Mode

If a value is written to port register n (Pn or RPn), the value is written to that port's output latch (Pn or RPn). However, the pin state does not change because the output buffer is off.

The value written to the output latch is held until another value is written.

To read the input level, read port pin input register n (PINn or RPINn).

8.6.2 Multiplexed Function Pin Output State in Control Mode

The port pin level can be read directly by reading port pin input register n (PINn or RPINn), regardless of the settings of the PMCn, PMn, PFCn, and PFCEn registers.

8.7 Trigger-Synchronous Ports (RP00 to RP37)

The state of the 32-bit port pins RP00 to RP37 can be updated in synchronization with an interrupt from an on-chip peripheral function.

Use the RPTRGMD register to set trigger-synchronous port control mode in 1-bit units. To select the target trigger, use the RPTFR0 to RPTFR3 registers.

For details, see the R-IN32M3 Series User's Manual (Peripheral Modules).

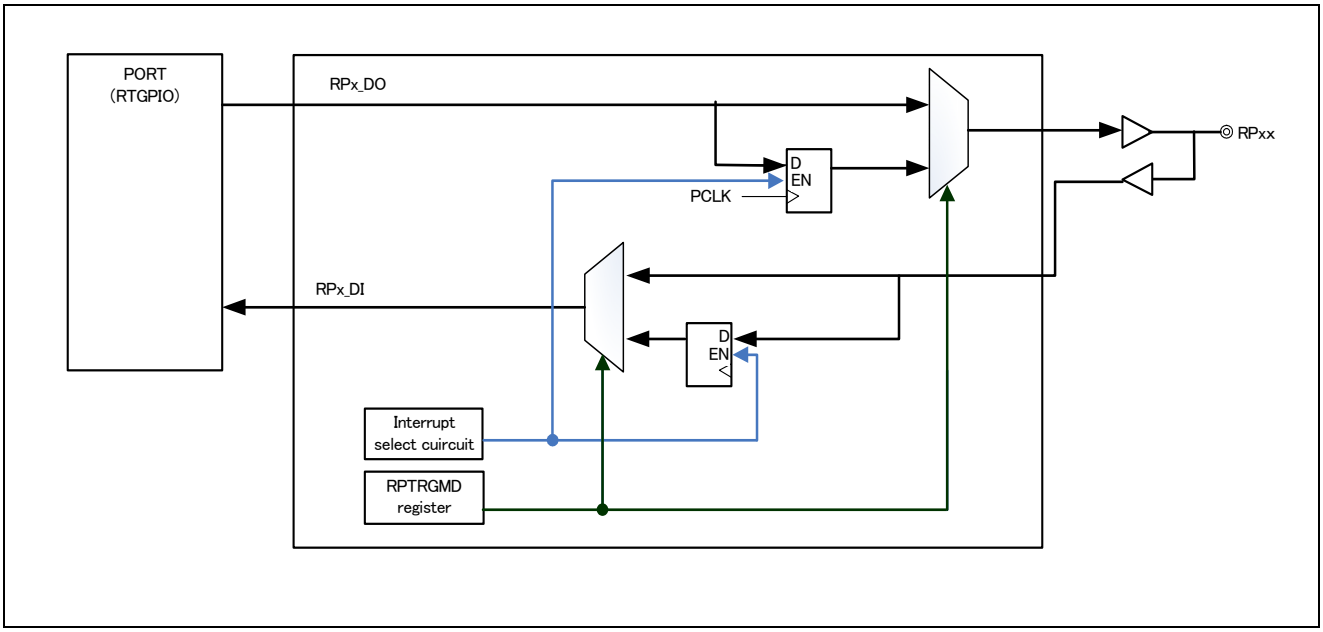


Figure 8.19 Configuration of Trigger-Synchronous Ports

9. Electrical Characteristics

For details on the electrical characteristics, refer to the R-IN32M3 Series Datasheet.

REVISION HISTORY	R-IN32M3 Series User's Manual: R-IN32M3-EC

Rev.	Date	Description	
		Page	Summary
1.00 (Preliminary)	Feb. 8, 2013	-	First edition issued
1.00	Apr. 03,2013	Overall	Modification of English expressions
		Overall	Change the description of "CC-Link" "CC-Link (Slave)" → "CC-Link (Remote device station)"
		1	Modification of the contents of ***1.1 Introduction***
		3	Standby mode deletion of Table1.1 Overview of R-IN32M3-EC
		9	Modification of the status of BUSCLK during the reset of ***2.1.2 External Memory Interface Signals*** Addition of synchronous burst access MEMC information of ***2.1.2 External Memory Interface Signals***
		10	Modification of the status of HD0-HD15, HBCYSTZ during the reset of ***2.1.3 External MPU Interface Signals***
		21	Modification of PONRZ function of ***2.1.16 System Signals*** Addition the signals of HOTRESETZ, VDDQ_MII of ***2.1.16 System Signals***
		24	Modification of the status of P40 of ***2.2Port status*** Modification of the contents of Note1 and Note2 of ***2.2Port status***
1.01	Dec. 09 ,2013	Overall	Modification of the supported station of CC-Link
2.00	Feb. 07,2014	4	Addition of a connection of GPIO block and DMAC_RTPORT bus of ***1.3 Internal block diagram*** Addition of a connection of RealTimeGPIO block and DMAC bus of ***1.3 Internal block diagram***
		6-24	Addition the status after reset timing of ***2.1 Signals by function***
		21	Add ***CCM_CLK80M*** pins to list of ***2.1.15 CC-Link Signals (Remote device station)***
		22	Deletion the description about VDDQ_MII of ***2.1.16 System Signals***
		24	Modification of Boot mode select of ***2.1.18 Operation mode Setting Signals***
		25	Addition Synchronous burst MEMC of ***2.2 Port status***
		28-29	Addition of a resister value of Pull up/down of ***2.3.5 Port Signals*** Modification of a description of the drive current of P10/P30/P31/P52 of ***2.3.5 Port Signals***
		29	Modification of title name of ***2.3.7 CC-Link Signal (Intelligent device station, Remote device station)***
		30	Modification of the end address of EtherCAT area of ***Fig.3.1 Memory Map (ALL)***
		33	Modification of the end address of EtherCAT area of ***Fig.3.5 External MPU interface area***
		38	Addition of the contents of Note of INTCCSRFSTB register of ***4.2 Interrupt list***
		41	Addition ***6.2 Peripheral circuit of EtherCAT***
		47	Addition ***7. Ether PHY Function***
		96	Modification of initial value of ***Fig.8.7 Port mode registers***

Rev.	Date	Description	
		Page	Summary
2.01	Apr. 18,2014	Overall	Modification of ***CC-Link Signals (Remote device station)***
		60	Modification of the contents of ACKNOWLEDGE bit of ***7.4.5 Register 5 - Auto-Negotiation Link Partner Ability (Base Page) Register***
3.00	Jun. 30,2014	22	Modification of attribution of FB of ***2.1.16 System Signals***
		30	Modification of the end address of EtherCAT area of ***Fig.3.1 Memory Map (ALL)***
		33	Modification of the end address of EtherCAT area of ***Fig.3.5 External MPU interface area***
		40-125	Modification of ***6 EtherCAT Slave Controller function***
3.01	Dec. 25,2014	3	Change status for Intelligent device station for CC-Link in ***1.3 Overview***
		196	Remove IOLP521, IOLP520 bit at ***8.5.4 Port 5 buffer function change registers (DRCTLP5L, DRCTLP5H)*** (because driving capability of P52 is fixed to 6mA.)
4.00	Jan. 22, 2016	6-25	2. Pin Functions Meaning of the items, symbols, and abbreviations, added to the list of pins Description unified
		10	2.1.3 External Memory Interface Pins • The value of BUSCLK during reset and after reset, modified • Supplemental explanations added to Note 1
		18	2.1.11 Trace Pins The value of TRACECLK during reset and after reset, modified
		20	2.1.14 CC-Link Pins (Intelligent Device Station) Functional description on CCM_CLK80M, modified
		21	2.1.15 CC-Link Pins (Remote Device Station) Note added to CCM_CLK80M
		22	2.1.16 System Pins • Functional description and active level of XT1/XT2/OSCTH/JTAGSEL, modified • The value of RSTOUTZ during reset and after reset, modified
		24, 25	2.1.18 Operating Mode Setting Pins • Functional description of the ADMUXMODE pin, modified • The list of the combinations of available operating mode setting pins, added
		26-35	2.2 Pin States The initial states for all boot modes and all port pins, added
		37	2.3.4 System Pins • Recommended connection when not using XT1/XT2, modified Note added • Recommended connection when not using OSCTH/JTAGSEL, modified
		39	2.3.7 Operation Mode Setting Pins Recommended connection when not in use, modified
		40	Figure 3.1 Memory Map (ALL) Instruction RAM area and instruction RAM mirror area, modified
		43	Figure 3.5 External MCU Interface Area Instruction RAM mirror area, modified

Rev.	Date	Description	
		Page	Summary
4.00	Jan. 22, 2016	44	4.1 Exceptions List Abbreviations of reset pins, modified SYSRESET register, added
		58	6.5 List of EtherCAT Registers, (7) PDI Registers Number of bits, modified
		62	6.5 List of EtherCAT Registers, (16) ETC Registers Remark added
		84	6.12.2 ESC Configuration Register (ESC_CONFIG) Initial value, and description on bit 0, modified Note added
		86	6.12.4 SYNC/LATCH PDI Configuration Register (SYNC_LATCH_CONFIG) Description on the initial value, modified Note 1 and Note 2, added
		127	6.20.4.2 Pulse Length of Sync Signals Register (DC_PULSE_LEN) Description on the initial value, modified Note added
4.01	Feb. 28, 2017	9	2.1.2 EtherCAT Slave Controller Pins Active level of CATRESTOUT modified
		15	2.1.5 Port Pins and Real-Time Port Pins Mode 2 of P73 pin modified
		20	2.1.14 CC-Link Pins (Intelligent Device Station) Function of CCM_MDIN0-CCM_MDIN3 modified
		22	2.1.16 System Pins Function of PONRZ modified
		47	4.2 List of Interrupts, Table 4.1 (2/4) Exception No.54 INTETHSW: Interrupt source name changed
		48-49	4.2 List of Interrupts, Table 4.1 (3/4), (4/4) ECC error interrupts added to exception No. 115 to 120
		50	5. Peripheral Modules Expressions of peripheral functions are unified to that in the User's Manual (Peripheral Modules)
		53	6.3 Interrupt and I/O Signals, Table 6.3 Active level of CATRESTOUT modified
		65	6.6.3 EtherCAT Reset Register (CATRESET) Caution 2 modified
		79	6.11.1 AL Control Register (AL_CONTROL) Device Identification Request added into bit5
		80	6.11.2 AL Status Register (AL_STATUS) Device Identification Status added into bit5 Write from PDI added
		85	6.12.3 PDI Configuration Register (PDI_CONFIG) Value indicated by ONCHIPBUS, modified (100 → 010)
		142-143	6.22 Reset circuit Explanation of reset circuit around ESC added

Rev.	Date	Description	
		Page	Summary
4.01	Feb. 28, 2017	150	7.2.4 Fast Link-Loss Detection Function Explanation of error count method modified
		151	7.3.1 Hardware Power-Down mode Minimum reset time added
		153	7.4 MII Management Registers in Ethernet PHY Explanation about the symbols below bit name of registers added
		154-176	7.4.1 Register 0 – Control Register to 7.4.24 Register 31 – PHY Special Control/Status Register Description changed PHY Address to Register Address
		179	7.5.3 Ethernet PHY Power-Up Status Register (PHYPUS) Time for bits to be cleared added
		180	7.6 LED signal added
5.00	Dec. 28, 2018	6	1.5 Base Addresses of the System Registers Area The description on the base addresses of the system registers area was added.
		18	2.1.7 DMA Interface Pins The description on the section and caution was modified.
		21	2.1.14 CC-Link Pins (Intelligent Device Station) Functional descriptions of the CC-Link (intelligent device station) pins were modified.
		41, 44	3. Memory Maps Note describing that the addresses the instruction RAM mirror area (768 Kbytes) where access actually occurs will change according to the select boot mode, was added. Figure 3.1 Memory Map (All) Figure 3.5 External MCU Interface Space
		183	8.2 Port Configuration "Application and Operation" for the port function control registers and the port function control expansion registers was modified.
		183	8.2 Port Configuration Caution on the port configuration was modified.
		197 to 205	8.3.3 Port Mode Control Register (PMC, RPMC) 8.3.4 Port Function Control Registers (PFC, RPFC) 8.3.5 Port Function Control Expansion Registers (PFCE, RPFCE) Notes on the multiplexed functions were modified.
		—	Error corrected, description modified, and contents and expressions adjusted
5.01	Jan. 12, 2021	3 55, 57 145	1.2 Overview 6.4 Functional Overview 7.1 Features Description on no support of EtherCAT P was added.
6.00	May 31, 2024	39	2.3.5 Test Pins Changed description of connection method when TEST1, TEST2 and TEST3 are not connected

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