Contents

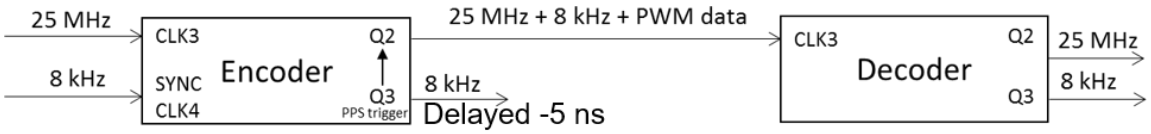
List of Figures

1. Overview

This document explains how to configure ClockMatrix for the transmission of Time of Day (ToD) frames using the Pulse Width Modulation (PWM) feature of the device. It discusses how to encode and decode a signal using the PWM feature. Two separate Clock Matrix boards are used in this configuration example: one to encode the ToD frame on a carrier signal, and the other to decode the ToD frame from the carrier signal. By going through this example, a user can use the PWM feature of the device to encode and decode any type of bit pattern (i.e., signature, user defined frame, or ToD frame) on a carrier clock or have working knowledge to do so.

The PWM encoder encodes PPS_frames that are transmitted on the output clock. It has a PWM demodulator that oversamples the clock and determines the value of the bits that were encoded. The decoder then takes the bits as detected by the demodulator and combines to identify the PWM_PPS frames. The frames are inserted into the PWM_FIFO. As a result, the goal is to write on the encoder side and read it on the decoder side as shown in the following diagram.

Figure 1. ClockMatrix PWM Feature Overview



All the GUI bits in this document are needed for the PWM_PPS to work. The write_data for the decoder and encoder are mandatory and should be configured exactly as discussed, while the write_data for the inputs, the reference monitors, DPLLs, and outputs are for illustration purposes only, but can be used to get started.

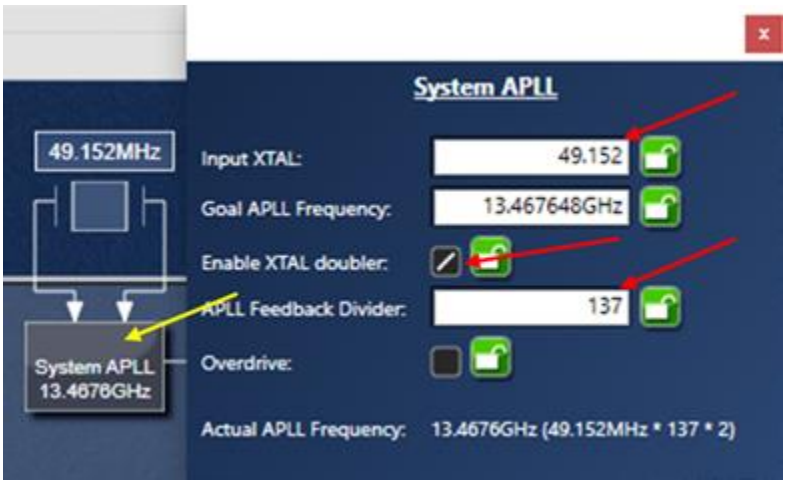
Timing Commander images are also shown in this document for use with the GUI, instead of register access. Some registers need to be accessed via Bit Sets of the GUI.

The words transmitter/encoder and receiver/decoder are used interchangeably in this document.

2. How to Set Up Clock Matrix for PWM_PPS Framing – Transmitter

1. Configure the SYS_APLL.

Figure 2. Timing Commander: System APLL Box

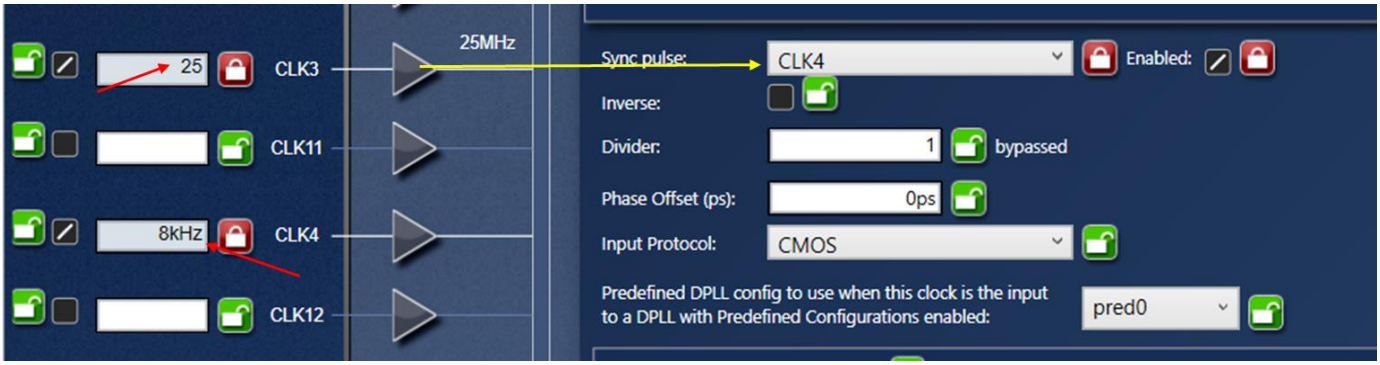


Click on the “System APLL” box and update the settings.

2. Configure the input for the input clock.

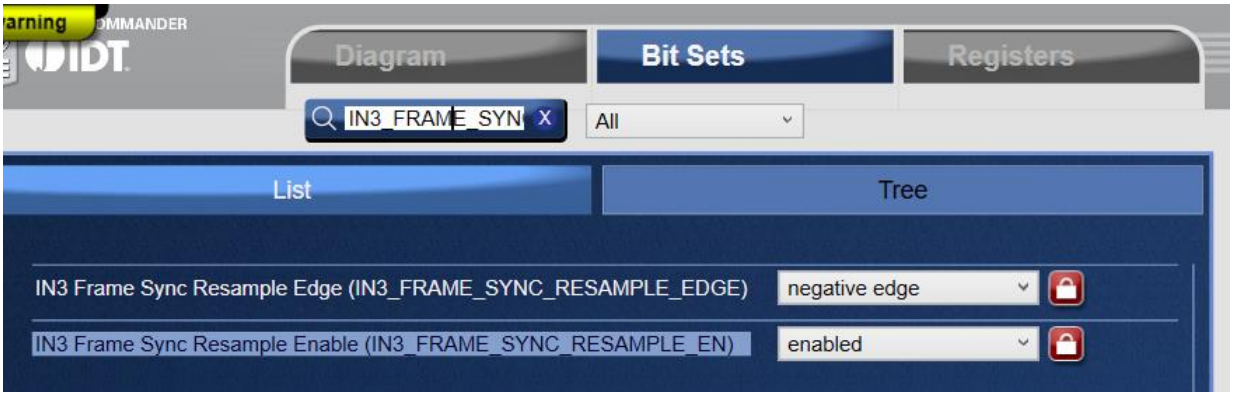
Connect the input clock to the configured input on the board. CLK3 is selected as the clock and CLK4 is selected as the corresponding sync pulse.

Figure 3. Timing Commander: CLK3 and CLK4 Fields



Enter 25 into CLK3 field and enter 8k into CLK4 field on the main menu. Click on the “Buffer” for CLK3 and select “CLK4” as the Sync Pulse. Also, click on the Enable bit.

Figure 4. Timing Commander: Switch to the Bit Sets Tab



Switch to the Bit Sets Tab and search for “IN3_FRAME_SYNC_RESAMPLE”, then enable the two bits.

3. Configure the reference monitors.

The reference monitor should have the same number as the input being used (e.g., for Input 3, REF_MON_3 should be configured). Input 3 is used in the example.

x = Reference Monitor number.

Figure 5. Timing Commander: Reference Monitors Location

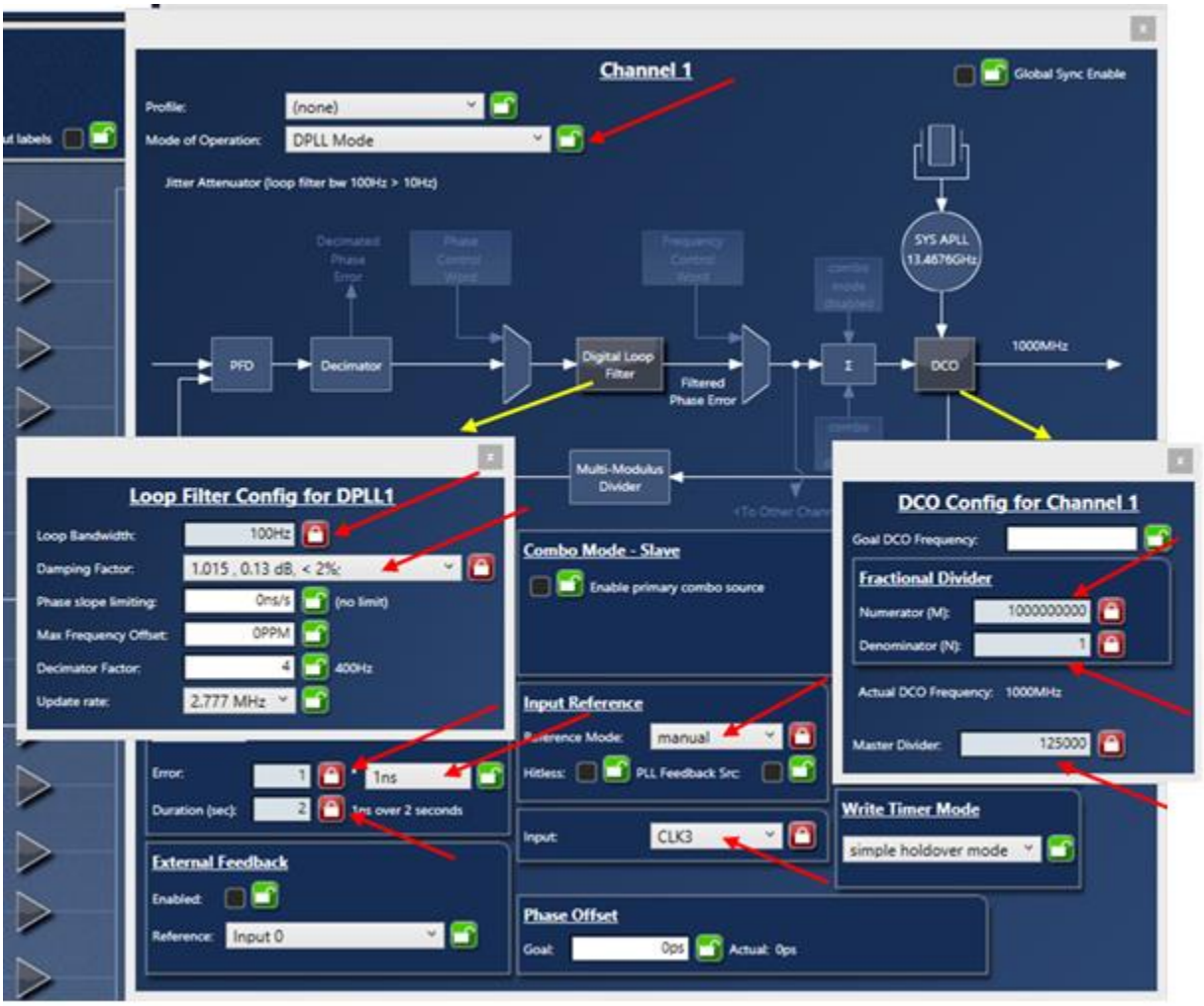
Reference Monitors are in the CLK Config by clicking the “buffer”.

4. Configure the DPLL (e.g., DPLL 1).

Any DPLL can be configured. DPLL1 is used in the example.

x = DPLL number

Figure 6. Timing Commander: Channel in DPLL Mode for Channel 1



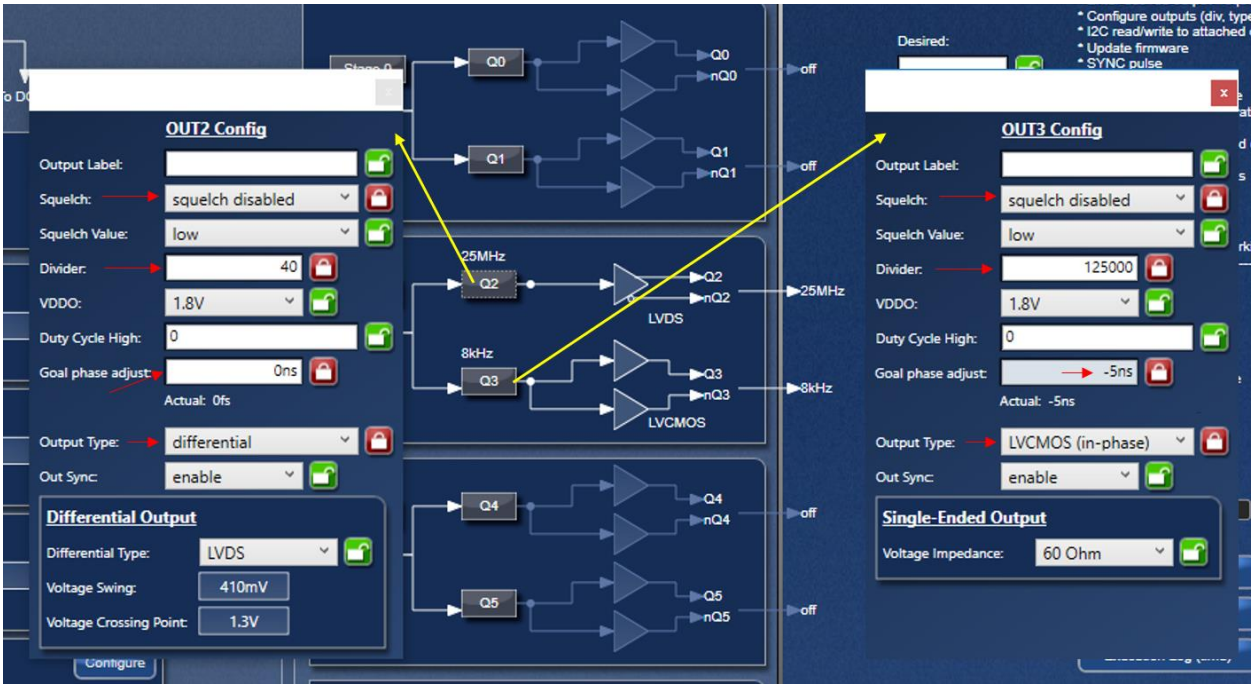
5. Configure the output to be used to send out the PPS_frames.

The outputs of the DPLL used must be configured (e.g., if DPLL 1 is used, outputs 2 and 3 must be configured). These outputs need to be connected to the input of the decoder on the other board. Differential (P and N) should be used at the output when sending PPS_frames. The PPS trigger signal must be delayed by -5ns to give the encoder enough setup time.

a. Output 2 (Q2) to transmit frames. Connect the P of this output to the P of the input configured in the decoder, and the N of this output to the N of the input configured in the decoder.

b. Output 3 (Q3) used as the PPS trigger

Figure 7. Timing Commander: Configure Outputs 2 and 3

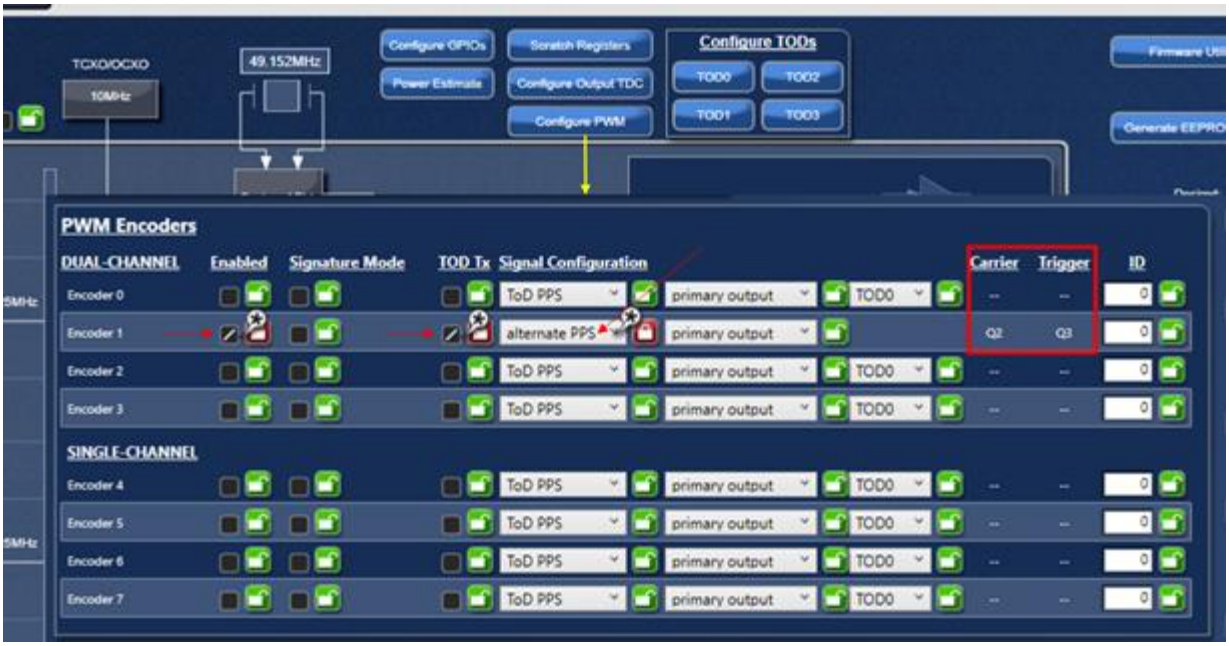


6. Configure the PWM encoder.

The encoder number must correspond to the DPLL number (e.g., encoder 1 is connected to DPLL1). Encoders[0:3] are dual-channel encoders. Encoders[4:7] are single-channel encoders. This example uses a dual-channel encoder.

The source of the PPS (i.e., what the framing data is timed off of) can be triggered either from the divided down output of the same DPLL as the carrier (i.e., synchronous source), or from the ToD accumulators (i.e., asynchronous source). The example in this document uses a synchronous source and does not use the ToD accumulators. The user enters the ToD data directly via a hardware register as described in the next section. In addition, Signature mode is not used because ToD data requires PWM_PPS.

Figure 8. Timing Commander: Configure Encoder 1



Configure Encoder 1 with DPLL1 as the source. Q2 is the carrier and Q3 is the trigger (PPS source)

7. Write directly to the PWM_TOD hardware register.

Write directly to this hardware register after the configuration and setup to transmit the ToD information.

x = Encoder number

The module address for the PWM_TOD hardware registers is not in the Programming Guide, so will be written here. Encoder 1 is used in the example.

Module address of:

PWM_ENC_0 = 0x9780
PWM_ENC_1 = 0x9800
PWM_ENC_2 = 0x9880
PWM_ENC_3 = 0x9900
PWM_ENC_4 = 0x9980
PWM_ENC_5 = 0x9A00
PWM_ENC_6 = 0x9A80
PWM_ENC_7 = 0x9B00

Offset address of PWM_TOD__0 = 0x10. There are 88 bits (11 bytes) to write.

Write to the PWM_TOD hardware register	`:reg_write(PWM_ENC_x + PWM_TOD__0, 88, 0xAABBCCDDEEFF1234567890);`

There is no GUI control for the hardware registers.

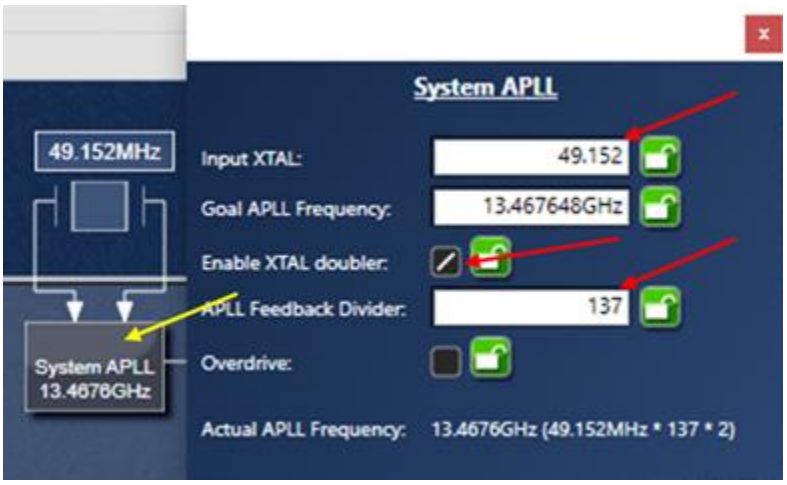
Set up the transmitter and ensure it is working properly. This happens when the DPLL is in a locked state.

3. How to Set Up Clock Matrix for PWM_PPS Framing – Receiver

The SYS_APLL, Inputs, Reference Monitors, DPLL, and Outputs of the receiver are configured similarly to the transmitter in the previous section.

1. Configure the SYS_APLL.

Figure 9. Timing Commander: System APLL

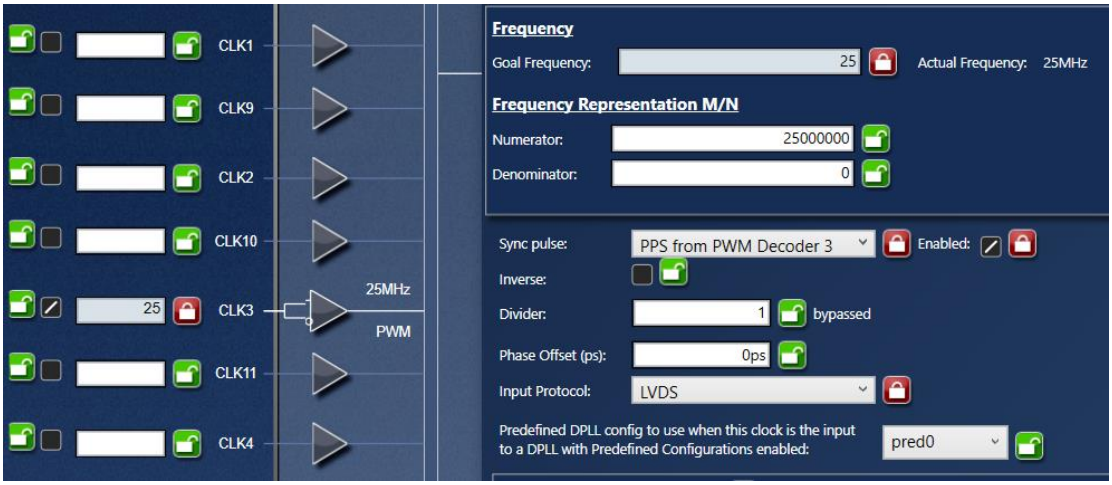


Click on the “System APLL” box and update the settings

2. Configure the input to be used to receive the PWM_PPS frames.

Connect the output transmitting the PWM_PPS frames from the transmitter of the first board to the configured input of the receiver on the second board. CLK3 is selected as the receiver input. Decoder 3 is while as the Sync Pulse Input. The decoder and clock index must match.

Figure 10. Timing Commander: CLK3 Field



Enter 25 into CLK3 field on the main menu. Click on the “Buffer” for CLK3 and select “PPS from PWM Decoder 3” as the Sync Pulse and the Enable bit. Choose “LVDS” for Input Protocol.

3. Configure the reference monitors.

x = Reference Monitor number.

Figure 11. Timing Commander: Reference Monitors Update

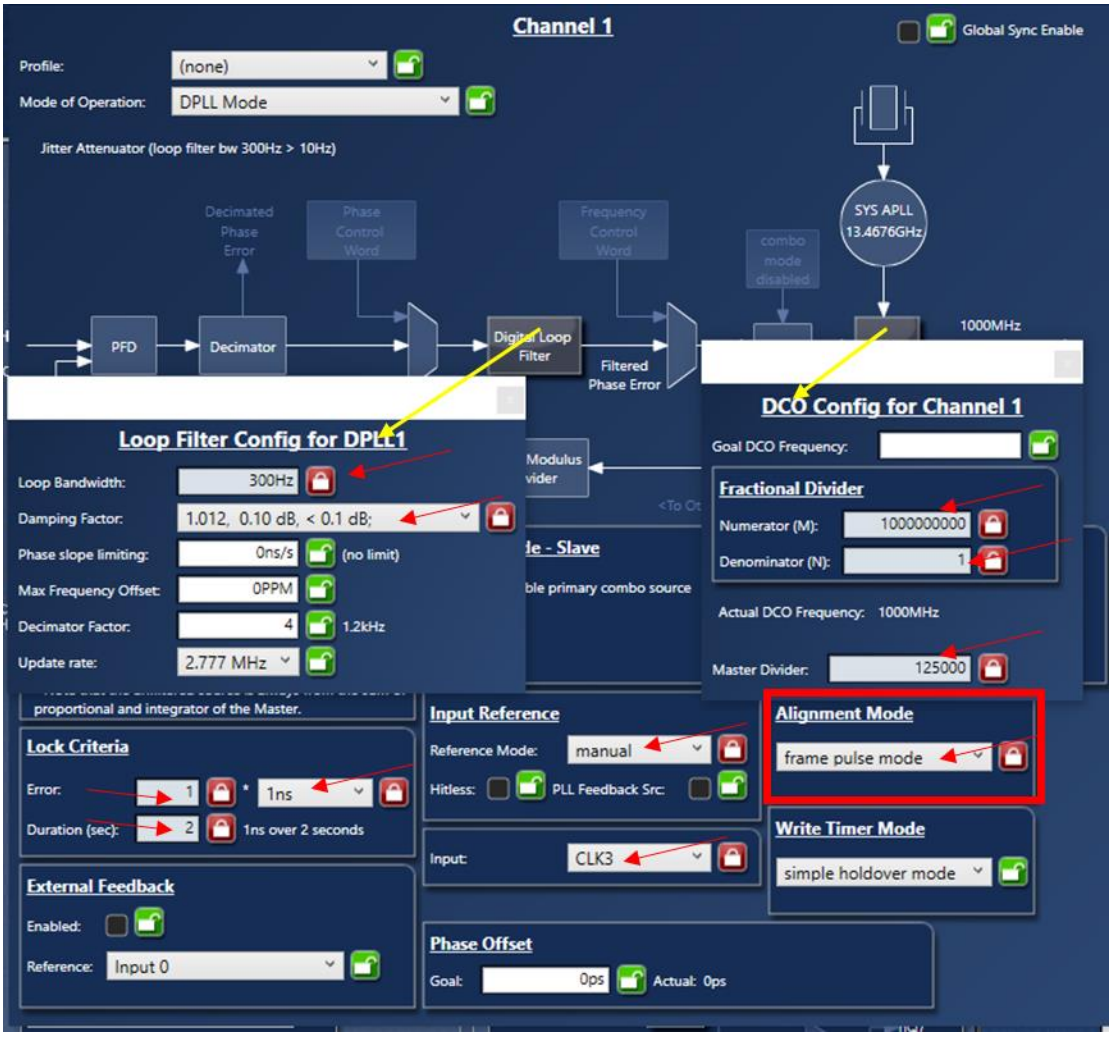
The Reference Monitors Update are in the CLK Config by clicking the “buffer”.

4. Configure the DPLL (e.g., DPLL 1).

Any DPLL can be configured. DPLL1 is used in the example.

x = DPLL number

Figure 12. Timing Commander: Channel in DPLL Mode for Channel 1



Note: When the receiver DPLL is different than the transmitter DPLL, “Alignment Mode” is selected to be “frame pulse mode”. This selection will lock the embedded PPS source at the input of the receiver to the 8kHz output at the output of the receiver.

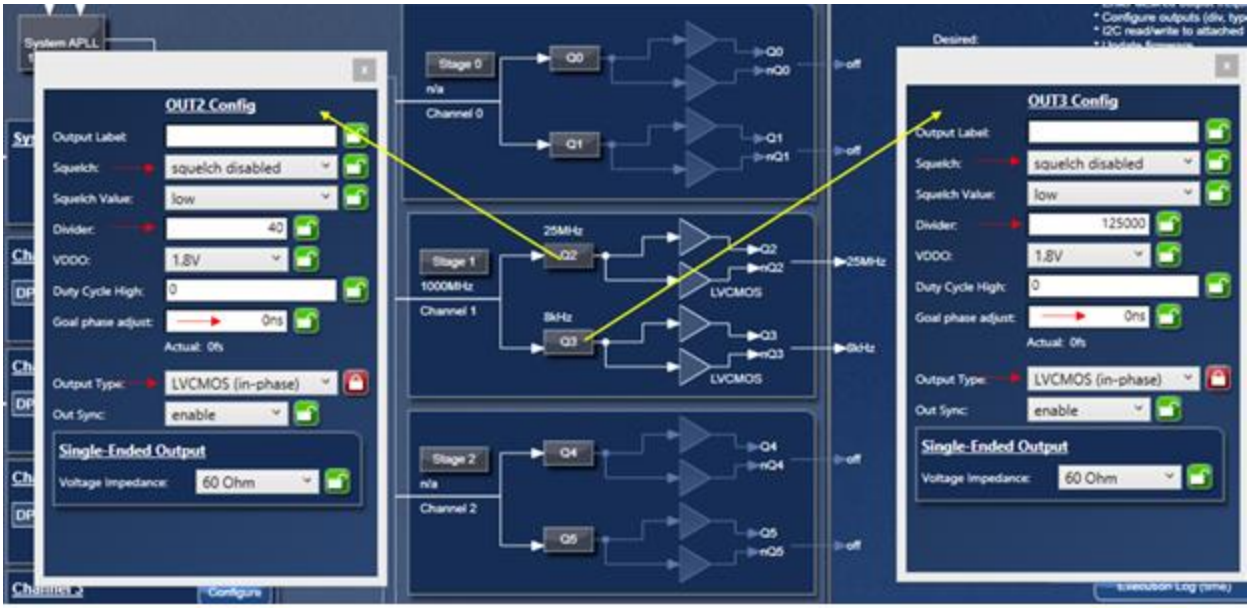
5. Configure the receiver output.

The outputs of the DPLL must be configured (e.g., DPLL 1 has outputs 2 and 3).

Output 2 shows the clock signal on which the ToD information was sent. Output 2 is not mandatory.

Output 3 is the frame pulse and is output when PWM information is received at the input of the receiver. Phase adjustments can be done to the 8kHz output frame pulse to align with the incoming frames at 8kHz at the input of the receiver on an oscilloscope. This is done to indicate when the PWM information is sent.

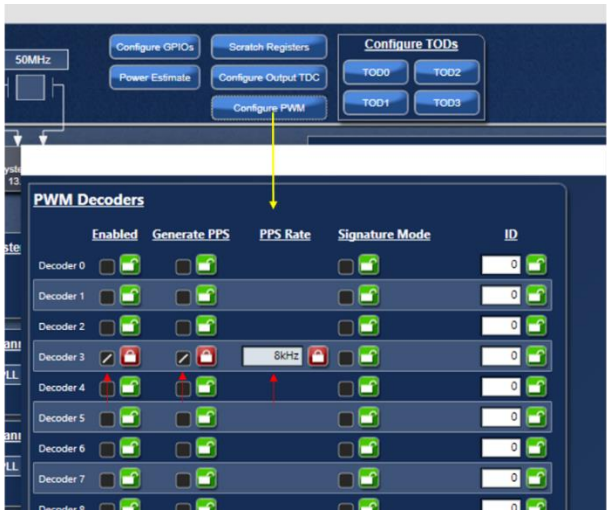
Figure 13. Timing Commander: Configure the Outputs 2 and 3

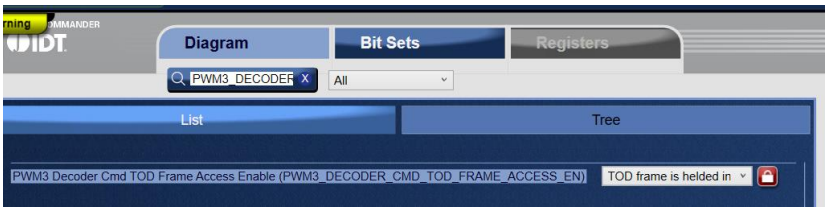


6. Configure the PWM decoder.

The decoder number must correspond to the input number (e.g., decoder 3 is connected to input 3). Decoder 3 is used to match the CLK3 input.

Figure 14. Timing Commander: Configure Decoder 3





Configure Decoder 3 to be used with CLK3 input. Switch to the Bit Sets tab and search for “PWM3_TOD”, then enable the bit.

7. Read from the PWM_FIFO hardware register.

Read from this hardware register after the configuration and setup to get the ToD information that was transmitted. This is where the transmitted PPS-frames are stored (i.e., in the PWM_FIFO). The value in the PWM_FIFO hardware registers should match the value in the PWM_TOD hardware registers.

Clock Matrix supports a procedure to read the ToD information from the FIFO. The pseudocode is as follows:

```
while True:
      while reg_read(PWM_FIFO + PWM_FIFO_STS + EMPTY, 1) & 0x01 == 0:
            reg_write(PWM_FIFO + PWM_FIFO_CTRL_0 + ENABLE_POP, 3, 0x05)
            data = reg_read(PWM_FIFO + PWM_RDATA_0_0 + RDATA, 88)
            tod_data = data & ((2 ** 88) - 1)
            print_address_and_data(PWM_FIFO + PWM_RDATA_0_0 + RDATA, tod_data))
```

The module addresses for the PWM_FIFO hardware registers are not in the Programming Guide; therefore, they are listed below for reference purposes.

Module address PWM_FIFO: 0xA380

Offset address of PWM_FIFO_CTRL_0 = 0x00

Offset address of PWM_FIFO_STS = 0x02

Offset address of PWM_RDATA_0_0 = 0x10

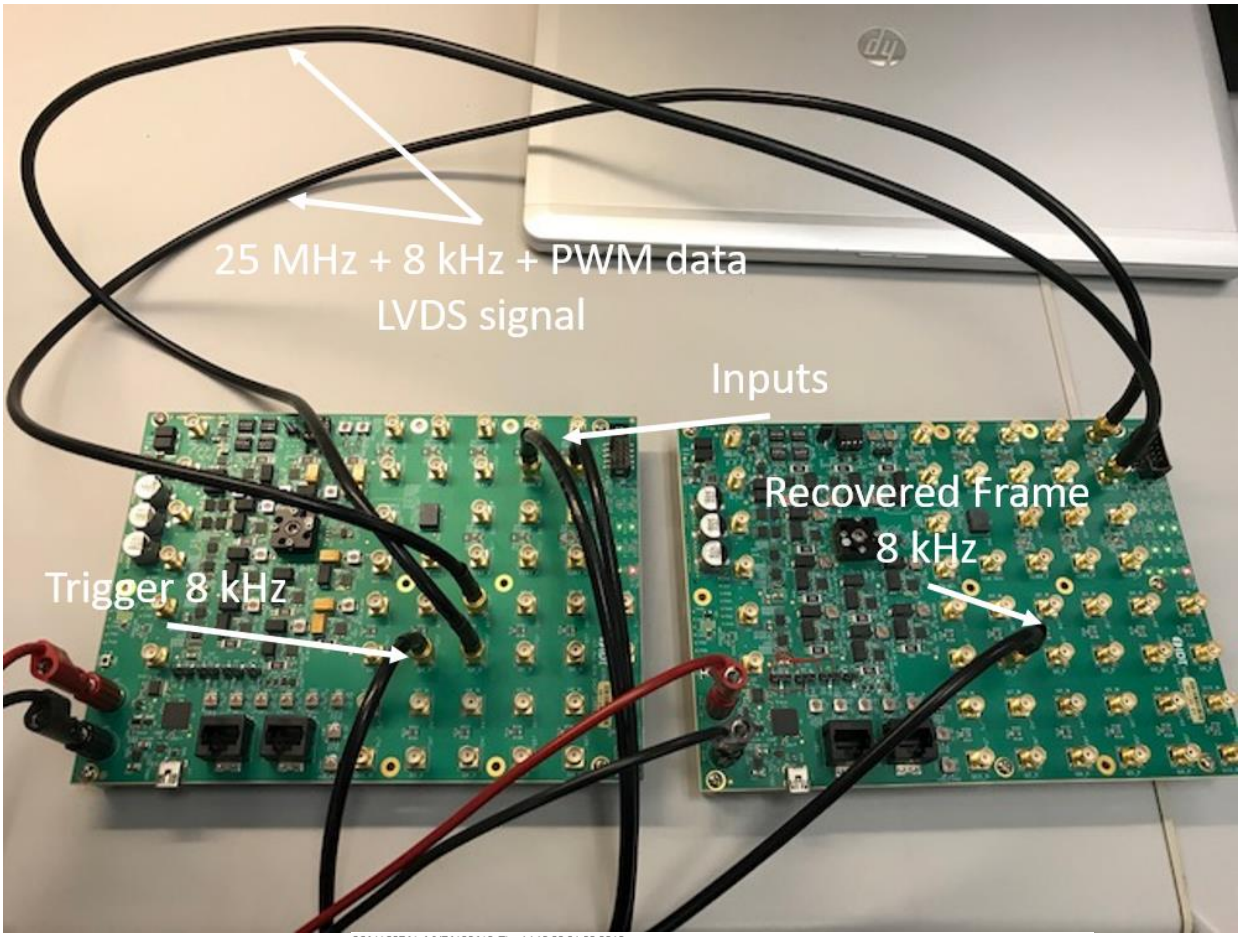
Once the FIFO is enabled and popped, the user has up to 1 second to retrieve the data from the FIFO.

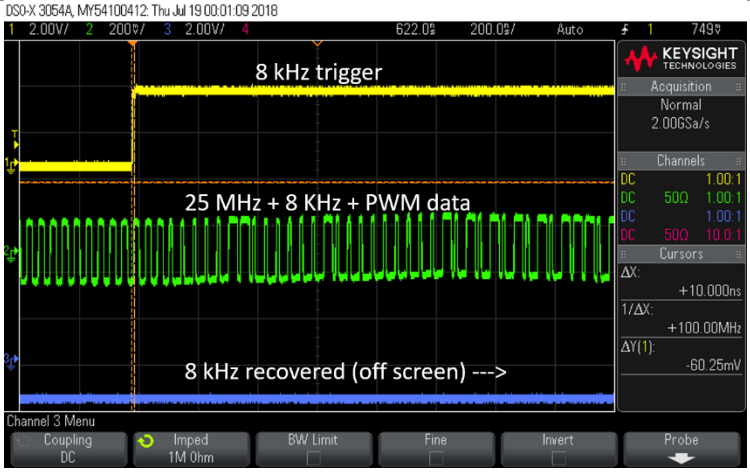
There is no GUI control for the hardware registers.

4. Lab Setup and Results

A picture of the encoder and decoder is shown below. The encoder is on the left and the decoder on the right. Scope plots are also shown in the figure. PWM ToD data is sent when the 8kHz signal is triggered on the encoder. When the decoder receives the PWM data, the data is sent to the FIFO while the DPLL can recover and lock to the 25MHz carrier and the 8kHz frame individually. Only the 8kHz frame is shown below. The same PWM data is sent every 1/(8kHz).

Figure 15. Lab Setup





5. Input Output Alignment

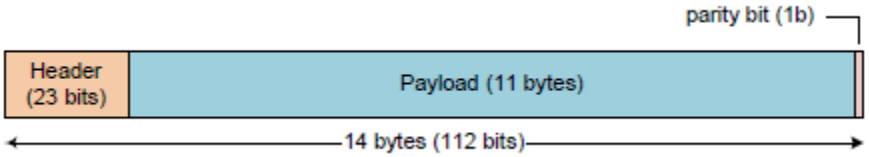
Sometimes it is useful to align the recovered 8kHz frame output of the decoder to the 8kHz frame input of the encoder. To align the edges, all of the delay cycles must be accounted for as follows:

- Encoder input to output delay = 3 cycles
- Frame pulse sampling delay = 1 cycles
- Decoder input to output delay = 2 cycles
- PWM frame length = 112 cycles
- Total delay = 118 cycles

Therefore, to align the 8kHz frame output at the output of the decoder to the 8kHz frame input at the input of the encoder, the 8kHz frame output requires negative 118 cycles of delay.

The 8kHz output frame pulse is only high after all of the PWM frame is sent. The PWM frame information is shown below and is also in the 8A3x datasheet.

Figure 16. PWM Frame



The PWM frame header is comprised of the following:

- Command Code (3 bits)
- Source Encoder ID (8 bits), defined in register SCSR_PWM_ENCODER_ID
- Broadcast (1 bit)
- Destination Decoder ID (8 bits), defined in register SCSR_PWM_DECODER_ID

6. Revision History

Revision Date	Description of Change
August 23, 2022	Eliminated pseudo-code.
December 17, 2021	Completed minor, non-technical changes.
August 14, 2018	Initial release.

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