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## 1. Introduction

The P9235A-RB Wireless Power Receiver (Tx) is an integrated circuit (IC) consisting of multiple high-power blocks and noise-sensitive circuits controlled by a microprocessor. When implementing the application circuit on a printed circuit board (PCB), there are often tradeoffs associated with managing the critical current paths. To optimize the design, place components on the circuit board based on circuit function to guarantee best performance. The thermal management of the P9235A-RB is also important to the product's performance and should be optimized when designing the PCB. Use the following guidance to place the components in order of priority based on operation.

There are three main categories of circuitry:

- Power circuits
- Sensitive circuits
- Non-sensitive circuits

### 1.1 Key Points for Optimal Layout

- Route the power connections wide and on the same side of the PCB as the P9235A-RB ( $\geq 100$  mils).
- Use the layer under the P9235A-RB side of the board as a solid ground plane.
- Connect the exposed thermal pad (EP) in the center of the P9235A-RB to all other layers with an array of 4x5 10 mil vias.
- Avoid unnecessary layer transitions of the AC power connections (LC node, LC tank driving FETs, and GND).
- Place the P9235A-RB as close as possible to the center of the board. Avoid placing it along the PCB edge.
- Connect as much copper as possible to every pin of the P9235A-RB, including pins that do not carry high current.
- Use low ESR resonance capacitors (Cs/Cd) to decrease losses in the LC and AC1 current path (COG preferred).
- Place components in the following order:
  - POWER CIRCUITS – NON H BRIDGE POWER STAGE:
    - CIN, CBOOST: Place all IC pin input voltage capacitors and boost capacitors close to their related pins ( $V_{IN}$ , LDO33, LDO18, VDDIO, BST\_BRG1, BST\_BRG2, DRV\_  $V_{IN}$ , VBRG\_IN:).
    - Buck Regulator L, Cout: Place the inductor as close as possible to the switch node pin to reduce the switching noise of that node. Place the buck regulator inductance and output capacitance such that they form the smallest possible current loop to minimize EMI transmissions.
  - SENSITIVE CIRCUITS – VOLTAGE AND CURRENT MEASUREMENT:
    - Current Sense: Place the bridge input current sense resistor directly in the current path to the tank FET drivers. Place the filtering components close to the sense resistor and tightly together.
    - Current Demodulation: Place the current demodulation circuit components tightly together and close to their related IC pins (ISNS\_OUT, IDEMI).
    - Voltage Demodulation: Place the voltage demodulation circuit components tightly together and close to their related IC pin (VDEM1).
  - POWER CIRCUITS – H BRIDGE POWER STAGE:
    - H Bridge: Place H bridge FETs (Q5, Q7) and LC tank capacitance (C44, C47, C48, C49) close to each other, to form a small current loop, to avoid EMI emissions.
    - H Bridge Cin: Place the V\_BRG FET-H-Bridge capacitors such that the traces are short. This is the large DC and AC current path.
  - SENSITIVE CIRCUITS – FET GATE DRIVER COMPONENTS:
    - Gate driver circuit: Place the Low Side FET Gate and High Side Gate Rs close to their respective pins (GH\_BRG1, 2, GL\_BRG1, 2) and connect the Output RC Snubbers directly onto their respective the H Bridge switch nodes.
    - Gate driver traces: Avoid running under the H Bridge switch nodes. Run these traces under the relatively quiet VBRG node instead. Place a ground layer between these traces and the top signal level. Surround these traces with the ground plane to provide a tight loop AC signal return path to avoid EMI noise.

## 2. Tx Power Circuits

The main power circuit of the P9235A-RB device includes the current sense resistor, the four FETs of the H bridge resonant tank driver, and the resonant tank. Secondary power circuits are the VCC5V, LDO33, and LDO18 regulators.

Figure 1. Schematic with Main Power Path (Orange) and Main (Noisy) AC Power Loops (Red)

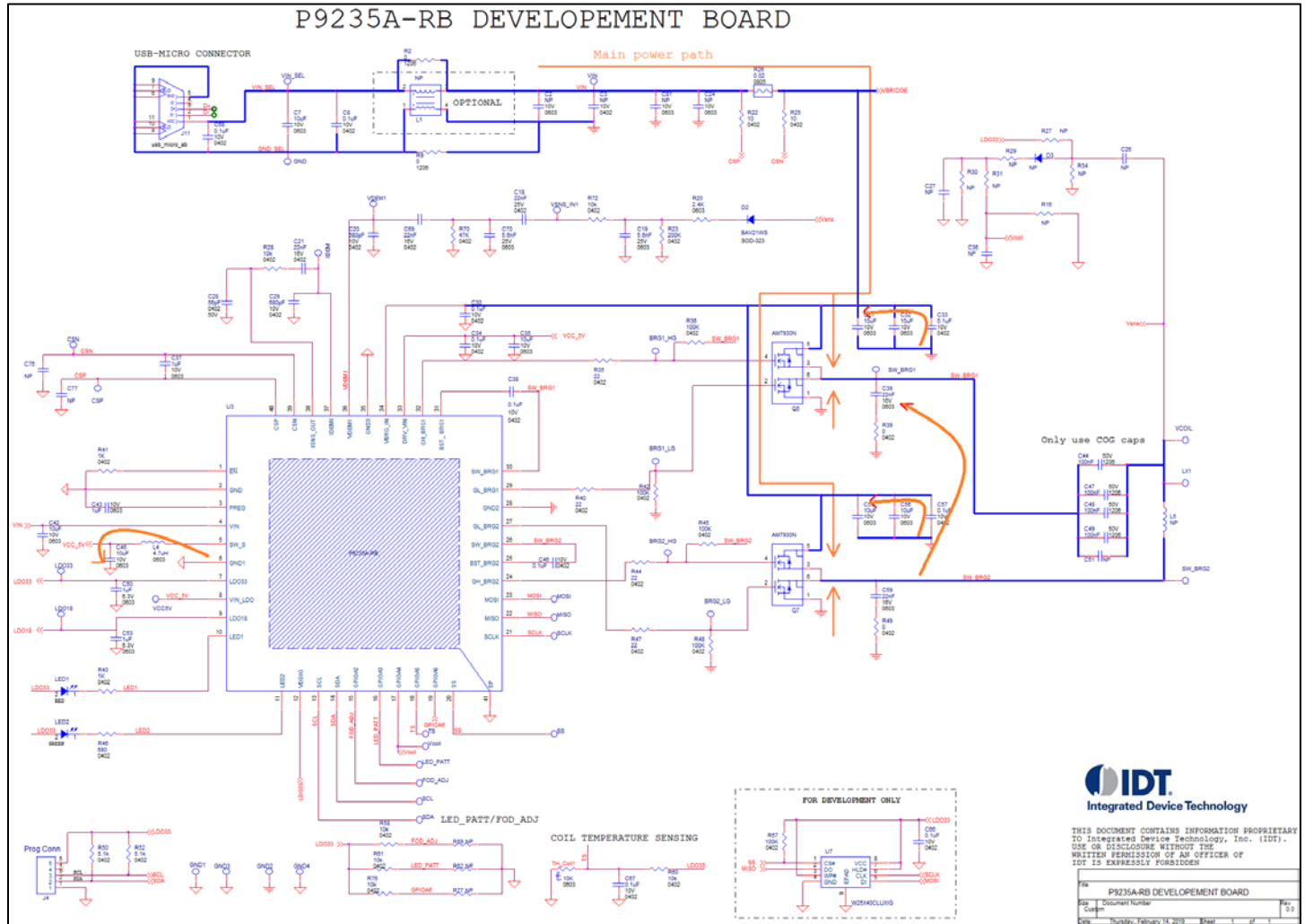
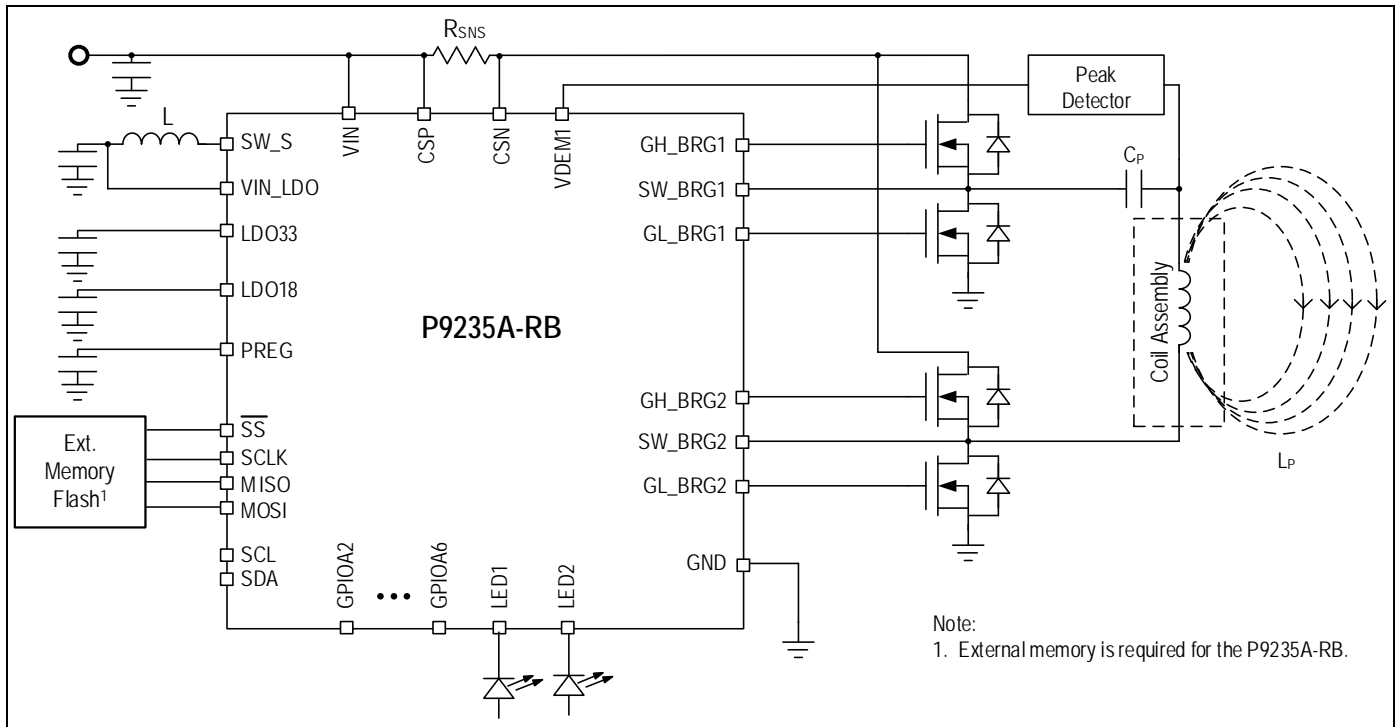
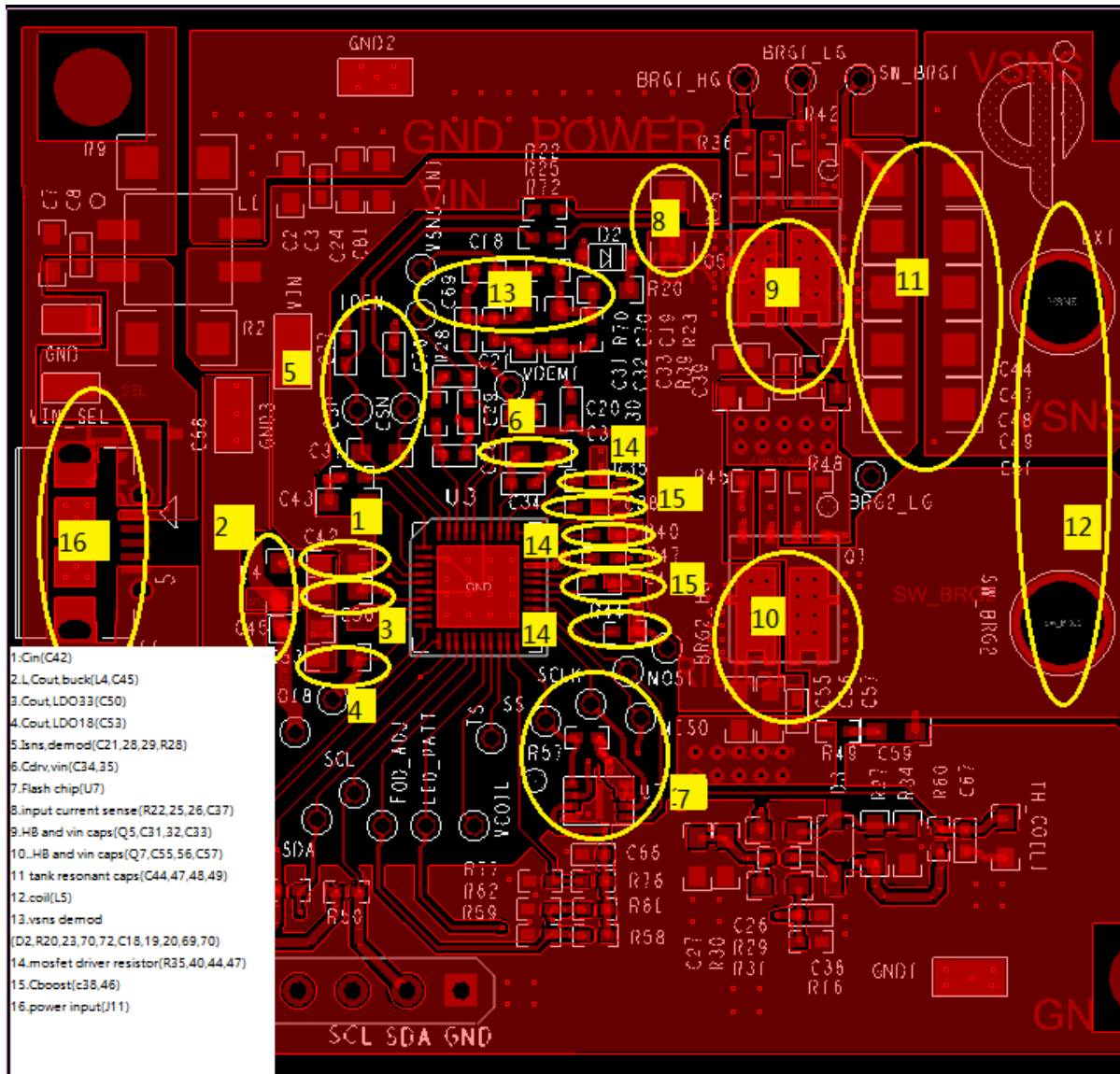


Figure 2. Recommended Orientation for the P9235A-RB and Generic Placement Guide for Select Critical Components



Recommendation: Once the final shape of the production or development PCB has been determined and the connection points for the power transfer coil ( $L_{TX}$ ) have been chosen, place the P9235A-RB on the board as close to the center of the PCB as possible, taking into consideration the mechanical requirements of the system under design. Determine its orientation based on the ability to route connections and place the required components in the following order of priority. First place the input and boost capacitors as close to their respective pins in this order of priority:  $V_{IN}$ , LDO33, LDO18, BST\_BRG1, BST\_BRG2, DRV\_VIN, and VBRG\_IN. The main power current path the connection from  $V_{IN}$  through the sense resistor ( $R_{SNS}$ ), through 1 of the two half bridge power FETs, through the tank capacitor, through the Tx coil (Coil Assembly) and out through 1 of the other half bridge power FETs. Figure 2 represents the optimal orientation of the P9235A-RB relative to the other main components. Not all necessary connections are shown in Figure 2. For a complete diagram of the recommended connections, see the schematic in Section 5. Trace widths are not to scale.

Figure 3. Actual Placement for the P9235A-RB EVK. Select Critical Components are circled in Yellow



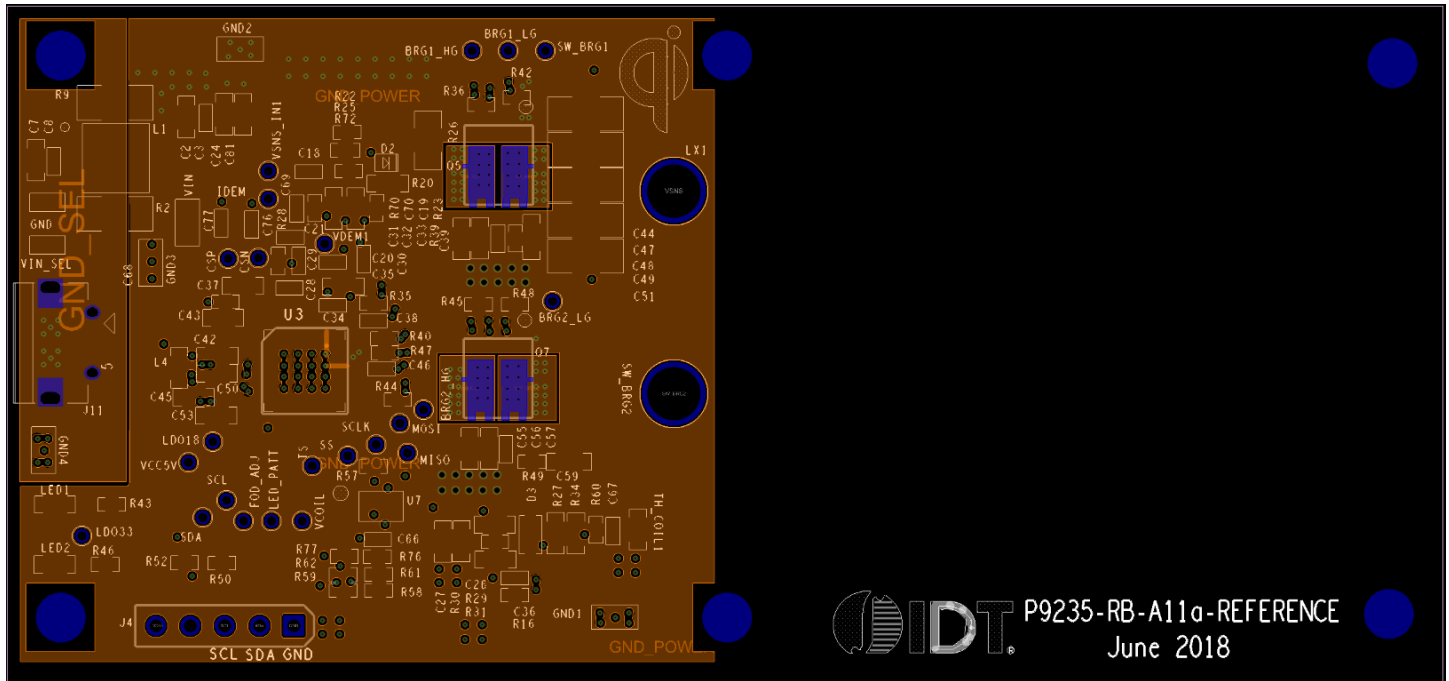
There are many things to take note of on this top layer with respect to creating an optimal layout (notes refer to the listing embedded in Figure 3):

- Closeness of  $C_{IN}$  and  $C_{boost}$  caps to their respective pins (notes 1,6,15)
- Tight (small) AC loops of FETs in relation to the LC tank (notes 9-12)
- Tight loops of the FETs in relation to the H bridge  $C_{in}$  capacitors (notes 9,10)
- Closeness of current and voltage demodulation to the IC (notes 5,13)
- Closeness of H bridge FET gate driver resistors to the IC (note 14)
- Tight loop of LC of 5V switching regulator for low loop inductance/noise (note 2)
- Closeness of L to its respective switching node for minimum noise (note 2)
- The H bridge FETs produce the most heat. Therefore, FET GND pads are connected to GND with the maximum number of 10mil vias for the best thermal performance.



- [a] Routing of the FET gate driver lines away from switching nodes as much as possible (note 1). The traces are routed under the  $V_{IN}$  and GND planes (electrically quiet areas). Also note the thick 30mil traces for the supply voltages (5V-note 2, 4; LDO33-note 5) and for the step down switching regulator's switch node (note 3). These thick traces prevent voltage drops when delivering the power, increasing reliability and efficiency.

Figure 6. P9235A-RB Physical Layout from Demo PCB of Bottom Layer  
GND Plane with Minimal Traces for Maximum Thermal Transfer



The outer layers of the PCB will be the most effective at transferring heat from the board to the ambient air or other objects. Spreading the heat into internal layers is also effective for lowering the operating temperature. Internal layers can effectively spread heat horizontally when they are not interrupted by traces and through-holes along their surface. An ideal layout will result in the entire PCB being close to the same temperature; however, to obtain this result, ensure that all board layers have planes that are continuous and in direct contact with the P9235A-RB thermal vias.

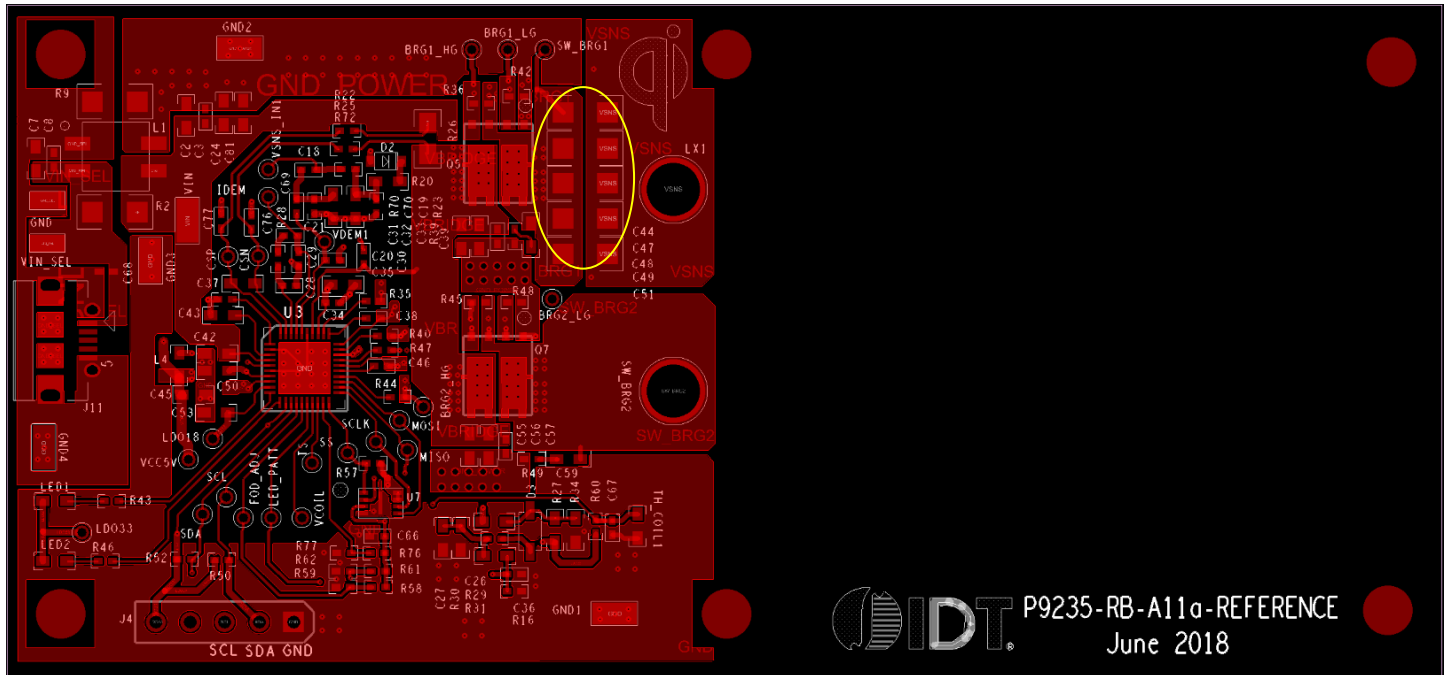
Select a single internal layer for routing most of the inner row/column pins to the rest of the PCB. The third layer is preferred for this purpose. The required nodes for connecting heat spreading planes are GND, the  $V_{IN}$  sources to the H bridge ( $V_{BRIDGE}$ , drain of  $Q_2$ ), and the switch nodes ( $VLX_1$ ,  $VLX_2$ ). The other connections will spread heat due to natural thermodynamics, but the listed nodes contact the primary heat sources of the P9235A-RB.



## 2.1 Resonance Capacitors

Next, place the resonance components. The C44, C47, C48, C49, and C51 capacitors should have wide copper planes connected to them and be in-line from the P9235A-RB to the Tx coil. COG capacitors will offer the highest performance and are recommended. X7R and X5R can be substituted, but low-ESR components should be used. Since all the load current and the current required to transmit energy to the receiver flows through the resonance capacitors, the heat developed within the resonance capacitors (Class II only) should be given opportunity to spread into large copper planes.

Figure 7. Resonance Capacitors



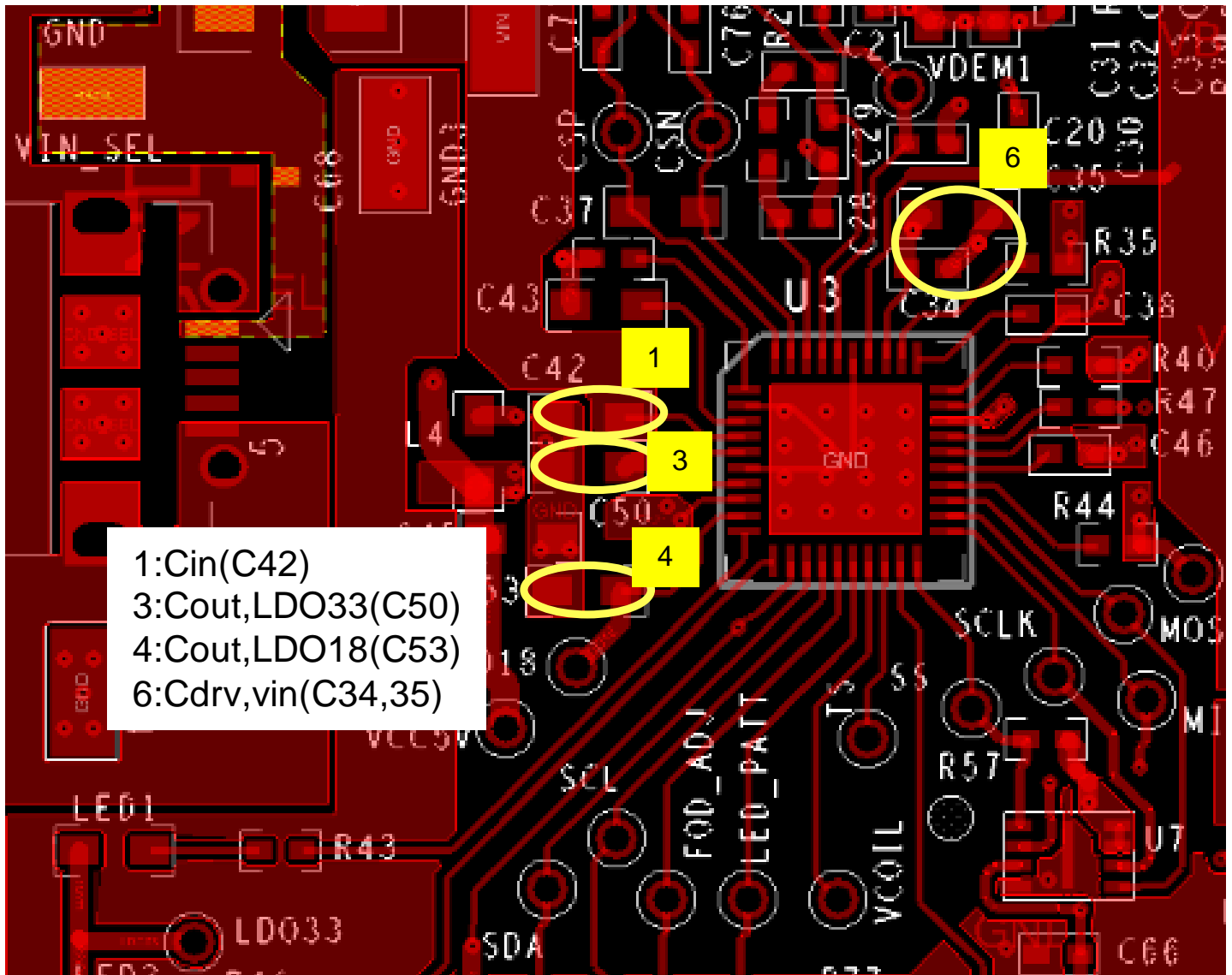
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June 2018



## 2.2 VCC5V V<sub>IN</sub>, VCC5V, LDO33, LDO18, VBRG\_IN, PE Circuit and DRV\_VIN Pin Capacitors

The VCC5V node, V<sub>IN</sub>, LDO33, LDO18, VBRG\_IN, and DRV\_VIN pin capacitors (C42, C50, C53, C34, C35) are used to stabilize internal voltage supplies used for normal operation. These capacitors must be located close to the P9235A-RB. A 10μF decoupling capacitor is recommended to be placed as close as possible to GND from the V<sub>IN</sub>, VCC5V, and DRV\_VIN nodes. A 1μF decoupling capacitor is recommended for LDO33 and LDO18 regulated output pins. A 0.1μF capacitor is also recommended in parallel with aforementioned decoupling capacitor. This will reduce the ESR of the decoupling which will reduce noise at the pin. VBRG\_IN requires a 0.1μF capacitor only.

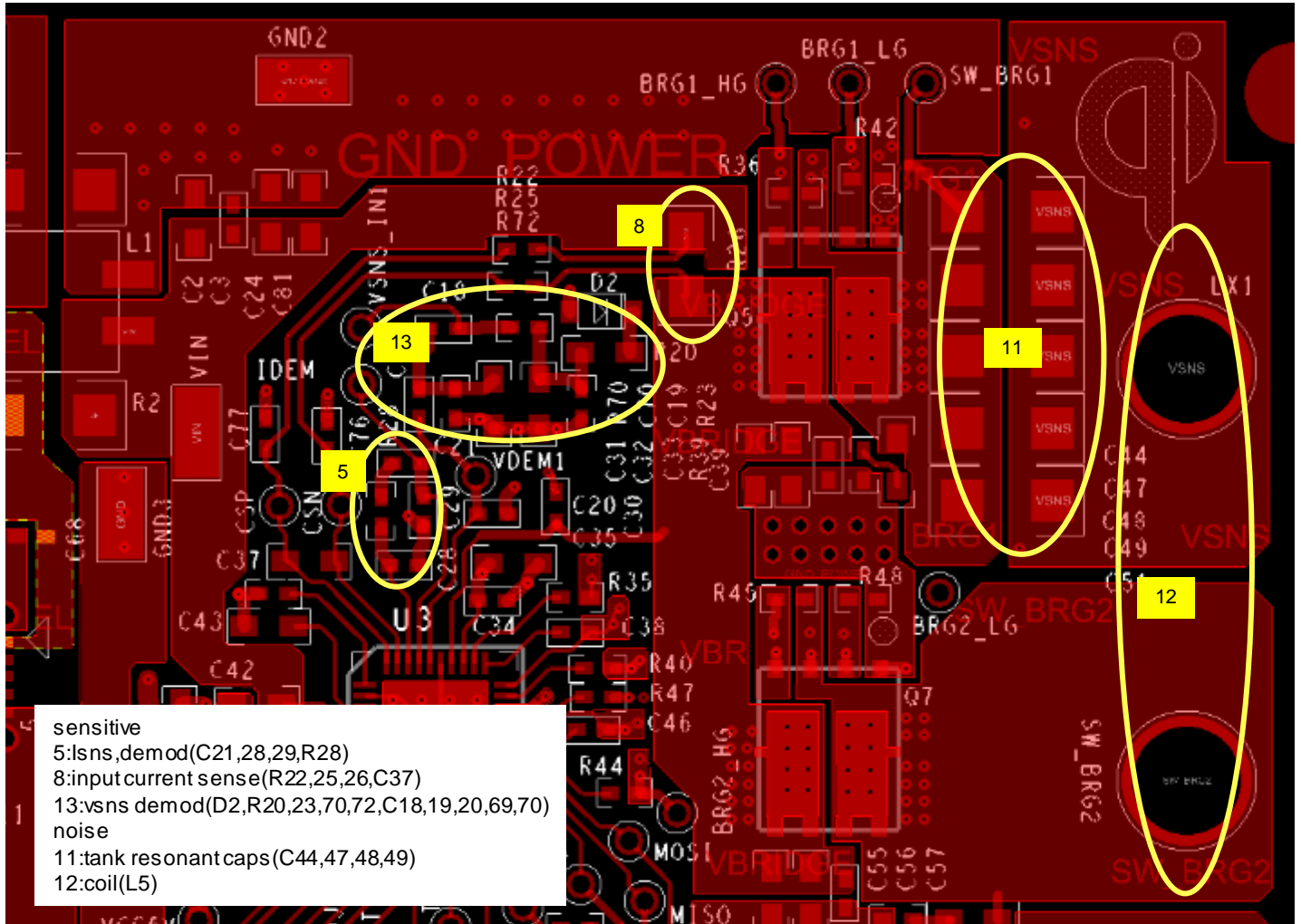
Figure 8. V<sub>IN</sub>, VCC5V, LDO33, LDO18, VBRG\_IN, and DRV\_VIN Pin Capacitors Placed Close to P9235A-RB with 0.1μF Placed Closest



### 2.3 Sensitive Circuits

The term “sensitive circuits” refers to noise-sensitive circuits that should be referenced to GND in the “quiet” ground area. AC coupling, the thermistor bypass capacitors, and other capacitors are for decoupling noise. The resonance nodes generate the highest harmonic noise, which must be filtered with decoupling capacitor. Place the current sense circuitry, the voltage demodulation circuitry, and the current demodulation circuitry, in quiet ground areas away from the resonance nodes.

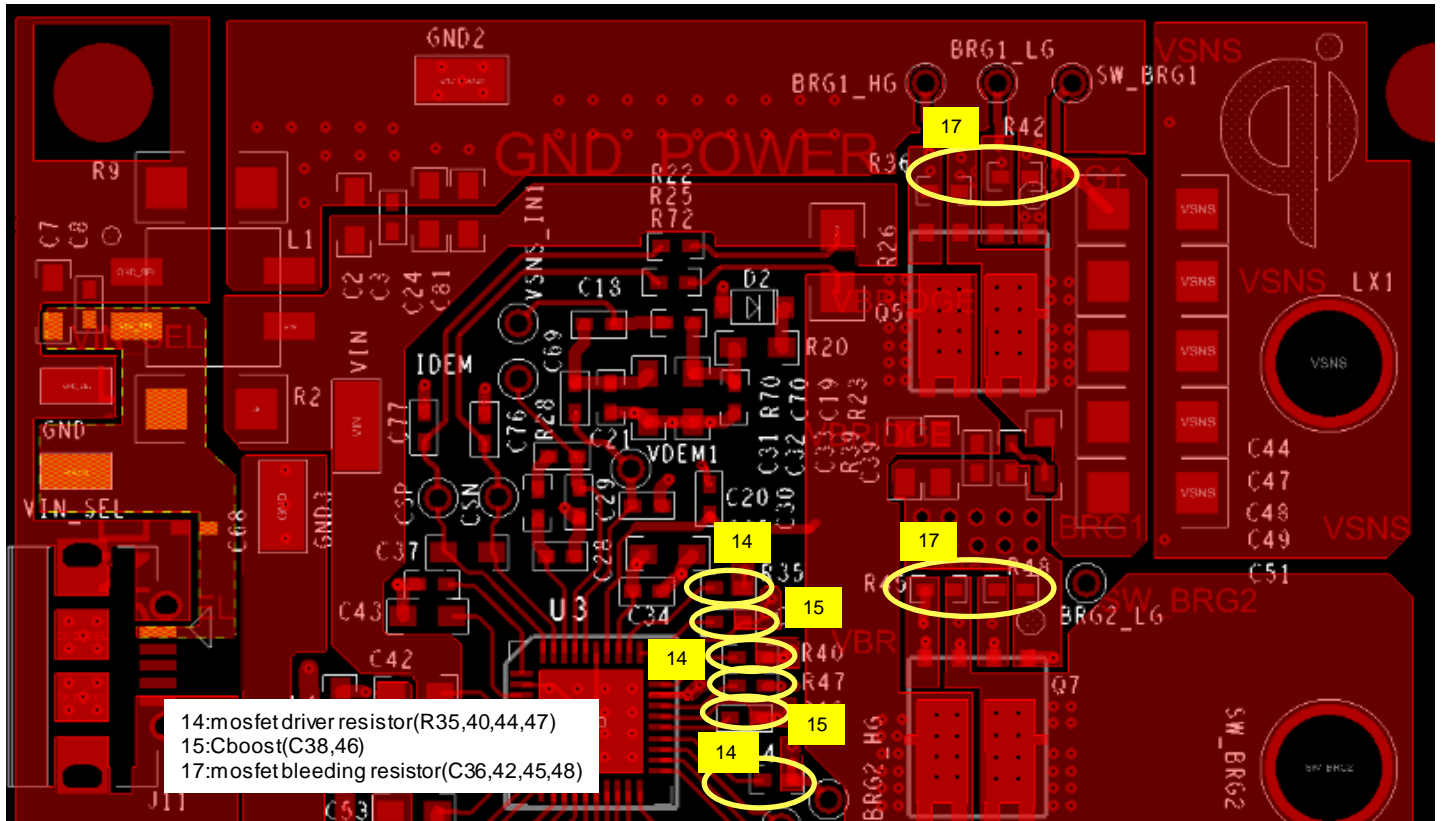
Figure 9. P9235A-RB Typical GND Noise Areas and Sensitive Circuit Placement



## 2.4 Boost Capacitors and Gate Drive Lines

Place the boost capacitors (C38, C46) close to their respective pins for maximum transfer of the capacitive energies. Place the gate driver resistors (R35, R40, R44, R47) close to their respective pins. This limits the switching noise generated. Place the FET gate bleed resistors (R36, R42, R45, R48) close to their respective FET gate pad/pin.

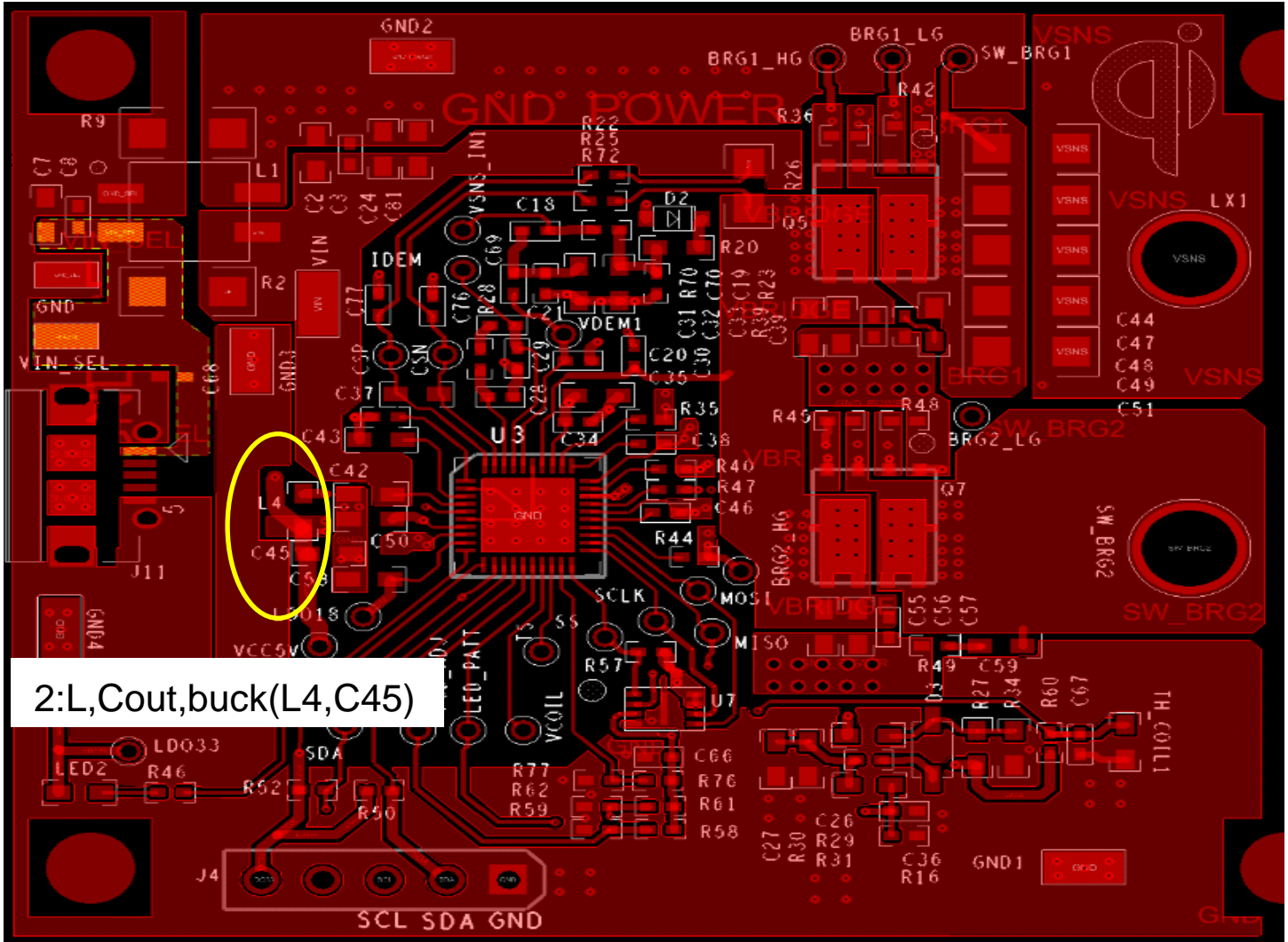
Figure 10. Boost Capacitors and Gate Drive Lines



## 2.5 5V Step Down Switching Regulator

Keep the switch node small by moving the inductor close to the switch node. This is only after placing all  $C_{IN}$  capacitors as close to their respective pins as possible. Make the  $L, C_{OUT}$  loop small to limit the loop inductance and related noise. Place the  $C_{OUT}$  such that the ground end of the capacitor is close to the nearest ground pin (pin 6).

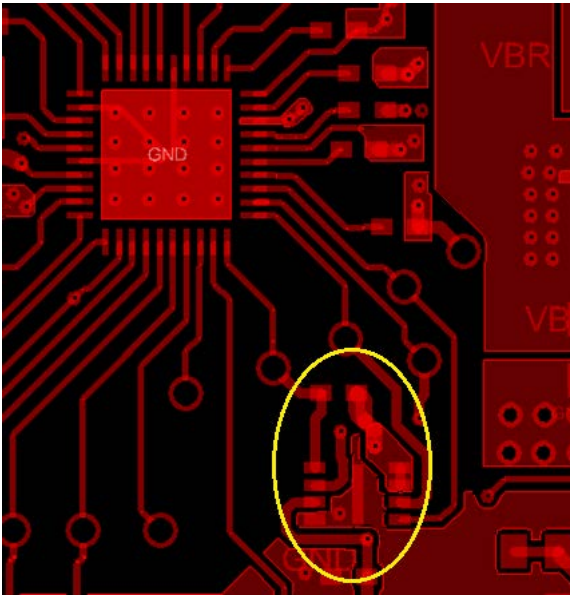
Figure 11. 5V Step Down Switching Regulator



## 2.6 Flash Circuit

In the flash programming application, P9235A-RB only contains the bootloader, the other program and data are stored into the flash. When P9235A-RB works, it will fetch the instructions or data from flash frequently. Therefore, for keeping signal integrity and minimize the EMI, it's recommended that: 1) the trace of SS, SCLK, MOSI, and MISO should be as short as possible. 2) Place the trace of SS, SCLK, MOSI, and MISO above or below the ground plane. 3) No bare pad is placed on the trace of SS, SCLK, MOSI, and MISO.

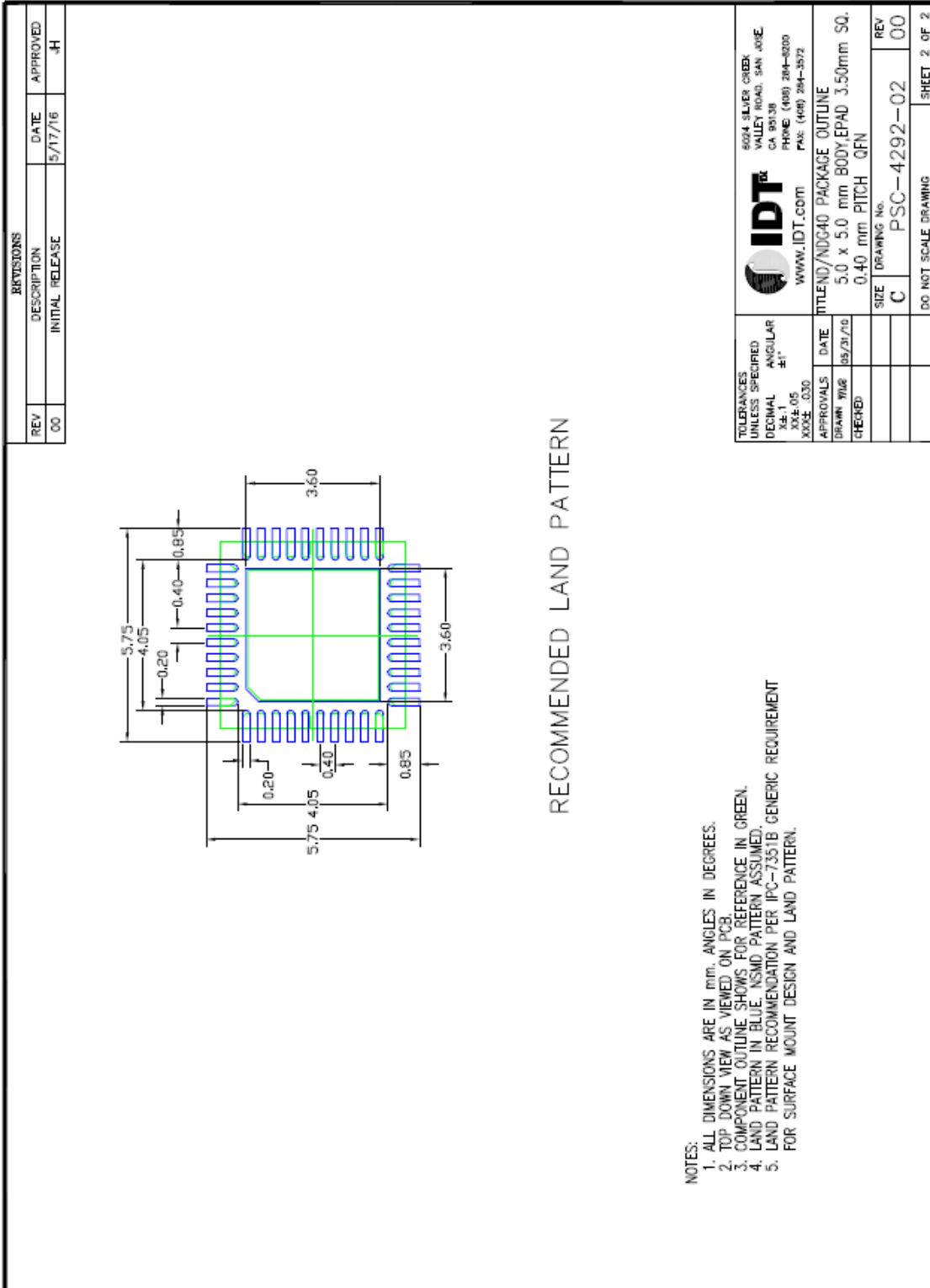
Figure 12. Flash Circuit



### 3. PCB Footprint Design

The P9235A-RB package is a fine-pitch 40-VFQFN device.

Figure 13. P9235A-RB Recommended PCB Land Pattern Drawing



## 4. Audible Noise Suppression

Wireless power receiver solutions have been observed to produce audible noise. If sound is detected, there are several steps that can be taken to reduce or eliminate the noise. The first priority is identifying the source (i.e., the rectifier capacitors, the Tx coil ferrite, communication capacitors). Typically, the rectifier capacitors are the components that generate the audible noise. The reason the noise is present and associated with the rectifier capacitors is due to the WPC communication signals being generated in the audible frequency range and the use of small-form factor ceramic capacitors. The noise occurs due to the piezoelectric effect of ceramic capacitors. The capacitors constrict and expand while providing the communication pulses, and this noise is amplified as it flexes the PCB.

The primary solution to this issue is to use low-acoustic noise capacitors. Alternatively, higher voltage rated components can have superior piezoelectric properties that can reduce the audible noise. Additionally, placing the capacitors on both sides of the PCB (directly above and below each other) counters the piezoelectric forces applied to the PCB (cancels the force by each capacitor). Another method is to add slots through the PCB on both outer sides of the capacitors or directly under each capacitor. One additional approach is to place additional lower capacitance value components in parallel to reduce the mechanical force of the piezoelectric effect per component.

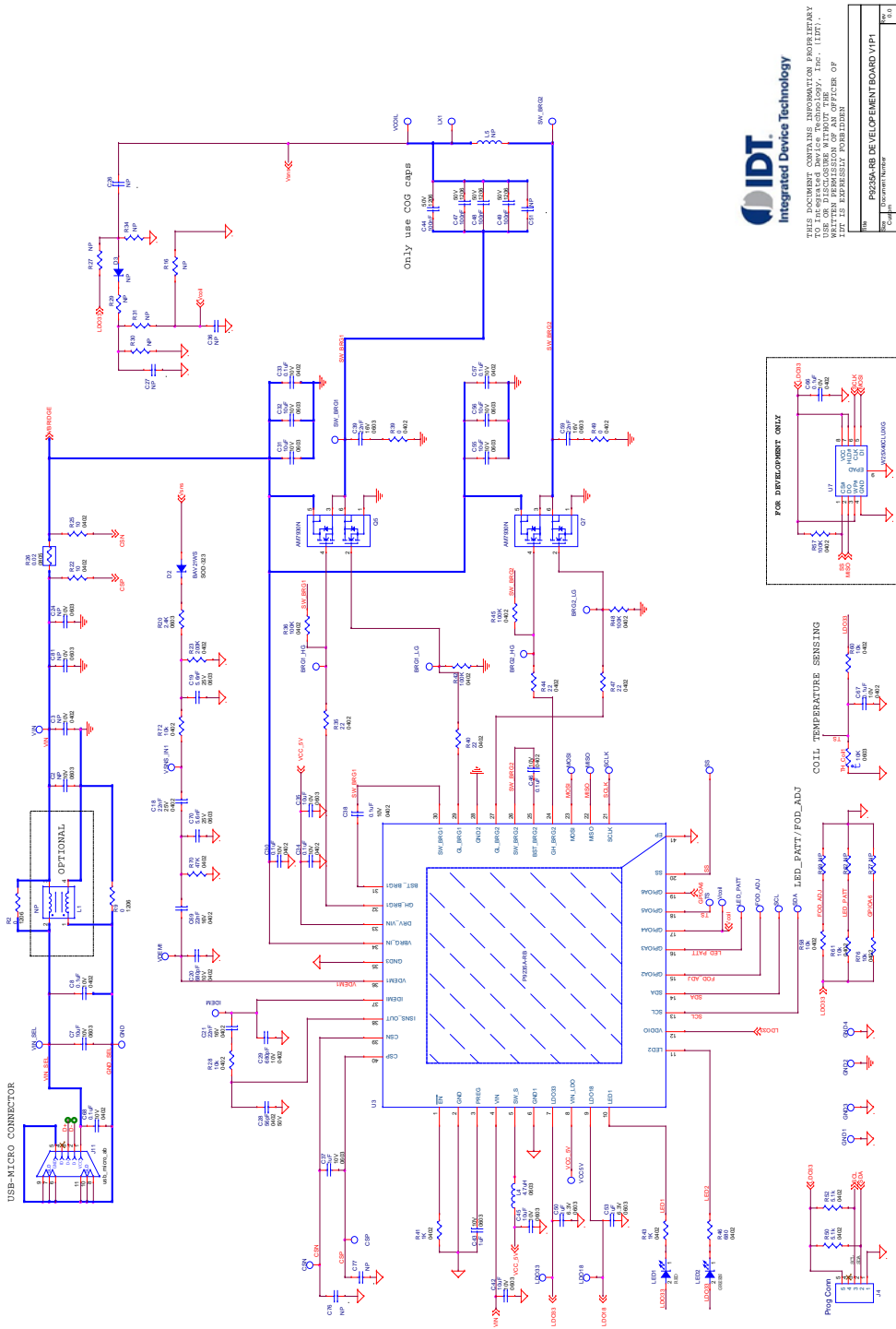
For any additional questions, contact IDT technical support (see last page for contact information).



# 5. Schematics, Bill of Materials (BOM), and Board Layout

Figure 14. Application Schematic

P9235A-RB DEVELOPEMENT BOARD V1P1



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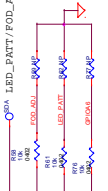
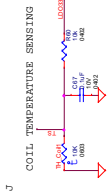
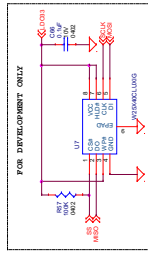


Table 1. Application Board Bill of Materials (BOM)

Item	Quantity	Reference	Part	Description	Part Number	PCB Footprint
1	8	C7,C31,C32,C35, C42,C45,C55,C56	10 $\mu$ F	CAP CER 10 $\mu$ F 10V X5R 0603	GRM188R61A106KE69D	603
2	10	C8,C30,C33,C34, C38,C46,C57,C66, C67,C68	0.1 $\mu$ F	CAP CER 0.1 $\mu$ F 10V X7R 0402	GRM155R71A104KA01D	402
3	1	C18	22nF	CAP CER 0.022 $\mu$ F 25V X5R 0402	GCM155R71E223KA55J	402
4	2	C19,C70	5.6nF	CAP CER 5600pF 25V X7R 0603	GRM188R71E562KA01D	603
5	2	C20,C29	680pF	CAP CER 680pF 10V X7R 0402	8.85012E+11	402
6	2	C21,C69	22nF	CAP CER 0.022 $\mu$ F 16V X5R 0402	GRM155R61C223KA01D	402
7	1	C28	56pF	CAP CER 56pF 50V C0G/NP0 0402	GRM1555C1H560FA01D	402
8	2	C37,C43	1 $\mu$ F	CAP CER 1 $\mu$ F 10V X5R 0603	GRM188R61A105KA61D	603
9	2	C39,C59	47nF	CAP CER 0.047 $\mu$ F 16V X7R 0603	GRM188R71C473KA01D	603
10	4	C44,C47,C48,C49	100nF	CAP CER 0.1 $\mu$ F 50V C0G/NP0 1206	GRM31C5C1H104JA01L	1206
11	2	C50,C53	1 $\mu$ F	CAP CER 1 $\mu$ F 6.3V X5R 0603	GRM188R61A105KA61D	603
12	1	D2	BAV21 WS	DIODE GEN PURP 200V 200MA SOD323	BAV21WS-7-F	SOD-323
13	7	GND1,GND2,GND3, GND4,VIN_SEL, VIN,GND	TP	TEST POINT PC MINIATURE SMT	5015	test_pt_sm _135x70
14	1	J4	Prog Conn	BERGSTIK II .100" SR STRAIGHT	68000-105HLF	sip5
15	1	J11	5P	CON 005 F RA OTH PC NLK SRW 800 MINIUSB	90080004	usb_micro _ab
16	1	LED1	LED	LED RED CLEAR 0603 SMD	150060RS75000	603
17	1	LED2	LED	LED GREEN CLEAR 0603 SMD	150060GS75000	603
18	1	L4	4.7 $\mu$ H	FIXED IND 4.7 $\mu$ H 620MA 550 MOHM	LQM18PN4R7MFRL	603
19	1	L5	NP			
20	2	Q5,Q7	AM793 0N	Dual N-Channel 30-V (D-S) MOSFET	AM7930N	DFN-5X6- 8Ld-N1
21	2	R2,R9	0	RES SMD 0 $\Omega$ JUMPER 1/4W 1206	RC1206JR-070RL	1206
22	1	R20	2.4K	RES SMD 2.4k $\Omega$ 1% 1/10W 0603	RC0603FR-072K4L	603
23	2	R22,R25	10	RES SMD 10 $\Omega$ 0.5% 1/16W 0402	RT0402DRE0710RL	402
24	1	R23	200K	RES SMD 200k $\Omega$ 1% 1/10W 0402	ERJ-2RKF2003X	402
25	1	R26	0.02	RES 0.02 $\Omega$ 1% 1/8W 0805	PF0805FRM7P0R02L	805
26	6	R28,R58,R60,R6, R72,R76	10k	RES SMD 10k $\Omega$ 1% 1/16W 0402	RC0402FR-0710KL	402

Item	Quantity	Reference	Part	Description	Part Number	PCB Footprint
27	4	R35,R40,R44,R47	22	RES SMD 22Ω 1% 1/10W 0402	RC1005F220CS	402
28	5	R36,R42,R45,R48, R57	100K	RES SMD 100kΩ 1% 1/16W 0402	RC0402FR-07100KL	402
29	2	R39,R49	0	RES SMD 0Ω JUMPER 1/16W 0402	RC0402JR-070RP	402
30	2	R41,R43	1K	RES SMD 1kΩ 5% 1/16W 0402	RC0402JR-071KL	402
31	1	R46	680	RES SMD 680Ω 5% 1/16W 0402	RC0402JR-07680RL	402
32	2	R50,R52	5.1k	RES SMD 5.1kΩ 5% 1/16W 0402	RC0402JR-075K1L	402
33	1	R70	47K	RES SMD 47kΩ 1% 1/16W 0402	RC0402FR-0747KL	402
34	1	TH_Coil1	10K	NTC THERMISTOR 10kΩ 1% 0603	ERT-J1VG103FA	603
35	1	U3	P9235 A-RB	IC wireless power transmitter	P9235A-RB	qfn40_5x5 _N
36	1	U7	W25X4 0CLUX IG	IC FLASH 4MBIT 104MHZ 8USON	W25X40CLUXIG TR	uson_2x3_ 8LD

Figure 15. Silkscreen – Top of Board

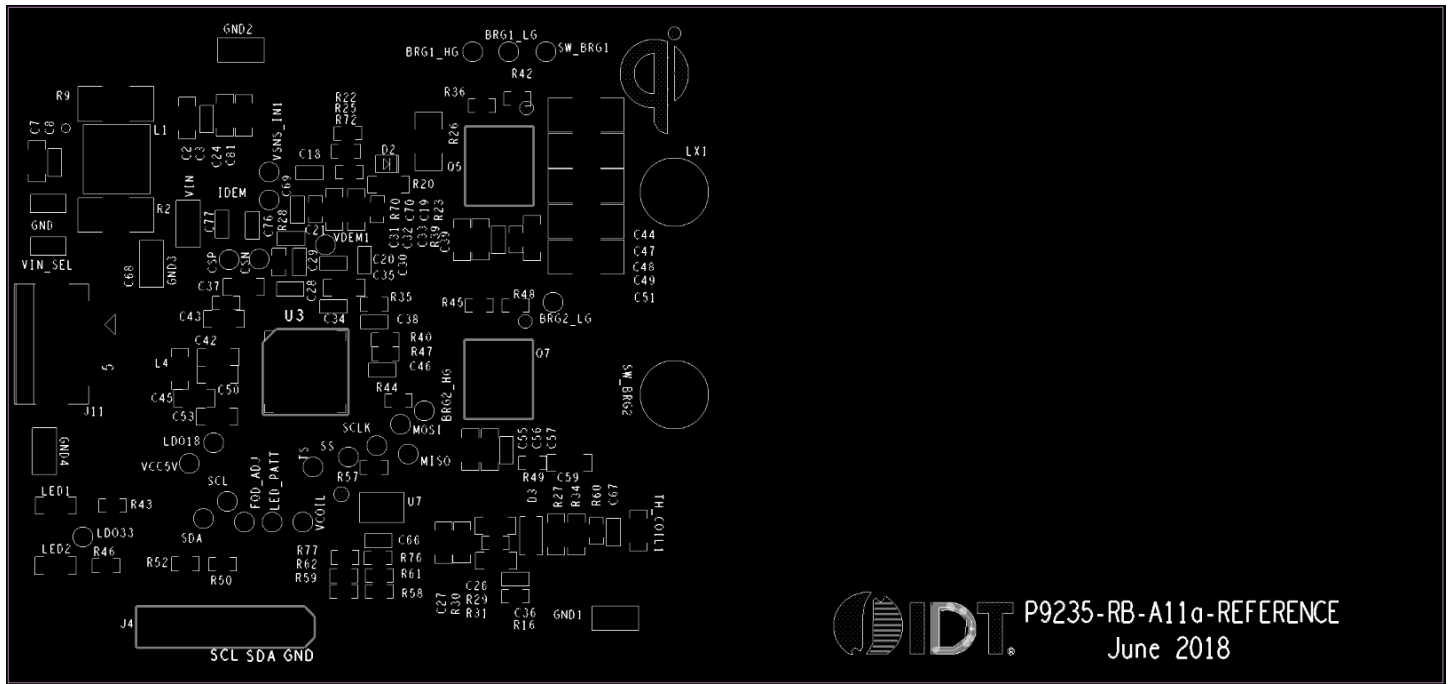


Figure 16. Copper – Top Layer

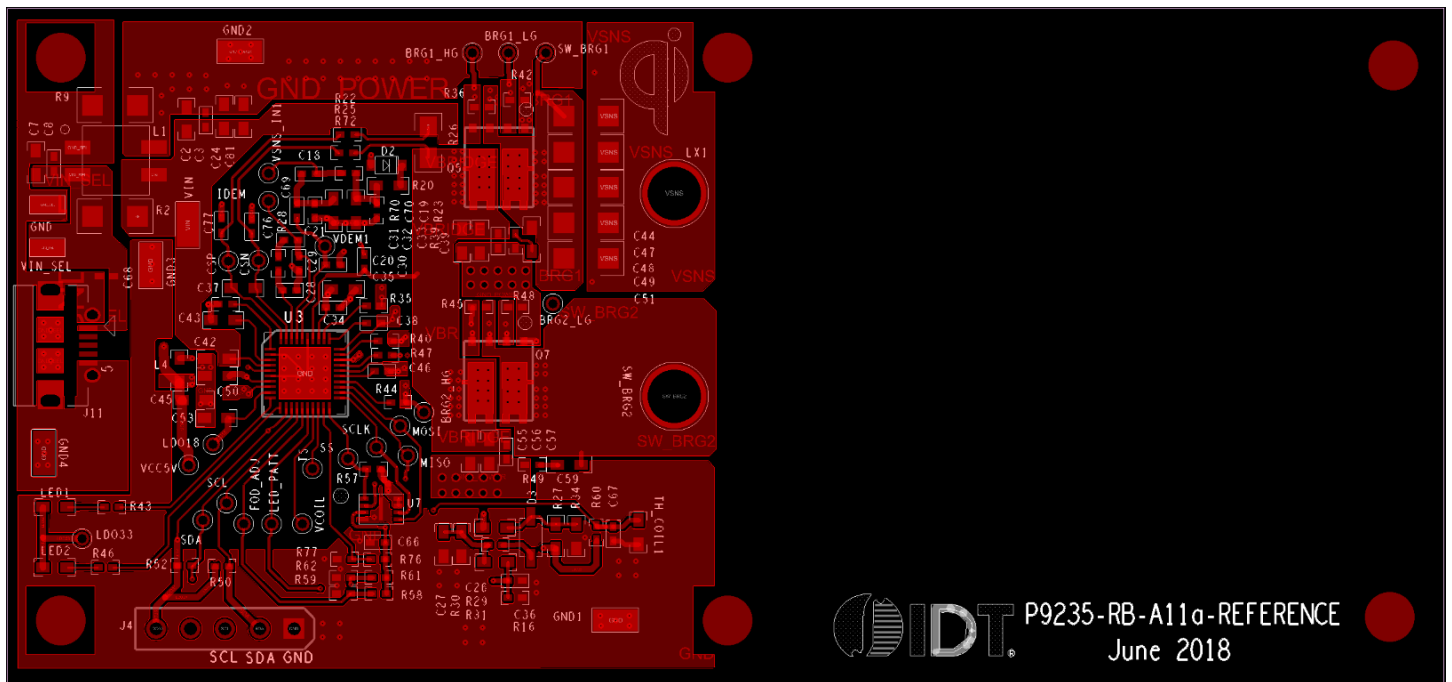


Figure 17. Copper L1 Layer

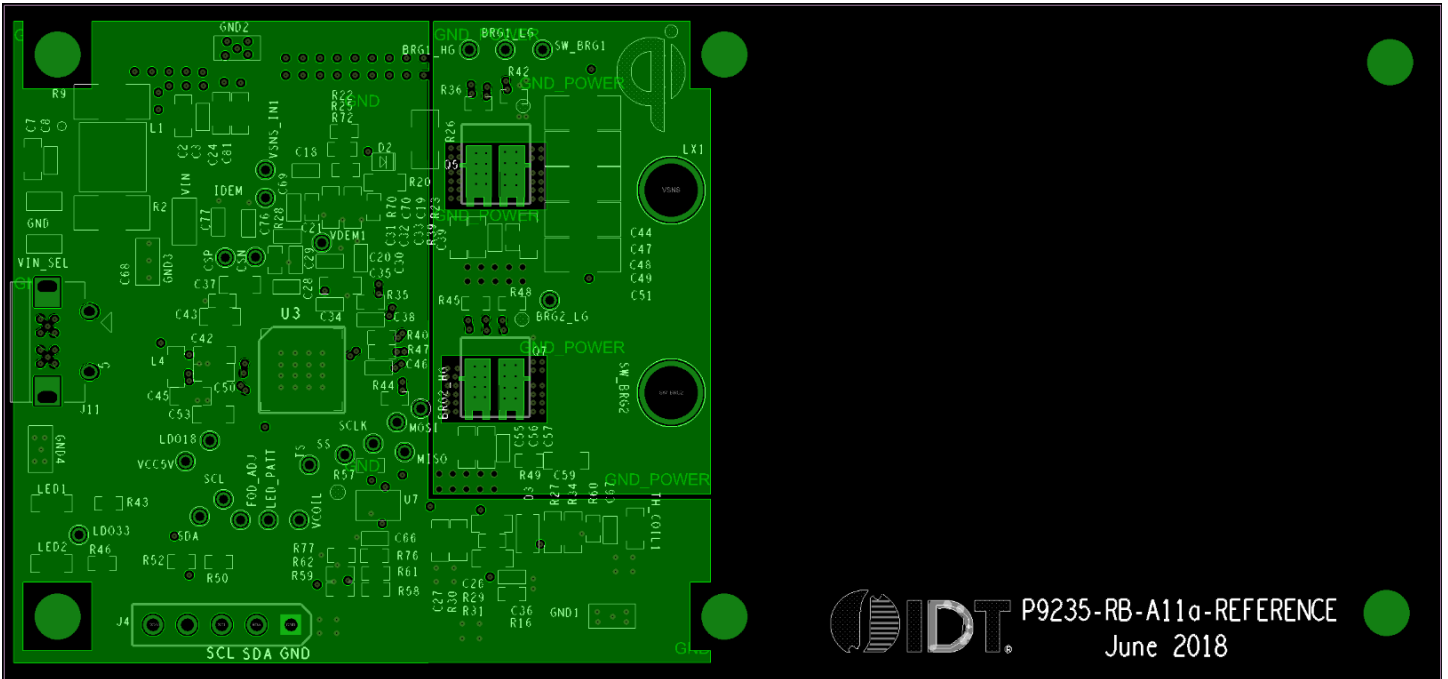


Figure 18. Copper L2 Layer

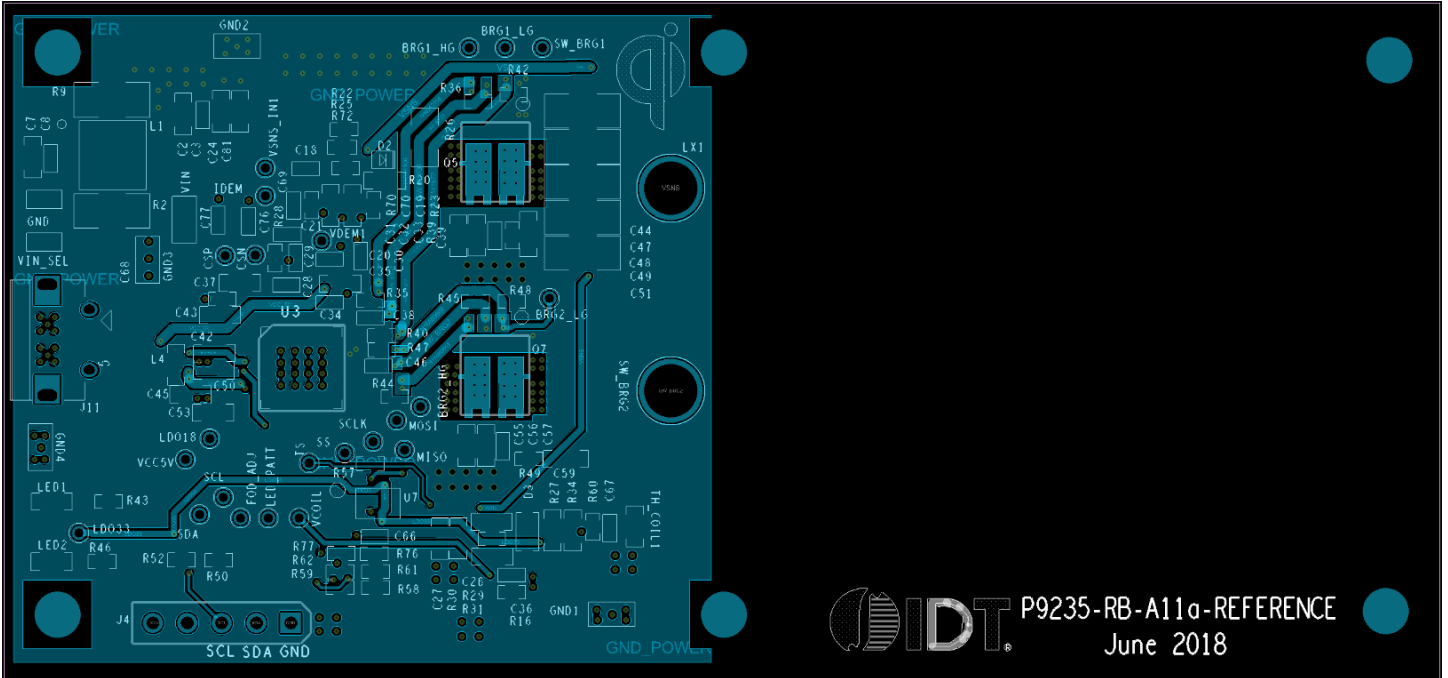
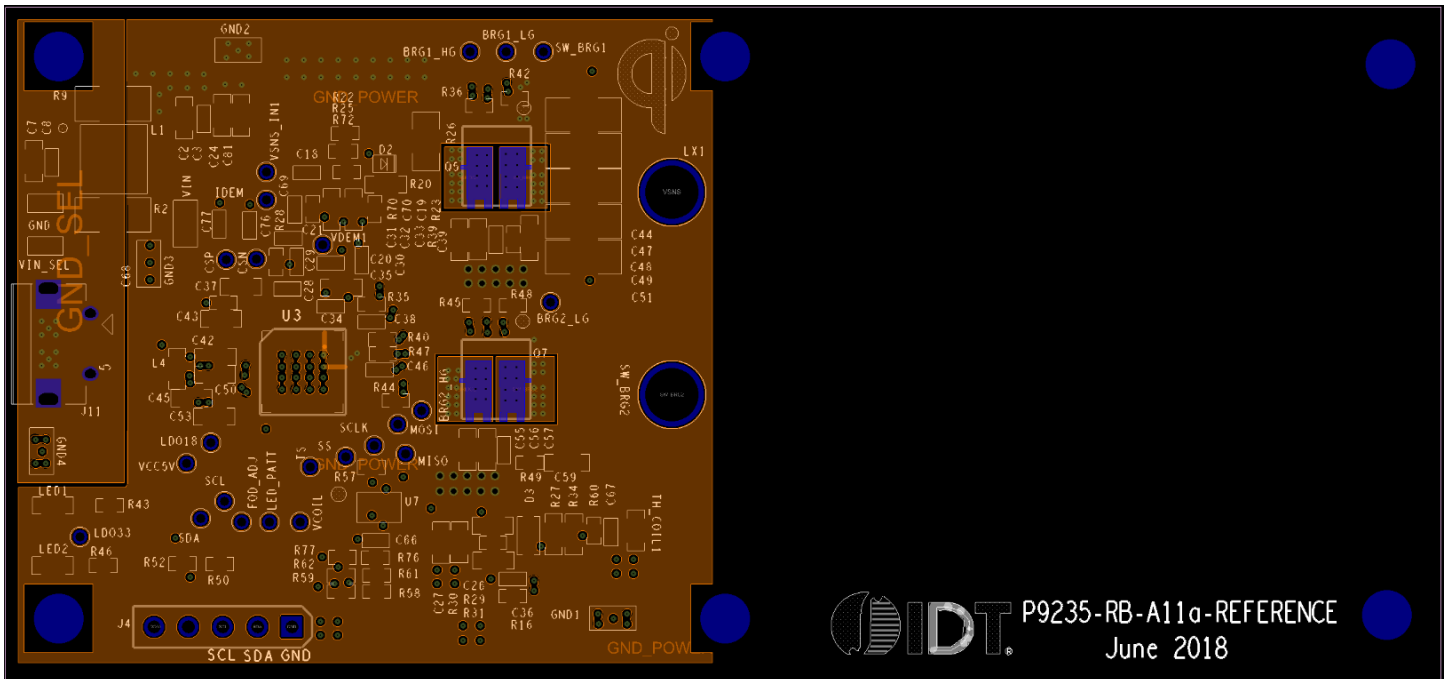


Figure 19. Copper Bottom



## 6. Revision History

Revision Date	Description of Change
March 19, 2019	Initial release.



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