RENESAS

RAJ240047

Integrated Li-ION Battery Management IC for 2-4 Series Cell

1. Introduction

1.1 Features

Fully integrated battery management product including battery capacity measurement and protection.

Supports 2-4 Li-Ion or Li-Polymer battery cells in series.

Ultra-low power Renesas RL78 CPU core

Built-in flash memory (block erase/write protection)

- Flash ROM: 128KB
- Data flash: 4 KB

Internal SRAM: 5.5 KB

Current integrating circuit (18-bit $\Delta\Sigma$A/D)

15-bit $\Delta\Sigma$A/D converter (external 3 channels, internal 5 channels including simple temperature sensor)

High side N-ch FET control circuit for charge and discharge current protection

Overcurrent detection circuit (discharge short-circuit current (2 channels), charge/discharge overcurrent, and wake-up current)

Battery voltage detection circuit (4 cells)

Battery cell conditioning circuit (4 cells)

Pack+ terminal voltage detection circuit

FUSE control circuit

MCU built-in high speed on-chip clock generator

AFE on-chip oscillator clock (4.194 MHz)

MCU runaway detection circuit

MCU build-in watchdog timer

Series regulator (VREG2: 3.3 V, VREG1: 1.8 V)

Reset circuit (VREG2, VREG1 monitoring)

MCU low power modes : HALT and STOP

High speed on-chip clock oscillator

- High speed operation :1 to 32 MHz
- Low speed operation :1 to 8 MHz

I/O port: 12

- CMOS input/output: 6
- CMOS input: 2
- N-ch open drain: 2
- High voltage input: 1
- High voltage output: 1

Serial interface:

- I2C
- UART
- Simplified I2C

MCU 16-bit timer: 5 channels

MCU 12-bit interval timer: 1 channel

AFE timer (setting range: 125 ms to 64 s)

8 bits PWM signal generator

Intel® Dynamic Battery Power Technology support

Impedance measurement circuit

Built-in on-chip debug function

Self programming function support

Power supply voltage: VCC = 4.0 to 25 V

Operation ambient temperature: Ta = -20 to +85°C

Package Information:

Plastic mold QFN (4mm x 4mm x 0.95mm)

1.2 Applications

- Notebook PC, Tablet PC, Docking Station
- Handheld measurement equipment, POS system
- UPS, Power bank

1.3 Description

RAJ240047 is Renesas battery management IC which incorporates a variety of battery fuel gauge features. Embedded Renesas RL78 CPU core has multiple low power modes and achieve high performance in ultra-low power operation. This product consists of MCU device and AFE device in a single package. Fuel gauge control firmware is stored in embedded flash memory and controls embedded analog and digital circuits to execute battery voltage / current / temperature measurement, remaining capacity estimation, over current / voltage / temperature protection and other battery management operations.

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2.   Pin Assignment

2.1   Pin Assignment Diagram

Package : 32 pin plastic mold QFN (4.0 x 4.0)

(Top View)
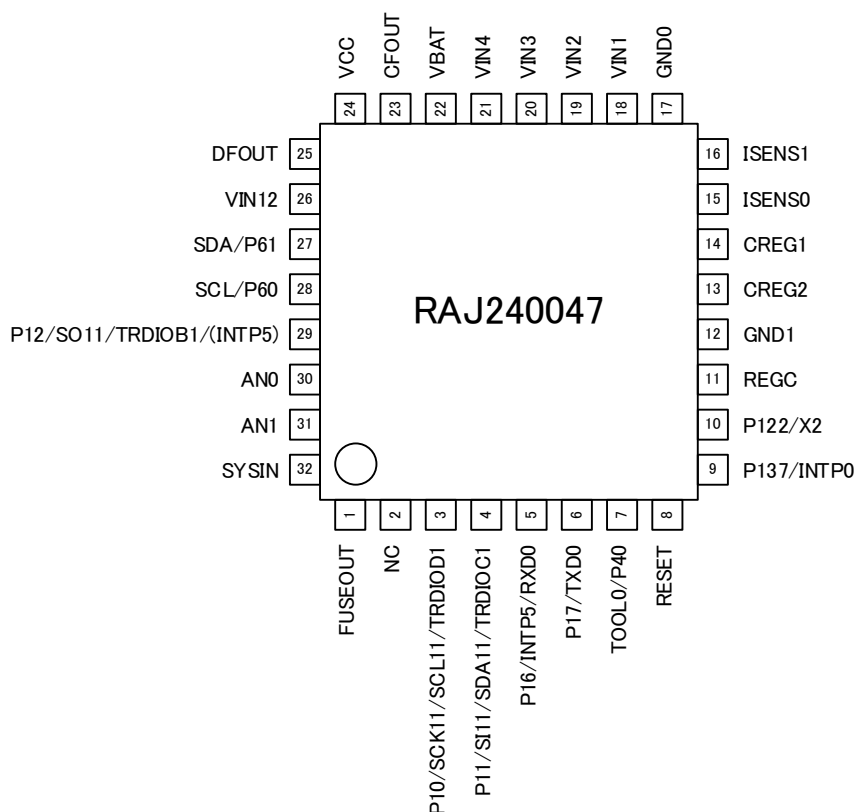
Caution 1. REGC pin connects to GND1 pin through a capacitor (0.47 to 1μF)
Caution 2. CREG1 pin connects to GND0 pin through a capacitor (1 μF).
Caution 3. CREG2 pin connects to GND1 pin through a capacitor (2.2 μF).
Remark 1. Pin function refers to [2.2Pin Function Table].
Remark 2. The function shown above in ( ) is assigned by setting of peripheral I/O re-direction register 0 (PIOR0).

2.2   Pin Function Table

(1/1)

No.	Name	Type	Description
1	DFOUT	HVO	Discharge FET control
2	NC	NC	No connect
3	P10/SCK11/SCL11/TRDIOD1	DIO (5-AN)	Port 10 Leave open in output mode if not used.
4	P11/SI11/SDA11/TRDIOC1	DIO (8R)	Port 11 Leave open in output mode if not used.
5	P16/INTP5/RXD0	DIO (5-BC)	Port 16 Leave open in output mode if not used.
6	P17/TXD0	DIO (5-BC)	Port 17 Leave open in output mode if not used.
7	TOOL0/P40	DIO (8-R)	Data Input/Output for tools
8	$\overline{RESET}$	DIN (2)	Reset Input
9	P137/INTP0	DIN (2)	Port 137 Connect to GND1 through a resistor if not used.
10	P122/X2	DIN (37-C)	Port 122 Connect to GND1 through a resistor if not used.
11	REGC	P	Regulator capacitor connection
12	GND1	P	Ground
13	CREG2	P	Regulator capacitor connection
14	CREG1	P	Regulator capacitor connection
15	ISENS0	AIN	Analog input for current integration circuit
16	ISENS1	AIN	Analog input for current integration circuit
17	GND0	P	Ground
18	VIN1	AIN	Battery voltage input
19	VIN2	AIN	Battery voltage input
20	VIN3	AIN	Battery voltage input
21	VIN4	AIN	Battery voltage input
22	VBAT	AIN	Battery voltage input
23	CFOUT	HVO	Charge FET control
24	VCC	P	Power supply
25	DFOUT	HVO	Discharge FET control
26	VIN12	AIN	Charger connection monitoring
27	SDA/P61	DIO	I2C Bus data I/O Input/Output
28	SCL/P60	DIO	I2C Bus data I/O Input/Output
29	P12/SO11/TRDIOB1/(INTP5)	DIO (5-BB)	Port 12 Leave open in output mode if not used.
30	AN0	AIN	Analog Input
31	AN1	AIN	Analog Input
32	SYSIN	HVIN	System detection pin

HVO	high voltage output	**P**	power
HVIN	high voltage input	**DIO**	digital I/O
HVIO	high voltage input/output	**DIN**	digital input
		AIN	analog input

2.3   Pin Equivalent Diagram

DIO (Type 5-BB)	DIO (Type 5-AN)

DIO (Type 5-BC)	DIO (Type 8-R)

DIN (Type 2)	DIN (Type 37-C)

Schmitt-triggered input with histeresis characteristics

External oscillation circuit:can not be used with this product.

VCC	VBAT, CFOUT
CREG1	**CREG2**
AN0 / AN1	**ISENSE0 / ISENSE1**
DIO (Type 13-R)	**SCL / SDA (AFE)**

RESET (AFE)	FUSEOUT

SYSIN	

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VIN1, VIN2, VIN3, VIN4

VIN12, DFOUT
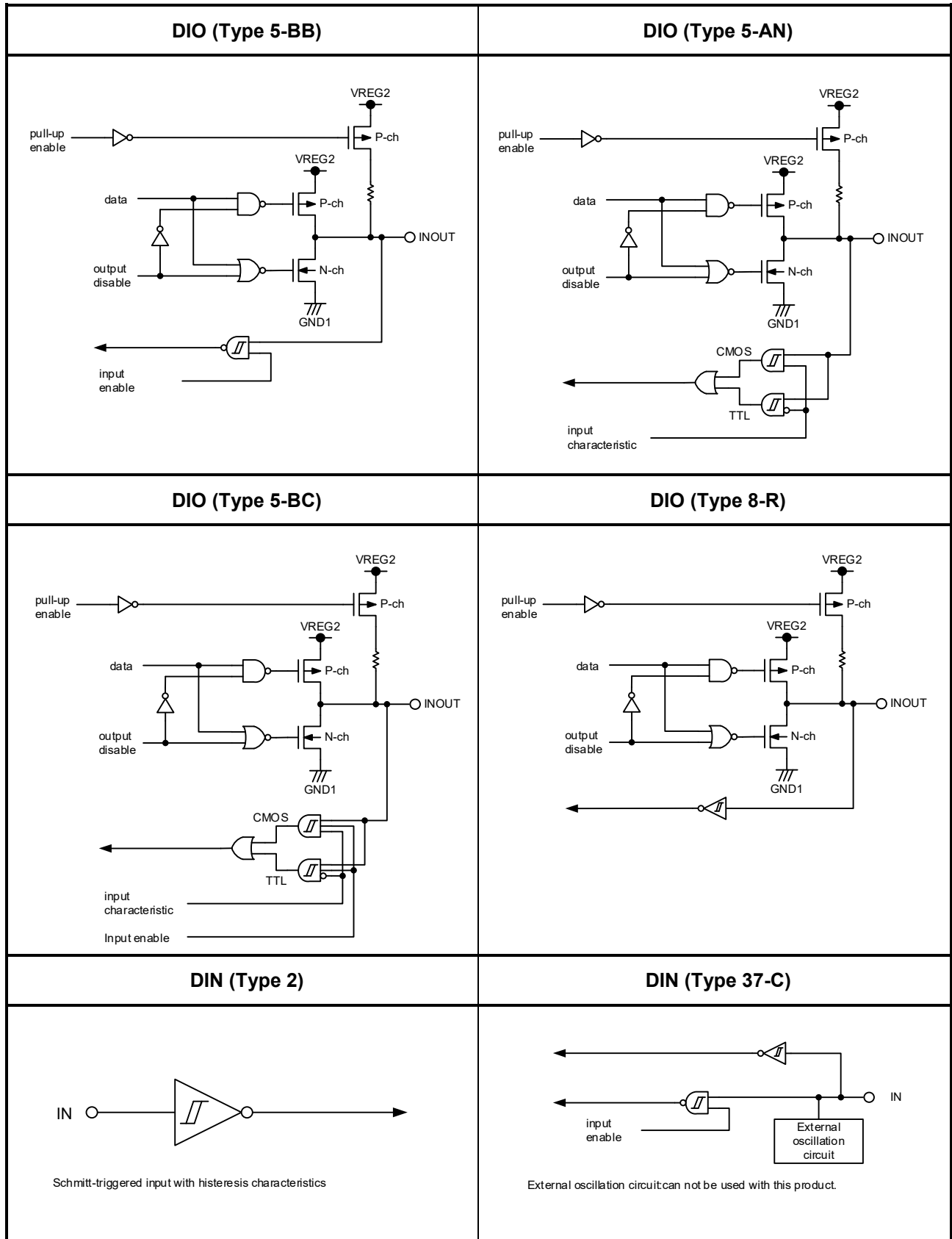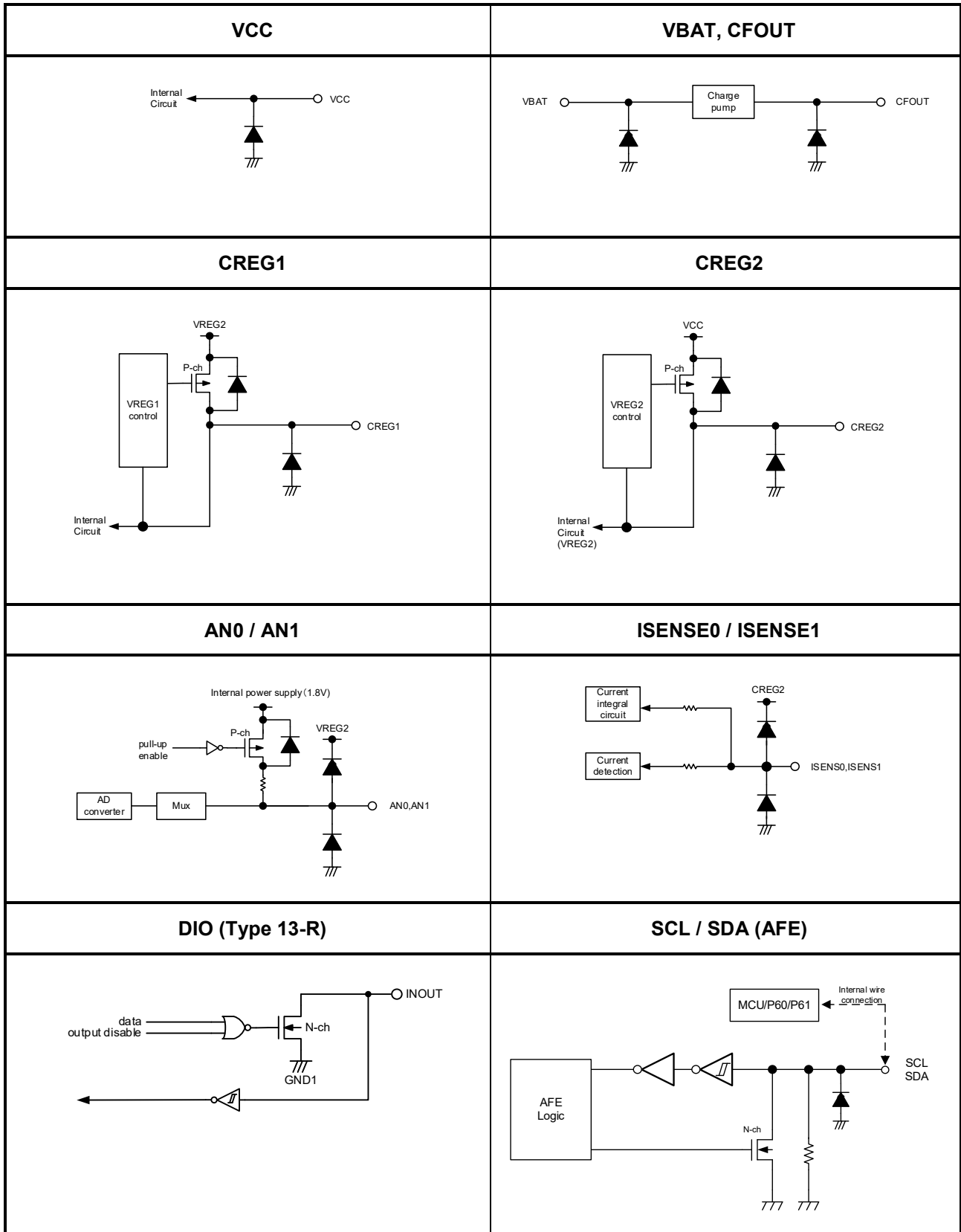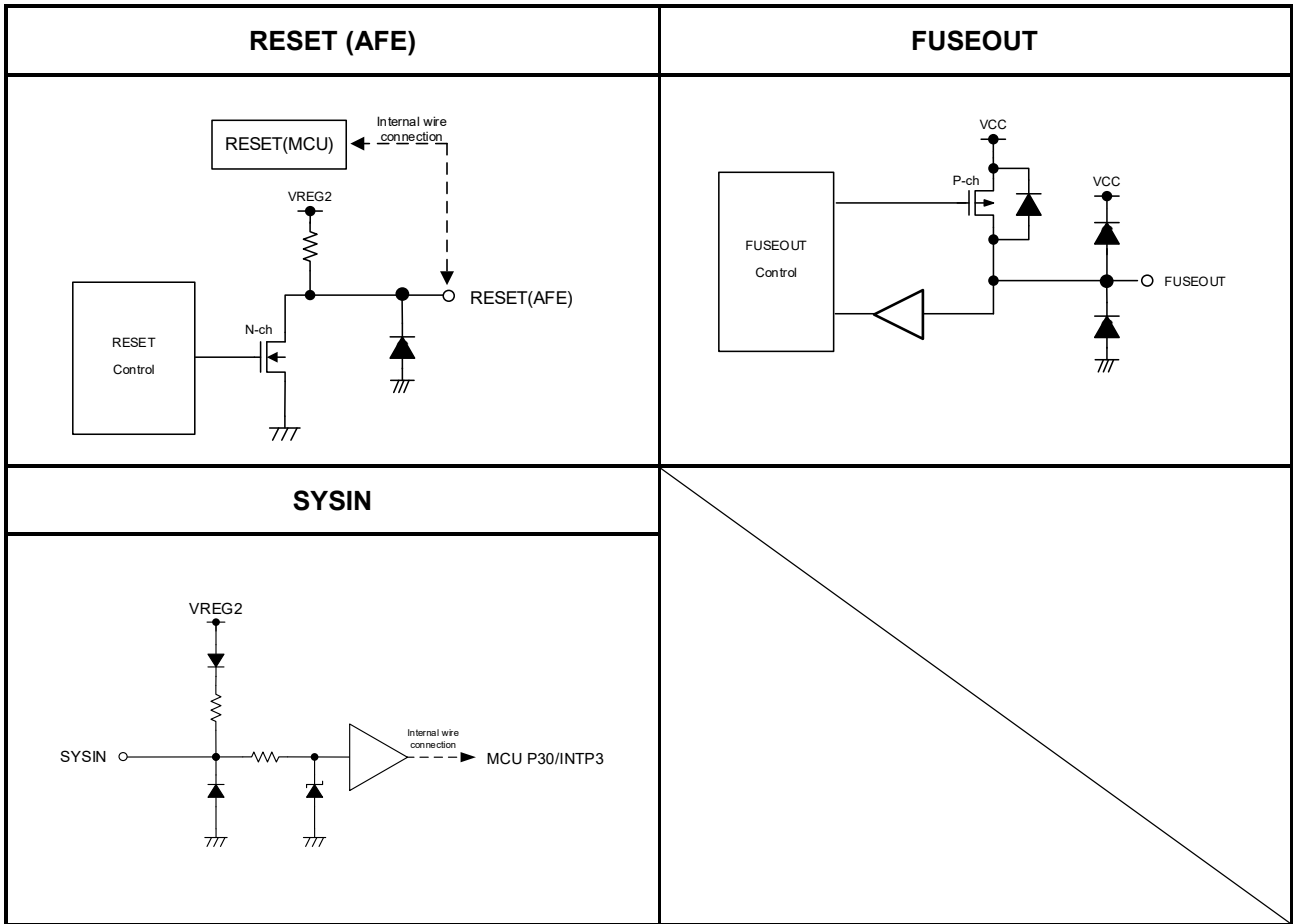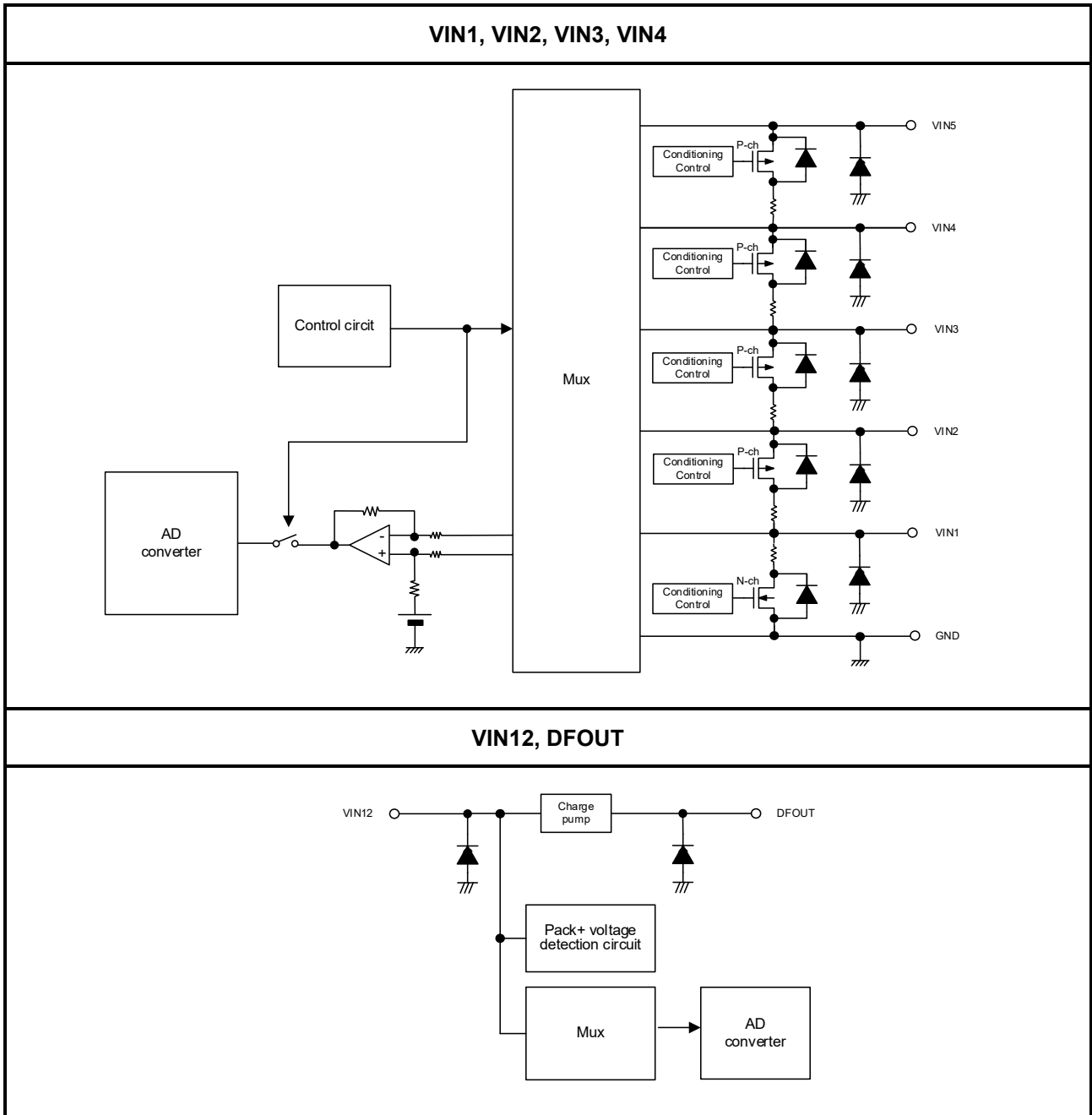
3. ELECTRICAL SPECIFICATIONS

Caution This product has an on-chip debug function, which is provided for development and evaluation.
Do not use the on-chip debug function in products designated for mass production because the guaranteed number of rewritable times of the flash memory may be exceeded when this function is used, and product reliability therefore cannot be guaranteed. Renesas Electronics is not liable for problems occurring when the on-chip debug function is used.

3.1 Absolute Maximum Ratings

Absolute Maximum Ratings (TA = 25 °C)

Parameter	Symbols	Condition		Ratings	Unit
Supply voltage	VCC			-0.5 to 30	V
	GND0, GND1			-0.5 to 0.3	V
CREG1 input voltage	VREG1	CREG1		-0.3 to 2.0 Note 2	V
CREG2 input voltage	VREG2	CREG2		-0.3 to 5.5 Note 3	V
REGC pin input voltage	VIREGC	REGC		-0.3 to 2.8 and -0.3 to VREG2 + 0.3 Note 1	V
Input voltage	VI1	P10 to P12, P16, P17, P122, P137, RESET, TOOL0(P40)		-0.3 to VREG2 + 0.3	V
	VI2	SDA(P61), SCL(P60) (N-ch open drain)		-0.3 to 5.5	V
	Vin-H	VIN4, VIN3, VIN2, VIN1, VIN12, SYSIN		-0.5 to 30	V
	Vin-B	VIN4-VIN3, VIN3-VIN2, VIN2-VIN1, VIN1-GND0		-0.5 to 7	V
Output voltage	VO1	P10 to P12, P16, P17, TOOL0(P40), SDA(P61), SCL(P60)		-0.3 to VREG2 + 0.3	V
	VO-DH	DFOUT		-0.5 to 30	V
	VO-CH	CFOUT		-0.5 to 30	V
	VO-FH	FUSEOUT		-0.3 to VCC + 0.3 And -0.5 to 30	V
Analog input voltage	VAI	AN0, AN1, AN2		-0.3 to 2.0	V
	VIS	ISENS0, ISENS1		-0.3 to 2.0	V
High-level output current	IOH	P10 to P12, P16, P17,TOOL0(P40)	Per pin	-40	mA
			Total of all pins	-100	mA
	IOH-FH	FUSEOUT		-10	mA
Low-level Output current	IOL	P10 to P12, P16, P17, TOOL0(P40)	Per pin	40	mA
			Total of all pins	100	mA
Power consumption	Pd	Topr=25°C		300	mW
Operating ambient Temperature	Topr			-20 to 85	°C
Storage temperature	Tstg			-65 to 150	°C

Note 1. Connect the REGC pin to GND1 via a capacitor (0.47 to 1μF). This value regulates the absolute maximum rating of the REGC pin. Do not use this pin with voltage applied to it.
Note 2. Connect the CREG1 pin to GND0 via a capacitor (1 μF). This value regulates the absolute maximum rating of the CREG1 pin. Do not use this pin with voltage applied to it.
Note 3. Connect the CREG2 pin to GND1 via a capacitor (2.2 μF). This value regulates the absolute maximum rating of the CREG2 pin. Do not use this pin with voltage applied to it.
VREG2 is power supply built-in IC.it is a 3.3V supply for IC.
Caution. Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.
Remark. Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

3.2   Power supply voltage condition

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Power supply voltage	VCC/VBAT		4.0	-	25	V
	GND0/GND1		-	0	-	V

3.3   Oscillation circuit characteristics

3.3.1   On-chip oscillator characteristics

(T_A = -20 to +85 °C, 4.0 V$\leq$VCC$\leq$25 V, GND0 = GND1 = 0 V)

Oscillator	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
High-speed on-chip oscillator Clock frequency [Note 1]	f_{IH}		-	8	-	MHz
Low-speed on-chip oscillator Clock frequency	f_{IL}		-	15	-	kHz
AFE on-chip oscillator Clock frequency [Note 2]	f_{OCO}		-	4.194	-	MHz
AFE on-chip oscillator Clock frequency accuracy	-		-2	-	+2	%

Note 1.   High-speed on-chip oscillator frequency is selected with bits 0 to 4 of the option byte (000C2H/010C2H) and bits 0 to 2 of the HOCODIV register.

Note 2.   This value is when it writes trimming data stored in flash memory to the OCOTRIM0 to OCOTRIM2 register.

3.4   DC characteristics

3.4.1   Pin characteristics

(T_A = -20 to +85 °C,   4.0 V≤VCC≤25 V, VREG2 = 3.3 V, GND0 = GND1 = 0 V)

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input voltage High	VIH1	P10 to P12, P16, P17, P122, P137, TOOL0(P40), $\overline{RESET}$		0.8 x VREG2	-	VREG2	V
	VIH2	SCL(P60), SDA(P61)		2.1	-	VREG2	V
	VIH3	SYSIN		0.7 x VREG2	-	VREG2	V
	VIH4	FUSEOUT		2	-	VCC	V
	VIH5	P10,P16,P17(TTL Input buffer)		2	-	VREG2	V
Input voltage low	VIL1	P10 to P12, P16, P17, P122, P137, TOOL0(P40), $\overline{RESET}$		0	-	0.2 x VREG2	V
	VIL2	SCL(P60), SDA(P61)		0	-	0.8	V
	VIL3	SYSIN		0	-	0.3 x VREG2	V
	VIL4	FUSEOUT		0	-	0.5	V
	VIL5	P10,P16,P17(TTL Input buffer)		0	-	0.5	V
Output voltage High	VOH1	P10 to P12, P16, P17, P40	IOL = -1.5mA	VREG2 - 0.5	-	VREG2	V
Output voltage Low	VOL1	P10 to P12, P16, P17, P40	IOL = 1.5mA	-	-	0.4	V
	VOL2	SCL(P60), SDA(P61)	IOL = 3.0 mA	-	-	0.4	V
FUSEOUT Output High Voltage	$V_{OH-FUSE}$	External Pulldown 100 kΩ		VCC - 0.5	-	-	V
Input leak current High	ILIH1	P10 to P12, P16, P17, P122, P137, TOOL0(P40), $\overline{RESET}$	VI = VREG2	-	-	1	µA
Input leak current Low	ILIL1	P10 to P12, P16, P17, P122, P137, TOOL0(P40), $\overline{RESET}$	VI = GND1	-	-	-1	µA
Pull-up resistor	RU	P10 to P12, P16, P17, P40	VI = GND1, When input port	10	20	100	kΩ
	RUA	AN0, AN1, AN2	VI = GND1	7.5	(10)	12.5	kΩ
	RUA	$\overline{RESET}$	VI = GND1	-	(20)	-	kΩ

Note 1.   The maximum value of VIH of pins P10, P11, and P17 is VREG2, even in N-ch open drain mode.
Note 2.   P10, P11, P17 do not output a high-level in N-ch open drain mode.

Remark 1.   Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.
Remark 2.   About pin characteristics of CFOUT, DFOUT, refer to [3.6.6 charge/discharge FET control circuit characteristics]
Remark 3.   About pin characteristics of VIN1, VIN2, VIN3, and VIN4 refer to [3.6.5 Battery voltage detection circuit characteristics]
Remark 4.   The parenthetical values are for reference.

3.4.2   Supply current characteristics

(T_A = -20 to +85 °C,   4.0 V≤VCC≤25 V, VREG2 = 3.3 V, GND0 = GND1 = 0 V)

Item	Symbol	Condition			MIN.	TYP.	MAX.	Unit
Supply Current[Note 1]	ICC1	Normal operation mode [Note 2]	Low-speed Operation	f_{HOCO} = 8 MHz f_{IH} = 8 MHz	-	(2.0)	-	mA
	ICC2	Wait mode [Note 3]	STOP mode	TA = +25 °C	-	(150)	-	µA
	ICC3	Power down mode	VCC≤14 V		-	(0.5)	1	µA

Note 1.   This is the current which flows in VCC.
Note 2.   This value includes the operation currents of the integrating current circuit, overcurrent detection circuit, charge FET control and discharge FET control.
Note 3.   This value includes the operation currents of overcurrent detection circuit, charge FET control and discharge FET control.

Remark 1. f_{HOCO}: high-speed on-chip oscillator clock frequency (32 MHz max.)
Remark 2. f_{IH} : high-speed on-chip oscillator clock frequency (32 MHz max.)
Remark 3.   Temperature condition of the TYP. Value is T_A=25 °C.
Remark 4.   The numerical value in a parenthesis is a reference value.
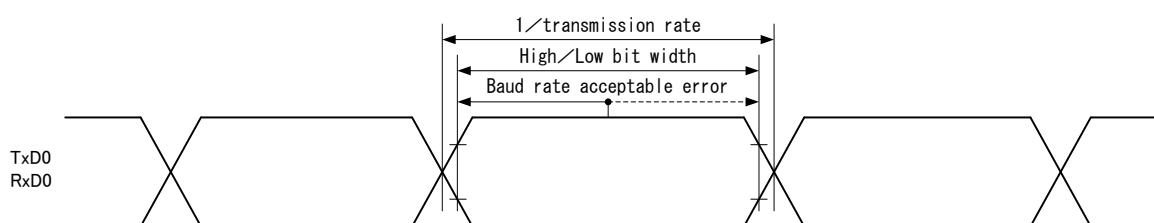
3.5 Peripheral function characteristics

3.5.1 Serial array unit

1. During communication at same potential (UART mode) (Dedicated baud rate generator output)

(T_A = -20 to +85 °C, 4.0 V≤VCC≤25 V, VREG2 = 3.3 V, GND0 = GND1 = 0 V)

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Transmission rate			-	-	$f_{MCK}/6$	bps
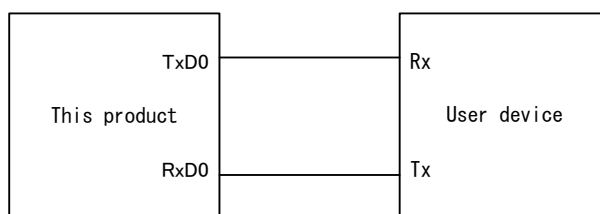
UART mode connection diagram (During communication at same potential)

UART mode bit width (During communication at same potential) (reference)

Caution   Select the normal input buffer for the RxDq pin and the normal output mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remark 1.   q: UART number (q = 0 to 3), g: PIM and POM number (g =0, 1, 5, 14)

Remark 2. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13)

2. During communication at same potential (CSI mode) (master mode ($f_{MCK}/4$), $\overline{SCKp}$…internal clock output)
(T_A = -20 to +85 °C,   4.0 V≤VCC≤25 V, VREG2 = 3.3 V, GND0 = GND1 = 0 V)

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
$\overline{SCKp}$ cycle time	t_{KCY1}		125 **Note 1**	-	-	ns
$\overline{SCKp}$ high-/low-level width	t_{KH1}, t_{KL1}		$t_{KCY1}/2$-18	-	-	ns
Sip setup time (to $\overline{SCKp}$ ↑) **Note 2**	t_{SIK1}		44	-	-	ns
Sip hold time (to $\overline{SCKp}$ ↑) **Note 2**	t_{KSI1}		19	-	-	ns
Delay time from $\overline{SCKp}$ ↓ to Sop output **Note 3**	t_{KSO1}	C = 30 pF **Note 4**	-	-	25	ns

Note 1.   The value must also be $4/f_{CLK}$ or more.
Note 2.   When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes "to $\overline{SCKp}$ ↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.
Note 3.   When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes "from $\overline{SCKp}$ ↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.
Note 4   C is the load capacitance of the $\overline{SCKp}$ and SOp output lines.

Caution.   Select the normal input buffer for the SIp pin and the normal output mode for the SOp pin and $\overline{SCKp}$ pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remark 1   p: CSI number (p=00), m: Unit number (m=0), n: Channel number (n=0)
                g: PIM, POM number (g=1)
Remark 2.   fMCK: Serial array unit operation clock frequency
                (Operation clock to be set by the CKSmn bit of serial mode register (SMRmn). m: Unit number
                n: Channel number (mn= 0))

3. During communication at same potential (CSI mode) (Slave mode, $\overline{\text{SCKp}}$…external clock input)
(T_A = -20 to +85 °C, 4.0 V≤VCC≤25 V, VREG2 = 3.3 V, GND0 = GND1 = 0 V)

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
$\overline{\text{SCKp}}$ cycle time Note 4	t_{KCY2}	16 MHz<f_{MCK}	$8/f_{MCK}$	-	-	ns
		f_{MCK}≤16 MHz	$6/f_{MCK}$	-	-	ns
$\overline{\text{SCKp}}$ high-/low-level width	t_{KH2}, t_{KL2}		$t_{KCY2}/2$	-	-	ns
Sip setup time (to $\overline{\text{SCKp}}$ ↑) Note 1	t_{SIK2}		$1/f_{MCK}+20$	-	-	ns
Sip hold time (to $\overline{\text{SCKp}}$ ↑) Note 1	t_{KSI2}		$1/f_{MCK}+31$	-	-	ns
Delay time from $\overline{\text{SCKp}}$ ↓ to Sop output Note 2	t_{KSO2}	C = 30 pF Note 3	-	-	$2/f_{MCK}+44$	ns

Note 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes "to $\overline{\text{SCKp}}$ ↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes "from $\overline{\text{SCKp}}$ ↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 3. C is the load capacitance of the SOp output lines.

Caution   Select the TTL input buffer for the SIp pin and $\overline{\text{SCKp}}$ pin and the normal output mode for the SIp pin by using port input mode register g (PIMg) and port output mode register g (POMg).
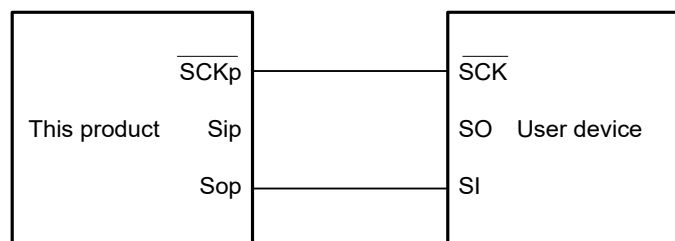
Remark 1. p: CSI number (p=00, 01, 10, 11, 20, 21, 30, 31), m: Unit number (m=0, 1)
n: Channel number (n= 0 to 3), g: PIM, POM number (g=0, 1, 3 to 5, 14)

Remark 2. fMCK: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register (SMRmn). m: Unit number
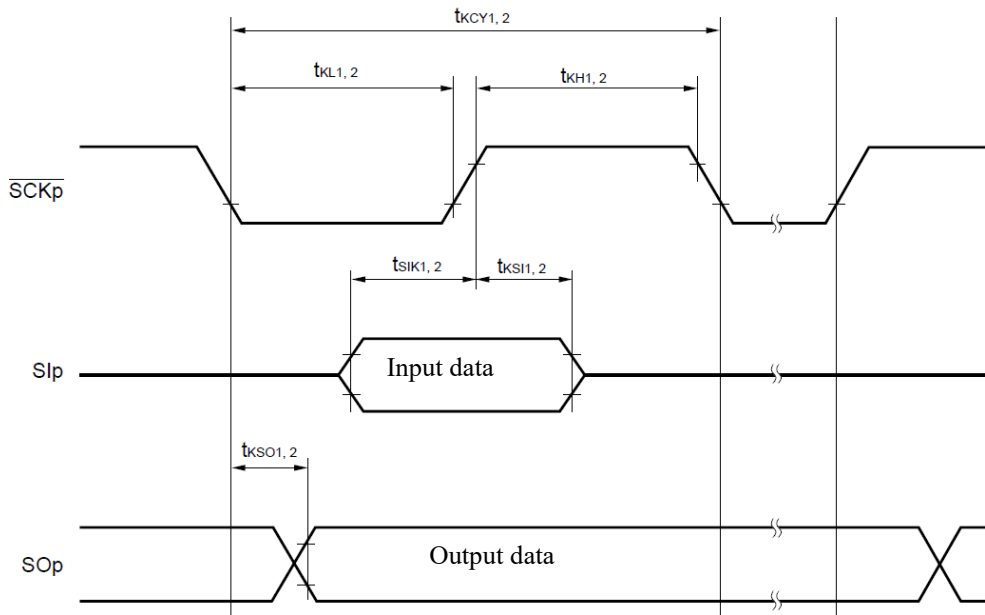n: Channel number (mn= 00 to 03, 10 to 13))

CSI mode connection diagram (During communication at same potential)
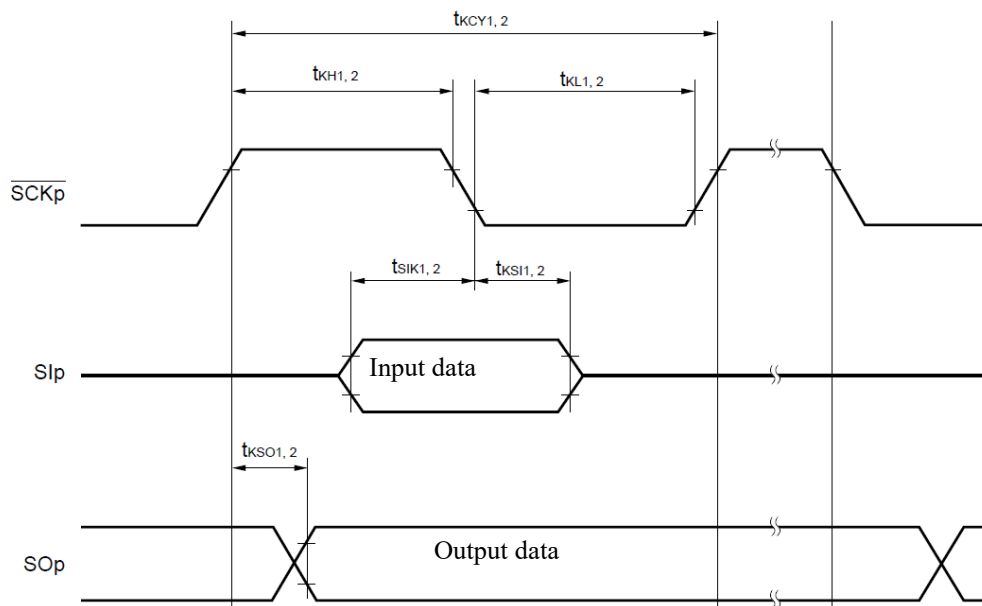
Remark 1. P: CSI number (p=00, 01, 10, 11, 20, 21, 30, 31)
Remark 2. m: Unit number, n: channel number (mn= 00 to 03, 10 to 13)

CSI mode serial transmission timing (During communication at same potential)

(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1)

CSI mode serial transmission timing (During communication at same potential)

(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0)

Remark 1. p:CSI number (p=00, 01, 10, 11, 20, 21, 30, 31)
Remark 2. m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13)

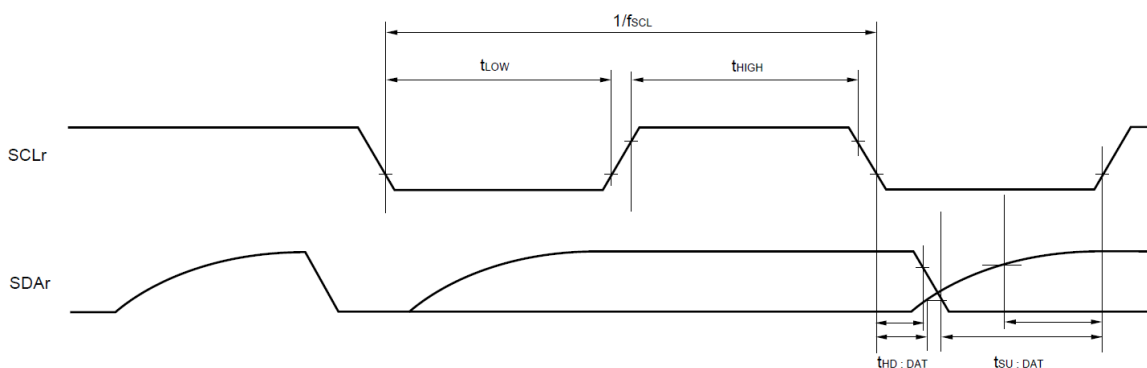4. During communication at same potential (simplified I²C mode)

(T_A = -20 to +85 °C, 4.0 V≤VCC≤25 V, VREG2 = 3.3 V, GND0 = GND1 = 0 V)

Item	Symbol	Condition	MIN.	MAX.	Unit
SCLr clock frequency	fSCL	Cb = 50 pF, Rb = 2.7 kΩ	-	1000	kHz
Hold time when SCLr = "L"	tLOW	Cb = 50 pF, Rb = 2.7 kΩ	475	-	ns
Hold time when SCLr = "H"	tHIGH	Cb = 50 pF, Rb = 2.7 kΩ	475	-	ns
Data setup time(reception)	tSU:DAT	Cb = 50 pF, Rb = 2.7 kΩ	1/fMCK+85 [Note]	-	ns
Data hold time(transmission)	tHD:DAT	Cb = 50 pF, Rb = 2.7 kΩ	0	305	ns

Note   Set the f_MCK value to keep the hold time of SCLr = "L" and SCLr = "H".
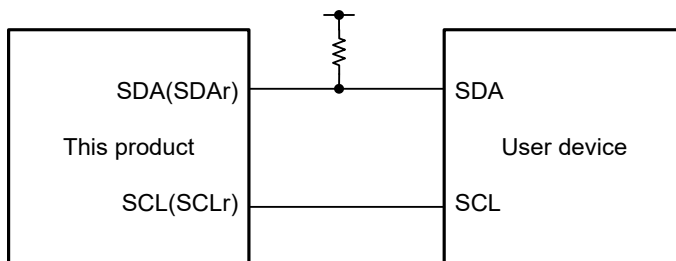
Simplified I²C mode connection diagram (During communication at same potential)

Simplified I²C mode serial transmission timing (During communication at same potential)

Caution   Select the TTL input buffer and the N-ch open drain output (VREG2 tolerance) mode for
the SDAr pin and the N-ch open drain output (VREG2 tolerance) mode for the SCLr pin
by using port input mode register g (PIMg) and port output mode register h (POMh).

Remark 1.   Rb[Ω]: Communication line (SDAr) pull-up resistance, Cb[F]: Communication line (SDAr, SCLr) load
capacitance
Remark 2.   r: IIC number (r = 00, 01, 10, 11, 20, 21, 30, 31), g: PIM number (g = 0, 1, 3 to 5, 14),
h: POM number (h = 0, 1, 3 to 5, 7, 14)
Remark 3.   fMCK: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).
m: Unit number(m = 0, 1), n: Channel number (n = 0, 2, mn = 00 to 03, 10 to 13))
Remark 4.   Communication at different potential (2.5 V, 3 V) (UART mode, CSI mode, simplified I²C mode)
The serial array unit of this product do not connect (communicate) the device at different potential.
Connecting device is same potential to VREG2 (CREG2 pin) certainly.

3.5.2 Serial interface IICA

(T_A = -20 to +85 °C, 4.0 V≤VCC≤25 V, VREG2 = 3.3 V, GND0 = GND1 = 0 V)

Item	Symbol	Condition	Standard Mode		Fast Mode		Fast Mode Plus		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCLA0 clock frequency	fSCL	Fast mode plus : fCLK≥10 MHz	-	-	-	-	0	1000	kHz
		Fast mode : fCLK≥3.5 MHz	-	-	0	400	-	-	kHz
		Standard mode : fCLK≥1 MHz	0	100	-	-	-	-	kHz
Setup time of restart condition Note 1	tSU: STA		4.7	-	0.6	-	0.26	-	µs
Hold time	tHD: STA		4.0	-	0.6	-	0.26	-	µs
Hold time when SCLA0 = "L"	tLOW		4.7	-	1.3	-	0.5	-	µs
Hold time when SCLA0 = "H"	tHIGH		4.0	-	0.6	-	0.26	-	µs
Data setup time(reception)	tSU: DAT		250	-	100	-	50	-	ns
Data hold time(transmission) Note 2	tHD: DAT		0	3.45	0	0.9	0	-	µs
Setup time of stop condition	tSU: STO		4.0	-	0.6	-	0.26	-	µs
Bus-free time	tBMF		4.7	-	1.3	-	0.5	-	µs

Note 1.   The first clock pulse is generated after this period when start/restart condition is detected.
Note 2.   The maximum value (MAX) of tHD: DAT is during normal transfer and wait state is inserted in the ~~ACK~~ (acknowledge) timing.

Remark.   The maximum value of Cb (communication line capacitance) and the value of Rb (communication line pull-up resistor) at that time in each mode are as follows.

Standard mode: Cb = 400 pF, Rb = 2.7 kΩ
Fast mode: Cb = 320 pF, Rb = 1.1 kΩ
Fast mode plus: Cb = 120 pF, Rb = 1.1 kΩ
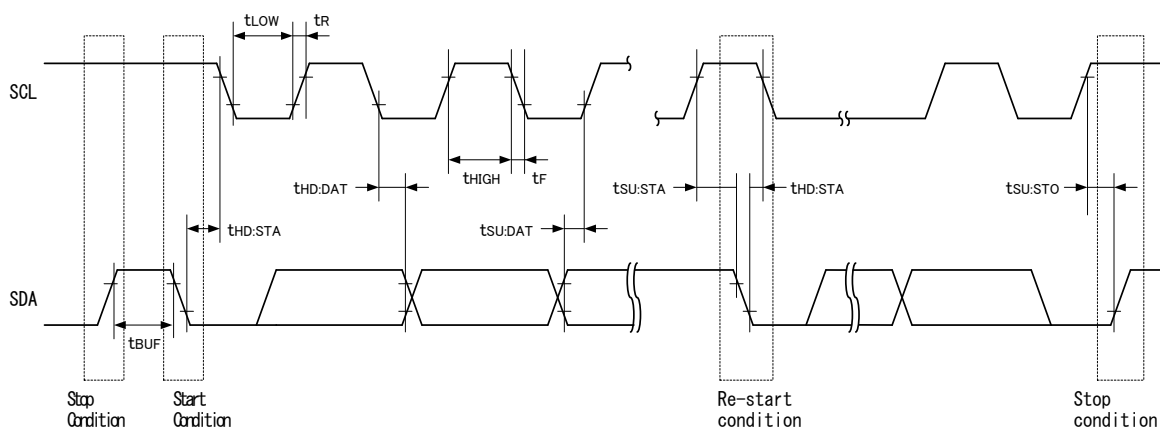
IICA serial transfer timing

3.5.3 On-chip debug (UART)

(T_A = -20 to +85 °C, 4.0 V≤VCC≤25 V, VREG2 = 3.3 V, GND0 = GND1 = 0 V)

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Transmission rate			115.2 k	-	1 M	bps

3.5.4 Interrupt

(T_A = -20 to +85 °C, 4.0 V≤VCC≤25 V, VREG2 = 3.3 V, GND0 = GND1 = 0 V)

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Interrupt input high-level width, low-level width	t_{INTH}, t_{INTL}	INTP0, INTP5	1	-	-	µs

3.6   Analog front end characteristics

3.6.1   A/D converter characteristics

(T_A = -20 to +85 °C,   4.0 V≤VCC≤25 V, VREG2 = 3.3 V, VREG1 = 1.8V, GND0 = GND1 = 0 V)

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Resolution	-		-	15	-	bit
Input voltage range	-		0	-	VREG1	V
Integral non-linearity error	-		-	-	±16	LSB
Conversion result(zero input) **Note**	-	VI=GND0	-	3266	-	LSB
Temperature dependency (zero input)	-	VI=GND0	-0.24	-	+0.24	LSB/°C
Conversion result (full-scale input) **Note**	-	VI= VREG1	-	29453	-	LSB
Temperature dependency (full-scale input)	-	VI= VREG1	-0.24	-	+0.24	LSB/°C
AN port input current	II (AD)		-	2.0	-	µA

Note.   This value of A/D conversion result is a decimal value.

3.6.2   Current integrating circuit characteristics

(T_A = -20 to +85 °C,   4.0 V≤VCC≤25 V, VREG2 = 3.3 V, GND0 = GND1 = 0 V)

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Resolution	-		-	18	-	bit
Input voltage range	-	ISENS1-ISENS0 Sensing resistor: 5 mΩ	-0.1	-	0.1	V
Conversion time	-	f1=4,194,304 Hz	-	(250)	-	ms
Integral non-linearity error	-		-	-	0.02	%FSR
ISENS0, ISENS1 Input current	II (CC)		-	0.2	-	µA

Remark.   The parenthetical values are for reference.

3.6.3   Overcurrent detection circuit characteristics

(T_A = -20 to +85 °C,   4.0 V$\leq$VCC$\leq$25 V, VREG2 = 3.3 V, GND0 = GND1 = 0 V)

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Discharge short-circuit current 1 detection voltage error	-		-	-	±50	mV
Discharge short-circuit current 2 detection voltage error	-	25 mV to 100 mV setting	-	-	±12.5	mV
		125 mV to 250 mV setting	-	-	±25	mV
Discharge overcurrent detection voltage error	-	25 mV to 50mV setting	-	-	±10	mV
		55 mV to 100 mV setting	-	-	±25	mV
Charge overcurrent detection voltage error	-	-25 mV to -100 mV setting	-	-	±10	mV
		-125 mV to -250 mV setting	-	-	±25	mV
Wakeup current detection voltage error [Note1,Note2]	-	Discharge side, 10 times mode ±1A detection sense resistance 5mohm	4.0	5.0	6.0	mV
Turbo boost current detection error[Note2]	-	10 times mode ±1A detection sense resistance 5mohm	4.0	5.0	6.0	mV
Discharge short-circuit current 1 detection time error	-		0	-	30.5	μs
Discharge short-circuit current 2 detection time error	-		0	-	30.5	μs
Discharge overcurrent detection time error	-		0	-	30.5	μs
Charge overcurrent detection time error	-		0	-	30.5	μs
Wakeup current detection time Error [Note 1]	-		58.6	-	62.5	ms

Note 1.   It is applied both to Charge wakeup detection and Discharge wakeup detection.
Note 2.   The error in the case where the calibration at each temperature. It does not include the error due to the temperature characteristics of the detection circuit.

3.6.4　Series regulator circuit characteristics

(T_A = 25 °C , VCC = 14 V, GND0 = GND1 = 0 V)

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Output voltage	Vreg2o	VCC=14 V, Io=50 µA, after trimming	-	(3.3)	-	V
Drive current [Note]	VR2d	VCC=VIN4≥4.0 V,VREG2≥3.0 V	20	-	-	mA
Output voltage(VREG1)	Vreg1o	VCC=14V,Io=10µA,after trimming	1.755	-	1.845	V

Note.　The sum of the I/O port High-level output current of the MCU of the operating current must be less than the drive current capability.

Remark.　The parenthetical value is for reference.

3.6.5　Battery voltage detection circuit characteristics

(T_A = 25 °C , VCC = 14 V, GND0 = GND1 = 0 V)

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Offset voltage	Voff	VCC=VIN4≥2.0 V x (number of Battery cells)	-	(100)	-	mV
Voltage gain (VIN1 to 5)	Gamp1	VCC=VIN4≥2.0 V x (number of Battery cells)	-	(0.28)	-	times
Voltage gain (VIN12)	Gamp2	VCC=VIN4≥2.0 V x (number of Battery cells)	-	(0.06)	-	times
Maximum detection battery voltage (VIN1 to 5)	Vmo_max1		5.0	(6.0)	-	V
Maximum detection voltage (VIN12)	Vmo_max2		25.0	-	-	V
Input voltage	-	VIN4	0	-	25	V
	-	VIN3, VIN2, VIN1	0	-	VIN4	V
	-	VIN4-VIN3, VIN3-VIN2, VIN2-VIN1, VIN1-GND	0	-	5	V
	-	VIN12	0	-	25	V

Remark.　The parenthetical value is for reference.

3.6.6   Charge/discharge FET control circuit characteristics

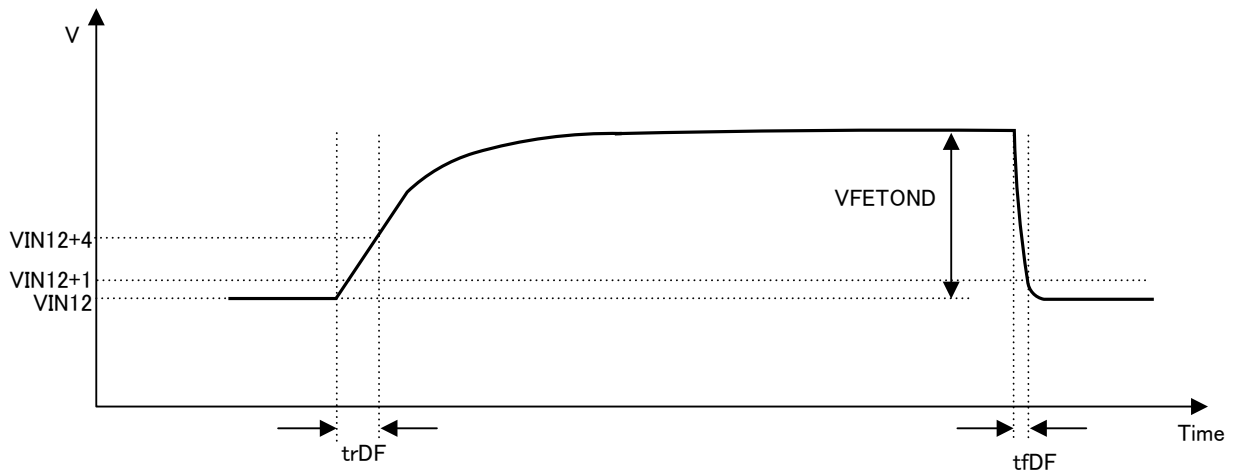(T_A = 25 °C , VCC = 14 V, GND0 = GND1 = 0 V)

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
CFOUT H output voltage	VFETONC1	CFOUT-VBAT, 4.0 V≤VCC<6.0 V, RL=10MΩ	4	(7)	12	V
	VFETONC2	CFOUT-VBAT, 6.0 V≤VCC, RL=10MΩ	9	(10)	12	V
CFOUT L output voltage	VFETOFFC	CFOUT-VBAT, VBAT=14 V, RL=10MΩ	-	(0)	0.2	V
CFOUT control time	trCF1	Lo (VBAT)→Hi (VBAT+4 V), CL=4700 pF, 4.0 V≤VCC<6.0 V	-	(1000)	3000	µs
	trCF2	Lo (VBAT) →Hi (VBAT+4 V), CL=4700 pF, 6.0 V≤VCC	-	(200)	600	µs
	tfCF	Hi (VBAT+4 V) → Lo (VBAT+1 V), CL=4700 pF	-	(80)	200	µs
DFOUT H output voltage	VFETOND1	DFOUT-VIN12, 4.0 V≤VCC<6.0 V, RL=10MΩ	4	(7)	12	V
	VFETOND2	DFOUT-VIN12, 6.0 V≤VCC, RL=10MΩ	9	(10)	12	V
DFOUT L output voltage	VFETOFFD	DFOUT-VIN12, VIN12=14 V, RL=10MΩ	-	(0)	0.2	V
DFOUT control time	trDF1	Lo (VIN12) → Hi (VIN12+4 V), CL=4700 pF, 4.0 V≤VCC<6.0 V	-	(1000)	3000	µs
	trDF2	Lo (VIN12) → Hi (VIN12+4 V), CL=4700 pF, 6.0 V≤VCC	-	(200)	600	µs
	tfDF	Hi (VIN12+4 V) → Lo (VIN12), CL=4700 pF External constant of VIN12: C=0.01 µF, R=10 kΩ	-	(250)	400	µs

Remark.   The parenthetical value is for reference.

CFOUT output timing characteristic
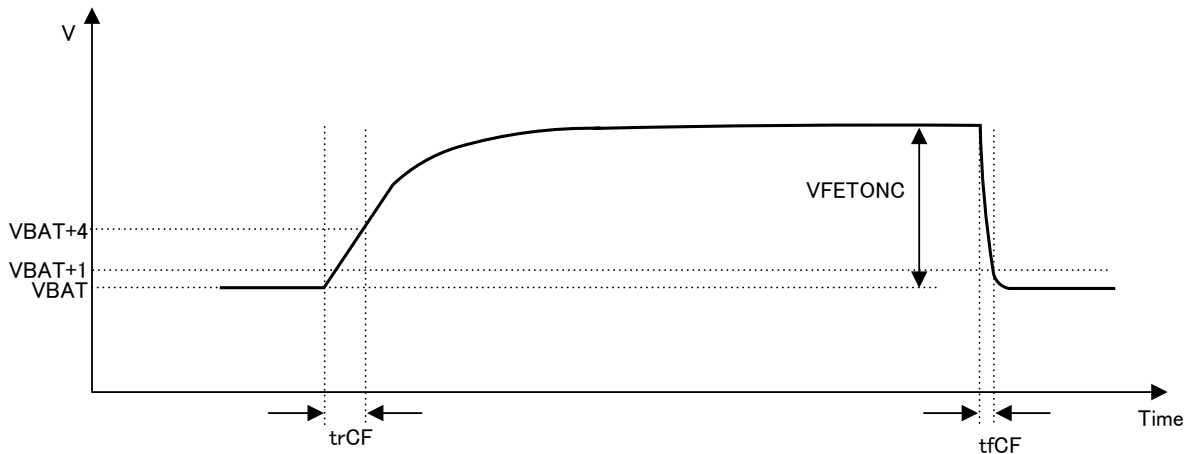
DFOUT output timing characteristic

3.6.7   Conditioning circuit characteristics

(T_A = 25 °C , VCC = 14 V, GND0 = GND1 = 0 V)

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
1cell ON resistance	RON1	VCC=VBAT=VIN4=14V, VIN3=10.5 V, VIN2=7 V, VIN1=3.5 V 1cell conditioning SW: ON	-	(500)	-	Ω
2cell ON resistance	RON2	VCC=VBAT=VIN4=14V, VIN3=10.5 V, VIN2=7 V, VIN1=3.5 V 2cell conditioning SW: ON	-	(500)	-	Ω
3cell ON resistance	RON3	VCC=VBAT=VIN4=14V, VIN3=10.5 V, VIN2=7 V, VIN1=3.5 V 3cell conditioning SW: ON	-	(500)	-	Ω
4cell ON resistance	RON4	VCC=VBAT=VIN4=14V, VIN3=10.5 V, VIN2=7 V, VIN1=3.5 V 4cell conditioning SW: ON	-	(500)	-	Ω

Remark.   The parenthetical value is for reference.

3.7   Flash memory programming characteristics

(T_A = -20 to +85 °C,   4.0 V≤VCC≤25 V, VREG2 = 3.3 V, GND0 = GND1 = 0 V)

Item	Symbol	Condition		MIN.	TYP.	MAX.	Unit
Number of code flash rewrites[Note1,2,3]	Cerwr	Retained for 20 years	T_a=85°C	1,000	-	-	times
Number of data flash rewrites[Note1,2,3,]		Retained for 1 years	T_a=25°C	-	1,000,000	-	
		Retained for 5 years	T_a=85°C	100,000			
		Retained for 20 years	T_a=85°C	10,000	-	-	

Note 1.   1 erase + 1 write after the erase is regarded as 1 rewrite. The retaining years are until rewrite after the rewrite.
Note 2.   When using flash memory programmer and Renesas Electronics self-programming library.
Note 3.   The one that shows the characteristics of the flash memory, this characteristic is the result of the reliability test.

4. Function Description

4.1 Overview

RAJ240047 is Renesas Battery Management IC which incorporates advanced battery fuel gauge features such as primary and secondary protection, voltage and current measurement, current integration, host communication interface and etc. This product consists of MCU block and AFE block in a single package and accomplish redundant protection mechanism by independent two blocks. Fuel gauge control firmware and data are stored in embedded flash memory and controls embedded analog and digital hardware circuits to achieve optimum battery management operation including high accuracy remaining capacity estimation and battery safety.

4.2 System block diagram
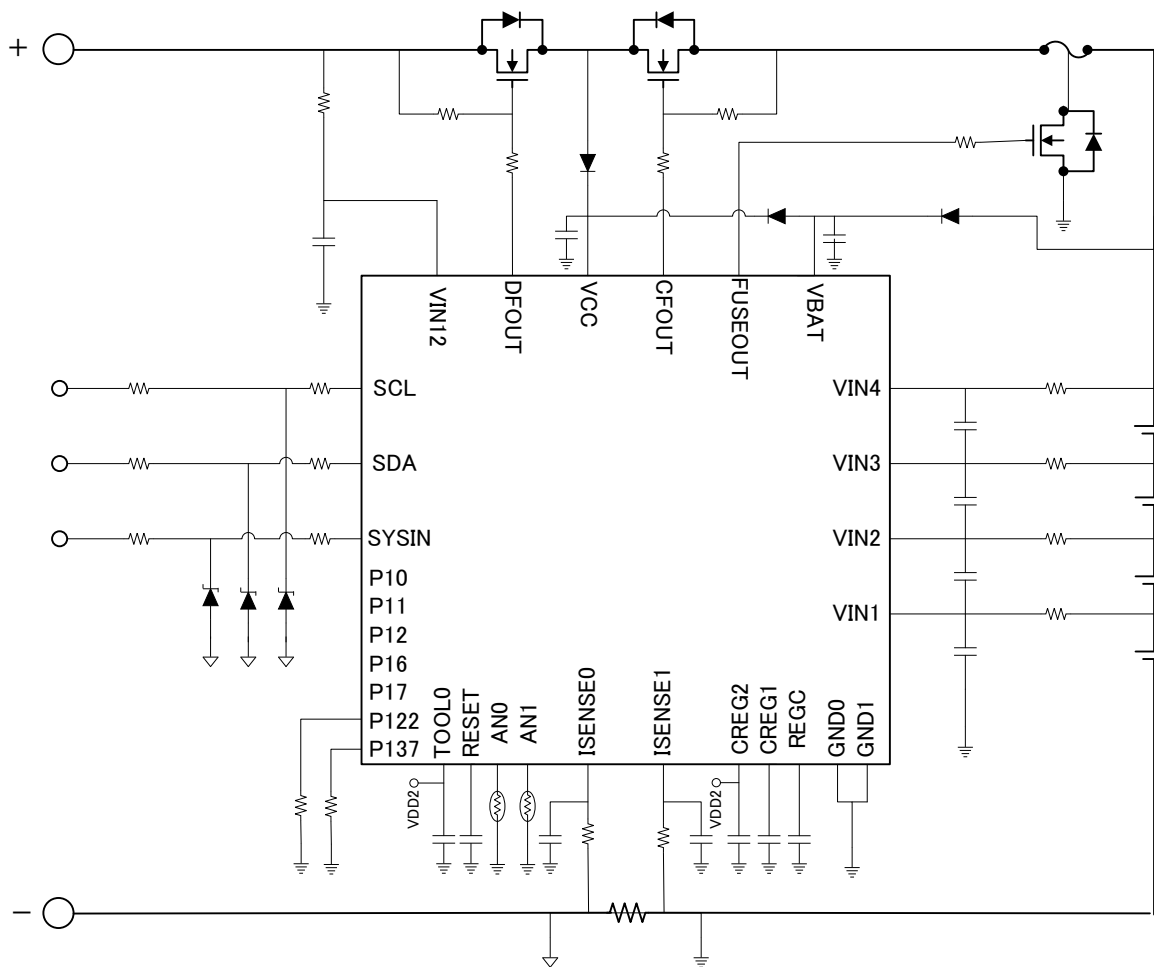
Simplified System Block Diagram

Note   This example of a peripheral circuit does not guarantee the operation of this IC. Evaluate the operation adequately with actual applications, and then determine the circuits and constants.
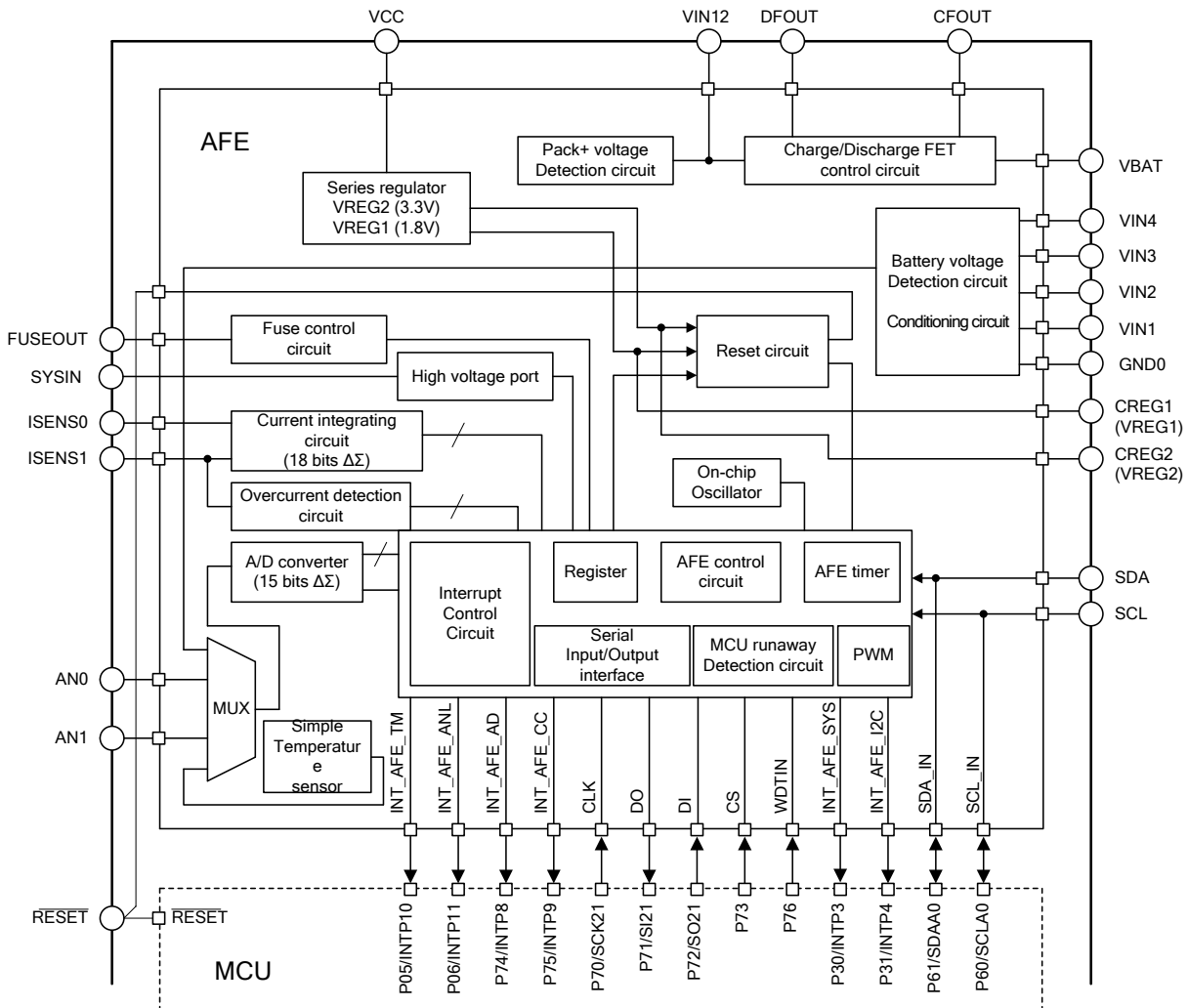
4.3   MCU Block Diagram
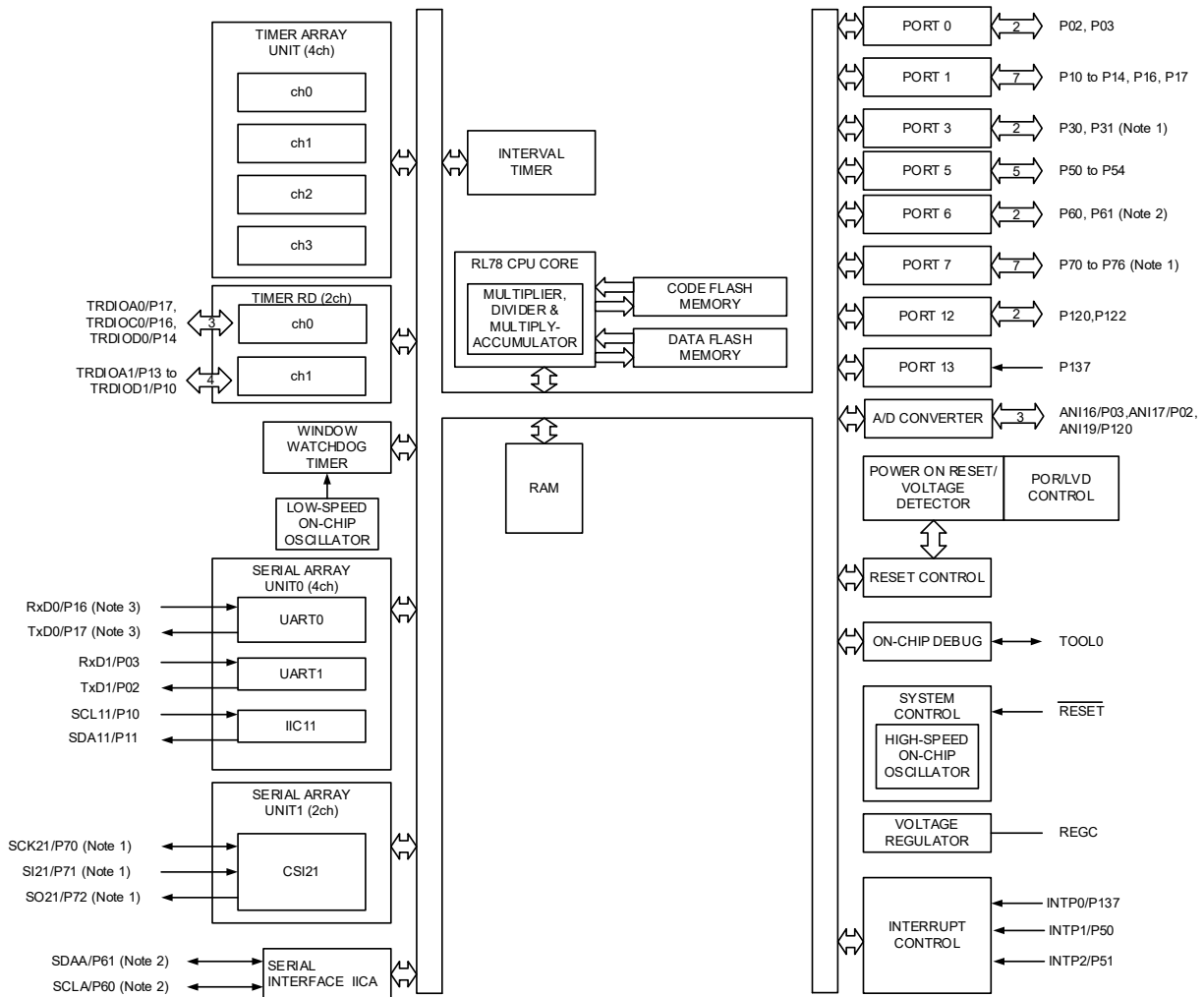
Note 1.   P30,P31,P70 to P76 are connected to AFE chip in the package.And do not connected to any pin.
Note 2.   P60/SDAA0 is connected to SDA pin and P61/SCLA0 is connected to SCL pin respectively.
Note 3.   Each interrupt request of AFE are assigned P05/INTP10,P06/INTP11. To use external interrupt function of
            P05,P06(INTP10,INTP11),it set the PIOR01 bit in the PIOR0 register to 1 and it's enabled peripheral
            I/O re-direction function. When setting the PIOR01 bit to 1,P16,P17 can be used as UART function(RxD0,TxD0)

MCU Internal Block Diagram

4.4   AFE Block Diagram

AFE Internal Block Diagram

4.5　Feature List

Note　　　　Following function overview is when setting peripheral I/O re-direction register 0 (PIOR0) to 02H.

(1/2)

Item		Description
Code flash memory		128KB
Data Flash memory		4 KB
RAM		5.5 KB
Main system clock	High speed on-chip Oscillator clock(fIH)	High speed operation:1 to 32 MHz Low speed operation:1 to 8 MHz
Low speed on-chip oscillator clock		15 kHz (TYP.)
General purpose register		8 bits × 32 registers (8 bits × 8 registers × 4 banks)
minimum instruction execution time		0.03125 μs(Internal high speed oscillation clock: fIH = 32 MHz)
Instruction set		• data transmission (8/16 bits) • Addition and subtraction/logical operations (8/16 bits) • Multiplication (8×8 bits,16×16 bits), Division (16÷16 bits,32÷32 bits) • Rotate, barrel shift, bit manipulation (set, reset, test, Boolean operation) etc.
I/O Port	CMOS input/output	16
	CMOS input	2
	I2C bus input/output	2
	High voltage port	Output only: 1 Input only: 1
Timer	16 bits timer	5 channels (TAU: 4 channels, Timer RD:2 channel)
	Watchdog timer	1 channel
	12 bits interval timer	1 channel
Serial interface		• UART: 2 channels • CSI: 1 channel/simple I2C:1 channel • CSI: 1 channel
	I2C bus	1 channel
Vector interrupt source	Internal	10
	External	9 (6 sources are connected to AFE in the chip)
Reset		• reset by RESET pin (reset circuit output of AFE, connect to RESETOUT) • internal reset by watchdog timer • internal reset by illegal instruction execution **Note** • internal reset by RAM parity error • internal reset by illegal memory access
On-chip debug function		Support

Note　　　　It occurs when executes instruction code of "FFH".
　　　　　　Reset by illegal instruction execution is not occurred emulation by on-chip debug emulator.

Item	Description
PWM	8 bits×1
A/D converter	15-bit resolution (ΔΣ method) ×2 channels + internal 5 channels
Current integrating circuit	1 channel:18 bits resolution
Current integrating circuit for impedance measurement	1 channel:11 bits resolution
Overcurrent detection circuit	Discharge short-circuit current detection 1, Discharge short-circuit current detection 2, Discharge overcurrent detection, charge overcurrent detection, Wake-up current detection (discharge, charge), turbo boost current detection
Simple temperature sensor	1 channel
Charge/Discharge FET control circuit	N-ch FET driver for charge control N-ch FET driver for discharge control
Battery voltage detection circuit	Battery voltage gain: 0.28 times Offset voltage: 0.1 V
Pack+ voltage detection circuit	Battery Pack+ pin monitor gain:0.06 times
Fuse control circuit	Fuse control function
Series regulator[Note1]	VREG2:power supply for MCU (3.3 V)
	High accuracy Power supply	VREG1(CREG1 pin):A/D converter, current integrating circuit (1.8 V)
Reset circuit	Series regulator output monitoring (VREG1, VREG2)
Conditioning circuit	5 cell support (On-resistor:500Ω)
MCU runaway detection circuit	20 bits×1(2 / 4 /8 [s] to be selected)
On-chip oscillator[Note2]	4.194 MHz (TYP.)
AFE timer	2 channels AFE timer A(setting range:125 ms to 64 s) AFE timer B(setting range:30.52 us to 125 ms)
Serial input/output interface	Communication between AFE and MCU (4-wire)
Power supply voltage	VCC=4.0 to 25 V
Operation ambient temperature	-20 to 85 [°C]
Package	48 pin QFP

Note 1.   Series regulator stabilization time is 10ms after AFE power on.
Note 2.   2ms wait is need for stabilization after On-chip oscillator is started.

4.6   Feature Description

4.6.1   ADC Circuit

15-bit delta-sigma ADC is implemented to measure instantaneous analog signal levels, such as voltage, current, temperature and etc. The multiplexer selects one of 8 channels to measure each signal. Appropriate channel of the multiplexer must be selected to measure desirable analog signal. ADC conversion results are stored in A/D data registers after the conversion.

ADC circuit block has a feature to execute multiple ADC conversions automatically. The multiplexer selects designated channel and ADC conversions are executed as specified in ADC automatic mode control register. An interrupt is asserted upon ADC conversion and the conversion result is stored in A/D data registers periodically.

Impedance measurement mode for Turbo-boost is an optional feature to measure voltage and current simultaneously. This optional feature was designed to measure battery impedance upon Turbo-boost operation and to calculate available maximum power.

Table 4-1 shows A/D converter performance, Figure 4-1 shows Block Diagram of A/D Converter.

Table 4-1 A/D converter performance

Item	Performance
A/D conversion method	ΔΣ conversion
Analog input voltage	0 V to VREG1
Operating clock φAD	fOCO divided by 4: 1.048576 MHz
	(fOCO=AFE on-chip oscillator)
Resolution	15 bits
Conversion accuracy	Integral non-linearity error: ±16 LSB
Analog input channel	AN0, AN1
	Battery voltage detection circuit output (AO)
	Simple temperature sensor
	VREG1, VREGpull, GND
A/D conversion start condition	Software trigger
Conversion rate per pin	1024 ΦAD cycles: 1 ms mode [Note]
	2048 ΦAD cycles: 2 ms mode [Note]
	4096 ΦAD cycles: 4 ms mode [Note]
	8192 ΦAD cycles: 8 ms mode [Note]

Note   One of the modes is selected by the bits ADTIME0 to ADTIME1 in the ADCON1 register.
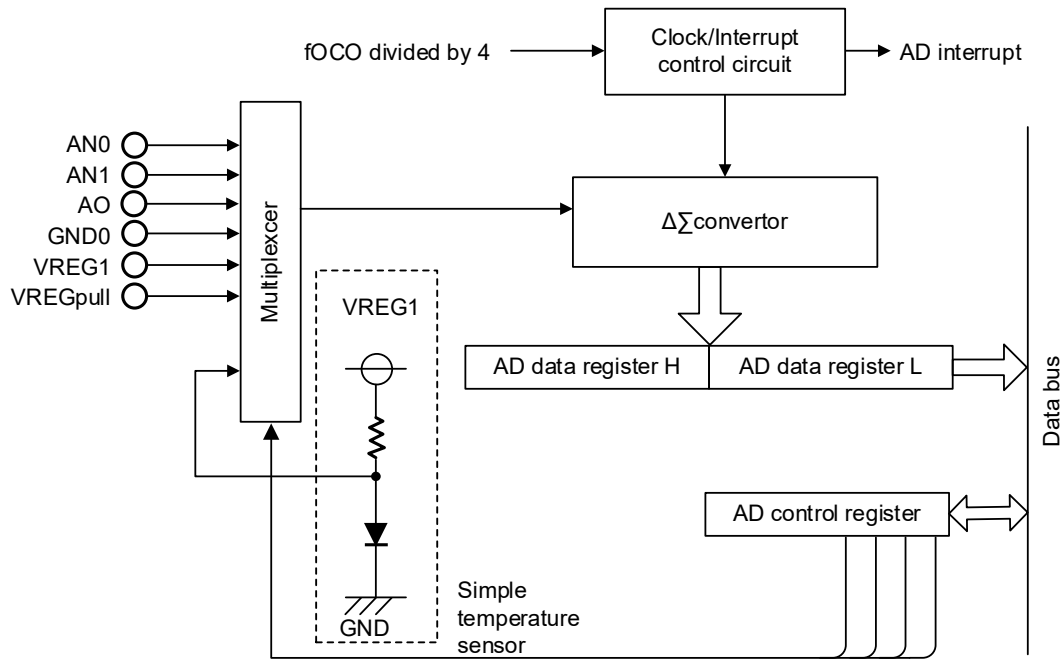
GND: GND
VREG1: High accuracy internal power supply for A/D (1.8V、 Equivalent to CREG1 terminal output voltage)
AO: Output of Battery voltage detection circuit

Figure 4-1 Block Diagram of A/D Converter

Dedicated multiplexer provides 8 channels for A/D conversion to measure signal voltage level. Select "battery voltage detect circuit output (AO)" and configure battery voltage detection circuit of AFE to measure battery voltage levels.
A/D converter multiplexer selection and conversion period can be configured in following registers.

1. AD control register (ADCON)

This register can control A/D converter operation enable, A/D conversion start, current integrating for impedance measurement operation enable and also can select a channel of AD conversion.

ADCON register can access by sending or receiving serial data to serial input-output interface using 3-wire serial I/O of MCU (CSI21). The register value is 00H by a reset signal from reset circuit

AFE address: 50H After Reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
ADCON	ADST	ADSLP	IMPST	0	ADSEL3	ADSEL2	ADSEL1	ADSEL0

ADSEL3	ADSEL 2	ADSEL 1	ADSEL 0	Select a channel of A/D conversion
0	0	0	0	AN0
0	0	0	1	AN1
0	0	1	0	Setting prohibited
0	0	1	1	Setting prohibited
0	1	0	0	Setting prohibited
0	1	0	1	Setting prohibited
0	1	1	0	Battery voltage detect circuit output (AO)
0	1	1	1	Sample temperature sensor
1	0	0	0	Setting prohibited
1	0	0	1	Setting prohibited
1	0	1	0	GND0 [Note 2]
1	0	1	1	CREG1 [Note 3]
1	1	0	0	Setting prohibited
1	1	0	1	VREG1_pull [Note 4]
1	1	1	0	Setting prohibited
1	1	1	1	Setting prohibited

IMPST	Current integrating for impedance measurement operation start control
0	Stop
1	Start

ADSLP	A/D conversion operation enable [Note 5]
0	Disable
1	Enable

ADST	A/D conversion operation control [Notes 1, 5]
0	Stop
1	Start

Figure 4-2 AD control register (ADCON) format

Note 1.   This bit is automatically 0 after A/D conversion is completed. If repeat operation, set 1 to this bit after written 0.
Note 2.   This one is used as reference GND (GND0 pin, 0 V) of A/D converter
Note 3.   This one is used as reference internal power (CREG1 pin 1.8 V) of A/D converter
Note 4.   This is used as internal power for thermistor pull-up resistor
Note 5.   When ADSLP bit and ADST bit set 1 simultaneously AD conversion starts 60[us] later.

2. AD control register 1 (ADCON1)

This register can select an A/D conversion time. And also can select current integrating circuit for impedance measurement conversion time at the same time.

ADCON1 register can access by sending or receiving serial data to serial input-output interface using 3-wire serial I/O of MCU (CSI21).

The register value is 00H by a reset signal from reset circuit

AFE address: 51H After Reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
ADCON1	0	0	0	0	0	0	ADTIME1	ADTIME0

ADTIME1	ADTIME0	A/D conversion time
0	0	1 ms
0	1	2 ms
1	0	4 ms
1	1	8 ms

Figure 4-3 AD control register 1 (ADCON1) format

4.6.2 Battery Voltage detection circuit

The battery voltage detection circuit can detect the battery cell voltage and the voltage of the Pack + pin. Input signals can be selected by setting VBSE0 to VBSE3 bits in the VBSE register and are connected to A/D converter input. This signal can be measured an analog value attenuated by a predetermined gain using A/D converter by selecting "Battery voltage detect circuit output (AO)" A/D converter multiplexer.

Figure 4-4 shows the Block Diagram of Battery Voltage detection circuit.
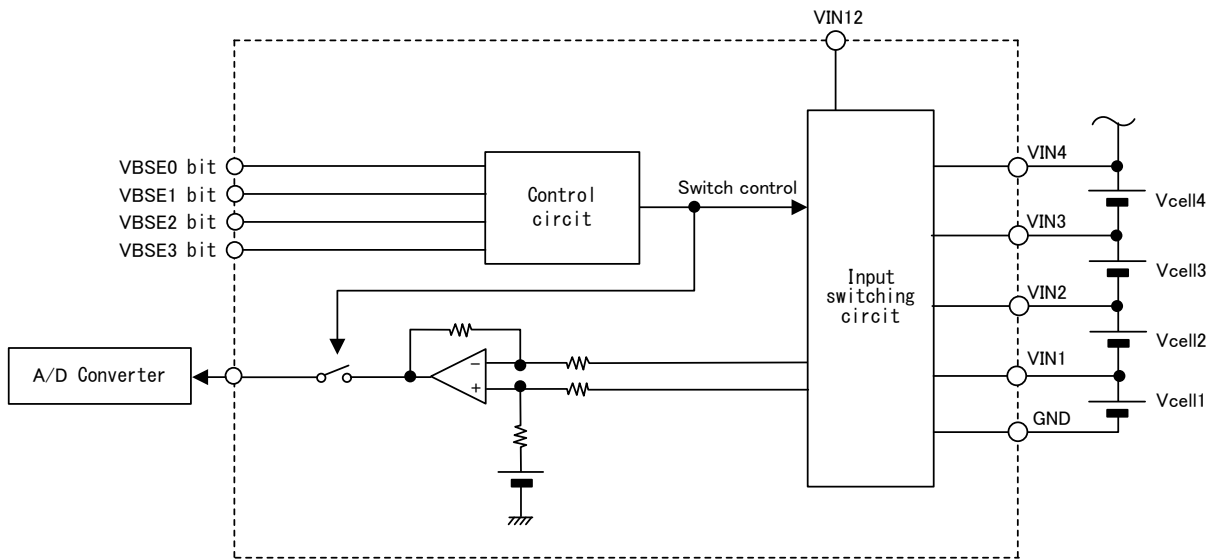
Figure 4-4 Block Diagram of Battery Voltage detection circuit

1. Analog output control Register (VBSE)

This register can be selected an analog output of battery voltage detection circuit that output to A/D converter.
VBSE register can access by sending or receiving serial data to serial input-output interface using 3-wire serial I/O of MCU (CSI21).
The register value is 00H by a reset signal from reset circuit.

AFE address: 02H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
VBSE	0	0	0	0	VBSE3	VBSE 2	VBSE 1	VBSE 0

VBSE3	VBSE 2	VBSE 1	VBSE 0	Battery voltage detection circuit output
0	0	0	0	HiZ output
0	0	0	1	VBAT1 output
0	0	1	0	VBAT2 output
0	0	1	1	VBAT3 output
0	1	0	0	VBAT4 output
0	1	0	1	Setting prohibited
0	1	1	0	VBAT1 offset output
0	1	1	1	VBAT2 offset output
1	0	0	0	VBAT3 offset output
1	0	0	1	VBAT4 offset output
1	0	1	0	Setting prohibited
1	0	1	1	VIN12 voltage output
1	1	0	0	VIN12 voltage offset output
1	1	0	1	SMBus I/O mode 10 minutes timer history[Note]
1	1	1	0	Setting prohibited
1	1	1	1	Setting prohibited

Figure 4-5 Analog output control Register (VBSE) format

Note.   After SMBus I/O mode start up, if one of the commands of the Flash write-erase and read isn't received and 10 minutes passed, AFE register of VBSE (02h bit3-0) is set to b1101 as a history of elapsed 10 minutes, software reset is done. History of the 10 minutes had elapsed can be seen from the user program. AFE register (VBSE: 02h bit3-0) is reset to the b0000 by AFE initialization. After referring to the history of the 10 minutes had elapsed, AFE register in the user program, it is need to initialize to (VBSE 02h bit3-0) the b0000. It is recommend to refer to the "RAJ240XXX flash memory SMBus input and output mode" for more information.

4.6.3 Current Integrating Circuit

The current integrating circuit measures the current flowing in a sense resistor by converting the potential difference across the terminals of the resistor connected between the ISENS1 and ISENS0 pins to a digital value. Analog signals are input from the ISENS1 and ISENS0 pins.

Table 4-2 shows current integrating circuit performance. Figure 4-6 shows current integrating circuit block diagram, Figure 4-7 shows operation timing of Current integrating circuit.

Table 4-2 Current integrating Circuit Performance

Item	Performance
Conversion method	ΔΣ conversion
Analog input voltage	-0.1 V to 0.1 V
Operating clock φCC	fOCO divided by 32: 131.072 kHz (fOCO=AFE on-chip oscillator)
Resolution	18bit
Conversion accuracy	Integral non-linearity error: ±0.02 %FSR
Analog input pin	Potential difference between ISENS1 and ISENS0 pins
Conversion time per cycle	250 ms (32,768φCC cycle)
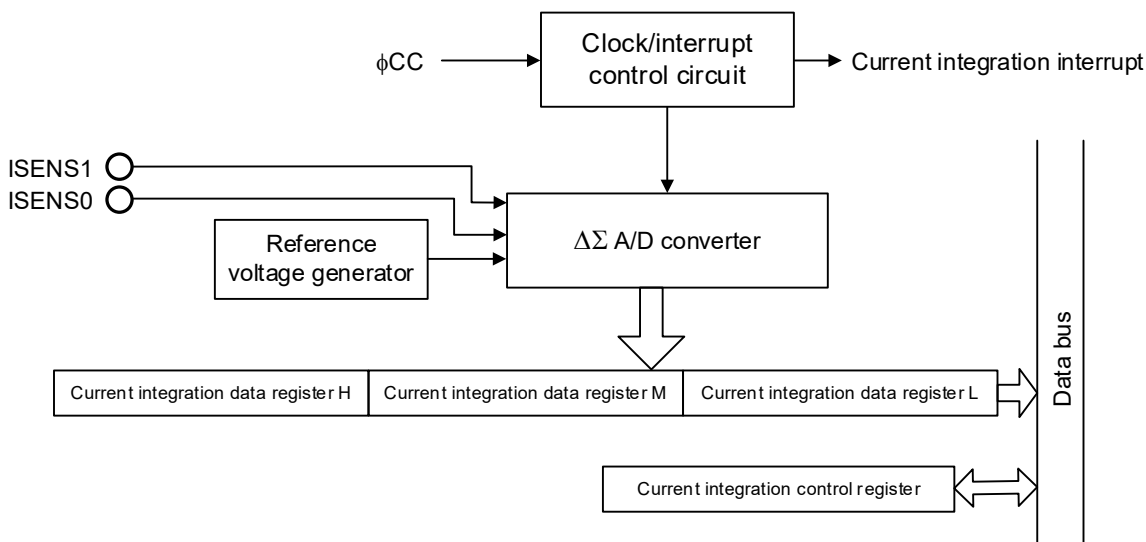
Figure 4-6 Current integrating circuit block diagram
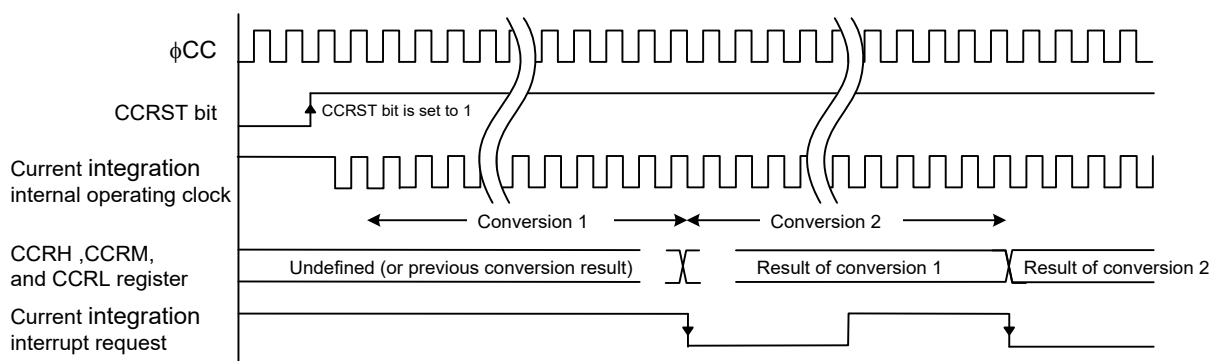
Figure 4-7 Operation timing of Current integrating circuit

4.6.4 Current Integration Circuit in Impedance Measurement Mode

The current integrating circuit for impedance measurement measures current of the sense resister connected between the pins ISENS1 and ISENS0 by converting the voltage of that into digital values. This circuit can measure the impedance value because it can measure the current with the A/D converter synchronously. Analog signals are input from the ISENS1 and ISENS0 pins.

Table 4-3 shows Current integrating Circuit for impedance Measurement Performance, Figure 4-8 shows current integrating circuit for impedance measurement block diagram, Figure 4-9 shows operation timing of current integrating circuit for impedance measurement.

Table 4-3 Current integrating Circuit for impedance Measurement Performance

Item	Performance
Conversion method	ΔΣ conversion
Analog input voltage	-0.1 V to 0.1 V
Operating clock φCC	fOCO divided by 32: 131.072 kHz (fOCO=AFE on-chip oscillator)
Resolution	Conversion time 1 ms(note 1): 7 bits Conversion time 2 ms(note 1): 8 bits Conversion time 4 ms(note 1): 9 bits Conversion time 8 ms(note 1): 10 bits
Analog input pin	Potential difference between ISENS1 and ISENS0 pins
Conversion time per cycle (note 1) Note	1 ms, 2 ms, 4 ms, 8 ms

Note   The conversion time varies with the setting of the ADTIME1 bit and the ADTIME0 bit in the ADCON1 register.
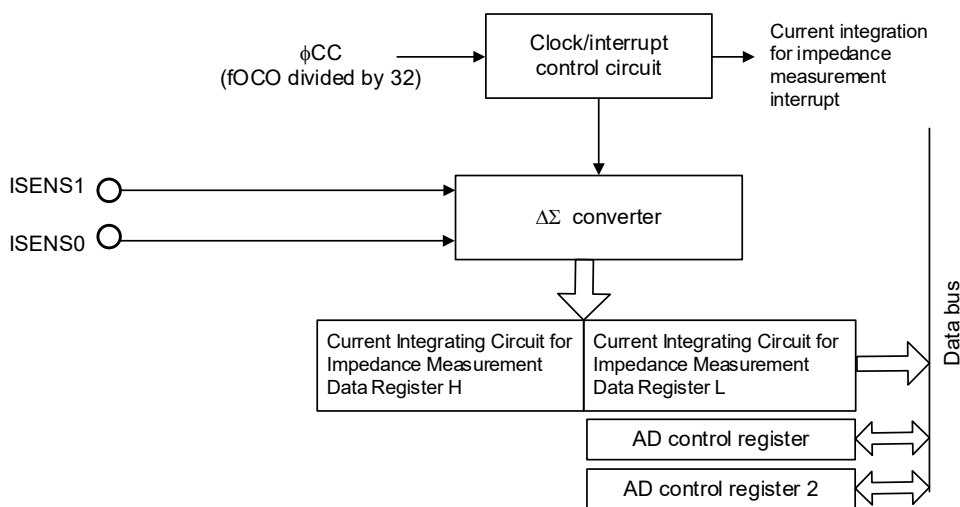
Figure 4-8 Current integrating circuit for impedance measurement block diagram
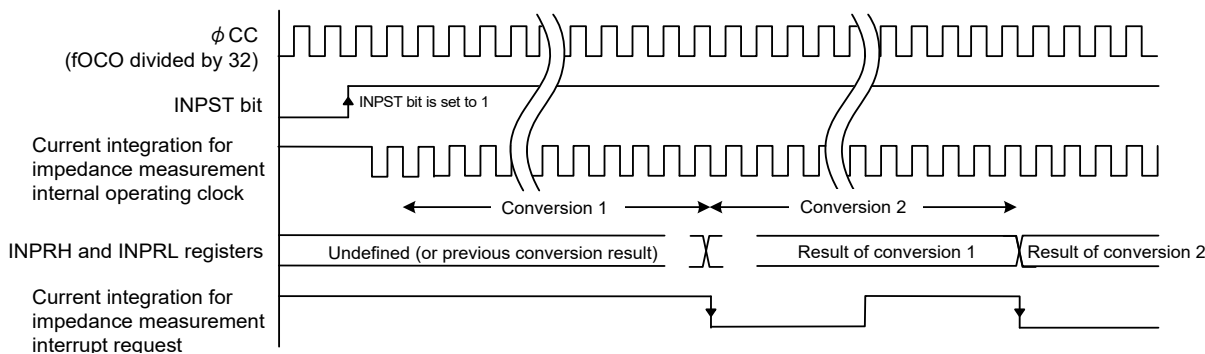
Figure 4-9 Operation timing of current integrating circuit for impedance measurement

4.6.5   FET control circuit

The FET control circuit has two on-chip voltage step-up circuits, and this product is able to control N-ch FETs as switches to control charging and discharging.

■   FET ON/OFF control
It can control the ON/OFF of charge FET, discharge FET by setting the FETC bit, FETD bit in the FCON register to 1.

■   Forced FET OFF Function
When the AFE identifies a short-circuit overcurrent, overcharge, or overdischarge state,
It can turn off the FET forcibly.
Forced OFF Function of discharge FET is set the BCFETEN bit in the BCDCON register or the SCFETEN bit in the SCDCON register or the DOCFETEN bit in the DOCDCON register to 1 to enable a FET control.
Forced OFF function of charge FET is set the COCFETEN bit in the COCDCON register to 1 to enable a FET control.
The state of forced FET OFF function is judged by reading the AFECON3 register.
In discharge FET control, read the DFDATMON bit in the AFECON3 register, in charge FET control, read the CFDATMON bit in the AFECON3 register respectively.

When the DFDATMON bit is "1", the DFOUT pin becomes VIN12 level.
When the CFDATMON bit is "1", the CFOUT pin becomes VBAT level

When the forced FET OFF function is available (forced OFF) the FETC bit, FETD bit in the FCON register values are invalid, it enables the forced FET OFF function control.

Table 4-4 shows the relations between FCON register value and FET forced OFF function and DFOUT/CFOUT pin control.

Table 4-4 FCON register value and relationship of the FET forced OFF function and DFOUT/CFOUT pin control

DFOUT control			CFOUT control		
DFDATMON bit	FETD bit	DFOUT pin	CFDATMON bit	FETC bit	CFOUTpin
0	0	OFF	0	0	OFF
0	1	ON	0	1	ON
1	0	VIN12 level	1	0	VBAT level
1	1		1	1	

Charge FET ON function when turbo boost current is detected
It is possible to forcibly do ON the charge FET that is OFF state when turbo boost current is detected. The charge FET forcibly ON function is enabled to set the TBCFETEN bit in the WUDCON2 register to 1 when turbo boost current detection is enabled.

4.6.6 Overcurrent Detection Circuit

The overcurrent detection circuit detects overcurrent such as short-circuit current that flows through the detection. Resistor connected between pins ISENS1 and ISENS0, and turns off the battery pack charge/discharge control FET to stop charging/discharging.

The overcurrent detection circuit incorporates discharge short-circuit current circuit 1, discharge short-circuit current circuit 2, discharge overcurrent circuit, and charge overcurrent circuit, for which detection voltage and detection time can be set independently.

In addition, the overcurrent detection circuit also incorporates a wakeup current detection circuit to generate an interrupt in case a current of 200 mA to 1 A flow through the detection resistor in power-down mode where the current integrating circuit is disabled when a battery is charging or discharging. Additionally, the overcurrent detection circuit also incorporates an automatically measurement function of cell voltage, a detection circuit has function that charge FET is ON.

Analog signals are input from the ISENS1 pin.

Table 4-5 shows Overcurrent Detection Circuit Performance, Figure 4-10 shows Block Diagram of Overcurrent Detection Circuit.

Table 4-5 Overcurrent Detection Circuit Performance

Item	Performance	
Analog input pin	ISENS1	
Operating clock	f32K (AFE on-chip oscillator divided by 128)	
Detection voltage Setting range (setting interval)	Discharge short-circuit current1	0.1 V to 0.8 V (0.1 V)
	Discharge short-circuit current 2	25 mV to 100 mV (12.5 mV) setting range 1 100 mV to 250 mV (25 mV) setting range 2
	Discharge overcurrent	25 mV to 50 mV (2.5 mV) setting range 1 50 mV to 100 mV (5 mV) setting range 2
	Charge overcurrent	-25 mV to -100 mV (12.5 mV) setting range 1 -100 mV to -250 mV (25 mV) setting range 2
	Wakeup current	-145 mV to 145 mV (2.5 mV)
	Turbo boost current	-145 mV to 145 mV (2.5 mV)
Detection time Setting range (setting interval)	Discharge short-circuit current1	0 μs to 427 μs (61 μs)
	Discharge short-circuit current 2	0 μs to 915 μs (61 μs)
	Discharge overcurrent	0.916 ms to 30.212 ms (1.95 ms)
	Charge overcurrent	0 μs to 915 μs (61 μs)
	Wakeup current	62.5 ms (It takes 244 μs to perform calibration)
	Turbo boost current	488 μs
Detection voltage error	Discharge short-circuit current1	±50 mV
	Discharge short-circuit current 2	±10 mV (setting range 1) /±25 mV (setting range 2)
	Discharge, charge overcurrent	±10 mV (setting range 1) /±25 mV (setting range 2)
	Wakeup current	±20 % (10 times mode, sense resistor 5mΩ, ±1A detection)
	Turbo boost current	±20 % (10 times mode, sense resistor 5mΩ, ±1A detection)
Wakeup current detection circuit Input scaling factor	10 times, 5 times, 2 times	

Caution.   If there is the same value in both setting range 1 and 2, setting range 1 is valid.

Internal 1.8V

Current integrating circuit

BCCMP[2:0] bit
SCCMP[4:0] bit
DOCCMP[5:0] bit
COCCMP[3:0] bit
WUCMP[6:0] bit
CWUCMP[6:0] bit
TBCON[6:0] bit

Ladder resistor
1step: 2.5mV

Comparator comparison voltage setting switch

BCEN bit
SCEN bit
DOCEN bit
COCEN bit
WUEN bit

BCRSTRT bit
SCRSTRT bit
DOCRSTRT bit
COCRSTRT bit
WURSTRT bit
CWURSTRT bit
TBRSTRT bit

BCDFLG bit
SCDFLG bit
DOCDFLG bit
COCDFLG bit
WUDFLG bit
CWUDFLG bit
TBDFLG bit

Overcurrent detection restart circuit

Overcurrent detection status circuit

BCEN bit
SCEN bit
DOCEN bit
WUEN bit

VSS

BCITIM[2:0] bit

Discharge short-circuit current detection 1 time counter

BCFETEN bit

CCSLP bit

ISENS0

ISENS1

Current integrating circuit/ overcurrent detection circuit ISENS switch

SCITIM[3:0] bit

Discharge short-circuit current detection 2 time counter

S Q
R

S Q
R

SCFETEN bit

DFET control
L:ON
H:OFF
(When detect)

DOCITIM[3:0] bit

Discharge overcurrent detection time counter

S Q
R

DOCFETEN bit

COCITIM[3:0] bit

Charge overcurrent detection time counter

S Q
R

COCEN bit

COCFETEN bit

CFET control
L:ON
H:OFF
(When detect)

Level shift circuit (+1.1V)

Wakeup current detection preamplifier circuit

XCIN/128

Wakeup discharge current detection time counter

S Q
R

WUCMPCAL bit

Level shift circuit (+1.1V)

WUGAIN

Level shift circuit (+1.1V)

10 times/ 5 times

Overcurrent detection comparator

Wakeup charge current detection time counter

S Q
R

Turbo boost current detection time counter

S Q
R

Overcurrent detection interrupt

Wakeup detection interrupt

Remarks
1. In order to output over-current detection interruption at the time of detection, be sure to set BCINTEN bit, SCINTEN bit, DOCINTEN bit, or COCINTEN bit to 1, and permit an interruption output.
2. In order to output the wake-up current detection interruption at the time of detection, be sure set WUINTEN bit or CWUINTEN bit to 1, and permit an interruption output.
3. Since the wake-up current detection function and the turbo boost current detection function are sharing one comparator, they serve as exclusion use in one of functions.
    Be sure set up in the TBMODSEL bit of WUDCON2 register.

Figure 4-10 Block Diagram of Overcurrent Detection Circuit

4.6.7   Series Regulator

The RAJ240047 incorporates a low-dropout 1.8 V and 3.3 V output series regulator. The 1.8 V regulator is used as the power source of A/D converter, current integrating circuit. The 3.3 V regulator is used as 3.3 V power supply.
Figure 4-11 shows the Block Diagram of Series Regulator.
Pch MOS transistors are used for output control. No external resistor or equivalent is required because output voltages are adjusted in the IC.
Attach a 2.2 µF capacitor to the VREG2 output and a 1.0 µF capacitor to the VREG1 to suppress input and load fluctuations.
The settling time after input, output, and load fluctuations should be 10 ms as a standard value.
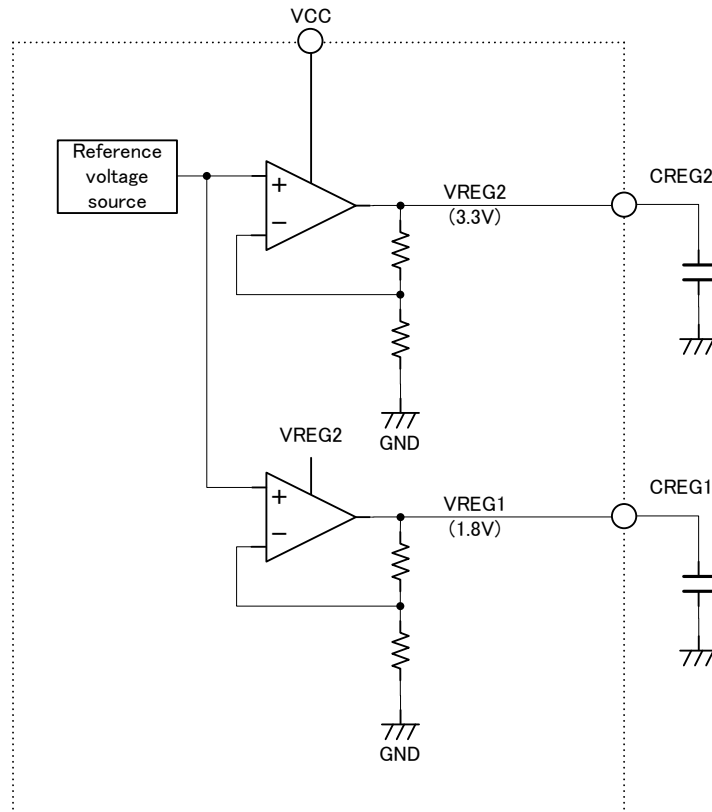
Figure 4-11 Block Diagram of Series Regulator

4.6.8   Reset Circuit

The reset circuit makes RESET (AFE) pin high level or low level by an output of power-on reset circuit or a reset request from MCU runaway detection circuit.

The reset circuit monitors 3.3 V and 1.8 V output voltage of the regulator circuit (VREG2, VREG1).

When the reset circuit detects voltage more than the reference value RESET (AFE) pin output becomes high level. When the reset circuit detects voltage lower than the reference value, the RESET (AFE) pin output signal becomes low level.

The reset circuit comprises comparators, a reference voltage, a Delay circuit, bleeder resistors, and N-ch transistor. The reset circuit output is N-ch transistor, RESET (AFE) output is high or low level depend on pull-up resistor built-in RESET (AFE) pin. The reset circuit provides hysteresis for the detection voltage and the cancel voltage. RESET (AFE) pin connects to RESET (MCU) pin and it uses as MCU hardware reset.

Figure 4-12 shows the Block Diagram of Reset circuit.
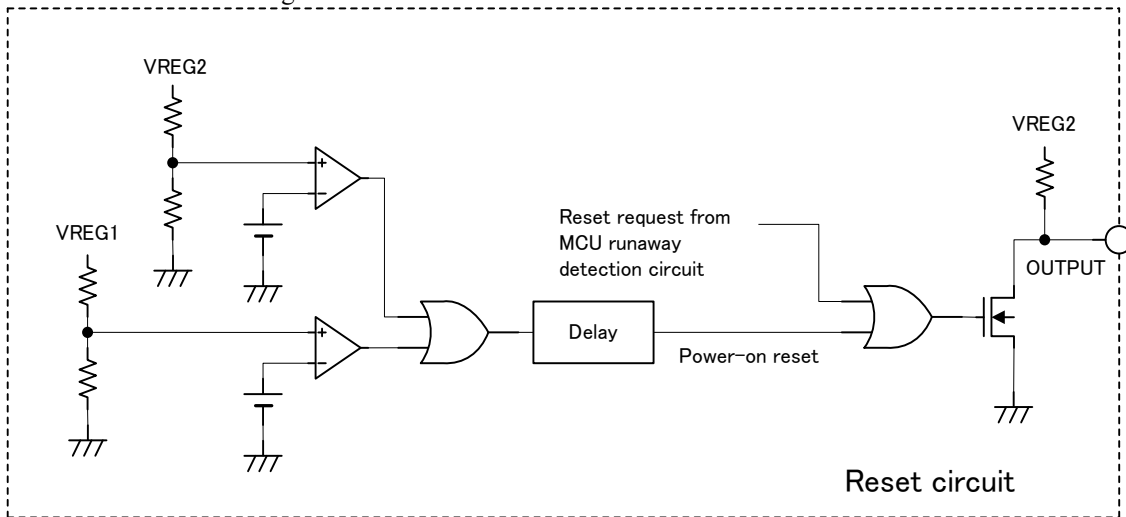
Figure 4-12 Block Diagram of Reset circuit

4.6.9   Serial Interface IICA

Serial interface IICA has the following three modes.

1. Operation stop mode
    This mode is used when serial transfers are not performed. It can therefore be used to reduce power consumption.

2. I^2C bus mode (multimaster supported)
    This mode is used for 8-bit data transfers with several devices via two lines: a serial clock (SCLA0) line and a serial data bus (SDAA0) line.
    This mode complies with the I^2C bus format and the master device can generated "start condition", "address", "transfer direction specification", "data", and "stop condition" data to the slave device, via the serial data bus. The slave device automatically detects these received status and data by hardware. This function can simplify the part of application program that controls the I^2C bus.
    Since the SCLA0 and SDAA0 pins are used for open drain outputs, serial interface IICA requires pull-up resistors for the serial clock line and the serial data bus line.

3. Wakeup mode
    The STOP mode can be released by generating an interrupt request signal (INTIICA0) when an extension code from the master device or a local address has been received while in STOP mode. This can be set by using the WUP0 bit of IICA control register 01 (IICCTL01).

●

Figure 4-13 shows a block diagram of serial interface IICA.
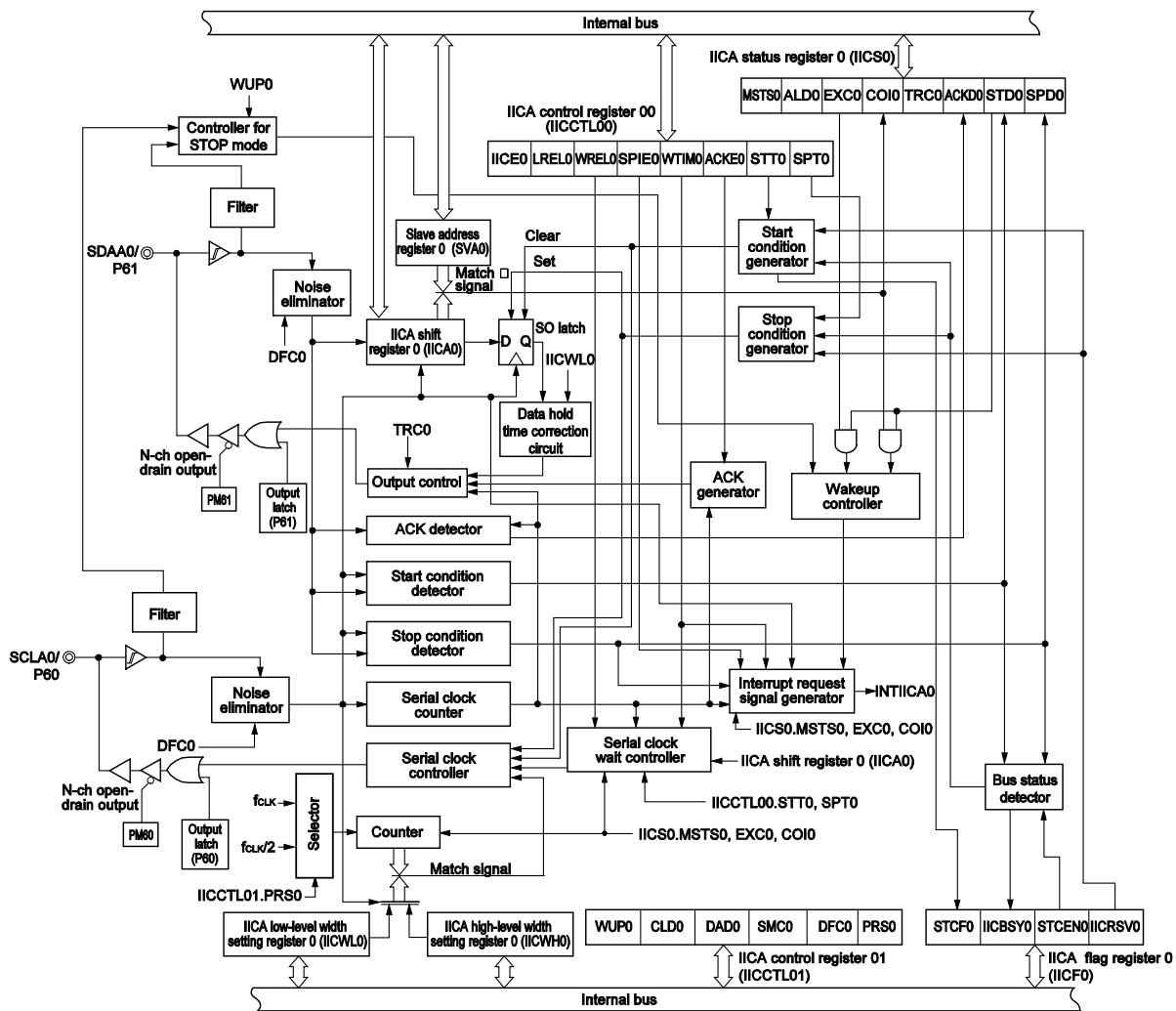
Figure 4-13 Block Diagram of Serial Interface IICA

4.6.10   Serial Array Unit

Serial array unit has four serial channels. Each channel can achieve 3-wire serial (CSI), UART, and simplified I²C communication.

1.   3 wire serial I/O (CSI11, CSI21)

Data is transmitted or received in synchronization with the serial clock ($\overline{\text{SCK}}$) output from the master channel.
3-wire serial communication is clocked communication performed by using three communication lines: one for the serial clock ($\overline{\text{SCK}}$), one for transmitting serial data (SO), one for receiving serial data (SI).

[Data transmission/reception]
- Data length of 7 or 8 bits
- Phase control of transmit/receive data
- MSB/LSB first selectable
- Level setting of transmit/receive data

[Clock control]
- Master/slave selection
- Phase control of I/O clock
- Setting of transfer period by prescaler and internal counter of each channel
- Maximum transfer rate
- During master communication: Max. $f_{CLK}/4$ **Note**
- During slave communication: Max. $f_{MCK}/6$ **Note**

[Interrupt function]
- Transfer end interrupt/buffer empty interrupt

[Error detection flag]
- Overrun error

It cannot be corresponding to SNOOZE mode in this product.

Note   Use the clocks within a range satisfying the $\overline{\text{SCK}}$ cycle time (t_{KCY}) characteristics (see 3 ELECTRICAL SPECIFICATIONS).

2.   UART (UART0)

This is a start-stop synchronization function using two lines: serial data transmission (TxD) and serial data reception (RxD) lines. By using these two communication lines, each data frame, which consist of a start bit, data, parity bit, and stop bit, is transferred asynchronously (using the internal baud rate) between the microcontroller and the other communication party. Full-duplex UART communication can be performed by using a channel dedicated to transmission (even-numbered channel) and a channel dedicated to reception (odd-numbered channel). The LIN-bus can be implemented by using timer array unit with an external interrupt (INTP0).

[Data transmission/reception]
- Data length of 7, 8, or 9 bits
- Select the MSB/LSB first
- Level setting of transmit/receive data and select of reverse
- Parity bit appending and parity check functions
- Stop bit appending

[Interrupt function]
- Transfer end interrupt/buffer empty interrupt
- Error interrupt in case of framing error, parity error, or overrun error

[Error detection flag]
- Framing error, parity error, or overrun error
- It cannot be corresponding to LIN-bus and SNOOZE mode in this product.

3. Simplified I²C (IIC11)

This is a clocked communication function to communicate with two or more devices by using two lines: serial clock (SCL) and serial data (SDA). This simplified I²C is designed for single communication with a device such as EEPROM, flash memory, or A/D converter, and therefore, it functions only as a master.

Make sure by using software, as well as operating the control registers, that the AC specifications of the start and stop conditions are observed.

[Data transmission/reception]

- Master transmission, master reception (only master function with a single master)
- ACK output function and ACK detection function
- Data length of 8 bits (When an address is transmitted, the address is specified by the higher 7 bits, and the least significant bit is used for R/W control.)
- Manual generation of start condition and stop condition

[Interrupt function]

- Transfer end interrupt

[Error detection flag]

- Parity error (ACK error), or overrun error

[Functions not supported by simplified I²C]

- Slave transmission, slave reception
- Arbitration loss detection function
- Wait detection functions

4.6.11   Conditioning circuit

The conditioning circuit is equipped with a function to internally discharge each cell of the battery connected. This function can decrease the voltage of an overcharged battery, which increases the safety of the battery pack. In addition, voltages between connected battery cells can be the same voltage, allowing full charge of all cells. This enables the battery pack to be used for a long period. The MCU selects a cell for self-discharge. Conditioning control is enabled by controlling the switches with the serial data from the MCU.

The conditioning circuit comprises MOS switches and logic circuit. Any battery cell (Vcell1 to Vcell5) can be set for self-discharge by setting the CDRON0 to CDRON 4 bit in the COND register.

Figure 4-14 shows the Block Diagram of Conditioning Circuit.
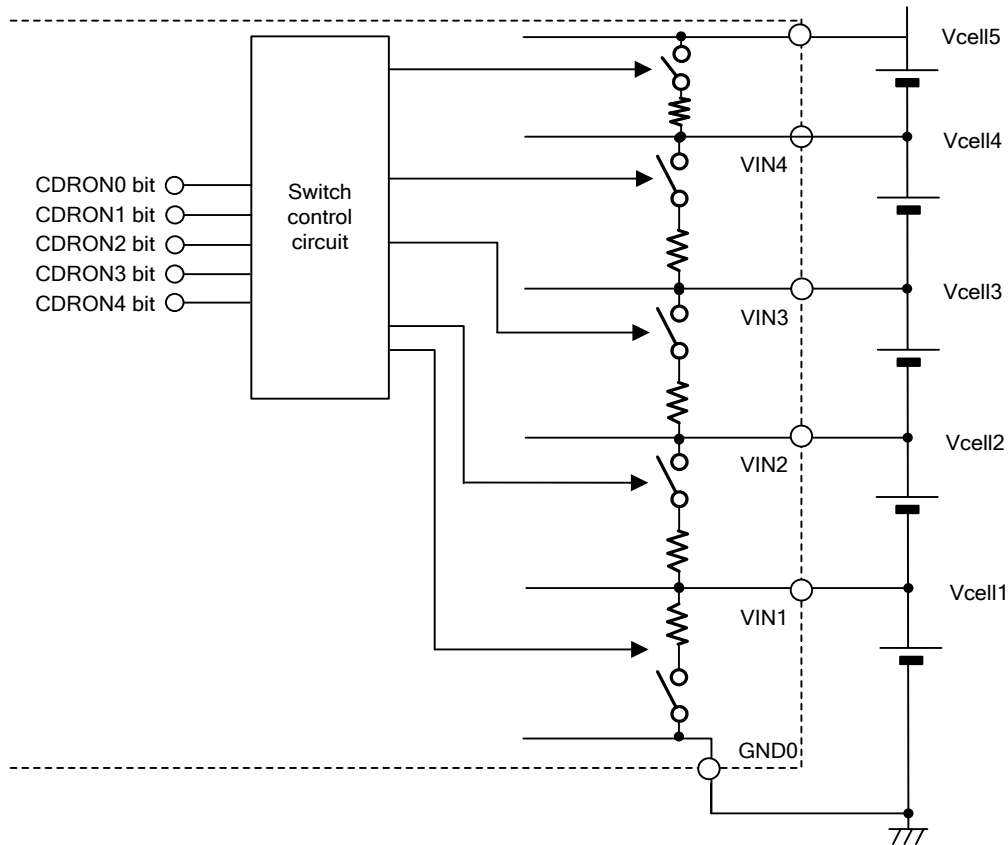
Figure 4-14 Block Diagram of Conditioning Circuit

4.6.12 Fuse control circuit

The fuse control circuit is used for a system controlling a fuse used for cutting charge/discharge path at the time of the abnormality. In addition, this fuse control circuit is able to read the failure mode identification register data from MCU after the fuse was cut off. It is possible to identify the failure mode.

Figure 4-15 shows Example for the Fuse Control System.

1. Fuse control
   When abnormal state is detected by MCU write the FUSECUT0, FUSECUT1 bit in the AFECON2 register to 11b, FUSEOUT pin becomes High level, and turn on the fuse cutting FET.
2. The failure mode identification
   It can read a state of FUSEOUT pin by reading the FUSEMON bit in the AFECON3 register.
   The FUSEOUT pin becomes HiZ level when VCC level output can't be controlled by fuse control function.
   Therefore it can detect a state that the fuse cutting FET is ON by the fuse cutting FET by reading the FUSEMON bit.

Input of FUSEOUT pin connects to P06/INTP11 of MCU internally, when FUSEOUT pin becomes VCC level it can detect external interrupt of MCU.
By INTP11 interrupt during fuse cut off, write the values of FUSECUT0, FUSECUT1, and FUSEMON bit in the flash memory. To read that written data from flash memory after fuse was cut off, it is possible to identify the failure mode.
The Interrupt request pin of FUSEOUT that connects to P06/INTP11 of MCU internally is the INT_AFE_ANL (abnormal interrupt).

Note.   INT_AFE_ANL is shared many AFE causes of interrupt. Therefore, confirm a cause of FUSEOUT pin by reading the FUSEIR bit in the INTIR register.
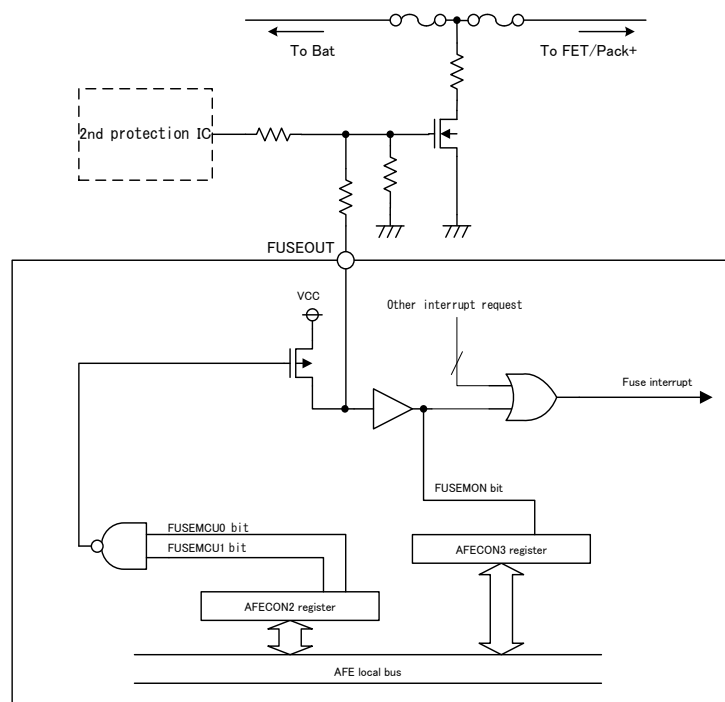
Figure 4-15 Example for the Fuse Control System

4.6.13   High voltage port

This product contains the high voltage port. Mounted high voltage port in this product is SYSIN pin.

SYSIN pin is able to use as input pin of system presence function which is recognized to connect up battery pack to main system.

SYSIN pin output connects P30/INTP3 of MCU in package, when L level inputs it can detect external interrupt (INTP3). Figure 4-16 Block diagram of SYSIN pin shows Block diagram of SYSIN pin.
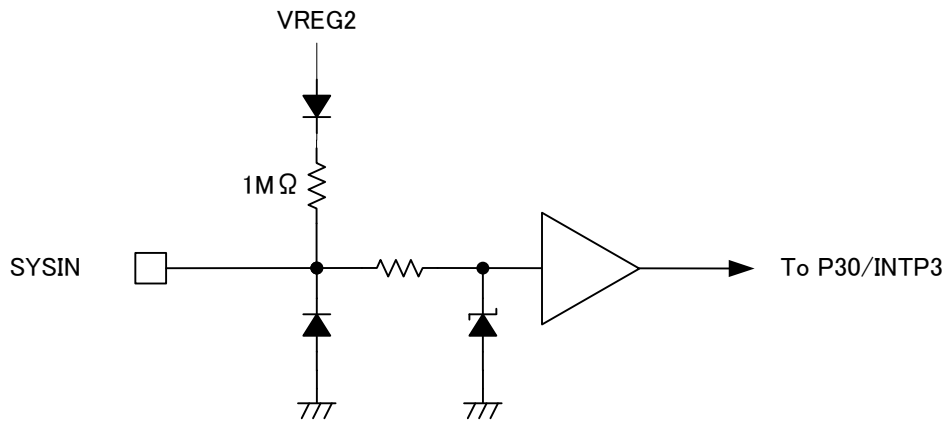
Figure 4-16 Block diagram of SYSIN pin

4.6.14   MCU runaway detection Circuit

MCU runaway detection circuit can be detected an MCU runaway. It can be monitoring CPU runaway independently of MCU watchdog timer.

MCU runaway detection circuit comprises pre-scaler to be divided AFE on-chip oscillator and 16 bits counter. It can be selected the overflow time from 2, 4, and 8 [s]

Table 4-6 shows MCU runaway detection circuit specification, Figure 4-17 shows Block Diagram of MCU runaway detection circuit.

Table 4-6 MCU runaway detection circuit specification

Item	Specification
Overflow time	2, 4, 8 [s]
Count source	AFE on-chip oscillator divided by 4
Counter bit length	19 bits

Operation of the overflow	(1) Overflow for first time
	• set the WDTIR bit to 1
	(2) Overflow for second time
	  when the MTRSEL bit is "0"
	• clear the FETC bit and the FETD bit to 0
	  when the MTRSEL bit is "1"
	• clear the FETC bit and the FETD bit to 0
	• MCU runaway detection reset is generated.

Refresh conditions	• P76 of MCU is applied to H pulse to WDTIN pin **Note**. • Power-on reset • Overflow time change

Note   The P76 of MCU is connected to WDTIN inside package. Also the WDTIN incorporated the pull-down resistor.
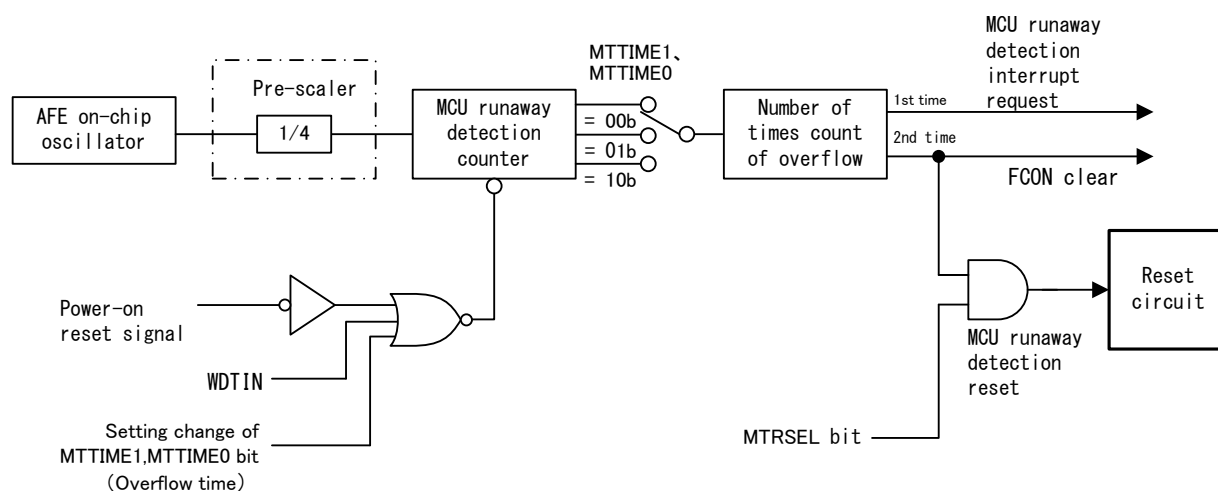
MTTIME1、MTTIME0、MTRFRSH : Bit of AWDTCON register
FCON : FET driver control register
WDTIN : Refresh signal input (The contact port between MCU and AFE).

Figure 4-17 Block Diagram of MCU runaway detection circuit

5. Application Guideline

5.1   Typical Application Specification

Typical specification example of Li-ION battery management unit is shown below.

Battery cell assembly : 4S1P (4 cells in series and 1 cell in parallel)
Host interface   : System Management Bus (SMBus) Specification, version 1.1.
Primary protection   : charge FET and discharge FET
Secondary protection : Fuse blow by FGIC (RAJ240047) or a secondary protection device.
Connector pins:
      Pack+   Positive battery pack terminal
      SMC   SMBus clock
      SMD   SMBus data
      B/I   Battery insertion detection
      Pack-   Negative battery pack terminal
External reverse charge protection circuit
Battery temperature measurement with two thermistors

5.2   Typical Application Circuit

Typical Application Circuit Schematic
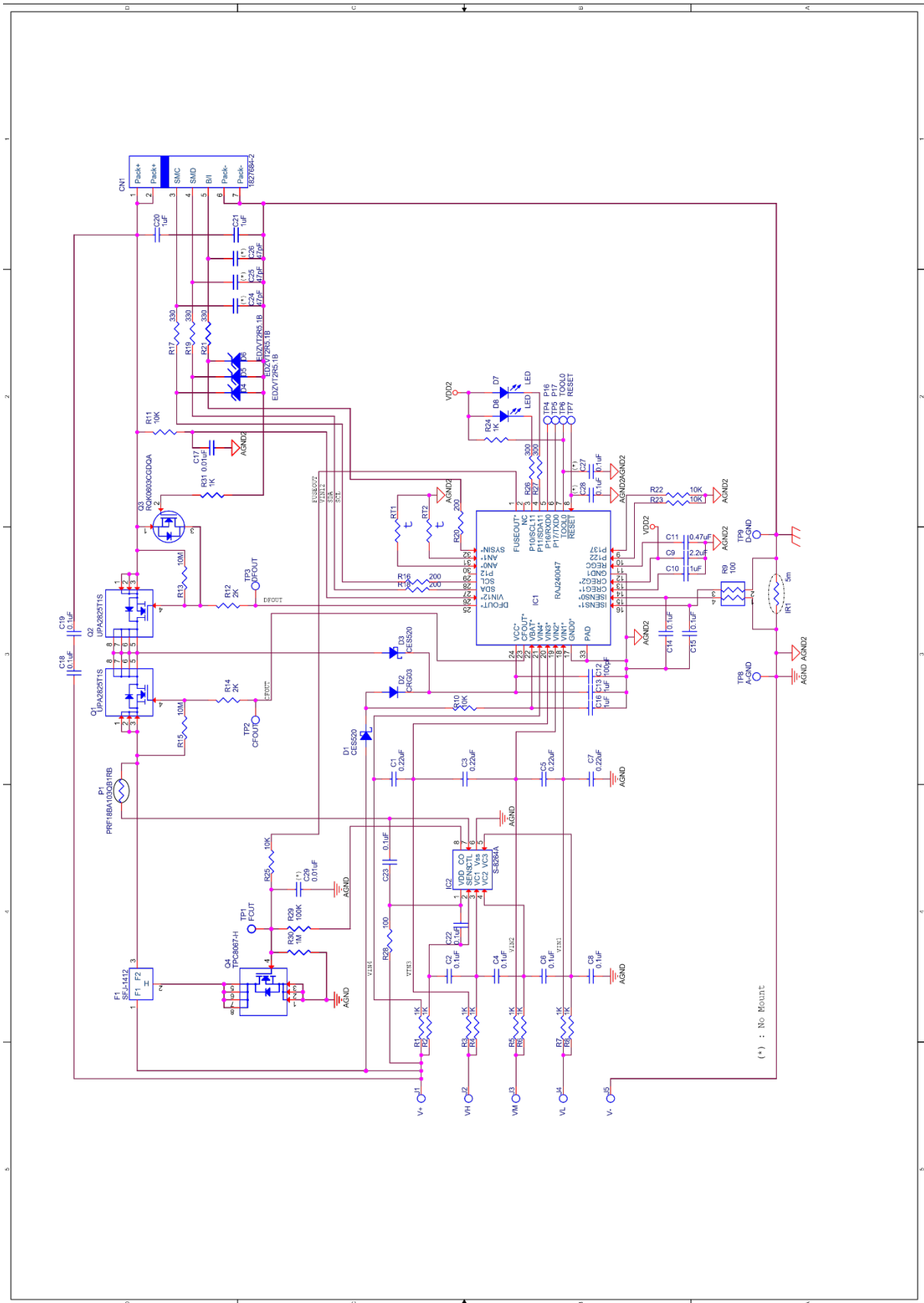
5.3   Circuit Design Guideline

5.3.1   Cell voltage monitor circuit

- Provide input filter independently for RAJ240047 and 2nd protection IC.
- Place resistors around 1kohm to VIN1 – VIN4 as they works also as surge protection. 0.22uF is recommended for C1, C3, C5 and C7 so cut-off frequency become 0.7 KHz with 1kohm.
- Higher cut-off frequency can be set if it's OK with voltage detection accuracy.
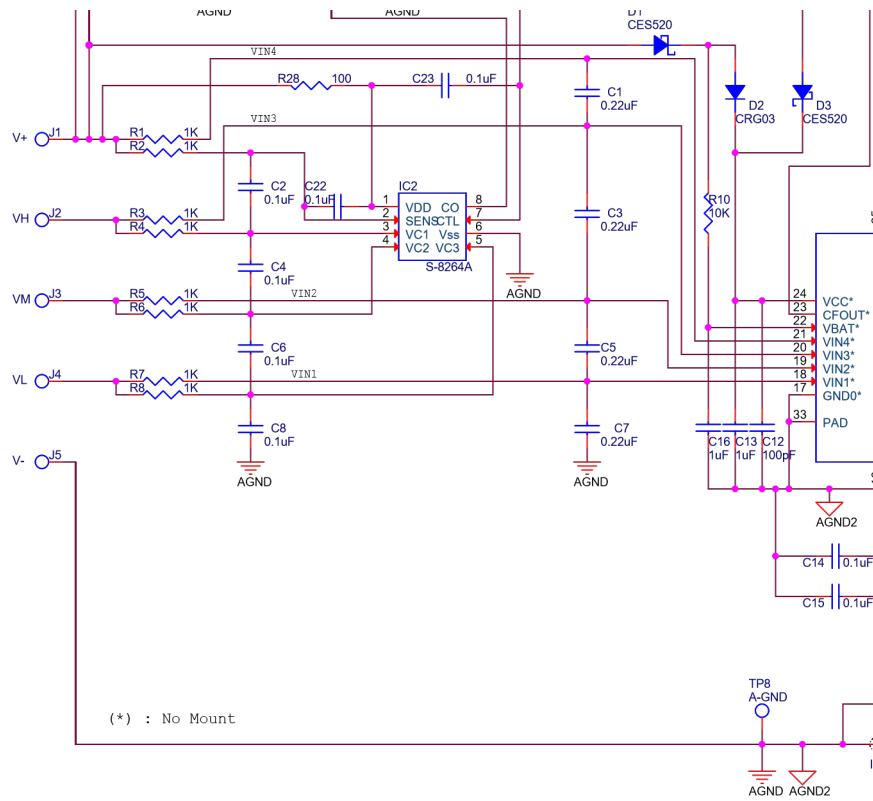
5.3.2   Charger connect detection circuit

- R11 plays a role for current limit when charger is reverse-charged. 10kΩ is recommendable, but when it is too large, charger connect detection circuit may operate erroneously.
- C17 works for stable charger connect detection and D-FET boost operation. 0.01µF is recommendable. If it is too large, OFF time when short-circuited will be long, if it is too small, boosted voltage may fluctuate.
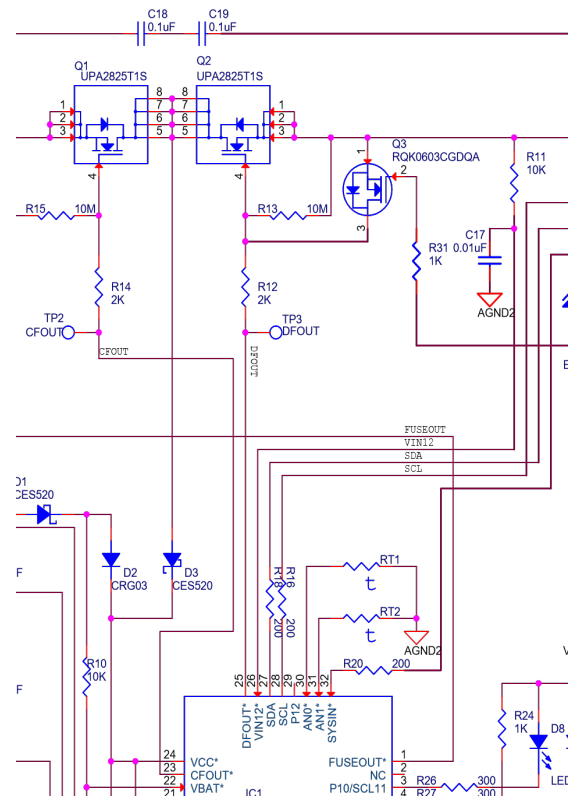
5.3.3   Current monitor

- Potential difference on sense resistor is monitored by current integration circuit.
- Put Low Pass Filter (100 Ω, 0.1µF) for input stage.
- Sense traces should be shielded for detecting small voltage difference.
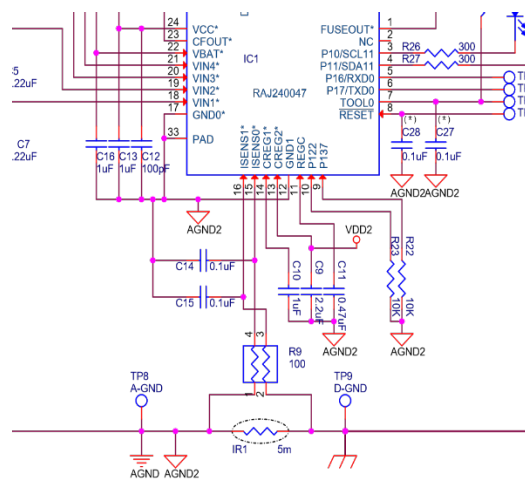
5.3.4 Fuse control

SPC is used for fuse.

The fuse is blown by the following three paths.
1. RAJ240047 drives FUSEOUT pin high to make Q4 ON.
2. When 2nd protection IC detects overcharge voltage, CO becomes high to make Q4 ON.
3. When posistor resistance becomes large by high temperature, CTL of 2nd protection IC becomes high to make CO high, then to make Q4 ON.
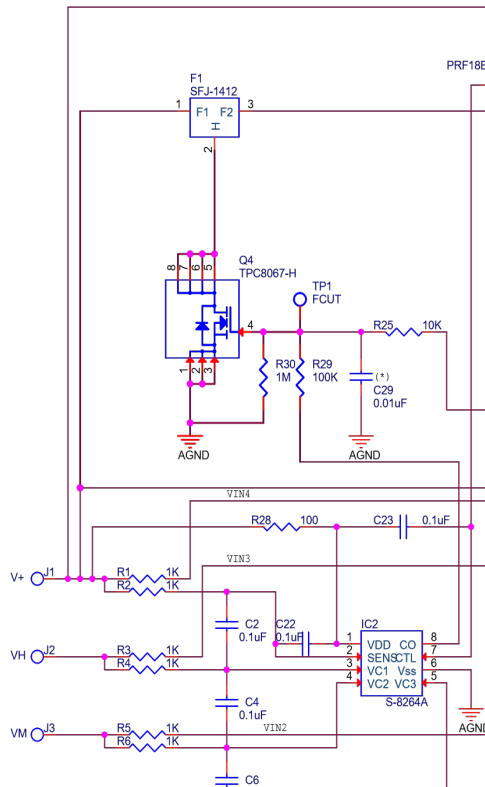
5.3.5 Protection FET control

- Q3 is located between gate and source of Q1 to make D-FET off when charger is reversely connected.
- R31 is for Q3 gate protection. (1kΩ is recommended.)
- R12/R14 are for gate protection and C-FET/D-FET noise reduction. (2kΩs is recommended.)
- R13/R15 are for fixing C-FET/D-FET gate voltage when FET is off. 10MΩs is recommended to prevent voltage drop.
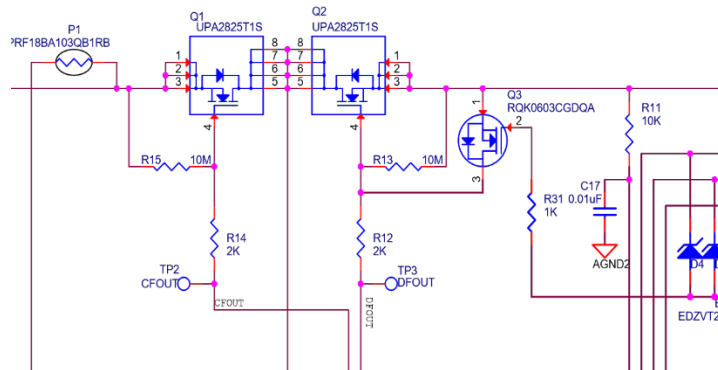
5.3.6   Thermistor

- ADC voltage measurement pins (AN0/AN1) are provided for thermistor use.
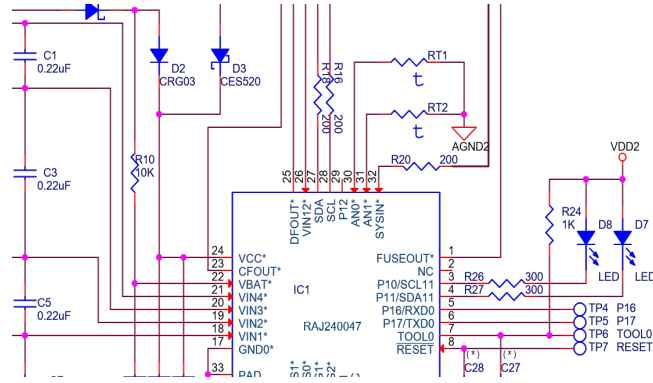
5.3.7   System presence

- Connect R21 (330 ohm) and R20 (200 ohm) for ESD protection at SYSIN input.
  Connect zener diode to protect against short-circuit with Pack+.
  Zener diode must be the one with its zener voltage less than 6.5V, an absolute maximum rating of VDD2.

5.3.8   Communication line

- Connect R17, R19 (330 ohm) and R16, R18 (200 ohm) for ESD protection at SCL/SDA input.
  Connect zener diode to protect against short-circuit with Pack+.
  Zener diode must be the one with its zener voltage less than 6.5V, an absolute maximum rating of VDD2.
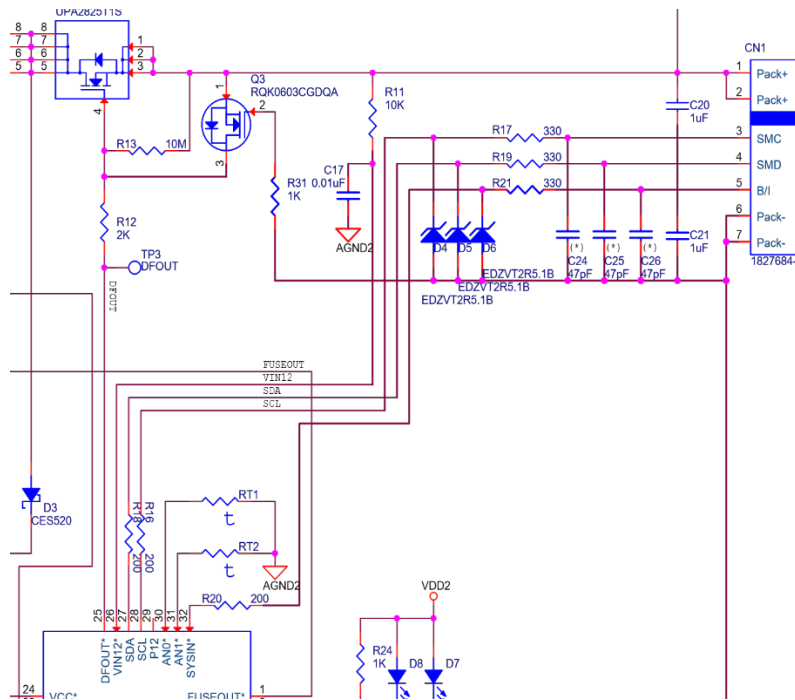
5.3.9   Power supply path

Power supply is provided to VCC through the following two paths.

1. Higher voltage out of battery and charger is provided as power supply.
2. Power supply is provided from battery side when fuse is blown.
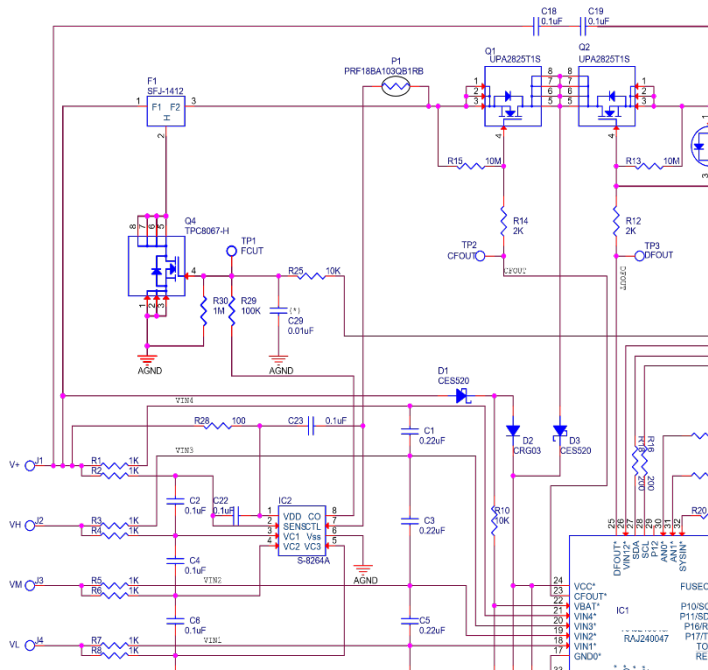
5.3.10   CREG1/CREG2/REGC capacitance

The following decoupling capacitor must be located as adjacent to each terminal as possible.
C10: CREG1/AGND2 (1μF is recommended.)
C9: CREG2/AGND2 (2.2μF is recommended.)
C11: REGC/AGND2 (0.47μF to 1μF is recommended.)
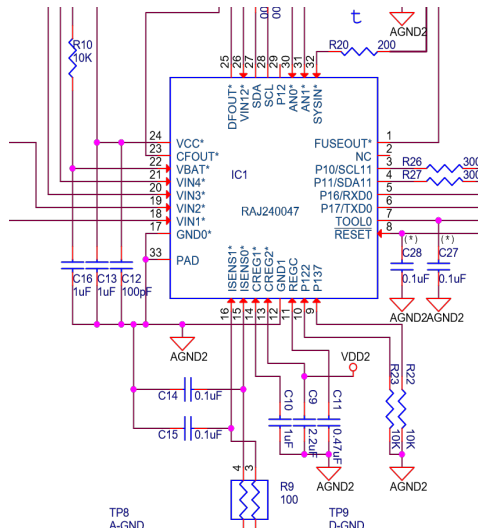
5.4 Layout Guidelines

5.4.1 Summary

- Large current patterns must be wide and short to minimize voltage drop and the heat generation.
- Bypass capacitors must be mounted as close as possible to the device VCC / VBAT and GND pins to prevent erroneous operations due to noise from power supply.
- Capacitors for voltage regulators must be located close to regulator pins to ensure loop stability and ESD tolerance.
- All IC ground must be connected to the negative terminal of battery cells except ground for communication lines.
- Communication lines must be away from small signal current sense line to prevent the input signal from being disturbed by the incoming radiation noise.
- RAJ240047 must be located away from any heat source (FET, current sense resistor and large current patterns) to minimize the influence of heat.
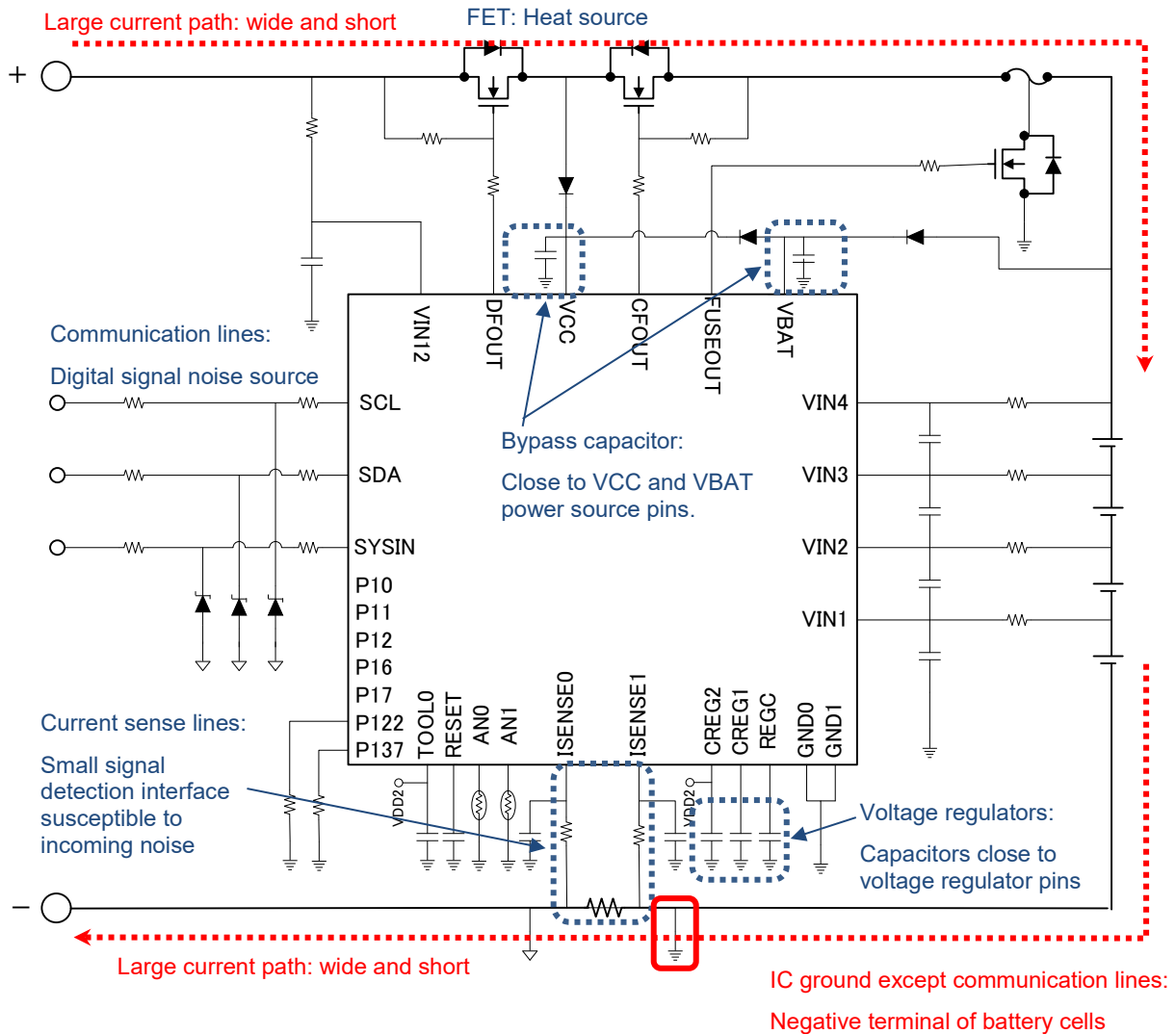
5.4.2   ESD protections on each terminal (basic policy)

- ESD applied on Pack+ terminal must be lead to the top side of the cell or to Pack- terminal through a capacitor.
- ESD applied to Pack- terminal must be lead to the GND side of the cell.
- ESD applied to communication terminals and other GPIOs must be lead to the GND side of the cell via Pack-terminal.
- The noise from PACK+ or PACK- must be lead to battery cell so that it will not interfere with RAJ240047 functions and measurements.
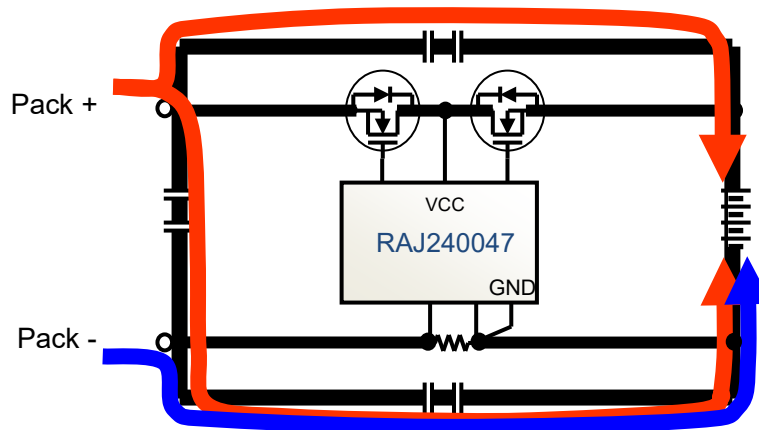
5.4.3   Pack+, Pack-

- Bypass capacitor must be placed between Pack+ and Pack-. (Countermeasure against ESD)
- Bypass capacitor must be located adjacent to Pack+, Pack-. (Minimize the ESD influence)
- Capacitors must be placed in series. (Countermeasure against short-circuit of capacitors)
- Don't use tantalum capacitor. (Tantalum capacitor can end up with short-circuited failure when damaged.)
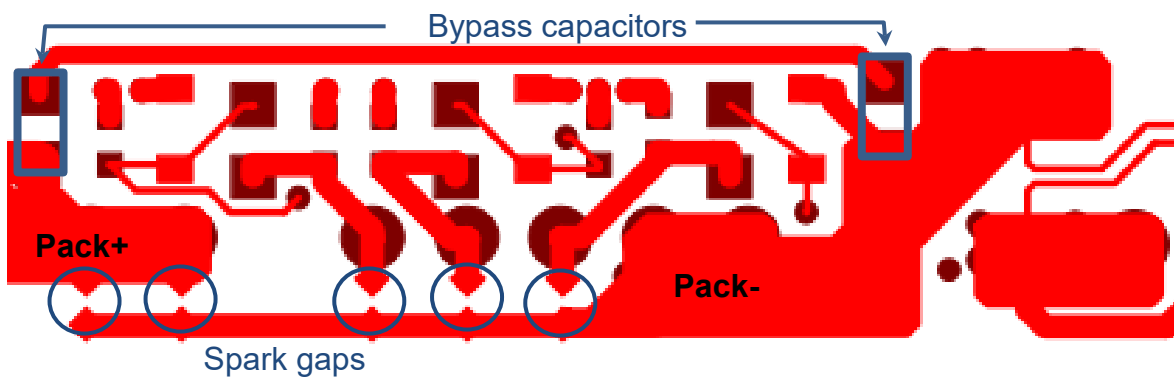
5.4.4   How AGND and AGND2 must be connected to the ground

- AGND and AGND2 of RAJ240047 must be connected to the one point of current detection resistor of the cell side by the pattern with an adequate width. (Prevent potential variation by large current.)
- The patterns between AGND and AGND2 must not be divided. (Keeping the GND potential of MCU and AFE equal)
- The lines from cell GND to current sensing resistor must be wide and as short as possible to avoid potential difference generated between cell GND and RAJ240047 when current flows.
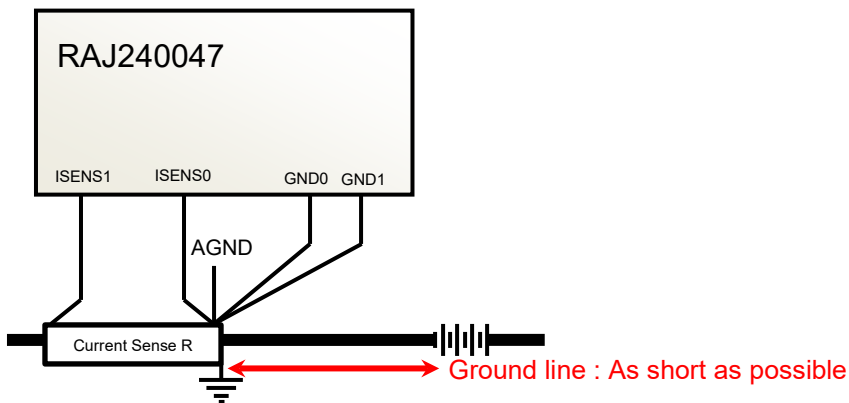
5.4.5   Bypass capacitor between VCC and GND0

- The patterns between VCC pin and a bypass capacitor and between GND0 pin and a bypass capacitor must be as short as possible and the same in length with each other. (Countermeasure for ESD) RAJ240047 and bypass capacitors must be placed on the same side of PCB without any through-hole.
- The lines to bypass capacitor must be wide and short. (To keep bypass capacitor effective in suppressing the potential variation.)
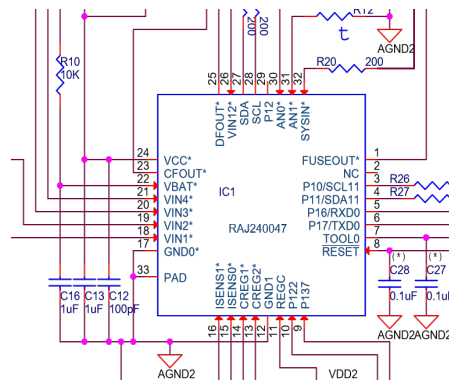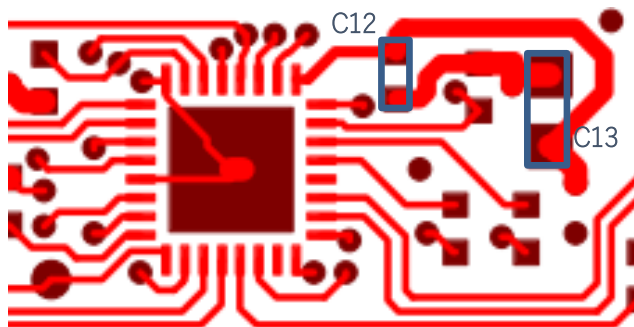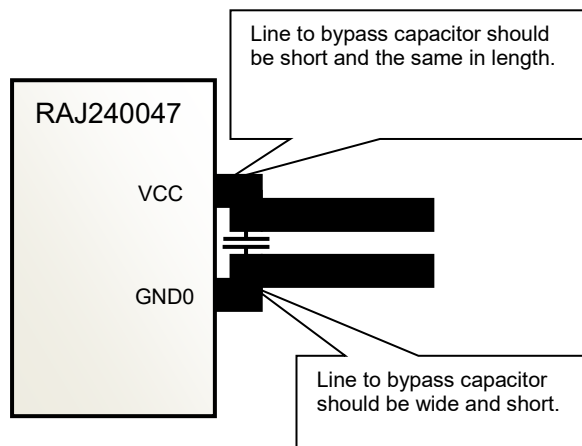
5.4.6 ISENS0, ISENS1

- Two lines from current sense resistor to ISENS0, ISEN1 must be the same in width and length, and in parallel with the same space between the two lines. (Prevent erroneous detections due to noise)
- The space between lines to ISENS0 and ISENS1 must be filled up with the shielding pattern one which is connected to GND. Also, the layer on the pack side of board must also be filled up with the shielding pattern. (Prevent erroneous detections due to noise)
- There must be no unnecessary divergence between current sense resistors to ISENS0 and ISENS1. (Incoming noise from the pattern unnecessarily divergence.)
- Capacitors connected to shielding pattern are recommended to be located adjacent to RAJ240047. (Countermeasure against noise)
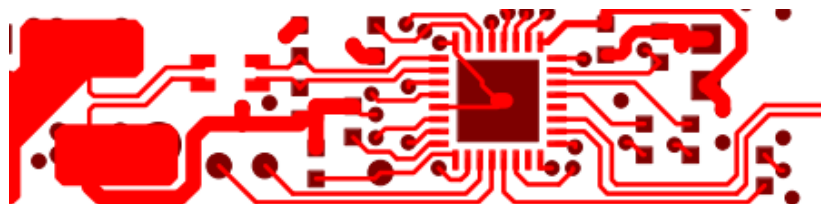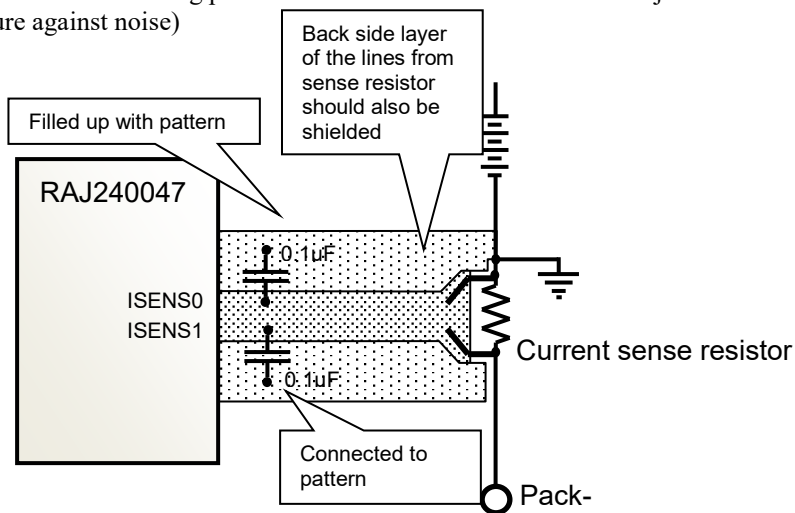
5.4.7 SMBus

- SMBus lines must be equipped with zener diodes. And it is necessary to mount resistors on the side of RAJ240047 and D-GND. (Zener diode and the resistor on the side of D-GND are for surge countermeasure, the resistor on the side of FG-IC for noise countermeasure.)
- The resistor on the side of RAJ240047 must be located as adjacent to FG-IC as possible. (Countermeasure for noise)

5.4.8 Unused Pins

- Unused pins are recommended to be connected to GND via resistor. (It is connected via resistor to GND against ESD. Setting low output by software prevents the terminal from becoming indefinite).

5.4.9 Cell GND

- The lines from cell GND to current sensing resistor must be wide and as short as possible. (To avoid potential difference generated between cell GND and RAJ240047 when current flows. Cell voltage on the side of GND cannot be detected correctly when potential difference is generated.)

6. Packaging Information

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-HVQFN32-4x4-0.40	PVQN0032LC-A	———	0.04g

Index area

Detail F

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	3.9	4.0	4.1
E	3.9	4.0	4.1
A	——	——	0.95
A1	0	——	——
b	0.15	0.2	0.25
e	——	0.4	——
Lp	0.20	0.30	0.40
x	——	——	0.05
y	——	——	0.05
ZD	——	0.6	——
ZE	——	0.6	——
D2	——	2.65	——
E2	——	2.65	——
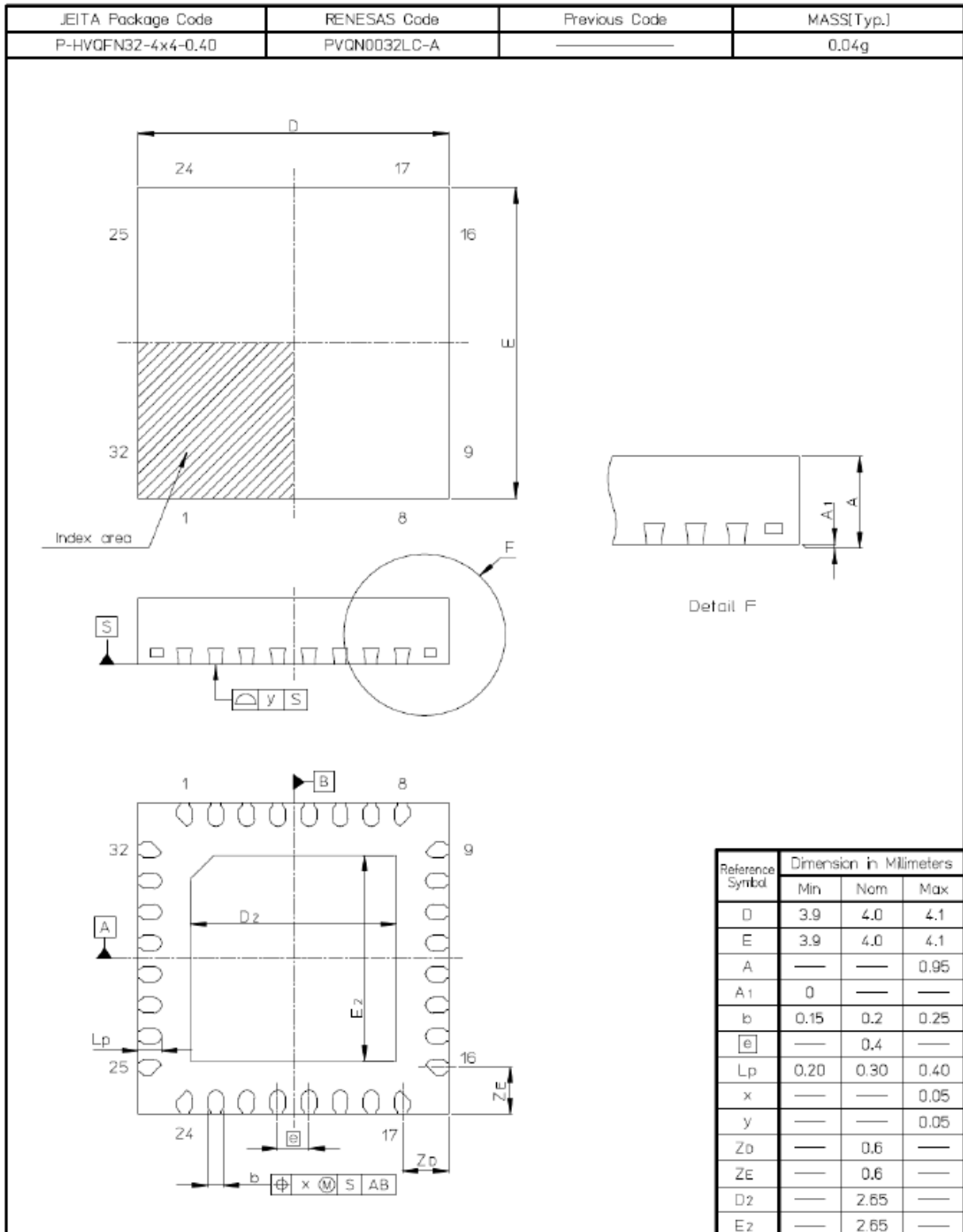
Revision History

Rev.	Date	Description		
		Page	**Summary**	
1.00	July 12, 2017		First Version	
1.01	Feb 15, 2019		Product lineup revision	

All documents should contain the following section break and paragraph as the last item. The footers of this document refer to the paragraph in order to reference the last page of the document.

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

    A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.

2. Processing at power-on

    The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.

3. Input of signal during power-off state

    Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.

4. Handling of unused pins

    Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.

5. Clock signals

    After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.

6. Voltage application waveform at input pin

    Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).

7. Prohibition of access to reserved addresses

    Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.

8. Differences between products

    Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.