ISL78083

Automotive Camera Power Management IC with Three Synchronous Buck Regulators and One Low Dropout Linear Regulator

The ISL78083 is a versatile multi-rail power IC comprised of a primary high voltage synchronous buck regulator, two secondary low voltage synchronous buck regulators, and an LDO regulator. It also offers four overvoltage and undervoltage monitors, three power-good indicators, and a reset output/fault indicator. To limit common-cause failures, the ISL78083 also includes a second reference for the OV/UV monitors, independent from the reference of the regulators.

The ISL78083 is intended for high-density power applications, requiring few external components and minimal board space. It offers an extensive feature set configured using internal One-Time Programmable (OTP) memory. Nearly all device options, such as each output voltage selection, power sequencing, and OV/UV thresholds are internally configured and require no external components for selection. The regulators also offer internal compensation. The bucks are synchronous to achieve high efficiency and are capable of operating in harsh environments requiring high ambient temperature.

ISL78083 is available in a 4mmx4mm 24 Ld Step Cut QFN (SCQFN) package with an exposed pad for improved thermal performance. It is AEC-Q100 qualified to Grade 1 and operates across an ambient temperature range of -40°C to 125°C and is electrically specified across a junction temperature range of -40°C to 150°C.

Applications

- Rear and surround view HD automotive cameras
- Driver monitoring cameras
- HD dash cam

Features

- V_{IN} operating range from 4.0V to 42V
  - Start range: 4.5V to 42V
- Fixed switching frequency: 2.2MHz with optional pseudo-random spread spectrum
- Three synchronous bucks with internal compensation and one LDO
  - Buck1 output range: 3.3V to 5.05V
  - Buck2 output range: 1.0V to 3.3V
  - Buck3 output range: 1.0V to 3.3V
  - LDO4 output range: 2.8V to 3.4V
- Output UV/OV thresholds, OTP: ±4%, ±6%, ±8%, ±12%
- OTP power up/down sequence and delay
- Optional output discharge on Buck2, Buck3, and LDO4
- Current at VIN input under shutdown: <1µA typical
- Protection features
  - Input voltage UVLO
  - Output OV/UV
  - Positive and negative current limits on bucks
  - Overcurrent protection on internal and output LDOs
  - Fail-safe controller
  - CRC of OTP registers
  - OTP hiccup or latch-off fault response

Related Literature

For a full list of related documents, visit our website:

- ISL78083 device page

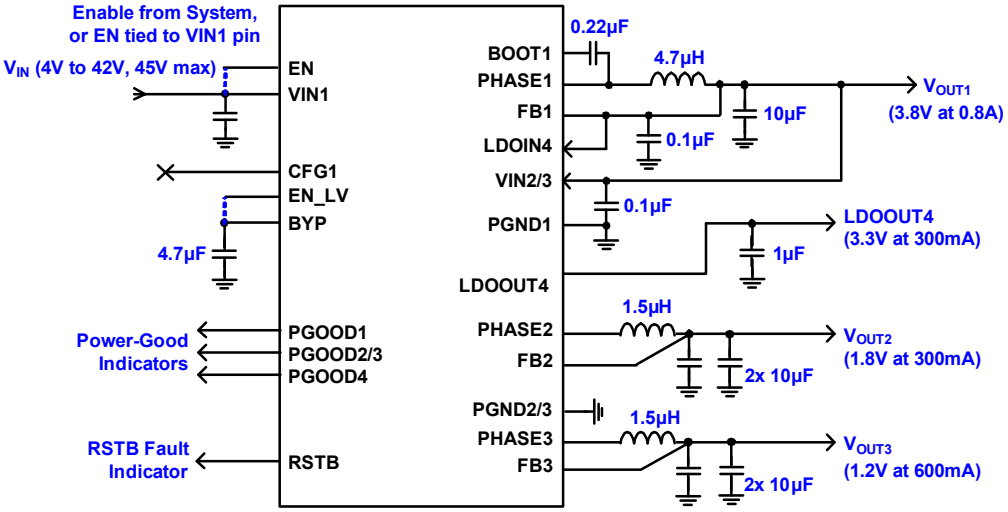


Figure 1. Typical Application

Contents

1. Overview

1.1 Typical Application Schematic

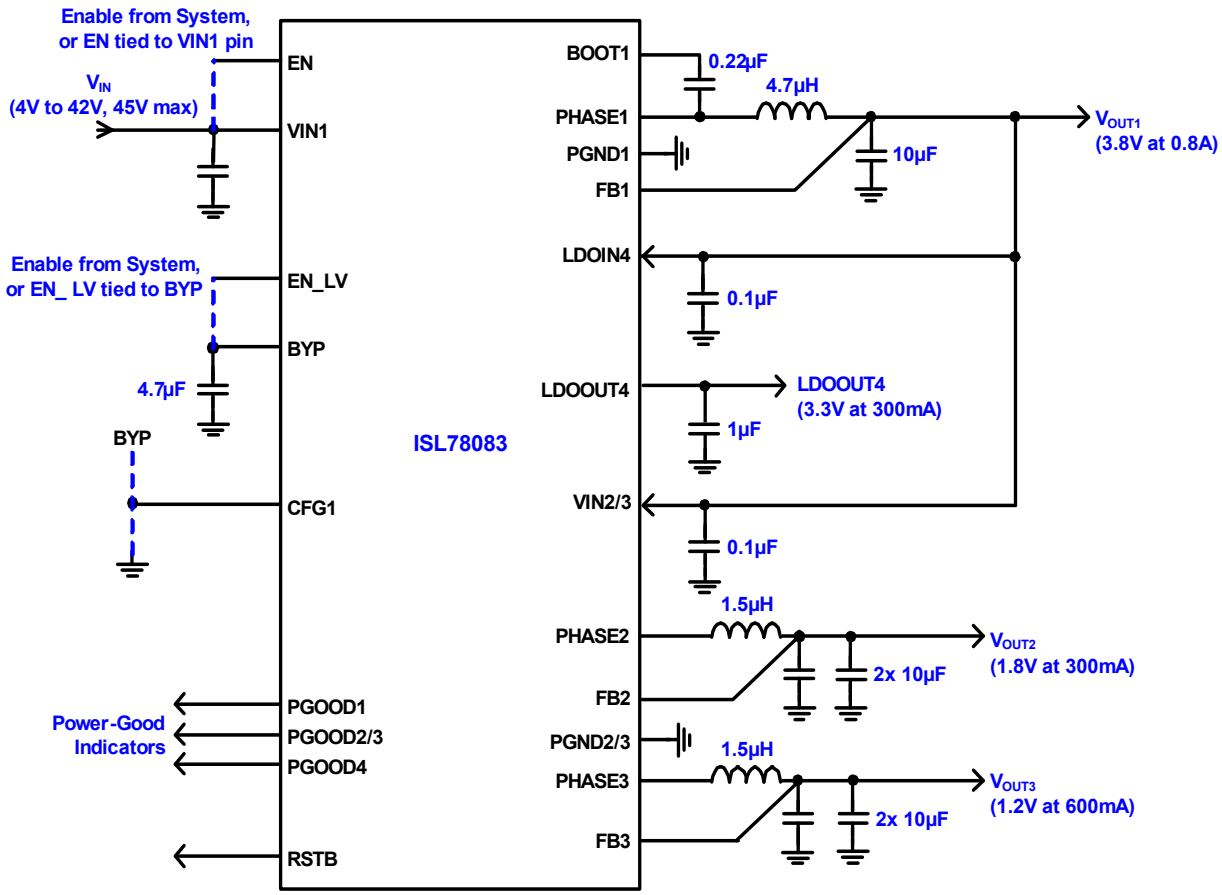


Figure 2. Typical Application Schematic

1.2 Block Diagram

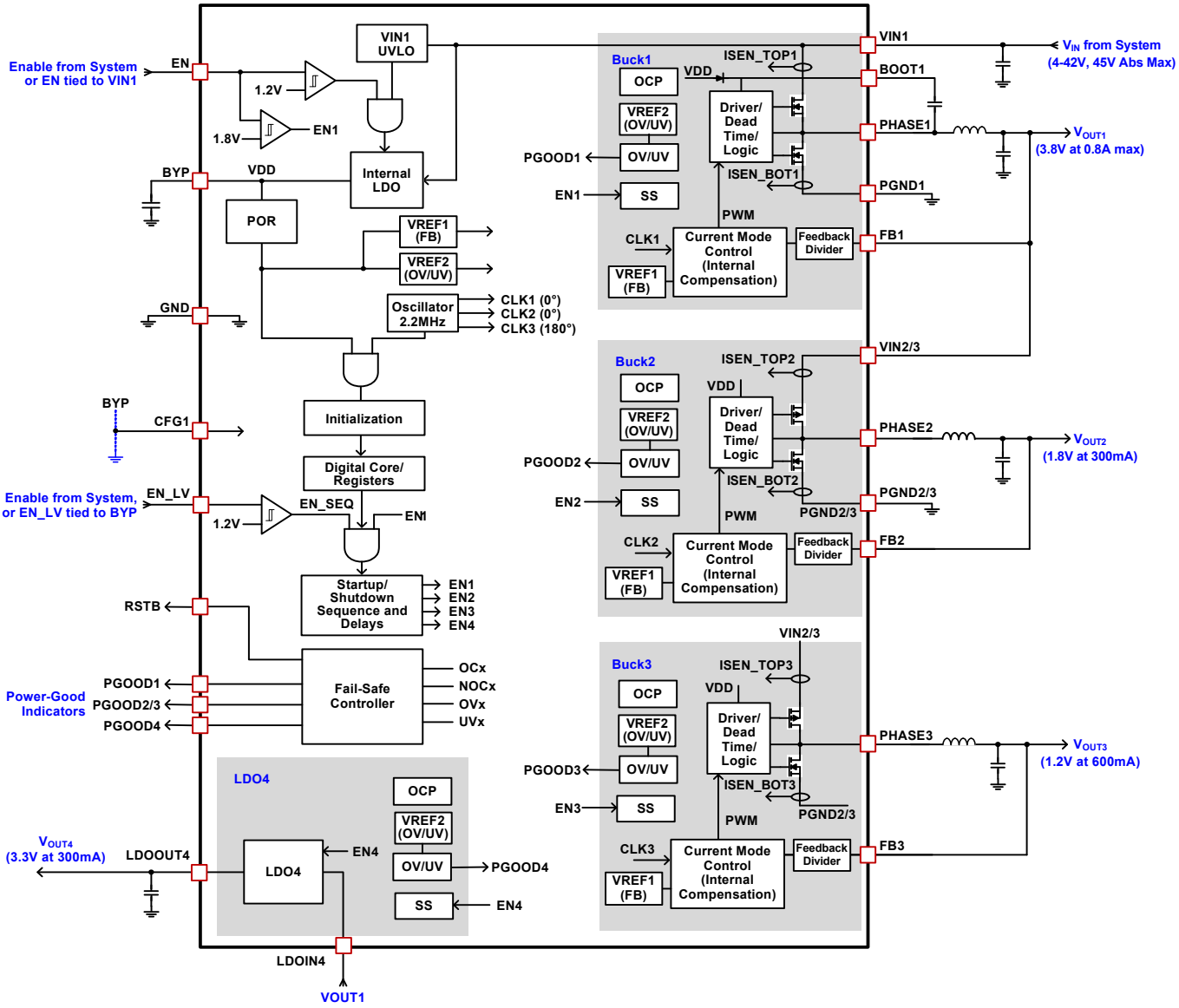


Figure 3. Block Diagram

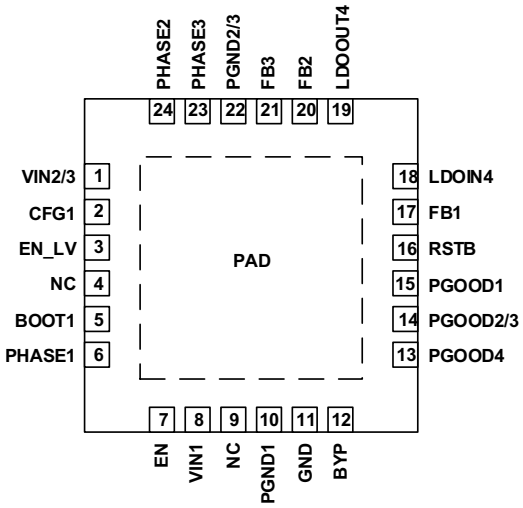
1.3 Ordering Information

Part Number (Notes 2, 3)	Part Marking	Temp Range (°C)	Tape and Reel (Units) (Note 1)	Package (RoHS Compliant)	Pkg. Dwg. #
ISL78083ARZ	78083 ARZ	-40 to +150	-	24 Ld SCQFN	L24.4x4K
ISL78083ARZ-T	78083 ARZ	-40 to +150	6k	24 Ld SCQFN	L24.4x4K
ISL78083ARZ-T7A	78083 ARZ	-40 to +150	250	24 Ld SCQFN	L24.4x4K

Notes:
1. See TB347 for details about reel specifications.
2. These Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J-STD-020.
3. For Moisture Sensitivity Level (MSL), see the ISL78083 device page. For more information about MSL, see TB363.

1.4 Pin Configuration

24 Ld QFN (Step Cut)
Top View



1.5 Pin Descriptions

Pin Name	Pin #	Description
VIN2/3	1	**Supply input for Buck2 and Buck3.** VIN2/3 must be connected to VOUT1. VIN2/3 supplies the high-side P-channel MOSFETs of the Buck2 and Buck3 switching regulators. Place ceramic decoupling capacitors (for example, 10µF in parallel with 0.1µF) from VIN2/3 to PGND2/3 and as close as possible to minimize the switching loop. The DC voltage applied to VIN2/3 should not exceed 5.5V during normal operation. The VIN2/3 pin can withstand voltage transients up to 7V.
CFG1	2	**Buck1 configuration input.** CFG1 is a tri-level control input that configures the Buck1 regulator for three different inductor and output capacitor ranges, depending on the application, for details see "Configure Pin" on page 11 in "Buck1 Electrical Specifications" on page 11. The three levels are (a) tied low to GND, (b) tied to BYP, and (c) open or floating. In the floating state, the CFG1 voltage is internally pulled to 50% (typical) of the BYP supply voltage. **Note:** The CFG1 pin state is read once and latched during Startup.
EN_LV	3	**Enable low voltage outputs control input.** EN_LV is a threshold-sensitive enable input to the chip that enables and disables the low voltage outputs (Buck2, Buck3, and LDO4). When EN_LV ≥ 1.2V (typical) and EN ≥ 1.8V (typical), the low voltage regulator startup sequencing begins. When EN_LV falls below 0.95V, the low voltage outputs turn off in reverse sequence. EN_LV is a low voltage pin with an operating input range of 0V to V_{BYP}.
NC	4, 9	**No connection.** Not internally connected. **Note:** This pin must be unconnected to provide spatial clearance between high-voltage and low-voltage pins on the IC. Do not connect this pin to any net or to GND.

Pin Name	Pin #	Description
BOOT1	5	**Buck1 high-side MOSFET driver supply**. BOOT1 provides bias voltage for the Buck1 high-side MOSFET driver. An internal bootstrap circuit creates a voltage between BOOT1 and PHASE1 suitable to drive the Buck1 internal high-side N-channel MOSFET. Renesas recommends placing a 0.22µF ceramic capacitor between the BOOT1 and PHASE1 pins. The internal bootstrap circuit recharges the boot capacitor when the Buck1 low-side switch is on. BOOT1 is a high-dV/dt node that should be isolated from sensitive traces as much as possible.
PHASE1	6	**Switching node of Buck1.** PHASE1 is the connection point of the high-side N-channel MOSFET and low-side N-channel MOSFET switches of Buck1 that drive the Buck1 inductor. PHASE1 is a high-dV/dt node that should be isolated from sensitive traces as much as possible.
EN	7	**Enable control input.** EN is a threshold-sensitive enable input to the chip. When EN ≥ 1.2V (typical), the BYP LDO is activated and IC circuits are powered-up, and the device goes into standby and no switching occurs (Standby state). When EN ≥ 1.8V (typical), HV Buck1 begins switching (V_{OUT1} ON state). See the EN_LV pin description for enable control of LV Bucks 2 and 3, and LDO4. When EN falls below 0.95V, the IC is disabled and all fault states are cleared (Shutdown state). EN can be tied to VIN1 for automatic startup. The DC voltage applied to EN should not exceed 42V during normal operation. The EN pin can withstand transients up to 45V.
VIN1	8	**Supply input for the IC and Buck1 switching regulator.** VIN1 supplies the high-side MOSFET of the Buck1 switching regulator and also supplies the internal BYP regulator that powers IC circuits. Place a 4.7µF to 10µF ceramic capacitor in parallel with a 0.1µF ceramic capacitor from VIN1 to PGND1 and as close as possible to the IC for minimum switching loop and smallest spikes due to fast switching. The DC voltage applied to the VIN1 pin should not exceed 42V during normal operation. The VIN1 pin can withstand transients up to 45V.
PGND1	10	**Ground return of Buck1.** Provides the return path for the low-side MOSFET and drivers of Buck1. It carries noisy power current and the traces connecting this pin to the decoupling capacitor between VIN1 and PGND1 should be as short as possible. Any sensitive signal traces should not share the path of this power ground return. Connect this pin to the ground copper plane and add multiple ground vias close to this pin.
GND	11	**System ground.** Small signal (analog) ground pin for internal sensitive analog circuits. Connect GND to a large copper ground plane free from large noisy signals. Connect this pin to PGND1 (Pin 10) directly at the pins, with separate ground islands for PGND1 and GND for the associated components. In layout power flow planning, divert any noisy high currents away from the area around this pin and the analog sense pins of the IC.
BYP	12	**BYP LDO bypass.** Bypass/output node of the internal linear regulator that provides the bias supply for the IC, including Buck1 drivers, BOOT capacitor, and most of the internal circuits. A minimum 4.7µF decoupling ceramic capacitor should be used between this pin to the ground plane close to PGND1. The BYP LDO typically supplies a fixed 4.3V output but the IC bias operating range is 3V to 5.5V. If VIN1 falls below 4.3V, the BYP output also falls below 4.3V.
PGOOD4	13	**Status output for LDO4.** PGOOD4 is an open-drain output that is pulled low when the LDO4 output voltage (LDOOUT4 pin) is outside the range of its undervoltage or overvoltage monitoring levels. If used, the PGOOD4 output requires a resistor pull-up to a supply voltage.
PGOOD2/3	14	**Status output for Buck2 and Buck3.** PGOOD2/3 is an open-drain output that is pulled low when either FB2 or FB3 is out of range of its respective undervoltage or overvoltage monitoring levels. If used, PGOOD2/3 output requires a resistor pull-up to a supply voltage.
PGOOD1	15	**Status output for Buck1.** PGOOD1 is an open-drain output that is pulled low when FB1 is out of range of its undervoltage or overvoltage monitoring levels. If used, the PGOOD1 output requires a resistor pull-up to a supply voltage.
RSTB	16	**System reset output.** The RSTB is an active low/active high output that provides a hard reset-low signal to the system MCU when an output fault occurs. Faults that trigger the RSTB output are listed in "RSTB" on page 28. **Note:** When the RSTB output is high, it is internally driven to the BYP voltage, typically 4.3V.
FB1	17	**Buck1 output voltage feedback input.** Connect FB1 to the output of Buck1 to provide the feedback sense voltage for the Buck1 regulator. An internal resistor divider at FB1 sets the output voltage. The Buck1 output voltage is factory-programmable at various levels from 2.8V to 5.05V (see Table 1 on page 21). The Buck1 UV/OV thresholds are factory-programmable at various levels (see Tables 2 and 3 on page 23). Route the FB1 trace away from noisy or high-dV/dt signals. **Note:** Buck1 UV/OV is sensed through the LDOIN4 input, not through the FB1 input.
LDOIN4	18	**Input to LDO4.** LDOIN4 is the input of the low-dropout linear regulator LDO4. LDO4IN must be connected to the output of Buck1. (The Buck1 output voltage is sensed at FB1, the pin adjacent to LDO4IN.) The LDOINB4 input voltage range is 3.3V to 5.5V. **Note:** LDOIN4 also functions as the UV/OV sense point for Buck1.

Pin Name	Pin #	Description
LDOOUT4	19	**Output of LDO4.** LDOOUT4 is the output of the low-dropout linear regulator LDO4. The output voltage is factory-programmable at various levels from 2.8V to 3.4V (see Table 1 on page 21). The LDO4 output voltage is monitored for fault conditions by factory-programmable UV and OV comparator levels.
FB2	20	**Buck2 output voltage feedback input.** Connect FB2 to the output of Buck2 to provide the feedback sense voltage for the Buck2 regulator. An internal resistor divider at FB2 sets the output voltage. The FB2 pin is also the sense point for the Buck2 UV and OV comparators. Route the FB2 trace away from noisy or high-dV/dt signals.
FB3	21	**Buck3 output voltage sensing input.** Connect FB3 to the output of Buck3 to provide the feedback sense voltage for the Buck3 regulator. An internal resistor divider at FB3 sets the output voltage. The FB3 pin is also the sense point for the Buck3 UV and OV comparators. Route the FB3 trace away from noisy or high-dV/dt signals.
PGND2/3	22	**Shared Power Ground return for Buck2 and Buck3.** PGND2/3 provides the return path for the low-side MOSFETs and drivers of Buck2 and Buck3. This path carries noisy power current; the copper trace from this pin to the decoupling capacitor between VIN2/3 and PGND2/3 should be as short as possible. Any sensitive signal traces should not share traces with this driver return path. Connect this pin to the ground copper plane and add multiple ground vias close to the pin.
PHASE3	23	**Switching node of Buck3.** PHASE3 is the connection point between the high-side P-channel MOSFET and low-side N-channel MOSFET switches of the Buck3 regulator. PHASE3 is a high-dV/dt node that should be isolated from sensitive traces as much as possible.
PHASE2	24	**Switching node of Buck2.** PHASE2 is the connection point between the high-side P-channel MOSFET and low-side N-channel MOSFET switches of the Buck2 regulator. PHASE2 is a high-dV/dt node that should be isolated from sensitive traces as much as possible.
Pad	-	**Package thermal pad.** PAD must be soldered to a large ground plane on the PCB that does not contain noisy power flow. Use as many vias as possible in PAD to help reduce the θ_{JA} of the IC package. PAD is not an electrical connection.

2. Specifications

2.1 Absolute Maximum Ratings

Parameter	Minimum	Maximum	Unit
Buck1 Power			
VIN1 to PGND1	-0.3	+45	V
PHASE1 to PGND1	-0.3	V_{IN} + 0.3	V (DC)
PHASE1 to PGND1	-2	V_{IN} + 0.3	V (20ns)
BOOT1 to PHASE1	-0.3	+6.0	V
Buck2, Buck3 Power			
VIN2/3 to PGND2/3 (DC)	-0.3	5.8	V
VIN2/3 to PGND2/3 (20ns)	-0.3	7.0	V
PHASE2, PHASE3 to PGND2/3 (DC)	-0.3	VIN2/3 + 0.3	V
PHASE2, PHASE3 to PGND2/3 (20ns)		7.0	V
PHASE2, PHASE3 to PGND2/3 (100ns)	-2V		V
Analog and Digital I/O			
EN to GND	-0.3	+45	V
FB1, FB2, FB3, EN_LV to GND	-0.3	+6.5	V
PGOOD1, PGOOD2/3, PGOOD4	-0.3	+6.5	V
RSTB to GND	-0.3	+6.5	V
CFG1 to GND	-0.3	BYP + 0.3	
ESD Rating	**Value**		**Unit**
Human Body Model (Tested per AEC-Q100-002E)	900		V
Charged Device Model (Tested per AEC-Q100-011D)			
Corner Pins	750		V
Other Pins	500		V
Latch-Up (Tested per AEC-Q100-004D; Class 2, Level A)	100		mA

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

2.2 Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
24 Ld SCQFN Package (Notes 4, 5)	37	2.5

Notes:

4. θ_{JA} is measured in free air with the component mounted on a high-effective thermal conductivity test board with direct attach features. See TB379.
5. For θ_{JC}, the case temperature location is the center of the exposed metal pad on the package underside.

Parameter	Minimum	Maximum	Unit
Maximum Junction Temperature	-55	+150	°C
Maximum Storage Temperature Range	-65	+150	°C
Pb-Free Reflow Profile	See TB493		

2.3 Recommended Operating Conditions

Parameter	Minimum	Maximum	Unit
VIN1 Supply Voltage	4 (Note 6)	42	V
EN to GND	0	42	V
EN_LV to GND	0	5.5	V
VIN2/3 Supply Voltage Range	3.3	5.5	V
Buck1 Output Current	0	0.75	A
Buck2, Buck3 Output Current (Note 7)	0	0.75	A
LDO4 Output Current	0	0.3	A
Junction Temperature Range	-40	+150	°C
Ambient Temperature Range	-40	+125	°C
CFG1 to GND	0	BYP	V

Notes:

6. Minimum VIN1 voltage for startup is 4.5V. After startup the device can operate down to 4.0V.
7. Output current for Buck2 and Buck3 is dependent on the voltage setting for that output. See "Buck2 and Buck3" on page 27 in the Functional Description section.

2.4 Electrical Specifications

T_J = -40°C to +150°C, VIN1 = 4V to 42V, unless otherwise noted. Typical values are at T_J = +50°C. **Boldface limits apply across the junction temperature range -40°C ≤ T_J ≤ +150°C.**

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Voltage						
VIN1 Startup Threshold Voltage				4.45		V
VIN1 Operating Voltage Range	V_{IN1}		**4**		**42**	V
VIN1 Supply Shutdown Current	I_{SD}	EN ≤ 0.4V, VIN1 = 12V		1	**10**	µA
VIN1 Supply Operating Current		"Typical Application Schematic" on page 4 EN = VIN1 = 12V, EN_LV = BYP, no load on all outputs		17		mA
VIN1 Undervoltage Threshold Voltage	$V_{IN1(UV)}$	VIN1 rising (factory programmed)	**4.338**	4.453	**4.569**	V
		VIN1 falling (fixed)	**3.273**	3.519	**3.805**	V
		VIN1 hysteresis		930		mV
EN Pin						
EN Shutdown Threshold Voltage	$V_{EN(OFF)}$				**0.4**	V
EN Enable Buck1 Threshold Voltage	$V_{EN(BK1)}$	EN rising (Buck1 enable)	**1.85**			V
		EN falling (Buck1 disable)			**0.4**	V
EN Disable Internal LDO Off-Delay		Delay from EN falling edge to commence shutdown sequence		300		µs
EN Pin Input Leakage		EN = 4V to 42V		0.03		µA
EN_LV PIN						
Input Leakage Current			**-1**		**1**	µA
Low Level Input Voltage	V_{IL}	Schmitt input			**0.8**	V
High Level Input Voltage	V_{IH}		**2.0**			V
		Falling hysteresis		340		mV
EN_LV Off-Delay		Delay from EN_LV falling edge to commence VOUT2/3/4 shutdown sequence.		300		µs

T_J = -40°C to +150°C, VIN1 = 4V to 42V, unless otherwise noted. Typical values are at T_J = +50°C. **Boldface limits apply across the junction temperature range -40°C ≤ T_J ≤ +150°C. (Continued)**

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Internal LDO (BYP)						
Internal LDO Voltage (BYP Pin)	$V_{DD(INT)}$	VIN1 = 12V, EN = 1.6V, I_{BYP} = 0mA	**4.20**	4.30	**4.41**	V
		VIN1 = 12V, EN = 1.6V, I_{BYP} = 20mA	**4.18**	4.29	**4.41**	V
Internal LDO Dropout Voltage ($V_{DROPOUT}$ = VIN1 – BYP)		VIN1 = 4V, EN = 1.6V, I_{BYP} = 20mA		87	**145**	mV
Power-On Reset						
Power-On Reset Threshold Voltage (BYP Pin)	V_{POR}	BYP falling	**2.921**	3.13	**3.216**	V
		BYP rising	**3.387**	3.58	**3.803**	V
		Rising hysteresis		450		mV
Oscillator						
Switching Frequency	f_{SW}	Spread spectrum disabled (default)	**1.98**	2.20	**2.42**	MHz
Fault Protection Hiccup Mode Interval	t_{HICCUP}	Internal reset timeout period	**188**	200	**214**	ms
Buck2 On-Edge to Buck1 On-Edge Phase Relationship				0		°
Buck3 On-Edge to Buck1 On-Edge Phase Relationship		Factory default (0° option available)		180		°

2.5 Buck1 Electrical Specifications

T_J = -40°C to +150°C, VIN1 = 4V to 42V, unless otherwise noted. Typical values are at T_J = +50°C. **Boldface limits apply across the junction temperature range -40°C ≤ T_J ≤ +150°C.**

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Configure Pin						
CFG1 Input Low Voltage					**1.245**	V
CFG1 Input Open Voltage		DC voltage measured at open pin	**2.121**		**2.380**	V
CFG1 Input High Voltage			**3.14**			V
Allowed Leakage in Open State			**-29.3**		**+31**	µA
Feedback Pin						
FB1 Pin Input Impedance	R_{FB1}			115		kΩ
FB1 Pin Voltage Accuracy at V_{OUT1} = 3.8V (Notes 8 and 9)	V_{FB1}	I_{VOUT1} = 0mA, off-time > minimum off-time	**3.783 [-0.45%]**	3.8	**3.854 [+1.42%]**	V
Buck1 Soft-Start Ramp Time		V_{OUT1} from 0% to 95%		1.2		ms
Pulse Skipping						
Upper Pulse-Skipping Threshold		VIN1 rising	**19.08**	19.5	**19.90**	V
		VIN1 falling hysteresis		1.0		V
Output Voltage Protection						
Undervoltage Threshold (Note 9)	$V_{FB1(UV)}$	V_{FB1} falling (factory programmed) Factory options: -4%, -6%, -12%	**3.467 (-8.76%)**	3.496 (-8%)	**3.535 (-6.97%)**	V
		V_{FB1} rising hysteresis	**+0.4**	+0.9	**+1.2**	%
Severe Undervoltage Threshold		V_{FB1} falling	**-24**	-20	**-16**	%
Undervoltage Fault Delay		FB1 < $V_{FB1(UV)}$ Factory option of additional 10µs delay		2		µs
Overvoltage Threshold (Note 9)	$V_{FB1(OV)}$	V_{FB1} rising (factory programmed) Factory options: +4%, +6%, +12%	**4.066 (-7.00%)**	4.104 (8%)	**4.150 (+9.21%)**	V
		V_{FB1} falling hysteresis	**-0.4**	-0.8	**-1.2**	%

T_J = -40°C to +150°C, VIN1 = 4V to 42V, unless otherwise noted. Typical values are at T_J = +50°C. **Boldface limits apply across the junction temperature range -40°C ≤ T_J ≤ +150°C. (Continued)**

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Severe Overvoltage Threshold		VFB1 rising	**+16**	+20	**+24**	%
Output Current Protection						
Overcurrent Limit, Cycle-by-Cycle, (Note 9)	$I_{1(OC1)}$	Factory-programmed. Factory options: 1.5A, 1.75A	**1.008**	1.17	**1.44**	A
Overcurrent Limit Blanking Time				54	**96**	ns
Overcurrent Limit, Hiccup/Latch-Off	$I_{1(OC2)}$		**1.71**	2.0	**2.42**	A
Overcurrent Hiccup Delay		Consecutive cycles on $I_{1(OC2)}$		7		Cycles
Negative Current Limit Detection	$I_{1(NLIM)}$		**-0.98**	-0.80	**-0.62**	A
Power MOSFETs						
High-Side Switch On-Resistance	r_{HDS}	I_{PHASE1} = 100mA, VIN1 = 12V, BYP = 3.8V, BOOT = 3.8V		330	**625**	mΩ
Low-Side Switch On-Resistance	r_{LDS}	I_{PHASE1} = 100mA, VIN1 = 12V, BYP = 3.8V		270	**540**	mΩ
Minimum On-Time	t_{ON}	VIN1 = 5.5V (Note 10)	**30**	65	**73**	ns
Minimum Off-Time	t_{OFF}	(Note 10)	**24**	60	**84**	ns
PHASE1 Rise Time	t_{RISE1}	"Typical Application Schematic" on page 4 VIN1 = 12V, Buck1 at no load		4		ns
PHASE1 Fall Time	t_{FALL1}			4		ns

2.6 Buck2 and Buck3 Electrical Specifications

T_J = -40°C to +150°C, VIN1 = 4V to 42V, unless otherwise noted. Typical values are at T_J = +50°C. **Boldface limits apply across the junction temperature range -40°C ≤ T_J ≤ +150°C.**

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Supply						
VIN2/3 Voltage Range		Internal compensation	**3.3**		**5.5**	V
VIN2/3 Undervoltage Threshold	$V_{IN2/3\_UV}$	VIN2/3 rising. No load Buck2, Buck3		2.42	**2.60**	V
		VIN2/3 falling. No load Buck2, Buck3	**2.10**	2.30		V
VIN2/3 Quiescent Supply Current	$I_{VIN2/3}$	"Typical Application Schematic" on page 4 f_{SW} = 2.2MHz, VIN2/3 = 3.8V, V_{OUT2} = 1.8V, V_{OUT3} = 1.2V. No output load		10		mA
VIN2/3 Shutdown Supply Current	$I_{SD\_VIN2/3}$	EN_LV = 0V, VIN2/3 = 5V		12	**18.3**	µA
Output Regulation						
FB2 Pin Voltage Accuracy at V_{OUT2} = 1.8V (Note 9)	V_{FB2}	I_{VOUT2} = 0mA	**1.792 [-0.44%]**	1.800	**1.817 (+0.94%)**	V
FB3 Pin Voltage Accuracy at V_{OUT3} = 1.2V (Note 9)	V_{FB3}	I_{VOUT3} = 0mA	**1.194 [-0.50%]**	1.200	**1.216 (+1.33%)**	V
Output Voltage Protection						
V_{OUT2} Undervoltage Threshold (Notes 9, 11)	$V_{FB2(UV)}$	V_{FB2} falling. Factory options: -4%, -6%, -12%	**1.639 (-8.94%)**	1.656 (-8%)	**1.679 (-6.72%)**	V
		V_{FB2} rising hysteresis	**+0.4%**	+0.8%	**+1.2%**	%
V_{OUT2} Overvoltage Threshold (Notes 9, 11)	$V_{FB2(OV)}$	V_{FB2} rising. Factory options: -4%, -6%, -12%	**1.921 (+6.72%)**	1.944 (+8%)	**1.970 (+9.44%)**	V
		V_{FB2} falling hysteresis	**-0.4%**	-0.8%	**-1.2%**	%
V_{OUT3} Undervoltage Threshold (Notes 9, 11)	$V_{FB3(UV)}$	V_{FB3} falling. Factory options: -4%, -6%, -12%	**1.089 (-9.25%)**	1.104 (-8%)	**1.119 (-6.75%)**	V
		V_{FB3} rising hysteresis	**+0.4%**	+0.8%	**+1.2%**	%

T_J = -40°C to +150°C, VIN1 = 4V to 42V, unless otherwise noted. Typical values are at T_J = +50°C. **Boldface limits apply across the junction temperature range -40°C ≤ T_J ≤ +150°C. (Continued)**

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
V_{OUT3} Overvoltage Threshold (Notes 9, 11)	$V_{FB3(OV)}$	V_{FB3} rising. Factory options: +4%, +6%, +12%	**1.279 (+6.58%)**	1.296 (+8%)	**1.315 (+9.58%)**	V
		V_{FB3} falling hysteresis	**-0.4%**	-0.8%	**-1.2%**	%
Undervoltage Fault Delay		FB2 > V_{FB2} (UV), or FB3 > V_{FB3} (UV) Factory option additional 10µs delay		2		µs
Output Current Protection						
Overcurrent Limit, Cycle-by-Cycle (Note 12)	$I_{2(LIM)}$, $I_{3(LIM)}$			1.17		A
Overcurrent Hiccup Mode Delay				100		Cycles
Negative Current Limit	$I_{2(NLIM)}$, $I_{3(NLIM)}$		**-0.99**	-0.8	**-0.60**	A
Feedback Pin						
FB2, FB3 Pin Input Impedance	R_{FB2}, R_{FB3}			36		kΩ
Buck2 Soft-Start Ramp Time		V_{OUT2} = 1.8V		1.2		ms
Buck3 Soft-Start Ramp Time		V_{OUT3} = 1.2V		0.85		ms
Power MOSFETs						
High-Side PMOS Switch On-Resistance		$I_{PHASE2,3}$ = 100mA, VIN2/3 = 3.8V	**152**	232	**370**	mΩ
Low-Side NMOS Switch On-Resistance		$I_{PHASE2,3}$ = 100mA, VIN2/3 = 3.8V	**87**	140	**260**	mΩ
PHASE2, PHASE3 Maximum Duty Cycle				90		%
PHASE2, PHASE3 Minimum On-Time					**100**	ns

2.7 LDO4 Electrical Specifications

T_J = -40°C to +150°C, VIN1 = 4V to 42V, unless otherwise noted. Typical values are at T_J = +50°C. **Boldface limits apply across the junction temperature range -40°C ≤ T_J ≤ +150°C.**

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Supply						
Input Voltage Range	V_{IN4}	Connected to VOUT1, VIN2/3	**3.3**		**5.5**	V
Output Regulation						
Output Voltage (Note 9)	$V_{LDOOUT4}$	Factory option 3.3V. VIN2/3 = 3.8V, $I_{LDOOUT4}$ = 100mA	**3.260 (-1.21%)**	3.29	**3.332 (+0.96)**	V
Dropout Voltage		$I_{LDOOUT4}$ = 300mA, 2% drop at LDOOUT4		102	**210**	mV
Power Supply Rejection Ratio		At 1kHz, T_A = 25°C, "Typical Application Schematic" on page 4, LDOIN4 = 3.8V, LDOOUT4 = 3.3V at 300mA		55		dB
LDOOUT4 Soft-Start Ramp Time		LDOOUT4 = 3.3V; $C_{LDOOUT4}$ = 1µF		1.55		ms
Output Voltage Protection						
Undervoltage Threshold (Notes 9, 11)	$V_{LDO4(UV)}$	LDOOUT4 falling. Factory options: -4%, -6%, -12%	**3.008 (-8.85%)**	3.036 (-8%)	**3.073 (-6.88%)**	V
		LDOOUT4 rising hysteresis	**+0.4%**	+0.8%	**+1.2%**	%
Overvoltage Threshold (Notes 9, 11)	$V_{LDO4(OV)}$	LDOOUT4 rising. Factory options -4%, -6%, -12%	**3.529 (+6.94%)**	3.564 (+8%)	**3.609 (+9.36%)**	V
		VLDOOUT4 falling hysteresis	**-0.4%**	-0.8%	**-1.2%**	%

T_J = -40°C to +150°C, VIN1 = 4V to 42V, unless otherwise noted. Typical values are at T_J = +50°C. **Boldface limits apply across the junction temperature range -40°C ≤ T_J ≤ +150°C. (Continued)**

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Undervoltage Fault Glitch Delay		LDOOUT <$V_{LDO4(UV)}$ Factory option of additional 10µs delay		2		µs
Output Current Protection						
Overcurrent Limit	$I_{4(LIM)}$		**306**	429	**554**	mA

2.8 Digital I/O Electrical Specifications

T_J = -40°C to +150°C, VIN1 = 4V to 42V, unless otherwise noted. Typical values are at T_J = +50°C. **Boldface limits apply across the junction temperature range -40°C ≤ T_J ≤ +150°C.**

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
PGOOD 1, 2/3, 4 Electrical Specifications						
PGOOD1, 2/3, 4 Low-Level Output Voltage	PG_{LOW1} PG_{LOW23} PG_{LOW4}	I_PGOODx = 5mA			**0.4**	V
PGOOD1, 2/3, 4 Open-Drain Leakage	IPG_{LK1} IPG_{LK23} IPG_{LK4}	I_PGOODx = 3.3V		0	**1**	µA
RSTB Pull-Up $r_{DS(ON)}$	$RSTB_{RDSHI}$			55		mΩ
RSTB Pull-Down $r_{DS(ON)}$	$RSTB_{RDSLO}$			85		mΩ

Notes:

8. Buck1 not in Pulse Skipping mode and Buck1 on-time is greater than the minimum on-time.
9. Electrical Specification limits apply only for the factory-programmed settings.
10. Minimum on-time and minimum off-time required to maintain loop stability.
11. Undervoltage and overvoltage factory programmed selections for FB1, FB2, FB3, and LDO4 are independent.
12. Peak current in Buck2 or Buck3 inductor may exceed the MAX limit for several cycles. This can persist for a maximum 100 cycles, approximately 46µs, before triggering output shutdown.
13. All temperature limits are established by characterization and are not production tested.

3. Typical Performance Curves

3.1 Efficiency, Input Current

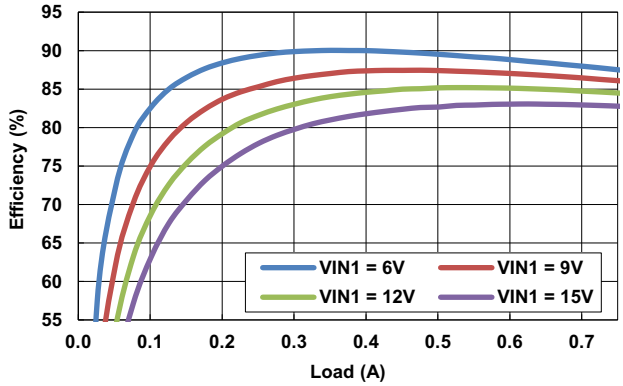


Figure 4. One-Stage Efficiency vs Load, V_{OUT1} = 3.8V

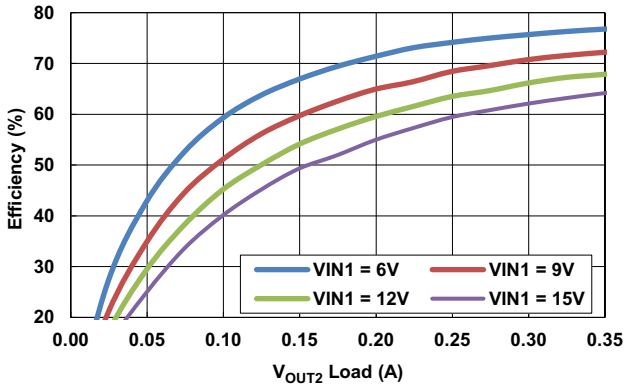


Figure 5. Two-Stage Efficiency vs Load, V_{OUT1} = 3.8V, V_{OUT2} = 1.8V

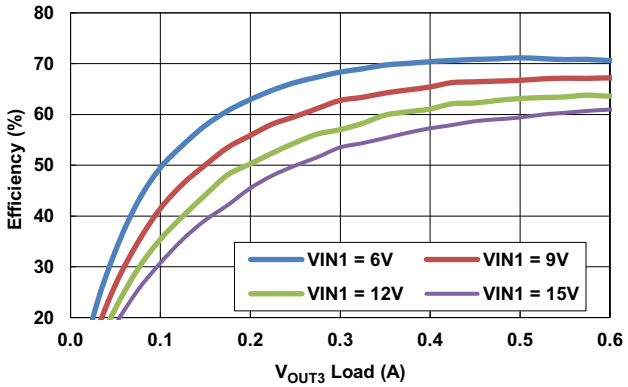


Figure 6. Two-Stage Efficiency vs Load, V_{OUT1} = 3.8V, V_{OUT3} = 1.2V

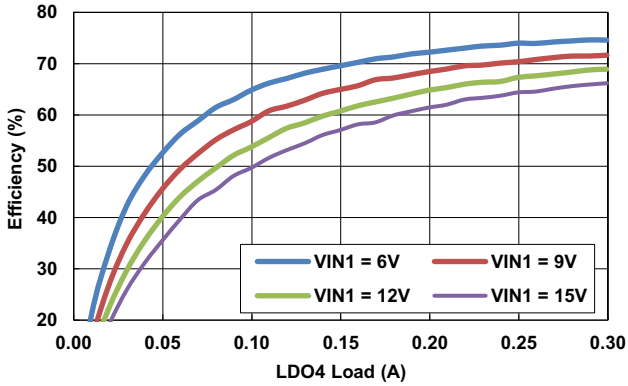


Figure 7. Two-Stage Efficiency vs Load, V_{OUT1} = 3.8V, LDO4 = 3.3V

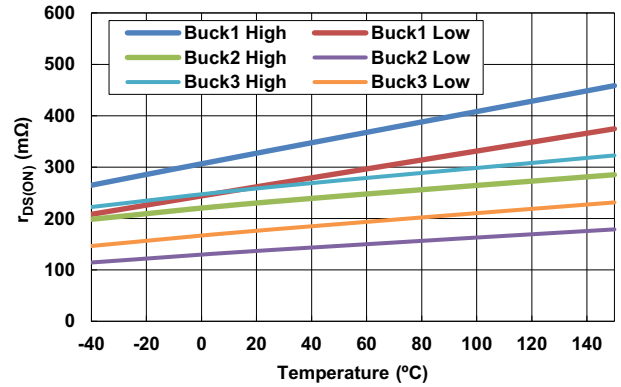


Figure 8. $r_{DS(ON)}$ vs Temperature, VIN1 = 12V, V_{OUT1} = 38V

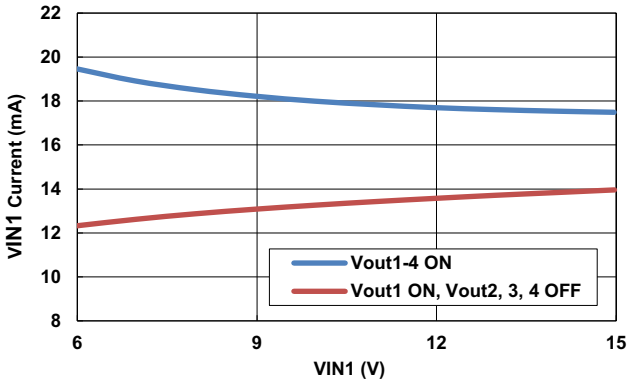


Figure 9. VIN1 Operating Current, No Load, External Pull-Up Supply for PGOOD1, 2/3, 4

3.2 Load Regulation

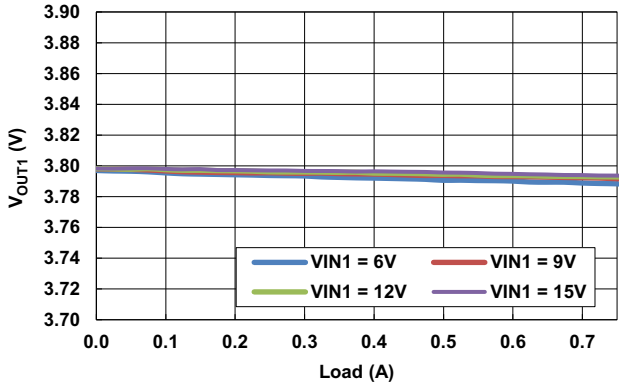


Figure 10. V_{OUT1} Load Regulation

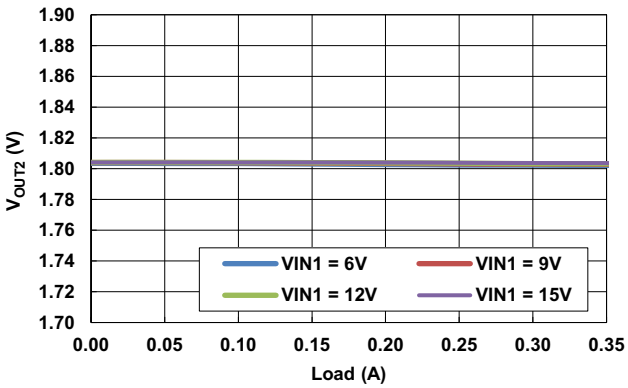


Figure 11. V_{OUT2} Load Regulation

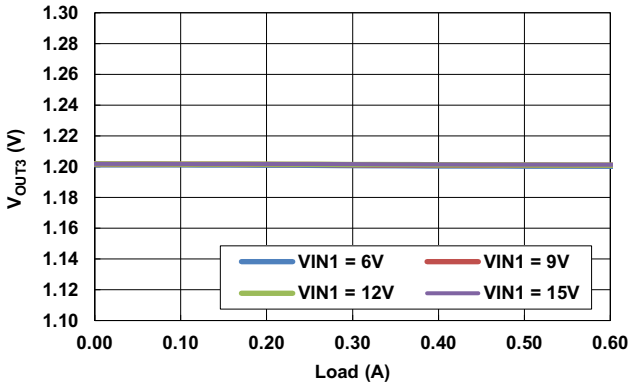


Figure 12. V_{OUT3} Load Regulation

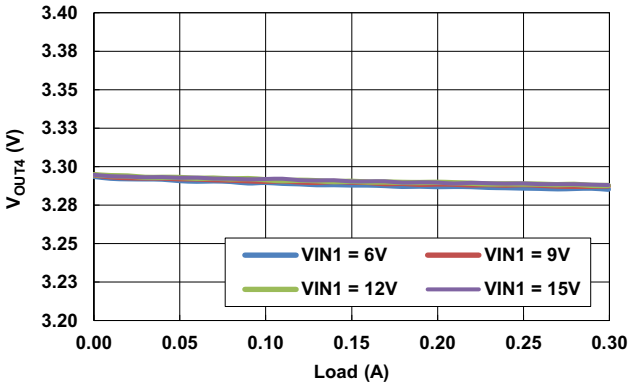


Figure 13. V_{OUT4} Load Regulation

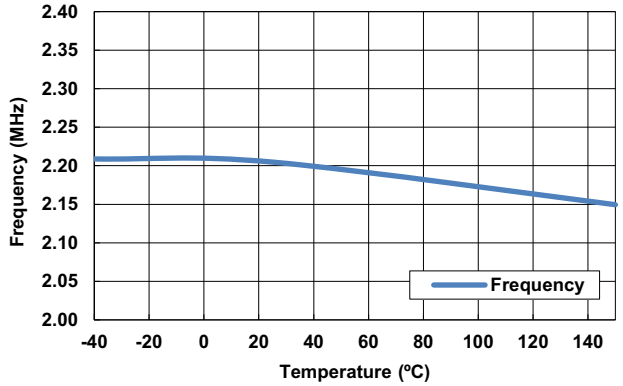


Figure 14. Frequency vs Temperature

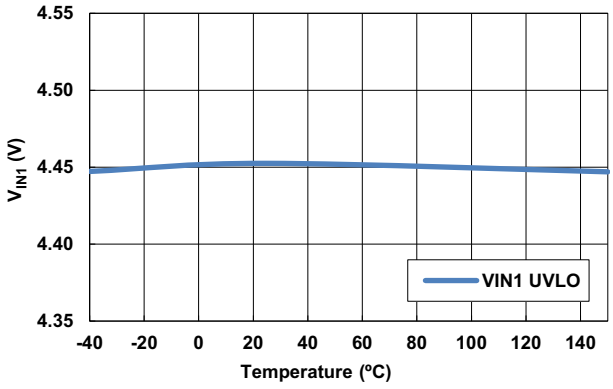


Figure 15. VIN1 UVLO Rising Edge vs Temperature

3.3 Line Regulation, Switching Waveforms

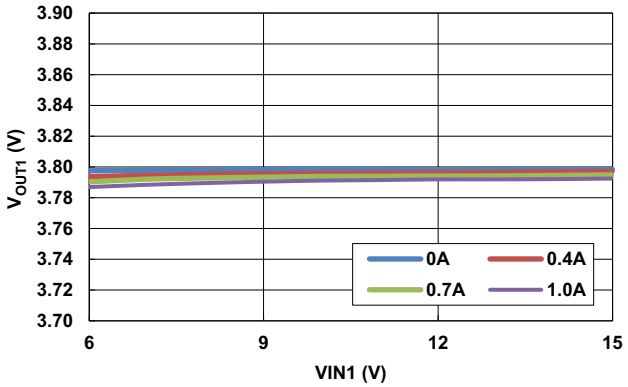


Figure 16. V_{OUT1} One-Stage Line Regulation

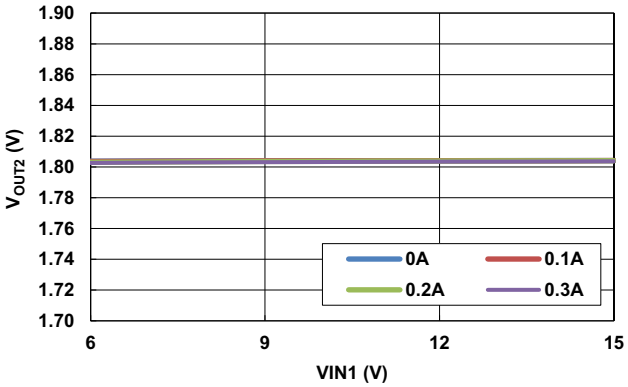


Figure 17. V_{OUT2} Two-Stage Line Regulation

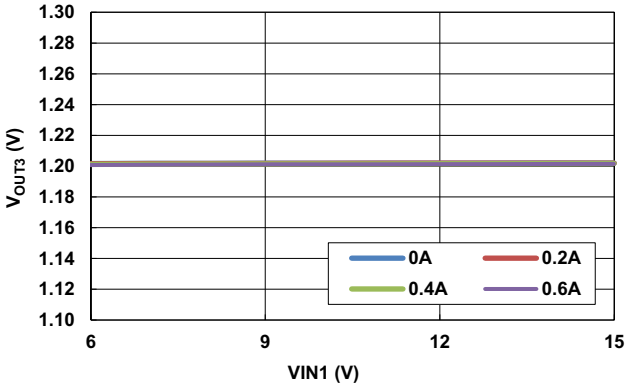


Figure 18. V_{OUT3} Two-Stage Line Regulation

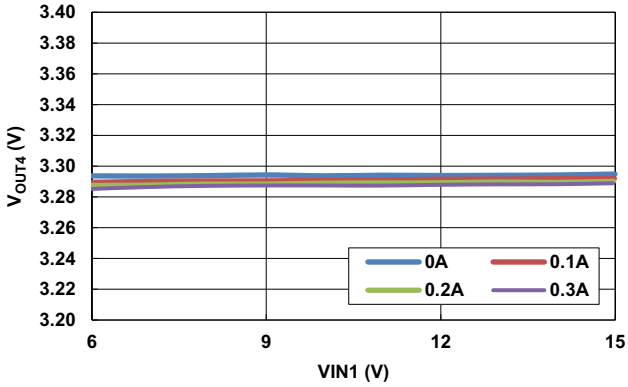


Figure 19. V_{OUT4} Two-Stage Line Regulation

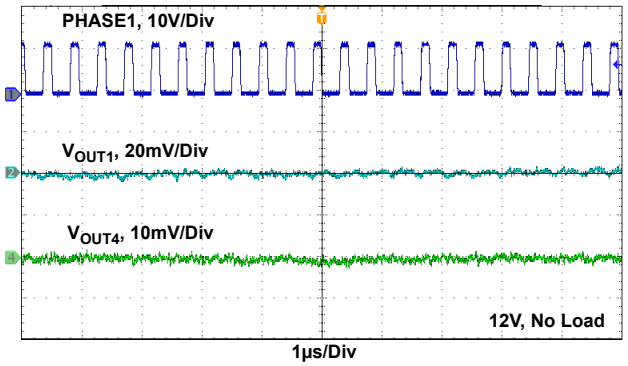


Figure 20. Switching: PHASE1, V_{OUT1}, LDO4

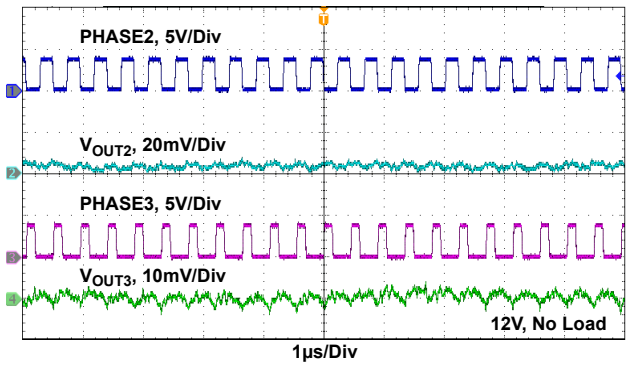


Figure 21. Switching: PHASE2, V_{OUT2}, PHASE3, V_{OUT3}

3.4 Load and Line Transient Response

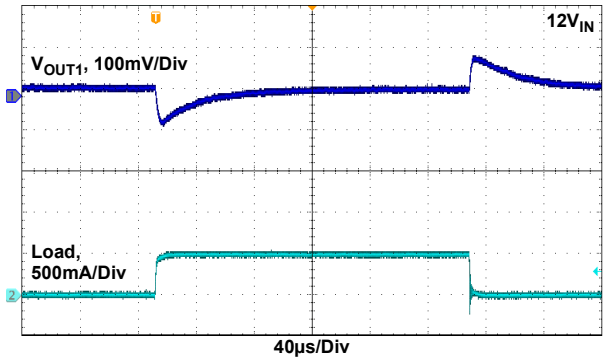


Figure 22. V_{OUT1} Load Transient, 0A/0.5A

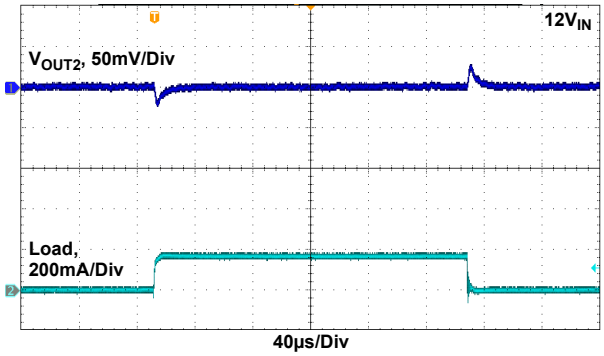


Figure 23. V_{OUT2} Load Transient, 0A/0.15A

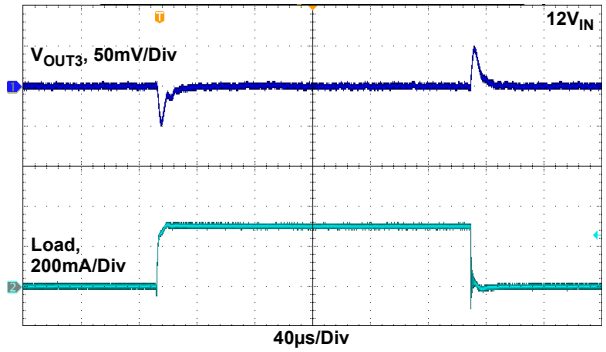


Figure 24. V_{OUT3} Load Transient, 0A/0.3A

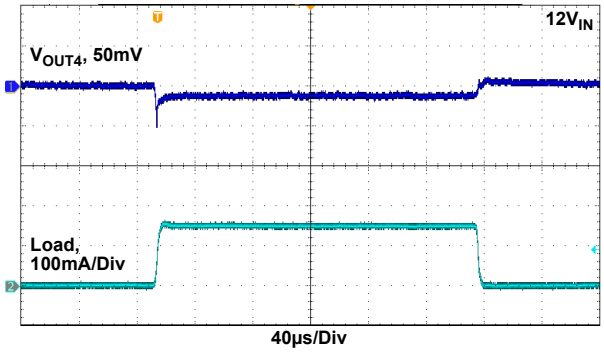


Figure 25. V_{OUT4} Load Transient, 0A/0.15A

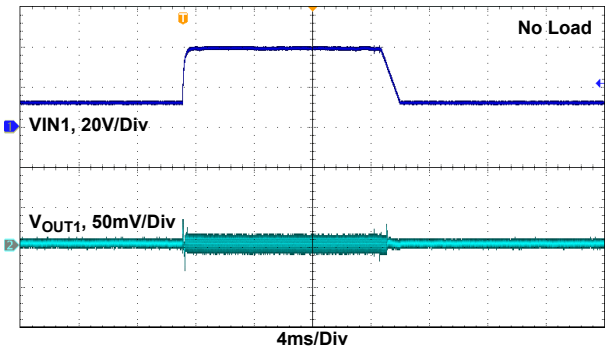


Figure 26. V_{OUT1} Line Transient, 12V/39V

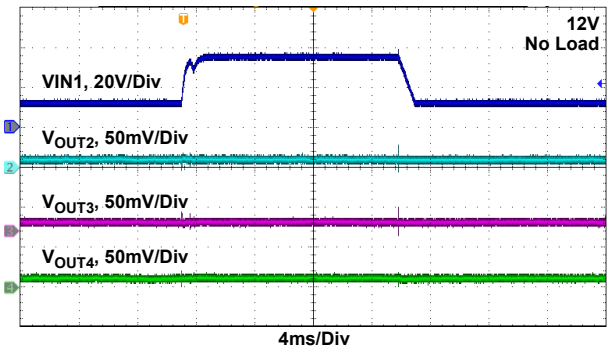


Figure 27. V_{OUT2}, V_{OUT3}, V_{OUT4} Line Transient, 12V/38V

3.5 Startup – EN Toggle

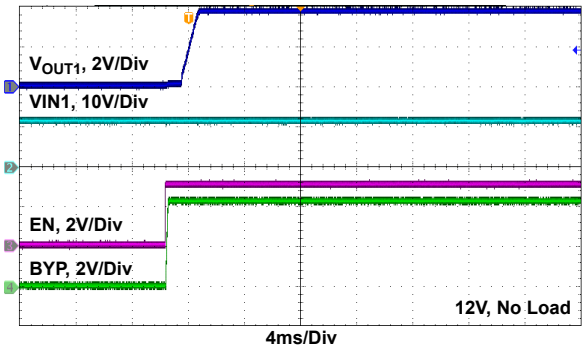


Figure 28. Startup with EN Toggle: V_{OUT1}, VIN1, EN, BYP

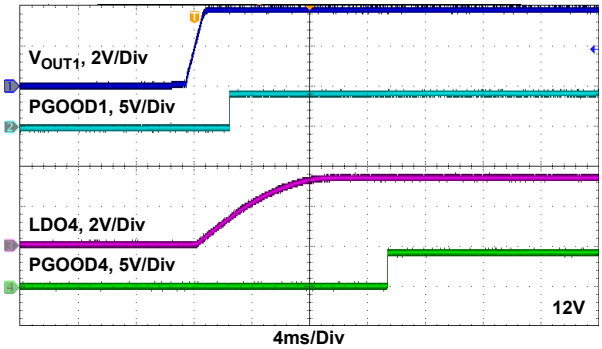


Figure 29. Startup with EN Toggle: V_{OUT1}, PGOOD1, LDO4, PGOOD4

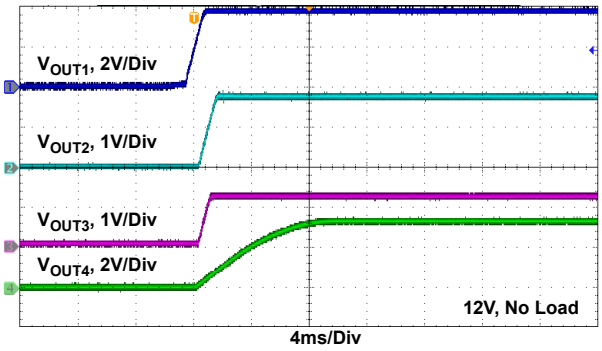


Figure 30. Startup with EN Toggle: V_{OUT1}, V_{OUT2}, V_{OUT3}, V_{OUT4}

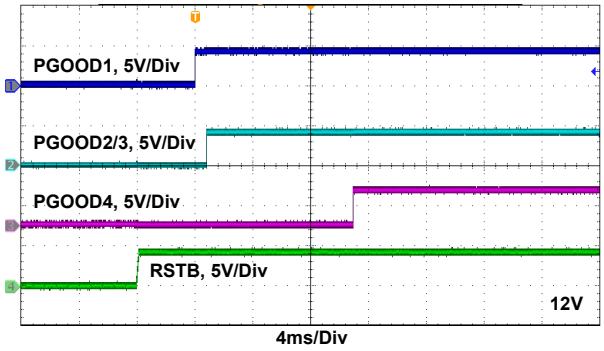


Figure 31. Startup with EN Toggle: PGOOD1, PGOOD2/3, PGOOD4, RSTB

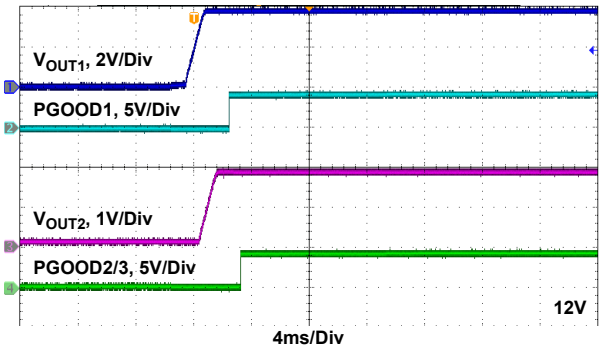


Figure 32. Startup with EN Toggle: V_{OUT1}, PGOOD1, V_{OUT2}, PGOOD2/3

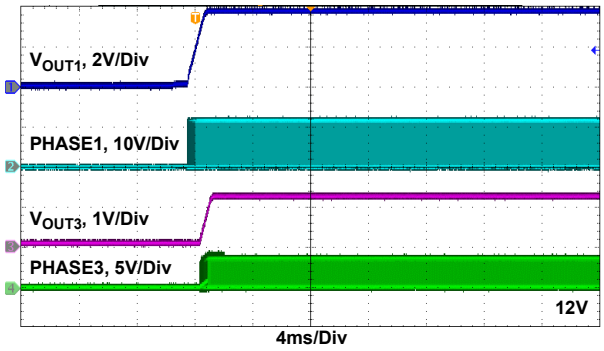


Figure 33. Startup with EN Toggle: V_{OUT1}, Phase1, V_{OUT3}, Phase3

3.6 Startup – VIN1 Ramp

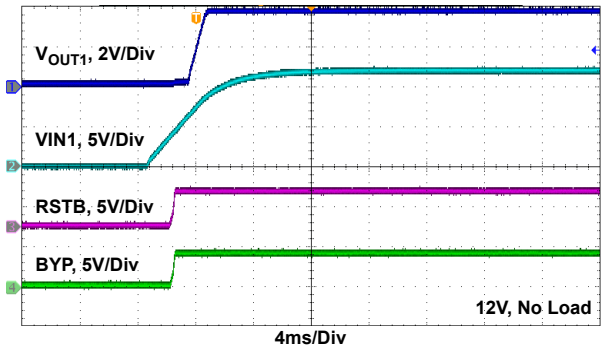


Figure 34. Startup with VIN1 Ramp: V_{OUT1}, VIN1, RSTB, BYP

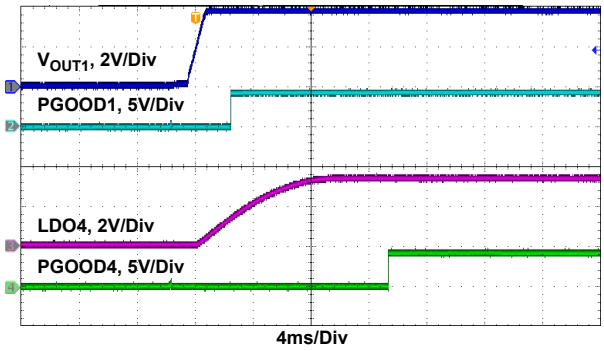


Figure 35. Startup with VIN1 Ramp: V_{OUT1}, PGOOD1, LDO4, PGOOD4

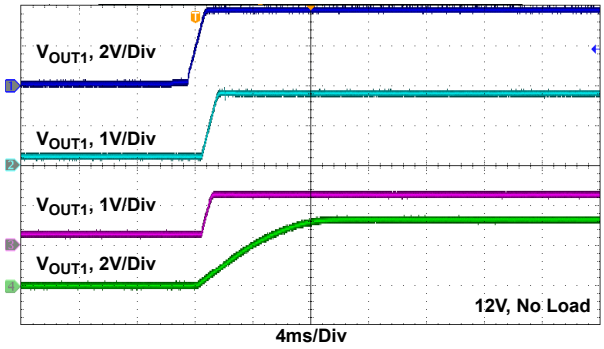


Figure 36. Startup with VIN1 Ramp: V_{OUT1}, V_{OUT2}, V_{OUT3}, V_{OUT4}

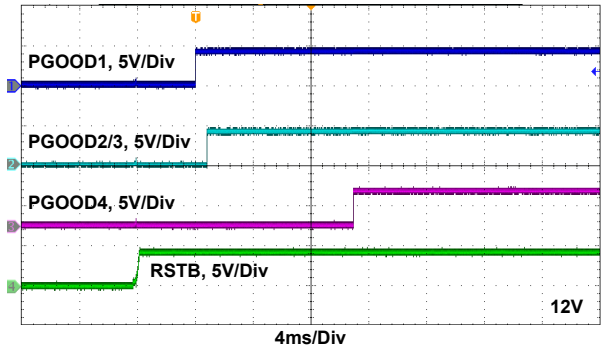


Figure 37. Startup with VIN1 Ramp: PGOOD1, PGOOD2/3, PGOOD4, RSTB

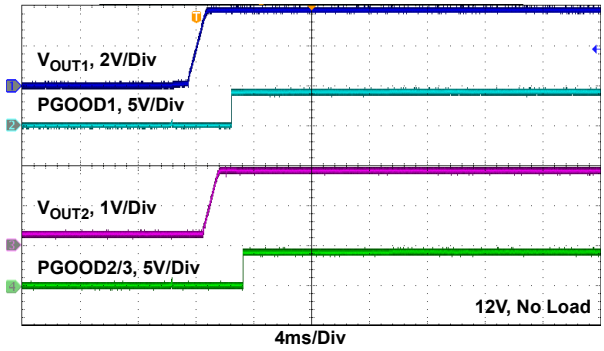


Figure 38. Startup with VIN1 Ramp: V_{OUT1}, PGOOD1, V_{OUT2}, PGOOD2/3

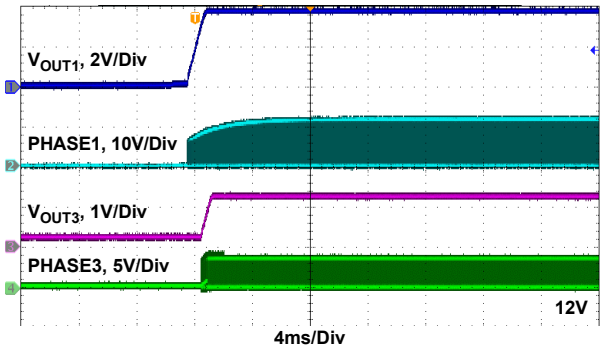


Figure 39. Startup with VIN1 Ramp: V_{OUT1}, Phase1, V_{OUT3}, Phase3

4. Functional Descriptions

4.1 Factory Programmable Output Voltages

The ISL78083 is a multi-rail regulator IC that is comprised of a primary high voltage buck converter (Buck1), two secondary low voltage buck converters (Buck2 and Buck3), and one low dropout linear regulator (LDO4).

In typical camera power applications, the primary buck typically takes its input (VIN1) from a filtered 12V car battery, and produces an intermediate voltage typically between 3.3V and 5V. The output voltage of Buck1 is fixed at 3.8V. Other Buck1 voltage options can be factory-programmed, see Table 1 for the list of possible Buck1 output voltages.

The secondary bucks share a common input pin (VIN2/3) that is supplied by the output of Buck1. They produce low voltage supply rails, with Buck2 fixed at 1.8V and Buck3 fixed at 1.2V. Other voltage options for Buck2 and Buck3 can be factory-programmed, see Table 1 for the list of possible Buck2 and Buck3 output voltages.
Note: Maximum output current for Buck2 and Buck3 is limited by the output voltage selection, see Figure 2 on page 4.

The linear regulator LDO4 uses the output voltage from Buck1 as an input through the LDOIN4 pin. The LDO4 output is typically filtered to produce a quiet rail for camera applications. The output voltage of LDO4 is fixed at 3.3V. Other LDO4 voltage options can be factory-programmed, see Table 1 for the list of LDO4 output voltages.

Note: The voltage level for each output is independently selectable. Buck2, Buck3, and LDO4 voltage selections must be compatible with the V_{OUT1} selection, within limitations set by the maximum duty cycle, minimum off-time, load current, and I•R voltage drops.

Table 1. Output Voltage Selections

Register 0x71		Register 0x73		Register 0x75		Register 0x77	
Option Code (hex)	Buck1 Output (V)	Option Code (hex)	Buck2 Output (V)	Option Code (hex)	Buck3 Output (V)	Option Code (hex)	LDO4 Output (V)
		01	1.00	01	1.00	01	2.80
		02	1.05	02	1.05	02	2.85
		03	1.10	03	1.10	03	2.90
		04	1.15	04	1.15	04	2.95
		05	1.20	05	1.20	05	3.00
		06	1.25	06	1.25	06	3.05
		07	1.30	07	1.30	07	3.10
		08	1.35	08	1.35	08	3.15
		09	1.40	09	1.40	09	3.20
		0A	1.45	0A	1.45	0A	3.25
0B	3.30	0B	1.50	0B	1.50	0B	3.30
0C	3.35	0C	1.55	0C	1.55	0C	3.35
0D	3.40	0D	1.60	0D	1.60	0D	3.40
0E	3.50	0E	1.65	0E	1.65		
0F	3.60	0F	1.70	0F	1.70		
10	3.70	10	1.75	10	1.75		
11	3.80	11	1.80	11	1.80		
12	5.00	12	1.85	12	1.85		
13	5.05	13	1.90	13	1.90		
		14	1.95	14	1.95		

Table 1. Output Voltage Selections (Continued)

Register 0x71		Register 0x73		Register 0x75		Register 0x77	
Option Code (hex)	Buck1 Output (V)	Option Code (hex)	Buck2 Output (V)	Option Code (hex)	Buck3 Output (V)	Option Code (hex)	LDO4 Output (V)
		15	2.00	15	2.00		
		16	2.05	16	2.05		
		17	2.10	17	2.10		
		18	2.15	18	2.15		
		19	2.20	19	2.20		
		1A	2.25	1A	2.25		
		1B	2.30	1B	2.30		
		1C	2.35	1C	2.35		
		1D	2.40	1D	2.40		
		1E	2.45	1E	2.45		
		1F	2.50	1F	2.50		
		20	2.55	20	2.55		
		21	2.80	21	2.80		
		22	3.30	22	3.30		

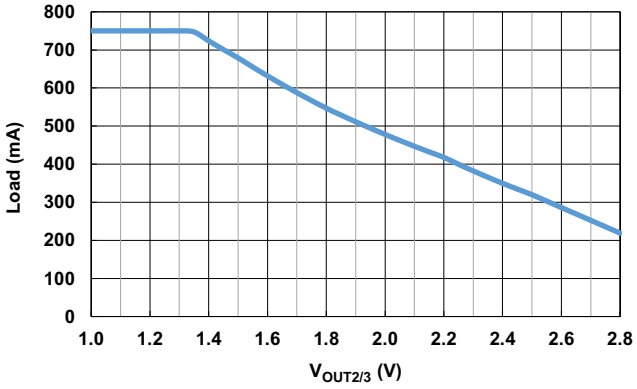


Figure 40. $V_{OUT2/3}$ Typical Load Capability

4.2 Undervoltage and Overvoltage Protection

The ISL78083 offers Undervoltage (UV) and Overvoltage (OV) threshold levels for Buck1, Buck2, Buck3, and LDO4. Buck2 and Buck3 output voltages are sensed at the FB2 and FB3 pins respectively, while LDO4 is sensed at the LDOOUT4 pin. The Buck1 regulator uses the LDOIN4 input pin for UV and OV sensing, and uses the FB1 input for output regulation. This separation of UV/OV sensing from feedback sensing on Buck1 provides additional output protection in cases where the feedback path is inadvertently broken due to events such as an opened solder joint.

The UV and OV thresholds for Buck1, Buck2, Buck3, and LDO4 are fixed at 92% and 108%. Other options for UV and OV thresholds are available for each output, see Table 2 on page 23 for UV threshold options and Table 3 on page 23 for OV threshold options. **Note:** UV and OV thresholds for each output can be chosen independently.

An undervoltage fault is reported when a Buck or the LDO output voltage falls below the preset threshold. An optional 10µs filter can be factory-programmed to provide additional glitch rejection. If selected, the 10µs is enabled for all outputs.

For the bucks, detection of an output overvoltage above the preset threshold immediately tri-states the corresponding output switches. An overvoltage fault is reported when a buck or the LDO output voltage remains above the preset threshold for 10µs (typical), which provides glitch rejection.

In the ISL78083, UV faults and OV faults force the corresponding PGOOD1, PGOOD2/3, or PGOOD4 voltage low for 200ms (typical) as a reset signal to the system controller. If the UV condition is caused by an overcurrent fault, the RSTB output is triggered.

Note: UV and OV faults on Buck2/3 do not disable the output or enable the hiccup restart protection. If the fault condition is removed, the output continues to regulate and the PGOOD2/3 output drives an open-circuit. Output disable with hiccup restart does occur if the fault is caused by overcurrent.

Table 2. Factory-Programmable UV Options for Buck1, Buck2, Buck3, and LDO4

Option Code (hex)	Buck1 UV Threshold Typical (%) Register 0x72, Bits 0-3	Buck2 UV Threshold Typical (%) Register 0x74, Bits 0-3	Buck3 UV Threshold Typical (%) Register 0x76, Bits 0-3	LDO4 UV Threshold Typical (%) Register 0x78, Bits 0-3
0	96	96	96	96
1	94	94	94	94
2 (default)	92	92	92	92
3	88	88	88	88

Table 3. Factory-Programmable OV Options for Buck1, Buck2, Buck3, and LDO4

Option Code (hex)	Buck1 OV Threshold Typical (%) Register 0x72, Bits 4-7	Buck2 OV Threshold Typical (%) Register 0x74, Bits 4-7	Buck3 OV Threshold Typical (%) Register 0x76, Bits 4-7	LDO4 OV Threshold Typical (%) Register 0x78, Bits 4-7
0	104	104	104	104
1	106	106	106	106
2 (default)	108	108	108	108
3	112	112	112	112

4.3 Protection Features

For enhanced protection the ISL78083 provides one set of reference/DAC circuits for the output voltage regulation of Buck1, Buck2, Buck3, and LDO4, and a separate set of reference/DAC circuits for the UV/OV detection. For Buck1, output UV/OV is sensed at the LDOIN4, whereas output regulation is sensed at the FB1. This separation inhibits a single-point failure in the Buck1 feedback path from causing a severe overvoltage at the output of Buck1. **Note:** FB1, LDOIN4, and the output of Buck1 must all be tied together on the PCB.

4.4 Input Undervoltage Lockout

The VIN1 Undervoltage Lockout (UVLO) has a default, a fixed rising edge of 4.5V (typical), and falling edge of 3.5V. Other options for the rising edge can be factory-programmed, see Table 4. The falling threshold for all options is fixed at 3.5V. **Note:** VIN1 must exceed the rising UVLO threshold before the IC can power up. The default setting is code 0 which is 4.5V. Though the device is capable of operating with VIN1 as low as 4V, the device cannot start up until VIN1 reaches 4.5V.

Note: At initial power-up, the default rising edge (4.5V) is in effect until the IC has initialized and configured the UVLO circuits. In cases where Option Codes 1, 2, or 3 are used, the ramp rate of VIN1 should be less than 1V/ms, to allow the UVLO circuits sufficient time to initialize before VIN1 rises above the 4.5V default threshold.

Table 4. Factory-Programmable VIN1 UVLO Options

Option Code (hex) Register 0x70	VIN1 UVLO Rising Threshold Typical (V)	VIN1 UVLO Falling Threshold Typical (V)
0 (default)	4.5	3.5
1	5.0	3.5
2	6.5	3.5
3	7.0	3.5

4.5 Output Startup and Shutdown

Startup and shutdown of the outputs are initiated using the EN and EN_LV pins. The EN input controls the Buck1 output and the EN_LV controls the low voltage outputs (LV outputs, Bucks 2, 3, and LDO4). If EN is driven high while EN_LV is held low, only Buck1 starts. After the Buck1 output has started, the low voltage outputs start when EN_LV is driven high. If the EN_LV input is driven low, the low voltage outputs shut down. If the EN is driven low, the low voltage outputs shut down first (if already ON), and the high-voltage Buck1 output shuts down.

The delay time between the start of Bucks 2, 3, and LDO4 is set to zero (no delay, all three outputs start at the same time). Other factory-programmable options for startup sequencing and delay between the LV outputs are available, see Table 5 and Table 6. The outputs are started in sequence, and the startup delays are the same between the different outputs. **Note:** The delay controls only the starting time for each output, not the actual rise time of each output voltage, which depends on the application, the load, and internal soft-start settings.

The shutdown delay time is set to zero by default. Other factory-programmable options for shutdown sequence and delay are available, see Tables 5 and 6. As with the startup delays, all shutdown delays between outputs are the same value. **Note:** The shutdown delay controls only the output disable timing, not the actual fall time of each output, which depends on the output capacitance, load, and the configuration of the optional output discharge function.

When shut down, each Buck2, Buck3, and LDO4 tri-states into high impedance. An optional internal pull-down for each of these outputs can be factory-programmed, to actively discharge the output during shutdown. **Note:** The pulldowns are active only for 200ms after the outputs are disabled, after which the pulldowns are disabled.

There are two different factory-programmable startup sequence options:

- Buck1 -> Buck2 -> Buck3 -> LDO4
- Buck1 -> LDO4 -> Buck2 -> Buck3

The shutdown sequence follows the reverse order of the startup sequence.

Note: Buck1 always powers up before the low voltage outputs, and always powers down after the low voltage outputs.

Table 5. Startup and Shutdown Delay Factory-Programmable Options

Register 0x79 Bits 3-5		Register 0x79 Bits 0-2	
Option Code (hex)	Startup Delay Typical (ms)	Option Code (hex)	Shutdown Delay Typical (ms)
0 (default)	0	0 (default)	0
1	0.5	1	0.5
2	1	2	1
3	2	3	2
4	4	4	4
5	8	5	8
6	16	6	16
7	32	7	32

Table 6. Startup and Shutdown Factory-Programmable Sequence

Option Code (hex) Register 0x79 Bit 7	Startup Sequence (EN High, EN_LV High)	Shutdown Sequence (EN Low)
0 (default)	Buck1 -> Buck2 -> Buck3 -> LDO4	LDO4 -> Buck3 -> Buck2 -> Buck1
1	Buck1 -> LDO4 -> Buck2 -> Buck3	Buck3 -> Buck2 -> LDO4 -> Buck1

If the EN_LV falls while EN remains high, the low voltage outputs are shutdown in sequence while Buck1 remains enabled. If EN is driven low, the low voltage outputs are shut down first in sequence and Buck1 shuts down.

Note: Both EN and EN_LV have a 300µs delay before reacting to any falling edge. If EN or EN_LV fall in the middle of a startup sequence, after 300µs the startup is halted and shutdown sequencing begins from the current state. The startup sequence does not need to complete before the shutdown sequence proceeds when the EN or EN_LV signal falls.

When a shutdown sequence is started, the shutdown is completed, the outputs remain off for 200ms, and the input that initiated the shutdown (EN and/or EN_LV input) is ignored for 200ms. After the 200ms delay is completed the outputs can be restarted.

Startup and shutdown sequencing is shown in Figure 41.

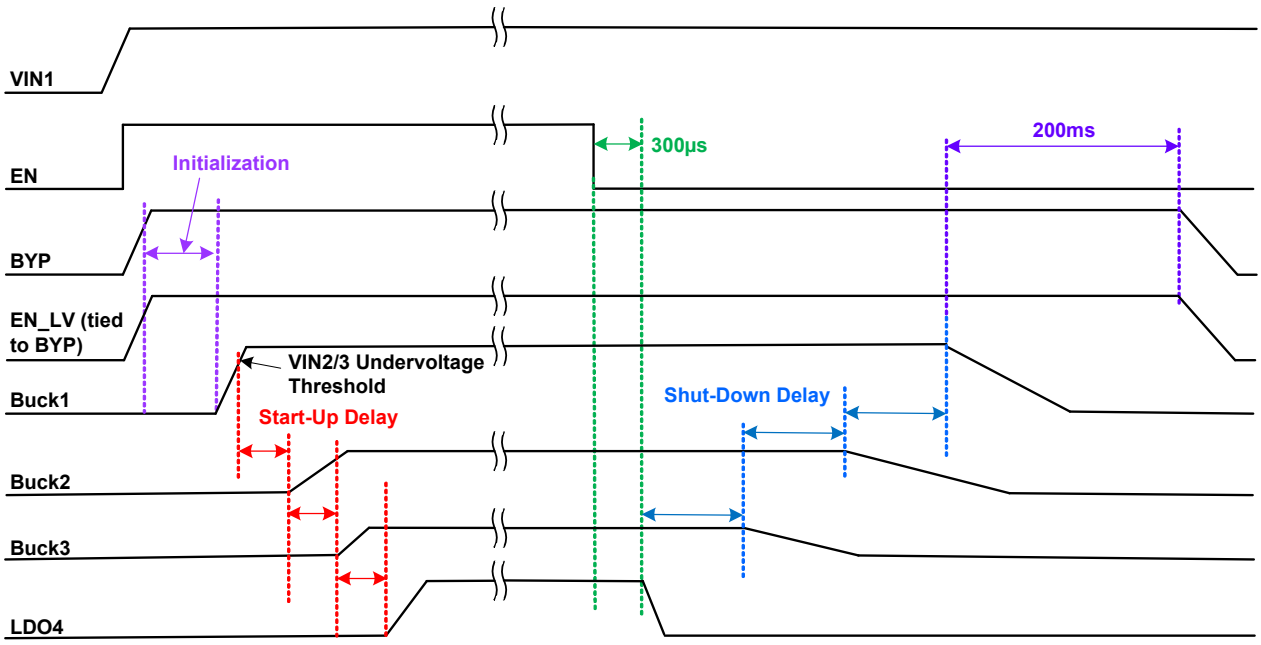


Figure 41. Sequence Timing Diagram

4.6 EN Input

EN is a high-voltage input that can tolerate voltages up to 42V DC. The following are the descriptions of the EN input states.

When EN is logic low (EN at ground), the device is fully shut down (Shutdown state) and current draw from VIN1 is typically 1µA.

When EN reaches 1.2V (typical), the internal BYP LDO regulator powers up (Standby state). When the BYP voltage exceeds the Power-On Reset (POR) threshold of 3.6V (typical), the device goes through internal initialization for typically 900µs, after which the device is ready to begin switching. If EN remains at 1.2V, the device remains in Standby and draws 4mA (typical) from VIN1. The PGOOD outputs are pulled low in this state.

When EN exceeds typically 1.8V (Buck1 ON) and the BYP voltage is above the POR threshold, the device begins the startup cycle for Buck1. If the EN_LV input is logic low, Buck1 remains on while the low voltage outputs (Buck2/3, LDO4) are off. If EN_LV is logic high and VIN2/3 (connected to Buck1 output) is above the VIN2/3

undervoltage threshold of 2.42V (typical), the device begins startup for Buck2/3 and LDO4, using the startup sequence and delay options selected, see Table 6 on page 25.

Falling edges on EN are filtered to prevent spurious shutdowns. If the EN input falls from a higher threshold to a lower threshold, the EN signal must remain at the lower threshold for 300µs before the IC responds. Falling edges on EN are handled differently depending on the threshold (state) and the state of the EN_LV pin.

EN falling edge, from Buck1 ON state to Standby state: after the EN pin falls to the Standby state threshold for 300µs, the device shuts down Buck1/2/3/LDO4, using the factory-programmed shutdown sequence and delay options. If the low voltage outputs (Buck2/3/LDO4) are already off (EN_LV at logic low), the Buck1 regulator shuts down after the shutdown delay has elapsed. In both cases, when Buck1 has shut down, the EN input is ignored for 200ms and all outputs remain off.

EN falling edge, from Buck1 ON state to Shutdown state: after the EN pin falls to the Shutdown threshold for 300µs, the device shuts down all outputs in the same sequence as described in the Buck1 ON state to Standby state case. After Buck1 has shut down, the BYP regulator remains on for 200ms and the EN input is ignored during this time. After 200ms, if the EN pin remains low (Shutdown), the BYP regulator and all internal circuits shut off, and the device goes into full shutdown with input (VIN1) current less than 10µA (typical).

4.7 EN_LV Input

EN_LV is a logic level input that controls the low voltage outputs (Buck2/3/LDO4). When EN_LV is set to logic high, the low voltage outputs start up using the factory-programmed sequence and startup delay options, if the EN input is in the Buck1 ON state and the VIN2/3 input is above its UVLO threshold (2.42V typical). If the EN input is in the Standby or Shutdown state, the Buck1 output is shut down and the low voltage outputs do not start.

To prevent spurious shutdowns, falling edges on EN_LV must be low for 300µs before the device responds. After EN_LV is at logic low for 300µs, the low voltage outputs shut down using the factory-programmed sequence and shutdown delay. After the last output is shut off, the EN_LV pin is ignored for 200ms and the outputs remain off.

Table 7 summarizes the behavior associated with the EN and EN_LV pins.

Table 7. EN and EN_LV Control

EN State	EN Voltage (V)	EN_LV	BYP	Buck1	Buck2/3/LDO4
Shutdown	$V_{EN} \le 0.4$	Logic High or Low	Off	Off	Off
Standby	$V_{EN} = 1.3$ (typical)	Logic High or Low	On	Off	Off
Buck1 ON	$V_{EN} = 1.8$ (typical)	Logic low	On	On	Off
Buck1 ON	$V_{EN} = 1.8$ (typical)	Logic high	On	On	On

Note: Output OFF and ON always follows the selected startup and shutdown sequence.

4.8 Buck1

The primary synchronous buck regulator, Buck1, has a minimum startup voltage of 4.5V. When started, the operating range is 4V to 42V. The Buck1 output voltage is connected to FB1 pin for voltage feedback sensing, which regulates the output at 3.8V. Column 2 of Table 1 on page 21 details the other available factory-programmed voltage settings. Buck1 is an internally-compensated PWM current mode converter that always operates in Forced Continuous Current Mode (FCCM). It shares a fixed 2.2MHz oscillator with Buck2 and Buck3. The output voltage of the regulator is sensed at the FB1 pin, which incorporates an internal resistive voltage divider.

Note: While the regulator operates with input voltages as low as 4V, the Buck1 output voltage can fall below regulation if the input voltage falls too low to maintain the output voltage under existing load and temperature conditions.

Reliability features for this converter include glitch-filtered undervoltage and overvoltage threshold (see "Undervoltage and Overvoltage Protection" on page 22), tri-stating the power switches on overvoltage, cycle-by-cycle overcurrent protection, cycle-by-cycle negative current limiting, and Hiccup mode protection. Fault sensing on Buck1 is done through the LDOIN4 input pin.

The recommended Buck1 component selections are listed in Table 8. The CFG1 pin default is connected to BYP. With the CFG1 pin connected to BYP, the recommended values are L_{OUT} = 4.7µH and C_{OUT_MIN} = 10µF. See the recommended vendor part numbers in Table 8. For other settings of the CFG1 pin, output inductor, and capacitor values, contact Renesas support.

Table 8. Buck1 Components

CFG1 Setting		Value	Vendor/Part Number
Float	L_{OUT}	4.7µH/1.6A	TDK/TDK/TFM252012ALMA4R7MTAA
	C_{OUT_MIN}	10µF/10V/X7R	Murata/GCJ21BR71A106KE01L

4.9 Buck2 and Buck3

The secondary synchronous buck regulators, Buck2 and Buck3, have input voltage operating ranges of 3.3V to 5.5V, and a factory-programmable output voltage range from 1.0V to 3.3V. Table 1 on page 21 lists the available output voltage options. Both are internally-compensated PWM current mode converters that always operate in FCCM. They share a fixed 2.2MHz switching frequency with Buck1. Buck2 is clocked in-phase with Buck1; Buck3 by default switches 180 degrees out of phase with Buck1 but can be factory-programmed to be synchronized to Buck1. The output voltages of Buck2 and Buck3 are sensed at the FB2 and FB3 pins respectively; both incorporate internal resistive voltage dividers. Reliability features for this converter include glitch-filtered undervoltage and overvoltage thresholds (see "Undervoltage and Overvoltage Protection" on page 22), tri-stating switches on OV, cycle-by-cycle overcurrent protection, cycle-by-cycle negative current limiting, and Hiccup mode protection.

Recommend component values for Buck2 and Buck3 are listed in Table 9.

Table 9. Buck2 and Buck3 Components

Buck2/3 Components	Value	Vendor/Part Number
L_{OUT_Buck2}	1.5µH	TDK/TFM201610ALMA1R5MTAA
C_{OUT_MIN2}	20µF	Murata/GCJ21BR71A106KE01L (10µF x 2)
L_{OUT_Buck3}	1.5µH/2.3A	TDK/TFM201610ALMA1R5MTAA
C_{OUT_MIN3}	20µF	Murata/GCJ21BR71A106KE01L (10µF x 2)

4.10 LDO4

The LDO4 linear regulator is a fixed 3.3V output, with a factory-programmable output voltage range from 2.8V to 3.4V. The minimum output capacitor for LDO4 is 1µF. Table 1 shows the available output voltage options. The input to LDO4 (LDOIN4) must be connected to the Buck1 output and has an input operating range of 3.3V to 5.5V. The LDOIN4 input also functions as the undervoltage and overvoltage sense point for Buck1. The maximum LDO4 output current is 300mA. Reliability features for this linear regulator include undervoltage and overvoltage thresholds (see Undervoltage and Overvoltage Protection), and overcurrent limiting (430mA typical). During overcurrent, LDO4 by default does not shut down; shutdown and hiccup restart is available as a factory-programmed option.

4.11 RSTB

The RSTB output is an active-high/active-low fault indicator, which can be activated by various faults. Table 10 lists the default (yes/no) settings for each parameter. Each fault listed in Table 10 can be factory-programmed to either trigger or not trigger a fault notification (RSTB output low). **Note:** The ISL78083 detects and reacts to a fault even if the RSTB notification for that fault is disabled.

Note: The active-high state of RSTB is pulled up internally to the BYP voltage. Circuits or logic signals connected to RSTB must be capable of withstanding the BYP voltage, typically 4.3V.

Table 10. RSTB Fault Indication Default Settings

Output	Undervoltage	Overvoltage	Overcurrent1	Negative Overcurrent	Overcurrent2	Severe Undervoltage	Severe Overvoltage
Buck1	No	No	Yes	No	Yes	Yes	Yes
Buck2	No	No	Yes	No			
Buck3	No	No	Yes	No			
LDO4	No	No	Yes				

4.12 Spread Spectrum Factory-Programmable Options

The three buck regulators share a fixed 2.2MHz oscillator. The phase shift between Buck1 and Buck2 is 0 degrees. The phase shift between Buck1 and Buck3 is 180 degrees by default, with a factory-programmable option of 0 degrees. The oscillator frequency is a fixed 2.2MHz by default, but factory-programmable Spread Spectrum options are available. The options allow choices for the Spread Spectrum dwell time, the percent (%) of frequency modulation, and the direction of modulation. The dwell time, percent modulation, and direction are independently selectable. Spread Spectrum options are listed in Table 11.

Table 11. Spread Spectrum Factory-Programmable Options

Register 0x7A Bits 5-4		Register 0x7A Bits 3-2		Register 0x7A Bits 1-0	
Option Code (hex)	Dwell	Option Code (hex)	% Modulation	Option Code (hex)	Direction
0 (default)	Random 1-63 cycle	0 (default)	Off	0 (default)	Off
1	Fixed 8 cycle	1	1%	1	Downward only
2	Random groups of 3, 7, 11, 15, 19, 23, 27, 31 cycles	2	2%	2	Downward and upward
3	Fixed 24 cycle	3	3%	3	Upward only

5. Layout Guidelines

As with all switching regulators, the Printed Circuit Board (PCB) layout requires careful attention to achieve good performance. Proper PCB layout minimizes the effects of voltage and current spikes that are inherent to fast-switching MOSFET circuits. The following are layout considerations:

- The PCB should have a minimum of four copper layers. Use a full ground plane in the internal layer directly below the top layer. For all components that connect to ground, make sure that each component has one or more vias nearby, to provide a low-impedance path to the ground plane.
- VIN1 input capacitance: Place the input filter capacitor (C_{IN1}) between VIN1 and PGND, as close to the IC pins as possible. Place the high-frequency decoupling capacitor closest to the IC. The loop formed by the input capacitors, VIN1, and PGND must be small to minimize high frequency noise. The copper traces between the capacitors and the IC should be as short and direct as possible.
- Place the Buck1 inductor L_1 near the PHASE1 pin of the IC and connect directly to the pin with short, wide copper.
- Place the boot capacitor (C_{boot}) next to Pins 5 and 6 and use short, direct copper connections.
- Place the VIN2/3 input capacitor ($C_{IN2/3}$) near the VIN2/3 pin of the IC. Place the high-frequency decoupling capacitor closest to the IC. Connect the capacitors to the VIN2/3 pin using short, wide copper. Place multiple ground vias at the ground connection of each capacitor, to provide a low-impedance ground path to the ground of the IC (PGND2/3, pin 22).
- Place Buck2 and Buck3 inductors (L_2 and L_3) next to their respective pins, PHASE2 and PHASE3. Route to the inductors using short, wide copper.
- Place the Buck2 and Buck3 output capacitors (C_{OUT2} and C_{OUT3}) near the inductor and connect using short, wide traces. Use multiple vias and copper on other layers if needed to connect from C_{OUT2} or C_{OUT3} to their load circuit.
- Place multiple ground vias at the ground connection of C_{OUT2} and C_{OUT3}, to provide a low-impedance ground path to the Buck2/3 ground return at the IC (PGND2/3, pin 22).
- Route the feedback for Buck3 directly from C_{OUT3} to the FB3 pin (Pin 21), as seen in the layout in light blue color. Provide some space clearance between the FB3 trace (which is noise-sensitive) and the high-noise PHASE3 trace.
- Route the feedback for Buck2 on an inner layer, connecting from C_{OUT2} to FB2 (Pin 22). FB2 is a noise-sensitive input. Route the trace so that it avoids passing underneath the inductors L_2, L_3, or L_1, and also avoids passing underneath under the PHASE signals or pins. Renesas recommends routing the trace on an inner layer, going around C_{OUT3}, and then routing to Pin 22. VOUT2 (Buck2 output) and the FB2 pin are shown in yellow in Figure 42 on page 30.
- LDOIN4 and FB1 (Pins 18 and 17) must be connected to VOUT1, which is the output of Buck1 and is connected to the VIN2/3 pin (Pin 1). Use wide copper to route from VOUT1 to LDOIN4. The LDOIN4 pin is the input for the LDOOUT4 output, which dictates that the LDOIN4 trace must carry all the LDO load current. When routing the connection from VOUT1 to LDOIN4, avoid routing underneath any of the inductors and also any PHASE nodes. Renesas recommends using inner layer copper, connecting from VOUT1 to LDOIN4 (all shown in white), routing directly underneath the IC, while avoiding the PHASE and BOOT pins of the IC (Pins 5, 6, 23, 24). **Note:** The LDOIN4 pin also functions as the overvoltage and undervoltage sense point for Buck1. To minimize I•R voltage drop due to copper resistance, use a wide trace to route to LDOIN4.
- FB1 (Pin 17) is the feedback input for Buck1. This pin ultimately connects to the same net as LDOIN4. It is possible to combine the path for FB1 and LDOIN4 into a single trace, however the trace needs to be wide to minimize I•R voltage drop due to the LDOIN4 loading. Alternatively, a separate trace on an inner layer can route from the V_{OUT1} output to the FB1 pin. Route this trace away from all high-noise nodes and components, including the inductors, capacitors C_{IN1} and $C_{IN2/3}$, and the PHASE and BOOT nodes.

- Place input and output capacitors for the LDO (100nF and CLDOOUT4) near the IC and routed directly with short wide traces. Place multiple ground vias at the ground connection of the capacitors to provide a low-impedance ground path to the ground return at the IC.
- Connect all the grounds pins (Pins 10, 11, and 22) and the thermal PAD (Pin 25) together using a single wide copper pad under the IC. Connect this copper pad to the ground plane using multiple vias, to provide a low-impedance path to the ground plane and also to provide heatsinking through the PCB copper.
- Place the BYP capacitor (C_{BYP}) very near the BYP pin (Pin 12). Route to the capacitor using a short, wide PCB trace, for both the BYP and the ground paths. If needed, place multiple ground vias at the ground connection of C_{BYP}, to provide a low-impedance ground path to the ground of the IC (PGND2/3, Pin 22).

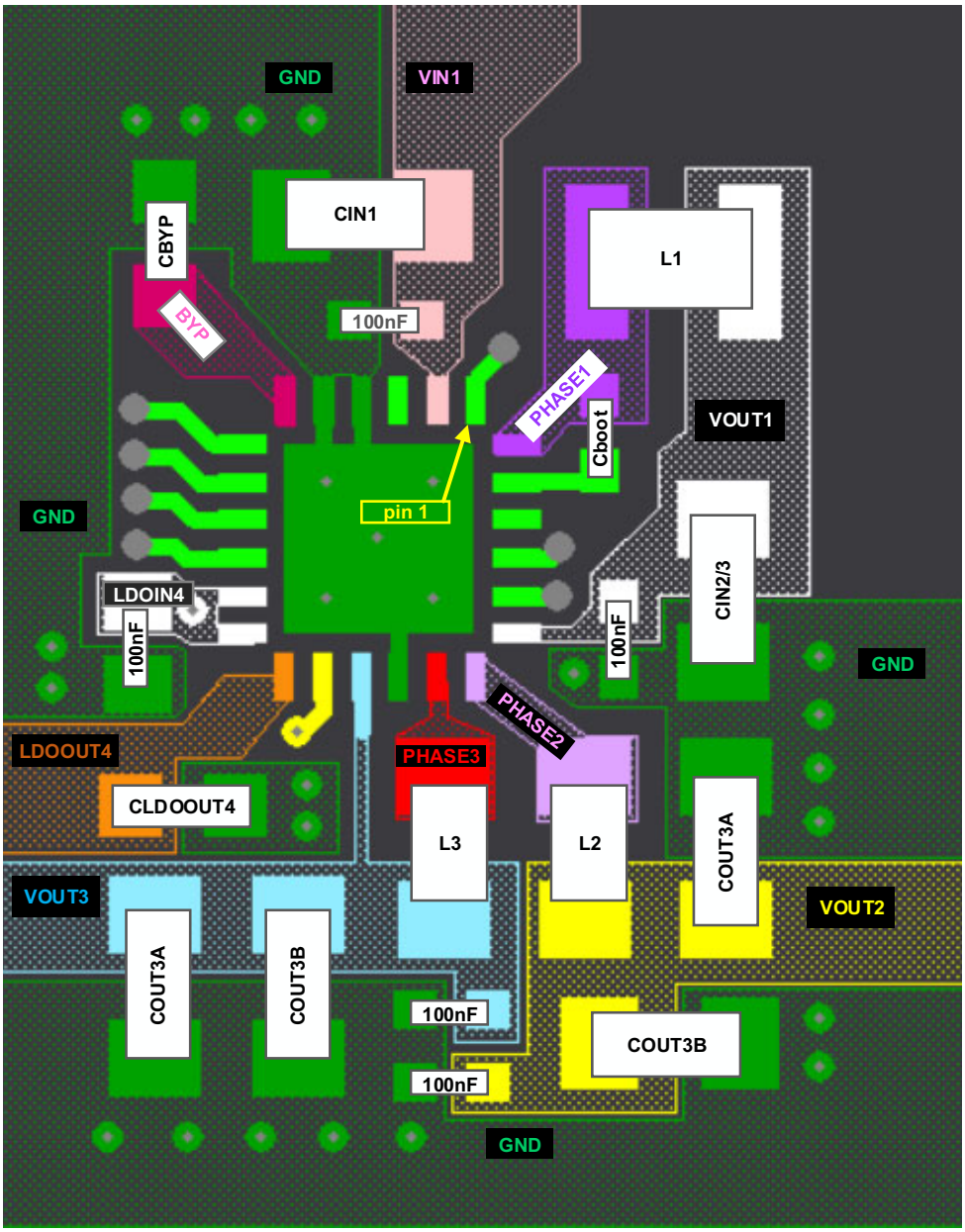


Figure 42. PCB Layout

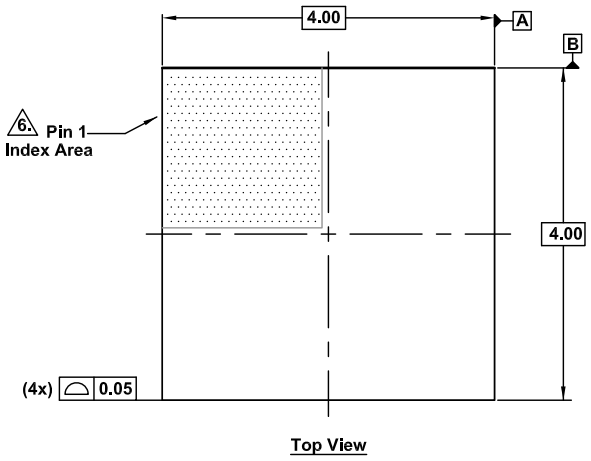
6. Revision History

Rev.	Date	Description
1.00	Nov.15.19	Initial release

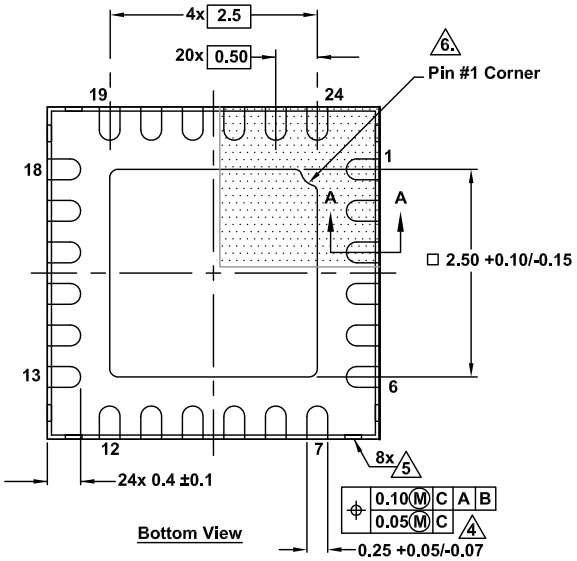
7. Package Outline Drawing

For the most recent package outline drawing, see L24.4x4K.

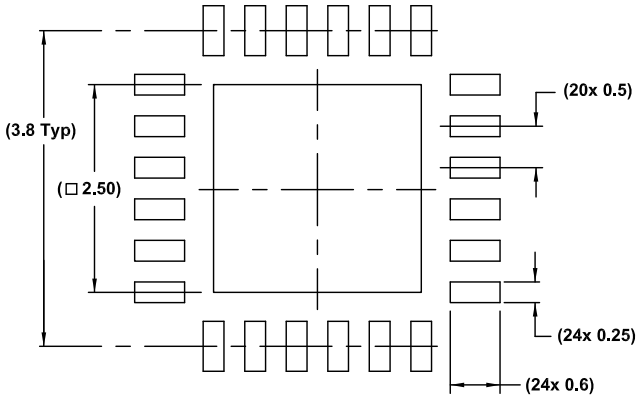
L24.4x4K
24 Lead Step Cut Quad Flat No-Lead Plastic Package (SCQFN)
Rev 2, 12/18



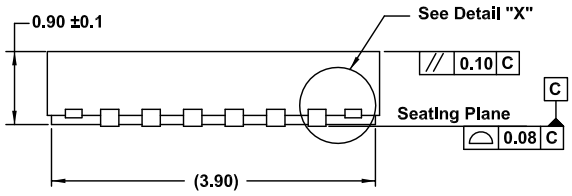
Top View



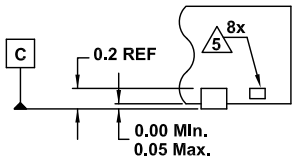
Bottom View



Typical Recommended Land Pattern



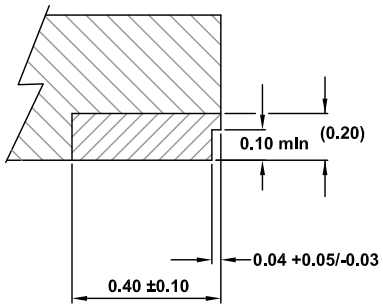
Side View



Detail "X"

Notes:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ±0.05
4. This dimension applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.



Section : A-A
Scale : NTS

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