

**HS-4424DRH, HS-4424DEH**

Dual, Noninverting Power MOSFET Radiation Hardened Drivers

FN8747  
Rev 3.00  
Jan 12, 2021

The radiation hardened HS-4424 family are noninverting, dual, monolithic high-speed MOSFET drivers designed to convert low voltage control input signals into higher voltage, high current outputs. The HS-4424DRH, HS-4424DEH are fully tested across the 8V to 18V operating range.

The inputs of these devices can be directly driven by the HS-1825ARH PWM device or by our ACS/ACTS and HCS/HCTS type logic devices. The fast rise times and high current outputs allow very quick control of high gate capacitance power MOSFETs in high frequency applications.

The high current outputs minimize power losses in MOSFETs by rapidly charging and discharging the gate capacitance. The output stage incorporates a low voltage lockout circuit that puts the outputs into a three-state mode when the supply voltage is below its Undervoltage Lockout (UVLO) threshold voltage.

Constructed with a dielectrically isolated Rad Hard Silicon Gate (RSG) BiCMOS process, these devices are immune to single event latch-up and have been specifically designed to provide highly reliable performance in harsh radiation environments.

**TABLE 1. HS4424 PRODUCT FAMILY SPECIFIC UVLO Vth**

PART NUMBER	UVLO (V)
HS-4424RH HS-4424EH	<10
HS4424BRH HS4424BEH	<7.5
HS4424DRH HS4424DEH	<8

**Related Literature**

For a full list of related documents, visit our website:

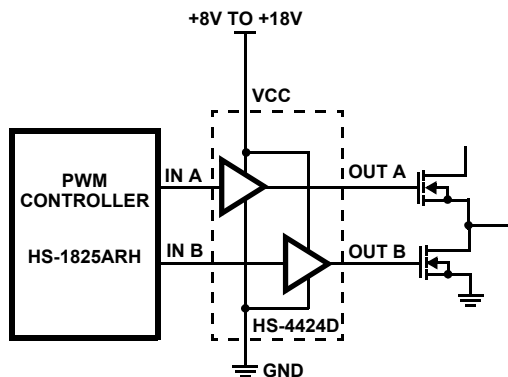
- [HS-4424DRH, HS-4424DEH](#)

**Features**

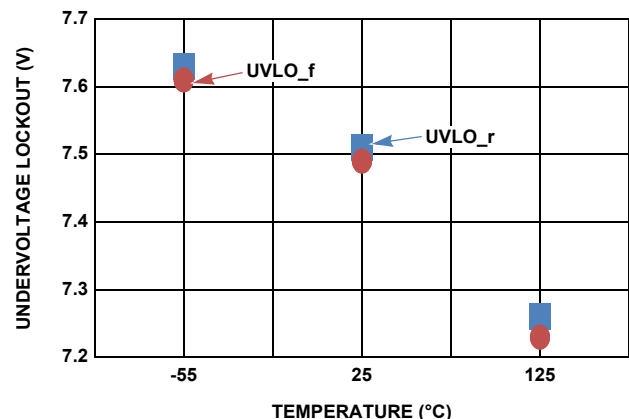
- Electrically screened to DLA SMD# [5962-99560](#)
- QML qualified per MIL-PRF-38535 requirements
- Latch-up immune
- Radiation acceptance testing - HS-4424DRH
  - High dose rate (50-300rad(Si)/s) . . . . . 300krad(Si)
- Radiation acceptance testing - HS-4424DEH
  - High dose rate (50-300rad(Si)/s) . . . . . 300krad(Si)
  - Low dose rate (0.01rad(Si)/s) . . . . . 50krad(Si)\*
  - \*Limit established by characterization
- I<sub>PEAK</sub> . . . . . >2A (minimum)
- Matched rise and fall times (C<sub>L</sub> = 4300pF) . . 75ns (maximum)
- Low voltage lockout feature . . . . . <8V
- Wide supply voltage range . . . . . 8V to 18V
- Propagation delay . . . . . 250ns (maximum)
- Consistent delay times with V<sub>CC</sub> changes
- Low power consumption
  - 40mW with inputs high
  - 20mW with inputs low
- Low equivalent input capacitance . . . . . 3.2pF (typical)
- ESD protected . . . . . >4kV

**Applications**

- Switching power supplies
- DC/DC converters
- Motor controllers

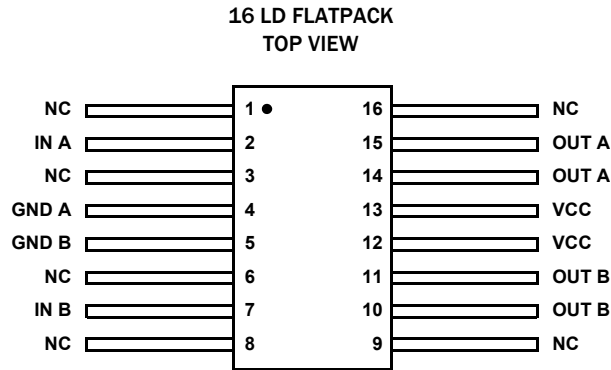


**FIGURE 1. TYPICAL APPLICATION**



**FIGURE 2. UNDERVOLTAGE LOCKOUT vs TEMPERATURE**

# Pin Configuration



## Pin Descriptions

PIN NUMBER	PIN NAME	EQUIVALENT ESD CIRCUIT	DESCRIPTION
1, 3, 6, 8, 9, 16	NC	NA	No Internal Connection
2	IN A	Circuit 2	Driver A Input
4	GND A	NA	Ground Reference A
5	GND B	NA	Ground Reference B
7	IN B	Circuit 2	Driver B Input
10, 11	OUT B	NA	Driver B Output
12, 13	VCC	Circuit 1	Positive Power Supply
14, 15	OUT A	NA	Driver A Output

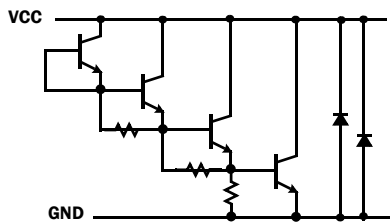


FIGURE 3. CIRCUIT 1

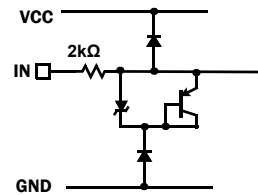


FIGURE 4. CIRCUIT 2

# Functional Block Diagram

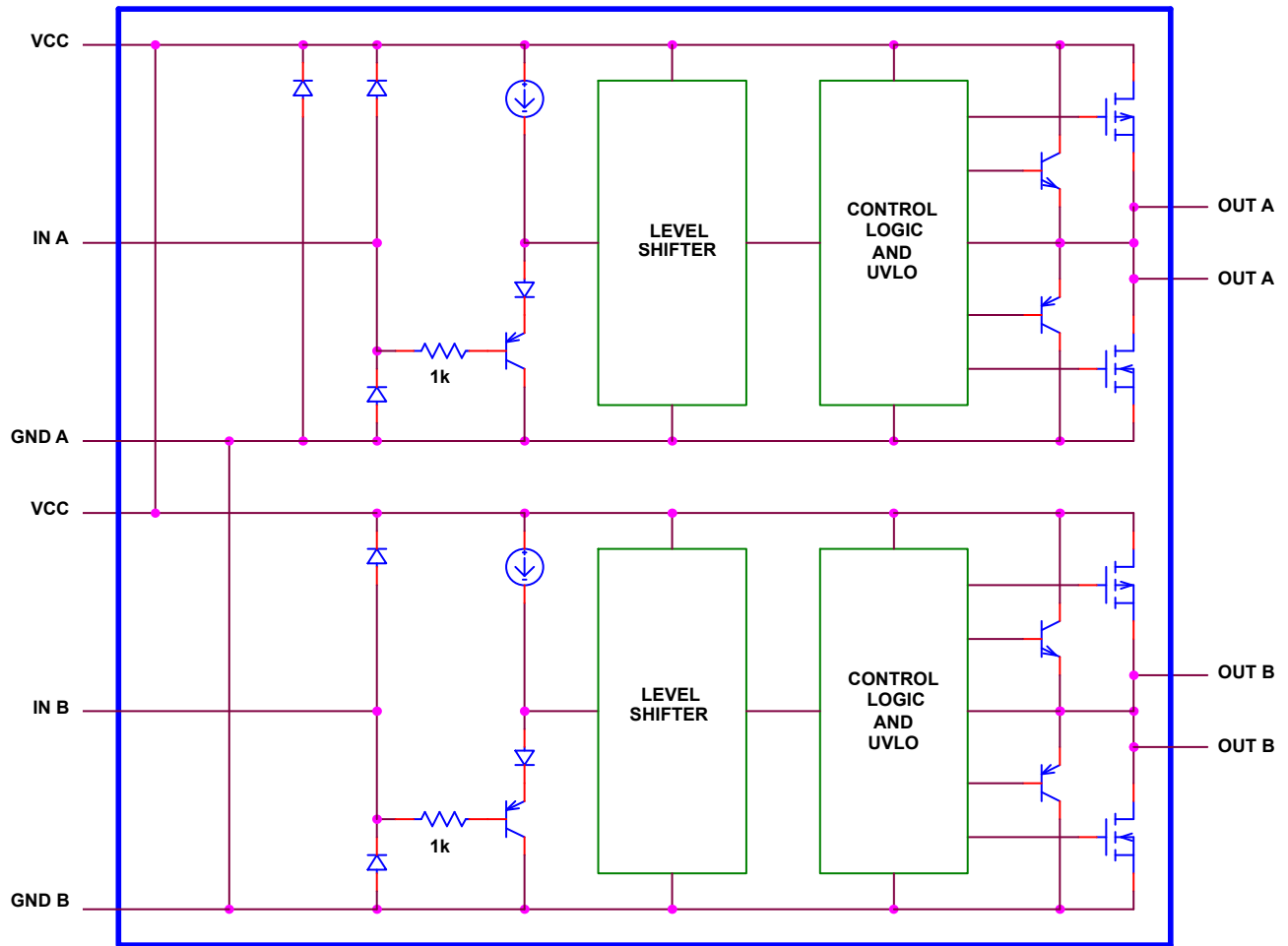


FIGURE 5. BLOCK DIAGRAM

## Ordering Information

SMD NUMBER ORDERING (Note 2)	PART NUMBER (Note 1)	RADIATION HARDNESS (Total Ionizing Dose)	TEMPERATURE RANGE (°C)	PACKAGE (RoHS Compliant)	PKG. DWG. #
5962F9956005V9A	HS0-4424DRH-Q (Note 3)	HDR to 300krad(Si)	-55 to +125	DIE	N/A
5962F9956005VXC	HS9-4424DRH-Q		-55 to +125	16 Ld Flatpack	K16.A
N/A	HS9-4424DRH/PROTO (Note 4)	N/A	-55 to +125	16 Ld Flatpack	K16.A
N/A	HS0-4424DRH/SAMPLE (Notes 3, 4)		-55 to +125	DIE SAMPLE	N/A
5962F9956006V9A	HS0-4424DEH-Q (Note 3)	HDR to 300krad(Si), LDR to 50krad(Si)	-55 to +125	DIE	N/A
5962F9956006VXC	HS9-4424DEH-Q		-55 to +125	16 Ld Flatpack	K16.A

### NOTES:

1. These Pb-free Hermetic packaged products employ 100% Au plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations.
2. Specifications for Rad Hard QML devices are controlled by the Defense Logistics Agency Land and Maritime (DLA). The SMD numbers listed in the table must be used when ordering.
3. Die product tested at  $T_A = +25^\circ\text{C}$ . The wafer probe test includes functional and parametric testing sufficient to make the die capable of meeting the electrical performance outlined in ["Electrical Specifications" on page 5](#).
4. The /PROTO and /SAMPLE are not rated or certified for Total Ionizing Dose (TID) or Single Event Effect (SEE) immunity. These parts are intended for engineering evaluation purposes only. The /PROTO parts meet the electrical limits and conditions across temperature specified in the DLA SMD and are in the same form and fit as the qualified device. The /SAMPLE parts are capable of meeting the electrical limits and conditions specified in the DLA SMD. The /SAMPLE parts do not receive 100% screening across temperature to the DLA SMD electrical limits. These part types do not come with a Certificate of Conformance because they are not DLA qualified devices.

### Absolute Maximum Ratings

Maximum Supply Voltage .....	20V
Min/Max Input Voltage .....	- 0.3V to V <sub>CC</sub>
Output Short-circuit Duration (1 output at a time) .....	Indefinite
<b>ESD Rating</b>	
Human Body Model (Tested per MIL-PRF-883 3015.7) .....	5kV
Machine Model (Tested per MIL-PRF-883 3015.7) .....	200V
Charged Device Model (Tested per JESD22-C101D) .....	750V

### Thermal Information

Thermal Resistance (Typical)	$\theta_{JA}$ (°C/W)	$\theta_{JC}$ (°C/W)
16 Ld Flatpack Package (Notes 5, 6) .....	34	5
Storage Temperature Range .....	-65°C to +150°C	
Maximum Operating Junction Temperature .....	+175°C	
Maximum Lead Temperature (Soldering 10 secs) .....	+265°C	

### Recommended Operating Conditions

Ambient Operating Temperature Range .....	-55°C to +125°C
Maximum Operating Junction Temperature .....	+150°C
Supply Voltage .....	8V to 18V

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

**NOTES:**

- $\theta_{JA}$  is measured in free air with the component mounted on a high effective thermal conductivity test board with direct attach features. See [IB379](#) for details.
- For  $\theta_{JC}$ , the case temperature location is the center of the package underside.

**Electrical Specifications** V<sub>CC</sub> = 8V, 12V, 18V, T<sub>A</sub> = +25°C, unless otherwise noted. **Boldface limits apply across the operating temperature range, -55°C to +125°C; over radiation total ionizing dose.**

PARAMETER	DESCRIPTION	TEST CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNIT
V <sub>SUPPLY</sub>	Supply Voltage Range		<b>8</b>		<b>18</b>	V
I <sub>CCSB LOW</sub>	18V Bias Current	V <sub>S</sub> = 18V, Inputs = 0V			3.5	mA
		V <sub>S</sub> = 18V, Inputs = 0V			<b>4</b>	mA
		V <sub>S</sub> = 18V, Inputs = 0V, post radiation			<b>4</b>	mA
I <sub>CCSB HIGH</sub>	18V Bias Current	V <sub>S</sub> , Inputs = 18V			3.5	mA
		V <sub>S</sub> , Inputs = 18V			<b>4</b>	mA
		V <sub>S</sub> , Inputs = 18V, post radiation			<b>4</b>	mA
I <sub>CCSB LOW</sub>	8V Bias Current	V <sub>S</sub> = 8V, Inputs = 0V			3.5	mA
		V <sub>S</sub> = 8V, Inputs = 0V			<b>4</b>	mA
		V <sub>S</sub> = 8V, Inputs = 0V, post radiation			<b>4</b>	mA
I <sub>CCSB HIGH</sub>	8V Bias Current	V <sub>S</sub> , Inputs = 8V			3.5	mA
		V <sub>S</sub> , Inputs = 8V			<b>4</b>	mA
		V <sub>S</sub> , Inputs = 8V, post radiation			<b>4</b>	mA
I <sub>IL_18</sub>	Input Current Low	V <sub>S</sub> = 18V, Inputs = 0V	-5	0.08	5	µA
		V <sub>S</sub> = 18V, Inputs = 0V	<b>-10</b>		<b>10</b>	µA
		V <sub>S</sub> = 18V, Inputs = 0V, post radiation	<b>-10</b>		<b>10</b>	µA
I <sub>IH_18</sub>	Input Current High	V <sub>S</sub> , Inputs = 18V	-5	0.08	5	µA
		V <sub>S</sub> , Inputs = 18V	<b>-10</b>		<b>10</b>	µA
		V <sub>S</sub> , Inputs = 18V, post radiation	<b>-10</b>		<b>10</b>	µA
I <sub>IL_8</sub>	Input Current Low	V <sub>S</sub> = 8V, Inputs = 0V	-5	0.08	5	µA
		V <sub>S</sub> = 8V, Inputs = 0V	<b>-10</b>		<b>10</b>	µA
		V <sub>S</sub> = 8V, Inputs = 0V, post radiation	<b>-10</b>		<b>10</b>	µA
I <sub>IH_8</sub>	Input Current High	V <sub>S</sub> , Inputs = 8V	-5	0.08	5	µA
		V <sub>S</sub> , Inputs = 8V	<b>-10</b>		<b>10</b>	µA
		V <sub>S</sub> , Inputs = 8V, post radiation	<b>-10</b>		<b>10</b>	µA
V <sub>OH</sub>	Output Voltage High	V <sub>S</sub> = 8V, I <sub>OUT</sub> = 5mA	V <sub>S</sub> - 0.75	V <sub>S</sub> - 0.45		V
			<b>V<sub>S</sub> - 0.9</b>			V

**Electrical Specifications**  $V_{CC} = 8V, 12V, 18V, T_A = +25^\circ C$ , unless otherwise noted. **Boldface limits apply across the operating temperature range,  $-55^\circ C$  to  $+125^\circ C$ ; over radiation total ionizing dose. (Continued)**

PARAMETER	DESCRIPTION	TEST CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNIT
V <sub>OL</sub>	Output Voltage Low	V <sub>S</sub> = 8V, I <sub>OUT</sub> = 5mA		0.45	0.8	V
					<b>0.8</b>	V
V <sub>OH</sub>	Output Voltage High	V <sub>S</sub> = 8V, I <sub>OUT</sub> = 50mA	V <sub>S</sub> - 0.95	V <sub>S</sub> - 0.75		V
			<b>V<sub>S</sub> - 1.1</b>			V
V <sub>OL</sub>	Output Voltage Low	V <sub>S</sub> = 8V, I <sub>OUT</sub> = 50mA		0.75	0.95	V
					<b>1.1</b>	V
V <sub>OH</sub>	Output Voltage High	V <sub>S</sub> = 12V, I <sub>OUT</sub> = 5mA	V <sub>S</sub> - 0.75	V <sub>S</sub> - 0.45		V
			<b>V<sub>S</sub> - 0.75</b>			V
V <sub>OL</sub>	Output Voltage Low	V <sub>S</sub> = 12V, I <sub>OUT</sub> = 5mA		0.45	0.8	V
					<b>0.8</b>	V
V <sub>OH</sub>	Output Voltage High	V <sub>S</sub> = 12V, I <sub>OUT</sub> = 50mA	V <sub>S</sub> - 0.95	V <sub>S</sub> - 0.75		V
			<b>V<sub>S</sub> - 1.1</b>			V
V <sub>OL</sub>	Output Voltage Low	V <sub>S</sub> = 12V, I <sub>OUT</sub> = 50mA		0.75	0.95	V
					<b>1.1</b>	V
V <sub>OH</sub>	Output Voltage High	V <sub>S</sub> = 18V, I <sub>OUT</sub> = 5mA	V <sub>S</sub> - 0.75	V <sub>S</sub> - 0.45		V
			<b>V<sub>S</sub> - 0.75</b>			V
V <sub>OL</sub>	Output Voltage Low	V <sub>S</sub> = 18V, I <sub>OUT</sub> = 5mA		0.45	0.8	V
					<b>0.8</b>	V
V <sub>OH</sub>	Output Voltage High	V <sub>S</sub> = 18V, I <sub>OUT</sub> = 50mA	V <sub>S</sub> - 0.95	V <sub>S</sub> - 0.75		V
			<b>V<sub>S</sub> - 1.1</b>			V
V <sub>OL</sub>	Output Voltage Low	V <sub>S</sub> = 18V, I <sub>OUT</sub> = 50mA		0.75	0.95	V
					<b>1.1</b>	V
V <sub>IH_18</sub>	Input Voltage High Threshold	V <sub>S</sub> = 18V	3			V
			<b>3.1</b>			V
V <sub>IL_18</sub>	Input Voltage Low Threshold	V <sub>S</sub> = 18V			0.8	V
					<b>0.8</b>	V
V <sub>IHYS_18</sub>	Input Voltage Threshold Hysteresis	V <sub>S</sub> = 18V	100			mV
V <sub>IH_12</sub>	Input Voltage High Threshold	V <sub>S</sub> = 12V	3			V
			<b>3.1</b>			V
V <sub>IL_12</sub>	Input Voltage Low Threshold	V <sub>S</sub> = 12V			0.8	V
					<b>0.8</b>	V
V <sub>HYS_12</sub>	Input Voltage Threshold Hysteresis	V <sub>S</sub> = 12V	100			mV
V <sub>IH_8</sub>	Input Voltage High Threshold	V <sub>S</sub> = 8V	3			V
			<b>3.1</b>			V
V <sub>IL_8</sub>	Input Voltage Low Threshold	V <sub>S</sub> = 8V			0.8	V
					<b>0.8</b>	V
V <sub>HYS_8</sub>	Input Voltage Threshold Hysteresis	V <sub>S</sub> = 8V	100			mV
UVLO <sub>r</sub>	Rising Undervoltage Lockout		7.2	7.5	7.8	V
			<b>6.9</b>		<b>7.95</b>	V
UVLO <sub>f</sub>	Falling Undervoltage Lockout		7.1	7.45	7.75	V
			<b>6.8</b>		<b>7.9</b>	V
HYS_UVLO	Undervoltage Lockout Hysteresis	UVLO <sub>r</sub> - UVLO <sub>f</sub>		23		mV
				24		mV
Min_PW	Minimum Input Pulse Width		100			ns

**Electrical Specifications**  $V_{CC} = 8V, 12V, 18V, T_A = +25^\circ C$ , unless otherwise noted. **Boldface limits apply across the operating temperature range,  $-55^\circ C$  to  $+125^\circ C$ ; over radiation total ionizing dose. (Continued)**

PARAMETER	DESCRIPTION	TEST CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNIT	
<b>TRANSIENT RESPONSE</b>							
$t_r, t_f$	Rise Time 10% to 90% of $V_{OUT}$	$V_S = 18V, C_L = 4300pF$			75	ns	
		$V_S = 18V, C_L = 4300pF$			<b>95</b>	ns	
		$V_S = 18V, C_L = 4300pF$ , post radiation			<b>95</b>	ns	
	Fall Time 90% to 10% of $V_{OUT}$	$V_S = 18V, C_L = 4300pF$				75	ns
		$V_S = 18V, C_L = 4300pF$				<b>95</b>	ns
		$V_S = 18V, C_L = 4300pF$ , post radiation				<b>95</b>	ns
	Rise Time 10% to 90% of $V_{OUT}$	$V_S = 12V, C_L = 4300pF$				75	ns
		$V_S = 12V, C_L = 4300pF$				<b>95</b>	ns
		$V_S = 12V, C_L = 4300pF$ , post radiation				<b>95</b>	ns
	Fall Time 90% to 10% of $V_{OUT}$	$V_S = 12V, C_L = 4300pF$				75	ns
		$V_S = 12V, C_L = 4300pF$				<b>95</b>	ns
		$V_S = 12V, C_L = 4300pF$ , post radiation				<b>95</b>	ns
Rise Time 10% to 90% of $V_{OUT}$	$V_S = 8V, C_L = 4300pF$				75	ns	
	$V_S = 8V, C_L = 4300pF$				<b>95</b>	ns	
	$V_S = 8V, C_L = 4300pF$ , post radiation				<b>95</b>	ns	
Fall Time 90% to 10% of $V_{OUT}$	$V_S = 8V, C_L = 4300pF$				75	ns	
	$V_S = 8V, C_L = 4300pF$				<b>95</b>	ns	
	$V_S = 8V, C_L = 4300pF$ , post radiation				<b>95</b>	ns	
$t_{PHL}, t_{PLH}$	50% of Rising Input to 10% of Rising Output	$V_S = 18V, C_L = 4300pF$			200	ns	
		$V_S = 18V, C_L = 4300pF$			<b>300</b>	ns	
		$V_S = 18V, C_L = 4300pF$ , post radiation			<b>300</b>	ns	
	50% of Falling Input to 90% of Falling Output	$V_S = 18V, C_L = 4300pF$				200	ns
		$V_S = 18V, C_L = 4300pF$				<b>300</b>	ns
		$V_S = 18V, C_L = 4300pF$ , post radiation				<b>300</b>	ns
	50% of Rising Input to 10% of Rising Output	$V_S = 12V, C_L = 4300pF$				250	ns
		$V_S = 12V, C_L = 4300pF$				<b>350</b>	ns
		$V_S = 12V, C_L = 4300pF$ , post radiation				<b>350</b>	ns
	50% of Falling Input to 90% of Falling Output	$V_S = 12V, C_L = 4300pF$				250	ns
		$V_S = 12V, C_L = 4300pF$				<b>350</b>	ns
		$V_S = 12V, C_L = 4300pF$ , post radiation				<b>350</b>	ns
	50% of Rising Input to 10% of Rising Output	$V_S = 8V, C_L = 4300pF$				300	ns
		$V_S = 8V, C_L = 4300pF$				<b>400</b>	ns
		$V_S = 8V, C_L = 4300pF$ , post radiation				<b>400</b>	ns
	50% of Falling Input to 90% of Falling Output	$V_S = 8V, C_L = 4300pF$				300	ns
		$V_S = 8V, C_L = 4300pF$				<b>400</b>	ns
		$V_S = 8V, C_L = 4300pF$ , post radiation				<b>400</b>	ns

## NOTE:

7. Compliance to datasheet limits is assured by one or more methods; production test, characterization and/or design.

# Typical Performance Curves

Unless otherwise specified,  $V_S = 8V, 12V, 18V, C_L = 4300pF, T_A = +25^\circ C$ .

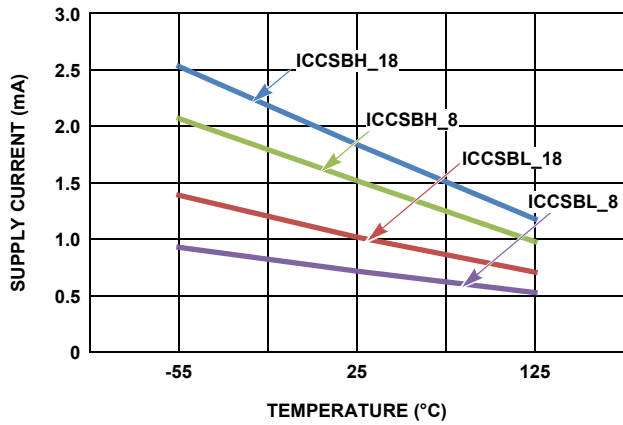


FIGURE 6. SUPPLY CURRENT vs TEMPERATURE

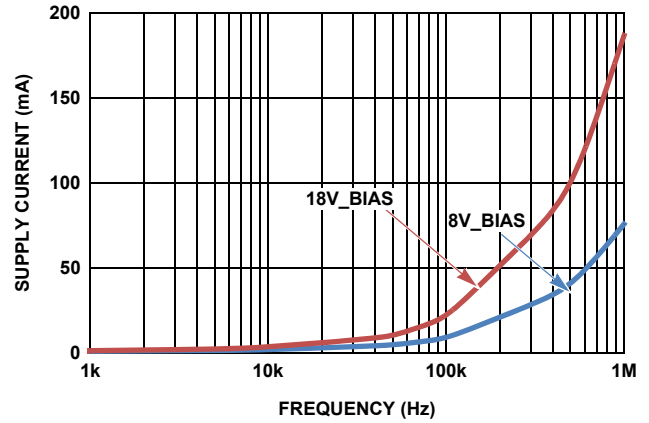


FIGURE 7. SUPPLY CURRENT vs DUAL SWITCHING AT FREQUENCY

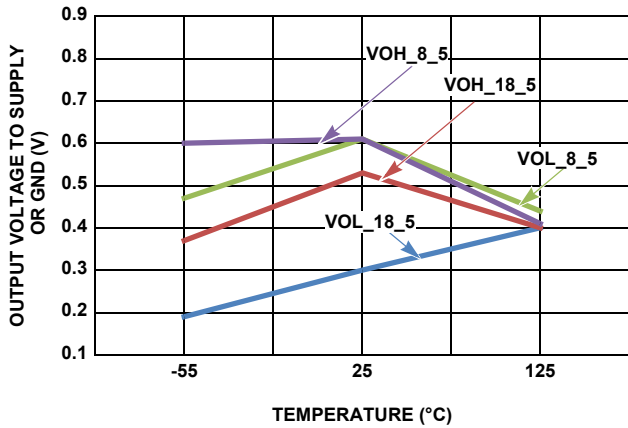


FIGURE 8. OUTPUT VOLTAGE vs TEMPERATURE (5mA)

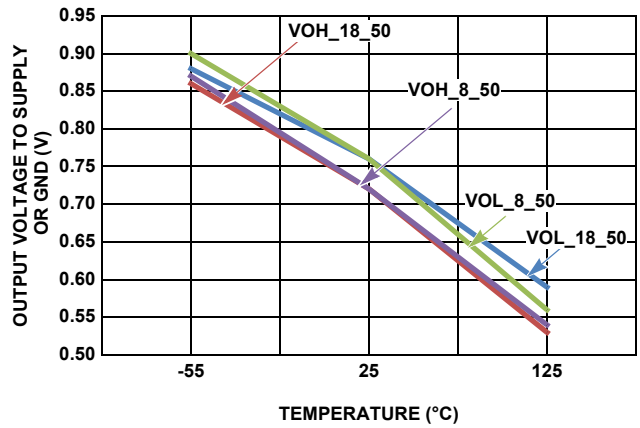


FIGURE 9. OUTPUT VOLTAGE vs TEMPERATURE (50mA)

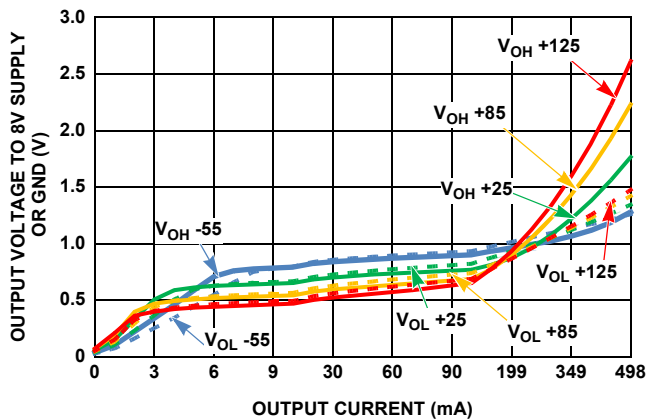


FIGURE 10. OUTPUT VOLTAGE vs OUTPUT CURRENT

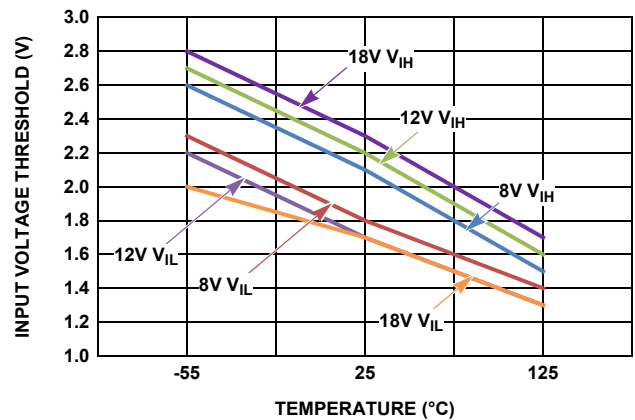


FIGURE 11. INPUT VOLTAGE THRESHOLD vs TEMPERATURE AND BIAS VOLTAGE



# Typical Performance Curves

Unless otherwise specified,  $V_S = 8V, 12V, 18V, C_L = 4300pF, T_A = +25^\circ C$ .

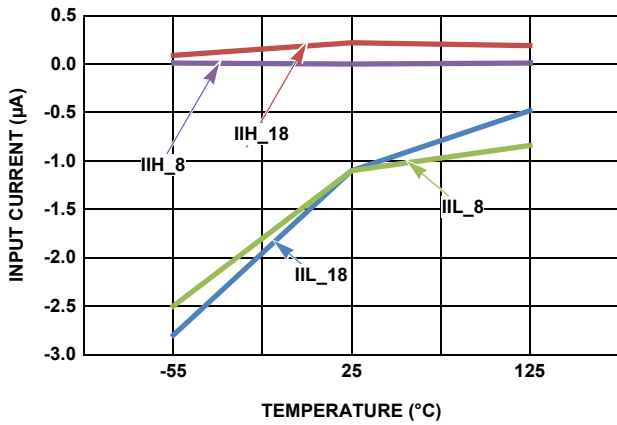


FIGURE 12. INPUT CURRENT vs TEMPERATURE AND BIAS VOLTAGE

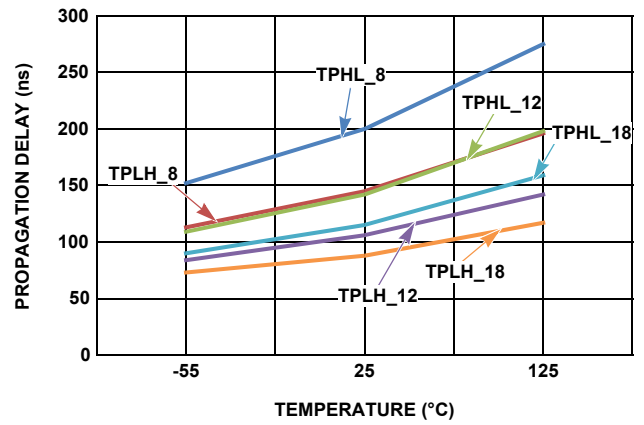


FIGURE 13. PROPAGATION DELAY vs TEMPERATURE

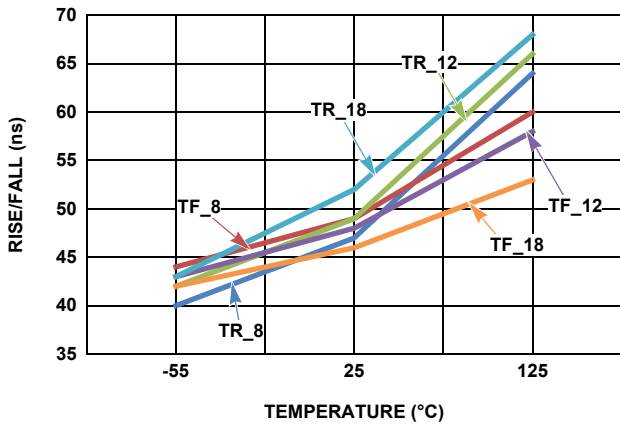


FIGURE 14. RISE/FALL TIME vs TEMPERATURE

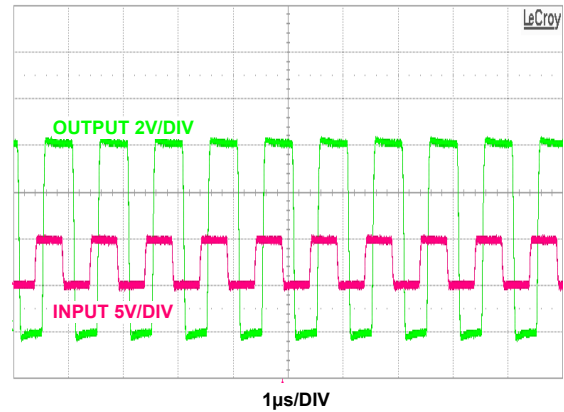


FIGURE 15. 1MHz AT 8V BIAS

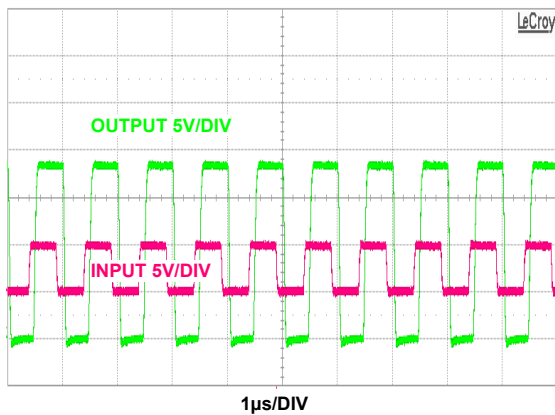


FIGURE 16. 1MHz AT 18V BIAS

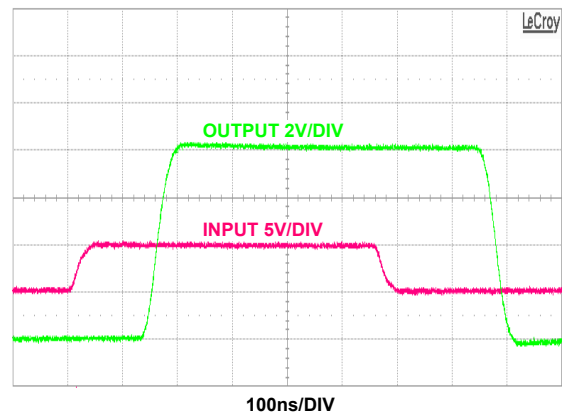


FIGURE 17. 8V RISING/FALLING PROPAGATION TIME

# Typical Performance Curves

Unless otherwise specified,  $V_S = 8V, 12V, 18V, C_L = 4300pF, T_A = +25^\circ C$ .

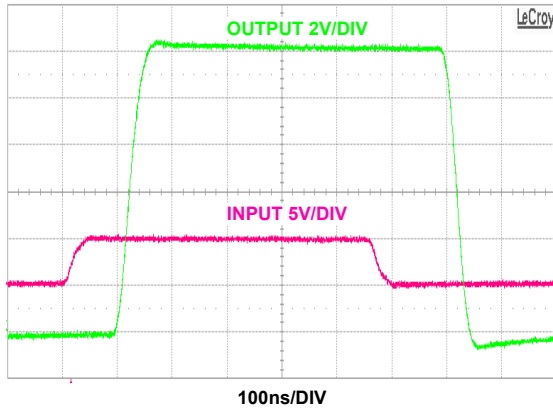


FIGURE 18. 12V RISING/FALLING PROPAGATION TIME

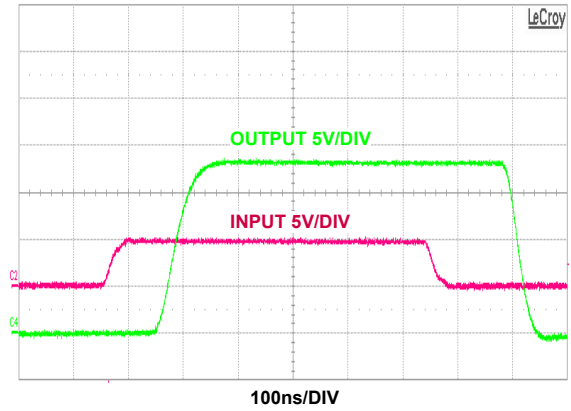


FIGURE 19. 18V RISING/FALLING PROPAGATION TIME

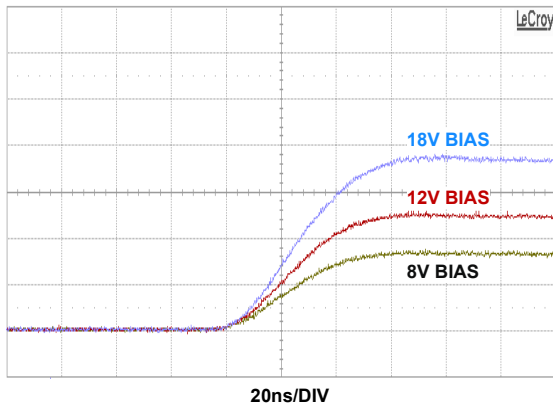


FIGURE 20. RISE TIME

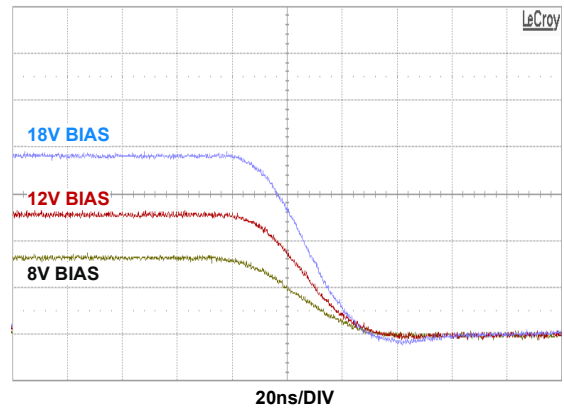


FIGURE 21. FALL TIME

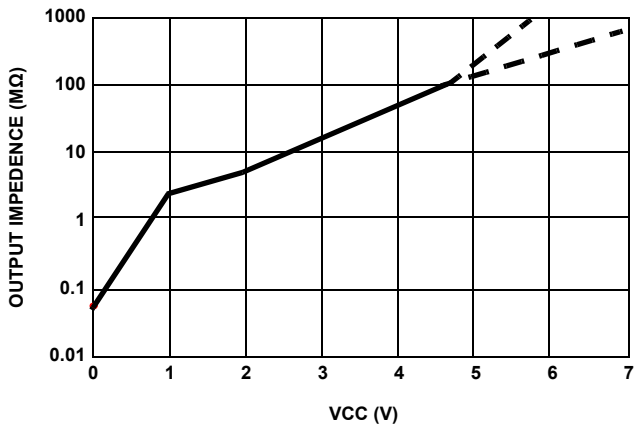


FIGURE 22. UVLO OUTPUT HIGH Z vs VCC

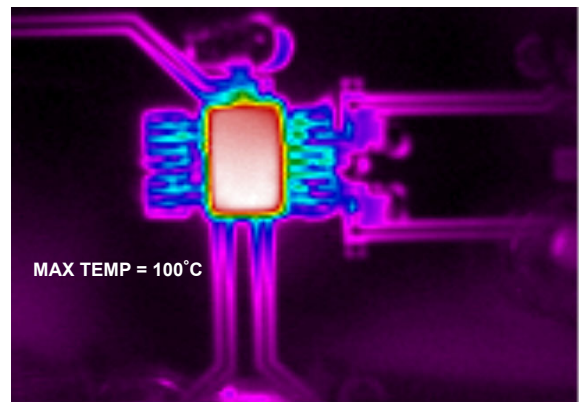


FIGURE 23. 18V, 1MHz OPERATING IR TEMP

## Post High, Low Dose Rate Radiation Characteristics

Unless otherwise specified,  $V_S = 1.2V$ ,  $T_A = +25^\circ C$ . This data is typical mean test data post 300kRAD (Si) radiation exposure at a high dose exposure rate of 50 to 300rad(Si)/s and post 50kRAD (Si) radiation exposure at a high dose exposure rate of <10mrad(Si)/s. This data is intended to show typical parameter shifts due to high dose rate radiation. These are not limits nor are they guaranteed.

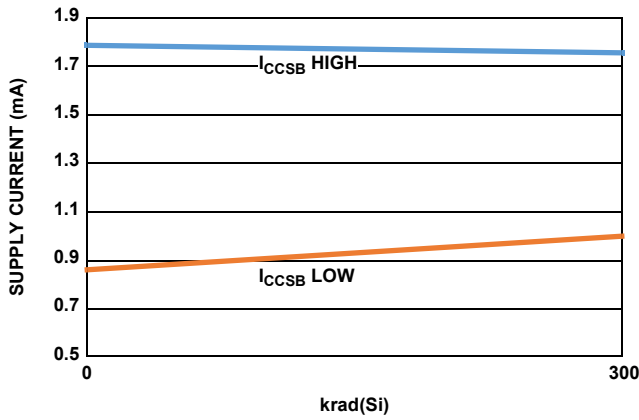


FIGURE 24. 18V SUPPLY CURRENT vs HDR RADIATION

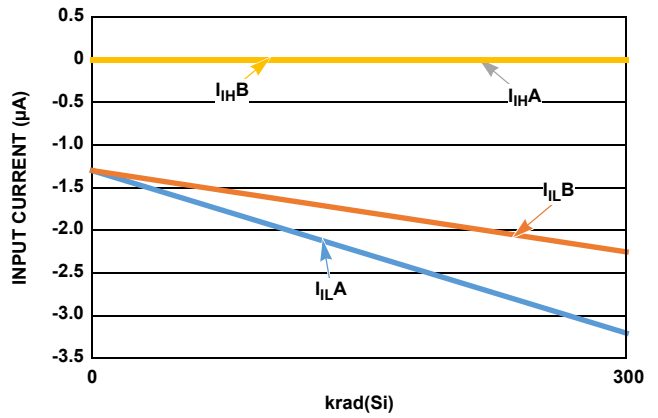


FIGURE 25. 18V INPUT CURRENT vs HDR RADIATION

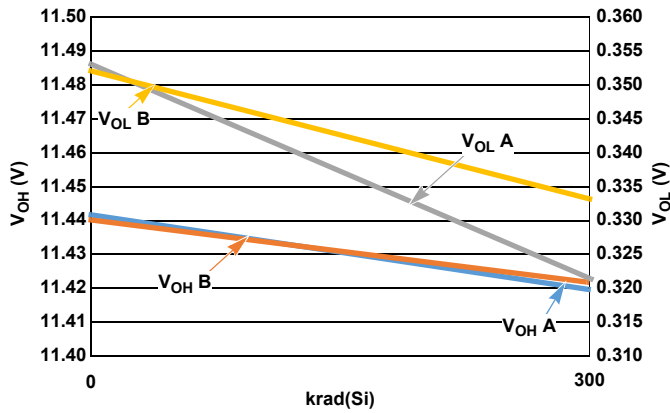


FIGURE 26. OUTPUT VOLTAGE vs HDR RADIATION

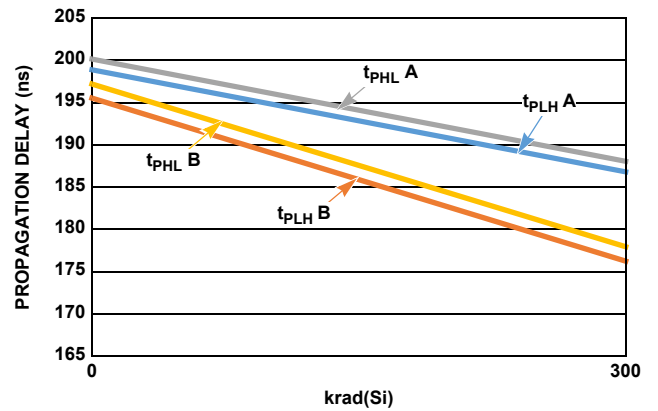


FIGURE 27. PROPAGATION DELAY vs HDR RADIATION

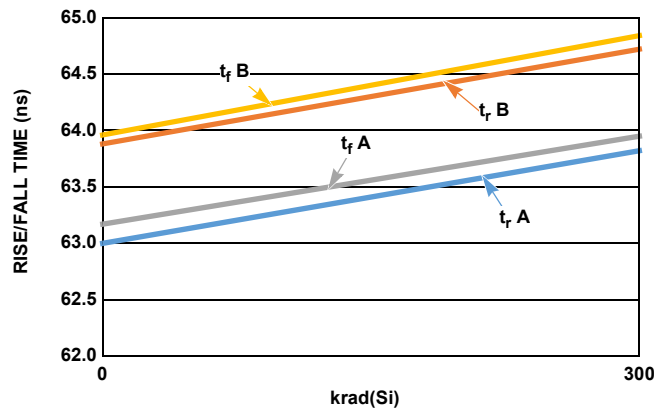


FIGURE 28. RISE/FALL TIME vs HDR RADIATION

## Post High, Low Dose Rate Radiation Characteristics

Unless otherwise specified,  $V_S = 12V$ ,  $T_A = +25^\circ C$ . This data is typical mean test data post 300kRAD (Si) radiation exposure at a high dose exposure rate of 50 to 300rad(Si)/s and post 50kRAD (Si) radiation exposure at a high dose exposure rate of <10mrad(Si)/s. This data is intended to show typical parameter shifts due to high dose rate radiation. These are not limits nor are they guaranteed. **(Continued)**

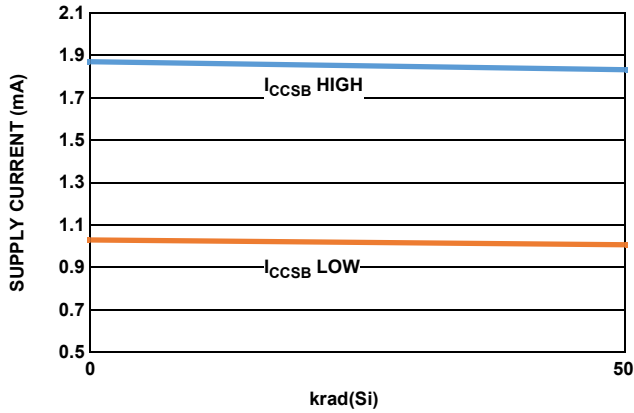


FIGURE 29. 18V SUPPLY CURRENT vs LDR RADIATION

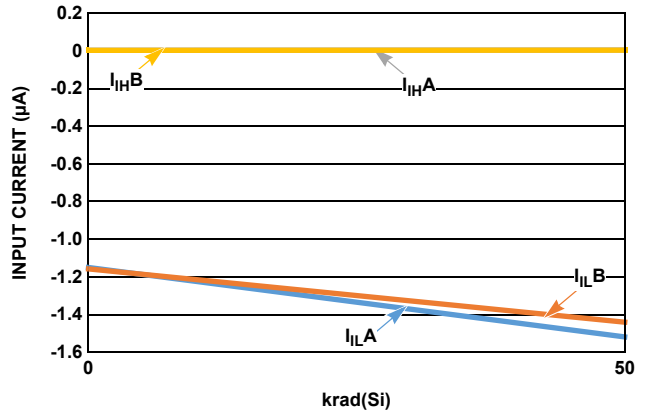


FIGURE 30. 18V INPUT CURRENT vs LDR RADIATION

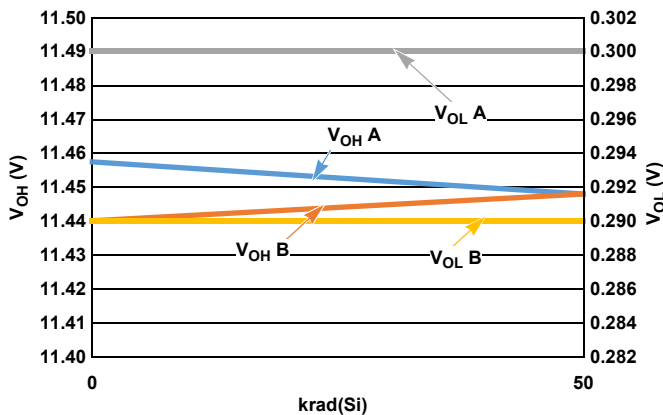


FIGURE 31. OUTPUT VOLTAGE vs LDR RADIATION

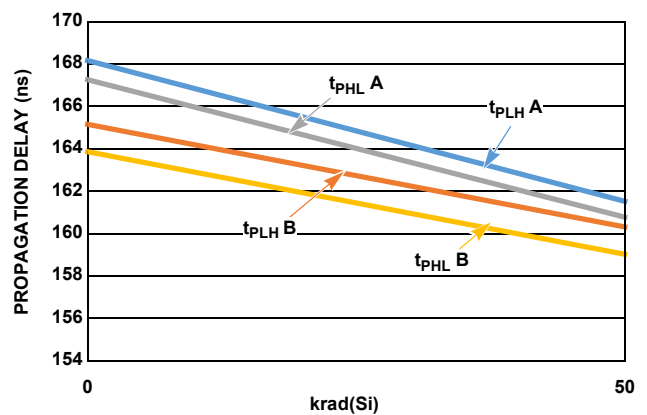


FIGURE 32. PROPAGATION DELAY vs LDR RADIATION

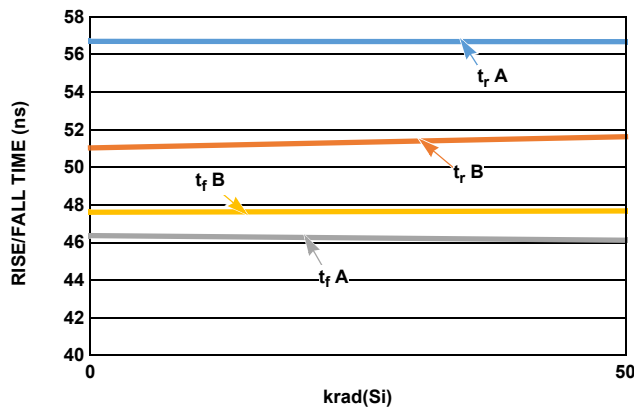


FIGURE 33. RISE/FALL TIME vs LDR RADIATION

## Applications Information

### Functional Description

The HS-4424DxH MOSFET drivers are designed for easy implementation with a PWM controller, such as the HS-1825ARH, as the input control signal driver. The HS-4424DxH consist of two independent drivers sharing bias voltage and ground connections at the die level.

### Undervoltage Lockout and Operating Voltage Range

The HS-4424DxH have a guaranteed UVLO of <8V across the operating temperature range. All devices are recommended to operate up to and are characterized and tested at a bias of 18V. The UVLO feature ensures that the internal MOSFET drivers have sufficient gate drive to operate in their saturated mode. When in a UVLO condition the HS-4424DxH outputs are put into a high impedance tri-stated mode.

Characterization and testing occurs (as appropriate) at 8V, 12V and 18V and across the -55°C to +125°C operating temperature range.

### Input Characteristics

The HS-4424DxH inputs are designed to be used with low voltage level signals (<1V for a low input level and >3V for a high input level) and also be capable of accepting input voltages up to the VCC level.

### Output Buffer

The HS-4424DxH output buffers are designed to drive >2A of peak output current into high capacitance loads and can be paralleled to increase the output current capability.

The output buffer uses a final drive stage comprised of a PNP lower and NPN upper complimentary pair of transistors for the high output current drive. To enhance the pull-up and pull-down of this bipolar pair, they are each paralleled with MOS devices to do so.

## Power Dissipation and Junction Temperature

It is possible to exceed the +150°C maximum recommended junction temperature under certain load and power supply conditions.

Calculate power dissipation using [Equation 1](#):

$$P_d = V \cdot I + 2 \cdot C \cdot V^2 \cdot f \quad (\text{EQ. 1})$$

Where

$P_d$  = Power dissipation

$V$  = Supply voltage

$I$  = Operating supply current

$C$  = Load capacitance

$f$  = Operating frequency

Calculate junction temperature  $T_J$  using [Equation 2](#):

$$T_J = P_d \cdot \Theta_{JC} + T_C \quad (\text{EQ. 2})$$

Where

$T_J$  = Junction temperature

$P_d$  = Power dissipation

$\Theta_{JC}$  = Junction-to-case thermal resistance

$T_C$  = Case temperature

## PCB Layout Guidelines

Use a ground plane in the PCB design, connect GND A and GND B pins directly to the ground plane in the same area, preferably close to the IC. Reference all input circuitry including IN A and IN B to a common node and reference all output circuitry including all OUT A and OUT B pins to a common node.

Bypass each VCC pin to the ground plane with a 0.047µF ceramic chip capacitor in parallel with a 4.7µF low ESR solid tantalum capacitor.

Clamp both OUT pins to VCC, each with a single diode. The 1n5819 (1A, 40V) Schottky diode is recommended.

## Die Characteristics

### Die Dimensions

4890 $\mu$ m x 3370 $\mu$ m (193mils x 133mils)  
Thickness: 483 $\mu$ m  $\pm$ 25.4 $\mu$ m (19mils  $\pm$ 1mil)

### Interface Materials

#### GLASSIVATION

Type: PSG (Phosphorous Silicon Glass)  
Thickness: 8.0k $\text{Å}$   $\pm$ 1.0k $\text{Å}$

#### TOP METALLIZATION

Type: AlSiCu  
Thickness: 16.0k $\text{Å}$   $\pm$ 2k $\text{Å}$

#### BACKSIDE FINISH

Silicon

#### PROCESS

Radiation Hardened Silicon Gate (DI)

## Assembly Related Information

### SUBSTRATE POTENTIAL

Floating (DI)

### LID POTENTIAL

Floating

### Additional Information

#### WORST CASE CURRENT DENSITY

$< 2 \times 10^5$  A/cm<sup>2</sup>

#### TRANSISTOR COUNT

125

### Weight of Packaged Device

0.591 grams (typical)

### Lid Characteristics

Finish: Gold

Case isolation to any lead:  $20 \times 10^9\Omega$  (minimum)

## Metallization Mask Layout

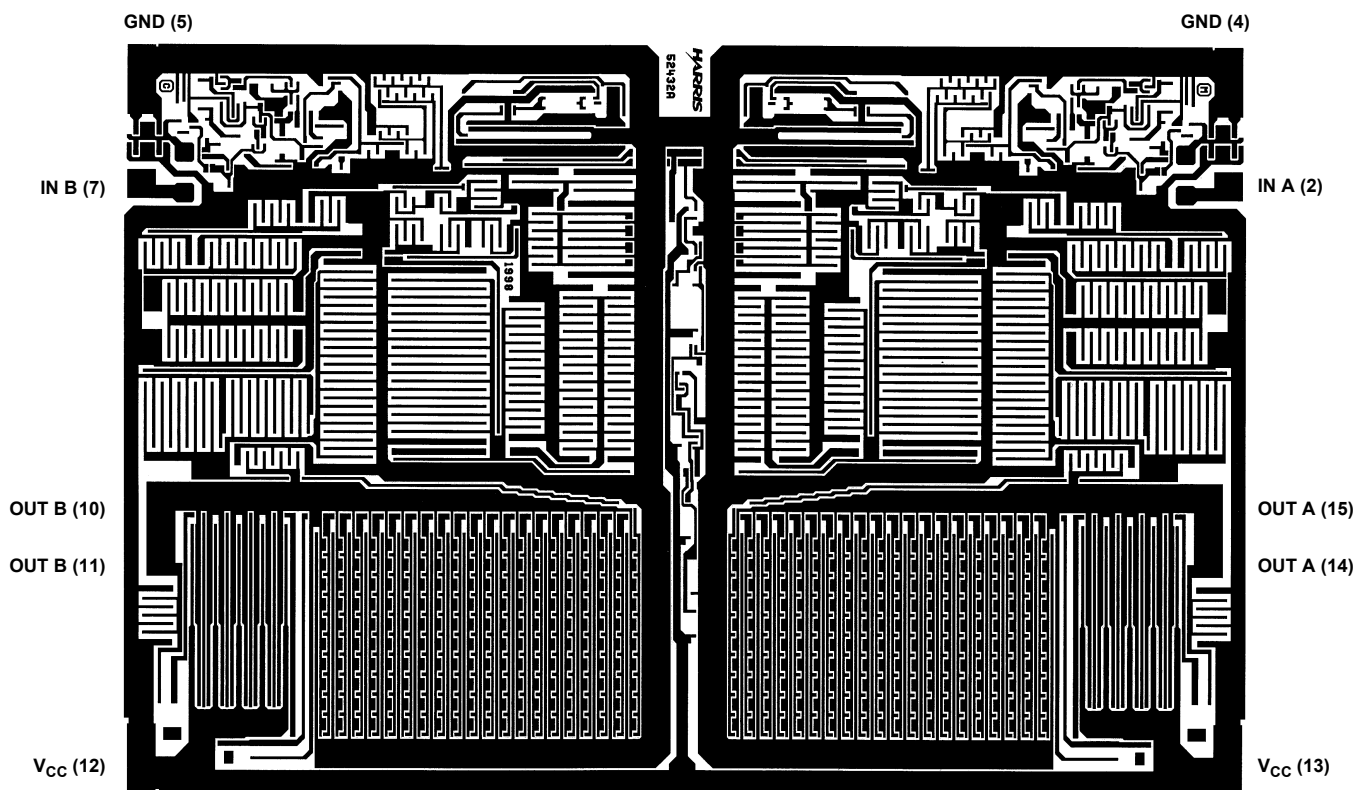


TABLE 2. DIE BOND PAD LAYOUT PAD OPENING SIZE AND X-Y COORDINATES FOR PAD CENTER

PAD NUMBER	PAD NAME	X DIMENSION (μm)	Y DIMENSION (μm)	X COORDINATE (μm)	Y COORDINATE (μm)
2	IN A	110	110	0	-434.5
4	GND	110	110	0	0
5	GND	110	110	-4529	0
7	IN B	110	110	-4529	-434.5
10	OUT B	110	110	-4447	-1772.5
11	OUT B	110	110	-4447	-2003.5
12	Vcc	110	110	-4529	-2823.5
13	Vcc	110	110	0	.2823.5
14	OUT A	110	110	-82	-2003.5
15	OUT A	110	110	-82	-1772.5

NOTE: Origin of coordinates is the center of the PAD 4

## Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to the web to make sure that you have the latest revision.

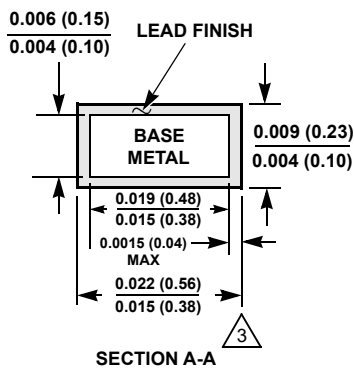
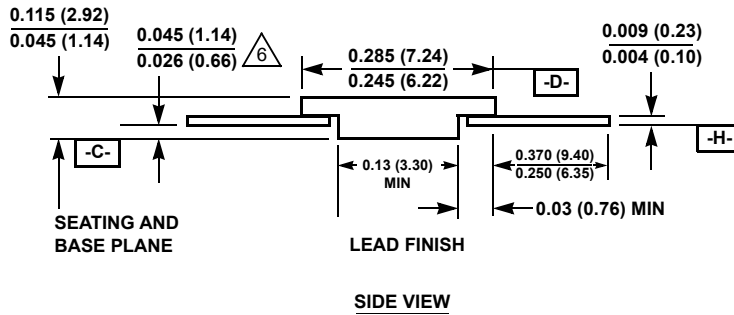
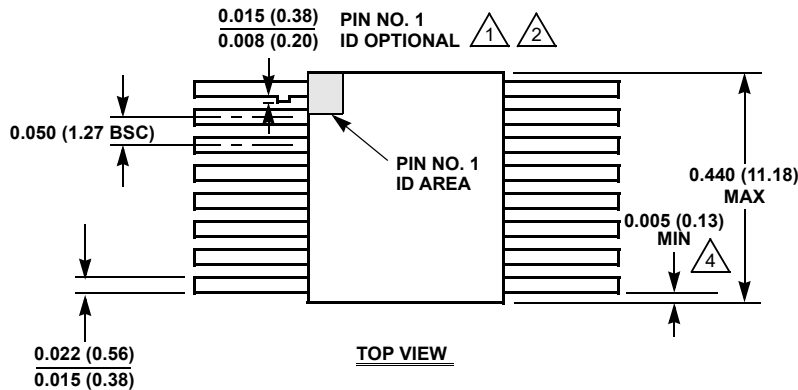
DATE	REVISION	CHANGE
Jan 12, 2021	3.00	Added Related Literature section. Updated Radiation acceptance testing feature bullets. Updated ordering information table by adding Rad hard information and Notes 3 and 4. Added Table 2. Removed About Intersil section
Oct 15, 2015	2.00	Added part number HS-4424DEH throughout datasheet.
Jul 1, 2015	1.00	Abs Max ratings on page 5 - removed abs max input current and related text on page 13. ESD Ratings - changed Machine Model from: 1kV to: 200V and Charged Device Model from: 4kV to: 750V Changed over temp limits for UVLO Rising from: MIN/MAX 7.0/7.9 to: 6.9/7.95 and Falling MIN/MAX from: 6.9/7.85 to: 6.8/7.9. Changed over temp 8V, 5mA VOH limit MIN from $V_S - 0.75$ to $V_S - 0.9$ .
Jun 8, 2015	0.00	Initial Release



# Package Outline Drawing

For the most recent package outline drawing, see [K14.A](#).

K16.A  
 16 LEAD CERAMIC METAL SEAL FLATPACK PACKAGE  
 Rev 2, 1/10



**NOTES:**

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark. Alternately, a tab may be used to identify pin one.
2. If a pin one identification mark is used in addition to a tab, the limits of the tab dimension do not apply.
3. The maximum limits of lead dimensions (section A-A) shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
4. Measure dimension at all four corners.
5. For bottom-brazed lead packages, no organic or polymeric materials shall be molded to the bottom of the package to cover the leads.
6. Dimension shall be measured at the point of exit (beyond the meniscus) of the lead from the body. Dimension minimum shall be reduced by 0.0015 inch (0.038mm) maximum when solder dip lead finish is applied.
7. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
8. Controlling dimension: INCH.

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(Rev.1.0 Mar 2020)

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