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Errata Notification

EN #: **FEN-01-02** Errata Revision #: 0
 Issue Date: August 29, 2001 Effective Date: August 29, 2001
 Product Affected: 72V01/02/03/04/05/06, 15ns speed grade.

ERRATA DETAILS: **ATTACHMENT** Yes No

Data Sheet Errata
 Device Manual Errata
 Application Notes Errata
 Other (Please Specify)

Datasheet update to reflect correct AC ELECTRICAL CHARACTERISTICS for the 15ns option.

Devices affected:

72V01L15J, 72V02L15J, 72V03L15J, 72V04L15J, 72V05L15J, 72V06L15J

IDT Web Site Location: http://www.idt.com/products/pages/FIFOs_DS_t.html

CUSTOMER NOTIFICATION:

As a result of Errata listed above, IDT has decided to notify you through this Errata Notification. We recommend you to review this notification in details prior to the use of affected product in your application. Please use acknowledgement below or E-Mail to request additional information.

If you have any questions, please feel free to contact your local IDT distributor or sales representative.

Customer: _____	E-Mail Address: _____
Name/Date: _____	Phone #: _____
Title: _____	Fax #: _____

CUSTOMER COMMENTS: _____

AC ELECTRICAL CHARACTERISTICS

(Commercial: VCC = 3.3V ± 0.3V, TA = 0°C to +70°C)

Symbol	Parameter	New Datasheet Spec		Previous Data Sheet Spec		Unit
		IDT72V01L15 IDT72V02L15 IDT72V03L15 IDT72V04L15 IDT72V05L15 IDT72V06L15		IDT72V01L15 IDT72V02L15 IDT72V03L15 IDT72V04L15 IDT72V05L15 IDT72V06L15		
		Min.	Max.	Min.	Max.	
fs	Shift Frequency	—	40	—	50	MHz
tRC	Read Cycle Time	25	—	20	—	ns
tA	Access Time	—	15	—	12	ns
tRR	Read Recovery Time	10	—	8	—	ns
tRPW	Read Pulse Width ⁽³⁾	15	—	12	—	ns
tRLZ	Read Pulse Low to Data Bus at Low Z ⁽⁴⁾	3	—	3	—	ns
tWLZ	Write Pulse High to Data Bus at Low Z ^(4,5)	5	—	5	—	ns
tDV	Data Valid from Read Pulse High	5	—	5	—	ns
tRHZ	Read Pulse High to Data Bus at High Z ⁽⁴⁾	—	15	—	12	ns
tWC	Write Cycle Time	25	—	20	—	ns
tWPW	Write Pulse Width ⁽³⁾	15	—	12	—	ns
tWR	Write Recovery Time	10	—	8	—	ns
tDS	Data Setup Time	11	—	9	—	ns
tDH	Data Hold Time	0	—	0	—	ns
tRSC	Reset Cycle Time	25	—	20	—	ns
tRS	Reset Pulse Width ⁽³⁾	15	—	12	—	ns
tRSS	Reset Setup Time ⁽⁴⁾	15	—	12	—	ns
tRSR	Reset Recovery Time	10	—	8	—	ns
tRTC	Retransmit Cycle Time	25	—	20	—	ns
tRT	Retransmit Pulse Width ⁽³⁾	15	—	12	—	ns
tRTS	Retransmit Setup Time ⁽⁴⁾	15	—	12	—	ns
tRTR	Retransmit Recovery Time	10	—	8	—	ns
tEFL	Reset to Empty Flag Low	—	25	—	12	ns
tHFH,FFH	Reset to Half-Full and Full Flag High	—	25	—	17	ns
tRTF	Retransmit Low to Flags Valid	—	25	—	20	ns
tREF	Read Low to Empty Flag Low	—	15	—	12	ns
tRFF	Read High to Full Flag High	—	15	—	14	ns
tRPE	Read Pulse Width after EF High	15	—	12	—	ns
tWEF	Write High to Empty Flag High	—	15	—	12	ns
tWFF	Write Low to Full Flag Low	—	15	—	14	ns
tWHF	Write Low to Half-Full Flag Low	—	25	—	17	ns
tRHF	Read High to Half-Full Flag High	—	25	—	17	ns
tWPF	Write Pulse Width after FF High	15	—	12	—	ns
tXOL	Read/Write to xOLow	—	15	—	12	ns
tXOH	Read/Write to xOHigh	—	15	—	12	ns
tXI	XI Pulse Width ⁽³⁾	15	—	12	—	ns
tXIR	XI Recovery Time	10	—	8	—	ns
tXIS	XI Setup Time	10	—	8	—	ns