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H8SX Family

Write Data Buffer for Peripheral Modules

Introduction

Using the write data buffer function enables the parallel execution of writing to a peripheral module and on-chip memory or external access.

This application note describes an example of operation using the write data buffer function for peripheral modules.

Target Device

H8SX/1663 Group

Preface

Although the writing of this application note is in accord with the hardware manual for the H8SX/1663 Group, the program it covers can also be run on other H8SX-Family devices which have internal I/O registers equivalent to those of the target devices indicated above. However, since some functional modules may be changed with the addition of functionality etc., be sure to perform thorough evaluation by confirming the details with the hardware manual for the target device.

Contents

1. Specifications

This sample program employs the write data buffer function for peripheral modules to execute writing to a peripheral module in parallel with reading from on-chip memory and then writing to an external memory-area. Writing to I/O port registers is performed in a peripheral-module write cycle, reading from on-chip RAM is performed as on-chip memory reading, and then writing to external SRAM is performed as writing to an external area.

In the sample application, writing to external SRAM involves access to an SRAM with byte control (byte-control SRAM) connected to area 2 of the external address space. Figure 1 shows an example of connection of the SRAM.

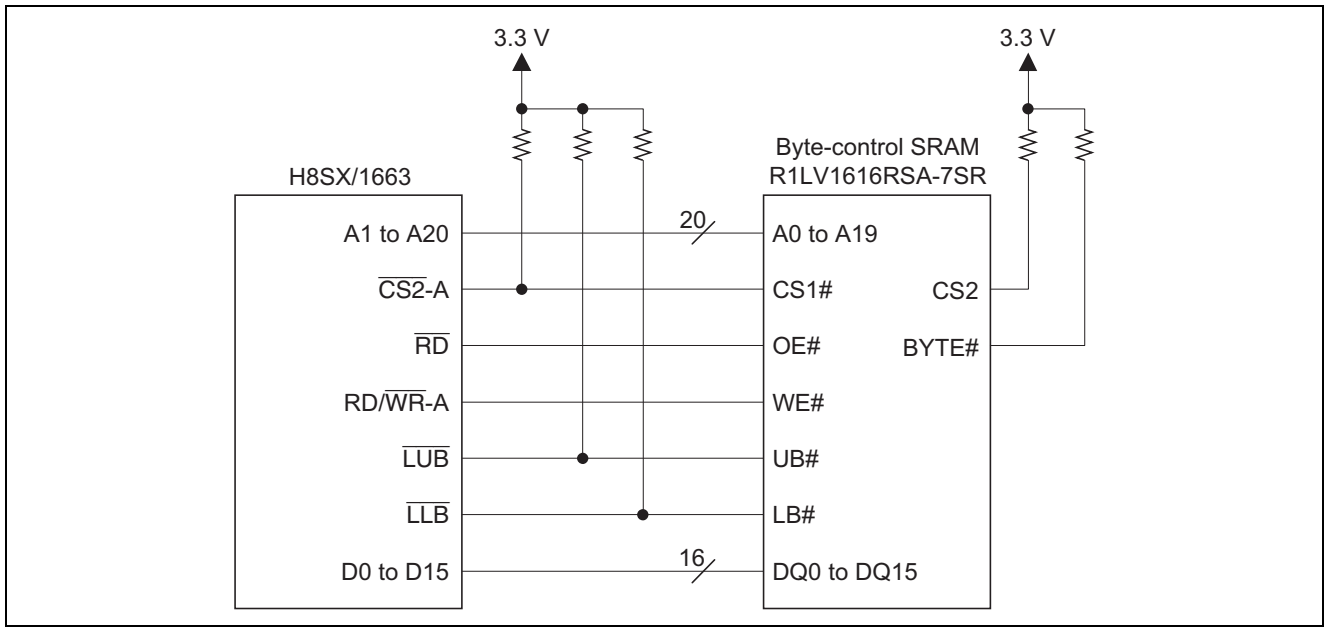


Figure 1 Example of Connection of an SRAM with Byte Control

2. Applicable Conditions

Table 1 Applicable Conditions

Item	Description	
Operating frequency	Input clock	: 16 MHz
	System clock (Iϕ)	: 32 MHz (input clock frequency × 2)
	Peripheral module clock (Pϕ)	: 16 MHz (input clock frequency × 1)
	External bus clock (Bϕ)	: 16 MHz (input clock frequency × 1)
Operating mode	Mode 6 (expansion mode with on-chip ROM enabled) Setting of mode pins: MD2 = 1, MD1 = 1, MD0 = 0, MD_CLK = 0	
Development tool	High-performance Embedded Workshop Ver.4.04.01	
C/C++ compiler	H8S, H8/300 SERIES C/C++ Compiler Ver.6.02.00 (from Renesas Technology Corp.)	
	Option settings -cpu=h8sxa:24:md, -code=machinecode, -optimize=1, -regparam=3, -speed=(register,shift,struct,expression)	
Optimizing linkage editor	Optimizing Linkage Editor Ver.9.03.00 (from Renesas Technology Corp.)	
	Option setting -start=P/01000, BCS2/0400000, B/0FF2000	

Table 2 Specifications of Byte-Control SRAM

Item	Description
Product name	R1LV1616RSD-7SR (from Renesas Technology Corp.)
Configuration	1 M × 16-bit words
Capacity	16 Mbits

3. Description of Module Used

3.1 Write Data Buffer Function for Peripheral Modules

The H8SX/1663 MCU has a write data buffer function for peripheral modules. This function enables the parallel execution of writing to peripheral modules and on-chip memory or external access. The write data buffer function for peripheral modules is enabled by setting the PWDBE bit in BCR2 to 1 and is available for use with the peripheral modules indicated below.

- Registers (other than PFCRs) for I/O ports
- 16-bit timer pulse unit (TPU)
- Programmable pulse generator (PPG)
- 8-bit timers (TMR)
- Serial communications interface (SCI)
- USB function module (USB)
- A/D converter
- D/A converter

4. Principles of Operation

This section describes the timing of operations with and without use of the write data buffer function for peripheral modules.

1. Timing when the write data buffer function for peripheral modules is not in use
   Figure 2 shows an example of the timing of operations when the write data buffer function for peripheral modules is not in use. When the PWDBE bit in BCR2 is set to 0, the write data buffer function for peripheral modules is disabled. In this case, reading from on-chip RAM and writing to external SRAM are executed at the end of the cycle of writing to the internal I/O registers

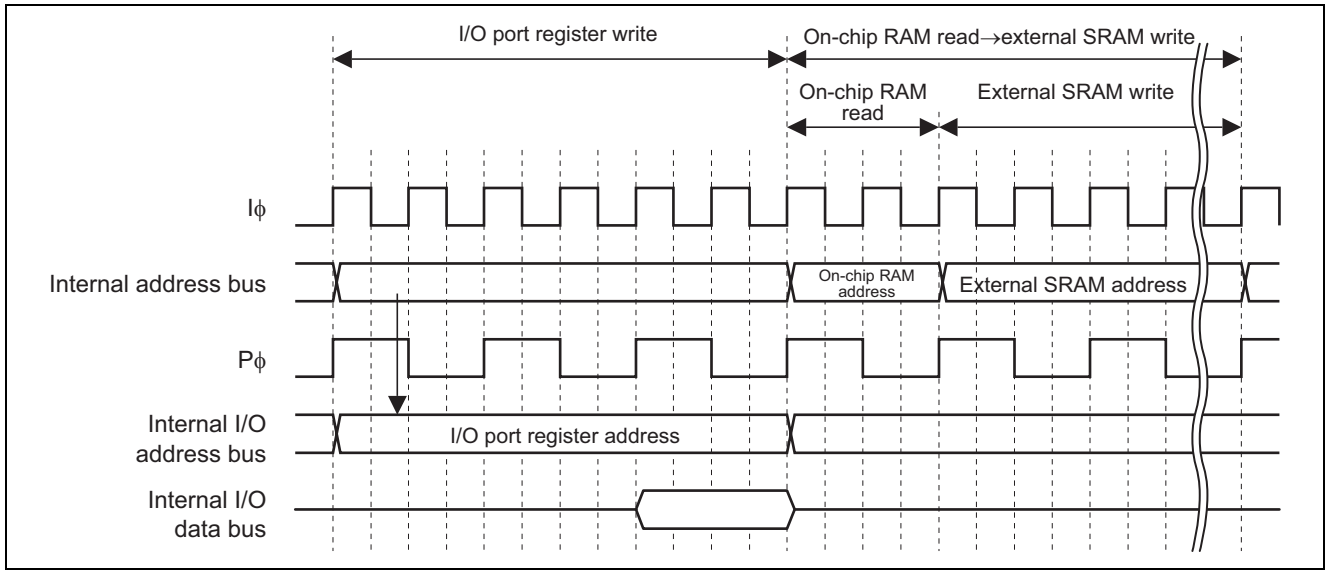


Figure 2 Example of Timing of Operations with the Write Data Buffer Function for Peripheral Modules not in Use (PWDBE = 0)

2. Timing when the write data buffer function for peripheral modules is in use
   Figure 3 shows an example of the timing of operations when the write data buffer function for peripheral modules is in use. When the PWDBE bit in BCR2 is set to 1, the write data buffer function for peripheral modules is enabled. In this case, writing to the I/O port register is the only operation being executed over the first two clock cycles, but reading from on-chip RAM and then writing to external SRAM are executed in parallel with this from the next clock cycle.

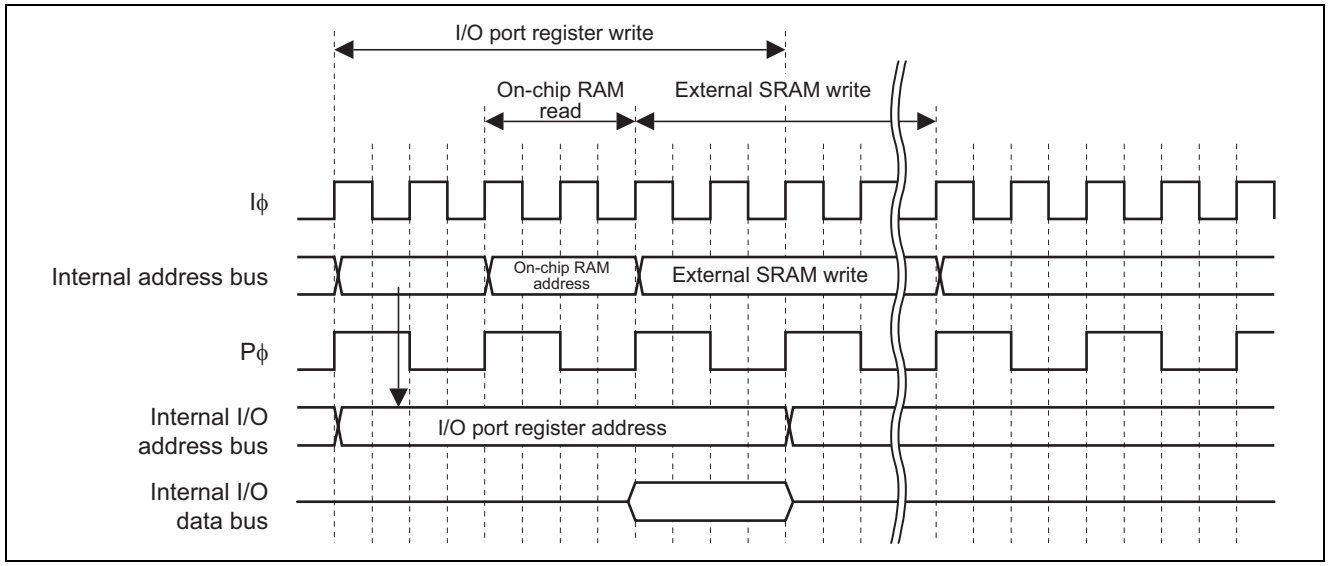


Figure 3 Example of Timing of Operations with the Write Data Buffer Function for Peripheral Modules in Use (PWDBE = 1)

5. Description of Software

5.1 Vector Table

Table 3 Vector Table for Interrupt Exception Handling

Exception Handling Source	Vector Number	Address in Vector Table	Destination Interrupt Processing Function
Reset	0	H'000000	init

5.2 List of Functions

Table 4 List of Functions in File main.c

Function Name	Description
init	Initialization routine Releases the module from the module stop mode, configures the clocks and calls the main function.
main	Main routine Calls the BscInit function and makes the setting for the write data buffer function for peripheral modules.
BscInit	Area 2 (byte-control SRAM area) initialization Sets a byte-control SRAM interface for area 2.

5.3 RAM Usage

Table 5 RAM Usage

Type	Name of Variable	Description	Used in Function
unsigned char	area2	User variable (byte-control SRAM area)	main
unsigned char	buf	User variable (on-chip RAM area)	main

5.4 Macro Definition

Table 6 Macro Definition

Identifier	Description	Used in Function
PGM_SELECT	Selection of program execution state PGM_SELECT = 0: The PWDBE bit in BCR2 is set to 0. PGM_SELECT = 1: The PWDBE bit in BCR2 is set to 1.	main

5.5 Description of Functions

5.5.1 Function init

1. Functional overview
   Initialization routine releases the module from module stop mode, configures the clocks, and calls the main function.
2. Arguments
   None
3. Return value
   None
4. Description of internal register usage
   Usage of internal registers in this function of the sample task is described below. Note that the settings shown below are not the initial values but the values used in this sample task.

- Mode control register (MDCR) Number of bits: 16 Address: H'FFFDC0

Bit	Bit Name	Setting	R/W	Description
15	MDS7	Undefined*	R	Indicates the value set by a mode pin (MD3). When MDCR is read, the input level on the MD3 pin is latched. This latching is released by a reset.
11	MDS3	Undefined*	R	Mode Select 3 to 0
10	MDS2	Undefined*	R	These bits indicate the operating mode selected by mode pins (MD2 to MD0; see table 7). When MDCR is read, the signal levels input on pins MD2 to MD0 are latched into these bits. The latches are released by a reset.
9	MDS1	Undefined*	R	
8	MDS0	Undefined*	R	

Note: * Determined by the settings on pins MD3 to MD0.

Table 7 Values of Bits MDS3 to MDS0

MCU Operating Mode	Pins			MDCR			
	MD2	MD1	MD0	MDS3	MDS2	MDS1	MDS0
2	0	1	0	1	1	0	0
4	1	0	0	0	0	1	0
5	1	0	1	0	0	0	1
6	1	1	0	0	1	0	1
7	1	1	1	0	1	0	0

- System clock control register (SCKCR) Number of bits: 16 Address: H'FFFDC4

Bit	Bit Name	Setting	R/W	Description
10	ICK2	0	R/W	System Clock (Iϕ) Select
9	ICK1	0	R/W	These bits select the frequency of the system clock
8	ICK0	1	R/W	provided to the CPU, DMAC, and DTC. 001: Input clock × 2
6	PCK2	0	R/W	Peripheral Module Clock (Pϕ) Select
5	PCK1	1	R/W	These bits select the frequency of the peripheral module
4	PCK0	0	R/W	clock. 010: Input clock × 1
2	BCK2	0	R/W	External Bus Clock (Bϕ) Select
1	BCK1	1	R/W	These bits select the frequency of the external bus clock.
0	BCK0	0	R/W	010: Input clock × 1

- MSTPCRA, MSTPCRB and MSTPCRC control the module stop mode. Setting a bit to 1 makes the corresponding module enter the module stop state, while clearing the bit to 0 releases the module from module stop mode.

- Module stop control register A (MSTPCRA) Number of bits: 16 Address: H'FFFDC8

Bit	Bit Name	Setting	R/W	Description
15	ACSE	0	R/W	All-Module-Clock-Stop Mode Enable This bit enables/disables all-module-clock-stop mode for reducing current drawn by stopping operation of the bus controller and I/O ports when the CPU executes the SLEEP instruction after the module stop state has been set for all of the on-chip peripheral modules controlled by MSTPCR. 0: All-module-clock-stop mode disabled 1: All-module-clock-stop mode enabled
13	MSTPA13	1	R/W	DMA controller (DMAC)
12	MSTPA12	1	R/W	Data transfer controller (DTC)
9	MSTPA9	1	R/W	8-bit timer unit (TMR_3 and TMR_2)
8	MSTPA8	1	R/W	8-bit timer unit (TMR_1 and TMR_0)
5	MSTPA5	1	R/W	D/A converter (channels 1 and 0)
3	MSTPA3	1	R/W	A/D converter (unit 0)
0	MSTPA0	1	R/W	16-bit timer pulse unit (TPU channels 5 to 0)

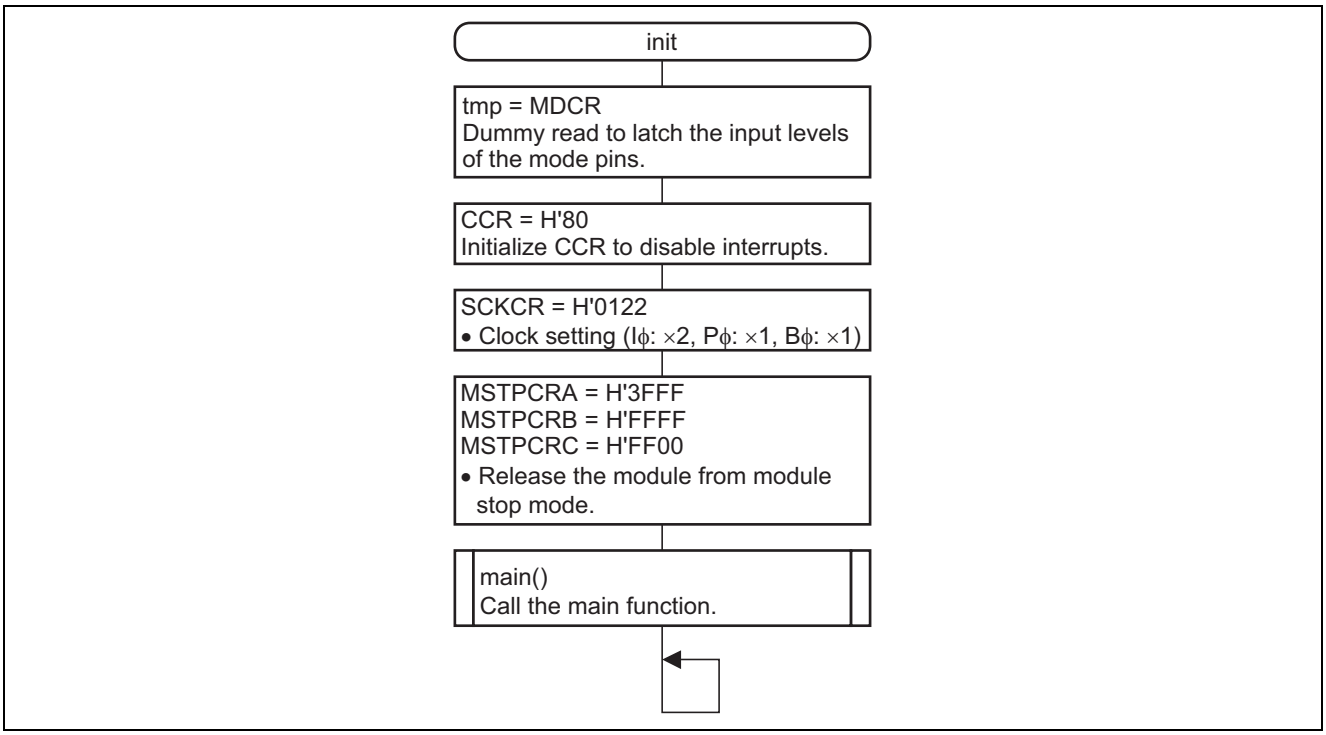
- Module stop control register B (MSTPCRB) Number of bits: 16 Address: H'FFFDCA

Bit	Bit Name	Setting	R/W	Description
15	MSTPB15	1	R/W	Programmable pulse generator (PPG)
12	MSTPB12	1	R/W	Serial communications interface_4 (SCI_4)
10	MSTPB10	1	R/W	Serial communications interface_2 (SCI_2)
9	MSTPB9	1	R/W	Serial communications interface_1 (SCI_1)
8	MSTPB8	1	R/W	Serial communications interface_0 (SCI_0)
7	MSTPB7	1	R/W	I^2C bus Interface_1 (IIC_1)
6	MSTPB6	1	R/W	I^2C bus Interface_0 (IIC_0)

- Module stop control register C (MSTPCRC) Number of bits: 16 Address: H'FFFDCC

Bit	Bit Name	Setting	R/W	Description
15	MSTPC15	1	R/W	Serial communications interface_5 (SCI_5), (IrDA)
14	MSTPC14	1	R/W	Serial communications interface_6 (SCI_6)
13	MSTPC13	1	R/W	8-bit timer unit (TMR_4, TMR_5)
12	MSTPC12	1	R/W	8-bit timer unit (TMR_6, TMR_7)
11	MSTPC11	1	R/W	Universal serial bus interface (USB)
10	MSTPC10	1	R/W	Cyclic redundancy check
4	MSTPC4	0	R/W	On-chip RAM_4 (H'FF2000 to H'FF3FFF)
3	MSTPC3	0	R/W	On-chip RAM_3 (H'FF4000 to H'FF5FFF)
2	MSTPC2	0	R/W	On-chip RAM_2 (H'FF6000 to H'FF7FFF)
1	MSTPC1	0	R/W	On-chip RAM_1 (H'FF8000 to H'FF9FFF)
0	MSTPC0	0	R/W	On-chip RAM_0 (H'FFA000 to H'FFBFFF)

5. Flowchart


init
tmp = MDCR
Dummy read to latch the input levels of the mode pins.
CCR = H'80
Initialize CCR to disable interrupts.
SCKCR = H'0122
• Clock setting (Iϕ: ×2, Pϕ: ×1, Bϕ: ×1)
MSTPCRA = H'3FFF
MSTPCRB = H'FFFF
MSTPCRC = H'FF00
• Release the module from module stop mode.
main()
Call the main function.

5.5.2 Function main

1. Functional overview
   Main routine calls function BscInit and makes the setting for the write data buffer for peripheral modules.
2. Arguments
   None
3. Return value
   None
4. Description of internal register usage
   Usage of internal registers in this function of the sample task is described below. Note that the settings shown below are not the initial values but the values used in this sample task.

- Port M data direction register (PMDDR) Number of bits: 8 Address: H'FFEE50
  Function: Sets pin PM4 as an output pin.
  Setting: H'10

- Port M data register (PMDR) Number of bits: 8 Address: H'FFEE51

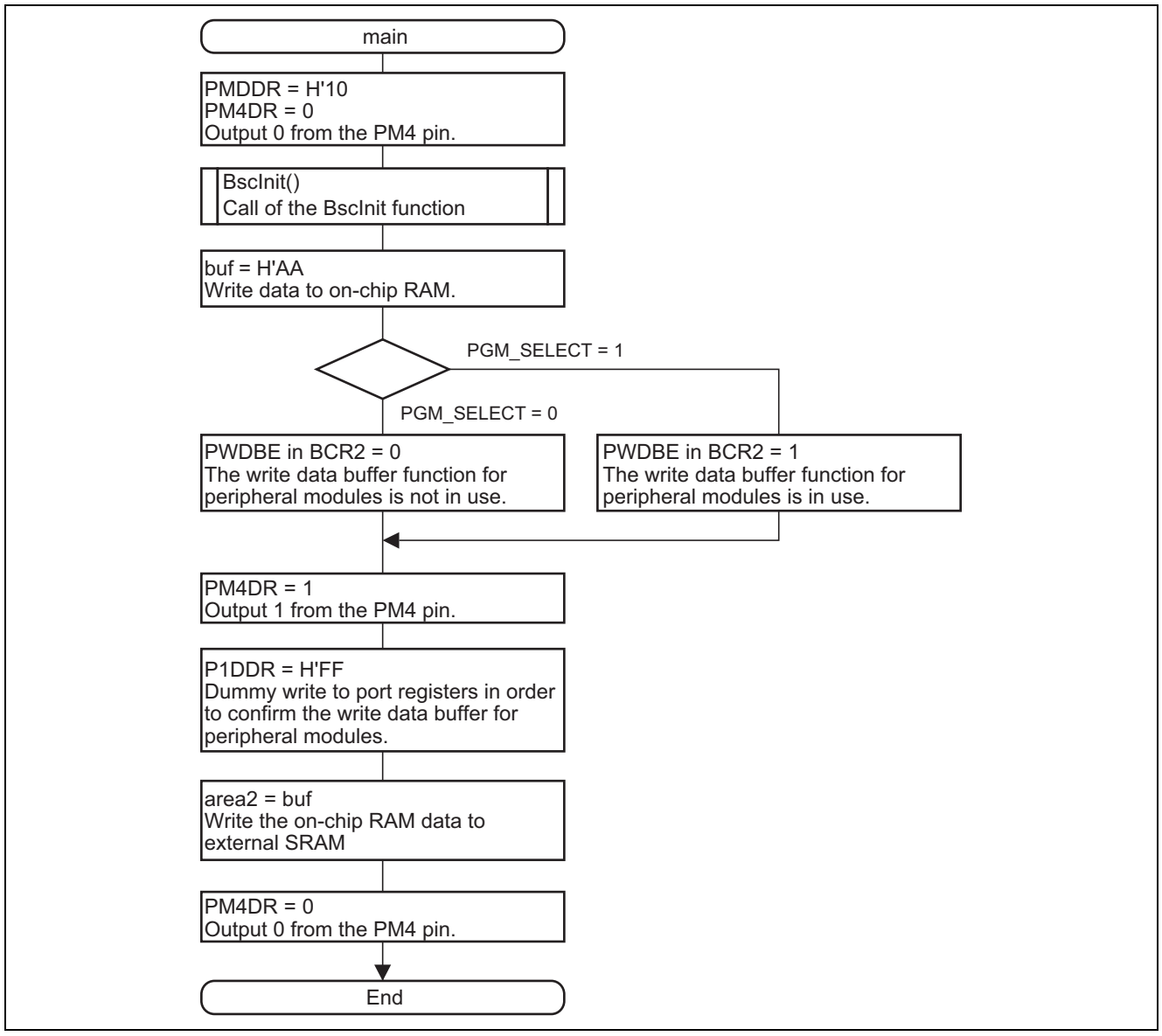
Bit	Bit Name	Setting	R/W	Description
4	PM4DR	0/1	R/W	0: The value 0 (low level) is output on pin PM4. 1: The value 1 (high level) is output on pin PM4.

- Port 1 data direction register (P1DDR) Number of bits: 8 Address: H'FFFB80
  Function: Sets pin P17 to P10 as an output pin.
  Setting: H'FF

- Bus control register 2 (BCR2) Number of bits: 16 Address: H'FFFD94

Bit	Bit Name	Setting	R/W	Description
0	PWDBE	0/1	R/W	Peripheral Module Write Data Buffer Enable Specifies whether or not the write data buffer function is used in cycles of writing to peripheral modules. 0: This setting corresponds to PGM_SELECT = 0. The write data buffer function is not in use. 1: This setting corresponds to PGM_SELECT = 1. The write data buffer function is in use.

5. Flowchart


main
PMDDR = H'10
PM4DR = 0
Output 0 from the PM4 pin.
BscInit()
Call of the BscInit function
buf = H'AA
Write data to on-chip RAM.
PGM_SELECT = 1
PGM_SELECT = 0
PWDBE in BCR2 = 0
The write data buffer function for peripheral modules is not in use.
PWDBE in BCR2 = 1
The write data buffer function for peripheral modules is in use.
PM4DR = 1
Output 1 from the PM4 pin.
P1DDR = H'FF
Dummy write to port registers in order to confirm the write data buffer for peripheral modules.
area2 = buf
Write the on-chip RAM data to external SRAM
PM4DR = 0
Output 0 from the PM4 pin.
End

5.5.3 Function BscInit

1. Functional overview
   The Bsclnit function initializes area 2 (byte-control SRAM area) and sets a byte-control SRAM interface for area 2.
2. Arguments
   None
3. Return value
   None
4. Description of internal register usage
   Usage of internal registers in this sample task is described below. Note that the settings shown below are not the initial values but the values used in this sample task.

- Port D data direction register (PDDDR) Number of bits: 8 Address: H'FFFB8C
  Function: Sets pins PD7 to PD1 as output pins for address output.
  Value: H'FF

- Port E data direction register (PEDDR) Number of bits: 8 Address: H'FFFB8D
  Function: Sets pins PE7 to PE0 as output pins for address output.
  Value: H'FF

- Port F data direction register (PFDDR) Number of bits: 8 Address: H'FFFB8E
  Function: Sets pins PF4 to PF0 as output pins for address output.
  Value: H'1F

- Port function control register 0 (PFCR0) Number of bits: 8 Address: H'FFFBC0

Bit	Bit Name	Setting	Description
7	CS7E	Undefined	CS7 to CS0 Enable
6	CS6E	Undefined	These bits select enabling or disabling of the corresponding $\overline{\text{CSn}}$
5	CS5E	Undefined	output pins.
4	CS4E	Undefined	0: Setting for an I/O port pin
3	CS3E	Undefined	1: Setting for a $\overline{\text{CSn}}$ output pin (n = 7 to 0)
2	CS2E	1	
1	CS1E	Undefined	
0	CS0E	Undefined	

- Port function control register 2 (PFCR2) Number of bits: 8 Address: H'FFFBC2

Bit	Bit Name	Setting	Description
6	CS2S	0	$\overline{\text{CS2}}$ Output Pin Select
			0: Specifies pin PB2 as $\overline{\text{CS2}}$-A output pin
			1: Specifies pin PB1 as $\overline{\text{CS2}}$-B output pin
3	RDWRS	0	RD/$\overline{\text{WR}}$ Output Pin Select
			0: Specifies pin PA1 as RD/$\overline{\text{WR}}$-A output pin
			1: Specifies pin PB6 as RD/$\overline{\text{WR}}$-B output pin
2	RDWRE	1	RD/$\overline{\text{WR}}$ Output Enable
			0: Output of RD/$\overline{\text{WR}}$ is disabled.
			1: Output of RD/$\overline{\text{WR}}$ is enabled.

- Port function control register 4 (PFCR4) Number of bits: 8 Address: H'FFFBC4

Bit	Bit Name	Setting	Description
4	A20E	1	Address A20 Enable 0: Disables the A20 output 1: Enables the A20 output
3	A19E	1	Address A19 Enable 0: Disables the A19 output 1: Enables the A19 output
2	A18E	1	Address A18 Enable 0: Disables the A18 output 1: Enables the A18 output
1	A17E	1	Address A17 Enable 0: Disables the A17 output 1: Enables the A17 output
0	A16E	1	Address A16 Enable 0: Disables the A16 output 1: Enables the A16 output

- Port function control register 6 (PFCR6) Number of bits: 8 Address: H'FFFBC6

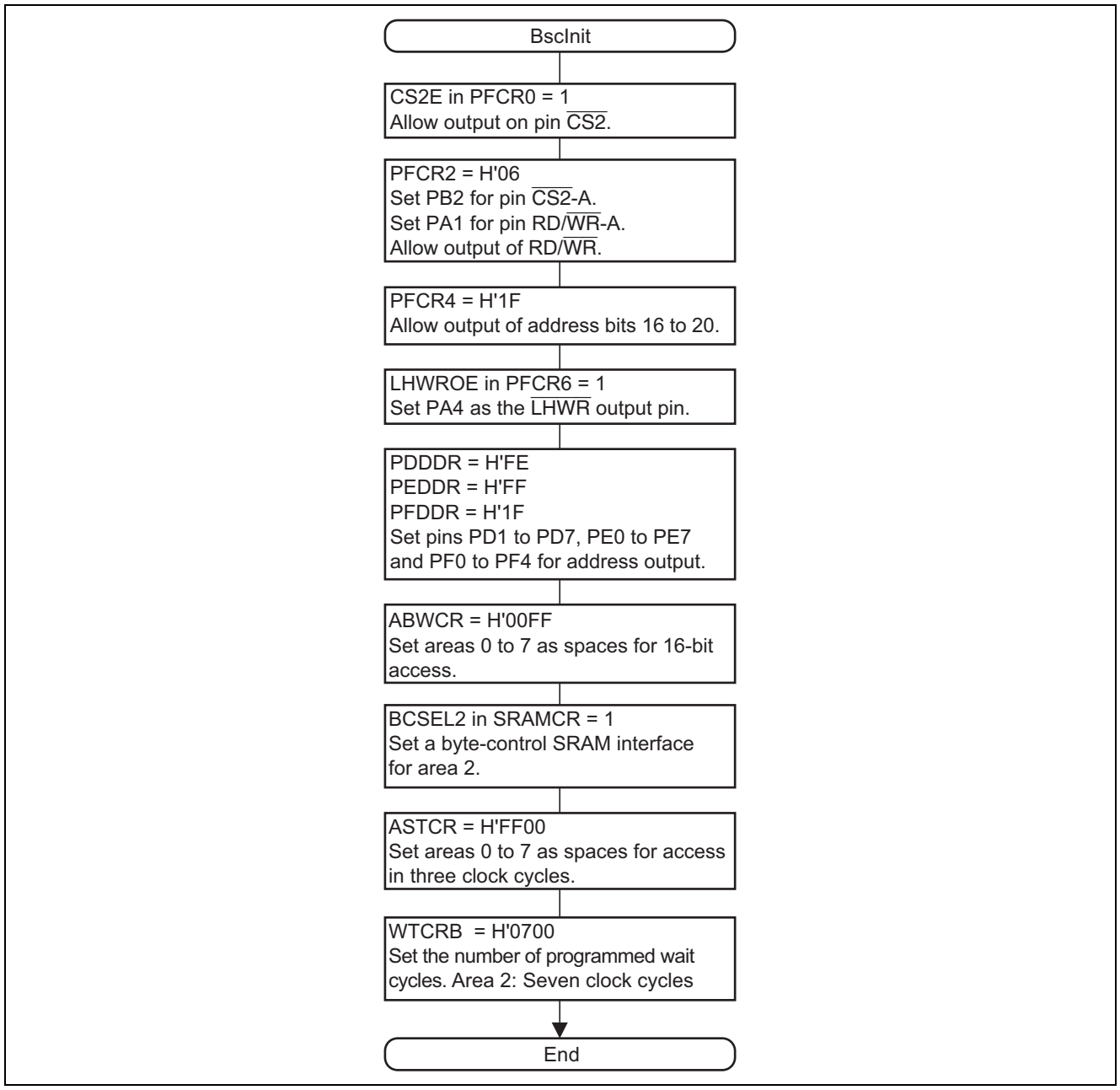
Bit	Bit Name	Setting	Description
6	LHWROE	1	$\overline{\text{LHWR}}$ Output Enable 0: Sets PA4 as an I/O port pin 1: Sets PF4 as the $\overline{\text{LHWR}}$ output pin

- Bus width control register (ABWCR) Number of bits: 16 Address: H'FFFD84
  Function: Sets areas 7 to 0 as spaces for 16-bit access.
  Value: H'00FF
- Access cycle-control register (ASTCR) Number of bits: 16 Address: H'FFFD86
  Function: Sets areas 7 to 0 as spaces for access in three clock cycles (states).
  Value: H'FF00
- Wait control register B (WTCRB) Number of bits: 16 Address: H'FFFD8A
  Function: Sets the number of programmed clock cycles of waiting (wait states). Seven clock cycles are inserted for access to area 2.
  Value: H'0700

- SRAM mode control register (SRAMCR) Number of bits: 16 Address: H'FFFD98

Bit	Bit Name	Setting	Description
10	BCSEL2	1	This bit selects the bus interface for the corresponding area. 0: Area n is a basic bus interface 1: Area n is a byte-control SRAM interface

5. Flowchart


BscInit
CS2E in PFCR0 = 1
Allow output on pin CS2.
PFCR2 = H'06
Set PB2 for pin CS2-A.
Set PA1 for pin RD/WR-A.
Allow output of RD/WR.
PFCR4 = H'1F
Allow output of address bits 16 to 20.
LHWROE in PFCR6 = 1
Set PA4 as the LHWR output pin.
PDDDR = H'FE
PEDDR = H'FF
PFDDR = H'1F
Set pins PD1 to PD7, PE0 to PE7
and PF0 to PF4 for address output.
ABWCR = H'00FF
Set areas 0 to 7 as spaces for 16-bit
access.
BCSEL2 in SRAMCR = 1
Set a byte-control SRAM interface
for area 2.
ASTCR = H'FF00
Set areas 0 to 7 as spaces for access
in three clock cycles.
WTCRB = H'0700
Set the number of programmed wait
cycles. Area 2: Seven clock cycles
End

6. Documents for Reference

- Hardware Manual
  H8SX/1663 Group Hardware Manual
  The most up-to-date version of this document is available on the Renesas Technology Website.
- Technical News/Technical Update
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Rev.	**Date**	**Page**	**Summary**
1.00	Sep.19.08	—	First edition issued

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