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H8/300H Tiny Series

Watchdog Timer using Internal Oscillator

Introduction

A watchdog timer operation is performed by using an internal oscillator.

Target Device

H8/3664

Contents

1. Specifications

1. A watchdog timer operation is performed by using an internal oscillator.
2. An internal reset occurs when the TCWD overflows.
3. During normal operation, the LED repeatedly turns on and off at constant intervals and the TCWD is initialized before overflow.
4. If the $\overline{\text{IRQ0}}$ switch (SW) is turned on, the TCWD is not initialized and generates an internal reset when TCWD overflows.
5. The LED is connected to the P74 output pin of port 7.
6. Figure 1.1 shows an example of the $\overline{\text{IRQ0}}$ input pin switch connection.

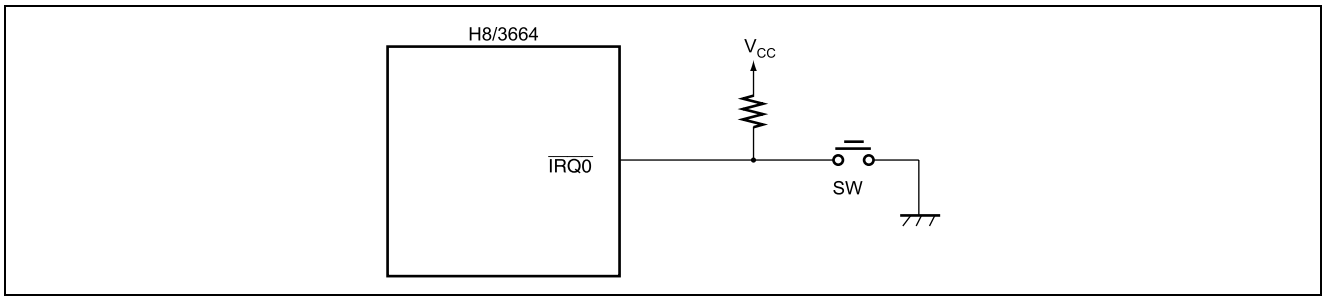


Figure 1 Example of $\overline{\text{IRQ0}}$ Input Pin Switch Connection

2. Description of Functions

1. In this sample task, a watchdog timer operation is implemented using an internal oscillator. Figure 2.1 is a block diagram of the watchdog timer function. The elements of the block diagram are described below.

- The internal oscillator is an RC circuit oscillator and is used as the input clock for TCWD. The time taken for TCWD to count from 0 to 255 and an internal reset to occur is 0.4 sec (rated value) with a minimum value of 0.2 sec.
- The timer control/status register WD (TCSRWD) controls writing to TCSRWD and TCWD and watchdog timer operation, and indicates the status of operation.
- The timer counter WD (TCWD) is an 8-bit readable/writable upward counter that is incremented by the internal clock input. In this sample task, an internal oscillator is selected as the input clock.
- The timer mode register WD (TMWD) selects an input clock. In this sample task, an internal oscillator is selected.

TCWD overflow cycle is calculated by the following equation:

$$\text{TCWD overflow cycle} = \frac{\text{Internal oscillator overflow time}}{256} \times (256 - \text{re-set value of TCWD})$$

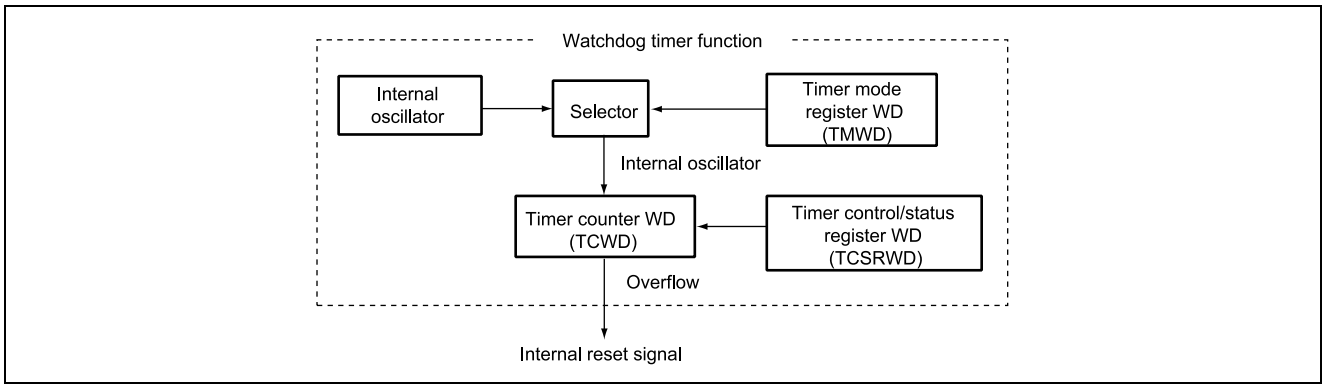


Figure 2.1 Block Diagram of Watchdog Timer Function

2. Table 2.1 lists the function allocation for this sample task. The functions listed in this table are allocated to implement the watchdog timer operation.

Table 2.1 Function Allocation

Function	Description
Internal oscillator	Input clock for TCWD
TCSRWD	Controls the watchdog timer operation and indicates the operation status.
TCWD	Watchdog timer counter
TMWD	Specifies an internal oscillator as the input clock.
$\overline{\text{IRQ0}}$	Switch input pin
P74	LED output

3. Description of Operation

Figure 3.1 illustrates the operation of this sample task. The hardware and software processing are applied as shown in figure 3.1 to implement the watchdog timer operation using the internal oscillator.

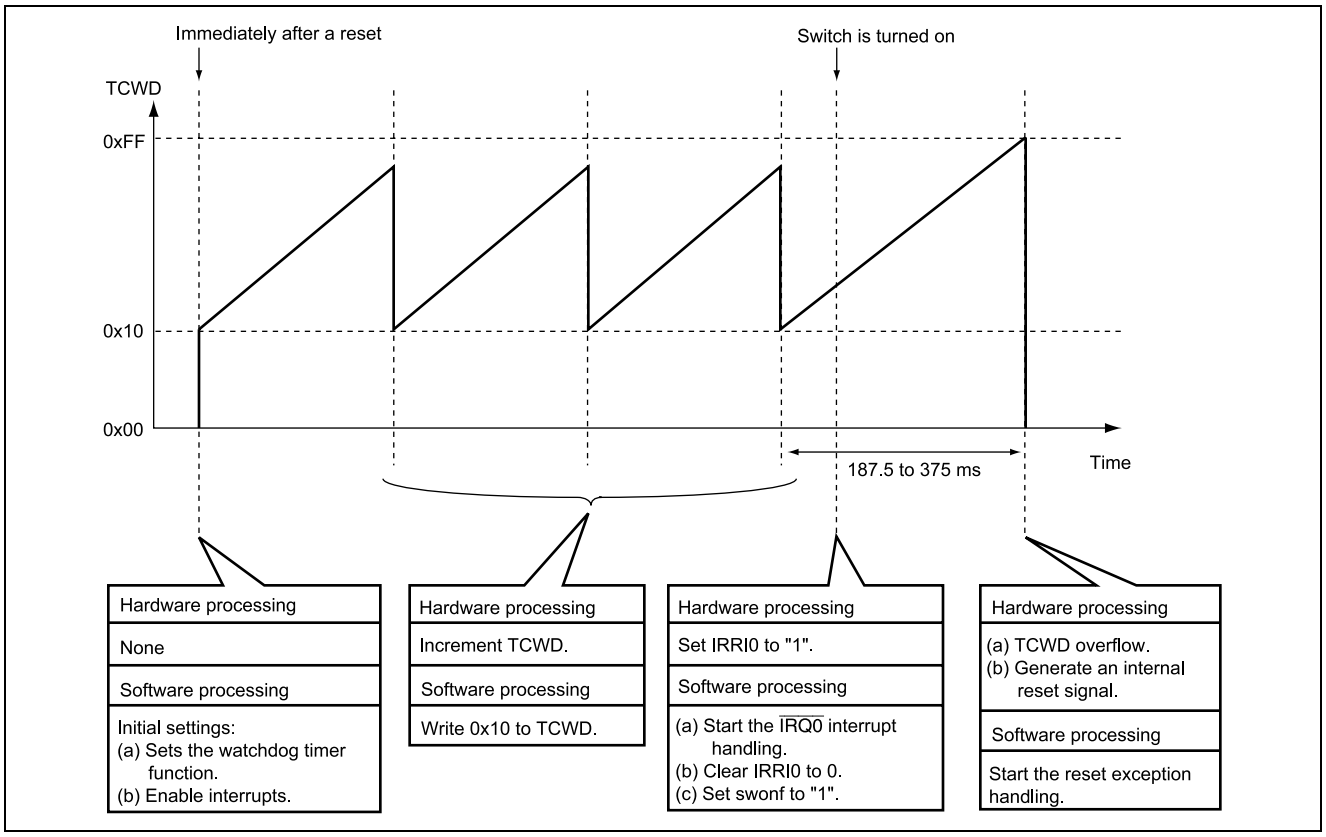


Figure 3.1 Principle of Operation

4. Description of Software

4.1 Modules

Table 4.1 describes the modules used in this sample task.

Table 4.1 Description of Modules

Module Name	Label Name	Function
Main routine	main	Sets the watchdog timer function, enables interrupts, controls LEDs, and checks the state of the switch connected to the $\overline{\text{IRQ0}}$ pin.
Switch on	irq0int	IRQ0 interrupt handling Sets swonf to 1.

4.2 Arguments

This sample task uses no arguments.

4.3 Internal Registers

The internal registers used in this sample task are described below.

- TCSRWDTimer control status register WD Address: 0xFFC0

Bit	Bit Name	Setting	Function
7	B6W1	0	Bit 6 write disable B6WI = 0: Enables a write to bit 6 of TCSRWD B6WI = 1: Disables a write to bit 6 of TCSRWD
6	TCWE	1	Timer counter W write enable TCWE = 0: Disables a write to TCWD. TCWE = 1: Disables a write to TCWD.
5	B4W1	0	Bit 4 write disable B4WI = 0: Enables a write to bit 4 of TCSRWD. B4WI = 1: Disables a write to bit 4 of TCSRWD.
4	TCSRWE	1	Timer control/status register W write disable TCSRWE = 0: Enables a write to bits 0 and 2 of TCSRWD. TCSRWE = 1: Disables a write to bits 0 and 2 of TCSRWD.
3	B2W1	1	Bit 2 write disable B4WI = 0: Enables a write to bit 2 of TCSRWD. B4WI = 1: Disables a write to bit 2 of TCSRWD.
2	WDON	0	Watchdog timer on WDON = 0: Stops counting up by TCWD. WDON = 1: Starts counting up by TCWD.
1	B0W1	1	Bit 2 write disable B0WI = 0: Enables a write to bit 0 of TCSRWD B0WI = 1: Disables a write to bit 0 of TCSRWD
0	WRST	0	Watchdog timer reset WRST = 0: Indicates that TCWD overflow has not occurred WRST = 1: Indicates that TCWD overflow has occurred and an internal reset signal is generated.

- TCWD Timer counter WD Address: 0xFFC1

  Function: An 8-bit counter that uses an internal oscillator as the input clock. If the TCWD overflows, an internal reset signal is generated.

  Setting: 0x10

- TMWD Timer mode register WD Address: 0xFFC2

Bit	Bit Name	Setting	Function
3	CKS3	CKS3 = 0	Clock select 3 to 0
2	CKS2	CKS2 = x	CKS3 = 0, CKS2 = x, CKS1 = x, CKS0 = x:
1	CKS1	CKS1 = x	Specify the TCWD input clock as the internal oscillator.
0	CSK0	CSK0 = x	(x: Don't care)

- PDR7 Port data register 7 Address: 0xFFDA

Bit	Bit Name	Setting	Function
4	P74	0	Port data register 74 P74 = 0: Sets the P74 pin output to a low level. P74 = 1: Sets the P74 pin output to a high level.

- PMR1 Port mode register 1 Address: 0xFFE0

Bit	Bit Name	Setting	Function
4	IRQ0	1	P14/$\overline{\text{IRQ0}}$ pin function select IRQ0 = 0: Specifies the P14/$\overline{\text{IRQ0}}$ pin as the P14 I/O pin. IRQ0 = 1: Specifies the P14/$\overline{\text{IRQ0}}$ pin as the $\overline{\text{IRQ0}}$ input pin.

- PCR7 Port control register 7 Address: 0xFFEA

Bit	Bit Name	Setting	Function
4	PCR74	0	Port control register 74 PCR74 = 0: Specifies the P74 pin as the P74 input pin. PCR74 = 1: Specifies the P74 pin as the P74 output pin.

- IEGR1 Interrupt edge select register 1 Address: 0xFFF2

Bit	Bit Name	Setting	Function
0	IEG0	0	IRQ0 edge select IEG0 = 0: Selects the falling edge for detection of the $\overline{\text{IRQ0}}$ pin input. IEG0 = 1: Selects the rising edge for detection of the $\overline{\text{IRQ0}}$ pin input.

- IENR1 Interrupt enable register 1 Address: 0xFFF4

Bit	Bit Name	Setting	Function
0	IEN0	0	IRQ0 interrupt request enable IEN0 = 0: Disables $\overline{\text{IRQ0}}$ pin interrupt requests. IEN0 = 1 Enables $\overline{\text{IRQ0}}$ pin interrupt requests.

- IIR1 Interrupt flag register 1 Address: 0xFFF6

Bit	Bit Name	Setting	Function
0	IRRI0	0	IRR0 interrupt request flag IRRI0 = 0: Indicates that there is no $\overline{\text{IRQ0}}$ pin interrupt requested. IRRI0 = 1: Indicates that there is an $\overline{\text{IRQ0}}$ pin interrupt requested.

4.4 Description of RAM

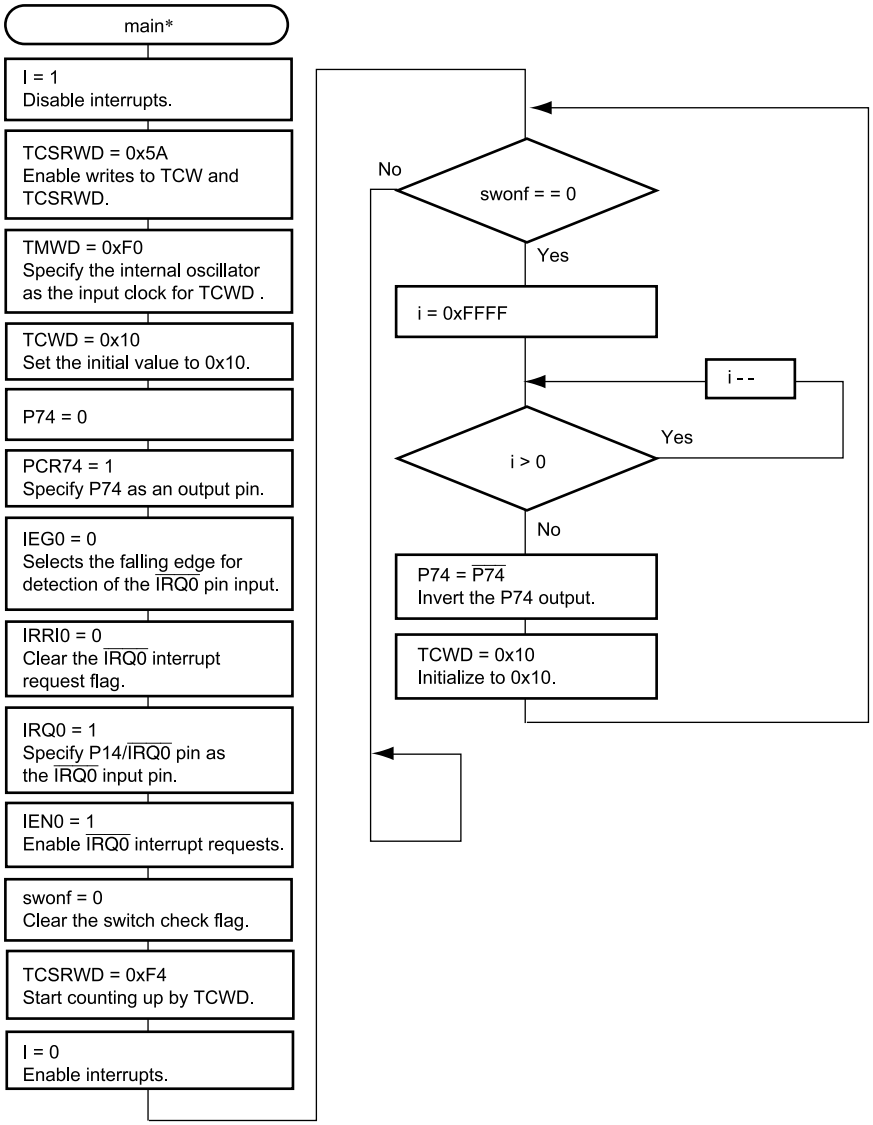
Table 4.2 describes the RAM used in this sample task.

Table 4.2 Description of RAM

Label Name	Function	Size	Used in
swonf	A flag that is used to determine the on/off state of the switch input.	1 byte	Main routine Switch on

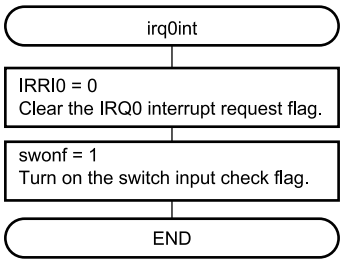
5. Flowcharts

1. Main routine



Note: * The stack pointer is specified by INIT.SRC (assembly language).

2. Switch on



6. Program Listing

```
/************************************************************************************************************************/
/*                                                                                                                      */
/*   H8/300HN Series -H8/3687-                                                                                          */
/      Application Note                                                                                                  */
/*                                                                                                                      */
/*   'Output 0 and 1 by output compare function'                                                                        */
/*                                                                                                                      */
/*   Function                                                                                                           */
/    : Timer Z output compare function                                                                                   */
/*                                                                                                                      */
/    External Clock :    16MHz                                                                                          */
/*   Internal Clock :    16MHz                                                                                          */
/*   Sub Clock :         32.768kHz                                                                                      */
/*                                                                                                                      */
/************************************************************************************************************************/

#include    <machine.h>

/************************************************************************************************************************/
/*   Symbol Definition                                                                                                  */
/************************************************************************************************************************/
struct BIT {
     unsigned char   b7:1;         /* bit7 */
     unsigned char   b6:1;         /* bit6 */
     unsigned char   b5:1;         /* bit5 */
     unsigned char   b4:1;         /* bit4 */
     unsigned char   b3:1;         /* bit3 */
     unsigned char   b2:1;         /* bit2 */
     unsigned char   b1:1;         /* bit1 */
     unsigned char   b0:1;         /* bit0 */
};

#define        TCR0           *(volatile unsigned char *)0xF700                  /* Timer control register_0                */
#define        TIORA0         *(volatile unsigned char *)0xF701                  /* Timer I/O Control Register A_0          */
#define        TCNT0          *(volatile unsigned short *)0xF706                 /* Timer counter_0                         */
#define        GRA0           *(volatile unsigned short *)0xF708                 /* General register A_0                    */
#define        GRB0           *(volatile unsigned short *)0xF70A                 /* General register B_0                    */
#define        TCR1           *(volatile unsigned char *)0xF710                  /* Timer control register_1                */
#define        TIORA1         *(volatile unsigned char *)0xF711                  /* Timer I/O Control Register A_1          */
#define        TSTR           *(volatile unsigned char *)0xF720                  /* Timer start register                    */
#define        TMDR           *(volatile unsigned char *)0xF721                  /* Timer mode register                     */
#define        TPMR           *(volatile unsigned char *)0xF722                  /* Timer PWM mode register                 */
#define        TFCR           *(volatile unsigned char *)0xF723                  /* Timer function control register         */
#define        TOER           *(volatile unsigned char *)0xF724                  /* Timer output master enable register     */
#define        TOCR           *(volatile unsigned char *)0xF725                  /* Timer output control register           */

/************************************************************************************************************************/
/*   Function define                                                                                                    */
/************************************************************************************************************************/
extern void INIT ( void );                                                      /* SP Set                                  */
void main ( void );
```

```
/************************************************************************************************************************/
/*   Vector Address                                                                                                     */
/************************************************************************************************************************/
#pragma section     V1                                          /* VECTOR SECTOIN SET                                   */
void (*const VEC_TBL1[])(void) = {                              /* 0x00 - 0x0f                                          */
     INIT                                                       /* 00 Reset                                             */
};

#pragma section                                                 /* P                                                    */
/************************************************************************************************************************/
/*   Main Program                                                                                                       */
/************************************************************************************************************************/
void main ( void )
{
     set_imask_ccr(1);                                          /* Interrupt Disable                                    */

     TSTR = 0xFC;                                               /* TCNT0 count stop                                     */
     TMDR = 0x0E;                                               /* TCNT0,TCNT1 Single Mode                              */
     TPMR = 0x88;                                               /* FTIOB0 is Normal Mode                                */
     TFCR = 0x80;                                               /* Chanel 0,1 is Normal Mode                            */
     TOER = 0xFC;                                               /* FTIOA0,FTIOB0 Output Enable                          */
     TCR0 = 0x01;                                               /* Rising edge, phi/2 Clock count                       */
     TOCR = 0x01;                                               /* First level set FTIOA0:1 FTIOB0:0                    */
     TIORA0 = 0xA9;                                             /* 0 output by GRA compare match                        */
                                                                /* 1 output by GRB compare match                        */
     GRA0 = 0x4000;                                             /* Set GRA0                                             */
     GRB0 = 0x8000;                                             /* Set GRB0                                             */
     TCNT0 = 0x0000;                                            /* Set TCNT0                                            */
     TSTR = 0xFD;                                               /* TCNT0 count start                                    */

     set_imask_ccr(0);                                          /* Interrupt Enable                                     */
     while(1);
}
```

Link address specifications

Section Name	Address
CV1	0x0000
CV2	0x001C
P	0x0100
B	0xFB80

Revision Record

		Description	
Rev.	Date	Page	Summary
1.00	Sep.29.03	—	First edition issued

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