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M16C/64 Group

Watchdog Timer

1. Abstract

The watchdog timer is the facility to detect program runaway.
The watchdog timer has a 15-bit counter and provides a facility to enable or disable count source protection mode.
Table 1 shows specifications of the watchdog timer.

Table 1. Watchdog Timer Specifications

Item	When count source protection mode is disabled	When count source protection mode is enabled
Count source	CPU clock	125 kHz on-chip oscillator clock
Count operation	Down-count	
Count start condition	• If WDTON bit at OFS1 address = 0 After reset, the watchdog timer automatically starts counting. • If WDTON bit at OFS1 address = 1 The watchdog timer starts counting by a write to the WDTS register.	
Count stop condition	Stop mode, wait mode or hold state	None
Operation on underflow	• If PM1 register PM12 bit = 0 Watchdog timer interrupt • If PM1 register PM12 bit = 1 Watchdog timer reset	Watchdog timer reset

The watchdog timer cycle differs depending on the CPU clock, prescaler divide ratio and whether count source protection mode is enabled. The watchdog timer cycles varying with each setting are listed in Table 2.

Table 2. Watchdog Timer Cycles

CSPR register CSPRO bit Note 1, Note 2	CM0 register CM07 bit	WDC register WDC7 bit	Watchdog timer cycle
0 (count source protection mode disabled)	0 (CPU clock is the main clock, PLL clock or 125 kHz on-chip oscillator)	0 (divided by 16)	$\frac{\text{16 (prescaler divide ratio)} \times \text{32768 (WDT count value)}}{\text{CPU clock}}$
		1 (divided by 128)	$\frac{\text{128 (prescaler divide ratio)} \times \text{32768 (WDT count value)}}{\text{CPU clock}}$
	1 (CPU clock is a sub-clock)	—	$\frac{\text{2 (prescaler divide ratio)} \times \text{32768 (WDT count value)}}{\text{CPU clock}}$
1 (count source protection mode enabled)	—	—	$\frac{\text{4096 (WDT count value)}}{\text{125 kHz on-chip oscillator}}$

— : Don't care (can be 1 or 0).
WDT : Watchdog timer
Note 1 : Unless the CSPROINI bit at the OFS1 address is 0 (after-reset count source protection mode enabled), the CSPRO bit is not set to 1 (count source protection mode enabled) after reset.
Note 2 : To set the CSPRO bit to 1, write 0 and then write 1 in succession in a program. The CSPRO bit cannot be cleared to 0 (count source protection mode disabled) in a program.

2. Introduction

The application example described in this document applies to the following MCU:

- Microcomputers: M16C/64 group

This application note can be used with other M16C Family MCUs which have the same special function registers (SFRs) as the above group. Check the manual for any modifications to functions. Careful evaluation is recommended before using the program described in this application note.

3. Application Example

In the explanation here, we show how to generate a watchdog timer interrupt or a watchdog timer reset using the CPU clock as the count source for the watchdog timer.

3.1 Description of the Application Example

(1) Write 00h and then write FFh to the WDTR register in succession. The watchdog timer is initialized to 7FFFh Note 1.

(2) The watchdog timer starts counting by a write to the WDTS register.

(3) Write to the WDTR register again while the count is in progress. The watchdog timer is initialized to 7FFFh Note 1, from which it continues counting.

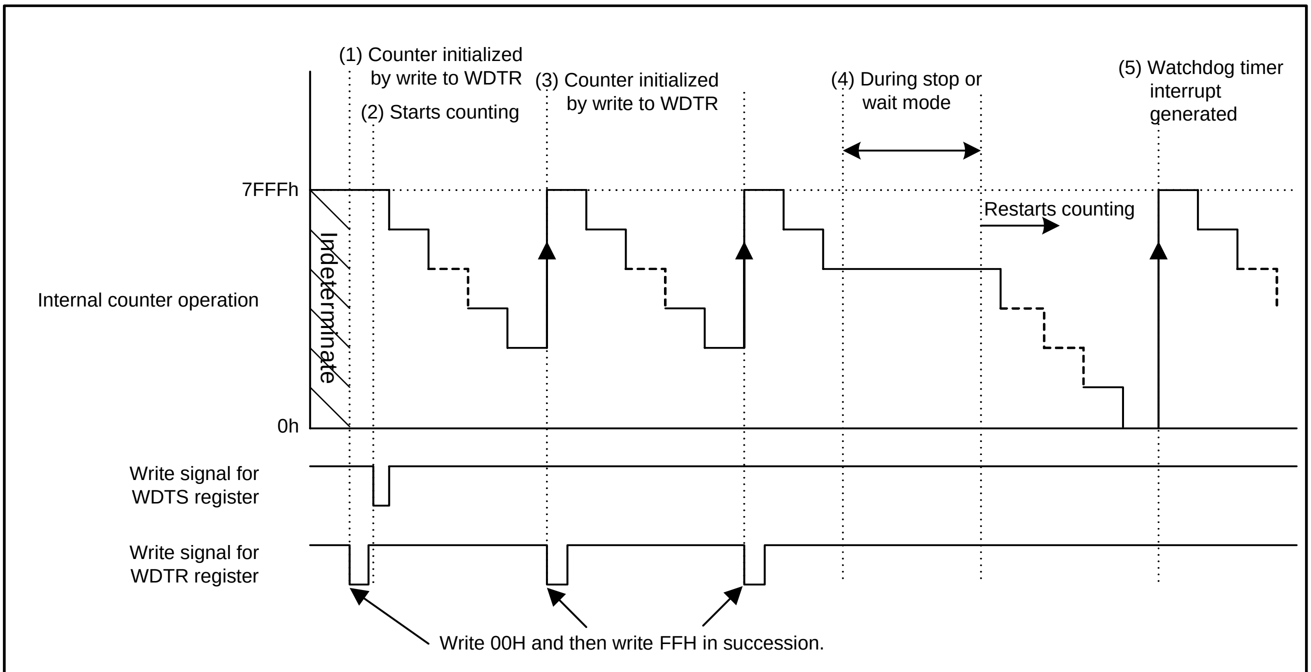
(4) When in wait mode, stop mode or hold state, the watchdog timer stops counting, retaining the last count it had before stopping. When placed out of wait mode or stop mode, it restarts counting from the count value it retained Note 2.

(5) Where a watchdog timer interrupt is used: When the watchdog timer underflows upon reaching the terminal count, a watchdog timer interrupt is generated. In this case, because the watchdog timer is not initialized, perform the write to the WDTR register described in (1) within an interrupt handler. The watchdog timer continues counting.
Where a watchdog timer reset is used: When the watchdog timer underflows upon reaching the terminal count, the pins and the CPU and SFR are initialized, running the program from the address indicated by the reset vector.

Note 1: If the CSPR register CSPRO bit = 1 (count source protection mode enabled), the watchdog timer is initialized to 0FFFh.

Note 2: If the CSPR register CSPRO bit = 1 (count source protection mode enabled), the watchdog timer does not stop even when it is in wait mode, stop mode or hold state.

Figure 1 shows an operation timing diagram.


(1) Counter initialized by write to WDTR
(2) Starts counting
(3) Counter initialized by write to WDTR
(4) During stop or wait mode
(5) Watchdog timer interrupt generated
7FFFh
Indeterminate
Internal counter operation
Restarts counting
0h
Write signal for WDTS register
Write signal for WDTR register
Write 00H and then write FFH in succession.

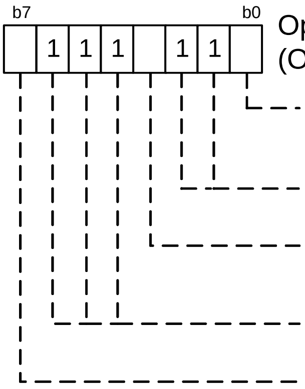
This diagram applies to the following register settings.
PM1 register PM12 bit = 0 (watchdog timer interrupt)
CSPR register CSPRO bit = 0 (count source protection mode disabled)

Figure 1. Watchdog Timer Operation Example

4. How to Set Up

The following shows how to set up the registers to accomplish the operation described in 3, “Application Example.” For details about each register, see the hardware manual of the M16C/64 group.

(1) Setting the optional feature select address



Optional feature select address (OFS1)

The OFS1 address is located in the flash memory (address FFFFFh). Write to this address along with the program.

If the block that includes the OFS1 address is erased, the OFS1 address becomes FFh.

WDTON Watchdog timer start select bit
0: Automatically starts the watchdog timer after reset
1: Keeps the watchdog timer idle after reset

Reserved bits
Set these bits to 1.

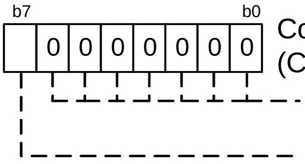
ROMCP1 ROM code protect bit
0: Enables ROM code protect
1: Disables ROM code protect

Reserved bits
Set these bits to 1.

CSPROINI After-reset count source protection mode select bit
0: Enables after-reset count source protection mode
1: Disables after-reset count source protection mode

When setting the CSPROINI bit to 0, be sure to set the WDTON bit to 0 also.

(2) Setting the count source protection mode register



Count source protection mode register (CSPR)

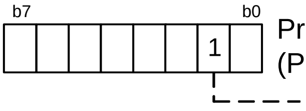
If the CSPROINI bit at the OFS1 address is cleared by writing 0, the value of this register after reset is ‘10000000b.’

Reserved bits
Set these bits to 0.

CSPRO Count source protection mode select bit
0: Disables count source protection mode
1: Enables count source protection mode

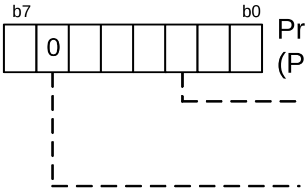
To set the CSPRO bit to 1, write 0 and then write 1 in succession. This bit cannot be cleared to 0 in a program.

(3) Setting processor mode register 1



Protect register (PRCR)

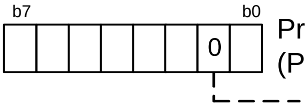
PRC1 Protect bit 1
PM0, PM1, PM2, TB2SC, INVC0, INVC1 register write enable
0: Disables write
1: Enables write



Processor mode register 1 (PM1)

PM12 Watchdog timer facility select bit
0: Watchdog timer interrupt
1: Watchdog timer reset

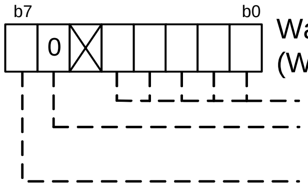
Reserved bit
Set this bit to 0.



Protect register (PRCR)

PRC1 Protect bit 1
PM0, PM1, PM2, TB2SC, INVC0, INVC1 register write enable
0: Disables write
1: Enables write

(4) Setting the watchdog timer control register



Watchdog timer control register (WDC)

Watchdog timer high-order bits

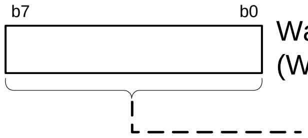
Reserved bit
Set this bit to 0.

WDC7 Prescaler select bit
0: Divide by 16
1: Divide by 128

If the CSPRO bit = 1 (count source protection mode enabled), the on-chip oscillator is selected for the count source, in which case the clock frequency division by the prescaler is not performed no matter how WDC7 is set.

If the CSPRO bit = 0 (count source protection mode disabled) and the selected CPU clock is a sub-clock, a division by 2 is assumed for the clock frequency division by the prescaler no matter how WDC7 is set.

(5) Setting the watchdog timer reset register

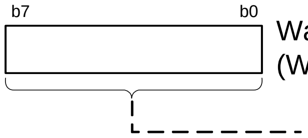


Watchdog timer reset register (WDTR)

Write 00h and then write FFh to this register in succession. The watchdog timer is initialized.
Watchdog timer initial value
- When count source protection mode is disabled: 7FFFh
- When count source protection mode is enabled: 0FFFh

Be sure that no interrupt or DMA transfer occurs between a write of 00h and a write of FFh.
After a watchdog timer interrupt is generated, use the WDTR register to initialize the watchdog timer.

(6) Setting the watchdog timer start register



Watchdog timer start register (WDTS)

The watchdog timer starts by a WDTS register write instruction.

5. Sample Programs

5.1 Writing to the OFS1 Address

The OFS1 address is located in the flash memory, so write to this address along with the program.
Figure 2 shows how to write a program fragment to the OFS1 address using the extended directive command ".OFSREG" of as30 in C language.

```
#if __WATCH_DOG__ != 0
    _asm(".ofsreg  0FEH");    /* WATCH DOG TIMER START When on Reset */
#else
    _asm(".ofsreg  0FFH");    /* WATCH DOG TIMER STOP When on Reset */
#endif
```

Figure 2. How to Write to the OFS1 Address

5.2 To Use a Watchdog Timer Interrupt

In the example here, the PLL clock (24 MHz) is chosen to be the CPU clock. Also, the CSPROINI and WDTON bits at the OFS1 address are set to 1.
While writing to the WDTR register, increment the display of port P10 every 500 ms. When the output of port P10 becomes 40h, stop writing to the WDTR register and turn off updating of the port 10 display.
When a watchdog timer interrupt is generated, decrement the display of port P10 every 500 ms while writing to the WDTR register in a watchdog timer interrupt handler. When the output of port P10 becomes 00h, turn off updating of the port 10 display.

```
/**********************************************************************************/
/*
/*  M16C/64 Group Program Collection
/*
/*  File name   :   rjj05b1289_int_src.c
/*  CPU         :   M16C/64 Group
/*  Function    :   Operation of Watchdog Timer
/*  Version     :   1.00 (2008-05-21) Initial
/*
/*  Copyright(C)2008, Renesas Technology Corp. , All rights reserved.
/*
/**********************************************************************************/
/* Refer to the corresponding application notes for program specifications.       */

#include    "sfr64.h"

void main(void);
void mcu_init(void);

/**********************************************************************************/
/*      DEFINE
/**********************************************************************************/
void    wdt_int(void);

/**********************************************************************************/
/*      RAM
/**********************************************************************************/

/**********************************************************************************/
/*      ROM
/**********************************************************************************/
```

```
/************************************************************************************/
/*      Pragma
/************************************************************************************/

/************************************************************************************/
/*      Main Program
/************************************************************************************/
void main(void)
{
     unsigned int i;

    mcu_init();                 /* MCU initialize */

    p10 = 0;
    pd10 = 0xff;

    ta0mr = 0x40;               /* Selection of timer mode
                                   Pulse output function select bit (0:Pulse is not output)
                                   Gate function select bit (00:Gate fuction not available)
                                   Count source (01:f8) */
    ta0 = 4000-1;               /* Setting counter value (1msec @24MHz, f8) */

    cpsrf = 0;                  /* Setting clock prescaler reset flag (0:No effect) */

    ta0ic = 0x00;               /* Setting interrupt priority levels in timer A0 */

    ta0s = 1;                   /* TimerA1 count start */

    prcr = 0x02;

    pm12 = 0;                   /* Watchdog Timer Function Select Bit(0 : Watchdog timer interrupt)
                                   */
    prcr = 0x00;

    wdc = 0;                    /* Setting watchdog timer control register
                                   Prescaler select bit is set to 0 (0:Divided be 16) */
    wdtr = 0x00;                /* Setting watchdog timer reset register
                                   Watchdog timer initialize  */
    wdtr = 0xff;                /* Setting watchdog timer value (0x7FFF) */

    i = 0;

    wdts = 1;                   /* Setting watchdog timer start register */

    while (1) {
        while (!ir_ta0ic) {}
        ta0ic = 0x00;
        i++;
        if ( i >= 500 ) {
            i = 0;
            p10++;
        }
        if ( p10 >= 64 ) {
            p10 = 64;
        } else {
            wdtr = 0x00;                /* Setting watchdog timer reset register
                                           Watchdog timer initialize  */
            wdtr = 0xff;                /* Setting watchdog timer value (0x7FFF) */
        }
    }
}

/************************************************************************************/
/*      MCU Initialize
/************************************************************************************/
void mcu_init()
{
     unsigned int i;
    prcr  = 0x03;                /* CM0,CM1,CM2,PLC0,PCLKR register protect off           */
                                 /* PM0,PM1,PM2,TB2SC,INVC0,INVC1 register protect off    */
    pm0   = 0x00;                /* Processor mode: Single-chip mode                      */
    pm1   = 0x08;                /* Watchdog timer function: Watchdog timer interrupt     */
                                 /* Internal reserved area: The entire area usable        */
                                 /* Wait: No wait state                                   */
    cm2   = 0x00;                /* System clock select: Main clock                       */
    cm1   = 0x20;                /* Main clock division select: No division mode          */
    cm0   = 0x08;                /* Main clock division select: CM16 and CM17 enabled     */
    pm20  = 0;                   /* SFR 2waits when PLL on                            */
    plc0  = 0x14;                /* PLL clock Multiply by 4                           */
                                 /* PLL multiplying factor select: Multiply by 8      */
                                 /* Reference frequency counter: Divide by 2          */
    plc07 = 1;                   /* PLL operation enable: PLL ON                      */
    for (i = 0; i < 20000; i++); /* Wait until the PLL clock becomes stable (tsu(PLL)) */
    cm11  = 1;                   /* System clock select: PLL clock                    */
    prcr  = 0x00;                /* Protect on                                        */
}

/******************************************
 * Watchdog timer interrupt routine      *
 ******************************************/
#pragma interrupt wdt_int()
void    wdt_int() {
    unsigned int i = 0;

    wdtr = 0x00;                /* Set the WDTS register in the beginning of the */
    wdtr = 0xff;                /* watchdog timer interrupt routine  */

    while (1) {
        while (!ir_ta0ic) {}
        ta0ic = 0x00;
        i++;

        wdtr = 0x00;
        wdtr = 0xff;

        if(i == 500){
            i = 0;
            if ( p10 != 0 ) {
                p10--;
            }
          }
    }
}
```

5.3 To Reset by a Watchdog Timer Underflow

In the example here, the PLL clock (24 MHz) is chosen to be the CPU clock. Also, the CSPROINI and WDTON bits at the OFS1 address are set to 1.

While writing to the WDTR register, increment the display of port P10 every 500 ms. When the output of port P10 becomes 40h, stop writing to the WDTR register and turn off updating of the port 10 display. The device is reset when the watchdog timer underflows upon reaching the terminal count.

```
/************************************************************************************/
/*
/*  M16C/64 Group Program Collection
/*
/*  File name   :   rjj05b1289_reset_src.c
/*  CPU         :   M16C/64 Group
/*  Function    :   Operation of Watchdog Timer
/*  Version     :   1.00 (2008-05-21) Initial
/*
/*  Copyright(C)2008, Renesas Technology Corp. , All rights reserved.
/*
/************************************************************************************/
/* Refer to the corresponding application notes for program specifications.       */

#include    "sfr64.h"

void main(void);
void mcu_init(void);

/************************************************************************************/
/*      DEFINE
/************************************************************************************/
void    wdt_int(void);

/************************************************************************************/
/*      RAM
/************************************************************************************/
```

```
/**********************************************************************************/
/*      ROM
/**********************************************************************************/

/**********************************************************************************/
/*      Pragma
/**********************************************************************************/

/**********************************************************************************/
/*      Main Program
/**********************************************************************************/
void main(void)
{
     unsigned int i;

    mcu_init();                 /* MCU initialize */

    p10 = 0;
    pd10 = 0xff;

    ta0mr = 0x40;               /* Selection of timer mode
                                   Pulse output function select bit (0:Pulse is not output)
                                   Gate function select bit (00:Gate function not available)
                                   Count source (01:f8) */
    ta0 = 4000-1;               /* Setting counter value (1msec @24MHz, f8) */

    cpsrf = 0;                  /* Setting clock prescaler reset flag (0:No effect) */

    ta0ic = 0x00;               /* Setting interrupt priority levels in timer A0 */

    ta0s = 1;                   /* TimerA1 count start */

    prcr = 0x02;

    pm12 = 1;                   /* Watchdog Timer Function Select Bit(1 : Watchdog timer reset)
                                   */
    prcr = 0x00;

    wdc = 0;                    /* Setting watchdog timer control register
                                   Prescaler select bit is set to 0 (0:Divided be 16) */
    wdtr = 0x00;                /* Setting watchdog timer reset register
                                   Watchdog timer initialize  */
    wdtr = 0xff;                /* Setting watchdog timer value (0x7FFF) */

    i = 0;

    wdts = 1;                   /* Setting watchdog timer start register */

    while (1) {
        while (!ir_ta0ic) {}
        ta0ic = 0x00;
        i++;
        if ( i >= 500 ) {
            i = 0;
            p10++;
        }
        if ( p10 >= 64 ) {
            p10 = 64;
        } else {
            wdtr = 0x00;                /* Setting watchdog timer reset register
                                           Watchdog timer initialize  */
            wdtr = 0xff;                /* Setting watchdog timer value (0x7FFF) */
        }
    }
}

/**********************************************************************************/
/*      MCU Initialize
/**********************************************************************************/
void mcu_init()
{
     unsigned int i;
    prcr  = 0x03;                /* CM0,CM1,CM2,PLC0,PCLKR register protect off          */
                                 /* PM0,PM1,PM2,TB2SC,INVC0,INVC1 register protect off   */
    pm0   = 0x00;                /* Processor mode: Single-chip mode                     */
    pm1   = 0x08;                /* Watchdog timer function: Watchdog timer interrupt    */
                                 /* Internal reserved area: The entire area usable       */
                                 /* Wait: No wait state                                 */
    cm2   = 0x00;                /* System clock select: Main clock                     */
    cm1   = 0x20;                /* Main clock division select: No division mode        */
    cm0   = 0x08;                /* Main clock division select: CM16 and CM17 enabled   */
    pm20  = 0;                   /* SFR 2waits when PLL on                              */
    plc0  = 0x14;                /* PLL clock Multiply by 4                             */
                                 /* PLL multiplying factor select: Multiply by 8        */
                                 /* Reference frequency counter: Divide by 2            */
    plc07 = 1;                   /* PLL operation enable: PLL ON                        */
    for (i = 0; i < 20000; i++); /* Wait until the PLL clock becomes stable (tsu(PLL))   */
    cm11  = 1;                   /* System clock select: PLL clock                      */
    prcr  = 0x00;                /* Protect on                                          */
}

/****************************************
 * Watchdog timer interrupt routine      *
 ****************************************/
#pragma interrupt wdt_int()
void    wdt_int() {
    unsigned int i = 0;

    wdtr = 0x00;                /* Set the WDTS register in the beginning of the */
    wdtr = 0xff;                /* watchdog timer interrupt routine  */

    while (1) {
        while (!ir_ta0ic) {}
        ta0ic = 0x00;
        i++;

        wdtr = 0x00;
        wdtr = 0xff;

        if(i == 500){
            i = 0;
            if ( p10 != 0 ) {
                p10--;
            }
          }
    }
}
```

6. Reference Documents

Hardware manual

M16C/64 Group Hardware Manual
(Get the latest version from the Renesas Technology website.)

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