# VersaClock 7 RC31 Series SYSREF

This document provides the steps needed to set up SYSREF on the VersaClock 7 (VC7) RC31 series using Renesas IC Toolbox (RICBox) software. For more information about RICBox, see the Renesas IC Toolbox User Guide.

## Contents



## 1. Installation

For more information on installing RICBox software for VC7, see the Renesas IC Toolbox User Guide.

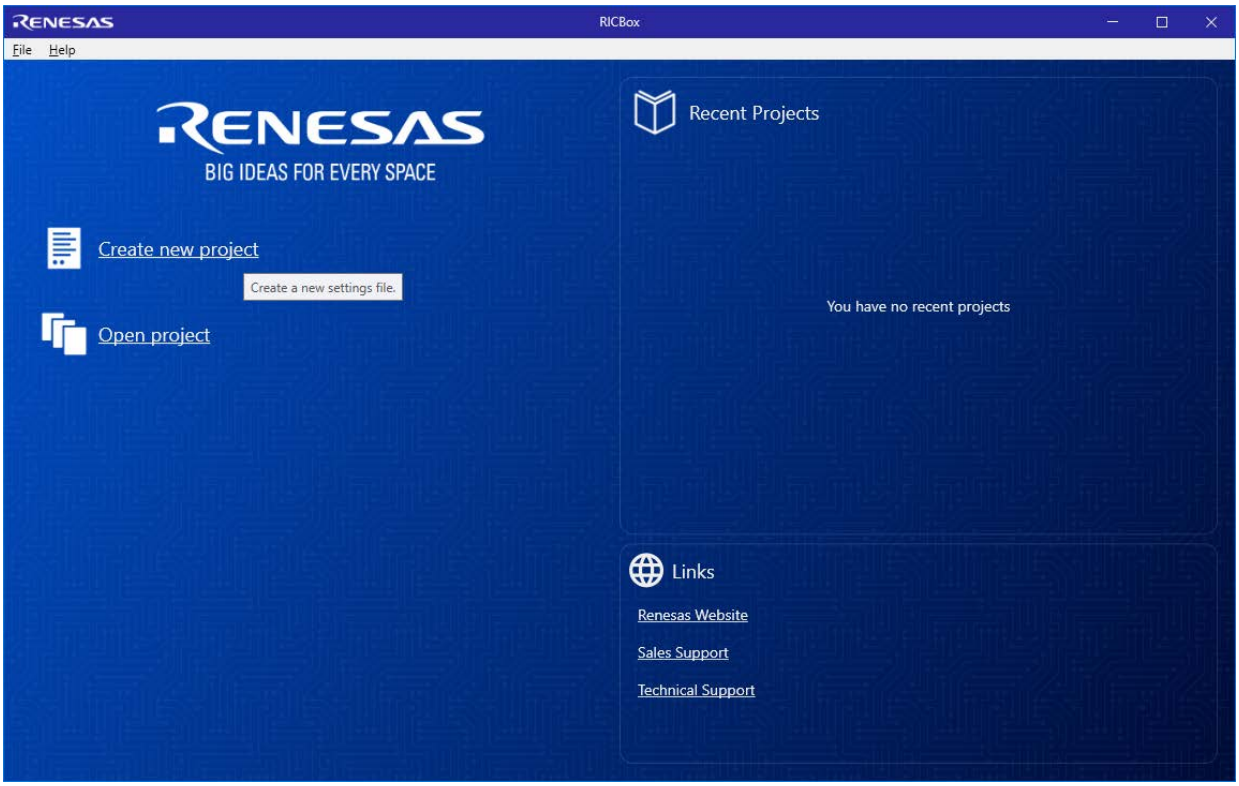
## 2. Creating and Loading Settings Files

RICBox settings files, or .rbs files, are used to save and distribute custom device configurations. Each settings file contains all of the register settings for a given device.

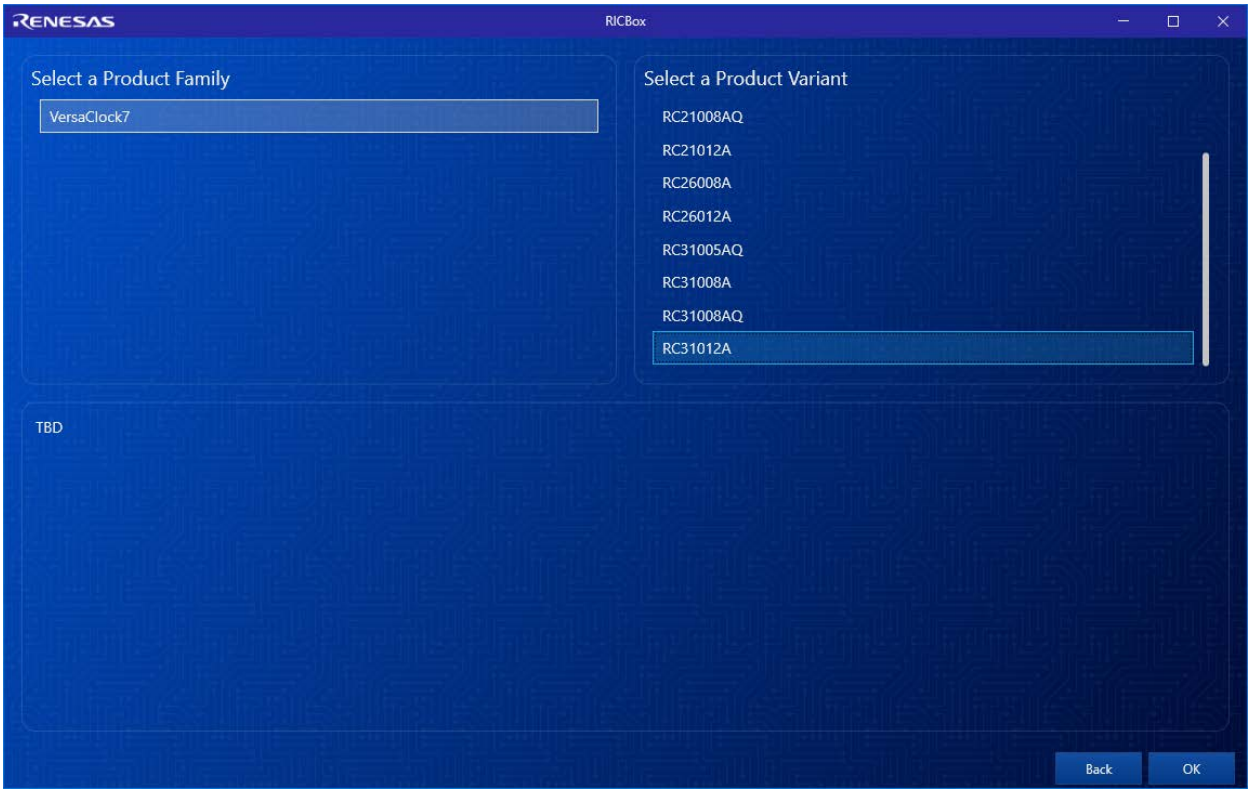
## 2.1 Creating a New Configuration

To create a new configuration:

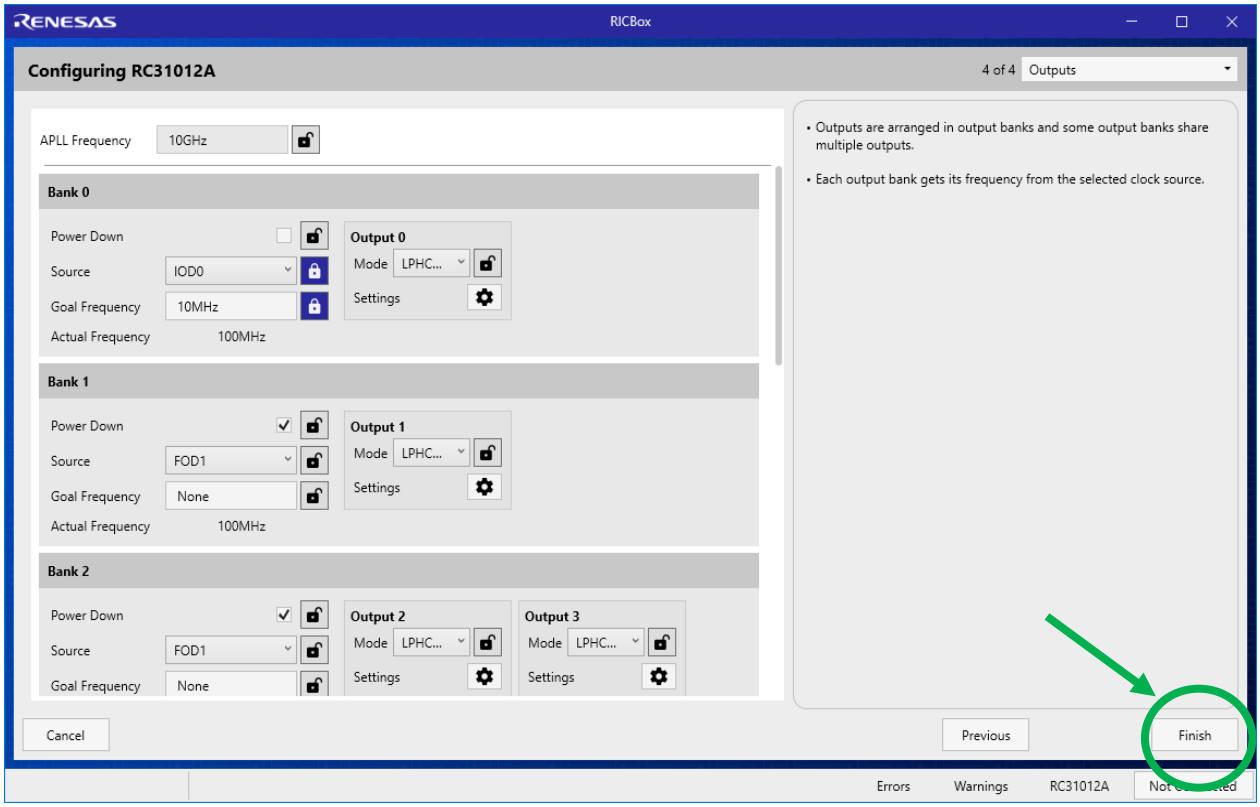
1. Open RICBox and click on the “Create new project” link.




2. Choose the RC31 device to be configured and click “OK”.

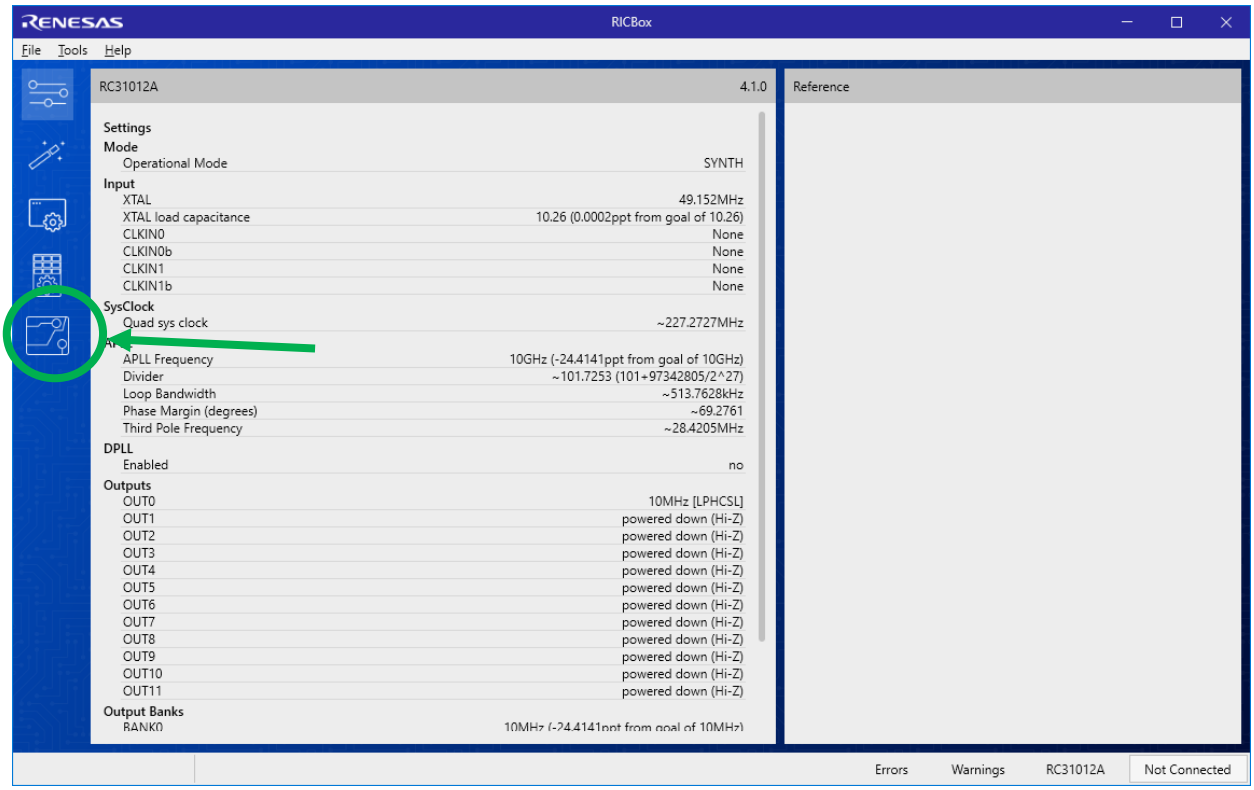


3. Configure the RC31 to match the application. However, for this example, Bank0 will be configured to source from IOD0 and output 10MHz. Click the “Finish” button when done.

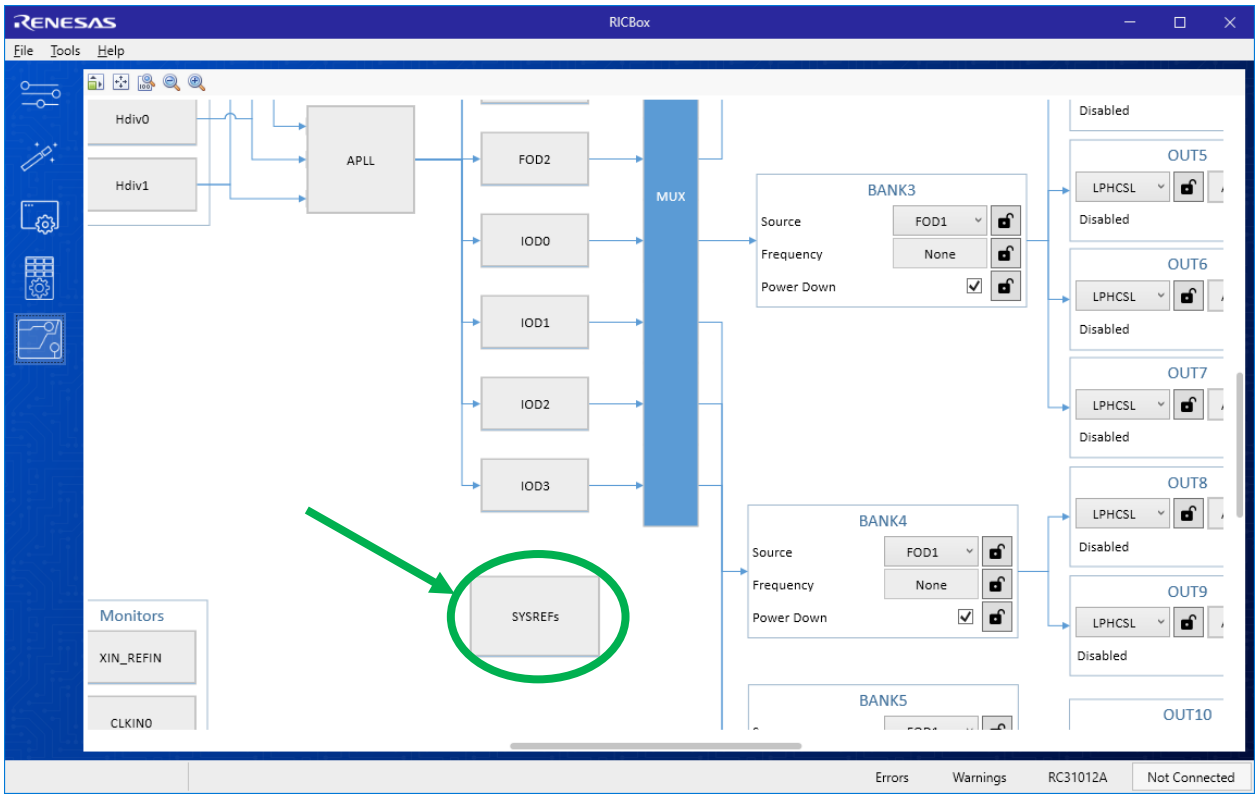


# 3. Setting Up SYSREF

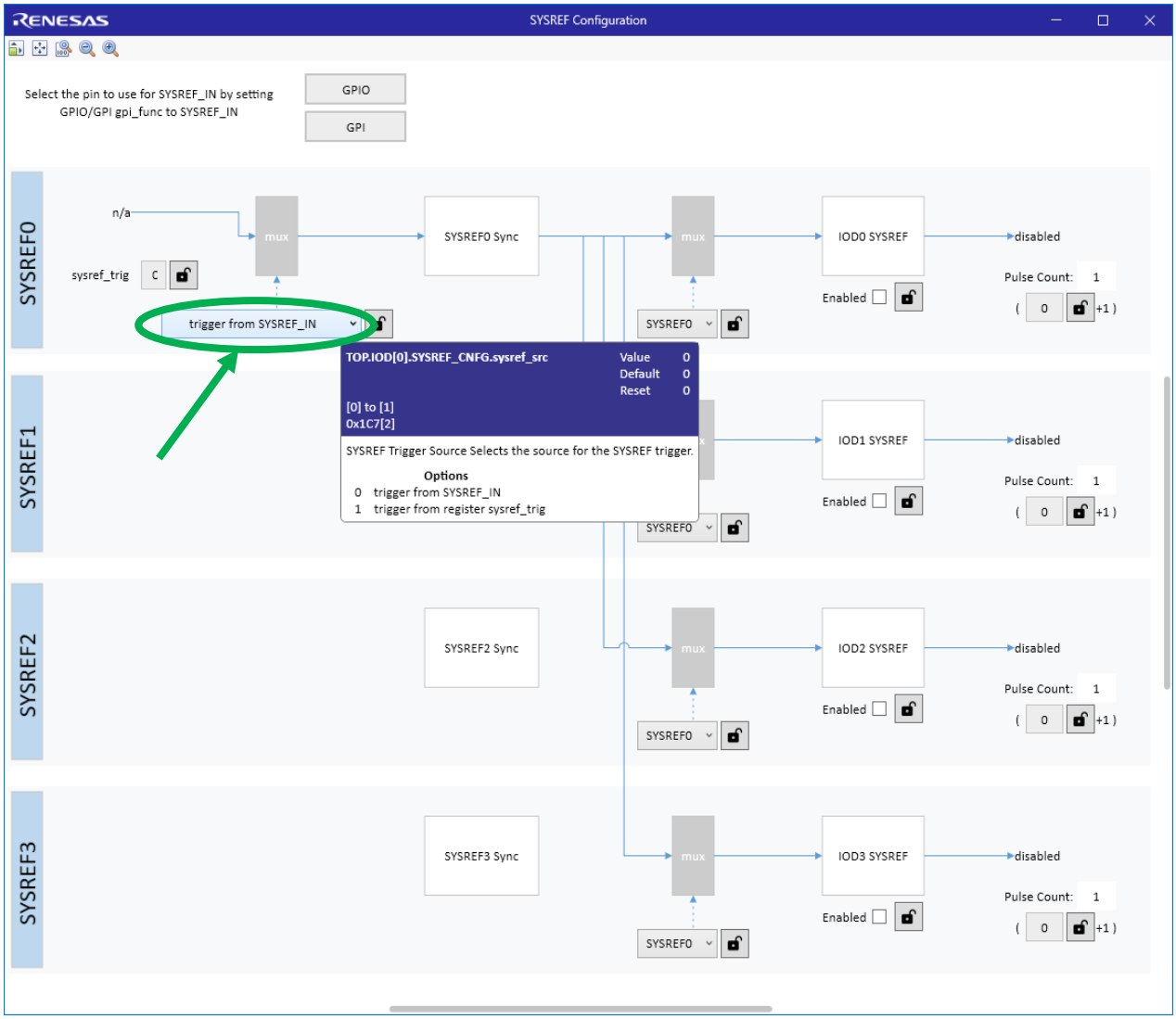
1. Click on the Block Diagram button to view block diagram.




2. Scroll down until the SYSREFs block is visible. Click the SYSREFs block to bring up the SYSREF Configuration GUI.



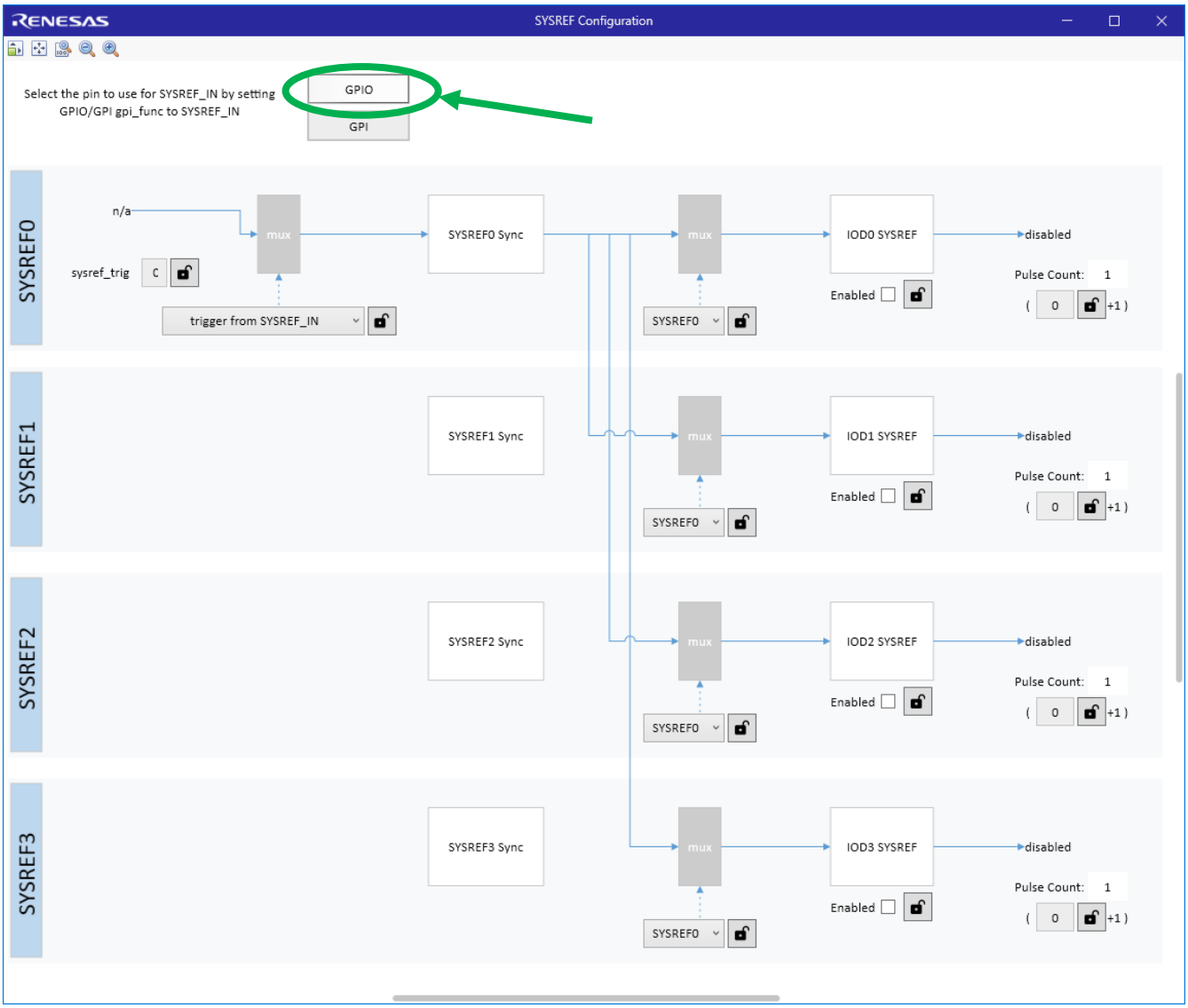
3. Decide how SYSREF0 will be triggered. Trigger from SYSREF_IN requires defining a GPIO/GPI as a SYSREF_IN. Trigger from register sysref_trig uses the respective register field value to transition from ‘0’ to ‘1’.



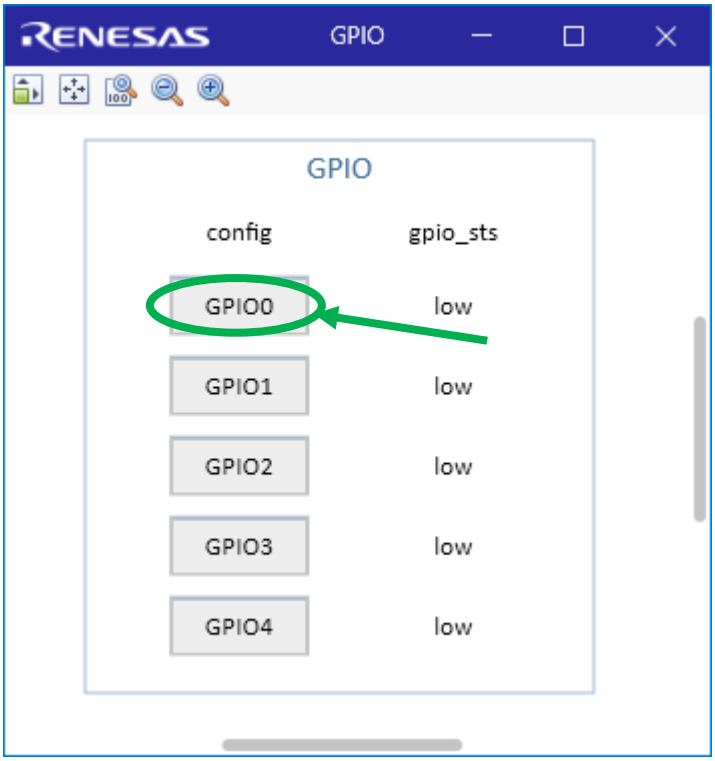
## 3.1 Setting Up GPIO/GPI for SYSREF_IN Trigger

After deciding that SYSREF will be triggered from SYSREF_IN, choose which GPIO/GPI will be the source. For this example, GPIO0 will be the source. To configure GPIO0:

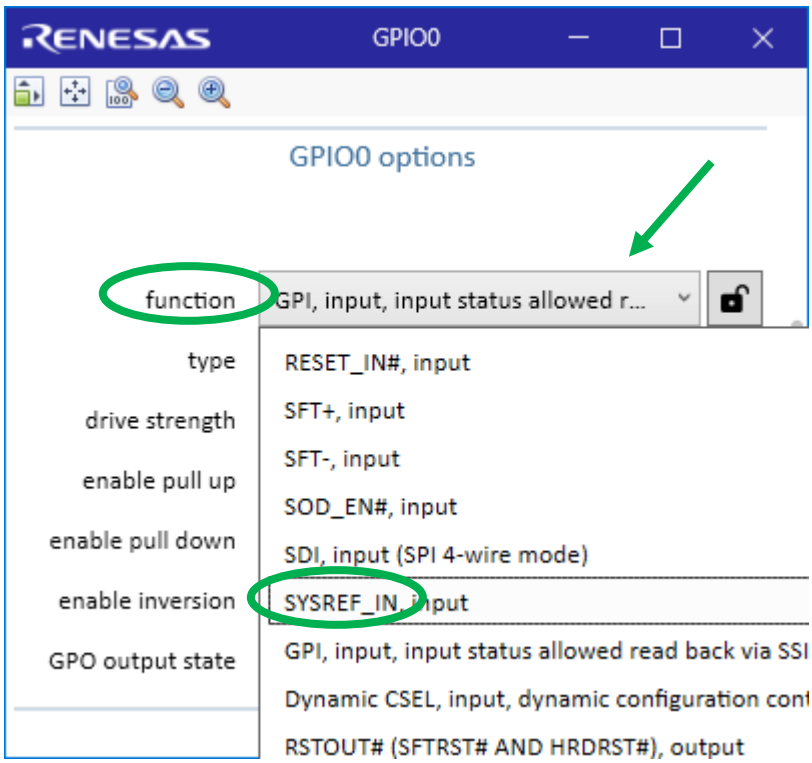
1. Click the GPIO button. This opens the GPIO window.



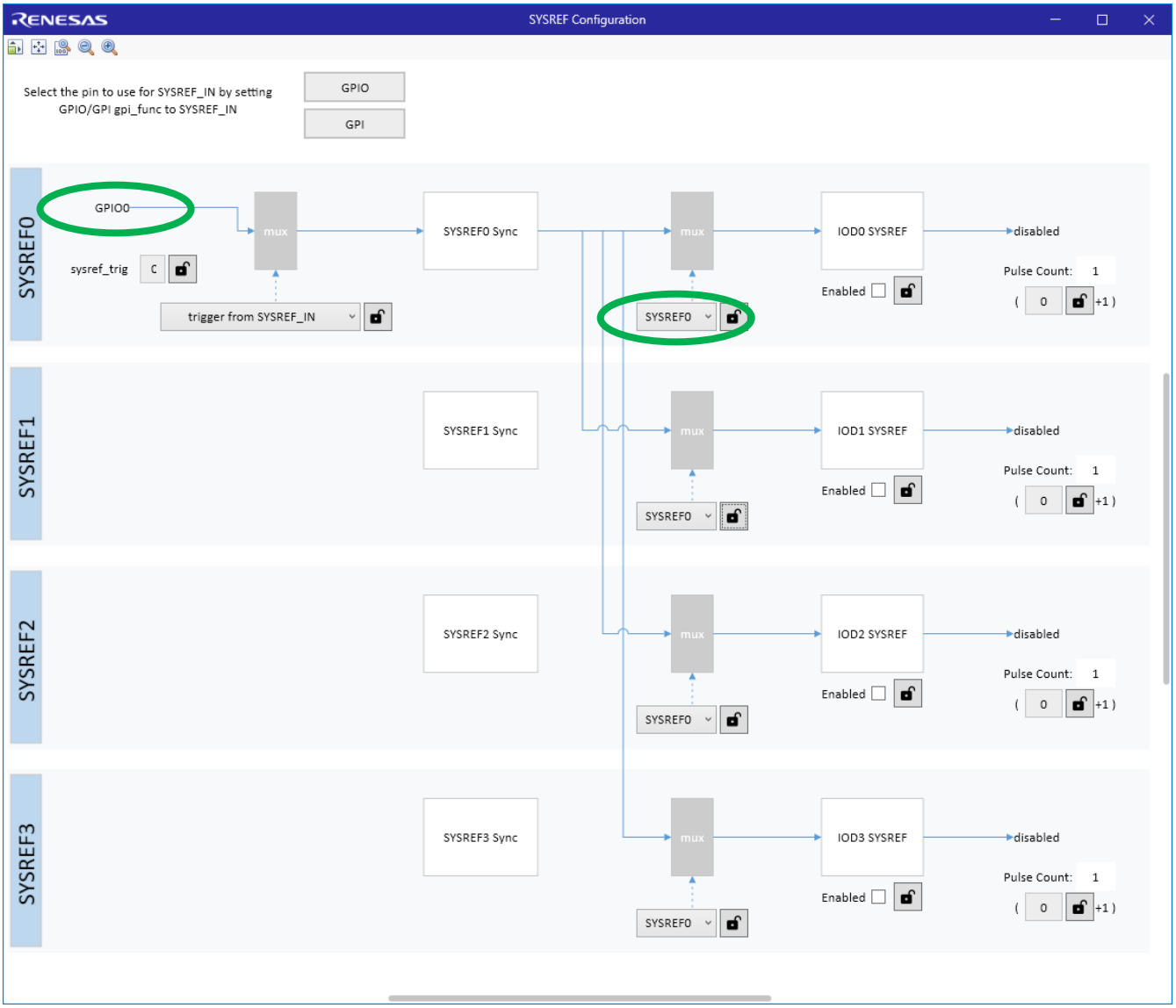
2. In the GPIO window, click the GPIO0 button. This will open a GPIO0 options window.



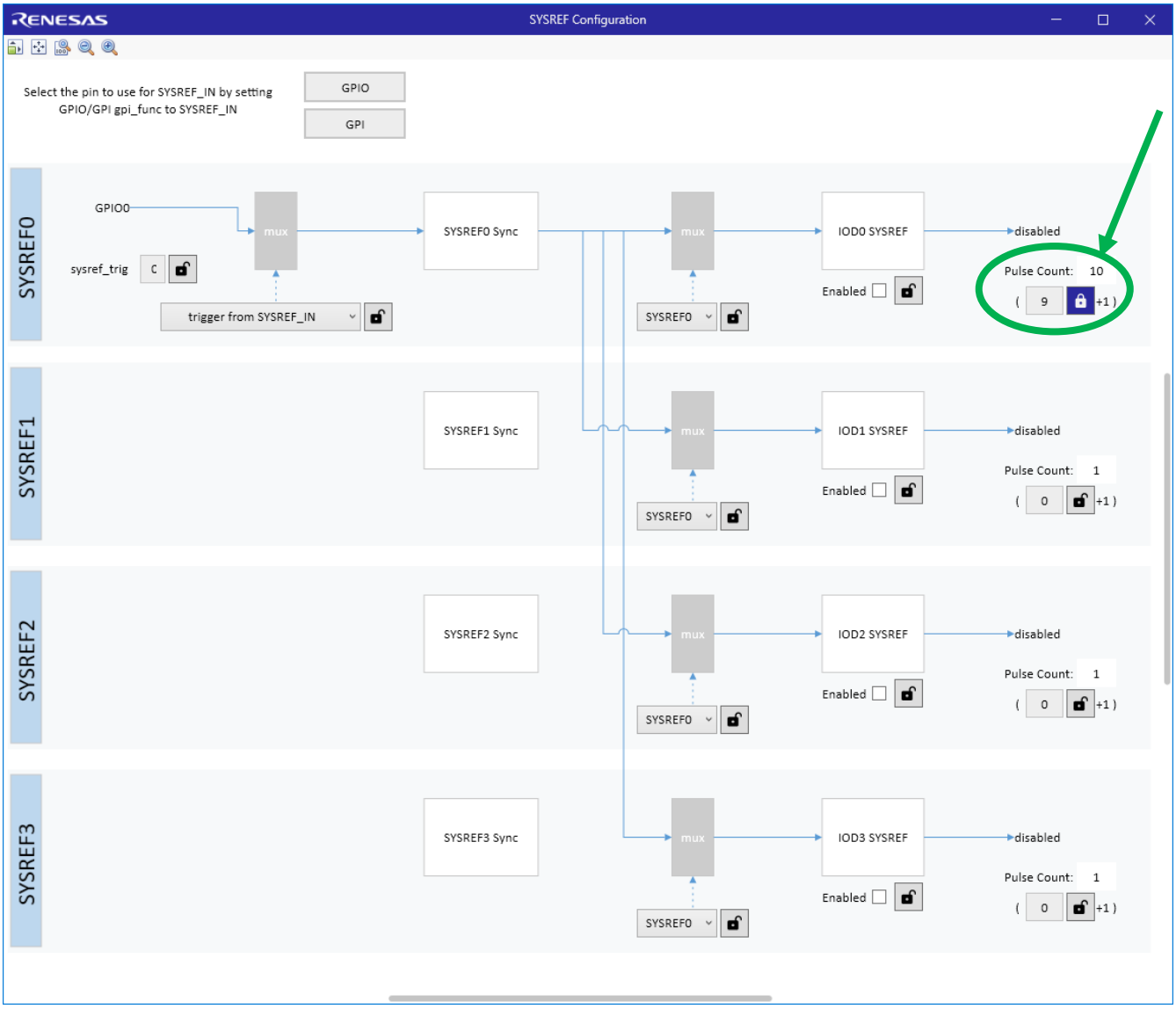

3. Click on the “function” pull-down list and select SYSREF_IN. RICBox will initially display a warning, but that will go away once SYSREF is enabled. Close the GPIO0 and GPIO windows.



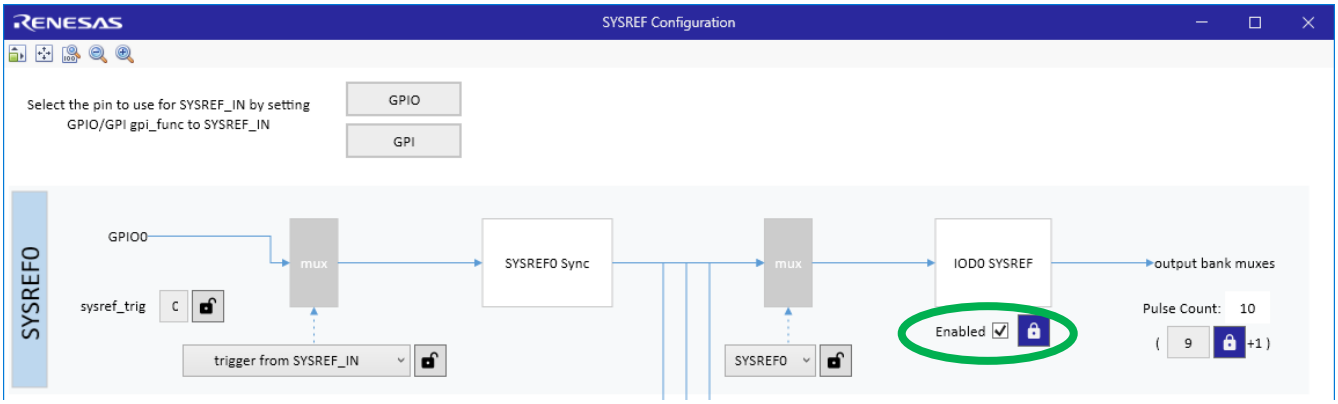
GPIO0 now appears in the SYSREF Configuration window for SYSREF0 channel. The reason GPIO0 is seen only in SYSREF0 channel is because the sysref_sync_src_sel field for all respective SYSREF channels are set to source from SYSREF0. For more information, see the register documentation in the RC31xxxA Programming Guide.



Depending on the SYSREF application, the next step is to set the number of pulses to generate. VC7 can support generating 1 to 256 pulses. To set the pulse count, enter the desired value in the “Pulse Count” (sysref_pulse_cnt) field. Note that the value entered will result in value + 1 pulses.




The final step is to enable SYSREF. Select the “Enabled” check box. The SYSREF pulses will generate from IOD0 when GPIO0 transitions from ‘0’ to ‘1’. Additional pulses will generate with additional GPIO0 toggles.



# 4. Revision History

| Revision | Date | Description |
|---|---|---|
| 1.00 | Feb 2, 2022 | Initial release. |

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