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H8/300H Tiny Series

Using Timer V Overflow to Increment 8-Bit Counter

Introduction

Timer V overflow is used to increment an 8-bit counter in RAM.

Target Device

H8/3664

Contents

1. Specifications

1. The overflow of timer V is used to increment an 8-bit counter in RAM.
2. A timer V interrupt is generated when timer counter V (TCNTV) overflows, and the counter in RAM is incremented or initialized during the timer V interrupt handling.
3. The 8-bit counter in RAM starts from the initial value of H'0x00. When the counter's value becomes H'0xFF, it is initialized to H'0x00 and incrementation resumes.
4. A timer V interrupt is set to be generated every 2.048 ms.

2. Description of Functions Used

1. In this sample task, the 8-bit counter is incremented by the timer V overflow. Figure 2.1 is a block diagram of timer V. The elements of the block diagram are described below.

- The system clock (ϕ) is a 16-MHz clock that is used as a reference clock for operating the CPU and peripheral functions.
- Prescaler S (PSS) is a 13-bit counter with clock input of ϕ and is incremented every cycle.
- Timer control register V0 (TCRV0) selects the TCNTV input clock, specifies clearing of the TCNTV, and enables various interrupt requests. In this sample task, the TCNTV input clock is specified as ϕ/128, the TCNTV is specified not be cleared, and an overflow interrupt is enabled.
- Timer control/status register V (TCSRV) is an 8-bit register that sets the compare match flag and timer overflow flag, and controls the compare match output. In this sample task, the TMOV pin output is disabled.
- Timer counter V (TCNTV) is an 8-bit readable/writable up-counter that is incremented by internal or external clock input. The clock to be input can be selected from six clocks generated by dividing ϕ or three external clocks.
- Timer control register V1 (TCRV1), in combination with TCRV0, selects the input clock for TCNTV.

The TCNTV's overflow cycle in this sample task is calculated by the following equation:

$$\text{TCNTV overflow cycle} = \frac{1}{\text{System clock}/\ 128} \times 256 = 2.048\ \text{ms}$$

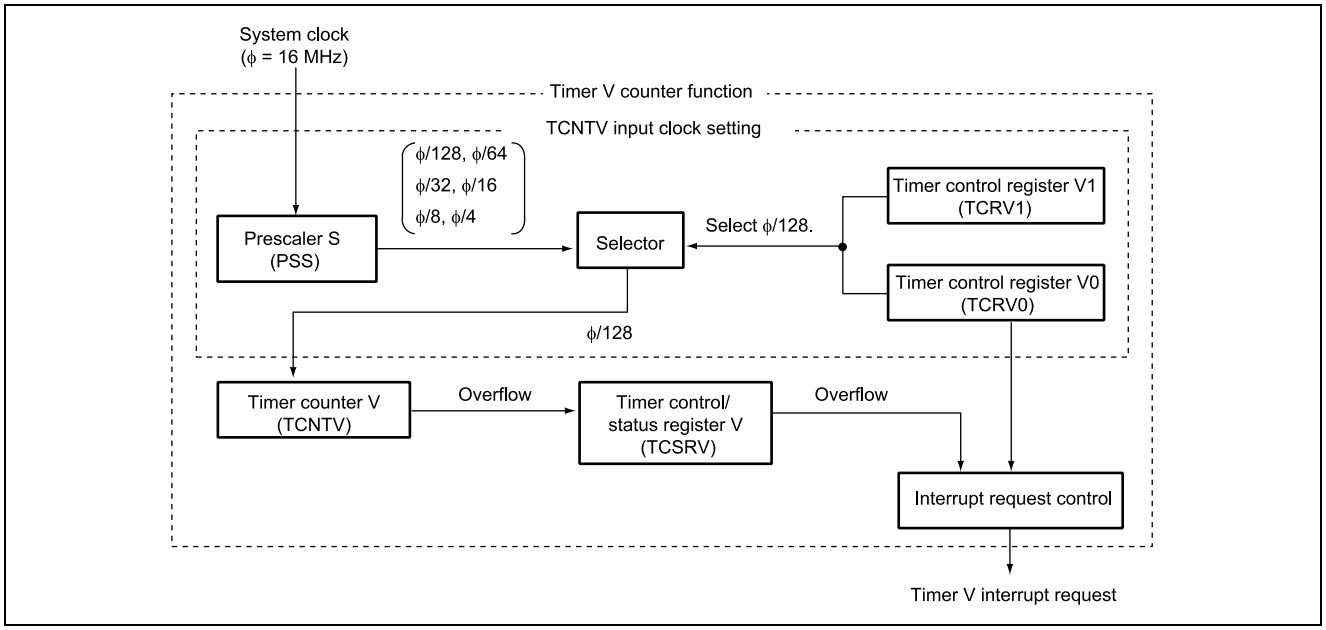


Figure 2.1 Timer V Block Diagram

2. Table 1 lists the function allocation for this sample task. The functions listed in table 2.1 are allocated so that the 8-bit counter is incremented by the timer V overflow.

Table 2.1 Function Allocation

Function	Description
PSS	13-bit counter with system clock input
TCRV1, TCRV0	Enables overflow interrupt requests. Specifies the input clock for TCNTV as ϕ/128.
TCNTV	8-bit up-counter with clock input of ϕ/128
TCSRV	Timer V overflow interrupt flag

3. Description of Operations

Figure 3.1 shows this sample task's principle of operation. The hardware and software processing shown in this figure applies the timer V overflow to increment the 8-bit counter.

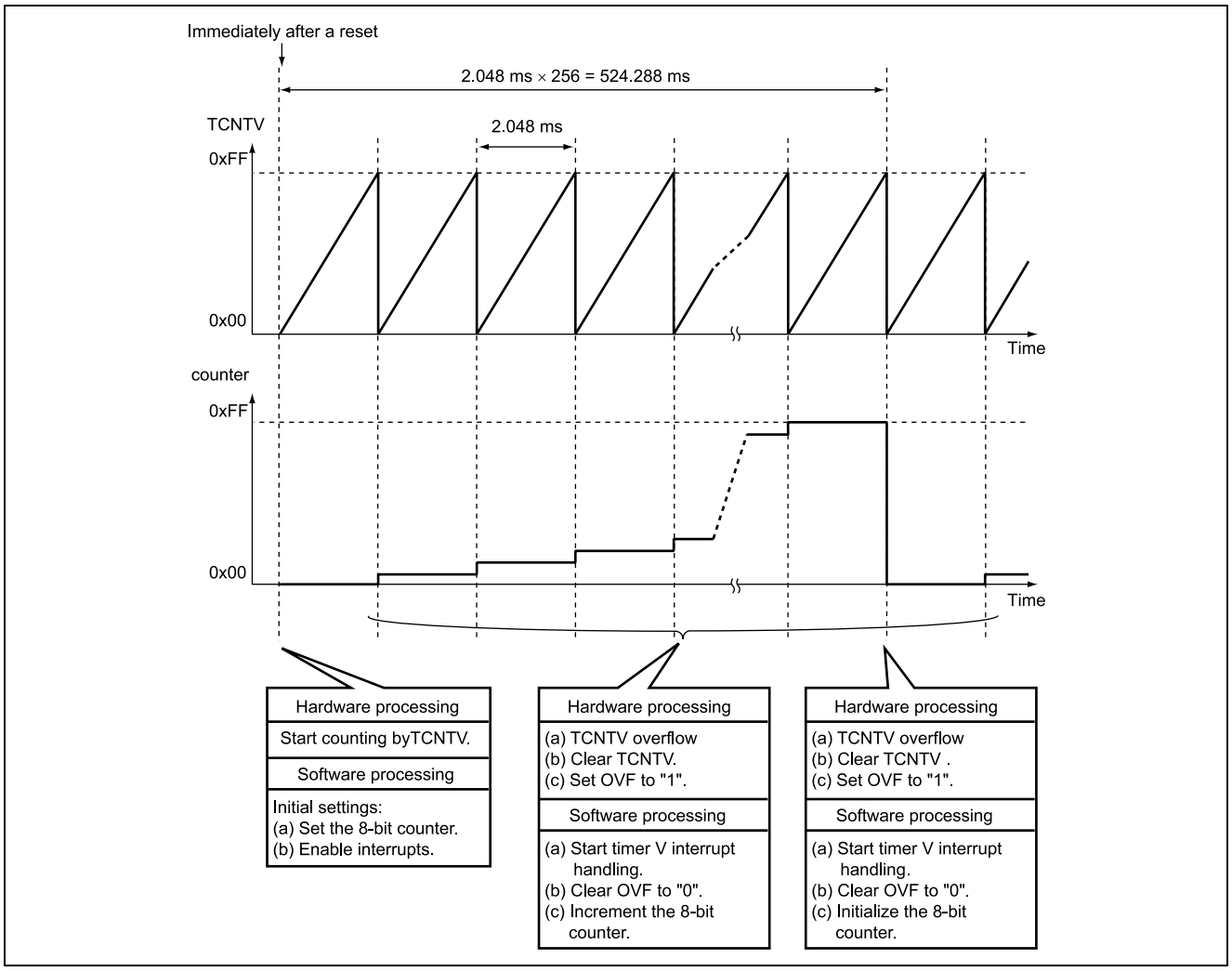


Figure 3.1 Operation Principle

4. Description of Software

4.1 Description of Modules

Table 4.1 describes the module used in this sample task.

Table 4.1 Description of Modules

Module Name	Label Name	Function
Main routine	main	Sets the 8-bit counter and enables interrupts.
Count up	tvint	This is the timer V interrupt handling routine that increments or initializes the 8-bit counter (counter).

4.2 Description of Arguments

This sample task uses no arguments.

4.3 Description of Internal Registers

The internal registers used in this sample task are described below.

- TCRV0 Timer control register V0 Address: 0xFFA0

Bit	Bit Name	Setting	Function
5	OVIE	1	Timer overflow interrupt enable OVIE = 0: Disables overflow (OVF) interrupt requests. OVIE = 1: Enables overflow (OVF) interrupt requests.
2	CKS2	CKS2 = 0	Clock select
1	CKS1	CKS1 = 1	CKS2 = 0, CKS1 = 1, CKS0 = 1:
0	CKS0	CKS0 = 1	TCNTV is incremented at the falling edge of internal clock ϕ/128.

- TCSRV Timer control/status register V Address: 0xFFA1

Bit	Bit Name	Setting	Function
5	OVF	1	Overflow flag OVF = 0: Indicates that no overflow has occurred. OVF = 1: Indicates that an overflow has occurred.

- TCNTV Timer counter V Address: 0xFFA4
  Function: An 8-bit up-counter that is incremented by the falling edge of internal clock ϕ/128.
  Setting: 0x00

- TCRV1 Timer control register V1 Address: 0xFFF5

Bit	Bit Name	Setting	Function
4	TVEG1	TVEG1 = 0	TVEG1 = 0, TVEG0 = 0: Disables the TRGV pin trigger input.
3	TVEG0	TVEG0 = 0	
2	TRGE	0	TRGE = 0: Disables the TCNTV count-up start by the TRGV pin input and the TCNTV count-up stop when the TCNTV is cleared upon a compare-match. TRGE = 1: Enables the TCNTV count-up start by the TRGV pin input and the TCNTV count-up stop when the TCNTV is cleared upon a compare-match.
0	ICKS0	1	Internal clock select 0 ICKS0, in combination with the CKS2 to CSK0 bits of TCRV0, selects the TCNTV input clock as internal clock ϕ/128.

4.4 Description of RAM

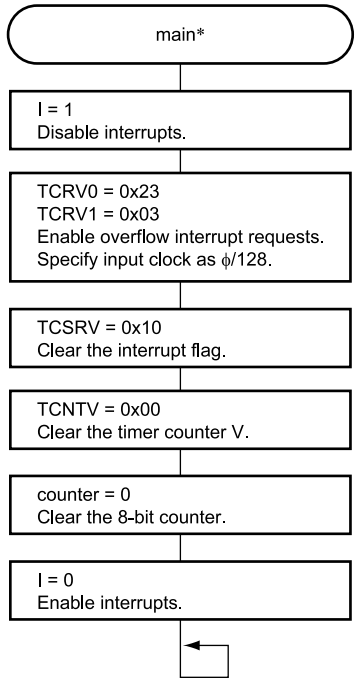
Table 4.2 describes the RAM used in this sample task.

Table 4.2 Description of RAM

Label Name	Function	Size	Used in
counter	8-bit counter	1 byte	Main routine Count up

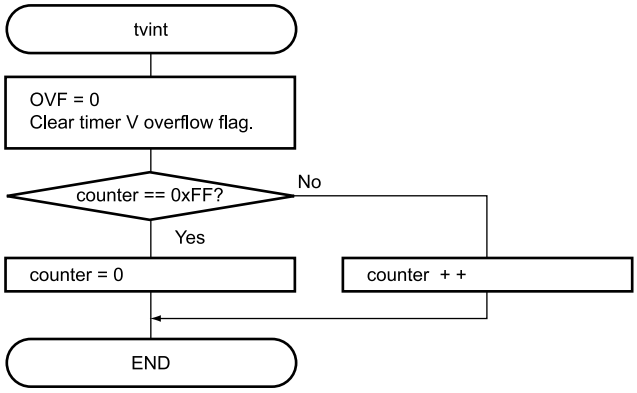
5. Flowchart

1. Main routine



Note: * The stack pointer is specified by INIT.SRC (assembly language).

2. Count up



6. Program Listing

```
/************************************************************************************************************************/
/*                                                                                                                      */
/*   H8/300HN Series -H8/3664-                                                                                          */
/*   Application Note                                                                                                   */
/*                                                                                                                      */
/*   '8-bit Counter Count-Up'                                                                                           */
/*                                                                                                                      */
/*   Function                                                                                                           */
/*   : Timer V Counter                                                                                                  */
/*                                                                                                                      */
/*   External Clock :    16MHz                                                                                          */
/*   Internal Clock :    16MHz                                                                                          */
/*   Sub Clock :         32.768kHz                                                                                      */
/*                                                                                                                      */
/************************************************************************************************************************/

#include    <machine.h>

/************************************************************************************************************************/
/*   Symbol Definition                                                                                                  */
/************************************************************************************************************************/
struct BIT {
     unsigned char   b7:1;         /* bit7 */
     unsigned char   b6:1;         /* bit6 */
     unsigned char   b5:1;         /* bit5 */
     unsigned char   b4:1;         /* bit4 */
     unsigned char   b3:1;         /* bit3 */
     unsigned char   b2:1;         /* bit2 */
     unsigned char   b1:1;         /* bit1 */
     unsigned char   b0:1;         /* bit0 */
};

#define        TCRV0          *(volatile unsigned char *)0xFFA0                /* Timer Control Register V0               */
#define        TCRV0_BIT      (*(struct BIT *)0xFFA0)                          /* Timer Control Register V0               */
#define        CMIEB          TCRV0_BIT.b7                                     /* Compare Match Interrupt Enable B        */
#define        CMIEA          TCRV0_BIT.b6                                     /* Compare Match Interrupt Enable A        */
#define        OVIE           TCRV0_BIT.b5                                     /* Timer Overflow Interrupt Enable         */
#define        CCLR1          TCRV0_BIT.b4                                     /* Counter Clear 1                         */
#define        CCLR0          TCRV0_BIT.b3                                     /* Counter Clear 0                         */
#define        CKS2           TCRV0_BIT.b2                                     /* Clock Select 2                          */
#define        CKS1           TCRV0_BIT.b1                                     /* Clock Select 1                          */
#define        CKS0           TCRV0_BIT.b0                                     /* Clock Select 0                          */
#define        TCSRV          *(volatile unsigned char *)0xFFA1                /* Timer Control/Status Register V         */
#define        TCSRV_BIT      (*(struct BIT *)0xFFA1)                          /* Timer Control/Status Register V         */
#define        CMFB           TCSRV_BIT.b7                                     /* Compare Match Flag B                    */
#define        CMFA           TCSRV_BIT.b6                                     /* Compare Match Flag A                    */
#define        OVF            TCSRV_BIT.b5                                     /* Timer Overflow Flag                     */
#define        OS3            TCSRV_BIT.b3                                     /* Output Select 3                         */
#define        OS2            TCSRV_BIT.b2                                     /* Output Select 2                         */
#define        OS1            TCSRV_BIT.b1                                     /* Output Select 1                         */
#define        OS0            TCSRV_BIT.b0                                     /* Output Select 0                         */
#define        TCORA          *(volatile unsigned char *)0xFFA2                /* Time constant register A                */
```

```
#define        TCORB          *(volatile unsigned char *)0xFFA3                  /* Time constant register B                */
#define        TCNTV          *(volatile unsigned char *)0xFFA4                  /* Timer counter V                         */
#define        TCRV1          *(volatile unsigned char *)0xFFA5                  /* Timer control register V1               */
#define        TCRV1_BIT      (*(struct BIT *)0xFFA5)                            /* Timer control register V1               */
#define        TVEG1          TCRV1_BIT.b4                                       /* TRGV Input Edge Select 1                */
#define        TVEG0          TCRV1_BIT.b3                                       /* TRGV Input Edge Select 0                */
#define        TRGE           TCRV1_BIT.b2                                       /* TCNTV starts counting up                */
#define        ICKS0          TCRV1_BIT.b0                                       /* Internal Clock Select 0                 */

#pragma interrupt   (tvint)

/************************************************************************************************************************/
/*   Function define                                                                                                    */
/************************************************************************************************************************/
extern void INIT ( void );                                                       /* SP Set                                  */
void main ( void );
void tvint ( void );

/************************************************************************************************************************/
/*   RAM define                                                                                                         */
/************************************************************************************************************************/
volatile unsigned char  counter;                                                 /* 8bit Counter                            */

/************************************************************************************************************************/
/*   Vector Address                                                                                                     */
/************************************************************************************************************************/
#pragma section     V1                                                           /* VECTOR SECTOIN SET                      */
void (*const VEC_TBL1[])(void) = {                                               /* 0x00 - 0x0f                             */
          INIT                                                                   /* 00 Reset                                */
};
#pragma section     V2                                                           /* VECTOR SECTOIN SET                      */
void (*const VEC_TBL2[])(void) = {
          tvint                                                                  /* 2C Timer V Interrupt                    */
};

#pragma section                                                                  /* P                                       */
/************************************************************************************************************************/
/*   Main Program                                                                                                       */
/************************************************************************************************************************/
void main ( void )
{
          set_imask_ccr(1);                                                      /* Interrupt Disable                       */

          TCRV0 = 0x23;                                                          /* TimerV Overflow Interrupt Enable        */
          TCRV1 = 0x03;                                                          /* Set phi/128                             */
          TCSRV = 0x10;                                                          /* Clear Interrupt Flag                    */
          TCNTV = 0x00;                                                          /* Clear TCNTV                             */

     counter = 0;                                                                /* Initialize 8bit Counter                 */
     set_imask_ccr(0);                                                           /* Interrupt Enable                        */

     while(1);
}
```

```
/*****************************************************************************************************************************************/
/*  Timer V Interrupt                                                                                                                    */
/*****************************************************************************************************************************************/
void tvint ( void )
{
          OVF = 0;                                                    /* Clear OVF                          */

          if(counter == 0xff)                                         /* 8bit Counter = 0xff?               */
               counter = 0;                                           /* Clear 8bit Counter                 */
          else
               counter++;                                             /* Increment 8bit Counter             */
}
```

Link address specifications

Section Name	Address
CV1	0x0000
CV2	0x002C
P	0x0100
B	0xFB80

Revision Record

		Description	
Rev.	Date	Page	Summary
1.00	Sep.29.03	—	First edition issued

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