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April 1st, 2010
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APPLICATION NOTE

Using Output Compare Function to Output Pulses with Different Phases

Introduction

Two pulses, each with a 50% duty cycle are output with an arbitrary phase difference by the output compare function of timer W, as shown in figure 1.1.

Target Device

H8/300H Tiny Series H8/3664

Contents

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1. Specifications

1. Two pulses, each with a 50% duty cycle are output with an arbitrary phase difference by the output compare function of timer W, as shown in figure 1.1.
2. Pulses with an arbitrary phase difference are output from the FTIOA and FTIOB pins.
3. The pulse cycle is set in general register A (GRA).
4. The phase difference between the pulse outputs from the FTIOA and FTIOB pins are set in general register B (GRB).
5. In this sample task, the pulses have 16.25-ms cycles and a phase difference of 3.125 ms.

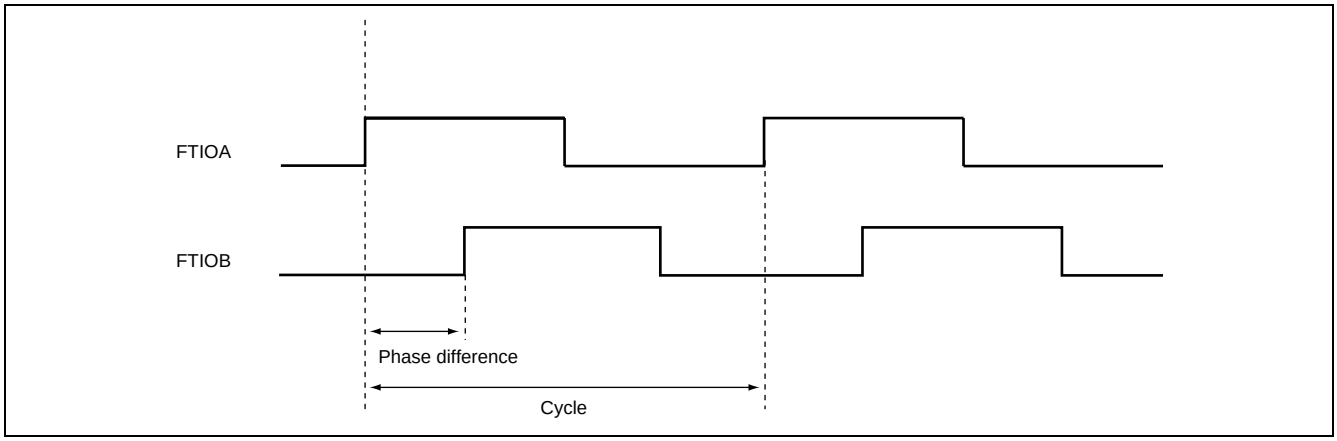

Figure 1.1 Timer W's Output Compare Function

2. Description of Functions Used

In this sample task, pulses are output with an arbitrary phase difference from the FTIOA and FTIOB pins by the output compare function of timer W.

Figure 2.1 is a block diagram of the output compare function of timer W. The elements of the block diagram are described below.

- The system clock (ϕ) is a 16-MHz OSC clock that is used as a reference clock for operating the CPU and peripheral functions.
- Prescaler S (PSS) is a 13-bit counter with clock input of ϕ. PSS is incremented every cycle.
- The timer counter (TCNT) is a 16-bit readable/writable up-counter that is incremented by internal or external clock input. The clock source can be selected from a total of four clocks: three clocks obtained by dividing the system clock by 2, 4, and 8, and an external clock. In this sample task, system clock/2 is selected as the TCNT input clock
- Timer control register W (TCRW) is an 8-bit readable/writable register that selects the TCNT input clock.
- Timer status register W (TSRW) is an 8-bit register that selects TCNT clearing, and controls TCNT interrupt request signals.
- Timer interrupt enable register W (TIERW) is an 8-bit readable/writable register that enables or disables each interrupt request.
- Timer mode register W (TMRW) is an 8-bit readable/writable register that starts and stops TCNT.
- Timer I/O control register 0 (TIOR0) is an 8-bit readable/writable register that sets the output compare registers and controls the output compare output.
- General register A (GRA) is a 16-bit readable/writable register that is compared with TCNT at all times. When the GRA and TCNT contents match, IMFA in TSRW is set to 1. If IMIEA in TIERW is set to 1 at this time, a CPU interrupt is requested. If IOA2 in TIORO is cleared to 0 when compare match A occurs, the level values set in IOA1 and IOA0 in TIORO are output to the FTIOA pin.
- General register B (GRB) is a 16-bit readable/writable register that is compared with TCNT at all times. When the GRB and TCNT contents match, IMFB in TSRW is set to 1. If IMIEB in TIERW is set to 1 at this time, a CPU interrupt is requested. If IOB2 in TIORO is cleared to 0 when compare match B occurs, the level values set in IOB1 and IOB0 in TIORO are output to the FTIOB pin.
- A pulse resulting from compare match A is output from the output compare A output (FTIOA) pin.
- A pulse resulting from compare match B is output from the output compare B output (FTIOB) pin.

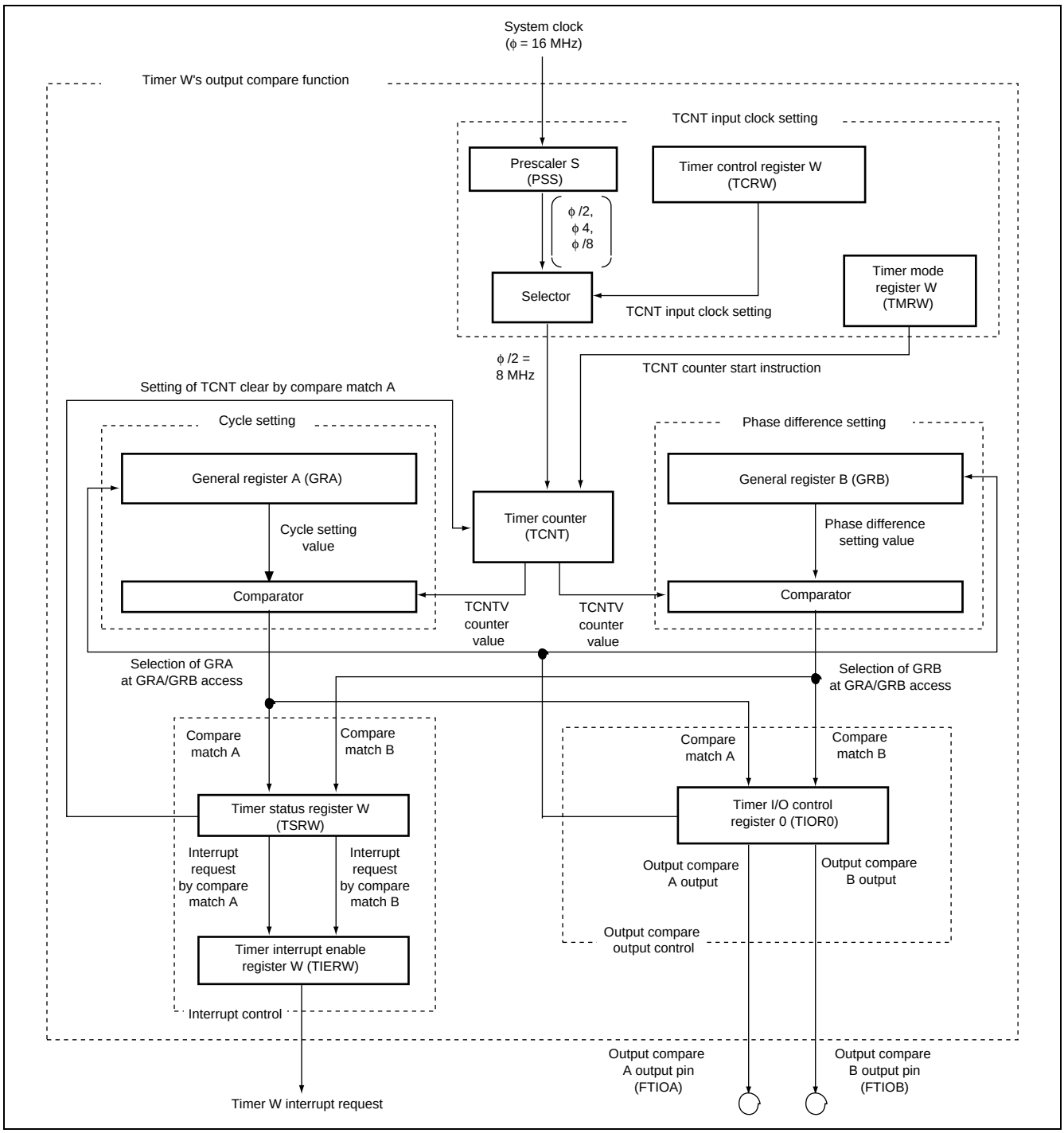

Figure 2.1 Timer W's Output Compare Function

Figure 2.2 shows how to set the cycle for the output pulses, and the phase difference between them.

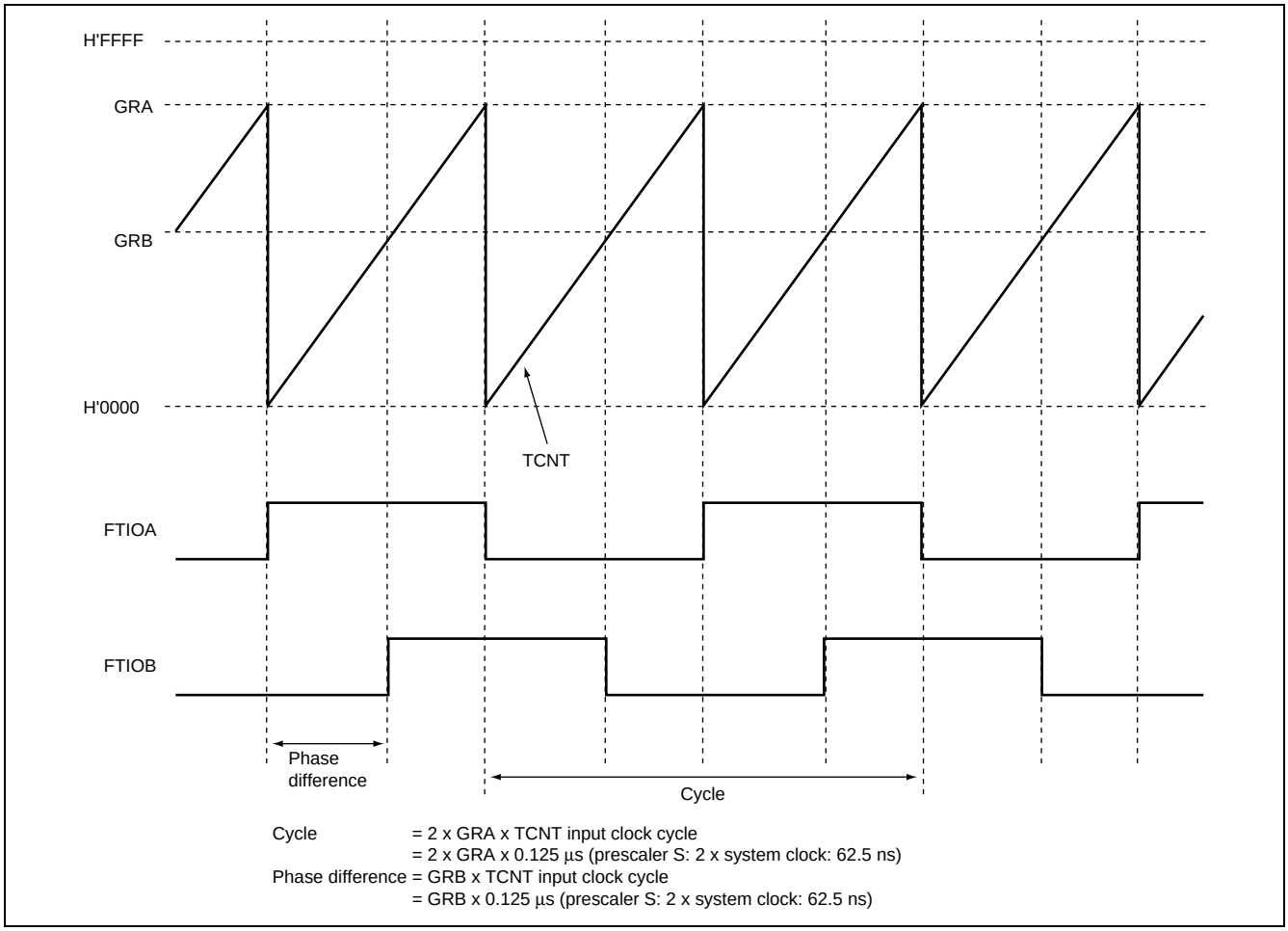

Figure 2.2 Setting of Cycle and Phase Difference for Output Pulses

Table 2.1 lists the function allocation for this sample task. The functions listed in table 2.1 are allocated so that pulses with an arbitrary phase difference are output by the output compare function of timer W.

Table 2.1 Function Allocation

Function	Description
PSS	13-bit counter with system clock input
TIERW	Enables interrupt requests by compare match A and compare match B
TSRW	Controls signals of interrupt requests by compare match A and compare match B, and enables TCNT clearing by compare match A
TCNT	16-bit up-counter incremented by clock input of system clock/2
GRA	Sets cycle of output pulses, and compare match A occurs when its contents match the TCNT contents
GRB	Sets phase difference between output pulses, and compare match B occurs when its contents match the TCNT contents
TCRW	Sets TCNT input clock
TMRW	Starts TCNT count
TIORO	Sets output compare registers and controls output compare output
FTIOA	Output pin for compare match A pulse
FTIOB	Output pin for compare match B pulse

3. Description of Operations

Figure 3.1 shows this sample task's principle of operation. The hardware and software processing shown in figure 3.1 applies the output compare function of timer W to output pulses with an arbitrary phase difference.

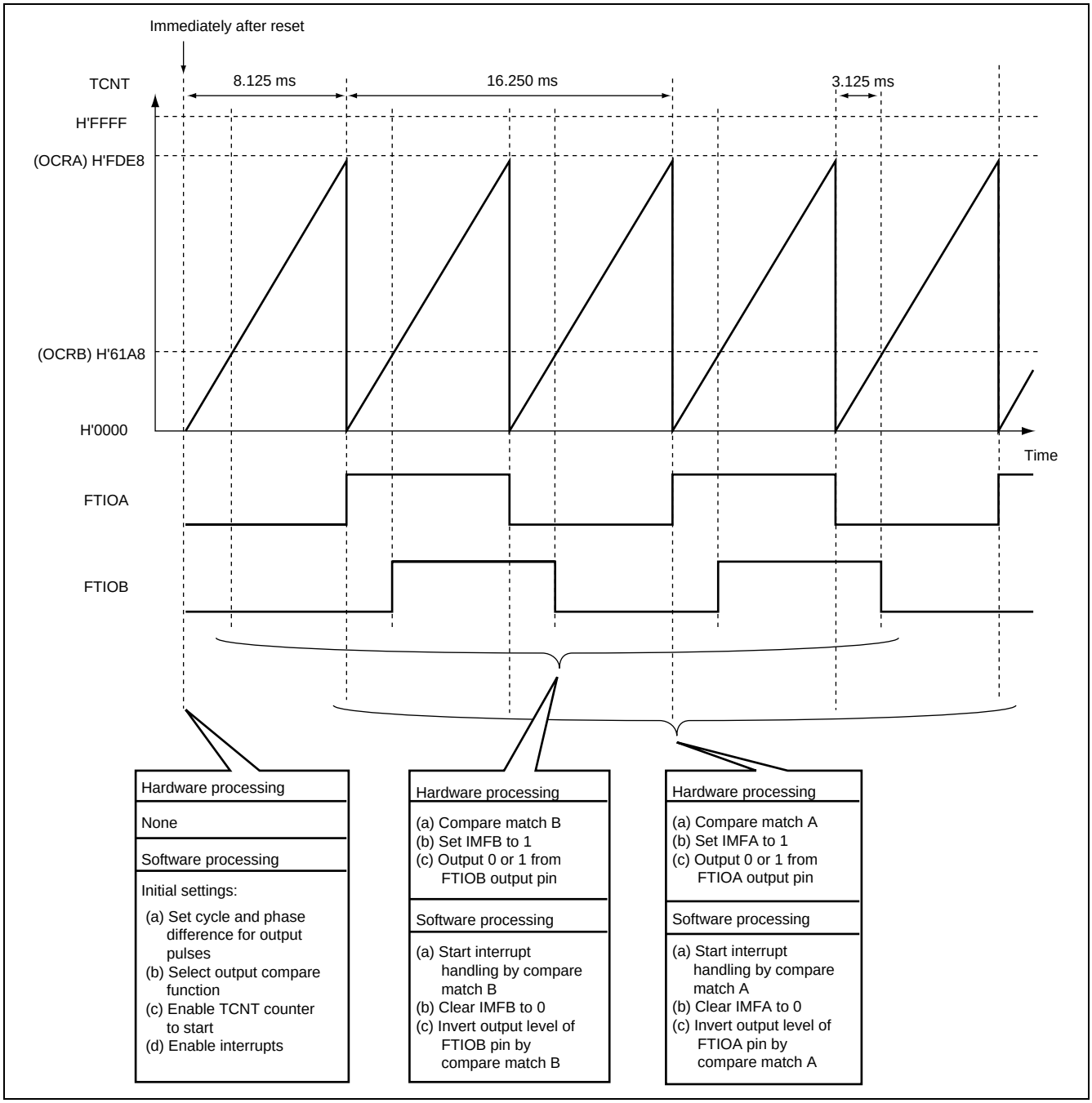

Figure 3.1 Operation Principle: Using Output Compare Function of Timer W to Output Pulses with Arbitrary Phase Difference

4. Description of Software

4.1 Description of Modules

Table 4.1 describes the software used in this sample task.

Table 4.1 Description of Modules

Module Name	Label Name	Function
Main routine	main	Selects the compare match function and enables interrupts.
Control of output compare output	twint	During the timer W interrupt handling routine, judges whether or not the interrupt request is by IMFA or IMFB, and inverts the output level of FTIOA or FTIOB according to the interrupt request type.

4.2 Description of Arguments

No arguments are used in this sample task.

4.3 Description of Internal Registers

Table 4.2 describes the internal registers used in this sample task.

Table 4.2 Description of Internal Registers

Register Name		Function	Address	Setting
TMRW	CTS	Timer mode register W (timer counter start):	H'FF80	
		When CTS is set to 1, TCNT starts.	Bit 7	1
		When CTS is cleared to 0, TCNT stops.		
TCRW	CCLR	Timer control register W (counter clear):	H'FF81	
		When CCLR is set to 1, TCNT clearing by compare match A is enabled.	Bit 7	1
		Timer control register W (clock select 2 to 0):	H'FF81	
	CKS2	When CKS2 and CKS1 are cleared to 0, and CKS0 is set to 1, the TCNT input clock is set to system clock/2.	Bit 6	CKS2 = 0
	CKS1		Bit 5	CKS1 = 0
	CKS0		Bit 4	CKS0 = 1
	TOB	Timer control register W (timer output level B):	H'FF81	
		When TOB is set to 1, the pulse level output to the FTIOB pin is high until compare match B occurs.	Bit 1	0
		When TOB is cleared to 0, the pulse level output to the FTIOB pin is low until compare match B occurs.		
	TOA	Timer control register W (timer output level A):	H'FF81	
		When TOA is set to 1, the pulse level output to the FTIOA pin is high until compare match A occurs.	Bit 0	0
		When TOA is cleared to 0, the pulse level output to the FTIOA pin is low until compare match A occurs.		

Table 4.2 Description of Internal Registers (cont)

Register Name		Function	Address	Setting
TIERW	IMIEB	Timer interrupt enable register W (output compare interrupt B enable): When IMIEB is set to 1, IMFB interrupt requests are enabled.	H'FF82 Bit 1	1
	IMIEA	Timer interrupt enable register W (output compare interrupt A enable): When IMIEA is set to 1, IMFA interrupt requests are enabled.	H'FF82 Bit 0	1
TSRW	IMFB	Timer status register W (output compare flag B): When IMFB is cleared to 0, a compare match between TCNT and GRB has not occurred. When IMFB is set to 1, a compare match between TCNT and GRB has occurred.	H'FF83 Bit 1	0
	IMFA	Timer status register W (output compare flag A): When IMFA is cleared to 0, a compare match between TCNT and GRA has not occurred. When IMFA is set to 1, a compare match between TCNT and GRA has occurred.	H'FF83 Bit 0	0
TIORO	IOB2	Timer I/O control register 0 (I/O control B2): When IOB2 is cleared to 0, this register functions as an output compare B register.	H'FF84 Bit 6	0
		Timer I/O control register 0 (I/O control B1 and B0):	H'FF84	
	IOB1	When IOB1 is set to 1, FTIOB pin output is toggled by compare match B.	Bit 5	IOB1 = 1
	IOB0	When IOB0 is set to 1, FTIOB pin output is toggled by compare match B.	Bit 4	IOB0 = 1
	IOA2	Timer I/O control register 0 (I/O control A2): When IOA2 is cleared to 0, this register functions as an output compare A register.	H'FF84 Bit 2	0
		Timer I/O control register 0 (I/O control A1 and A0):	H'FF84	
	IOA1	When IOA1 is set to 1, FTIOA pin output is toggled by compare match A.	Bit 1	IOA1 = 1
	IOA0	When IOA0 is set to 1, FTIOA pin output is toggled by compare match A.	Bit 0	IOBA = 1
TCNT		Timer counter: 16-bit up-counter incremented by clock input of system clock/2.	H'FF86	H'7530
GRA		General register A: When the GRA value matches the TCNT value, compare match A occurs.	H'FF88	H'FDE8
GRB		General register B: When the GRB value matches the TCNT value, compare match B occurs.	H'FF8A	H'61A8

4.4 Description of RAM

RAM is not used in this sample task.

5. Flowcharts

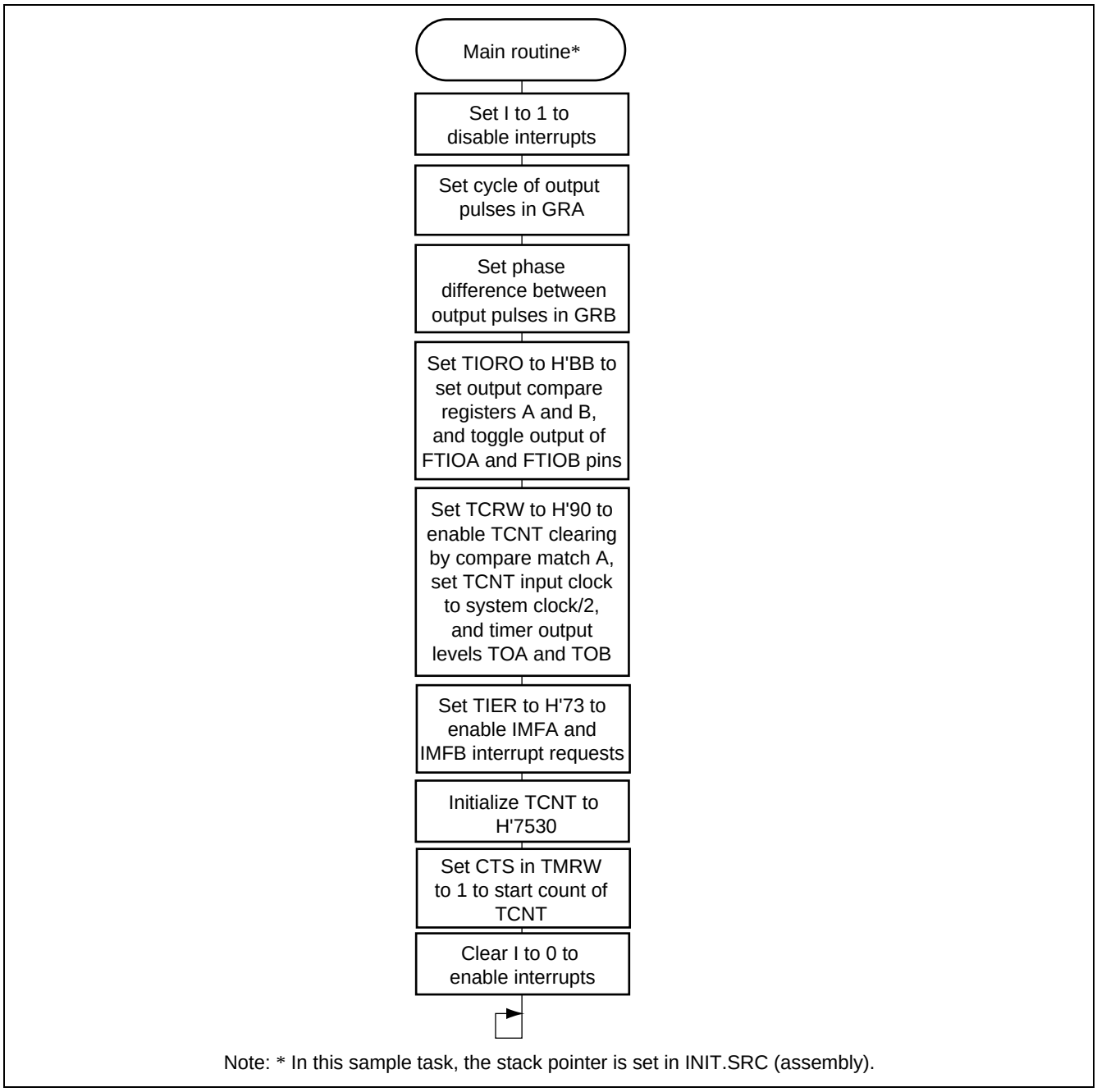

Figure 5.1 Flowchart for Main Routine

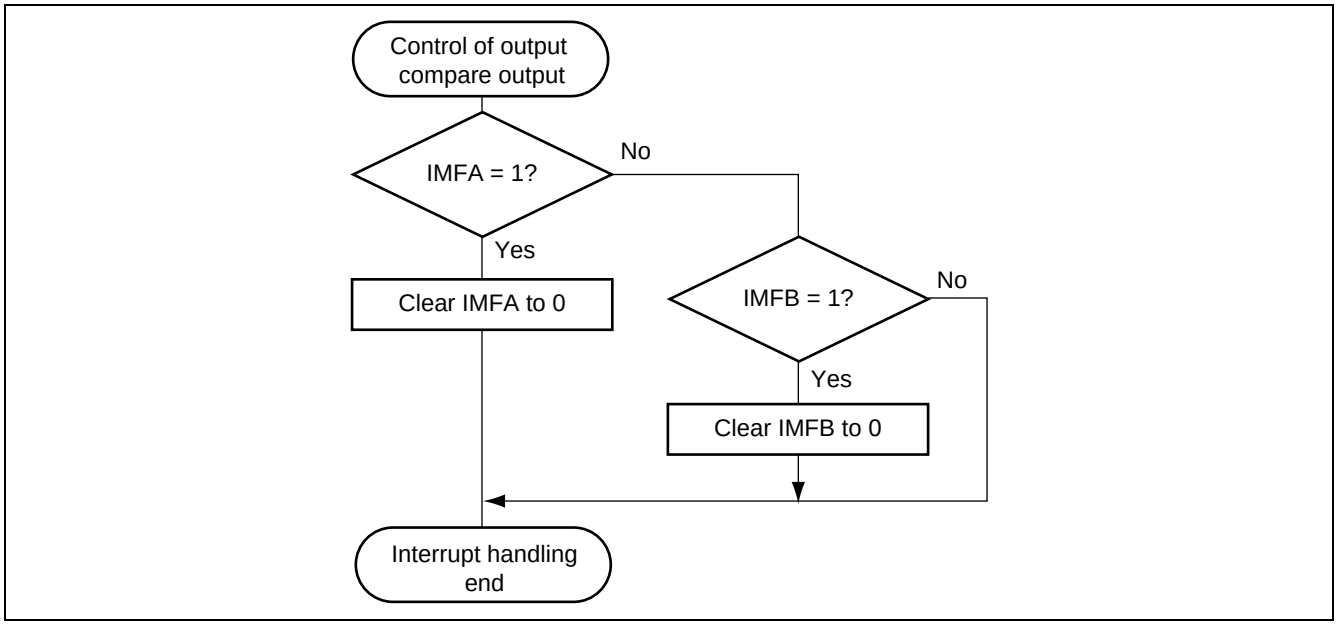

Figure 5.2 Flowchart for Timer W Interrupt Handling Routine

6. Program Listing

INIT.SRC (Program listing)

```
      .EXPORT  _INIT
      .IMPORT  _main
 ;
      .SECTION    P,CODE
 _INIT:
     MOV.W    #H'FF80,R7
     LDC.B    #B'10000000,CCR
     JMP      @_main
 ;
        .END
```

```
/************************************************************/
/*                                                          */
/*    H8/300H Tiny Series -H8/3664-                         */
/*    Application Note                                      */
/*                                                          */
/*    'Pulse Output of Random Phase Difference by           */
/*     Output Compare Function'                             */
/*                                                          */
/*    Function                                              */
/*    : Timer W Output Compare                              */
/*                                                          */
/*    External Clock : 16MHz                                */
/*    Internal Clock : 16MHz                                */
/*    Sub Clock      : 32.768kHz                            */
/*                                                          */
/************************************************************/

#include    <machine.h>

/************************************************************/
/*    Symbol Defnition                                      */
/************************************************************/
struct BIT {
    unsigned char    b7:1;      /* bit7 */
    unsigned char    b6:1;      /* bit6 */
```

```
    unsigned char    b5:1;      /* bit5 */
    unsigned char    b4:1;      /* bit4 */
    unsigned char    b3:1;      /* bit3 */
    unsigned char    b2:1;      /* bit2 */
    unsigned char    b1:1;      /* bit1 */
    unsigned char    b0:1;      /* bit0 */
};

#define        TMRW        *(volatile unsigned char *)0xFF80   /* Timer Mode     Register W         */
#define        TCRW        *(volatile unsigned char *)0xFF81   /* Timer Control Register W          */
#define        TCRW_BIT    (*(struct BIT *)0xFF81)             /* Timer Control Register W          */
#define        CCLR        TCRW_BIT.b7                         /* Counter Clear A                   */
#define        CKS1        TCRW_BIT.b5                         /* Clock Select 1                    */
#define        CKS0        TCRW_BIT.b4                         /* Clock Select 0                    */
#define        TOB         TCRW_BIT.b1                         /* Timer Output Level B              */
#define        TOA         TCRW_BIT.b0                         /* Timer Output Level A              */
#define        TIERW       *(volatile unsigned char *)0xFF82   /* Timer Interrupt Enable Register   */
#define        TIERW_BIT   (*(struct BIT *)0xFF82)             /* Timer Interrupt Enable Register   */
#define        OVIE        TIERW_BIT.b7                        /* Timer Overflow Interrupt Enable   */
#define        IMIEB       TIERW_BIT.b1                        /* Output Compare Interrupt B Enable */
#define        IMIEA       TIERW_BIT.b0                        /* Output Compare Interrupt A Enable */
#define        TSRW        *(volatile unsigned char *)0xFF83   /* Timer Status Register W           */
#define        TSRW_BIT    (*(struct BIT *)0xFF83)             /* Timer Status Register W           */
#define        OVF         TSRW_BIT.b7                         /* Timer Over flow                   */
#define        IMFB        TSRW_BIT.b1                         /* Output Compare Flag B             */
#define        IMFA        TSRW_BIT.b0                         /* Output Compare Flag A             */
#define        TIOR0       *(volatile unsigned char *)0xFF84   /* Timer I/O Control Register 0      */
#define        TIOR0_BIT   (*(struct BIT *)0xFF84)             /* Timer I/O Control Register 0      */
#define        IOB2        TIOR0_BIT.b6                        /* I/O Control Register B2           */
#define        IOB1        TIOR0_BIT.b5                        /* I/O Control Register B1           */
#define        IOB0        TIOR0_BIT.b4                        /* I/O Control Register B0           */
#define        IOA2        TIOR0_BIT.b2                        /* I/O Control Register A2           */
#define        IOA1        TIOR0_BIT.b1                        /* I/O Control Register A1           */
#define        IOA0        TIOR0_BIT.b0                        /* I/O Control Register A0           */
#define        TCNT        *(volatile unsigned int *)0xFF86    /* Time Counter                      */
#define        GRA         *(volatile unsigned int *)0xFF88    /* General Register A                */
#define        GRB         *(volatile unsigned int *)0xFF8A    /* General Register B                */

#pragma        interrupt    (twint)
```

```
/************************************************************/
/*     Function Definition                                  */
/************************************************************/
extern    void    INIT ( void );                             /* SP Set                              */
void      main     ( void );
void      twint    ( void );

/************************************************************/
/*    Vector Address                                        */
/************************************************************/
#pragma    section        V1                                /* VECTOR SECTOIN SET                  */
void (*const VEC_TBL1[])(void) = {
/* 0x00 - 0x0f */
    INIT                                                    /* 00 Reset                             */
};
#pragma    section        V2                                /* VECTOR SECTOIN SET                   */
void (*const VEC_TBL2[])(void) = {
    twint                                                   /* 2A Timer W Interrupt                 */
};
#pragma    section                                          /* P                                    */
/************************************************************/
/*    Main Program                                          */
/************************************************************/
void main ( void )
{
    set_imask_ccr(1);                                       /* Interrupt Disable                     */

    GRA = 0xFDE8;                                           /* Initialize GRA                        */
    GRB = 0x61A8;                                           /* Initialize GRB                        */

    TIOR0 = 0xBB;                                           /* Initialize Output Compare Function    */
    TCRW = 0x90;                                            /* Initialize TCNT Input Clock Period    */
    TIERW = 0x73;                                           /* Initialize IMIEA/IMIEB Interrupt Enable */

    TCNT = 0x7530;                                          /* Initialize TCNT                       */
    TMRW = 0xC8;                                            /* Initialize timer Mode Register        */

    set_imask_ccr(0);                                       /* Interrupt Enable                      */
```

```
    while(1)    {
       ;
    }

}
/*********************************************************/
/*    Timer W Interrupt                                  */
/*********************************************************/
void twint ( void )
{

    if ( IMFA == 1 ){                                   /* IMFA = "1" ?                */
        IMFA = 0;                                       /* Clear IMFA                  */
    }
    else{
        if( IMFB == 1 ){                                /* IMFB = "1" ?                */
            IMFB = 0;                                   /* Clear IMFB                  */
        }
    }
}
```

Link Address Setting:

Section Name	Address
CV1	H'0000
CV2	H'002A
P	H'0100