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H8/300H Super Low Power Series

Using Input-Capture Function of Timer G to Measure Pulse Period

Introduction

The period of a pulse input to Input Capture Input Pin (TMIG) is measured by using the Timer G input capture function. The maximum pulse period that can be measured is 1.638 ms and the measurement is accurate to within 6.4 µs.

Target Device

H8/38099

Contents

1. Specifications

1. The period of a pulse input to Input Capture Input Pin (TMIG) is measured using the Timer G input capture function.
2. The counter value of Timer Counter G (TCG) between rising edges of an input pulse is counted and the period of an input pulse is measured based on this counter value.
3. The maximum pulse period that can be measured is 1.638 ms and the measurement accuracy is 6.4 µs.

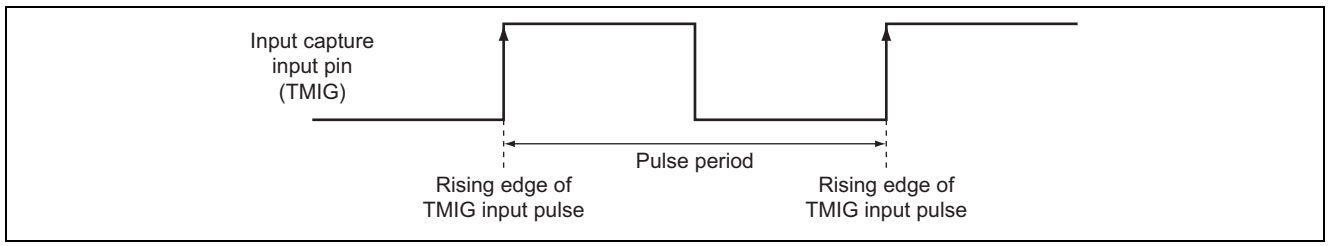


Figure 1 Measurement of Input Pulse Period

2. Description of Functions Used

2.1 Block Diagram of Timer G

Figure 2 shows the block diagram of the Timer G input capture function

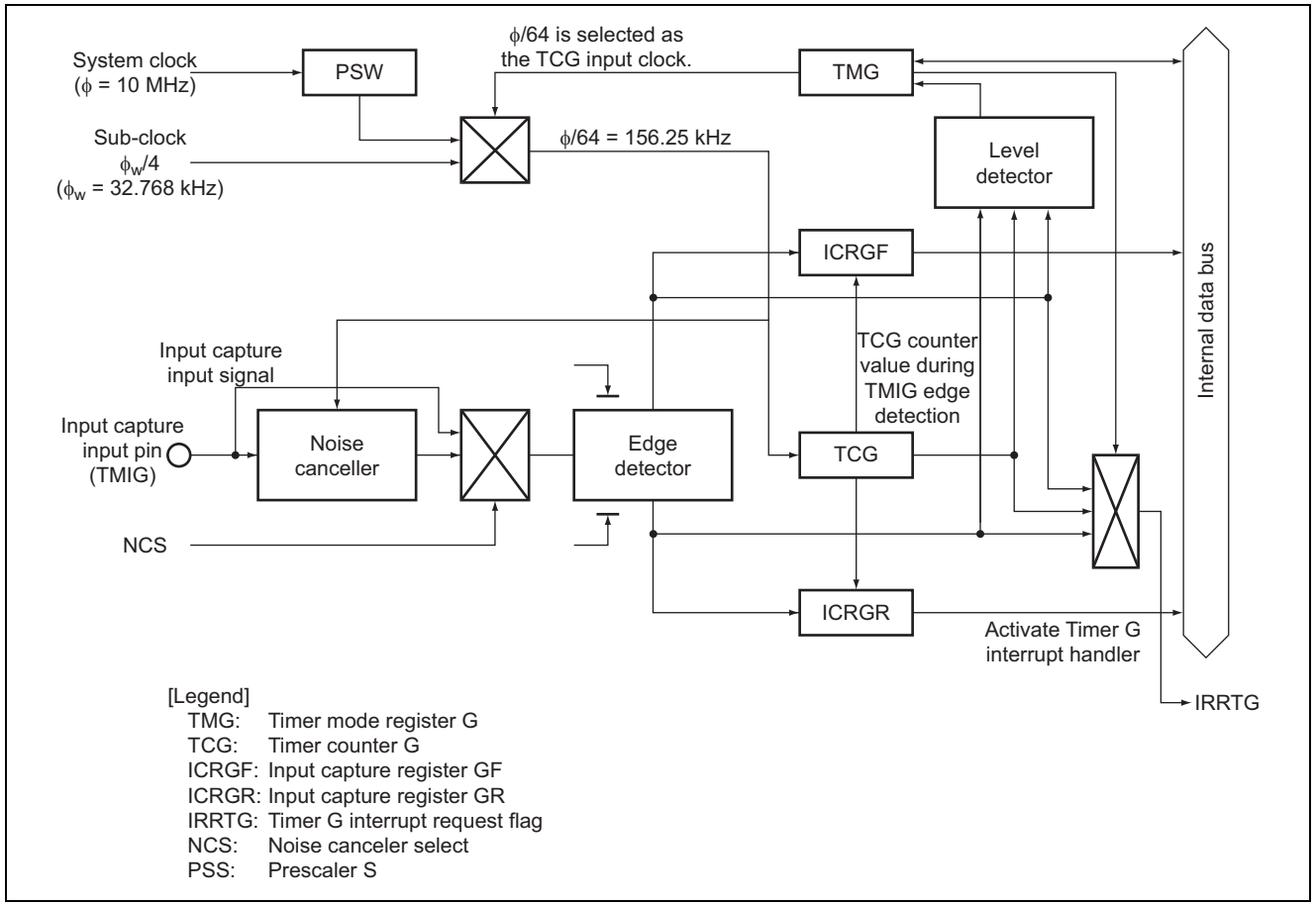


Figure 2 Block Diagram of Timer G Input Capture Function

2.2 Functions Used

2.2.1 Description of Functions

In this sample task, the period of pulses input to Input Capture Input Pin (TMIG) is measured using the Timer G input capture function. Details of the bits of the individual registers will be explained in 4.3, “Internal Registers”.

- The system clock (ϕ)
  The system clock (ϕ) is a 10-MHz system clock and is a reference clock to operate the CPU and its peripheral functions.
- The prescaler S (PSS)
  The prescaler S (PSS) is a 17-bit counter using ϕ as input and is counted up every cycle.
- The Port Mode Register F (PMRF)
  The Port Mode Register F (PMRF) controls the selection of the pin function on port F. Setting the TMIG bit in PMRF to 1 selects operation of pin PF0 as the TMIG input pin and operation of Timer G as an input capture timer.
- The Timer Counter G (TCG)
  The Timer Counter G (TCG) is an 8-bit up-counter which is incremented by clock input. The input clock is selected by bits CKS1 and CKS0 in TMG. TMIG in PMRF is set to 1 to operate TCG as an input capture timer. In input capture timer operation, the TCG value can be cleared by the rising edge, falling edge, or both edges of the input capture input signal, according to the setting made in TMG. When TCG overflows from H'FF to H'00, when OVIE in TMG is 1, IRRTG in IRR2 is set to 1, and when IENTG in IENR2 is 1, an interrupt request is sent to the CPU. TCG cannot be read or written by the CPU. It is initialized to H'00 upon reset.
- The Input Capture Register GR (ICRGR)
  The Input Capture Register GR (ICRGR) is an 8-bit read-only register. When a rising edge of the input signal is detected, the current TCG value is transferred to ICRGR. When IIEGS in TMG is 0 at this time, IRRTG in IRR2 is set to 1, and when IENTG in IENR2 is 1, an interrupt request is sent to the CPU. To ensure dependable input capture operation, the pulse width of the input capture input signal must be at least 2ϕ or $2\phi_{sub}$ (when the noise canceller is not used). ICRGF is initialized to H'00 upon reset.
- Timer Mode Register G (TMG)
  Timer Mode Register G (TMG) is an 8-bit read/write register. It selects 4 types of TCG internal clocks, counter clearing, and the interrupt request edge of input capture input signal, and controls enable/disable of overflow interrupt request, and indicates the overflow flag. TMG is initialized to H'00 upon reset.
- A pulse, whose frequency is subject to measurement, is input through Input Capture Input Pin (TMIG).

2.2.2 Calculation of Input Pulse Periods

The method to calculate input pulse periods in this sample task is shown below. Pulse periods cannot be measured accurately when the TCG overflows. Input pulse period must be therefore shorter than the TCG overflow period (1.638 ms).

- The following are defined in the user RAM area: PRDHL, for storage of the TCG value that is transferred to the Input Capture Register GR (ICRGR) on detection of a rising edge of the input pulse; the SRTF flag, which indicates whether or not an interrupt is the second to be generated by rising edges of the input pulse, and the ENDF flag, which indicates whether or not the measurement is complete.
- Capture of the rising edge of the first input pulse drives clearing of the TCG counter value.
- Capture of the rising edge of the second input pulse drives transfer of the ICRGR value, which has been transferred from TCG, to PRDHL.
- The following formula (1) provides the input pulse period.

  Input pulse period
  = (TCG counter value stored in PRDHL) × (TCG input clock period)
  = (TCG counter value stored in PRDHL) × 6.4 μs (1/(ϕ: 10 MHz/PSS: 64)) ..... (1)

- When the TCG overflows after the first rising edge of the input pulse is captured, the value of H'FF is stored in PDRHL.

2.2.3 Watchdog Timer Function

H8/38099 incorporates a watchdog timer (WDT) that is turned on by default after a reset. The WDT is an 8-bit timer that can generate an internal reset signal when the timer counter overflows because a system crash has prevented the CPU from writing to it. In this sample task, the WDT function is not used, so it is turned off.

- Timer Control/Status Register WD1 (TCSRWD1)
  Timer Control/Status Register WD1 (TCSRWD1) performs TCSRWD1 and TCWD write control. TCSRWD1 also controls the watchdog timer operation and indicates the operating state. TCSRWD1 must be rewritten by using the MOV instruction. Bit-manipulation instructions cannot be used to change the setting.

2.3 Assignment of Functions

Table 1 lists the assignment of functions applicable to this sample task. The functions are assigned as indicated in table 1, and frequencies are measured by the Timer G input capture function.

Table 1 Assignment of Functions

Function	Assignment of Functions
PSS	A 17-bit up-counter using the system clock as input
TMG	This selects the event-counter function, whether counting is up or down, and the input clock.
TCG	An 8-bit up-counter driven by the detection of rising edges on the TMIC input pin.
ICRGR	When a rising edge of the TMIG input pulse is detected, the TCG counter value is stored.
NCS	This controls the noise-cancellation function and is not used in this task.
IENTG	This enables interrupt requests of rising edges of TMIG pin input.
IRRTG	An interrupt flag of rising edge of TMIG pin input.
TMIG	Pulses to be measured are input.
TCSRWD1	This stops the watchdog timer.

3. Principle of Operation

Figure 3 illustrates the principle of operation of this sample task. As shown in figure 3, pulse periods are measured by the Timer G input capture function by means of hardware processing and software processing.

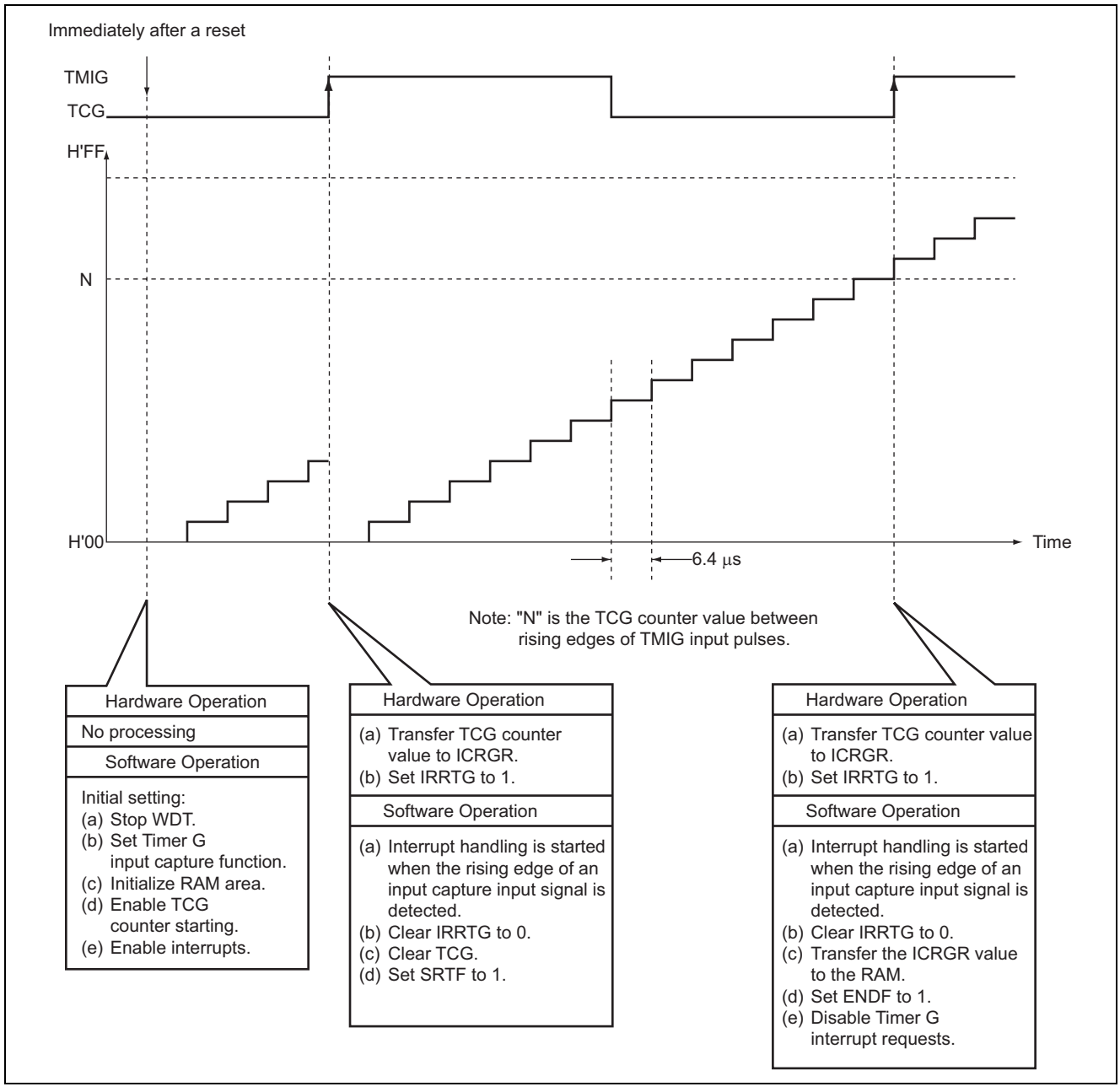


Figure 3 Principle of Operation of Pulse Period Measurement by Timer G Input Capture Function

4. Description of Software

4.1 Modules

The modules applicable to this sample task are listed in table 2.

Table 2 Description of Modules

Module Name	Label Name	Function
Main Routine	main	Sets the Timer G input capture function, sets the TMIG input pin function, and enables interrupts.
Period Measurement End	tgint	During the Timer G interrupt handling, initializes TCG to H'00 when the first IRRTG interrupt occurs, stores ICRGR data in the RAM when the second IRRTG interrupt occurs, and disables Timer G interrupt requests.

4.2 Arguments

No arguments are used in this sample task.

4.3 Internal Registers

The following tables list the internal registers used in this sample task.

- Timer Mode Register G (TMG) Address: H'FF84

Bit	Bit Name	Setting Value	R/W	Description
7	OVFH	0	R/(W)*	Timer Overflow Flag H Indicates that TCG has overflowed from H'FF to H'00 when the input capture input signal is high. This flag is set by hardware and cleared by software. It cannot be set by software. [Setting condition] • Set when input capture input signal is high level and TCG overflows from H'FF to H'00. [Clearing condition] • Writing 0 to OVFH after reading OVFH = 1
6	OVFL	0	R/(W)*	Timer Overflow Flag L Indicates that TCG has overflowed from H'FF to H'00 when the input capture input signal is low, or in interval operation. This flag is set by hardware and cleared by software. It cannot be set by software. [Setting condition] • Set when TCG overflows from H'FF to H'00 while input capture input signal is low level or during interval operation [Clearing condition] • Writing 0 to OVFL after reading OVFL = 1
5	OVIE	1	R/W	Timer Overflow Interrupt Enable Selects enabling or disabling of interrupt generation when TCG overflows. 0: TCG overflow interrupt request is disabled 1: TCG overflow interrupt request is enabled
4	IIEGS	0	R/W	Input Capture Interrupt Edge Select Selects the input capture input signal edge that generates an interrupt request. 0: Interrupt generated on rising edge of input capture input signal 1: Interrupt generated on falling edge of input capture input signal
3	CCLR1	1	R/W	Counter Clear 1 and 0
2	CCLR0	0	R/W	Specify whether or not TCG is cleared by the rising edge, falling edge, or both edges of the input capture input signal. 00: TCG clearing is disabled 01: TCG cleared by falling edge of input capture input signal 10: TCG cleared by rising edge of input capture input signal 11: TCG cleared by both edges of input capture input signal
1	CKS1	0	R/W	Clock Select
0	CKS0	0	R/W	Select the clock input to TCG from four internal clock sources. 00: Internal clock: counting on ϕ/64 01: Internal clock: counting on ϕ/32 10: Internal clock: counting on ϕ/2 11: Internal clock: counting on ϕ_W/4

Note: * Only 0 can be written to clear the flag.

- Input Capture Register GR (ICRGR) Address: H'FF86

Bit	Bit Name	Setting Value	R/W	Description
7	ICRGR7	—	R	ICRGR is an 8-bit read-only register. When a rising edge of the input capture input signal is detected, the current TCG value is transferred to ICRGR. When IIEGS in TMG is 0 at this time, IRRTG in IRR2 is set to 1, and when IENTG in IENR2 is 1, an interrupt request is sent to the CPU. To ensure dependable input capture operation, the pulse width of the input capture input signal must be at least 2ϕ or 2ϕ_{SUB} (when the noise canceller is not used). ICRGR is initialized to H'00 upon reset.
6	ICRGR6	—	R	
5	ICRGR5	—	R	
4	ICRGR4	—	R	
3	ICRGR3	—	R	
2	ICRGR2	—	R	
1	ICRGR1	—	R	
0	ICRGR0	—	R	

- Interrupt Enable Register 2 (IENR2) Address: H'FFF4

Bit	Bit Name	Setting Value	R/W	Description
4	IENTG	1	R/W	Timer G Interrupt Request Enable The timer G interrupt request is enabled when this bit is set to 1.

- Interrupt Request Register 2 (IRR2) Address: H'FFF7

Bit	Bit Name	Set Value	R/W	Description
4	IRRTG	1	R/W	Timer G Interrupt Request Flag [Setting condition] • The timer G input capture or overflow occurs. [Clearing condition] • Writing of 0 to this bit.

- Port Mode Register F (PMRF) Address: H'F03C

Bit	Bit Name	Setting Value	R/W	Description
0	TMIG	1	R/W	PF0/TMIG Pin Function Switch 0: PF0 I/O pin 1: TMIG input pin

4.4 RAM Usage

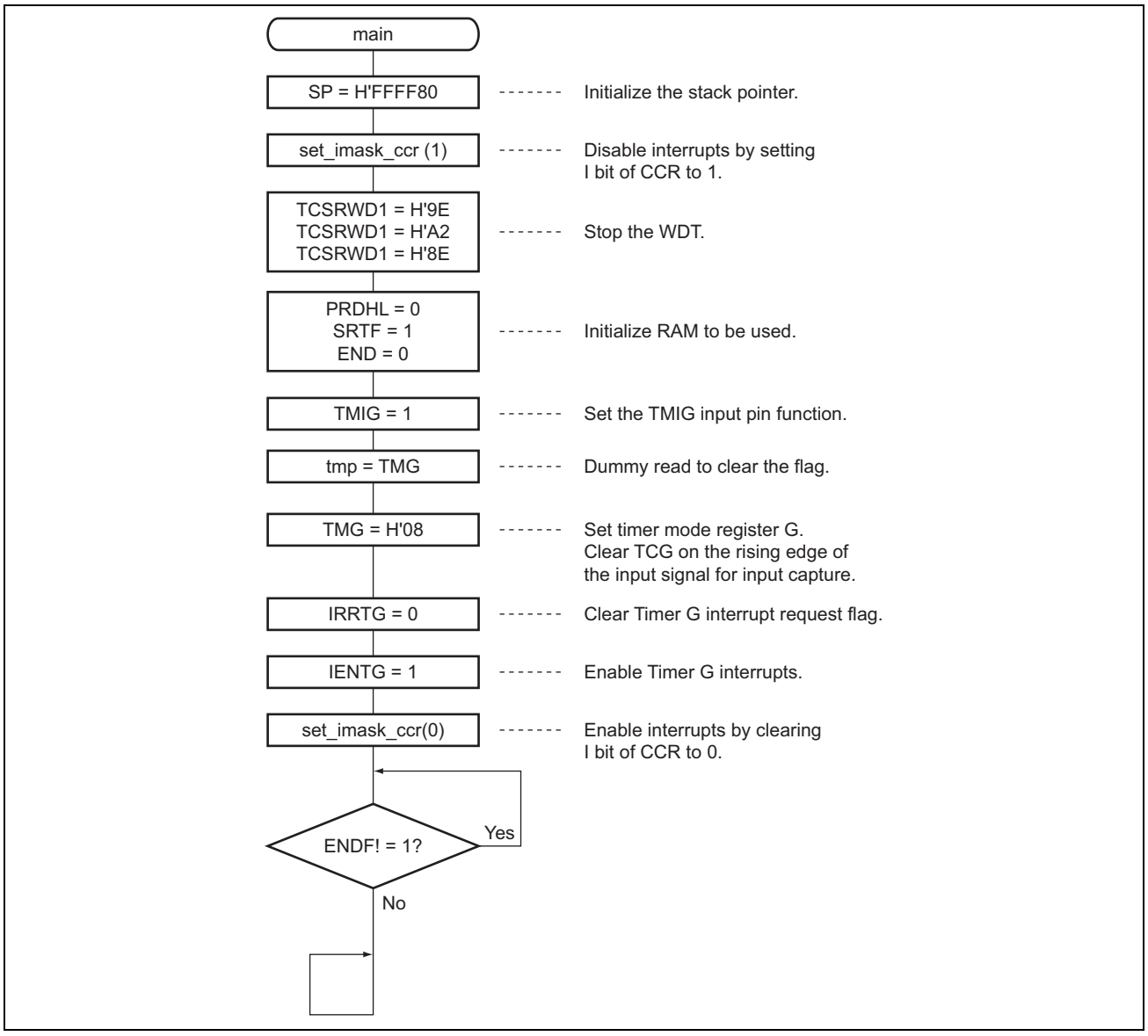
Table 3 lists and describes the RAM usage in this sample task.

Table 3 RAM Usage

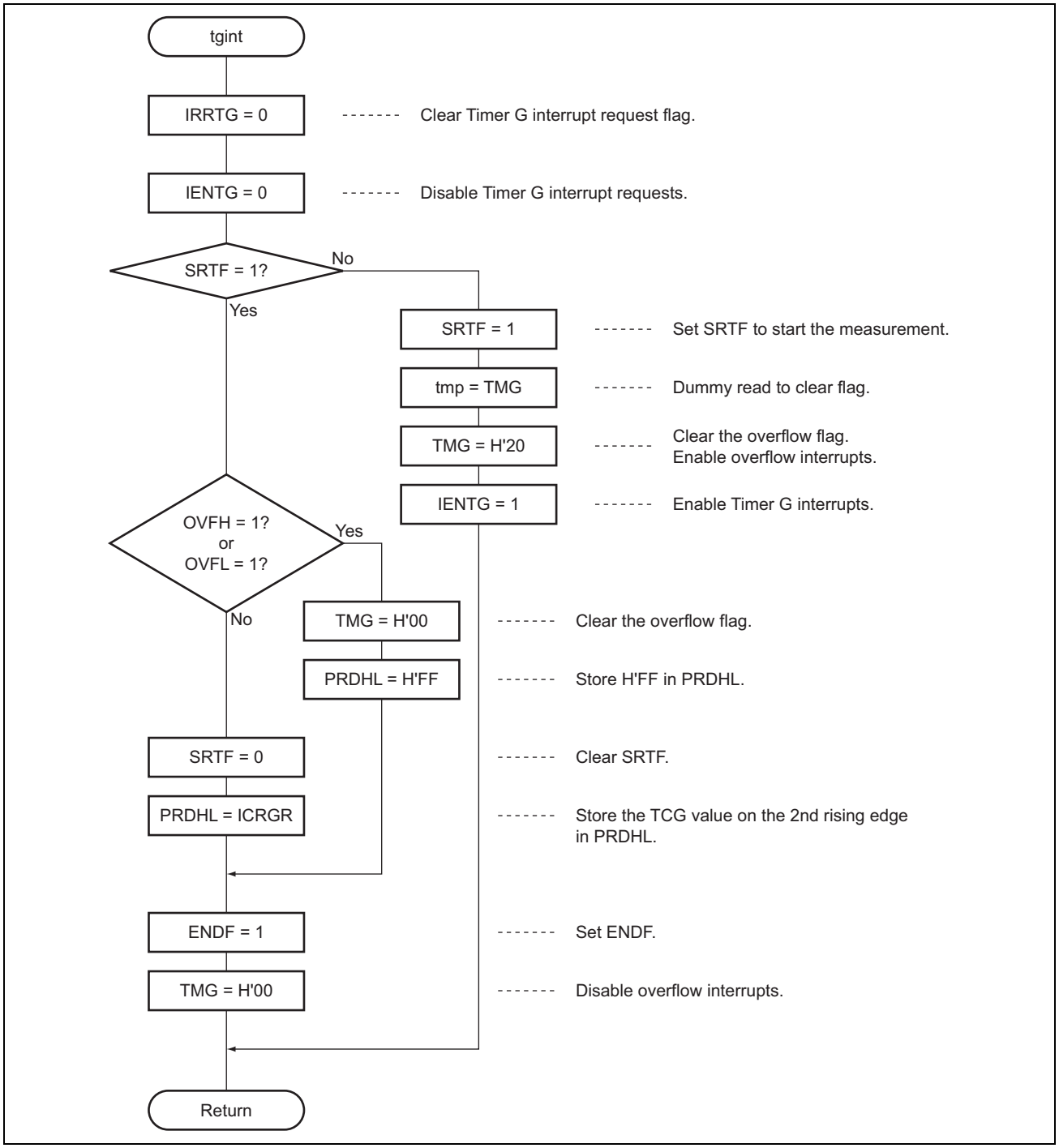
Type	Label Name		Description	Used in
unsigned char	PRDHL		Stores the TCG count value between rising edges of the TMIG input capture input signal	tgint
unsigned char	USRF	SRTF	Flag to indicate whether or not the interrupt is the second Timer G interrupt	tgint
		ENDF	Flag to indicate whether or not period measurement has ended	main, tgint

5. Flowcharts

5.1 Function main



5.2 Function tgint



6. Link Address Specifications

Section Name	Address
CV1	H'000000
CV2	H'0000D8
P	H'000800
B	H'FFF380

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