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April 1st, 2010
Renesas Electronics Corporation

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<div style="background:red;">**APPLICATION NOTE**</div>

Using Function to Start Counting on Trigger Input for Pulse Output

Introduction

A pulse with an arbitrary pulse width at an arbitrary delay after the timer V trigger input (TRGV) is output, as shown in figure 1.1.

Target Device

H8/300H Tiny Series H8/3664

Contents

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1. Specifications

1. A pulse with an arbitrary pulse width at an arbitrary delay after the timer V trigger input (TRGV) is output, as shown in figure 1.1.

2. The pulse is output from the timer V output (TMOV) pin.

3. The delay after the TRGV input is set in timer constant register A (TCORA).

4. The output pulse width is set in timer constant register B (TCORB).

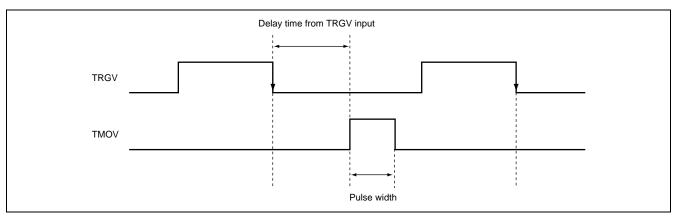5. In this sample task, a pulse with a 0.2-ms pulse width is output with a 0.8-ms delay after the TRGV input.

Figure 1.1   Using Function of Starting to Count on Trigger Input for Pulse Output

2. Description of Functions Used

In this sample task, a pulse with an arbitrary pulse width is output from the TMOV output pin after an arbitrary delay from the TRGV input by timer V's function of starting to count on trigger input.

Figure 2.1 is a block diagram of timer V's function of starting count on trigger input. The elements of the block diagram are described below.

- The system clock (ϕ) is a 16-MHz OSC clock that is used as a reference clock for operating the CPU and peripheral functions.
- Prescaler S (PSS) is a 13-bit counter with clock input of ϕ. PSS is incremented every cycle.
- Timer counter V (TCNTV) is an 8-bit readable/writable up-counter that is incremented by internal or external clock input. The clock source can be selected from a total of nine clocks: six clocks obtained by dividing the system clock, and three external clocks.
- Timer control register V0 (TCRV0) is an 8-bit readable/writable register that selects the TCNTV input clock and controls clearing of TCNTV. In this sample task, system clock/64 is selected as the TCNTV input clock, and compare match B is selected as the clearing condition of TCNTV.
- Timer control register V1 (TCRV1) is an 8-bit readable/writable register that selects the valid edge at the TRGV pin, starts TCNTV up-count with the TRGV pin input, enables TCNTV up-count to be halted when TCNTV is cleared by a compare match, and selects the TCNTV input clock together with TCRV0.
- Timer control/status register V (TCSRV) is an 8-bit register that controls compare match output. In this sample task, 0 is output from the TMOV pin when compare match B occurs, and 1 is output from the TMOV pin when compare match A occurs.
- Timer constant register A (TCORA) is an 8-bit readable/writable register that is compared with TCNTV at all times. When the TCORA and TCNTV contents match, compare match A occurs, and as a result, 1 is output from the TMOV pin.
- Timer constant register B (TCORB) is an 8-bit readable/writable register that is compared with TCNTV at all times. When the TCORB and TCNTV contents match, compare match B occurs, and as a result, 0 is output from the TMOV pin and TCNTV is cleared to H'00.
- A pulse is output from the timer V output (TMOV) pin.
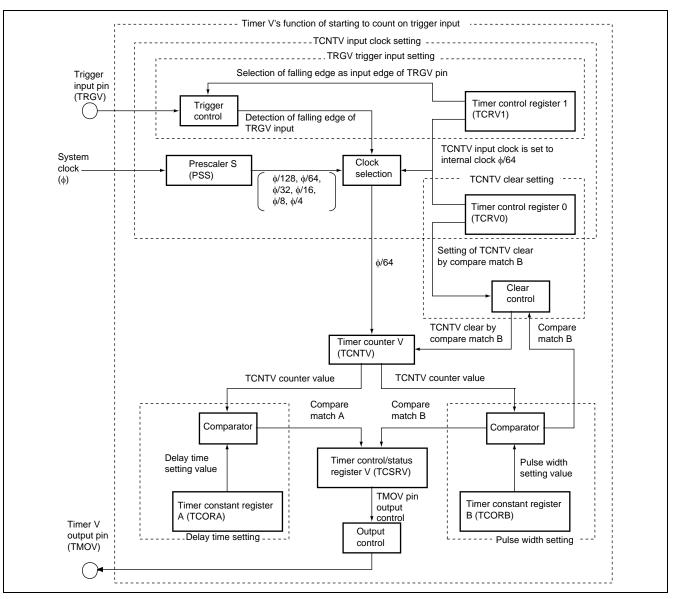- A trigger is input to the trigger input (TRGV) pin.

Figure 2.1 Timer V's Function of Starting to Count on Trigger Input

Figure 2.2 shows how to set the delay and pulse width for a pulse that has an arbitrary pulse width and is output after an arbitrary delay from the TRGV input.
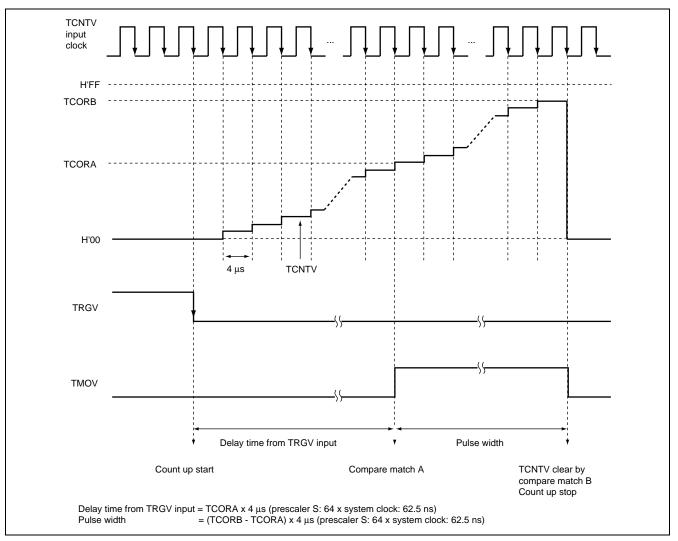

Figure 2.2 Setting of Delay after TRGV Input and Pulse Width

Table 2.1 lists the function allocation for this sample task. The functions listed in table 2.17 are allocated so that timer V's function of starting to count on trigger input outputs a pulse.

Table 2.1   Function Allocation

Function	Description
PSS	13-bit counter with system clock input
TCNTV	8-bit counter with clock input of system clock/64
TCORA	Sets compare match A by delay time setting
TCORB	Sets compare match B by pulse width setting
TCRV0	Selects the TCNTV input clock and TCNTV clearing condition
TCRV1	Selects the valid edge of the TRGV pin, enables TRGV input, and sets the TCNTV input clock
TCSRV	Controls compare match output
TMOV	Pulse output pin
TRGV	Trigger input pin

3. Description of Operations

Figure 3.1 shows the this sample task's principle of operation. The hardware and software processing shown in figure 3.1 applies timer V's function of starting to count on trigger input to output a pulse.
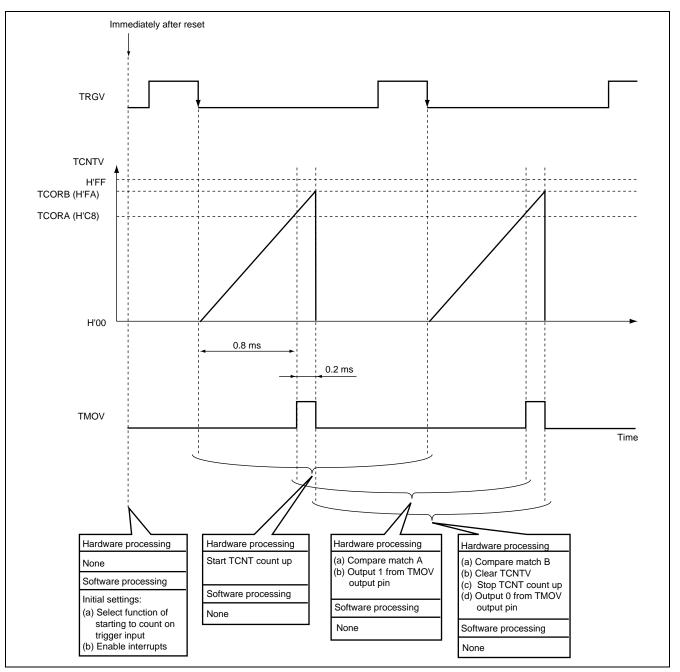

Figure 3.1   Operation Principle: Using Timer V's Function of Starting to Count on Trigger Input for Pulse Output

4. Description of Software

4.1 Description of Modules

Table 4.1 describes the software used in this sample task.

Table 4.1   Description of Module

Module Name	Label Name	Function
Main routine	main	Sets compare match A or B, initializes TCNTV, and sets the TRGV input pin and TMOV output pin.

4.2 Description of Arguments

No arguments are used in this sample task.

4.3 Description of Internal Registers

Table 4.2 describes the internal registers used in this sample task.

Table 4.2   Description of Internal Registers

Register Name	Function	Address	Setting
TCRV0	Timer control register V0: When TCRV0 is set to H'13, CMFB, CMFA, and OVF interrupts are disabled, TCNTV is cleared when compare match B occurs, and the TCNTV input clock is set to system clock/64.	H'FFA0	H'13
TCSRV	Timer control/status register V: When TCSRV is set to H'16, the TMOV pin output is 1 at compare match A and 0 at compare match B.	H'FFA1	H'16
TCORA	Time constant register A: When TCORA is set to H'C8, compare match A occurs when the TCNTV value has become H'C8.	H'FFA2	H'C8
TCORB	Time constant register B: When TCORB is set to H'FA, compare match B occurs when the TCNTV value has become H'FA.	H'FFA3	H'FA
TNCTV	Timer counter V: 8-bit up-counter incremented by clock input of system clock/64	H'FFA4	H'00

Table 4.2   Description of Internal Registers (cont)

Register Name		Function	Address	Setting
TCRV1		Timer control register V1:	H'FFA5	H'F6
		When TCRV1 is set to H'F6, the valid edge at the TRGV pin is set to the falling edge, TCNTV counting start by TRGV pin input and TCNTV counting stop by TCNTV clearing caused by a compare match are enabled, and the TCNTV input clock is set to system clock/64.		
PMR1	IRQ3	Port mode register 1 (P1$_7$/$\overline{\text{IRQ3}}$/TRGV pin function switch):	H'FFE0	
		When IRQ3 is set to 1, the P1$_7$/$\overline{\text{IRQ3}}$/TRGV pin functions as the Bit 7 $\overline{\text{IRQ3}}$/TRGV input pin.		1

4.4 Description of RAM

RAM is not used in this sample task.
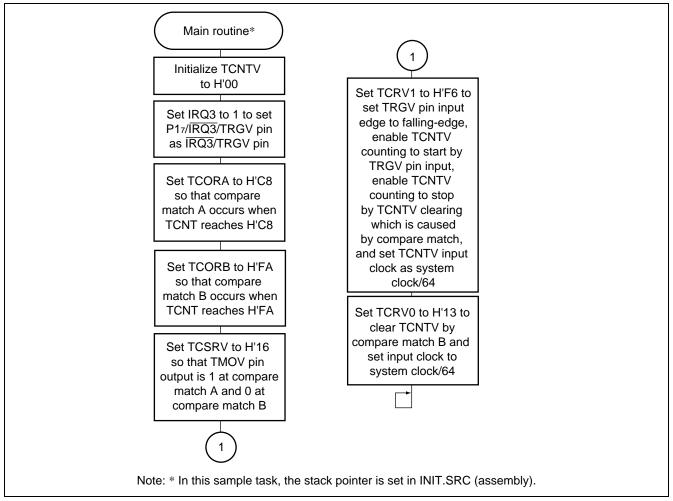
5. Flowchart

Figure 5.1 Flowchart for Main Routine

6. Program Listing

INIT.SRC (Program listing)

```
 .EXPORT_INIT

 .IMPORT_main

 ;

 .SECTION    P,CODE

 _INIT:

 MOV.W#H'FF80,R7

 LDC.B#B'10000000,CCR

 JMP@_main

 ;

  .END
```

```
/**********************************************************/
/*                                                        */
/*    H8/300H Tiny Series -H8/3664-                       */
/*    Application Note                                    */
/*                                                        */
/*    'Pulse Output by Trigger Input Count                */
/*     Start Function'                                    */
/*                                                        */
/*    Function                                            */
/*    : Timer V Trigger Input Count Start Function'       */
/*                                                        */
/*    External Clock : 16MHz                              */
/*    Internal Clock : 16MHz                              */
/*    Sub Clock      : 32.768kHz                          */
/*                                                        */
/**********************************************************/


 #include    <machine.h>
```

```
/***********************************************************/
/*     Symbol Defnition                                    */
/***********************************************************/


struct BIT {

    unsigned char    b7:1;        /* bit7 */

    unsigned char    b6:1;        /* bit6 */

    unsigned char    b5:1;        /* bit5 */

    unsigned char    b4:1;        /* bit4 */

    unsigned char    b3:1;        /* bit3 */

    unsigned char    b2:1;        /* bit2 */

    unsigned char    b1:1;        /* bit1 */

    unsigned char    b0:1;        /* bit0 */

};


    #define    TCRV0     *(volatile unsigned char *)0xFFA0   /* Time Constant Register V0          */

    #define    TCSRV     *(volatile unsigned char *)0xFFA1   /* Timer Control/Status Register V    */

    #define    TCORA     *(volatile unsigned char *)0xFFA2   /* Time Constant Register A           */

    #define    TCORB     *(volatile unsigned char *)0xFFA3   /* Time Constant Reguster B           */

    #define    TCNTV     *(volatile unsigned char *)0xFFA4   /* Timer Counter V                    */

    #define    TCRV1     *(volatile unsigned char *)0xFFA5   /* Timer Control Register V1          */

    #define    PMR1_BIT  (*(struct BIT *)0xFFE0)             /* TPort Mode Register 1              */

    #define    IRQ3      PMR1_BIT.b7                         /* P17/IRQ3/TRGV Terminal Function Change */


/***********************************************************/
/*     Function Definition                                 */
/***********************************************************/
extern    void    INIT ( void );                            /* SP Set            */

void      main    ( void );

void      trgmn   ( void );


/***********************************************************/
/*     Vector Address                                      */
/***********************************************************/
#pragma    section      V1                                  /* VECTOR SECTOIN SET */

void (*const VEC_TBL1[])(void) = {

/* 0x00 - 0x0f */

    INIT                                                    /* 00 Reset          */


};
```

```
#pragma    section                           /* P                                    */
/**********************************************************/
/*    Main Program                            */
/**********************************************************/
void main ( void )
{

    TCNTV = 0x00;                    /* Initialze TCNTV                              */

    IRQ3 = 1;                        /* Initialze TRGV Input Terminal Function       */

    TCORA = 0xC8;                    /* Initialize Compare Match A(Set Output Pulse Delay Time) */

    TCORB = 0xFA;                    /* Initialize Compare Match B(Set Output Pulse Width)    */

    TCSRV = 0x16;                    /* Initialize TMOV Terminal Output              */

    TCRV1 = 0xF6;                    /* Initialize Trigger Input Function            */

    TCRV0 = 0x13;                    /* Initialize TCNTV Clear Condition & TCNTV Input Clock  */

    while(1)   {
        ;
    }
}
```

Link Address Setting:

Section Name	Address
CV1	H'0000
CV2	H'002A
P	H'0100
B	H'FB80