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April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (<http://www.renesas.com>)

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H8/300H Tiny Series

Using Compare Match Function for Timer W 0/1 Output

Introduction

Timer W outputs 0 or 1 on a compare-match of its timer counter TCNT.

Target Device

H8/3664

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1. Specifications

1. Timer W outputs 0 or 1 on a compare-match of its timer counter TCNT.
2. The FTIOA pin normally outputs 1 and outputs 0 when TCNT matches GRA.
3. The FTIOB pin normally outputs 0 and outputs 1 when TCNT matches GRB.

2. Description of Functions Used

1. In this sample task, timer W outputs 0 or 1 from its output pins on a compare-match of the timer counter (TCNT) of timer W. Figure 2.1 is a block diagram of timer W. The elements of the block diagram are described below.
 - The system clock (ϕ) is a 16-MHz clock that is used as a reference clock for operating the CPU and peripheral functions.
 - Prescaler S (PSS) is a 13-bit counter with clock input of ϕ . PSS is incremented every cycle.
 - Timer mode register W (TMRW) controls starting and stopping of the TCNT.
 - Timer control register W (TCRW) specifies the condition for clearing TCNT, the input clock of TCNT, and the initial output which will be output until the first compare-match. In this sample task, TCNT is incremented by $\phi/2$, TCNT is not cleared on compare-match, and the initial output values on the FTIOA and FTIOB pins are specified as 1 and 0, respectively.
 - Timer I/O control register 0 (TIOR0) controls the GRA and GRB. In this sample task, GRA and GRB are specified as output-compare registers, 0 is output from the FTIOA pin on a compare-match with GRA, and 1 is output from the FTIOB pin on a compare-match with GRB.
 - Timer counter (TCNT) is a 16-bit readable/writable up-counter that is incremented by the internal clock or external clock input. In this sample task, TCNT is incremented on the rising edge of $\phi/2$.
 - General register A (GRA) is a 16-bit readable/writable register that is always compared with the TCNT. In this sample task, GRA is set to 0x4000.
 - General register B (GRB) is a 16-bit readable/writable register that is always compared with the TCNT. In this sample task, GRB is set to 0x8000.
 - Input-capture/output-compare A pin (FTIOA) is specified as an output-compare output pin and outputs 0 when TCNT matches GRA.
 - Input-capture/output-compare B pin (FTIOB) is specified as an output-compare output pin and outputs 1 when TCNT matches GRB.

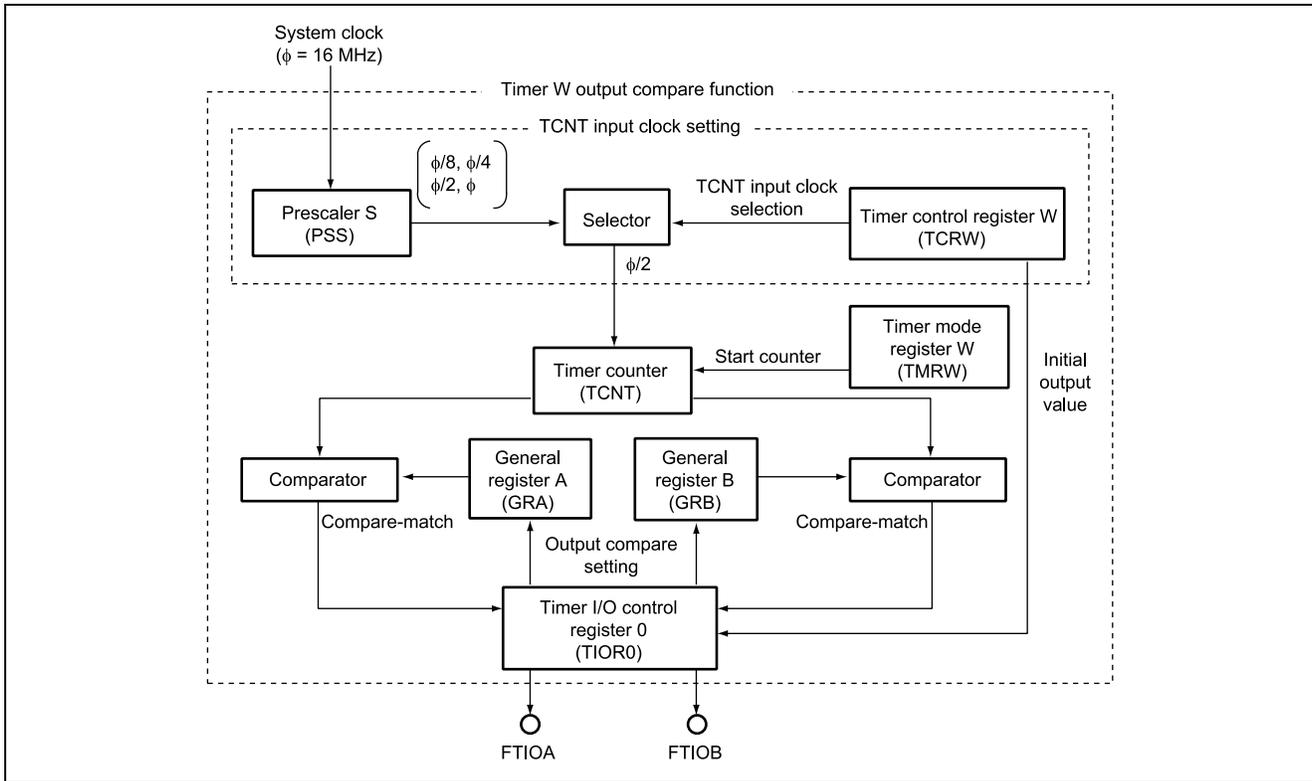


Figure 2.1 Block Diagram of Timer W Compare-Match 0/1 Output

Table 2.1 lists the function allocation for this sample task. The functions listed in this table are allocated so that 0 or 1 is output on a compare-match of timer W.

Table 2.1 Function Allocation

Function	Description
PSS	13-bit counter with system clock input
TMRW	Controls the TCNT start and stop.
TCRW	Specifies the TCNT clearing method, input clock, and initial output of the pins.
TIOR0	Specifies the output values of FTIOA and FTIOB pins on a compare-match
TCNT	16-bit counter
GRA	Compared with TCNT.
GRB	Compared with TCNT.
FTIOA pin	Outputs 0 on a compare-match with GRA.
FTIOB pin	Outputs 1 on a compare-match with GRB.

3. Description of Operations

Figure 3.1 shows the principle of operation. Hardware and software processing are applied in the way shown in figure 3.1 to output 0 or 1 on a compare-match of timer W.

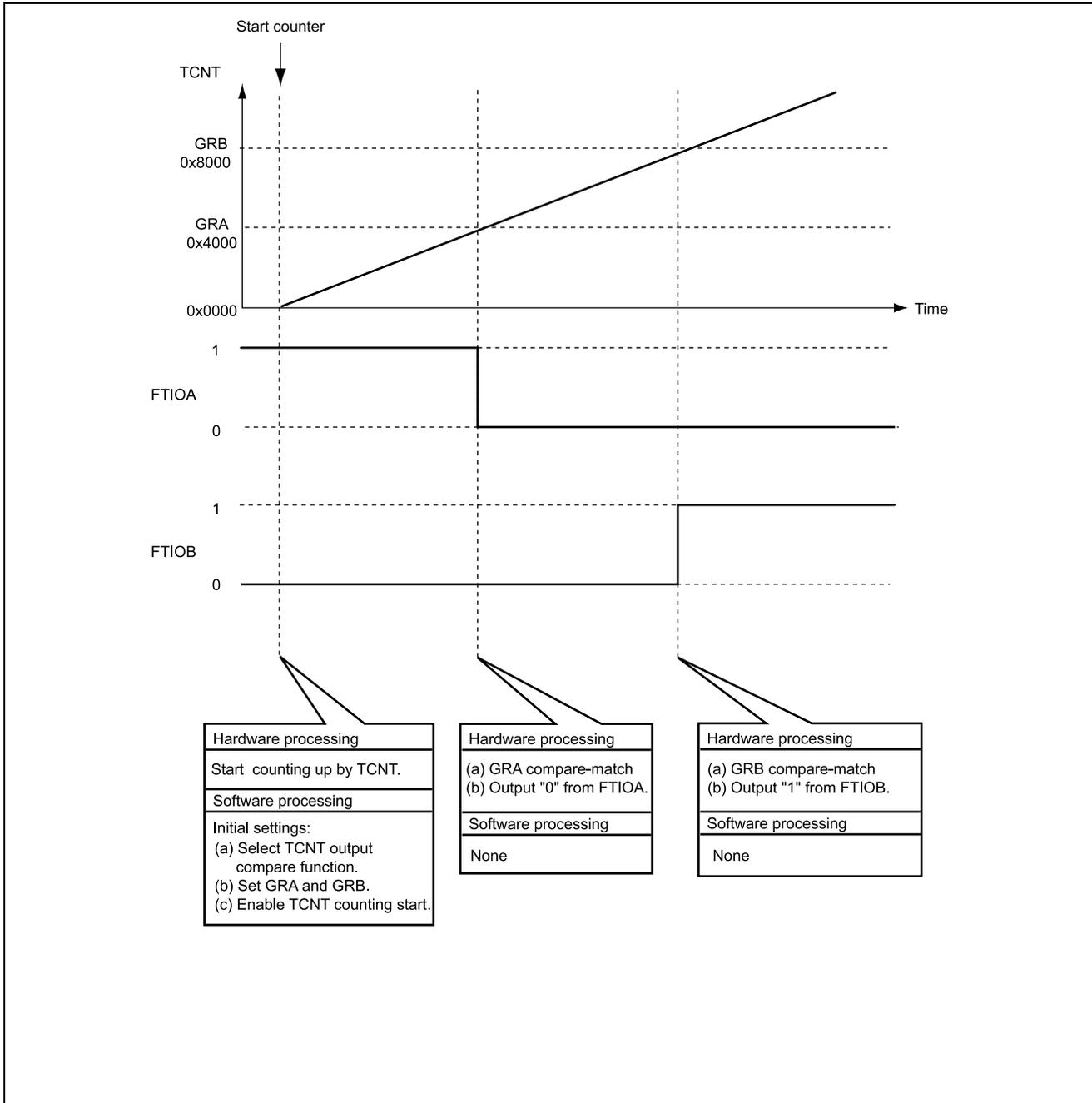


Figure 3.1 Operation Principle

4. Description of Software

4.1 Description of Modules

Table 4.1 describes the module used in this sample task.

Table 4.1 Description of the Module

Module Name	Label Name	Function
Main routine	main	Sets up timer W compare-match function, starts the counter, and sets up the output pins.

4.2 Description of Arguments

This sample task uses no arguments.

4.3 Description of Internal Registers

The internal registers used in this sample task are described below.

- TMRW Timer mode register W Address: 0xFF80

Bit	Bit Name	Setting	Function
7	CTS	0	Counter start CTS = 0: Starts counting by TCNT. CTS = 1: Stops counting by TCNT.
0	PWMB	0	PWM mode B PWMB = 0: The FTIOB pin is in output-compare output mode PWMB = 1: The FTIOB pin is in PWM output mode

- TCRW Timer control register W Address: 0xFF81

Bit	Bit Name	Setting	Function
7	CCLR	0	Counter clear CCLR = 0: Disables clearing of TCNT. CCLR = 1: Clears TCNT on compare-match A.
6	CKS2	CKS2 = 0	Clock select 2 to 0
5	CKS1	CKS1 = 0	CKS2 = 0, CKS1 = 0, CKS0 = 1: Counts by $\phi/2$
4	CKS0	CKS0 = 1	
1	TOB	0	Timer output level set B TOB = 0: Specifies the FTIOB pin initial output value as 0 TOB = 1: Specifies the FTIOB pin initial output value as 1
0	TOA	1	Timer output level set A TOA = 0: Specifies the FTIOA pin initial output value as 0 TOA = 1: Specifies the FTIOA pin initial output value as 1

- TIOR0 Timer I/O control register 0 Address: 0xFF84

Bit	Bit Name	Setting	Function
6	IOB2	IOB2 = 0	I/O control B2 to B0
5	IOB1	IOB1 = 1	IOB2 = 0, IOB1 = 1, IOB0 = 0:
4	IOB0	IOB0 = 0	Specifies the GRB as an output-compare register and specifies the FTIOB pin to output 1 on a compare-match with GRB.
2	IOA2	IOA2 = 0	I/O control A2 to A0
1	IOA1	IOA1 = 0	IOA2 = 0, IOA1 = 0, IOA0 = 1:
0	IOA0	IOA0 = 1	Specifies the GRA as an output-compare register and specifies the FTIOA pin to output 0 on a compare-match with GRA.

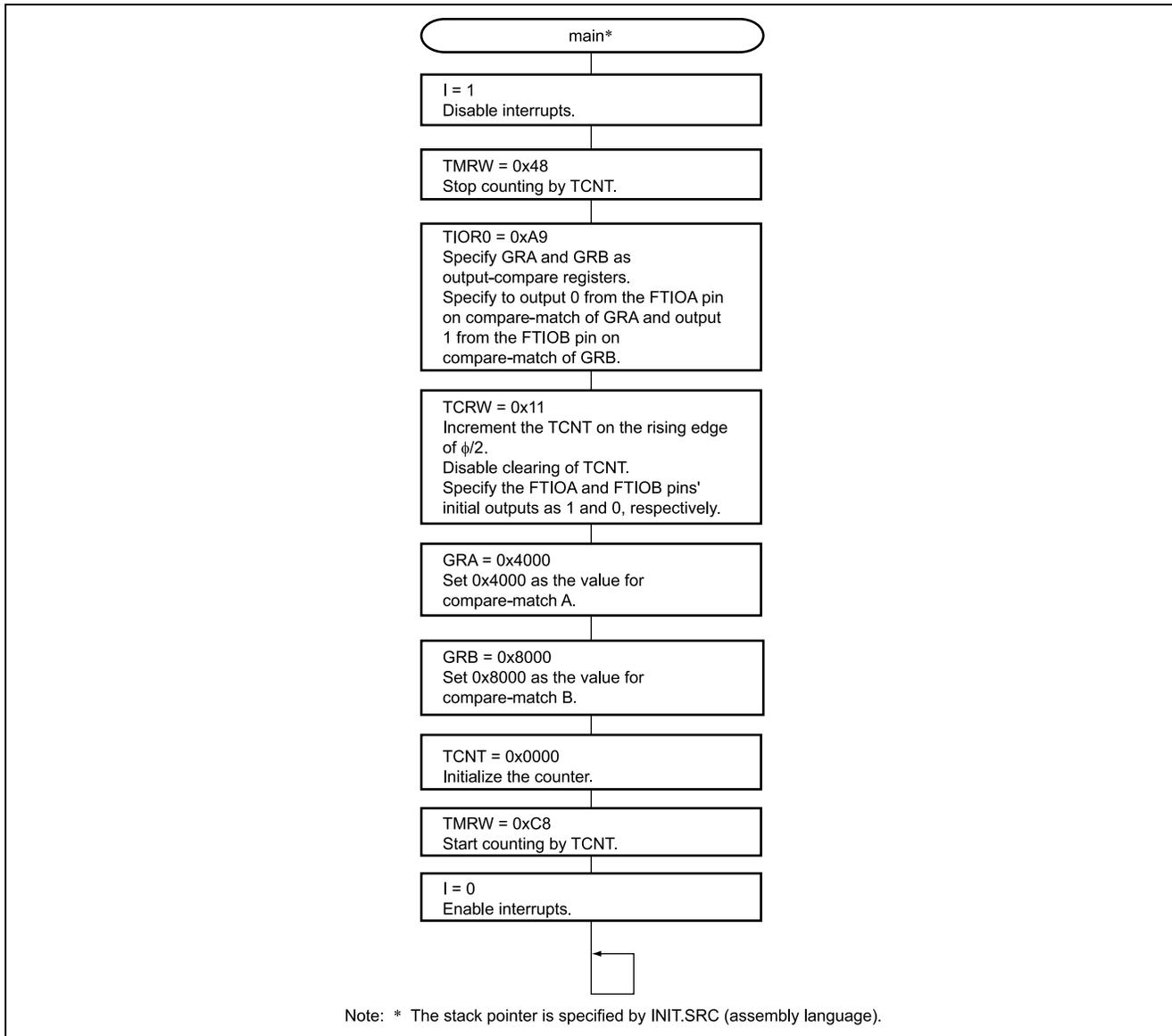
- TCNT Timer counter Address: 0xFF86
 Function: A 16-bit up-counter that is incremented on the rising edge of $\phi/2$.
 Setting: 0x0000
- GRA General register A Address: 0xFF88
 Function: Generates a compare-match when the value in the GRA matches the TCNT counter value.
 Setting: 0x4000
- GRB General register B Address: 0xFF8A
 Function: Generates a compare-match when the value in the GRB matches the TCNT counter value.
 Setting: 0x8000

4.4 Description of RAM

This sample task does not use RAM.

5. Flowchart

Main routine



6. Program Listing

```

/*****
/*
/* H8/300HN Series -H8/3664-
/* Application Note
/*
/* 'Output 0 and 1 by output compare function'
/*
/* Function
/* : Timer W output compare function
/*
/* External Clock : 16MHz
/* Internal Clock : 16MHz
/* Sub Clock : 32.768kHz
/*
*****/

#include <machine.h>

/*****
/* Symbol Definition
*****/
struct BIT {
    unsigned char b7:1 /* bit7 */
    unsigned char b6:1; /* bit6 */
    unsigned char b5:1; /* bit5 */
    unsigned char b4:1; /* bit4 */
    unsigned char b3:1; /* bit3 */
    unsigned char b2:1; /* bit2 */
    unsigned char b1:1; /* bit1 */
    unsigned char b0:1; /* bit0 */
};

#define TMRW *(volatile unsigned char *)0xFF80 /* Timer mode register W */
#define TCRW *(volatile unsigned char *)0xFF81 /* Timer control register W */
#define TIORO *(volatile unsigned char *)0xFF84 /* Timer I/O control register 0 */
#define TCNT *(volatile unsigned short *)0xFF86 /* Timer counter */
#define GRA *(volatile unsigned short *)0xFF88 /* General register A */
#define GRB *(volatile unsigned short *)0xFF8A /* General register B */

/*****
/* Function define
*****/
extern void INIT ( void ); /* SP Set */
void main ( void );

/*****
/* Vector Address
*****/
#pragma section V1 /* VECTOR SECTOIN SET */
void (*const VEC_TBL1[])(void) = {
    INIT /* 00 Reset */
};

#pragma section /* P */

```

```

/*****
/*   Main Program
*****/
void main ( void )
{
    set_imask_ccr(1);                /* Interrupt Disable          */

    TMRW = 0x48;                    /* Counter stop/Output Compare Mode */
    TIOR0 = 0xA9;                   /* 0 output by GRA compare match    */
                                        /* 1 output by GRB compare match    */
    TCRW = 0x11;                    /* Rising edge, phi/2 Clock count   */
    GRA = 0x4000;                   /* Set GRA                          */
    GRB = 0x8000;                   /* Set GRB                          */
    TCNT = 0x0000;                  /* Initialize TCNT                  */
    TMRW = 0xC8;                    /* TCNT count start                */

    set_imask_ccr(0);                /* Interrupt Enable            */

    while(1);
}

```

Link address specifications

Section Name	Address
CV1	0x0000
P	0x0100

Revision Record

Rev.	Date	Description	
		Page	Summary
1.00	Sep.29.03	—	First edition issued

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