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Renesas Electronics Corporation

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April 1, 2003

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APPLICATION NOTE

Using 16-Bit Event-Counting Function to Count Pulses

Introduction

The 16-bit event-counting function of timer W is used to count the rising edges of the pulses input to the timer clock input pin (FTCI).

Target Device

H8/300H Tiny Series H8/3664

Contents

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1. Specifications

1. The 16-bit event-counting function of timer W is used to count the rising edges of the pulses input to the timer clock input pin (FTCI).
2. The timer counter (TCNT) is set to be incremented on the rising edge of the external clock. Incrementing continues until the 1024th rising edge is received.
3. After the 1024th rising edge has been counted, the TCNT external clock input is stopped and TCNT stops.

2. Description of Functions Used

In this sample task, the number of pulses input to the FTCI input pin is counted by the 16-bit event-counting function of timer W.

Figure 2.19 is a block diagram of the 16-bit event-counting function of timer W. The elements of the block diagram are described below.

- The timer counter (TCNT) is a 16-bit readable/writable up-counter that is incremented by internal or external clock input. The clock source can be selected from a total of four clocks: three clocks obtained by dividing the system clock by 2, 4, and 8, and an external clock. In this sample task, the external clock is selected as the TCNT input clock
- Timer control register W (TCRW) is an 8-bit readable/writable register that selects the TCNT input clock.
- Timer status register W (TSRW) is an 8-bit register that controls TCNT interrupt request signals.
- Timer interrupt enable register W (TIERW) is an 8-bit readable/writable register that enables or disables each interrupt request. In this sample task, only the timer overflow interrupt request is enabled; all other interrupt requests are disabled.
- An external clock is input from the timer clock input pin (FTCI).
- Timer mode register W (TMRW) is an 8-bit readable/writable register that starts and stops TCNT.

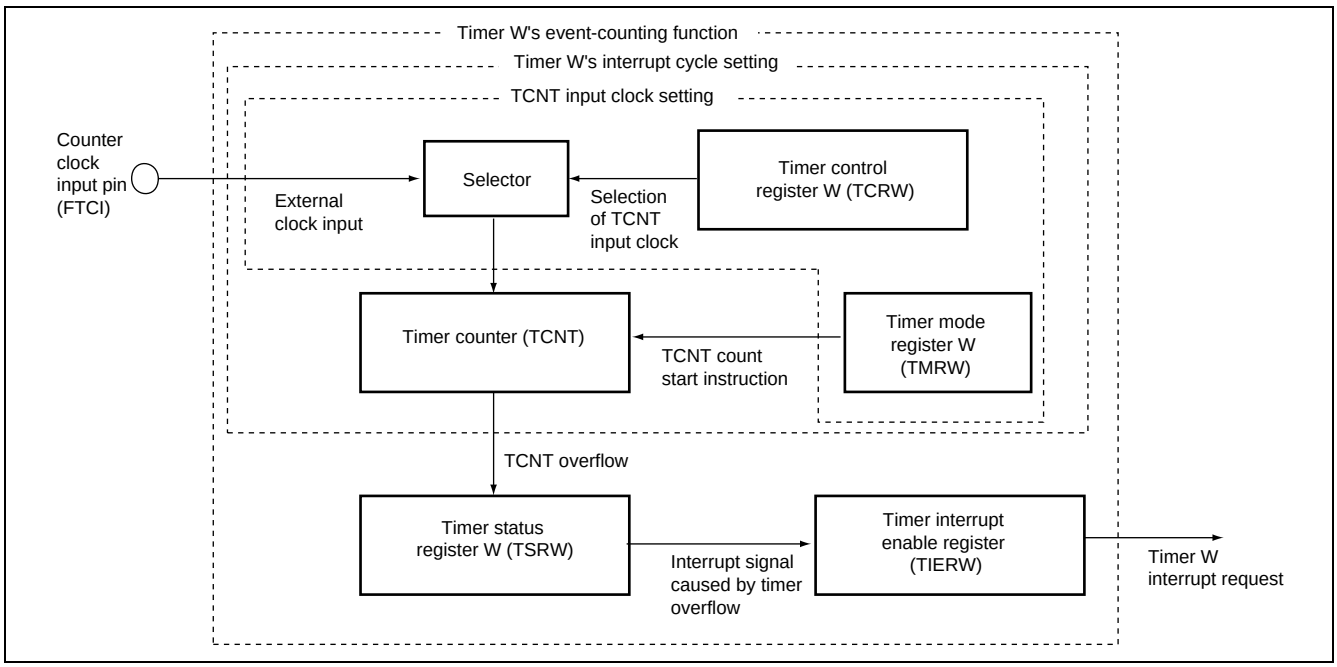


Figure 2.1 Timer W's 16-Bit Event-Counting Function

Table 2.1 lists the function allocation for this sample task. The functions listed in table 2.1 are allocated so that the number of input pulses is counted by the 16-bit event-counting function of timer W.

Table 2.1 Function Allocation

Function	Description
TCNT	16-bit counter with external clock input
TCRW	Sets TCNT input clock
TSRW	Controls signals of timer overflow interrupt requests
TIERW	Enables timer overflow interrupt requests
TMRW	Starts TCNT count
FTCI	Pulse input pin

3. Description of Operations

Figure 3.1 shows this sample task's principle of operation. The hardware and software processing shown in figure 3.1 applies the 16-bit event-counting function of timer W to count the number of input pulses.

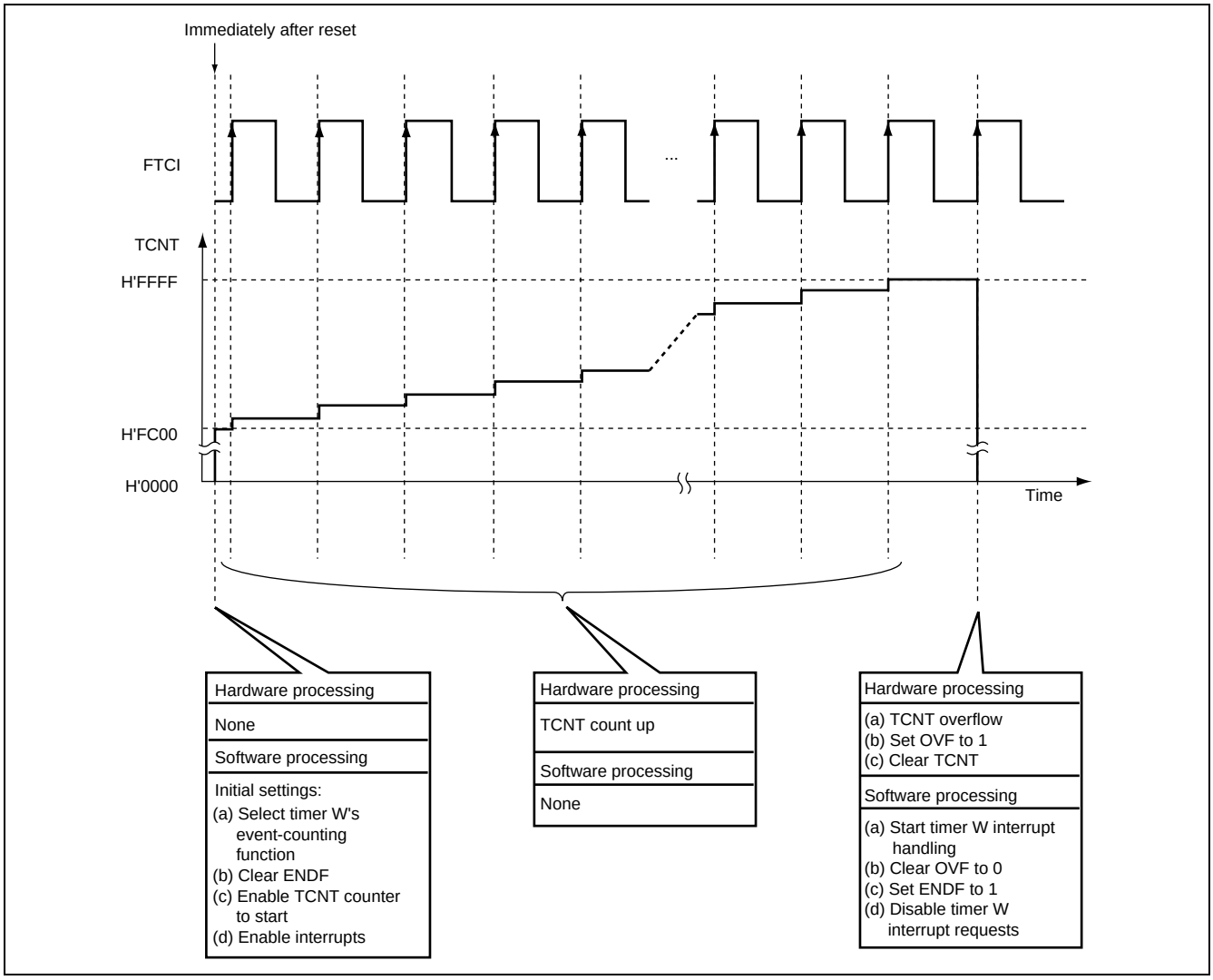


Figure 3.1 Operation Principle: Using 16-Bit Event-Counting Function of Timer W to Count Number of Input Pulses

4. Description of Software

4.1 Description of Modules

Table 4.1 describes the software used in this sample task.

Table 4.1 Description of Modules

Module Name	Label Name	Function
Main routine	main	Selects the 16-bit event-counting function, enables interrupts, and stops TCNT when the rising edge of the 1024th TCNT input clock has been counted.
Count end	twint	During the timer W interrupt handling routine, sets ENDF to 1 to disable timer W interrupts.

4.2 Description of Arguments

No arguments are used in this sample task.

4.3 Description of Internal Registers

Table 4.2 describes the internal registers used in this sample task.

Table 4.2 Description of Internal Registers

Register	Name	Function	Address	Setting
TMRW	CTS	Timer mode register W (timer counter start): When CTS is set to 1, TCNT starts. When CTS is cleared to 0, TCNT stops.	H'FF80 Bit 7	 1
TCRW		Timer control register W (clock select 2 to 0):	H'FF81	
	CKS2	When CKS2 is set to 1, and CKS1 and CKS0 are set to X (either 1 or 0), the TCNT input clock is set to the external clock.	Bit 6	CKS2 = 1
	CKS1		Bit 5	CKS1 = X
	CKS0		Bit 4	CKS0 = X
TIERW	OVIE	Timer interrupt enable register W (timer overflow interrupt enable): When OVIE is cleared to 0, OVF interrupt requests are disabled. When OVIE is set to 1, OVF interrupt requests are enabled.	H'FF82 Bit 7	 1
TSRW	OVF	Timer status register W (timer overflow): When OVF is cleared to 0, FRC overflow has not occurred. When OVF is set to 1, FRC overflow has occurred.	H'FF83 Bit 7	 0
TCNT		Timer counter: 16-bit up-counter incremented by external clock input.	H'FF86	H'00

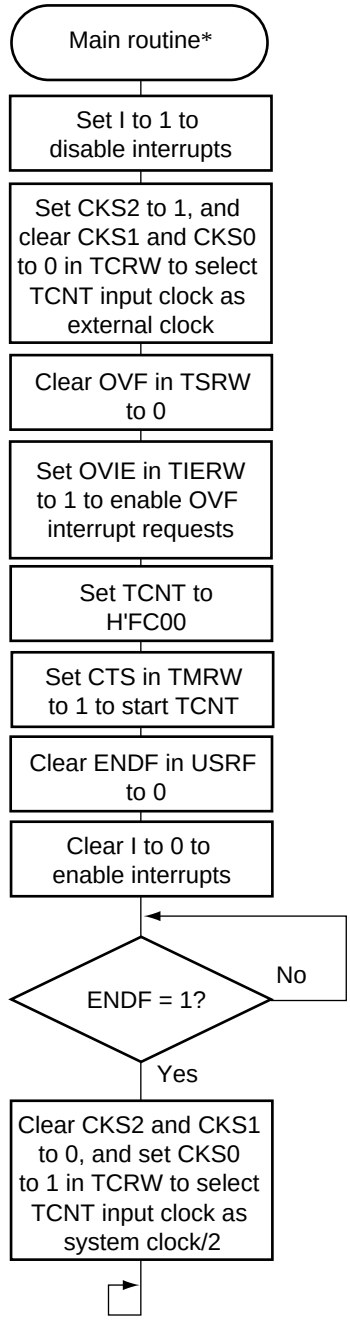
4.4 Description of RAM

Table 4.3 describes the RAM used in this sample task.

Table 4.3 Description of RAM

Label Name		Function	Address	Used in
USRF	ENDF	Flag for judging whether or not the rising edge of the input pulse has been detected for 1024 times	H'FB80 Bit 0	Main routine Count end

5. Flowcharts



Note: * In this sample task, the stack pointer is set in INIT.SRC (assembly).

Figure 5.1 Flowchart for Main Routine

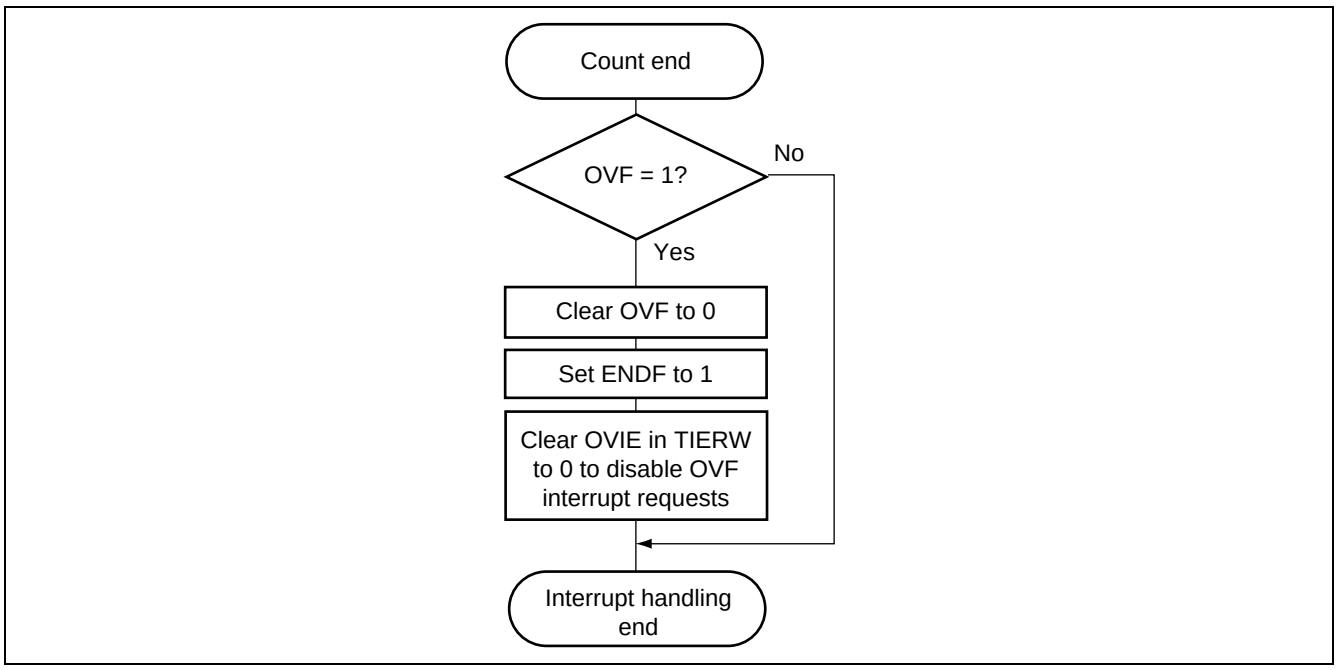


Figure 5.2 Flowchart for Timer W Interrupt Handling Routine

6. Program Listing

INIT.SRC (Program listing)

```
      .EXPORT  _INIT
      .IMPORT  _main
 ;
      .SECTION    P,CODE
 _INIT:
     MOV.W    #H'FF80,R7
     LDC.B    #B'10000000,CCR
     JMP      @_main
 ;
      .END
```

```
/************************************************************/
/*                                                          */
/*    H8/300H Tiny Series -H8/3664-                         */
/*    Application Note                                      */
/*                                                          */
/*    'Measurement of Input Pulses by 16-bit                */
/*     Event Counter Function'                              */
/*                                                          */
/*    Function                                              */
/*    : Timer W 16bit Event Counter                         */
/*                                                          */
/*    External Clock : 16MHz                                */
/*    Internal Clock : 16MHz                                */
/*    Sub Clock      : 32.768kHz                            */
/*                                                          */
/************************************************************/

#include    <machine.h>
```

```
/************************************************************/
/*    Symbol Defnition                                      */
/************************************************************/
struct BIT {
    unsigned char    b7:1;      /* bit7 */
    unsigned char    b6:1;      /* bit6 */
    unsigned char    b5:1;      /* bit5 */
    unsigned char    b4:1;      /* bit4 */
    unsigned char    b3:1;      /* bit3 */
    unsigned char    b2:1;      /* bit2 */
    unsigned char    b1:1;      /* bit1 */
    unsigned char    b0:1;      /* bit0 */
};

#define        TMRW        *(volatile unsigned char *)0xFF80   /* Timer Mode     Register W       */
#define        TCRW        *(volatile unsigned char *)0xFF81   /* Timer Control Register W        */
#define        TCRW_BIT    (*(struct BIT *)0xFF81)             /* Timer Control Register W        */
#define        CKS1        TCRW_BIT.b5                         /* Clock Select 1                  */
#define        CKS0        TCRW_BIT.b4                         /* Clock Select 0                  */
#define        TIERW       *(volatile unsigned char *)0xFF82   /* Timer Interrupt Enable Register */
#define        TIERW_BIT   (*(struct BIT *)0xFF82)             /* Timer Interrupt Enable Register */
#define        OVIE        TIERW_BIT.b7                        /* Timer Overflow Interrupt Enable */
#define        TSRW        *(volatile unsigned char *)0xFF83   /* Timer Status Register W         */
#define        TSRW_BIT    (*(struct BIT *)0xFF83)             /* Timer Status Register W         */
#define        OVF         TSRW_BIT.b7                         /* Timer Over flow                 */
#define        TCNT        *(volatile unsigned int *)0xFF86    /* Time Counter                    */
#define        PCR8_BIT    (*(struct BIT *)0xFFEB)             /* Port Control Register 8         */
#define        PCR80       PCR8_BIT.b0                         /* FTCI Select 0                   */

#pragma        interrupt    (twint)
/************************************************************/
/*     Function Definition                                  */
/************************************************************/
extern    void    INIT ( void );                            /* SP Set                          */
void      main     ( void );
void      twint    ( void );
```

```
/************************************************************/
/*    RAM define                                            */
/************************************************************/

unsigned char    USRF;                                      /* User Flag Erea               */


#define        USRF_BIT    (*(struct BIT *)&USRF)
#define        ENDF        USRF_BIT.b0                        /* End Flag                    */

/************************************************************/
/*    Vector Address                                        */
/************************************************************/
#pragma    section        V1                                 /* VECTOR SECTOIN SET           */
void (*const VEC_TBL1[])(void) = {
/* 0x00 - 0x0f */
    INIT                                                     /* 00 Reset                     */
};
#pragma    section        V2                                 /* VECTOR SECTOIN SET           */
void (*const VEC_TBL2[])(void) = {
    twint                                                    /* 2A Timer W Interrupt         */
};
#pragma    section                                           /* P                            */
/************************************************************/
/*    Main Program                                          */
/************************************************************/
void main ( void )
{
    set_imask_ccr(1);                                        /* Interrupt Disable            */

    PCR80 = 0;                                               /* Initialize FTCI Input Tarminal */

    TCRW = 0x40;                                             /* Initialize TCNT Input Clock  */

    TSRW = 0x70;                                             /* Clear OVF                    */

    TIERW = 0xF0;                                            /* OVF Interrupt Enable         */

    TCNT = 0xFC00;                                           /* Initialize FRC(Timer Counter) */
```

```
    TMRW = 0xC8;                                    /* Timer Counter Count Start      */

    ENDF = 0;                                       /* Initialize ENDF                */

    set_imask_ccr(0);                               /* Interrupt Enable               */

    while(ENDF != 1){                               /* ENDF = 1 ?                     */
        ;
    }

    TCRW = 0x10;                                    /* Initialize TCNT Input Clock    */

    while(1){
        ;
    }

}

/************************************************************/
/*    Timer W Interrupt                                     */
/************************************************************/
void twint ( void )
{

    if ( OVF == 1 ){
        OVF = 0;                                    /* Clear OVF                      */
        ENDF = 1;                                   /* Set ENDF                       */
        OVIE = 0;                                   /* OVF Interrupt Disable          */
    }
}
```

Link Address Setting:

Section Name	Address
CV1	H'0000
CV2	H'002A
P	H'0100
B	H'FB80