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SH7280 Group

Transmission and Reception of Serial Data by the SCIF in Clock Synchronous Mode (Full-Duplex Communications)

Introduction

This application note describes transmission and reception of serial data by using the clock-synchronous transfer function of the serial communications interface with FIFO (SCIF). This application note is a summary for quick reference of information required in the design of user software.

Target Device

SH7285

Contents

1. Preface

1.1 Specifications

This sample application employs the clock-synchronous serial transfer function of the serial communications interface with FIFO (SCIF) to perform data transmission and reception. Figure 1 shows an example of connection for transmission and reception by the SCIF in clock-synchronous mode.

- SCIF3 is used.
- The communications format has a fixed 8-bit data length.
- Interrupts for transmission and reception are used to conduct full-duplex communications on SCIF3. That is, the data-transfer controller (DTC) is activated by the transmit-data-empty interrupt on the transmitting side and the receive-data-full interrupt on the receiving side.
- Once 32 bytes of data have been transmitted and received, each operation for transmission is halted.

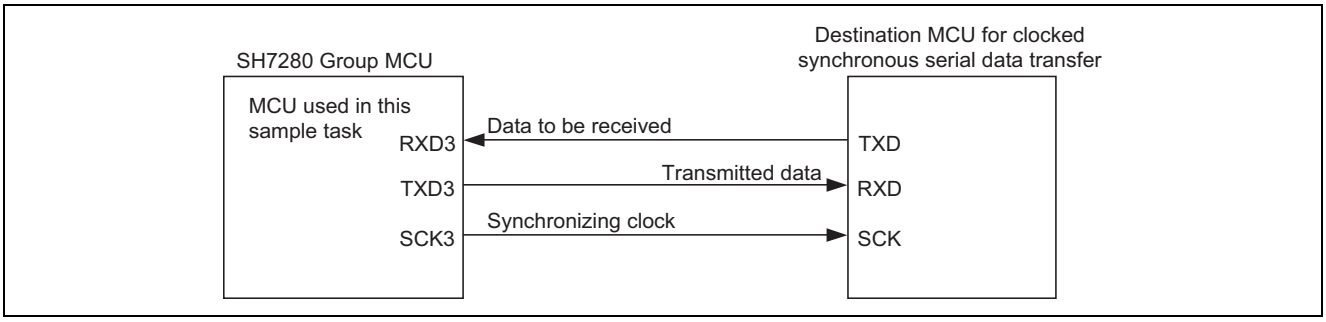

Figure 1 Connection Example for Transmission and Reception by the SCIF in Clock-Synchronous Mode

1.2 Module Used

Serial communications interface with FIFO (SCIF3)

1.3 Applicable Conditions

MCU	SH7285	
Operating frequency	Internal clock:	100 MHz
	Bus clock:	50 MHz
	Peripheral clock:	50 MHz
C compiler	SuperH RISC Engine Family C/C++ Compiler Package Ver.9.11	
	(from Renesas Technology Corp.)	

2. Description of the Sample Application

This sample application employs interrupt source of the serial communications interface with FIFO (SCIF), a transmit-FIFO-data-empty interrupt (TXI) and a receive-FIFO-data-full interrupt (RXI) to transmit and receive serial data in clock-synchronous mode. In clock-synchronous mode, the SCIF transmits and receive serial data in synchronization with clock pulses.

2.1 Summary of MCU Module Used

In clock-synchronous mode, the SCIF transmits and receives data in synchronization with clock pulses. This mode is suitable for high-speed serial communications. An internal clock or an external clock from the SCK pin can be selected as the SCIF clock source. When an internal clock has been selected, a synchronizing clock is output from the SCK pin. When an external clock has been selected, a synchronizing clock is input into the SCK pin. The transmitting and receiving sections of the SCIF are independent, so full-duplex communications is possible while sharing the same clock. Both the transmitter and receiver have a 16-stage FIFO buffered structure so that data can be read or written during transmission and reception, which enables high-speed continuous data transfer.

In clock-synchronous serial communications, each data bit is output on the communications line from one falling edge of the serial clock to the next. Data is guaranteed valid at the rising edge of the serial clock.

In each character, the serial data bits are transmitted in order from the LSB (first) to the MSB (last). After output of the MSB, the communications line remains in the state of the MSB.

For details on the SCIF, please refer to the section on serial communications interface with FIFO in the *SH7280 Group Hardware Manual*.

Table 1 gives an overview of serial communications in clock-synchronous mode. Figure 2 shows a block diagram of the SCIF.

Table 1 Overview of Serial Data Communications in Clock-Synchronous Mode

Item	Description
Number of interfaces	1 (SCIF3)
Clock sources	For internal clock: Pϕ, Pϕ/4, Pϕ/16, Pϕ/64 (Pϕ: peripheral clock) For external clock: input clock on the SCK3 pin
Data format	Transfer data length: Fixed at 8 bits Order: LSB first and MSB first are selectable
Baud rate	For internal clock: 1 to 500 kbps (Pϕ = 50 MHz) For external clock: up to 8,333,333.3 bps (Pϕ = 50 MHz, external input clock of 8.3333 MHz)
Error detection	Overrun error
Interrupt requests	Transmit-FIFO-data-empty interrupt (TXI) Receive-FIFO-data-full interrupt (RXI) Break interrupt (BRI)
Clock sources	Internal and external clocks are selectable • Internal clock When the internal clock has been selected, the SCIF operates using the clock from the baud-rate generator and outputs this clock to external devices as the synchronizing clock. • External clock When the external clock has been selected, the SCIF operates on the input synchronizing clock, not using the on-chip baud rate generator.

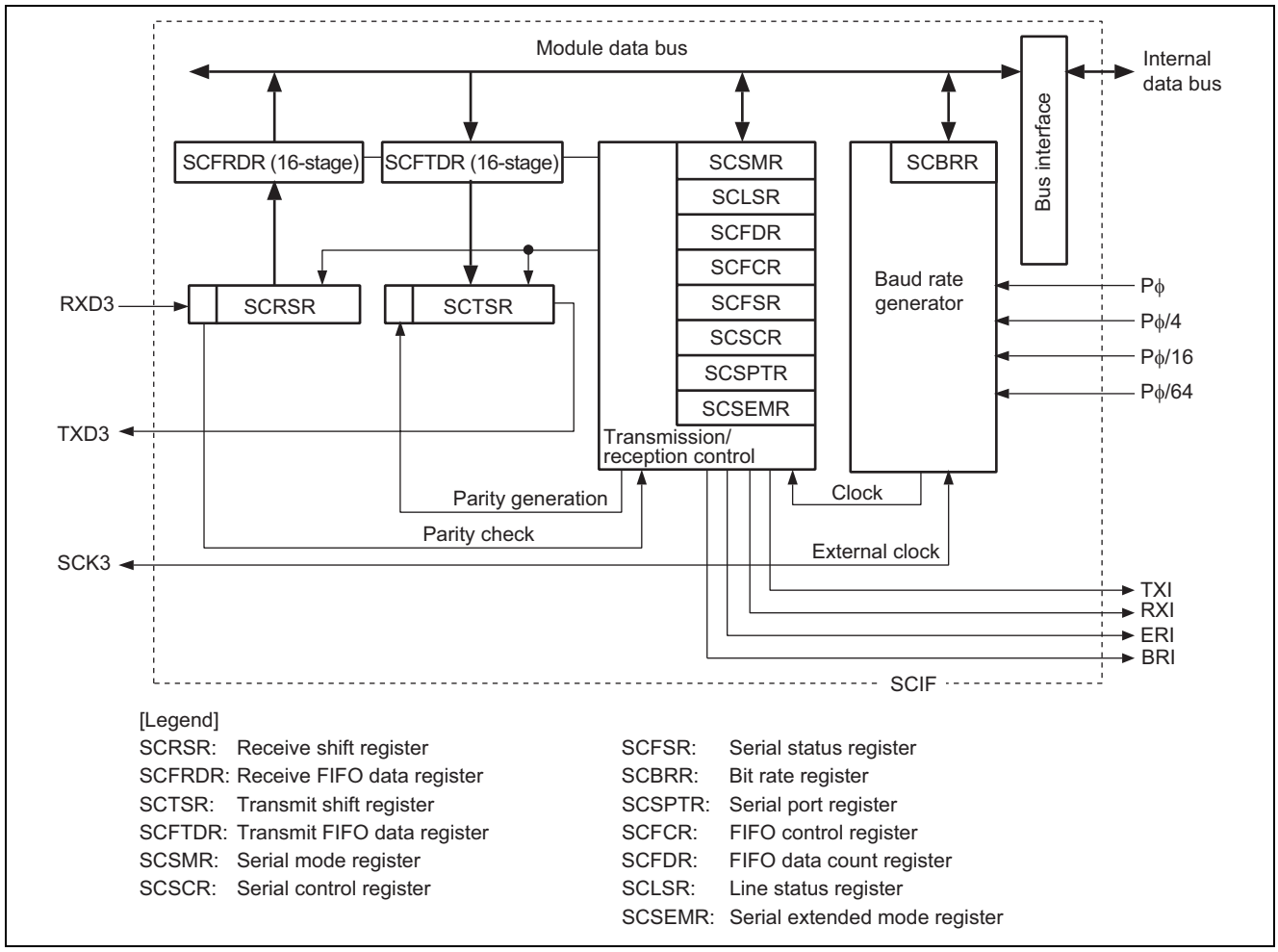

Figure 2 Block Diagram of the SCIF

2.2 Description of the Sample Program

Table 2 gives the settings for SCIF communications function of this sample program, and figure 3 shows the operations in data transmission and reception.

Table 2 Settings for Communications Function of the Sample Program

Item	Description
Module	SCIF3
Communications mode	Clock-synchronous mode
Interrupts	Transmit-FIFO-data-empty interrupt (TXI) Receive-FIFO-data-full interrupt (RXI) Break interrupt (BRI)
Transfer rate	100 kbps
Number of data to be transmitted and received	32 bytes
Data length	8-bit data (fixed)
Bit order	LSB-first
Synchronizing clock	Internal clock/ synchronizing clock on the SCK pin
FIFO data trigger number	Receive FIFO data trigger: 8 Transmit FIFO data trigger: 8
Loop-back test function	Disabled

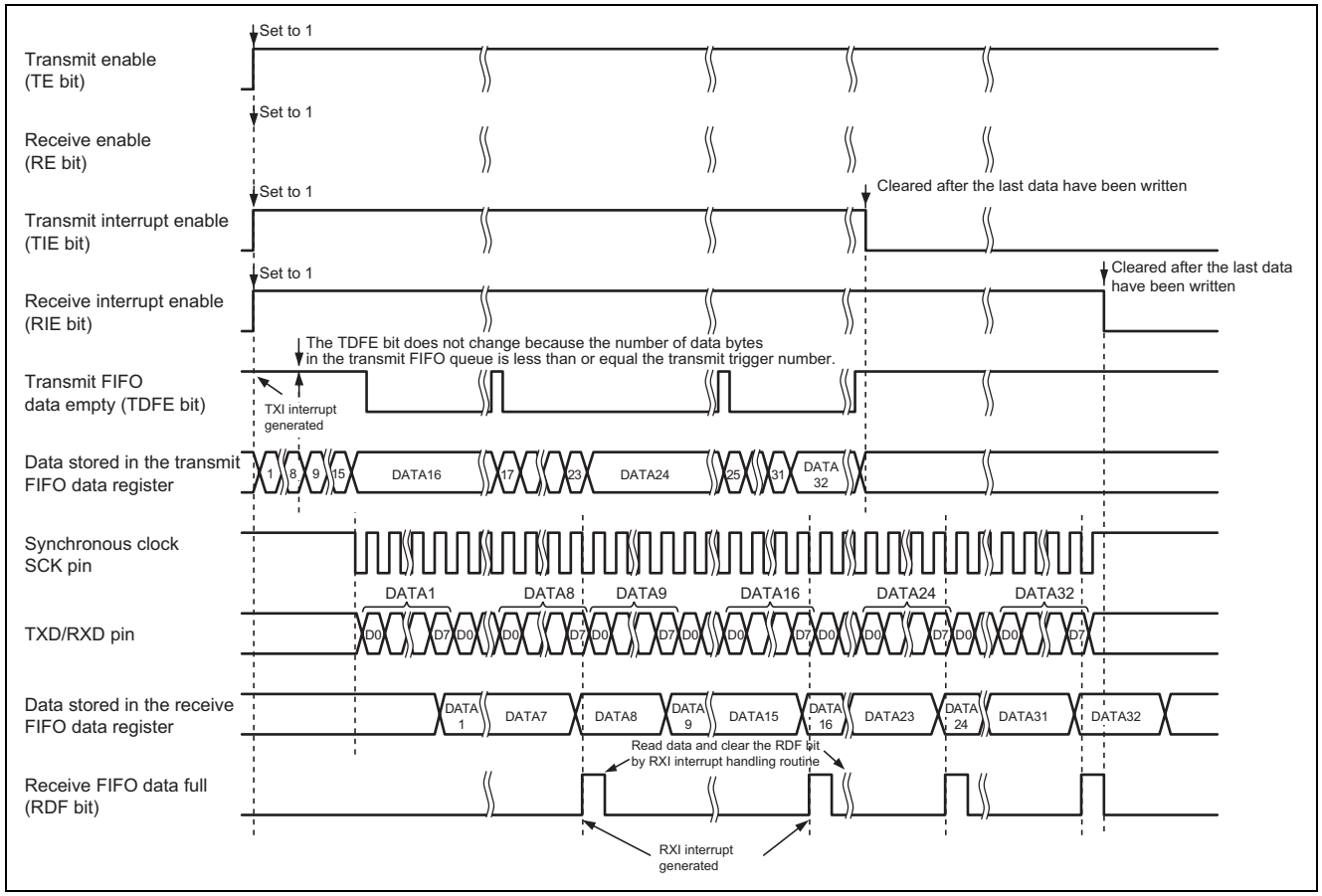

Figure 3 Operations for Data Transmission and Reception

2.3 Procedure for Setting Module Used

This section describes the procedure for setting up SCIF3 for clock-synchronous mode operation.

Figure 4 shows the flow of processing by the sample program, figure 5 shows the flow of settings for release from module-standby mode, figure 6 shows the flow for setting up the pin function controller. Furthermore, figure 7 shows the flow for initialization of data transmission and reception in clock-synchronous mode, figure 8 shows the flow for handling transmit interrupts in clock-synchronous mode, and figure 9 shows the flow for handling receive interrupts in clock-synchronous mode, and figure 10 shows the flow for handling receive error interrupts in clock-synchronous mode. For details on the settings of individual registers, see the *SH7280 Group Hardware Manual*.

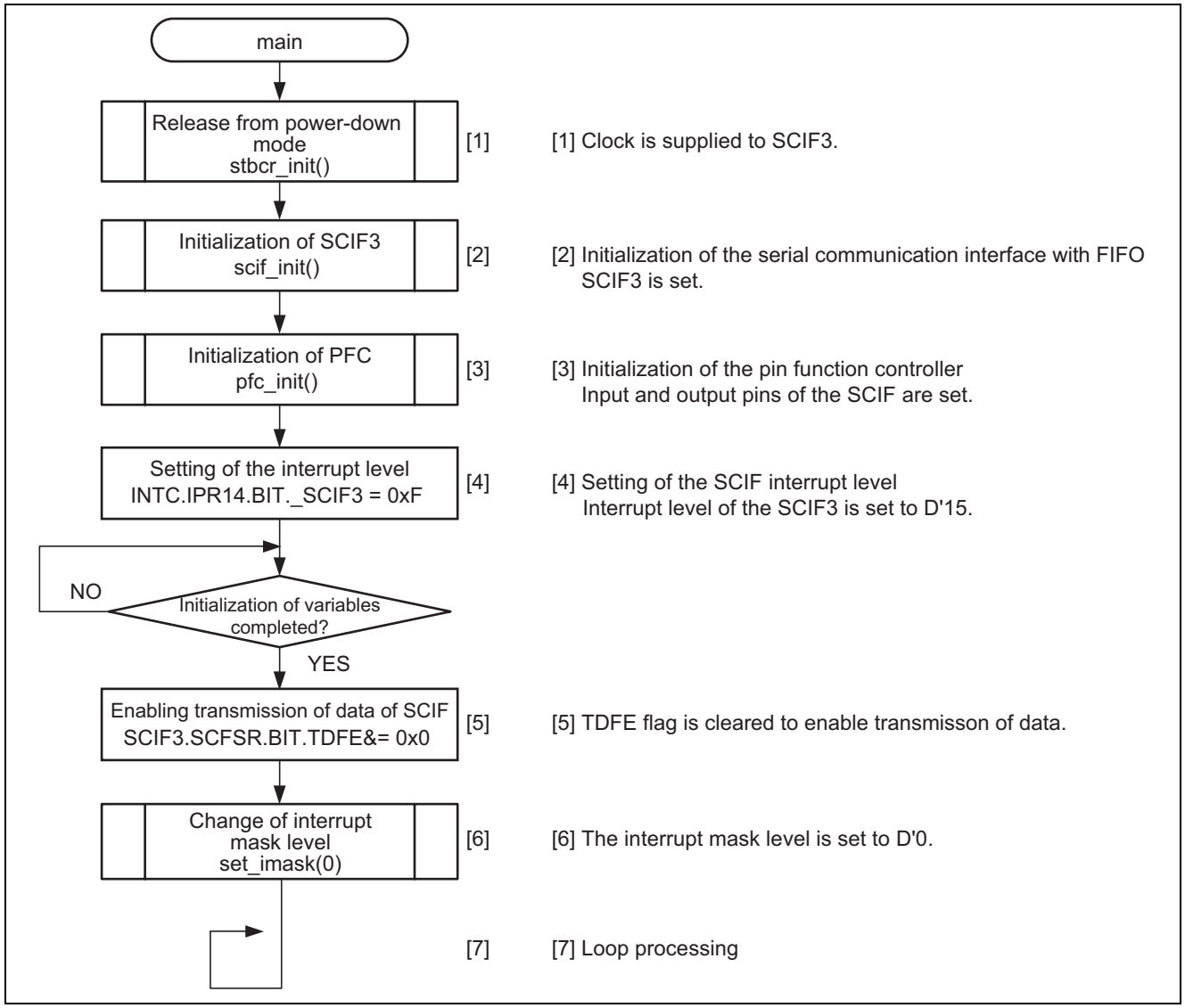

Figure 4 Flow of Processing by the Sample Program

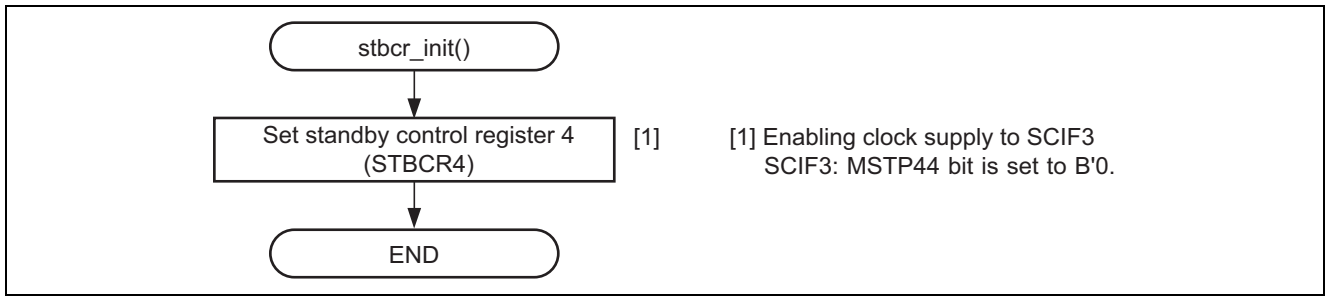

Figure 5 Flow of Settings for Release from Module-Standby Mode

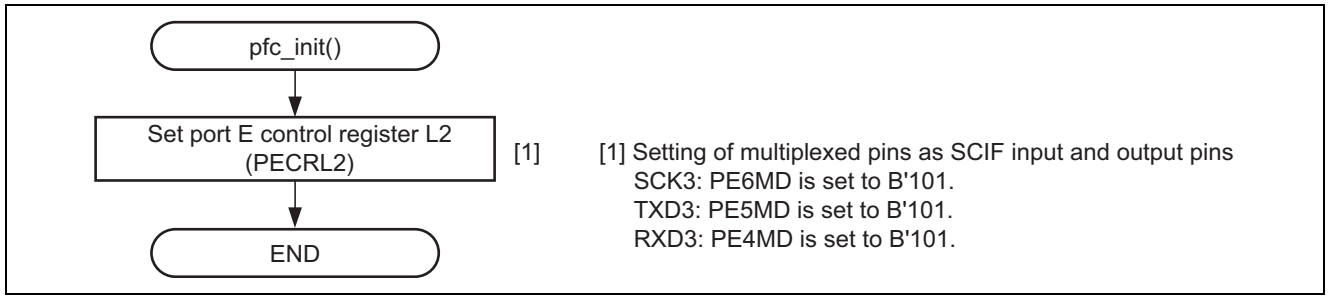

Figure 6 Flow for Setting up the Pin Function Controller

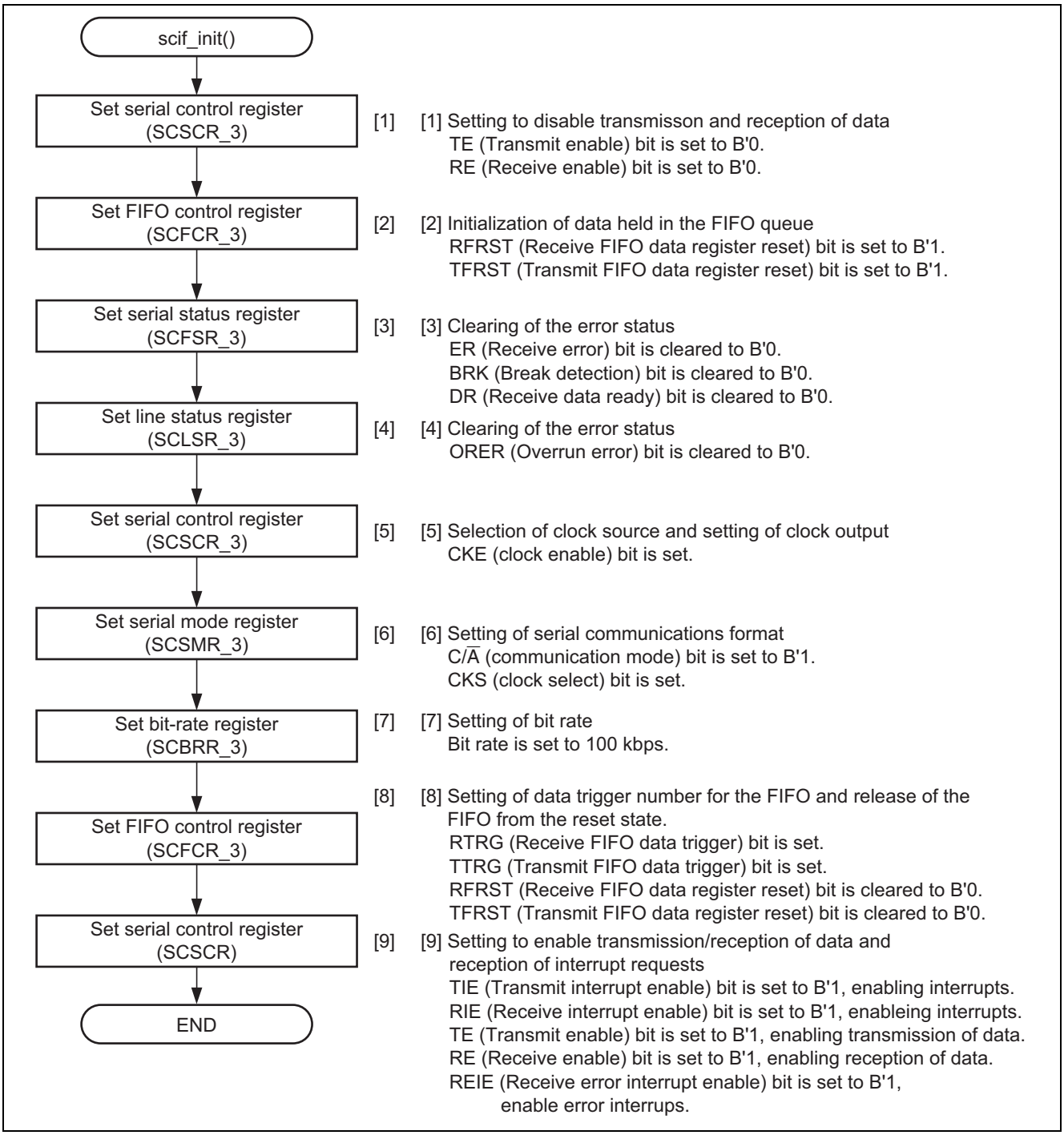

Figure 7 Flow for Initialization of Data Transmission and Reception in Clock-Synchronous Mode

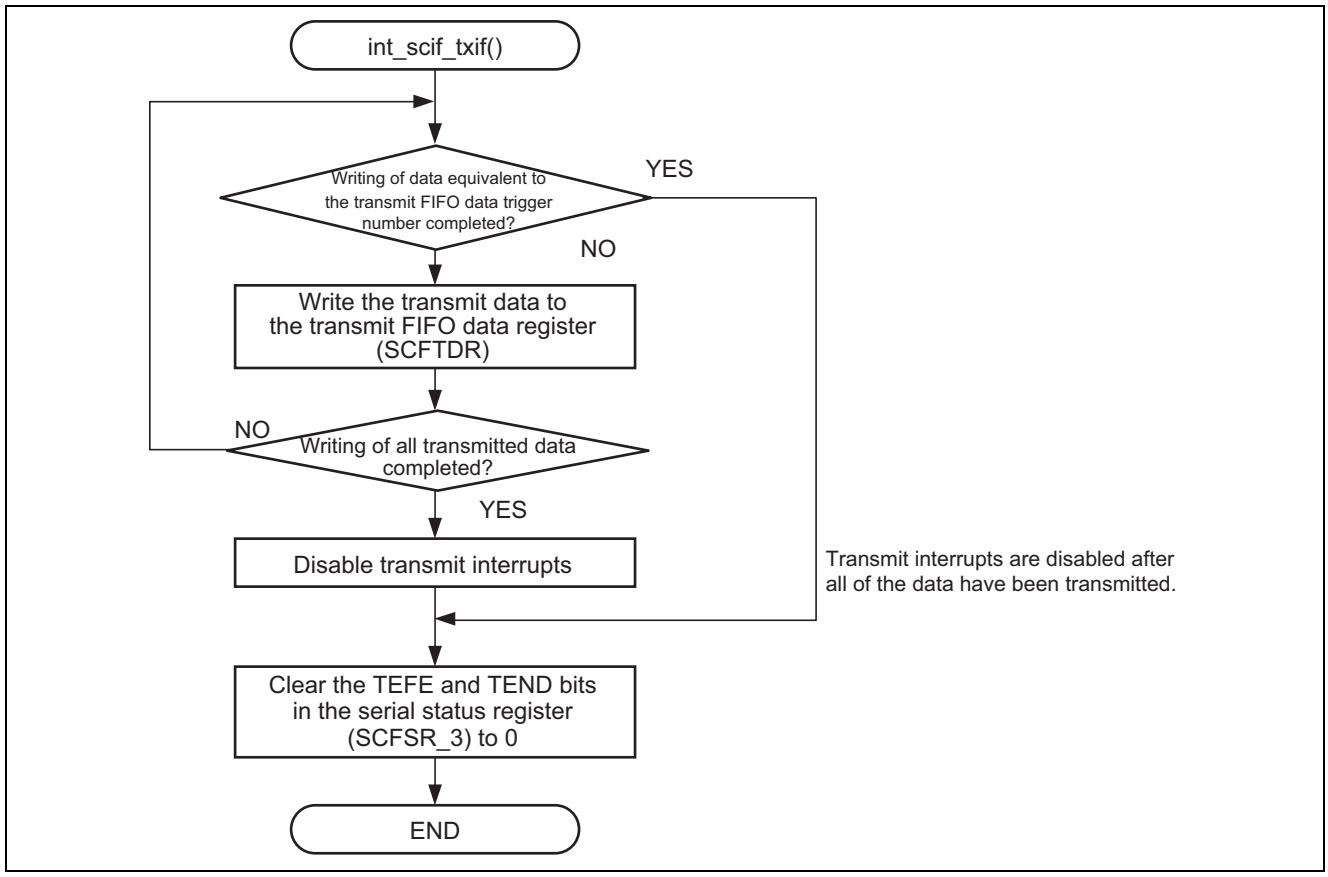

Figure 8 Flow for Handling Transmit Interrupts in Clock-Synchronous Mode

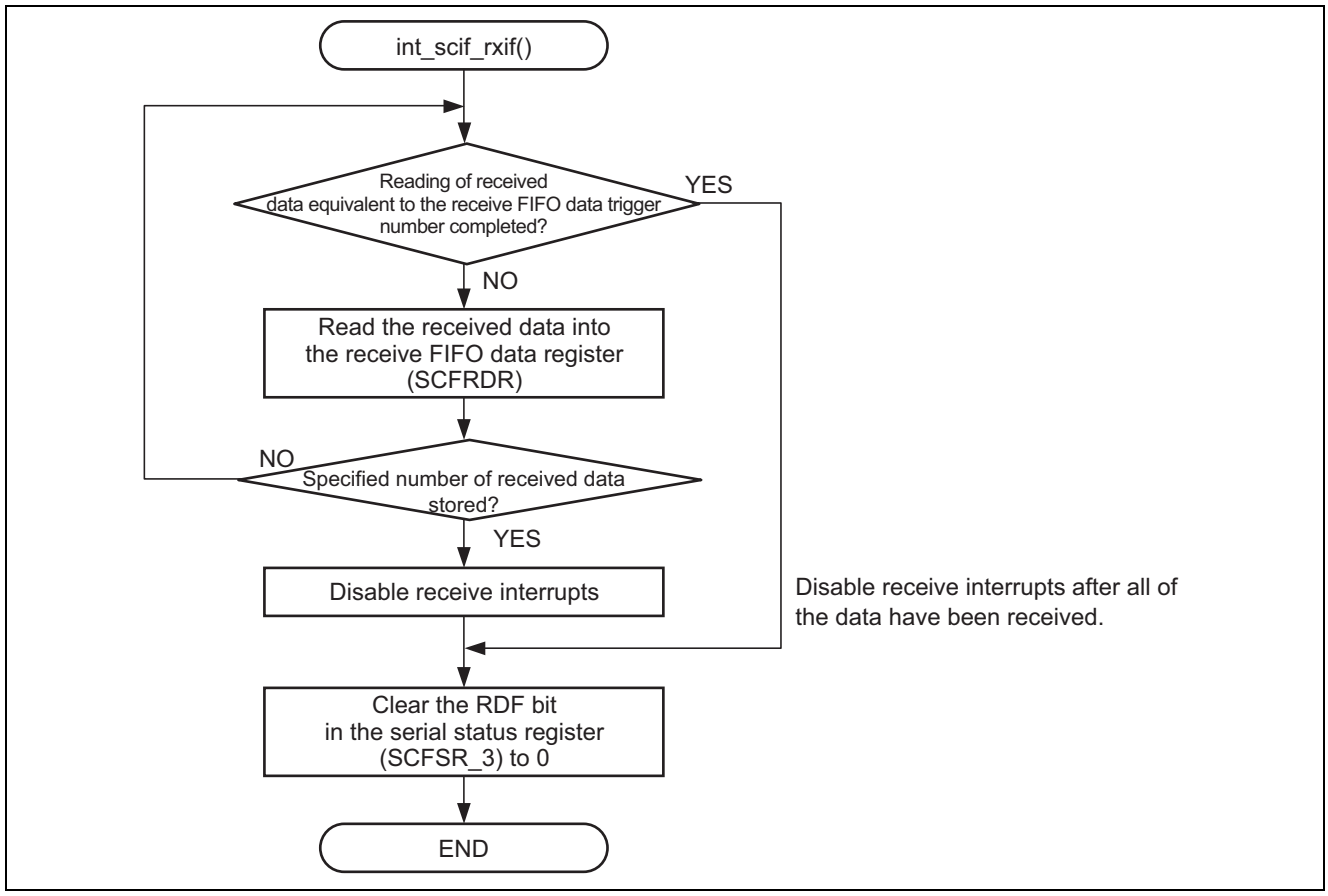

Figure 9 Flow for Handling Receive Interrupts in Clock-Synchronous Mode

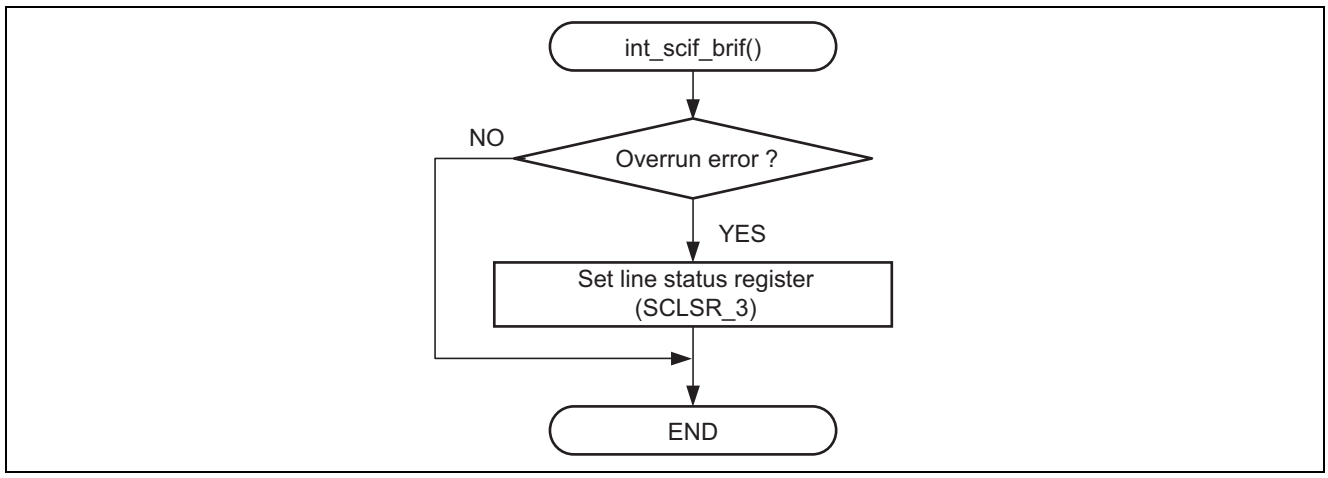

Figure 10 Flow for Handling Receive Error Interrupts in Clock-Synchronous Mode

2.4 Procedure for Processing by the Sample Program

In this sample program, character strings are transmitted and received after initialization of SCIF3 for data reception in clock-synchronous mode.

2.4.1 Clock Pulse Generator (CPG)

Table 3 gives settings for the register of the clock pulse generator in the sample program.

Table 3 Settings for Register in Clock Pulse Generator

Register Name	Address	Setting	Description
Frequency control register (FRQCR)	H'FFFE0010	H'0101	STC [2:0] = B'001: × 1/2 (Bϕ) IFC [2:0] = B'000: × 1 (Iϕ) PFC [2:0] = B'001: × 1/2 (Pϕ)

2.4.2 Standby Control Register

Table 4 gives settings for the standby control register in the sample program.

Table 4 Settings for Standby Control Register

Register Name	Address	Setting	Description
Standby control register 4 (STBCR4)	H'FFFE040C	H'E4	MSTP44 = B'0: SCIF3 operates

2.4.3 Interrupt Controller (INTC)

Table 5 gives settings for the register of the interrupt controller in the sample program.

Table 5 Settings for Register of Interrupt Controller

Register Name	Address	Setting	Description
Interrupt priority register 14 (IPR14)	H'FFFE0C10	H'000F	IPR14 [3:0] = H'F: SCIF3 is at a level 15

2.4.4 Pin Function Controller (PFC)

Table 6 gives settings for the register of the pin function controller in the sample program.

Table 6 Settings for Register of Pin Function Controller

Register Name	Address	Setting	Description
Port E control register L2 (PECRL2)	H'FFFE3A14	H'0555	PE6MD [2:0] = B'101: SCK3 input/output PE5MD [2:0] = B'101: TXD3 output PE4MD [2:0] = B'101: RXD3 input

2.4.5 Serial Communications Interface with FIFO

Table 7 gives settings for the registers of the SCIF in the sample program.

Table 7 Settings for SCIF Register

Register Name	Address	Setting	Description
Serial mode register (SCSMR)	H'FFFE8800	H'0080	C/$\overline{A}$ = B'1: Clock-synchronous mode CHR = B'0: 8-bit data CKS [1:0] = B'00: Pϕ clock
Bit rate register (SCBRR)	H'FFFE8804	D'124	Clock-synchronous mode Bit rate: 100k (bit/s) *1
Serial control register (SCSCR)	H'FFFE8808	H'0002	Initialization RIE = B'0: Disables receive-FIFO-data-full interrupt (RXI), receive-error-interrupt (ERI), and break interrupt (BRI) requests RE = B'0: Disables reception of data REIE = B'0: Disables receive-error-interrupt (ERI) and break interrupt (BRI) requests
			At the time of setting Clock-synchronous mode CKE [1:0] = B'00: Internal clock, SCK pin is used for synchronizing clock output
		H'00FA	When transmitting/receiving operation is enabled TIE = B'1: Enables transmit-FIFO-data-empty interrupt (TXI) request RIE = B'1: Enables receive-FIFO-data-full interrupt (RXI) request TE = B'1: Enables transmission of data RE = B'1: Enables reception of data REIE = B'0: Enables receive-error-interrupt (ERI) and break interrupt (BRI) requests
Serial status register (SCFSR)	H'FFFE8810	H'0060	Initial value TEND = B'1: Transmit end flag TDFE = B'1: Transmit-FIFO-data-empty flag
		H'0000	At the time of setting All flags are cleared to 0.
FIFO control register (SCFCR)	H'FFFE8818	H'0060	Initialization TFRST = B'1: Enables reset operation of transmitted data in the transmit-FIFO-data register RFRST = B'1: Enables reset operation of received data in the receive-FIFO-data register

	H'0080	At the time of setting RTRG [1:0] = B'10: 8 number of received data TTRG [1:0] = B'00: 8 number of transmitted data TFRST = B'0: Disables reset operation of transmitted data in the transmit-FIFO-data register RFRST = B'0: Disables reset operation of received data in the receive-FIFO-data register LOOP = B'0: Disables loop back test

Note: 1. For details on bit rate settings, see the table of bit rates and SCBRR settings in the section on the serial communication interface with FIFO of the *SH7280 Group Hardware Manual*.

3. Documents for Reference

- Software Manual
  SH-2A, SH2A-FPU Software Manual
  The most up-to-date version of this document is available on the Renesas Technology Website.

- Hardware Manual
  SH7280 Group Hardware Manual
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