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April 1st, 2010
Renesas Electronics Corporation

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H8/300L SLP Series

Transition to Watch Mode

Introduction

Transition in operating modes is performed through hardware and software processing: starting from the high-speed active mode to watch mode, then to subactive mode. The system finally goes back to the high-speed active mode.

Target Device

H8/38024

Contents

1. Specifications

1. This sample task shows an example of making transition to the watch mode.
2. The system enters the watch mode by executing a SLEEP instruction when SSBY in SYSCR1 is 1 and TMA3 in TMA is 1 in the active mode.
3. The mode changes to the subactive mode when a Timer A interrupt request is generated in the watch mode while LSON in SYSCR1 is 1.
4. The mode changes to the watch mode again after counting the number of Timer A interrupt requests in the subactive mode.
5. A Timer A interrupt request is generated every 0.5 sec. The LED is turned on and off alternately every 0.5 sec in Timer A interrupt handling.
6. The LED is connected to P92 output pin of port 9.
7. P92 is a large-current port.
8. The mode changes directly from the subactive mode to the high-speed active mode when 120 Timer A interrupt requests have been made, i.e. 60 sec have elapsed, then processing ends.

2. Description of Functions

1. In this sample task, the operating mode is changed to the watch mode, a power down mode. Figure 2.1 is a diagram of mode transition to the watch mode. The function of the watch mode is described below.
   - When a SLEEP instruction is executed in the active or subactive mode while SSBY in SYSCR1 is set to 1 and TMA3 in TMA is set to 1, the mode changes to the watch mode.
   - In the watch mode, the on-chip peripheral functions stop operation except for Timer A.
   - The contents of the CPU registers, internal registers of some of the on-chip peripheral functions, and on-chip RAM are retained as long as the rated voltage is supplied. The I/O ports hold their states they had before the transition.
   - The watch mode can be terminated by an interrupt (IRQ0, Timer A) or by $\overline{\text{RES}}$ pin input. After the termination of the watch mode, the system enters an operating mode according to the combination of LSON in SYSCR1 and MSON in SYSCR2: the high-speed active mode if LSON = 0 and MSON = 0, the medium-speed active mode if LSON = 0 and MSON = 1, or the subactive mode if LSON = 1.
   - When transition is made to the active mode, an interrupt exception handling starts after the time set by STS2 to STS0 in SYSCR1 has elapsed and a stable system clock is supplied to the entire LSI.
   - The watch mode will not be terminated by an interrupt if the I bit in CCR is 1 or an acceptance of interrupts is disabled by the interrupt enable register.
   - In the case of terminating the watch mode by $\overline{\text{RES}}$ pin, the oscillation of the system clock starts when the $\overline{\text{RES}}$ pin is driven "Low". When the $\overline{\text{RES}}$ pin is driven "High" after the specified oscillation stabilization time has elapsed, the CPU starts reset exception handling. It should be noted that the system clock is supplied to the entire LSI at the moment the system clock oscillation has started. The $\overline{\text{RES}}$ pin must be kept "Low" until the oscillation of the system clock stabilizes.
   - In this sample task, the watch mode is terminated by a Timer A interrupt. After the watch mode is terminated, the mode changes to the subactive mode.
   - If a SLEEP instruction is executed in the subactive mode while SSBY is set to 1 and LSON is set to 0 in SYSCR1, MSON is set to 0 and DTON is set to 1 in SYSCR2, and TMA3 in TMA is set to 1, the mode changes directly to the high-speed active mode via the watch mode after the time set by STS2 to STS0 in SYSCR1 has elapsed.
   - The oscillation stabilization time after the termination of subactive mode is set by STS2 to STS0 in SYSCR1.
   - In this sample task, the oscillation stabilization time is set to 1.638 ms.

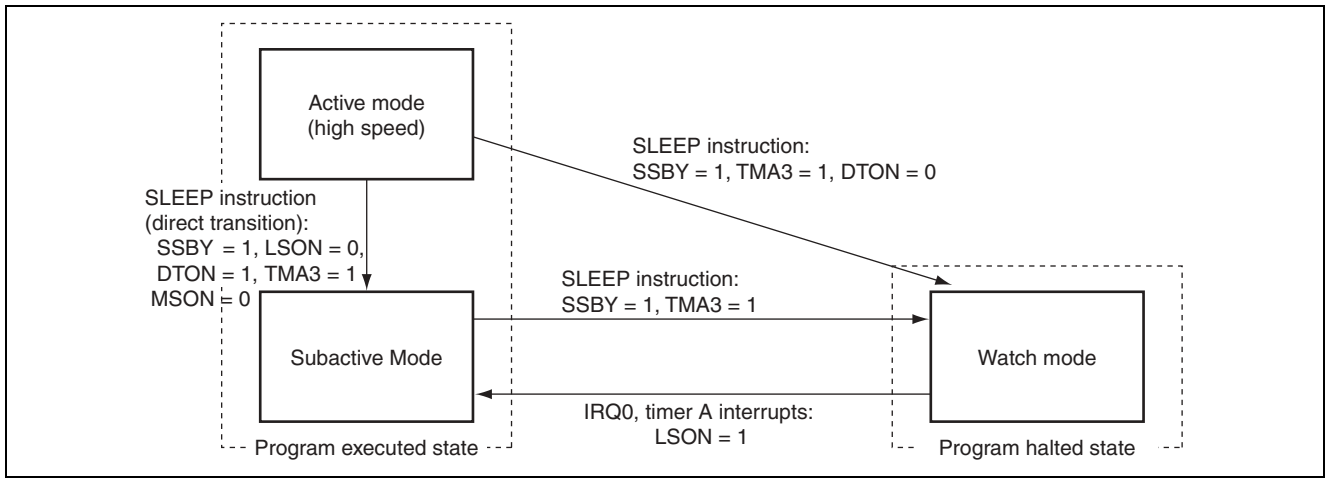


Figure 2.1 Mode Transition from/to Watch Mode

2. Table 2.1 shows the assignment of functions in this sample task. Mode transition to the watch mode is performed by assigning the functions as shown in table 2.1.

Table 2.1 Function Assignment

Function	Assignment
PSW	A 5-bit up counter using the subclock (32.768 kHz)/4 as input.
SYSCR1	Controls power down modes.
SYSCR2	Controls power down modes.
PDR9	P92 output pin data storage
P92	LED output
TMA	Sets Timer A clock time-base function and TCA overflow period.
TCA	An 8-bit up-counter which overflows every 0.5 sec. by the clock time-base function
IRRTA	Indicates whether or not a Timer A interrupt request has been generated.
IRRDT	Indicates whether or not a direct transition interrupt request has been generated.
IENTA	Enables or disables Timer A interrupt requests.
IENDT	Enables direct transition interrupt requests.

3. Principle of Operation

1. Figure 3.1 illustrates the operation of this sample task. Transition to the watch mode is made through hardware and software processing as shown in the figure.

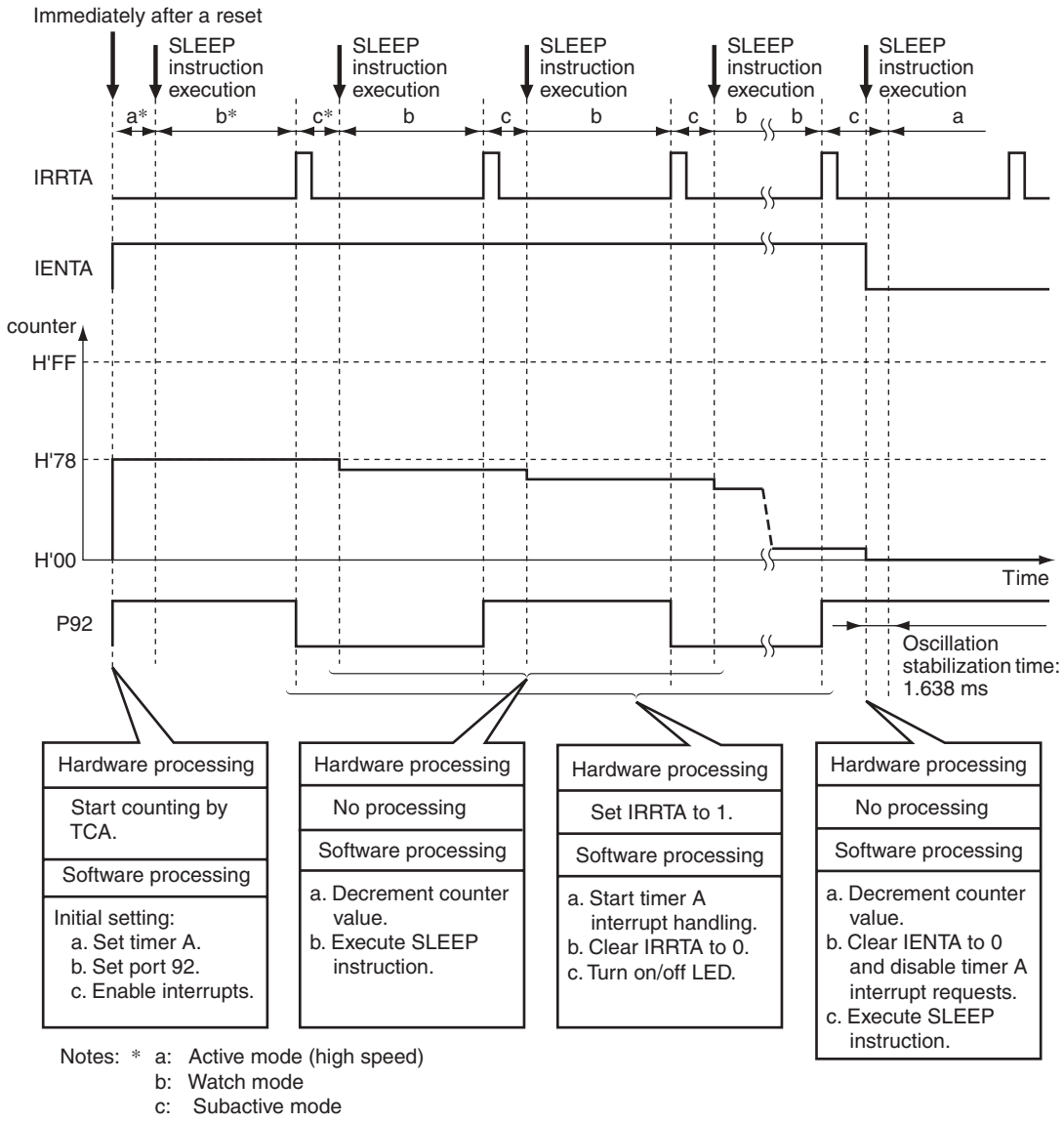


Figure 3.1 Principle of Operation of Making Transition to Watch Mode

4. Description of Software

4.1 Modules

The modules used in this sample task are shown in table 4.1.

Table 4.1 Description of Modules

Module	Label	Function
Main routine	main	Makes settings for Timer A interrupt and port 9, enables interrupts, makes transition to the watch mode, and disables Timer A interrupts.
LED control	taint	A Timer A interrupt handling routine which controls the LED.
Direct transition	dtint	A direct transition interrupt handling routine which clears the direct transition interrupt request flag.

4.2 Arguments

This sample task does not use arguments.

4.3 Internal Registers

Table 4.2 shows the internal registers used in this sample task.

Table 4.2 Description of Internal Registers

Register		Function	Address	Setting
TMA		Timer Mode Register A If TMA = H'19, Timer A function is set to the clock time-base function and TCA overflow period is set to 0.5 sec.	H'FFB0	H'19
TCA		Timer Counter A An 8-bit up-counter which overflows every 0.5 sec by the clock time-base function and uses PSW output clock as input.	H'FFB1	H'00
PDR9	P92	Port Data Register 9 (Port Data Register 92) If P92 = 0, the output level on P92 pin is "Low". If P92 = 1, the output level on P92 pin is "High".	H'FFDC Bit 2	1
SYSCR1	SSBY	System Control Register 1 (Software Standby) If SSBY = 1, a transition is made to the standby mode or watch mode after a SLEEP instruction is executed in the active mode. A transition is made to the subsleep mode after a SLEEP instruction is executed in the subactive mode.	H'FFF0 Bit 7	1
	STS2 STS1 STS0	System Control Register 1 (Standby Timer Select 2, 1, 0) If STS2 = 0, STS1 = 0, and STS0 = 0, oscillation stabilization time after the termination of watch mode is set to 1.638 ms.	H'FFF0 Bit 6 Bit 5 Bit 4	STS2 = 0 STS1 = 0 STS0 = 0
	LSON	System Control Register 1 (Low Speed ON Flag) If LSON = 0, the CPU operating clock is set to the system clock after the watch mode is terminated. If LSON = 1, the CPU operating clock is set to the subsystem clock after the watch mode is terminated.	H'FFF0 Bit 3	1

Register		Function	Address	Set Value
SYSCR2	DTON	System Control Register 2 (Direct Transfer ON Flag) If DTON = 0, a transition is made to the standby, watch or sleep mode when a SLEEP instruction is executed in the active mode. a transition is made to the watch or subsleep mode when a SLEEP instruction is executed in the subactive mode. If DTON = 1, A direct transition is made to the high-speed active mode (when SSBY = 1, TMA3 = 1,LSON = 0, MSON = 0) or to the medium-speed active mode (when SSBY = 1, TMA3 = 1, LSON = 0, MSON = 1) when a SLEEP instruction is executed in the subactive mode.	H'FFF1 Bit 3	0
	MSON	System Control Register 2 (Medium Speed ON Flag) If MSON = 0, the system operates in the high-speed active mode after the standby, watch or sleep mode is terminated. The system operates in the high-speed sleep mode if a SLEEP instruction is executed in the active mode.	H'FFF1 Bit 2	0
	SA1 SA0	System Control Register 2 (Subactive Mode Clock Select 1, 0) If SA1 = 0 and SA0 = 0, the CPU operating clock in the subactive mode is set to $\phi_w/8$.	H'FFF1 Bit 1 Bit 0	SA1 = 0 SA0 = 0
IENR1	IENTA	Interrupt Enable Register 1 (Timer A Interrupt Enable) If IENTA = 0, Timer A interrupt requests are disabled. If IENTA = 1, Timer A interrupt requests are enabled.	H'FFF3 Bit 7	1
IENR2	IENDT	Interrupt Enable Register 2 (Direct Transition Interrupt Enable) If IENDT = 0, interrupt requests by direct transition are disabled. If IENDT = 1, interrupt requests by direct transition are enabled.	H'FFF4 Bit 7	1
IRR1	IRRTA	Interrupt Request Register 1 (Timer A Interrupt Request Flag) If IRRTA = 0, a Timer A interrupt is not requested. If IRRTA = 1, a Timer A interrupt has been requested.	H'FFF6 Bit 7	0
IRR2	IRRDT	Interrupt Request Register 2 (Direct Transition Interrupt Request Flag) If IRRDT = 0, an interrupt by direct transition is not requested. If IRRDT = 1, an interrupt by direct transition has been requested	H'FFF7 Bit 7	0

4.4 Description of RAM

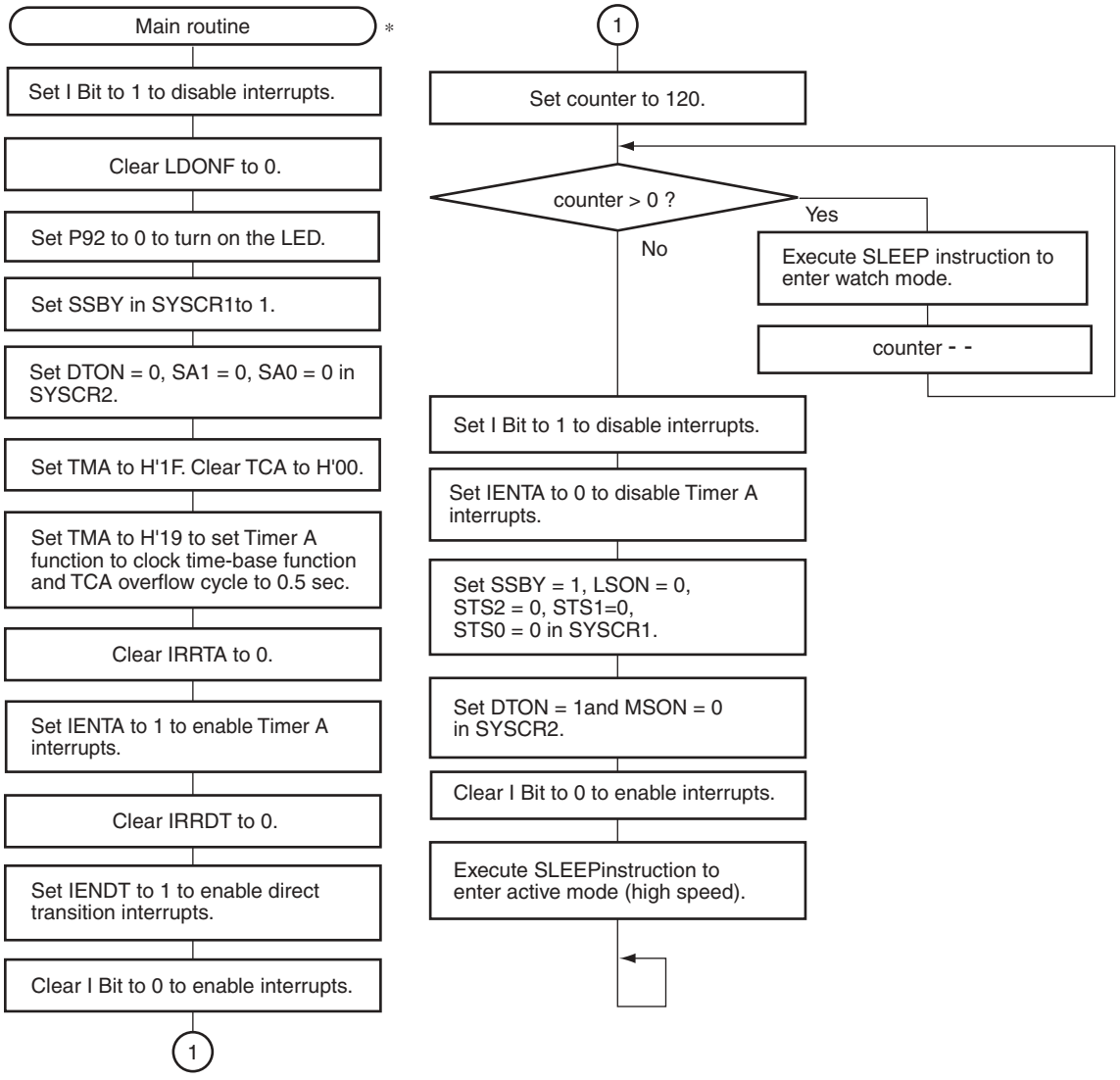
Table 4.3 describes the RAM area used in this sample task.

Table 4.3 Description of RAM

Label		Function	Address	Used in
USRF	LDONF	Flag to judge whether the LED is on or off.	H'FB80 Bit 0	LED control

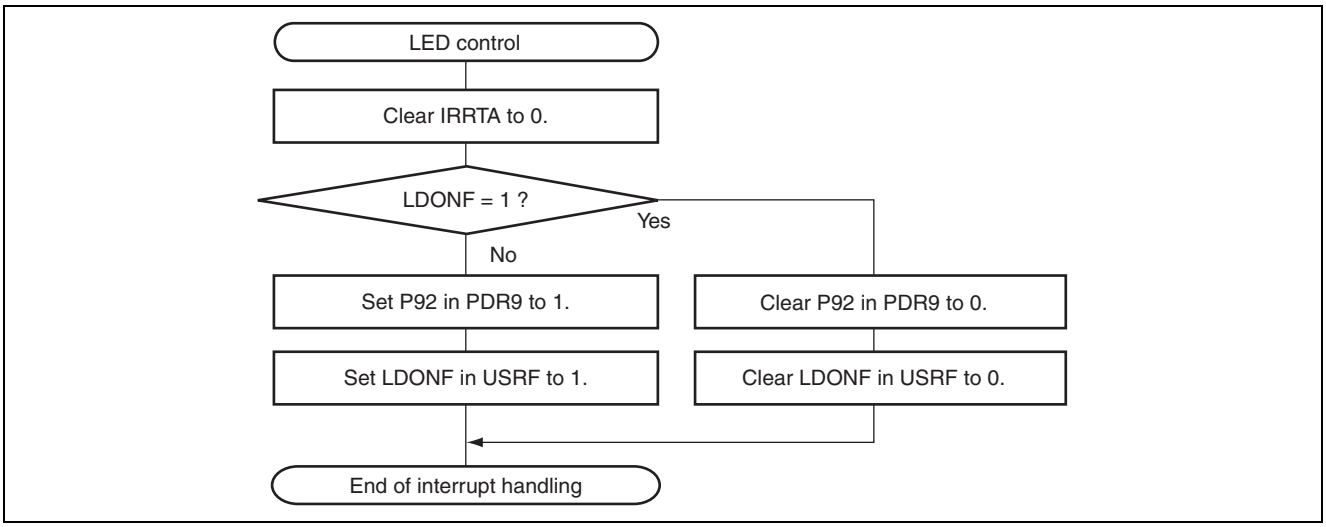
5. Flowchart

1. Main routine

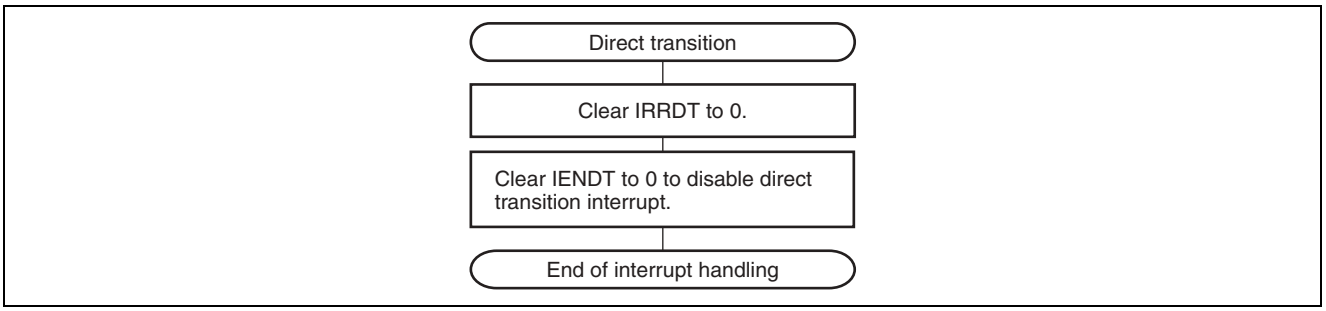


Note: * In this sample task, the stack pointer is set in INIT.SRC (assembly language).

2. Timer A interrupt handling routine



3. Direct transition interrupt handling routine



6. Program Listing

INIT.SRC (Program listing)

```
    .EXPORT   _INIT
    .IMPORT   _main
;
    .SECTION  P,CODE
_INIT:
    MOV.W     #H'FF80,R7
    LDC.B     #B'10000000,CCR
    JMP       @_main
;
    .END
```

```
/************************************************************************************************************************/
/*                                                                                                                      */
/*  H8/300L Super Low Power Series                                                                                      */
/*      -H8/38024 Series-                                                                                               */
/*  Application Note                                                                                                    */
/*                                                                                                                      */
/*  'Transition to Watch Mode'                                                                                          */
/*                                                                                                                      */
/*  Function                                                                                                            */
/*  : Power-Down Mode                                                                                                   */
/*     Watch Mode                                                                                                       */
/*                                                                                                                      */
/*  External Clock : 10MHz                                                                                              */
/*  Internal Clock : 5MHz                                                                                               */
/*  Sub Clock      : 32.768kHz                                                                                          */
/*                                                                                                                      */
/************************************************************************************************************************/

#include    <machine.h>

/************************************************************************************************************************/
/*  Symbol Definition                                                                                                   */
/************************************************************************************************************************/
struct BIT {
    unsigned char   b7:1;       /* bit7 */
    unsigned char   b6:1;       /* bit6 */
    unsigned char   b5:1;       /* bit5 */
    unsigned char   b4:1;       /* bit4 */
    unsigned char   b3:1;       /* bit3 */
    unsigned char   b2:1;       /* bit2 */
    unsigned char   b1:1;       /* bit1 */
    unsigned char   b0:1;       /* bit0 */
};

#define     TMA         *(volatile unsigned char *)0xFFB0       /* Timer Mode Register A                */
#define     TCA         *(volatile unsigned char *)0xFFB1       /* Timer Counter A                      */
#define     PDR9_BIT    (*(struct BIT *)0xFFDC)                 /* Port Data Register 9                 */
#define     P92         PDR9_BIT.b2                             /* Port Data Register 92                */
#define     SYSCR1      *(volatile unsigned char *)0xFFF0       /* System Control Register 1            */
#define     SYSCR1_BIT  (*(struct BIT *)0xFFF0)                 /* System Control Register 1            */
#define     SSBY        SYSCR1_BIT.b7                           /* Software Standby                     */
#define     STS2        SYSCR1_BIT.b6                           /* Standby Timer Select 2               */
#define     STS1        SYSCR1_BIT.b5                           /* Standby Timer Select 1               */
#define     STS0        SYSCR1_BIT.b4                           /* Standby Timer Select 0               */
```

```
#define     LSON        SYSCR1_BIT.b3                       /* Low Speed On Flag                        */
#define     MA1         SYSCR1_BIT.b1                       /* Active Mode Clock Select 1               */
#define     MA0         SYSCR1_BIT.b0                       /* Active Mode Clock Select 0               */
#define     SYSCR2      *(volatile unsigned char *)0xFFF1   /* System Control Register 2                */
#define     SYSCR2_BIT  (*(struct BIT *)0xFFF1)             /* System Control Register 2                */
#define     NESEL       SYSCR2_BIT.b4                       /* Noise Elimination Sampling               */
                                                            /*                          Frequency Select */
#define     DTON        SYSCR2_BIT.b3                       /* Direct Transfer On Flag                  */
#define     MSON        SYSCR2_BIT.b2                       /* Middle Speed On Flag                     */
#define     SA1         SYSCR2_BIT.b1                       /* Subactive Mode Clock Select 1            */
#define     SA0         SYSCR2_BIT.b0                       /* Subactive Mode Clock Select 0            */
#define     IENR1_BIT   (*(struct BIT *)0xFFF3)             /* Interrupt Enable Register 1              */
#define     IENTA       IENR1_BIT.b7                        /* Timer A Interrupt Enable                 */
#define     IENR2_BIT   (*(struct BIT *)0xFFF4)             /* Interrupt Enable Register 2              */
#define     IENDT       IENR2_BIT.b7                        /* Direct Transfer Interrupt Enable         */
#define     IRR1_BIT    (*(struct BIT *)0xFFF6)             /* Interrupt Request Register 1             */
#define     IRRTA       IRR1_BIT.b7                         /* Timer A Interrupt Request Flag           */
#define     IRR2_BIT    (*(struct BIT *)0xFFF7)             /* Interrupt Request Register 2             */
#define     IRRDT       IRR2_BIT.b7                         /* Direct Transfer Interrupt Request Flag   */

#pragma interrupt   (taint)
#pragma interrupt   (dtint)
/************************************************************************************************************/
/*  Function define                                                                                         */
/************************************************************************************************************/
extern void INIT ( void );                                  /* SP Set                                   */
void        main ( void );
void        taint ( void );
void        dtint ( void );

/************************************************************************************************************/
/*  RAM define                                                                                              */
/************************************************************************************************************/
unsigned char   USRF;                                       /* User Flag Area                           */

#define     USRF_BIT    (*(struct BIT *)&USRF)
#define     LDONF       USRF_BIT.b0                         /* Switch On Flag                           */

/************************************************************************************************************/
/*  Vector Address                                                                                          */
/************************************************************************************************************/
#pragma section     V1                                      /* Vector Section Set                       */
void (*const VEC_TBL1[])(void) = {
    INIT                                                    /* 0x0000 Reset Vector                      */
};
#pragma section     V2                                      /* Vector Section Set                       */
void (*const VEC_TBL2[])(void) = {
    taint                                                   /* 0x0016 timer A Interrupt Vector          */
};
#pragma section     V3                                      /* Vector Section Set                       */
void (*const VEC_TBL3[])(void) = {
    dtint                                                   /* 0x0028 Direct Transfer Interrupt Vector  */
};

#pragma section                                             /* P                                        */
```

```
/*****************************************************************************************************************/
/*  Main Program                                                                                                 */
/*****************************************************************************************************************/
void    main ( void )
{
    int counter;

    set_imask_ccr(1);                                   /* Interrupt Disable                    */

    P92 = 0;                                            /* Turn On LED                          */
    LDONF = 0;                                          /* Initialize LDONF                     */

    SYSCR1 = 0x8F;                                      /* Set SYSCR1                           */
    SYSCR2 = 0xE0;                                      /* Set SYSCR2                           */

    TMA = 0x1F;                                         /* Initialize TCA                       */
    TMA = 0x19;                                         /* Initialize TCA Overflow Period       */
    IRRTA = 0;                                          /* Clear IRRTA                          */
    IENTA = 1;                                          /* Timer A Interrupt Enable             */

    IRRDT = 0;                                          /* Clear IRRDT                          */
    IENDT = 1;                                          /* Direct Transfer Interrupt Enable     */

    set_imask_ccr(0);                                   /* Interrupt Enable                     */

    for(counter = 120; counter > 0; counter--){
        sleep();                                        /* Transition to Watch Mode             */
    }

    set_imask_ccr(1);                                   /* Interrupt Disable                    */

    IENTA = 0;
    SYSCR1 = 0x87;                                      /* Set SYSCR1                           */
    SYSCR2 = 0xE8;                                      /* Set SYSCR2                           */

    set_imask_ccr(0);                                   /* Interrupt Enable                     */

    sleep();                                            /* Transition to Sleep Mode             */

    while(1){
        ;
    }
}
```

```
/*****************************************************************************************************************/
/*  Timer A Interrupt                                                                                            */
/*****************************************************************************************************************/
void    taint ( void )
{
    IRRTA = 0;                                          /* Clear IRRTA                                  */

    if(LDONF = =  1){                                   /* LDONF = "1" ?                                */
        P92 = 0;                                        /* Turn Off LED                                 */
        LDONF = 0;                                      /* Clear LDONF                                  */
    }
    else{
        P92 = 1;                                        /* Turn On LED                                  */
        LDONF = 1;                                      /* Set LDONF                                    */
    }
}

/*****************************************************************************************************************/
/*  Direct Transfer Interrupt                                                                                    */
/*****************************************************************************************************************/
void    dtint ( void )
{
    IRRDT = 0;                                          /* Clear IRRDT                                  */
    IENDT = 0;                                          /* Direct Transfer Interrupt Enable             */
}
```

Link address specifications

Section Name	Address
CV1	H'0000
CV2	H'0016
CV3	H'0028
P	H'0100
B	H'FB80

Revision Record

Rev.	Date	Description	
		Page	Summary
1.00	Dec.19.03	—	First edition issued

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