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R32C/100 Series

Stop Mode Set-up

1. Abstract

This document describes the settings and shows an example application for entering stop mode.

2. Introduction

The application described in this document applies to the following MCU:

- MCU: R32C/118 Group

This program can be used with other R32C/100 Series MCUs which have the same special function registers (SFRs) as the R32C/118 Group. Check the manual for any additions or modifications to functions. Careful evaluation is recommended before using this application note.

3. Overview

Stop mode is a low power consumption function that stops all clocks in the MCU.

In stop mode, all oscillation is stopped. Therefore, as the CPU clock and peripheral function clocks are stopped, the CPU and peripheral functions operated by these clocks are also stopped. This mode consumes the least amount of power.

To enter stop mode, execute the STOP instruction while in either low-speed mode or low power consumption mode.

Use a hardware reset, NMI, low voltage detect interrupt, or peripheral function interrupt to exit stop mode.

This document describes the settings to enter stop mode, and shows how to exit stop mode using the INT0 interrupt (peripheral interrupt source).

The figure below shows the transition to stop mode.

Note:
1. The sample program in this application note stops the main regulator when entering stop mode, further reducing power consumption.

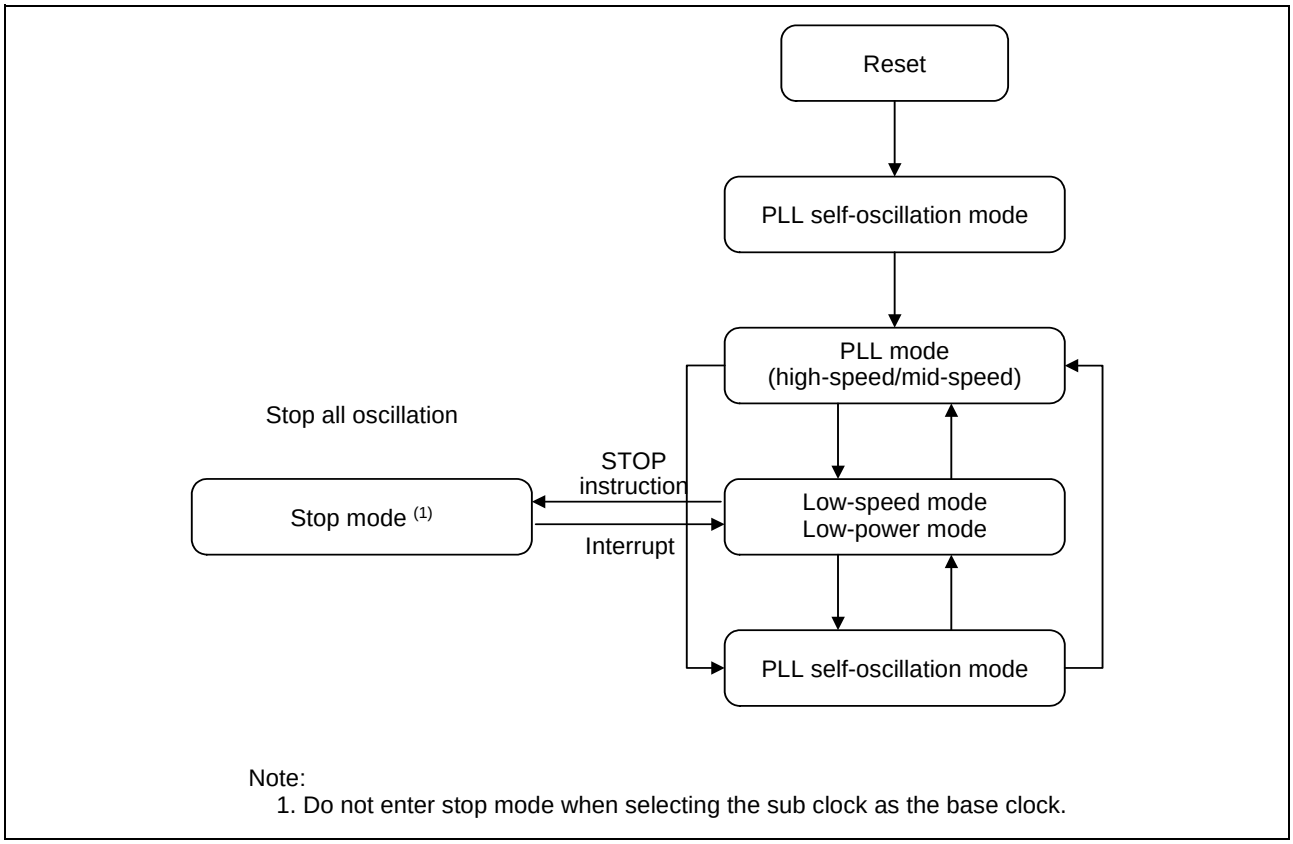


Figure 3.1 Transition to Stop Mode

4. Setting

This section describes how to enter stop mode.

4.1 Entering Stop Mode

The MCU enters stop mode by executing the STOP instruction. Follow the steps below to enter stop mode.

• Initial Setting
After setting the interrupt priority level for wake-up to 7 (bits RLVL2 to RLVL0 in registers RIPL1 and RIPL2), set each interrupt priority level.

• Before Entering Stop Mode
(1) Set the I flag to 0.
(2) Set the interrupt request level for each interrupt source (interrupt number from 1 to 127) to 0, if its interrupt request level is not 0.
(3) Perform a dummy read of any interrupt control registers.
(4) Set the processor interrupt priority level (IPL) in the flag register (FLG) to 0.
(5) Enable interrupts temporarily by executing the following instructions:
FSET I
NOP
NOP
FCLR I
(6) Set the interrupt request level for the interrupt to exit wait mode. Do not rewrite the interrupt control register after this step.
(7) Set the IPL in the flag register.
(8) Set the interrupt priority level for resuming to the same level as the IPL.
Interrupt request level of the interrupt used to exit wait mode > IPL = Interrupt priority level for resuming.
(9) Change the base clock to main clock divided by 256 (f256) or on-chip oscillator clock divided by 4 (fOCO4) (1).
(10) Set the I flag to 1.
(11) Execute the STOP instruction.

After Exiting Stop Mode
After exiting stop mode, immediately set the interrupt priority level for wake-up to 7.

Note:
1. When using the oscillation stop detect function, change the base clock after setting the CM20 bit in the CM2 register to 0 (oscillation stop detect function disabled).

The Table 4.1 lists the Interrupt Priority Level of Interrupt Used To Exit Stop Mode and the IPL Setting Value.

Table 4.1 Interrupt Priority Level of Interrupt Used To Exit Stop Mode and the IPL Setting Value

Interrupt priority level of interrupt used to exit stop mode	IPL
7	3

4.2 Setting the I Flag and IPL and Using the STOP Instruction

The asm function is used in setting the I flag and IPL and in using the STOP instruction. See the figures below for more details.

```
asm("FCLR   I");
        Set the I flag to 0.

asm("FSET   I");
        Set the I flag to 1.
```

Figure 4.1 I Flag Settings Using the asm Function

```
asm("LDIPL   #3");
        Set IPL to 3.
```

Figure 4.2 IPL Settings Using the asm Function

```
asm("STOP");
        Execute the STOP instruction.
```

Figure 4.3 Executing the STOP Instruction Using the asm Function

4.3 Exiting Stop Mode

Exit stop mode using a hardware reset, NMI, low voltage detect interrupt, or peripheral function interrupt.

When exiting stop mode using a hardware reset or NMI (but not a peripheral function interrupt), after setting bits ILVL2 to ILVL0 in the peripheral function interrupt to 000b (interrupt disabled), execute the STOP instruction.

When using a peripheral function interrupt or NMI to exit stop mode, the CPU clock is the same clock as the CPU clock when executing the STOP instruction.

Table 4.2 Interrupts and Conditions for Exiting Stop Mode

Interrupt	Condition
NMI	
Low voltage detect interrupt	
External interrupt	
Key input interrupt	
Timer A interrupt Timer B interrupt	When counting an external pulse with a frequency of 100 Hz or less in event counter mode
Serial interface interrupt (excluding UART7 and UART8)	When using an external clock
I^2C bus line interrupt	
CAN wake-up interrupt	

4.4 Notes on Setting Protected Registers

This application note describes using the protect function to set protected registers.

The protect function protect important registers from being easily rewritten. Protected registers can be rewritten after disabling the protect function.

The table below shows the protect registers and protected registers.

Table 4.3 The Protect Register and Protected Registers

Protect Register	Write Disabled/Enabled	Protected Registers
PRCR	PRC0 Bit 0: Write disabled 1: Write enabled	CM0 to CM2, and PM3
	PRC1 Bit 0: Write disabled 1: Write enabled	PM0, PM2, CSOP0 to CSOP2, INVC0 to INVC1, IOBC, and I2CMR
	PRC2 Bit 0: Write disabled 1: Write enabled	PLC0 to PLC1, and PD9, P9_iS (i = 0 to 7)
PRCR2	PRC27 Bit 0: Write disabled 1: Write enabled	CM3
PRCR3	PRC31 Bit 0: Write disabled 1: Write enabled	VRCR, LVDC, and DVCR
PRR	b7 to b0 Not AAh: Write disabled AAh: Write enabled	CCR, FMCR, PBC, FEBC0, FEBC3, EBC0 to EBC3, CB01, CB12, and CB23

4.5 Setting Overview

Figure 4.4 shows the Procedure for Entering Stop Mode and Figure 4.5 shows the Procedure for Entering Stop Mode. Refer to 4.6 “Setting Overview” for details.

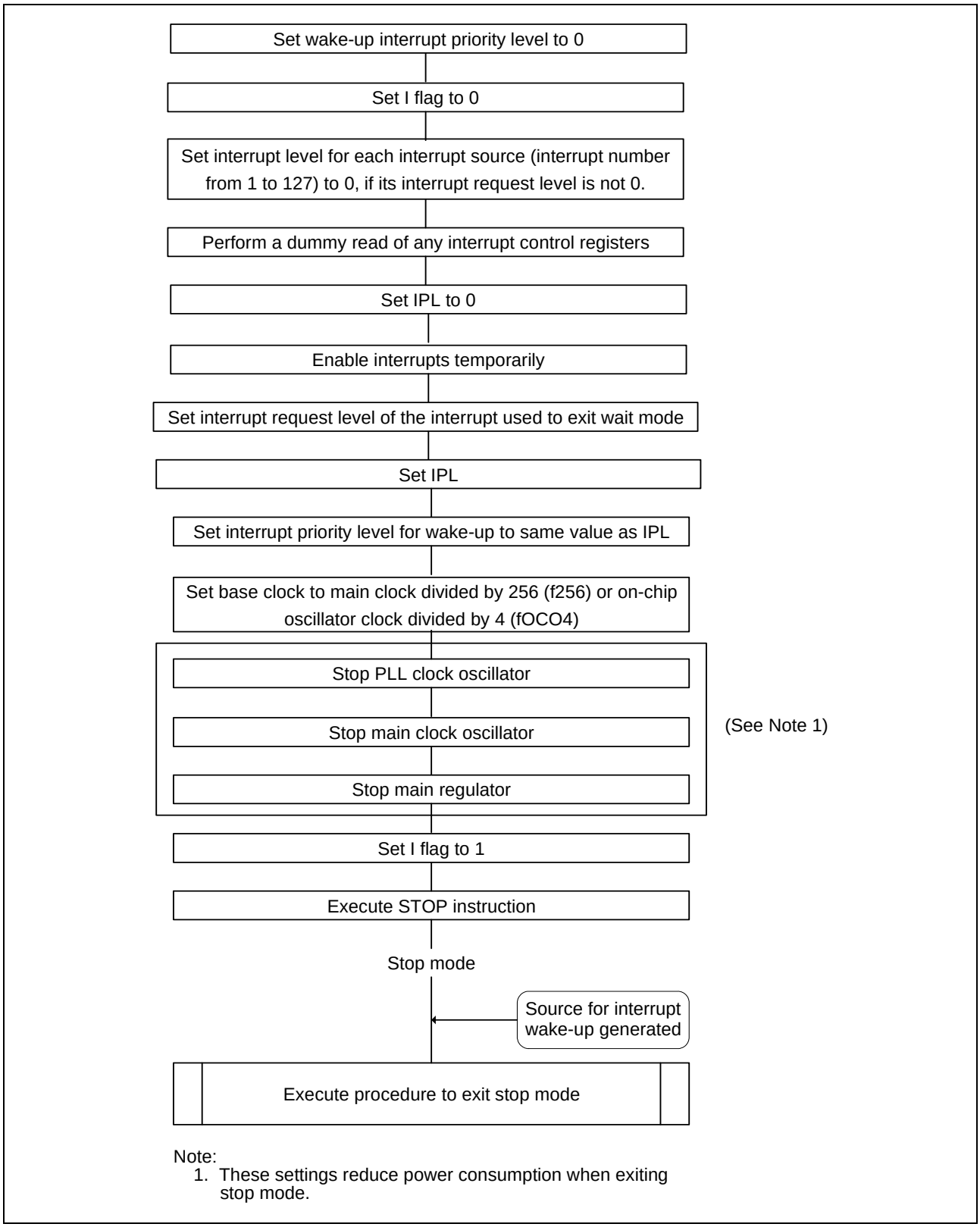
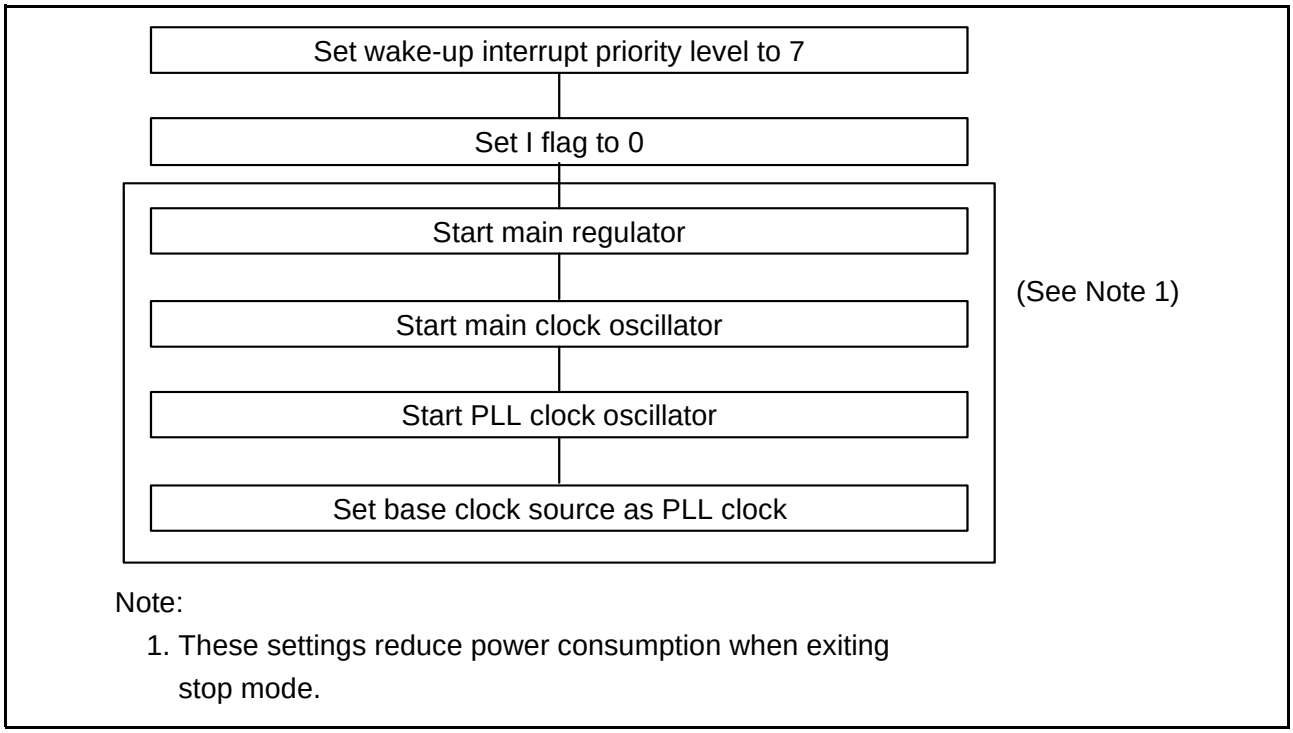


Figure 4.4 Procedure for Entering Stop Mode



Note:
1. These settings reduce power consumption when exiting stop mode.

Figure 4.5 Procedure for Exiting Stop Mode

4.6 Setting Overview

4.6.1 Procedure for Entering Stop Mode

Set the interrupt priority level for wake-up.

b7 b0: X X 0 X 0 1 1 1 — Wake-up Interrupt Priority Level Control Register i (i = 1, 2) (RIPLi)

- RLVL2 to RLVL0 — Interrupt Priority Level for Wake-up Select Bit
  - 111b: Level 7
- FSIT — Fast Interrupt Select Bit
  - 0: Use interrupt priority level 7 for interrupt
- DMAII — DMAII Select Bit
  - 0: Use interrupt priority level 7 for interrupt

Disable the interrupt.

```
asm("FCLR   I");
```

Set the interrupt request level for each interrupt source (interrupt number from 1 to 127) to 0, if its interrupt request level is not 0.

b7 b0: X X X X 0 - - - — Interrupt Control Register
TA0IC to TA4IC, TB0IC to TB5IC, S0TIC to S8TIC, S0RIC to S8RIC, BCN0IC to BCN6IC, DM0IC to DM3IC, AD0IC, KUPIC, IIO0IC to IIO11IC, I2CIC, I2CLIC, C0FTIC to C1FTIC, C0FRIC to C1FRIC, C0TIC to C1TIC, C0RIC to C1RIC, C0EIC to C1EIC, C0WIC to C1WIC

- ILVL2 to ILVL0 — Interrupt Request Level Select Bit
  - Select a level
- IR — Interrupt Request Flag
  - 0: No interrupt requested

(Set the IR bit to 0)

- Set to 0.

b7 b0: X X - - 0 - - - — Interrupt Control Register (INT0IC to INT8IC)

- ILVL2 to ILVL0 — Interrupt Request Level Select Bit
  - Select a level
- IR — Interrupt Request Flag
  - 0: No interrupt requested

(Set the IR bit to 0)

- POL — Polarity Switch Bit
  - 0: Falling edge or low level signal selected
  - 1: Rising edge or high level signal selected
- LVS — Level/Edge Sensitive Select Bit
  - 0: Edge sensitive
  - 1: Level sensitive
- Set to 0.

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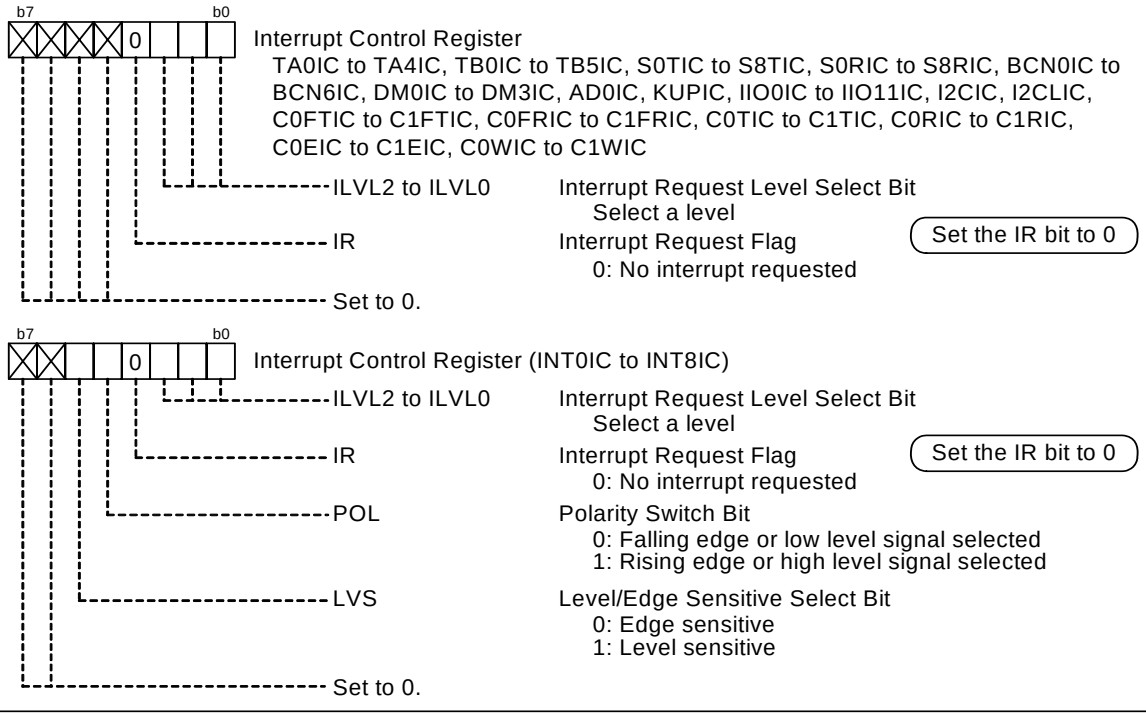
Set the interrupt request level of the interrupt used to exit wait mode.



Perform a dummy read of any interrupt control registers.

Set the IPL to 0.

```
asm("LDIPL    #0")
```

Enable interrupts temporarily by executing the following instructions:

```
asm(" FSET    I")
asm("NOP")
asm("NOP");
asm("FCLR    I"):
```

Continued on next page

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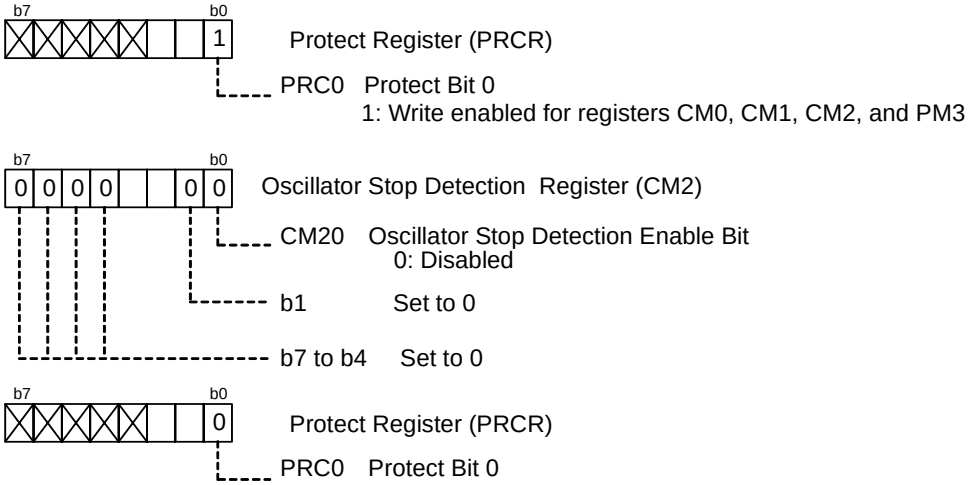
Set the IPL.

```
asm("LDIPL    #3");
```

Set wake-up interrupt priority level to same value as IPL.
Interrupt request level of the interrupt used to exit wait mode > IPL = Interrupt priority level for resuming

When using the oscillation stop detector, disable the function before changing the base clock.



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Set the base clock as on-chip oscillator divided by 4 (fOCO4).

b7 b0

1	0	0	0	0	0	0	0

Protect Register 2 (PRCR2)

PRC27 CM3 Protect Bit
1: Write enabled

b7 b0

X	X	X	X	X	X	0	0

Low-Speed Mode Clock Control Register (CM3)

CM31 to CM30 Low Speed Mode Base Clock Select Bit
10b:fOCO4 (on-chip oscillator divided by 4)

b7 b0

0	0	0	0	0	0	0	0

Protect Register 2 (PRCR2)

PRC27 CM3 Protect Bit
0: Write disabled

b7 b0

Protect Register (PRR)

PRR Protect Release Register
AAh: Write enabled

b7 b0

1	0						

Clock Control Register (CCR)

BCD1 to BCD0 Base Clock Divide Ratio Select Bit

00b:Divide-by 6
01b:Divide-by 4
10b:Divide-by 3
11b:Divide-by 2

CCD1 to CCD0 CPU Clock Divide Ratio Select Bit
00b: Divide-by 4
01b: Divide-by 3
10b: Divide-by 2
11b: No division

PCD1 to PCD0 Peripheral Bus Clock Divide Ratio Select Bit
00b: Do not use this combination
01b: Divide-by 2
10b: Divide-by 3
11b: Divide-by 4

BCS Base Clock Source Select Bit (1)
1:fC, fOCO4 or f256

Note:
1. To set this bit to 1, a 32-bit write access to addresses 0004h to 0007h should be performed.
Example: asm("OR.L #00000080h,00000004h");

b7 b0

Protect Register (PRR)

PRR Protect Register (PRR)
Value other than AAh: Write disabled

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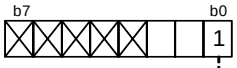
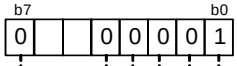
Stop the PLL clock oscillator.



Protect Register (PRCR)

PRC0 Enable to write to registers CM0, CM1, CM2, and PM3
1: Write enabled



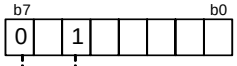
System Clock Control Register 1(CM1)

CM10 PLL Clock Oscillator Stop Bit (1)
1: Stop PLL clock oscillator

Set to 0

Note:
1. When the BCS bit in the CCR register is set to 0 (PLL clock selected as base clock source), the CM10 bit cannot be set to 1.
The PM21 bit in the PM2 register is set to 1 (clock change disabled), the CM10 bit is not changed by a write access.

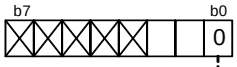
Stop the main clock oscillator.



System Clock Control Register 0(CM0)

CM05 Main Clock Oscillator (XIN-XOUT) Stop Bit (1)
1: Stop main clock oscillator

Set to 0



Protect Register (PRCR)

PRC0 Enable to write to registers CM0, CM1, CM2, and PM3
0: Write disabled

Note:
1. When the PM21 bit in the PM2 register is 1 (clock change disabled), neither the CM02 bit nor the CM05 bit changes, even if written to. It cannot detect whether or not the main clock oscillator.
When the CM05 bit is set to 1, the clock applied to the XOUT pin becomes high. Since the on-chip feedback resistor remains connected, the XIN pin is connected to the XOUT pin via the feedback resistor.

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Stop the main regulator.

b7 b0

0	0	0	0	0	0	1	0

Protect Register 3 (PRCR3)

Set to 0

PRC31 Protect Bit 31 (Enable to write to registers VRCR, LVDC, and DVCR)
1: Write enabled

Set to 0

b7 b0

X	X	X	X	X	X	X	1

Voltage Regulator Control Register (VRCR) (1)

MRS Main Regulator Shut-down Bit
1: Stop main regulator (2)

b7 b0

0	0	0	0	0	0	0	0

Protect Register 3 (PRCR3)

Set to 0

PRC31 Protect Bit 31 (Enable to write to registers VRCR, LVDC, and DVCR)
0: Write disabled

Set to 0

Notes:
1. This bit is fixed to 0 if the CM05 bit in the CM0 register is 0 (main clock oscillator active) or the CM10 bit in the CM1 register is 0 (PLL clock oscillator active) .
2. While the main regulator is stopped, do not rewrite the flash memory.

Set the I flag to 1.
asm("FSET I");

Execute the STOP instruction.
asm("STOP");

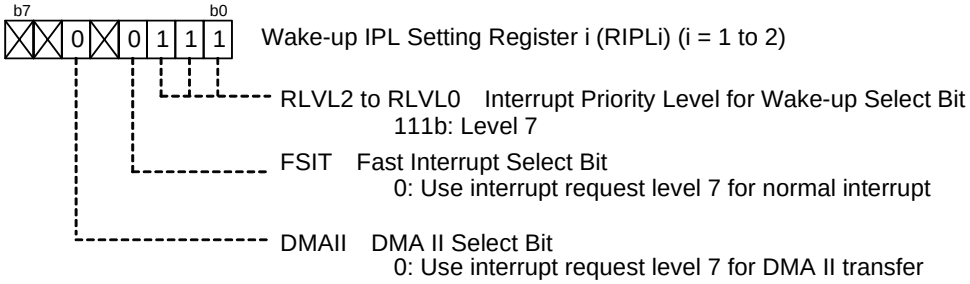
Stop mode

4.6.2 Procedure for Exiting Stop Mode

Stop mode

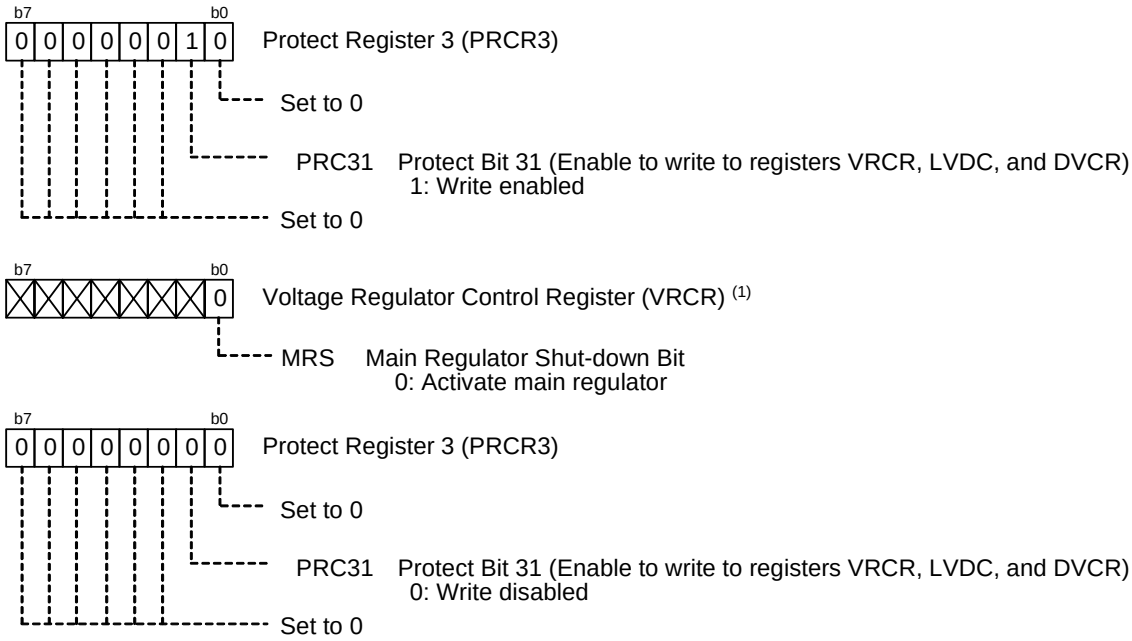
Source for interrupt wake-up generated

Set the wake-up interrupt priority level to 7.



Set the I flag to 1.
asm("FCLR I");

Activate the main regulator.



Note:
1. This bit is fixed to 0 if the CM05 bit in the CM0 register is 0 (main clock oscillator active) or the CM10 bit in the CM1 register is 0 (PLL clock oscillator active) .

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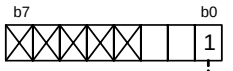
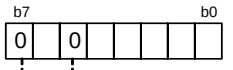
Start the main clock oscillator.



Protect Register (PRCR)

PRC0 Enable to write to registers CM0, CM1, CM2, and PM3
1: Write enabled



System Clock Control Register 0 (CM0)

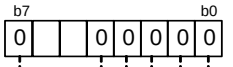
CM05 Main Clock Oscillator (XINXOUT) Stop Bit (1)
0: Start main clock oscillator

Set to 0

Note:
1. When the PM21 bit in the PM2 register is 1 (clock change disabled), neither the CM02 bit nor the CM05 bit changes, even if written to.
This bit stops the main clock oscillator when entering low power mode. It cannot detect whether or not the main clock oscillator stops. When the CM05 bit is set to 1, the clock applied to the XOUT pin becomes high.
Since the on-chip feedback resistor remains connected, the XIN pin is connected to the XOUT pin via the feedback resistor.

* If needed, wait for the main clock oscillator stabilization time.

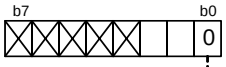
Start the PLL clock oscillator.



System Clock Control Register 1 (CM1)

CM10 PLL Clock Oscillator Stop Bit (1)
0: Start PLL clock oscillator

Set to 0



Protect Register (PRCR)

PRC0 Enable to write to registers CM0, CM1, CM2, and PM3
0: Write disabled

Note:
1. When the BCS bit in the CCR register is set to 0 (PLL clock selected as base clock source), the CM10 bit cannot be set to 1.
The PM21 bit in the PM2 register is set to 1 (clock change disabled), the CM10 bit is not changed by a write access.

* If needed, wait for the PLL clock oscillator stabilization time tLOCK(PLL)(1 ms).

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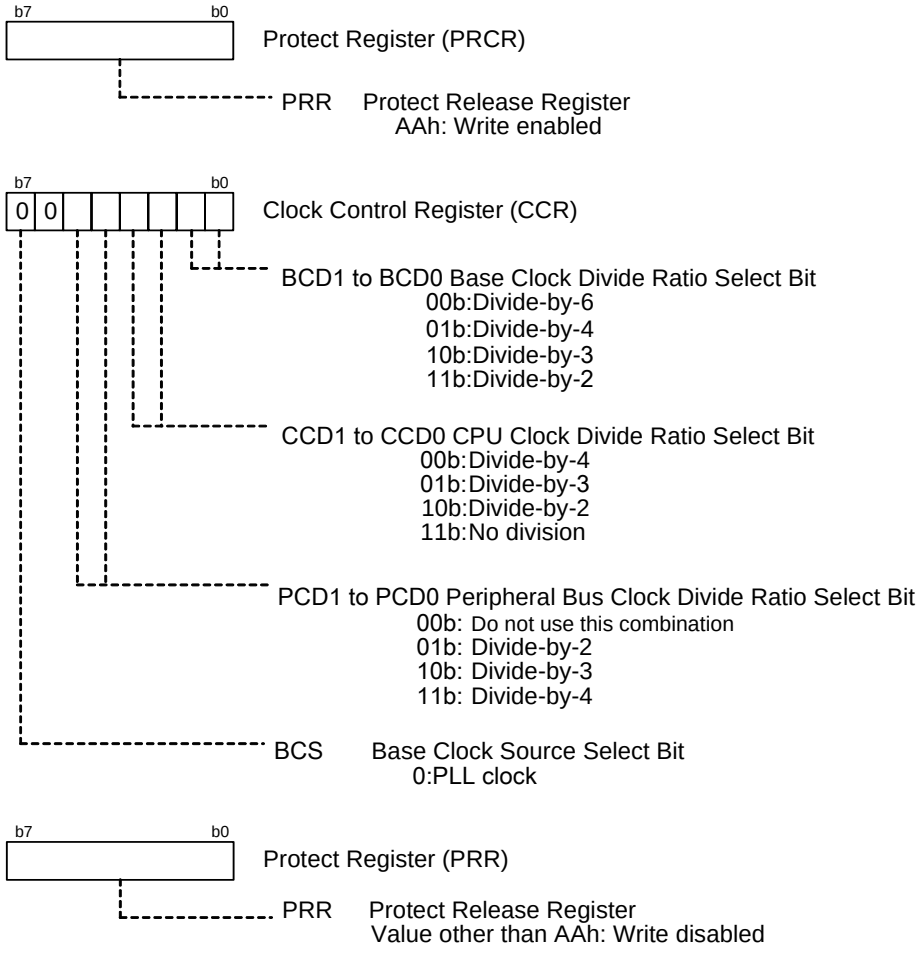
Set the clock control register.



5. Sample Program

A sample program can be downloaded from the Renesas Technology website.

5.1 Explanation

In the sample program, after the MCU enters low power mode from low speed mode, it enters stop mode. The INT0 interrupt is used to exit stop mode, and after exiting stop mode, the MCU enters in the following order: low power mode, low-speed mode, and PLL mode.
When an INT0 interrupt request is received in PLL mode, the MCU reenters stop mode.
When the MCU enters stop mode, a low level is output to port P0_0. When the MCU exits stop mode, a high level is output to port P0_0.

Refer to the hardware manual for settings to enter low speed mode and to oscillate the sub clock and on-chip oscillator clock.

Table 5.1 lists the Clock Operation in Low-speed Mode, Low Power Mode, and Wait Mode.
Table 5.2 lists the $\overline{\text{INT0}}$ Setting
Figure 5.1 shows the Sample Program Mode Change
Figure 5.2 shows the Sample Program Operation
Figure 5.3 shows the Sample Program Operation 2

Table 5.1 Clock Operation in Low-speed Mode, Low Power Mode, and Wait Mode

Clock Name	PLL Mode	Low speed Mode	Low power Mode	Stop Mode
Main clock	Oscillated		Stopped	
Sub clock	Stopped (unused)			Stopped
On-chip oscillator	Oscillated			Stopped
PLL clock	Oscillated		Stopped	
Base clock source	Oscillated	fOCO4		
Peripheral function clock source	All oscillated		Only fC32 oscillated	Stopped
Base clock	Oscillated			Stopped

Table 5.2 INT0 Setting

Polarity Switch	Level/Edge Sensitive Switch
Falling edge, low level signal	Edge sensitive

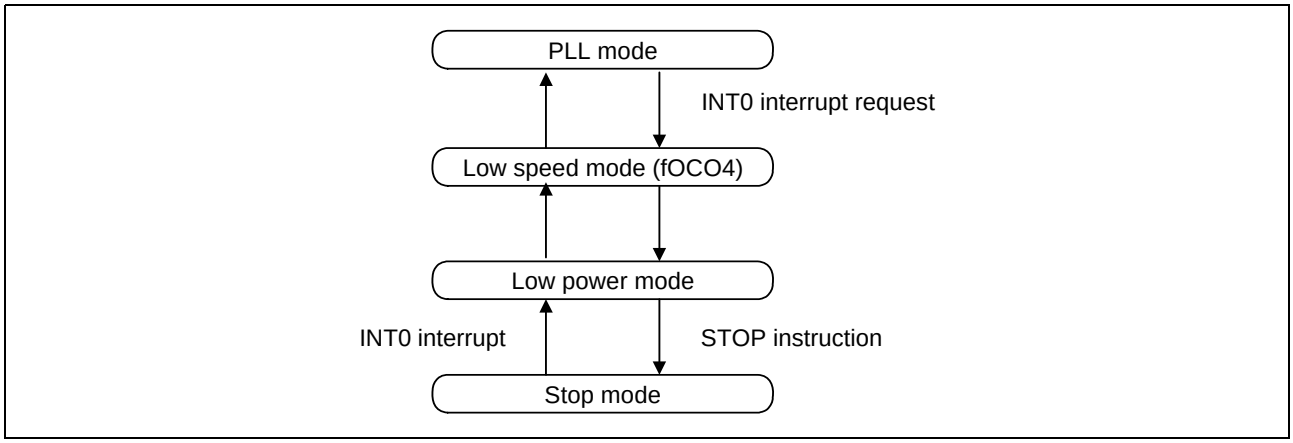


Figure 5.1 Sample Program Mode Change

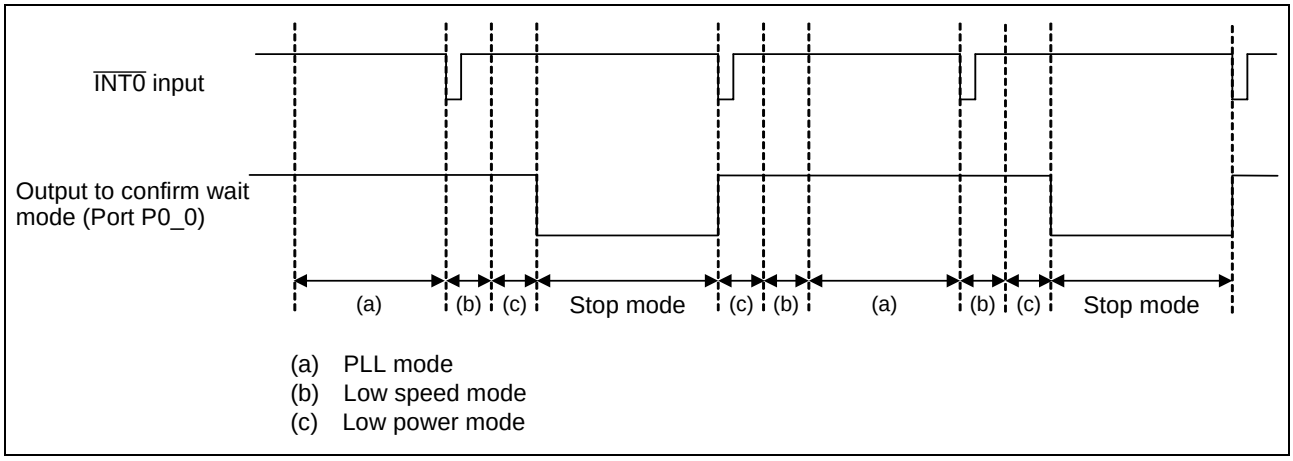


Figure 5.2 Sample Program Operation

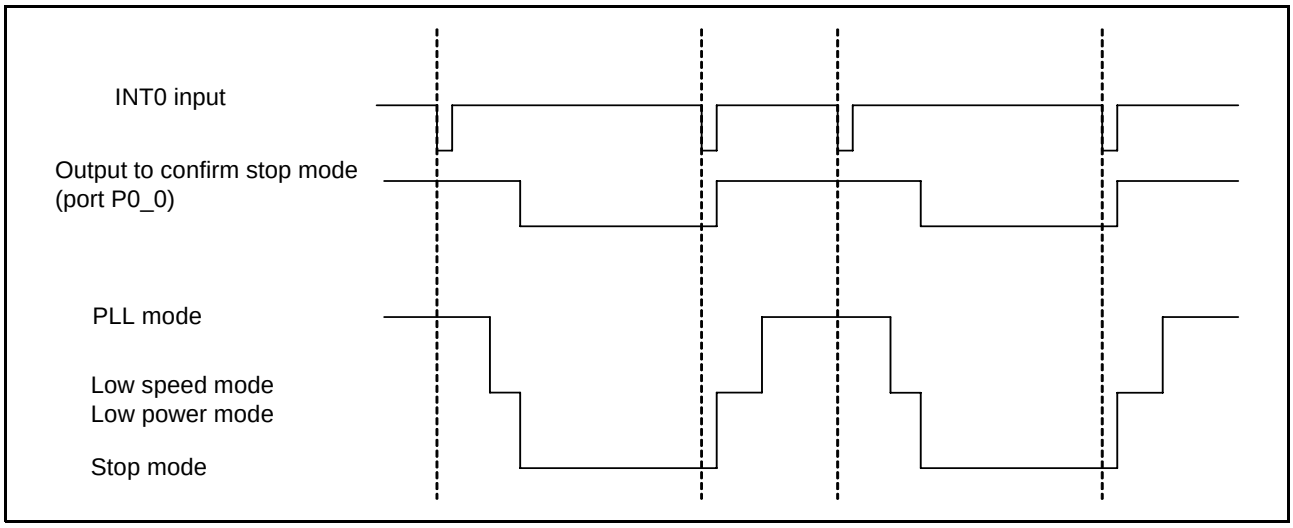


Figure 5.3 Sample Program Operation 2

5.2 Program Flow

Figure 5.4 shows the Main Function Flowchart.
Figure 5.5 shows the Stop Mode Transition Flowchart.
Figure 5.6 shows the Exit Stop Mode Flowchart.

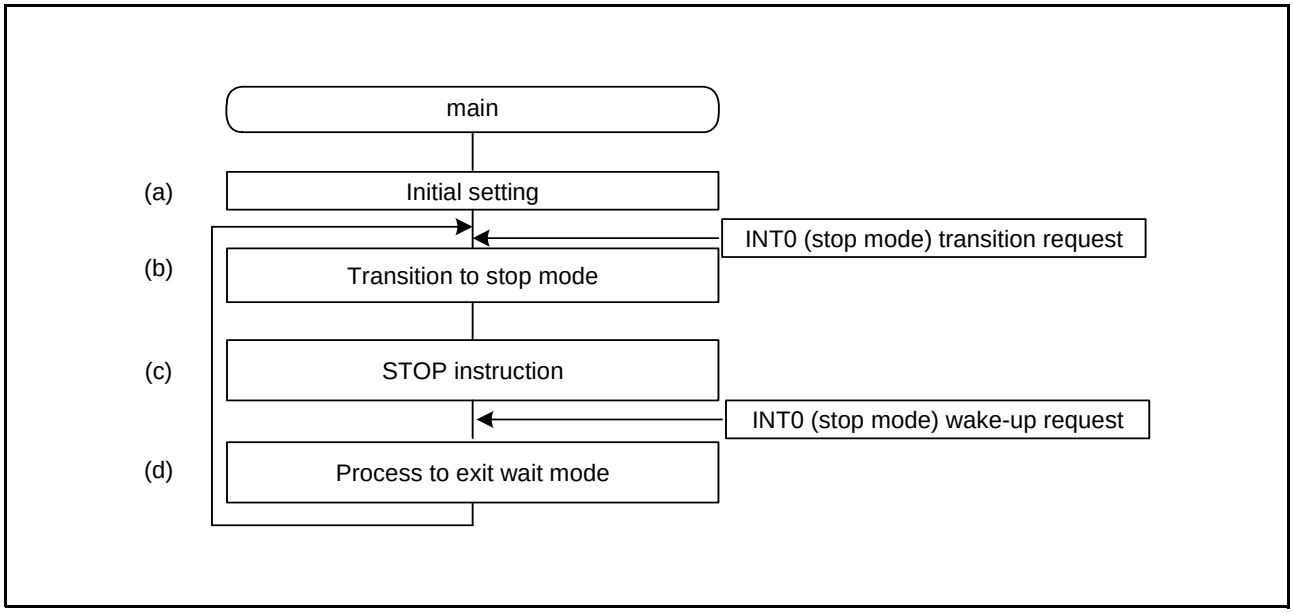


Figure 5.4 Main Function Flowchart

5.3 Program Flow

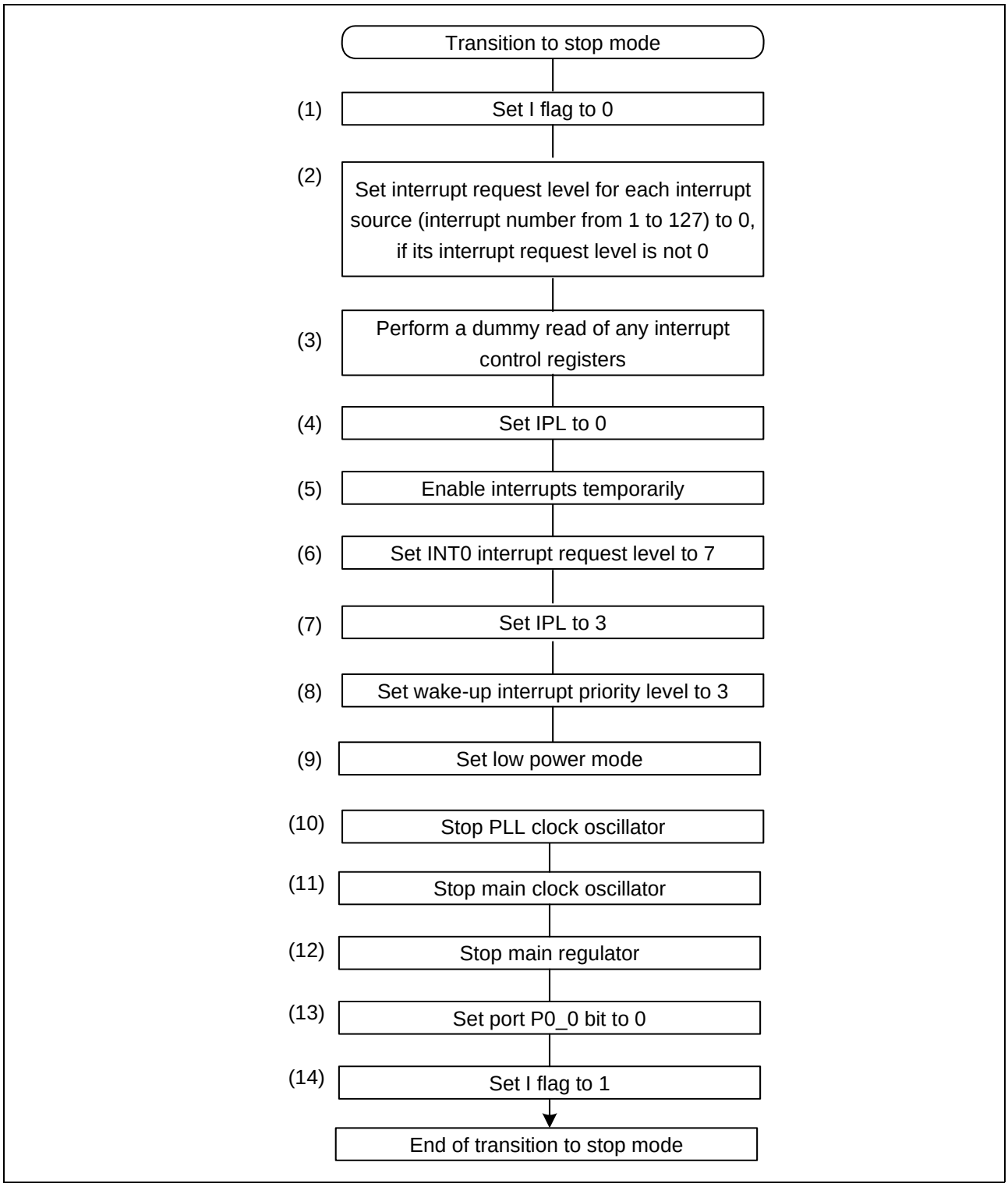


Figure 5.5 Stop Mode Transition Flowchart

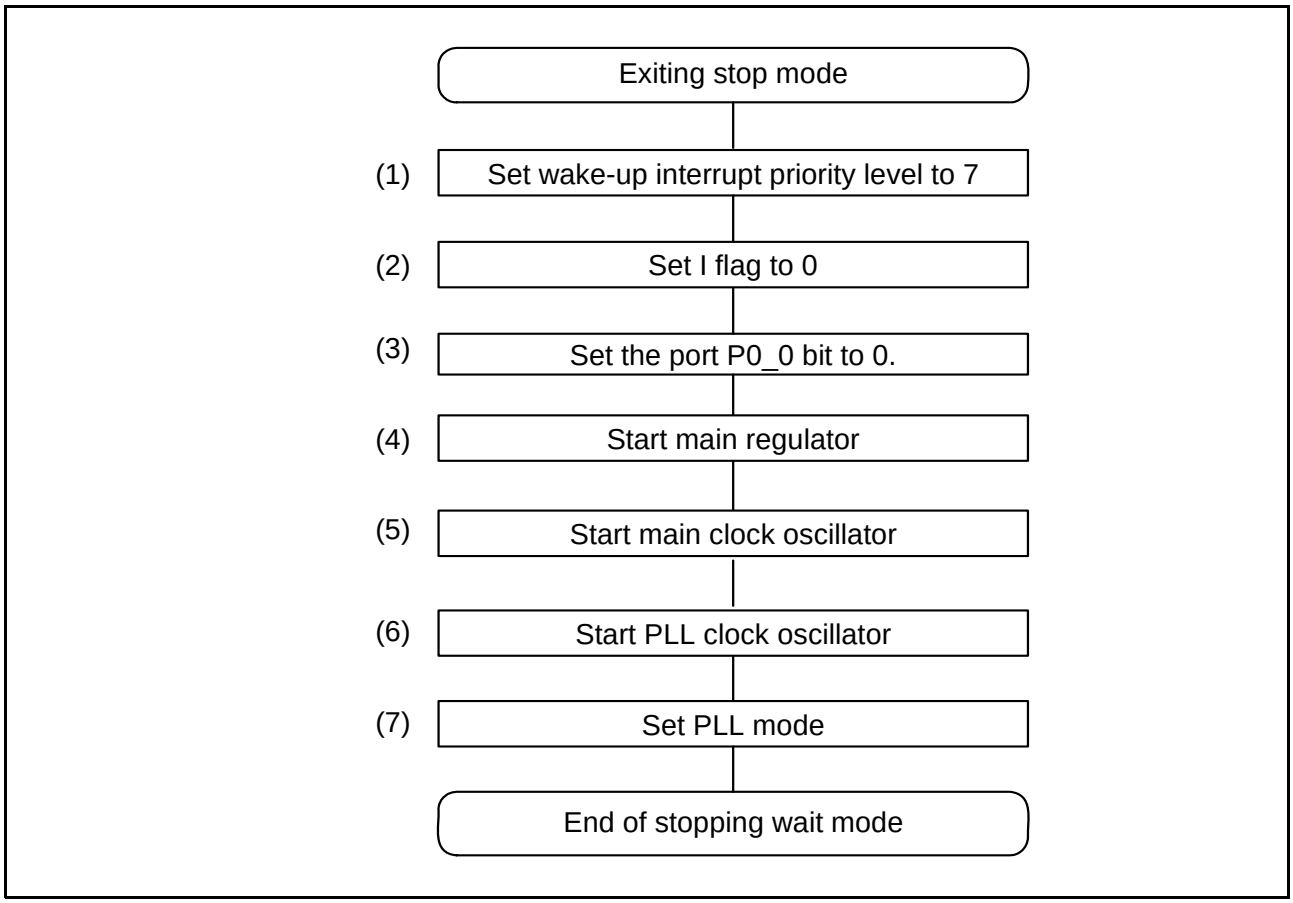


Figure 5.6 Exit Stop Mode Flowchart

6. Reference Documents

Hardware Manual
R32C/118 Group Hardware Manual Rev.1.00
The latest version can be downloaded from the Renesas Technology website.

Technical Update/Technical News
The latest information can be downloaded from the Renesas Technology website.

C Compiler Manual
R32C/100 Series C Compiler Package Ver. 1.02 Compiler User's Manual Rev. 1.00
The latest version can be downloaded from the Renesas Technology website.

Website and Support

Renesas Technology Website
http://www.renesas.com/

Inquiries
http://www.renesas.com/inquiry
csc@renesas.com

REVISION HISTORY	Stop Mode Set-up

Rev.	Date	Description	
		Page	Summary
1.00	Mar. 5, 2010	—	Initial release

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