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# H8SX Family

## Simultaneous Transmission and Reception by SCI in Asynchronous Mode

### Introduction

Simultaneous transmission and reception of 128 bytes of data is performed by means of the asynchronous serial data communication function of serial communication interface 4 (SCI_4).

### Target Device

H8SX/1638, H8SX/1648, H8SX/1653, H8SX/1658R, H8SX/1663, H8SX/1668R Groups

### Preface

Although the writing of this application note is in accord with the hardware manual for the H8SX/1653 Group, the program covered in this application note can be run on the target devices indicated above. However, since some functional modules may be changed for the addition of functionality etc., be sure to perform a thorough evaluation by confirming the details with the hardware manual for the target device.

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## 1. Specifications

Simultaneous transmission and reception of 128 bytes of data is performed using the asynchronous serial data communication function of SCI_4.

- Figure 1 shows an example of connection for simultaneous transmission and reception by the SCI in asynchronous mode.
- The communication format is shown in table 1.
- When a power-on reset occurs on the master side, a low-level trigger is output from the P13 pin on the master side and the master side starts simultaneous transmission and reception of 128 bytes of data.
- When a low-level trigger is input from the master side to the $\overline{\text{IRQ3}}$ pin on the slave side, the slave side starts simultaneous transmission and reception of 128 bytes of data.
- In this sample task, simultaneous transmission and reception of 128 bytes of data is controlled by software through the interrupt exception processing.

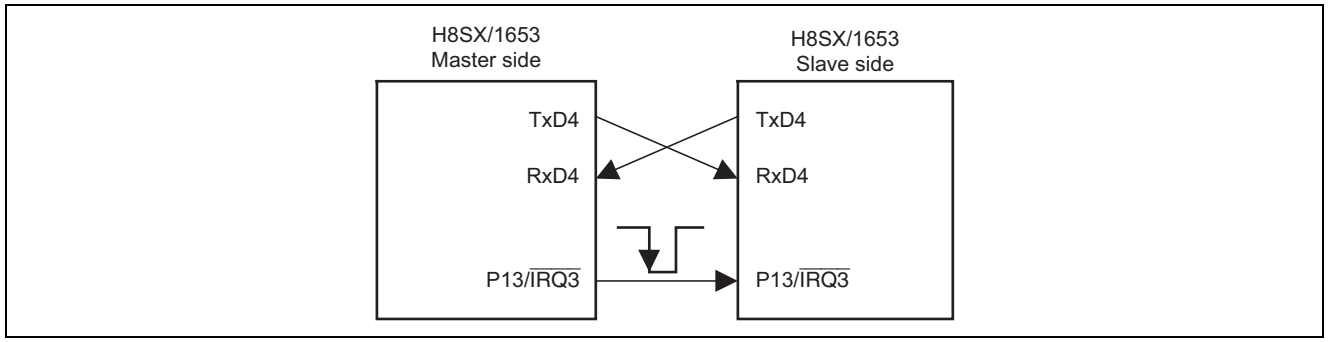



**Figure 1 Connection for Simultaneous Transmission and Reception by SCI in Asynchronous Mode**

**Table 1 Serial Transmit Format in Asynchronous Mode**

| Format Item | Setting |
|---|---|
| Pϕ | 16 MHz |
| Serial communication mode | Asynchronous mode |
| Clock source | On-chip baud rate generator |
| Transfer rate | 38,400 bps |
| Data length | 8 bits |
| Parity bit | None |
| Stop bit | 1 bit |
| Serial/parallel conversion format | LSB-first |

## 2. Conditions for Application

**Table 2 Conditions for Application**

| Item | Contents | |
|---|---|---|
| Operating frequency | Input clock: | 16 MHz |
| | System clock (Iϕ): | 16 MHz |
| | Peripheral module clock (Pϕ): | 16 MHz |
| | External bus clock (Bϕ): | 16 MHz |
| Operating mode | Mode 6 (MD2 = 1, MD1 = 1, MD0 = 0)<br>MD_CLK = 0 | |
| Development tool | High-performance Embedded Workshop Version 4.00.02 | |
| C/C++ compiler | H8S, H8/300 Series C/C++ Compiler Version 6.01.00<br>(from Renesas Technology Corp.) | |
| Compile option | -cpu = h8sxa:24:md, -code = machinecode, -optimize = 1, -regparam = 3,<br>-speed = (register, shift, struct, expression) | |

**Table 3 Section Settings**

| Address | Section Name | Description |
|---|---|---|
| H'001000 | P | Program area |
| | C | Data table storage area |
| H'FF2000 | B | Uninitialized data area (RAM area) |

# 3. Description of Modules Used

## 3.1 Description of SCI_4

In this sample task, simultaneous transmission and reception of 128 bytes of data is performed using the asynchronous serial data communication function of SCI_4. Figure 2 shows a block diagram of SCI_4 and the functions regarding figure 2 are described below.

- On-chip peripheral module clock Pϕ
  Pϕ is a reference clock used to drive the on-chip peripheral functions and is generated by the clock pulse generator.
- Receive shift register_4 (RSR_4)
  RSR_4 is a register used to receive serial data. When RSR_4 receives one frame of serial data input from the RxD4 pin, that data is automatically transferred to receive data register_4 (RDR_4). RSR_4 cannot be directly accessed by the CPU.
- Receive data register_4 (RDR_4)
  RDR_4 is an 8-bit register that stores receive data. When one frame of data has been received, the data is automatically transferred from RSR_4 to RDR_4. RSR_4 and RDR_4 form a double buffer, thus enabling continuous reception of data. Since RDR_4 is a register used only for data reception, RDR_4 can only be read by the CPU.
- Transmit shift register_4 (TSR_4)
  TSR_4 is a register used to transmit serial data. When transmitting data, data is first transferred from transmit data register_4 (TDR_4) to TSR_4, and then the transmit data is output from the TxD4 pin. TSR_4 cannot be directly accessed by the CPU.
- Transmit data register_4 (TDR_4)
  TDR_4 is an 8-bit register that stores transmit data. When TSR_4 is detected as empty, the data written to TDR_4 is automatically transferred to TSR_4. Since TDR_4 and TSR_4 form a double buffer, if the next data has been written to TDR_4 when one frame of data is transmitted, the written data is transferred to TSR_4, thus enabling continuous transmission of data. TDR_4 can always be read from or written to by the CPU. However, be sure to confirm that the TDRE bit in serial status register_4 (SSR_4) is 1 before writing to TDR_4.
- Serial mode register_4 (SMR_4)
  SMR_4 is an 8-bit register used to set the serial data transfer format and select the clock source for the on-chip baud rate generator.
- Serial control register_4 (SCR_4)
  SCR_4 is a register used to enable or disable transmission/reception or interrupt requests, and to select the transmit/receive clock source.
- Serial status register_4 (SSR_4)
  SSR_4 consists of the SCI_4 status flags and transmission/reception multiprocessor bits. The TDRE, RDRF, ORER, PER, and FER bits can only be cleared.
- Smart card mode register_4 (SCMR_4)
  SCMR_4 is a register used to select the smart card interface and its format. In this sample task, this register is set to select normal asynchronous or clock synchronous mode.

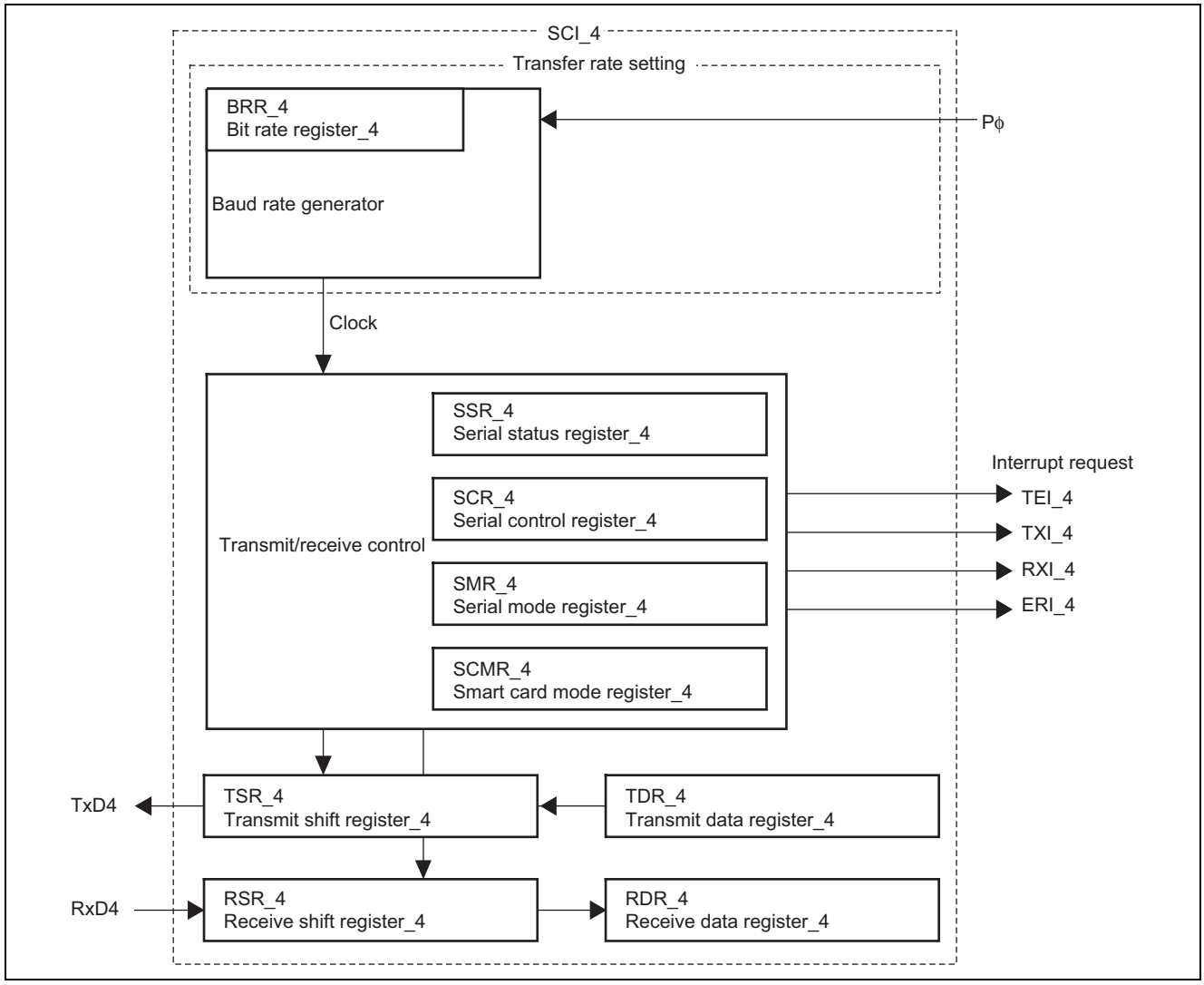



**Figure 2 Block Diagram of SCI_4**

# 4. Description of Operation

## 4.1 Overview of Operation

Figure 3 illustrates the operation of this sample task. Simultaneous transmission and reception of 128 bytes of data is performed on the master side and slave side.

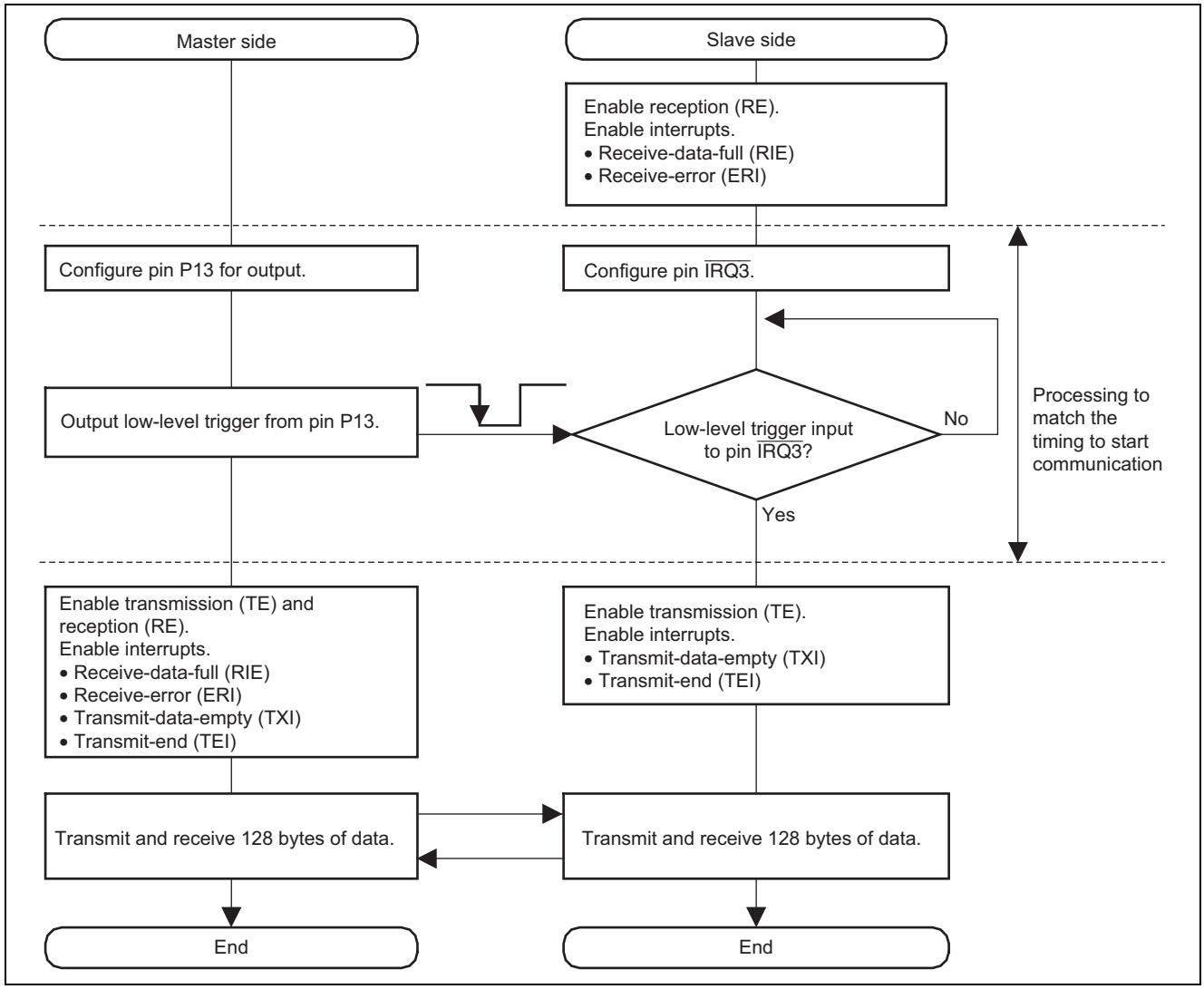



**Figure 3 Overview of Operation**

## 4.2 Transmit Operation

Figure 4 shows the timing of transmission. The hardware processing and software processing are shown in table 4 for describing figure 4.

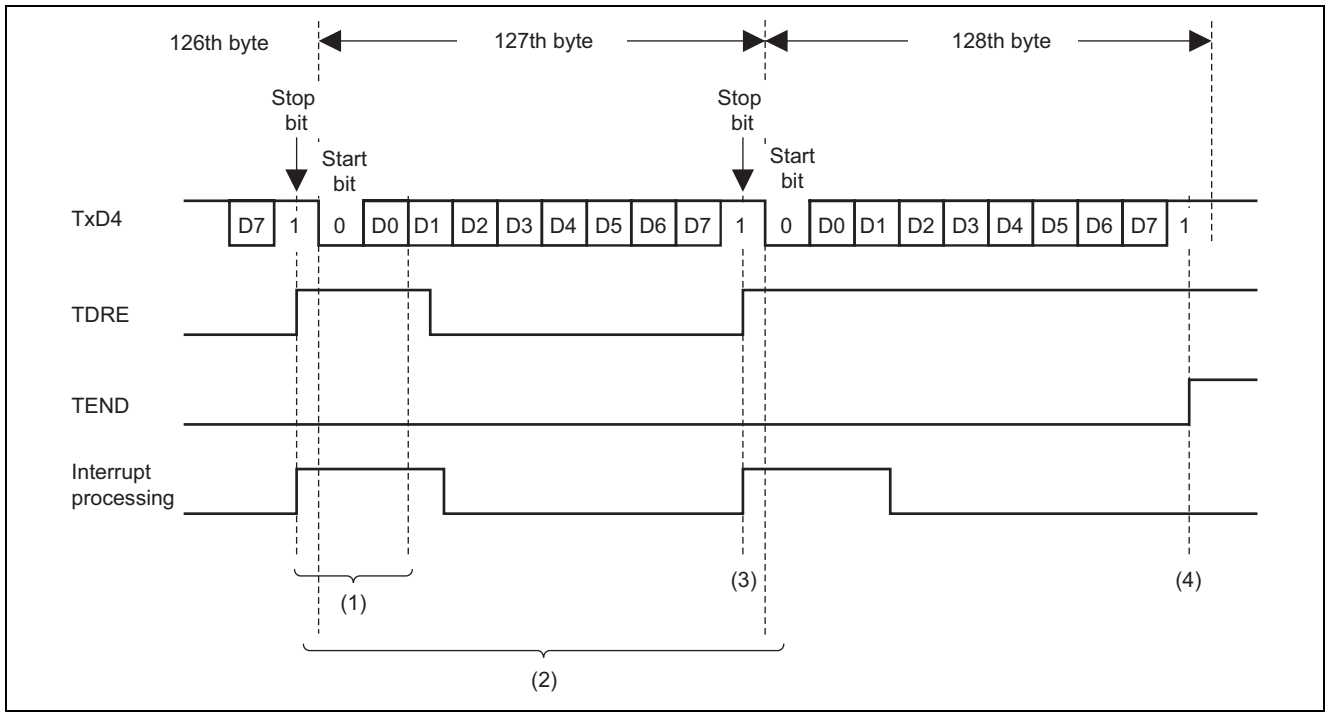



**Figure 4 Transmit Operation Timing**

**Table 4 Hardware and Software Processing**

| | Hardware Processing | Software Processing |
|---|---|---|
| (1) | (a) Set the TDRE bit to 1. | TXI interrupt processing<br>(a) Write transmit data to TDR_4.<br>(b) Clear the TDRE bit to 0. |
| (2) | (a) Transfer the TDR_4 contents to TSR_4.<br>(b) Output the TSR_4 contents to the TxD4 pin. | None |
| (3) | (a) Set the TDRE bit to 1. | TXI interrupt processing<br>(a) Write transmit data to TDR_4.<br>(b) Clear the TDRE bit to 0.<br>(c) Disable the TXI interrupt. |
| (4) | (a) Set the TDRE bit to 1.<br>(b) Set the TEND bit to 1. | TEI interrupt processing<br>(a) Clear the TEND bit to 0.<br>(b) Clear the TE bit to 0.<br>(c) Disable the TEI interrupt. |

## 4.3 Receive Operation

Figure 5 shows the timing of reception. The hardware processing and software processing are shown in table 5 for describing figure 5.

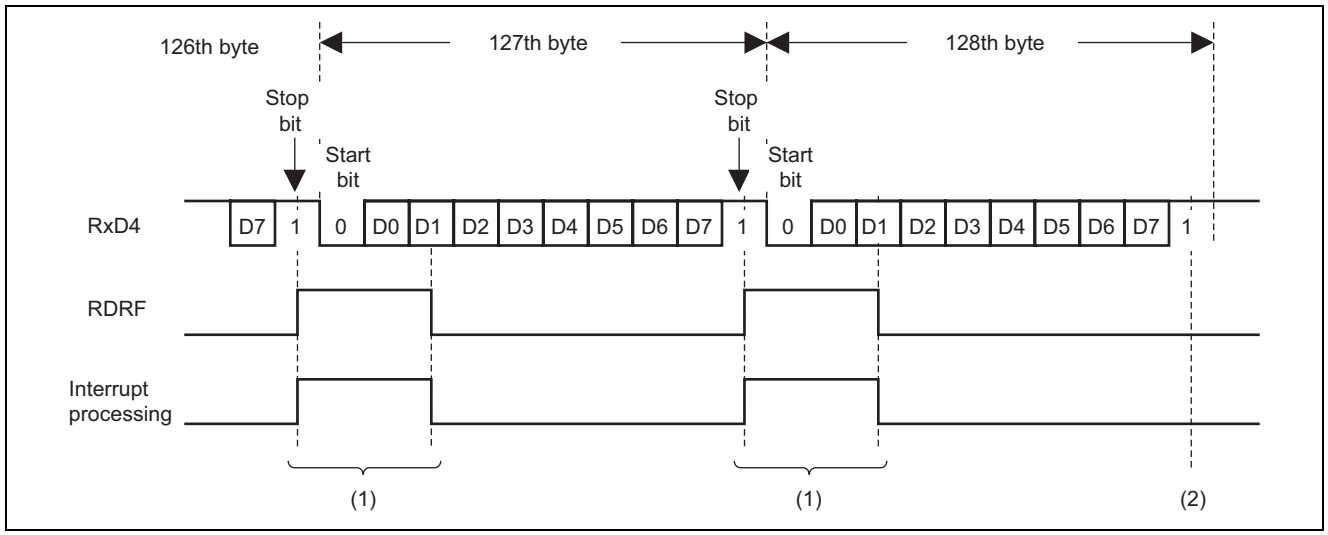



**Figure 5 Receive Operation Timing**

**Table 5 Hardware and Software Processing**

| | Hardware Processing | Software Processing |
|---|---|---|
| (1) | (a) Set the RDRF bit to 1.<br>(b) After reception has finished successfully, transfer receive data from RSR_4 to RDR_4. | RXI interrupt processing<br>(a) Read the receive data in RDR_4.<br>(b) Clear the RDRF bit to 0. |
| (2) | (a) Set the RDRF bit to 1.<br>(b) After reception has finished successfully, transfer receive data from RSR_4 to RDR_4. | RXI interrupt processing<br>(a) Read the receive data in RDR_4.<br>(b) Clear the RDRF bit to 0.<br>(c) Clear the RE bit to 0.<br>(d) Disable the RXI and ERI interrupts. |

# 5. Description of Software

## 5.1 List of Functions

**Table 6 List of Functions**

| Function Name | Functions |
|---|---|
| init | Initialization routine<br>Cancels module stop mode, sets the clocks, and calls the main function. |
| main | Main routine<br>Makes the initial settings for the SCI and performs communication at a transfer rate of 38,400 bps. |
| eri4_int | Receive-error interrupt processing routine<br>Writes the error status information in SSR_4 to RAM and initializes SSR_4. |
| rxi4_int | Receive-data-full interrupt processing routine<br>Transfers the receive data in RDR_4 to RAM for storage. |
| txi4_int | Transmit-data-empty interrupt processing routine<br>Writes the transmit data in RAM to TDR_4 to perform transmission. |
| tei4_int | Transmit-end interrupt processing routine<br>Disables the TEI interrupt request and sets endflg to 1. |

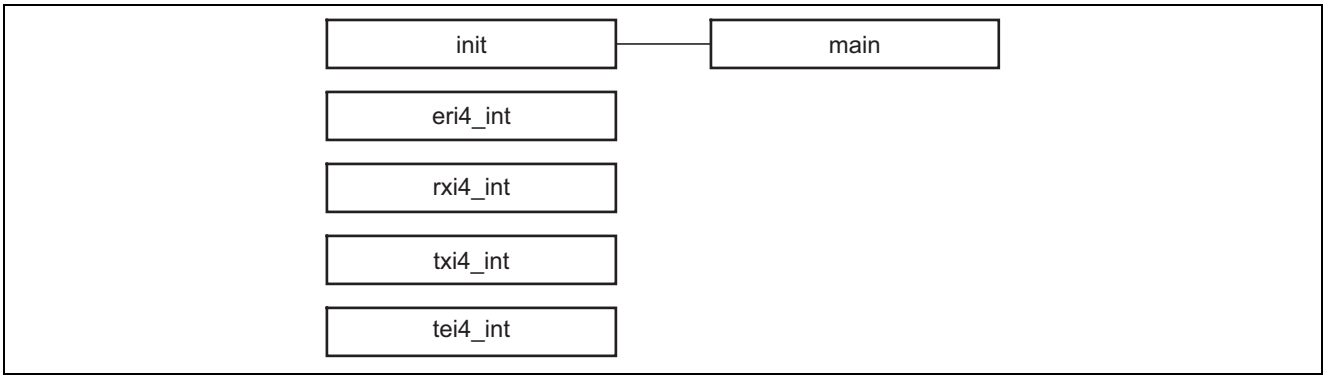



**Figure 6 Hierarchical Structure**

## 5.2 Vector Table

**Table 7 Interrupt Exception Handling Vector Table**

| Exception Handling Source | Vector Number | Vector Table Address | Exception Handling Routine |
|---|---|---|---|
| Reset | 0 | H'000000 | init |
| SCI_4 ERI4 | 160 | H'000280 | eri4_int |
| SCI_4 RXI4 | 161 | H'000284 | rxi4_int |
| SCI_4 TXI4 | 162 | H'000288 | txi4_int |
| SCI_4 TEI4 | 163 | H'00028C | tei4_int |

## 5.3 RAM Usage

**Table 8 RAM Usage**

| Type | Label Name | Description | Used In |
|---|---|---|---|
| unsigned char | endflg | Transmit end flag<br>0: Transmission is in progress<br>1: Transmission has ended | main, tei4_int |
| unsigned char | errbuf | Receive error buffer<br>Stores the contents of SSR_4 when an overrun error, framing error, or parity error occurs. | main, eri4_int |
| unsigned char | tcnt | Transmit counter | main, txi4_int |
| unsigned char | rcnt | Receive counter | main, rxi4_int |
| unsigned char | rcv_dt[128] | RAM area for storing receive data | main, rxi4_int |

## 5.4 Data Table

**Table 9 Data Table**

| Type | Array Name | Description | Used In |
|---|---|---|---|
| unsigned char | trs_dt[128] | ROM area for storing the transmit data<br>128-byte data of H'00, H'01, ... , H'7F | main, txi4_int |

## 5.5 Macro Definition

**Table 10 Macro Definition**

| Identifier | Description | Used In |
|---|---|---|
| MASTER | Generates a program for the master side | main |
| SLAVE | Generates a program for the slave side | main |

## 5.6 Description of Functions

### 5.6.1 init Function

(1) Functional overview

Initialization routine which cancels module stop mode, sets the clocks, and calls the main function.

(2) Argument

None

(3) Return value

None

(4) Description of internal registers

The internal registers used in this sample task are described below. The setting values shown below are the values used in this sample task and differ from their initial values.

- System clock control register (SCKCR) Address: H'FFFDC4

| Bit | Bit Name | Setting | R/W | Function |
|---|---|---|---|---|
| 10 | ICK2 | 0 | R/W | System Clock (Iϕ) Select |
| 9 | ICK1 | 1 | R/W | These bits select the system clock frequency. The CPU, DMAC, |
| 8 | ICK0 | 0 | R/W | and DTC modules are driven by the system clock.<br>010: Input clock × 1 |
| 6 | PCK2 | 0 | R/W | Peripheral Module Clock (Pϕ) Select |
| 5 | PCK1 | 1 | R/W | These bits select the frequency of the peripheral module clock. |
| 4 | PCK0 | 0 | R/W | 010: Input clock × 1 |
| 2 | BCK2 | 0 | R/W | External Bus Clock (Bϕ) Select |
| 1 | BCK1 | 1 | R/W | These bits select the frequency of the external bus clock. |
| 0 | BCK0 | 0 | R/W | 010: Input clock × 1 |

- MSTPCRA, MSTPCRB, and MSTPCRC are the registers that control module stop mode. Setting the bits in these registers places the corresponding modules in module stop mode, and clearing the bits cancels module stop mode.

- Module stop control register A (MSTPCRA) Address: H'FFFDC8

| Bit | Bit Name | Setting | R/W | Function |
|---|---|---|---|---|
| 15 | ACSE | 0 | R/W | All-module-clock-stop mode enable<br>Enables or disables transition to all-module-clock-stop mode.<br>If this bit is set to 1, all-module-clock-stop mode is entered when the SLEEP instruction is executed by the CPU while all the modules under control of the MSTPCR registers are placed in module stop mode. In all-module-clock-stop mode, even the bus controller and I/O ports are stopped to reduce the supply current.<br>0: Disables transition to all-module-clock-stop mode.<br>1: Enables transition to all-module-clock-stop mode. |
| 13 | MSTPA13 | 1 | R/W | DMA controller (DMAC) |
| 12 | MSTPA12 | 1 | R/W | Data transfer controller (DTC) |
| 9 | MSTPA9 | 1 | R/W | 8-bit timer (TMR_3 and TMR_2) |
| 8 | MSTPA8 | 1 | R/W | 8-bit timer (TMR_1 and TMR_0) |
| 5 | MSTPA5 | 1 | R/W | D/A converter (channels 1 and 0) |
| 3 | MSTPA3 | 1 | R/W | A/D converter (unit 0) |
| 0 | MSTPA0 | 1 | R/W | 16-bit timer pulse unit (TPU channels 5 to 0) |

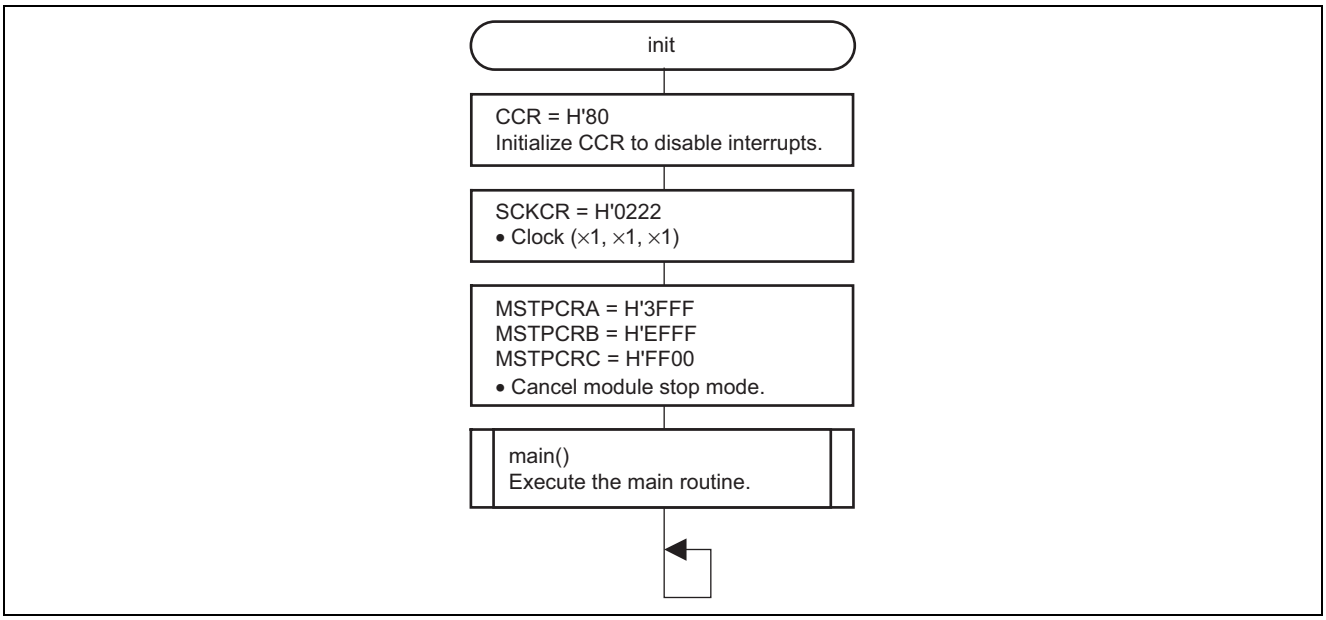
- Module stop control register B (MSTPCRB) Address: H'FFFDCA

| Bit | Bit Name | Setting | R/W | Function |
|---|---|---|---|---|
| 15 | MSTPB15 | 1 | R/W | Programmable pulse generator (PPG) |
| 12 | MSTPB12 | 0 | R/W | Serial communication interface_4 (SCI_4) |
| 10 | MSTPB10 | 1 | R/W | Serial communication interface_2 (SCI_2) |
| 9 | MSTPB9 | 1 | R/W | Serial communication interface_1 (SCI_1) |
| 8 | MSTPB8 | 1 | R/W | Serial communication interface_0 (SCI_0) |
| 7 | MSTPB7 | 1 | R/W | $I^2C$ bus interface_1 (IIC_1) |
| 6 | MSTPB6 | 1 | R/W | $I^2C$ bus interface_0 (IIC_0) |

- Module stop control register C (MSTPCRC) Address: H'FFFDCC

| Bit | Bit Name | Setting | R/W | Function |
|---|---|---|---|---|
| 15 | MSTPC15 | 1 | R/W | Serial communication interface_5 (SCI_5), (IrDA) |
| 14 | MSTPC14 | 1 | R/W | Serial communication interface_6 (SCI_6) |
| 13 | MSTPC13 | 1 | R/W | 8-bit timer (TMR_4 and TMR_5) |
| 12 | MSTPC12 | 1 | R/W | 8-bit timer (TMR_6 and TMR_7) |
| 11 | MSTPC11 | 1 | R/W | Universal serial bus interface (USB) |
| 10 | MSTPC10 | 1 | R/W | CRC computation unit |
| 4 | MSTPC4 | 0 | R/W | On-chip RAM_4 (H'FF2000 to H'FF3FFF) |
| 3 | MSTPC3 | 0 | R/W | On-chip RAM_3 (H'FF4000 to H'FF5FFF) |
| 2 | MSTPC2 | 0 | R/W | On-chip RAM_2 (H'FF6000 to H'FF7FFF) |
| 1 | MSTPC1 | 0 | R/W | On-chip RAM_1 (H'FF8000 to H'FF9FFF) |
| 0 | MSTPC0 | 0 | R/W | On-chip RAM_0 (H'FFA000 to H'FFBFFF) |

(5) Flowchart



### 5.6.2 main Function

(1) Functional overview

Main routine which makes the initial settings for the SCI and performs communication at a transfer rate of 38,400 bps.

(2) Argument

None

(3) Return value

None

(4) Description of internal registers

The internal registers used in this sample task are described below. The setting values shown below are the values used in this sample task and differ from their initial values.

- Port 1 data direction register (P1DDR) Address: H'FFFB80

| Bit | Bit Name | Setting | R/W | Function |
|---|---|---|---|---|
| 3 | P13DDR | 1 | R/W | 0: Pin P13 is an input pin.<br>1: Pin P13 is an output pin. |

- Port 1 input buffer control register (P1ICR) Address: H'FFFB90

| Bit | Bit Name | Setting | R/W | Function |
|---|---|---|---|---|
| 3 | P13ICR | 1 | R/W | 0: Input buffer of pin P13 is disabled. Input signal is fixed high.<br>1: Input buffer of pin P13 is enabled. Pin state is reflected in the peripheral module. |

- Port 6 input buffer control register (P6ICR) Address: H'FFFB95

| Bit | Bit Name | Setting | R/W | Function |
|---|---|---|---|---|
| 1 | P61ICR | 1 | R/W | 0: Input buffer of pin P61 is disabled. Input signal is fixed high.<br>1: Input buffer of pin P61 is enabled. Pin state is reflected in the peripheral module. |

- Port function control register C (PFCRC) Address: H'FFFBCC

| Bit | Bit Name | Setting | R/W | Function |
|---|---|---|---|---|
| 3 | ITS3 | 0 | R/W | $\overline{\text{IRQ3}}$ Pin Select<br>0: P13 is set as $\overline{\text{IRQ3}}$-A input pin<br>1: P53 is set as $\overline{\text{IRQ3}}$-B input pin |

- IRQ sense control register L (ISCRL) Address: H'FFFD6A

| Bit | Bit Name | Setting | R/W | Function |
|---|---|---|---|---|
| 7 | IRQ3SR | 0 | R/W | IRQ3 Sense Control Rise |
| 6 | IRQ3SF | 1 | R/W | IRQ3 Sense Control Fall<br>01: Interrupt request is generated on the falling edge of $\overline{\text{IRQ3}}$ input |

- Serial mode register_4 (SMR_4) Address: H'FFFE90

| Bit | Bit Name | Setting | R/W | Function |
|---|---|---|---|---|
| 7 | C/$\overline{A}$ | 0 | R/W | Communication Mode<br>0: Operates in asynchronous mode<br>1: Operates in clock synchronous mode |
| 6 | CHR | 0 | R/W | Character Length<br>0: 8-bit length data is transmitted<br>1: 7-bit length data is transmitted |
| 5 | PE | 0 | R/W | Parity Enable<br>0: No parity bit addition<br>1: Parity bit addition performed |
| 3 | STOP | 0 | R/W | Stop Bit Length<br>Selects the stop bit length at transmission.<br>0: 1 stop bit<br>1: 2 stop bits<br>In reception, only the first stop bit is checked, regardless of the setting of this bit. If the second stop bit is 0, it is treated as the start bit of the next transmit frame. |

- Bit rate register_4 (BRR_4) Address: H'FFFE91
  Function: 8-bit register for adjusting the bit rate. When Pϕ = 16 MHz, CKS1 and CKS0 bits = B'00 in SMR_4, and BRR_4 = 12, the bit rate is set at 38400 bps.
  Setting: 12

- Serial control register_4 (SCR_4) Address: H'FFFE92

| Bit | Bit Name | Setting | R/W | Function |
|---|---|---|---|---|
| 7 | TIE | 0/1 | R/W | Transmit Interrupt Enable<br>0: TXI interrupt is disabled<br>1: TXI interrupt is enabled |
| 6 | RIE | 0/1 | R/W | Receive Interrupt Enable<br>0: RXI and ERI interrupts are disabled<br>1: RXI and ERI interrupts are enabled |
| 5 | TE | 0/1 | R/W | Transmit Enable<br>0: Transmission is disabled<br>1: Transmission is enabled |
| 4 | RE | 0/1 | R/W | Receive Enable<br>0: Reception is disabled<br>1: Reception is enabled |
| 2 | TEIE | 0/1 | R/W | Transmit-End Interrupt Enable<br>0: TEI interrupt is disabled<br>1: TEI interrupt is enabled |
| 1 | CKE1 | 0 | R/W | Clock Enable 1, 0 |
| 0 | CKE0 | 0 | R/W | These bits select the clock source.<br>00: On-chip baud rate generator |

- Serial status register_4 (SSR_4) Address: H'FFFE94

| Bit | Bit Name | Setting | R/W | Function |
|---|---|---|---|---|
| 7 | TDRE | Undefined | R/(W)* | Transmit Data Register Empty<br>Indicates whether TDR contains transmit data.<br>[Setting conditions]<br>• When the TE bit in SCR is 0<br>• When data is transferred from TDR to TSR<br>[Clearing conditions]<br>• When 0 is written to TDRE after reading TDRE = 1<br>• When the DMAC transfers transmit data to TDR due to a TXI interrupt |
| 6 | RDRF | 0 | R/(W)* | Receive Data Register Full<br>Indicates whether RDR contains receive data.<br>[Setting condition]<br>• When reception is finished successfully, and receive data is transferred from RSR to RDR<br>[Clearing conditions]<br>• When 0 is written to RDRF after reading RDRF = 1<br>• When the DMAC or DTC transfers data from RDR due to an RXI interrupt<br>Even if the RE bit in SCR is cleared to 0, the RDRF flag is unaffected and its previous state retained.<br>If reception of the next data is completed while the RDRF flag is still set to 1, an overrun error occurs and the received data is lost. |
| 5 | ORER | 0 | R/(W)* | Overrun Error<br>[Setting condition]<br>• When an overrun error occurs during reception<br>[Clearing condition]<br>• When 0 is written to ORER after reading ORER = 1 |
| 4 | FER | 0 | R/(W)* | Framing Error<br>[Setting condition]<br>• When a framing error occurs during reception<br>[Clearing condition]<br>• When 0 is written to FER after reading FER = 1 |
| 3 | PER | 0 | R/(W)* | Parity Error<br>[Setting condition]<br>• When a parity error occurs during reception<br>[Clearing condition]<br>• When 0 is written to PER after reading PER = 1 |

| Bit | Bit Name | Setting | R/W | Function |
|---|---|---|---|---|
| 2 | TEND | Undefined | R | Transmit End<br>[Setting conditions]<br>• When the TE bit in SCR is 0<br>• If the TDRE bit is 1 when the last bit in the transmit character is transmitted<br>[Clearing conditions]<br>• When 0 is written to TDRE after reading TDRE = 1<br>• When the DMAC writes transmit data to TDR due to a TXI interrupt |

Note: * Only 0 can be written to clear the flag.

- Smart card mode register_4 (SCMR_4) Address: H'FFFE96

| Bit | Bit Name | Setting | R/W | Function |
|---|---|---|---|---|
| 0 | SMIF | 0 | R/W | Smart Card Interface Mode Select<br>0: Operates in normal asynchronous or clock synchronous mode<br>1: Operates in smart card interface mode |

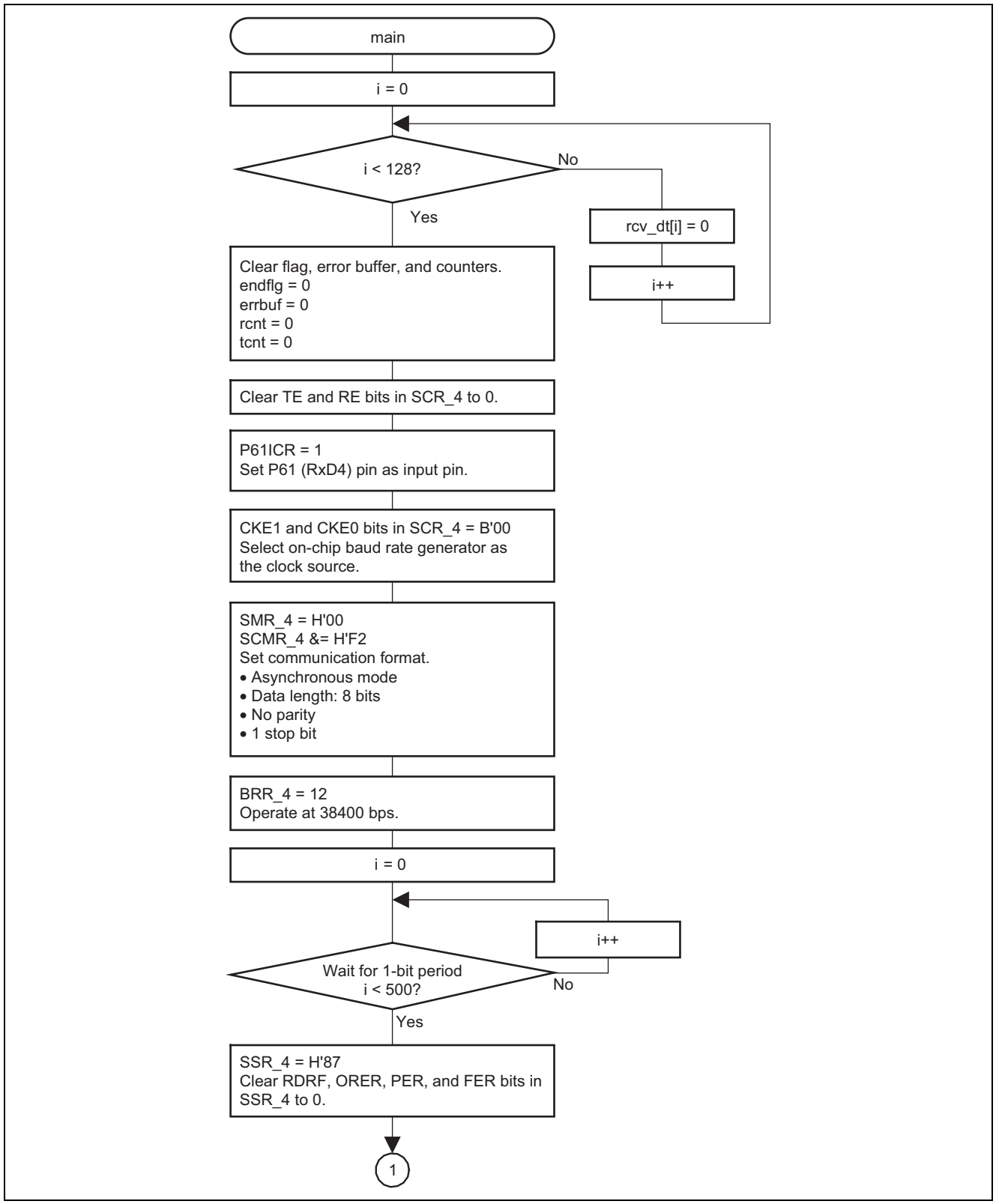
- IRQ status register (ISR) Address: H'FFFF36

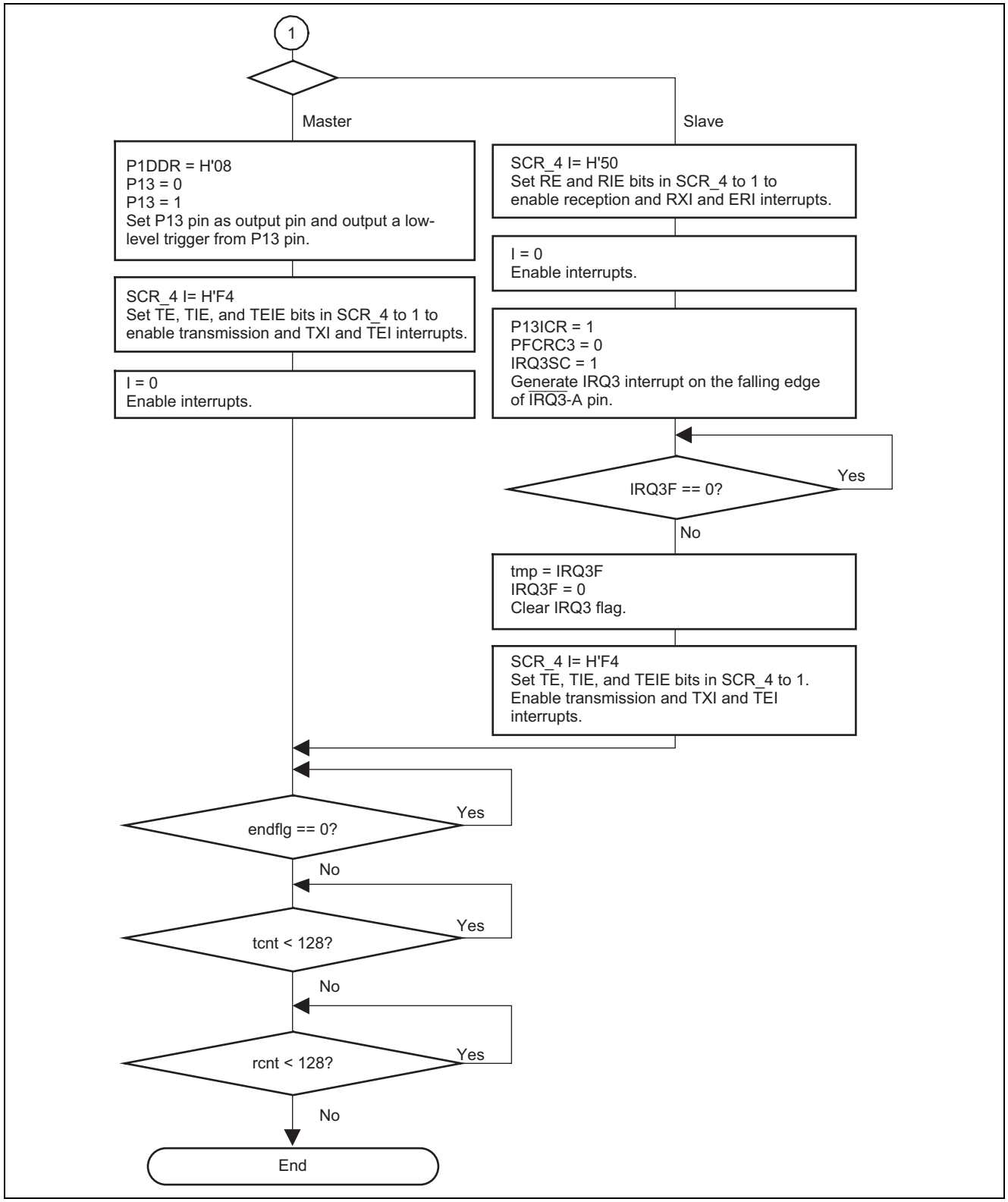
| Bit | Bit Name | Setting | R/W | Function |
|---|---|---|---|---|
| 3 | IRQ3F | Undefined | R/W | [Setting condition]<br>• When the interrupt source event selected by ISCR has occurred<br>[Clearing conditions]<br>• When 0 is written to IRQ3F after reading IRQ3F = 1<br>• If interrupt exception processing is executed when low-level detection is set and the $\overline{\text{IRQ3}}$ input is high<br>• If IRQ3 interrupt exception processing is executed when falling-edge, rising-edge, or both-edge detection is set<br>• When the DTC is activated by an IRQ3 interrupt and the DISEL bit in MRB of the DTC is 0 |

- Port 1 data register (P1DR) Address: H'FFFF50

| Bit | Bit Name | Setting | R/W | Function |
|---|---|---|---|---|
| 3 | P13DR | 0/1 | R/W | 0: Pin P13 outputs a low level<br>1: Pin P13 outputs a high level |

(5) Flowchart


main
i = 0
i < 128?
No
Yes
rcv_dt[i] = 0
i++
Clear flag, error buffer, and counters.
endflg = 0
errbuf = 0
rcnt = 0
tcnt = 0
Clear TE and RE bits in SCR_4 to 0.
P61ICR = 1
Set P61 (RxD4) pin as input pin.
CKE1 and CKE0 bits in SCR_4 = B'00
Select on-chip baud rate generator as
the clock source.
SMR_4 = H'00
SCMR_4 &= H'F2
Set communication format.
• Asynchronous mode
• Data length: 8 bits
• No parity
• 1 stop bit
BRR_4 = 12
Operate at 38400 bps.
i = 0
i++
Wait for 1-bit period
i < 500?
No
Yes
SSR_4 = H'87
Clear RDRF, ORER, PER, and FER bits in
SSR_4 to 0.
1


1
Master
Slave
P1DDR = H'08
P13 = 0
P13 = 1
Set P13 pin as output pin and output a low-level trigger from P13 pin.
SCR_4 I= H'F4
Set TE, TIE, and TEIE bits in SCR_4 to 1 to enable transmission and TXI and TEI interrupts.
I = 0
Enable interrupts.
SCR_4 I= H'50
Set RE and RIE bits in SCR_4 to 1 to enable reception and RXI and ERI interrupts.
I = 0
Enable interrupts.
P13ICR = 1
PFCRC3 = 0
IRQ3SC = 1
Generate IRQ3 interrupt on the falling edge of IRQ3-A pin.
IRQ3F == 0?
Yes
No
tmp = IRQ3F
IRQ3F = 0
Clear IRQ3 flag.
SCR_4 I= H'F4
Set TE, TIE, and TEIE bits in SCR_4 to 1. Enable transmission and TXI and TEI interrupts.
endflg == 0?
Yes
No
tcnt < 128?
Yes
No
rcnt < 128?
Yes
No
End

### 5.6.3 eri4_int Function

(1) Functional overview

Reception error interrupt processing routine.

(2) Argument

None

(3) Return value

None

(4) Description of internal register

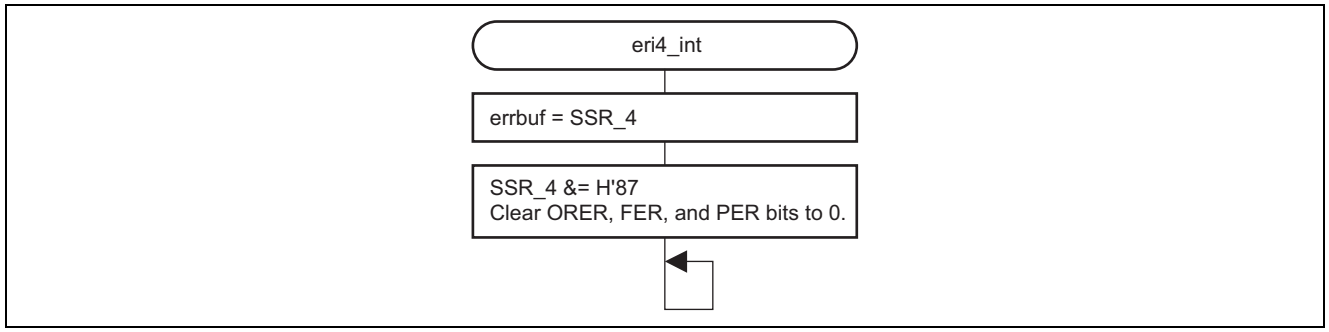
The internal registers used in this sample task are described below. The setting values shown below are the values used in this sample task and differ from their initial values.

- Serial status register_4 (SSR_4) Address: H'FFFE94

| Bit | Bit Name | Setting | R/W | Function |
|---|---|---|---|---|
| 5 | ORER | 0 | R/(W)* | Overrun Error<br>[Setting condition]<br>• When an overrun error occurs during reception<br>[Clearing condition]<br>• When 0 is written to ORER after reading ORER = 1 |
| 4 | FER | 0 | R/(W)* | Framing Error<br>[Setting condition]<br>• When a framing error occurs during reception<br>[Clearing condition]<br>• When 0 is written to FER after reading FER = 1 |
| 3 | PER | 0 | R/(W)* | Parity Error<br>[Setting condition]<br>• When a parity error occurs during reception<br>[Clearing condition]<br>• When 0 is written to PER after reading PER = 1 |

Note: * Only 0 can be written to clear the flag.

(5) Flowchart



### 5.6.4 rxi4_int Function

(1) Functional overview

Receive interrupt processing routine which receives one byte of data.

(2) Argument

None

(3) Return value

None

(4) Description of internal registers

The internal registers used in this sample task are described below. The setting values shown below are the values used in this sample task and differ from their initial values.

- Serial control register_4 (SCR_4) Address: H'FFFE92

| Bit | Bit Name | Setting | R/W | Function |
|---|---|---|---|---|
| 6 | RIE | 0 | R/W | Receive Interrupt Enable<br>0: RXI and ERI interrupts are disabled<br>1: RXI and ERI interrupts are enabled |
| 4 | RE | 0 | R/W | Receive Enable<br>0: Reception is disabled<br>1: Reception is enabled |

- Serial status register_4 (SSR_4) Address: H'FFFE94

| Bit | Bit Name | Setting | R/W | Function |
|---|---|---|---|---|
| 6 | RDRF | 0 | R/(W)* | Receive Data Register Full<br>Indicates whether RDR contains receive data.<br>[Setting condition]<br>• When reception is finished successfully, and receive data is transferred from RSR to RDR<br>[Clearing conditions]<br>• When 0 is written to RDRF after reading RDRF = 1<br>• When the DMAC or DTC transfers data from RDR due to an RXI interrupt<br>Even if the RE bit in SCR is cleared to 0, the RDRF flag is unaffected and its previous state retained.<br>If reception of the next data is completed while the RDRF flag is still set to 1, an overrun error occurs and the received data is lost. |

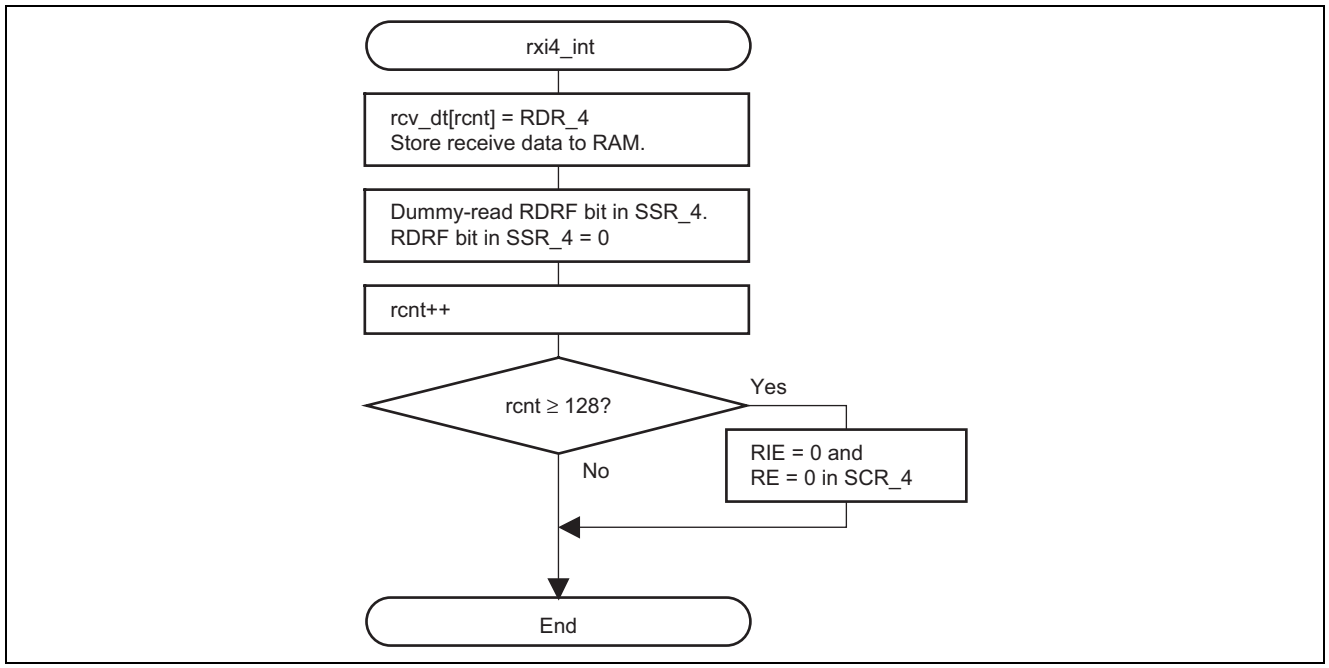
Note: * Only 0 can be written to clear the flag.

- Receive data register_4 (RDR_4) Address: H'FFFE95

  Function: 8-bit read-only register that stores receive data

  Setting: Undefined

(5) Flowchart




### 5.6.5 txi4_int Function

(1) Functional overview

Transmit interrupt processing routine which transmits one byte of data.

(2) Argument

None

(3) Return value

None

(4) Description of internal registers

The internal registers used in this sample task are described below. The setting values shown below are the values used in this sample task and differ from their initial values.

- Serial control register_4 (SCR_4) Address: H'FFFE92

| Bit | Bit Name | Setting | R/W | Function |
|---|---|---|---|---|
| 7 | TIE | 0 | R/W | Transmit Interrupt Enable<br>0: TXI interrupt is disabled<br>1: TXI interrupt is enabled |

- Transmit data register_4 (TDR_4) Address: H'FFFE93

  Function: 8-bit readable/writable register that stores transmit data

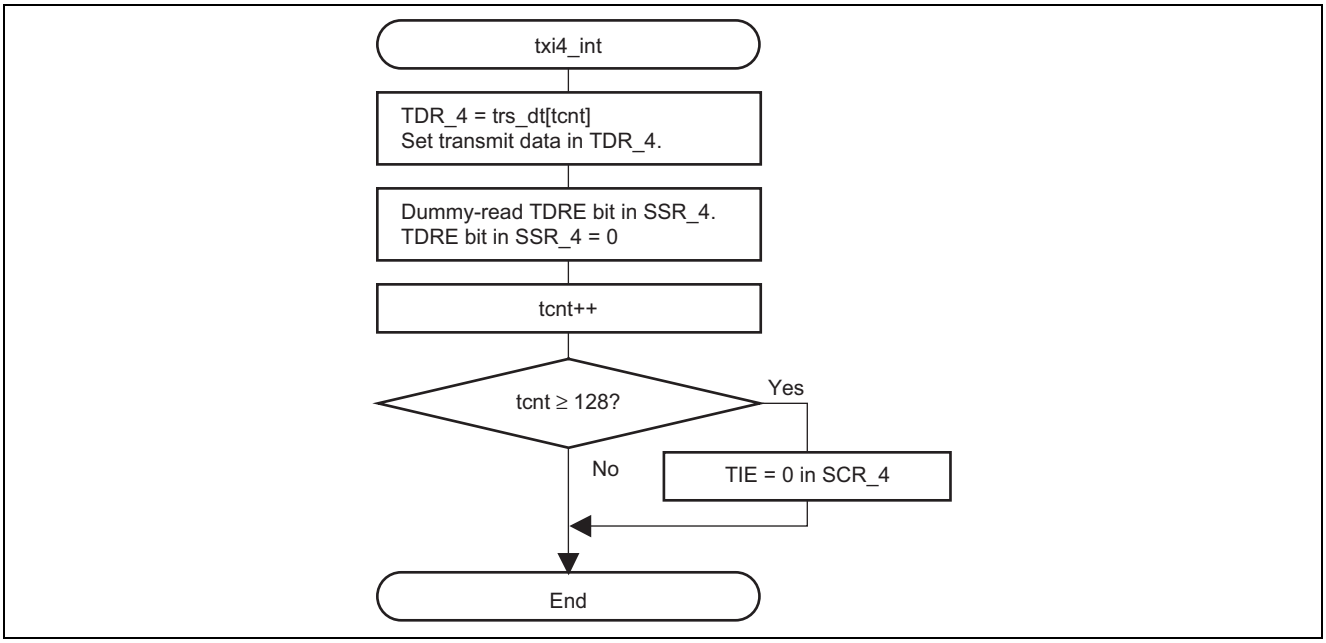
  Setting: trs_dt[tcnt]

- Serial status register_4 (SSR_4) Address: H'FFFE94

| Bit | Bit Name | Setting | R/W | Function |
|---|---|---|---|---|
| 7 | TDRE | Undefined | R/(W)* | Transmit Data Register Empty<br>Indicates whether TDR contains transmit data.<br>[Setting conditions]<br>• When the TE bit in SCR is 0<br>• When data is transferred from TDR to TSR<br>[Clearing conditions]<br>• When 0 is written to TDRE after reading TDRE = 1<br>• When the DMAC transfers transmit data to TDR due to a TXI interrupt |

Note: * Only 0 can be written to clear the flag.

(5) Flowchart



### 5.6.6 tei4_int Function

(1) Functional overview

Transmit end interrupt processing routine.

(2) Argument

None

(3) Return value

None

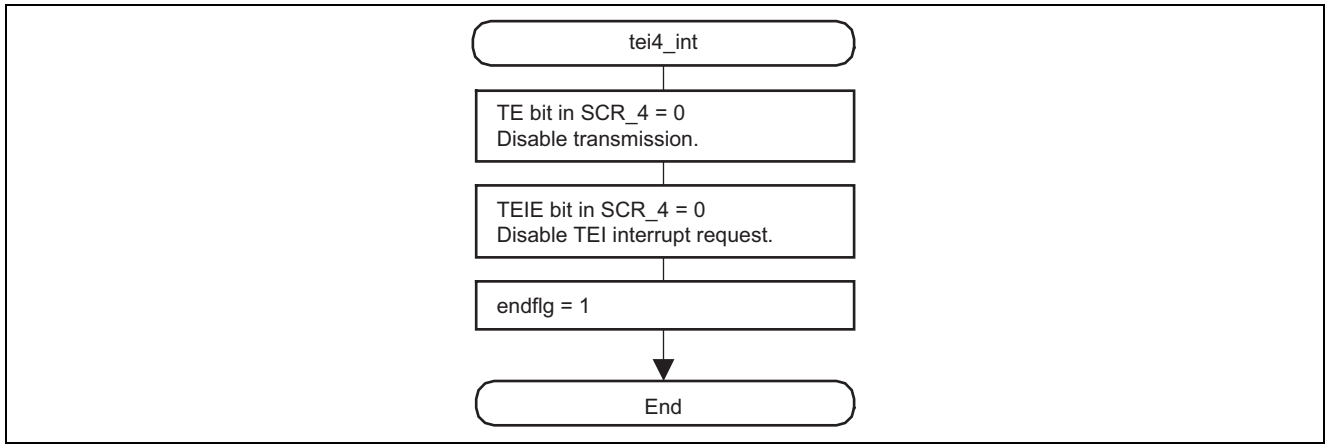
(4) Description of internal register

The internal registers used in this sample task are described below. The setting values shown below are the values used in this sample task and differ from their initial values.

- Serial control register_4 (SCR_4) Address: H'FFFE92

| Bit | Bit Name | Setting | R/W | Function |
|---|---|---|---|---|
| 5 | TE | 0 | R/W | Transmit Enable<br>0: Transmission is disabled<br>1: Transmission is enabled |
| 2 | TEIE | 0 | R/W | Transmit-End Interrupt Enable<br>0: TEI interrupt is disabled<br>1: TEI interrupt is enabled |

(5) Flowchart



## 6. Note on Usage

When the pin of the device functions as an input for the peripheral modules, the corresponding bits of the input buffer control register (PnICR) should be set to 1. For details, see the hardware manual.

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## Revision Record

| | | Description | |
|---|---|---|---|
| **Rev.** | **Date** | **Page** | **Summary** |
| 1.00 | Mar.10.06 | — | First edition issued |
| 2.00 | Mar.07.08 | 1, 24 | Page 1: Target devices added<br>Page 24: Note on usage added |
| | | | |
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