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H8SX Family

Short Format for Word/Longword-Sized Immediate Operands

Introduction

This application note describes the short format of word- and longword-sized immediate operands, which is one enhancement to the instruction set for the H8SX family relative to the set for the H8S.

Target Devices

H8SX family

Contents

1. Overview

The H8SX CPU used in H8SX-family products is a 32-bit CPU having an architecture that maintains upward compatibility with the H8/300, H8/300H, and H8S CPUs, and an instruction set that has been strengthened for better CPU performance. This leads to greatly improved code efficiency relative to the earlier series. This improved code efficiency reduces the amount of space that programs take up in ROM and the number of instruction-fetching cycles in program execution.

In the H8SX CPU, the instructions incorporate the capability of reduction in the length of the word and longword immediate operands. This is one way to realize programs that take up less space in ROM and require less time for instruction fetching. This application note describes this enhancement to the instruction set, i.e. the availability of short format of the word- and longword-sized immediate operands.

2. Applicable Conditions

Table 1 Applicable Conditions

Item	Contents
Development tool	High-performance Embedded Workshop Version 4.00.03
C/C++ compiler	H8S, H8/300 Series C/C++ Compiler Version 6.01.01 (from Renesas Technology Corp.)
H8SX compiler options	-cpu = h8sxa:24:md, -code = machinecode, -optimize = 1, -regparam = 3 -speed = (register,shift,struct,expression)
H8S compiler options	-cpu = 2600a:24, -code = machinecode, -optimize = 1, -regparam = 3 -speed = (register,shift,struct,expression)

Table 2 Section Settings

Address	Section Name	Description
H'001000	P	Program area
H'FF2000	B	RAM area

3. Configuration

Figure 1 illustrates the short format of the word- and longword-sized immediate operands. For the H8SX CPU, as shown in table 3, the #xx:3 and #xx:4 formats have been added to the H8/300, H8/300H, and H8S CPUs' addressing mode for immediate operands.

Table 3 Addressing Mode for Immediate Operands

CPU	Immediate				
H8/300	—	—	#xx:8	#xx:16	—
H8/300H	—	—	#xx:8	#xx:16	#xx:32
H8S	—	—	#xx:8	#xx:16	#xx:32
H8SX	#xx:3	#xx:4	#xx:8	#xx:16	#xx:32
	↑ Added	↑ Added			

For example, with the earlier H8S CPU, the #xx:16 format is used to set an immediate value of 0 to 7 in a short-type variable as a word-sized operand. With the H8SX CPU, however, the #xx:3 format is used instead, which eliminates the need to allocate a 16-bit area for program code and thereby reduces the program size.

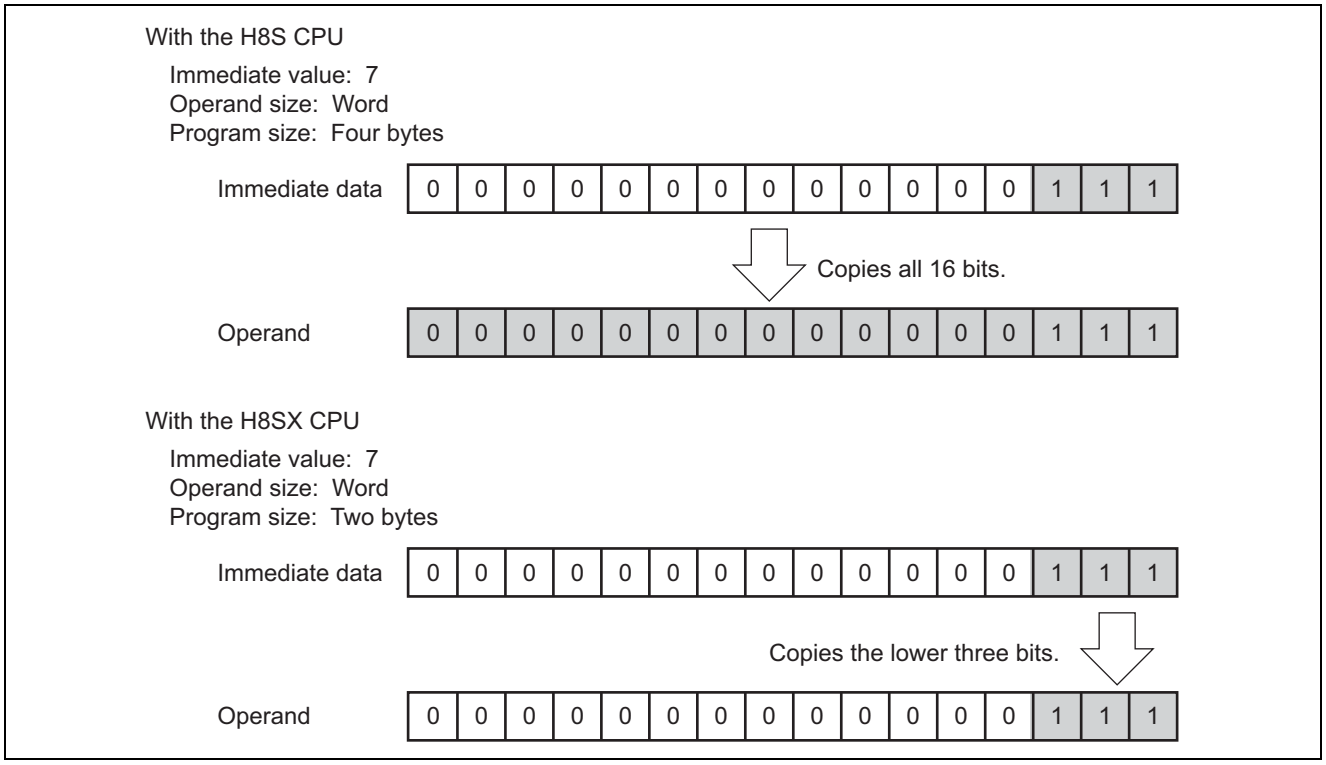
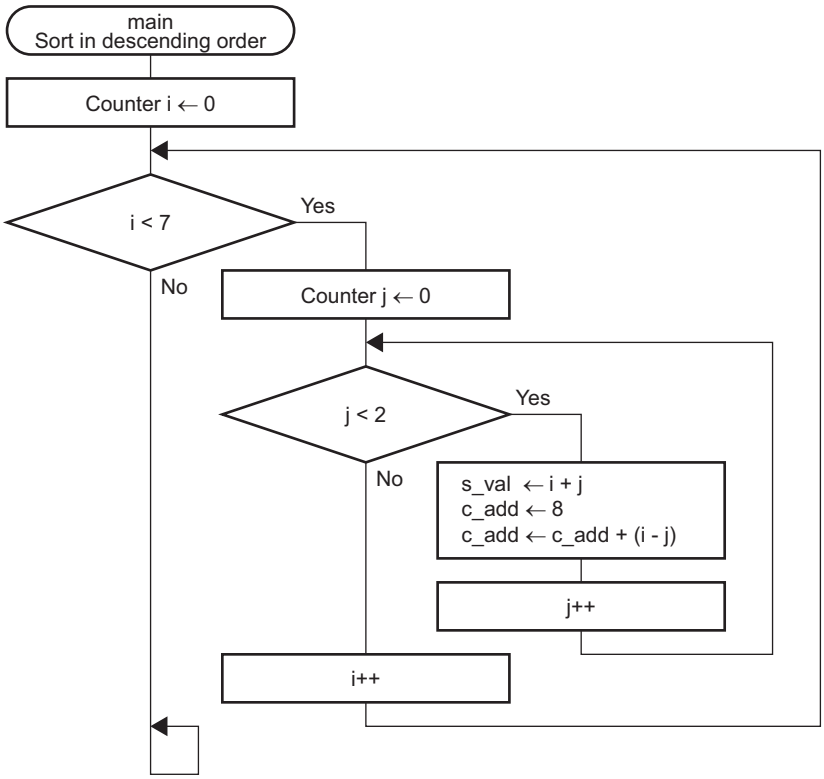


Figure 1 Example of Short Format for Word- and Longword-Sized Immediate Operands

4. Sample Program

4.1 Flowchart

This sample program is intended to convey an understanding of the short format of the word- and longword-sized immediate operands, one way in which the H8SX instruction set has been enhanced relative to that of the H8S. Shown below is a flowchart of the sample program, which compares the value of counter i with an immediate value of 7.



Note: * The results of compilation given in the following pages are to allow comparison with the H8S CPU. However, the results of compiling actual application programs will vary significantly with the source program and conditions of compilation.
Therefore, the results of compilation in this application note are only for reference.

4.2 Program Listing

A listing of the sample program in the C programming language is shown below. The results of compilation for the H8S CPU and H8SX CPU are given in section 4.3.

```
/************************************************************/
/*  Application Note                                        */
/************************************************************/

#include    <machine.h>

/************************************************************/
/* RAM allocation                                           */
/************************************************************/
short s_val;                                        /* short data          */
volatile char  c_add;                               /* char data           */

/************************************************************/
/* function prototype                                       */
/************************************************************/
void main ( void );

/************************************************************/
/*  Vector Address                                          */
/************************************************************/
#pragma entry main(sp=0xFFC000,vect=0)              /* H'0000 : Reset      */

#pragma section                                     /* P                   */
/************************************************************/
/*  Main Program                                            */
/************************************************************/
void main ( void )
{
    unsigned short i, j;

    for ( i = 0; i < 7; i++ ) {                     /* i Loop              */
        for ( j = 0; j < 2; j++ ) {                 /* j Loop              */
            s_val = i + j;                          /* i + j               */
            c_add = 8;                              /* c_add Initialize    */
            c_add += (i-j);
        }
    }

    while(1);
}
```

4.3 Results of Compilation

4.3.1 Results for the H8S CPU

The assembly code is shown below.

```
P                                                   ; section
  00000000 _main:                                   ; function: main
  00000000     MOV.L       #H'00FFC000,SP
  00000006     SUB.W       R0,R0
  00000008 L22:
  00000008     MOV.B       #2:8,R2L
  0000000A     SUB.B       R1H,R1H
  0000000C     MOV.W       R0,E1
  0000000E L23:
  0000000E     MOV.W       E1,@_s_val:32
  00000014     MOV.B       #8:8,R1L
  00000016     MOV.B       R1L,@_c_add:32
  0000001C     MOV.B       R0L,R1L
  0000001E     SUB.B       R1H,R1L
  00000020     MOV.B       @_c_add:32,R3L
  00000026     ADD.B       R3L,R1L
  00000028     MOV.B       R1L,@_c_add:32
  0000002E     INC.W       #1,E1
  00000030     INC.B       R1H
  00000032     DEC.B       R2L
  00000034     BNE         L23:8
  00000036     INC.W       #1,R0
  00000038     CMP.W       #7:16,R0
  0000003C     BLO         L22:8
  0000003E L25:
  0000003E     BRA         L25:8
B                                                   ; section
  00000000 _s_val:                                  ; static: s_val
  00000000     .RES.W      1
  00000002 _c_add:                                  ; static: c_add
  00000002     .RES.B      1
$VECT0                                              ; section
  00000000     .DATA.L     _main
```

4.3.2 Results for the H8SX CPU

The assembly code is shown below.

```
  00000000 _main:                                 ; function: main
  00000000     MOV.L       #H'00FFC000,SP
  00000006     SUB.W       R2,R2
  00000008 L22:
  00000008     MOV.W       #H'0200:16,R1
  0000000C     MOV.W       R2,E0
  0000000E L23:
  0000000E     MOV.W       E0,@_s_val:32
  00000014     MOV.B       #8:4,@_c_add:32
  0000001A     MOV.B       R2L,R0L
  0000001C     SUB.B       R1L,R0L
  0000001E     ADD.B       R0L,@_c_add:32
  00000026     INC.W       #1,E0
  00000028     INC.B       R1L
  0000002A     DEC.B       R1H
  0000002C     BNE         L23:8
  0000002E     INC.W       #1,R2
  00000030     CMP.W       #7:3,R2
  00000032     BLO         L22:8
  00000034 L25:
  00000034     BRA         L25:8
B                                               ; section
  00000000 _s_val:                              ; static: s_val
  00000000     .RES.W      1
  00000002 _c_add:                              ; static: c_add
  00000002     .RES.B      1
$VECT0                                          ; section
  00000000     .DATA.L     _main
```

4.4 Comparison of the Results of Compilation

The key portions of the compilation results for the H8S CPU and H8SX CPU are shown in tables 3 and 4, respectively. As shown in the tables, #7:3 is output with the H8SX CPU in contrast to #7:16 output with the H8S CPU, reducing the length of the instruction from 4 to 2 bytes and the execution time from 2 to 1 cycle.

Table 3 Results for the H8S CPU

Assembly Code		Instruction Length (Bytes)	Execution Time (Number of Cycles)
CMP.W	#7:16,R0	4	2
Total		4	2

Table 4 Results for the H8SX CPU

Assembly Code		Instruction Length (Bytes)	Execution Time (Number of Cycles)
CMP.W	#7:3,R2	2	1
Total		2	1

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Rev.	**Date**	**Page**	**Summary**
1.00	Sep.11.06	—	First edition issued

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