RX72M Group

SH7214/SH7216 to RX72M Microcontroller Migration Guide

Summary

This application note describes points requiring special attention, points of difference, etc., that need to be borne in mind when replacing the SH7214 or SH7216 with the RX72M in a user system. For detailed information on each function, refer to the latest version of the User's Manual: Hardware.

In this application note the SH7214 and SH7216 are referred to collectively as the SH7216 Group, and the specifications of the SH7216 are treated as representative. Although there are minor differences in functions and pins among the products composing the SH7216 Group, functionally they are all basically equivalent to the SH7216. This application note therefore applies to the entire SH7216 Group.

Target Device: RX72M

Contents

1. CPU Architecture

1.1 System Registers

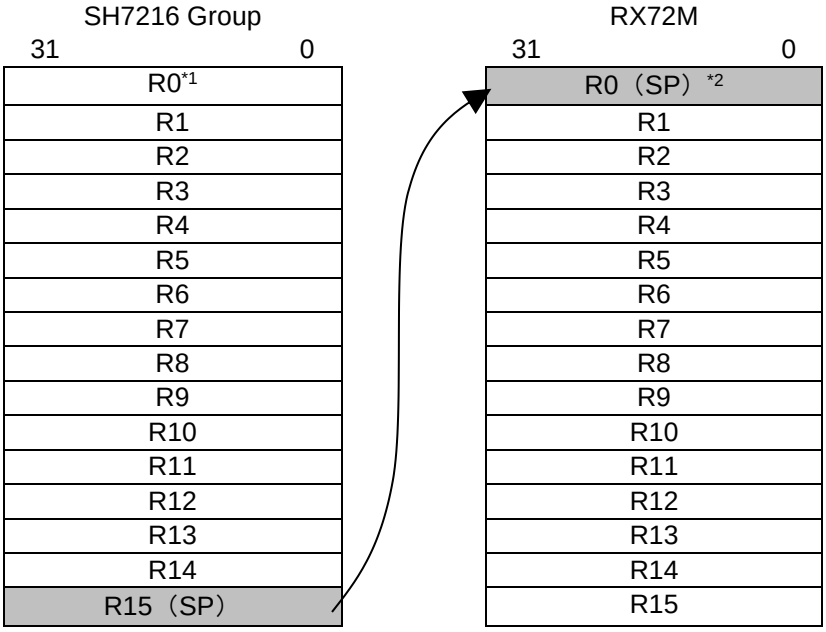
The points of difference between the registers of the SH7216 Group and the RX72M are described below.

1.1.1 General-Purpose Registers

The SH7216 Group and RX72M each have 16 32-bit general-purpose registers. They differ in that the register used as the stack pointer (SP) is different.

- SH7216 Group: R15
- RX72M: R0

Figure 1.1 shows the general-purpose registers of the SH7217 Group and RX72M. On the SH7216 Group R0 is also used as an index register.



Note 1. Used as the index register in the indexed register indirect and indexed GBR indirect addressing modes. R0 may be fixed as the source or destination register, depending on the instruction.

Note 2. The stack pointer (SP) can be switched between operation as the interrupt stack pointer (ISP) and as the user stack pointer (USP) by means of the U bit in PSW.

Figure 1.1 Differences Between General-Purpose Registers

1.1.2 Control Registers

Figure 1.2 shows the points of difference between the CPU registers (other than the general-purpose registers) of the SH7216 Group and the RX72M.

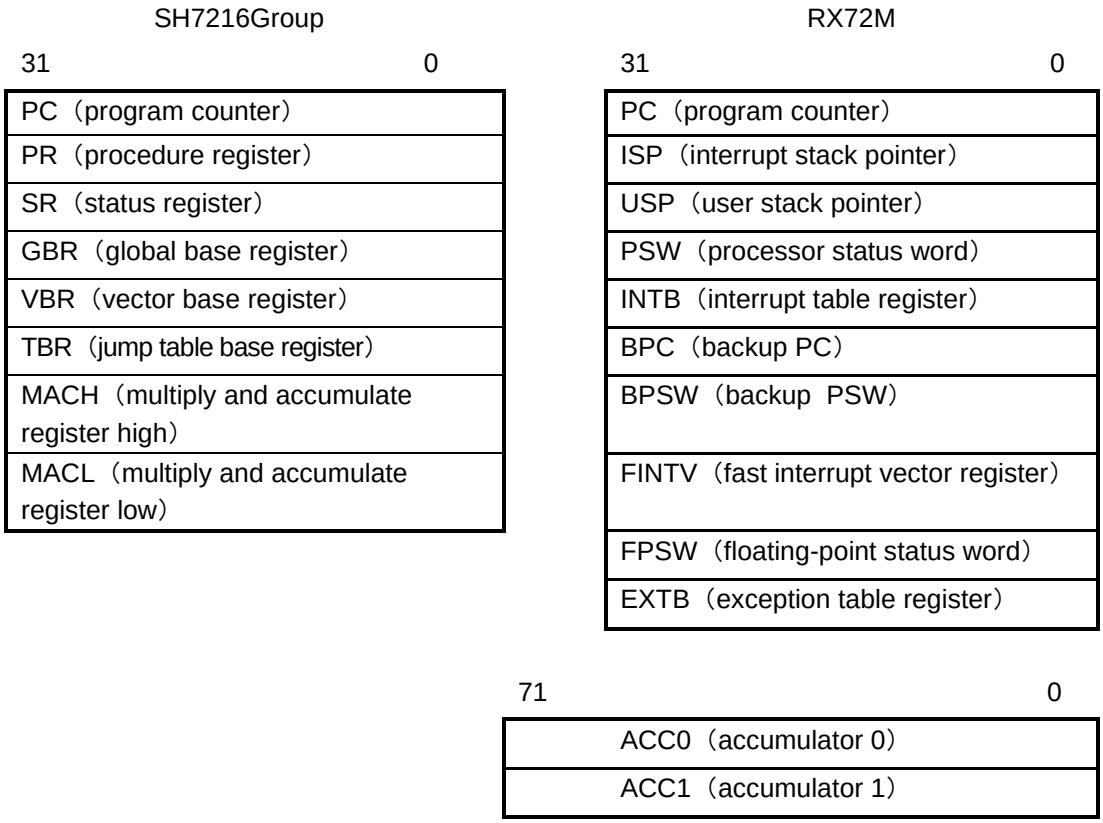


Figure 1.2 Points of Difference Between CPU Registers (Excluding General-Purpose Registers)

The RX72M has no registers corresponding to PR, GBR, and TBR on the SH7216 Group. The ACC0 and ACC1 registers on the RX72M corresponds to MACH and MACL on the SH7216 Group. An outline of the control registers that are implemented on the RX72M but not on the SH7216 Group is presented below.

Table 1.1 RX72M Control Registers Not Present on SH7216 Group

Register Name	Description
Interrupt stack pointer (ISP) User stack pointer (USP)	The RX72M has two types of stack pointers. The type of stack pointer used (ISP or USP) can be switched by means of the stack pointer select bit (U) in the processor status word (PSW) register.
Interrupt table register (INTB)*1	Specifies the start address of the interrupt vector table.
Exception table register (EXTB)*1	Specifies the start address of the exception vector table.
Backup PC (BPC) Backup PSW (BPSW)	The RX72M supports fast interrupts in addition to ordinary interrupts. For fast interrupts, the contents of PC and PSW are saved to dedicated registers (BPC and BPSW), thereby reducing the processing time needed to save the register data.
Fast interrupt vector register (FINTV)	This register specifies the jump destination when a fast interrupt occurs.
Floating-point status word (FPSW)	This register indicates the status of the calculation result (floating-point calculation result) generated by the RX72M's on-chip FPU.

Note 1. The functionality of this register is equivalent to that of VBR on the SH7216 Group.

Figure 1.3 and Table 1.2 show the points of difference between the status registers of the SH7216 Group and the RX72M.

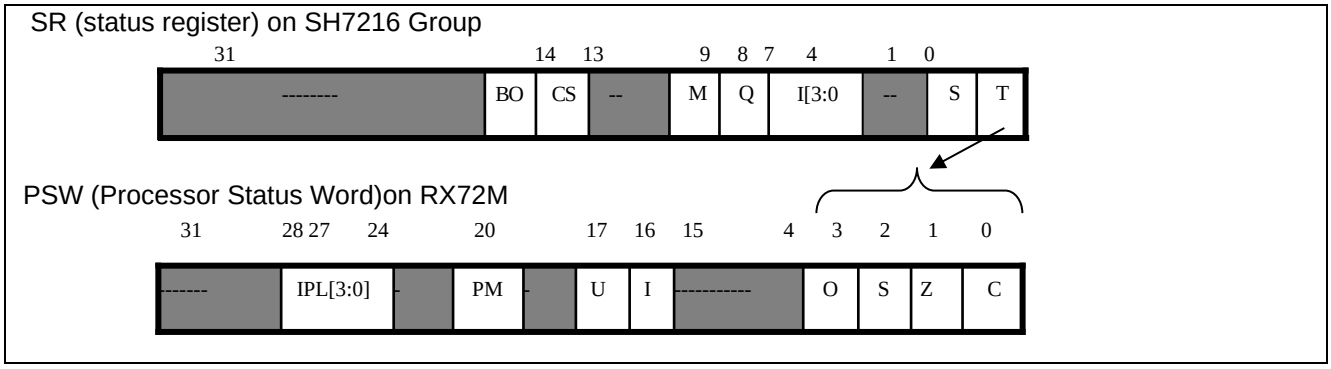


Figure 1.3 Differences Between SR (SH7216 Group) and PSW (RX72M)

Table 1.2 Differences Between SR (SH7216 Group) and PSW (RX72M)

SH Bit Name	RX Bit Name	Description
T	C Z S O	The calculation result (true/false, carry/borrow, etc.) indicated by the T bit on the SH7216 Group is shown by four flags (C, Z, S, and O) on the RX72M. C: Carry flag (0/1 = No carry has occurred./A carry has occurred.) Z: Zero flag S: Sign flag O: Overflow flag
S	—	Controls the functionality that prevents overflows during ALU arithmetic operations performed by the DSP unit of the SH7216 Group. On the RX72M there is no bit corresponding to the S bit, and the occurrence of an overflow during a floating-point operation is reported by the FPSW flag. It is also possible to perform exception handling when an overflow occurs.
I[3:0]	IPL[3:0]	These are the interrupt mask bits. Both the SH7216 Group and the RX72M support level settings from 0 (lowest) to 15 (highest). Only interrupts with a priority level higher than this setting are accepted.
Q	—	The Q bit is used by the DIV0U, DIV0S, and DIV1 instructions on the SH7216 Group. There is no corresponding bit on the RX72M.
M	—	The M bit is used by the DIV0U, DIV0S, and DIV1 instructions on the SH7216 Group. There is no corresponding bit on the RX72M.
CS	—	On the SH7216 Group the CS bit is used in CLIP instruction execution, but there is no equivalent bit on the RX72M.
BO	—	On the SH7216 Group the BO bit indicates that a register bank has overflowed, but there is no equivalent bit on the RX72M.
—	I	Interrupt enable bit 0: Interrupts are disabled. 1: Interrupts are enabled. This bit is used to enable interrupt requests on the RX72M. The initial state is 0, so it is necessary to set this bit to 1 in order to accept interrupts. It is set to 1 when a WAIT instruction is accepted and cleared to 0 when an exception is accepted. Note that the interrupt status flag of the interrupt controller is reset when an interrupt request occurs, regardless of the setting of this bit.
—	U	This bit specifies the stack pointer used by the RX72M. 0: Interrupt stack pointer (ISP) 1: User stack pointer (USP) This bit is cleared to 0 when an exception is accepted. It is set to 1 when a transition from supervisor mode to user mode occurs.
—	PM	This bit specifies the processor mode of the RX72M. 0: Supervisor mode 1: User mode This bit is cleared to 0 when an exception is accepted.

1.2 Option-Setting Memory

The RX72M is provided with an option-setting memory area containing registers for selecting the microcontroller state after a reset of the endian mode, watchdog timer operation, etc. Option-setting memory is allocated in the configuration setting area and user boot area of the flash memory, and the available setting methods are different for the two areas. For details, see the User's Manual: Hardware.

1.2.1 Outline of Option-Setting Memory

Figure 1.4 shows an outline of the option-setting memory area.

Address	Register name	Register overview
FE7F 5D00h～FE7F 5D03h	Endian selection registers (MDE)	CPU endian settings
FE7F 5D04h～FE7F 5D07h	Optional function selection register 0 (OFS0)	Various settings of watchdog timer
FE7F 5D08h～FE7F 5D0Bh	Optional function selection register 1 (OFS1)	Setting of voltage detection function, etc
FE7F 5D0Ch～FE7F 5D0Fh	Reserved area	—
FE7F 5D10h～FE7F 5D13h	TM Identification Data Register (TMINF)	TM Area that can be used for code storage that can identify the program stored in the target area
FE7F 5D14h～FE7F 5D1Fh	Reserved area	—
FE7F 5D20h～FE7F 5D23h	Bank selection register (BANKSEL)	Select the program boot bank when the code flash memory is in dual mode
FE7F 5D24h～FE7F 5D3Fh	Reserved area	—
FE7F 5D40h～FE7F 5D43h	Serial programmer command control register (SPCC)	Set enable / prohibition of serial programmer connection
FE7F 5D44h～FE7F 5D47h	Reserved area	—
FE7F 5D48h～FE7F 5D4Bh	TM enable flag register (TMEF)	Enables / disables the TM function for the code flash memory
FE7F 5D4Ch～FE7F 5D4Fh	Reserved area	—
FE7F 5D50h～FE7F 5D5Fh	OCD / Serial Programmer ID Setting Register (OSIS)	Stores the control code or ID code used to protect the ID code of the OCD / serial programmer
FE7F 5D60h～FE7F 5D63h	Reserved area	—
FE7F 5D64h～FE7F 5D67h	Flash access window setting register (FAW)	Set write protection bit and activation area selection bit
FE7F 5D68h～FE7F 5D6Fh	Reserved area	—
FE7F 5D70h～FE7F 5D73h	ROM code protect register (ROMCODE)	Prohibit flash memory read, program, and erase
FE7F 5D74h～FE7F 5D7Fh	Reserved area	—

Figure 1.4 RX72M Option-Setting Memory Area

1.2.2 Endian Setting

The SH7216 Group is fixed in big-endian mode. On the RX72M, instructions are fixed in little-endian, and the data order is selectable between little-endian and big-endian. The endian setting is specified by means of the endian select bits (MDE[2:0]) in the MDE register in the option-setting memory.

When switching from the SH7216 Group to the RX72M, it is possible to use big-endian order by specifying big-endian in the option settings of the genuine Renesas compiler. This allows migration without the need to be conscious of endianness in the user program.

The endian setting can be switched for each CS area in the external address space. However, instruction code cannot be allocated to an external space with an endian setting that differs from that of the MCU. When allocating instruction code to an external space, ensure that an area with the same endian setting as the MCU is used. (For details, see the User's Manual: Hardware.)

Endian settings based on the compiler option setting are illustrated in Figure 1.5.

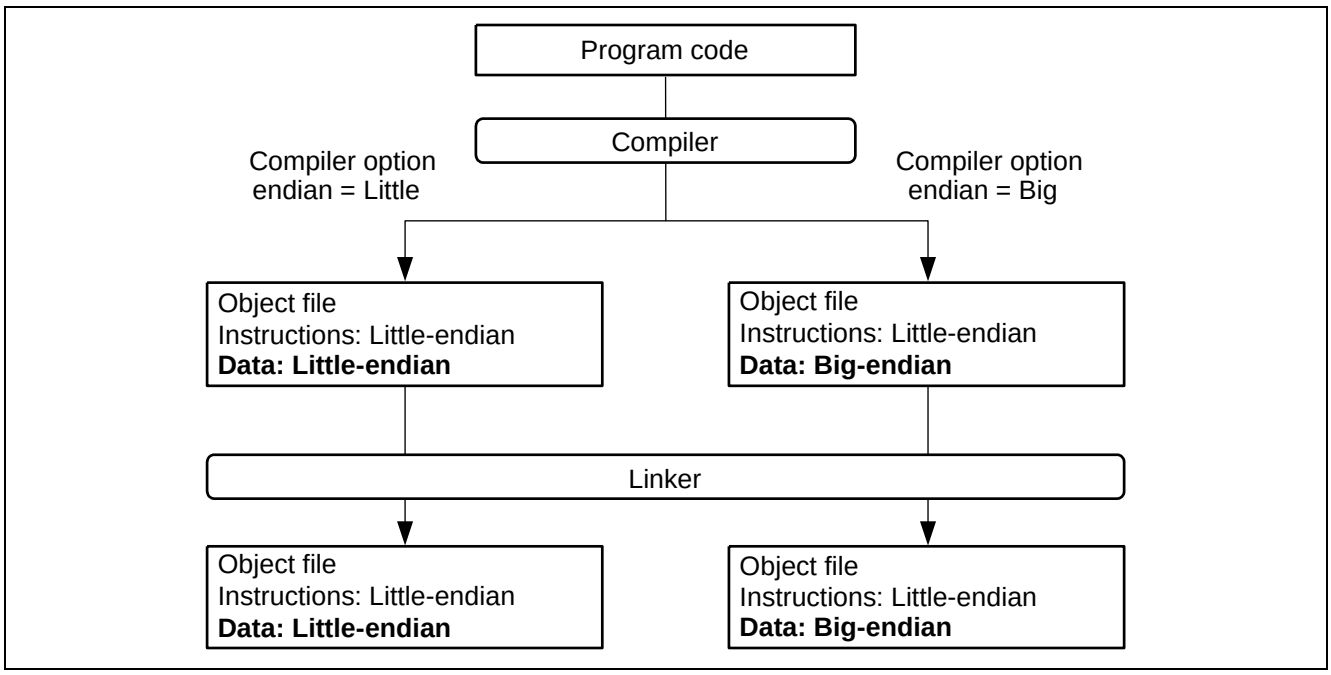


Figure 1.5 RX72M Specifying Endianness by Compiler Option

1.2.3 Specifying TM Identification Data and Setting TM Enable Flags

The RX72M is provided with a trusted memory (TM) function to prevent third parties from reading software stored in blocks 8 and 9 of the code flash memory. The TM function prevents reading of some designated areas even internally by the microcontroller, such as the on-chip flash memory, and allows instruction execution only.

This function is useful when storing program for processing encryption algorithms, device control processing program incorporating valuable intellectual property, commercial middleware, or the like in the code flash memory.

1.2.4 OCD(On-Chip debugger)/Serial Programmer Settings

The RX72M can provide limit on access for OCD (on-chip debuggers) and serial programmers.

When the serial programmer is completely prohibited from connection, it is controlled by the SPE bit of the SPCC register.

When the OCD/serial programmer is allowed to connect, the protection process can be done by judging the ID code written on the option setting.

A check is performed to determine if the code sent by the OCD/serial programmer matches the ID code in the option-setting memory. The connection to the OCD/serial programmer is enabled if the codes match, but no connection is possible if the codes do not match. The ID code of the OCD/serial programmer is stored in the OSIS register.

1.3 Reset Function

1.3.1 Reset Sources\

Figure 1.3 lists the reset sources of the SH7216 Group and RX72M.

Table 1.3 Reset Sources

Item	SH7216 Group	RX72M
Reset type	• Power-on reset (RES# pin reset/H-UDI reset assert command/WDT overflow) • Manual reset (MRES# pin reset/WDT overflow)	• RES# pin reset • Power-on reset (internal reset) • Voltage monitor 0 reset • Voltage monitor 1 reset • Voltage monitor 2 reset • Deep software standby reset • Independent watchdog timer reset • Watchdog timer reset • Software reset

1.3.1.1 Reset Vector Configuration

The SH7216 Group has separate vectors for power-on resets and for manual resets (PC and SP).*1

The RX72M has a single reset vector for multiple reset sources. The reset source is identified in reset status registers 0 to 2 during reset processing, and processing for the corresponding source is performed.

1.3.1.2 Stack Pointer

On the SH7216 Group, it is necessary to specify the end address (+1) of the stack area in the reset vector. There is no stack pointer setting area in the vector table on the RX72M, so the stack pointer is set in ISP and USP.

Note 1. See 1.7.4, Vector Configuration, for details of the vector tables.

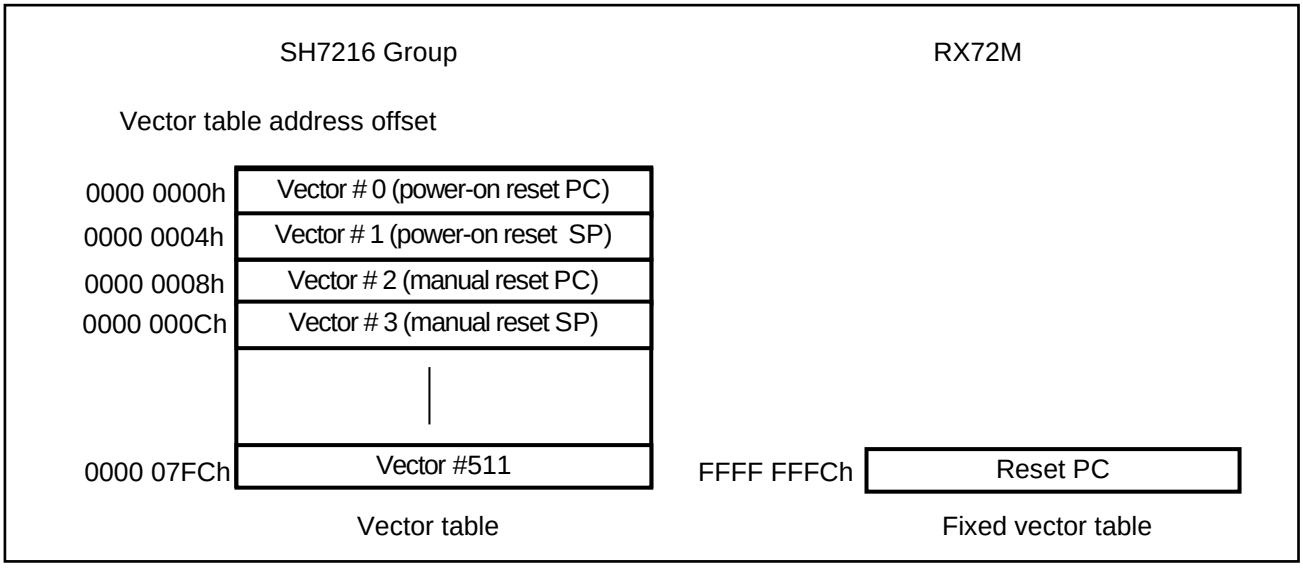


Figure 1.6 Reset Vector Comparison

1.3.2 Reset Sources and Initialization Scope

The initialization scope of the reset sources differs between the SH7216 Group and the RX72M. Table 1.4 lists the reset sources and their initialization scope on the SH7216 Group, and Table 1.5 lists the reset sources and their initialization scope on the RX72M. For details, see the User's Manual: Hardware.

Table 1.4 SH7216 Group Reset Sources and Initialization Scope

Item		CPU FPU	On-Chip Peripheral Module, I/O Port	WRCSR of WDT, FRQCR of CPG
Power-on reset	RES# pin reset	○	○	○
	H-UDI command	○	○	○
	WDT overflow	○	○	—
Manual reset	MRES# pin reset	○	—*1	—
	WDT overflow	○	—*1	—

○: Reset —: No reset

Note 1. The BN bit in IBNR of the INTC is initialized.

Table 1.5 RX72M Reset Sources and Initialization Scope

	Reset Sources								
Reset Target	RES# Pin Reset	Power-On Reset	Voltage Monitor 0 Reset	Independent Watchdog Timer Reset	Watchdog Timer Reset	Voltage Monitor 1 Reset	Voltage Monitor 2 Reset	Deep Software Standby Reset	Software Reset
Power-on reset detection flag	○	—	—	—	—	—	—	—	—
Cold start/warm start determination flag	—	○	—	—	—	—	—	—	—
Voltage monitor 0 reset detection flag	○	○	—	—	—	—	—	—	—
Independent watchdog timer reset detection flag	○	○	○	—	—	—	—	○	—
Independent watchdog timer registers	○	○	○	—	—	—	—	○	—
Watchdog timer reset detection flag	○	○	○	○	—	—	—	○	—
Watchdog timer registers	○	○	○	○	—	—	—	○	—
Voltage monitor function 1 registers	○	○	○	○	○	—	—	*1	—
Voltage monitor 2 reset detection flag	○	○	○	○	○	○	—	—	—
Voltage monitor function 2 registers	○	○	○	○	○	○	—	*2	—
Deep software standby reset detection flag	○	○	○	○	○	○	○	—	—
Software reset detection flag	○	○	○	○	○	○	○	○	—
Realtime clock registers*3	—	—	—	—	—	—	—	—	—
High-speed on-chip oscillator–related registers	○	○	○	○	○	○	○	—	○
Main clock oscillator–related registers	○	○	○	○	○	○	○	—	○
Pin states	○	○	○	○	○	○	○	—	○
Low power consumption–related registers*4	○	○	○	○	○	○	○	—	○
Registers other than the above, CPU, and internal state	○	○	○	○	○	○	○	○	○

○: Reset —: No reset

Note 1. Only LVD1CR1 and LVD1SR are initialized.

Note 2. Only LVD2CR1 and LVD2SR are initialized.

Note 3. Some control bits are initialized by all resets.

Note 4. The DPSBKRy registers are not initialized by any reset.

1.3.3 Cold Start/Warm Start Determination Function

On the RX72M it is possible to determine whether the most recent reset processing was caused by a power-on reset (cold start) or by a reset signal during operation (warm start).

When a power-on reset occurs because the external voltage (VCC) has exceeded the threshold, the cold/warm start determination flag (RSTSR1.CWSF) is cleared to 0, indicating a cold start. Since the flag is not cleared to zero by any other type of reset, 1 can be written to it by a program, indicating a warm start.

1.3.4 Write Protection

The RX72M is protected by a register write protection function to protect important registers from being overwritten if program runaway occurs. The software reset register is protected by this function.

If necessary, set protect bit 1 (PRCR.PRC1) to 1 to enable writes before writing to the software reset register.

1.4 Clock Settings

1.4.1 Clock Sources

Table 1.6 lists the clock sources of the SH7216 Group and RX72M.

Table 1.6 Clock Sources

SH7216 Group	RX72M
Oscillator (EXTAL and XTAL) + PLL circuit USB oscillator (USBEXTAL and USBXTAL) *1	• Main clock oscillator (EXTAL and XTAL) + PLL circuit • Subclock oscillator (XCIN and XCOUT) • High-speed on-chip oscillator (HOCO) + PLL circuit • Low-speed on-chip oscillator (LOCO) • IWDT-dedicated on-chip oscillator

In the description below, the high-speed on-chip oscillator is referred to as the HOCO and the low-speed on-chip oscillator as the LOCO.

* 1: The RX72M does not have a USB oscillator, but a main clock oscillator or a high-speed on-chip oscillator can supply the clock to USB.

1.4.2 Clock Generation Circuit

On the SH7216 Group application of divider settings and oscillation stop detection control are performed in software. On the RX72M a variety of clock control operations are performed in software.

On the RX72M the LOCO operates as the clock source after a reset. The operation of necessary clock sources and PLL circuits other than the LOCO is started during system initialization, and various clocks are selected, such as the system clock and bus clocks. When making changes to clock-related settings, it is necessary to consider the register setting sequence and the oscillation and clock oscillation stabilization time.

See the following application note for details of the clock setting procedure.

RX72M Group Initial Settings （R01AN4530EJ）

1.4.3 Write Protection

The RX72M is protected by a register write protection function to protect important registers from being overwritten if program runaway occurs, and the registers related to the clock generation circuit are protected by this function.

If necessary, set protect bit 0 (PRCR.PRC0) or protect bit 1 (PRCR.PRC1) to 1 to enable writes before writing to these registers.

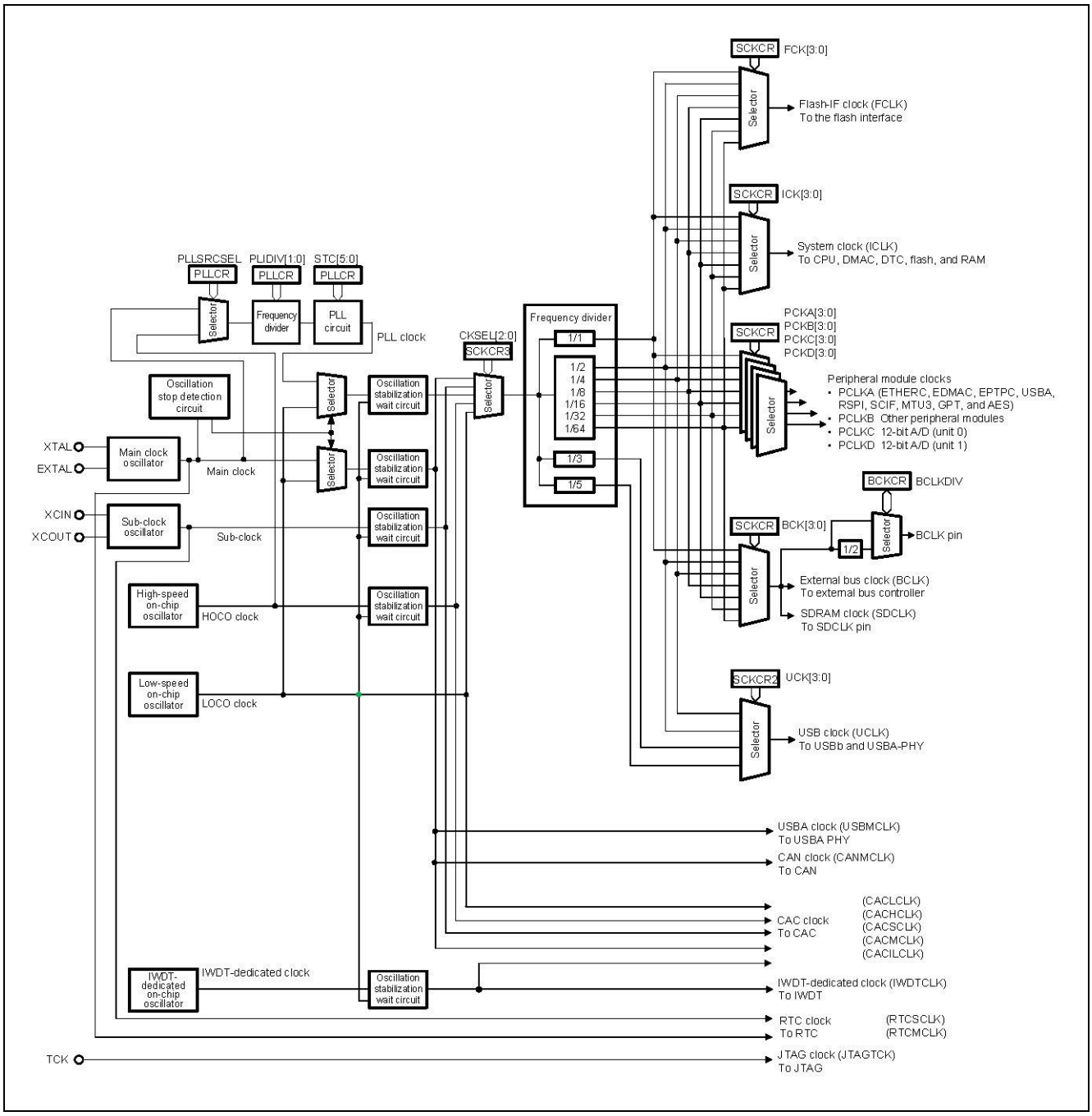


Figure 1.7 RX72M Block Diagram of Clock Generation Circuit

1.5 Operation Modes

1.5.1 Comparison of Operation Modes

Table 1.7 shows a comparison of the operation modes of the SH7216 Group and RX72M.

For details of each operation mode, see the User's Manual: Hardware.

Table 1.7 Comparison of Operation Modes

SH7216 Group	RX72M	Description
MCU extension mode 0	On-chip ROM disabled extended mode	An operation mode in which the on-chip ROM is disabled and the external address space is enabled. The external bus width differs from that of mode 0 and mode 1 on the SH7216 Group.
MCU extension mode 1		
MCU extension mode 2	On-chip ROM enabled extended mode	An operation mode in which the on-chip ROM is enabled and the external address space is enabled
Single-chip mode	Single-chip mode	An operation mode in which the on-chip ROM is enabled and the external address space is disabled
Boot mode	Boot mode (SCI interface)	An operation mode in which the on-chip flash memory modifying program (boot program), which is stored in a dedicated area internal to the microcontroller, is run. The on-chip ROM can be programmed by a device external to the microcontroller by using the asynchronous serial interface.
USB boot mode	Boot mode (USB interface)	An operation mode in which the on-chip flash memory modifying program (boot program), which is stored in a dedicated area internal to the microcontroller, is run. The on-chip ROM (code flash memory) can be programmed by a device external to the microcontroller by using the USB interface.
User boot mode	—	An operation mode in which the on-chip flash memory modifying program (user boot program), arbitrarily written by the user in a dedicated area internal to the microcontroller, is run.
User program mode	Single chip mode	A mode in which the om-chip flash memory is rewritten by the write / erase control program prepared in advance by the user, which transitions only by changing the setting of the FWE pin value. The RX72M can also achieve the same function in single-chip mode, but there is no need to change the pins.

1.5.2 Comparison of Memory

Figure 1.8 shows a comparison of memory maps in on-chip ROM enabled mode.

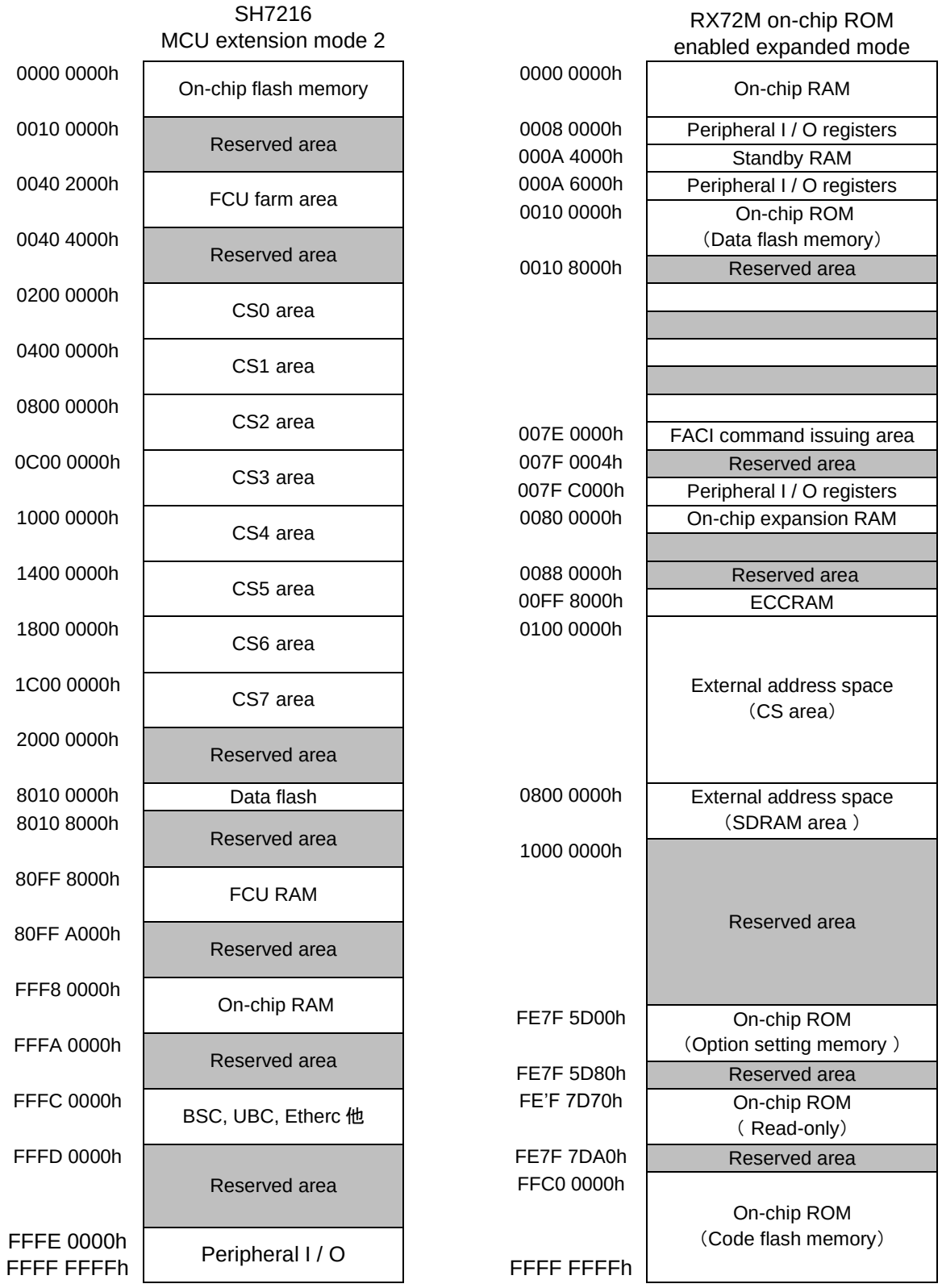


Figure 1.8 Memory Map Comparison (On-Chip ROM Enabled Mode)

Figure 1.9 shows a comparison of memory maps in single-chip mode.

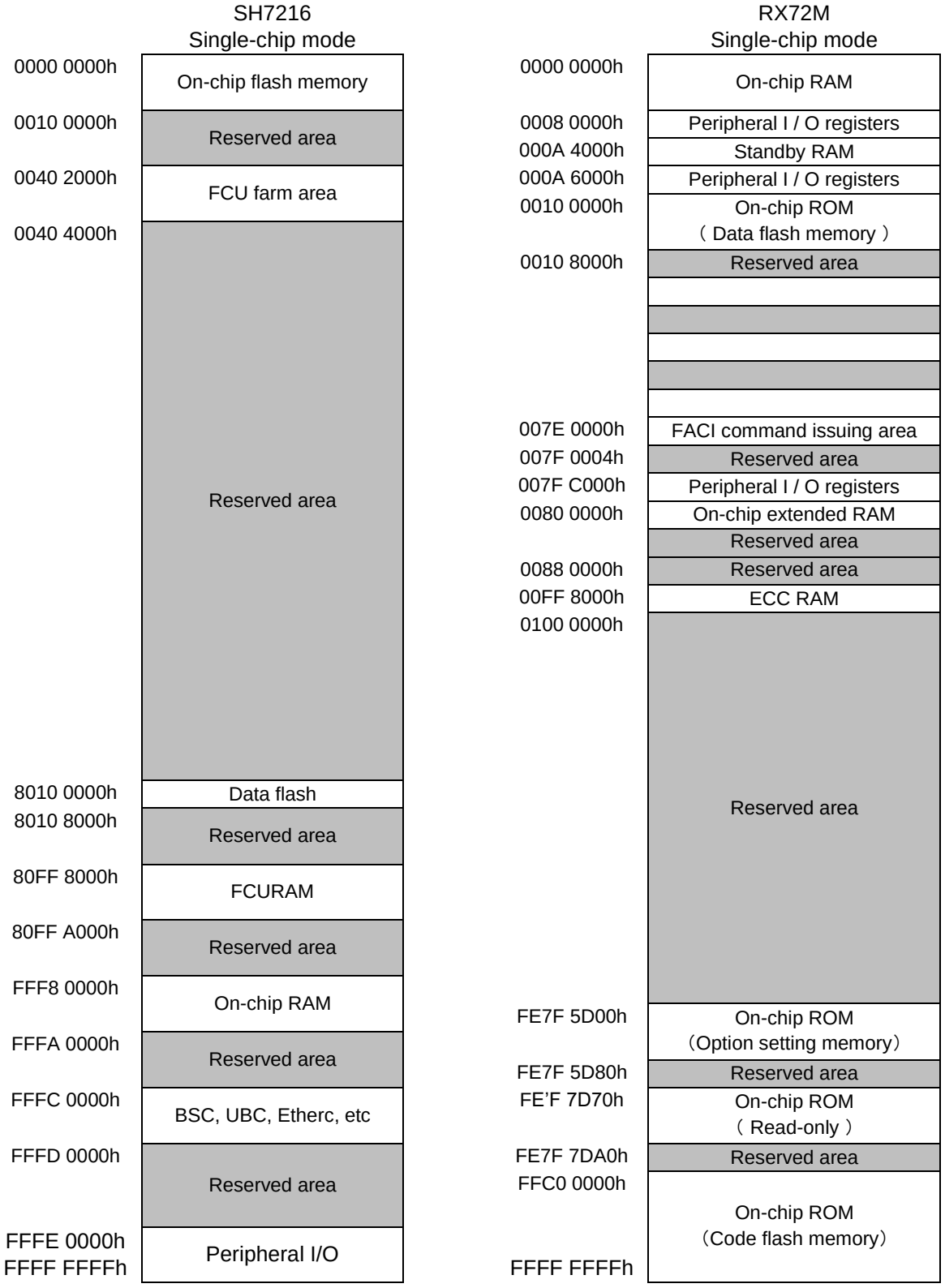


Figure 1.9 Memory Map Comparison (Single-Chip Mode)

Figure 1.10 shows a comparison of memory maps in on-chip ROM disabled mode.

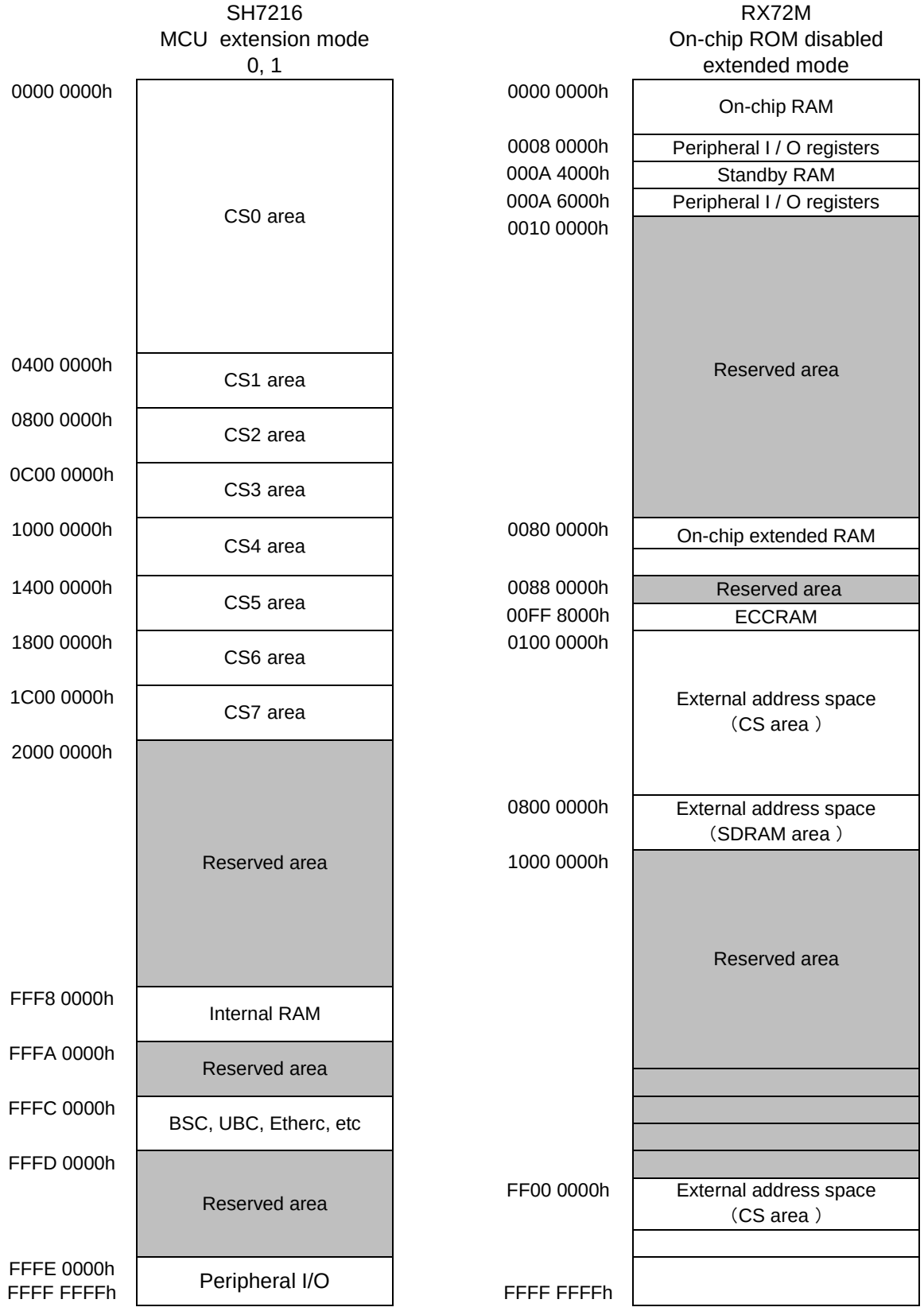


Figure 1.10 Memory Map Comparison (On-Chip ROM Disabled Mode)

- On the RX72M the RAM is allocated to addresses adjacent to 0000 0000h and ROM (for reading data) to addresses adjacent to FFFF FFFFh.
- On the RX72M the peripheral I/O registers are allocated within the address range from 0008 0000h to 000A 3FFFh and 000A 6000h to 000F FFFFh, and only the flash-related registers are allocated within the address range from 007F E000h to 007F FFFFh.
- On the RX72M the external address space is allocated within the address ranges from 0100 0000h to 0FFF FFFFh and FF00 0000h to FFFF FFFFh, and configured as up to eight CS spaces of 16 MB each and a 128 MB SDRAM space. In on-chip ROM enabled extended mode the CS0 area from FF00 0000h to FFFF FFFFh is disabled.

1.5.3 Operation Mode Settings

Whereas on the SH7216 Group operation mode settings are made only with the MD1, MD0, and FWE pins, on the RX72M operation mode settings can be made by means of the MD and UB pins when a reset is canceled, or by software after a reset is canceled.

Table 1.8 lists the operation modes that are determined by pin settings, and Table 1.9 lists the operation modes that are set in software after a reset is canceled.

Table 1.8 Pin Settings and Operation Modes on RX72M

Pin		
MD	**UB**	**Operation Mode**
High	—	Single-chip mode
Low	Low	Boot mode (SCI interface)
	High	Boot mode (USB interface)
Low → High*1	Low	Boot mode (FINE interface)

Note 1. After resetting the MD pin to Low, switch to High between 20 and 100 msec.

Table 1.9 SYSCR0 Register Settings and Operation Modes on RX72M

SYSCR0 Register		
ROME Bit*1	**EXBE Bit**	**Operation Mode Name**
0 (on-chip ROM disabled)	0 (external bus disabled)	Single-chip mode
1 (on-chip ROM enabled)*2	0 (external bus disabled)*2	
0 (on-chip ROM disabled)	1 (external bus enabled)	On-chip ROM disabled extended mode
1 (on-chip ROM enabled)	1 (external bus enabled)	On-chip ROM enabled extended mode

Note 1. Once the ROME bit is cleared to 0 it cannot be set to 1 again.
Note 2. After the STSCR0 register is reset, ROME = 1 and EXBE = 0.

1.5.4 Write Protection

The RX72M is protected by a register write protection function to protect important registers from being overwritten if program runaway occurs, and the operation mode related registers are protected by this function.

If necessary, set protect bit 1 (PRCR.PRC1) to 1 to enable writes before writing to these registers.

1.6 Processor Modes

The RX72M supports two processing modes: supervisor mode and user mode. These processor modes enable hierarchical CPU resource protection.

Table 1.10 RX72M Processor Modes

Processor Modes	Transition Conditions	Outline
Supervisor mode	• Reset cancellation • Exception occurrence (PSW.PM bit cleared to 0) When an exception occurs a transition to supervisor mode takes place, but the processor mode preceding the exception is restored following return from the exception handler.	All CPU resources are accessible, and all instructions can be executed (no limitations). This is the mode in which the OS and other system programs ordinarily operate.
User mode	• PSW.PM bit set to 1 In this case, first set to 1 the PSW.PM bit saved to the stack, then execute the RTE instruction. Alternately, first set to 1 the PSW.PM bit saved to BPSW, then execute the RTFI instruction.	Write access to some CPU resources, such as some bits in PSW and to BPC and BPSW, is restricted, and privileged instructions cannot be used. This is the mode in which user programs such as application programs ordinarily operate.

Transitioning from supervisor mode to user mode

The C/C++ Compiler Package for RX Family provides the intrinsic function chg_pmusr()*1 for switching to user mode.

The intrinsic function can be declared in the C source code. The output code does not perform a normal function call, but outputs the corresponding assembler code.

Note 1. The __chg_pmusr() function is available for use in C/C++ Compiler Package for RX Family (V.2.05.00) and later.

Figure 1.11 Processor Mode Setting Example (User Mode)

Transitioning from user mode to supervisor mode

An exception is generated by using the INT instruction or BRK instruction to generate an unconditional trap. A transition to supervisor mode occurs during exception handling.

Figure 1.12 Processor Mode Setting Example (Supervisor Mode)

1.7 Exception Handling

The points of difference regarding exception handling in general on the SH7216 Group and RX72M, including interrupts, are described below.

1.7.1 Types of Exception Handling

Table 1.11 shows a comparative listing of exception sources on the SH7216 Group and RX72M.

Table 1.11 Exception Source Comparison

SH7216 Group	RX72M	Main Points of Difference
Power-on reset Manual reset	Reset	On the RX72M there is a single reset vector. Reset status registers 0 to 2 are checked during reset interrupt handling to determine the reset source, and appropriate processing is performed.
Address error	Address exception	In SH7216, it occurs when accessing the access prohibited area, word, longword, double longword data from other than the respective boundaries, and when accessing the external memory in single chip mode. RX72M occurs when a 64-bit operand is accessed for a address other than a 32-bit boundary address. Access to the prohibited area is detected by the memory protection unit. In SH7216, when this exception occurs, the PC of the next instruction is evacuated. RX72M, evacuate the PC of the exception occurrence instruction
Interrupt （NMI）	Non-maskable interrupt	The RX72M has separate vector tables for maskable and non-maskable interrupts.
Interrupt (External / Internal)	Interrupt (External / Internal)	RX72M also has high-speed interrupts (level 15)
Register bank error	—	—
TRAP instruction (TRAPA instruction)	Unconditional trap (INT, BRK instruction)	The SH7216 Group has 32 sources, but the RX72M has 16 sources with dedicated vectors (up to 256 sources when sources also used for interrupts are included).
General illegal instruction Illegal slot instruction	Undefined instruction	In SH7216, when undefined codes located other than immediately after the delay branch (delay slot) are decoded, general opaque examples are undefined codes placed immediately after the delay branch instruction (delay slot), instructions to rewrite PC, 3 2-bit instructions, RESBANK instructions, the DIVS or DIVU instructions are decoded. The RX72M raises an undefined instruction exception when it detects the execution of an undefined instruction.
Integer division instruction	—	RX72M has no exceptions for integer division instructions.
Floating-point operation instruction	Single-precision floating-point exceptions	None
—	Privileged instruction	The SH7216 Group has no exception that occurs when a privileged instruction is detected in user mode.

1.7.2 Exception Handling Priority

Table 1.12 shows the comparative priority of exception sources on the SH7216 Group and the RX72M.

Table 1.12 Exception Event Priority

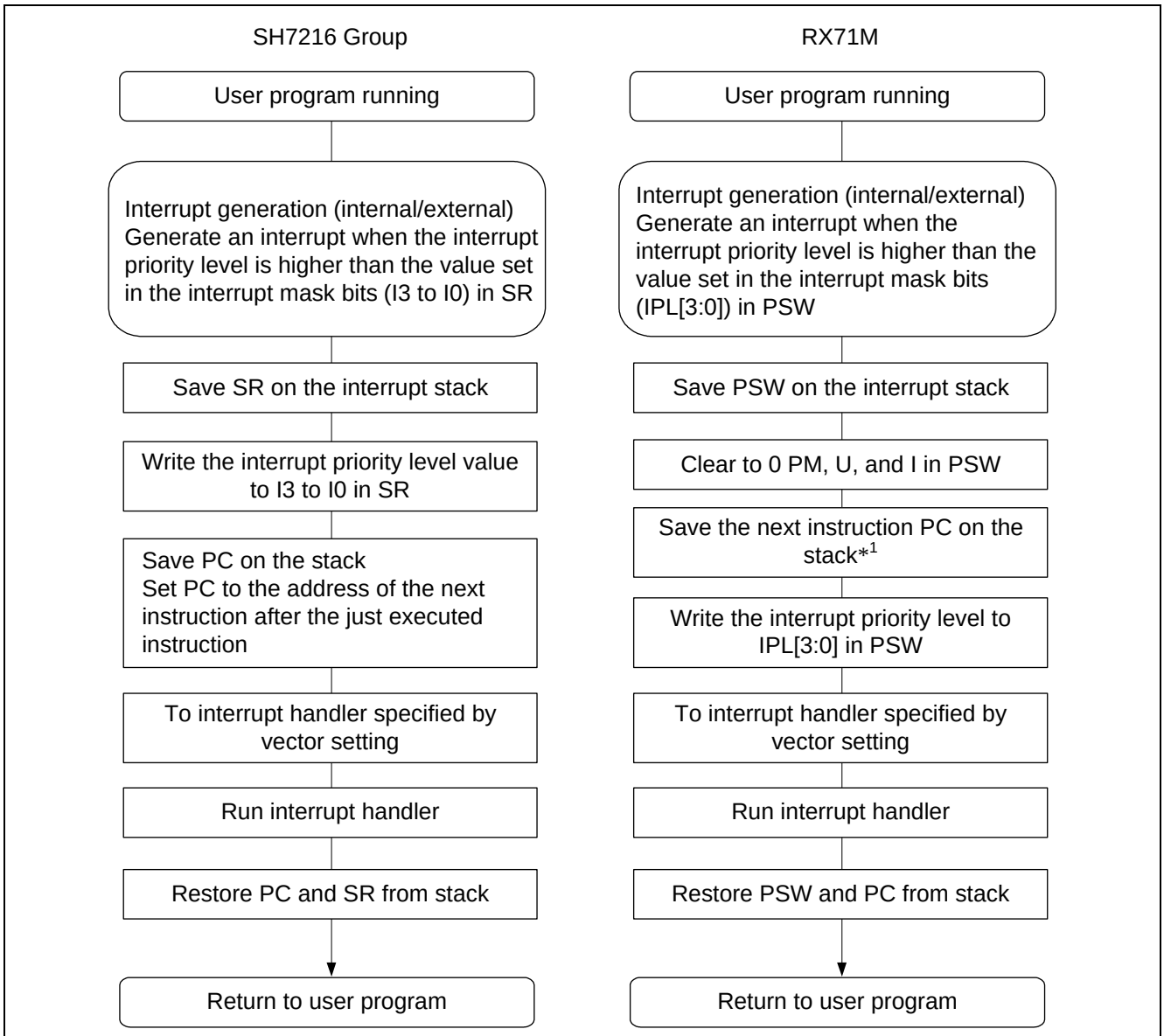
Priority*1	SH7216 Group	RX72M
High	Power-on reset	Reset
▲	Manual reset	Non-maskable interrupt
|	Address error	Interrupt
|	Floating-point operation instruction, integer division instruction	Access exception (instruction access exception)
|	Register bank error	Undefined instruction exception, privileged instruction exception
|	Interrupt	Unconditional trap
|	TRAP instruction	Address exception
|	General illegal instruction	Access exception (operand access exception)
Low	illegal slot instruction	Single precision floating point exception

Note 1. Among interrupts, the priority is determined by the interrupt controller.

Whereas on the SH7216 Group interrupts have low priority, on the RX72M they have high priority.

1.7.3 Basic Processing Sequence of Exception Handling

Figure 1.13 is a flowchart of interrupt exception handling on the SH7216 Group and the RX72M.



Note 1. When the instruction being executed is RMPA, SCMPU, SMOVB, SMOVF, SMOVU, SSTR, SUNTIL, or SWHILE, the PC of the instruction being executed is saved on the stack.

Figure 1.13 Interrupt (Internal/External) Processing Sequence

1.7.4 Vector Configuration

Both the SH7216 Group and the RX72M have a relocatable vector configuration, which allows vector tables to be reallocated.

On the SH7216 Group VBR (the vector base register) specifies the start of the vector table. (Note that VBR is initialized to 0 after a reset, so it is not possible to change the reset vector.)

On the RX72M INTB (the interrupt table register) specifies the start of the interrupt vector table, and EXTB (the exception table register) specifies the start of the exception vector table. Relocatable interrupt and unconditional trap vectors are assigned in the interrupt vector table. System exceptions are assigned in the exception vector table. The RX72M has a fixed reset vector. Also, the fast interrupt vector address is set in the FINTV register.

Figure 1.14 shows the differences between the vector tables.

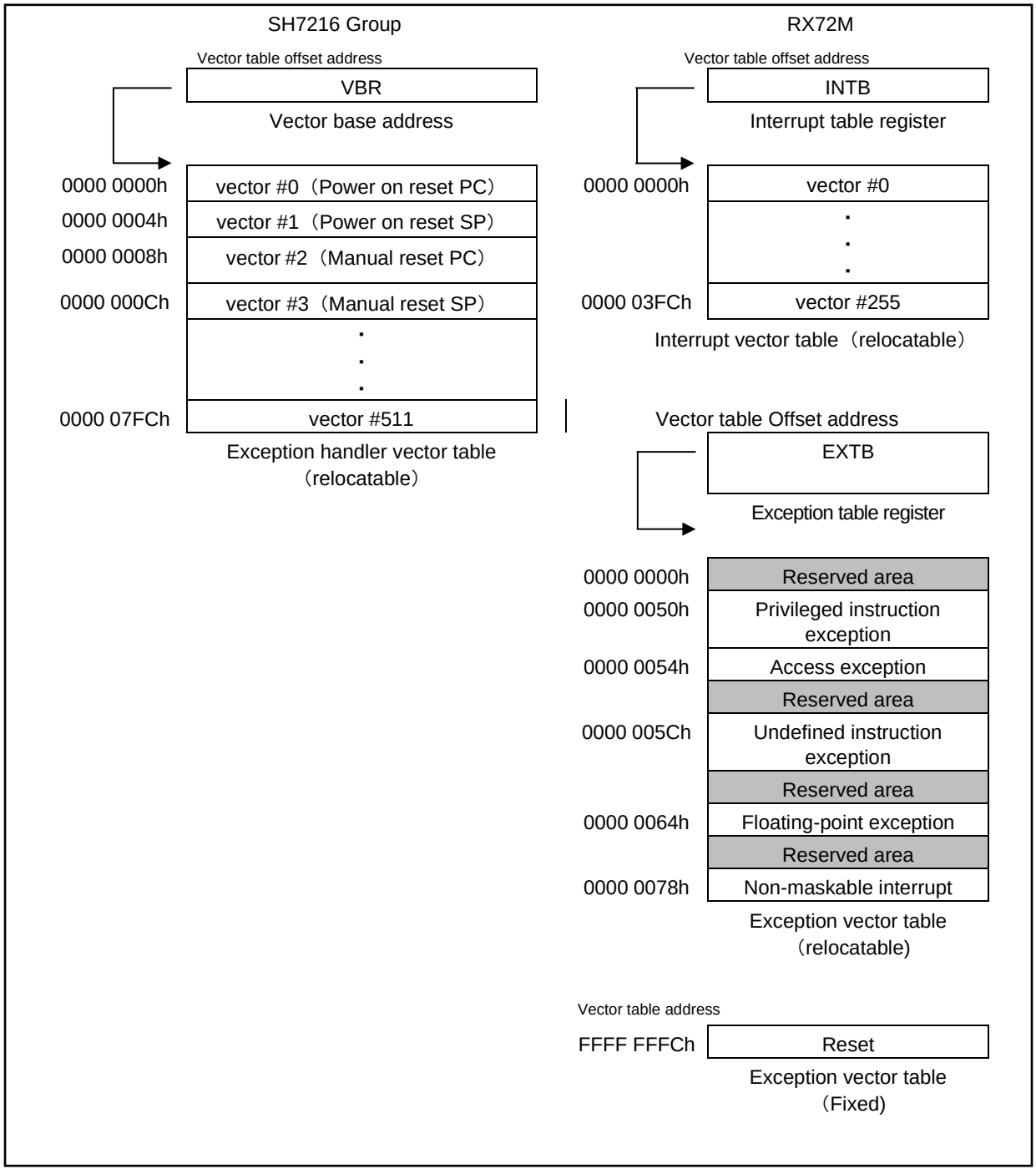


Figure 1.14 Vector Table Settings

1.7.5 Interrupt Masking by SR (SH7216 Group) and PSW (RX72M)

On the RX72M the I bits in control register PSW are used to set the interrupt mask level. The I bits indicate which interrupts are enabled and which are disabled.

Table 1.13 Interrupt-Related Bits in SR and PSW

SH7216 Group	RX72M	
SR Register	**PSW Register**	**Description**
I[3:0]	IPL[3:0]	CPU interrupt mask level (priority level) Setting value: 0 to Fh (levels 0 to 15) When an interrupt request occurs, this level setting is compared with the priority level set for the individual interrupt source, and the interrupt is enabled if its level setting is higher than the mask level.
—	I	Interrupt enable bit 0: Interrupts are disabled. 1: Interrupts are enabled. When an interrupt occurs, the interrupt status flag in the interrupt controller is set to 1. After a system reset, this bit is set to 1, enabling acceptance of interrupts. When an exception is accepted, this bit is cleared to 0 and no interrupts are accepted while its value remains 0.

1.8 Interrupt Handling

This section describes the differences in interrupt handling between the SH7216 Group and RX72M, with the focus on the interrupt controller.

1.8.1 Interrupt Controller

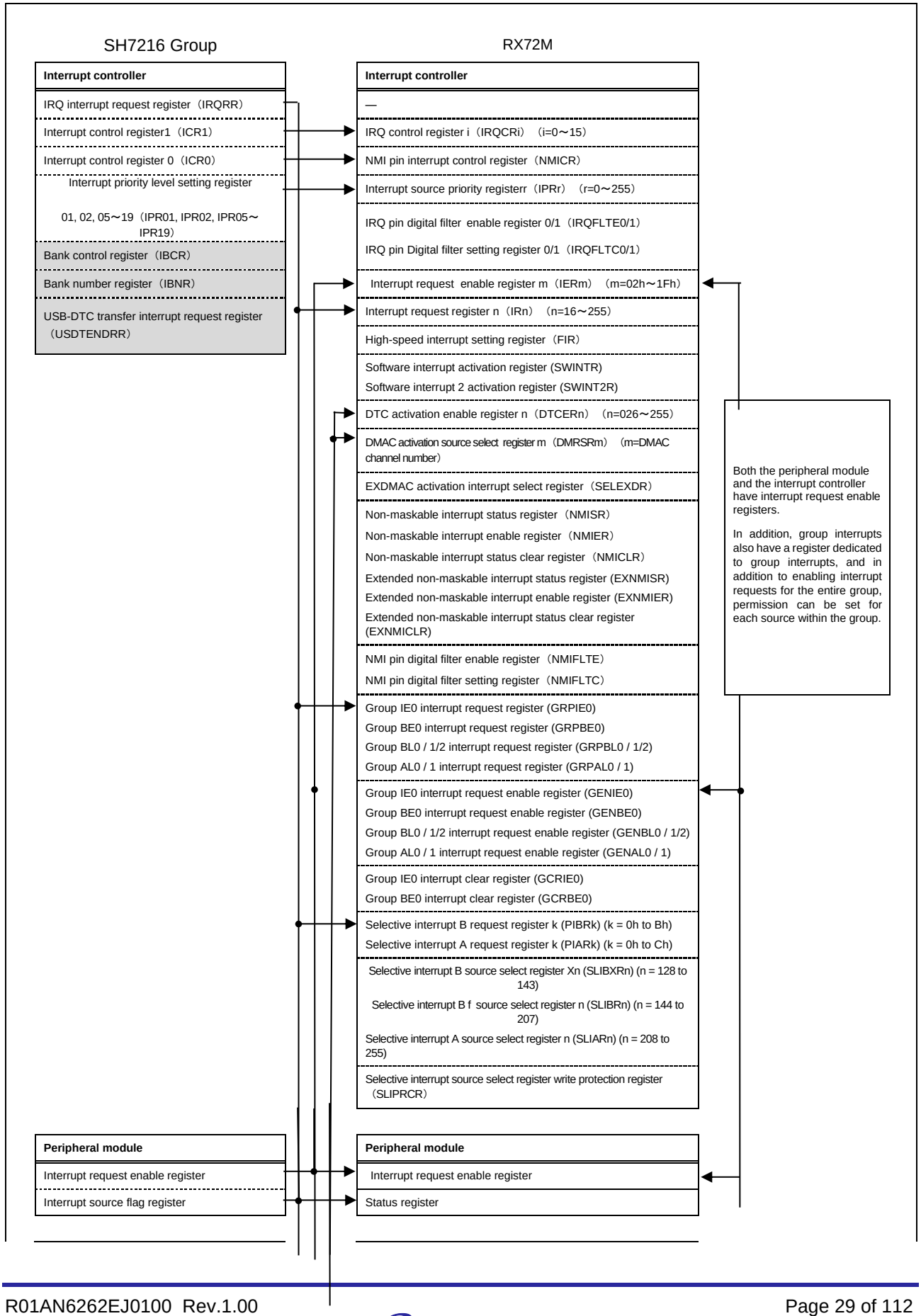
Table 1.14 lists the differences in the interrupt controller specifications.

Table 1.14 Comparison of SH7216 Group and RX72M Specifications (Interrupt Controller)

Item		SH7216 Group	RX72M
Interrupts	Peripheral function interrupts	• Interrupts from peripheral modules • Interrupt detection: Edge	• Interrupts from peripheral modules • Interrupt detection: Edge/level*1 • Group interrupt function • Selective interrupt B function • Selective interrupt A function
	External pin interrupts	• IRQ0 to IRQ7 pins • Sources: 8 • Interrupt detection: Low level, falling edge, rising edge, or both edges can be specified for each source.	• IRQ0 to IRQ15 pins • Sources: 16 • Interrupt detection: Low level, falling edge, rising edge, or both edges can be specified for each source. • Noise canceler function
	User break interrupt	• Supported	• Supported by the debugger function of the emulator
	H-UDI interrupt	• Supported	• Supported by the debugger function of the emulator
	Other sources	• Memory error interrupt	Memory error interrupt
	Noise cancellation	None	Digital filter settings are supported for the IRQi pins.
	Software interrupts	None	Supported
	Interrupt priority	A level from 0 to Fh can be specified for each source by a register setting.	A level from 0 to Fh can be specified for each source by a register setting.
	Fast interrupt function	None	Supported
	DTC/DMAC activation	DTC/DMAC activation supported*2	DTC/DMAC activation supported
	EXCMAC control	None	A software configurable interrupt can be used to start the EXDMAC.
Non-maskable interrupts	NMI pin interrupts	• Interrupt detection method (selection of falling or rising edge) • NMI input level read bit provided	• Interrupt detection method (selection of falling or rising edge) • Digital filter function
	Other sources (Other than exception handling)	None	• Interrupt at oscillation stop detection • WDT underflow or refresh error • IWDT underflow or refresh error • Voltage monitor 1 interrupt • Voltage monitor 2 interrupt • RAM error interrupt • Double precision floating point exception
Register banks		15 register banks	16 banks register banks

Note 1. The detection method is fixed for fixed-connection peripheral modules.
Note 2. On the SH7216 Group activation source setting is performed on the DTC or DMAC.

Figure 1.15 shows the points of difference between the interrupt controller of the SH7216 Group and the RX72M.



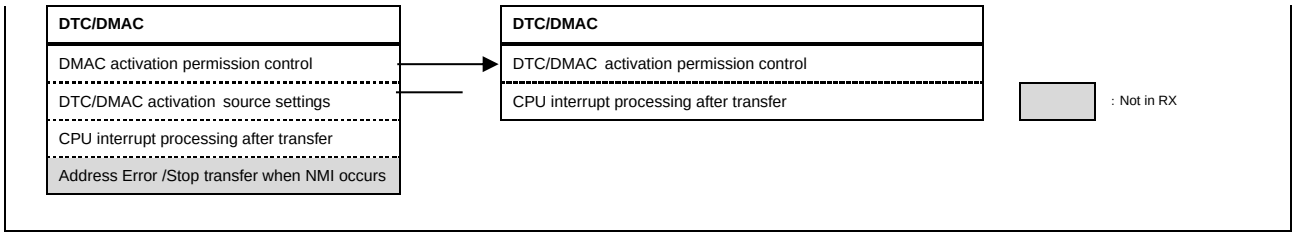


Figure 1.15 Differences Between Interrupt Controller Registers

The interrupt controller of the SH7216 Group controls IRQ interrupt flags, while peripheral module interrupt flags are controlled by the peripheral modules.

On the RX72M the interrupt controller controls all interrupt status flags, for both IRQs and peripheral modules.*1 In addition, the interrupt controller controls the activation source settings for the DTC and DMAC. The disable transfer at NMI occurrence function of the DTC and DMAC on the SH7216 Group is not implemented on the RX72M.

Note 1. The interrupt controller contains an interrupt request register for each interrupt source, but there are also interrupt enable bits implemented in the peripheral modules. (For details, see the User's Manual: Hardware.)

1.8.2 Interrupt Flag Management

When a peripheral module of the SH7216 Group generates an interrupt by edge detection, the corresponding interrupt source flag is cleared (the flag is cleared and a dummy read is performed) by the interrupt handler. This is done because the interrupt will be generated once again if the flag is not cleared by the handler.

On the RX72M the interrupt status flags are managed internally by the interrupt controller, and interrupt requests are sent to the CPU or DTC/DMAC. The interrupt controller has a function whereby, when edge detection is used, the corresponding interrupt status flag is cleared automatically when a response is received indicating acceptance of an interrupt. When level detection is used, both the request flag within the peripheral module and the corresponding interrupt status flag are cleared automatically. For details, see the User's Manual: Hardware.

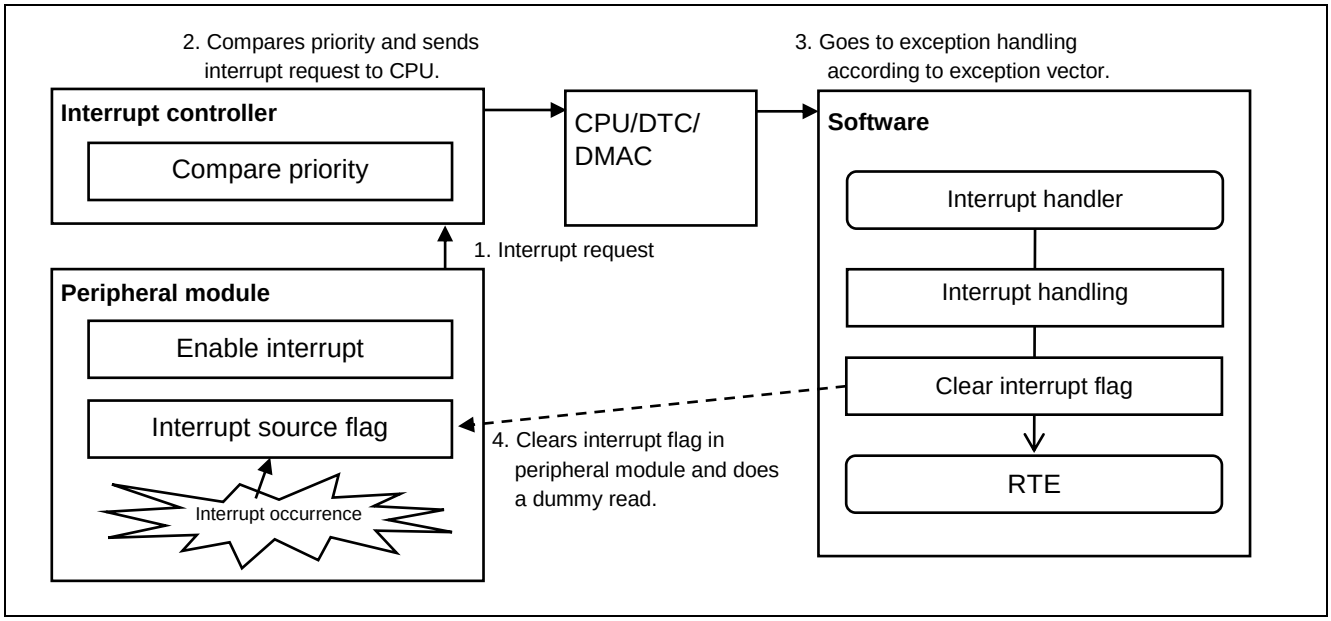


Figure 1.16 SH7216 Group Peripheral Module Interrupt (Edge Detection)

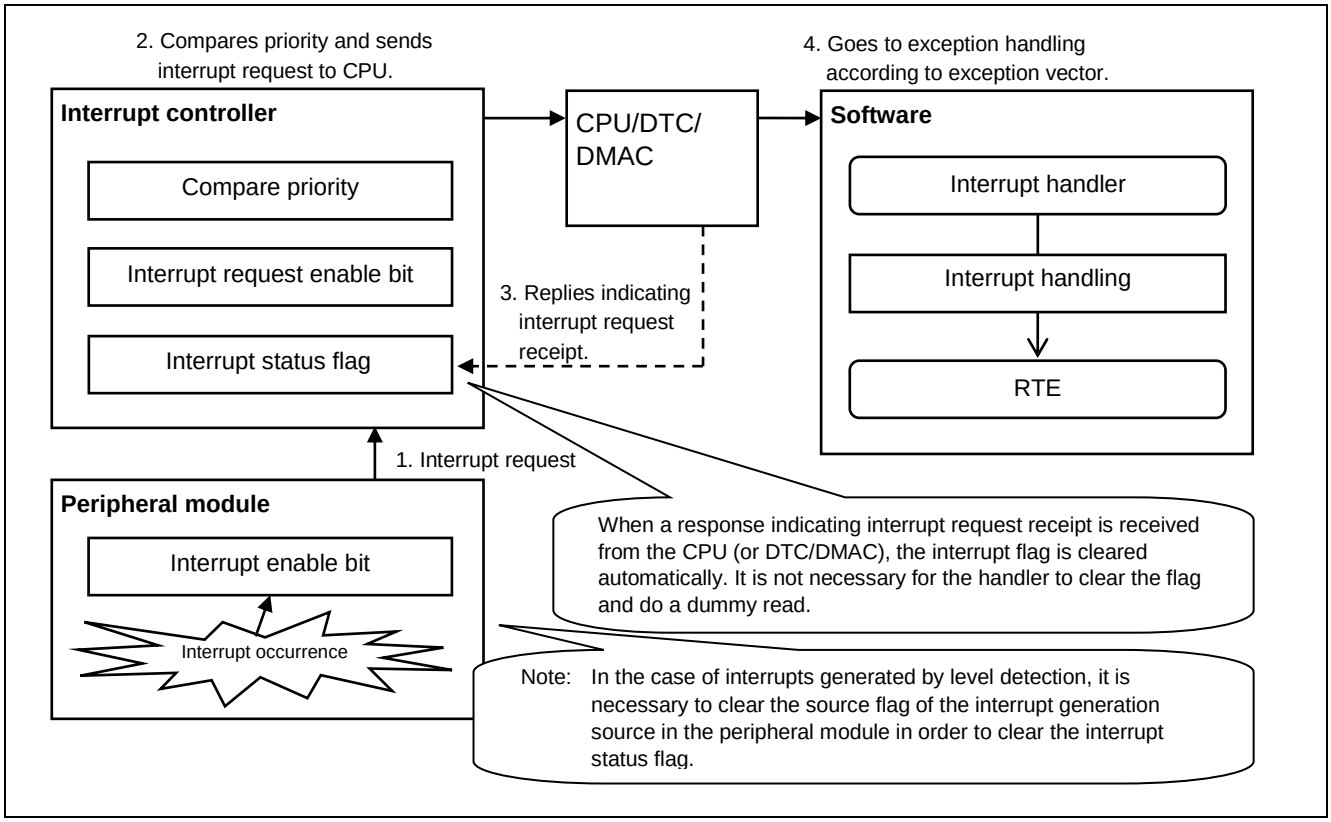


Figure 1.17 RX72M Peripheral Module Interrupt (Edge Detection)

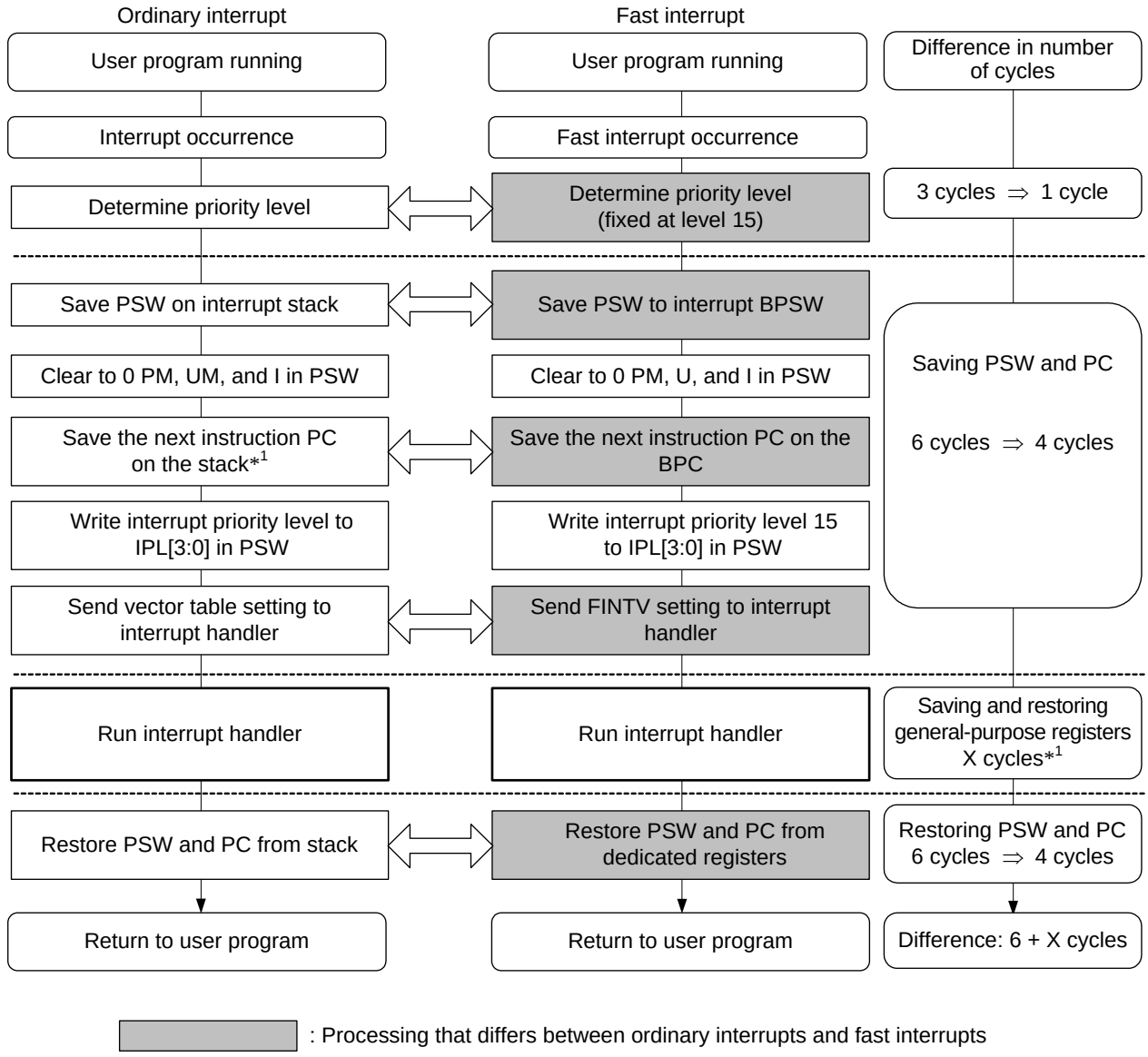
1.8.3 Fast Interrupt Control

In addition to ordinary interrupts, the RX72M supports fast interrupts.

Ordinary interrupt: After determining the interrupt priority it is necessary to save the contents of the control registers and general-purpose registers to the internal RAM or the external RAM by software.

Fast interrupt: Operation gives the interrupt the highest priority. When the interrupt occurs, the contents of the control registers are saved to dedicated registers, allowing interrupt activation to be realized faster than an ordinary interrupt.

It is possible to assign a portion of the general-purpose registers to exclusive use for interrupts by setting a compiler option. This eliminates the need to save and restore the contents of the general-purpose registers, further speeding up the interrupt.



Note 1. Fast interrupts have a single save register stage. Therefore, multistage fast interrupts are not possible. It is necessary to decide on a single function that will use fast interrupts.

Figure 1.18 Differences Between Ordinary Interrupts and Fast Interrupts on the RX72M

1.8.4 Digital filter

The RX72M has a digital filter function for the input signals to the IRQi pin and NMI pin. It is possible to set the sampling clock for digital filters, and the interrupt signal which is less than three times in the sampling clock base is not accepted as interrupts, so it is possible to improve the noise resistance performance.

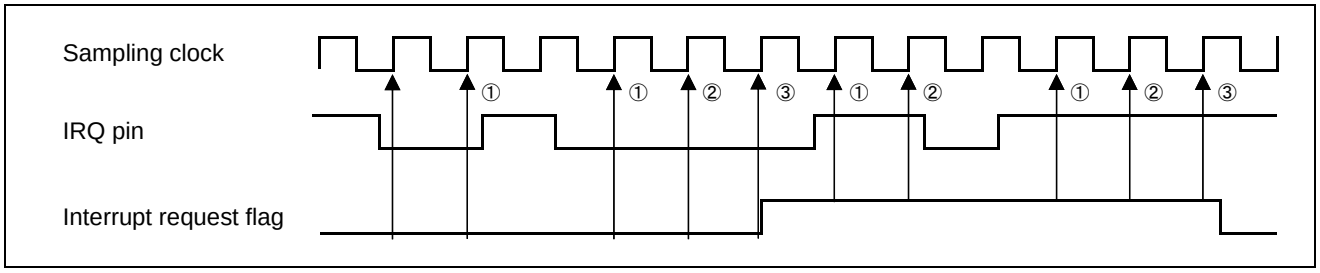


Figure 1.19 RX72M Digital Filter Operation Example

1.8.5 Multiple Interrupts

On the SH7216 Group if a high-priority interrupt occurs while a low-priority interrupt handler is running, the low-priority interrupt handler is suspended and the high-priority interrupt handler is executed. Once the high-priority interrupt handler finishes, the suspended low-priority interrupt handler is restarted.

On the RX72M if a high-priority interrupt occurs while a low-priority interrupt handler is running, the high-priority interrupt is not accepted until the low-priority interrupt handler finishes. This is because the PSW.I bit is cleared to 0 (interrupts are disabled) in a normal interrupt handler. In order to realize handling of multiple interrupts equivalent to that of the SH7216 Group, it is necessary to set the PSW.I bit to 1 (interrupts are enabled) in the interrupt handler.

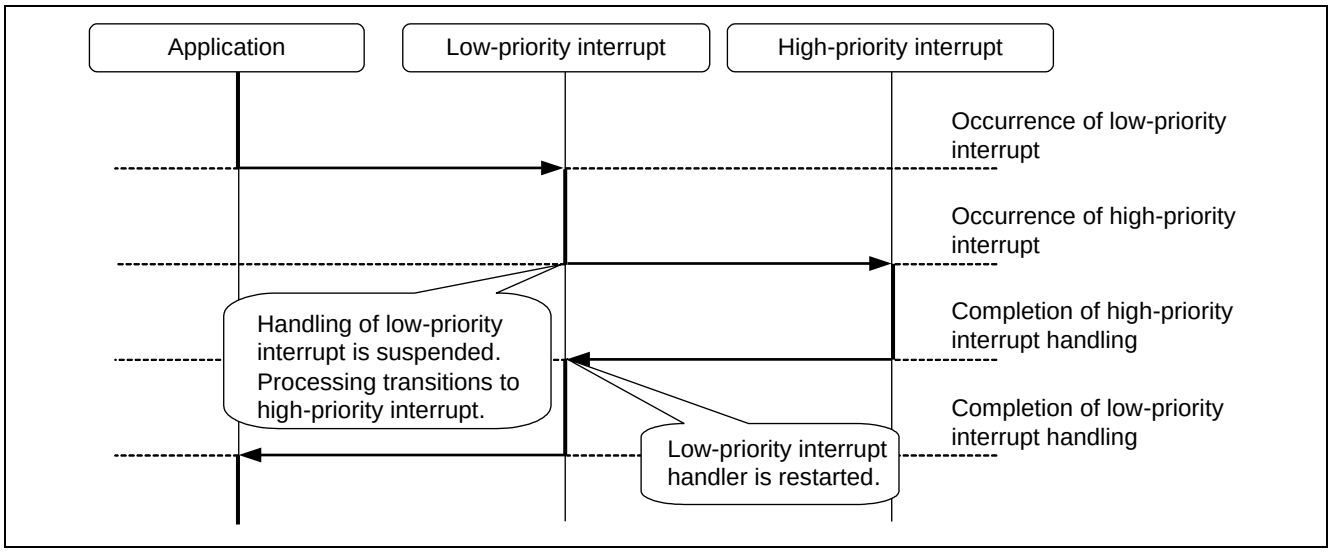


Figure 1.20 SH7216 Group Multiple Interrupt Sequence

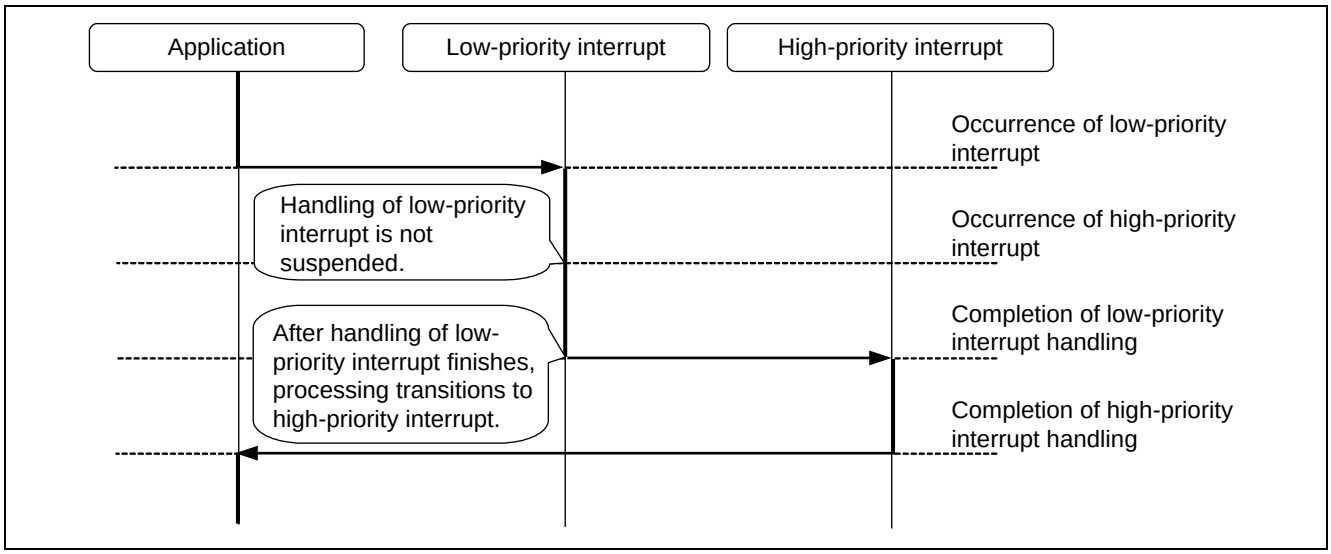


Figure 1.21 RX72M Interrupt Sequence (Not Controlled by PSW.I Bit)

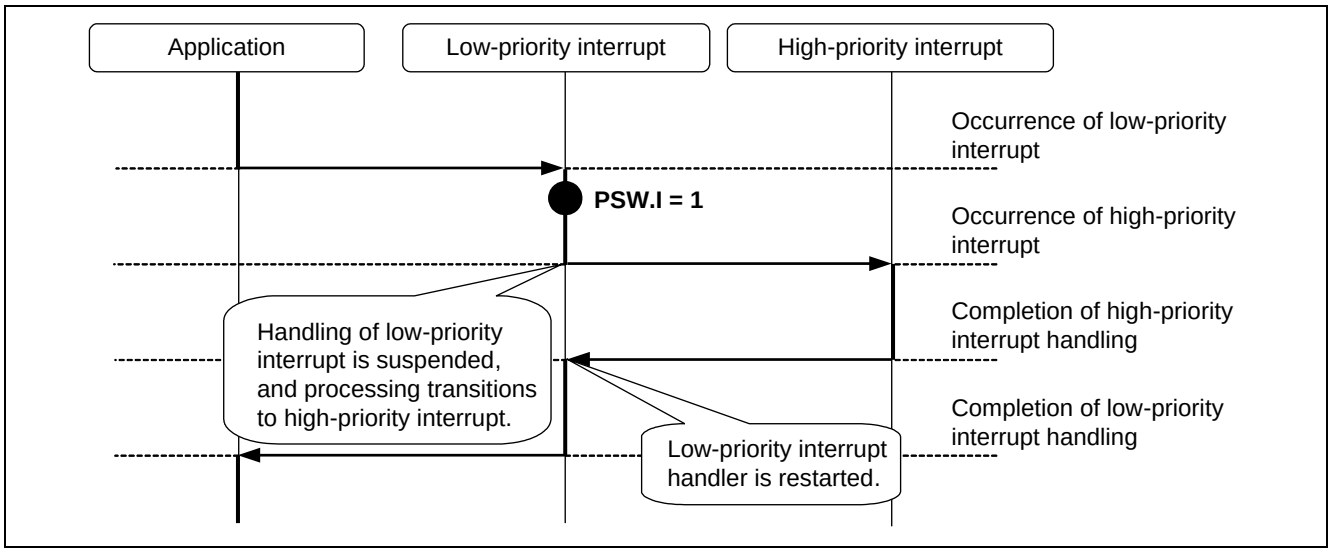


Figure 1.22 RX72M Interrupt Sequence (Controlled by PSW.I Bit)

1.8.6 Group Interrupts

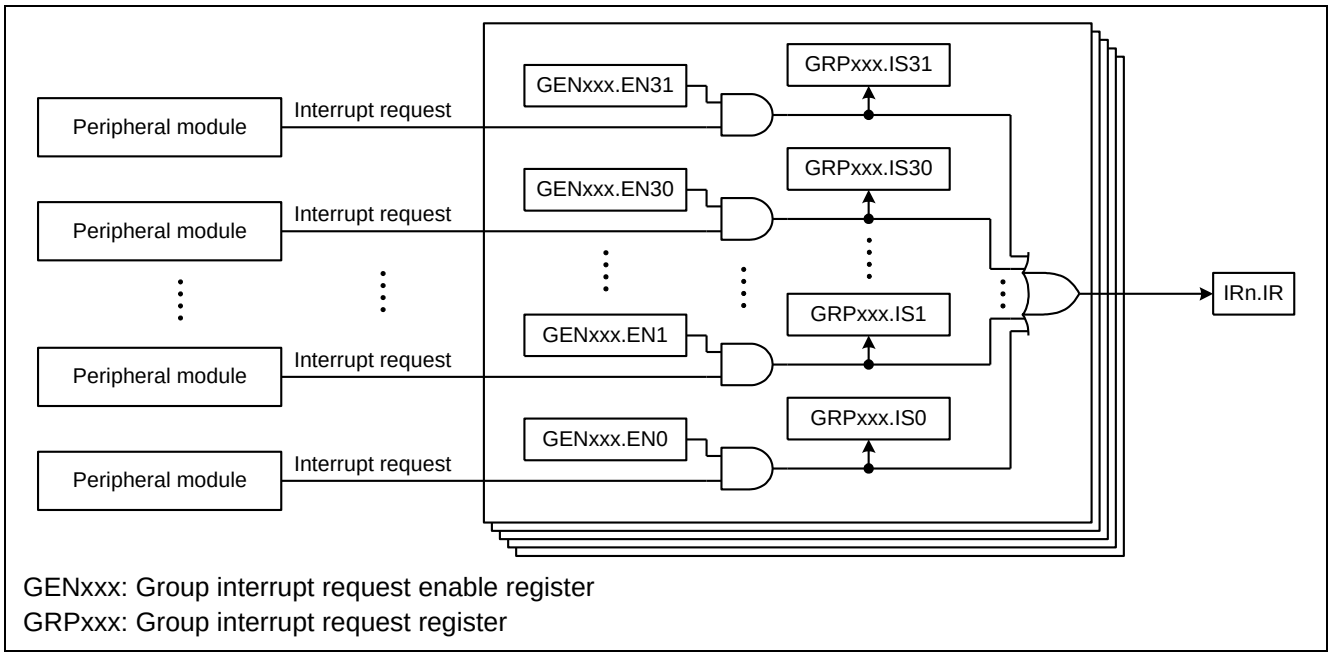
Group interrupts allow multiple interrupt sources to be assigned to a single vector. Group interrupt detection is by means of a logical OR operation on all the interrupt requests assigned to the group. This means that when an interrupt request is detected, it is necessary to identify the interrupt request from among those in the group by means of software.

Interrupt sources are assigned to different groups according to the operating clock of the peripheral module and the interrupt detection method.

The clearing condition for each group interrupt status flag differs according to the interrupt detection method. Table 1.15 lists the types of group interrupts and the clearing conditions of their status flags.

Table 1.15 RX72M Group Interrupt Types

Group	Peripheral Module Operating Clock	Interrupt Detection Method	Group Interrupt Status Flag
Group IE0	ICLK	Edge detection	Cleared automatically when 1 is written to the corresponding interrupt source clear bit (GCRIE0.CLR0 / GCRBE0.CLRn) of the interrupt controller.
Group BE0	PCLKB	Level detection	Cleared automatically when the peripheral module's interrupt status flag is cleared. Also cleared automatically when the interrupt controller's interrupt request enable bit (ENj in GENBL0, GENBL1,GENBL2 or GENAL0, GENAL1) is cleared to 0.
Group BL0			
Group BL1			
Group BL2			
Group AL0	PCLKA		
Group AL1			



GENxxx: Group interrupt request enable register
GRPxxx: Group interrupt request register

Figure 1.23 Group Interrupt Configuration on the RX72M

1.8.7 Software Configurable Interrupts

A single interrupt source among multiple peripheral modules can be selected for each software configurable interrupt, which is then assigned an interrupt vector number from 128 to 255.

Software configurable interrupts are classified into two types, A and B, according to the peripheral module operating clock. Table 1.16 lists the types of software configurable interrupts.

The software configurable interrupt status flags are not cleared automatically, but there is no effect on the generation of interrupt requests even if the corresponding flags are not cleared.

Table 1.16 Types of Software Configurable Interrupts on the RX72M

Software Configurable Interrupt Name	Peripheral Module Operating Clock	Interrupt Detection Method	Software Configurable Interrupt Status Flag
Software Configurable Interrupt A	PCLKA	Edge detection	Not cleared automatically, but there is no effect on interrupt request generation even if the flag is not cleared.
Software Configurable Interrupt B	PCLKB		

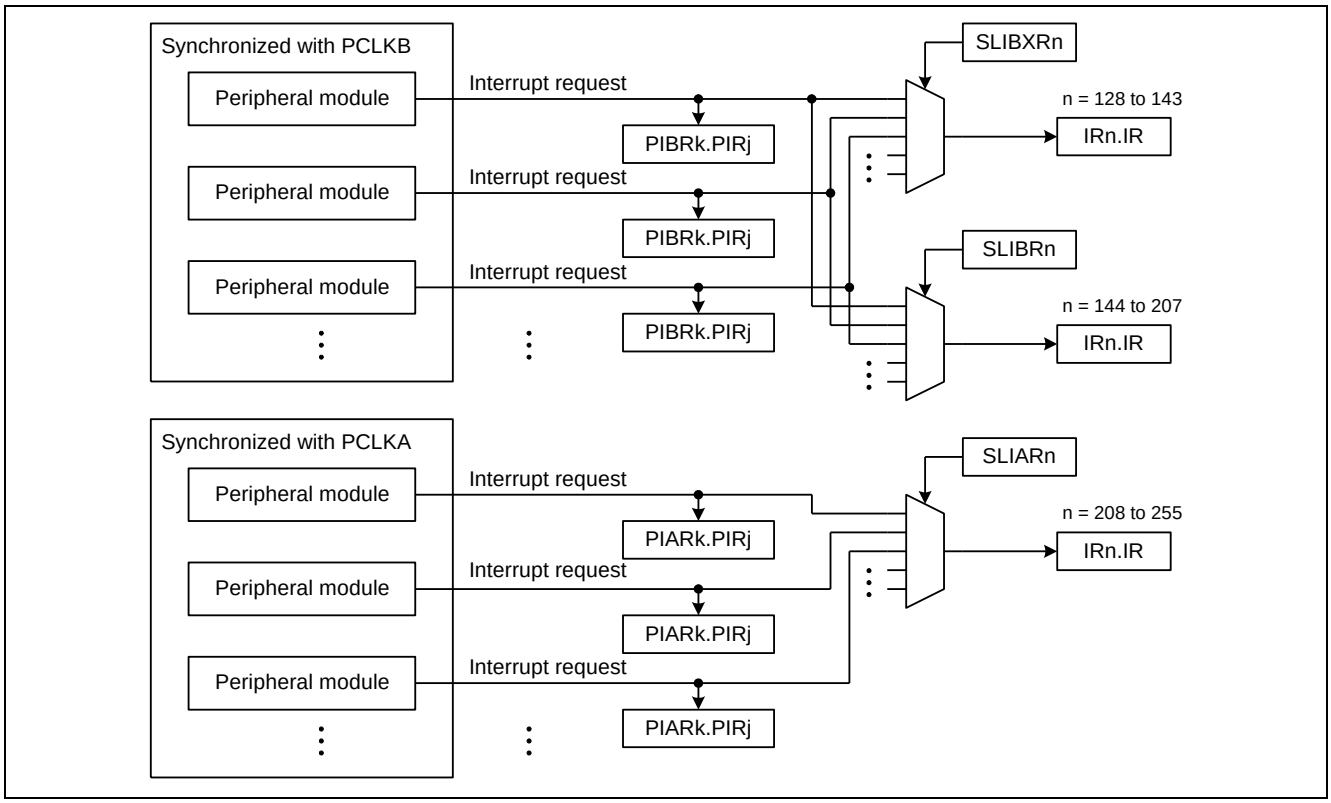


Figure 1.24 Software Configurable Interrupt Configuration on the RX72M

2. On-Chip Functions

2.1 List of On-Chip Functions

Table 2.1 lists the on-chip functions of the SH7216 Group and RX72M.

For details on the functions of the RX72M only, refer to the User's Manual: Hardware.

Table 2.1 On-Chip Functions

SH7216 Group	RX72M
Clock pulse generator (CPG)	Clock generation circuit
Interrupt controller (INTC)	Interrupt controller （ICUD）
User break controller (UBC)	It can be supported by the debugger function of the emulator.
Data transfer controller (DTC)	Data transfer controller (DTCb)
Bus state controller (BSC)	Bus
Direct memory access controller (DMAC)	DMA controller (DMACAa) EXDMA controller (EXDMACa)
Multi-function timer pulse unit 2 (MTU2) Multi-function timer pulse unit 2S (MTU2S)	Multi-function timer pulse unit 3 (MTU3a)
Port output enable (POE2)	Port output enable 3 (POE3a)
Watchdog timer (WDT)	Watchdog timer (WDTA) Independent watchdog timer (IWDTa)
Serial communication interface (SCI) Serial communication interface with FIFO (SCIF)	Serial communication interface (SCIj, SCIi, SCIh)
Renesas serial peripheral interface (RSPI)	Serial peripheral interface (RSPIc)
I^2C bus interface 3 (IIC3)	I^2C bus interface (RIICa)
A/D converter (ADC)	12-bit A/D converter (S12ADFa)
Controller area network (RCAN-ET)	CAN module (CAN)
USB function module (USB)	USB 2.0 FS host/function module (USBb)
Ethernet controller (EtherC)	Ethernet controller (ETHERC)
Ethernet controller direct memory access controller (E-DMAC)	DMA controller for the Ethernet controller (EDMACa)
Compare match timer (CMT)	Compare match timer (CMT) Compare match timer W (CMTW)
Pin function controller (PFC)	Multi-function pin function controller (MPC)
I/O port	I/O port
Flash memory Data flash	Flash memory*1
On-chip RAM (max. 128 KB)	RAM (max. 512 KB, 32 KB) Standby RAM (max. 8 KB)
Power-down mode	Low power consumption function
User debugging interface (H-UDI)	It can be supported by the debugger function of the emulator.

SH7216 Group	RX72M
User debugging interface (H-UDI)	Voltage detection circuit (LVDA) Clock frequency accuracy measurement circuit (CAC) Battery backup function Register write protection function Memory-protection unit (MPU) Event link controller (ELC) General PWM timer (GPTW) Port output enable for GPTW (POEG) 16-bit timer pulse unit (TPUa) Programmable pulse generator (PPG) 8-bit timer (TMRb) Realtime clock (RTCd) PTP module for the Ethernet controller (EPTPCb) PHY management interface (PMGI) EtherCAT slave controller (ESC) Quad serial peripheral interface (QSPI) CRC calculator (CRCA) Extended serial sound interface (SSIE) SD host interface (SDHI) MultiMediaCard interface (MMCIF) Parallel data capture unit (PDC) Graphic LCD controller (GLCDC) 2D drawing engine (DRW2D) Boundary scan Trigonometric arithmetic calculator (TFU) Trusted Secure IP (TSIP) ΔΣ Modulator interface (DSMIF) 12-bit D/A converter (R12DAa) Temperature sensor (TEMPS) Data operation circuit (DOC) Standby RAM

Note 1. The RX72M flash memory includes data flash memory in addition to code flash memory.

2.2 I/O Ports/ Multifunction pin controller (MPC)

2.2.1 Number of I/O Ports

Table 2.2 lists the number of I/O ports on the SH7216 Group and RX72M.

Table 2.2 Number of I/O Ports

Item	Package	Port Function
Number of I/O ports on SH7216 Group	PLQP0176KB-A PLQP0176LB-A PLBG0176GA-A	I/O: 100 Input: 10 Total: 110 Pull-up resistor: 100
Number of I/O ports on RX72M	PLBG0224GA-A	I/O: 182 Input: 1 Pull-up resistor: 182 Open-drain output: 182 5 V tolerant: 19
	PLBG0176GA-A PLQP0176KB-C	I/O: 136 Input: 1 Pull-up resistor: 136 Open-drain output: 136 5 V tolerant: 19
	PLQP0144KA-B	I/O: 111 Input: 1 Pull-up resistor: 111 Open-drain output: 111 5 V tolerant: 17
	PLQP0100KB-B	I/O: 72 Input: 1 Pull-up resistor: 72 Open-drain output: 72 5 V tolerant: 12

2.2.2 I/O Settings

Both the SH7216 Group and RX72M have multiplexed pins. Therefore, it is necessary to make pin settings to assign each pin to either general I/O or an on-chip module function.

On the SH7216 Group port functions are determined by settings made to the pin function controller (PFC). The I/O ports are configured as ports A to F.

The SH7216 Group's I/O port register settings are shown in Figure 2.1, the I/O port register configuration in Table 2.3, and the pin function controller (PFC) register configuration in Table 2.4.

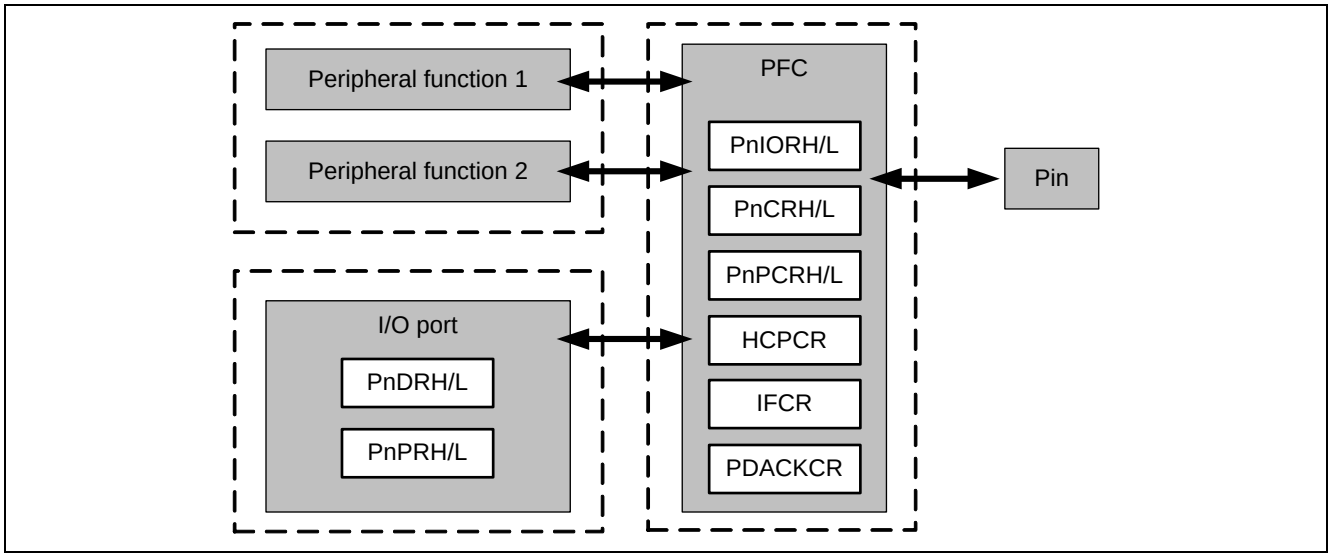


Figure 2.1 SH7216 Group I/O Settings

Table 2.3 SH7216 Group Register Configuration (I/O Ports)

Register	Function Name	Function
PnDRH	Port n data register H	Port n data registers
PnDRL	Port n data register L	Pin function is general output: Stores pin output data. Pin function is general input: Reflects pin states.
PnPRH	Port n port register H	Port n data read-only registers
PnPRL	Port n port register L	They reflect pin states.

n: Port name (n = A to F)

Table 2.4 SH7216 Group Register Configuration (PFC)

Register	Function Name	Function
PnIORH	Port n IO register H	Pin input/output direction selection
PnIORL	Port n IO register L	
PnCRHm	Port n control register Hm	Multiplexed pin function selection
PnCRLm	Port n control register Lm	
PnPCRH	Port n pull-up MOS control register H	Selects the input pull-up MOS setting.
PnPCRL	Port n pull-up MOS control register L	
HCPCR	High-current port control register	Sets the state of high-current ports.
IFCR	IRQOUT function control register	Sets the state of IRQ output pin.
PDACKCR	DACK output timing control register	Sets the DACK pin output timing.

n: Port name (n = A to E)

m: Setting number (m = 1 to 4)

On the RX72M port functions are specified by making settings to the multi-function pin controller (MPC). The I/O ports are configured as ports 0 to 9, A to G, and J.

The following types of I/O port settings are supported on the RX72M.

- Open drain control register: Port output format selection
  CMOS output, N-channel open-drain output, or P-channel open-drain output
- Pull-up control register: Input pull-up resistor on/off selection
- Drive capacity control register: Selection between normal drive output and high drive output
- 5 V tolerant input ports are provided.

Because it is a multiplex terminal like SH7216, the Pin function settings must be determined using the I / O ports and the Multifunctional Pin Controller (MPC).

The RX72M's I/O settings are shown in Figure 2.2.

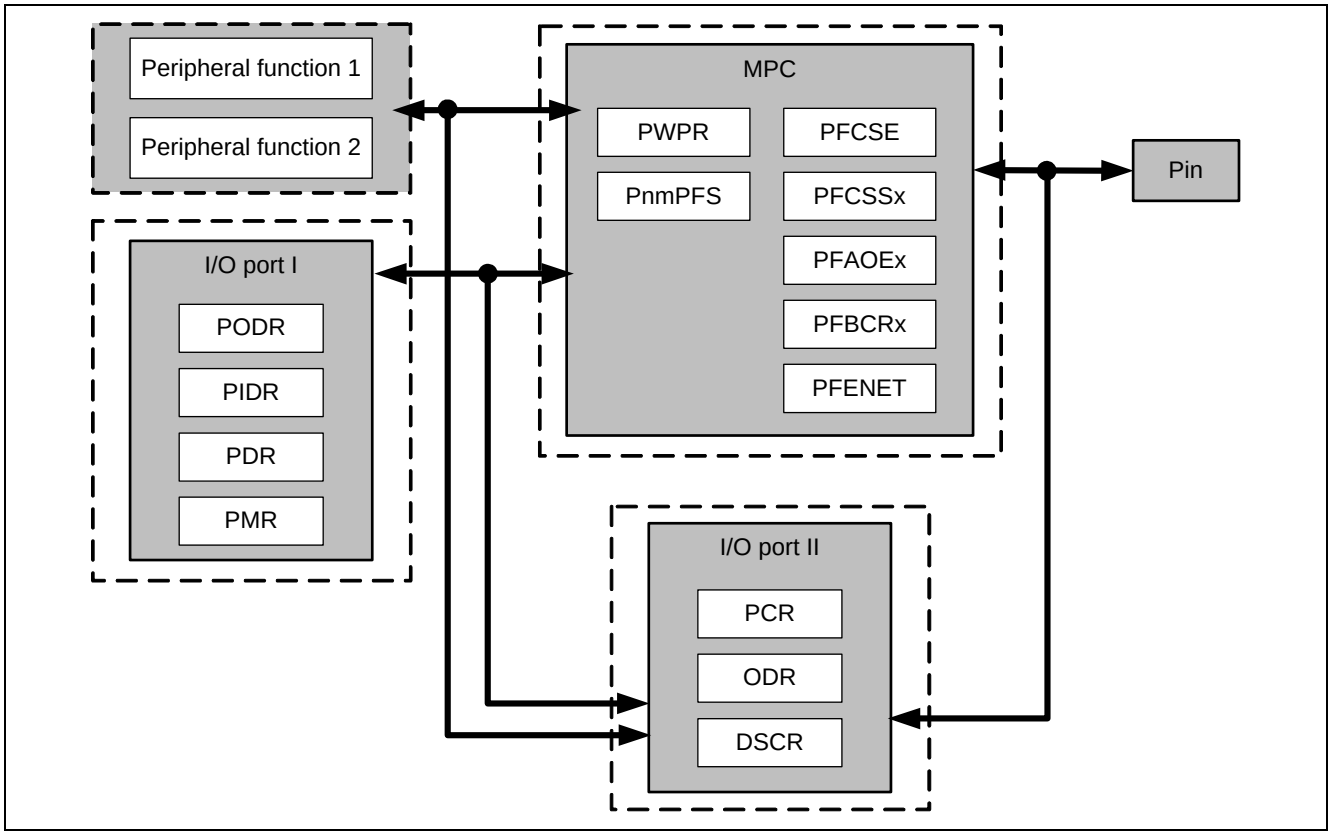


Figure 2.2 I/O Settings on the RX72M

To use a pin as a general I/O pin it is sufficient to make a setting (PMR, PDR, ODR0 / 1, PCR, DSCR settings) in the appropriate I/O port register. Figure 2.3 shows the initialization sequence for using pins as general I/O pins on the RX72M.

The pin function control registers (PnmPFS) of the MPC are used to assign peripheral functions to pins. For setting examples when using peripheral functions that include general I/O, refer to the individual chapters for each of the peripheral functions. Figure 2.4 shows the initialization sequence for assigning pins to peripheral functions on the RX72M.

Table 2.5 RX72M Register Configuration (I/O Ports)

Register	Function Name	Function
PDR	Port direction register	Specifies input or output for pins selected as general I/O ports.
PODR	Port output register	Stores pin output data for general output ports.
PIDR	Port input register	Reflects port pin states.
PMR	Port mode register	Used for port pin function settings. Specifies whether each pin is used as a general I/O port or for a peripheral function.
ODR0	Open drain control register 0	Selects the port output format from among the following: • CMOS output • N-channel open drain • P-channel open drain
ODR1	Open drain control register 1	Selects the port output format from among the following: • CMOS output • N-channel open drain
PCR	Pull-up control register	Turns the port input pull-up resistor on or off.
DSCR	Drive capacity control register	Specifies the drive capacity. • Normal drive output • High drive output
DSCR2	Drive capacity control register2	Normal/ High drive output High drive output for high speed interface

Table 2.6 RX72M Register Configuration (MPC)

Register	Function Name	Function
PWPR	Write-protect register	Write-protect function for PnmPFS register
PnmPFS	Pnm pin function control register	Selects functions of multiplexed pins.
PFCSE	CS output enable register	Disables or enables output on CSn# (n: 0 to 7).
PFCSS0	CS output pin select register 0	Selects output pins for CS0 to CS3.
PFCSS1	CS output pin select register 1	Selects output pins for CS4 to CS7.
PFAOE0	Address output enable register 0	Settings when using pins for address bus
PFAOE1	Address output enable register 1	Settings when using pins for address bus
PFBCR0	External bus control register 0	Settings when using pins for external bus
PFBCR1	External bus control register 1	Settings when using pins for external bus
PFBCR2	External bus control register 2	Settings when using pins for external bus
PFBCR3	External bus control register 3	Settings when using pins for external bus
PFENET	Ethernet control register	Settings when using Ethernet PHY mode

n: Port name (n = 0 to 9, A to G, H,J,K to N, Q)
m: Pin number (m = 0 to 7)

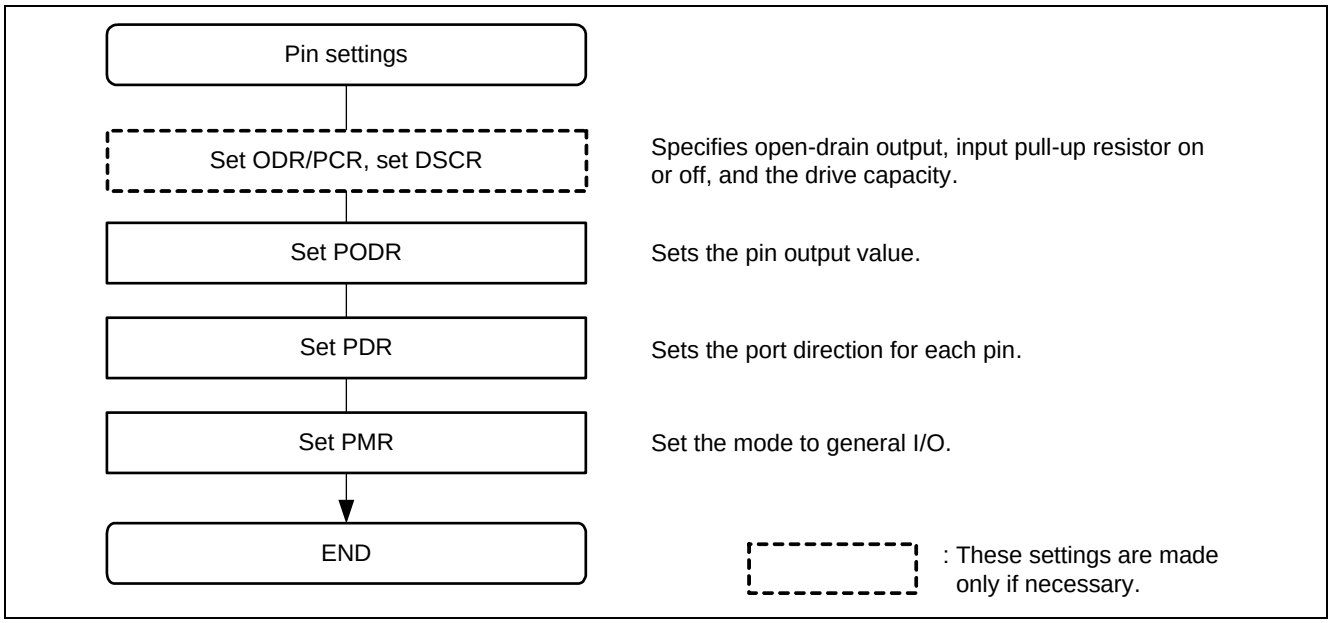
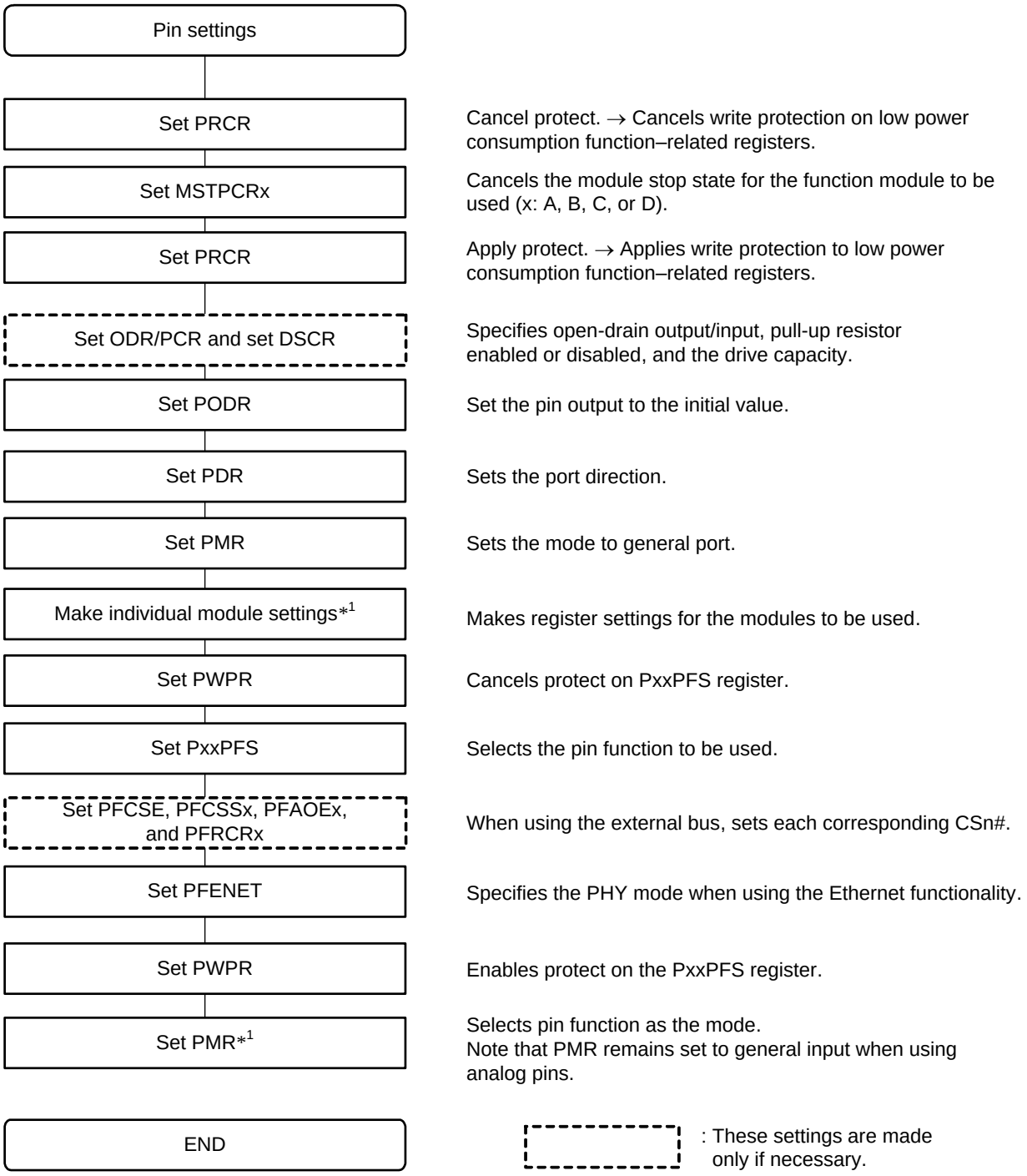


Figure 2.3 RX72M Pin General I/O Setting Flowchart



Note: For details on the MPC settings used to assign functions to pins, see the section describing the specific peripheral function.

Note 1. The order of PMR settings and module settings differs according to the module.

Figure 2.4 RX72M Pin Peripheral Function Setting Flowchart

2.3 Buses

2.3.1 Comparison of Specifications

The SH7216 Group incorporates a BSC that provides bus state controller functionality.

Table 2.7 is a comparative listing of the specifications of the SH7216 Group and RX72M.

Table 2.7 Comparison of SH7216 Group and RX72M Specifications (Bus)

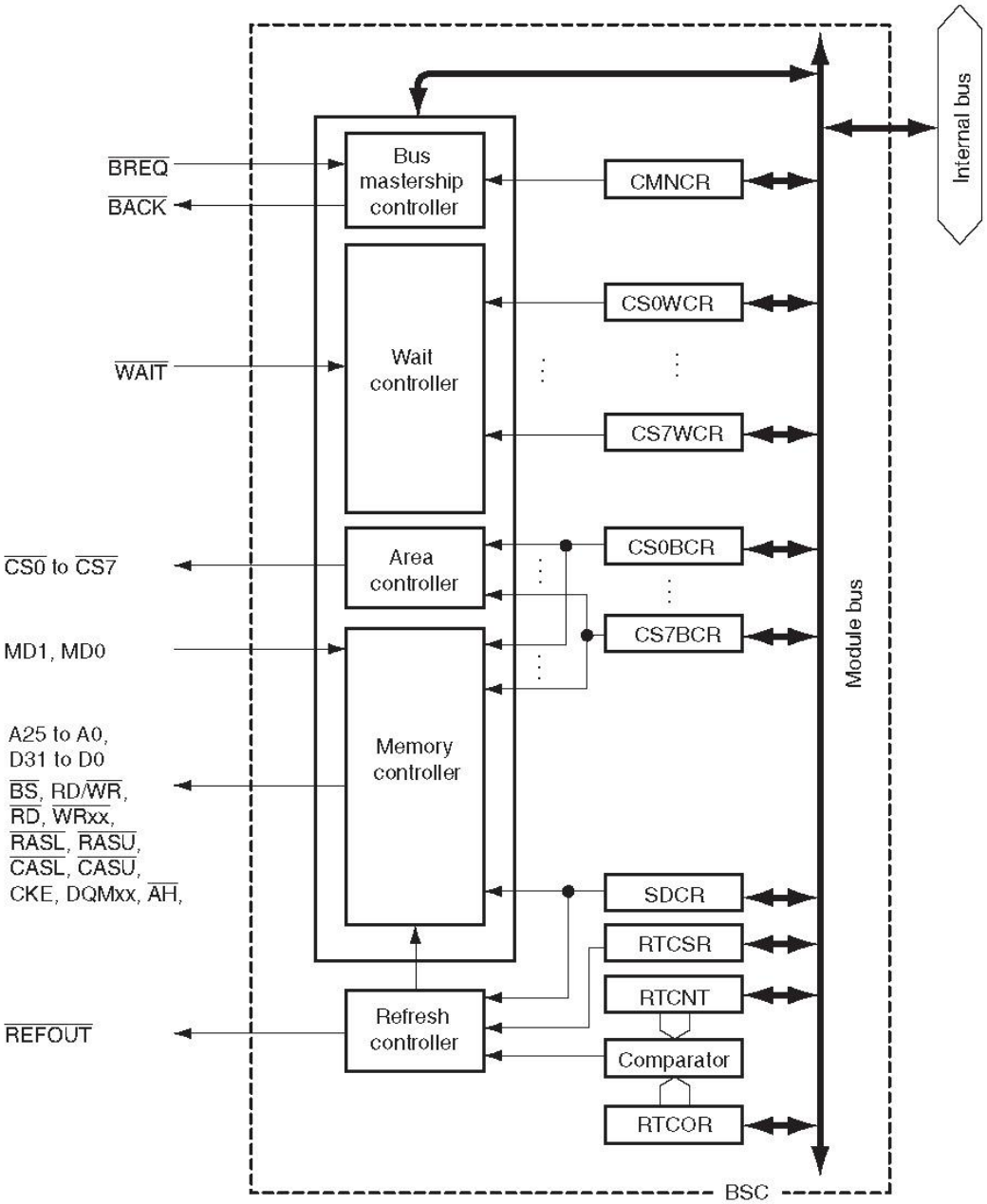
Item	SH7216 Group (BSC)	RX72M
External bus address space	• External address space designated as areas CS0 to CS7 (max. 64 MB each) Ability to select SDRAM for up to two CS areas (max. 64 MB)	• External address space designated as areas CS0 to CS7 (16 MB each) • Independent SDRAM space (max. 128 MB)
Bus width	Ability to select the data bus width (8, 16, or 32 bits) for each area	Ability to select the data bus width (8, 16, or 32 bits) for each area
Endianness	Area 0: Fixed big-endian Areas 1 to 7: Endian setting selectable independently by area	Endian setting by area*1
Bus arbitration	• CPU bus and external bus have fixed priority. • Ability to output bus enable (BACK) after receiving a bus request (BREQ) from an external device.	• Fixed or toggled priority — Memory bus — Internal peripheral bus — External bus • Fixed priority — CPU bus — Internal main bus
Interrupt Request occurrence	• The refresh counter can be used as an interval timer	• Can be supported by timers such as MTU3
External bus arbitration	• Supported	• Not supported
Other	• CS area — Access wait control — CSn assert duration extension — MPX I/O interface (address data multiplexed) — Support for SRAM with byte selection — Burst ROM (synchronous/asynchronous) support • SDRAM area — Auto refresh and self-refresh — CAS latency setting	• CS area — Ability to insert recovery cycles — Cycle wait function — CSn# signal timing control — RD# and WR# signal control timing — Write access mode — Ability to access address and data multiplexed I/O devices • SDRAM area — Multiplexed output of row and column addresses — Auto refresh and self-refresh — CAS latency setting • Write buffer — Write buffer function

Note 1. Refer to 1.2.2, Endian Setting for information on endian settings.

2.3.2 Bus Block Diagrams

Comparative bus block diagrams of the SH7216 Group and RX72M are presented below.

Figure 2.5 is a block diagram of the BSC of the SH7216 Group, and Figure 2.6 is a bus block diagram of the RX72M.



[Legend]
CMNCR: Common control register
CSnWCR: CSn space wait control register (n = 0 to 7)
CSnBCR: CSn space bus control register (n = 0 to 7)
SDCR: SDRAM control register
RTCSR: Refresh timer control/status register
RTCNT: Refresh timer counter
RTCOR: Refresh time constant register

Figure 2.5 SH7216 Group Bus Block Diagram

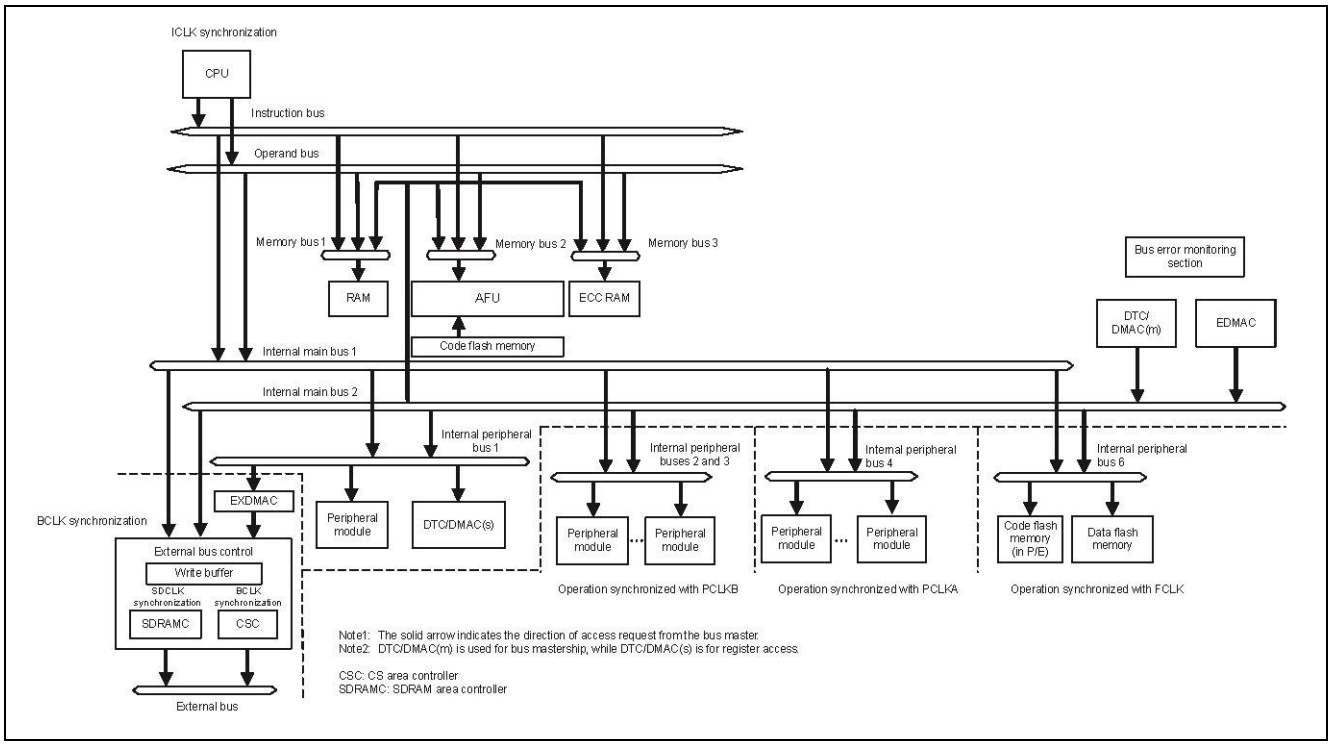


Figure 2.6 RX72M Bus Block Diagram

Table 2.8 shows the bus types on the RX72M. The RX72M has a different bus architecture than the SH7216 Group, and the memory buses, internal buses, and peripheral buses each have multiple stages. This enables parallel operation by the CPU and DMAC, DTC, or EDMAC and between the modules on the peripheral buses, thereby speeding up operation overall.

Table 2.8 RX72M Buses

Bus	Connected Modules, etc.	Clock
CPU buses (instruction bus and operand bus)	Instruction bus: CPU, on-chip memory Operand bus: CPU, on-chip memory(RAM, Extended RAM, ECCRAM, Code flash memory)	ICLK
Memory bus 1	On-chip RAM	ICLK
Memory bus 2	Code flash memory	ICLK
Memory bus 3	Extended RAM, ECCRAM	ICLK
Internal main bus 1	CPU	ICLK
Internal main bus 2	DTC, DMAC, EDMAC, on-chip memory (RAM, Extended RAM, ECCRAM, Code flash memory)	ICLK
Internal peripheral bus 1	Peripheral functions (DTC, DMAC, EXDMAC, interrupt controller, bus error monitoring block)	ICLK (EXDMAC: BCLK)
Internal peripheral bus 2	Peripheral functions (peripheral functions other than those connected to peripheral buses 1, 3, 4, and 5)	PCLKB
Internal peripheral bus 3	Peripheral functions (USB, DSMIF,PDC, standby RAM)	PCLKB
Internal peripheral bus 4	Peripheral functions（EDMAC、ETHERC、PMGI、EPTPC、MTU3、GPTW、SCI、RSPI）	PCLKA
Internal peripheral bus 5	Peripheral functions (GLCDC, DRW2D, ESC)	PLCKA
Internal peripheral bus 6	Code flash memory (P/E), data flash memory	FCLK
External buses (CS areas)	External devices	BCLK
External buses (SDRAM)	SDRAM	SDCLK

ICLK: System clock PCLKA, PCLKB: Peripheral module clock
FCLK: Flash IF clock BCLK: External bus clock SDCLK: SDRAM clock

2.4 Data Transfer Controller (DTCb)

2.4.1 Comparison of Specifications

Data transfer controller functionality is provided on the SH7216 Group by the DTC and on the RX72M by the DTCb.

On both the SH7216 Group and RX72M transfer information is located in the RAM and specified by means of DTC vectors. The basic operation of the three transfer modes (normal transfer mode, repeat transfer mode, and block transfer mode) is identical on the two platforms. Table 2.9 is a comparative listing of the specifications of the SH7216 Group and RX72M.

Table 2.9 Comparison of SH7216 Group and RX72M Specifications (DTC)

Item	SH7216 Group (DTC)	RX72M (DTCb)
Transfer modes	• Normal transfer mode • Repeat transfer mode • Block transfer mode	
Activation sources	• External interrupt • Peripheral function interrupt	• External interrupt • Peripheral function interrupt • Software interrupt
Activation enable/ disable control	Activated by DTC enable register of DTC module.	Activated by DTC activation enable register of interrupt controller.
Transfer spaces	Transfer between the following spaces is possible: • On-chip memory space • On-chip peripheral module space (excluding DMAC, DTC, BSC, UBC, and FLASH) • External memory space • Memory-mapped external device space At a minimum, the on-chip peripheral module space must be specified as either the transfer source or transfer destination.	Transfer between the following spaces is possible: • On-chip memory space • On-chip peripheral module space • External memory space
Transfer units	• Normal transfer mode: Selectable among 8, 16, and 32 bits • Repeat transfer mode: Selectable among 8, 16, and 32 bits • Block transfer mode: Selectable within range from 8 bits to 256 longwords	
Transfer counts	• Normal transfer mode: 1 to 65,536 • Repeat transfer mode: 1 to 256 times (repeat after completion of specified transfer count) • Block transfer mode: 1 to 65,536	
CPU interrupt requests	• An interrupt generated by a CPU interrupt request may be used as the DTC activation source. • A CPU interrupt at single data unit transfer-end may be used. • A CPU interrupt after transfer of a specified number of data units may be used.	
Method	Control information is allocated for each interrupt source by using DTC vectors.	
Other	• Chain transfer • Transition to module-stop state • The following functions can be used to high-speed transmission and reduce memory usage: — Transfer information read skipping — Write-back skipping — Short-address mode — Bus mastership release timing setting	• Chain transfer • Transition to module-stop state • The following functions can be used to high-speed transmission and reduce memory usage: — Transfer information read skipping — Write-back skipping — Sequence transfer — Event link — Writeback disable — Displacement addition

2.4.2 Register Comparison

On the SH7216 Group operation of the DTC is enabled by canceling the module-stop state for the DTC. On the RX72M, in addition to canceling the module-stop state for the DTC, it is necessary to make a setting in the DTC module start register (DTCST) to enable DTC operation.

Table 2.10 provides a comparative listing of the registers of the SH7216 Group and the RX72M.

Guide to Symbols in "Changes" Column of Table

◎: Register with same bit assignments on SH7216 Group and RX72M

△: Register with different bit assignments on SH7216 Group and RX72M

—: Register not present on SH7216 Group or RX72M

Table 2.10 SH7216 Group and RX72M Register Comparison (DTC)

SH7216 Group (DTC)	RX72M (DTCa)	Changes
DTC mode register A (MRA)	DTC mode register A (MRA)	◎
DTC mode register B (MRB)	DTC mode register B (MRB)	◎
—	DTC mode register C (MRC)	
DTC source address register (SAR)	DTC transfer source register (SAR)	◎
DTC destination address register (DAR)	DTC transfer destination register (DAR)	◎
DTC transfer count register A (CRA)	DTC transfer count register A (CRA)	◎
DTC transfer count register B (CRB)	DTC transfer count register B (CRB)	◎
DTC control register (DTCCR)	DTC control register (DTCCR)	△
DTC vector base register (DTCVBR)	DTC vector base register (DTCVBR)	◎
Bus function extending register (BSCEHR) DTC short address mode (DTSA bit)	DTC address mode register (DTCADMOD)	△
DTC enable registers A to E (DTCERA to DTCERE)*1	—	—
—	DTC module start register (DTCST)	—
	DTC status register (DTCSTS)	
	DTC index table base register (DTCIBR)	—
	DTC operation register (DTCOR)	—
	DTC sequence transfer permission register (DTCSQE)	—
	DTC address displacement register (DTCDISP)	—

Note 1. On the RX72M transfer request settings from peripheral modules are made by means of the interrupt controller.

2.4.3 Activation Source Settings

On the SH7216 Group peripheral modules can activate the DTC by making settings in activation source DTC enable registers A to E (DTCERA to DTCERE) of the DTC module. On the RX72M DTC activation sources are specified by means of settings to DTC transfer request enable register n (DTCERn) of the interrupt controller. This allows specific interrupts to be enabled as activation sources for enabling the DTC.

2.4.4 DTC Vector Configuration

The DTC vector configuration of the SH7216 Group and RX72M is shown below.

On the SH7216 Group the upper 20 bits of the start address of the DTC vector table are the DTC vector base address (DTCVBR) and the lower 12 bits are calculated as “400h + vector number × 4”. The base address of the DTC vector table is aligned with a 4 KB boundary such that the lower 12 bits are 0.

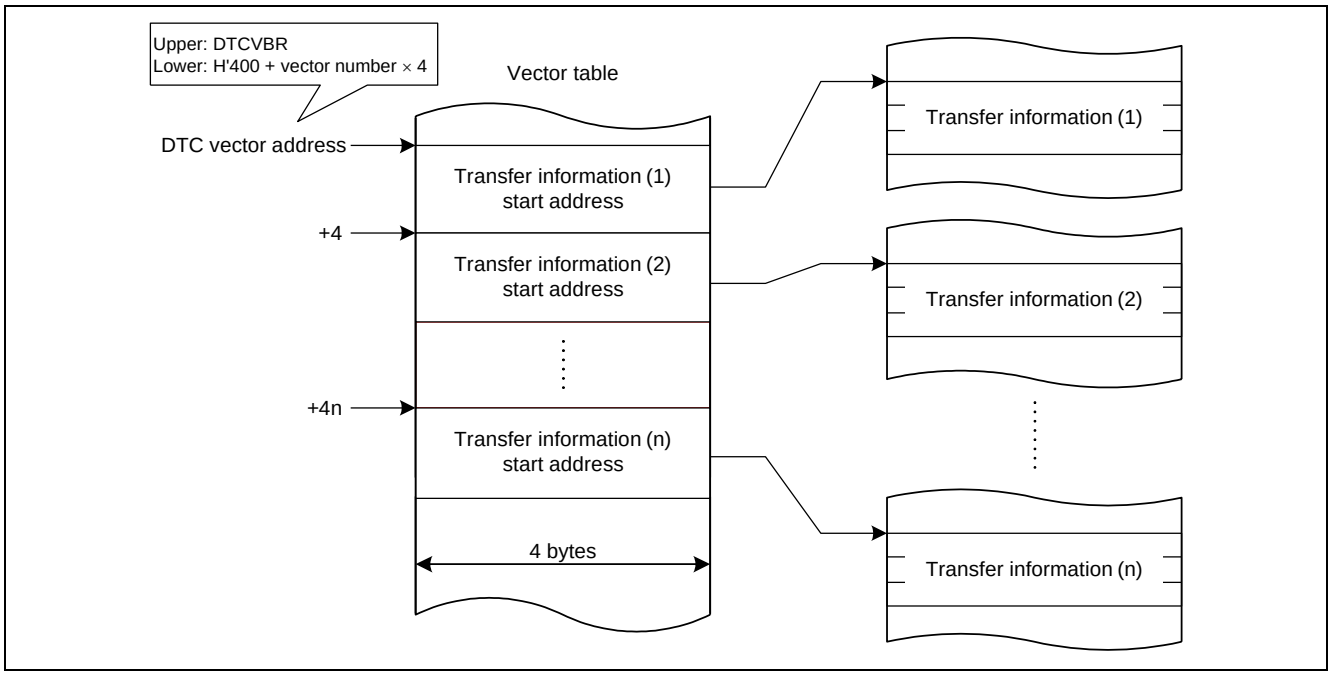


Figure 2.7 DTC Vector Configuration on SH7216 Group

On the RX72M the start address of the DTC vector table is calculated as “DTC vector base address (DTCVBR) + (vector number × 4)”. The base address of the DTC vector table is aligned with a 1 KB boundary such that the lower 10 bits are 0.

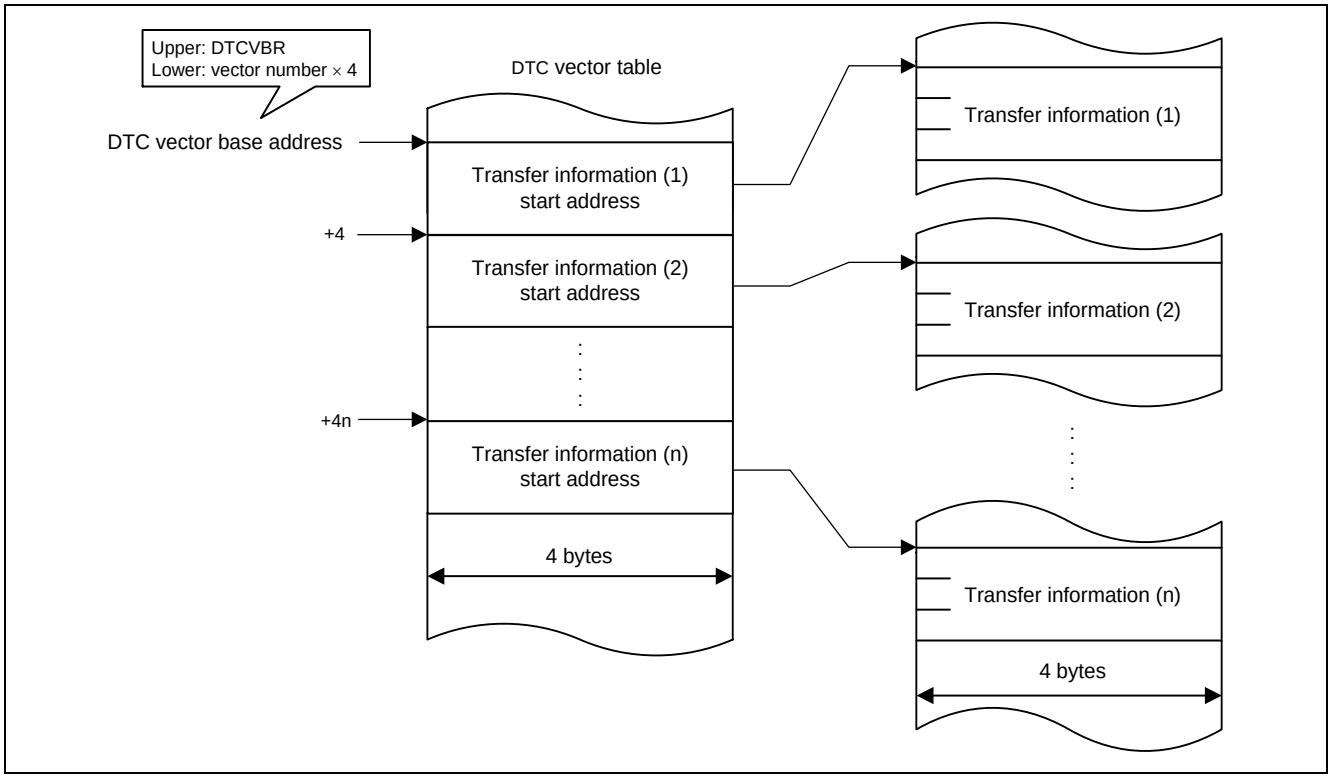


Figure 2.8 DTC Vector Configuration on RX72M

2.4.5 Allocation of Transfer Information

On the SH7216 Group the format of DTC transfer information is fixed at big-endian. On the RX72M the endian setting for DTC transfer information depends on the allocation area. The allocation of transfer information other than the endian setting is identical.

Short address mode is selected on the SH7216 Group by making a setting in the bus function extending register (BSCEHR) of the BSC and on the RX72M by making a setting in the DTC address mode register (DTCADMOD). Figure 2.9 illustrates the DTC transfer source and transfer destination addresses in short address mode.

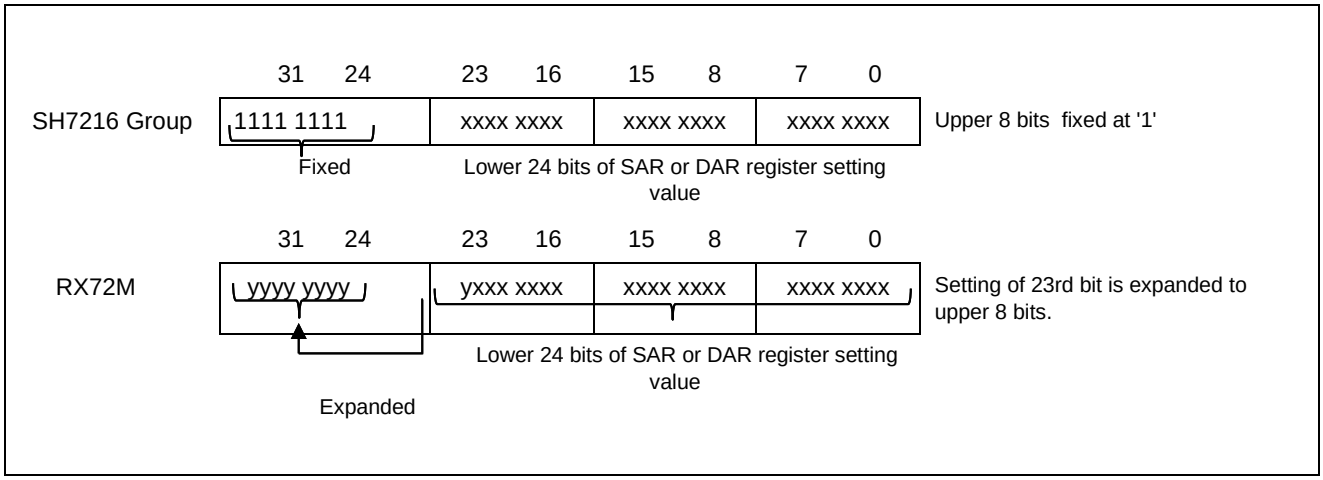


Figure 2.9 Transfer Source and Transfer Destination Addresses in Short Address Mode

Figure 2.10 shows the allocation of DTC transfer information on the SH7216 Group and RX72M.

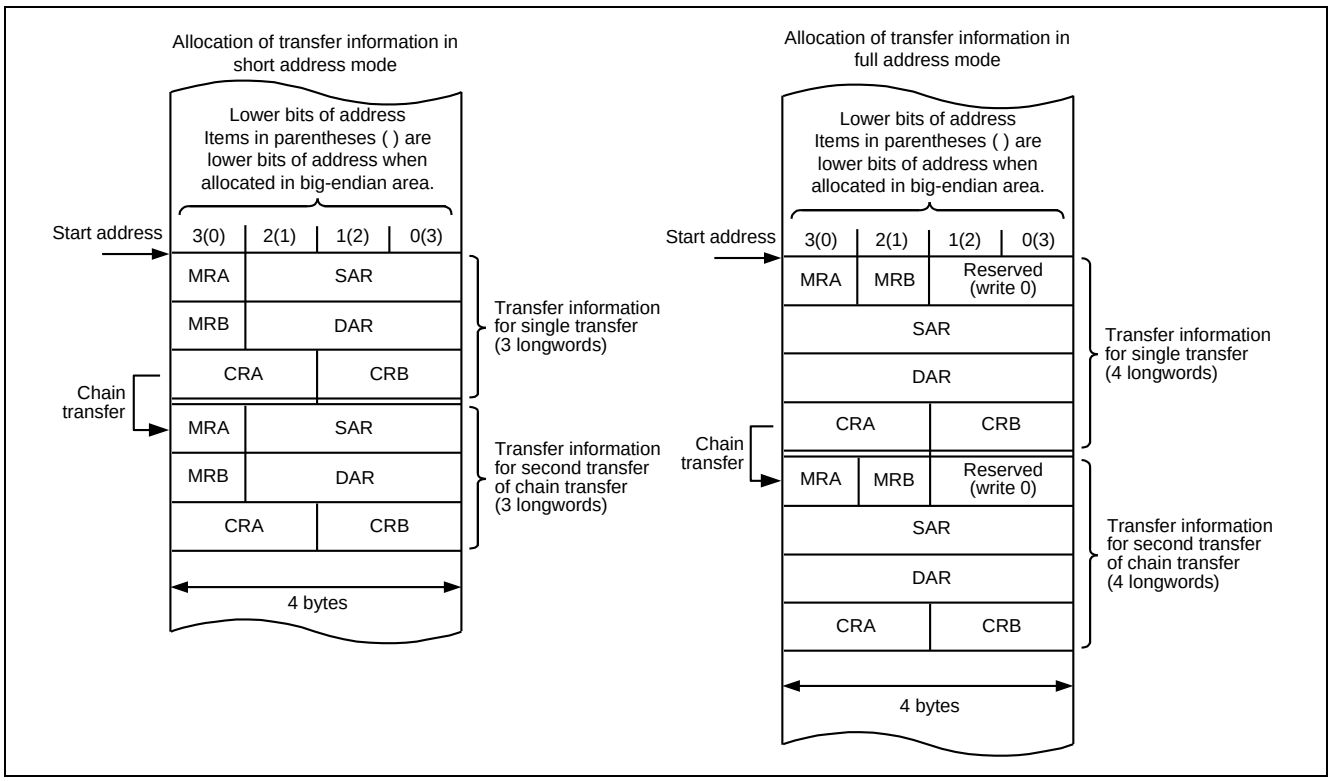


Figure 2.10 Allocation of Transfer Information

2.4.6 Module Stop

On the RX72M the DTCb module-stop state is canceled after a reset.

The module-stop setting bit (MSTPCRA.MSTPA28) is common to both the DTCb and DMACAa on the RX72M, so module-stop control for these two modules is simultaneous.

Refer to 2.20, Low Power Consumption Function for information on the module-stop state.

2.5 DMA Controller (DMACAa)

2.5.1 Comparison of Specifications

Direct memory access control functionality is implemented on the SH7216 Group by an on-chip DMAC and on the RX72M by an on-chip DMACAa and by a dedicated on-chip EXDMACa for transfers between external areas.

The internal bus configuration of the RX72M differs from that of the SH7216 Group. It supports independent data transfers by CPU instruction execution and by the DMAC or DTC for improved transfer performance. Table 2.11 is a comparative listing of the specifications of the SH7216 Group and RX72M.

Table 2.11 Comparison of SH7216 Group and RX72M Specifications (DMAC)

		SH7216 Group	RX72M	
Item		**DMAC**	**DMACAa**	**EXDMACa**
Number of channels		8 channels	8 channels	2 channels
Maximum transfer count (maximum transfer data unit count on RX)		16 M (16,777,216)	64 M data units (block transfer mode max. total transfer count: 1,024 data units × 65,536 blocks) Free running is also supported.	1 M data units (block transfer mode max. total transfer count: 1,024 data units × 1,024 blocks)
Activation sources		• External request • On-chip module request • Auto request (software trigger equivalent)	(External requests not supported.) • On-chip module request • Software trigger • External interrupt	• External request • On-chip module request • Software trigger
Channel priority		Selectable between the following: • Channel 0 > channel 1 > ... > channel 7 • Channel 0 > channel 4 > ... > channel 3 > channel 7 • Round robin	Fixed (channel 0 > channel 1 > ... > channel 3)	Fixed (channel 0 > channel 1)
Transfer data	1 data unit	8 bits, 16 bits, 32 bits, 128 bits	8 bits, 16 bits, 32 bits	8 bits, 16 bits, 32 bits
	Repeat size	—	Data units: 1 to 1,024	Data units: 1 to 1,024
	Block size	—	Data units: 1 to 1,024	Data units: 1 to 1,024
	Cluster size	—	—	Data units: 1 to 8
Transfer modes		None (The transfer mode on the SH is equivalent to normal transfer mode on the RX.)	• Normal transfer mode • Repeat transfer mode • Block transfer mode	• Normal transfer mode • Repeat transfer mode • Block transfer mode • Cluster transfer mode
Bus modes		• Cycle-steal mode • Burst mode	—	—
Address modes		• Single address mode • Dual address mode	—	• Single address mode • Dual address mode
Address update mode		• Fixed address • Increment • Decrement	• Fixed address • Offset addition • Increment • Decrement	• Fixed address • Offset addition • Increment • Decrement
Interrupt request	Transfer-end interrupt	• When data transfer finishes • When 1/2 of data	• Normal transfer mode: At the end of the specified number of transfers	

		transfer finishes	• Repeat transfer mode: At the end of transfer for the specified number of repeats • Block transfer mode: At the end of transfer of the specified number of blocks • Cluster transfer mode: At the end of forwarding a large number of specified classes (EXDMAC only)	
	Transfer escape-end interrupt	—	Generated after completion of data transfer equivalent to the repeat size or when the extended repeat area overflows.	
Other		• Reload function • Output of transfer-end signal	• Extended repeat area function • Event link function	• Extended repeat area function

2.5.2 DMAC Block Diagram

Figure 2.11 is a block diagram of the SH7216 Group's DMAC.

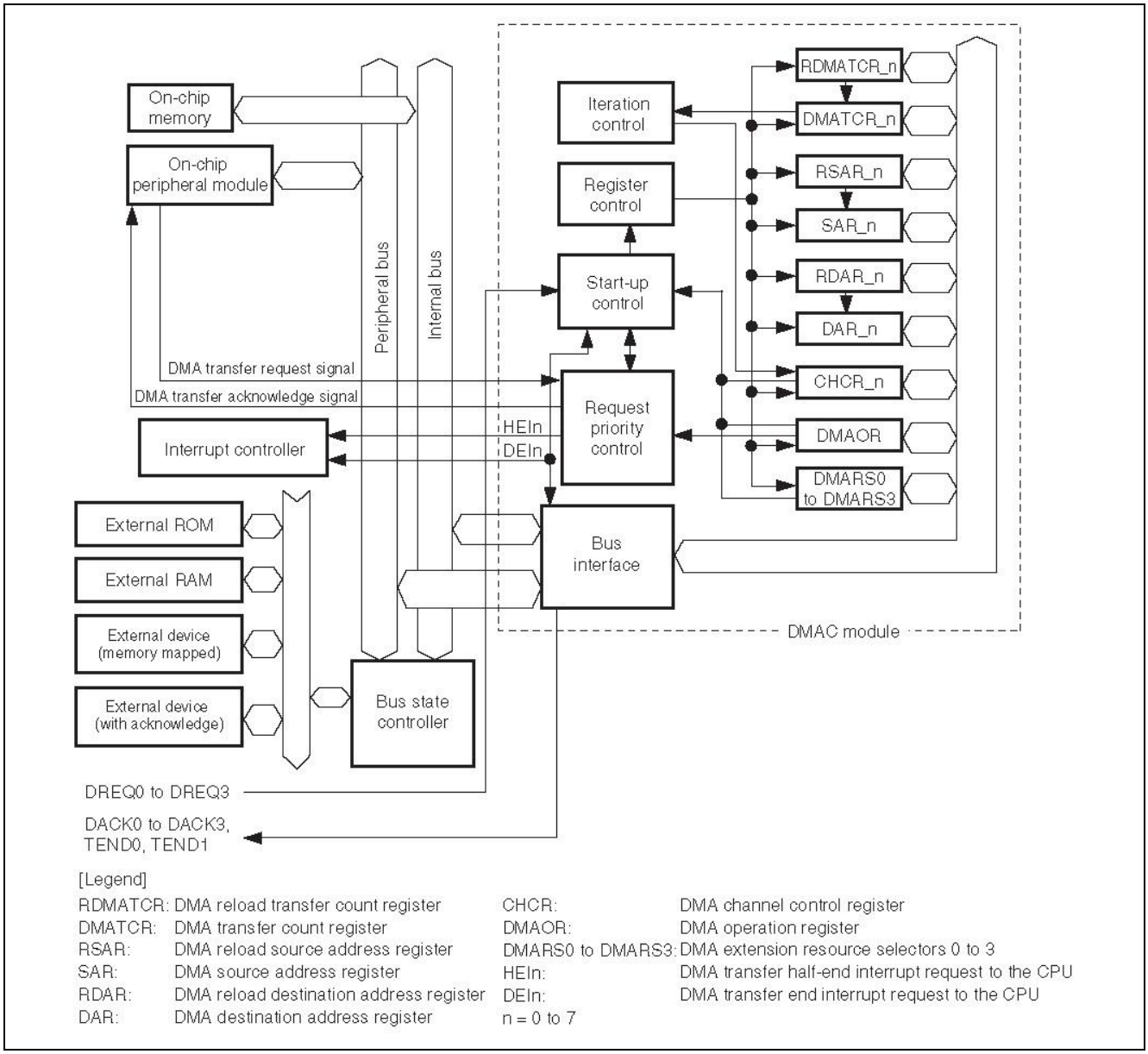


Figure 2.11 SH7216 Group DMAC Block Diagram

Figure 2.12 is a block diagram of the RX72M's DMACAa.

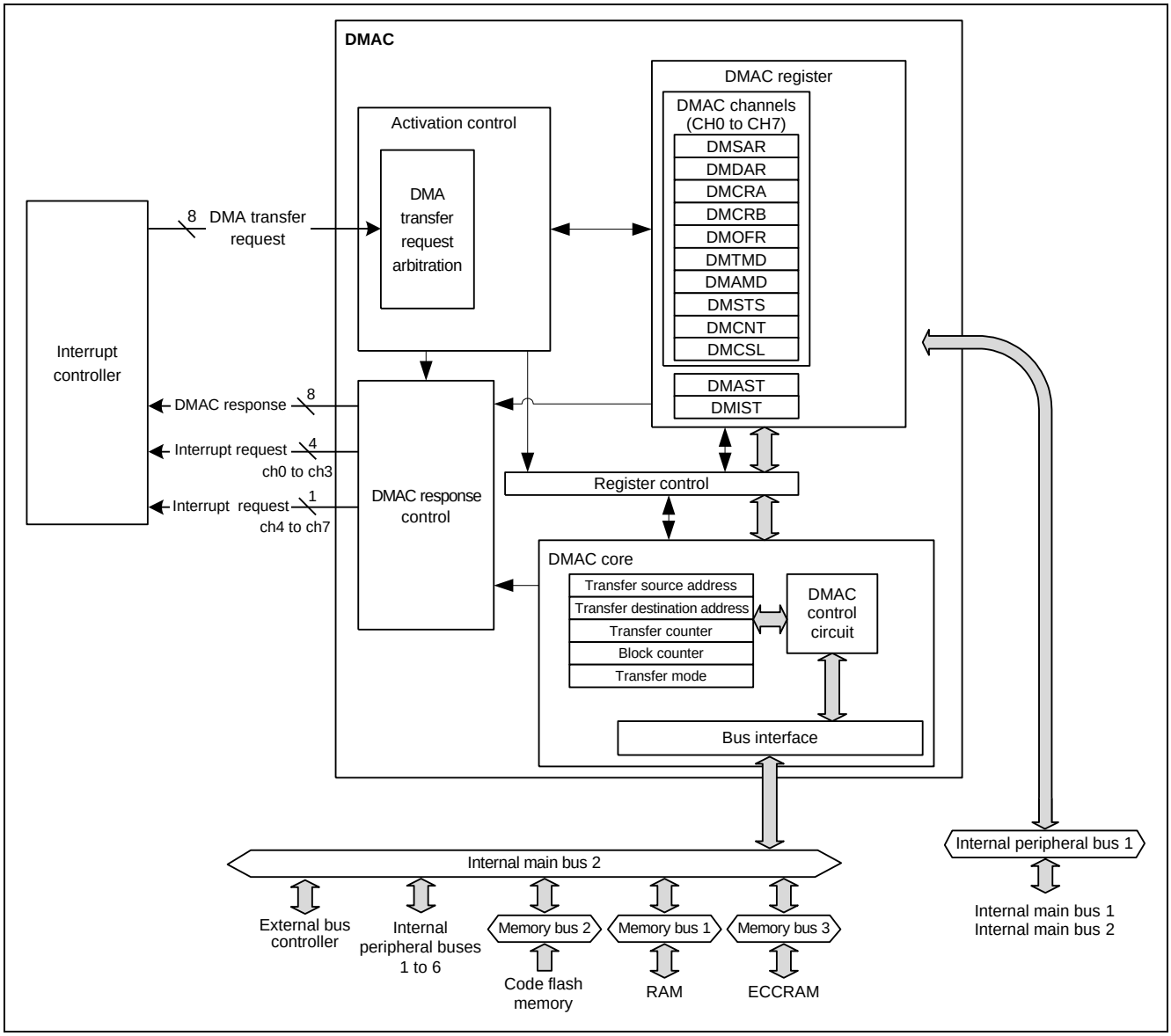
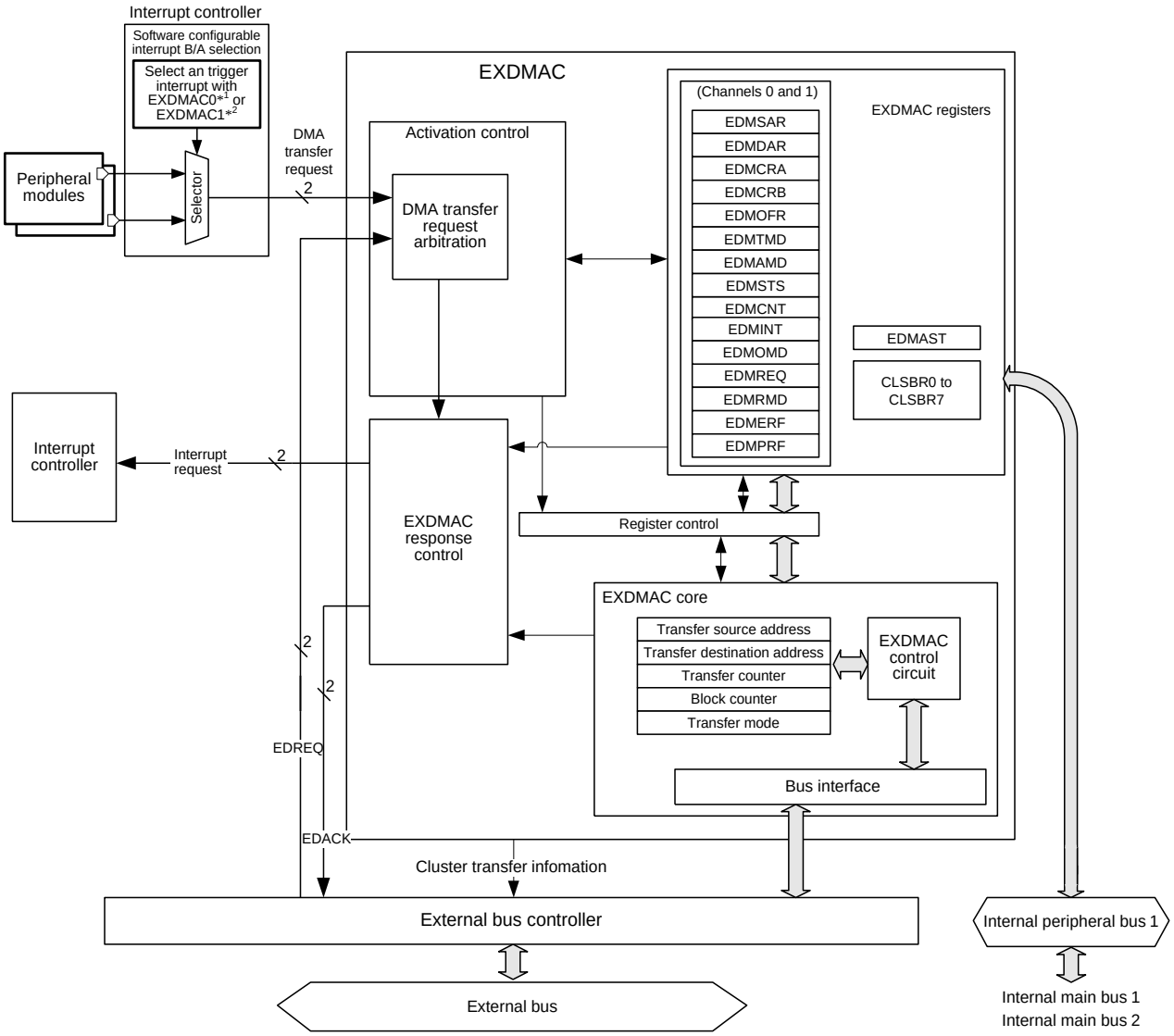


Figure 2.12 RX72M DMACAa Block Diagram

Figure 2.13 is a block diagram of the RX72M's EXDMACa.



Note 1. A software configurable interrupt B request from TPU1.TRGA selected in ICU.SLIBR144 or a software configurable interrupt A request from MTU1.TRGA selected in ICU.SLIAR208

Note 2. A software configurable interrupt B request from TPU1.TRGA selected in ICU.SLIBR145 or a software configurable interrupt A request from MTU1.TRGA selected in ICU.SLIAR209

Figure 2.13 RX72M EXDMACa Block Diagram

2.5.3 Register Comparison

Table 2.12 and Table 2.13 provide a comparative listing of the registers of the SH7216 Group and the RX72M.

Guide to Symbols in "Changes" Column of Table

◎: Register with same bit assignments on SH7216 Group and RX72M

△: Register with different bit assignments on SH7216 Group and RX72M

—: Register not present on SH7216 Group or RX72M

Table 2.12 SH7216 Group and RX72M Register Comparison (DMAC/DMACAa)

SH7216 Group (DMAC)*1	RX72M (DMACAa)*2	Changes
DMA operation register (DMAOR)	DMAC module start register (DMAST)	△
DMA source address register n (SAR_n)	DMA transfer source address register (DMACm.DMSAR)	◎
DMA destination address register n (DAR_n)	DMA transfer destination address register (DMACm.DMDAR)	◎
DMA transfer count register n (DMATCR_n)	DMA transfer count register (DMACm.DMCRA)	◎
DMA channel control register n (CHCR_n)*3	DMA transfer mode register (DMACm.DMTMD) DMA address mode register (DMACm.DMAMD) DMA interrupt setting register (DMACm.DMINT) DMA transfer enable register (DMACm.DMCNT) DMA status register (DMACm.DMSTS) DMA software start register (DMACm.DMREQ)	△
—	DMA block transfer count register (DMACm.DMCRB)	—
	DMA activation source flag control register (DMACm.DMCSL)	
	DMA offset register (DMAC0.DMOFR)	
	DMAC74 interrupt status monitor register (DMIST)	
DMA extension resource selectors 0 to 3 (DMARS0 to DMARS3) DMA reload source address register n (RSAR_n) DMA reload destination address register n (RDAR_n) DMA reload transfer count register n (RDMATCR_n)	—	—

Note 1. DMAC n: 0 to 7

Note 2. DMACAa m: 0 to 7

Note 3. On the RX72M transfer request settings from peripheral modules are made by means of the interrupt controller.

Table 2.13 SH7216 Group and RX72M Register Comparison (DMAC/EXDMACa)

SH7216 Group (DMAC)*1	RX72M (EXDMACa)*2	Changes
DMA operation register (DMAOR)	EXDMA module start register (EDMAST)	△
DMA source address register n (SAR_n)	EXDMA transfer source address register (EXDMACm.EDMSAR)	◎
DMA destination address register n (DAR_n)	EXDMA transfer destination address register (EXDMACm.EDMDAR)	◎
DMA transfer count register n (DMATCR_n)	EXDMA transfer count register (EXDMACm.EDMCRA)	◎
DMA channel control register n (CHCR_n)*3	EXDMA transfer mode register (EXDMACm.EDMTMD) EXDMA address mode register (EXDMACm.EDMAMD) EXDMA interrupt setting register (EXDMACm.EDMINT) EXDMA transfer enable register (EXDMACm.EDMCNT) EXDMA external request sense mode register (EXDMACm.EDMRMD) EXDMA output setting register (EXDMACm.EDMOMD) EXDMA status register (EXDMACm.EDMSTS) EXDMA software start register (EXDMACm.EDMREQ)	△
—	EXDMA block transfer count register (EXDMACm.EDMCRB)	—
	EXDMA offset register (EXDMAC0.EDMOFR)	
	EXDMA external request flag register (EXDMACm.EDMERF)	
	EXDMA peripheral request flag register (EXDMACm.EDMPRF)	
	Cluster buffer register y (CLSBRy) (y = 0 to 7)	
DMA extension resource selectors 0 to 3 (DMARS0 to DMARS3) DMA reload source address register n (RSAR_n) DMA reload destination address register n (RDAR_n) DMA reload transfer count register n (RDMATCR_n)	—	—

Note 1. DMAC n: 0 to 7

Note 2. DMACAa m: 0 or 1

Note 3. On the RX72M transfer request settings from peripheral modules are made by means of the interrupt controller.

2.5.4 Activation Source Settings

On the SH7216 Group activation sources that enable peripheral modules to activate the DMA are specified by setting the resource select bits in the DMA channel control registers (RS[3:0] in CHCR_0 to CHCR_7) and making appropriate settings in the DMA extension resource selectors (DMARSm). On the RX72M DMA activation sources are specified by setting activation source vector numbers in the DMAC trigger select registers (DMRSRm) of the interrupt controller, thereby enabling DMA activation by the corresponding interrupts.

Table 2.14 lists the types of DMA activation sources.

Table 2.14 DMA Activation Source Comparison

DMA Activation Sources	SH7216 Group	RX72M	
	DMAC	DMACAa	EXDMACa
Activation by software	Supported	Supported	Supported
Activation by external device via request pin	Supported (DREQn pin) Rising edge Falling edge Low level High level	Not supported	Supported (DREQm pin) Rising edge Falling edge Low level
Activation by interrupt from external interrupt input pin	Not supported	supported (IRQ pin)	Not supported
Activation by peripheral module	Supported (MTU, ADC, SCIF, IIC, CMT, USB, RSPI, CAN)	Supported （CMT, CMTW, USB, RSPI, QSPI, SDHI, MMCIF, SSIE, SRC, RIIC, SCI, PDC, SCIF, MTU, GPT, EPTPC, AES, TPU, ADC, SHA, ELC）	Supported (TPU, MTU)

n, m: Number of DMA channels (n = 0 to 3, m = 0 or 1)

2.5.5 Transfer Count

The RX72M supports free running operation, in which transfer count is not specified. Table 2.15 lists transfer count settings in normal transfer mode on the SH7216 Group and RX72M.

Table 2.15 Transfer Count Setting Values

Transfer count	SH7216 Group	RX72M (DMACAa, EXDMACa)
1	00000001h	0001h
65,535	FFFFh	FFFFh (max. transfer count)
16,777,215	00FFFFFFh	—
16,777,216	00000000h (max. transfer count)	—
Free running (no transfer count specified)	—	0000h

2.5.6 Transfer Sources and Destinations

Table 2.16 to Table 2.18 list the transfer sources and destinations supported by each DMA controller.

Table 2.16 SH7216 Group DMAC Transfer Sources and Destinations

	Transfer Destination				
Transfer Source	**External Device with DACK**	**External Memory**	**Memory-Mapped External Device**	**On-Chip Memory**	**On-Chip Peripheral Module**
External Device with DACK	—	●○	●○	—	—
External Memory	●○	○	○	○	○
Memory-Mapped External Device	●○	○	○	○	○
On-Chip Peripheral Module	—	○	○	○	○
On-Chip Memory	—	○	○	○	○

●: Single address mode transfers supported. ○: Dual address mode transfers supported.
—: Transfer not supported

Table 2.17 RX72M DMACAa Transfer Sources and Destinations

	Transfer Destination				
Transfer Source	**External Device with DACK**	**External Memory**	**Memory-Mapped External Device**	**On-Chip Memory**	**On-Chip Peripheral Module**
External Device with DACK	—	—	—	—	—
External Memory	—	○	○	○	○
Memory-Mapped External Device	—	○	○	○	○
On-Chip Peripheral Module	—	○	○	○	○
On-Chip Memory	—	○	○	○	○

○: Transfers supported. —: Transfer not supported

Table 2.18 RX72M EXDMACa Transfer Sources and Destinations

	Transfer Destination				
Transfer Source	**External Device with EDACK**	**External Memory**	**Memory-Mapped External Device**	**On-Chip Memory**	**On-Chip Peripheral Module**
External Device with EDACK	—	●	●	—	—
External Memory	●	○	○	—	—
Memory-Mapped External Device	●	○	○	—	—
On-Chip Peripheral Module	—	—	—	—	—
On-Chip Memory	—	—	—	—	—

●: Single address mode transfers supported. ○: Dual address mode transfers supported.
—: Transfer not supported

2.5.7 Address Modes

The SH7216 Group has two address modes: single address mode and dual address mode.

The EXDMACa of the RX72M has a single address mode and a dual address mode like the SH7216 Group. In single address mode a DMA transfer can be completed in a single bus cycle. Two bus cycles are required to complete a DMA transfer in dual address mode. On the DMACAa the address mode concept does not apply, but the method of specifying addresses and the operation are equivalent to dual address mode on the SH7216 Group.

2.5.8 Bus Modes

On the SH7216 Group the bus mode can be specified as either cycle-steal mode or burst mode. In cycle-steal mode the bus is released to another bus master when a single transfer finishes. In burst mode the bus is not released after the start of a DMA transfer until the transfer finishes.

On the RX72M it is not possible to specify the bus mode of the DMACAa or EXDMACa. This is because the bus architecture differs from that of the SH7216 Group. The RX72M supports parallel operation when the bus master accesses a different slave. On the RX72M it is possible for the DMAC to perform transfers between the peripheral bus and the external bus while the CPU is accessing the ROM to fetch CPU instructions or the RAM to manipulate operands.

Figure 2.14 shows an example in which the DMAC accesses the peripheral bus and the external bus using internal main bus 2 while the CPU is accessing the code flash memory and RAM.

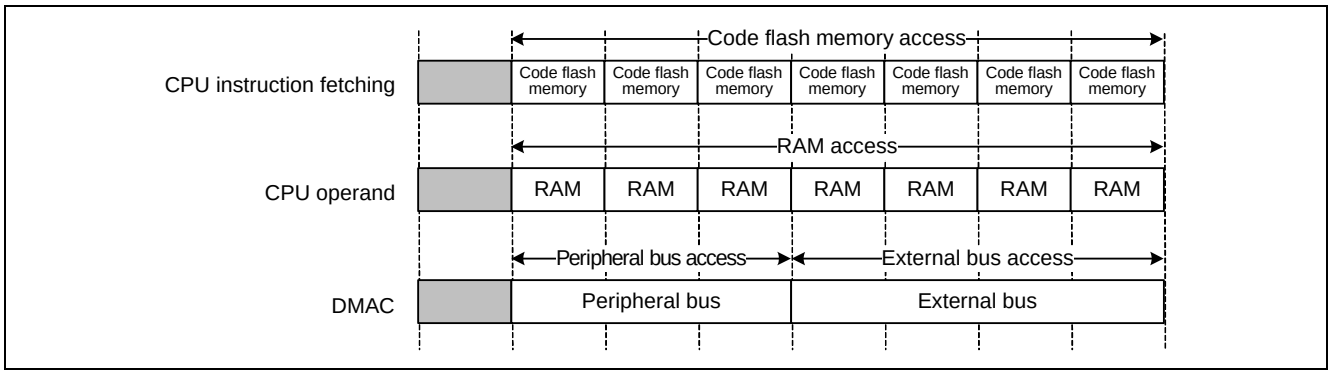


Figure 2.14 RX72M Parallel Bus Operation

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2.5.9 Module Stop

On the RX72M the DMACAa and EXDMACa module-stop state is canceled after a reset.

The module-stop setting bit (MSTPCRA.MSTPA28) is common to both the DTCb and DMACAa on the RX72M, so module-stop control for these two modules is simultaneous. The EXDMACa has an independent module-stop setting bit (MSTPCRA.MSTPA29), allowing it to be controlled individually.

Refer to 2.20, Low Power Consumption Function for information on the module-stop state.

2.6 Multi-function Timer Pulse Unit 3 (MTU3a)

2.6.1 Comparison of Specifications

Multi-function timer pulse unit functionality is provided on the SH7216 Group by the MTU2 and MTU2S and on the RX72M by the MTU3a.

The RX72M includes the MTU functionality of the SH7216 Group (Software compatibility). Table 2.19 lists comparative specifications of the SH7216 Group and RX72M.

Table 2.19 Comparison of SH7216 Group and RX72M Specifications (MTU)

		SH7216 Group		RX72M
Item		**MTU2**	**MTU2S**	**MTU3a**
Functional compatibility by channel	16-bit timer	MTU0	—	MTU0
		MTU1	—	MTU1
		MTU2	—	MTU2
		MTU3	MTU3S	MTU3, MTU6
		MTU4	MTU4S	MTU4, MTU7
		MTU5	MTU5S	MTU5
	32-bit timer	—	—	MTU8
Pulse I/O		Max. 16	Max. 8	Max. 28
Pulse input		3	3	3
Count clock		Selectable for each channel among eight clocks employing the peripheral clock (Pϕ) and external clocks (TCLKA, TCLKB, TCLKC, and TCLKD)	Selectable for each channel among six clocks employing the MTU2S clock (Mϕ).	Selectable for each channel among 14 clocks employing the peripheral module clock (PCLKA) and external clocks (MTCLKA, MTCLKB, MTCLKC, MTCLKD, and MTIOC1A).
DTC/DMAC activation		DTC/DMAC activation supported	DTC activation supported	DTC/DMAC activation supported
A/D conversion start triggers		Trigger generation supported	Trigger generation supported	Trigger generation supported
Interrupt sources		28	13	43
Noise cancellation		None	None	Ability to enable noise filtering for external clock pins
Other		• Cascade connection	—	• Event link • Cascade connection

2.6.2 Handling of interrupt Flags

SH7216's MTU2, MTU2S and RX72M's MTU3 are software compatible. The functions of MTU0 to MTU4 and MTU6 to MTU8 can be ported without changing the register except for the timer status register (TSR) interrupt flag. (Initial settings such as terminal settings need to be changed separately)

The RX72M does not have an interrupt flag in the timer status register (TSR), but you can achieve the same processing by setting an interrupt controller.

The MTU2S of the SH7216 Group can activate the DTC only, but the RX72M can activate the DTC and DMAC on all channels.

The RX72M MTU interrupt is provided with software configurable interrupt A. The interrupt controller's software configurable interrupt A status flags (PIARk.PIRn) are not cleared automatically, but even if left uncleared they do not affect the generation of interrupt requests.

Refer to 1.8, Interrupt Handling for information about interrupts.

Table 2.20 Comparison of SH7216 Group and RX72M Specifications (MTU)

	SH7216 Group							
	MTU0	**MTU1**	**MTU2**	**—**	**MTU3 MTU3S**	**MTU4 MTU4S**	**MTU5 MTU5S**	**—**
	RX72M							
Item	**MTU0**	**MTU1**	**MTU2**	**MTU1 MTU2*2**	**MTU3 MTU6**	**MTU4 MTU7**	**MTU5**	**MTU8**
Compare match nA*3	○	○	○	—	○	○	—	○
Input capture nA*3	○	○	○	○	○	○	—	○
Compare match nB*3	○	○	○	—	○	○	—	○
Input capture nB*3	○	○	○	○	○	○	—	○
Compare match nC*3	○	—	—	—	○	○	—	○
Input capture nC*3	○	—	—	—	○	○	—	○
Compare match nD*3	○	—	—	—	○	○	—	○
Input capture nD*3	○	—	—	—	○	○	—	○
Overflow	○	○	○	○	○	○	—	○
Underflow	—	○	○	○	—	○*1	—	—
Compare match nE	○	—	—	—	—	—	—	—
Compare match nF	○	—	—	—	—	—	—	—
Compare match nU*3	—	—	—	—	—	—	○	—
Input capture nU*3	—	—	—	—	—	—	○	—
Compare match nV*3	—	—	—	—	—	—	○	—
Input capture nV*3	—	—	—	—	—	—	○	—
Compare match nW*3	—	—	—	—	—	—	○	—
Input capture nW*3	—	—	—	—	—	—	○	—

n: Channel number ○: Supported —: Not supported

Note 1. Complementary PWM mode only

Note 2. 32-bit access

Note 3. "S" is appended at the end to indicate MTU2S.

2.6.3 Register Comparison

Table 2.21 is a comparative listing of the registers on the SH7216 Group and RX72M.

Guide to Symbols in "Changes" Column of Table

◎: Register with same bit assignments on SH7216 Group and RX72M

△: Register with different bit assignments on SH7216 Group and RX72M

—: Register not present on SH7216 Group or RX72M

Table 2.21 SH7216 Group and RX72M Register Comparison (MTU)

Register Name*1	SH7216 Group (MTU2, MTU2S)	RX72M (MTU3a)	Changes
Timer control register	TCR_0 to TCR_4 TCRU/V/W_5 TCR_3/4S	MTU0.TCR to MTU4.TCR MTU5.TCRU/V/W MTU6/7.TCR	◎
	TCRU/V/W_5S	—	—
	—	MTU8.TCR	—
Timer control register 2	—	MTU0.TCR2 to MTU4.TCR2 MTU6.TCR2 to MTU8.TCR2 MTU5.TCR2U/V/W	—
Timer mode register (SH7216 Group) Timer mode register 1 (RX72M)	TMDR_0/3/4 TMDR_3/4S	MTU0/3/4.TMDR1 MTU6/7.TMDR1	◎
	TMDR_1/2	MTU1/2.TMDR1	△
	—	MTU8.TMDR1	—
Timer mode register 2	—	MTU.TMDR2A/B	—
Timer mode register 3	—	MTU1.TMDR3	—
Timer I/O control register	TIORH_0 TIOR_1	MTU0.TIORH MTU1.TIOR	△
	TIORL_0 TIOR_2 TIORU/V/W_5 TIORH/L_3/4 TIORH/L_3/4S	MTU0.TIORL MTU2.TIOR MTU5.TIORU/V/W MTU3/4.TIORH/L MTU6/7.TIORH/L	◎
	TIORU/V/W_5S	—	—
	—	MTU8.TIORH/L	—
Timer compare match clear register	TCNTCMPCLR	MTU5.TCNTCMPCLR	◎
	TCNTCMPCLRS	—	—
Timer interrupt enable register	TIER_0 to TIER_5 TIER_3/4S TIER2_0	MTU0.TIER to MTU5.TIER MTU6/7.TIER MTU0.TIER2	◎
	TIER_5S	—	—
	—	MTU8.TIER	—

Register Name*1	SH7216 Group (MTU2, MTU2S)	RX72M (MTU3a)	Changes
Timer status register	TSR_1 to TSR_4 TSR_3/4S	MTU1.TSR to MTU4.TSR MTU6/7.TSR	△
	TSR_0 TSR2_0 TSR_5/5S	—	—
Timer buffer operation transfer mode register	TBTM_0/3/4 TBTM_3/4S	MTU0/3/4.TBTM MTU6/7.TBTM	◎
Timer input capture control register	TICCR	MTU1.TICCR	◎
Timer A/D conversion start request control register	TADCR, TADCRS	MTU4.TADCR, MTU7.TADCR	◎
Timer A/D conversion start request cycle set register	TADCORA/B_4 TADCORA/B_4S	MTU4.TADCORA/B MTU7.TADCORA/B	◎
Timer A/D conversion start request cycle set buffer register	TADCOBRA/B_4 TADCOBRA/B_4S	MTU4.TADCOBRA/B MTU7.TADCOBRA/B	◎
Timer counter	TCNT_0 to TCNT_4 TCNTU/V/W_5 TCNT_3/4S	MTU0.TCNT to MTU4.TCNT MTU5.TCNTU/V/W MTU6/7.TCNT	◎
	TCNTU/V/W_5S	—	—
	—	MTU8.TCNT	—
Timer longword counter	—	MTU1.TCNTLW	—
Timer general register	TGR_0 (A to F) TGR_1/2 (A, B) TGR_3/4 (A to D) TGR_5 (U, V, W) TGR_3/4S (A to D)	MTU0.TGR (A to F) MTU1/2.TGR (A, B) MTU3/4.TGR (A to D) MTU5.TGR (U, V, W) MTU6/7.TGR (A to D)	◎
	TGR_5S (U, V, W)	—	—
	—	MTU3/6.TGR (E) MTU4/7.TGR (E, F) MTU8.TGR (A to D)	—
Timer longword general register	—	MTU1.TGRA/BLW	—
Timer start register	TSTR	MTU.TSTRA	◎
	TSTRS, TSTR_5	MTU.TSTRB, MTU5.TSTR	◎
	TSTR_5S	—	—
Timer synchronous register	TSYR, TSYRS	MTU.TSYRA, MTU.TSYRB	◎
Timer synchronous clear register	TSYCRS	MTU6.TSYCR	◎
Timer counter synchronous start register	TCSYSTR	MTU.TCSYSTR	◎
Timer read/write enable register	TRWER, TRWERS	MTU.TRWERA, MTU.TRWERB	◎
Timer output master enable register	TOER, TOERS	MTU.TOERA, MTU.TOERB	◎
Timer output control register 1	TOCR1, TOCR1S	MTU.TOCR1A, MTU.TOCR1B	◎
Timer output control register 2	TOCR2, TOCR2S	MTU.TOCR2A, MTU.TOCR2B	◎
Timer output level buffer register	TOLBR, TOLBRS	MTU.TOLBRA, MTU.TOLBRB	◎

Register Name*1	SH7216 Group (MTU2, MTU2S)	RX72M (MTU3a)	Changes
Timer gate control register (SH7216 Group) Timer gate control register A (RX72M)	TGCR	MTU.TGCRA	◎
	TGCRS	—	—
Timer sub counter	TCNTS, TCNTSS	MTU.TCNTSA, MTU.TCNTSB	◎
Timer period data register	TCDR, TCDRS	MTU.TCDRA, MTU.TCDRB	◎
Timer period buffer register	TCBR, TCBRS	MTU.TCBRA, MTU.TCBRB	◎
Timer dead time data register	TDDR, TDDRS	MTU.TDDRA, MTU.TDDRB	◎
Timer dead time enable register	TDER, TDERS	MTU.TDERA, MTU.TDERB	◎
Timer buffer transfer set register	TBTER, TBTERS	MTU.TBTERA, MTU.TBTERB	◎
Timer waveform control register	TWCR, TWCRS	MTU.TWCRA, MTU.TWCRB	◎
Timer interrupt skipping set register (SH7216 Group) Timer interrupt skipping set register 1 (RX72M)	TITCR, TITCRS	MTU.TITCR1A, MTU.TITCR1B	◎
Timer interrupt skipping set register 2	—	MTU.TITCR2A, MTU.TITCR2B	—
Timer interrupt skipping counter (SH7216 Group) Timer interrupt skipping counter 1 (RX72M)	TITCNT, TITCNTS	MTU.TITCNT1A, MTU.TITCNT1B	◎
Timer interrupt skipping counter 2	—	MTU.TITCNT2A, MTU.TITCNT2B	—
Timer interrupt skipping mode register	—	MTU.TITMRA, MTU.TITMRB	—
Noise filter control register n	—	NFCR0 to NFCR4 in MTU0 to MTU4 NFCR6 to NFCR8 in MTU6 to MTU8 MTU0.NFCRC	—
Noise filter control register 5	—	MTU5.NFCR5	—

Note 1. On the SH7216 Group MTU2S register names have S appended at the end.

2.6.4 Module Stop

As on the SH7216 Group, the MTU3a of the RX72M is set to the module-stop state after a reset, and no clock is supplied.

Refer to 2.20, Low Power Consumption Function for information on the module-stop state.

2.7 Port Output Enable 3(POE3a)

2.7.1 Comparison of Specifications

Port output enable functionality is provided on the SH7216 Group by the POE2 and on the RX72M by the POE3a.

The RX72M includes the POE functionality of the SH7216 Group (Upward compatibility). Table 2.22 lists comparative specifications of the SH7216 Group and RX72M.

Table 2.22 Comparison of SH7216 Group and RX72M Specifications (POE)

Item	SH7216 Group (POE2)	RX72M (POE3)
Clock source	Peripheral clock (Pϕ)	Peripheral module clock (PCLKB)
Pins subject to high-impedance control	• MTU0 pins • MTU high-current pins — MTU3 pins — MTU4 pins — MTU3S pins — MTU4S pins	• MTU0 pins • MTU complementary PWM output pins — MTU3 pins — MTU4 pins — MTU6 pins — MTU7 pins
High-impedance request generation conditions	• Change in input pin state — Falling edge — Low level for Pϕ/8 × 16 cycles — Low level for Pϕ/16 × 16 cycles — Low level for Pϕ/128 × 16 cycles • Combined output signal level match for 1 cycle or more (short) • Register setting	• Change in input pin state — Falling edge — Low level for PCLKB/8 × 16 cycles — Low level for PCLKB/16 × 16 cycles — Low level for PCLKB/128 × 16 cycles • Combined output signal level match for 1 cycle or more (short) • Register setting • Detection of clock generation circuit oscillation stop
Interrupt sources	• High-impedance request by change in input pin state • High-impedance request by output signal level comparison	• High-impedance request by change in input pin state • High-impedance request by output signal level comparison
Other	—	Ability to add high-impedance control conditions for MTU complementary PWM output pins and MTU0 pins

2.7.2 Input/Output Pins

The SH7216 group's input terminals support only POE0 # to POE4 # and POE8 # for the MTU, while the RX72M also supports other input pins that are multiplexed to the MTU.

On the SH7216 Group the MTU0 pins are high-impedance only when assigned as general I/O pins when the MTU2 or MTU2S function is selected. On the RX72M multiplexed MTU complementary PWM output pins, MTU0 pinsare high-impedance even when the MTU is not selected.

Table 2.23 lists the input pins on the SH7216 Group and RX72M, and Table 2.24 provides a comparative listing of output pin combinations.

Table 2.23 POE Input Pins

SH7216 Group	RX72M	Subject to High-Impedance Control*1
POE0# to POE3#	POE0#	SH7216 Group: MTU3 and MTU4 pins RX72M: MTU3, MTU4, and all other control target pins
POE4#	POE4#	SH7216 Group: MTU3S and MTU4S pins RX72M: MTU6, MTU7 and all other control target pins
POE8#	POE8#	MTU0 pins and all other control target pins
—	POE10#	All control target pins
—	POE11#	All control target pins

Note 1. On the RX72M the addition of high-impedance control conditions enables control of other pins as well.

Table 2.24 POE Output Pin Combinations

SH7216 Group	RX72M	Subject to High-Impedance Control
TIOC3B and TIOC3D	MTIOC3B and MTIOC3D	MTU3 and MTU4 pins
TIOC4A and TIOC4C	MTIOC4A and MTIOC4C	
TIOC4B and TIOC4D	MTIOC4B and MTIOC4D	
TIOC3BS and TIOC3DS	MTIOC6B and MTIOC6D	SH7216 Group: MTU3S and MTU4S pins RX72M: MTU6 and MTU7 pins
TIOC4AS and TIOC4CS	MTIOC7A and MTIOC7C	
TIOC4BS and TIOC4DS	MTIOC7B and MTIOC7D	

2.7.3 Register Comparison

On the SH7216 Group the port impedance state is specified by making settings to the port output enable control registers (POECR1 and POECR2). On the RX72M the port impedance state is specified by making settings to the port output enable control registers (POECR1 and POECR2), and the ports assigned to the various pins are specified by making settings to the pin select registers (M0SELR1 and M0SELR2, M3SELR, and M4SELR1 and M4SELR2) of the MTU channels.

Table 2.25 is a comparative listing of the registers on the SH7216 Group and RX72M.

Guide to Symbols in "Changes" Column of Table

◎: Register with same bit assignments on SH7216 Group and RX72M

△: Register with different bit assignments on SH7216 Group and RX72M

—: Register not present on SH7216 Group or RX72M

Table 2.25 SH7216 Group and RX72M Register Comparison (POE)

SH7216 Group (POE2)	RX72M (POE3a)	Changes
Input level control/status register 1 (ICSR1)	Input level control/ status register 1 (ICSR1)	◎
Input level control/status register 2 (ICSR2)	Input level control/ status register 2 (ICSR2)	◎
Input level control/status register 3 (ICSR3)	Input level control/ status register 3 (ICSR3)	◎
—	Input level control/ status register 4 (ICSR4) Input level control/ status register 5 (ICSR5) Input level control/ status register 6 (ICSR6)	—
Output level control/status register 1 (OCSR1)	Output level control/ status register 1 (OCSR1)	◎
Output level control/status register 2 (OCSR2)	Output level control/ status register 2 (OCSR2)	◎
Software port output enable register (SPOER)	Software port output enable register (SPOER)	△
Port output enable control register 1 (POECR1)	Port output enable control register 1 (POECR1) MTU0 pin select register 1 (M0SELR1) MTU0 pin select register 2 (M0SELR2)	△
Port output enable control register 2 (POECR2)	Port output enable control register 2 (POECR2) MTU3 pin select register (M3SELR) MTU4 pin select register 1 (M4SELR1) MTU4 pin select register 2 (M4SELR2)	△
—	Active level setting register 1 (ALR1)	—
	Port output enable control register 4 (POECR4) Port output enable control register 5 (POECR5) MTU6 pin select register (M6SELR)	

2.7.4 High-Impedance Control by Oscillation Stop Detection

The RX72M provides the ability to transition user-specified MTU complementary PWM output pins, MTU0 pins to the high-impedance state when oscillation stop is detected by the oscillation stop detection function of the clock generation circuit.

Pins that transition to the high-impedance state when oscillation stop is detected revert to the default state after a reset, but the high-impedance state is canceled by means of register settings.

2.7.5 Addition of High-Impedance Control Conditions

The RX72M supports the addition of high-impedance control conditions for the MTU complementary PWM output pins, MTU0 pins. Table 2.26 lists the high-impedance control conditions that can be added.

Table 2.26 Additional High-Impedance Control Conditions on RX72M

Subject to High-Impedance Control	Additional High-Impedance Control Conditions
MTU3 and MTU4 pins	Input level detection on POE4#, POE8#, POE10#, and POE11#
MTU6 and MTU7 pins	Input level detection on POE0#, POE8#, POE10#, and POE11#.
MTU0 pins	Input level detection on POE0#, POE4#, POE10#, and POE11#.

2.7.6 Interrupts

On the RX72M POE3a is assigned to group interrupt BL1. The interrupt controller’s group BL1 interrupt status flag (GRPBL1.ISn) is automatically cleared when the corresponding bit in the module’s status register is cleared.

Refer to 1.8, Interrupt Handling for information about interrupts.

2.8 Watchdog Timers (WDTA)

2.8.1 Comparison of Specifications

The SH7216 Group incorporates the WDT as its watchdog timer module. The RX72M incorporates, in addition to the WDTA, the IWDTa, which operates on a dedicated independent clock and is able to operate when the microcontroller is in the low-power-consumption state.

Table 2.27 lists comparative specifications of the SH7216 Group and RX72M.

Table 2.27 Comparison of SH7216 Group and RX72M Specifications (WDT)

Item	SH7216 Group (WDT)	RX72M (WDTA, IWDTa)
Clock sources	Peripheral clock (Pϕ)	WDTA: Peripheral module clock (PCLKB) IWDTa: IWDT dedicated clock (IWDTCLK) PCLKB ≥ 4 × IWDTCLK frequency after IWDTCLK frequency division
Clock frequency division ratio	Pϕ /1, 64, 128, 256, 512, 1,024, 4,096, 16,384	WDTA: PCLKB/4, 64, 128, 512, 2048, 8192 IWDTa: IWDTCLK/1, 16, 32, 64, 128, 256
Count operation	8-bit up-counter	14-bit down-counter
Operating modes	• Watchdog timer mode • Interval timer mode	Change in the option setting memory, not the concept of operation mode • Reset output enabled (equivalent to watchdog timer mode) • Interrupt requests enabled (equivalent to interval timer mode)
Count start condition	• Timer control /Enable timer enable bit in status register	Select from the following actions • 1) Counting automatically starts after a reset is released(Auto-start mode) • 2) Counting is started by refresh operation (Register start mode)
Count stop condition	• Timer enable bit setting • After internal reset caused by overflow • Power-on reset caused by RES pin (counter and setting initialization)	• Reset (counter and setting initialization) • Underflow • Refresh error • In low power consumption states(depends on the register setting)
Operation at overflow/ underflow	Watchdog timer mode • Internal reset (power-on reset and manual reset) • WDTOVF output Interval timer mode • Interrupt	When reset output enabled • Internal reset When interrupt request output enabled • Interrupt
Interrupt sources	• Overflow of up-counter	• Underflow of down-counter • Refresh error
Other	—	• Event link (IWDTa only) • Window function • Also operates in low-power-consumption state (IWDTa only) • Settings made in option function select register 0 in auto-start mode — Clock division ratio — Refresh window start/end — Timeout period — Enabling of interrupt requests and resets

2.8.2 Count Start Conditions

On the SH7216 Group count operation starts when 1 is written to the timer enable bit. With the RX72M, it is possible to select a register start mode (similar to the SH7216 group) that starts counting by writing a register in the option function selection register, or an auto start mode that automatically starts counting after reset.

When auto-start mode is selected on the RX72M, count operation starts automatically after a reset, in accordance with the setting of option function select register (OFS0). When register start mode is selected, count operation is started by a refresh, after the appropriate register settings are made following reset cancelation.

2.8.3 Refresh Operation

On the RX72M the count is refreshed after 00h and then FFh is written to the WDT refresh register (WDTRR). Writes to the WDT refresh register must take place within the refresh-enabled interval. To refresh the count of IWDTa, perform the same write operation to the IWDT refresh register (IWDTRR) within the refresh-enabled interval.

Table 2.28 Comparison of Refresh Operation

Item	SH7216 Group	RX72M (WDTA)
Refresh condition	Write to watchdog timer counter (WTCNT)	00h and then FFh written to refresh register (WDTRR) within refresh-enabled interval
Counter initial value after refresh	Value written to watchdog timer counter (WTCNT)	Register start mode • Value selected by timeout period selection bits in WDT control register (WDTCR.TOPS) Auto start mode • Value selected by WDT timeout period select bits in option function select register (OFS0.WDTTOPS)

2.8.4 Register Write Limitations

Limitations apply when writing to the WDT registers of the SH7216 Group and RX72M. These register write limitations are summarized below.

Table 2.29 SH7216 Group Register Write Limitations

Item	Write Limitations
Watchdog timer counter (WTCNT) Watchdog reset control/status register (WRCSR) • Reset enable (WRCSR.RSTE) • Reset select (WRCSR.RSTS)	Writing in word-size units in the following configuration: • Upper byte: 5Ah • Lower byte: Write data
Watchdog timer control/status register (WTCSR) Watchdog reset control/status register (WRCSR) • Watchdog timer overflow (WRCSR.WOVF)	Writing in word-size units in the following configuration: • Upper byte: A5h • Lower byte: Write data

Table 2.30 RX72M Register Write Limitations

Item	Write Limitations
WDT control register (WDTCR) WDT reset control register (WDTRCR) IWDT control register (IWDTCR) IWDT reset control register (IWDTRCR) IWDT count stop control register (IWDTCSTPR)	Can be written to once in the interval between reset cancellation and the first refresh operation.

2.8.5 Interrupts

On the RX72M WDTA and IWDTa interrupts may be non-maskable or maskable. The interrupt controller interrupt status flag (IRn.IR) is cleared automatically when the corresponding interrupt is accepted.

Refer to 1.8, Interrupt Handling for information about interrupts.

2.8.6 All-Module Stop

The WDTA and IWDTa do not support a module-stop function.

The WDTA and IWDTa behave differently when the RX72M is in the all-module stop state. Table 2.31 lists the states of these modules when the microcontroller is in the all-module stop state.

Table 2.31 Module States in All-Module Stop State on RX72M

Module Name	Module State
Watchdog timer (WDTA)	Count stopped (state retained)
Independent watchdog Timer (IWDTa)	Selectable in option setting memory

2.8.7 Option Settings

On the RX72M it is possible to specify the microprocessor's state after a reset by setting the start mode select bits (OFS0.IWDTSTRT and OFS0.WDTSTRT).

2.9 Serial Communication Interface (SCIj, SCIi, SCIh)

2.9.1 Comparison of Specifications

The SH7216 Group incorporates the SCI, which provide serial communication interface functionality, and the RX72M incorporates the SCIj , SCIi and SCIh.

The SCIi and SCIj provides, in addition to conventional asynchronous and clock-synchronous transfer capabilities, extended asynchronous functionality that supports a smartcard (IC card) interface. In addition, it supports simple I^2C bus interface single-master operation and simple SPI bus interface operation. SCIh has an extended serial interface in addition to the above features. For details of the transfer methods not supported on the SH7216 Group, refer to RX72M Group User's Manual: Hardware.

Table 2.32 provides a comparative listing of the specifications of the SH7216 Group and RX72M.

Table 2.32 Comparison of SH7216 Group and RX72M Specifications (SCI)

Item		SH7216 Group (SCI)	RX72M (SCIg, SCIh)
Number of channels		4 channels (SCI0 to SCI2, SCI4)	SCIh：1channel（SCI12） SCIi：5channels（SCI7 to 11） SCIj：7channels（SCI0 to 6）
Clock source		Peripheral clock (Pϕ)	Peripheral module clock (PCLKB)
Serial communication modes		• Asynchronous • Clock-synchronous	• Asynchronous • Clock-synchronous • Smartcard interface • Simple I^2C bus • Simple SPI bus
Transfer speed		Any bit rate may be selected using the on-chip baud rate generator.	
Full-duplex communication		Double-buffer configurations for transmission and reception to enable continuous transmission and continuous reception	
Data transfer		Selectable between LSB-first and MSB-first (except for asynchronous 7-bit data)	Selectable between LSB-first and MSB-first (MSB-first only on simple I^2C bus)
DTC/DMAC activation		DTC activation supported	DTC/DMAC activation supported
Interrupt sources		• Transmit data-empty • Transmit end • Receive data-full • Receive error	• Transmit data-empty • Transmit end • Receive data-full • Receive error • Date match Used in simple I^2C mode. • Start condition • Restart condition • Stop condition generation-end
Asynchronous mode	Data length	7 bits, 8 bits	7 bits, 8 bits, 9 bits
	Stop bits	1 bit, 2 bits	
	Parity function	Even parity, odd parity, or no parity	
	Receive error detection	Parity error, overrun error, or framing error	
	Hardware flow control	No	Supported (controllable with CTSn# and RTSn# pins)
	Data match detection	No	Compares receive data and comparison data, and generates interrupt when they are matched
	Break detection	Detection of when a framing error occurs is possible by directly reading the level of the RXDn pin.	When a framing error occurs, a break can be detected by reading the RXDn pin level directly or reading the SPTR.RXDMON flag.

Item		SH7216 Group (SCI)	RX72M (SCIg, SCIh)
	Clock source	Selectable between internal and external clock	Selectable between internal and external clock Ability to input transfer rate clock from TMR (SCI5, SCI6)
Asynchronous mode	Multi-processor communication	Yes	
	Noise cancellation	No	On-chip digital noise filter for input on RXDn pins
	Other	—	• Transmit/receive FIFO • Double-speed mode • Selectable start bit detection condition • Multi-processor communications
Clock-synchronous mode	Data length	8 bits	
	Receive error detection	Overrun error	
	Hardware flow control	No	Supported (controllable with CTSn# and RTSn# pins)
	Transmit/receive FIFO	No	• 16-stage FIFOs for transmit and receive buffers
Other		—	• Simple IIC mode • Simple SPI mode • Event link (SCI5 only) • Expanded serial mode (SCI12 only) • Bit rate modulation

2.9.2 Register Comparison

Table 2.33 is a comparative listing of the registers on the SH7216 Group and RX72M.

Guide to Symbols in "Changes" Column of Table

◎: Register with same bit assignments on SH7216 Group and RX72M

△: Register with different bit assignments on SH7216 Group and RX72M

—: Register not present on SH7216 Group or RX72M

Table 2.33 SH7216 Group and RX72M Register Comparison (SCI)

SH7216 Group (SCI)*1	RX72M (SCIh, SCIi, SCIj)*2	Changes
Transmit data register n (SCTDR_n)	Transmit data register (SCIm.TDR)	◎
Transmit shift register (SCTSR)	Transmit shift register (TSR)	◎
Receive data register n (SCRDR_n)	Receive data register (SCIm.RDR)	◎
Receive shift register (SCRSR)	Receive shift register (RSR)	◎
Serial mode register n (SCSMR_n)	Serial mode register (SCIm.SMR)	◎
Serial control register n (SCSCR_n)	Serial control register (SCIm.SCR)	◎
Serial status register n (SCSSR_n)	Serial status register (SCIm.SSR/SSRFIFO)	◎
Bit rate register n (SCBRR_n)	Bit rate register (SCIm.BRR)	◎
Serial direction control register n (SCSDCR_n)	Smartcard mode register (SCIm.SCMR)	△
Serial port register n (SCSPTR_n)	—	—
—	Receive data register HL (SCIm.RDRHL)	—
	Receive FIFO data register (FRDR)	
	Transmit data register H (TDRH)	
	Transmit data register L (TDRL)	
	Transmit data register HL (SCIm.TDRHL)	
	Transmit FIFO data register(FTDR)	
	Modulation duty register (SCIm.MDDR)	
	Serial extended mode register (SCIm.SEMR)	
	Noise filter setting register (SCIm.SNFR)	
	I^2C mode registers 1 to 3 (SCIm.SIMR1 to SCIm.SIMR3)	
	I^2C status register (SCIm.SISR)	
	SPI mode register (SCIm.SPMR)	
	Receive FIFO data register（SCIp,FRDR）	
	Transmit FIFO data register（SCIp,FTDR）	
	FIFO control register (SCIp, FCR)	
	FIFO data count register (SCIp, FDR)	
	Line status register（SCIp,LSR）	
	Comparison data register（SCIq,CDR）	
	Data comparison control register（SCIq,DCCR）	
	Serial port register（SCIq,SPTR）	
	Extended serial mode enable register (SCI12.ESMER)	
	Control registers 0 to 3 (SCI12.CR0 to SCI12.CR3)	
	Port control register (SCI12.PCR)	
	Interrupt control register (SCI12.ICR)	
	Status register (SCI12.STR)	
	Status clear register (SCI12.STCR)	
	Control field 0 data register (SCI12.CF0DR)	

SH7216 Group (SCI)*1	RX72M (SCIh, SCIi, SCIj)*2	Changes
	Control field 0 compare enable register (SCI12.CF0CR)	
	Control field 0 receive data register (SCI12.CF0RR)	
	Primary control field 1 data register (SCI12.PCF1DR)	
	Secondary control field 1 data register (SCI12.SCF1DR)	
	Control field 1 compare enable register (SCI12.CF1CR)	
	Control field 1 receive data register (SCI12.CF1RR)	
	Timer control register (SCI12.TCR)	
	Timer mode register (SCI12.TMR)	
	Timer prescaler register (SCI12.TPRE)	
	Timer count register (SCI12.TCNT)	

Note 1. SCI n: 0 to 2, 4
Note 2. SCI m: 0 , 12
Note 3. SCI p：7 to 11
Note 4. SCI q：0 to 11

2.9.3 Clock Source Selection

TMR clock input (SCI5, SCI6, or SIC12 only) may be selected as the clock source for asynchronous mode communication on the RX72M. Also, whereas on the SH7216 Group a 16-bit clock is fixed as the base clock for one bit period, on the RX72M an 8-bit or 16-bit clock can be selected.

2.9.4 Interrupts

Whereas on the SH7216 Group a receive data-full or transmit data-empty interrupt can be used to activate the DTC only, on the RX72M these interrupts can be used to activate both the DTC and the DMAC.

On the RX72M when a receive data-full or transmit data-empty interrupt occurs while the corresponding interrupt status flag (IRn.IR) is set to 1, the interrupt request is also stored internally by the module, and after the interrupt status flag (IRn.IR) is cleared to 0 it is reset to 1 by the stored request.

On the RX72M some interrupts are assigned to group interrupt BL0. The interrupt controller's interrupt status flag (IRn.IR) is cleared automatically when the corresponding interrupt is accepted. Group BL0 interrupt status flag (GRPBL0.ISn) is cleared automatically when the corresponding bit in the module's status register is cleared.

Table 2.34 lists interrupt sources for the SH7216 Group and RX72M.

Refer to 1.8, Interrupt Handling for information about interrupts.

Table 2.34 SCI Interrupt Sources

		Activation by Interrupt	
Priority	Interrupt Source	SH7216 Group	RX72M
High	Receive error	Not possible	Not possible
▲	Receive data-full	DTC activation possible	DMAC and DTC activation possible
|	Transmit data-empty		
Low	Transmit end	Not possible	Not possible

2.9.5 Module Stop

As on the SH7216 Group, the SCIh, SCIi, and SCIj of the RX72M is set to the module-stop state after a reset and no clock is supplied.

Refer to 2.20, Low Power Consumption Function for information on the module-stop state.

2.10 Serial Communications Interface with FIFO (SCIF)

2.10.1 Comparison of Specifications

The serial communications interface with FIFO functionality is provided on the SH7216 Group by the SCIF and on the RX72M by the SCIi.

Table 2.35 provides a comparative listing of the specifications of the SH7216 Group and RX72M.

Table 2.35 Comparison of SH7216 Group and RX72M Specifications (SCIF)

Item		SH7216 Group (SCIF)	RX72M (SCIi)
Clock source		Peripheral clock (Pϕ)	Peripheral module clock (PCLKA)
Serial communication mode		• Asynchronous • Clock-synchronous	
Transfer speed		Any bit rate may be selected using the on-chip baud rate generator.	
Full-duplex communication		Continuous transmit and receive operation possible using 16-stage FIFO buffering	
Data transfer		LSB-first	Selectable between LSB-first and MSB-first
DTC/DMAC control		DTC/DMAC control supported	
Interrupt Source		• Transmit FIFO data-empty • Break • Receive FIFO data-full • Receive error	• Transmit FIFO data-empty • Break • Receive FIFO data-full • Receive error • Transmit-end • Receive data-ready
Asynchronous mode	Data length	7 bits, 8 bits	7 bits, 8 bits,9 bits
	Stop bits	1 bit, 2 bits	
	Parity function	Even parity, odd parity, or no parity	
	Receive error detection	Parity error, overrun error, flaming error	
	Hardware flow control	No	Supported (controllable with CTSn# and RTSn# pins)
	Break detection	Break detection is possible. Also, framing errors can be detected by reading the level of the RXDn pin directly.	Break detection is possible.
	Clock source	Selectable between internal and external clock	
	Noise cancellation	No	On-chip digital noise filter for input on RXDn pins
Clock-synchronous mode	Data length	8 bits	
	Receive error detection	Overrun error	
	Hardware flow control	No	Supported (controllable with CTSn# and RTSn# pins)
Other		—	Bit rate modulation

2.10.2 Register Comparison

Table 2.36 is a comparative listing of the registers on the SH7216 Group and RX72M.

Guide to Symbols in "Changes" Column of Table

◎: Register with same bit assignments on SH7216 Group and RX72M

△: Register with different bit assignments on SH7216 Group and RX72M

—: Register not present on SH7216 Group or RX72M

Table 2.36 SH7216 Group and RX72M Register Comparison (SCIF)

SH7216 Group (SCIF)*1	RX72M (SCIi)*2	Changes
Transmit FIFO data register n (SCFTDR_n)	Transmit FIFO data register (SCIFAm.FTDR)	◎
Transmit shift register (SCTSR)	Transmit shift register (TSR)	◎
Receive FIFO data register n (SCFRDR_n)	Receive FIFO data register (SCIFAm.FRDR)	◎
Receive shift register (SCRSR)	Receive shift register (RSR)	◎
Serial mode register n (SCSMR_n)	Serial mode register (SCIFAm.SMR)	◎
Serial control register n (SCSCR_n)	Serial control register (SCIFAm.SCR)	◎
Serial status register n (SCFSR_n)	Line status register (SCIFAm.LSR)	△
Bit rate register n (SCBRR_n)	Bit rate register (SCIFAm.BRR)	◎
Serial port register n (SCSPTR_n)	Serial port register (SCIFAm.SPTR)	◎
FIFO control register n (SCFCR_n)	FIFO control register (SCIFAm.FCR)	◎
FIFO data count register n (SCFDR_n)	FIFO data count register (SCIFAm.FDR)	◎
Line status register n (SCLSR_n)	Line status register (SCIFAm.LSR)	◎
Serial extended mode register n (SCSEMR_n)	Serial extended mode register (SCIFAm.SEMR)	△
—	Modulation duty register (SCIFAm.MDDR)	—

Note 1. SCI n: 3

Note 2. SCI m: 8 to 11

2.10.3 Interrupts

On both the SH7216 Group and the RX72M the receive FIFO data-full and transmit FIFO data-empty interrupts can be used to activate the DTC and DMAC.

On the RX72M some interrupts are assigned to group interrupt AL0. The interrupt controller's interrupt status flag (IRn.IR) is cleared automatically when the corresponding interrupt is accepted. Group AL0 interrupt status flag (GRPAL0.ISn) is cleared automatically when the corresponding bit in the module's status register is cleared.

Table 2.37 lists interrupt sources on the SH7216 Group, and Table 2.38 lists interrupt sources on the RX72M.

Refer to 1.9, Interrupt Handling for information about interrupts.

Table 2.37 SCIF Interrupt Sources on SH7216 Group

Interrupt Source	Activation by Interrupt	Priority
Break or overrun	Not possible	High
Receive error		↑
Receive FIFO data-full or receive data-ready	DMAC and DTC activation possible	
Transmit FIFO data-empty		Low

Table 2.38 SCIFA Interrupt Sources on RX72M

Interrupt Source	Activation by Interrupt
Receive error	Not possible
Receive FIFO full	DMAC and DTC activation possible
Receive data-ready	
Date mach	
Transmit FIFO empty	
Transmit-end	Not possible

2.10.4 Module Stop

As on the SH7216 Group, the SCIFA of the RX72M is set to the module-stop state after a reset and no clock is supplied.

Refer to 2.20, Low Power Consumption Function for information on the module-stop state.

2.11 Serial Peripheral Interface (RSPIc)

2.11.1 Comparison of Specifications

Serial peripheral interface functionality is provided on the SH7216 Group by the RSPI and on the RX72M by the RSPIc.

Table 2.39 presents a comparison of the specifications of the SH7216 Group and RX72M.

Table 2.39 Comparison of SH7216 Group and RX72M Specifications (RSPI)

Item	SH7216 Group (RSPI)	RX72M (RSPIc)
Clock sources	Peripheral clock (Pϕ) External clock (RSPCK)	Peripheral module clock (PCLKA) External clock (RSPCK)
Transmit/receive data length	8 to 16, 20, 24, or 32 bits	
Transfer operation	SPI (4-wire method) Clock-synchronous communication (3-wire method)	
Data format	Selectable between MSB-first and LSB-first	
Clock phase/polarity	Variable	
SSL polarity	Variable	
Operating modes	• Master transmit mode • Master receive mode • Slave transmit mode • Slave receive mode	
Communication operating mode	Full-duplex communication	Selectable between full duplex and transmit only
Multi-master support	Yes	
Sequence control	Sequence length: 4	Sequence length: 8
Loopback mode	Data inverted	Ability to select data inversion
DTC/DMAC activation	DTC/DMAC activation supported	
Interrupt sources	• Transmit buffer-empty • Receive buffer-full • Overrun error • Mode fault error	• Transmit buffer-empty • Receive buffer-full • RSPI idle • Overrun error • Underrun error • Parity error • Mode fault error
Other	—	• Event link • Parity bit addition

2.11.2 Register Comparison

Table 2.40 is a comparative listing of the registers on the SH7216 Group and RX72M.

Guide to Symbols in "Changes" Column of Table

◎: Register with same bit assignments on SH7216 Group and RX72M

△: Register with different bit assignments on SH7216 Group and RX72M

—: Register not present on SH7216 Group or RX72M

Table 2.40 SH7216 Group and RX72M Register Comparison (RSPI)

SH7216 Group (RSPI)	RX72M (RSPIa)*1	Changes
RSPI control register (SPCR)	RSPI control register (RSPIn.SPCR)	◎
RSPI pin control register (SPPCR)*2	RSPI pin control register (RSPIn.SPPCR)	△
RSPI command registers 0 to 3 (SPCMD0 to SPCMD3)	RSPI command registers 0 to 7 (RSPIn.SPCMD0 to RSPIn.SPCMD7)	◎
RSPI bit rate register (SPBR)	RSPI bit rate register (RSPIn.SPBR)	◎
RSPI status register (SPSR)	RSPI status register (RSPIn.SPSR)	△
RSPI data register (SPDR)	RSPI data register (RSPIn.SPDR)	△
RSPI data control register (SPDCR)	RSPI data control register (RSPIn.SPDCR)	◎
RSPI slave select polarity register (SSLP)	RSPI slave select polarity register (RSPIn.SSLP)	◎
RSPI sequence control register (SPSCR)	RSPI sequence control register (RSPIn. SPSCR)	△
RSPI sequence status register (SPSSR)	RSPI sequence status register (RSPIn.SPSSR)	△
SPI slave select negation delay register (SSLND)	RSPI slave select negation delay register (RSPIn.SSLND)	◎
RSPI clock delay register (SPCKD)	RSPI clock delay register (RSPIn.SPCKD)	◎
RSPI next-access delay register (SPND)	RSPI next-access delay register (RSPIn.SPND)	◎
—	RSPI control register 2 (RSPIn.SPCR2)	—
—	RSPI data control register 2 (RSPIn.SPDCR2)	

Note 1. RSPIn n: 0

Note 2. RSPI output pin mode setting is accomplished using the I/O port function on the RX72M.

2.11.3 Interrupts

On both the SH7216 Group and RX72M the receive buffer-full and transmit buffer-empty interrupts can be used to activate the DTC and DMAC.

On the RX72M an interrupt request generated while the receive buffer-full or transmit buffer-empty interrupt status flag (IRn.IR) is set to 1 is stored internally by the module, and after the interrupt status flag (IRn.IR) is cleared to 0 it is once again set to 1 by the stored request.

On the RX72M some interrupts are assigned to group interrupt AL0. The interrupt controller's interrupt status flag (IRn.IR) is cleared automatically when the corresponding interrupt is accepted. The group AL0 interrupt status flag (GRPAL0.ISn) is cleared automatically when the corresponding bit in the module's status register is cleared.

Refer to 1.8, Interrupt Handling for information about interrupts.

2.11.4 Module Stop

The RSPIc of the RX72M, like the SSU of the SH7216 Group, is set to the module-stop state after a reset, and no clock is supplied.

Refer to 2.20, Low Power Consumption Function for information on the module-stop state.

2.12 I²C Bus Interface (RIICa)

2.12.1 Comparison of Specifications

I²C bus interface functionality is provided on the SH7216 Group by the IIC3 and on the RX72M by the RIICa, which supports communication operation compliant with SMBus (ver. 2.0).

Table 2.41 is a comparative listing of the specifications of the SH7216 Group and RX72M.

Table 2.41 Comparison of SH7216 Group and RX72M Specifications (IIC)

Item		SH7216 Group (IIC3)	RX72M (RIICa)
Number of channels		1 channel	3 channels
Clock source		Peripheral clock (Pϕ)	Peripheral module clock (PCLKB)
Communication format		• I²C bus format • Clock-synchronous serial format*1	• I²C bus format • SMBus format
Data transfer		Fixed at MSB-first MSB-first and LSB-first can be selected for the clock-synchronous serial format	Fixed at MSB-first Supports SCI clock synchronization
I²C bus format (SMBus)	Operating modes	• Master transmit/receive mode • Slave transmit/receive mode	
	Start condition/ stop condition	Automatically generated	
	Address detection	• 7-bit slave addresses	• Supports 7- or 10-bit slave addresses • General call address detection • Device ID address detection • SMBus host address detection
	DTC/DMAC activation	DTC activation supported	DTC/DMAC activation supported
	Interrupt sources	• Arbitration lost • NACK detection • Stop condition detection • Receive data-full • Transmit data-empty • Transmit end	• Arbitration lost detection • NACK detection • — • Receive data-full • Transmit data-empty • Transmit end • Timeout detection • Start condition detection • Stop condition detection
	Multi-master support	Bit synchronization circuit Ability to specify a transfer rate at least 1/1.8 times the fastest transfer rate of another master	SCL synchronization circuit
Noise cancellation		Ability to specify the noise cancellation width for the SCL and SDA pins Up to 3-stage latch circuit	On-chip digital noise filter in SCL and SDA pins, noise cancellation width can be adjusted Up to 5-stage latch circuit
Other		—	• Event link function • SCL clock duty ratio setting • SDA output delay function • SCL auto low-hold function • Bus hang-up support

Note 1. The RIICa on the RX72M does not support clock-synchronous serial format, but the clock-synchronous communication format of the SCIi , SCIj and SCIh can be used as a substitute.

2.12.2 Register Comparison

Table 2.42 is a comparative listing of the registers on the SH7216 Group and RX72M.

Guide to Symbols in "Changes" Column of Table

◎: Register with same bit assignments on SH7216 Group and RX72M

△: Register with different bit assignments on SH7216 Group and RX72M

—: Register not present on SH7216 Group or RX72M

Table 2.42 SH7216 Group and RX72M Register Comparison (IIC)

SH7216 Group (IIC3)	RX72M (RIICa)*1	Changes
I²C bus control register 1 (ICCR1)	I²C bus control register 1 (RIICn.ICCR1)	△
I²C bus control register 2 (ICCR2)	I²C bus control register 2 (RIICn.ICCR2)	
I²C bus mode register (ICMR)	I²C bus mode register 1 (RIICn.ICMR1)	△
I²C bus interrupt enable register (ICIER)	I²C bus mode register 3 (RIICn.ICMR3)*2	△
	I²C bus interrupt enable register (RIICn.ICIER)	
	I²C bus function enable register (RIICn.ICFER)	
I²C bus status register (ICSR)	I²C bus status register 1 (RIICn.ICSR1)	△
	I²C bus status register 2 (RIICn.ICSR2)	
Slave address register (SAR)	Slave address register Ly (RIICn.SARLy) (y = 0 to 2)	△
	I²C bus mode register 3 (RIICn.ICMR3)*2	
I²C bus transmit data register (ICDRT)	I²C bus transmit data register (RIICn.ICDRT)	◎
I²C bus receive data register (ICDRR)	I²C bus receive data register (RIICn.ICDRR)	◎
I²C bus shift register (ICDRS)	I²C bus shift register (ICDRS)	◎
NF2CYC register (NF2CYC)	I²C bus mode register 3 (RIICn.ICMR3)*2	△
—	I²C bus mode register 2 (RIICn.ICMR2)	—
	Slave address register Uy (RIICn.SARUy) (y = 0 to 2)	
	I²C bus bit rate low-level register (RIICn.ICBRL)	
	I²C bus bit rate high-level register (RIICn.ICBRH)	
	I²C bus status enable register (RIICn.ICSER)	

Note 1. RIICn, n: 0 or 2

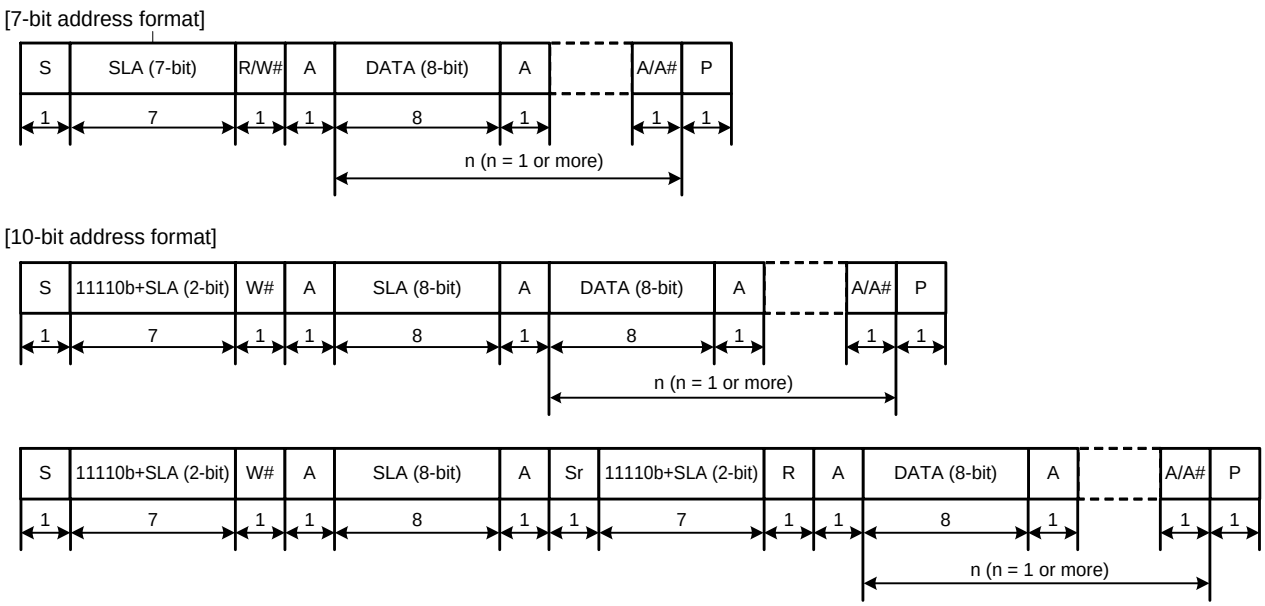
Note 2. The functions of some registers on the SH7216 Group are divided among multiple registers on the RX72M.

2.12.3 Address Detection

The SH7216 Group can detect 7-bit slave addresses of a single type.

The RX72M can detect three types of slave addresses, as well as general call addresses, device ID addresses, and SMBus host addresses. In addition, the slave address bit count can be specified as either 7-bit or 10-bit.

Figure 2.15 shows the RX72M I²C bus format.



n: Transfer data byte count
S: Start condition
SLA: Slave address
R/W#: Transmit/receive direction
A: Acknowledge
A#: Not acknowledge
Sr: Restart condition
DATA: Transmit/receive data
P: Stop condition

Figure 2.15 RX72M I2C Bus Format

2.12.4 Arbitration Lost Detection

In addition to the ordinary arbitration lost detection function stipulated in the I²C bus specification, the RX72M provides functions for prevention of issuance of overlapping start requests, arbitration lost detection during NACK transmission, and arbitration lost detection during slave receive operation.

2.12.5 Bus Hang-up

If synchronization of the master device and slave device on the I²C bus is disrupted due to noise or the like, a bus hang-up may occur where the SCL line or SDA line becomes fixed at a single level.

To deal with bus hang-ups, the RX72M provides a timeout detection function that monitors the SCL line to detect bus hang-up states and, to recover from bus hang-up states caused by disrupted synchronization, an SCL clock additional output function, an RIIC reset function, and an internal reset function.

2.12.6 SCL Clock

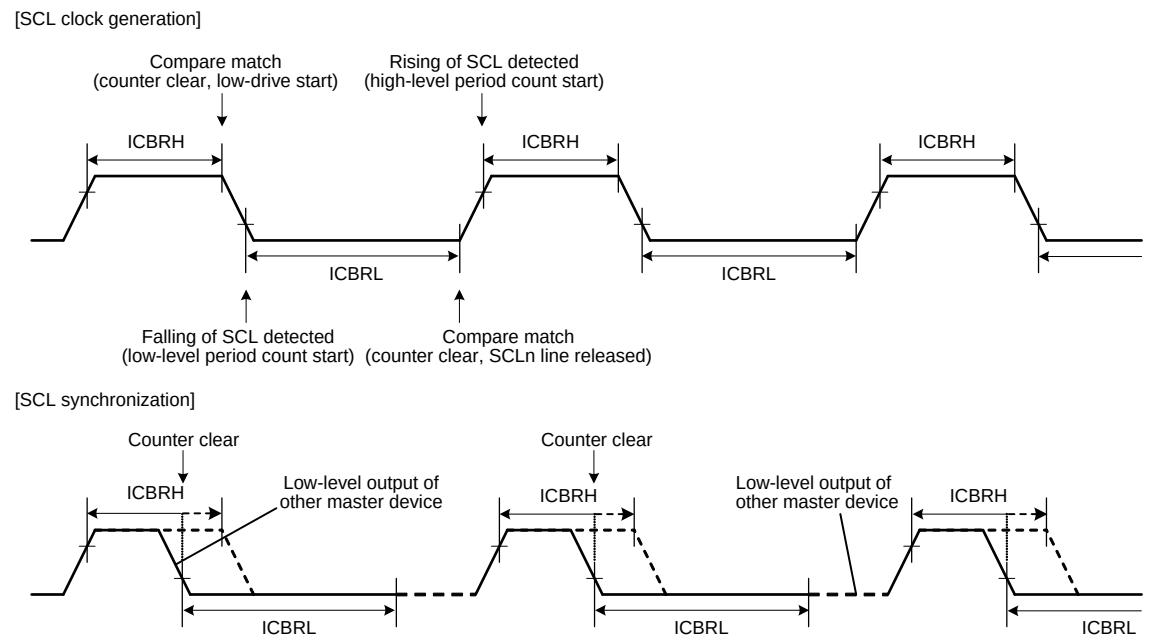
Under the I²C bus format transmission and reception of data are synchronized with the SCL clock output by the master device.

When operating in master mode, the SCL clock transfer rate on the SH7216 Group is determined by the peripheral clock division ratio setting in I²C bus control register 1 (ICCR1). On the RX72M the SCL transfer rate and duty ratio are determined by the SCL clock high-level period setting in the I²C bus bit rate high-level register (ICBRH) and the SCL clock low-level setting in the I²C bus bit rate low-level register (ICBRL).

The RX72M provides a transmit data accidental transmission prevention function, a NACK receive transfer cutoff function, and a receive data loss prevention function. The SCL line is automatically held low when certain conditions are met.

When the I²C bus format is used in a multi-master configuration, conflicts can arise between the SCL clock that that of the other master device. This is why the SH7216 Group is provided with a bit synchronization circuit, and the RX72M with an SCL synchronization circuit, that monitors the SCLn line in master mode and generates the SCL clock with bit-by-bit synchronization.

Figure 2.16 illustrates SCL clock generation and SCL synchronization on the RX72M.



ICBRH: I²C-bus bit rate high-level register (SCL clock high-level period counter)
ICBRL: I²C-bus bit rate low-level register (SCL clock low-level period counter)

Figure 2.16 SCL Clock Generation and SCL Synchronization

2.12.7 Noise Cancellation

In addition to a setting for the noise cancellation width, on the RX72M it is possible to enable or disable the digital noise filter circuit by making a setting in the I²C-bus function enable register (ICFER).

2.12.8 Interrupts

On both the SH7216 Group and RX72M the receive data-full and transmit data-empty interrupts can be used to activate the DTC and the DMAC.

On the RX72M when a receive data-full or transmit data-empty interrupt occurs while the corresponding interrupt status flag (IRn.IR) is set to 1, the interrupt request is also stored internally by the module, and after the interrupt status flag (IRn.IR) is cleared to 0 it is reset to 1 by the stored request.

On the RX72M some interrupts are assigned to group interrupt BL1. The interrupt controller's interrupt status flag (IRn.IR) is cleared automatically when the corresponding interrupt is accepted. The group BL1 interrupt status flag (GRPBL1.ISn) is cleared automatically when the corresponding bit in the module's status register is cleared.

Table 2.43 and Table 2.44 list interrupt sources for the SH7216 Group and RX72M.

Refer to 1.8, Interrupt Handling for information about interrupts.

Table 2.43 SH7216 Group IIC3 Interrupt Sources (I2C Bus Format)

Priority	Interrupt Source	Activation by Interrupt
High ↑	Stop condition detection	Not possible
	NACK detection Arbitration lost/overrun error	
	Receive data-full	DMAC and DTC activation possible
	Transmit data-empty	
Low	Transmit end	Not possible

Table 2.44 RX72M RIICa Interrupt Sources

Priority	Interrupt Source		Activation by Interrupt
High ↑	Communication error/ event occurrence	Arbitration lost	Not possible
		NACK detection	
		Timeout	
		Start condition detection	
		Stop condition detection	
	Receive data-full		DMAC and DTC activation possible
	Transmit data-empty		
Low	Transmit end		Not possible

2.12.9 Module Stop

As on the SH7216 Group, the RIICa of the RX72M is set to the module-stop state after a reset, and no clock is supplied.

Refer to 2.20, Low Power Consumption Function for information on the module-stop state.

2.13 A/D Converter (S12ADFa)

2.13.1 Comparison of Specifications

As an A / D converter, the SH7216 group has an ADC and the RX72M has a on-chip 12-bit A / D converter (S12ADCFa).

Table 2.45 is a comparative specification of the SH7216 Group and RX72M.

Table 2.45 Comparison of SH7216 Group and RX72M Specifications (ADC)

Item	SH7216 Group (ADC)	RX72M (S12ADCFa)
Number of input channels	8 channels (4 channels × 2)	Unit 0 (S12AD): 8 channels Unit 1 (S12AD1): 21 channels +1extensions
Clock source	AD clock (Aϕ)	S12AD: Peripheral module clock (PCLKC) S12AD1: Peripheral module clock (PCLKD)
Resolution	12 bits	Max. 12 bits (selectable among 8, 10, and 12 bits)
A/D conversion method	Successive approximation	Successive approximation
Conversion speed	1.0 μs per 1channel (AD clock: 25 MHz)	Per 1channel 12-bit conversion mode: 0.48 μs 10-bit conversion mode: 0.45 μs 8-bit conversion mode: 0.42 μs (A / D conversion clock ADCLK = 60MHz operation)
Conversion modes	• Single-cycle scan mode • Continuous scan mode	• Single scan mode • Continuous scan mode • Group scan mode
A/D conversion start conditions	• Software trigger • Synchronous trigger (MTU2, MTU2S) • Asynchronous trigger (ADTRG pin)	• Software trigger • Synchronous trigger (MTU, TMR, TPU, ELC) • Asynchronous trigger (ADTRG0# pin, ADTRG1# pin)
Operations linked to A/D conversion-end interrupt	• CPU interrupt generation • DMAC or DTC activation	• CPU interrupt generation • DMAC or DTC activation
Conversion targets	• AN pin	• AN pin • Internal reference voltage (S12AD1) • Temperature sensor (S12AD1)
DTC/DMAC activation	DTC/DMAC activation supported	DTC/DMAC activation supported
Interrupt sources	• A/D conversion end	• A/D conversion end • Digital compare
Other	• Sample and hold function • Channel-specific Sample-and-hold function (module 0) • A/D data register auto-clear function	• Event link

	• Sample and hold function • Channel-specific Sample-and-hold function (S12AD) • Variable sampling state count function • A/D converter self-diagnostic function • Selectable between A/D-converted value addition mode or average mode • Analog input disconnection detection assist function • Double trigger mode • 12-/10-/8-bit conversion switching • A/D data register auto-clear function • Extended analog input function • Comparison function (ability to select window function)

2.13.2 Input Channels

On the SH7216 Group the ADC comprises two modules, each of which has four analog input channels. On the RX72M the S12ADC comprises two units, S12AD and S12AD1, one with eight channels and the other with 21 channels. As on the SH7216 Group, on the RX72M each unit incorporates an A/D converter. Simultaneous operation is possible, but continuous scan operation spanning the two units is not supported.

Figure 2.17 compares the A/D converter configurations of the SH7216 Group and RX72M.

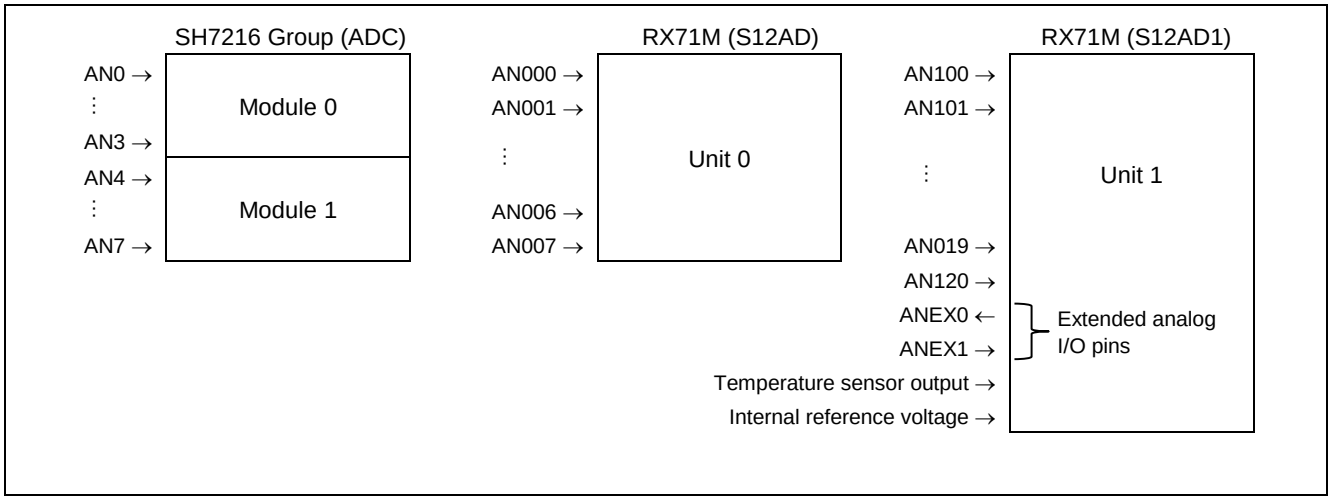


Figure 2.17 Comparison of A/D Converter Configurations

2.13.3 Scanning Sequence

Table 2.46 lists the scanning sequence when all channels are specified.

Table 2.46 A/D Converter Scanning Sequence

Microcontroller	A/D Converter	Conversion Sequence
SH7216 Group	ADC (module 0)	AN0 ⇒ AN1 ⇒ AN2 ⇒ AN3
	ADC (module 1)	AN4 ⇒ AN5 ⇒ AN6 ⇒ AN7
RX72M	S12AD	AN0 ⇒ AN1 ⇒ omitted ⇒ AN6 ⇒ AN7 ⇒ Temperature sensor output ⇒ Internal reference voltage It is possible to select group A priority control for group scan operation.
	S12AD1	AN100 ⇒ AN101 ⇒ omitted ⇒ AN119 ⇒ AN120 ⇒Temperature sensor output ⇒ Internal reference voltage It is possible to select group A priority control for group scan operation.

2.13.4 Operating Modes

Table 2.47 lists correspondences between the operating modes of the SH7216 Group and RX72M.

Table 2.47 Correspondences between A/D Converter Operating Modes

SH7216 Group	RX72M
Single-cycle scan	Single scan mode
Continuous scan	Continuous scan mode
—	Group scan mode When the specified synchronous trigger occurs, A/D conversion is performed once each on the multiple channels specified for each group. After A/D conversion completes for each group, an interrupt is generated if interrupts have been enabled.

2.13.5 Interrupts

ADC interrupts can be used to activate the DTC and DMAC on both the SH7216 Group and the RX72M.

On the RX72M the S12ADFa interrupts are assigned to group interrupt BL1 and to software configurable interrupt B. The group BL1 interrupt status flag (GRPBL1.ISn) is cleared automatically when the corresponding bit in the module's status register is cleared. The software configurable interrupt B status flag (PIBRk.PIRn) is not cleared automatically, but there is no effect on the generation of interrupt requests.

Refer to 1.8, Interrupt Handling for information about interrupts.

2.13.6 Module Stop

As on the SH7216 Group, the S12ADFa of the RX72M is set to the module-stop state after a reset, and no clock is supplied.

Refer to 2.20, Low Power Consumption Function for information on the module-stop state.

2.14 CAN

2.14.1 Comparison of Specifications

Controller area network functionality is provided on the SH7216 Group by the RCAN-ET module and on the RX72M by the CAN module (CAN).

Table 2.48 is a comparative specification of the SH7216 Group and RX72M.

Table 2.48 Comparison of SH7216 Group and RX72M Specifications (CAN)

Item	SH7216 Group (RCAN-ET)	RX72M (CAN)
Number of channels	1 channel	3 channels
Protocol	Support for CAN standard 2.0B ISO-11898 compliant bit timing	ISO 11898-1 compliant
Clock source	Peripheral bus clock (Pϕ) 20 to 50 MHz	Peripheral module clock (PCLKB) or CAN clock (CANMCLK)
Bit rate	Max. 1 Mbps	Max. 1 Mbps
Mailboxes per channel	(Equivalent to normal mailbox mode on RX72M) Transmit/receive: 15 Receive: 1	Normal mailbox mode • Transmit/receive: 32 FIFO mailbox mode • Transmit/receive: 24 • Transmit: 4-stage FIFO • Receive: 4-stage FIFO
Supported ID selection	• Both standard ID and extended ID	• Standard ID • Extended ID • Both standard ID and extended ID
Test functions	• Listen-only mode • Self-test mode 1 (external) • Self-test mode 2 (internal) • Write error counter • Error-passive mode	• Listen-only mode • Self-test mode 0 (external) • Self-test mode 1 (internal) • — • —
DTC/DMAC activation	DTC/DMAC activation supported	—
Interrupt source	• Data frame receive • Remote frame receive • Message transmit/transmit cancel • 2 error systems	• Receive-end • Transmit-end • Receive FIFO • Transmit FIFO • Error
Other	• HCAN2-compatible ID rearrangement • Auto-wakeup from CAN sleep mode • Auto-transmit of data frames • Acceptance filter	• — • — • — • Acceptance filter support • Time stamp function • One-shot receive • Mailbox search support • Channel search support

2.14.2 Mailboxes

The SH7216 Group has 16 mailboxes, each comprising 18 bytes. Figure 2.18 shows the mailbox configuration on the SH7216 Group.

- Mailbox 0: Receive-only mailbox
- Mailboxes 1 to 15: Transmit/receive mailboxes

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IDE	RTR	0	STDID[10:0]											EXTID[17:16]	
EXTID[15:0]															
IDE_ LAFM	0	0	STDID_LAFM[10:0]											EXTID_ LAFM[17:16]	
EXTID_LAFM[15:0]															
MSG_DATA_0								MSG_DATA_1							
MSG_DATA_2								MSG_DATA_3							
MSG_DATA_4								MSG_DATA_5							
MSG_DATA_6								MSG_DATA_7							
0	0	NMC	ATX*1	DART*1	MBC[2:0]			0	0	0	0	DLC[3:0]			

Note 1. ATX and DART are not supported by mailbox 0.

Figure 2.18 SH7216 Group Mailbox Configuration

The SH71M has 32 mailboxes, each comprising 16 bytes. Figure 2.19 shows the mailbox configuration on the RX72M.

Normal mailbox mode

- Mailboxes 0 to 31: Transmit/receive mailboxes

FIFO mailbox mode

- Mailboxes 0 to 23: Transmit/receive mailboxes
- Mailboxes 24 to 27: Mailboxes for transmit FIFO
- Mailboxes 28 to 31: Mailboxes for receive FIFO

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IDE	RTR	—	SID[10:0]											EID[17:16]	
EID[15:0]															
—	—	—	—	—	—	—	—	—	—	—	—	DLC[3:0]			
DATA_0								DATA_1							
DATA_2								DATA_3							
DATA_4								DATA_5							
DATA_6								DATA_7							
TSH[7:0]								TSL[7:0]							

Figure 2.19 RX72M Mailbox Configuration

Some mailbox items on the SH7216 Group are accomplished on the RX72M by means of register settings. Table 2.49 compares mailbox settings on the SH7216 Group and the RX72M.

Guide to Symbols in "Changes" Column of Table

◎: Same setting on SH7216 Group and RX72M

△: Different setting on SH7216 Group and RX72M

—: Register not present on SH7216 Group or RX72M

Table 2.49 Comparison of Mailbox Settings on SH7216 Group and RX72M

SH7216 Group*1	RX72M*2	Changes
MB[x].CONTROL0.IDE	MBj.IDE	◎
MB[x].CONTROL0.RTR	MBj.RTR	◎
MB[x].CONTROL0.STDID[10:0]	MBj.SID[10:0]	◎
MB[x].CONTROL0.EXTID[17:0]	MBj.EID[17:0]	◎
MB[x].LAFM.IDE_LAFM	—	—
MB[x].LAFM.STDID_LAFM[10:0]	MKRk.SID[10:0], MKIVLR register	△
MB[x].LAFM.EXTID_LAFM[17:0]	MKRk.EID[17:0], MKIVLR register	△
MB[x].MSG_DATA[0 to 7].MSG_DATA_0 to 7	MBj.DATA0 to MBj.DATA7	◎
MB[x].CONTROL1.NMC	CTLR.MLM (channel unit)	△
MB[x].CONTROL1.ATX	—	—
MB[x].CONTROL1.DART	MCTLj.ONESHOT	△
MB[x].CONTROL1.MBC[2:0]	MCTLj.RECREQ, MCTLj.TRMREQ	△
MB[x].CONTROL1.DLC[3:0]	MBj.DLC[3:0]	◎
—	MBj.TSL[7:0] MBj.TSH[7:0]	—

Note 1. x: 0 to 15

Note 2. j: 0 to 31, k: 0 to 7

2.14.3 Acceptance Filtering

Both the SH7216 Group and RX72M support acceptance filtering, which enables mailboxes to accept messages with multiple receive IDs.

Whereas on the SH7216 Group acceptance filter settings are made to the local acceptance filter mask (LAFM) in each mailbox, on the RX72M they are made to mask register k (MKRk) and the mask invalid register (MKIVLR).

Table 2.50 Acceptance Filter Setting Specifications

Item	SH7216 Group	RX72M
Target	IDE Standard ID Extended ID	Standard ID Extended ID
Mask settings	Local acceptance filter mask (LAFM): Individual mask settings for each mailbox 0: Compare target ID bit. 1: Do not compare target ID bit.	Mask register k (MKRk): Individual mask settings for four mailboxes 0: Compare target ID bit. 1: Do not compare target ID bit. Mask invalid register (MKIVLR): Mask enable/disable settings for each mailbox

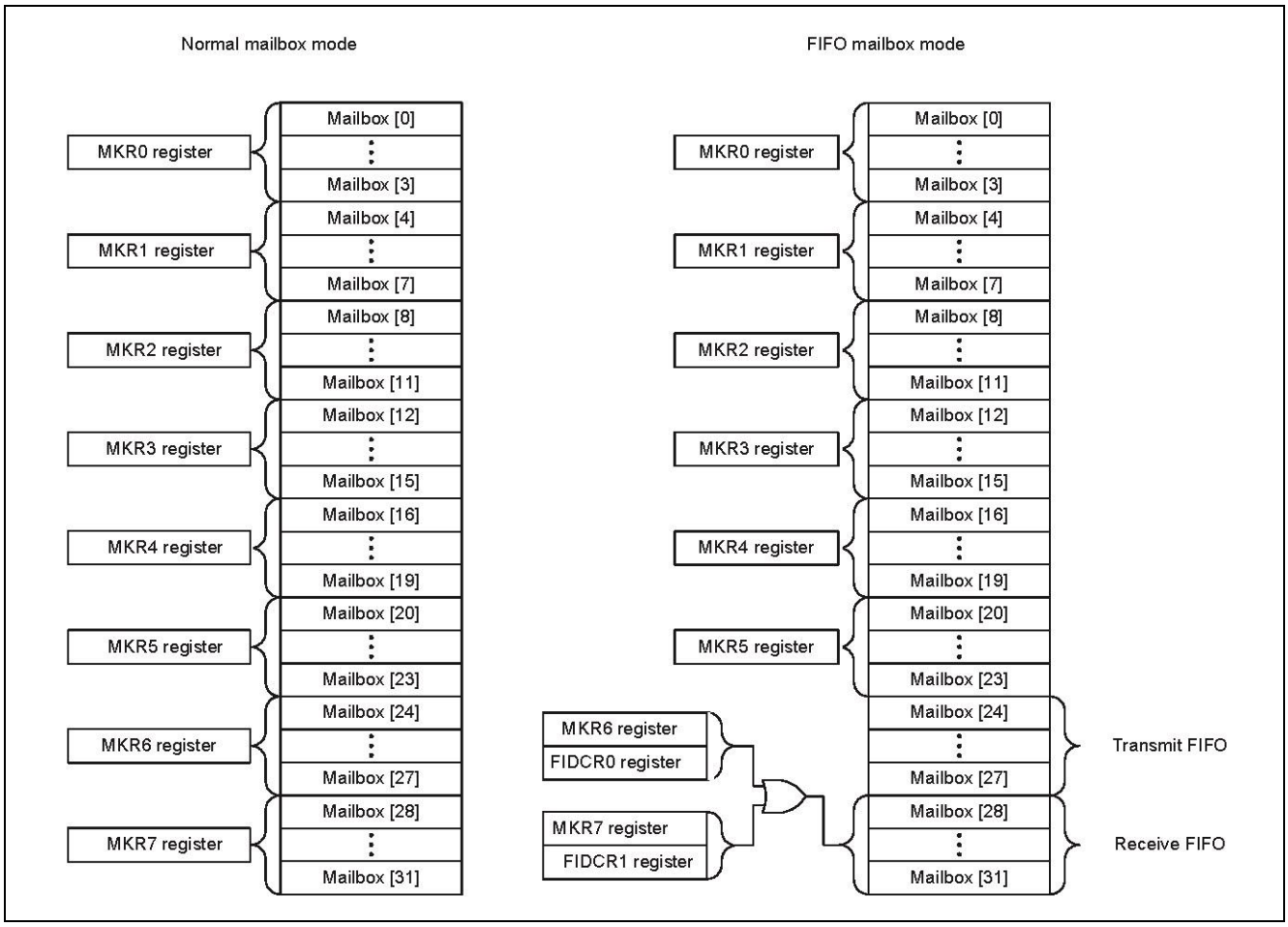


Figure 2.20 Correspondence of Mask Registers and Mailboxes on RX72M

2.14.4 Transmission Priority

On both the SH7216 Group and the RX72M it is possible to select the priority of message transmission.

The mailbox numbers and their priority when mailbox number priority mode is selected differ on the SH7216 Group and on the RX72M. Table 2.51 shows the transmission priority specifications of the SH7216 Group and the RX72M.

Table 2.51 Transmission Priority Specifications

Item	SH7216 Group	RX72M
ID priority	The message with the arbitration field having the lowest digital value has the highest priority (ISO 11898-1 compliant).	
Mailbox number priority	The highest mailbox number has the highest priority Mailbox 15 to mailbox 1	The lowest mailbox number has the highest priority Mailbox 0 to mailbox 31

2.14.5 Mode Transitions

Whereas on the SH7216 Group a transition to configuration mode occurs after a hardware reset, on the RX72M a transition to CAN sleep mode occurs.

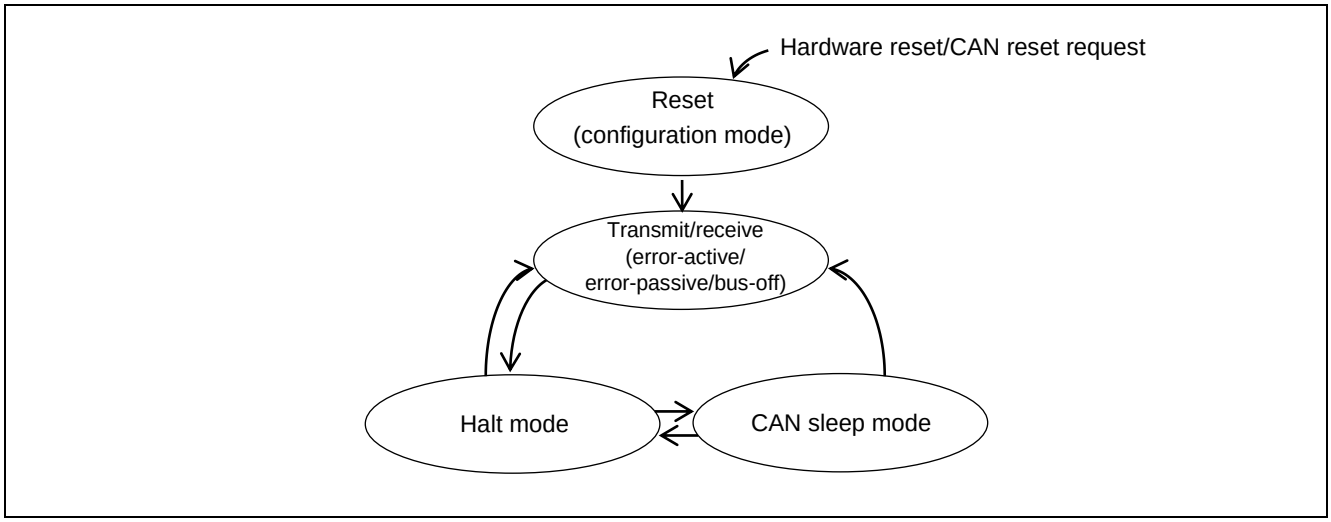


Figure 2.21 SH7216 Group State Transitions

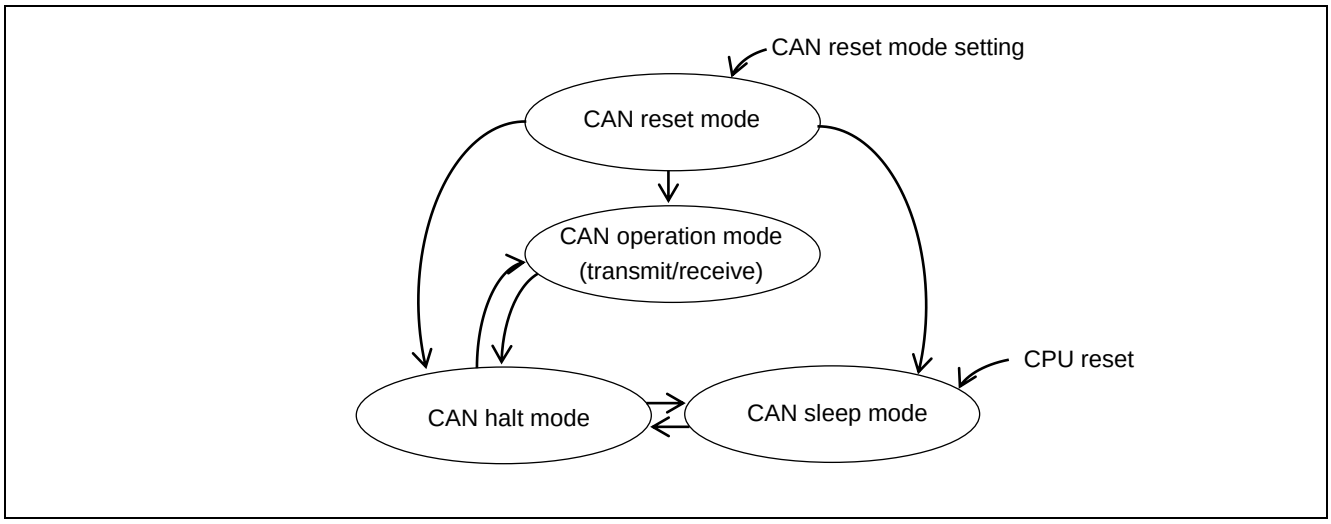


Figure 2.22 RX72M State Transitions

2.14.6 Interrupts

Whereas on the SH7216 Group a data frame receive or remote frame receive interrupt can be used to activate the DTC and the DMA, on the RX72M no CAN interrupts can be used to activate the DTC and the DMAC.

On the RX72M CAN interrupts are assigned to the group BE0 interrupt and to software configurable interrupt B. The group BE0 interrupt status flag (GRPBE0.ISn) is cleared when 1 is written to the interrupt source clear bit (GCRBE0.CLRn). The software configurable interrupt B status flag (PIBRk.PIRn) is not cleared automatically, but it has no effect on the generation of interrupt requests even if left uncleared.

Refer to 1.8, Interrupt Handling for information about interrupts.

2.14.7 Module Stop

As on the SH7216 Group, the CAN of the RX72M is set to the module-stop state after a reset, and no clock is supplied.

Refer to 2.20, Low Power Consumption Function for information on the module-stop state.

2.15 USB2.0FS Host / Function Module (USBb)

2.15.1 Comparison of Specifications

As a module compatible with USB 2.0, the SH7216 group has a built-in USB function module (USB).

The RX72M also incorporates a USB 2.0 FS Host / Function Module (USBb) that supports all transfer types defined in USB Standard 2.0.

Table 2.52 is a comparative specification of the SH7216 Group and RX72M.

Table 2.52 Comparison of SH7216 Group and RX72M Specifications (USB)

	SH7216 Group	RX72M
Item	**USB**	**USBb**
Controller functions	• Function controller function	• Host controller function • Function controller function • On-The-Go (OTG)
Clock source	USB clock (Uϕ)	Peripheral module clock (PCLKB) USB clock (UCLK)
Transfer speed	• Full-speed mode	• Low-speed mode*2 • Full-speed mode
Communication data transfer types	• Control transfer • Bulk transfer • Interrupt transfer	• Control transfer • Bulk transfer • Interrupt transfer • Isochronous transfer
Power modes	• Self-power mode	• Self-power mode • Bus-power mode
Endpoints/pipes	Endpoints: Up to 10	Pipes: Up to 10 The endpoint numbers assigned to pipes 1 to 9 are selectable.
DTC/DMAC activation	DTC/DMAC activation supported	DTC/DMAC activation supported
Other	• D+ line pull-up control pin (PUPD) • Ability to switch to low-power mode when USB cable is disconnected or internal clock for protocol processing stops	• Incorporation into MCU of D+/D− line pull-up and pull-down resistors • For USB cable disconnection monitoring, detect the cable disconnection with USB0_VBUS and stop the module • Support for following functions when function controller is selected: — Control transfer stage management function — Device state management function — SOF recovery function

Note 1. USBMCLK is supplied to the PLL incorporated into the USB-PHY of the USB, and the PHY clock generation method is selectable.

Note 2. Supported by host controller only.

2.16 Ethernet Controller (ETHERC)

2.16.1 Comparison of Specifications

Ethernet controller functionality with support for the Ethernet and IEEE 802.3 MAC layer protocol standards is provided on the SH7216 Group by the EtherC and on the RX72M by the ETHERC.

Direct memory access controller functionality for the Ethernet controller is provided on the SH7216 Group by the E-DMAC and on the RX72M by the EDMACa.

The RX72M also integrates a PTP module for the Ethernet controller (EPTPCb) to handle synchronization between devices.

Table 2.53 and Table 2.54 are comparative specifications of the SH7216 Group and RX72M.

Table 2.53 Comparison of SH7216 Group and RX72M Specifications (EtherC)

Item	SH7216 Group (EtherC)	RX72M (ETHERC)
Number of input channels	1 channel	2 channels
Protocol	Flow control compliant with IEEE 802.3x	Flow control compliant with IEEE 802.3x
Data transmission/ reception	Frame transmission/reception compliant with Ethernet/IEEE 802.3	Frame transmission/reception compliant with Ethernet/IEEE 802.3
Transfer speed	10 Mbps 100 Mbps	10 Mbps 100 Mbps
Communication mode	Full-duplex communication Half-duplex communication	Full-duplex communication Half-duplex communication
Inerface	MII compliant with IEEE 802.3u	MII and RMII compliant with IEEE 802.3u
Other	Magic Packet™*1 detection Wake-On-LAN (WOL) signal output	Magic Packet™*1 detection Wake-On-LAN (WOL) signal output

Note 1. Magic Packet is a trademark of Advanced Micro Devices, Inc.

Table 2.54 Comparison of SH7216 Group and RX72M Specifications (E-DMAC)

Item	SH7216 Group (E-DMAC)	RX72M (EDMACAa)
Number of channels	1 channel: EtherC	2 channels: ETHERC 1 channel: EPTPCb
Data transfer	Transmission/reception control using descriptors	Transmission/reception control using descriptors
Transfer methods	• Single frame transmission/reception • Multi-buffer transmission/reception	• Single-buffer frame transmission/ reception • Multi-buffer frame transmission/reception
Transfer unit	Block transfer (32-byte units)	Block transfer (32-byte units)
Other	• Reflection in descriptor of transmit/ receive frame status	• Reflection in descriptor of transmit/ receive frame status • Insertion of padding in receive data

2.17 Compare Match Timer (CMT)

2.17.1 Comparison of Specifications

Compare match timer functionality is provided on the SH7216 Group by the CMT and on the RX72M by the CMT, which has a 16-bit timer, and the CMTW, which has a 32-bit timer.

The RX72M includes all the CMT functionality of the SH7216 Group (backward compatibility). Table 2.55 provides a comparative listing of the specifications of the SH7216 Group and RX72M.

Table 2.55 Comparison of SH7216 Group and RX72M Specifications (CMT)

	SH7216 Group	RX72M	
Item	**CMT**	**CMT**	**CMTW**
Number of units (channels)	1 unit (total 2 channels)	2 units (total 4 channels)	2 units (total 2 channels)
Clock source	Internal clock (Pϕ)	Peripheral module clock (PCLKB)	Peripheral module clock (PCLKB)
Clock frequency division ratio	Pϕ/8, 32, 128, 512	PCLKB/8, 32, 128, 512	PCLKB/8, 32, 128, 512
Count operation	16-bit up-counter	16-bit up-counter	Max. 32-bit up-counter (selectable between 16 and 32 bits)
DTC/DMAC activation	DTC/DMAC activation supported	DTC/DMAC activation supported	DTC/DMAC activation supported
Interrupt sources	• Compare match	• Compare match	• Compare match • Input compare • Output compare
Other	—	Event link	Event link

2.17.2 Register Comparison

The CMT of the SH7216 and RX72M are software compatible. However, the RX72M does not have interrupt flags, but equivalent processing can be accomplished by using the interrupt controller.

Table 2.56 and Table 2.57 are a comparative listing of the registers on the SH7216 Group and RX72M.

Guide to Symbols in "Changes" Column of Table

◎: Register with same bit assignments on SH7216 Group and RX72M

△: Register with different bit assignments on SH7216 Group and RX72M

—: Register not present on SH7216 Group or RX72M

Table 2.56 SH7216 Group and RX72M Register Comparison (CMT)

SH7216 Group (CMT)*1	RX72M (CMT)*2	Changes
Compare match timer start register (CMSTR)	Compare match timer start register 0 (CMSTR0) Compare match timer start register 1 (CMSTR1)	◎
Compare match timer control/ status register n (CMCSR_n)	Compare match timer control register (CMTm.CMCR)	△
Compare match counter n (CMCNT_n)	Compare match timer counter (CMTm.CMCNT)	◎
Compare match constant register n (CMCOR_n)	Compare match constant register (CMTm.CMCOR)	◎

Note 1. CMT n: 0 or 1

Note 2. CMT m: 0 to 3

Table 2.57 SH7216 Group and RX72M Register Comparison (CMTW)

SH7216 Group (CMT)*1	RX72M (CMTW)*2	Changes
Compare match timer start register (CMSTR)	Timer start register (CMTWm.CMWSTR)	△
Compare match timer control/ status register n (CMCSR_n)	Timer control register (CMTWm.CMWCR)	△
Compare match counter n (CMCNT_n)	Timer counter (CMTWm.CMWCNT)	△
Compare match constant register n (CMCOR_n)	Compare match constant register (CMTWm.CMWCOR)	△
—	Timer I/O control register (CMTWm.CMWIOR)	—
	Input capture registers 0 and 1 (CMTWm.CMWICR0 and CMTWm.CMWICR1)	
	Output compare registers 0 and 1 (CMTWm.CMWOCR0 and CMTWm.CMWOCR1)	

Note 1. CMT n: 0 or 1
Note 2. CMTW m: 0 or 1

2.17.3 Interrupts

CMT interrupts can be used to activate the DTC and the DMAC on both the SH7216 Group and the RX72M.

On the RX72M some of the CMT and CMTW interrupts are assigned to software configurable interrupt B. The interrupt controller's interrupt status flag (IRn.IR) is cleared automatically when the corresponding interrupt is accepted. The software configurable interrupt B status flag (PIBRk.PIRn) is not cleared automatically, but there is no effect on the generation of interrupt requests.

Refer to 1.8, Interrupt Handling for information about interrupts.

2.17.4 Module Stop

As on the SH7216 Group, the CMT of the RX72M is set to the module-stop state after a reset, and no clock is supplied.

Refer to 2.20, Low Power Consumption Function for information on the module-stop state.

2.18 Code Flash Memory

2.18.1 Comparison of Specifications

Table 2.58 is a comparative listing of the specifications of the SH7216 Group and RX72M.

Table 2.58 Comparison of SH7216 Group and RX72M Specifications (Code Flash Memory)

Item	SH7216 Group	RX72M
Size	User MAT: Max. 1 MB User boot MAT: 32 KB	User area: Max. 4 MB
Block size × block count	1 MB products • 128 KB × 3 blocks • 64 KB × 9 blocks • 8 KB × 8 blocks 768 KB product • 128 KB × 1 block • 64 KB × 9 blocks • 8 KB × 8 blocks 512 KB product • 64 KB × 7 blocks • 8 KB × 8 blocks	4 MB products Linear mode: • 32 KB × 126 blocks • 8 KB × 8 blocks Dual mode(Each bank): • 32 KB × 62 blocks • 8 KB × 8 blocks 2 MB products Linear mode: • 32 KB × 62 blocks • 8 KB × 8 blocks Dual mode(Each bank): • 32 KB × 30 blocks • 8 KB × 8 blocks
Write unit	256 bytes	128 bytes
Erase unit	User MAT • Writer mode: Erasure of entire area • Other than writer mode: Block units User boot MAT: Erasure of entire area	Block units
Write/erase count	1,000 times	100,000 times
Programming modes	On-board programming • Boot mode • USB boot mode • User boot mode • User programming mode Off-board programming • Writer mode	On-board programming • Serial programming • Boot mode (SCI / USB / FINE) • Self programming • Single chip mode Off-board programming • Programming with parallel programmers
Other	• Automatic bit rate matching • Protect mode • Suspend/resume function • BGO function (ability to run programs not assigned to code flash memory while programming or erasing of code flash memory is in progress) • ROM caching for faster operation	• Automatic bit rate matching • Protection function (prevention of unintentional overwriting) • Suspend/resume function • BGO function -Ability to read code flash memory while programming of code flash memory is in progress - Ability to read date flash memory while erasing code flash memory program • Security function (prevention of unauthorized modification/reading) • TM function (prevention of unauthorized reading) • 16-byte unique ID

On the RX72M FACI commands can be used to program the code flash memory. Refer to the following application note for details:RX Family Flash Module Firmware Integration Technology (R01AN2184EJ)

2.19 Data Flash

2.19.1 Comparison of Specifications

Table 2.59 is a comparative listing of the specifications of the SH7216 Group and RX72M.

Table 2.59 Comparison of SH7216 Group and RX72M Specifications (Data Flash Memory)

Item	SH7216 Group	RX72M
Size	Data MAT: 32 KB	Data area: 32 KB
Block size × block count	8 KB × 4 blocks	64 KB × 512 blocks
Write unit	Boot mode : 256 bytes Other than boot mode: 8-byte or 128-byte units	4 bytes
Erase unit	Block units	64/128/256 bytes
Write/erase count	30,000 times	100,000 times
Programming modes	On-board programming • Boot mode • USB boot mode • User boot mode • User mode/user programming mode	On-board programming • Serial programming • Boot mode (SCI / USB / FINE) • Self programming • Single chip mode Off-board programming • Programming with parallel programmers
Other	• Automatic bit rate matching • Protect mode • Suspend/resume function • BGO function (ability to run programs from code flash memory while programming or erasing of data flash memory is in progress) • Blank checking function	• Automatic bit rate matching • Protection function (prevention of unintentional overwriting) • Suspend/resume function • BGO function -Ability to read code flash memory while programming of code flash memory is in progress - Ability to read date flash memory while erasing code flash memory program • Blank checking function • Security function (prevention of unauthorized modification/reading) • 16-byte unique ID

On the RX72M FACI commands can be used to program the code flash memory. Refer to the following application note for details:

RX Family Flash Module Firmware Integration Technology (R01AN2184EJ)

2.20 Low Power Consumption Function

2.20.1 Comparison of Mode Specifications

Table 2.60 and Table 2.61 summarize the methods for transitioning to and canceling the various low-power states on the SH7216 Group and RX72M, and list the operating states of the clock, CPU, and on-chip modules.

Table 2.60 SH7216 Group Low-Power States

Transition and Cancelation Methods, and Operating States	Sleep Mode	Module Standby Function	Software Standby Mode
Transition method	Control register + instruction	Control register	Control register + instruction
Cancelation method other than reset	Interrupt DMA address error	Control register	Interrupt
Clock	Operating	Operating	Stopped
CPU	Stopped	Operating	Stopped
On-chip peripheral modules	Operating	Specified modules stopped	Stopped

Table 2.61 RX72M Low-Power States

Transition and Cancelation Methods, and Operating States	Sleep Mode	All-Module Clock Stop Mode	Software Standby Mode	Deep Software Standby Mode
Transition method	Control register + instruction	Control register + instruction	Control register + instruction	Control register + instruction
State after release	Program execution state (Interrupt processing)	Program execution state (Interrupt processing)	Program execution state (Interrupt processing)	Program execution state (Reset processing)
Cancelation method other than reset	Interrupt	Interrupt	Interrupt	Interrupt
Main clock oscillator, sub-clock oscillator	Operation possible	Operation possible	Operation possible	Operation possible
High-speed on-chip oscillator, low-speed on-chip oscillator	Operation possible	Operation possible	Stopped	Stopped
IWDT dedicated on-chip oscillator	Operation possible	Operation possible	Operation possible	Stopped (settings undetermined)
PLL PPLL	Operation possible	Operation possible	Stopped	Stopped
CPU	Stopped (settings retained)	Stopped (settings retained)	Stopped (settings retained)	Stopped (settings undetermined)
RAM	Operation possible (settings retained)	Stopped (settings retained)	Stopped (settings retained)	Stopped (settings undetermined)
Standby RAM	Operation possible (settings retained)	Stopped (settings retained)	Stopped (settings retained)	Stopped (settings retained/ undetermined)*1
Flash memory	Operation possible	Stopped (settings retained)	Stopped (settings retained)	Stopped (settings retained)

Transition and Cancelation Methods, and Operating States	Sleep Mode	All-Module Clock Stop Mode	Software Standby Mode	Deep Software Standby Mode
USBFS host/function module (USBb)	Operation possible	Stopped	Stopped	Stopped (settings retained/ undetermined)*1
Watchdog timer (WDT)	Stopped (settings retained)	Stopped (settings retained)	Stopped (settings retained)	Stopped (settings undetermined)
Independent watchdog timer (IWDT)	Operation possible	Operation possible	Operation possible	Stopped (settings undetermined)
Realtime clock (RTC)	Operation possible	Operation possible	Operation possible	Operation possible
8-bit timer (TMR)	Operation possible	Operation possible	Stopped (settings retained)	Stopped (settings undetermined)
Port Output Enable (POE)	Operation possible	Operation possible	Stopped (settings retained)	Stopped (settings undetermined)
Voltage detection circuit (LVDA)	Operation possible	Operation possible	Operation possible	Operation possible
Power-on reset circuit	Operation possible	Operation possible	Operation possible	Operation possible
Peripheral modules	Operation possible	Stopped (settings retained)	Stopped (settings retained)	Stopped (settings undetermined)
I/O ports	Operation possible	Settings retained	Settings retained	Settings retained

Stopped (settings retained):
State in which the values of the internal registers are retained and the internal state is operation suspended.

Stopped (settings undetermined):
State in which the values of the internal registers are undetermined and the internal state is power-off.

Note 1. Either “settings retained” or “settings undetermined” may be selected by means of a control register setting

2.20.2 Mode Transitions

Figure 2.23 diagrams the transitions between the modes of the RX72M, and Table 2.62 lists transition conditions.

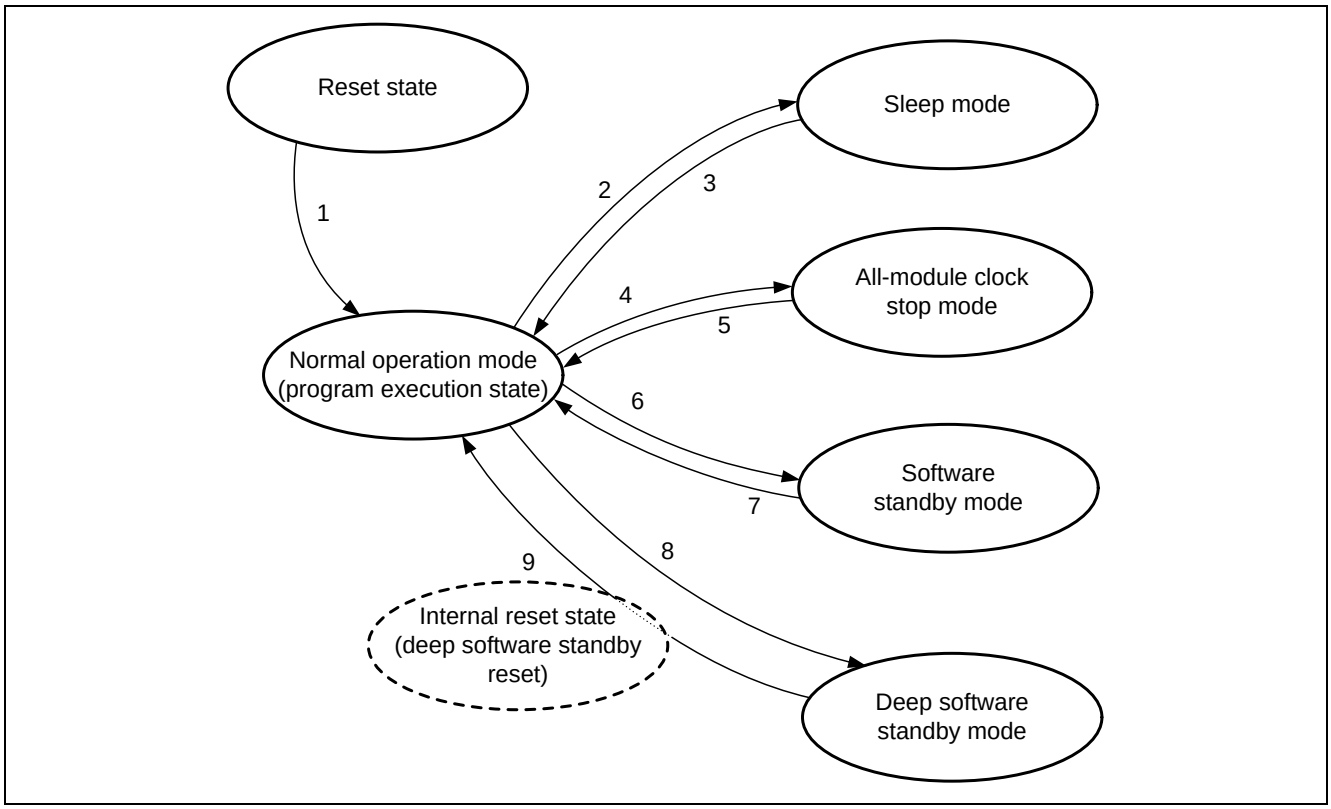


Figure 2.23 RX72M Mode Transitions

Table 2.62 List of RX72M Mode Transitions and Events

No.	Event	Transition Condition (The following conditions are specified before the event.)
1	RES# pin = high	—
2	WAIT instruction executed	SBYCR.SSBY = 0
3	All interrupts	—
4	WAIT instruction executed	SBYCR.SSBY = “0”, MSTPCRA.ACSE = “1”, MSTPCRA = “FFFF FF[C-F]Fh” MSTPCRB = “FFFF FFFFh”, MSTPCRC[31:16] = “FFFFh”, MSTPCRD = “FFFF FFFFh”
5	External and peripheral interrupts	External pin interrupts (NMI, IRQ0 to IRQ15) Peripheral function interrupts (8-bit timer, RTC alarm, RTC cycle, IWDT, USB suspend/resume, voltage monitor 1, voltage monitor 2, oscillation stop detection)*1
6	WAIT instruction executed	SBYCR.SSBY = 1, DPSBYCR.DPSBY = 0
7	External and peripheral interrupts	External pin interrupts (NMI, IRQ0 to IRQ15) Peripheral function interrupts (RTC alarm, RTC cycle, IWDT, USB suspend/resume, voltage monitor 1, voltage monitor 2)*1
8	WAIT instruction executed	SBYCR.SSBY = 1, DPSBYCR.DPSBY = 1
9	External and peripheral interrupts	Some pins used as external pin interrupt sources (NMI, IRQ0-DS to IRQ15-DS, SCL2-DS, SDA2-DS, CRX1-DS), peripheral function interrupts (RTC alarm, RTC cycle, USB suspend/resume, voltage monitor 1, voltage monitor 2)*1 After one of the above interrupts occurs the internal reset state lasts for a specified duration, after which the internal reset and deep software standby mode are canceled at the same time, and the CPU operates in normal operation mode using the LOCO (recovery after a reset).

Note 1. Each interrupt has detailed conditions. For descriptions, see the User’s Manual: Hardware.

2.20.3 Module-Stop State

On the SH7216 Group the modules other than the RAM and ROM are set to the module-stop state after a reset, and no clock is supplied.

On the RX72M the modules other than the DMAC,DTC, EXDMACa, RAM, ECCRAM,Expansion RAM and standby RAM are set to the module-stop state after a reset, and no clock is supplied. The DTC and DMAC share a common module-stop setting bit (MSTPCRA.MSTPA28), so module-stop control is applied to them both simultaneously. The EXDMACa has an independent module-stop setting bit (MSTPCRA.MSTPA29), so it can be controlled individually.

As on the SH7216 Group, on the RX72M it is necessary to cancel the module-stop state before using any module that enters the module-stop state after a reset.

When changing module-stop state settings on the RX72M it is necessary to turn off register write protection in the protect register (PRCR) before accessing the module-stop control register (MSTPCRn).

Table 2.63 lists the clock supply state after a reset of each module.

Table 2.63 Clock Supply State after Reset

Function Name*1	SH7216 Group	RX72M*2
RAM	Clock supplied (operating)	Clock supplied (operating)
User break controller (UBC)	No clock supplied	—
Data transfer controller (DTC)		Clock supplied (operating)
Direct memory access controller (DMAC)		
Multi-function timer pulse unit (MTU)		No clock supplied
Serial communication interface (SCI, SCIF)		
Serial peripheral interface (RSPI)		
I^2C bus interface (IIC)		
A/D converter (ADC)		
Compare match timer (CMT)		

Note 1. The function names listed are those for the SH7216 Group.

Note 2. On the RX72M there are other modules affected by the module-stop function in addition to those listed in the table.

2.20.4 Write Protection

The RX72M is protected by a register write protection function that protects important registers from being overwritten in the event of a program runaway. The low power consumption function-related registers are protected by this function.

If necessary, set protect bit 1 (PRCR.PRC1) to 1 to enable writes before writing to these registers.

3. Sample Code

For the setting example of each function, set according to the purpose with the smart configurator and generate the code.

4. Reference Documents

4.1 Reference Documents

Section 4.1 lists the documents referenced in the preparation of this application note. When referring to the documents listed below, substitute the latest version if a newer version is available. The latest versions of these documents can be confirmed and downloaded from the Renesas Electronics Website.

Table 4.1 Reference Documents

SH7214 Group, SH7216 Group User's Manual: Hardware (R01UH0230EJ0400)
SH-2A, SH2A-FPU User's Manual: Software (R01US0031EJ)
RX72M Group User's Manual: Hardware (R01UH0493EJ0110)
RX Family Flash Module Firmware Integration Technology (R01AN2184EJ)
RX Family RXv3 Instruction Set Architecture User's Manual: Software (R01US0316EJ0100)
RX72M Group Renesas Starter Kit+ User's Manual (R20UT3217EG0100)
Renesas Starter Kit+ for RX72M CPU Board Schematics (R20UT3216EG0100)
RX72M Group Initial Settings Example (R01AN4530EJ0100)

Consistency with Technical Updates

This application note reflects the contents of the following technical update:

TN-RX*-A127A/E

Adds function of “RX64M Group, RX72M Group User’s Manual: Hardware”

Page 2746 of 2923 (RX72M Group)

Specifications of code flash memory and data flash memory add unique ID.

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Revision History

		Description	
Rev.	**Date**	**Page**	**Summary**
1.00	Sep.22, 2022	—	First edition issued

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins

   Handle unused pins in accordance with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.

   — The characteristics of Microprocessing unit or Microcontroller unit products in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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