SH7239 Group

A/D Converter
— Two-Channel Scan Mode A/D Conversion Sample Program

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Introduction

This application note describes a sample program that uses the A/D converter's two-channel scan mode combined with the multifunction timer/pulse unit 2 A/D converter start request delayed function.

Target Device

SH7239A/SH7239B

When using the sample code presented in this application note with other microcontrollers, modify the code according to the specifications of the microcontroller used and test thoroughly.

Contents

1. Introductions

1.1 Specifications

This application presents a sample program that uses the two-channel scan mode provided by the A/D converter module (ADC). This program also uses the multifunction timer/pulse unit 2 (MTU2) A/D converter start request delayed function.

Figure 1 shows the structure of the functions used and figure 2 shows the A/D converter start request timing generated by the MTU2 module.

- The operating mode of ADC module 0 is set to two-channel scan mode.
- Group 0 (AN0 and AN1) and group 1 (AN2 and AN3) are selected as the A/D input pins.
- The MTU2 A/D converter start request delayed function is used. The TGR4AN A/D converter start trigger starts group 0 and the TGR4BN A/D converter start trigger starts group 1.
- The results of A/D conversion are stored in RAM on the A/D conversion complete interrupt.
- The MTU2 channels 3 and 4 are set to complementary PWM mode and output a 3-phase complementary PWM signal. A trigger signal synchronized with the PWM carrier is also output.
- The PWM output duty is set during MTU2 TGRA3 compare match interrupt handling and the A/D converter start trigger start timing is updated.

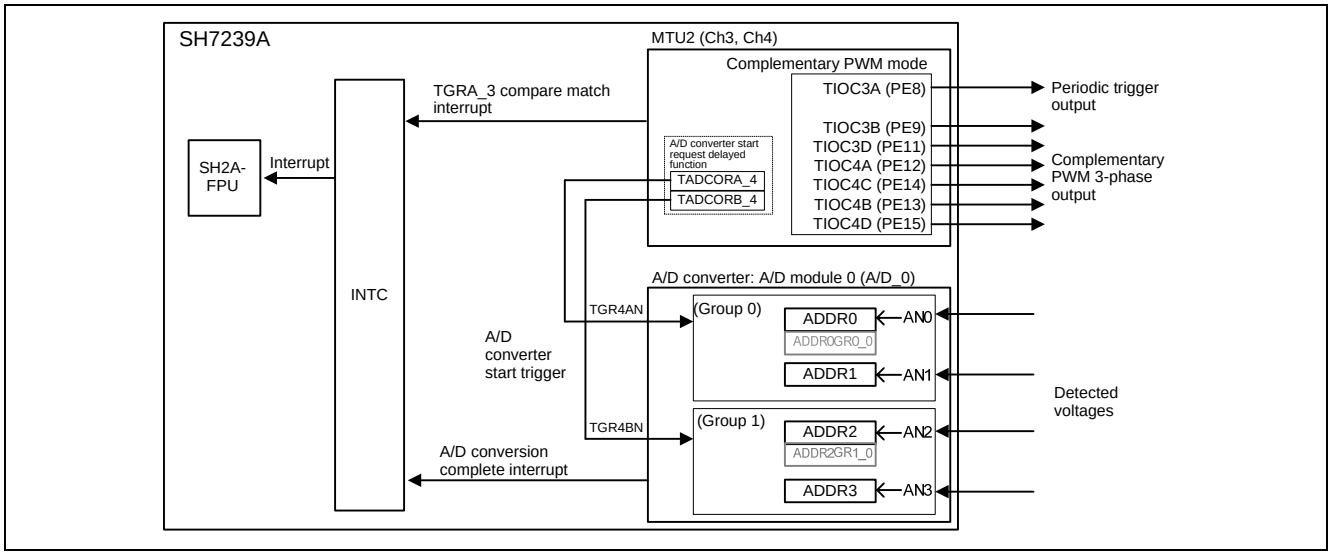


Figure 1 MTU2 A/D Conversion Start Structure

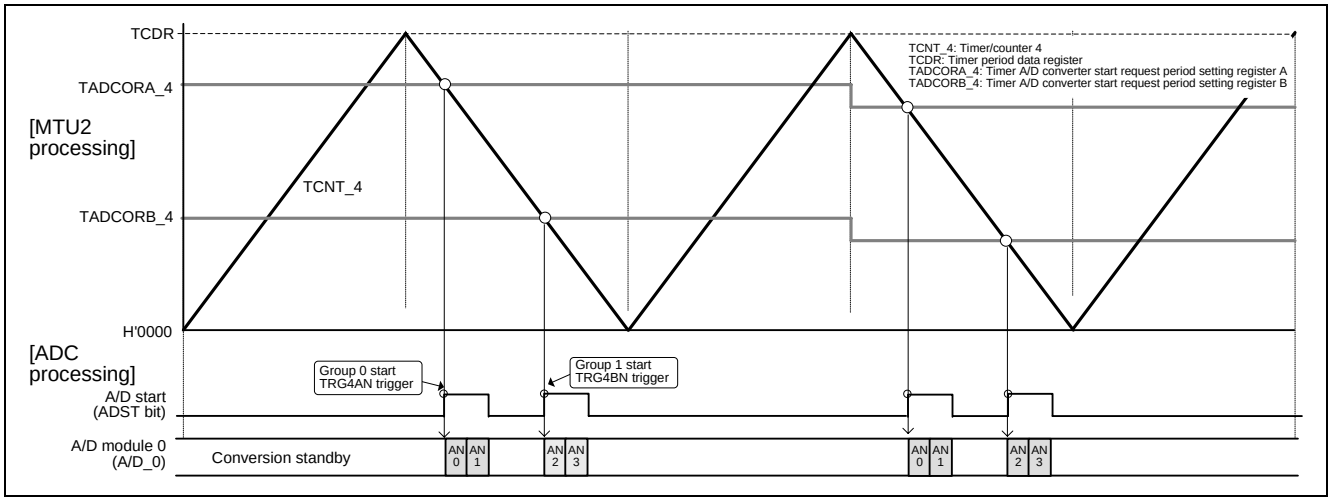


Figure 2 MTU2 A/D Converter Start Trigger and A/D Conversion Timing

1.2 Functions Used

- A/D converter (ADC)
- Multifunction timer/pulse unit 2 (MTU2)
- Pin function controller (PFC)
- Interrupt controller (INTC)

1.3 Usage Conditions

Microcontroller	SH7239A / SH7239B
Operating frequencies	Internal clock: 160 MHz / 100 MHz Bus clock: 40 MHz / 50 MHz Peripheral clock: 40 MHz / 50 MHz AD clock: 40 MHz / 50 MHz MTU clock: 80 MHz / 100 MHz
MCU operating mode	Single-chip mode
Integrated development environment	Renesas Electronics High-performance Embedded Workshop Ver.4.07.00
C compiler	Renesas Electronics SuperH RISC engine Family C/C++ Compiler Package Ver.9.03 Release02
Compiler options	-cpu=sh2afpu -fpu=single -include="$(WORKSPDIR)\inc" -object="$(CONFIGDIR)\$(FILELEAF).obj" -debug -gbr=auto –chgincpath -errorpath -global_volatile=0 -opt_range=all -infinite_loop=0 -del_vacant_loop=0 -struct_alloc=1 –nologo

1.4 Related Application Notes

SH7239 Group Example of Initialization (R01AN0297EJ)

2. Sample Program

This sample program uses the A/D converter (ADC) and the multifunction timer/pulse unit 2 (MTU2).

2.1 Overview of Functions Used

2.1.1 A/D Converter (ADC)

The A/D converter is a 12-bit successive-approximation A/D converter module, and these microcontrollers include three of these modules (A/D_0, A/D_1, and A/D_2). A/D converter operating modes include single-cycle scan mode, continuous scan mode, and two-channel scan mode.

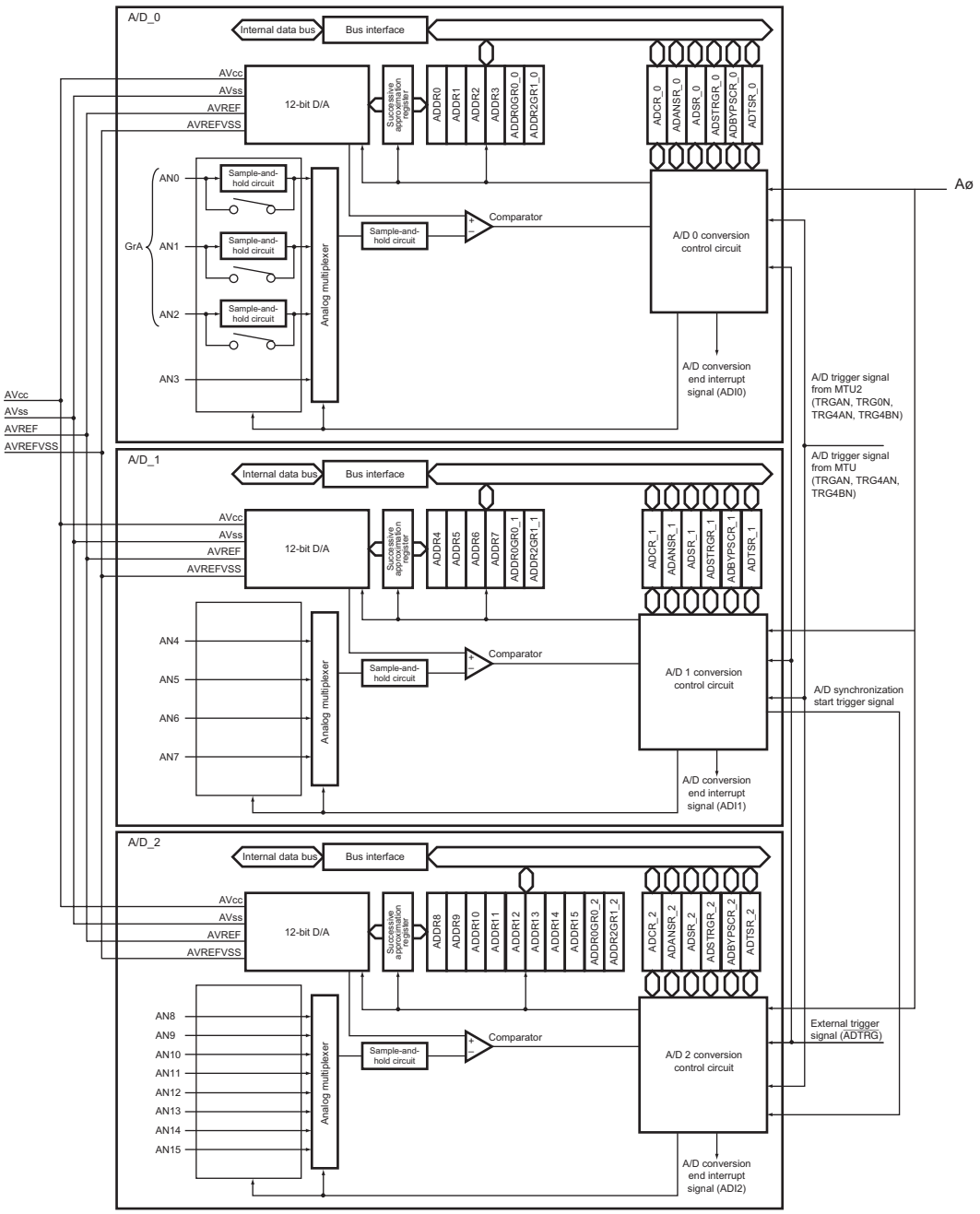
In single-cycle scan mode, the ADC module converts one or more channels once each and then terminates. The ADST bit is automatically cleared to 0. In contrast, in continuous scan mode, the specified one or more channels are repeatedly scanned until the ADST bit is cleared to 0 in software. And in two-channel scan mode, 4 analog input channels are divided into two groups (group 0 and group 1) and A/D conversion of the specified channels is performed once each by the selected triggers for group 0 and group 1, after which A/D converter operation terminates.

Table 1 lists the details of the ADC module and figure 3 shows its block diagram.

For detailed information on the ADC, see the A/D Converter section in the SH7239 Group, SH7237 Group User's Manual: Hardware.

Table 1 ADC Module Overview

Item	Description
Resolution	12 bits
Conversion speed	A minimum of 1.25 µs per channel (when the AD clock is 40 MHz) A minimum of 1.0 µs per channel (when the AD clock is 50 MHz)
Number of modules	3 modules
Number of input channels	16 channels total • A/D_0: 4 channels (ch0 to ch3) • A/D_1: 4 channels (ch4 to ch7) • A/D_2: 8 channels (ch8 to ch15)
Operating modes	Single-channel scan mode Continuous scan mode Two-channel scan mode
Sample-and-hold function	Sample-and-hold circuits for each module • Common to ch0 to ch3: 1 circuit • Common to ch4 to ch7: 1 circuit • Common to ch8 to ch15: 1 circuit Dedicated sample-and-hold circuits for each channel • ch0 to ch2: One circuit for each channel (3 circuits, total)
A/D conversion start sources	Software: Setting the ADST bit Timers: MTU2 (TRGAN, TRG0N, TRG4AN, or TRG4BN) MTU2S (TRGAN, TRG4AN, or TRG4BN) External trigger: $\overline{\text{ADTRG}}$ (an IC pin)



[Legend]

ADDR: A/D data register
ADCR: A/D control register
ADANSR: A/D analog input channel select register
ADSR: A/D status register
ADSTRGR: A/D start trigger select register
ADBYPSCR: A/D bypass control register
ADTSR: A/D trigger select register
ADDR0GR0: A/D group-0 data-0 register
ADDR2GR1: A/D group-1 data-2 register
GrA: Group A

Figure 3 Block Diagram of A/D Converter

2.1.2 ADC Input Pins

Table 2 lists the ADC analog input pins used. Since using these input pins requires attention to certain points, refer to the Usage Notes section in the A/D Converter chapter in SH7239 Group and SH7237 Group User's Manual: Hardware.

Each of the three A/D modules (A/D_0, A/D_1, and A/D_2) in the A/D converter has a single, common to all channels, sample-and-hold circuit for each module. These can be operated independently.

Each of the analog input pins (AN0, AN1, and AN2) for channels 0 to 2 (group A) in A/D module 0 (A/D_0) has a built-in, dedicated, per-channel sample-and-hold circuit. These are separate from the per-module shared between channels sample-and-hold circuits and since there are three built-in dedicated sample-and-hold circuits, one for each channel (analog input pin), the selected channels can be sampled at the same time.

Table 2 ADC Input Pins

Module Class	Pin	Function	Signals that can be sampled at the same time	Group in two-channel scan mode
A/D module 0 (A/D_0)	AN0	Analog input pin 0	Group A (GrA)	Group 0
	AN1	Analog input pin 1		
	AN2	Analog input pin 2		Group 1
	AN3	Analog input pin 3	—	
A/D module 1 (A/D_1)	AN4	Analog input pin 4	—	Group 0
	AN5	Analog input pin 5	—	
	AN6	Analog input pin 6	—	Group 1
	AN7	Analog input pin 7	—	
A/D module 2 (A/D_2)	AN8	Analog input pin 8	—	Group 0
	AN9	Analog input pin 9	—	
	AN10	Analog input pin 10	—	Group 1
	AN11	Analog input pin 11	—	
	AN12	Analog input pin 12	—	
	AN13	Analog input pin 13	—	
	AN14	Analog input pin 14	—	
	AN15	Analog input pin 15	—	

2.1.3 ADC Two-Channel Scan Mode

Two-channel scan mode divides the analog inputs for two channels from each A/D module (A/D_0, A/D_1, and A/D_2) into two groups, group 0 and group 1, and allows the start factor based on individual triggers to be selected for group 0 and group 1. This function can be used when the operating mode is set to two-channel scan mode.

The ADC operating mode is set with the ADCS bit in the A/D control register (ADCR) and the 2CHSE bit in the A/D trigger select register. To select two-channel scan mode, set the 2CHSE bit in ADTSR to 1 regardless of the value of the ADCS bit in ADCR.

In two-channel scan mode, when conversion of all channels selected by the settings has completed, the ADF bit in the A/D status register (ADSR) is set to 1 and the ADST bit in ADCR is cleared automatically. When the ADF bit is set to 1, if the ADIE bit in ADCR has been set to 1, an A/D conversion complete interrupt (ADI) will be generated. To clear the ADF bit to 0 in software, first read the bit when it has the value 1 and then write 0 to that bit.

It is also possible to select whether the conversion complete interrupt in two-channel scan mode is generated after the completion of conversion for group 0 and group 1 separately, or after both group 0 and group 1 have both completed. Select the ADF bit set timing with the CONADF bit in ADTSR. When triggers are used to start conversion, set the start factors separately for both ADTSR group 0 and group 1. Note that if a conversion request for group 1 occurs during a group 0 conversion, that group 1 conversion request is ignored.

(1) Two-Channel Scan Mode Operation — Example 1

Figure 4 shows operation example 1 for two-channel scan mode.

The operating mode is set to two-channel scan mode and the channels used are set to be group 0 (AN0 and AN1) and group 1 (AN2 and AN3). The group 0 A/D conversion start factor is set to be the MTU2 TRG4AN and the group 1 A/D conversion start factor is set to be the MTU2 TRG4BN. Each of these triggers (TRG4AN and TRG4BN) is generated on the decrement of the timer/counter TCNT4.

The ADF bit in the A/D status register (ADSR), which indicates the completion of A/D conversion, is specified to be set each time a group 0 or group 1 conversion completes when the CONADF bit in the A/D trigger select register (ADTSR) is 0. In this example, it is set twice. When the CONADF bit is set to 1, it is only set after the completion of both the group 0 and the group 1 conversions.

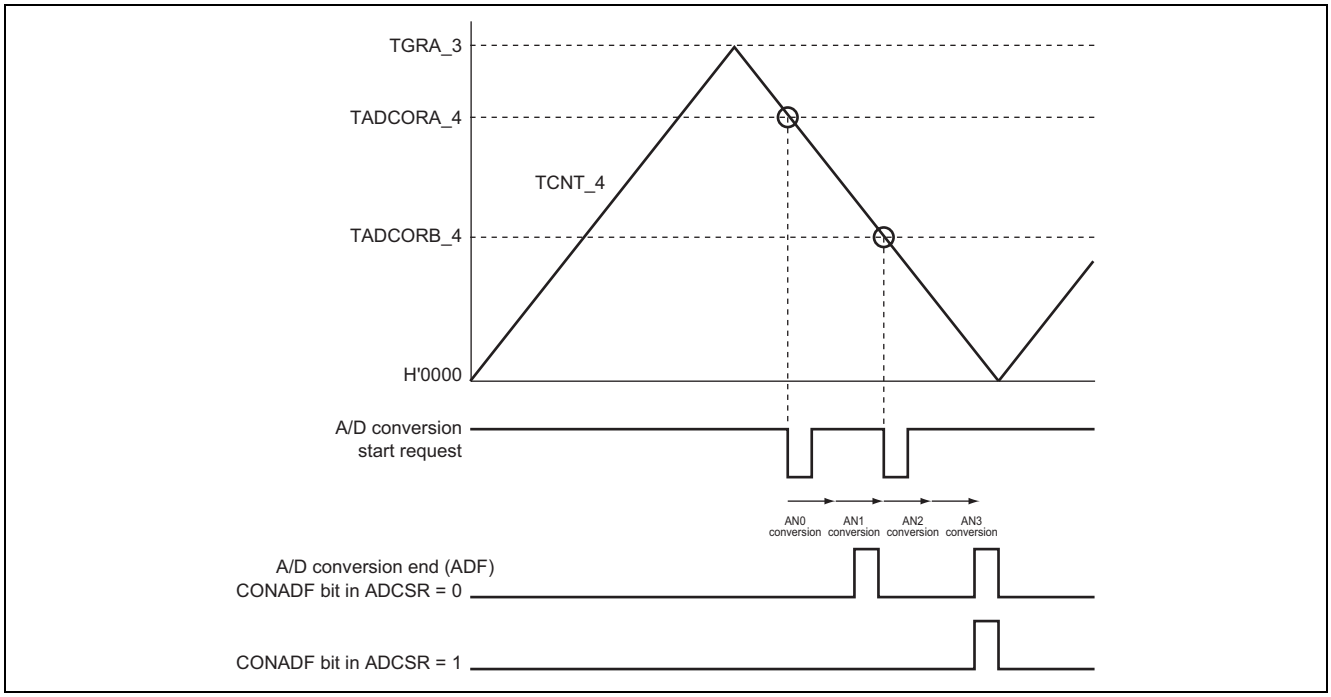


Figure 4 A/D Converter Two-Channel Scan Mode Operation Example 1

(2) Two-Channel Scan Mode Operation — Example 2

Figure 5 shows operation example 2 for two-channel scan mode.

The operating mode is set to two-channel scan mode and the channels used are set to be group 0 (AN0) and group 1 (AN2). The A/D conversion start request for group 0 is set to be both TRG4AN and TRG4BN from MTU2 (the TRG0S field in the ADTSR_0 register is set to B'0101). This enables start of A/D conversion of a single group by two different triggers (TRG4AN and TRG4BN). The group 1 A/D conversion start request is set to TRGAN. The TRG4AN and TRG4BN triggers are both generated when TCNT4 is decremented.

In this case, the group 0 A/D conversion is started twice, by the TRG4AN and TRG4BN triggers, and the group 1 A/D conversion is started once by the TRGAN trigger. The first conversion result for group 0 A/D conversion is stored in A/D data register 0 (ADDR0) and the second is stored in A/D group 0 data 0 register 0 (ADDR0GR0_0), After the second A/D conversion completes, the data can be read from those registers.

The ADF bit in the A/D status register (ADSR), which indicates the completion of A/D conversion, is specified to be set each time a group 0 or group 1 conversion completes when the CONADF bit in the A/D trigger select register (ADTSR) is 0. In this example, it is set three times. When the CONADF bit is set to 1, it is only set after the completion of both the group 0 and the group 1 conversions.

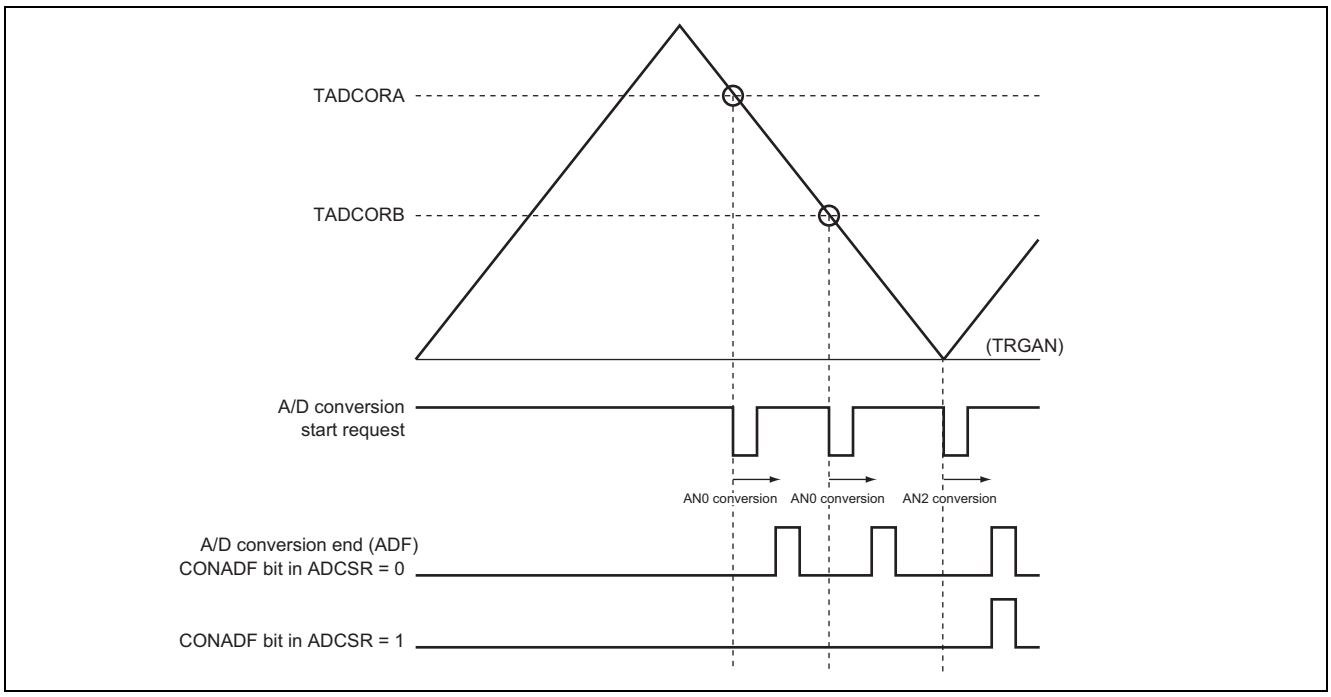


Figure 5 A/D Converter Two-Channel Scan Mode Operation Example 2

2.1.4 Multifunction Timer/Pulse Unit 2 (MTU2)

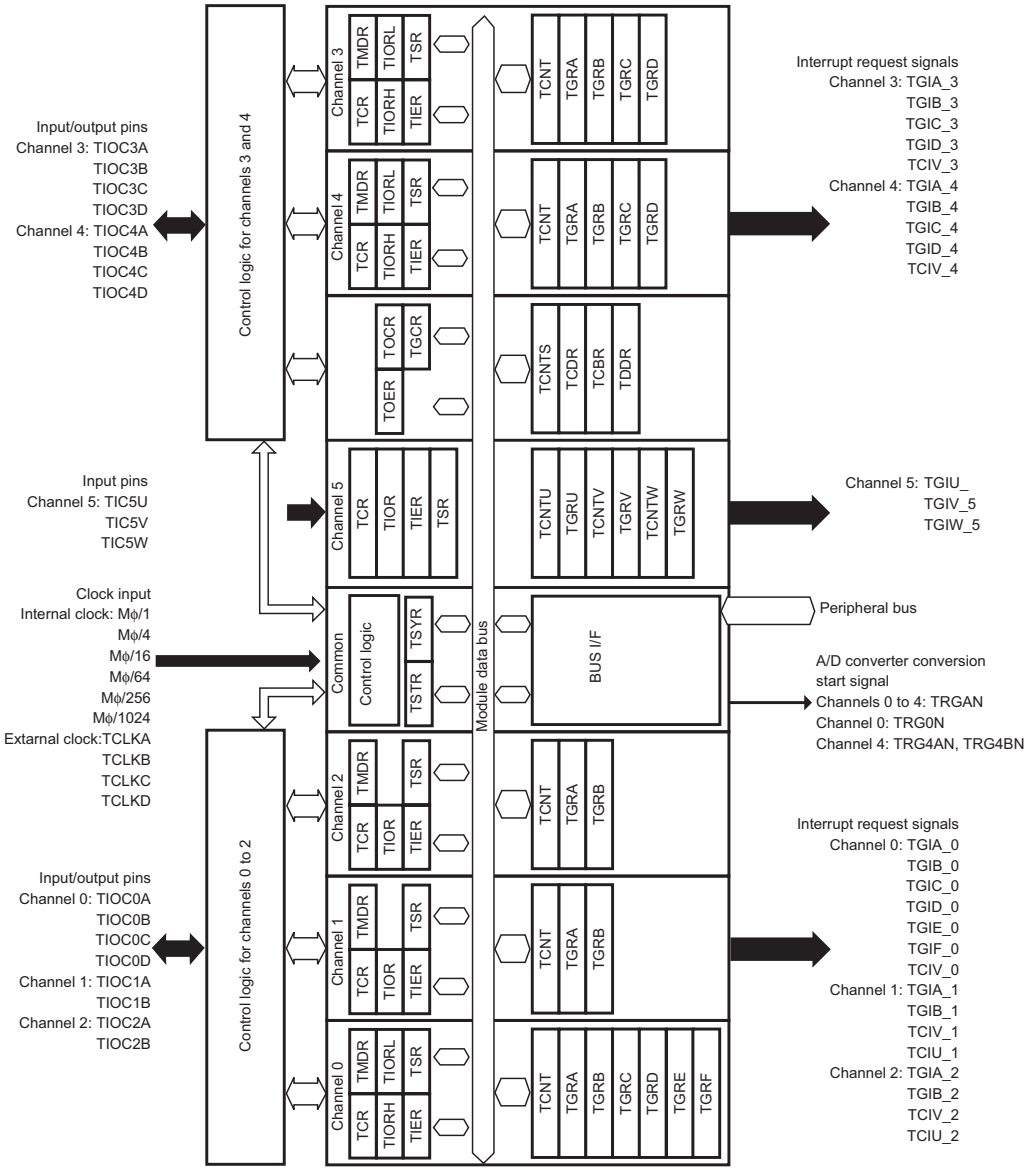
MTU2 is a multifunction timer unit that consists of six 16-bit timer channels. Each channel supports a variety of functions including compare match and input capture. By setting channels 3 and 4 to complementary PWM mode or reset synchronization mode, up to six PWM outputs can be controlled. Furthermore, it can be used to generate A/D converter start triggers by using the A/D converter start request delay function.

Table 3 presents an overview of MTU2 and figure 6 shows its block diagram.

See the Multifunction Timer/Pulse Unit 2 section in SH7239 Group and SH7237 Group User's Manual: Hardware for further details on MTU2.

Table 3 Multifunction Timer/Pulse Unit 2 Overview

Item	Description
Number of channels	Six 16-bit timer channels (channels 0 to 5)
Counter clock	One of 8 counter input clocks can be selected for each channel (one of 4 clocks for channel 5)
Operation of channels 0 to 5	• Compare match based waveform output • Input capture function • Counter clear operation • Simultaneous write to multiple timer counters (TCNT) • Synchronized clear using compare match or input capture • Up to 12 phases of PWM output by combing synchronized operation with synchronized I/O for each register by synchronized counter operation
A/D converter trigger	• A/D converter conversion start triggers can be generated • A/D conversion can be started with the A/D converter start request delay function • In complementary PWM mode, interrupts can be generated at counter peaks and valleys and the A/D converter conversion start triggers can be decimated.
Buffer operation	Register buffer operation can be specified for channels 0, 3, and 4
Operating modes	• Channels 0 to 4 can be set up for PWM mode • Phase counting mode can be set up independently for channels 1 and 2 • Output of a total of six positive and negative PWM waveforms (three phases) can be set up using complementary PWM mode and reset synchronized PWM mode by linking channels 3 and 4
Interrupt requests	A total of 28 interrupts including compare match and input capture interrupts
Other features	• Cascade connected operation • High-speed access using an internal 16-bit bus • Register data can be transferred automatically • Module standby mode can be used • Channel 5 supports a dead time compensation function



[Legend]

TSTR: Timer start register	TCNTS: Timer subcounter
TSYR: Timer synchronous register	TCDR: Timer cycle data register
TCR: Timer control register	TCBR: Timer cycle buffer register
TMDR: Timer mode register	TDDR: Timer dead time data register
TIOR: Timer I/O control register	TGRA: Timer general register A
TIORH: Timer I/O control register H	TGRA: Timer general register B
TIORL: Timer I/O control register L	TGRA: Timer general register C
TIER: Timer interrupt enable register	TGRA: Timer general register D
TGCR: Timer gate control register	TGRA: Timer general register E
TOER: Timer output master enable register	TGRA: Timer general register F
TOCR: Timer output control register	TGRA: Timer general register U
TSR: Timer status register	TGRA: Timer general register V
TCNT: Timer counter	TGRA: Timer general register W

Figure 6 Multifunction Timer/Pulse Unit 2 Block Diagram

2.1.5 MTU2 Complementary PWM Mode

By using channels 3 and 4 in combination, MTU2 can be used in complementary PWM mode. In complementary PWM mode, the MTU2 can generate a three-phase PWM waveform output in which the positive phase and negative phase do not overlap. It is also possible to set up PWM waveform output that does not have a non-overlap period (short-circuit prevention period). The TIOC3B, TIOC3D, TIOC4A, TIOC4B, TIOC4C, and TIOC4D pins are used as the complementary PWM mode PWM output pins. Note that the TIOC3A pin can be used as a toggle output synchronized with the PWM period.

Figure 7 shows the MTU2 channel 3 and 4 structure when complementary PWM mode is used.

See the Multifunction Timer/Pulse Unit 2 section in SH7239 Group and SH7237 Group User's Manual: Hardware for further details on complementary PWM mode.

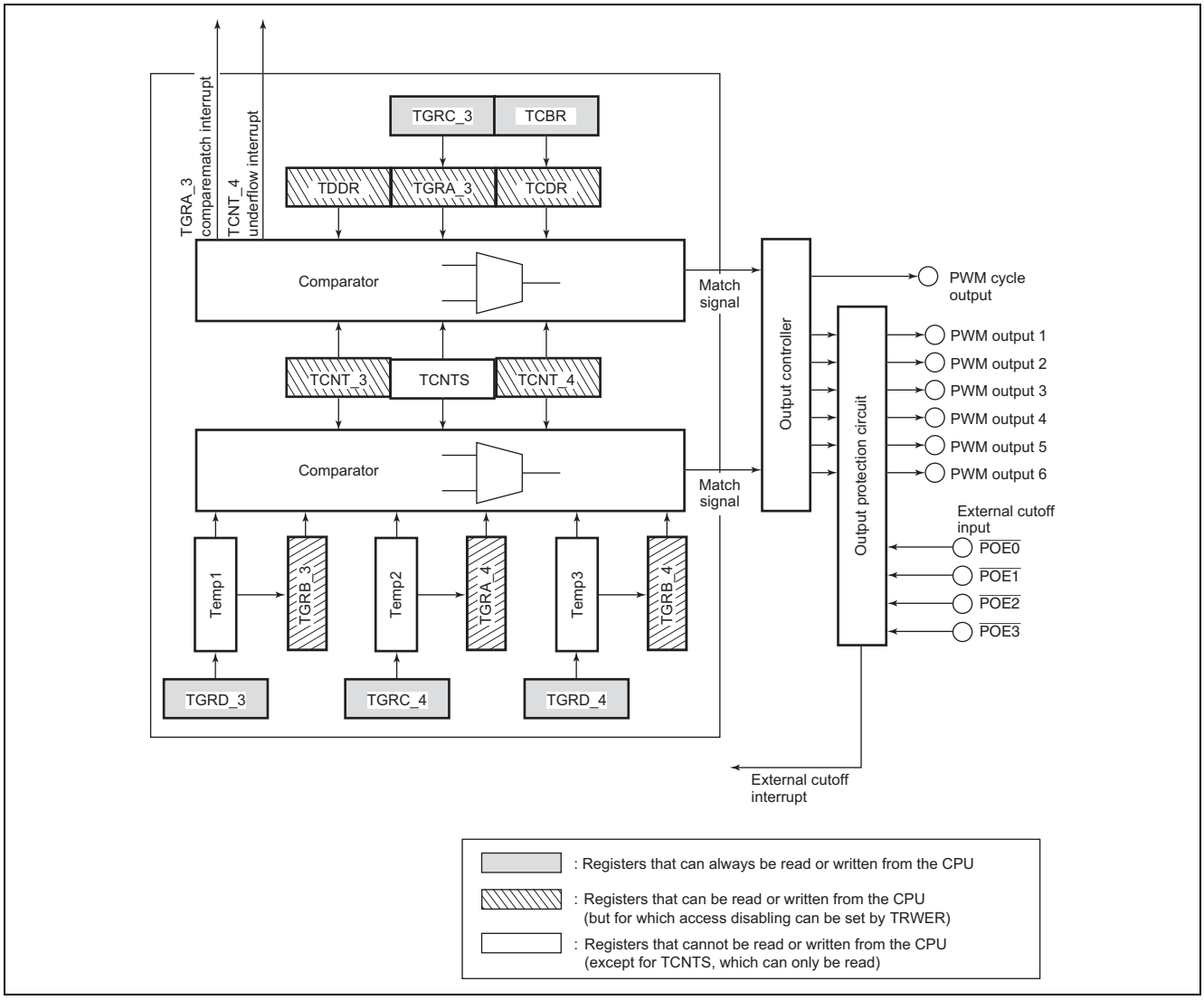


Figure 7 MTU2 Channels 3 and 4 Block Diagram in Complementary PWM Mode

2.1.6 MTU2 A/D Converter Start Request Delay Function

The MTU2 can issue A/D converter start requests by setting the MTU2 channel 4 timer A/D converter start request control register (TADCR), the timer A/D converter start request period registers (TADCORA_4 and TADCORB_4), and the timer A/D converter start request buffer registers (TADCOBRA_4 and TADCOBRB_4).

The A/D converter start request delay function compares the MTU2 channel 4 timer counter (TCNT_4) with the timer A/D converter start request period registers (TADCORA_4 and TADCORB_4) and issues an A/D converter start request when they match.

- Issue an A/D converter start request (TRG4AN) when TCNT_4 and TADCORA_4 match.
- Issue an A/D converter start request (TRG4BN) when TCNT_4 and TADCORB_4 match.

The MTU2 also provides a function that decimates A/D converter start requests (TRG4AN and TRG4BN) coupled with the interrupt decimation function according to the settings of the ITA3AE, ITA4VE, ITB3AE, and ITB4VE bits.

Figure 8 shows an example of the basic operation of the A/D converter start request signal (TRG4AN). In this example, the MTU2 is set up so that the A/D converter start request signal (TRG4AN) is issued on the decrement of TCNT_4 and the buffer transfer timing (the transfer from the period buffer register to the period register) occurs at the TCNT_4 valley.

See the Multifunction Timer/Pulse Unit 2 section in SH7239 Group and SH7237 Group User's Manual: Hardware for further details on the A/D converter start request delay function.

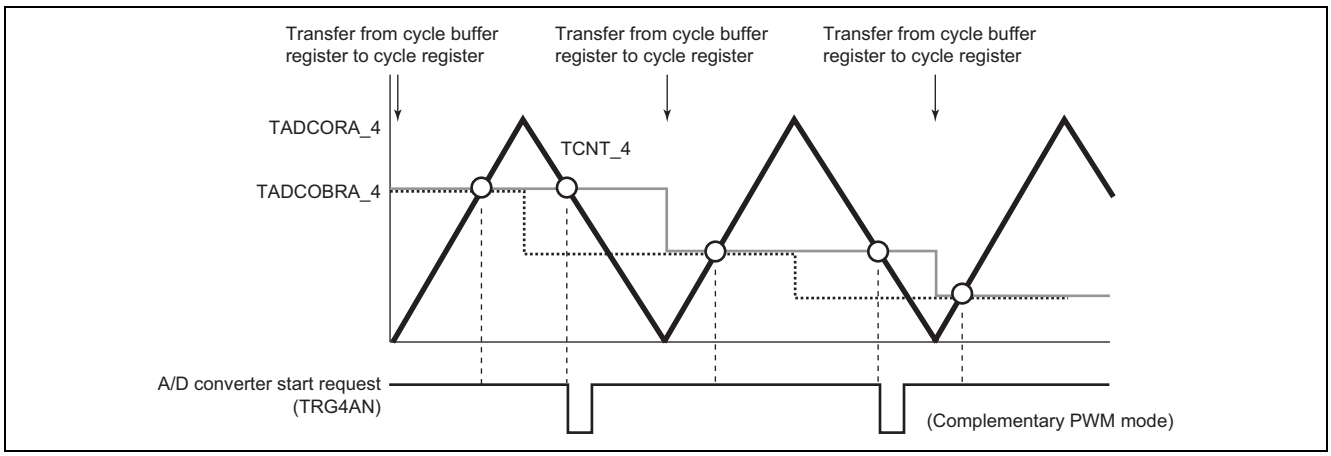


Figure 8 MTU2 A/D Converter Start Request Delay Function Basic Operation

2.2 Sample Program Operation

2.2.1 Sample Program Operational Settings

Tables 4 and 5 list the settings used by the sample program.

In the sample program, ADC A/D module 0 (A/D_0) is set to two-channel scan mode and A/D conversion is started by an A/D converter start trigger. The MTU2 A/D converter start request delay function is used as the A/D converter start trigger.

Table 4 ADC Settings

Item	Description
Module and input pin used	A/D_0 (AN0, AN1, AN2, AN3)
Conversion mode	Two-channel scan mode • Group 0 (AN0 and AN1) • Group 1 (AN2 and AN3)
Automatic ADDR clear	Disabled
Interrupts	A/D conversion complete interrupt (ADI0) • Interrupt priority level 10 • When both group 0 and group 1 have completed
A/D conversion start	MTU2 A/D converter start trigger • Group 0: TRG4AN • Group 1: TRG4BN
Dedicated per-channel sample-and-hold circuits	Unused

Table 5 MTU2 Settings

Item	Description
Channels used	Channels 3 and 4
Operating mode	Complementary PWM mode 3 • Data transfer at counter peaks and valleys
Pin functions	• TIOC3A pin: Toggle output synchronized with the PWM output period • TIOC3B pin: PWM output 1 (positive phase waveform) • TIOC3D pin: PWM output 1 (negative phase waveform) • TIOC4A pin: PWM output 2 (positive phase waveform) • TIOC4C pin: PWM output 2 (negative phase waveform) • TIOC4B pin: PWM output 3 (positive phase waveform) • TIOC4D pin: PWM output 3 (negative phase waveform)
Active levels	• Positive phase output: active low output • Negative phase output: active low output
Counter clock	Mϕ/4 = 20 MHz (SH7239A) / 25 MHz (SH7239B)
PWM carrier period	500 us (2 KHz)
Dead time	4 us
PWM duty	Variable • The set value is updated during interrupt (TGIA) handling
A/D converter start request delay function	• Triggers are generated on the TCNT_4 decrement (TRG4AN and TRG4BN) • Not linked to the interrupt decimation function
Interrupts	TGRA_3 compare match interrupt (TGIA3) • Interrupt priority level: 15

2.2.2 Sample Program Operation

Figures 9 and 10 show the operation of the sample program.

The MTU2 A/D converter start triggers are used for A/D conversion; TRG4AN is used to start group 0 (AN0 and AN1) and TRG4BN is used to start group 1 (AN2 and AN3). When both the group 0 and group 1 A/D conversions complete, A/D conversion complete interrupt handling is started. The A/D conversion results are acquired by this interrupt handling.

The MTU2 channel 4 A/D converter start request delay function is used to generate the two A/D converter start triggers (TRG4AN and TRG4BN).

These trigger start timings can be modified by changing the settings of the timer A/D converter start request buffer registers (TADCOBRA_4 and TADCOBRB_4). The TADCOBRA_4 and TADCOBRB_4 registers are updated during TGRA3 compare match interrupt handling, which occurs once each MTU2 PWM carrier period.

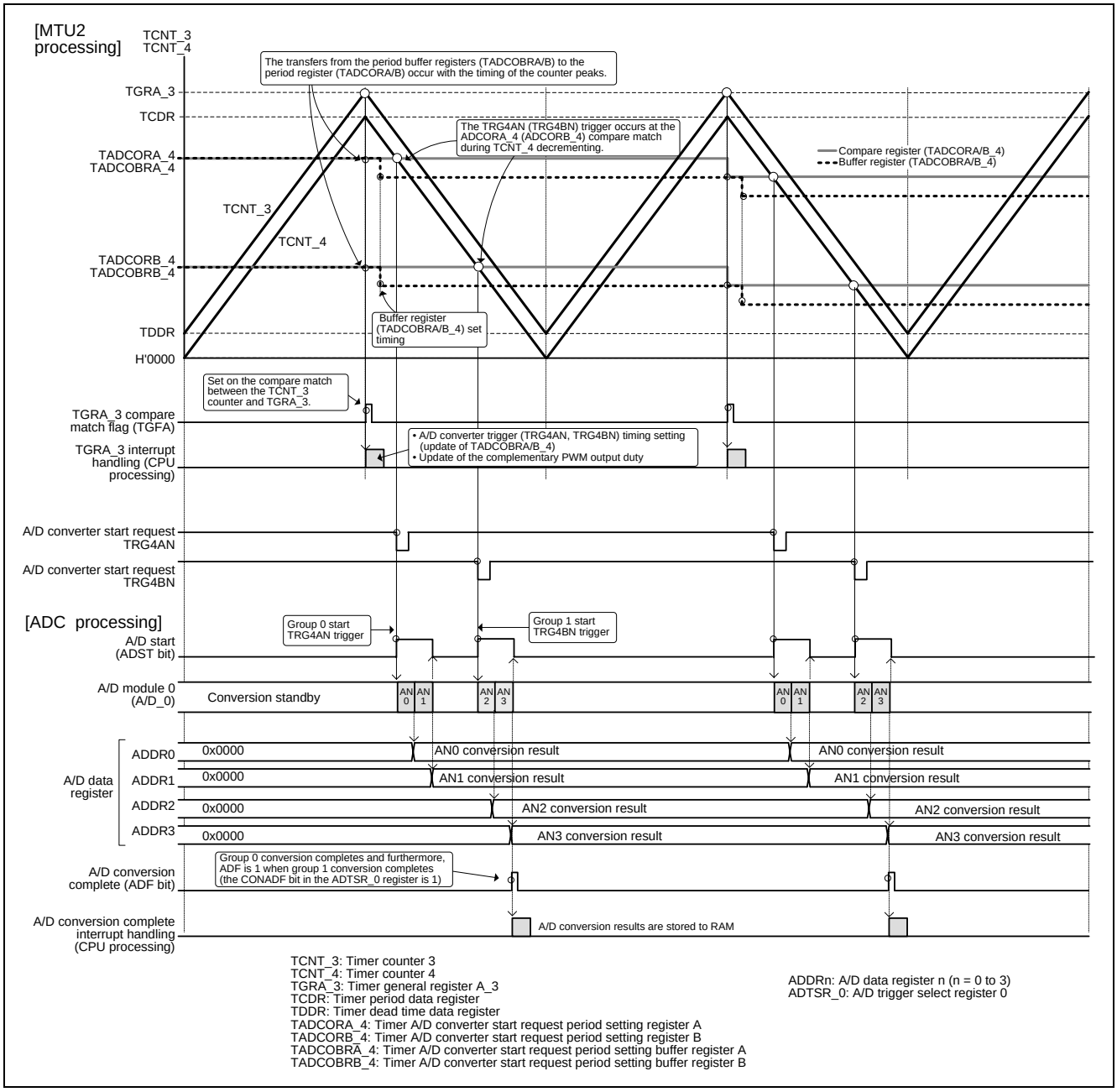


Figure 9 Sample Program Operation (Two-channel scan mode A/D conversion)

Here, MTU2 channels 3 and 4 are set to complementary PWM mode 3. A 3-phase complementary PWM output with dead time (short-circuit prevention period) is generated and a total of six PWM outputs are produced including positive phase and reverse phase signals. The active level for these PWM outputs is the low level. Also, a toggle output synchronized with the PWM period is output from the TIOC3A pin.

The TGRA3 compare match interrupt is generated with the timing of the TCNT counter peak each PWM carrier period. The 3-phase PWM output duty setting is updated during interrupt handling.

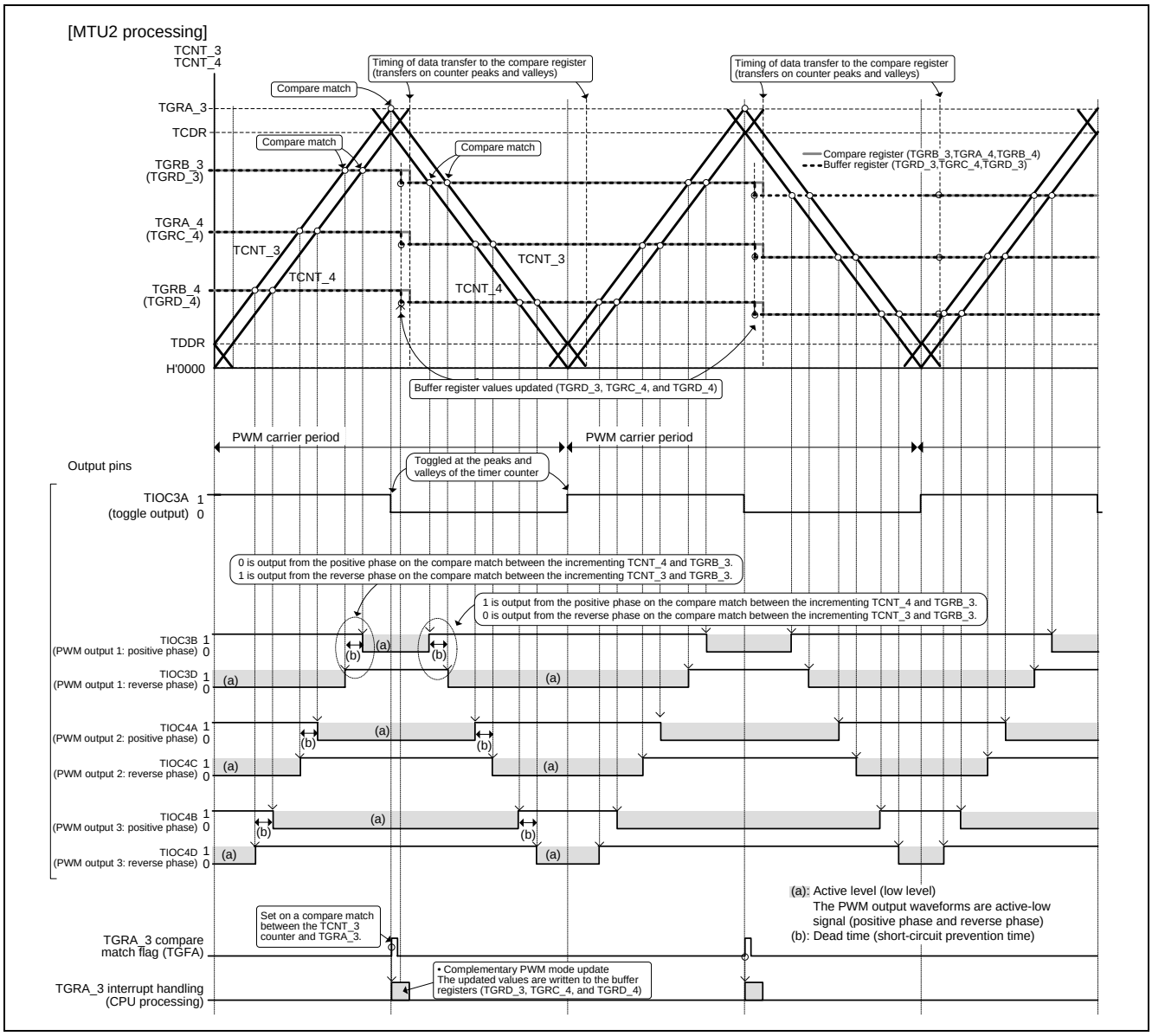


Figure 10 Sample Program Operation (MTU2 complementary PWM mode)

2.3 Sample Program Structure

2.3.1 File Structure

Table 6 lists the files in the sample program. Files generated automatically by the integrated development environment are not shown.

Table 6 File Structure

File	Description	Notes
main.c	Main module	Main processing and INTC initialization
adc.c	ADC control module	ADC initialization and interrupt handling
mtu2.c	MTU2 control module	MTU2 and PFC initialization and interrupt handling

2.3.2 Constants

Table 7 lists the constants used in the sample program.

Table 7 Constants Used in the Sample Program

Constant	Setting Value	Description
C_CYCLE	5000 or 6250	One half of the MTU2 PWM carrier period (1/2 of 500 µs) SH7239A: 5000 / SH7239B: 6250
DEAD_TIME	80 or 100	MTU2 PWM dead time (4 µs) SH7239A: 80 / SH7239B: 100
PUL_CYCLE	PUL_CYCLE + DEAD_TIME	Maximum value for TCNT_3
PUL_DUTY_MIN	PUL_CYCLE * 5 / 100	Minimum value for the PWM output active time (5% duty)
PUL_DUTY_MAX	PUL_CYCLE * 95 / 100	Maximum value for the PWM output active time (95% duty)
INITIAL_DUTY_0	PUL_DUTY_MIN	Initial value for PWM output 1 active time (0° phase)
INITIAL_DUTY_120	PUL_DUTY_MIN + (PUL_DUTY_MAX – PUL_DUTY_MIN) * 2 / 3	Initial value for PWM output 1 active time (120° phase)
INITIAL_DUTY_240	PUL_DUTY_MIN + (PUL_DUTY_MAX – PUL_DUTY_MIN) * 2 / 3	Initial value for PWM output 1 active time (240° phase)
AD_TRG_GAP	100	A/D converter start trigger delay cycle

2.3.3 Enumerations and Structures

Figure 11 shows the enumerations and structures used in the sample program.

```
typedef enum
{
    DUTY_UP,
    DUTY_DOWN
} duty_grad_t;

typedef struct
{
    uint16_t    value;
    duty_grad_t gradient;
} duty_info_t;

typedef struct
{
    uint16_t group_A;   /* TRG4AN timing */
    uint16_t group_B;   /* TRG4BN timing */
} ad_trigger_t;
```

Figure 11 Enumerations and Structures Used in the Sample Program

2.3.4 Variables

Table 8 lists the global variables.

Table 8 Global Variables

Type	Variable Name	Usage	Functions in which Used
uint16_t	g_ad_data[4]	Array that holds the results of A/D conversion	INT_AD_ADI0
ad_trigger_t	g_AD_trigger	A/D converter start request timing setting • group_A: Timing for group A • group_B: Timing for group B	mtu2_init INT_MTU2_MTU3_TGI3A
duty_info_t	g_pwm_duty[3]	PWM duty settings • [0]: PWM 1 output (TIOC3B/TIOC3D pins) • [1]: PWM 2 output (TIOC4A/TIOC4C pins) • [2]: PWM 3 output (TIOC4B/TIOC4D pins)	mtu2_init INT_MTU2_MTU3_TGI3A

2.3.5 Functions

Table 9 lists the functions.

Table 9 Functions

Function	Description
main	Main processing
io_intc_init	Interrupt controller initialization
io_ad_init	A/D converter initialization
INT_AD_ADI0	A/D converter conversion complete interrupt handling
io_mtu2_init	Multifunction timer/pulse unit 2 initialization
io_mtu2_pfc_init	PWM output port initialization (pin function controller setup)
Io_mtu2_start	PWM output start processing
INT_MTU2_MTU3_TGI3A	MTU2 channel 3 TRGA_3 compare match interrupt handling

2.3.6 Function Specifications

The specifications of the functions defined in the sample program are shown below.

main

Overview	Main processing
Header	
Declaration	void main(void)
Description	After initializing the ADC, MTU2, PFC and INTC modules, this routine starts PWM output and enters an infinite loop.
Arguments	None
Return values	None

io_intc_init

Overview	Interrupt controller initialization
Header	
Declaration	void io_intc_init(void)
Description	Sets up the INTC registers for ADC and MTU2 interrupts
Arguments	None
Return values	None

io_ad_init

Overview	A/D converter initialization
Header	
Declaration	void io_ad_init(void)
Description	After clearing the ADC module standby state, this function sets the ADC registers.
Arguments	None
Return values	None

INT_AD_ADI0	
Overview	A/D conversion complete interrupt handling
Header	
Declaration	void INT_AD_ADI0(void)
Description	Clears the A/D end flag to 0 and stores the converted data in a global variable.
Arguments	None
Return values	None

io_mtu2_init	
Overview	Multifunction timer/pulse unit 2 initialization
Header	
Declaration	void io_mtu2_init(void)
Description	After clearing the MTU2 module standby mode, this routine sets the MTU2 registers as required.
Arguments	None
Return values	None

io_mtu2_pfc_init	
Overview	PWM output port initialization (pin function controller setup)
Header	
Declaration	void io_mtu2_pfc_init(void)
Description	Sets the PFC registers as required for PWM output.
Arguments	None
Return values	None

io_mtu2_start	
Overview	PWM output start
Header	
Declaration	void io_mtu2_start (void)
Description	Starts PWM output from MTU2.
Arguments	None
Return values	None

INT_MTU2_MTU3_TGI3A	
Overview	MTU2 channel 3 TRGA_3 compare match interrupt handling
Header	
Declaration	void INT_MTU2_MTU3_TGI3A(void)
Description	After clearing the compare match interrupt flag, this routine updates the PWM 1 to PWM 3 duty and the A/D converter timing.
Arguments	None
Return values	None

2.4 Sample Program Processing

2.4.1 Main Processing

Figure 12 shows the flowchart for the main processing routine.

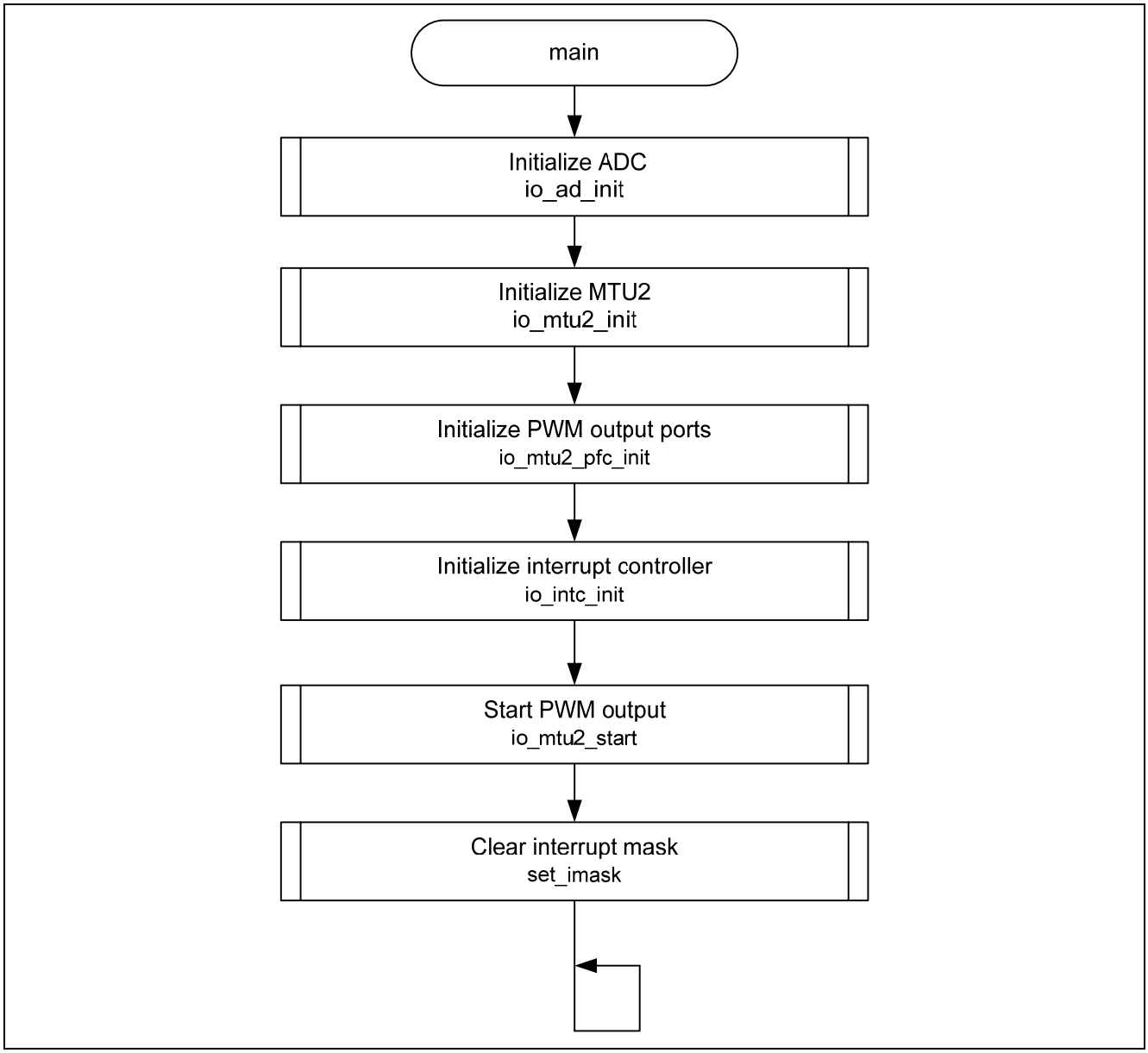


Figure 12 Main Processing

2.4.2 Interrupt Controller Initialization

Figure 13 shows the flowchart for interrupt controller initialization.

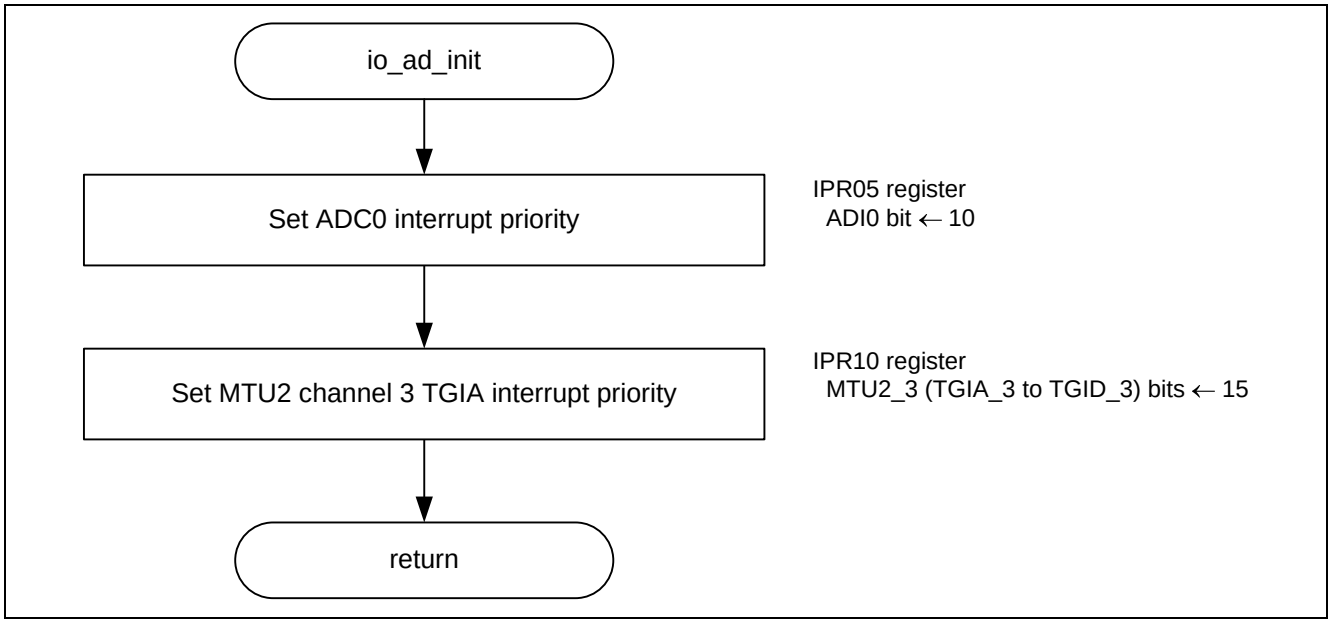


Figure 13 Interrupt Controller Initialization

2.4.3 A/D Converter Initialization

Figure 14 shows the flowchart for A/D converter initialization.

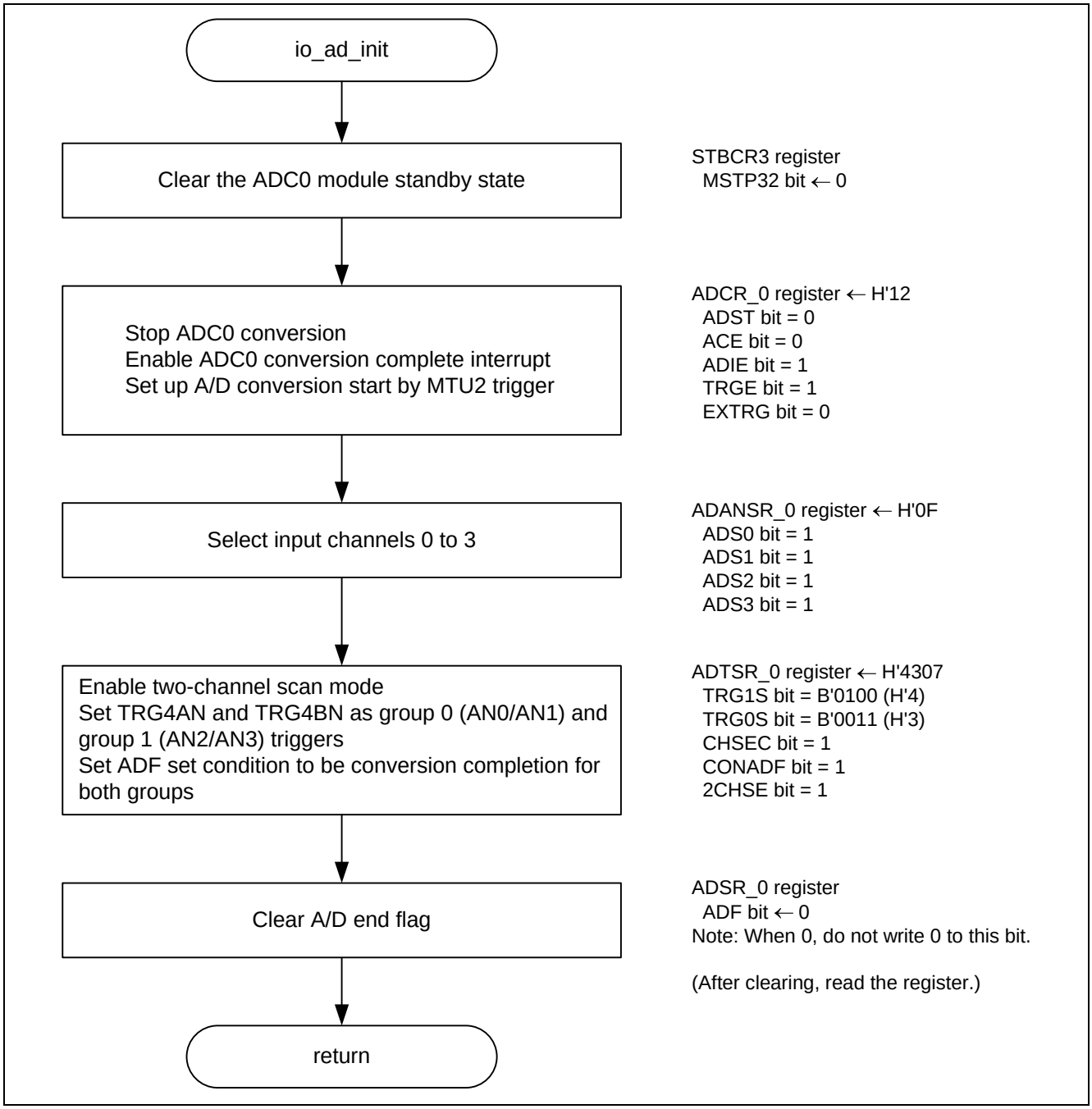


Figure 14 A/D Converter Initialization

2.4.4 A/D Conversion Complete Interrupt Handling

Figure 15 shows the flowchart for A/D conversion complete interrupt handling.

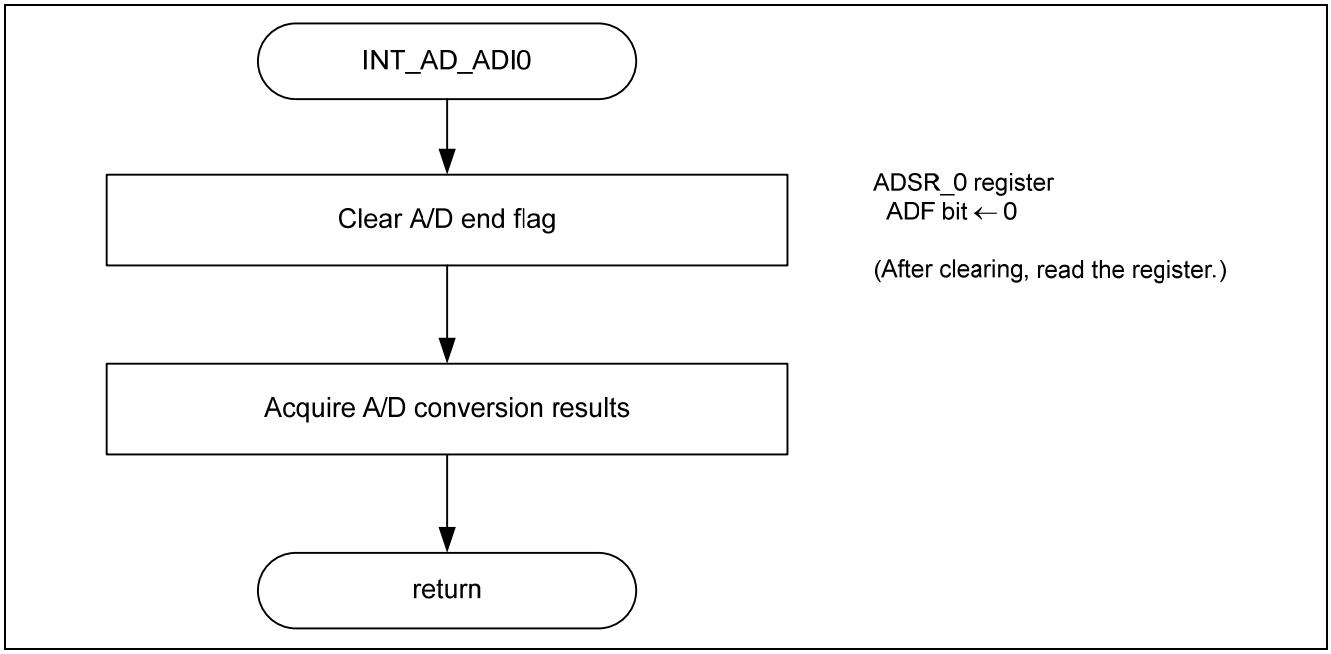


Figure 15 A/D Conversion Complete Interrupt Handling

2.4.5 Multifunction Timer/Pulse Unit 2 Initialization

Figure 16 shows the flowchart for multifunction timer/pulse unit 2 initialization.

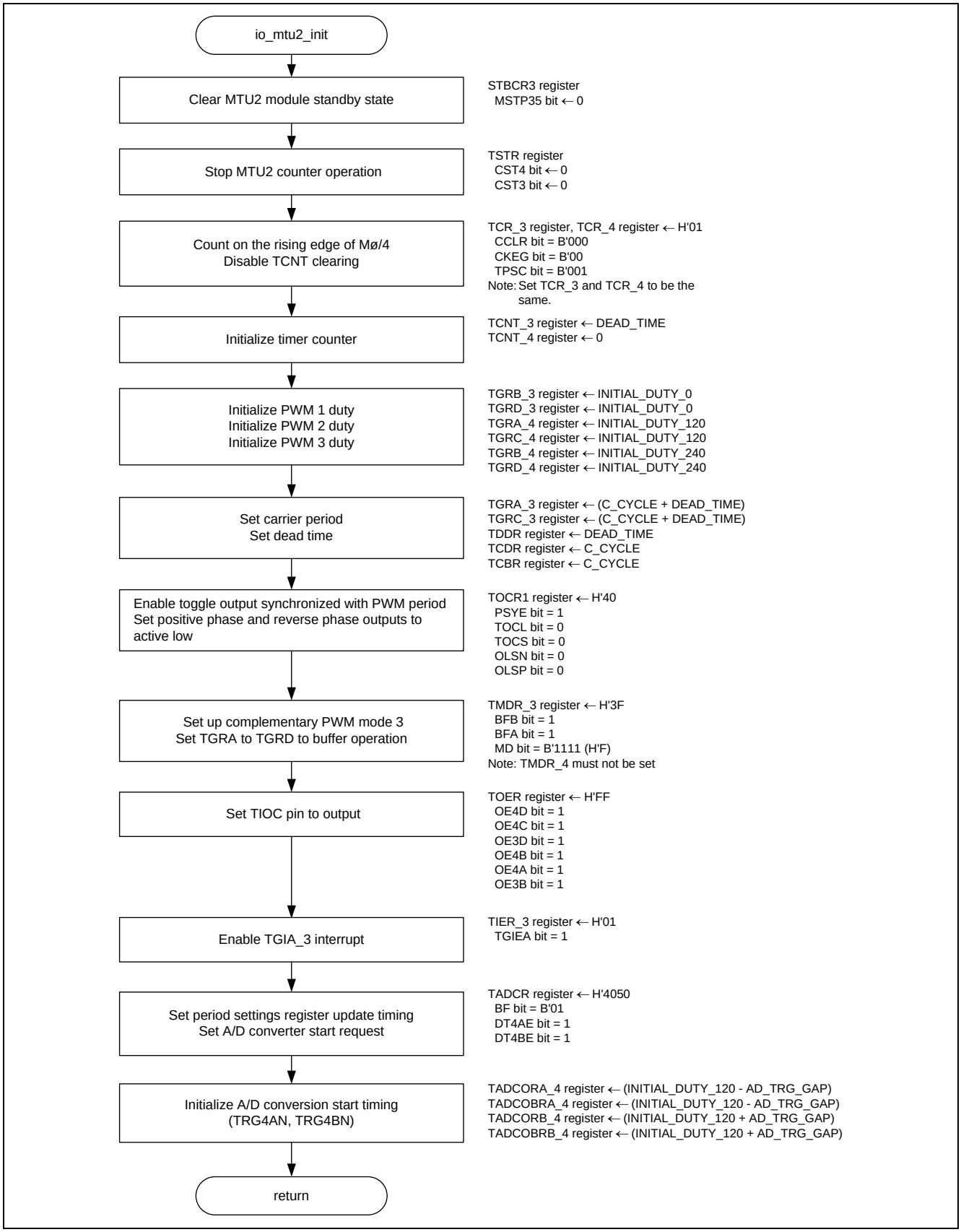


Figure 16 Multifunction Timer/Pulse Unit 2 Initialization

2.4.6 PWM Output Port Initialization

Figure 17 shows the flowchart for PWM output port initialization.

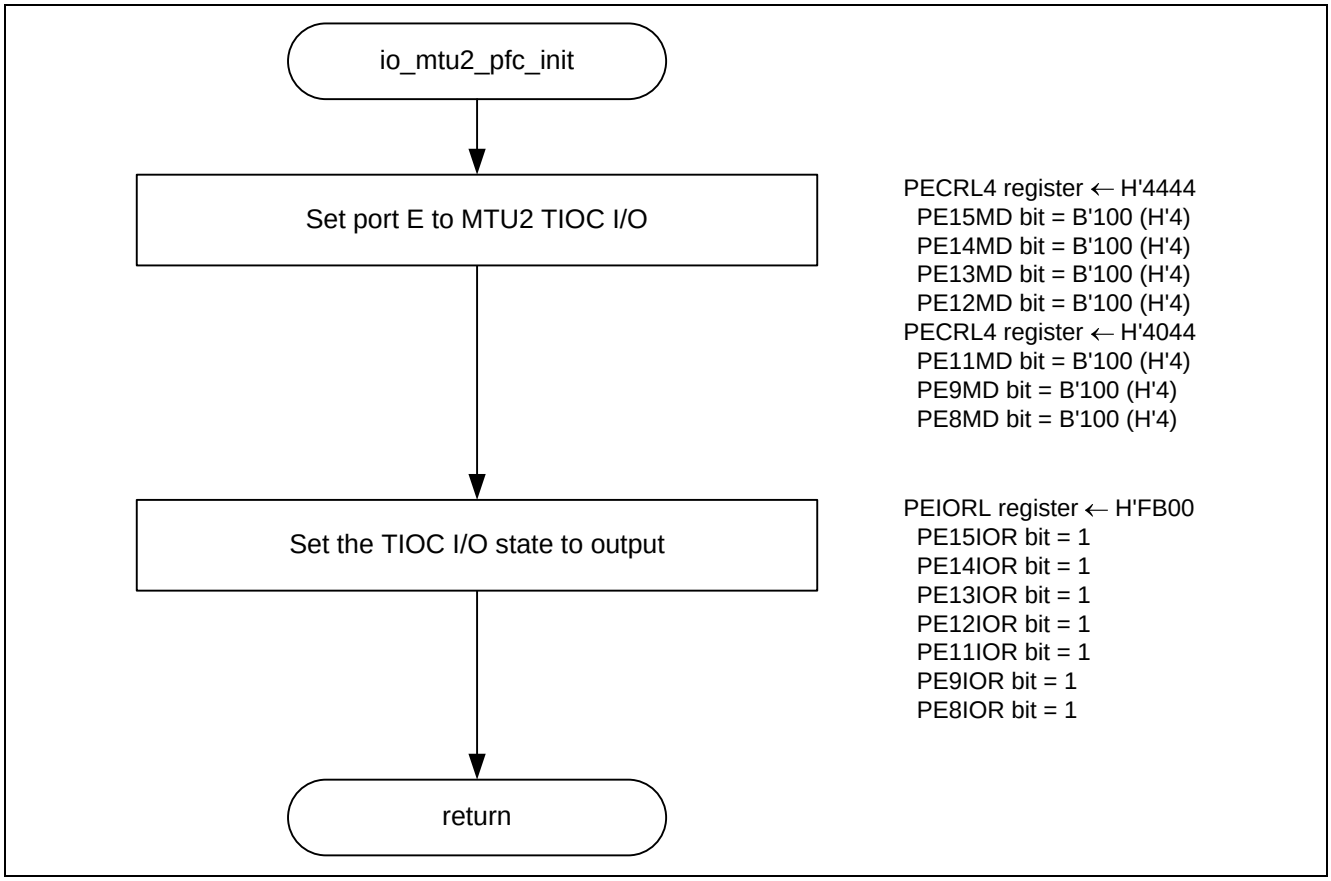


Figure 17 PWM Output Port Initialization

2.4.7 PWM Output Start Processing

Figure 18 shows the flowchart for PWM output start processing.

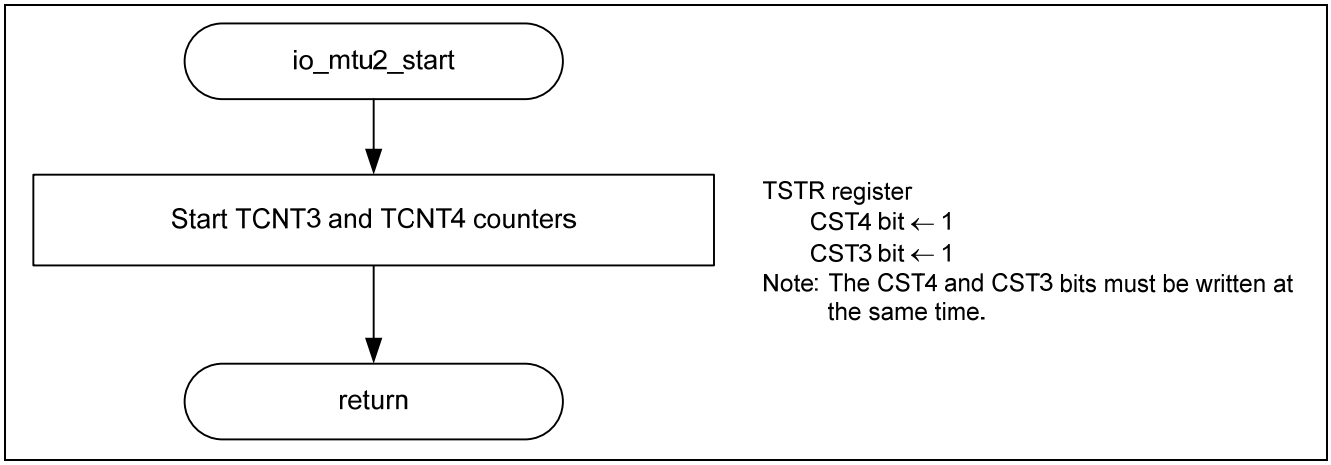


Figure 18 PWM Output Start Processing

2.4.8 MTU2 Channel 3 TGRA_3 Compare Match Interrupt Handling

Figure 19 shows the flowchart for MTU2 channel 3 TGRA_3 compare match interrupt handling.

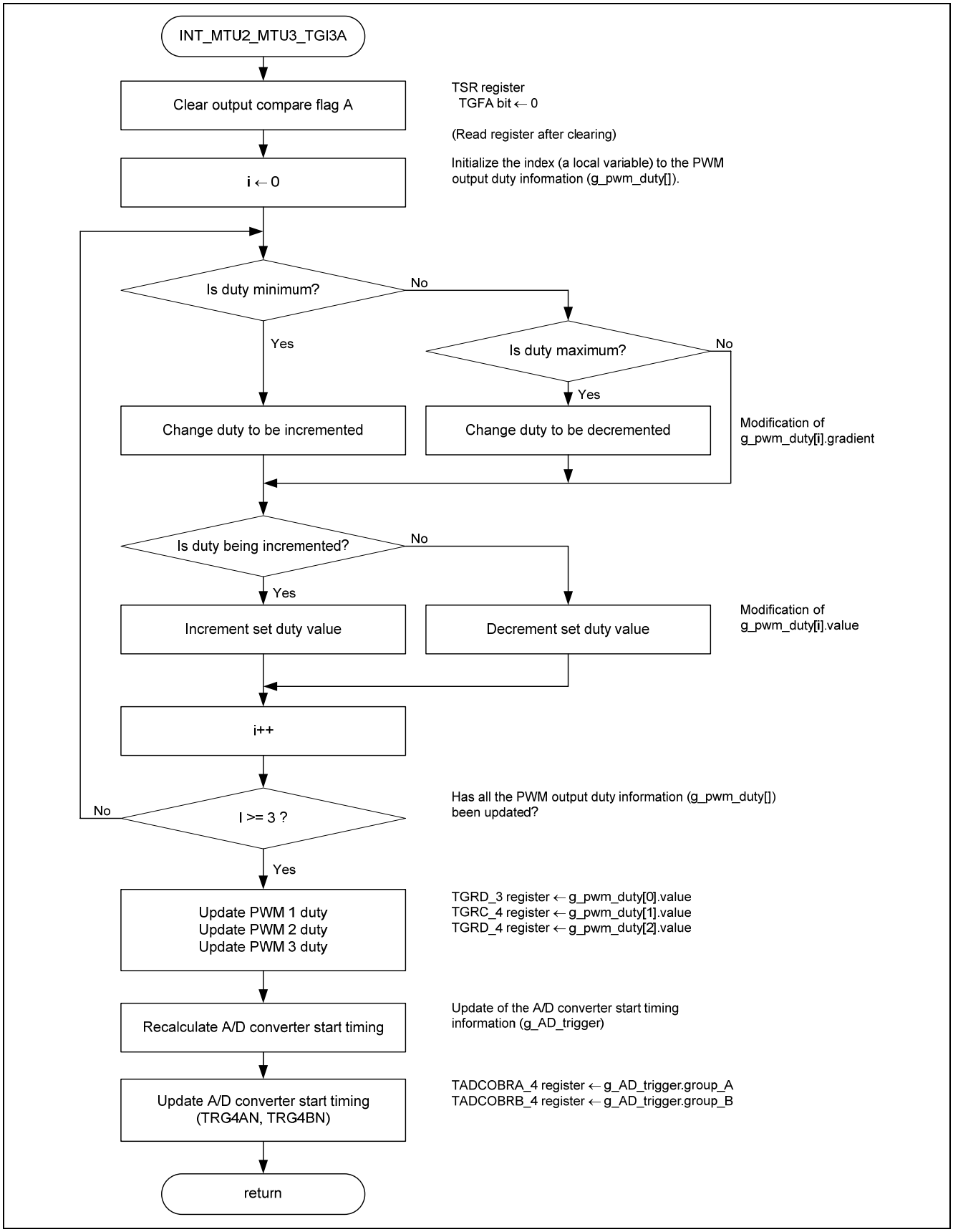


Figure 19 MTU2 Channel 3 TGRA_3 Compare Match Interrupt Handling

2.5 Sample Program Register Settings

2.5.1 A/D Converter (ADC)

Table 10 lists the A/D converter (ADC) register settings.

Table 10 A/D Converter (ADC) Register Settings

Register Name	Address	Setting Value	Function
A/D control register 0 (ADCR_0)	H'FFFF E800	H'12	ADST = 0: A/D conversion stopped ACE = 0: ADDR automatic clear disabled ADIE = 1: A/D conversion complete interrupt enabled TRGE = 1: A/D conversion start by external trigger or MTU2/MTU2S enabled EXTRG = 0: A/D conversion start by MTU2/MTU2S selected
A/D analog channel select register 0 (ADANSR_0)	H'FFFF E820	H'0F	ADS0 = 1: AN0 selected ADS1 = 1: AN1 selected ADS2 = 1: AN2 selected ADS2 = 1: AN3 selected
A/D trigger select register 0 (ADTSR_0)	H'FFFF E930	H'4307	• TRG1S[3:0] = B'0100: TRG4BN (MTU2) set to be the trigger for group 1 • TRG0S[3:0] = B'0011: TRG4AN (MTU2) set to be the trigger for group 0 • CHSEC = 1: Channel selection in two-channel scan mode — Group 0 (AN0 and AN1) — Group 1 (AN2 and AN3) • CONADF = 1: ADF is set when both group 0 and group 1 conversions have completed • 2CHSE = 1: Two-channel scan mode enabled

2.5.2 Multifunction Timer/Pulse Unit 2 (MTU2)

Tables 11 to 13 list the register settings for multifunction timer/pulse unit 2 (MTU2).

Table 11 Multifunction Timer/Pulse Unit 2 (MTU2) Register Settings (1)

Register	Address	Setting Value	Function
Timer control register 3 (TCR_3)	H'FFFE 4200	H'01	CCLR[2:0] = B'000: TCNT clear disabled CKEG[1:0] = B'00: Count on rising edges TPSC[2:0] = B'001: TCNT is incremented on Mϕ/4.
Timer control register 4 (TCR_4)	H'FFFE 4201		CCLR[2:0] = B'000: TCNT clear disabled CKEG[1:0] = B'00: Count on rising edge TPSC[2:0] = B'001: TCNT is incremented on Mϕ/4. (The same settings as TCR_3 in complementary PWM mode)
Timer counter 3 (TCNT_3)	H'FFFE 4210	D'80 or D'100	Initialized to the TDDR set value in complementary PWM mode. • Mϕ = 80 MHz (SH7239A): D'80 • Mϕ = 100 MHz (SH7239B): D'100
Timer counter 4 (TCNT_4)	H'FFFE 4212	H'0000	Initialized to H'0000
Timer general register A 3 (TGRA_3)	H'FFFE 4218	D'5080 or D'6350	• Upper limit for TCNT_3 in complementary PWM mode • Set to (carrier period/2 + dead time). — Mϕ = 80 MHz (SH7239A): D'5080 — Mϕ = 100 MHz (SH7239B): D'6250
Timer general register C 3 (TGRC_3)	H'FFFE 4224	D'5080 or D'6350	TGRA_3 buffer register in complementary PWM mode (Set to the same value as TGRA_3 at initialization.)
Timer general register B 3 (TGRB_3)	H'FFFE 421A	D'254 or D'317	• PWM output 1 compare register in complementary PWM mode • Sets the PWM duty initial output value. — Mϕ = 80 MHz (SH7239A): D'254 — Mϕ = 100 MHz (SH7239B): D'317
Timer general register D 3 (TGRD_3)	H'FFFE 4226	D'254 to D'4826 or D'317 to D'6032	• TGRB_3 buffer register in complementary PWM mode • Sets the PWM duty update value. — Mϕ = 80 MHz (SH7239A): D'254 to D'4826 — Mϕ = 100 MHz (SH7239B): D'317 to D'6032 (Set to the same value as TGRB_3 at initialization.)
Timer general register A 4 (TGRA_4)	H'FFFE 421C	D'3302 or D'4127	• PWM output 2 compare register in complementary PWM mode • Sets the PWM duty initial output value. — Mϕ = 80 MHz (SH7239A): D'3302 — Mϕ = 100 MHz (SH7239B): D'4127
Timer general register C 4 (TGRC_4)	H'FFFE 4228	D'254 to D'4826 or D'317 to D'6032	• TGRA_4 buffer register in complementary PWM mode • Sets the PWM duty update value. — Mϕ = 80 MHz (SH7239A): D'254 to D'4826 — Mϕ = 100 MHz (SH7239B): D'317 to D'6032 (Set to the same value as TGRA_4 at initialization.)

Table 12 Multifunction Timer/Pulse Unit 2 (MTU2) Register Settings (2)

Register	Address	Setting Value	Function
Timer general register B 4 (TGRB_4)	H'FFFE 421E	D'3302 or D'4127	• PWM output 3 compare register in complementary PWM mode • Sets the PWM duty initial output value. — Mϕ = 80 MHz (SH7239A): D'3302 — Mϕ = 100 MHz (SH7239B): D'4127
Timer general register D 4 (TGRD_4)	H'FFFE 422A	D'254 to D'4826 or D'317 to D'6032	• TGRB_4 buffer register in complementary PWM mode • Sets the PWM duty update value. — Mϕ = 80 MHz (SH7239A): D'254 to D'4826 — Mϕ = 100 MHz (SH7239B): D'317 to D'6032 (Set to the same value as TGRB_4 at initialization.)
Timer dead time data register (TDDR)	H'FFFE 4216	D'80 or D'100	(Only used in complementary PWM mode) Sets the dead time value (the offset value for TCNT_4 relative to TCNT_3). • Mϕ = 80 MHz (SH7239A): D'80 • Mϕ = 100 MHz (SH7239B): D'100
Timer period data register (TCDR)	H'FFFE 4214	D'5000 or D'6250	(Only used in complementary PWM mode) Sets the TCNT_4 upper limit (carrier frequency/2). • Mϕ = 80 MHz (SH7239A): D'5000 • Mϕ = 100 MHz (SH7239B): D'6250
Timer period buffer register (TCBR)	H'FFFE 4222	D'5000 or D'6250	(Only used in complementary PWM mode) • Buffer register for TCDR • Set to the same value as TCDR.
Timer output control register 1 (TOCR1)	H'FFFE 420E	H'40	• PSYE = 1: Toggle output synchronized with the PWM period enabled • TOCL = 0: Writing to the TOCS, OLSN, and OLSP bits enabled • TOCS = 0: Setting TOCR1 selected • OLSN = 0: Reverse phase output level selected — Initial output = high, active level = low. • OLSP = 0: Positive phase output level selected — Initial output = high, active level = low.
Timer mode register 3 (TMDR_3)	H'FFFE 4202	H'3F	• BFB = 1: Buffer operation for TGRB and TGRD • BFA = 1: Buffer operation for TGRA and TGRC • MD[3:0] = B'1111: Complementary PWM mode 3
Timer mode register 4 (TMDR_4)	H'FFFE 4203	—	• When channel 3 is set to complementary PWM mode, channel 4 automatically follows the channel 3 setting. • Do not set TMDR_4 when complementary PWM mode is used.
Timer output master enable register (TOER)	H'FFFE 420A	H'FF	OE4D = 1: MTU2 output from the TIOC4D pin enabled OE4C = 1: MTU2 output from the TIOC4C pin enabled OE3D = 1: MTU2 output from the TIOC3D pin enabled OE4B = 1: MTU2 output from the TIOC4B pin enabled OE4A = 1: MTU2 output from the TIOC4A pin enabled OE3B = 1: MTU2 output from the TIOC3B pin enabled
Timer interrupt enable register 3 (TIER_3)	H'FFFE 4208	H'01	TGIEA = 1: interrupt requests due to the TGFA bit (TGIA_3) enabled

Table 13 Multifunction Timer/Pulse Unit 2 (MTU2) Register Settings (3)

Register	Address	Setting Value	Function
Timer A/D converter start request control register (TADCR)	H'FFFE 4240	H'4050	• BF[1:0] = B'01: Transfers the period setting buffer register value to the period setting register at the TCNT_4 peak. • UT4AE = 0: A/D converter start requests (TRG4AN) when TCNT_4 is being incremented disabled • DT4AE = 1: A/D converter start requests (TRG4AN) when TCNT_4 is being decremented enabled • UT4BE = 0: A/D converter start requests (TRG4BN) when TCNT_4 is being incremented disabled • DT4BE = 1: A/D converter start requests (TRG4BN) when TCNT_4 is being decremented enabled • ITA3AE = ITA4VE = ITB3AE = ITB4VE = 0: Operation of A/D converter start requests (TRG4AN and TRG4BN) and the TGIA_3 and TCIV_4 interrupt decimation function enabled
Timer A/D converter start request period setting register A 4 (TADCORA_4)	H'FFFE 4244	D'3202 or D'4027	• The A/D converter start request timing register for the A/D converter start request delay function (TRG4AN is generated on a match with TCNT_4) • Initialized with (the set value of TGRA_4 minus D'100).
Timer A/D converter start request period setting buffer register A 4 (TADCOBRA_4)	H'FFFE 4248	D'154 to D'4726 or D'217 to D'5932	• The buffer register for TADCORA_4 • Set to the TADCORA_4 update value (the set value of TGRC_4 minus D'100) (Set to the same value as TADCORB_4 at initialization)
Timer A/D converter start request period setting register B 4 (TADCORB_4)	H'FFFE 4246	D'3402 or D'4227	• The A/D converter start request timing register for the A/D converter start request delay function (TRG4BN is generated on a match with TCNT_4) • Initialized with (the set value of TGRA_4 plus D'100).
Timer A/D converter start request period setting buffer register B 4 (TADCOBRB_4)	H'FFFE 424A	D'354 to D'4926 or D'417 to D'6132	• The buffer register for TADCORB_4 • Set to the TADCORB_4 update value (the set value of TGRC_4 plus D'100) (Set to the same value as TADCORB_4 at initialization)
Timer start register (TSTR)	H'FFFE 4280	H'00	At initialization: CST4 = 0: Stops the TCNT_4 count operation. CST3 = 0: Stops the TCNT_3 count operation. CST2 = 0: Stops the TCNT_2 count operation. CST1 = 0: Stops the TCNT_1 count operation. CST0 = 0: Stops the TCNT_0 count operation.
		H'C0	At PWM output start: CST4 = 1: TCNT_4 counting operates CST3 = 1: TCNT_3 counting operates (CST4 and CST3 must be set at the same time.)

2.5.3 Interrupt Controller (INTC)

Table 14 lists the interrupt controller register settings.

Table 14 Interrupt Controller (INTC) Register Settings

Register	Address	Setting Value	Function
Interrupt priority level setting register 05 (IPR05)	H'FFFE 0820	H'00A0	• Bits 7 to 4 = B'1010 Sets the ADI0 interrupt level to 10. • Bits 3 to 0 = B'000 Disables the ADI1 interrupt.
Interrupt priority level setting register 10 (IPR10)	H'FFFE 0C08	H'00F0	• Bit 15 to 12 = B'0000 Disables the MTU2_2 (TGIA_2, TGIB_2) interrupt. • Bit 11 to 8 = B'0000 Disables the MTU2_2 (TCIV_2, TCIU_2) interrupt. • Bit 7 to 4 = B'1111 Sets the MTU2_3(TGIA_3 to TGID_3) interrupt level to 15. • Bit 3 to 0 = B'0000 Disables the MTU2_3 (TCIV_3) interrupt.

2.5.4 Pin Function Controller (PFC)

Table 15 lists the pin function controller register settings.

Table 15 Pin Function Controller Register Settings

Register	Address	Setting Value	Function
Port E control register L4 (PECRL4)	H'FFFE 3A10	H'4444	PE15MD[2:0] = B'100: TIOC4D I/O selected PE14MD[2:0] = B'100: TIOC4C I/O selected PE13MD[2:0] = B'100: TIOC4B I/O selected PE12MD[2:0] = B'100: TIOC4A I/O selected
Port E control register L3 (PECRL3)	H'FFFE 3A12	H'4044	PE11MD[2:0] = B'100: TIOC3D I/O selected PE10MD[2:0] = B'000: PE10 I/O (port) selected PE9MD[2:0] = B'100: TIOC3B I/O selected PE8MD[2:0] = B'100: TIOC3A I/O selected
Port E IO register L (PEIORL)	H'FFFE 3A06	H'FB00	PE15IOR = 1: TIOC4D (PE15) set to output PE14IOR = 1: TIOC4C (PE14) set to output PE13IOR = 1: TIOC4B (PE13) set to output PE12IOR = 1: TIOC4A (PE12) set to output PE11IOR = 1: TIOC3D (PE11) set to output PE10IOR = 0: PE10 set to input PE9IOR = 1: TIOC3B (PE9) set to output PE8IOR = 1: TIOC3A (PE8) set to output PE7IOR to PE0IOR = 0: PE7 to PE0 set to input

3. Reference Documents

- Software Manual
  SH-2A, SH2A-FPU User's Manual: Software, Rev.4.00 (R01US0031EJ)
  (The latest version can be downloaded from the Renesas Electronics Web site.)
- SH7239 Group, SH7237 Group User's Manual: Hardware, Rev.1.00 (R01UH0086EJ)
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Revision Record

Rev.	Date	Description	
		Page	Summary
1.00	Jun.15.12	—	First edition issued

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The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins
   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.
   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.
2. Processing at Power-on
   The state of the product is undefined at the moment when power is supplied.
   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.
3. Prohibition of Access to Reserved Addresses
   Access to reserved addresses is prohibited.
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4. Clock Signals
   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.
   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.
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