SH7239 Group

A/D Converter
— Single-Cycle Scan Mode A/D Conversion Sample Program

R01AN1148EJ0100
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Introduction

This application note describes a sample program that performs single-cycle scan mode A/D conversion using the A/D converter.

Target Device

SH7239A/SH7239B

When using the sample code presented in this application note with other microcontrollers, modify the code according to the specifications of the microcontroller used and test thoroughly.

Contents

1. Introduction

1.1 Specifications

- This sample application performs A/D conversion using the A/D converter (ADC) in single-cycle scan mode.
- A/D conversion is performed using analog input channels 0 to 3 (AN0 to AN3) and the conversion data for three cycles is stored in RAM.

1.2 Functions Used

A/D converter (ADC)

1.3 Conditions

Microcontroller	SH7239A / SH7239B
Operating frequencies	Internal clock: 160 MHz / 100 MHz Bus clock: 40 MHz / 50 MHz Peripheral clock: 40 MHz / 50 MHz A/D clock: 40 MHz / 50 MHz
MCU operating mode	Single-chip mode
Integrated development environment	Renesas Electronics High-performance Embedded Workshop Ver.4.07.00
C compiler	Renesas Electronics SuperH RISC engine Family C/C++ Compiler Package Ver.9.03 Release02
Compiler options	-cpu=sh2afpu -fpu=single -include="$(WORKSPDIR)\inc" -object="$(CONFIGDIR)\$(FILELEAF).obj" -debug -gbr=auto –chgincpath -errorpath -global_volatile=0 -opt_range=all -infinite_loop=0 -del_vacant_loop=0 -struct_alloc=1 –nologo

1.4 Related Application Notes

SH7239 Group Example of Initialization (R01AN0297EJ)

2. Sample Application Description

This sample application uses the A/D converter (ADC) to perform A/D conversions in single-cycle scan mode 3 times and stores the resulting data in RAM.

2.1 Overview of Functions Used

The A/D converter is a 12-bit successive-approximation A/D converter module, and these microcontrollers include three of these modules (A/D_0, A/D_1, and A/D_2). A/D converter operating modes include single-cycle scan mode, continuous scan mode, and two-channel scan mode.

In single-cycle scan mode, the ADC module converts one or more channels once each and then terminates. The ADST bit is automatically cleared to 0. In contrast, in continuous scan mode, the specified one or more channels are repeatedly scanned until the ADST bit is cleared to 0 in software. And in two-channel scan mode, 4 analog input channels are divided into two groups (group 0 and group 1) and A/D conversion of the specified channels is performed once each by the selected triggers for group 0 and group 1, after which A/D converter operation terminates.

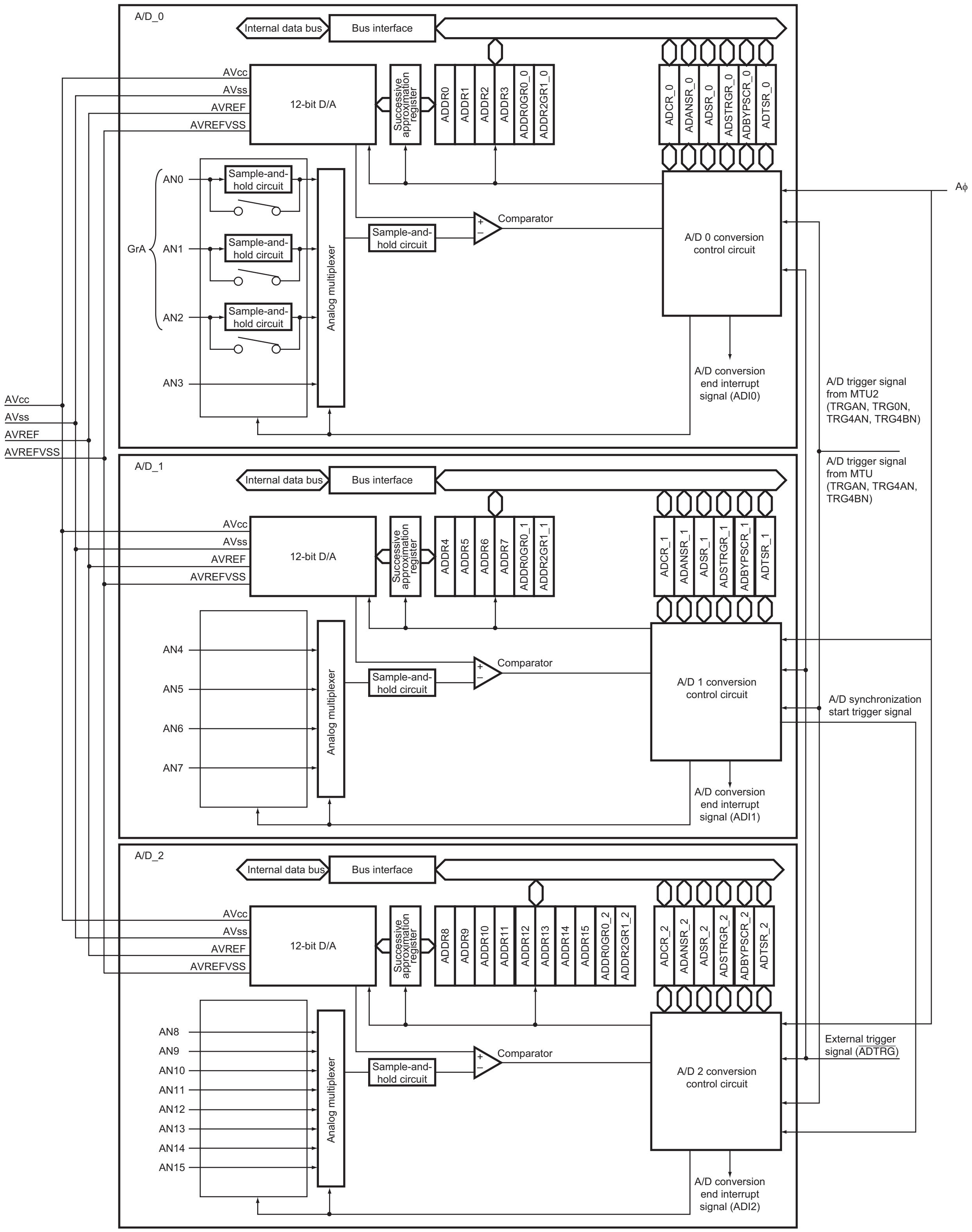
Furthermore, channels 0 to 2 each have a dedicated sample-and-hold circuit, and multiple channels can be sampled at the same time.

Table 1 lists the details of the ADC module and figure 1 shows its block diagram.

For detailed information on the ADC, see the A/D Converter section in the SH7239 Group, SH7237 Group User's Manual: Hardware.

Table 1 ADC Module Overview

Item	Description
Resolution	12 bits
Conversion speed	A minimum of 1.25 µs per channel (when the AD clock is 40 MHz) A minimum of 1.0 µs per channel (when the AD clock is 50 MHz)
Number of modules	3 modules
Number of input channels	16 channels total • A/D_0: 4 channels (ch0 to ch3) • A/D_1: 4 channels (ch4 to ch7) • A/D_2: 8 channels (ch8 to ch15)
Operating modes	Single-channel scan mode Continuous scan mode Two-channel scan mode
Sample-and-hold function	Sample-and-hold circuits for each module • Common to ch0 to ch3: 1 circuit • Common to ch4 to ch7: 1 circuit • Common to ch8 to ch15: 1 circuit Dedicated sample-and-hold circuits for each channel • ch0 to ch2: One circuit for each channel (3 circuits, total)
A/D conversion start sources	Software: Setting the ADST bit Timers: MTU2 (TRGAN, TRG0N, TRG4AN, or TRG4BN) MTU2S (TRGAN, TRG4AN, or TRG4BN) External trigger: $\overline{\text{ADTRG}}$ (an IC pin)



[Legend]

ADDR: A/D data register
ADCR: A/D control register
ADANSR: A/D analog input channel select register
ADSR: A/D status register
ADSTRGR: A/D start trigger select register
ADBYPSCR: A/D bypass control register
ADTSR: A/D trigger select register
ADDR0GR0: A/D group-0 data-0 register
ADDR2GR1: A/D group-1 data-2 register
GrA: Group A

Figure 1 Block Diagram of A/D Converter

2.2 Sample Program Operation

2.2.1 Sample Program Operational Settings

Table 2 lists the settings used by the sample program.

The sample program sets up single-cycle scan mode for the ADC A/D module 0 (A/D_0) and starts A/D conversion in software.

Table 2 ADC Settings

Item	Description
Module and input pin used	A/D_0 (AN0, AN1, AN2, AN3)
Conversion mode	Single-cycle scan mode
Automatic ADDR clear	Disabled
Interrupts	Unused
A/D conversion start	Started by writing to the ADST bit in software
Dedicated per-channel sample-and-hold circuits	Unused

2.2.2 Sample Program Operation

Figure 2 shows the operation of the sample program.

A/D conversion is started by writing 1 to the ADST bit in the ADCRR_0 register in software. When all of the A/D conversions for AN0 to AN3 have completed, the A/D conversion complete flag is set to 1. The ADST bit is automatically cleared to 0 and A/D conversion terminates. The sample program verifies the completion of A/D conversion by polling the A/D conversion complete flag and acquires the result from the A/D data register. This processing is repeated three times.

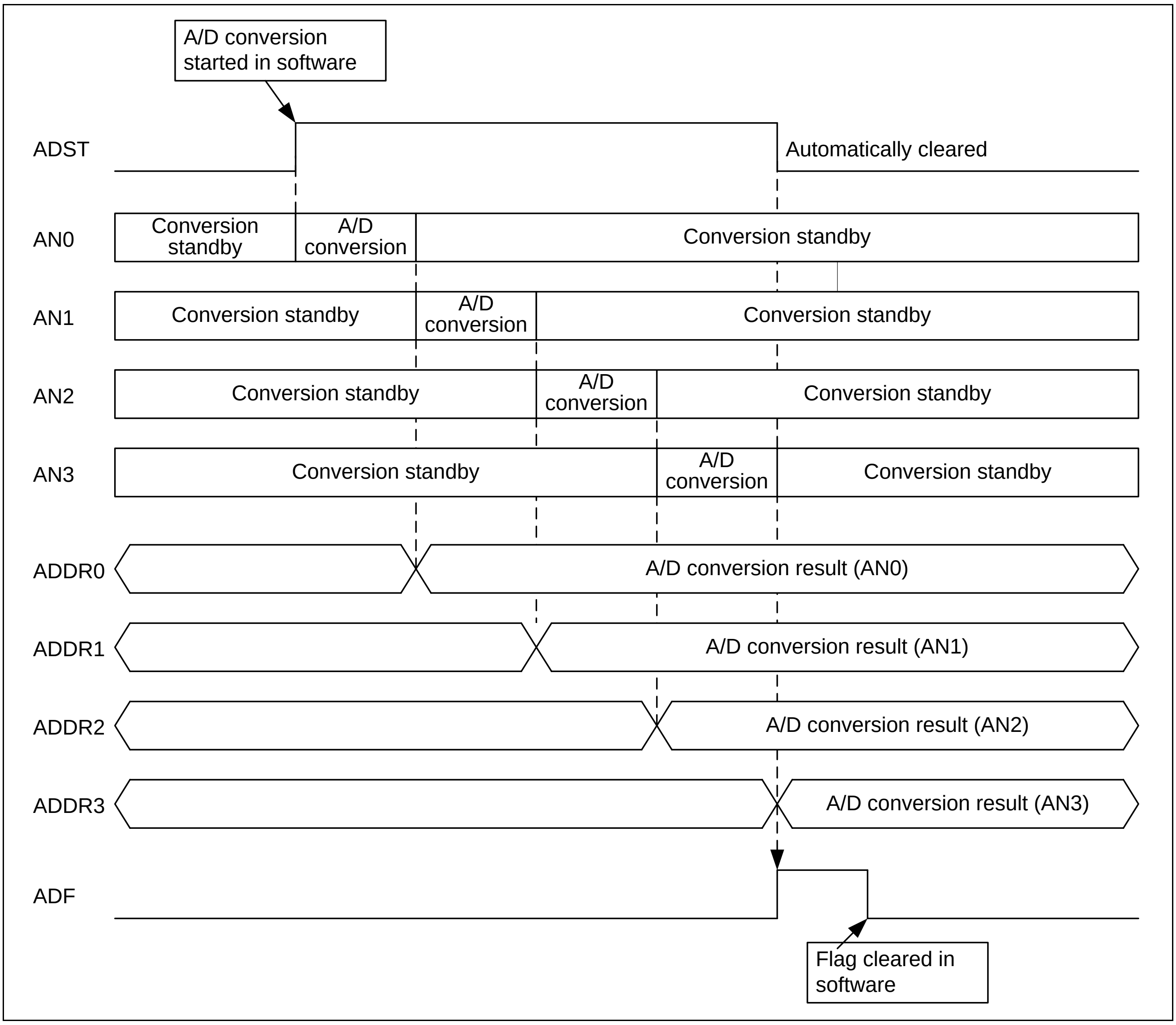


Figure 2 Sample Program Operation

2.3 Sample Program Structure

2.3.1 File Structure

Table 3 lists the files in the sample program. Files generated automatically by the integrated development environment are not shown.

Table 3 File Structure

File	Description	Notes
main.c	Main module	Initialization and A/D conversion processing

2.3.2 Constants

Table 4 lists the constants used in the sample program.

Table 4 Constants Used in the Sample Program

Constant	Setting Value	Description
AD_COUNT	3	Used in the array declaration for storage of A/D conversion results (conversion count)
CH_COUNT	4	Used in the array declaration for storage of A/D conversion results (channel count)

2.3.3 Variables

Table 5 lists the global variables.

Table 5 Global Variables

Type	Variable Name	Usage	Functions in which Used
uint16_t	g_ad_data[AD_COUNT][CH_COUNT]	Array that stores the results of A/D conversion	main

2.3.4 Functions

Table 6 lists the functions.

Table 6 Functions

Function	Description
main	Main processing
io_ad_init	A/D converter initialization
io_ad_1cyc_scan	A/D conversion processing

2.3.5 Function Specifications

The specifications of the functions defined in the sample program are shown below.

main

Overview	Main processing
Header	
Declaration	void main(void)
Description	After initializing the ADC, this function performs 3 A/D conversions and stores the results in a variable in RAM. After that, it enters an infinite loop.
Arguments	None
Return values	None

io_ad_init

Overview	A/D converter initialization
Header	
Declaration	void io_ad_init(void)
Description	After clearing the ADC module standby state, this function sets the ADC registers.
Arguments	None
Return values	None

io_ad_1cyc_scan

Overview	A/D conversion processing	
Header		
Declaration	void io_ad_1cyc_scan(uint16_t * ad_buf)	
Description	After starting the A/D converter and waiting for conversion to complete, this function clears the A/D end flag to 0 and stores the converted data at the address specified by the argument.	
Arguments	uint16_t * ad_buf	Start address of the storage area for A/D conversion results
Return values	None	

2.4 Sample Program Processing

2.4.1 Main Processing

Figure 3 shows the flowchart for the main processing routine.

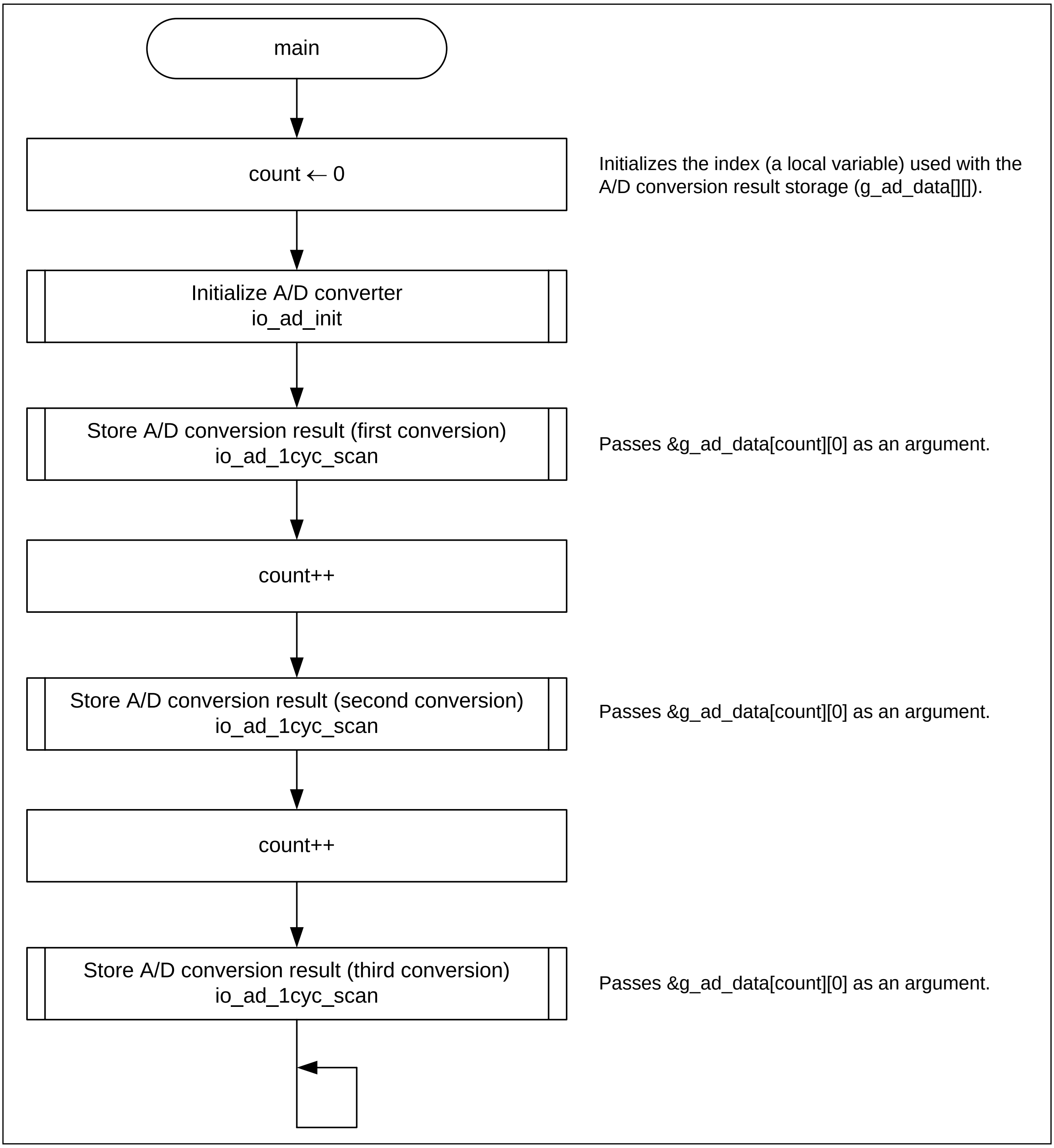


Figure 3 Main Processing

2.4.2 A/D Converter Initialization

Figure 4 shows the flowchart for A/D converter initialization.

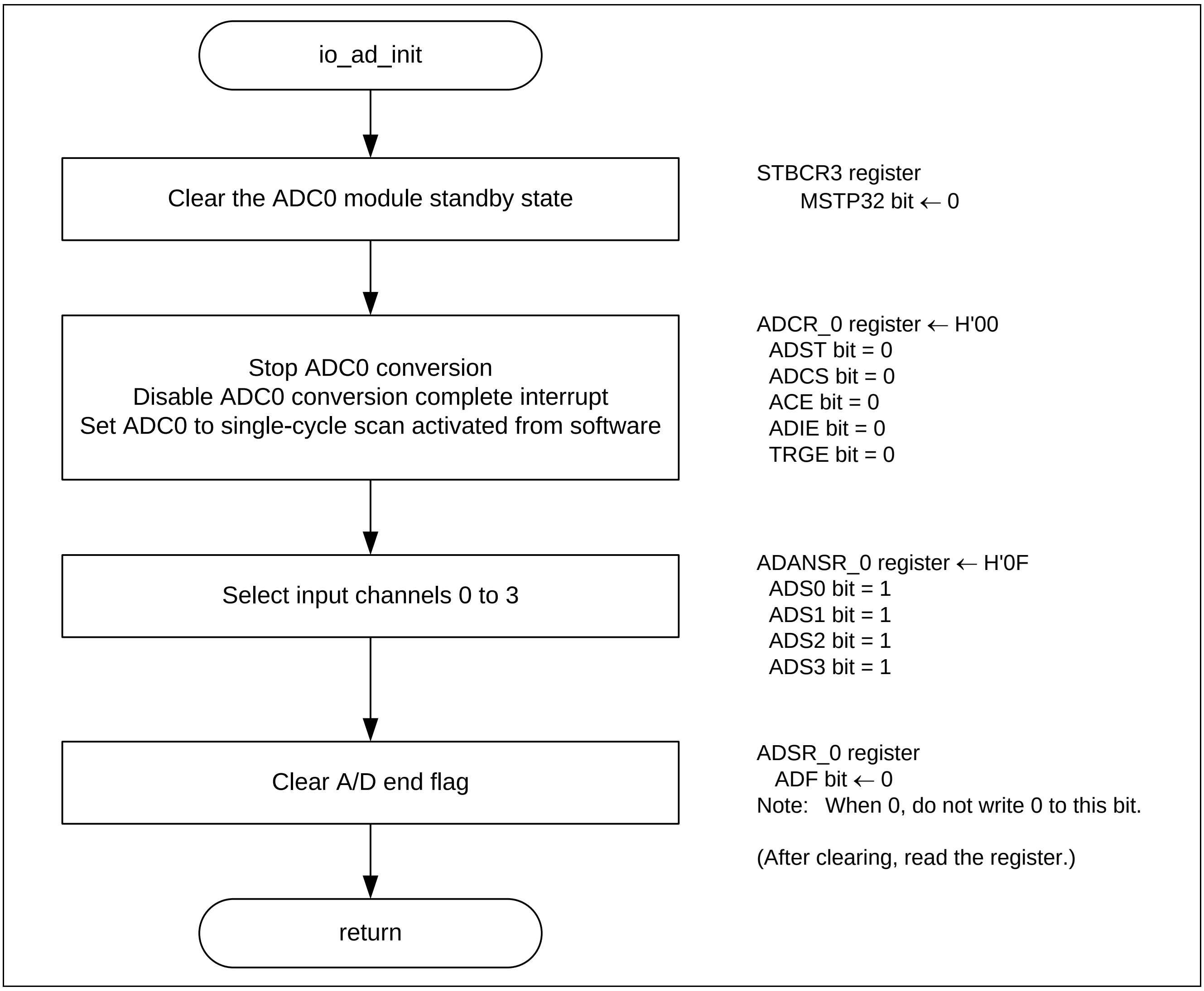


Figure 4 A/D Converter Initialization

2.4.3 A/D Conversion Processing

Figure 5 shows the flowchart for A/D conversion processing.

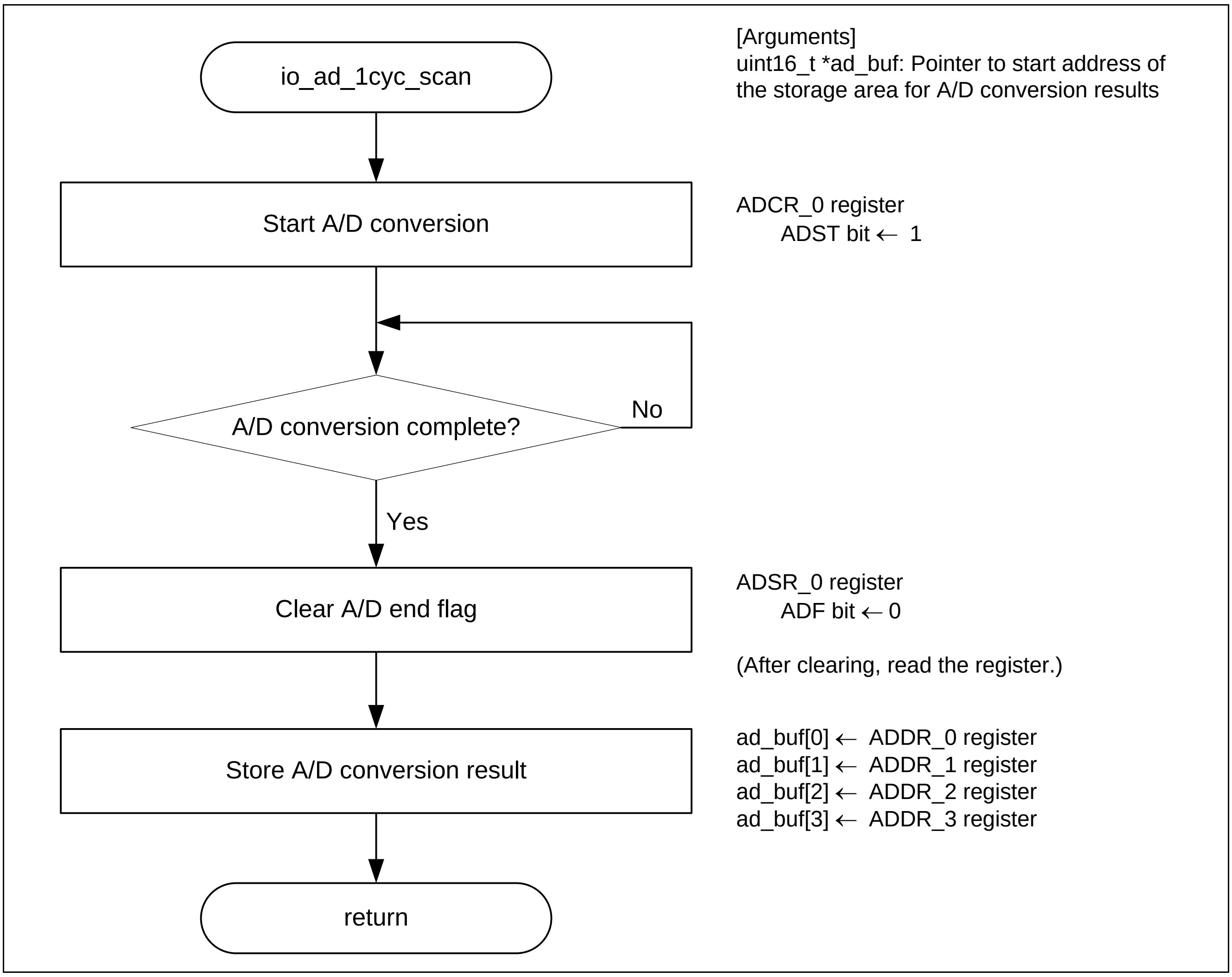


Figure 5 A/D Conversion Processing

2.5 Sample Program Register Settings

Table 7 lists the sample program register settings.

Table 7 Sample Program Register Settings

Register	Address	Setting Value	Function
A/D control register 0 (ADCR_0)	H'FFFF E800	H'00	At initialization ADST = 0: A/D converter stopped ADCS = 0: Single-cycle scan mode ACE = 0: ADDR automatic clear disabled ADIE = 0: A/D conversion complete interrupt disabled TRGE = 0: A/D conversion start by external trigger or MTU2/MTU2S disabled
		H'80	At A/D conversion start ADST = 1: Start A/D conversion
A/D analog channel selection register 0 (ADANSR_0)	H'FFFF E820	H'0F	ADS0 = 1: AN0 selected ADS1 = 1: AN1 selected ADS2 = 1: AN2 selected ADS3 = 1: AN3 selected

3. Reference Documents

- Software Manual
  SH-2A, SH2A-FPU User's Manual: Software, Rev.4.00 (R01US0031EJ)
  (The latest version can be downloaded from the Renesas Electronics Web site.)

- SH7239 Group, SH7237 Group User's Manual: Hardware, Rev.1.00 (R01UH0086EJ)
  (The latest version can be downloaded from the Renesas Electronics Web site.)

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Revision Record

Rev.	Date	Description	
		Page	Summary
1.00	Jun.15.12	—	First edition issued

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins
   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.
   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.
2. Processing at Power-on
   The state of the product is undefined at the moment when power is supplied.
   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.
3. Prohibition of Access to Reserved Addresses
   Access to reserved addresses is prohibited.
   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.
4. Clock Signals
   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.
   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.
5. Differences between Products
   Before changing from one product to another, i.e. to one with a different type number, confirm that the change will not lead to problems.
   — The characteristics of MPU/MCU in the same group but having different type numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different type numbers, implement a system-evaluation test for each of the products.

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