SH7216/SH7239 Group

Example of Setting the CPG to Change the Operating Frequency

R01AN1182EJ0100
Rev.1.00
Jul. 12, 2012

Abstract

This document describes an example of setting the clock pulse generator (CPG) to change the operating frequency for the SH7216/SH7239.

Products

SH7216/SH7239

When using this application note with other Renesas MCUs, careful evaluation is recommended after making modifications to comply with the alternate MCU.

Contents

1. Specifications

The internal clock (Iϕ) frequency in the frequency control register (FRQCR) of the clock pulse generator (CPG) can be changed by pressing and holding down the interrupt switch. In the sample code, the change of Iϕ can be visibly indicated by the LED blinking.

This application note describes how to change the Iϕ, but the functions used in the sample code are also applicable to change the bus clock (Bϕ) and the peripheral clock (Pϕ).

Table 1.1 lists the Peripheral Functions and Their Applications, and Figure 1.1 shows the System Diagram.

Table 1.1 Peripheral Functions and Their Applications

Peripheral Function	Application
Clock pulse generator (CPG)	Changes the clock operating frequency
Interrupt controller (INTC)	Input the IRQ interrupt when the switch (SW) is pressed down
I/O port	Uses the port to output to the LED

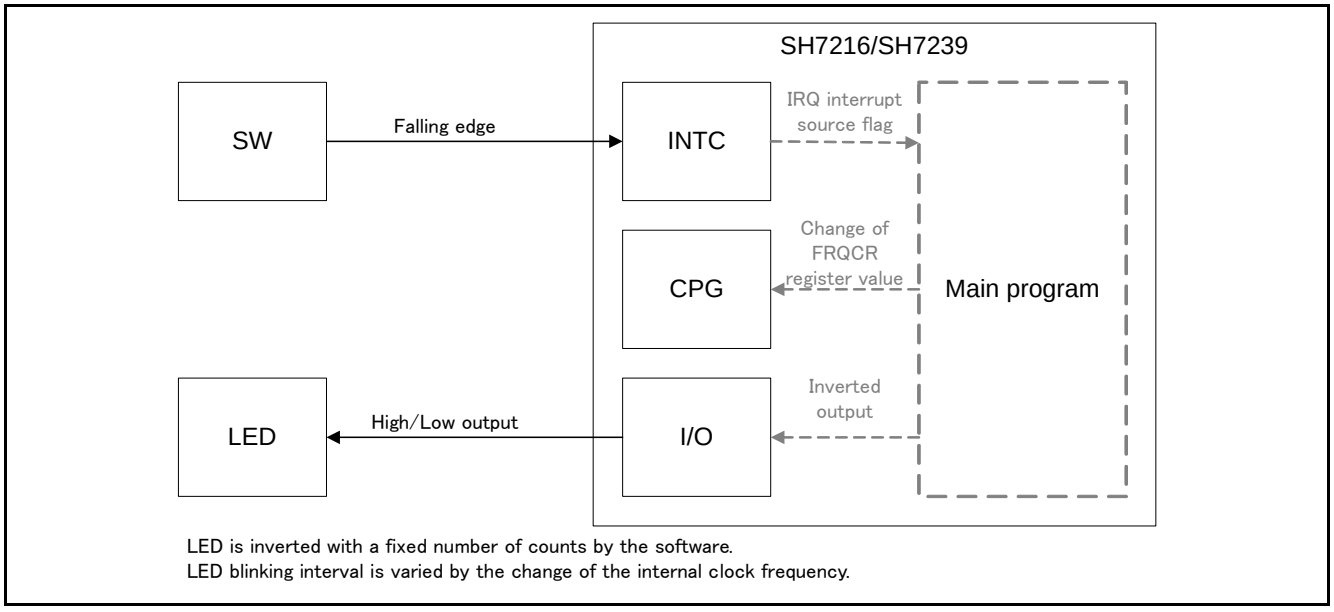

Figure 1.1 System Diagram

2. Operation Confirmation Conditions

The sample code accompanying this application note has been run and confirmed under the conditions below.

Table 2.1 SH7216 Operation Confirmation Conditions

Item	Contents
MCU used	SH7216
Operating frequency	Internal clock (Iϕ): 200MHz Bus clock (Bϕ): 50MHz Peripheral clock (Pϕ): 50MHz
Operating voltage	3.3V (Vcc)
Integrated development environment	Renesas Electronics High-performance Embedded Workshop Ver.4.07.00
C compiler	Renesas Electronics SuperH RISC engine Family C/C++ compiler package Ver.9.01 Release 00
	Compiler Option cpu=sh2afpu -fpu=single -include="$(WORKSPDIR)\inc" -object="$(CONFIGDIR)\$(FILELEAF).obj" -debug -gbr=auto -fpscr=safe -chgincpath -errorpath -global_volatile=0 -opt_range=all -infinite_loop=0 -del_vacant_loop=0 -struct_alloc=1 -nologo
Operating mode	User program mode
Sample code version	1.00
Board used	R0K572167C000BR

Table 2.2 SH7239 Operation Confirmation Conditions

Item	Contents
MCU used	SH7239 (R5F72395ADFP)
Operating frequency	Internal clock (Iϕ): 160MHz Bus clock (Bϕ): 40MHz Peripheral clock (Pϕ): 40MHz
Operating voltage	3.3V (Vcc)
Integrated development environment	Renesas Electronics High-performance Embedded Workshop Ver.4.07.00
C compiler	Renesas Electronics SuperH RISC engine Family C/C++ compiler package Ver.9.03 Release 02
	Compiler Option -cpu=sh2afpu -fpu=single -include="$(WORKSPDIR)\inc" -object="$(CONFIGDIR)\$(FILELEAF).obj" -debug -gbr=auto -chgincpath -errorpath -global_volatile=0 -opt_range=all -infinite_loop=0 -del_vacant_loop=0 -struct_alloc=1 -nologo
Operating mode	Single chip mode
Sample code version	1.00
Board used	R0K572390C000BR

3. Reference Application Notes

For additional information associated with this document, refer to the following application notes.

- SH7216 Group Example of Initialization (REJ06B1073)
- SH7239 Group Example of Initialization (R01AN0297EJ)
- SuperH RISC engine C/C ++ compiler package Application note: [Introduction guide] Start-up guide for SH-1, SH-2 and SH-2A (REJ06J0015)

4. Peripheral Functions

Refer to the following documents to change the operation frequency of the clock pulse generator (CPG).

When using the SH7216 Group, the basic information is provided in "SH7214 Group and SH7216 Group User's Manual: Hardware".

When using the SH7239 Group, the basic information is provided in "SH7239 Group and SH7239 Group User's Manual: Hardware".

4.1 Notes for Changing Clock Pulse Generator (CPG) Frequency

The frequency of the internal clock, the bus clock and the peripheral clock can be changed by altering division ratio of the divider in the CPG. When altering the division ratios of the internal clock, the bus clock and the peripheral clock, set IFC2 to 0 bit, STC2 to 0 bit, and PFC2 to 0 bit of the frequency control register (FRQCR) respectively.

For the SH7216 group, the division ratios of the MTU2S clock and the AD clock can be altered by setting MSDIVS1 to 0 bit of the MTU2S clock frequency control register (MCLKCR) and ASDIVS1 to 0 bit of the AD clock frequency control register (ACLKCR).

For the SH7239 group, the division ratios of the MTU clock and the AD clock can be altered by setting MSDIVS1 to 0 bit of the MTU clock frequency control register (MCLKCR) and ASDIVS1 to 0 bit of the AD clock frequency control register (ACLKCR).

Notes for setting the frequency control register (FRQCR) are described below.

- Use the program on the on-chip RAM to change the FRQCR:
  - Only word access is applicable for the FRQCR.
  - Execute the NOP instruction for 32Pϕ clock division after affirming the FRQCR setting value.

- The procedure below must be followed to perform the setting:

1) Stop modules other than the CPU, the on-chip ROM and the on-chip RAM.
2) Make sure to initialize the WDT when using the WDT.
3) Set the bit of IFC2 to IFC0, STC2 to STC0, PFC2 to PFC0, MSDIVS1, MSDIVS0, ASDIVS1 and ASDIVS0 to the desired values.
   - The values must be set as follows:
     Internal clock (Iϕ) ≥ Bus clock (Bϕ) ≥ Peripheral clock (Pϕ)
   - Do not over the maximum operating frequency.
     - The maximum operating frequency for the SH7216:
       Iϕ: 200MHz, Bϕ: 50MHz, Pϕ: 50MHz
     - The maximum operating frequency for the SH7239:
       Iϕ: 160MHz, Bϕ: 40MHz, Pϕ: 40MHz
   - Set as follows when using the MTU2S clock for the SH7216:
     100MHz ≥ MTU2S clock (Mϕ) ≥ Peripheral clock (Pϕ)
   - Set as follows when using the MTU clock for the SH7239:
     80MHz ≥ MTU clock (Mϕ) ≥ Peripheral clock (Pϕ)
4) When additionally change the value of Bϕ after setting Bϕ and Pϕ more than 1/4 times, do not change the values of Iϕ, Bϕ and Pϕ at the same time. Follow the procedure below.
   4.1 One-eighth the value of Pϕ. (PFC of the FRQCR register is B'101)
   4.2 Set the value of Bϕ to the desired value after changing the value of Pϕ.
   4.3 Set the value of each Iϕ and Pϕ to the desired value.

5. Hardware

5.1 Pins Used

Table 5.1 lists the Pins Used and Their Functions for SH7216. Table 5.2 lists the Pins Used and Their Functions for SH7239.

Table 5.1 Pins Used and Their Functions for SH7216

Pin Name	Input/Output	Function
PD16/IRQ0	**Input**	Used as a trigger for the frequency change (R0K572167C001BR:SW1) Generates the IRQ0 interrupt on the falling edge
PE9	**Output**	Inverts high/low output with a fixed clock period as the port output The interval of the period is changed by altering the internal clock frequency (R0K572167C001BR: Confirm by the LED0 blinking)

Table 5.2 Pins Used and Their Functions for SH7239

Pin Name	Input/Output	Function
PA9/IRQ3	**Input**	Used as a trigger for the frequency change (R0K572390C000BR:SW2) Generates the IRQ3 interrupt on the falling edge
PE12	**Output**	Inverts high/low output with a fixed clock period as the port output The interval of the period is changed by altering the internal clock frequency (R0K572390C000BR: Confirm by the LED0 blinking)

6. Software

6.1 Operation Overview

The IRQ generated on the falling edge of the input pins triggers a change of the operating frequency. It enables the LED to blink at intervals of fixed count to visibly confirm the change of the frequency.

- Initializes the CPG by initializing the hardware in the process of power-on reset after copying the first FRQCR register setting program from the Internal ROM to the on-chip RAM.
- The FRQCR setting function is copied to the on-chip RAM when initializing the section performed by the function _INITSCT. After that, the FRQCR setting function is executed on the on-chip RAM.
- In the main function, enters the infinite loop after executing the initial setting.
- Sets the flag when executing the IRQ interrupt to be generated on the falling edge of the input pins.
- In the infinite loop, the IRQ interrupt flag is monitored, and the inversion for the port output is repeatedly performed.
  - When the IRQ interrupt flag is set, change the value of the clock pulse generator (CPG). The division ratio of the internal clock (Iϕ) frequency is modified according to the following steps.
    ×1 -> ×1/2 -> ×1/4 -> ×1 -> ×1/2 -> ×1/4 -> ×1 ->....
  - After inverting the port output value, waits in the software to keep the inverted value. The waiting time is the time to loop the empty for statement only for the times specified by the constant LED_WAIT_COUNT. When the IRQ interrupt flag is not set, the inversion of output and the waiting will be repeatedly performed.

Figure 6.1 shows the Procedure for Operation Overview.

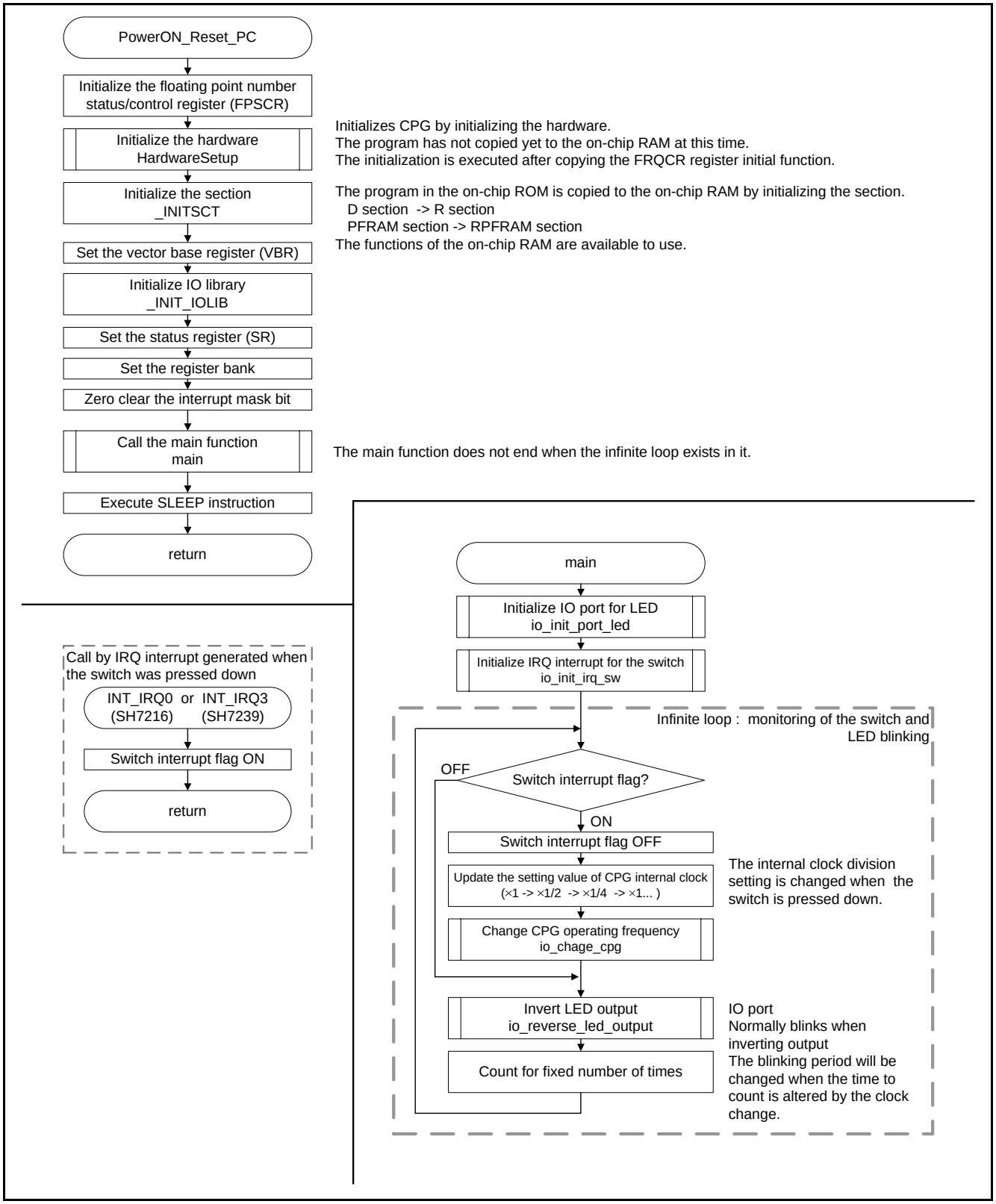

Figure 6.1 Procedure for Operation Overview

6.2 Constants

Table 6.1 lists the Constants Used in the Sample Code.

Table 6.1 Constants Used in the Sample Code

Constant	Setting Value	Contents
LED_WAIT_COUNT	H'400000	Counts of the interval for inverting output of the LED port
CPG_FRQCR_CLK_DIV1	H'0000	Sets the clock frequency division ratio ×1/1
CPG_FRQCR_CLK_DIV2	H'0001	Sets the clock frequency division ratio ×1/2
CPG_FRQCR_CLK_DIV4	H'0003	Sets the clock frequency division ratio ×1/4
CPG_FRQCR_CLK_DIV8	H'0005	Sets the clock frequency division ratio ×1/8
CPG_FRQCR_BIT_IFC	H'0070	IFC (Iϕ division setting) bit location (6 to 4)
CPG_FRQCR_BIT_STC	H'0700	STC (Bϕ division setting) bit location (10 to 8)
CPG_FRQCR_BIT_PFC	H'0007	PFC (Pϕ division setting) bit location (2 to 0)
CPG_FRQCR_SHIFT_IFC	4	Number of shifts for IFC bit location
CPG_FRQCR_SHIFT_STC	8	Number of shifts for STC bit location
CPG_FRQCR_SHIFT_PFC	0	Number of shifts for PFC bit location

6.3 Variable

Table 6.2 lists the Global Variable.

Table 6.2 Global Variable

Type	Variable Name	Contents	Function Used
int32_t	g_flag_sw	Switch pressed flag 1 : switch pressed 0 : switch not pressed	main INT_IRQ0 (limited to SH7216) INT_IRQ3 (limited to SH7239)

6.4 Functions

Table 6.3lists the Functions.

Table 6.3 Functions

Function Name	Outline
main	Main processing
io_init_port_led	Initialization of the IO port for the LED
io_init_irq_sw	Initialization of the IRQ interrupt for the switch
INT_IRQ0	IRQ0 Interrupt processing (SH7216)
INT_IRQ3	IRQ3 Interrupt processing (SH7239)
io_reverse_led_output	Inverting of the LED output
io_change_cpg	Changing of the CPG operating frequency
io_change_cpg_frqcr_reg	Setting for the FRQCR register

6.5 Function Specifications

The following tables list the sample code function specifications.

main	
Outline	Main processing
Header	
Declaration	void main(void)
Description	Enters the infinite loop after initializing IO port for the LED and IRQ interrupt for the switch. In the infinite loop, monitoring is executed to ensure the switch is pressed down, and inversion of the IO port output to blink the LED is performed consistently. Changes the internal clock frequency of the CPG when the switch is pushed. Keeps the same output value by counting a given number after inverting the IO port output. The LED blinks at fixed intervals while the switch is not pressed. The number of counts does not change when the switch is pushed, but the LED blinking period will be altered when the operating frequency is changed.
Argument	None
Return value	None

io_init_port_led	
Outline	Initialization of the IO port for the LED
Header	
Declaration	void io_init_port_led(void)
Description	Initializes the IO port used to blink the LED. Installs the pin function which is connected to the LED to the IO port at PFC. Sets Low output as the initial value of the IO port output.
Argument	None
Return value	None

io_init_irq_sw	
Outline	Initialization of the IRQ interrupt for the switch
Header	
Declaration	void io_init_irq_sw(void)
Description	Initializes the IRQ so that interrupts can be generated by pressing down the switch. Installs the pin function which is connected to the switch to the IRQ at PFC. Sets the IRQ sense select to the falling edge detector at INTC, and specifies the interrupt priority level to 1.
Argument	None
Return value	None

INT_IRQ0	
Outline	IRQ0 Interrupt processing (SH7216)
Header	
Declaration	void INT_IRQ0(void)
Description	Executes the IRQ0 interrupt which is generated when the switch (SW1) is pushed. Sets the flag indicating the switch is on.
Argument	None
Return value	None

INT_IRQ3	
Outline	IRQ3 interrupt processing (SH7239)
Header	
Declaration	void INT_IRQ3(void)
Description	Executes the IRQ3 interrupt which is generated when the switch (SW2) is pushed. Sets the flag indicating the switch is on.
Argument	None
Return value	None

io_reverse_led_output	
Outline	Inverting of the LED output
Header	
Declaration	void io_reverse_led_output(void)
Description	Inverts the IO port output value to blink the LED.
Argument	None
Return value	None

io_change_cpg	
Outline	Changing the CPG operating frequency
Header	
Declaration	int32_t io_change_cpg(uint16_t iclk_div, uint16_t bclk_div, uint16_t pclk_div)
Description	Executes setting for the FRQCR register according to the specified argument. Checks the argument and the conditions. When inapplicable value is specified, returns the negative value without setting. When applicable setting value is specified, call the function io_change_cpg_frqcr_req to set the value to the FRQCR. Select the values from the following constants to set them to the three arguments listed below. - CPG_FRQCR_CLK_DIV1: Set the clock frequency division ratio ×1/1 - CPG_FRQCR_CLK_DIV2: Set the clock frequency division ratio ×1/2 - CPG_FRQCR_CLK_DIV4: Set the clock frequency division ratio ×1/4 - CPG_FRQCR_CLK_DIV8: Set the clock frequency division ratio ×1/8
Argument	uint16_t iclk_div : Internal clock frequency (Iϕ) division setting uint16_t bclk_div : Bus clock frequency (Bϕ) division setting uint16_t pclk_div : Peripheral clock frequency (Pϕ) division setting
Return value	0 : Normal end -1 : Argument error Return -1 to end without changing the CPG operating frequency when the illegal value is specified to the argument. -2 : Error condition When the argument does not satisfy the condition below, return -2 to end without changing the CPG operating frequency. Internal clock≥Bus clock≥Peripheral clock

io_change_cpg_frqcr_reg	
Outline	Setting for the FRQCR register
Header	
Declaration	void io_change_cpg_frqcr_reg(uint16_t frqcr_reg)
Description	Sets the argument value to the FRQCR register. This function is the program to be allocated in the RPFRAM section on the on-chip RAM. - Sets the FRQCR register by the word access - Reads and Executes NOP instruction for the 32Pϕ clock division after setting. (512 times of NOP instructions are executed in the sample code)
Argument	uint16_t frqcr_reg : The value to be set to the FRQCR register
Return value	None

6.6 Flowcharts

6.6.1 Main Processing

Figure 6.2 shows the procedure of the Main Processing.

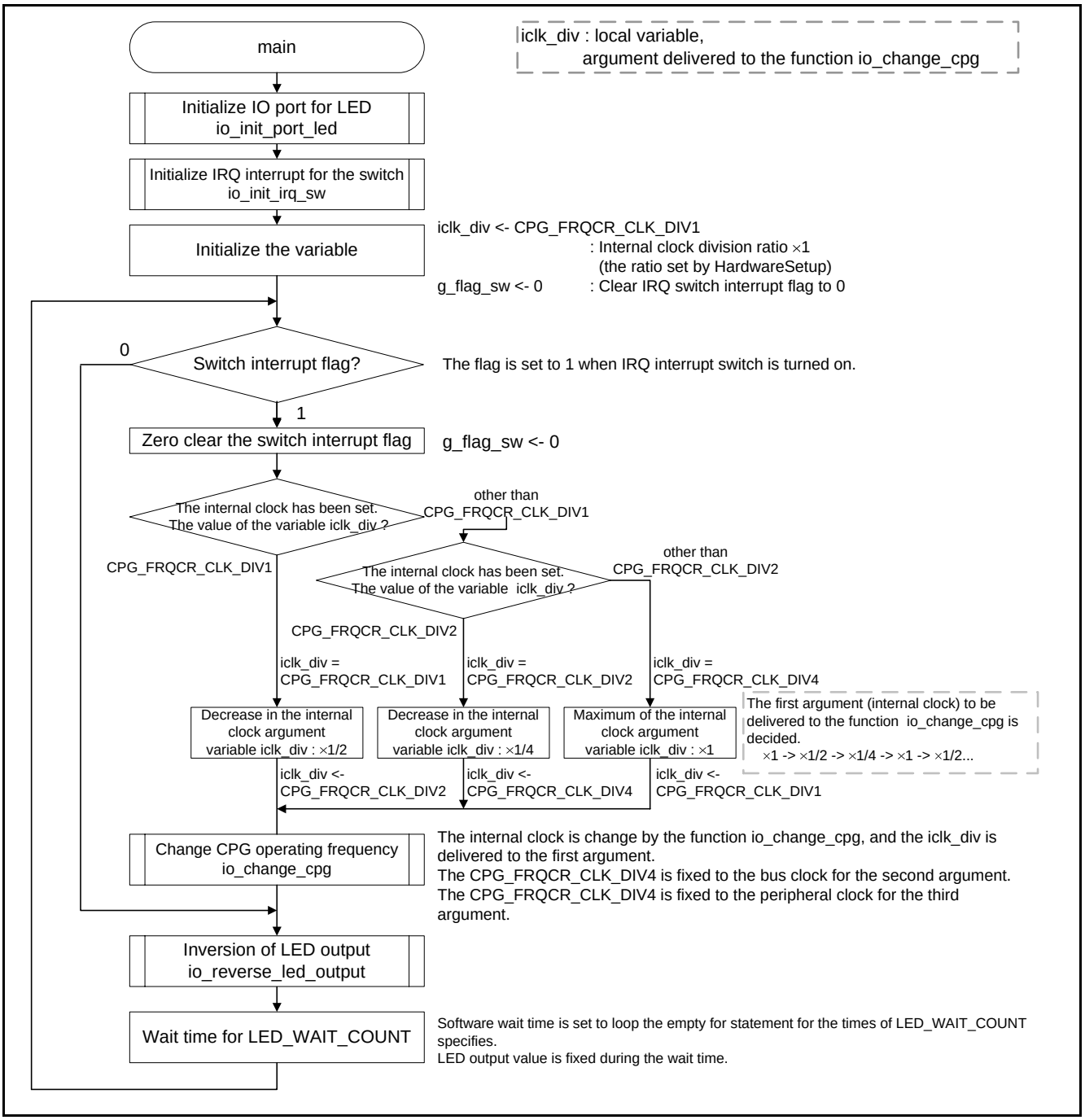

Figure 6.2 Main Processing

6.6.2 Initialization of IO Port for LED

Figure 6.3 shows the procedure of the Initialization of IO Port for LED.

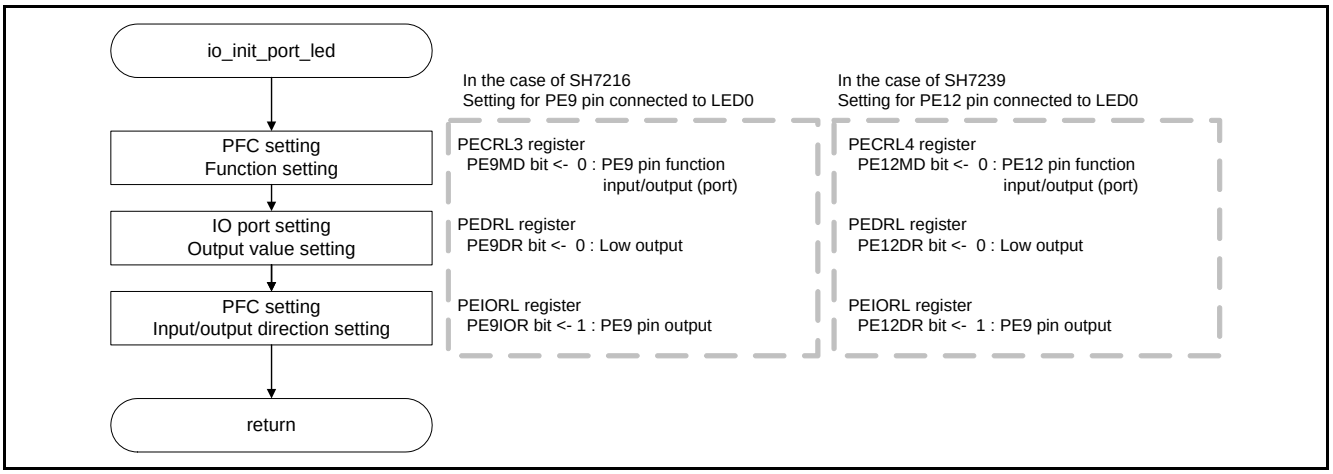

Figure 6.3 Initialization of IO Port for LED

6.6.3 Initialization of IRQ Interrupt for the Switch

Figure 6.4 show the procedure of the Initialization of IRQ Interrupt for the Switch.

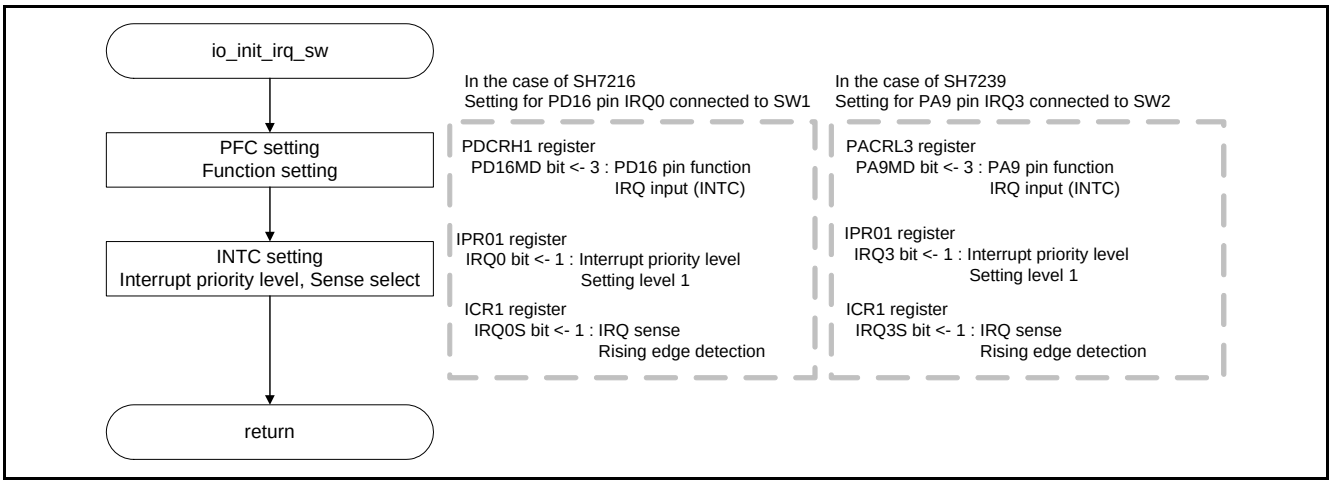

Figure 6.4 Initialization of IRQ Interrupt for the Switch

6.6.4 IRQ0 Interrupt Processing (SH7216)

Figure 6.5 shows the procedure of the IRQ0 Interrupt Processing (SH7216).

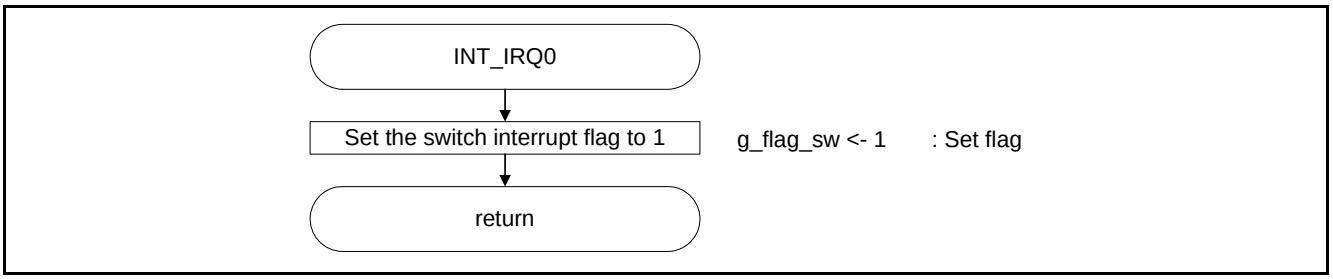

Figure 6.5 IRQ0 Interrupt Processing (SH7216)

6.6.5 IRQ3 Interrupt Processing (SH7239)

Figure 6.6 shows the procedure of the IRQ3 Interrupt Processing (SH7239).

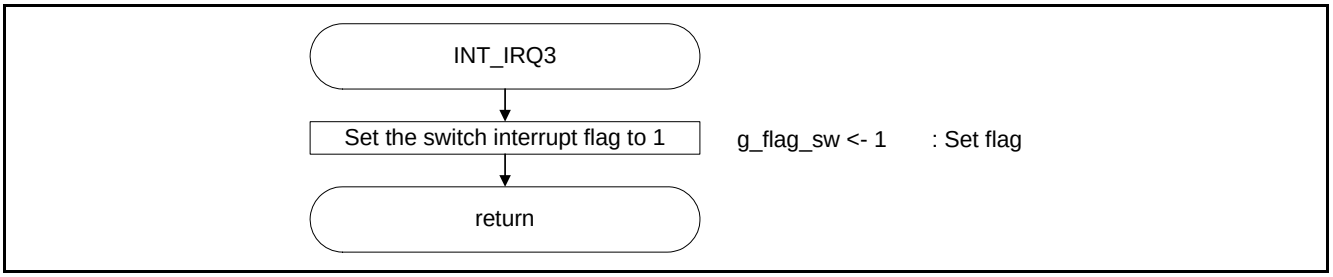

Figure 6.6 IRQ3 Interrupt Processing (SH7239)

6.6.6 Inversion of LED Output

Figure 6.7 shows the procedure of the Inversion of LED Output.

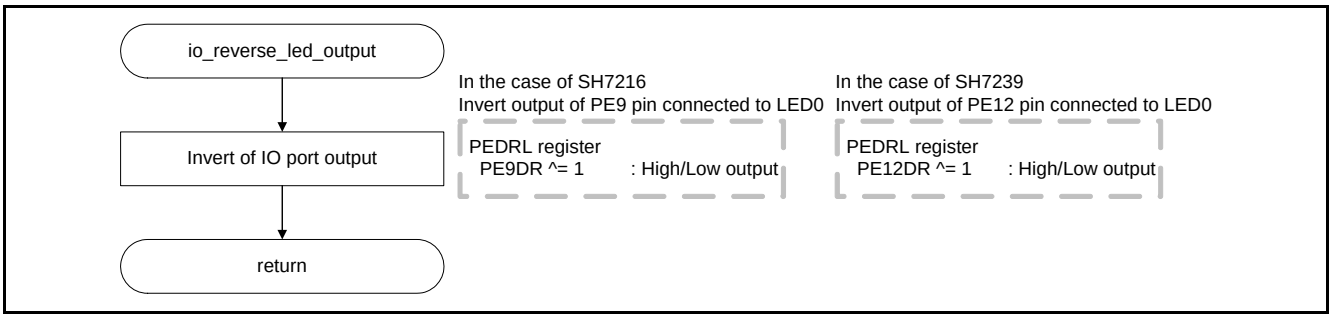

Figure 6.7 Inversion of LED Output

6.6.7 Changing CPG Frequency

Figure 6.8 shows the procedure of the Changing of CPG Frequency.

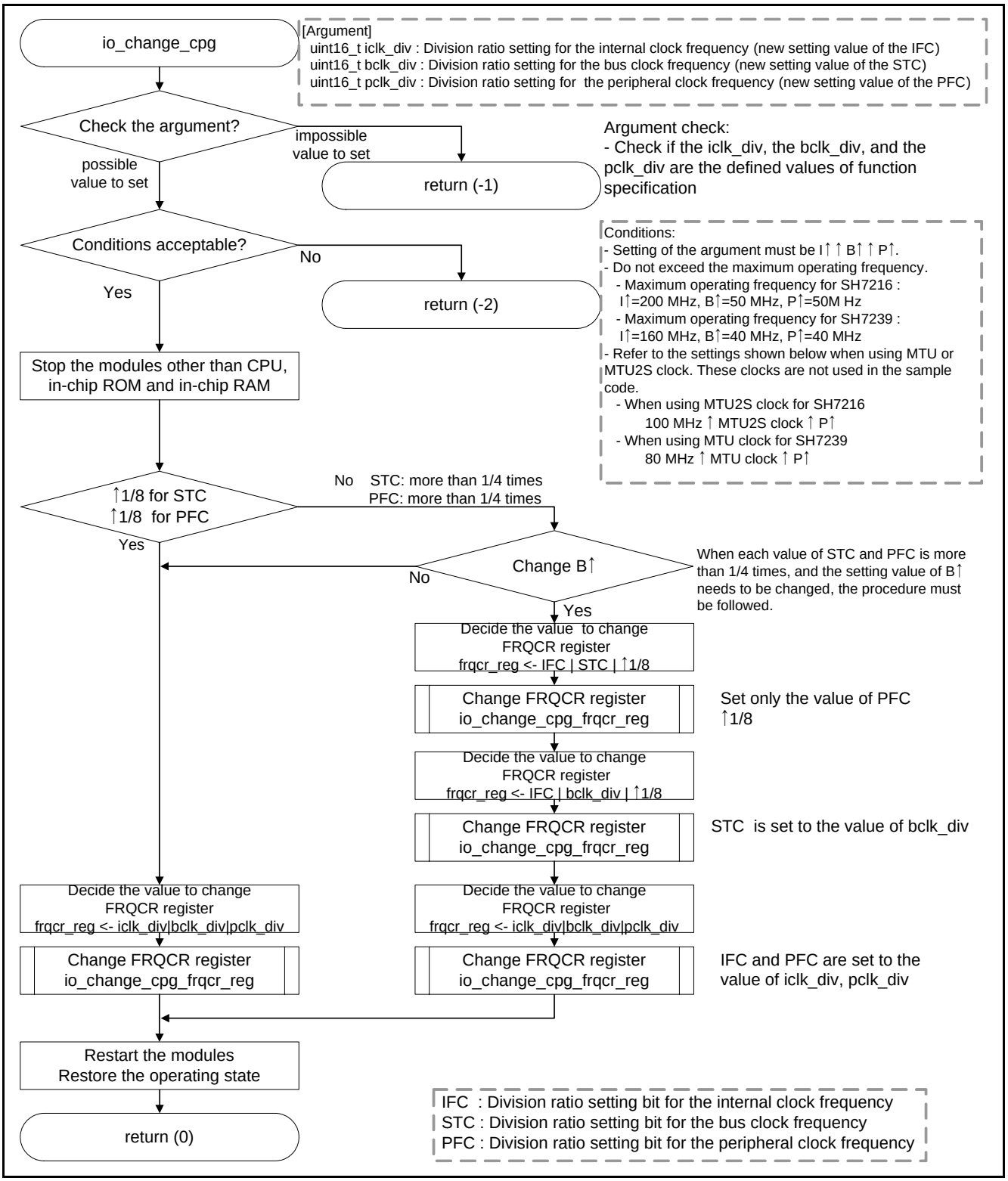

Figure 6.8 Changing of CPG Frequency

6.6.8 Setting for FRQCR Register

Figure 6.9 show the procedure of the Setting for FRQCR register.

The function io_change_cpg_frqcr_reg in Figure 6.9 is allocated to the section on the on-chip RAM. Regarding to the ROM support or memory initialization, refer to "SuperH RISC engine C/C ++ compiler package Application note: [Introduction guide] Start-up guide for SH-1, SH-2 and SH-2A".

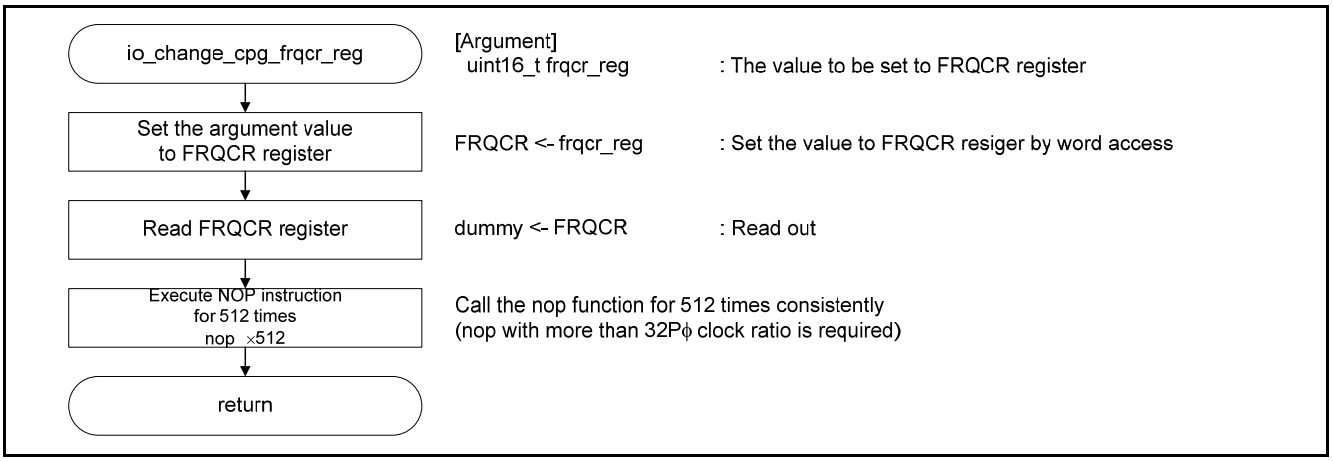

Figure 6.9 Setting for FRQCR register

7. Sample Code

Sample code can be downloaded from the Renesas Electronics website.

8. Reference Documents

User's Manual: Hardware
SH7214 Group, SH7216 Group User's Manual: Hardware Rev.3.00 (R01UH0230EJ)
SH7239 Group, SH7237 Group User's Manual: Hardware Rev.1.00 (R01UH0086EJ)
The latest version can be downloaded from the Renesas Electronics website.

Technical Update/Technical News
SH7239 Group, SH7237 Group User's Manual: Hardware Correction of Errors (TN-SH7-A791A/E)
The latest information can be downloaded from the Renesas Electronics website.

User's Manual: Development Tools
SuperH C/C++ Compiler Package V.9.04 User's Manual Rev.1.01 (R20UT0704EJ)
The latest version can be downloaded from the Renesas Electronics website.

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REVISION HISTORY	SH7216/SH7239 Group Application Note Example of Setting of the CPG to Change the Operation Frequency

Rev.	Date	Description	
		Page	Summary
1.00	Jul. 12, 2012	—	First edition issued

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins
   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.
   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.
2. Processing at Power-on
   The state of the product is undefined at the moment when power is supplied.
   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.
3. Prohibition of Access to Reserved Addresses
   Access to reserved addresses is prohibited.
   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.
4. Clock Signals
   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.
   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.
5. Differences between Products
   Before changing from one product to another, i.e. to one with a different type number, confirm that the change will not lead to problems.
   — The characteristics of MPU/MCU in the same group but having different type numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different type numbers, implement a system-evaluation test for each of the products.

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